altair™ 8K PROM Card

(88-PMC8)
Documentation

a subsidiary of **Pertec Computer Corporation**

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a subsidiary of **Pertec Computer Corporation**
2450 Alamo S.E. /Albuquerque, New Mexico 87106

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SECTION I
INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

The 88-PMC8 Documentation is divided into four major sections as follows:

I. Introduction--Section I contains a synopsis of the organization of the 88-PMC8 manual and a brief description of the board and its capabilities.

II. Theory of Operation--Section II provides the information needed to understand the operation of the board at a technical level. Included are EPROM programming and erasing procedures; descriptions of the board's circuitry and functions; and schematics and waveforms.

III. Troubleshooting--Section III contains simple troubleshooting procedures, presented in table form, which are designed to aid in locating and correcting most problems.

IV. Assembly--Section IV contains the detailed instructions (complete with silkscreen reproductions) needed to assemble the board.

1-2. PRODUCT DESCRIPTION

The 88-PMC8 board is a highly useful memory device. Unlike conventional "volatile" memory boards, programmed data is retained during power-down conditions. Once programmed, data within the EPROM will not change unless it is "erased" by exposure to ultraviolet light under controlled conditions. (Erasure procedures are fully explained in Paragraph 2-5.)

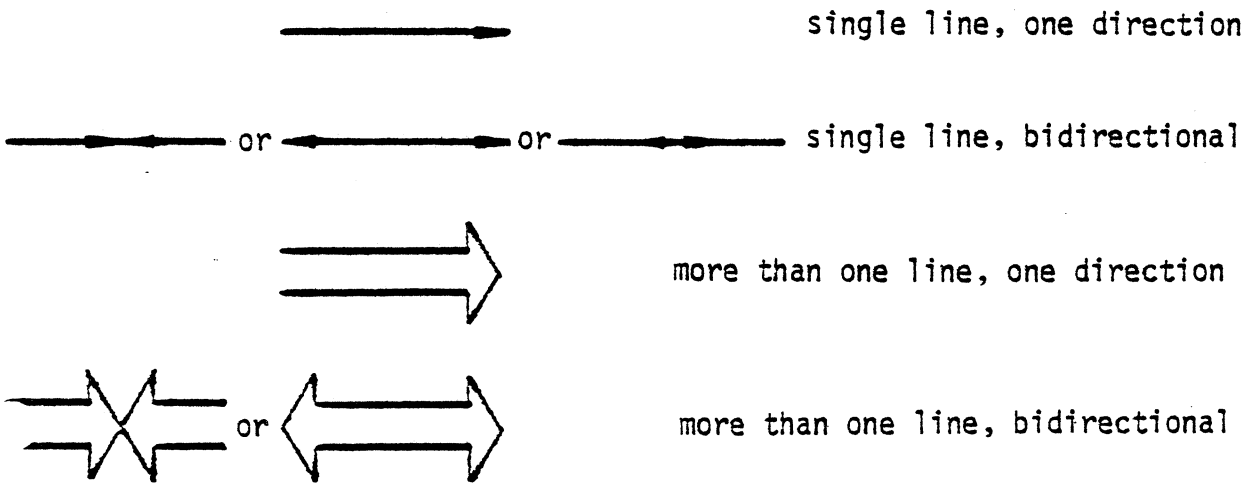
The 88-PMC8 is functionally similar to the other Altair 8800 static memory boards. Contained on the board are circuitry for Address (Board) Select, EPROM Select, 12-Volt Switch, Read and Write, and provisions for eight 1024 by 8 bit Erasable Programmable Read Only Memory chips (EPROMs). Data is stored in memory in groups of 8 bits referred to as bytes or words of data. The board is programmed by means of a Store Data instruction or a Move Data to Memory instruction. A Load Data or Move Data From Memory instruction is used to read the board.

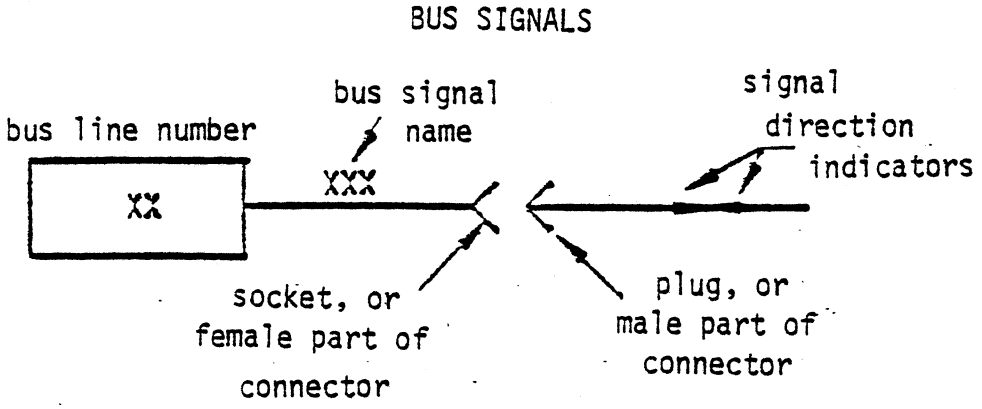
SECTION II
THEORY OF OPERATION

2-1. SCHEMATIC REFERENCING

A detailed schematic of the 88-PMC8 board (Figure 2-3) is provided to aid in determining signal direction. Table 2-A shows how signal direction is indicated on signal lines and how to interpret the signal bus designations.

Table 2-A. Signal Direction and Bus Signals





2-2. LOGIC CIRCUITS

The logic circuits shown in the 88-PMC8 schematics are presented in Table 2-B. This table contains the functional name, symbolic representation and a brief description of each logic circuit.

The active state of the inputs and outputs of the circuit is graphically displayed by the presence or absence of small circles. A small circle at an input to a logic circuit indicates the input is an active LOW; i.e. a LOW will enable the input. A small circle at the output of a logic circuit indicates the output is an active LOW; i.e. the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

Table 2-C illustrates the internal pin configurations of the integrated circuits.

Table 2-B

Logic Circuits

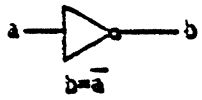
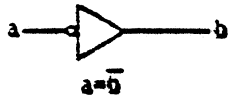
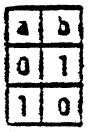
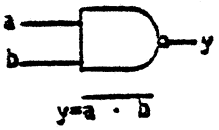
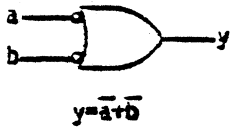
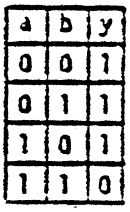
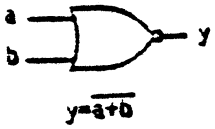
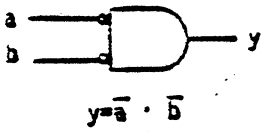
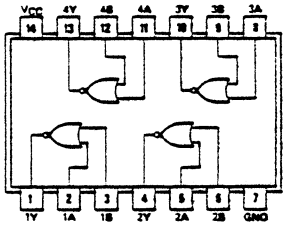
Name	Normal	Equivalent	Description
Inverter or Buffer			An inverter is a gate whose output is the inverse of its input. 
NAND gate			The NAND gate gives a LOW output when all of its inputs are HIGH. As the truth table will show, it is the equivalent of an OR gate with all of its inputs inverted. 
NOR gate			The NOR gate gives a LOW output when any of its inputs are HIGH. It is equivalent to an AND gate with all of its inputs inverted.

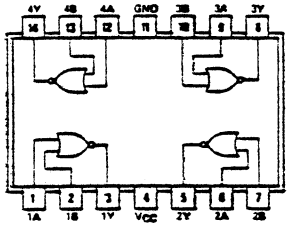
Table 2-C. Internal Pin Configurations

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$



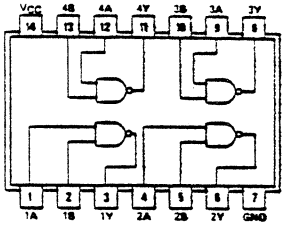
SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



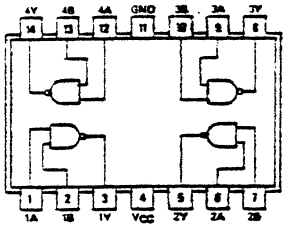
SN5402/SN7402(W)
SN54L02/SN74L02(T)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$



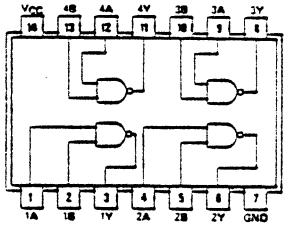
SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)



SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

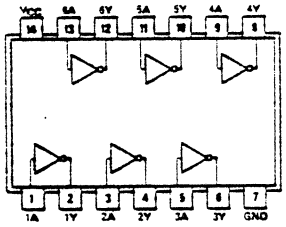
positive logic:
$Y = \overline{AB}$



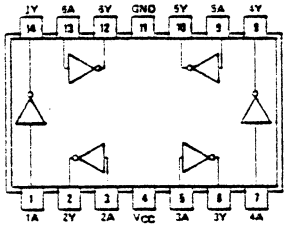
SN5403/SN7403(J, N)
SN54L03/SN74L03(J, N)
SN54LS03/SN74LS03(J, N, W)
SN54S03/SN74S03(J, N, W)

HEX INVERTERS

positive logic:
$Y = \overline{A}$



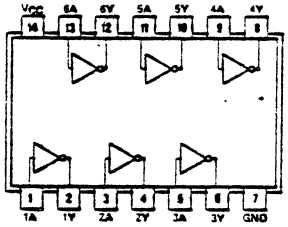
SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)



SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

IEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

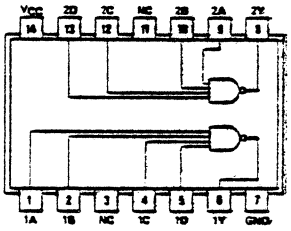
positive logic:
$Y = \overline{A}$



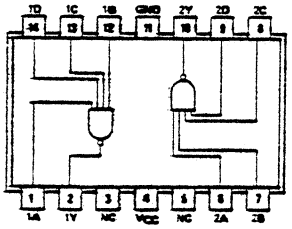
SN5406/SN7406(J, N, W)

DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$



SN5420/SN7420(J, N)
SN54H20/SN74H20(J, N)
SN54L20/SN74L20(J, N)
SN54LS20/SN74LS20(J, N, W)
SN54S20/SN74S20(J, N, W)



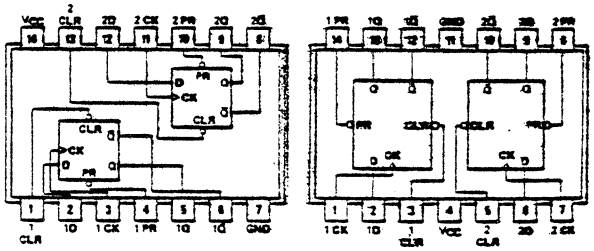
SN5420/SN7420(W)
SN54H20/SN74H20(W)
SN54L20/SN74L20(T)

NC—No internal connection

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$



SN5474/SN7474(J, N)
SN54H74/SN74H74(J, N)
SN54L74/SN74L74(J, N)
SN54LS74/SN74LS74(J, N, W)
SN54S74/SN74S74(J, N, W)

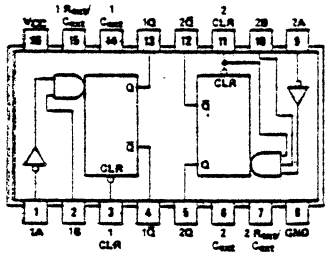
SN5474/SN7474(W)
SN54H74/SN74H74(W)
SN54L74/SN74L74(T)

H = high level (steady state), L = low level (steady state), X = irrelevant
⎍ = high-level pulse: data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
↑ = transition from low to high level, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎌
H	↓	H	⎍	⎌
↑	L	H	⎍	⎌



SN54123/SN74123(J, N, W)
SN54L123/SN74L123(J, N)

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎌ = one low-level pulse, X = irrelevant (any input, including transitions).
B. To use the internal timing resistor of '121, 'L121, '122, or 'L122, connect R_{int} to V_{CC}.
C. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
D. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
E. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

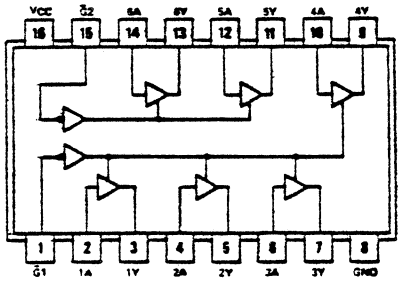
- True Data
- 4-Line and 2-Line Enable Inputs Can Be Organized for 4-Bit Bytes or Digit Control

'367
FUNCTION TABLE
(EACH DRIVER)

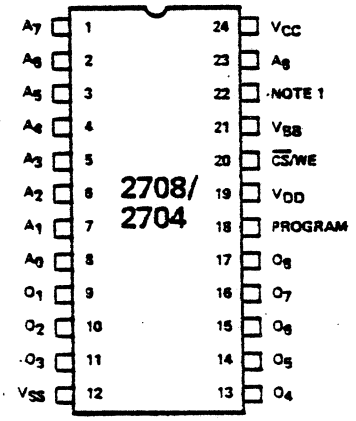
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

H = high level, L = low level,
X = irrelevant, Z = high-impedance

SN54367 . . . J OR W PACKAGE
SN74367 . . . J OR N PACKAGE
(TOP VIEW)



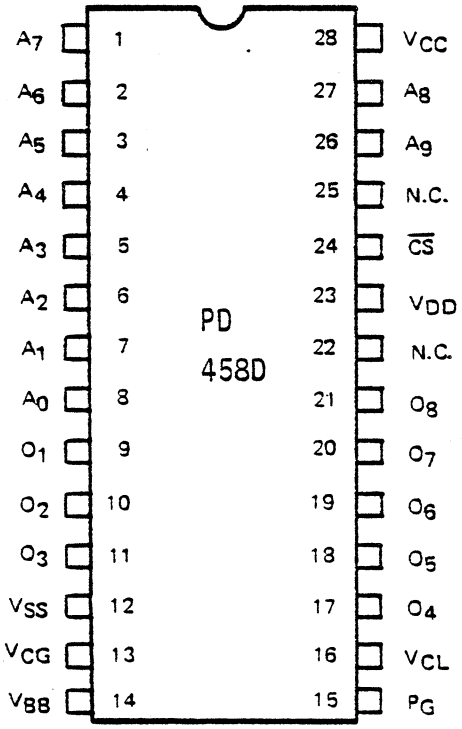
CONNECTION DIAGRAM



NOTE 1. 2704: PIN 22 = V_{SS}.
2708: PIN 22 = A_9.

PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT



N.C. – No correction

2-3. EPROM MEMORY GENERAL DESCRIPTION

With the insertion of each EPROM (2708 IC), 1024 (1K) bytes of memory are added to the board. However, if all 8 EPROM ICs are not installed, the full 8K address block in memory will be "used up" just as if the missing EPROMs were present.

After erasure, all bits in the EPROM appear HIGH and are forced LOW by writing a 0 into the selected bits. When reprogramming an EPROM, a LOW can overwrite a HIGH, but a HIGH cannot replace a LOW unless the entire EPROM is erased.

2-4. EPROM PROGRAMMING PROCEDURE

During a WRITE cycle, the erased EPROMs are installed in the card, the programming switch (S2) is set to the WRITE position, the transfer program is accessed, sense switches (if used) are set up, and the program is run. A power down of the board with S2 in the WRITE position will cause erroneous data to be deposited in the EPROMs. For this reason, S2 should be switched back to the NORMAL position after the run is complete.

> CAUTION
>
> Never remove or replace an EPROM in the board with power on. Turn off the machine or use a switchable extender card when removing or installing EPROMs.

The user may devise his own programming procedure, however, a 2708 EPROM chip (WRPROM) containing a programming routine (PRMCTR) is optionally available and may be obtained from the MITS Marketing Department. The PRMCTR program controls the programming and transfer functions for the Altair 88-PMC8 board. It is totally position independent; i.e. it can run from any PROM location without special modifications.

The PRMCTR controls the programmer functions of the card and meets the manufacturers' specifications for programming of PROMs. A terminal rather than the front panel switches is used for communication, making it suitable for a Turnkey system. The chip supports either a 2SIO board at channel 020 or an SIO board at Ø with the same sense switch settings as 4.1 Altair BASIC. PRMCTR has the ability to program up to a maximum of 31K bytes at one time. A 14 byte stack specified upon

initialization is required.

The WRPROM also allows block transfers of memory (from 1 to 32K bytes long): from PROM to RAM, from RAM to PROM, from RAM to RAM or from PROM to PROM in any increment. The chip also has an Automatic Transfer or Program Verify Mode to check the accuracy of a transfer.

2-5. EPROM ERASING PROCEDURE

Each 2708 EPROM can be erased by exposure to ultraviolet light at a wavelength of 2537 angstroms. The recommended integrated dosage (i.e. UV exposure x exposure time) is 10W - sec/cm^2. In order to insure that all bits are erased, this dosage includes a guard band of two to four times the initial period (the time needed to erase all bits). This guard band guarantees erasure of the device at extremes of temperature.

Table 2-D lists several suitable UV sources and their corresponding power ratings and recommended exposure times. Under-erasing may result in lost data. In order to insure proper data retention, follow the exposure times given in Table 2-D. The lamps should be placed approximately 1 inch away from the EPROMs to be erased. (Shortwave filters should not be installed in the lamps during this procedure.)

CAUTION
Ultraviolet light can be harmful to the eyes and skin; shield the lamps while they are in use.

Table 2-D. UV Erasure Sources

Lamp Model Number*	Power Rating	Recommended Time
S-68	12000 W/cm^2	60 minutes
S-52	12000 W/cm^2	60 minutes
UVS-54	5700 W/cm^2	120 minutes
R-52	13000 W/cm^2	60 minutes
UVS-11	5500 W/cm^2	120 minutes

*These models are manufactured by Ultra-Violet Products, Inc., 5114 Walnut Grove Ave., San Gabriel, California.

2-6. ADDRESS (BOARD) SELECT CIRCUITRY

In order to insure correct read and write operations, use switch S1 to select the proper address lines as shown in Table 2-E.

For a schematic representation of the Board Select operation, refer to Figure 2-3, sheet 2, zone A6. ICs N and M control address lines A13, A14 and A15. Either the buffered address line or the inverted address line is input to IC M where decoding is performed. Once the True condition (all inputs HIGH) occurs, output pin 8 (zone A5) goes LOW. This LOW signal is referred to throughout the text as Board Select.

Table 2-E. Address Selection

Board Address	Pole #2 (A13)	Pole #3 (A14)	Pole #4 (A15)
0	Down	Down	Down
8K	Up	Down	Down
16K	Down	Up	Down
24K	Up	Up	Down
32K	Down	Down	Up
40K	Up	Down	Up
48K	Down	Up	Up
56K	Up	Up	Up

Pole #1 is connected to (A12). For special applications it is possible to connect IC M pin 9 to S1, allowing the card to be used as a 4K PROM card. The board can be modified by cutting the land from IC M pin 9 to resistor R51, and connecting IC M pin 9 to S1 pin 15 or 16. When Pole #1 is down, the first 4 EPROMs are selected according to Table 2-D. When S1 is up, the second set of 4 EPROMs will be selected when the board is addressed and (A12) is True.

2-7. EPROM SELECT CIRCUITRY

Refer again to Figure 2-3, sheet 2. IC F is used in conjunction with ICs A through E to select a particular EPROM. IC F (zone A7) inputs inverted address lines $\overline{A10}$, $\overline{A11}$ and $\overline{A12}$ and, coincident with a valid LOW $\overline{\text{Board Select}}$ signal on pin 12, outputs a LOW select signal to one of the eight EPROM select circuits (see Table 2-F).

The following discussion is relative to the first addressable EPROM on the board (EPROM Ø). Circuit operation for all other EPROMs is identical to that of EPROM Ø.

When address lines $\overline{A10}$, $\overline{A11}$ and $\overline{A12}$ are HIGH and there is a valid LOW $\overline{\text{Board Select}}$ signal at IC F pin 12 (zone A7), output pin 9 of IC F and pin 6 of IC D (zone B2) go LOW. If IC D pin 5 is also LOW, output pin 4 goes HIGH and is inverted by IC E. This inversion causes IC E pin 8 (zone B2) to go LOW. EPROM pin 20 is then $\overline{\text{Chip Selected}}$ LOW.

This scheme can enable only one EPROM at a time. When pin 5 of IC D goes HIGH and is inverted through IC D, the resulting LOW at IC E pin 9 (zone B2) "deselects" the EPROM. IC E is an open collector device which pulls up pin 20 of the EPROM to Vcc (+5v) through resistor R33 during deselection.

IC H (zone A5) controls IC L pin 3 (zone B4) and, consequently, IC D pin 5 (zone B2). IC H pin 6 (zone A5) is normally HIGH unless a WRITE command is sent to the board (refer to Section 2-8 for further information on WRITE circuitry). IC H pin 9 (zone B5) controls IC L pin 1 (zone B4) and thus, IC L pin 3.

Flip-Flop H is controlled by ICs J and K (zone A4). During the first state of every machine cycle, a PSYNC signal pulses HIGH on the Altair bus. This signal is "ANDed" with SMEMR in IC K (zone A4), causing IC K pin 3 to pulse LOW within the first time state of each memory read machine cycle. IC K pin 3 is then tied to the PRESET input to the flip-flop (IC H pin 10, zone A4) which sets flip-flop H at the beginning of each Memory Read cycle. IC J pin 3 (zone B4) is tied to the PDBIN line. After PDBIN goes LOW, output pin 4 of IC J goes HIGH, clocking the flip-flop into the Reset condition and also causing IC L pin 1 (zone B4) to go LOW. As described in the preceding paragraph, this operation "deselects" the EPROM after the falling edge of the PDBIN signal has clocked data into the CPU. Early deselection of the EPROM saves power on the board and insures that no two EPROM enables overlap.

Table 2-F. EPROM Selection in IC F

$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	IC(F) OUTPUT PINS 9	7	6	5	4	3	2	1
H	H	H	L	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H
H	L	H	H	H	L	H	H	H	H	H
L	L	H	H	H	H	L	H	H	H	H
H	H	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	L	H
L	L	L	H	H	H	H	H	H	H	L

*NOTE: A LOW Board Select must be True at IC F pin 12 or all output pins will be HIGH.

2-8. 12-VOLT SWITCH CIRCUITRY

The EPROMs on the card are separated into two groups of four. Transistor Q6 supplies power from the +12v power supply bus to the first four EPROMs on the card; Q5 supplies the remaining four. Q6 is turned on when IC K pin 8 (zone A5) goes LOW. A LOW signal at IC K pin 11 (zone A5) turns on Q5. Pins 10 and 12 of IC K are tied to IC J pin 2 (zone A5), the inverted $\overline{\text{Board Select}}$ signal. Thus, the +12v switches are disabled unless $\overline{\text{Board Select}}$ ($\overline{\text{BS}}$) is true (LOW), in which case IC J pin 2 goes HIGH. Inverted address line $\overline{\text{A12}}$ is tied to IC K pin 9 (zone A5). $\overline{\text{A12}}$ is inverted through IC J pin 12 (zone A5) and is tied to IC K pin 13 (zone A5). As a result, IC K pin 8 (zone A5) goes LOW when A12 is LOW and the board is selected. Thus, +12 volts are switched to the first four EPROMs. If the board is selected and A12 is HIGH, the last four EPROMs are turned on by IC K pin 11 (zone A5).

2-9. READ CIRCUITRY (Figure 2-1)

One of 1024 bytes is selected within each EPROM by the ten address lines (AØ-A9), which (after being filtered by resistors) tie directly to all EPROMs in parallel.

To read a given EPROM data byte, the desired byte must be addressed, the proper chip select must be enabled, and the +12v power supply must be turned on. The data is then present at the eight EPROM output pins. Because these outputs are parallelled across all eight EPROMs, only one EPROM may be enabled at a time.

The output EPROM data bus must be gated onto the CPU data input bus during the PDBIN Read cycle. This is accomplished via tri-state buffers IC R and IC S. The enable lines for these buffers (pin 1 on both ICs) are tied to IC L pin 8 (zone A1) which goes LOW to enable the buffers when IC L pins 9 and 10 (zone A2) are both HIGH. A HIGH at IC J pin 10 occurs when IC L pin 6 (zone A1) goes LOW; i.e. when PDBIN and SMEMR are HIGH, as during a Memory Read cycle. Thus, data from the selected EPROM is gated onto the DIØ-DI7 input data bus during a Memory Read cycle to the board.

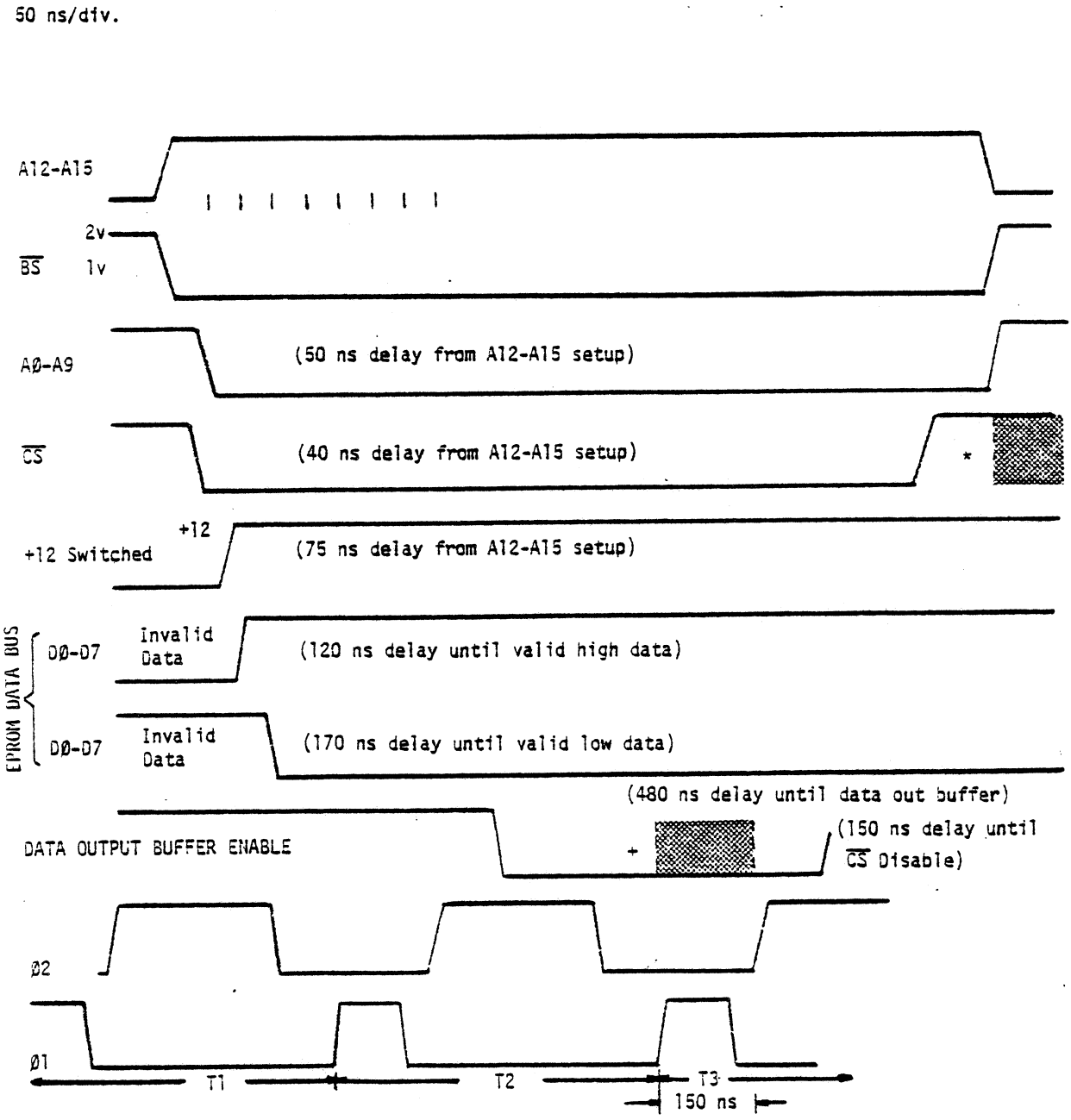
The Protect Status line should be LOW when the card is accessed (unless the EPROMs are to be reprogrammed.) When the Protect Status line is LOW, IC R pin 14 (zone B1) is set LOW through switch S2. (Pin 14 is

set HIGH when S2 is in the WRITE position.) IC R pin 15 provides the enable signal for the Protect Status buffer and is actuated when IC M pin 6 (zone A7) goes LOW. IC M pin 6 goes LOW when the board is addressed as long as the machine cycle is not an Input or an Output instruction. SINP and SOUT are inverted in IC T (zone A6), causing pin 4 to go LOW on an Input or an Output command, thus disabling IC M pin 6 and the Protect Status buffer. Pins 1 and 2 of IC M (zone A7) are pulled up by resistor R51 and pin 5 is enabled during $\overline{\text{Board Select}}$.

The PRDY Tri-state buffer is enabled at the same time as the Protect Status buffer and its signal is originated through ICs L and J. When IC L pin 11 (zone A3) goes HIGH, IC J inverts this signal to a LOW. If IC R pin 15 is enabled, the CPU will go into a WAIT cycle and will halt processing until PRDY is released HIGH again.

IC L pin 12 (zone A3) floats HIGH if jumper J6-J7 is not installed. As previously described, IC H pin 6 (zone A5) is HIGH during a Read operation. Therefore, a WAIT signal is not normally generated since IC L pin 11 (zone A3) is LOW. If jumper J6-J7 is installed, however, IC L pin 11 will pulse HIGH when IC K pin 3 (zone A4) goes LOW. This occurs at the beginning of each Memory Read cycle and generates a momentary LOW pulse on the PRDY line which forces a CPU WAIT state to be executed during each Read command. This WAIT state is a 500 ns pulse, since IC K pin 3 again goes HIGH when the PSYNC signal falls LOW during the second state of a machine cycle.

During a Write cycle (see Section 2-10), a LOW signal from IC H pin 6 (zone A5) holds the PRDY line LOW, thus generating a WAIT state the length of which is determined by IC H set time.



* EPROM Data "Float" 120 ns after $\overline{CS}$ Disable

\+ Valid CPU Data Sample Time

Figure 2-1. Read Cycle

2-10. WRITE CIRCUITRY (Figure 2-2)

The 88-PMC8 board's Write circuitry makes use of all of the previously described circuitry and contains the additional circuits listed below.

1. Circuitry to enable the CPU output data bus which transfers data into the EPROMs during programming.
2. Timing circuitry to hold processing during a Write to EPROM and to enable the +12v Chip Select and +26v programming switches.
3. Chip Select (+12v) switch circuitry used to pulse the CS line (pin 20) of each EPROM during a Write command to EPROM.
4. +26v Programming switches to pulse the programming pin (pin 18) on each EPROM during a Write command to the EPROMs.

The $\overline{\text{SWO}}$ and SOUT signals are used to decode a Write command to the board. When both signals are LOW, a valid Write to memory is in effect. Resistor R52 and capacitor C25 form a differentiator circuit which insures that IC G only triggers on the leading edge of the pulse from IC T pin 1. Pin 1 of IC T (zone B6) goes HIGH and fires the first half of one-shot IC G if $\overline{\text{Board Select}}$ is in the valid LOW state. IC G pin 4 (zone A6) then goes LOW which sets the first half of flip-flop H. IC H pin 6 (zone A5) goes LOW when set, causing several operations to occur.

First, IC L pin 2 (zone B4) goes LOW which "deselects" all EPROMs. In the Write mode, deselect actually indicates that all EPROMs are ready to be written into.

Second, a LOW is applied to tri-state buffer pin 15 of ICs S (zone C8) and P (zone B8) and pin 1 of IC P (zone B8). These ICs are the input data bus buffers. The LOW enable signal allows data from the CPU bus to be buffered through to the EPROM data bus so that bus data may be stored in the EPROMs.

Third, a LOW signal is applied to IC L pin 13 (zone A3) which causes the PRDY line to be pulled LOW. This LOW signal generates a reoccurring WAIT state which guarantees that the CPU will not change pertinent data or address lines during the Write cycle to EPROM (approximately 1 ms).

Finally, IC K pin 4 (zone B3) is pulled LOW, causing pin 6 (of IC K) to go HIGH. This HIGH signal provides transistor switch Q12 with positive base drive to turn it on and to allow +12 volts to be passed to the emitter of Q12. The CS lines of all eight EPROMs are bussed together through diodes D1, D3, D5, D7, D9, D11, D13 and D15. Thus, all EPROM CS lines are pulled up to approximately +12 volts.

After approximately 100 µs, pin 4 of IC G (zone A6) again returns HIGH, strobing the second half of one-shot G. Pin 12 of IC G goes LOW for approximately 1 ms which forces IC E pin 5 (zone B2) LOW and pin 6 (of IC E) HIGH. Transistor switch Q11 is then turned on. Q11 passes +30v to transistor switches Q1-Q4 and Q7-Q10. These switches use EPROM select lines from IC F and inverters A, C and E to apply +30v at programming pin 18 of a particular EPROM. For example, if EPROM #2 is being addressed, IC F pin 6 (zone A7) and IC C pin 5 (zone C4) go LOW. This causes IC C pin 6 (zone C4) to float HIGH and, if Q11 is turned on, the pin 6 signal will float up to approximately +30v which will turn on Q8 and supply +30v to EPROM pin 18. When address lines change to disable EPROM #2, the programming pin of the EPROM is pulled LOW through diode D12.

After IC G pin 12 (zone A5) returns HIGH, IC H is clocked into a Reset condition that produces the following results:

1. IC E pin 5 (zone B2) goes HIGH, causing switch Q11 (+30v) to turn off. Thus, +30v is removed from the EPROM being written into.
2. IC H pin 6 (zone A5) goes HIGH, disabling data bus buffer ICs S pin 15 (zone C1) and P pins 1 and 15 (zone B8).
3. IC K pin 4 (zone B3) goes HIGH, disabling the +12v switch (Q12) and removing +12v from the CS lines of the EPROM.
4. IC L pin 2 (zone B4) goes HIGH, enabling gate L pin 3 to supply EPROM $\overline{\text{Chip Selects}}$ during subsequent Read cycles to EPROM.
5. IC L pin 13 (zone A3) goes HIGH which releases the PRDY line. This action causes the CPU to resume processing either by writing the next byte of EPROM, reading the current byte of EPROM or performing another function.

Note that actual writing time for one byte is 1 ms (max), but the cumulative programming time (for the 2708 type EPROM) is 10 ms (min) per byte for valid data retention. Therefore, the Write program must sequentially write into each of the 1024 sequential bytes in each EPROM, then repeat the process for 100 total passes through all of the EPROMs. After all 1024 bytes in each EPROM have been written 100 times, the program should make a comparison check of each byte of EPROM to the original data block to insure valid data entry.

When writing to the EPROMs on the board, diodes D1, D3, D5, D7, D9, D11, D13 and D15 drive the $\overline{CS}$ lines to +12v. Due to the internal construction of the EPROMs, a 10 µs delay is required (after $\overline{CS}$ has returned LOW) before data can be valid. If an attempt is made to read the EPROMs before the 10 µs period has elapsed, erroneous data may be read. If, however, the cathode lead of D15 is pulled from its socket, the $\overline{CS}$ line of EPROM Ø is not driven to +12v and the 10 µs delay is not required. The cathode lead of D15 should be removed when a program located at EPROM Ø is to be used to write EPROMs on the board. This will allow EPROM Ø to be read immediately after every Write to the board.

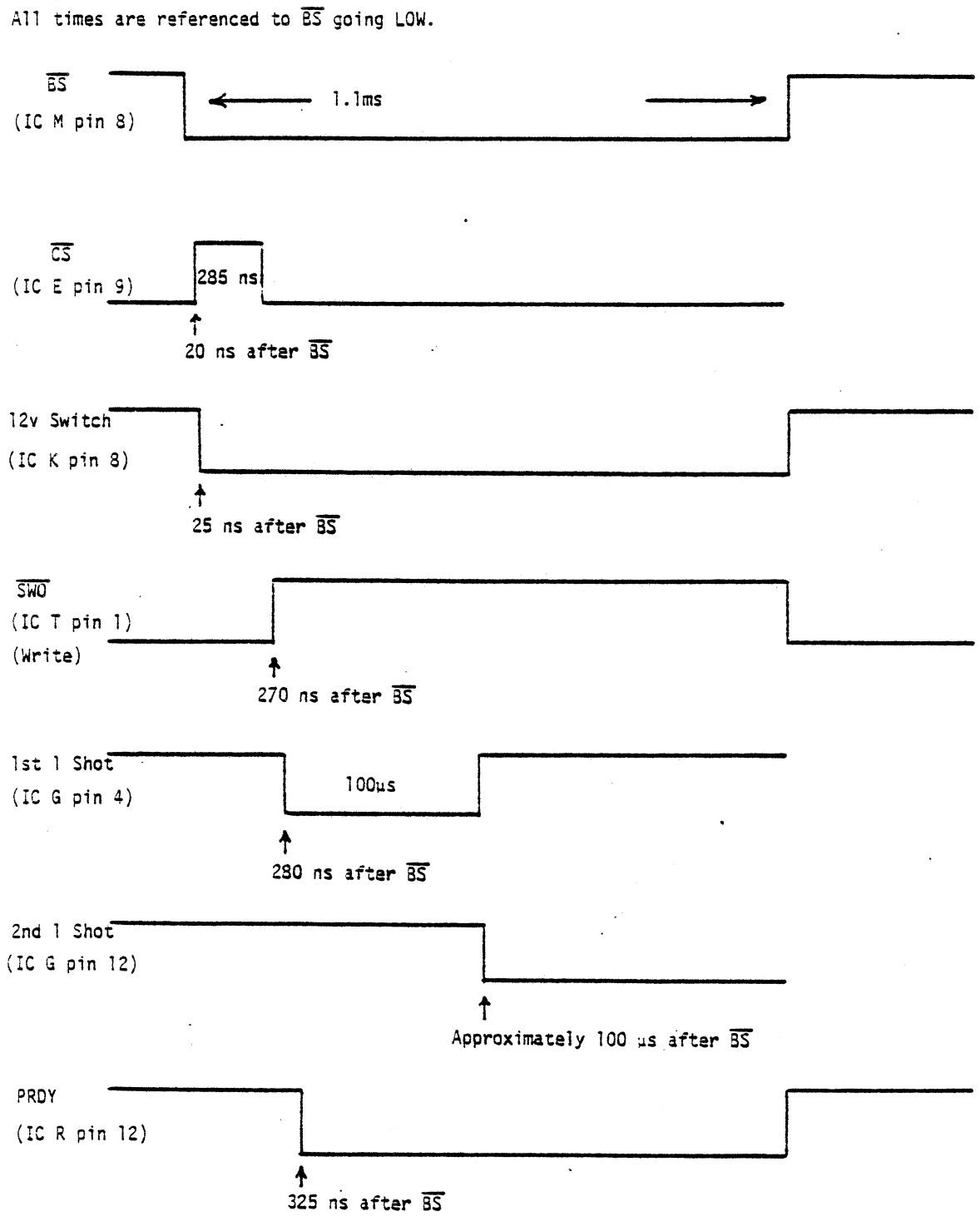


Figure 2-2. Program Cycle

2-11. OPTIONAL CONFIGURATIONS

The modifications shown in Table 2-G enable the customer to utilize electrically erasable EPROMs such as the NEC MPD 458D type EPROM. The advantage of this type of PROM is that its erase time is approximately 1 minute and reprogramming cycles are reduced from 100 passes to 1 pass. However, to properly utilize the EPROM, different hardware modifications are necessary, depending on whether the EPROM is being written into or read from. Table 2-G lists modifications for either mode and includes standard configuration modifications to return to 2708 type operation. Note that erasure of the 458 type EPROM requires circuitry that is not supplied by MITS.

Refer to Paragraph 2-6 for information on the optional 4K modification.

Table 2-G. User Modifications (88-PMC8)

MODIFICATION	2708 (STD. CONFIGURATION)	PD 458 (READ)	PD 458 (WRITE)
(WAIT State Jumper)	Install (J6/J7) if a WAIT State is desired	Install (J6/J7) if a WAIT State is desired	X
(Vcc Jumpers)	Install (J2/J1) Remove (J3/J1)	Install (J2/J1) Remove (J3/J1)	Remove (J2/J1) Install (J3/J1)
(Vdd Jumpers) **	Bypass R3 with a jumper wire	Remove R3 (& jumper, if present)	Install R3 (Remove jumper if present)
	Remove R9 (& jumper, if present)	Bypass R9 with a jumper wire	Install R9 (Remove jumper, if present)
(+26V Module Jumper)	Install (J4/J5)	Remove (J4/J5)	Install (J4/J5)
Jumpers wires between Pins (15 & 16)* on each eprom (8 places) (Back side of board)	Remove jumpers, if present	Install jumpers	Remove jumpers, if present
(Vbb Supply)	Install 7812 Output lead (Bottom pin) & remove jumpers across C11 & C12	Install 7812 Output lead (Bottom pin) & remove jumpers across C11 & C12	Remove output lead from 7812 regulator (Bottom pin) & bypass C11 & C12 with jumpers
Jumpers across R8, R12, R15, R20, R25, R26, R29, R32	X	Install jumpers	Remove jumpers

NOTE: Card must be turned OFF when doing all modifications.

X = Don't Care
* Pins designated are socket numbers - not eprom pin numbers
** - Values for R3 & R9 are given in Figure 2-3, sheet 1.

SECTION III
TROUBLESHOOTING

3-1. GENERAL PROCEDURES

Section III is designed to aid the user in pinpointing trouble areas and correcting problems that may be encountered with the 88-PMC8 board. These troubleshooting procedures are intended only as a guide. They contain simple tests that should locate and correct most malfunctions. However, if the problem(s) encountered cannot be rectified, send the board to the MITS Repair Department or your local Altair dealer.

Refer to the Troubleshooting Flowchart, Figure 3-1. Note that there are two main problem divisions:

1. The board will not Read or Write. For problems of this kind, follow Tables 3-A through 3-E.
2. The board Reads properly, but will not Write. For problems of this kind, follow Tables 3-F through 3-J.

After the problem is found, the board should be rechecked to make sure it can program correctly.

Substitution of EPROMs is a fast, efficient way to decide whether the card or the EPROM itself is at fault. Unfortunately, the time-consuming method of checking bit-for-bit at each address is the only way to guarantee EPROM data. If two boards are purchased, however, it is much simpler and faster to check bit-for-bit between boards.

In all of the following tests, LOW and HIGH refer to standard logic levels (see Paragraph 2-2) unless otherwise noted.

> WARNING
>
> If the board has undergone a catastrophic failure, EPROMs may be destroyed if inserted into the board before the problem(s) has been corrected. For this reason, install only one EPROM in the board until it is known that at least one EPROM can be successfully read.

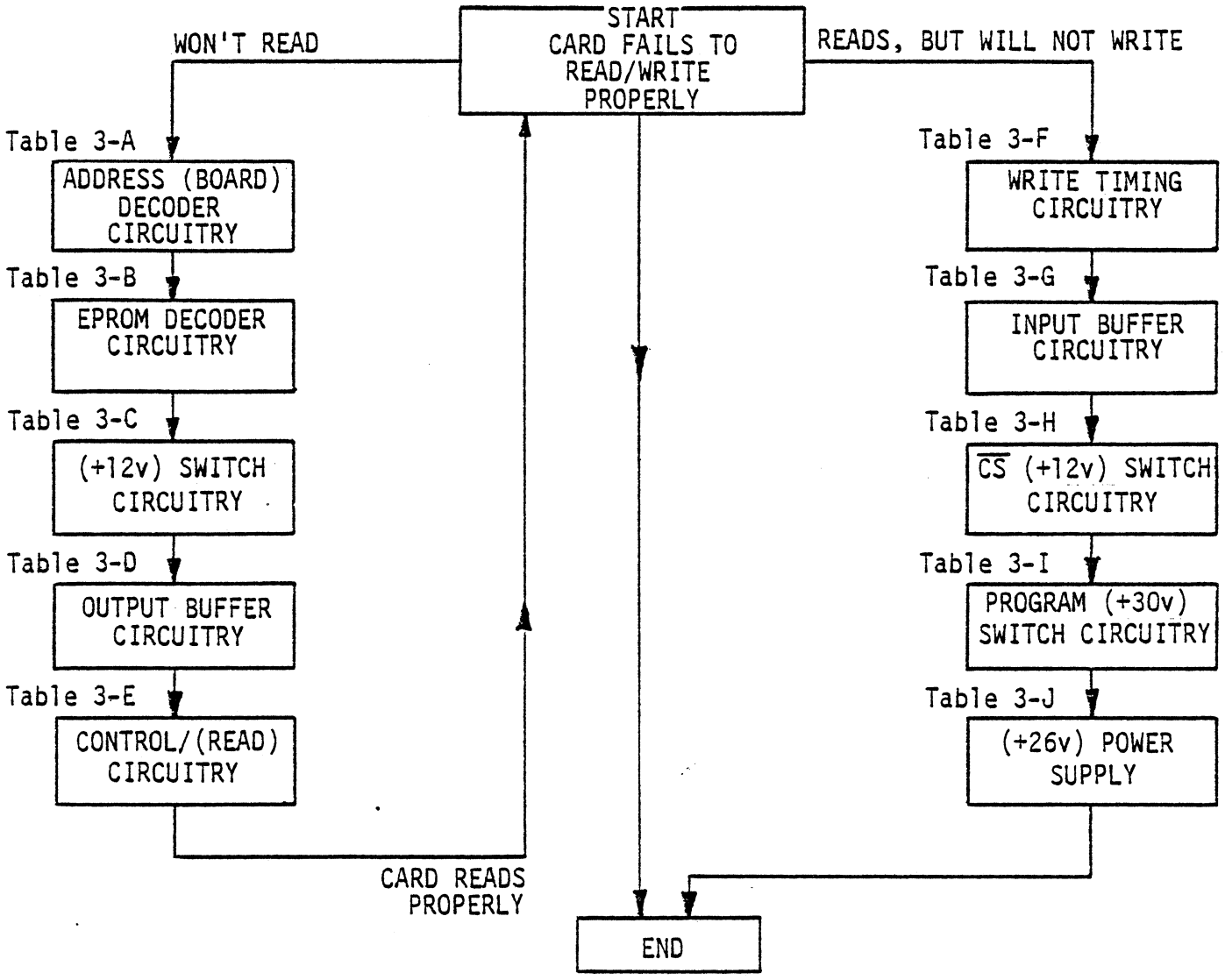


Figure 3-1. Troubleshooting Flow Chart

3-2. VISUAL INSPECTION

The first step in troubleshooting is to carefully examine each board for solder bridges, open lands, misplaced components, etc. A thorough inspection of this kind will eliminate one possibility for errors and will allow troubleshooting efforts to be concentrated elsewhere. Carefully check each board using the list below.

1. Look for solder bridges.
2. Look for leads that have not been soldered.
3. Look for cold solder connections.
4. Examine the board's lands for "hairline opens" or "bridges."
5. Check the ICs for proper pin placement and good socket connections.
6. Examine the electrolytic and tantalum capacitors for proper polarity.
7. Examine the diodes for proper polarity.
8. Check the color codes on all resistors.

When these checks have been successfully completed, proceed to the proper table as shown in Figure 3-1.

3-3. IMPORTANT NOTES

1. If the board was purchased in kit form or has suffered a catastrohpic failure, a quick checkout procedure (starting with Table 3-A) should be performed before the EPROMs are installed and the voltage levels at all EPROM pins should be verified. This procedure may prevent EPROM desctruction due to solder bridges, broken lands, etc.

2. If the CPU fails to respond to commands while the 88-PMC8 is accessed, the PRDY (pin 72) signal on the bus may be held LOW through a logic error on the board. If this is the problem, carefully bend up pin 11 of IC R, proceed with testing until the fault is found, and replace the pin. Note that WRITE timing will not be correct if Program 3-II is run. In this case, the timing of ICs G and H should be checked by single stepping through the program to verify correct timing.

Table 3-A. Read Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Check power supply voltages at VR1, VR2 and VR3 as listed below. +5v ± .5v +12v ± .5v -5v ± .5v	Proceed to Step 2.	Check bus voltages and, if correct, replace bad regulators.
2	Attach an oscilloscope probe to IC M pin 8 (Board Select). Set up the board address to 56K by raising poles 2, 3 and 4 on switch S-1. Turn power on, and raise sense switches A13, A14 and A15 Reset the machine to the zero memory location. Pin 8 should be HIGH.	If a HIGH is present at pin 8, proceed to Step 3.	Check the +5v power supply at VR1 and also at IC M pin 14. IC M pins 10, 12 and 13 should be LOW in the Reset condition. If not, check for an open switch (S1).
3	Examine 56K and check for a LOW at pin 8 (of IC M).	If present, Board Select is working properly. Proceed to Step 5.	If absent, proceed to Step 4.
4	Reset the computer, and check pins 10, 12 and 13 of IC M for LOW signals. These gates invert address lines A13, A14 and A15 which should be LOW when Reset and HIGH when 56K is examined.	Proceed to Step 5.	If pins 10, 12 and 13 are HIGH, pin 8 should go LOW. If a LOW is not present at pin 8, replace IC M. If IC N pins 10, 8 and 12 do not invert A13, A14 and A15 as described, IC N should be replaced.
5	Repeat steps 2 and 3, and observe IC J pin 2. It should invert the $\overline{BS}$ signal at IC M pin 8.	Proceed to Table 3-B.	IC J is defective and should be replaced.

Table 3-B. EPROM Decoder Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Examine 56K and check for a LOW at EPROM Ø pin 20. When Reset, pin 20 should go HIGH. Examine 57K, and check for a LOW at pin 20 of EPROM 1. Step through all 8 EPROM addresses, and examine in 1K increments. Insure that pin 20 goes LOW when accessed and HIGH when Reset in each case.	Proceed to Table 3-C.	Proceed to Step 2.
2	Check for a LOW signal at IC F pin 12 while examining each address (56K - 64K) in 1K increments. Check for a HIGH when the computer is Reset. Also check for HIGHs at IC F output pins 1 through 7 and 9, when Reset.	Proceed to Step 3.	If the power supply voltages are correct, replace IC F.
3	When examining 56K, IC F pin 9 should go LOW and all other output pins should go HIGH. If correct, step through each 1K incremented address (through 64K), and verify that pins 7, 6, 5, 3, 2 and 1 go LOW in turn, and that no two pins go LOW at the same time.	Proceed to Step 4.	Examine IC F pins 15, 14 and 13. These pins should follow inverted address lines A10, A11 and A12, respectively. Examine each switch while it is in the up position, then Reset. IC N (which is connected to A10, A11 and A12) should be replaced if it fails to pass this test.

Step	Instructions	If Correct	If Incorrect
4	(Note: The $\overline{CS}$ circuit for EPROM Ø is described below. All other EPROM $\overline{CS}$ circuits are identical if the tests in step 1 fail.) When 56K is examined and IC F pin 9 goes LOW, pins 5 and 6 of IC D should also go LOW. IC D pin 4 should go HIGH and IC E pin 8 should invert the signal to a LOW, pulling pin 20 of EPROM Ø LOW.	Proceed to Table 3-C.	If pin 5 of IC D is not LOW, check IC L pin 3 for a LOW signal. When examining an EPROM, IC L pin 2 should be HIGH. Pin 1 should be HIGH when the computer is not in a RUN state. If these conditions are not present, proceed to Table 3-E. (After step 3 in Table 3-E has been successfully completed, return to this step.) If IC L pins 1 and 2 are HIGH, but pin 3 is not LOW, replace IC L. If IC D pins 5 and 6 go LOW but pin 4 does not go HIGH, replace IC D. If IC E does not invert the signal at IC D pin 4, replace IC E.

Table 3-C. +12v Switch Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Reset the computer, and check IC K pin 9 for a HIGH and pin 13 for a LOW.	Proceed to Step 2.	Replace IC J or IC N.
2	Examine 4K while holding sense switch A12 up. Pin 13 of IC K should go HIGH and pin 9 should go LOW.	Proceed to Step 3.	Replace IC J or IC N.
3	Examine 56K, and check IC K pin 8 for a LOW and pin 11 for a HIGH.	Proceed to Step 4.	Replace IC K.
4	Examine 60K and check IC K pin 11 for a LOW and pin 8 for a HIGH.	Proceed to Step 5.	Replace IC K.
5	When IC K pin 8 is LOW, Q6 should turn on and should pass +12v from the emitter to the collector, and consequently, to pin 19 on EPROMs Ø through 3. When IC K pin 11 is LOW, Q5 should turn on and should pass +12v to EPROMs 4 through 7.	Proceed to Table 3-D.	Check for +12v at the base of Q5 and Q6 (center lead) when K8 or K11 is HIGH. If absent, replace Q5 or Q6.

Table 3-D. Output Buffer Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	If the tests in Table 3-A through 3-C have been successfully completed, it should be possible to examine data within the EPROM. Examine 56K and look for the first byte of data at EPROM output pins 17 (MSB), 16, 15, 14, 13, 11, 10 and 9 (LSB). (The first byte of the optional transfer EPROM is 076 octal.)	If data is correct at the EPROM output pins, check for the same data at the following corresponding DIØ-DI7 bus lines: IC S pin 9 (MSB) and pin 3; IC R pins 3, 9, 5 and 7; IC S pins 5 and 7 (LSB)*. If this data is correct, proceed to Step 3. If incorrect, proceed to Step 2.	If data is absent or incorrect, check for LOWs at all address lines (EPROM pins 1 through 8, 22 and 23). Supply voltage limits are given in Table 3-A, Step 1. Check for +5v at pin 24, -5v at pin 21, a valid $\overline{CS}$ LOW signal at pin 20, and +12v at pin 19. If absent or incorrect, replace voltage regulators as necessary, or repeat $\overline{CS}$ tests.
2	Check for a LOW signal at pin 1 (enable) of ICs R and S. If HIGHs are present, the outputs will be in the high-impedance state and will float up to Vcc from pullups on the CPU board.	If a LOW signal is present but inconsistent and input to output signals are present at ICs R and S, replace these ICs as necessary. (Note that ICs R and S do not invert the data.)	If absent, check for HIGHs at IC L pins 9 and 10. Pin 9 should be HIGH if IC L pin 6 is LOW (i.e. when the machine is held in the Examine state). If incorrect, replace IC L. IC L pin 10 should follow the numbered Board Select signal at IC J pin 2.
3	To test the $\overline{PS}$ and PRDY buffers, examine 56K and check IC M pin 6 for a LOW. This LOW signal enables IC R pin 15 and allows $\overline{PS}$ (pin 69 on the bus) to track the S2 switch.	Proceed to Step 4.	If absent, check for HIGHs at IC M pins 1, 2, 4 and 5. If pin 4 is not HIGH, check IC T pin 4. In the Examine state, pins 5 and 6 of IC T should go LOW and force pin 4 HIGH. If incorrect, replace IC T. If pin 5 of IC M does not go HIGH, refer to Table 3-A, Step 4.

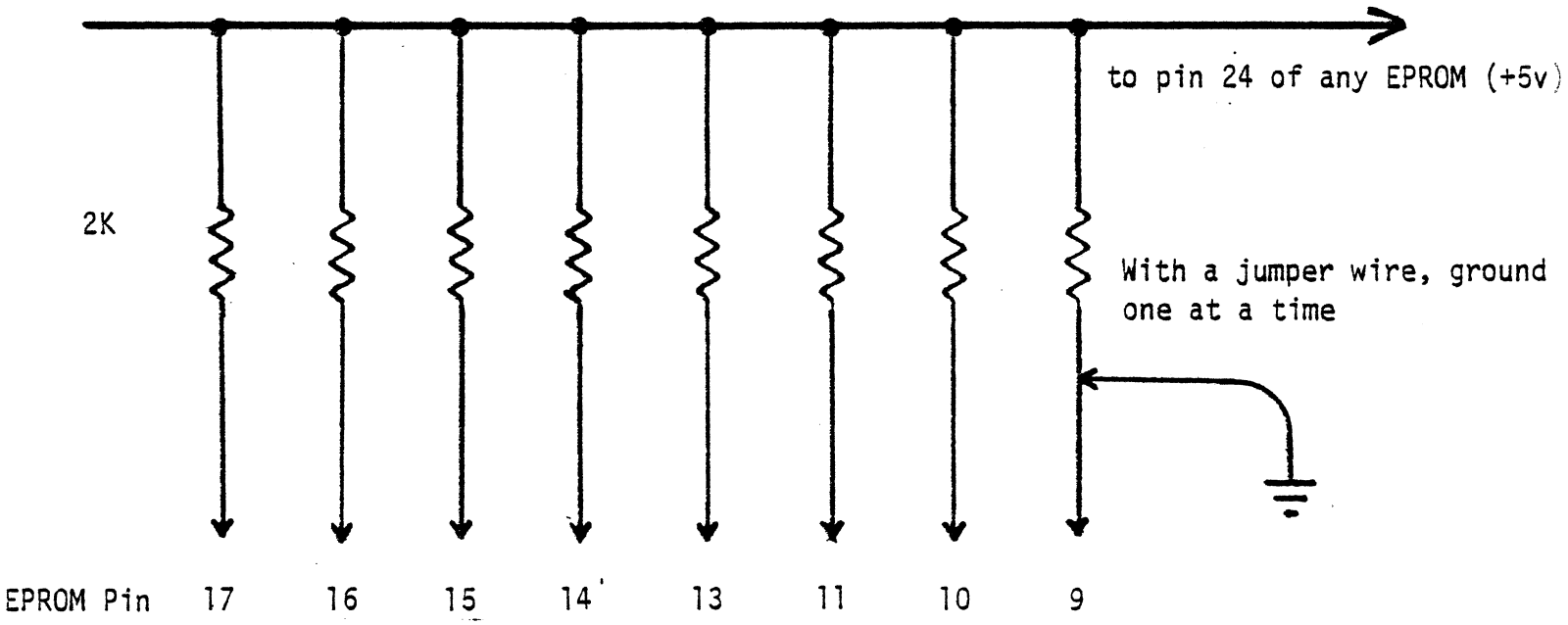
Step	Instructions	If Correct	If Incorrect
4	In the Protect position, $\overline{PS}$ should go LOW; and in the Write position, $\overline{PS}$ should go HIGH. In a similar manner, $\overline{PRDY}$ (pin 72 on the bus) should follow the inverted signal from IC L pin 11. While resting in the Examine state, a LOW at IC L pin 11 forces IC J pin 8 and IC R pin 11 HIGH.	Proceed to Table 3-E.	If IC L pin 11 is not LOW, proceed to Table 3-E.

*A convenient way to quickly check all data bits at once is via the front panel data LEDs. Single step through Program 3-I until the last address byte (location 2) is displayed on the LEDs. Single step once more, and the actual data word will be displayed. By remaining in this state, data buffering can be checked as shown in Figure 3-2. If problems are suspected in the data buffering section of the board, the DI bus levels should also be checked with an oscilloscope.

Program 3-I. Read Program

Location	Data	Instruction
000	072	Read 1st byte from PROM Card
001	(000)	(56K)
002	200	
003	303	
004	(000)	Jump back and repeat
005	(000)	

Note: Remove all EPROMs before performing this test.



With pullups installed, sequentially ground one pin at a time and verify the response at the DI bus lines.

Figure 3-2. Data Buffering Check

Table 3-E. Control (Read) Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Examine 56K and check for a HIGH output at IC H pin 6.	Proceed to Step 2.	If pin 6 is not HIGH, check pin 4 for a short to ground or for a LOW pulse during Reset or Examine.* If present, replace IC G. If there is no short and a pulse cannot be detected, replace IC H.
2	Examine 56K and monitor IC H pin 9 for a HIGH output.	Proceed to Step 3.	If absent, check for a HIGH at IC K pin 3. If absent, replace IC K or IC H or check for a short at IC K pin 3.
3	Holding Reset should clear flip-flop H and should reset pin 9 LOW.	If correct, proceed to Step 4.	If this does not occur, check IC J pin 4. Releasing the Reset switch should force pin 4 LOW, and actuating Reset should force it HIGH. If incorrect, replace IC J or IC H.
4	Normally output pin 11 of IC L is LOW since input pins 12 and 13 are HIGH. If the WAIT state jumper (J6-J7) is installed, however, pin 12 will pulse LOW when running Program 3-I. This LOW pulse will reflect through IC L pin 11 as a HIGH pulse inverted by J pin 8 and will be buffered out through IC R pin 11 to the bus as a momentary (500 ns) LOW pulse.	Proceed to Table 3-F.	If improper operation is still found, carefully retrace the steps in Tables 3-A through 3-E, taking special notice of logic levels, fast pulses, noise, etc. Also, try simulating EPROM data by installing pullup resistors to each data output line. Then sequentially ground each line, and verify that data is forced onto the DI bus correctly. Use 2K resistors with a common point of +5v (see Figure 3-2). Programming capability should be re-verified after the Read portion of the board has been repaired. Start with the initial test in Table 3-F, and verify correct operation.

*This may be a very fast noise spike.

Table 3-F. Write Timing Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Load Program 3-II into the machine and run, keeping the board address at 56K. Monitor pin 4 of IC G for LOW pulses approximately 100 µs in length at intervals of approximately 1.3ms.	If pulses are correct (±20%), proceed to Step 3.	If pulses are missing, check IC G pin 2. If pulses are missing from pin 2, check IC T pins 2 and 3. Pin 2 of IC T should remain LOW and pin 3 should repeatedly pulse LOW. If the pulses at pins 2 and 3 are correct, replace IC T. If a constant LOW is present at IC G pin 4, check IC H pin 6. If pin 6 pulses LOW for 2 µs at 10 µs intervals, the problem is probably linked to the PRDY line circuitry (no WAIT state to CPU). Replace IC L and/or IC J.*
2	Monitor IC H pin 6, and look for LOW pulses approximately 1.3 ms in length.	Proceed to Table 3-G.	Replace IC G or IC J.*

Program 3-II. Write Program

Location	Data	Comments
000	076	Load Accumulator
001	(000)	(Data Byte)
002	062	Write to PROM Board
003	(000)	(56K)
004	200	
005	303	
006	(000)	Jump back and repeat
007	(000)	

*See Paragraph 3-3.

Table 3-G. Input Buffer Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	While running program 3-II, monitor pin 15 of ICs P and S and pin 1 of IC P. All three pins should have LOW pulses corresponding to those found at IC H pin 6.	Proceed to Step 2.	Check for an open land and repair as necessary. Check output level of IC H.
2	Stop the program, Reset and single step until the above mentioned pins go LOW and hold. Data will now be transferred from the DØ bus lines through ICs P and S onto the EPROM data bus. Look for the proper binary code at EPROM pins 17 (MSB), 16, 15, 14, 13, 11, 10 and 9 (LSB) corresponding to the data byte (location 001 in Program 3-II).	Proceed to Step 3.	Replace P or S buffers if corresponding input/output signals disagree while the enable pins (1 or 15) are held LOW.
3	Change the data byte to 001, and repeat step 2, noting that the EPROM bus lines change accordingly. Separately check each of the 6 remaining data lines in the same manner. Be sure to change the data byte for each line exclusively.		

Table 3-H. CS +12v Switch Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Remove any EPROMs containing programs and replace them with EPROMs that have been erased. Run Program 3-H, and monitor IC K pin 6 for 1.3 ms HIGH pulses.	Proceed to Step 2.	Replace IC K.
2	Move S2 to the Write position. Transistor Q12 passes +12v from its collector to emitter when IC K pin 6 is HIGH. Therefore, +12v pulses should be seen at the junction of Q12, D15 and R43.	If the +12v pulses are present at the junction, proceed to Step 3.	The +30v power supply module biases the base of Q12. Check for voltage pulses in excess of 12v at this point. If not present, proceed to Table 3-J, then complete this test. If pulses are not present at the junction, Q12 is probably defective and should be replaced.
3	If pulses are present at the junction of Q12, D15 and R43, they should also be present at pin 20 of all of the EPROMs.	If present, proceed to Table 3-I.	If pulses are absent, D15 may be open or faulty logic may be pulling IC E pin 8 LOW. Also check for a short to ground at the cathode of the following diodes: D1, D3, D5, D7, D9, D11, D13. Repair as necessary.
4	Turn off S2.		

Table 3-I. Program (+30v) Switch Circuitry Check

Step	Instructions	If Correct	If Incorrect
1	Run Program 3-II, and monitor IC E pin 6 for HIGH 1.3 ms pulses.	Proceed to Step 2.	If pulses are missing, IC E is defective and should be replaced.
2	When IC E pin 6 goes HIGH, transistor Q11 passes +26v from its collector to emitter. Therefore, +26v pulses should occur at the junction of Q11, D17 and R39 where they are passed to the program switches at each EPROM.	Proceed to Step 3.	Check for +27v at Q11 collector with S2 on. If not present, proceed to Table 3-J, then complete this test. If pulses are missing, Q11 is defective and should be replaced.
3	Check for +26v pulses at the collector of Q10.*	If pulses are present, check for +26v pulses at pin 18 of EPROM Ø. If present, proceed to Table 3-J. If absent, monitor IC E pin 2 which should go HIGH each time EPROM Ø is selected. This HIGH should turn on Q10. If pulses are absent at pin 2, replace IC E. If pulses are present at pin 2, but Q10 fails to turn on, Q10 should be replaced.	Missing pulses indicate that R39 is open, a program transistor has shorted out or the +26v power supply has failed.

*This test describes the EPROM Ø Write operation. Other EPROMs are similar in operation and can be verified by changing the address byte (location 004) in Program 3-II.

Table 3-J. +30v Power Supply Voltage Level Check

Step	Instructions	If Correct	If Incorrect
1	Verify that the proper +30v power supply level is present by measuring the voltage at J4 or J5. The level should be between 27v and 30v.	If Write trouble still persists, insure that correct software and erasing procedures are being implemented.	If the voltage is incorrect, the power supply module must be returned to the factory for service or replacement.

Note: Since the power supply presents extra loading to the +5v regulator, it is recommended that the module be turned off (via S2) when not in use. This will maintain efficiency and will lower power dissipation in the regulator.

SECTION IV
ASSEMBLY

4-1. INTRODUCTION

Section IV contains complete step-by-step instructions for component installation and mounting of the 88-PMC8 board. Two organizational aids are provided throughout the instructions: 1) parts identification lists with spaces provided to check off each component as it is installed and 2) reproductions of the board's silkscreen showing previously installed components, components being installed and components yet to be installed (see Figure 4-1).

Before beginning the assembly procedures, carefully read the enclosed "MITS Kits Assembly Hints" booklet. It contains helpful suggestions and several important warnings. Failure to heed these warnings could cause you to void the warranty.

Check the contents of the kit using the parts list (Appendix A) to make sure all of the required components are enclosed. As you construct the board, read each step carefully and follow the instructions in the order in which they are presented. Always complete each step before going on to the next. Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

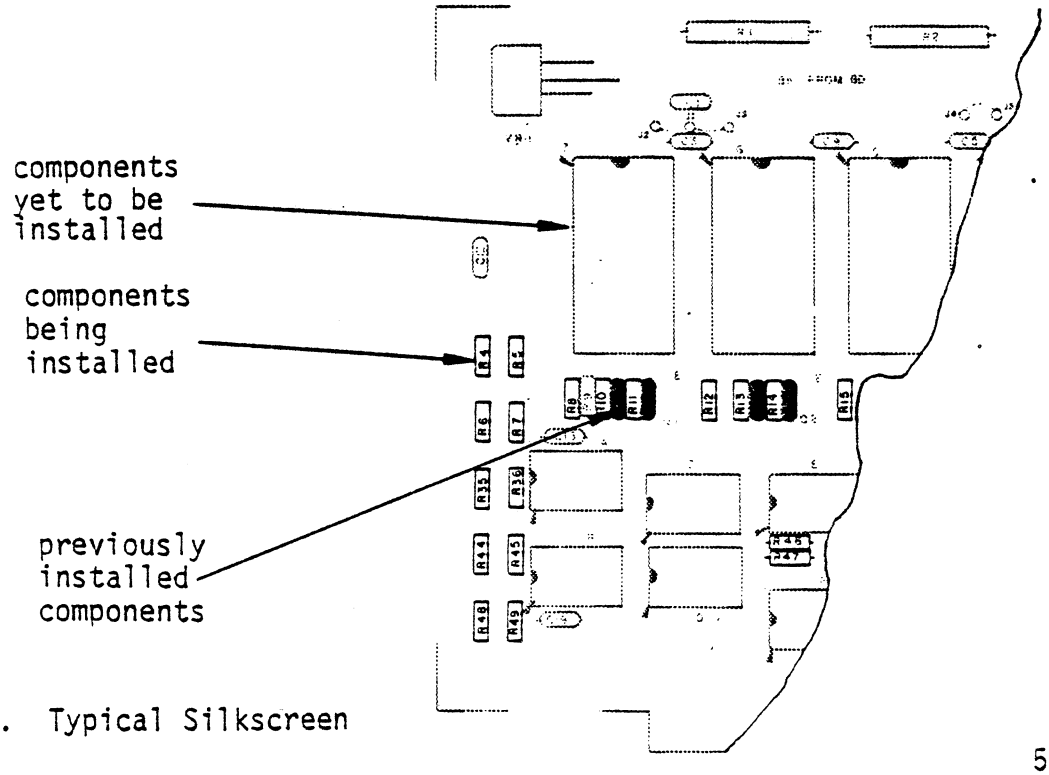


Figure 4-1. Typical Silkscreen

4-2. VISUAL INSPECTION

It is recommended that a visual inspection of the board be made before beginning the assembly procedures. A thorough inspection of this kind will eliminate one possibility for errors should the board fail to operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

Look for etching "bridges" or "opens" in the printed circuit lands, as shown in Figure 4-2 below.

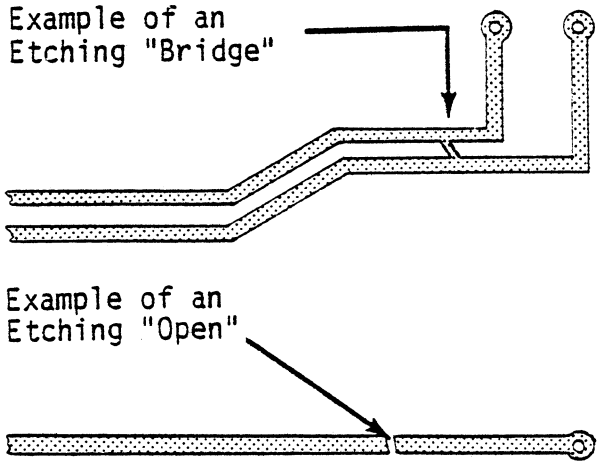


Figure 4-2. Visual Inspection

4-3. COMPONENT INSTALLATION INSTRUCTIONS

Paragraphs 4-4 through 4-12 describe the proper procedures for installing various types of components on the board. Read these instructions very carefully, and refer to them when necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void the warranty. Procedures of a less general nature are included in the remainder of the text.

4-4. Resistor Installation Instructions

Resistors have four, or possibly five, color-coded bands as represented in Table 4-A. The fourth band is gold or silver and indicates the tolerance. When assembling MITS kits, you need only be concerned with the three bands of color to one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value, and the third band represents a multiplier.

For example, a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. Refer to Table 4-A. Red denotes a value of 2, and violet a value of 7. Multiply 27 by the yellow multiplier band (10,000) to arrive at a total of 270,000 ohms (270K). The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the manual.

Make sure the colored bands on each resistor match the colors called for in the list of resistor values and color codes given in the specific assembly instructions. When the correct value has been selected, install the resistor according to the following instructions.

1. Use needle-nose pliers to bend the leads of the resistor at right angles to match their respective holes on the board.
2. Install the resistor into its correct holes on the silkscreened side of the board, and secure by bending the leads slightly outward.
3. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

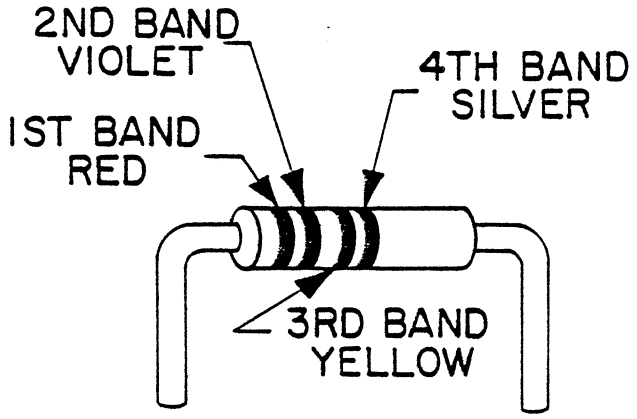


Figure 4-3. Resistor Color Codes

Table 4-A. Resistor Color Codes

Color	Bands 1 & 2	3rd Band (Multiplier)
Black	0	1
Brown	1	10
Red	2	10^2
Orange	3	10^3
Yellow	4	10^4
Green	5	10^5
Blue	6	10^6
Violet	7	10^7
Gray	8	10^8
White	9	10^9

4-5. Capacitor Installation Instructions

A. Electrolytic and Tantalum Capacitors

Polarity must be noted on electrolytic and tantalum capacitors before they are installed. Electrolytic capacitors may have one or possibly two of three types of polarity markings. Refer to Figure 4-4a. One type has plus (+) signs on the positive end; another has a band or a groove around the positive side in addition to the plus signs. The third type has an arrow with a negative (-) sign in the tip of the arrow. The capacitor must be oriented so that the arrow points to the negative side. Tantalum capacitors are marked with "+" signs on the positive side, as shown in Figure 4-4b.

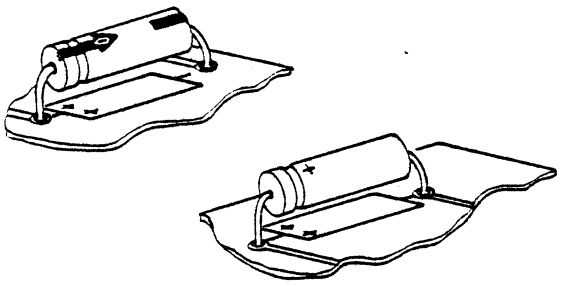


Figure 4-4a.
Electrolytic Capacitors

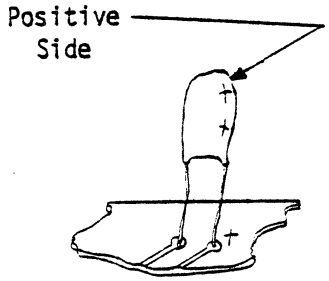


Figure 4-4b.
Tantalum Capacitors

Consult the capacitor value chart included with the specific instructions and install electrolytic and tantalum capacitors using the following procedure.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board. Insert the capacitor leads into the holes on the silkscreened side of the board, aligning the positive side with the "+" signs printed on the board. Secure by bending the leads slightly outward.
2. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

B. Epoxy Dipped Ceramic and Ceramic Disk Capacitors

Epoxy dipped ceramic and ceramic disk capacitors are non-polarized. Both types of capacitors are shown in Figure 4-4c.

Epoxy Dipped Ceramic Capacitor

Ceramic Disk Capacitor

Figure 4-4c.
Epoxy Dipped Ceramic and Ceramic Disk Capacitors

Consult the capacitor value chart included in the specific assembly instructions, and install these capacitors according to the following procedure.

1. Bend the two capacitor leads to conform to their respective holes on the board.
2. Insert the capacitor into the correct holes on the silkscreened side of the board, and secure by bending the leads slightly outward.
3. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

4-6. Diode Installation Instructions

Diodes are marked with a band on the cathode end. Each diode must be installed so that the cathode end is oriented towards the band printed on the board as shown in Figure 4-5. Failure to correctly orient the diodes may result in permanent damage to the unit.

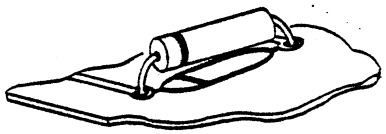


Figure 4-5. Diode Orientation

Refer to the list of diode part numbers included in the specific assembly instructions, and install each diode according to the steps below.

1. Bend the leads of the diode at right angles to match their respective holes on the board.
2. Orient the cathode end with the band silkscreened on the board, and insert the diode into its proper holes. Secure by bending the leads slightly outward.
3. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

4-7. Transistor Installation Instructions

Before installation, refer to the listing of part numbers included in the specific assembly instructions to check the part number of each transistor. Some types of transistors may look identical, but differ in electrical characteristics. If substitute part numbers are given, check the transistor identification chart (Figure 4-6) to make sure the correct substitutions are made.

The transistor must be oriented so that the emitter lead is installed in the hole on the board labelled with an "E." Refer to Figure 4-6 to determine which lead is the emitter.

1. After the correct transistor has been selected and the leads have been properly oriented, insert the transistor into its holes on the silkscreened side of the board. Secure by bending the leads slightly outward.
2. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

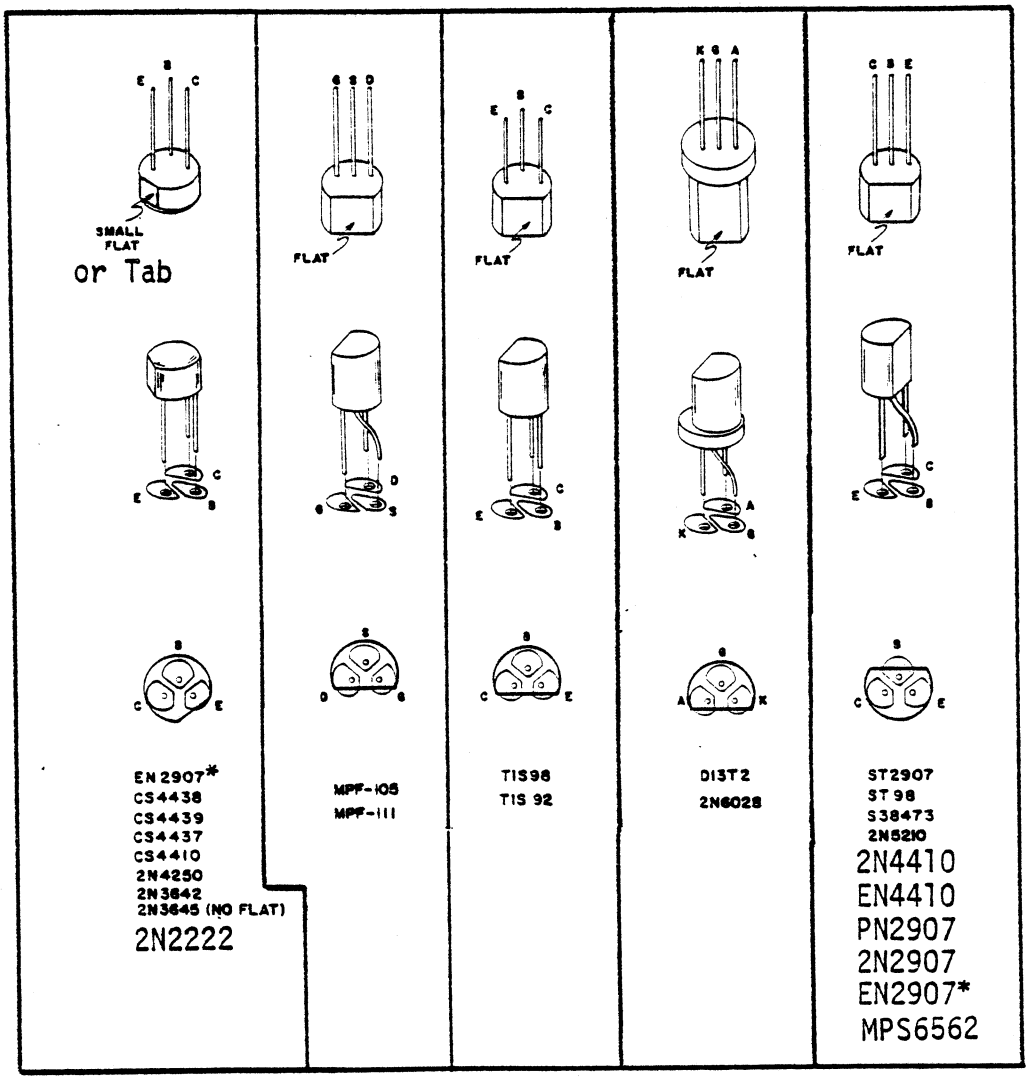
4-8. Transistor Identification

Figure 4-6 shows the outline of each type of transistor and the correct orientation for the three leads. Use this information to determine the correct orientation for each transistor.

A list of possible substitutions is given below. If transistors other than the ones shown below are used, damage may occur. When making substitutions, refer to Figure 4-6 to determine the correct orientation for the leads.

2N4410 = EN4410 = CS4410 = CS4437, CS4438, TIS98, ST98, S38473 (NPN)

EN2907 = 2N2907 = PN2907 = ST2907, CS4439 (PNP)



*Configuration of the leads on EN2907 may vary.

Figure 4-6. Transistor Identification

4-9. IC Installation Instructions

All ICs must be oriented so that pin 1 corresponds with the pad marked with an arrowhead. Refer to the IC identification chart in Paragraph 4-10 to identify pin 1. All ICs can be easily damaged and should be handled carefully. Always try to hold the IC by the ends, touching the pins as little as possible. When removing the IC from its holder, carefully straighten any bent pins with needle-nose pliers. All pins should be evenly spaced and should be aligned perpendicular to the body of the IC itself.

A. Installing ICs without sockets

1. Orient the IC so that pin 1 coincides with the arrowhead on the board.
2. Align the pins on one side of the IC so that just the tips are inserted into their holes.
3. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exert a little inward pressure, and try again. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all of the pins have been started into their holes, push the IC into the board the rest of the way, and secure with masking tape.
4. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges.
5. Clip off any excess lead lengths, and remove the masking tape.

B. Installing ICs with sockets

1. Refer to Figure 4-7, and orient the socket so that pin 1 coincides with the arrowhead on the board. Set the socket into its holes and secure with masking tape.

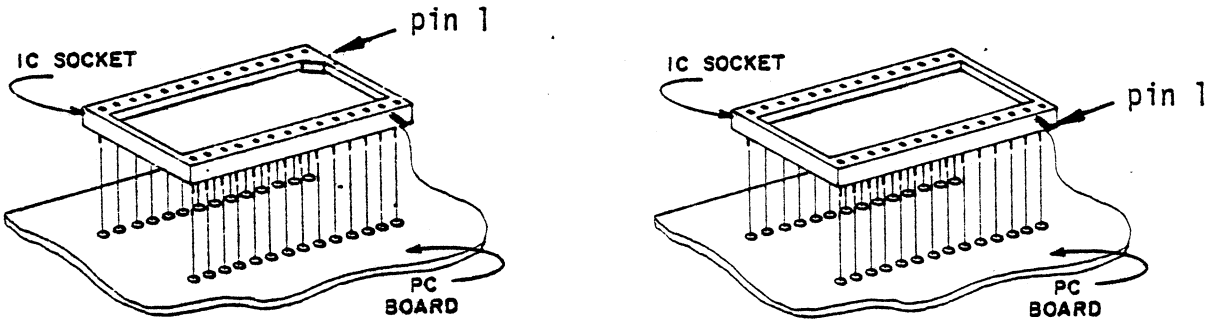


Figure 4-7. IC Socket Orientation

2. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges.
3. Clip off any excess lead lengths, and remove the masking tape.
4. Orient the IC over the socket so that pin 1 coincides with pin 1 on the socket.
5. Align the pins on one side of the socket so that just the tips are inserted into the holes.
6. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exert a little inward pressure, and try again. When the tips of all of the pins have been started into their holes, push the IC into the socket the rest of the way.

4-10. IC Identification

Integrated circuits (ICs) may have one, or a combination, of several different markings which are used to determine correct orientation. Refer to Figure 4-8 to locate pin 1 of the ICs. Pin 1 must be aligned with the arrowhead on the board, as shown in Figure 4-8a. The outlines shown in Figure 4-8a are silkscreened directly on the board.

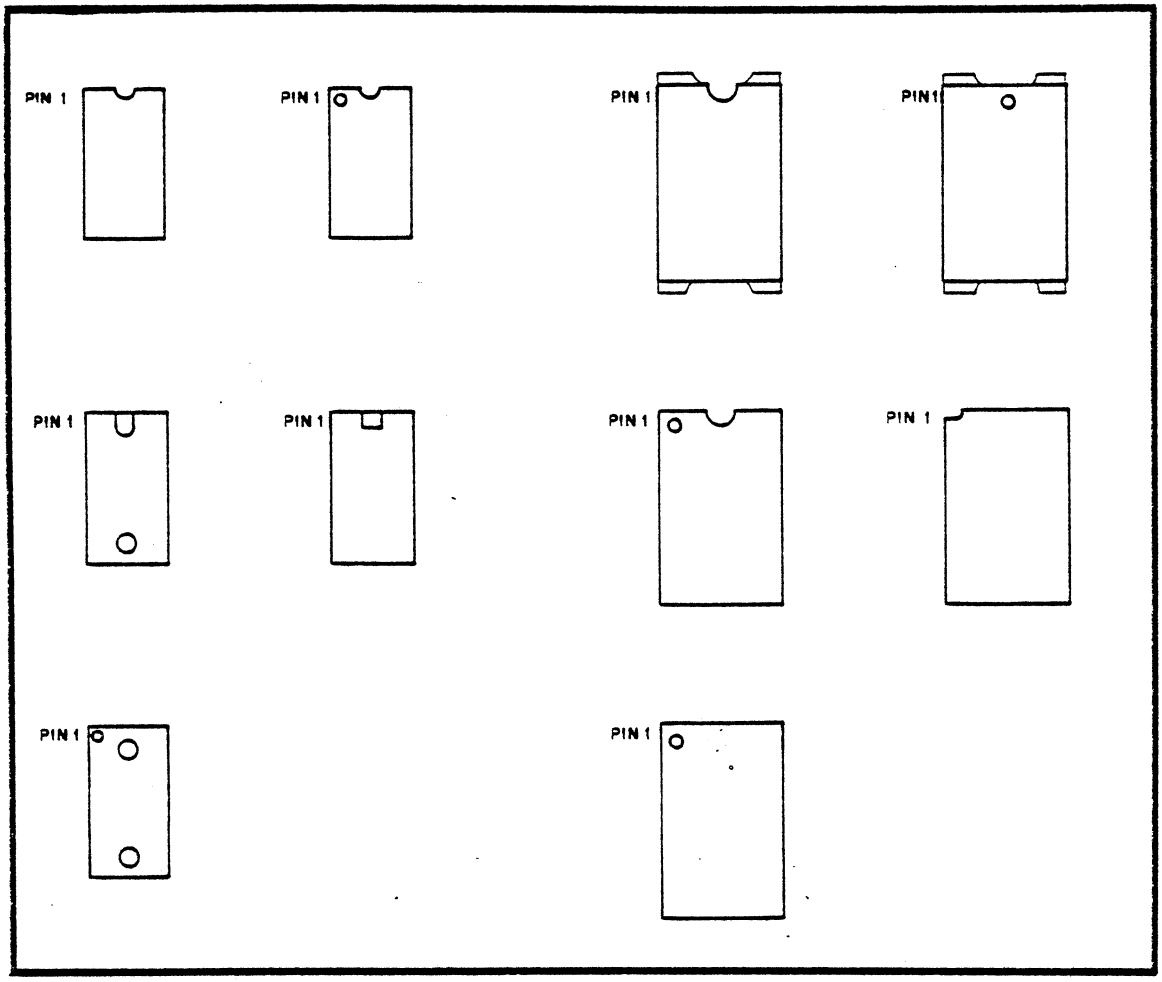


Figure 4-8. IC Identification

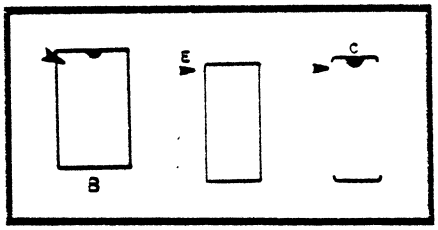


Figure 4-8a. IC Silkscreen Designations

4-11. DIODE INSTALLATION (Figure 4-9)

Install diode D15 (Bag 3) according to the following instructions.

1. Solder the 716 AG-2D socket pin onto the board in the cathode hole of D15.
2. Insert the anode lead of D15 into the silkscreened side of the board and solder to the foil pattern on the back of the board.
3. Clip the cathode lead so that it is 1/4 inch long.
4. Plug the lead into the socket pin.

Install the remaining diodes, D1 through D14 and D16 through D18 (Bag 3), according to the instructions in Paragraph 4-6.

Diode	Part Number
( ) D1 through D18	1N914

4-11. DIODE INSTALLATION (Figure 4-9)

Install diode D15 (Bag 3) according to the following instructions.

1. Solder the 716 AG-2D socket pin onto the board in the cathode hole of D15.
2. Insert the anode lead of D15 into the silkscreened side of the board and solder to the foil pattern on the back of the board.
3. Clip the cathode lead so that it is 1/4 inch long.
4. Plug the lead into the socket pin.

Install the remaining diodes, D1 through D14 and D16 through D18 (Bag 3), according to the instructions in Paragraph 4-6.

Diode	Part Number
( ) D1 through D18	1N914

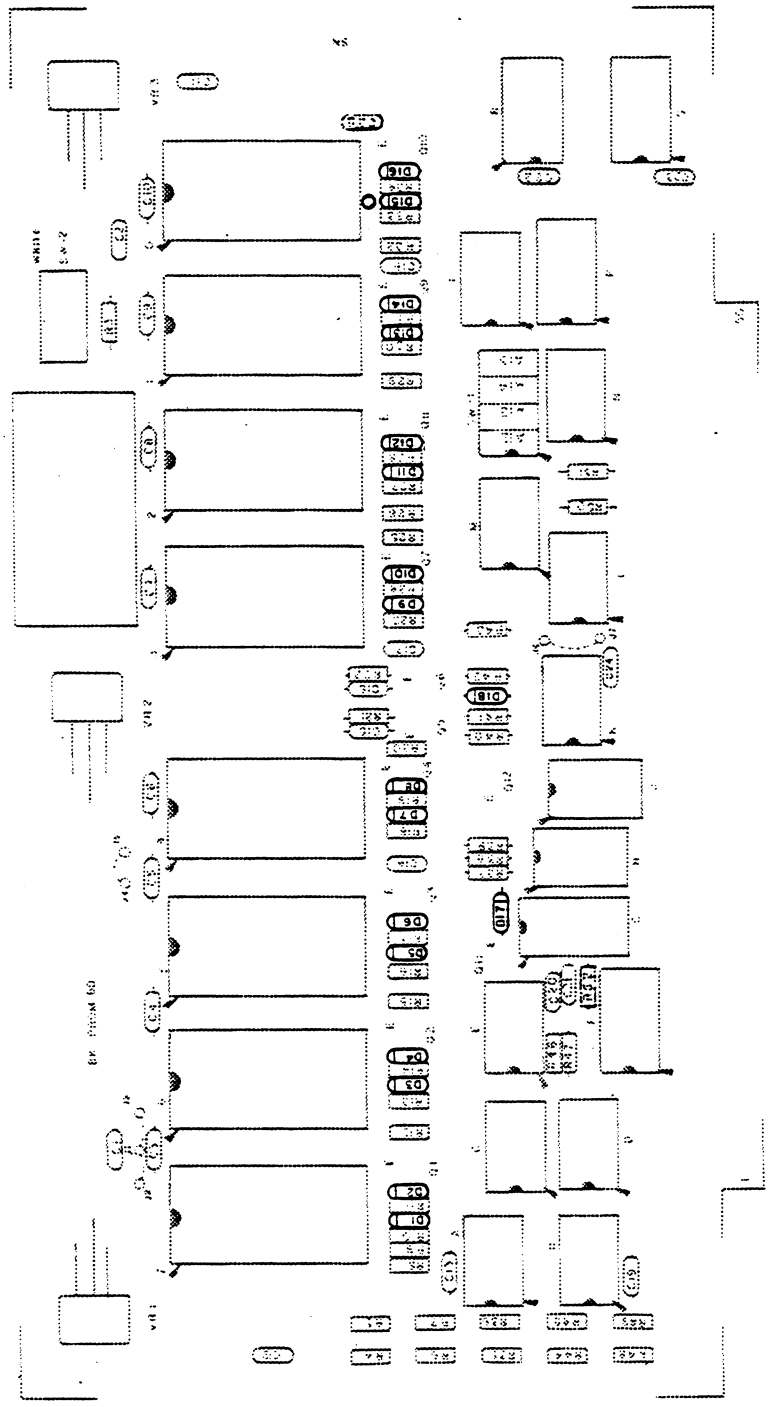


Figure 4-9. Diode Installation

4-12. RESISTOR INSTALLATION (Figure 4-10)

Install the following 47 resistors (Bag 1) according to the instructions in Paragraph 4-4.

Resistor	Value
( ) R4, R5, R6, R7, R35, R36, R41, R42, R44, R45, R48, R49	1K ohm (brown, black, red) 1/4W
( ) R8, R12, R15, R20, R25, R26, R29, R32	10K ohm (solid gray) 1/4W
( ) R10, R13, R16, R18, R23, R27, R30, R33, R37, R38, R43, R51	4.7K ohm (yellow, violet, red) 1/4W
( ) R11, R14, R17, R19, R24, R28, R31, R34	15K ohm (brown, green, orange) 1/4W
( ) R21, R22, R40	3K ohm (orange, black, red) 1/4W
( ) R46	27K ohm (red, violet, orange) 1/4W
( ) R47	47K ohm (yellow, violet, orange) 1/4W
( ) R50	68 ohm (blue, gray, black) 1/4W
( ) R52	470 ohm (yellow, violet, brown) 1/4W

NOTE

Resistors R3, R9 and R39 are optional (see Paragraph 2-11).

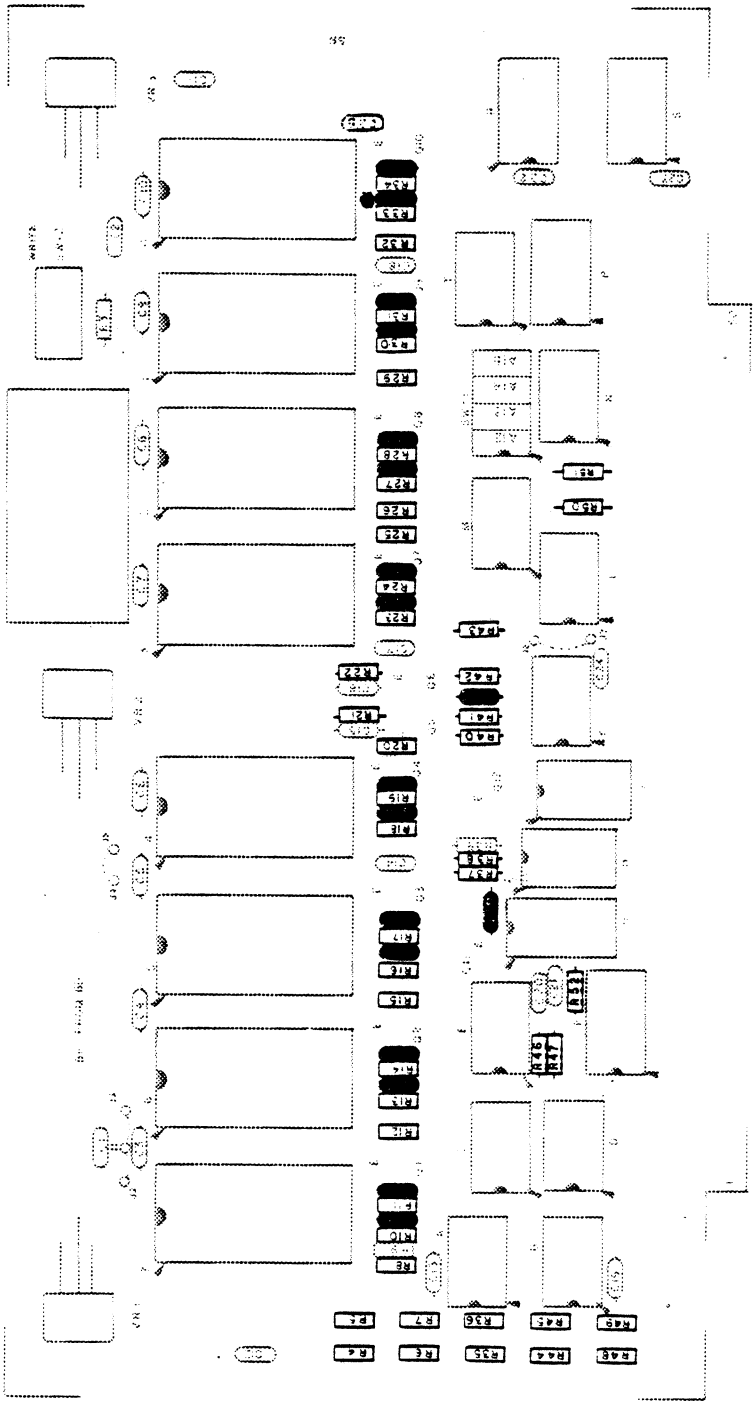


Figure 4-10. Resistor Installation

4-13. TRANSISTOR INSTALLATION (Figure 4-11)

Install transistors Q1 through Q12 (Bag 3) according to the instructions in Paragraph 4-7.

Transistor	Part Number
( ) Q1, Q2, Q3, Q4, Q7, Q8, Q9, Q10, Q11, Q12	2N2222
( ) Q5, Q6	MPS 6562

4-13. TRANSISTOR INSTALLATION (Figure 4-11)

Install transistors Q1 through Q12 (Bag 3) according to the instructions in Paragraph 4-7.

Transistor	Part Number
( ) Q1, Q2, Q3, Q4, Q7, Q8, Q9, Q10, Q11, Q12	2N2222
( ) Q5, Q6	MPS 6562

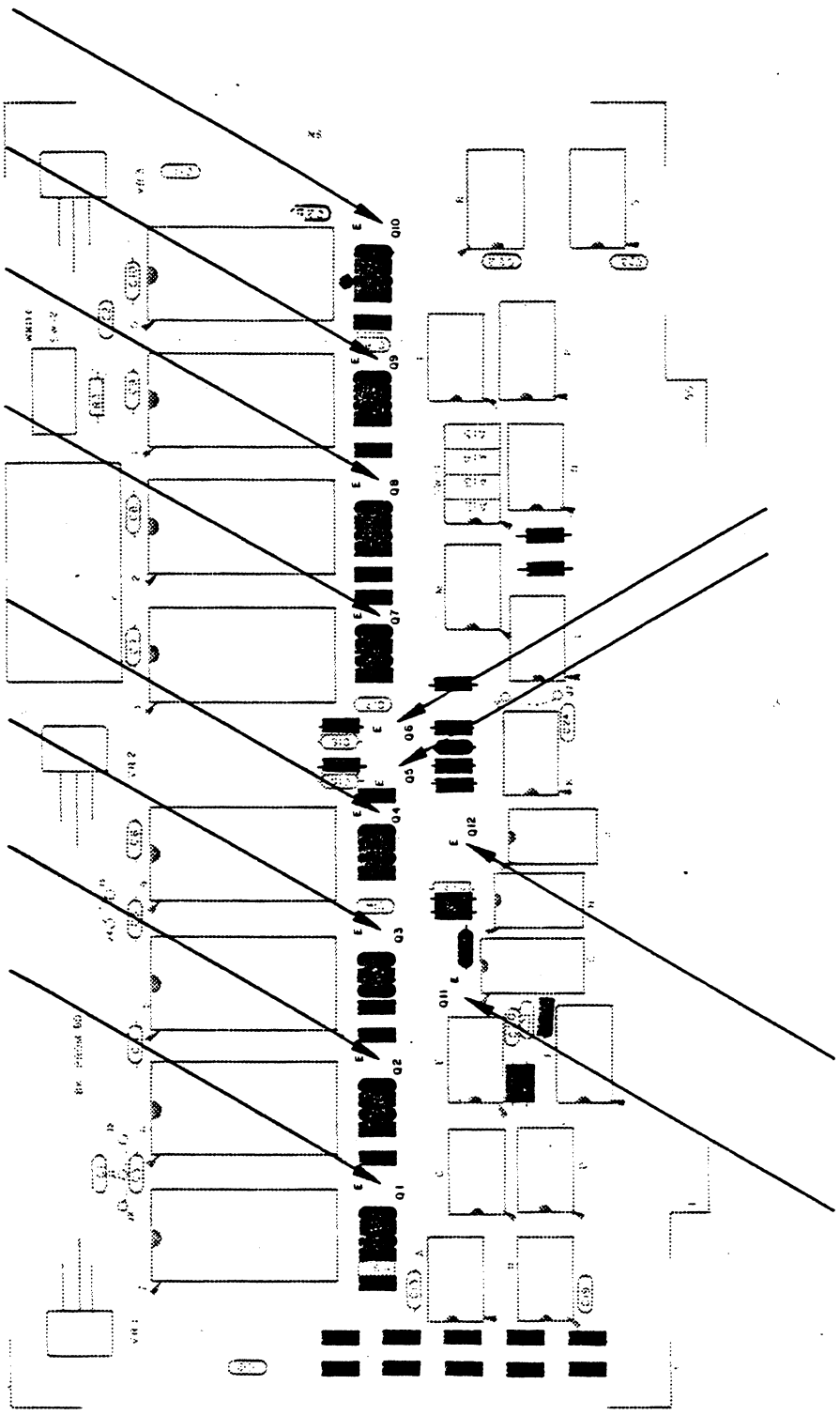


Figure 4-11. Transistor Installation

4-14. IC SOCKET INSTALLATION (Figure 4-12)

Install EPROM sockets 0 through 7 (Bag 4) according to the instructions in Paragraph 4-9, Section B, Steps 1, 2 and 3. Install the optional EPROM ICs according to the instructions in Paragraph 4-9, Section B, Steps 4, 5 and 6.

Silkscreen Designation	Socket Size
( ) EPROM sockets 0 through 7	28-pin

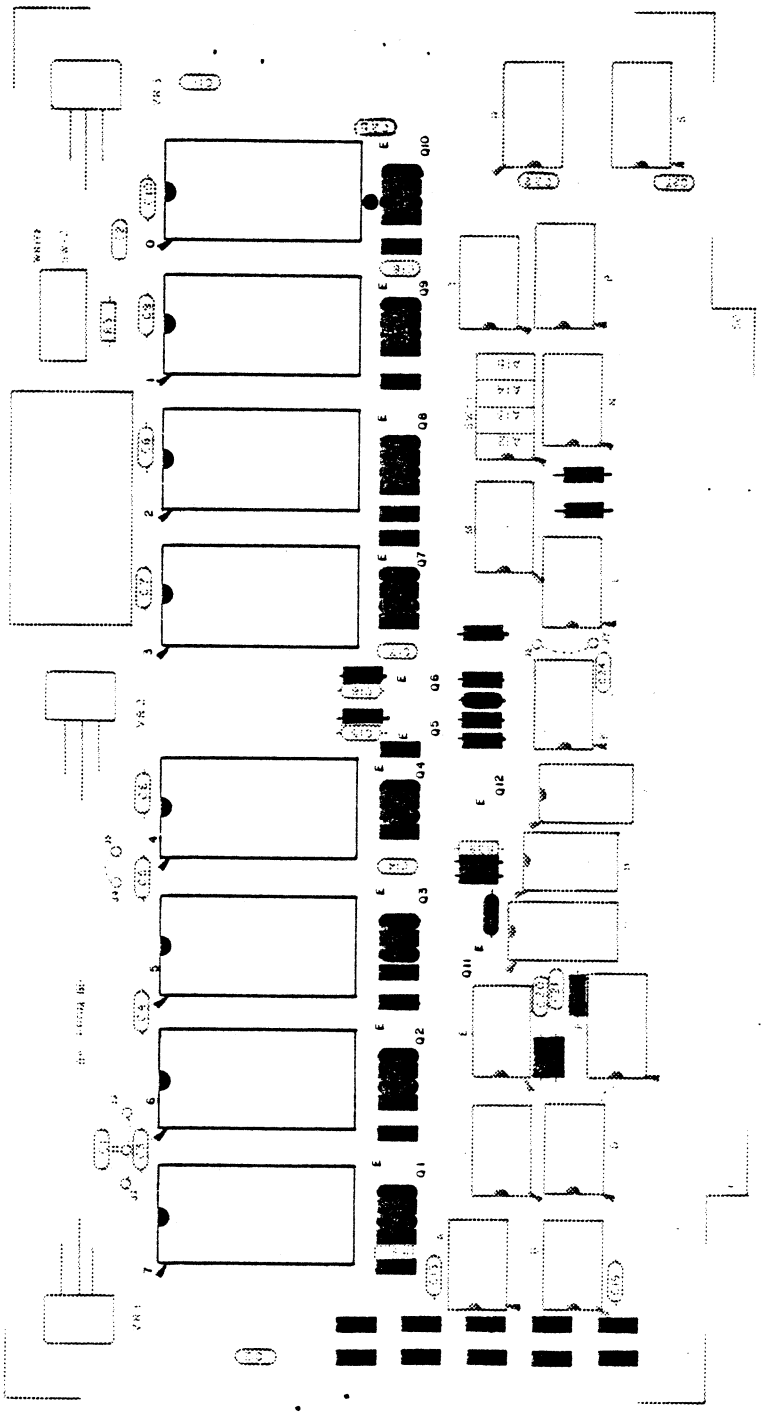


Figure 4-12. IC Socket Installation

4-15. CAPACITOR INSTALLATION (Figure 4-13)

Install capacitors C1 through C25 (Bag 1) according to the instructions in Paragraph 4-5.

Capacitor	Value
( ) C1, C2	22µf, 35v, dipped tantalum
( ) C3, C4, C5, C6, C7, C8, C9, C10, C13, C14, C15, C17, C18, C19, C21, C22, C23	.1µf, 16v, ceramic disk
( ) C11, C12, C20, C24, C25	.001µf, 16v, dipped ceramic
( ) C16	10µf, 16v, dipped tantalum

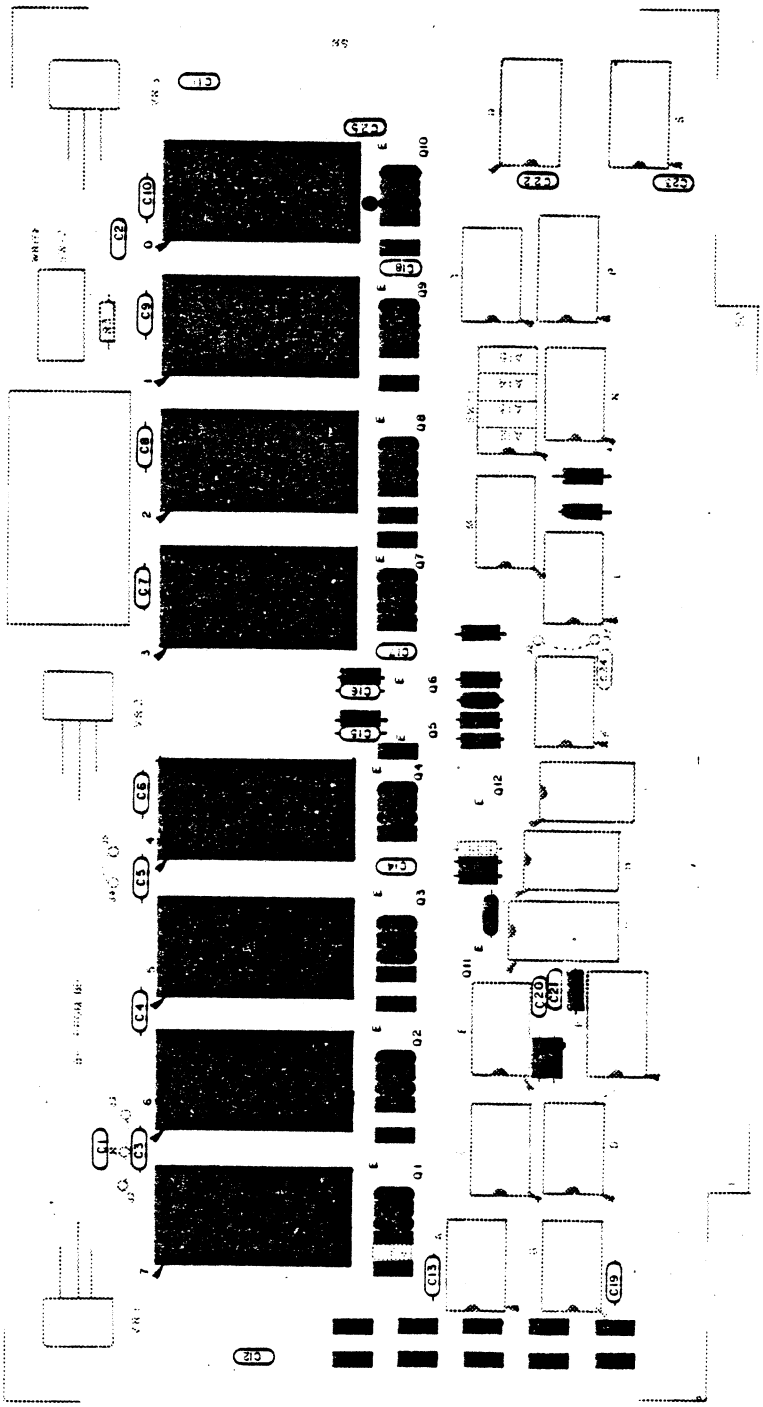


Figure 4-13. Capacitor Installation

4-16. IC INSTALLATION (Figure 4-14)

Install the following 17 ICs (Bag 5) according to the instructions in Paragraph 4-9, Section A.

Silkscreen Designation	Part Number
( ) A, C, E	7406
( ) B, D, T	7402
( ) F	7442
( ) G	74123
( ) H	7474
( ) J, N	7404
( ) K	7403
( ) L	7400
( ) M	7420
( ) P, R, S	74367

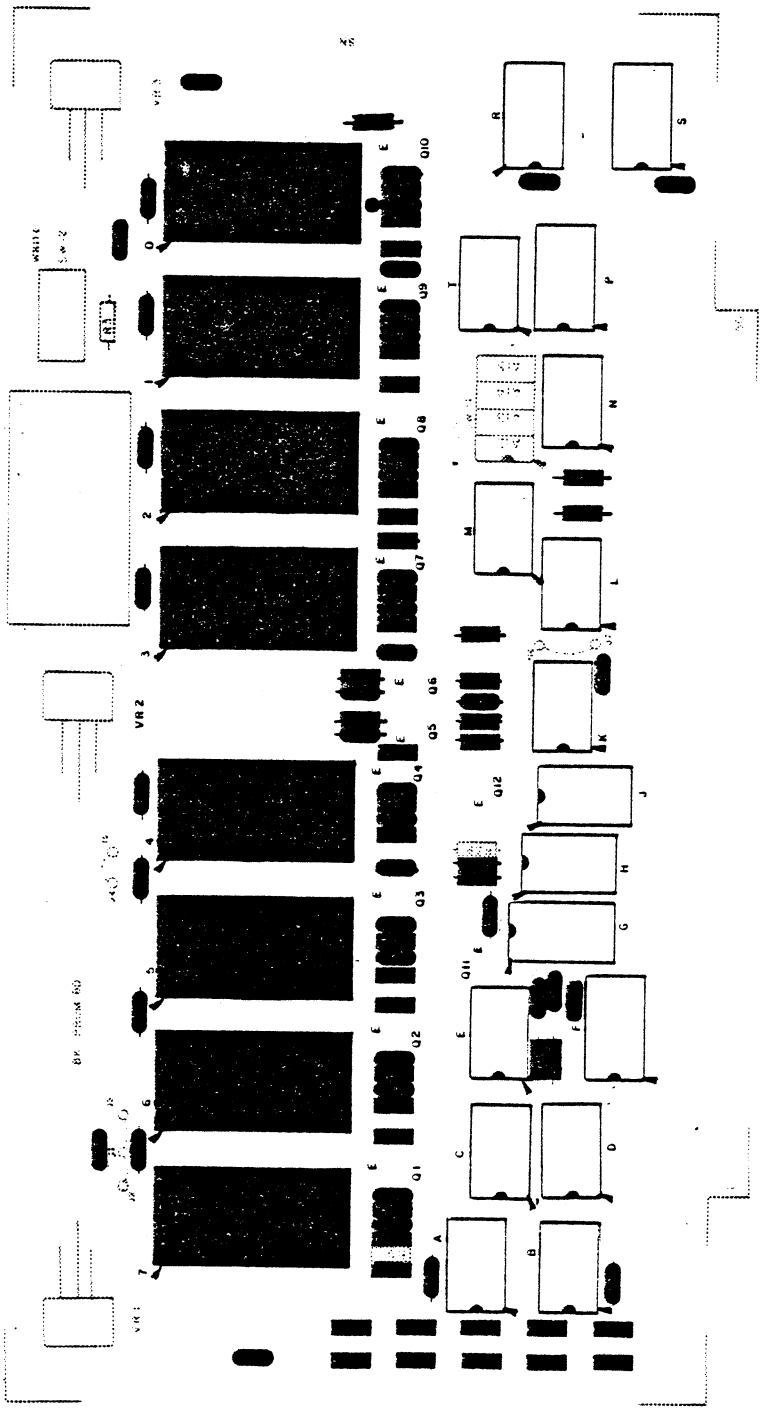


Figure 4-14. IC Installation

4-17. VOLTAGE REGULATOR INSTALLATION (Figures 4-15 and 4-15a)

Install voltage regulators VR1 through VR3 with heat sinks (Bag 2) according to the following instructions.

1. Set the regulator in place on the silkscreened side of the board, aligning the leads with their designated holes.
2. Use needle-nose pliers to bend each lead at a right angle to conform to its proper hole on the board.

> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all metal surfaces that come into contact with each other.

3. Referring to Figures 4-15a and 4-15, set the regulator and heat sink in place on the silkscreened side of the board, and secure with a #6-32 x 3/8 inch screw and a #6-32 nut.
4. Solder the three leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges.
5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1	7805
( ) VR2	7812
( ) VR3	7905

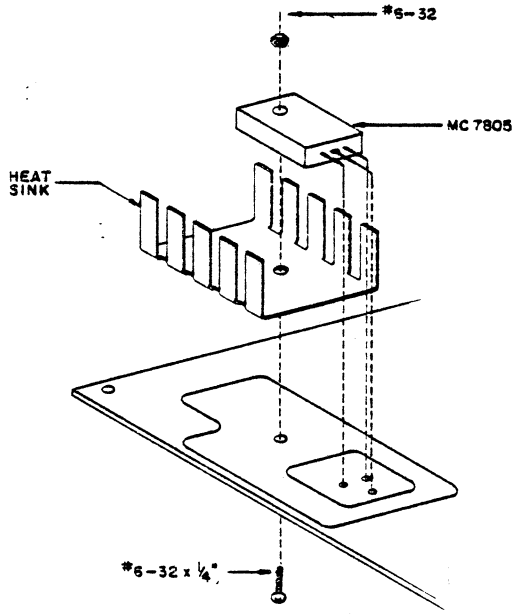


Figure 4-15a.
Voltage Regulator Orientation

4-18. SWITCH INSTALLATION (Figures 4-15 and 4-15b)

Install SW1 (Bag 3) according to the following instructions.

1. Orient SW1 so that the numbers 1,2,3,4 are towards the top of the board.
2. Insert the leads into the silkscreened side of the board, and secure with masking tape.
3. Solder each lead to the foil pattern on the back of the board. Be sure not to leave any solder bridges.
4. Clip off any excess lead lengths, and remove the masking tape.

Install SW2 (Bag 3) according to the following instructions.

1. Referring to Figure 4-15b, orient the switch over the silk-screened side of the board.
2. Insert all 10 leads into their holes, and secure with masking tape.
3. Solder each lead to the foil pattern on the back of the board. Be sure not to leave any solder bridges.
4. Clip off any excess lead lengths, and remove the masking tape.

Switch	Part Number
( ) SW1	CTS 206-124
( ) SW2	MSS-2250R

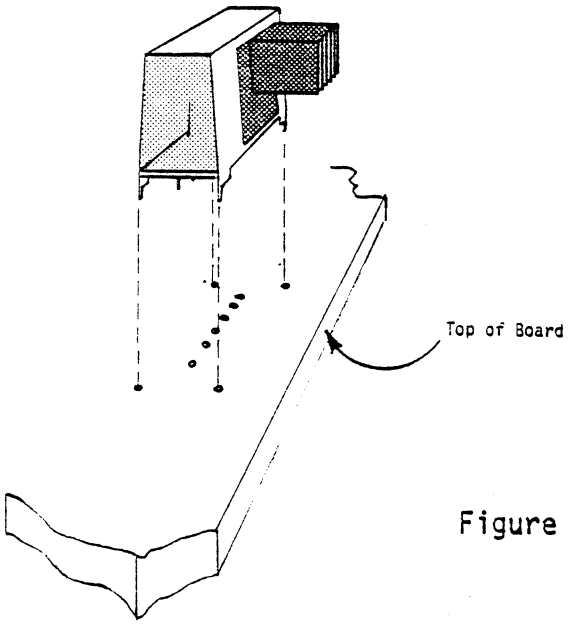


Figure 4-15b. Switch Orientation

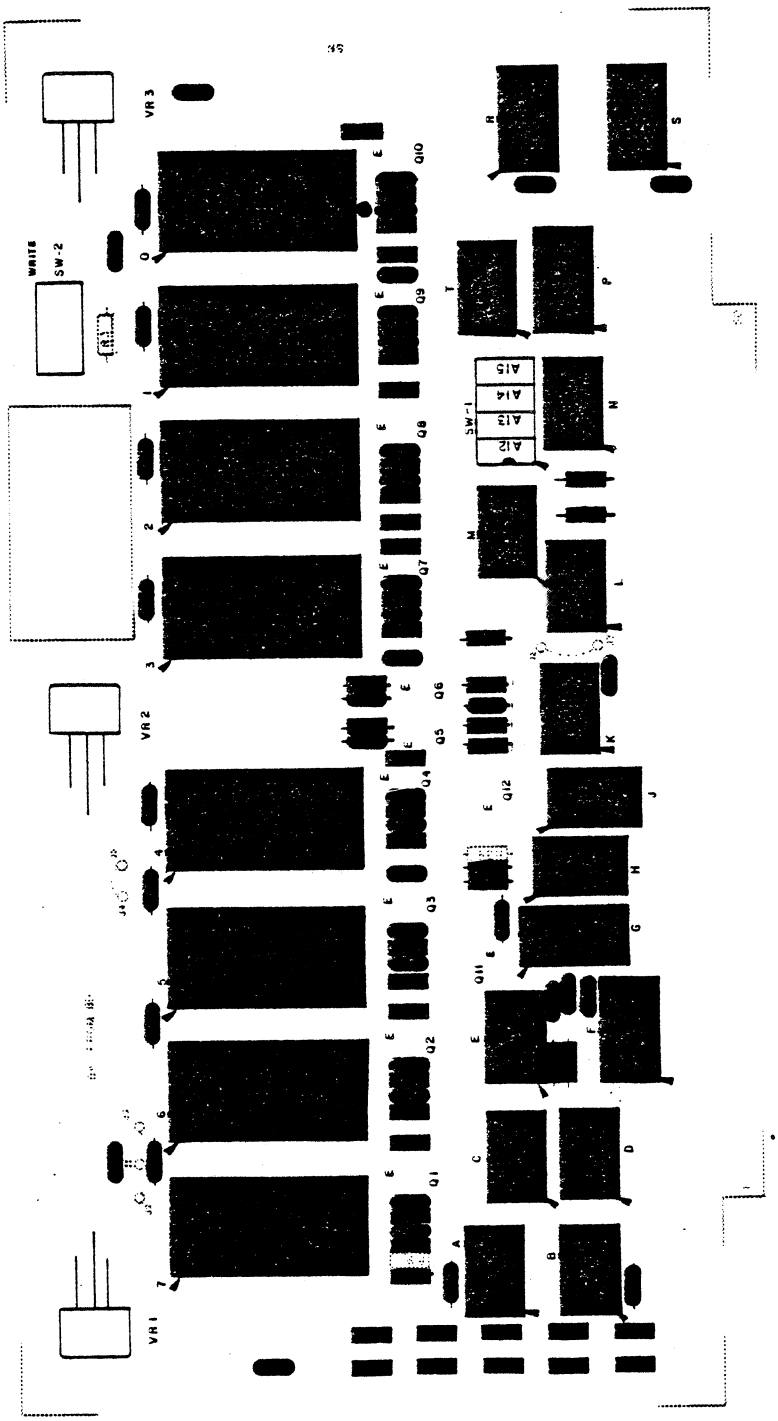


Figure 4-15. Voltage Regulator and Switch Installation

4-19. JUMPER INSTALLATION (Figure 4-16)

Refer to the Power Supply Schematic, Figure 3-2 (sheet 1 of 2) and Paragraph 2-11 for jumper options. Use the length of jumper wire (Bag 4) included in the kit to make the connections.

4-20. POWER SUPPLY MODULE INSTALLATION (Figures 4-16 and 4-16a)

Install the power supply module, VS1 (Bag 4), according to the following instructions.

1. Referring to Figure 4-16a, orient VS1 over its proper holes on the silkscreened side of the board.
2. Insert the four leads into the board and solder to the foil pattern on the back of the board.
3. Clip off any excess lead lengths.

( ) VS1

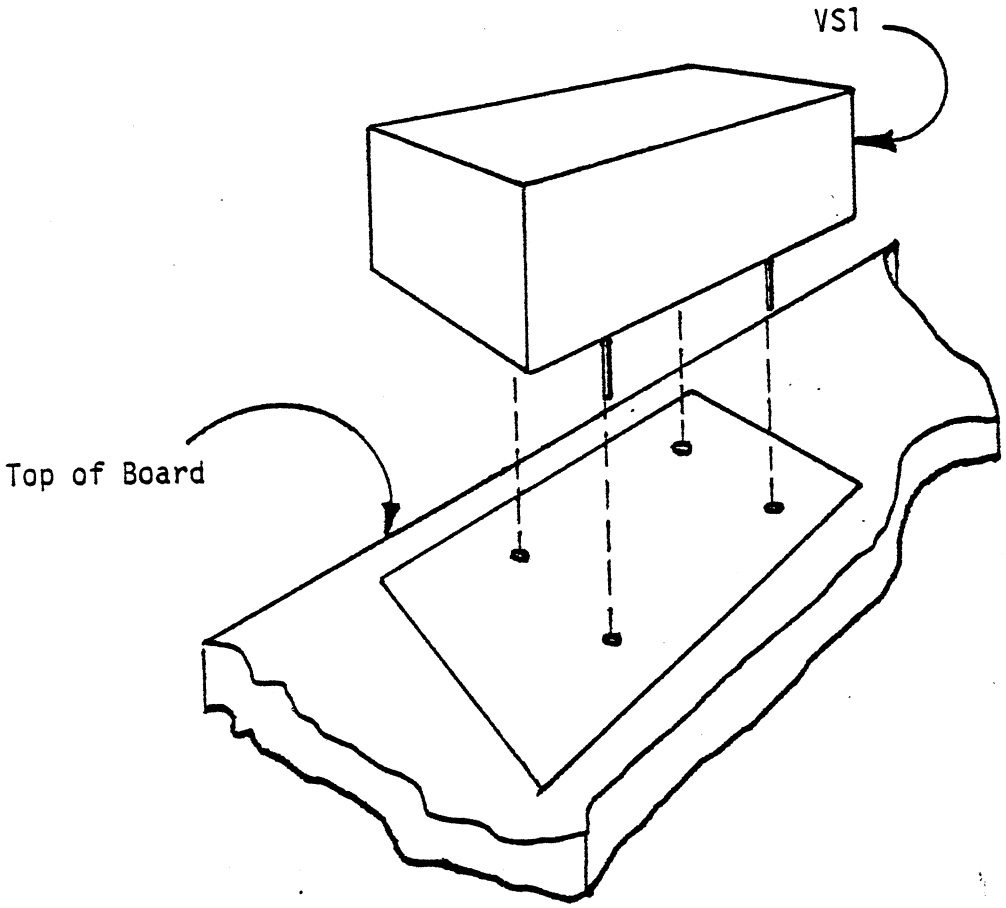


Figure 4-16a.
Power Supply Module Orientation

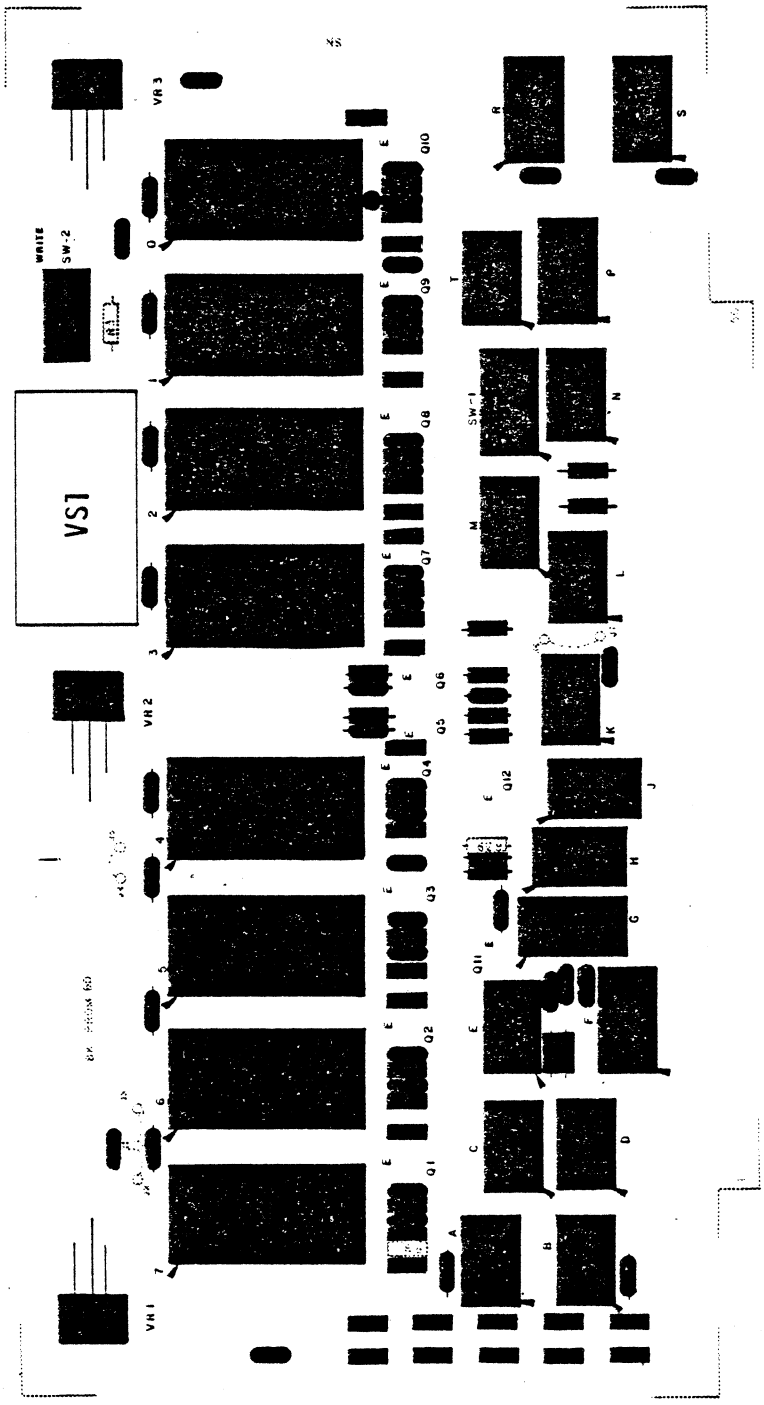


Figure 4-16. Jumper and Power Supply Module Installation

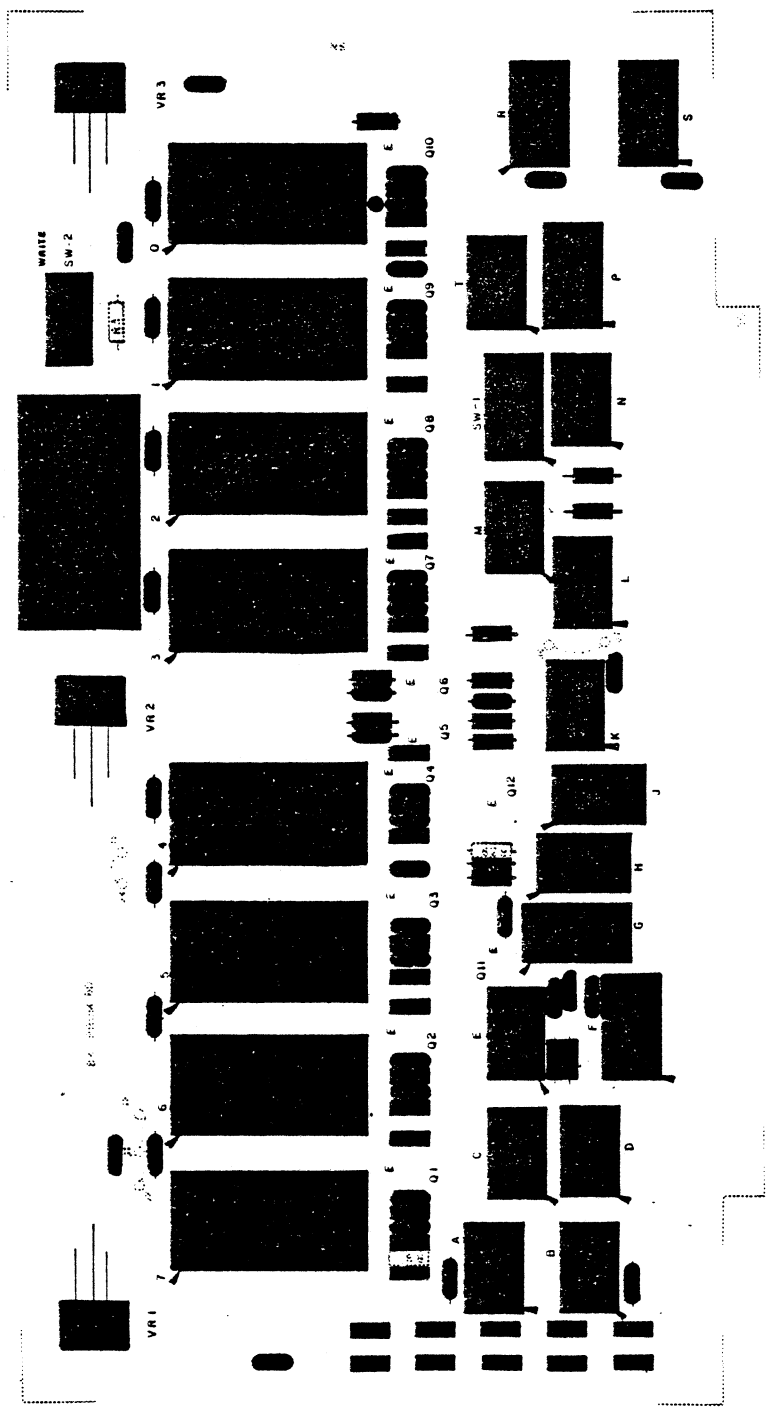


Figure 4-17. Completed Board Assembly

4-21. INSTALLATION OF BOARD INTO MAINFRAME

1. Before installing the 88-PMC8 board, check the board for solder shorts, open lands and missing components.
2. Remove the four #6-32 x 3/8 inch screws (two on each side) from the computer case, and slide the case bottom forward so that the bottom of the motherboard is exposed.
3. Insert the 100-pin edge connector into the motherboard so that pin 1 is in the lower right position (when you are looking at the front of the computer).
4. Solder each pin to the bottom of the motherboard. Be careful not to leave any solder bridges. Clip off any excess lead lengths.
5. Slide the board down through the card guides, and insert the card stab connector into the edge connector so that the silk-screened side of the board is towards the right side of the computer.
6. Slide the case bottom back into place, and replace the four #6-32 x 3/8 inch screws.

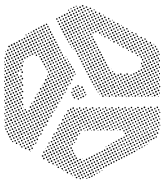
4-22. BURN-IN PROCEDURE

When assembly of the 88-PMC8 board has been completed, we recommend that a "burn-in" procedure be performed to uncover possible malfunctions that may occur at this time. After the board has been installed, turn the unit on, and set the case top in place. Leave the computer on for a period of 48 to 100 hours. If problems are encountered, refer to the Troubleshooting section of the 88-PMC8 manual.

appendix A
parts list

Bag #	Quantity	Component	MITS Part #
1	1	68 ohm, 1/4W resistor	101913
	12	1K ohm, 1/4W resistor	101903
	3	3K ohm, 1/4W resistor	101981
	12	4.7K ohm, 1/4W resistor	101912
	8	10K ohm, 1/4W resistor	101905
	8	15K ohm, 1/4W resistor	101979
	1	27K ohm, 1/4W resistor	101907
	1	47K ohm, 1/4W resistor	101914
	1	470 ohm, 1/4W resistor	101902
	1	10µf, 16v dipped tantalum capacitor	100394
	2	22µf, 35v dipped tantalum capacitor	100393
	17	.1µf, 16v ceramic disk capacitor	100327
	5	.001µf, 16v dipped tantalum capacitor	100385
2	3	heat sink	101667
	3	#6-32 x 3/8" screw	100925
	3	#6-32 hex nut	100933
	1	7805, 5v voltage regulator	101074
	1	7812, 12v voltage regulator	101085
	1	7905, -5v voltage regulator	101146
	2	MPS 6562 transistor (PNP)	102828
	10	2N2222 transistor (NPN)	102822
	18	1N914 diode	100705
3	1	CTS 206-124 dip switch	102321
	1	MSS 2250R slide switch	102328
	8	28-pin socket	102124
	6"	jumper wire	103083
	1	27v power supply module	101419
	1	716 AG-2D socket pin	102515

Bag #	Quantity	Component	MITS Part #
4	2	7404 integrated circuit	101022
	1	7403 integrated circuit	101014
	3	7402 integrated circuit	101021
	1	7400 integrated circuit	101020
	1	7420 integrated circuit	101038
	1	7474 integrated circuit	101152
	3	74367 integrated circuit	101040
	1	7442 integrated circuit	101145
	1	74123 integrated circuit	101060
	3	7406 integrated circuit	101054
Misc.	1	88-PMC8 printed circuit board	100230
	1	Theory of Operation, Trouble-shooting and Assembly Manual	102705



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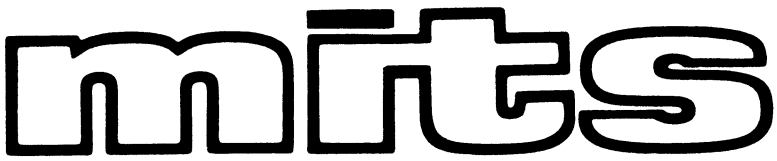

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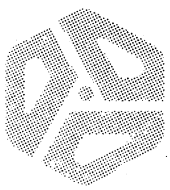

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November 1977

1. INTRODUCTION

WR is a program which performs the following functions:

Transferring data from any location in PROM board to any location in RAM

Programming any PROM location on the PMC8 board with data from any other location in PROM

Programming any PROM location on the PMC8 board with data from any location in RAM.

WR is supplied as a programmed PROM to be mounted on the 88-PMC8 board. The WR PROM is fully relocatable. That is, it may be placed at any address as long as the starting address of the program is an even multiple of 256 bytes. The program may be transferred from PROM to RAM and run out of RAM, as well.

2. OPERATION

Before attempting to start the WR program, make sure the Write switch on the PMC8 board programmer is off. This will help prevent inadvertant damage to the PROMs or the programmer circuitry.

To run WR with the full front panel 8800 computer, use the following procedure:

1) Examine the first location of the WR program. This is done by setting the address switches on the front panel to the starting address and actuating the EXAMINE switch.
2) Set the sense switches for the terminal interface device. The WR PROM supports only the 2SIO and SIO interface boards which have the following sense switch settings.

   2SIO all switches down (must be addressed at 020_8)

   SIO A13 up, the rest down (must be addressed at 000_8)

3) Depress the RUN switch on the front panel.

To run WR with the 8800b Turnkey computer and the Turnkey Monitor PROM, use the following procedure:

1) Make sure the sense switches on the Turnkey Module have been set properly.
2) Set the RUN/STOP switch to RUN and then actuate START.
3) When the Turnkey Monitor prints its prompt period, type J and the starting address of the WR program.

4) When WR starts, it initiates the following dialog with the user. First the computer prints

ENTER STACK LOCATION?

The user responds with the first address of a six byte area in RAM that WR can use for its stack. This area may be anywhere in RAM that the user chooses, except for the first six bytes. The address must be entered in octal and followed by a return (denoted <cr>).

Now WR asks

WHERE TO TRANSFER?

to which the user responds with the octal address of the first location of the destination area. This address, like all of the other responses in the dialog, is followed by a <cr>.

WR determines the locations of the data to be transferred by asking

FIRST LOCATION TO TRANSFER?

and

LAST LOCATION TO TRANSFER?

In each case, the user answers with the appropriate octal address and a <cr>.

In case an error is made in entering any of these addresses, STOP the computer and go back to step 1. WR ignores any non-octal characters in the input string, so such mistakes may be corrected simply by typing the correct octal digit.

Finally, WR asks

PROGRAM OR TRANSFER?

To transfer information from PROM to RAM, simply type a <cr>. To program a PROM, type T, turn on the Write switch on the programmer and then type the <cr>.

WR takes approximately 15 minutes to program 8K bytes of PROM. When it is finished, it reads the newly programmed PROM to verify the information. The process of transferring information from PROM to RAM is the same except that it is much faster. After the verification cycle, WR prints one of the following messages:

VERIFICATION COMPLETED -- NO ERRORS DETECTED

or

ERROR DETECTED -- VERIFICATION NOT COMPLETED.

The verification process stops as soon as the first error is detected. To locate this error, STOP the computer, turn off the Write switch and go back to step one. This time, divide the range of addresses to be transferred in half and specify 'transfer' instead of 'program.' This causes the program to verify the first half of the intended programming data quickly. If the error is not detected again, go back to step one and try the other half. If the error is detected again, repeat the procedure, dividing the range of addresses in half once again. In this way, the error can be isolated quickly to the chip level.