altair™ 8800
ANALOG CONVERSION SYSTEM
ANALOG TO
DIGITAL CONVERTER (88-ADC)
MULTIPLEXER (88-MUX)

mits

M E M O R A N D U M

TO: Marketing, Testing and Production

SUBJECT: 88-ADC and 88-MUX System

FROM: Engineering

DATE: 1/19/77

The following items should be noted for future reference concerning ordering,
shipping and technical advice for these cards:

1. An A/D system is one of two basic types:
    Type 1. -- 8 Channel
    Type 2. -- 24 Channel

2. An 88-ADC card ordered without 88-MUX will be shipped with cable assembly
    #8810-301. (System Type 1)

3. An 88-ADC card ordered in conjunction with an 88-MUX (Type 2 system) will be
    shipped with cable assembly #8810-302. If additional 88-MUX cards are ordered
    for other systems, an additional cable assembly will be shipped for each additional
    MUX card. If more than one 88-MUX is ordered to be used within the same system,
    88-MUX option #2 below must be specified.

4. If an 88-MUX is ordered for a previously purchased 88-ADC and will be the only
    88-MUX in the system, it will be shipped with cable assembly #8810-302.
    NOTE: If additional 88-MUX cards are ordered to be used with an already
           existing 88-MUX card, the old cable assembly must be returned and
           re-worked.

5. Additional options are listed below:

           Contact Engineering on all options before making a quote!!!!

88-ADC Option #1: Differential instrumentation amplifier (AD 521). --- $25 Extra
                   (Useful in noisy environments and small signal applications)
88-MUX Option #1: Differential inputs to amplifiers + special cable. -- $15 Extra
                   (Useful in noisy environments)
88-MUX Option #2: Required by all systems using more than one 88-MUX. -- $15 Extra
                   Special Cable Assembly

Quote 60 Days Delivery on all Options

88-ADC   OPTION #1

(Differential Configuration)

The AD 521 should be implemented as follows:
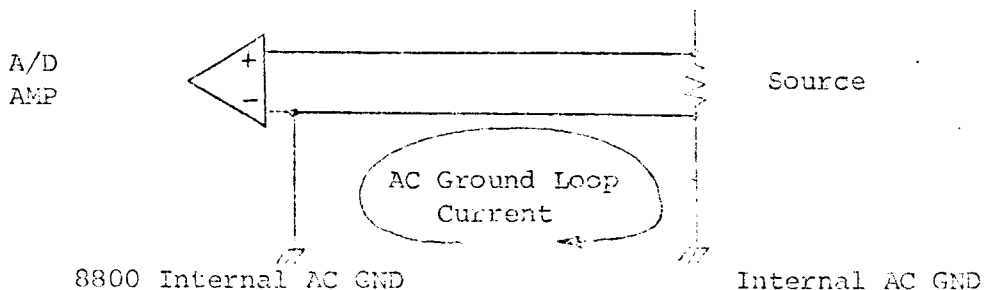
1. Drill out drill hole (D2).   (D2) is a <u>square</u> pad directly beneath R6 on the board.   This isolates input pin 3 of the amplifier from ground. (Use a #61 drill)

2. Remove the 741 (B) and insert the AD 521 (C).

3. If resistor (R3) is present, remove it.   (Note that scaling and/or filtering are not offered in differential configuration)

4. If the (4051) MUX IC (U) is present, remove it.

5. Select gain desired according to:

GAIN	R7
1	100K ohm *≈ 0.9K*
10	10K ohm
100	1K ohm
1000	100 ohm

R8 = 100K ohm

Use precision resistors and solder R7 and R8 into the board.

6. A suitable cable may be made by using 2 conductor shielded wire.   One conductor goes to PI-2 and the other, PI-4.   The shield should go to PI-1.

7. If AC ground loops are present, erratic results may be obtained especially in high gain or lowlevel signal applications.. Try ungrounding the shield or tying the shield first to one side, then the other differential input line.


```
A/D                    +                              Source
AMP                    −
                       
                 AC Ground Loop
                     Current
   8800 Internal AC GND              Internal AC GND
```

If some form of internal AC ground path is inavertently supplied at the A/D (−) terminal the signal seen by the (+) amplifier terminal will vary according to changing current in the ground loop.   Thus output of the amplifier will reflect this variation <u>multiplied by the gain factor</u>!

8. At high gains, noise may be improved by adding a 1K ohm resistor in series with PI-Pin 4 and the AD521 - Pin 3.   Also tack a 47 pf capacitor between Pins 1 and 3 of the amplifier, keeping all leads as short as possible.

(Differential Configuration)

To modify an 88-MUX, perform the following steps:

1. Drill out all drill holes in ground lines of PC Card. Refering to the PC card layout there are (24) lands with double feed thru holes near the top of the card. The bottom feedthru of each land should be drilled out with a #61 bit (.039"). Care should be taken not to break the land away from the top feedthru yet insure the entire removal of the plating-thru the card on the bottom hole.

2. For amplifier #1, gain is determined by the formula:

$$\text{Gain Factor} = \frac{R4}{R1} \text{ where } R4 = R3 \text{ and } R2 = R1.$$

Choose $R4 \leqq 1$ meg ohm for optimum noise and frequency response. Use of precision resistors is recommended for R1 - R4. Note also that for amplifier #2, R6-R9 replace R1-R4, respectively, and so on for all 24 circuits. Note that scaling and filtering is not possible in differential mode.

3. A differential-type special cable must be used for each 88-MUX with differential option. (Assy. #8810-303)

88-MUX   OPTION #2

(For conversion from single to multiple 88-MUX systems.)

1. Each 88-MUX requires one cable assy. #8810-302 (Assy # 8810-303 if differential MUX Option #1).

2. Remove the connection to Pin #1 at the 100 pin edge connector end and reconnect to Pin #5. The ten wires going to the 20 pin Molex connector should be cut off all cables except for one cable which will interface the 88-ADC.

   NOTE: It may be necessary to remove the connection at Pin A, strip back the wire, and reconnect Pin A. Use care not to short the shield wire to any other pins.

3. Connect a short length of wire from Pin 16 on one edge connector to Pin 16 on the next connector thus tying Pin 16 on all MUX edge connectors together via a "daisy-chain".

4. In a similar manner daisy-chain Pin 17, 18, 20, X, V, U and T on all edge connectors.

5. In a similar manner daisy-chain Pin 5 across all edge connectors. If desired, use a short piece of shielded cable and tie the shield ends to Pin A at each connector. Be careful not to short any pins with the exposed shield.

ili intech CMI function modules

168-12QZ
Analog-to-Digital Converter

DESCRIPTION

The 168-12QZ Analog-to-Digital Converter is designed for accurate and reliable performance with adjustment-free but versatile operation, at low cost. An improved form of the successive-approximation technique of conversion is used to convert unipolar input voltages (0 to +5 V, 0 to +10 V) or bipolar input voltages (±5 V, or ±10 V) to corresponding digital output codes of straight binary, offset binary or two's complement binary. The successive-approximation technique compares the analog input with the output of a D/A converter that tests each bit successively (MSB first) until the D/A output is equal to the analog input, within the quantizing error.

Versatility and convenience of operation are key features of the 168-12QZ. Based on the unprecedented circuit design of the 170/171 family, these converters are completely self-contained, low-profile modules that include a precision D/A converter, high-speed voltage comparator, precision temperature compensated reference network, clock, counter and latch circuitry. They are designed for user flexibility. By varying external pin connections, four different analog input ranges and three different types of digital output codes can be obtained. Both BUSY and it's complement are provided to allow synchronization with other external components: such as output storage latches, sample/hold amplifiers, or multiplexers.

With this pin-compatible and function compatible converter, Intech/Function Modules takes the worry out of single sourcing.

FEATURES

- 12-Bit Resolution and Accuracy
- No Missing Codes from 0 to +70°C
- 40 μs Conversion Time
- DTL/TTL Logic Levels
- Versatile Configurations
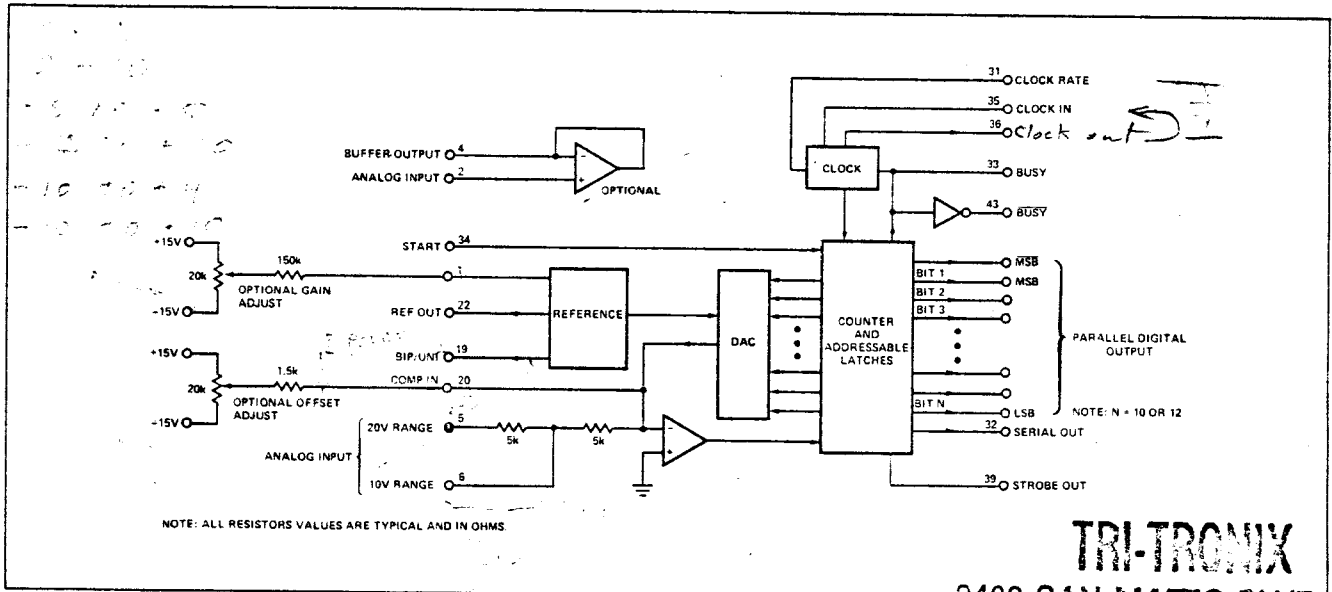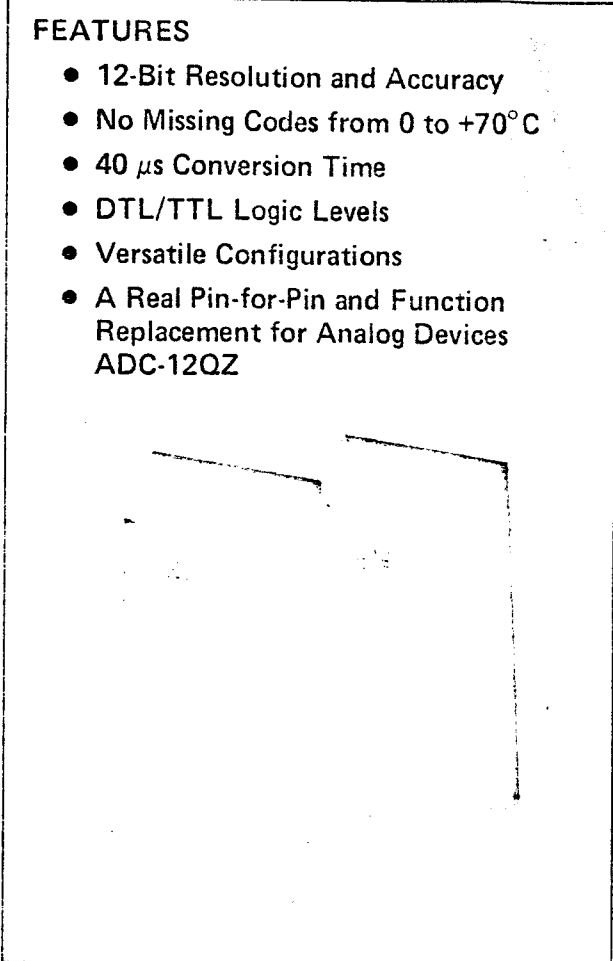- A Real Pin-for-Pin and Function Replacement for Analog Devices ADC-12QZ

Figure 1. Function Block Diagram

TRI-TRONIX

ELECTRICAL SPECIFICATIONS (Typical @ 25°C and ±15 V Supply)

Parameter		168-12QZ	Unit
RESOLUTION, Binary		12	bits
ACCURACY			
Quantizing Error		±½	LSB
Nonlinearity Error	max	±½	LSB
Differential Nonlinearity			
Error	max	±½	LSB
Missing Codes, 0 to 70°C		None	
Offset Error[1]		±10	mV
Gain Error[1]		±0.05	%
STABILITY			
Offset vs Temperature			
Unipolar	max	±5	ppm/°C
Bipolar	max	±10	ppm/°C
Gain vs Temperature	max	±30	ppm/°C
Differential Nonlinearity			
vs Temperature	max	±10	ppm/°C
Power Supply Sensitivity			
Offset		±10	ppm/%
Gain		±20	ppm/%
Warm-up Time		5	minutes
CONVERSION TIME[2]		40	µs
ANALOG INPUT			
Input Voltage Range			
Unipolar		0 to +5, +10	V
Bipolar		–5 to +5, –10 to +10	V
Input Impedance			
0 to +5 V FS		2.5	kΩ
0 to +10 V, ±5 V FS		5	kΩ
±10 V FS		10	kΩ
Buffered[3]		1000	MΩ
LOGIC INPUT[4]			
Start		Positive pulse, DC coupled 100 ns min width, rise & fall time 1 µs max, 2 TTL loads	
Clock In		1 TTL load	
LOGIC OUTPUTS[4]			
Data (Parallel or Serial)		TTL level, 5 unit loads/bit	
Busy		HI during conversion, 5 unit loads	
Strobe		Serial data synchronization, 5 unit loads	
Codes			
Unipolar (Parallel or Serial)		Binary, positive true	
Bipolar			
Parallel		Offset Binary, positive true or two's complement binary, positive true	
Serial		Offset Binary, positive true	
INTERNAL REFERENCE		yes	
TEMPERATURE RANGE			
Rated		0 to +70	°C
Operation		–25 to +85	°C
Storage		–55 to +125	°C
POWER SUPPLY			
Voltage		±15 ±2%, +5 ±5%	V
Current			
+15 V		20	mA
–15 V		30	mA
+5 V		210	mA

NOTES:
1. Offset and gain errors are adjustable to zero.
2. Conversion time is measured from the trailing edge of the START pulse to the HI going LO transition of the BUSY output.
3. Units with buffer available on special order only. Add $20.00 to price for 1 to 24 quantity. Specify -B on order.
4. All digital inputs and outputs are completely TTL compatible. One unit load is identical to that defined for standard 54/74 series TTL.

ACCURACY

For an analog-to-digital converter, the accuracy specifications provide a "window" of analog input level that can cause a particular digital output. All ADC's have an inherent quantizing effect that causes an uncertainty of ±½ LSB. This ±½ LSB is the limit in resolution of a particular ADC. With a resolution of 12 bits binary and with a maximum differential nonlinearity of ±½ LSB or ±0.0122% of full scale, the 168-12QZ ADC offers excellent accuracy and performance for general purpose, low cost systems.

CONVERSION TIME

The total time necessary to make a conversion is independent of input signal level. This is because the successive-approximation technique of conversion must make all bit comparisons regardless of input level. The actual conversion time will depend on clock frequency which may vary as much as ±20% from unit to unit. But the absolute maximum conversion time including temperature variation will never be more than 40 µs.

CODING

Full-scale for the 168-12QZ is determined by external pin connections. The converter can accept unipolar inputs of 0 to +5 V or 0 to +10 V and bipolar analog inputs of ±5 V or ±10 V. One least-significant-bit (LSB) and converter coding is shown in the following table.

		Bits (Data Output)						
	Analog Input	MSB 1	2	3 ---	9	10	11	LSB 12
Unipolar Straight Binary	+(FS–1 LSB)	1	1	1	1	1	1	1
	½ FS	1	0	0	0	0	0	0
	1 LSB	0	0	0	0	0	0	1
	0	0	0	0	0	0	0	0
Bipolar Offset Binary	+(FS–1 LSB)	1	1	1	1	1	1	1
	½ FS	1	1	0	0	0	0	0
	1 LSB	1	0	0	0	0	0	1
	0	1	0	0	0	0	0	0
	–1 LSB	0	1	1	1	1	1	1
	–½ FS	0	1	0	0	0	0	0
	–FS	0	0	0	0	0	0	0

OPERATION

A positive-going pulse with a minimum width of 100 ns to the START convert input will initiate the conversion cycle. This pulse must be a TTL level (+2.4 minimum for HI, +0.4 maximum for LO) and capable of

driving 2 TTL loads. The BUSY output will switch to a logic HI approximately 75 ns later. The trailing edge of the START convert pulse begins the conversion by setting the most significant bit, bit 1 (MSB) to the LO state and bits 2 through 12 to the HI state. At the end of conversion, the BUSY output goes from HI to LO (+2.4 V minimum to +0.4 V maximum). At this time, the conversion is completed and the parallel digital output is valid.

The conversion will be completed approximately 150 ns ahead of the BUSY output negative-going transition, so the leading edge of the BUSY or $\overline{BUSY}$ can be used as a strobe to transfer the output data. Because of the technique of conversion, the total conversion time will always be the same regardless of the input level, but will never be more than 40 μs. Therefore, the converter can be externally commanded to convert at rates of up to 25,000 conversions per second. See Figure 2 for timing diagram.

CONNECTING THE CLOCK

Although the 168-12QZ contains its own internal clock oscillator, connection to it is accomplished with an external jumper between pins 35 and 36 of the module. This jumper between CLOCK OUT (pin 36) and CLOCK IN (pin 35) must be installed unless otherwise specified. The 168-12QZ is intended to operate only with the internal clock.

The internal clock is set to run at the maximum permissable rate. Although running it at a slower rate will not improve the converter's accuracy, in some applications a slower conversion time may permit synchronization or compatibility with interfacing equipment. This may be accomplished by connecting a capacitor between CLOCK OUT (pin 36) and CLOCK RATE ADJ (pin 31). The conversion time can be extended to at least 35 ms in this manner. The capacitor's value is determined by the formula:

$$\text{Conversion Time (in } \mu s) \approx (1 + \frac{C_{ext}}{2000}).$$

where C_{ext} = external capacitance in pF.

SERIAL DATA OUTPUT

A latched serial output (taken from the output of a TTL flip-flop) is brought out to pin 32. The data is transmitted MSB first, and is coded positive-true offset binary for bipolar input ranges. Prior to the beginning of a conversion this output will match the state of the twelfth bit (LSB) of the previous conversion (assuming the previous conversion was allowed to go to completion). In most applications the state of the serial output prior to the beginning of a conversion will be of no consequence.

Figure 3 indicates one method for transmitting data serially to a remote location using only three wires plus a digital ground). The data is clocked into a receiving shift register using the 168-12QZ strobe output as a clock source for the shift register.

The Timing Diagram (Figure 2) shows that the serial data bits are valid on successive strobe pulse leading edges ("0" to "1" transitions). This allows the strobe

pulse to clock the shift register directly, since the shift register transfers information on "0" to "1" transitions of the clock input. The first bit, which is the MSB is valid on the first strobe pulse's leading edge. Each complete conversion has exactly twelve strobe pulses, one for each bit.
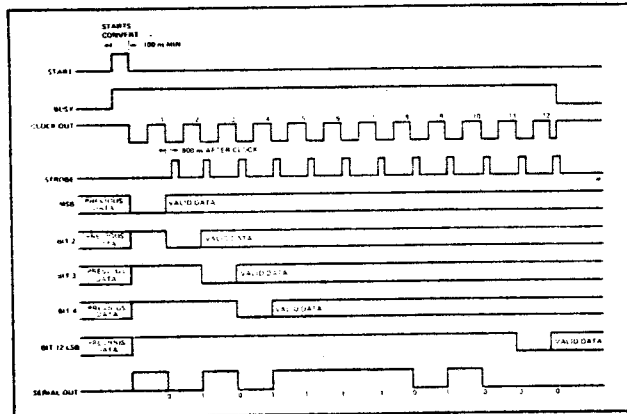

Figure 2. Timing Diagram

OPTIONAL EXTERNAL ADJUSTMENTS

OFFSET ADJUST

As a user option, the analog input offset can be adjusted by applying an offset voltage to Comp In input (pin 20). A 20 kΩ trim potentiometer with excitation voltage of ± 15 V and the wiper connected to pin 20 through a 1.5 MΩ resistor will provide approximately ± 20 LSB of adjustment. If finer adjustment is required, then the range of adjustment can be reduced by adding a larger resistor in series with the potentiometer wiper. Pin 20 should be left open if an offset adjustment is not needed.

GAIN ADJUST

The gain, or scale factor, may also be externally adjusted. A 20 kΩ trim potentiometer with excitation voltage of ± 15 V and the wiper connected to GAIN ADJUST (pin 1) through a 150 kΩ resistor will provide approximately ± 13 LSB range of adjustment. If finer adjustment is required, then the range of adjustment can be reduced by adding a larger resistor in series with the potentiometer wiper. Pin 1 should be left open if a gain adjustment is not needed.
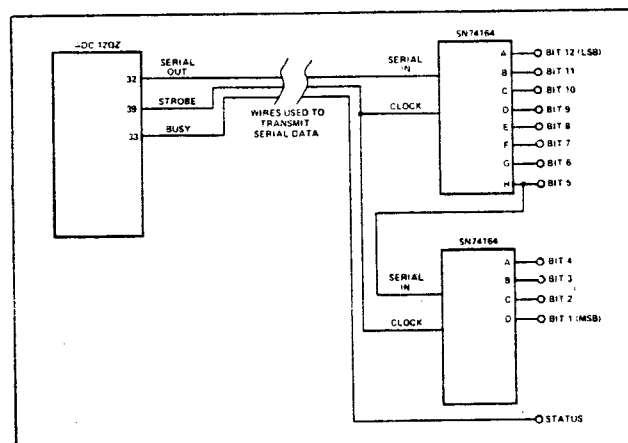

Figure 3. Block Diagram — Serial Data Transfer

Robert Lopez (handwritten)

PIN CONNECTIONS

INPUT SCALING

The input voltage range is selectable by pin connection. When the optional internal, high-impedance, buffer amplifier is used, the BUFFER output is connected to the SPAN inputs. For a 10 V SPAN, connect the BUFFER output (pin 4) to SPAN 10 V (pin 6). For a 20 V SPAN, connect BUFFER output (pin 4) to SPAN 20 V (pin 5). For a 5 V SPAN, connect the BUFFER output (pin 4) to SPAN 10 V (pin 6) and connect SPAN 20 V (pin 5) to COMP IN (pin 20). When not using the internal buffer amplifier, connect the analog input directly to the SPAN inputs.

UNIPOLAR OPERATION (0 to +5 V or 0 to +10 V With Or Without Optional Buffer Input)

Connect the MODE output (pin 19) to ANALOG COMMON (pin 23). Use SPAN 10 V (pin 6) for 0 to +10 V input range. For 0 to +5 V input range use SPAN 10 V (pin 6) as ANALOG INPUT and connect SPAN 20 V (pin 5) to COMP IN (pin 20). The output code will be natural binary.

BIPOLAR OPERATION

Connect the MODE output (pin 19) to COMP IN (pin 20). Use SPAN 10 V (pin 6) for ±5 V input range, SPAN 20 V (pin 5) for ±10 V input range. The output code will be natural offset binary. For Two's Complement coding use $\overline{MSB}$ (pin 70) as the most-significant-bit ($\overline{bit\ 1}$).

ZERO ADJUSTMENT PROCEDURE

1. Unipolar operation:
   a. Set input voltage to precisely +½ LSB.
   b. Adjust offset control until converter just barely switches from 000000000000 to 000000000001.

2. Bipolar operation:
   a. Set input voltage to precisely minus full scale +½ LSB.
   b. Adjust offset control until converter just barely switches from 000000000000 to 000000000001.
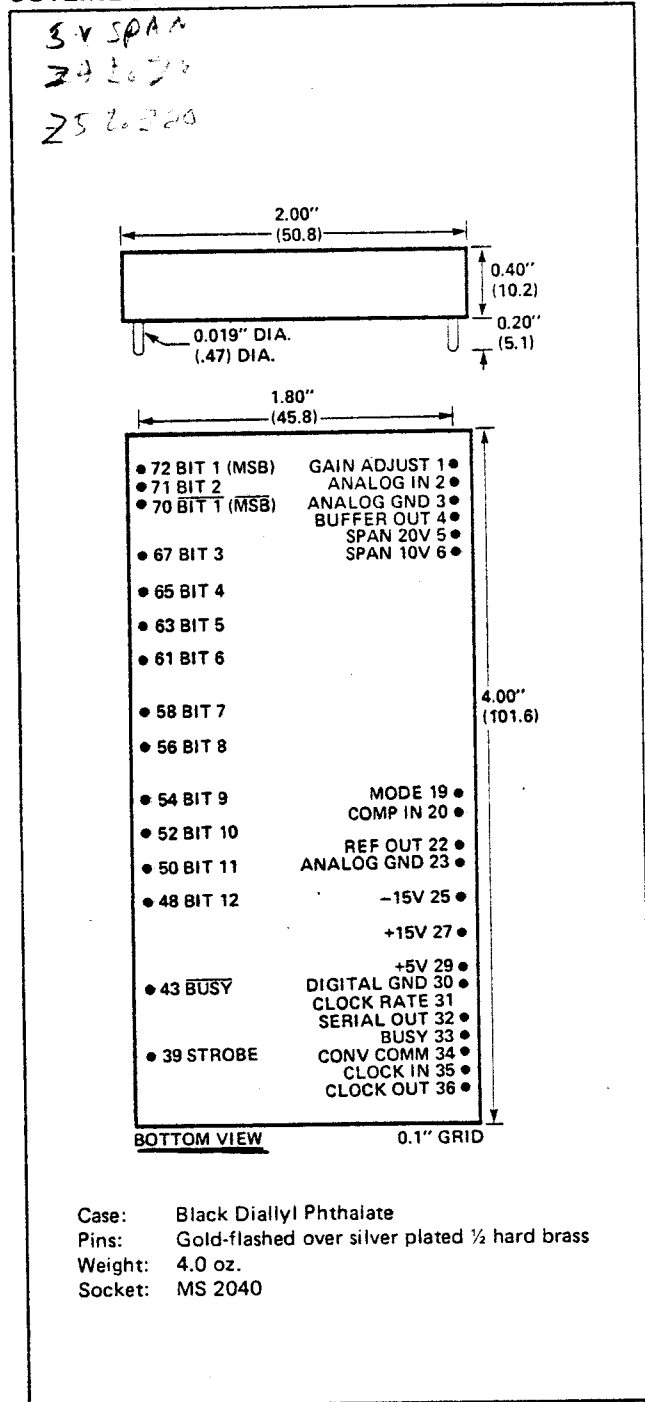
GAIN ADJUSTMENT PROCEDURE

1. Set input voltage to precisely full scale less ½ LSB. Note this is 1½ LSB less than nominal full scale.

2. Adjust gain control until converter just barely switches from 111111111110 to 111111111111.

GROUNDING CONNECTIONS

The DIGITAL COMMON (pin 30) must be connected externally to the ANALOG COMMON (pin 23) at same point in the system. Also, the commons of the +5 V and ±15 V power supplies must be tied to this same common. For optimum performance, the system common should be located at the A/D converter and separate power supplies should be committed to the A/D converter. But if the power supplies are shared among several loads, then the recommended practice is to connect the DIGITAL COMMON directly to the +5 V common. The supply commons are then connected to a central common.

OUTLINE DIMENSIONS

5 V SPAN (handwritten)

2.00″ (50.8)
0.40″ (10.2)
0.20″ (5.1)
0.019″ DIA. (.47) DIA.
1.80″ (45.8)
4.00″ (101.6)

● 72 BIT 1 (MSB)   GAIN ADJUST 1 ●
● 71 BIT 2   ANALOG IN 2 ●
● 70 $\overline{BIT\ 1}$ ($\overline{MSB}$)   ANALOG GND 3 ●
                               BUFFER OUT 4 ●
                               SPAN 20V 5 ●
● 67 BIT 3   SPAN 10V 6 ●
● 65 BIT 4
● 63 BIT 5
● 61 BIT 6
● 58 BIT 7
● 56 BIT 8
● 54 BIT 9   MODE 19 ●
                            COMP IN 20 ●
● 52 BIT 10   REF OUT 22 ●
● 50 BIT 11   ANALOG GND 23 ●
● 48 BIT 12   –15V 25 ●
                             +15V 27 ●
                              +5V 29 ●
● 43 $\overline{BUSY}$ DIGITAL GND 30 ●
                         CLOCK RATE 31 ●
                          SERIAL OUT 32 ●
                               BUSY 33 ●
● 39 STROBE   CONV COMM 34 ●
                           CLOCK IN 35 ●
                          CLOCK OUT 36 ●

BOTTOM VIEW   0.1″ GRID

Case: Black Diallyl Phthalate
Pins: Gold-flashed over silver plated ½ hard brass
Weight: 4.0 oz.
Socket: MS 2040

PIN CONNECTIONS

1. Pins 23 and 30 must be connected together externally.
2. Pins 3 and 23 are connected internally.

intech cmi function modules

282 Brokaw Road, Santa Clara, California 95050   Telephone (408) 244-0500   TWX 910 338-0254

Robert Hoper *(crossed out)*

A 14 ↑
examine 061

A₁₄ A₁₁ ↑
Run.
Stop
Examine 0 - 363
All ↑ Run (Type) CLOAD B

Robert Hoper (crossed out)
Frank Stephens

88-ADC TEST

Equipment Required

You will need a 8800 A, B, or Sherwood Chassis, (*Sherwood A to D Cards must be tested in a Sherwood Chassis) and a Terminal. The chassis should contain the following: A CPU, at least 8K of memory; IO Card and two switchable Extender Cards. You will also need a voltage source. Optional cards which will help include:

ACR, (3.2) 8K Basic on Proms. *(Prom Test) A14 up hit examine All up - hit Run, then Stop. Switches down, examine back to zero, lift All back up if you have a 2SIO, then hit run. write CLOAD B → start tape +*

Load Basic and load MUX Diagnostic program either from paper tape or cassette *when tape passes 10 → u. + return, when it reaches 46, TTY will print OK* tape. Examine the 88 ADC Card for the following before you place it in the chassis. *Print Run* *[See zero adjustment]*

PRODUCTION 88-ADC

Production A to D Cards can be identified by 2 small regulators located under the +5V regulator on the left side of the card. Production A to D Cards also have 2 connectors along the top and most components holes will have parts installed.

Inspect the card for the following jumpers. 5 address jumpers @ approx. lower center of the board. Above the A to D module jumper @ J2 and jumper @ J3 to J4.

NOTE   Correct J3 to use in the right hand J3.

Inspect the back side of the card for jumpers between pin 6 and pin 8 of IC U(CD 4051) jumper from P1 pin 1 to P2 pin 6. +5VDC land going to R13. R14 & $15 should be cut very near the resistors and a jumper should go from the common resistor pad to the +12VDC land. This is the 2nd land down from the top of the card. There should be no other jumpers on the card.

TEST

✗ Stop and reset the computer. Turn off all three switches on the extender *IMPORTANT* card. Carefully plug the A to D Card into the extender card. Turn on all three ₋witches. Verify that the computer is still at location 0 and that it contains an octal 363 at location 0.

on Mux Bd Black Box Leads
go on right side of capacitors

Power Supplies *in left hand corner of bd.*

-15 lead on top

Check with a scope or meter pins 25(-12V), 27(+12) and 29(+5V) <u>on the A to D</u>

<u>module.</u> These three voltages should be within ±.5VDC of the listed value.

Power supply voltage must be correct before you proceed.

Zero Adjustment

24 channels

Run program, enter "3,3" and ch "#0": the teletype should start printing a

voltage. Connect the voltage source cable to connector P1 on the A to D Card.

Measure the voltage going into P1 with a <u>digital voltmeter</u>, adjust this voltage

for -5.000 volts (±.005 volts leave DVM connected while setting zero comp).

If the A to D card is working correctly the teletype should be printing a voltage

between -4.5 and -5. volts. If not locate and correct the defect. Adjust R1 *(yellow pod on top of bd.) w/ screw on top*

(located at the top left side of the A to D) until the teletype is printing -5. *Need DVM & read Teletype to be*

the same

Note if the teletype is printing -5 when you start you will have to adjust R1 until *same*

voltage

the teletype prints -4.9xxx volts. The teletype will not print values more negative

than -5 volts. With the teletype printing -4.9xxx now adjust R1 until it <u>just</u>

prints -5.0. This completes the zero compensation adjustment.

Check These 3

Tracking

-5   2.5   +5

(Leave equipment set up as in zero adjustment test) Set the voltage source

for -2.500V(±.005V) and verify that the teletype prints -2.500V (±.05V). Set the

voltage source for values of 0.000V, +2.500V, and +5.000 volts. (All voltage set

within ±.005V). The teletype should track these input voltages within ±.05 volts.

8 Channel Multiplexer Test

If you don't want teletype to prints then write Run 2 (but continue running)

2.5 v)

"Control C" teletype to exit program. Connect 8-ch multiplexer cable to plug

(Mux cable)

Take color coded wire & hook into 2nd hole —

P2 of the A to D Card. Note this should be the cable which will be shipped with *Gnd in hole 1*

Ex. Brown — hole 2 Run program.

the unit. Connect the DB-25 connector, pins1 & 6 (GND) to the voltage source.**

Adjust the voltage source for +2.5V (±.005V). Run the program. Enter "4,3". The *Red - hole 2 (Take Brown out) Run program*

te. pe should print Ch. #0= 2.5V (±.05V). All other channels should be -5V. *Reconnect*

the voltage source and rerun the program for each of the other channels.

Hook up appropriate wire and Run 2

→ 4,3

Brown Channel 0 Reads -2.5V
-5 v Channel 1
-5 v Channel 2

**Disreguard stamped "1" on plastic connector

Robert Hooper (handwritten)

24 Channel Control Test

Stop and reset the computer. Turn all 3 switches off on the extra extender card. Connect a known good 24 channel mux cable to a known good 88-(Production) Mux Card. Carefully insert the Mux card into the extender card. Turn on all three switches. Insure that the computer is at address zero and data is octal 363. *Stop, reset comp. will see* (handwritten) If not reset and deposit as required. Connect the 20 pin connector to the A to D card and connect the mux cable to the voltage source. Run the program. Enter "3,3" and ch "#0". Set voltage source selector switch to "decrement" position. Set the gain switch for gain 1. *(on back)* Adjust source until TTY just prints 5. *(4.9) Hook up to Mux.* "Control C" on the teletype. Run the program. Enter "2,3". The teletype print out should have ch#0 = 500. All other channels should descend in value (example ch#0 = 500 ch #1 = 487 ¡#2 = 450). Absolute value is not important—only that each channel is lower in value then the next higher channel #.

Place voltage source selector in the "incr" position. Run the program & enter "2,3". Ch #0 should now be the lowest value and Ch #23 should be the highest value. Each channel should be slightly higher in value then the previous channel.

This completes the A to D test.

STOCK WITHDRAWL SHEET   DEPT: _____   DATE: _____

PAGE _1_ OF _2_   PULLED BY: _____

TO BUILD QTY: _____   OF: 88 A/D CONVERTER BOARD AND CABLE - PRODUCTION

PLEASE ENTER QUANTITIES IN PENCIL TO FACILITATE CHANGES

MITS P/N	NAME AND DESCRIPTION	QTY. PER UNIT	QTY. REQ'D.	ISSUED	SHORT	REMARKS	UNIT COST	COST EXT.
100190	A/D PRINTED CIRCUIT BOARD	1						
101667	HEAT SINK, SMALL	1						
100925	6-32 X 3/8 SCREW	1						
100942	6 LOCKWASHER	1						
100933	6-32 HEX NUT	1						
101074	MA7805 VOLTAGE REGULATOR	1						
102033	20K 10 TURN TRIM POT 43P203	1				Special		
101788	20 PIN RIGHT ANGLE WAFER	1						
101881	10 PIN RIGHT ANGLE WAFER	1						
101889	PLUG IN PINS 50463-6 AMP	35						
101177	9673Z A/D CONVERTER	1						
102101	8 PIN I.C. SOCKET	.1						
102102	14 PIN I.C. SOCKET	9						
102103	16 PIN I.C. SOCKET	5						
102106	40 PIN I.C. SOCKET	2						
101097	S6820 40 PIN CHIP	2						
101056	MA741 8 PIN I.C. CHIP	1						
101020	7400 14 PIN I.C. CHIP	1						
101054	7406 14 PIN I.C. CHIP	1						
101073	74L04 14 PIN I.C. CHIP	3						
101080	74L00 14 PIN I.C. CHIP	1						
101082	74L30 14 PIN I.C. CHIP	1						
101119	74LS73 14 PIN I.C. CHIP	1						
101132	4051 CMOS 16 PIN I.C. CHIP	1						
101040	74367 16 PIN I.C. CHIP	3				738...		
101078	74L123 16 PIN I.C. CHIP	1						
102305	2N2907 TRANSISTOR METAL CAN	2						
101179	78L12 REGULATOR TRANSISTOR	1	Plastic					
101178	79M12 REGULATOR TRANSISTOR	1	Metal Can					
100705	IN914 DIODE	17						

TO BUILD QTY: _____ OF: 88 A/D CONVERTER BOARD AND CABLE - PRODUCTION

PLEASE ENTER QUANTITIES IN PENCIL TO FACILITATE CHANGES

TS P/N	NAME AND DESCRIPTION	QTY. PER UNIT	QTY. REQ'D.	ISSUED	SHORT	REMARKS	UNIT COST	COS EXT
01902	470 OHM 1/4W 5% RESISTOR	1						
01903	1K 1/4W 5% RESISTOR	3						
01945	2.2K 1/2W 5% RESISTOR	1						
01912	4.7K 1/4W 5% RESISTOR	12						
01905	10K 1/4W 5% RESISTOR	4						
02081	330K 1/2W 5% RESISTOR	1						
00381	.01MF 50V CAP, SK20Y5V103M050	1						
00380	.1MF 50V CAP, SK30Y5V104M050	1						
00323	5MF 25V CAP. ELECT.	3						
00352	10MF 25V CAP, ELECT.	4						
00334	20PF 10V CAP, DISC	1						
03083	#30 GAGE KYNAR WIRE	1 FT						
01982	3.9K 1/2W 5% RESISTOR	1						
	A/D CONVERTER CABLE							
03079	15 CONDUCTOR CABLE W-1124	26"						
01720	10 PIN MOLEX CONN. FEMALE	1						
01723	TERMINAL PIN FOR 101720	9						
02112	ITT-7325 DB-25S CONNECTOR	1						
01791	POLARIZING KEY	1						
03073	3/8" HEAT SHRINK TUBE	6"						
	ASSEMBLE CABLE							
	PER MITS DRAWING							
	8810-301							

DUAL TRACKING
VOLTAGE REGULATORS

4194

DESIGN FEATURES

- Simultaneously Adjustable Outputs With One Resistor to ±42V.
- Load Current ±200mA with .2% Load Regulation

- Internal Thermal Shutdown at T_i = 175°C
- External Balance for ±V_O Unbalancing
- 3W Power Dissipation

The RM4194 and RC4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200mA. A single external resistor adjustment can be used to change both outputs between the limits of ±50mV and ±42V.

These devices are designed for local "on-card" regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

The device is available in two package types to accommodate various power requirements. The TK (TO-66) power package can dissipate up to 3W at T_A = 25°C. The D 14-pin dual in-line will dissipate up to 900mW.

SCHEMATIC DIAGRAM
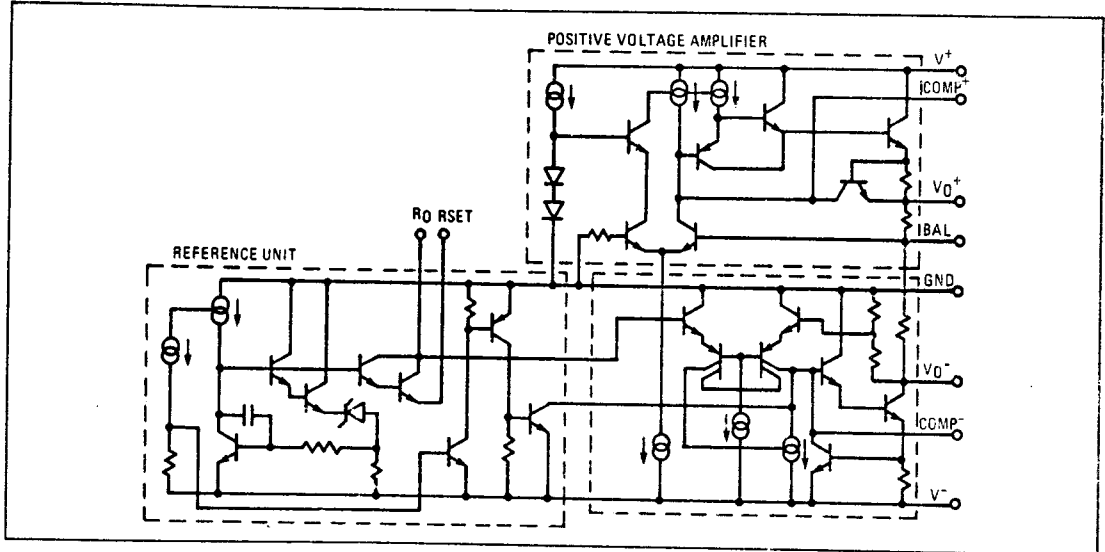
CONNECTION INFORMATION

TK (TO-66) Package
(Bottom View)

Order Part Nos.:
RC4194TK, RM4194TK

D Dual In-line Package
(Top View)

Order Part Nos.:
RC4194D, RM4194D
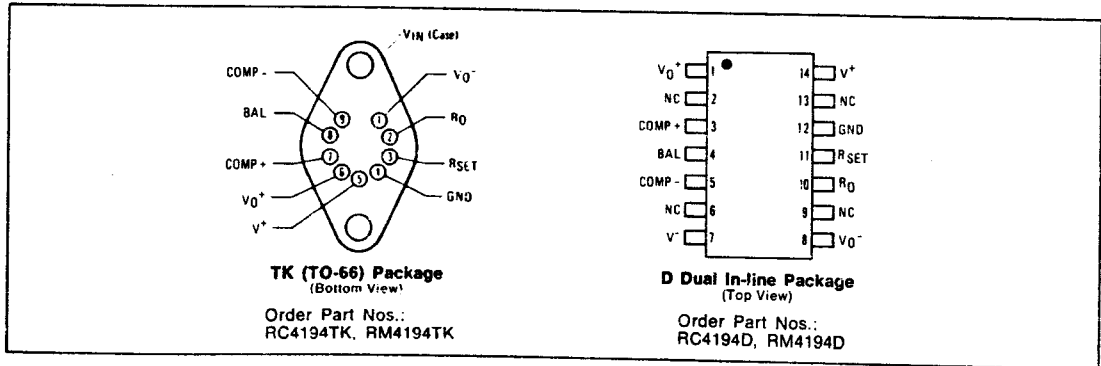
DUAL TRACKING VOLTAGE REGULATORS

ABSOLUTE MAXIMUM RATINGS

Input Voltage ±V to Ground .... RM4194: ±45V
RC4194: ±35V

Input-Output Voltage Differential .... RM4194: ±45V
RC4194: ±35V

Power Dissipation at $T_A = 25°C$
D Package 900mW
TK Package 3.0W

Load Current
D Package 150mA
TK Package 250mA

Operating Junction Temperature Range .... RM4194: −55°C to +150°C
RC4194:   0°C to +125°C

Storage Temperature Range .... −65°C to +150°C

Lead Temperature (Soldering, 10s) .... +300°C

ELECTRICAL CHARACTERISTICS
$(±5 \leq V_{OUT} \leq V_{MAX}$ • RM4194: $−55°C \leq T_j \leq +125°C$; RC4194: $0°C \leq T_i \leq +70°C)$

PARAMETER	CONDITIONS	RM4194			RC4194			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$\Delta V_{in} = 0.1V_{in}$		0.02	0.1		0.02	0.1	% V_{out}
Load Regulation	4194TK: $I_L = 1$ to 200mA 4194D: $I_L = 1$ to 100mA		0.001	0.002		0.001	.004	% V_o/mA
TC of Output Voltage			0.002	0.015		0.003	0.015	%/°C
Stand-By Current Drain (Note 1.)	$V_{in} = V_{max}$, $V_o = 0V$		+0.3	+1.0		+0.3	+1.5	mA
	$V_{in} = V_{max}$, $V_o = 0V$		−1.2	−2.0		−1.2	−3.0	
Input Voltage Range		±9.5		±45	±9.5		±35	V
Output Voltage Scale Factor	$R_{set} = 71.5K$ $T_j = 25°C$	2.45	2.5	2.55	2.38	2.5	2.62	KΩ/V
Output Voltage Range	$R_{set} = 71.5K$	0.05		±42	0.05		±32V	V
Output Voltage Tracking				1.0			2.0	%
Ripple Rejection	$f = 120Hz$, $T_j = 25°C$		70			70		dB
Input-Output Voltage Differential	$I_L = 50mA$	3.0			3.0			V
Output Short Circuit Current	$V_{in} = ±30V$ Max.		300			300		mA
Output Noise Voltage	$C_L = 4.7\mu F$, $V_o = ±15V$ $f = 10Hz$ to $100KHz$		250			250		μV RMS
Internal Thermal Shutdown			175			175		°C

THERMAL CHARACTERISTICS

PARAMETER	CONDITIONS	PACKAGE	
		D	TK (TO-66)
Power Dissipation	$T_A = 25°C$	900mW	3W
	$T_C = 25°C$	2.2W	17.5W
Thermal Resistance	Junction to Ambient, θ_{J-A}	128°C/W	41.6°C/W
	Junction to Case, θ_{J-C}	55°C/W	7.15°C/W

NOTE:
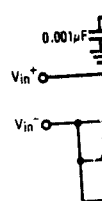± I_Quiescent will increase by 50μA/V_OUT on positive side and 100μA/V_OUT on
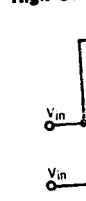negative side.
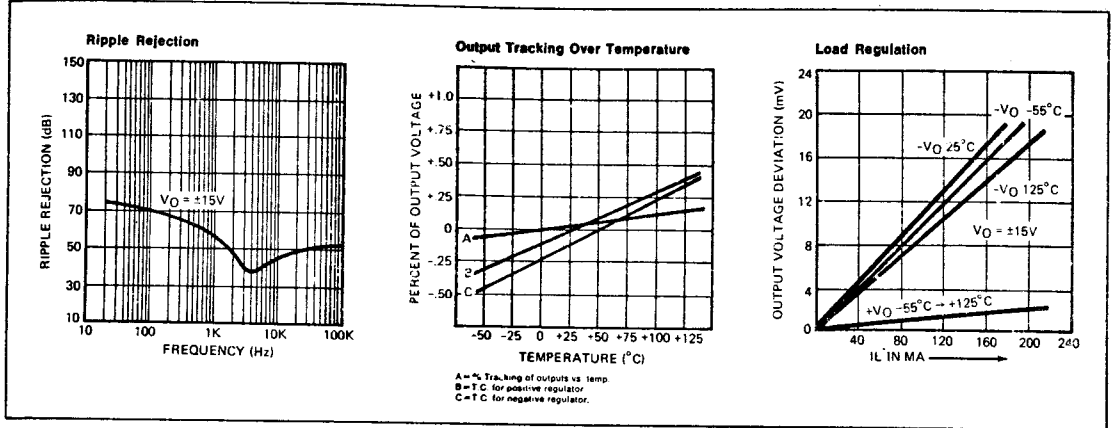
Ripple Rejection

TYPICAL APPLICATIONS

Balanced Out

Unbalanced

High Out

*For best tracking, temperature coefficient of Rg
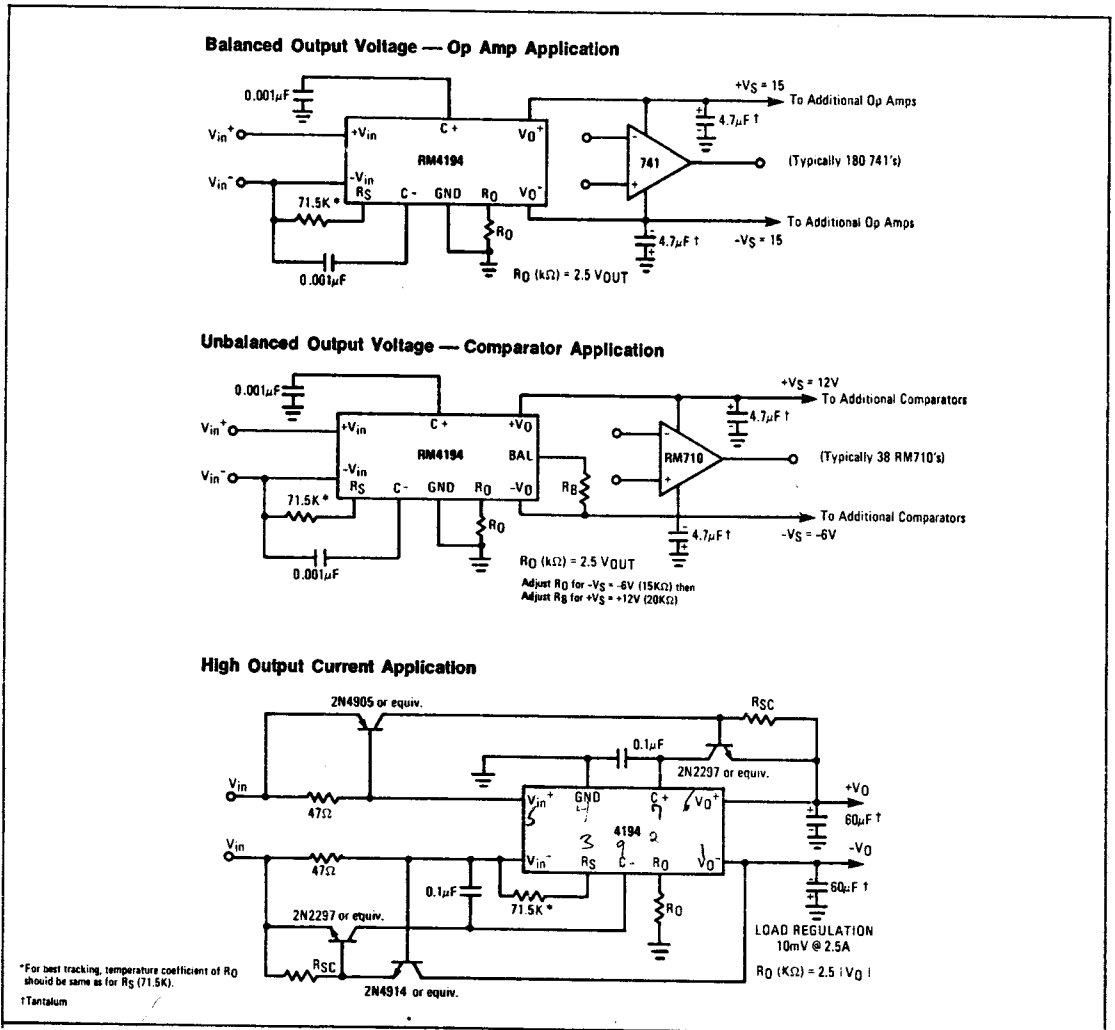should be same as for Rs (71.5K).

†Tantalum

RM4194: ±45V
RC4194: ±35V
RM4194: ±45V
RC4194: ±35V

.... 900mW
.... 3.0W

.... 150mA
.... 250mA
-55°C to +150°C
0°C to +125°C
-65°C to +150°C
.... +300°C

C4194		
TYP	MAX	UNITS
0.02	0.1	% V_out
0.001	.004	% V_o/mA
0.003	0.015	%/°C
+0.3	+1.5	mA
-1.2	... 0	
	...35	V
2.5	2.62	KΩ/V
	±32V	V
	2.0	%
70		dB
		V
300		mA
250		µV RMS
175		°C

KAGE		
TK (TO-66)		
3W		
17.5W		
41.6°C/W		
7.15°C/W		

TYPICAL ELECTRICAL TEST DATA

Ripple Rejection

RIPPLE REJECTION (dB) — $V_O = \pm15V$
FREQUENCY (Hz)

Output Tracking Over Temperature

PERCENT OF OUTPUT VOLTAGE
TEMPERATURE (°C)

A — % Tracking of outputs vs. temp.
B — T.C. for positive regulator.
C — T.C. for negative regulator.

Load Regulation

OUTPUT VOLTAGE DEVIATION (mV)
$-V_O$ -55°C
$-V_O$ 25°C
$-V_O$ 125°C
$V_O = \pm15V$
$+V_O$ -55°C → +125°C
IL IN MA

TYPICAL APPLICATIONS

Balanced Output Voltage — Op Amp Application

0.001µF
$V_{in}{}^{+}$
$V_{in}{}^{-}$
71.5K *
0.001µF
+V_in   C +   V_O+
-V_in
RS   C -   GND   R_O   V_O-
RM4194
R_O
$+V_S = 15$
4.7µF †
741
4.7µF †
To Additional Op Amps
(Typically 180 741's)
To Additional Op Amps
$-V_S = 15$
R_O (kΩ) = 2.5 V_OUT

Unbalanced Output Voltage — Comparator Application

0.001µF
$V_{in}{}^{+}$
$V_{in}{}^{-}$
71.5K *
0.001µF
+V_in   C +   +V_O
-V_in   BAL
RS   C -   GND   R_O   -V_O
RM4194
R_O
R_B
RM710
4.7µF †
4.7µF †
$+V_S = 12V$
To Additional Comparators
(Typically 38 RM710's)
To Additional Comparators
$-V_S = -6V$
R_O (kΩ) = 2.5 V_OUT
Adjust R_O for -V_S = -6V (15KΩ) then
Adjust R_B for +V_S = +12V (20KΩ)

High Output Current Application

2N4905 or equiv.
RSC
0.1µF
2N2297 or equiv.
V_{in}
47Ω
V_{in}
47Ω
0.1µF
2N2297 or equiv.
71.5K *
RSC
2N4914 or equiv.
V_in+   GND   C +   V_O+
4194
V_in-   RS   C -   R_O   V_O-
R_O
$+V_O$
60µF †
$-V_O$
60µF †
LOAD REGULATION
10mV @ 2.5A
R_O (KΩ) = 2.5 |V_O |

*For best tracking, temperature coefficient of R_O
should be same as for RS (71.5K).
†Tantalum

altair 8800
CONVERSION SYSTEM
SECTION I
INTRODUCTION

altair 8800
ANALOG CONVERSION SYSTEM
ANALOG TO
DIGITAL CONVERTER (88-ADC)
MULTIPLEXER (88-MUX)

Table of Contents

List of Tables

List of Programs

1-1. SCOPE AND ARRANGEMENT

The 8800 Analog to Digital Converter Board (88-ADC) and 8800 Multiplexer (88-MUX) Documentation provides a general description of the printed circuit board(s) and detailed theory of their operation. The manual contains five sections as follows:

1. Section I contains a general description of the Altair 88-ADC and 88-MUX boards.

2. Section II provides the user with the options available with the 88-ADC and 88-MUX boards. It is very important to read this section before attempting to utilize the system.

3. Section III includes a detailed theory explanation of the 88-ADC and 88-MUX circuit operations.

4. Troubleshooting information for the 88-ADC and 88-MUX boards is found in Section IV.

5. Four possible applications utilizing the 88-ADC and 88-MUX boards are shown in Section V.

1-2. DESCRIPTION

Many of the applications for the Altair computer require the ability to interface with real world analog signals. The 88-Analog to Digital Converter Card (88-ADC) permits the Altair 8800a or 8800b computer to measure analog voltages often encountered in scientific and industrial applications with an accuracy of one part in 4096.

The analog to digital converter module contains all of the circuitry needed to represent an analog voltage as a 12-bit binary value. The 88-ADC includes a buffer amplifier with a true differential input instrumentation amplifier option. An on-board 8-channel multiplexer is used to select one of the eight input signals. Since the 88-ADC is treated as an I/O device, it contains the circuitry to address the board and the associated timing circuitry.

Optionally, one or more 24-channel multiplexer cards (88-MUX) may be added to replace the 8-channel multiplexer. The 88-MUX expands the input capacity of the 88-ADC for applications requiring a large number of analog inputs.

The 88-ADC is actually a stand-alone card for many systems because it contains the on-board 8-channel multiplexer. However, the real potential of the ADC and MUX conversion system lies in the ability of the 88-MUX to process more than eight signals. Thus, by using four 88-MUX cards it is possible to process up to 96 analog signals for large system layouts.

The 88-MUX card is of extremely flexible design, being easily implemented in most any system. With simple modifications, the 88-MUX board can be set up to handle a true "differential" signal on each channel. The gain and scale factoring of each channel can be set independently. Filtering can also be added to provide the desired roll-off characteristics although factoring and filtering are not offered in a differential configuration.

1-3. SPECIFICATIONS

88-ADC

Resolution (binary bits)	12 bits
Conversion Time	65μs. (max)
Accuracy	
Quantizing Error	±1/2 LSB
Nonlinearity	±1/2 LSB
Offset	Externally Adjustable to zero
Stability	
Offset vs. Temp.	20 PPM/°C (max)
Gain vs. Temp.	80 PPM/°C (max)
Nonlinearity vs. Temp.	20 PPM/°C (max)
Gain vs. Supply Voltage	±30 PPM/%Vs (max)
Analog Input Impedance	1000 Megohms
Standard Option Voltage Ranges	
Unipolar	0 to +5 volts
	0 to +10 volts
Bipolar	-5 to +5 volts
	-10 to +10 volts (without MUX)
Operating Temperature Range	0 to +70°C

Power Supply Requirements   +5 volts at 500MA

+15 volts at 40MA

-15 volts at 30MA

88-MUX

Gain   up to 1000

Input Impedance   1 Megohm

Offset   5 mvolts (max)

Input Signal Level   0 to +10 volts

-5 to +5 volts

Settling Time to 0.01%   15µsec. (max)

op amp

altair 8800
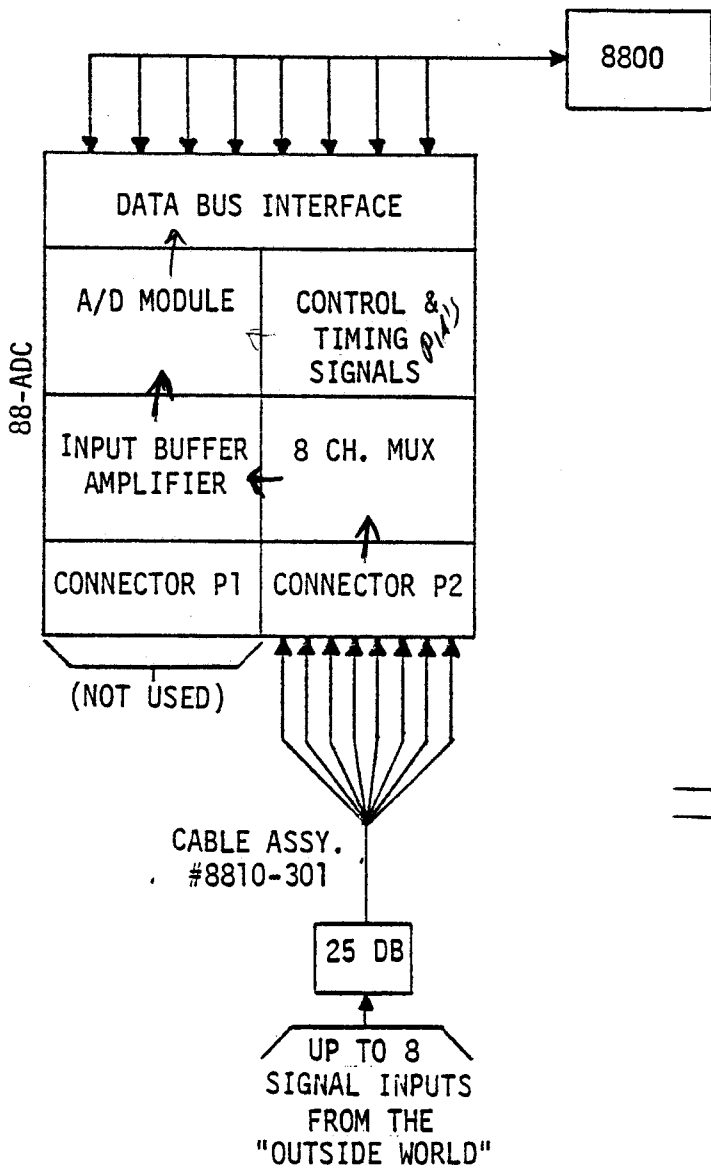## CONVERSION SYSTEM
SECTION II
OPTIONS

2-1. INTRODUCTION

The 8800 Analog to Digital Converter board (88-ADC) may be ordered with or without the 8800 Multiplexer (88-MUX) board. This section contains the necessary information for setting up either an 8-channel or 24-channel multiplexer system, including voltage range selection and scaling, voltage gain increase, input buffer amplifier option and zero adjustment. It is very important to read the following paragraphs before attempting to utilize your system.

2-2. MULTIPLEXER

The standard configuration of the 88-ADC board includes an 8-channel CMOS multiplexer. The input signals for this system are interfaced to the card via a 10-pin connector, P2. However, control logic is provided on the board for decoding up to twenty-four channels of input data by utilizing the 88-MUX multiplexer board and input connector, P1. For larger systems, up to four 88-MUX cards may be used, resulting in a 96-channel capability. Input signals are interfaced to both multiplexer systems via one or more cables from DB-25 connectors on the chassis rear panel. Proper cable-connector utilization and corresponding software control is necessary to select between the 8 or 24-channel multiplexer. Refer to Figures 2-1 and 2-1a for an 8-channel system and Figures 2-2 and 2-2a for a 24-channel system.

Figure 2-1. 8-Channel System

10 PIN MOLEX		
	25 DB	A/D MOLEX (P2)
(CH O)	1	10
	2	9
	3	8
	4	7
	5	4
	6	3
	7	2
(CH 7)	8	1
(GND)	25	6 (REQUIRES A JUMPER ON A/D (P2-6) TO (P1-1)
		5 (KEY)
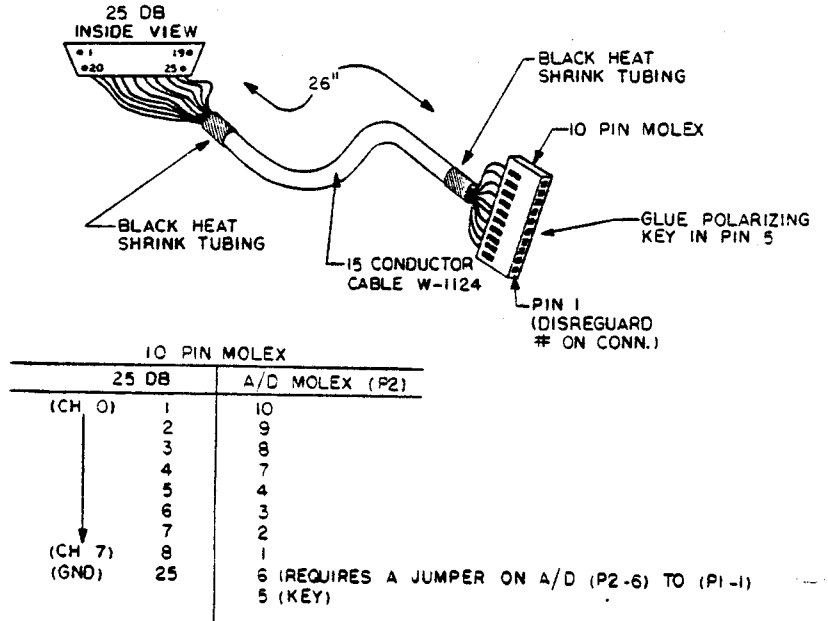
Figure 2-1a. 8-Channel MUX Cable Layout

8800

DATA BUS INTERFACE

88-ADC

A/D MODULE | CONTROL & TIMING SIGNALS

INPUT BUFFER AMPLIFIER | 8 CH. MUX *

CONNECTOR P1 | CONNECTOR P2

(NOT USED)

*FOR CONVERSION FROM A 24-CH. SYSTEM
TO AN 8-CH. SYSTEM OR
A SYSTEM WITHOUT A MUX,
SEE SECTION 2-2.

PART OF CABLE ASSY, 8810-302 **

CABLE ASSY.
8810-302

88-MUX

PART OF 100 PIN CONNECTOR | SECTION C CH. 16-28 | PART OF 100 PIN CONNECTOR
| SECTION B CH. 8-15 |
| SECTION A CH. 0-7 |

25 DB

UP TO 24 INPUT SIGNALS FROM "OUTSIDE WORLD"

88-MUX (OPTIONAL)

24 ADDITIONAL INPUTS

88-MUX (OPTIONAL)

24 ADDITIONAL INPUTS
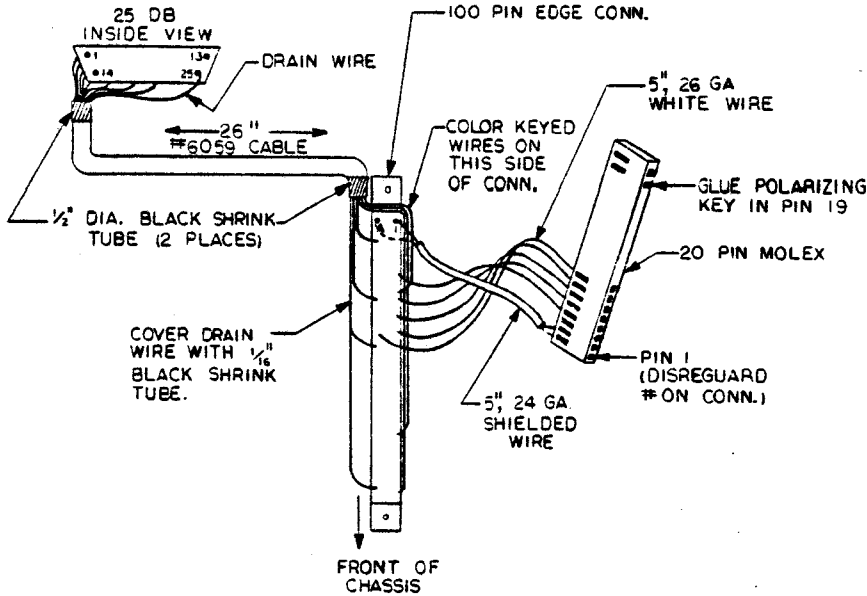
88-MUX (OPTIONAL)

24 ADDITIONAL INPUTS

** SYSTEMS USING MORE THAN ONE 88-MUX REQUIRE CABLE MODIFICATION
AS DESCRIBED IN NOTE 1 OF CABLE DRAWING #8810-302. ALSO NOTE THAT SYSTEMS
USING DIFFERENTIAL INPUTS REQUIRE SPECIAL CABLES (CONTACT FACTORY).

Figure 2-2. 24-Channel System

100 PIN EDGE CONNECTOR (MUX END)	25 DB (INPUTS)	CABLE COLOR	SIGNAL NAME	
6	24	BLACK	SC3	(CH 23)
7	23	GREEN	SC7	
8	22	BROWN	SC6	
9	21	RED	SC5	
12	20	RED	SC4	
13	19	GREEN	SC3	
14	18	RED	SC2	
15	17	BLUE	SC1	
21	16	RED	SB8	
22	15	WHITE	SB7	
23	14	RED	SB6	
24	13	YELLOW	SB5	
27	12	BLACK	SB4	
28	11	YELLOW	SB3	
29	10	BLACK	SB2	
30	9	ORANGE	SB1	
41	8	BLACK	SA8	
42	7	RED	SA7	
43	6	BLACK	SA6	
44	5	BLUE	SA5	
47	4	BLACK	SA4	
48	3	BROWN	SA3	
49	2	BLACK	SA2	
50	1	WHITE	SA1	(CH 0)

NOTE: ALL DRAIN WIRES SHOULD BE TIED TOGETHER BENEATH THE HEAT SHRINK TUBING (AT THE 25 DB) AND A SINGLE WIRE TAKEN TO PIN 25. AT THE MUX END, THE SHIELDS SHOULD AGAIN BE TIED AND THE SINGLE LEAD SHOULD GO TO PIN A.

20 PIN MOLEX

| MUX 100 PIN	A/D MOLEX (P1)
A	1 (SHIELD)
1 (SEE NOTE 1)	2 (A/D INPUT)
16	13 (MA 0)
17	12 (MA 1)
18	11 (MA 2)
20	10 (MA 3)
X	14 (MA 4)
V	15 (MA 5)
U	16 (MA 6)
T	17 (MA 7)

NOTES:
1. IF MORE THAN ONE 88-MUX CARD IS TO BE USED THIS SIGNAL SHOULD COME FROM PIN 5 ON THE MUX 100-PIN CONN. ALSO, ALL PINS LISTED SHOULD BE BUS-JUMPERED BETWEEN MUXES.
2. DIFFERENTIAL INPUT OPTION REQUIRES (2) 25 DB CONNECTORS AND A SPECIAL CABLE.

Figure 2-2a.   24-Channel MUX Cable Layout

All 88-ADC boards are shipped with the 8-channel multiplexer configuration. If the board is to be used with a 24-channel system or operated without a multiplexer, the CMOS 4051 8-channel multiplexer (IC U) should be removed from the 88-ADC board. This insures that improper channel selection will not cause a conflict of input signal selection at the input buffer amplifier. Refer to the MOS IC Special Handling Precautions, section 2-9 (page 32), for removal and installation of IC U.

If you have received the REV 1 88-MUX board, please note the follow-
ing error on the board:

There is a missing etch on the circuit marked A5. It is near the
junction of R23, C13 and R22. If R23 is to be utilized, it will be
necessary to install a jumper between R22 and R23 (use circuit B1 as an
example). Refer to the drawing below for the position of the missing
land. You may also want to refer to the 88-MUX Silkscreen (page 49) at
IC A5, zone C4, for the component layout.
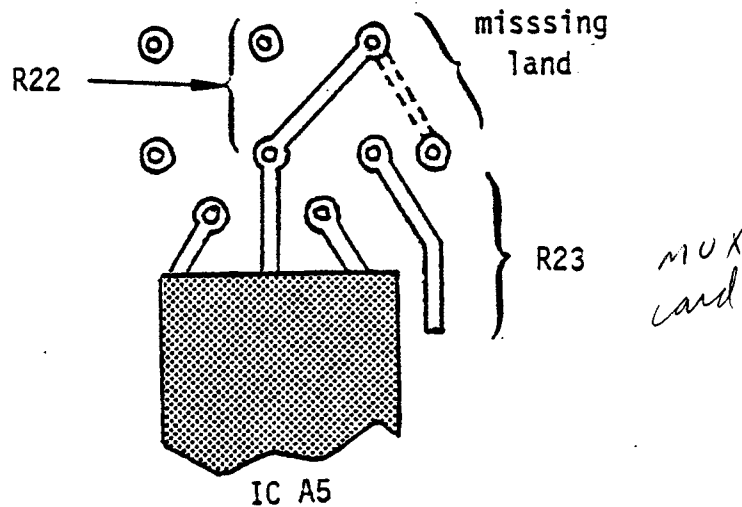
2-3. 88-ADC A/D MODULE INPUT VOLTAGE RANGES

The A/D module can be set up to read the voltage ranges shown in
Table 2-A by implementing the proper jumpering options. Figure 2-3,
88-ADC Silkscreen, shows the locations for the jumpering options listed.
When utilizing one or more 88-MUX cards in a system, it is imperative
that the selected voltage range is the same for the A/D module and the
88-MUX amplifiers. (Refer to Section 2-4.)

WARNING
When installing the jumper wires, be sure not to short any lands together or form solder bridges.

Table 2-A.   A/D Module Input Voltage Ranges

A/D MODULE INPUT VOLTAGE RANGE	J1	J2	J3	J4	J5	Additional Procedures
UNIPOLAR						
0 TO +5v		X	X		X	
0 TO +10v		X	X			
BIPOLAR						
-5 TO +5v (Std. Config.)		X		X		
-10 TO +10v (No MUX)	X	X		X		Drill out D1
X = JUMPER INSTALLED						

```
                         NOTE
J3 and J4 jumpers have a common pad labelled J3/J4 on the
board.  Only one end of J5 is labelled.  The other end of
J5 is found directly to the right of the square pad going
to the A/D module, pin 6.
```
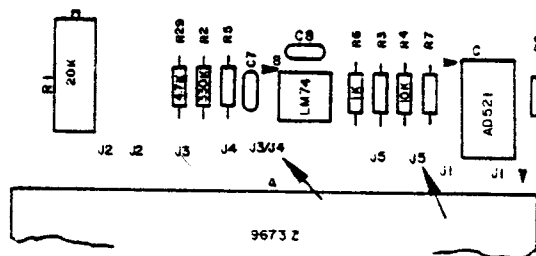

Figure 2-3.   88-ADC Silkscreen
(Jumper Locations)

2-4.   88-ADC INPUT RANGES USING MULTIPLEXERS

The standard configuration of both types of multiplexers provides
for the (-5v to +5v) voltage range at each amplifier input. Other input
ranges can be set up by selecting the proper resistor values on the
multiplexer. Either multiplexer is capable of processing signals over
a maximum 15v range. Table 2-B lists the possible ranges and the corres-
ponding resistor changes.

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Table 2-B. 88-ADC Input Ranges Using Multiplexers

88-ADC INPUT VOLTAGE RANGE	24 Channel MUX (88-MUX)		8 Channel MUX (88-ADC)	
	R135	R138	R26	R24
UNIPOLAR 0 TO +5v 0 TO +10v	5.2K	4.3K	180⌐	6.8K
BIPOLAR -5 TO +5v (Std. Config.)	18.2K	Not Used	1K	2.2K

Since both multiplexer systems are limited to a maximum input voltage range of 15 volts, the (-10 to +10v) range cannot be multiplexed directly. There are two methods that can be implemented to handle this range. First, the A/D module can convert over this entire voltage range without multiplexing if the signals are input via pins 1 and 2 on connector P1 (or an external multiplexing system can interface at this point). The second method is to scale down all voltages accordingly, using an 88-MUX based system. For example, if the input voltage divider network resistors of an 88-MUX card are properly chosen, an external signal range of (-10v to +10v) will appear as a (-5v to +5v) range to the 88-ADC card.

The following example references components on an 88-MUX card amplifier #1. Refer to the 88-MUX schematic, Figure 3-3, at the end of Section III. Use the formula for a voltage divider:

$$V_{OUT} = V_{IN}(R_3)/(R_3 + R_4)$$

Scaling down the input voltage range will always reduce accuracy by an appropriate factor. In many cases, however, the increase in allowable voltage span will more than compensate for this error.

Example 1: Suppose a (-20v to +20v) span is desired. Scaling by
a factor of 4 will give the best accuracy over the total
range.

Voltage Divider Formula: $V_{OUT} = V_{IN}(R_3)/(R_3 + R_4)$

Desired Voltage: $V_{OUT} = 5v$; V_{IN} 20v

Thus, $5 = 20v(R_3)/(R_3 + R_4)$ and $1/4 = (R_3)/(R_3 + R_4)$

To keep the input impedance relatively high, choose $R_3 = 1$ Megohm.
$(1/4 = 1$ Megohm/$(1$ Megohm $+ R_4)$, thus $R_4 = 3$ Megohms.) The source impe-
dance has a significant factor on accuracy, especially as it becomes
large. Referring to Figure 2-4, the % error can be calculated as follows
(neglecting amplifier loading effects):

V_{OUT}(theoretical) $= V_{IN}(R_3)/(R_3 + R_4)$

V_{OUT}(actual) $= V_{IN}(R_3)/(R_3 + R_4 + R_s)$
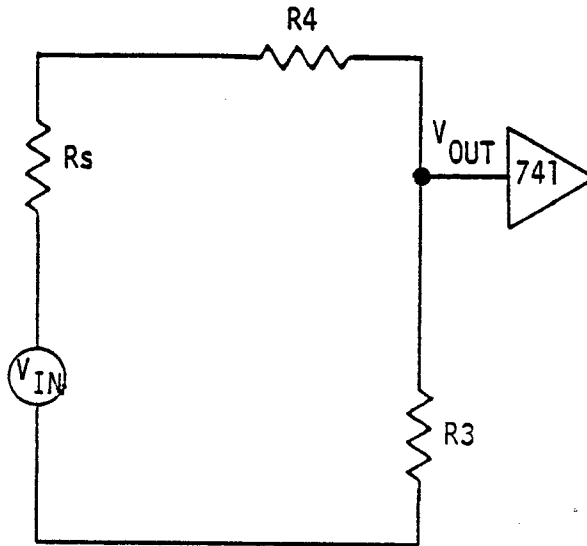
where R_s is the source impedance.

Figure 2-4. % Error In Scaling

Thus, the % error introduced to the system by adding a scaling network can be stated as follows:

$$\% \text{ error} = \left(\frac{\left| V_{OUT}(\text{theoretical}) - V_{OUT}(\text{actual}) \right|}{\left| V_{OUT}(\text{theoretical}) \right|} \right) X \ 100$$

and from Example 1,

$V_{OUT}(\text{theoretical}) = 20 \text{ volts } (1 \text{ Megohm})/(1 \text{ Megohm} + 3 \text{ Megohm}) = 5v$

$V_{OUT}(\text{actual}) = 20 \text{ volts } (1 \text{ Megohm})/(1 \text{ Megohm})/(1 \text{ Megohm} + 3 \text{ Megohm} + R_s)$
$\qquad\qquad = 20 \text{ volts } (1 \text{ Megohm})/(4 \text{ Megohm} + R_s)$

Thus, the % error $= \left(\frac{\left| 5 \text{ volts} - 20 \text{ volts } (1 \text{ Megohm})/ 4 \text{ Megohm} + R_s \right)}{\left| 5 \text{ volts} \right|} \right) X \ 100$

and if R_s = 10 ohms, then % error = .00025%

$\qquad R_s$ = 100 ohms, then % error = .0025%

$\qquad R_s$ = 1000 ohms, then % error = .025%

The A/D module error is .0244%. The total board error is the sum of the module error plus the scaling error. For this example, as R_s becomes larger than 100 ohms, the source impedance causes an increasingly significant portion of the total board error.

Generally, the lower the source impedance or the higher the scaling resistors, the smaller the % error factor. Beyond a certain point, however, an increase in scaling resistor impedance will begin to introduce noise. 10 Megohms is the largest recommended value for R_3 or R_4.

NOTE

The preceeding calculations are identical for scaling voltages on other amplifiers of the 88-MUX card. R_7 and R_8 replace R_3 and R_4, respectively, for amplifier #2, and so on.

2-5. 88-MUX GAIN

For very small signal levels, an increase in voltage gain (unity is standard configuration) will improve the voltage span seen by the A/D module. Any gain may be specified from 1 up to 1000 by using appropriate resistor values. The channels can be set up independently for __different__ gain factors. Gain of amplifier #1 is given by:

$$\text{GAIN} = \frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_4}{R_1} \quad *$$

Thus, neglecting divider effects from R_2 and R_3, a value for R_4 and R_1 can be computed.

Example 2:   If the input signal is a 10 Mv (.01 volt) level, a factor of 1000 will increase the signal to 10 volts. (Gain factors larger than 1000 are not recommended.)

Thus, $1000 = \dfrac{R_1 + R_4}{R_1}$

If R_4 = 1 Megohm, then $1000 = \dfrac{R_1 + 1 \text{ Megohm}}{R_1}$

$1000\ R_1 + R_1 = 1$ Megohm

$999\ R_1 = 1.00 \times 10^6$ and $R_1 \sim$ 1K ohm

Note that R_4 should never be greater than 1 Megohm and at this gain frequency considerations will limit the amplifier's response at around 1 KHz. (Signals changing at rates faster than this figure may be inaccurately buffered.)

Gain factoring can also be accomplished at the 88-ADC input buffer amplifier by selecting R_3 and R_4 in the same manner as above. __All channels are affected in this case.__

* Gain is unity when R_1 is removed from the circuit.

2-6. 88-ADC INPUT BUFFER AMPLIFIER

An optional instrumentation amplifier (differential configuration) may be used in place of the input buffer amplifier which is already on-board. For small signal applications (less than 50 mv), the 88-ADC should be specified with option #1. The AD521 instrumentation amplifier can successfully track as low as 1mv (.001 volts). Capability is also provided for differential inputs by utilizing a modified 88-MUX board. The modification consists of opening up 24 drill-holes in the analog ground lines (GA1, GA2, . . . etc) and using a special interface cable (#8810-303). By utilizing such a differential system, noise immunity may be increased significantly when rapidly changing signal levels are being read on adjacent channels.

2-7. ZERO ADJUSTMENT

For unipolar zero adjustment, follow these instructions:

a) Set a reference power supply to +0.0012 volts and connect to multiplexer channel #0.

b) Enter Program 2-I, MUX Isolation Test (page 20), with the appropriate parameters to loop on channel #0.

c) While Program 2-I is running, adjust pot R1 for a zero output reading.

d) Repeat steps b) and c) if necessary.

For bipolar zero adjustment, perform steps a) through d) except set the input signal level to -4.9988 volts.
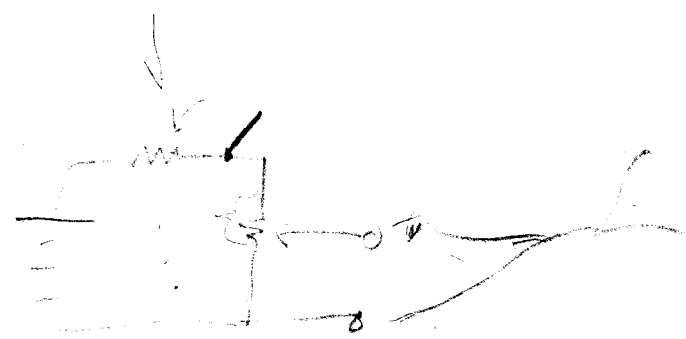
Program 2-I. MUX Isolation Test

This program will read up to 96 channels with an 88-MUX
system, up to 8 channels with the on-board 8-channel MUX,
or directly through the 88-ADC without a multiplexer.
SA is the number of samples desired at each channel.

```
10  REM TO READ ONLY ONE CHANNEL CHANGE 70 : I = (DESIRED CH.#) AND
20  REM DELETE STATEMENT 240
30  REM CH.# IS THE LAST CHANNEL YOU WANT TO TEST
50  INPUT"ENTER VI";VI
60  INPUT"ENTER BIAS";BIAS
65  INPUT"CH.#";CN
68  INPUT"ENTER SAMPLES";SA
70  FOR I=0 TO CN
72  PRINT:PRINT"CH.#";I
75  FOR J=0 TO SA
80  OUT130,0
90  OUT131,255
100 OUT130,4
110 OUT128,0
120 OUT129,255
130 OUT128,4
140 OUT134,0
150 OUT135,0
160 OUT134,4
170 OUT132,0
180 OUT133,0
195 OUT132,4
200 OUT131,I:OUT129,I
210 MS=INP(133):LS=INP(135)
220 V=((16*MS+((LS/16)AND 15))*VI/4095)-BIAS
230 PRINTV;
235 NEXT J
240 NEXT I
```

SELECTED V. SPAN	VI=	BIAS=
0 ← 5v	5	0
0 ← 10v	10	0
-5 ← +5v	10	5
-10 ← +10v No MUX	20	10

2-8. SOFTWARE

The 88-ADC board can be utilized in one of several different configurations. Depending on system requirements, one configuration may have considerable advantages over another. Two easily implemented schemes (A and B below) are briefly presented in this section to aid the user in selecting the most useful configuration for his particular system.

Note that in both methods it is possible to configure the board to handle interrupts following the normal jumpering scheme for vectored interrupt lines. The interrupt can be generated from the 88-ADC module itself or from an external piece of equipment with a "trigger" signal.

A. Standard Configuration

This method is employed more often since it is more versatile in application, especially for persons programming in BASIC. It is applicable to all systems not requiring synchronization to an external event. If the system program is written entirely in BASIC (no machine language), Program 2-I can be utilized. The advantages of Program 2-I include ease of programming and debugging. The major disadvantage is speed (maximum sample rate between samples is almost one second). For many applications, this sample rate is too slow and a high speed program would be more useful.

Three possible variations (listed below) can be implemented with this method. Sample Programs 2-II through 2-V contain the necessary information to apply any of these approaches to a particular system. These sample programs are found on pages 24 through 31.

1. a true "machine" language program which is fast but more complex to write, especially if data manipulation must be done in this form

2. a "hybrid" program written in BASIC which accesses a USR (user-called) machine language "acquisition" program

3. "real-time" output to a smart terminal

Utilization of the machine language acquisition results in a maximum sample rate of approximately 65 microseconds. Sample Program 2-II is an example of the first variation (without data manipulation) and Sample Program 2-III is an example of the "hybrid" version of Program 2-II.

In both sample programs (2-II and 2-III), approximately 45 microseconds are used for storage of each data sample (two bytes), followed by the start of the next conversion, and "housekeeping" functions (i.e. checking if the data block is filled). This leaves only 20 microseconds for data manipulation if the maximum A/D rate is to be maintained. Thus, the second variation (hybrid) is probably more versatile since the maximum sample rate is maintained and data manipulation is more easily handled in BASIC.

If the third approach is implemented, interrupt flag IRQA may be useful. The terminal must be able to interpret which of the two bytes are LSB/MSB. Also, in a steady output stream, the terminal should know which bytes link together to form one sample.

B. Synchronous Mode

The second method utilizing the 88-ADC makes use of an external event or "SYNC" pulse to initiate each conversion, thus "slaving" the 88-ADC to an external "trigger" signal. Only one conversion is completed for each trigger pulse, eliminating the processing time during intervals of irrelevant data. This occurs with a slight increase in the maximum acquisition rate, approximately 78 microseconds between samples.

To implement this scheme, the status of the IRQ flags are monitored without allowing another start until the in-process conversion has been completed. The external trigger for CB1 is input via P1 pin 9 and should be standard logic levels (LOW $\leq$ .8 volts, HIGH $\geq$ 2 volts).

The Std. Config. Mode can also be initiated by an interrupt (or by doing a status check of the CB1 flag). A "burst" of data is input and handled as previously described. However, the burst may contain more data than is required, resulting in excessive handling time.

Program 2-V is the "hybrid" version of Program 2-IV.

C. The following hints are important when designing any 88-ADC program:

1. The last four bits of the LSB byte in each sample should be masked out when reconstructing samples.

2. If interrupts are enabled from the CB1 "trigger" line, care should be taken to insure sufficient processing time is allowed between trigger words, or system errors will result.

3. In the Synchronous Mode (B), the status check for the trigger word is approximately 18 microseconds long. If the trigger word is "out-of-sync" to the time when the program enters the status check loop, the maximum sample rate may be extended by 13 microseconds.

4. Referring to the block of NOP instruction in Programs 2-II and 2-IV, the delay time must be included or the data conversion will not be completed at the time when data is read and stored by the CPU.

D. **Notes for Sample Programs 2-II Through 2-V**

① START ADDRESS - These two bytes specify starting address of the data block in memory. If only one sample of data is needed, this address should be two less than the END address.

② END ADDRESS - This word is the MSB address byte and represents the end of the data block in memory (i.e. the last data storage address is one byte less than this address).

③ IRQB STATUS FLAG - This word initializes PIA 1, enabling or disabling the IRQB interrupt line. It also determines the desired active transition (positive or negative going edge) of the trigger word applied to P1 pin 9. It is possible to use this word in the STD. CONFIG. mode to initiate the data acquisition and is required for proper operation in the SYNC mode. The trigger signal will affect the status flag whether the IRQ line is enabled or not.

CONTROL WORD	DESIRED TRIGGER TRANSITION	DESIRED INTERRUPT ACTION
006	↑	IRQB DISABLED
004	↓	IRQB DISABLED
007	↑	IRQB ENABLED
005	↓	IRQB ENABLED

④ A/D MODULE STATUS FLAG - This word determines the status of the A/D module. During a conversion, the CA1 line of PIA 1 monitors the BUSY line of the A/D module which is HIGH during a conversion and LOW upon completion. If enabled, the falling edge generates an interrupt on the IRQA interrupt line. The status channel flag (bit 7) can also be monitored to verify the completion of a conversion, if desired, by using a scheme similar to the status check of channel 204 in the SYNC program (2-IV or 2-V).

CONTROL WORD	DESIRED TRIGGER TRANSITION	DESIRED INTERRUPT ACTION
004	↓	IRQA DISABLED
005	↓	IRQA ENABLED

⑤ 8-CHANNEL MUX SETUP - This byte specifies which channel is accessed (000-007) if it is necessary to perform the acquisition through one of eight channels of the on-board multiplexer. If BASIC is used with the USR function, it is possible to POKE sequential channel numbers into this byte each time through the program.

⑥ DATA BYTE ORDER - Note the storage order of the two data bytes (MSB and LSB) in the STD. CONFIG. and SYNC modes. These may be reversed in some applications, and the major advantage to this reversal occurs when an interrupt or status flag is used (see ③ and ④). A data channel read from the appropriate section of PIA 1 will always reset bit 7 and the IRQ line for that section and may affect program timing.

⑦ 24-CHANNEL MUX/AD STROBE - The function of this byte is similar to that of the 8-channel MUX (refer to ⑤) for reading the 88-MUX up to channel 96 (000-140).

⑧ REAL-TIME OUTPUT - With the addition of a high speed smart terminal, it may be possible to output data in real time (without storage) by rewriting statement 160, 161 and 164, 165 as shown below:

	OLD	NEW	
160	002	323	where XXX = desired I/O channel
161	003	XXX	
164	002	323	
165	003	XXX	

Note that the terminal must keep track of which byte is MSB/LSB and which bytes should be strung together as one sample point.
(The interrupt lines may be useful for a timing reference signal.)

1st Half of Sample Programs 2-II and 2-IV. A/D Block Storage Program

| OCTAL		DECIMAL		Op. Code (Octal)	Comments
Address	Data	Address	Data		
(037) 100	001	8000	1	LXIB	Setup start
101	(1)000	8001	0	DATA (1)	address of stored
102	040	8002	32		block of data.
103	076	8003	62	MVIA	
104	000	8004	0	[0]	
105	323	8005	211	OUT	
106	[200]	8006	128	CH.200	
107	323	8007	211	OUT	
110	[202]	8008	130	CH.202	Pre-initialize
111	323	8009	211	OUT	PIAs and define
112	[204]	8010	132	CH.204	as input/output
113	323	8011	211	OUT	devices.
114	[206]	8012	134	CH.206	
115	323	8013	211	OUT	
116	[205]	8014	133	CH.205	
117	323	8015	211	OUT	
120	[207]	8016	135	CH.207	
121	076	8017	62	MVIA.	
122	377	8018	255	[377]	
123	323	8019	211	CUT	
124	[201]	8020	129	CH.201	
125	323	8021	211	OUT -	
126	[203]	8022	131	CH.203	
127	076	8023	62	MVI	Sets up PIA0 (A)
130	004	8024	4	[004]	section for 8-
131	323	8025	211	OUT	channel MUX ad-
132	202	8026	130	CH.202	dress (if used).
133	076	8027	62	MVI	Sets up PIA0 so
134	054	8028	44	[054]	CB1 line pulses
135	323	8029	211	OUT	each time CH.
136	200	8030	128	CH.200	201 is output.
137	076	8031	62	MVIA	Sets up PIA1 for
140	(3)004	8032	4	[004](3)	status/interrupt
141	323	8033	211	OUT	flag in (B) section
142	204	8034	132	CH.204	from P1 pin 9 ( ).
143	076	8035	62	MVIA	Sets up PIA1 for
144	(4)004	8036	4	[004] (4)	status/interrupt
145	323	8037	211	OUT	flag in (A) section
146	206	8038	134	CH.206	
147	076	8039	62	MVIA	Selects one of eight
150	(5)[000]	8040	0	[000] (5)	MUX channels from
151	323	8041	211	OUT	on-board MUX (if
152	203	8042	131	CH.203	used).

At this point, initialization is complete. The remainder
of the program must be selected as either STD. CONFIG. Mode (A),
Program 2-II or SYNC Mode (B), Program 2-IV.

2nd Half of Sample Program 2-II. A/D Block Storage (STD. CONFIG. Mode)

OCTAL Address	OCTAL Data	DECIMAL Address	DECIMAL Data	Op. Code (Octal)	Comments
(037) 153	202	8043	195	JMP	Jump to strobe A/D.
154	166	8044	118	[ADD.]	
155	037	8045	31		
156	⑥333	8046	219	INPUT	Read (MSB) data
157	205	8047	133	CH.205(B)	byte and store.
160	⑧002	8048	2	STAX B	
161	003	8049	3	INR B INXB	Increment store address.
162	333	8050	219	INPUT	Read (LSB) data
163	207	8051	135	CH.207(A)	byte and store.
164	002	8052	2	STAX B	
165	003	8053	3	INR B INXB	Increment store address.
166	076	8054	62	MVIA	Strobe A/D for next
167	⑦000	8055	0	[000] ⑦	conversion.(Also set
170	323	8056	211	OUT	1 of 24 88-MUX chan-
171	201	8057	129	CH.201	nels, if used)
172	076	8058	62	LDA MVIA	Load end block store
173	②100	8059	64	[100] ②	address and compare
174	270	8060	184	CMP B	to see if block full.
175	312	8061	202	JZ	If full, jump to end
176	214	8062	140	[ADD.]	of program.
177	037	8063	31		
200	000	8064	0		Required delay for
201	000	8065	0		conversion to com-
202	000	8066	0		plete. (Can be
203	000	8067	0		replaced with in-
204	000	8068	0		structions to handle
205	000	8069	0		previously stored
206	000	8070	0		data bytes. But
207	000	8071	0		instruction time to-
210	000	8072	0		tal ≤ 18μsec. for
211	303	8073	195	JMP	maximum conversion
212	156	8074	110	[ADD.]	rate.) Jump back to read.
213	037	8075	31		
214	303	8076	195	JMP	Program end. Jump to
215	[ ]	8077	[ ]	[ADD.]	processing program or
216		8078			do a return.
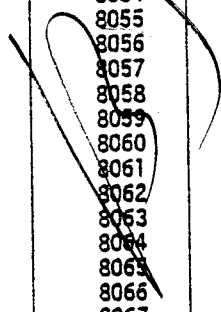
replace 303 w/ ___ (311)

34

076
000
323
201
074
377
323
201
303
000
000

303
034
000

323 — out 3/2 Apr
201 —

2H
129

Sample Program 2-III.   Fast A/D - STD. CONFIG. (65μs)

```
2   VI=10:BIAS=5
4   INPUT"PL,    CN";PL,    CN
6   FOP   J=0 TO CN:PRINT:PRINT"CH.#";J
8   POKE  8040,J:POKE  8055,J
10   POKE   8000,1:POKE  8001,0:POKE  8002,32:POKE  8003,62
20   POKE   8004,0:POKE  8005,211:POKE  8006,128
30   POKE   8007,211:POKE  8008,130:POKE  8009,211
40   POKE   8010,132:POKE  8011,211:POKE  8012,134
50   POKE   8013,211:POKE  8014,133:POKE  8015,211
60   POKE   8016,135:POKE  8017,62:POKE  8018,255
70   POKE   8019,211:POKE  8020,129:POKE  8021,211
80   POKE   8022,131:POKE  8023,62:POKE  8024,4
90   POKE   8025,211:POKE  8026,130:POKE  8027,62
100   POKE   8028,44:POKE  8029,211:POKE  8030,128
110   POKE   8031,62:POKE  8032,4:POKE  8033,211
120   POKE   8034,132:POKE  8035,62:POKE  8036,4
130   POKE   8037,211:POKE  8038,134:POKE  8039,62
140   POKE   8041,211:POKE  8042,131
150   POKE   8043,195:POKE  8044,118:POKE  8045,31
160   POKE   8046,219:POKE  8047,133:POKE  8048,2
170   POKE   8049,3:POKE  8050,219:POKE  8051,135
180   POKE   8052,2:POKE  8053,3:POKE  8054,62
190   POKE   8056,211:POKE  8057,129
200   POKE   8058,62:POKE  8059,64:POKE  8060,184
210   POKE   8061,202:POKE  8062,140:POKE  8063,31
220   POKE   8064,0:POKE  8065,0:POKE  8066,0
230   POKE   8067,0:POKE  8068,0:POKE  8069,0
240   POKE   8070,0:POKE  8071,0:POKE  8072,0
250   POKE  8073,195:POKE  8074,110:POKE  8075,31
260   POKE   8076,195:POKE  8077,64:POKE  8078,31
500   POKE   8076,201
510   POKE  73,64:POKE  74,31:REM USR ADDRESS
600   X=USR(Y)
700   FOR I=8194 TO 16384 STEP 2
850   LS=PEEK(I+1):MS=PEEK(I)
860   V=((16*MS+((LS/16)AND 15))*VI/4095)-BIAS
865   IF PL=1 THEN 2000
870   PRINTV,
900   NEXT I
1000   NEXT J:END
2000   D=36
2010   A=INT(V*5)
2020   X=D+A
2026   IF PL=0 THEN 2040
2030   PRINT TAB(X)"*"
2040   GOTO 900
OK
```

PL = 1 for PLOT; 0 for NO PLOT
CN = last ch. # to be read
Change statement 2 for proper module voltage range

A/D BLOCK STORE (cont.)

OCTAL		DECIMAL		Op. Code (Octal)	Comments
Address	Data	Address	Data		
(037) 153	303	8043	195	JMP	Jump to status check.
154	176	8044	127	[ADD.]	
155	037	8045	31		
156	(6)333	8046	219	INPUT	Read (LSB) data byte
157	207	8047	135	CH.207(A)	and store.
160	(8)002	8048	2	STAX B	
161	003	8049	3	INXB	Increment store address.
162	333	8050	195	INPUT	Read (MSB) data byte
163	205	8051	133	CH.205(B)	and store.
164	002	8052	2	STAX B	
165	003	8053	3	INCR B	Increment store address.
166	333	8054	195	INPUT	Check status CH. 204
167	204	8055	132	CH.204	(wait in loop until Bit
170	027	8056	23	RAL	7 is set HIGH).
171	322	8057	210	JNC	(3)
172	166	8058	118	[ADD.]	~13µs
173	037	8059	31		
174	076	8060	62	076	Strobe A/D for next
175	(7)000	8061	0	[000] (7)	conversion. (Also set
176	323	8062	211	OUT	1 of 24 88-MUX chan-
177	201	8063	129	CH.201	nels, if used)
200	076	8064	62	076	Load end block store
201	(2)100	8065	64	[100] (2)	address and compare to
202	270	8066	184	CMPB	see if block full. If
203	312	8067	202	JZ	full, jump to end of
204	222	8068	146	[ADD.]	program.
205	037	8069	31		
206	000	8070	0		Required delay for
207	000	8071	0		conversion to complete.
210	000	8072	0		(Can be replaced with
211	000	8073	0		instructions to handle
212	000	8074	0		previously stored data
213	000	8075	0		bytes. But instruction
214	000	8076	0		time total ≤ 18µsec. for
215	000	8077	0		maximum conversion rate.)
(037) 216	000	8078	0		Last delay NOP. Now
217	303	8079	195	JMP	jump back to read.
220	156	8080	110	[ADD.]	
221	037	8081	31		
222	303	8082	195	JMP	Program end. Jump to
223	[ ]	8083	[ ]	[ADD.]	processing program or
224		8084	[ ]		do a return.

Sample Program 2-V. Fast A/D - SYNC Mode (78µs)

```
2   VI=10:BIAS=5
4   INPUT "PL,    CN";PL,    CN
6   FOR J=0 TO CN:PRINT:PRINT"CH.#";J
8   POKE   8040,J:POKE   8061,J
10  POKE   8000,1:POKE   8001,0:POKE   8002,32:POKE   8003,62
20  POKE   8004,0:POKE   8005,211:POKE   8006,128
30  POKE   8007,211:POKE   8008,130:POKE   8009,211
40  POKE   8010,132:POKE 8011,211:POKE   8012,134
50  POKE   8013,211:POKE   8014,133:POKE   8015,211
60  POKE   8016,135:POKE   8017,62:POKE   8018,255
70  POKE   8019,211:POKE   8020,129:POKE   8021,211
80  POKE   8022,131:POKE   8023,62:POKE   8024,4
90  POKE   8025,211:POKE   8026,130:POKE   8027,62
100   POKE   8028,44:POKE   8029,211:POKE   8030,128
110   POKE   8031,62:POKE   8032,4:POKE   8033,211
120   POKE   8034,132:POKE   8035,62:POKE   8036,4
130   POKE   8037,211:POKE   8038,134:POKE   8039,62
140   POKE   8041,211:POKE   8042,131
150   POKE   8043,195:POKE   8044,127:POKE   8045,31
160   POKE   8046,219:POKE   8047,135:POKE   8048,2
170   POKE   8049,3:POKE   8050,219:POKE   8051,133
180   POKE   8052,2:POKE   8053,3:POKE   8054,219
190   POKE   8055,132:POKE   8056,23:POKE   8057,210
200   POKE   8058,118:POKE   8059,31:POKE   8060,62
210   POKE   8062,211:POKE   8063,129
220   POKE   8064,62:POKE   8065,64:POKE   8066,184
230   POKE   8067,202:POKE   8068,146:POKE   8069.31
240   POKE   8070,0:POKE   8071,0:POKE   8072,0
250   POKE   8073,0:POKE   8074,0:POKE   8075,0
260   POKE   8076,0:POKE   8077,0:POKE   8078,0
270   POKE   8079,195:POKE   8080,110:POKE   8081,31
280   POKE   8082,195:POKE   8083,64:POKE   8084,31
500   POKE   8032,5:POKE   8036,5:POKE   8082,201:REM SETUP FLAGS&RETURN
510   POKE   73,64:POKE   74,31:REM USR ADDRESS
600   X=USR(Y)
700   FOR I=8194 TO 16384 STEP 2
850   MS=PEEK(I+1):LS=PEEK(I)
860   V=((16*MS+((LS/16)AND 15))*VI/4095)-BIAS
865   IF PL=1 THEN 2000
870   PRINTV,
900   NEXT I
1000   NEXT J:END
2000   D=36
2010   A=INT(V*5)
2020   X=D+A
2026   IF PL=0 THEN 2040
2030   PRINTTAB(X)"*"
2040   GOTO 900
OK


PL = 1 for PLOT; 0 for NO PLOT
CN = last ch. # to be read
Change statement 2 for proper voltage range
```
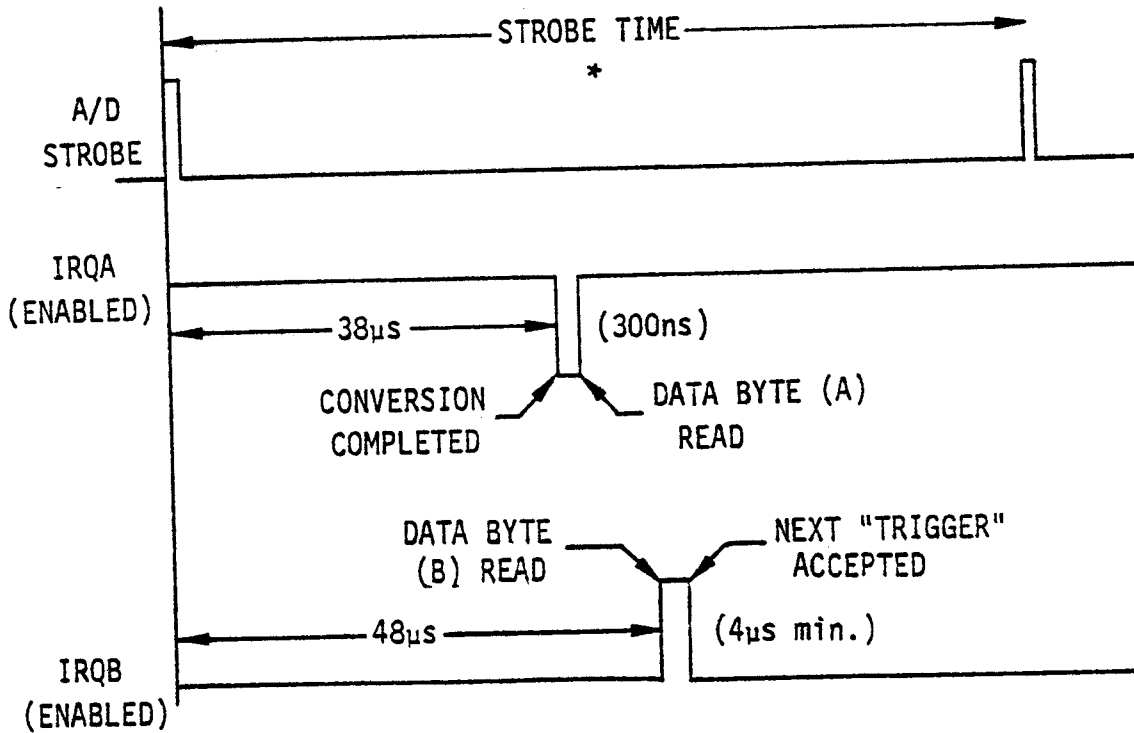
The following timing diagram is given for SYNC Mode (B)
with statements 140 and 144 = 005 to enable interrupts.

*STD. CONFIG. : 65μsec. MIN
 SYNC Mode   : 78μsec. MIN, not including 13μsec. unknown
                              "window" (see text)

Figure 2-5. Timing Diagram for SYNC Mode

2-9. MOS IC SPECIAL HANDLING PRECAUTIONS

There is one MOS integrated circuit on the 88-ADC board, IC U.
The IC is very sensitive to static electricity and transient voltages.
In order to prevent damage to the component, read over the following
precautions and adhere to them as closely as possible. FAILURE TO DO SO
MAY RESULT IN PERMANENT DAMAGE TO THE IC.

a) All equipment (soldering iron, tools, solder, etc.) should be
at the same potential as the PC board, the assembler, the work
surface and the IC with its container. This can be accomplished
by continuous physical contact with the work surface, the com-
ponents and everything else involved with the operation.

b) When handling the IC, develop the habit of first touching the
conductive container in which it is stored before touching the
IC itself.

c) If the IC has to be moved from one container to another, touch
both containers before doing so.

d) Do not wear clothing which will build up static charges. Pre-
ferably wear clothing made of cotton rather than wool or syn-
thetic fibers.

e) Always touch the PC board before touching the IC to the board.
Try to maintain this contact as much as possible while instal-
ling the IC.

f) Handle the IC by the edges. Avoid touching the pins themselves
as much as possible.

g) Dry air moving over plastic can build up considerable static
charges. Avoid placing the IC near any such area or object.

altair 8800

CONVERSION SYSTEM
SECTION III
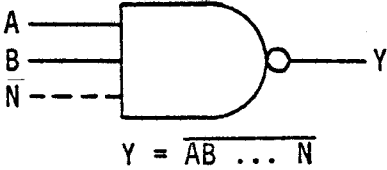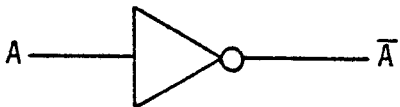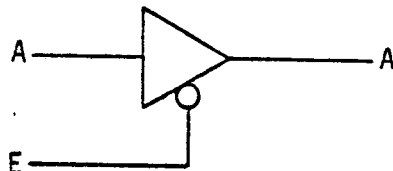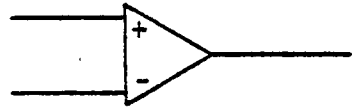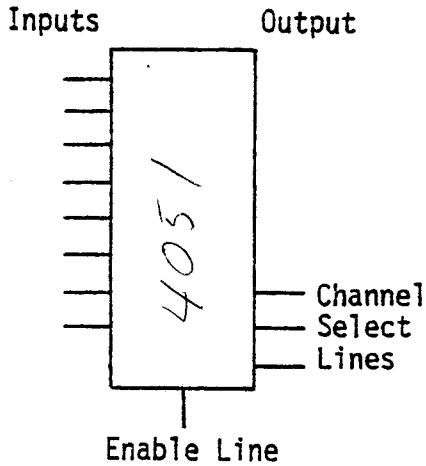## THEORY OF OPERATION

3-1. GENERAL

Section III provides a detailed theory explanation of the circuit contained within the 88-ADC and 88-MUX boards, including a description of the logic symbols used in the schematics.

Although most applications will utilize either the 8-channel or 24-channel multiplexer system, the input signal for the 88-ADC board can bypass the multiplexer system independently through connector P1. This section will describe how the input signal can enter directly through P1, through the 8-channel multiplexer on the 88-ADC board, or through the 24-channel 88-MUX board.
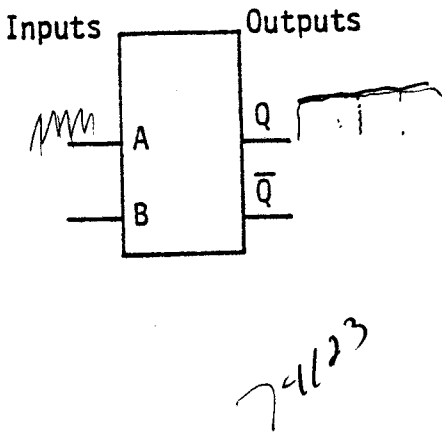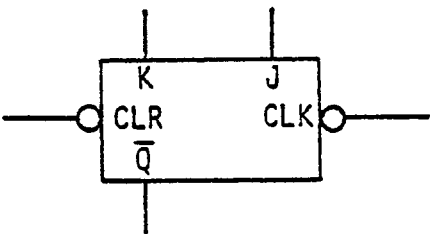
3-2. LOGIC CIRCUITS

The logic circuits used in the 88-ADC (Figure 3-2) and 88-MUX (Figure 3-3 and 3-4) schematics are presented in Table 3-1. The table provides the functional name, symbolic representation and brief description of each logic circuit. Where applicable, a truth table is furnished to aid in understanding circuit operation. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH. Note that LOW active signals are written with a bar on top and the absence of such a bar signifies an active HIGH signal level.

Table 3-A.   Symbol Definitions

NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate	A B N $Y = \overline{AB \ldots N}$	The NAND gate performs one of the fundamental logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output. The output is HIGH if any of the inputs are LOW.
Inverter	A ——⊳○—— $\overline{A}$	The inverter is a device whose output is the opposite state of the input.
Non-Inverting Bus Driver	A ——⊳—— A E	The non-inverting bus driver is a device whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input. When disabled, the outputs enter a high impedance state.
Operational Amplifier	+ −	The operational amplifier is a device that is operated as a buffer for analog (linear) signals.
CMOS Multiplexer	Inputs Output 4051 Channel Select Lines Enable Line	The CMOS multiplexer outputs one of eight input channels, depending on the code received at the channel select lines.

Table 3-A. Symbol Definitions (Contd)

NAME	LOGIC SYMBOL	DESCRIPTION
Dual Retriggerable Monostable Multivibrator	Inputs Outputs A Q B $\overline{Q}$ 74123	A monostable multivibrator has but one stable state from which it can be triggered to change states for a predetermined interval. External capacitance and resistance are selected to achieve a desired pulse width. Retriggerable means that before the output pulse is terminated, the input can be triggered again, allowing output pulses of long durations. The A input must go LOW while the B input is held HIGH to initiate an output pulse.
J-K Dual Flip-Flop with Clear	K J CLR CLK $\overline{Q}$	The output of this flip-flop can be modified by conditioning the J and K inputs HIGH or LOW. Data is transferred to the output on the falling edge of the clock pulse. The CLEAR (CLR) input overrides the CLOCK (CLK) and DATA inputs and sets the Q output LOW.

3-3. 88-ADC INPUT BUFFER AMPLIFIER (Figure 3-2)

The input signal origin for the 88-ADC is through connector P1, pins 1 and 2 (zone D3). (P1 pin 1 = (+) input, and P1 pin 2 = ground.) The voltage gain from the buffer amplifier (IC B, zone C3) is given by the ratio $V_{OUT} = V(R_3 + R_4)/R_3$ and is strictly a function of R_3 and R_4 where V_{OUT} = voltage out of amplifier (IC B) pin 6 and V = voltage present at pin 3. If R_3 is not installed, the gain will be unity which is the standard configuration. Input scaling can be realized by proper selection of R_5 and R_6 as given by $V = V_{IN}(R_5)/(R_5 + R_6)$ where V_{IN} = voltage at P1 pin 2 and V = voltage at amplifier (IC B) pin 3. R_5 and C7 can be selected to provide the desired roll-off response.

3-4. A/D MODULE (Figure 3-2)

The A/D module (see Figure 3-1, A/D Module Internal Block Diagram) is operated as a successive approximation register with the following internal sections: clock, binary counter/shift register (CSR), digital to analog converter (DAC) and comparator circuit. On the leading edge of a positive going START conversion pulse pin 34 (zone C5), the BUSY signal pin 33 is latched and the most significant bit (MSB) pin 72 (zone C4) of the (CSR) is set up to be tested first. The MSB is set True, resulting in a corresponding (DAC) output. The DAC provides an analog output voltage which is dependent on the binary code input. This analog voltage output is compared to the input signal within the comparator and a digital True (1) or False (0) signal is clocked into the proper bit location in the (CSR) register. The process is then repeated, using the next most significant bit. This results in a string of True or False binary weighted bits which are shifted into the register until the least significant bit (LSB) has been "tested" and the comparator toggles True. Completion of the (LSB) test indicates "equality" of the digitally encoded DAC output and input signals. Once the LSB has been "tested," the BUSY signal goes LOW and the digitally coded voltage may be read as valid. Note that during "conversion" time, the data output lines will be toggling back and forth between HIGH and LOW states and will not be stable until after the LSB has been tested and the BUSY signal goes LOW.
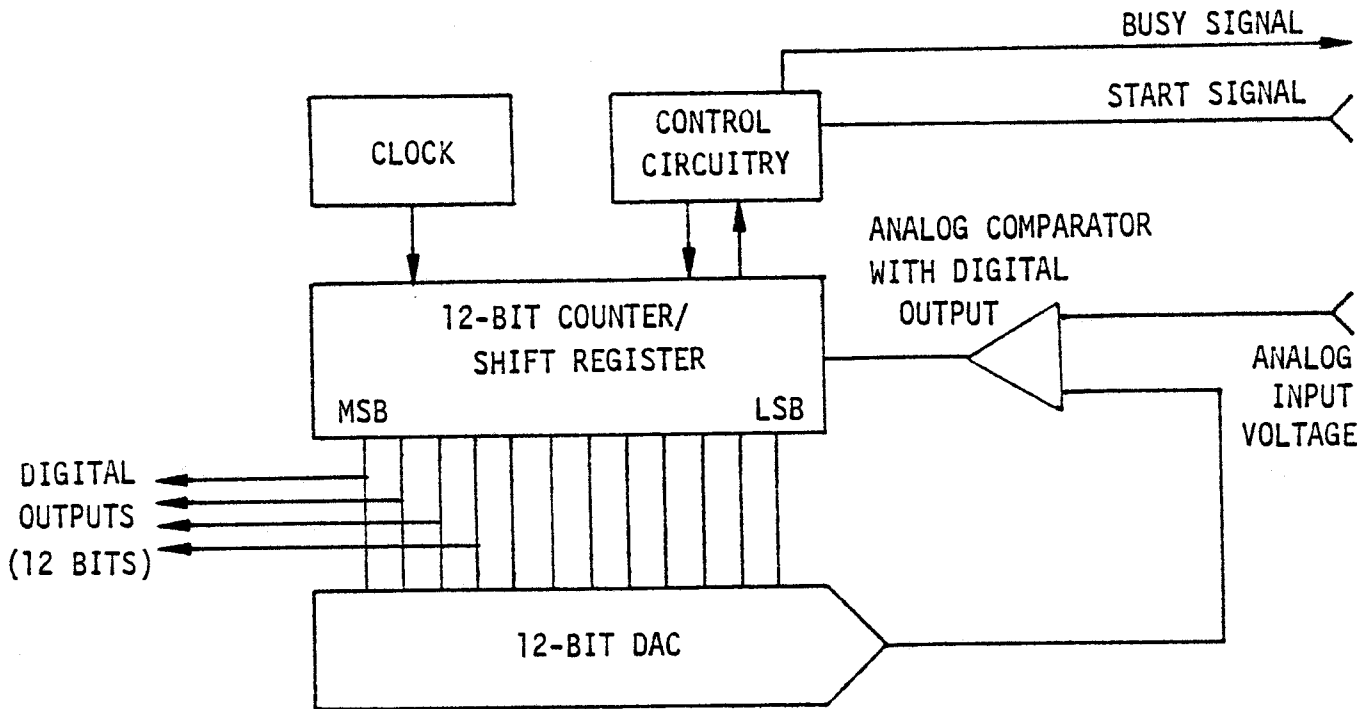
Figure 3-1. A/D Module Internal Block Diagram

3-5. CONTROL SIGNALS (Figure 3-2)

Card selection for the 88-ADC is accomplished by ICs G, H, J and K (zones B6, B7 and A7). Jumpers I3 through I7 are used to establish the address code as shown in Table 3-B.

Table 3-B. Address Selection

JUMPER	ADDRESS LINE	I/O ADDRESS (DECIMAL)	EXAMPLE: CHANNEL # =	
I3	A3	8	$\overline{A3}$	
I4	A4	16	$\overline{A4}$	
I5	A5	32	$\overline{A5}$	= Octal 200
I6	A6	64	$\overline{A6}$	or Decimal 128 (Std. Config.)
I7	A7	128	A7	

NAND gate G pin 11 and pin 8 (zone B6) generate input or output signals to or from the CPU, respectively. These signals are used to enable the bus output drivers S and P (zone A5 and A4) and input drivers S and R (zone A3). They are also used to strobe the R/W lines on PIAs M and N pins 21 (zone B4 and B3, respectively). The R/W line determines in which direction data will flow through the PIA. The output of G pin 6 (zone B6) sets the CS1 control lines HIGH on PIA-M and PIA-N pin 24 on <u>either</u> an input or an output and this enables the PIA.

Upon receiving a Read command, the PDBIN signal is inverted to the input of NAND gate G pin 1 (zone B6). With a Write, the $\overline{PWR}$ signal goes directly to input pin 2 of G. The output of G pin 3 strobes the "E" lines pin 25 of the PIAs with a positive going pulse. The "E" pulse strobes data or control signals into the PIA internal registers.

A WAIT state must be introduced during an input to the CPU from the 88-ADC because of the inherent slowness of the PIA latches as compared to the CPU speed. This is accomplished by ICs G, E, F and H. When the E flip-flop (zone C6) is set HIGH, the $\overline{Q}$ output pin 13 goes LOW, causing PRDY to remain LOW and a temporary HALT in processing occurs. The PWAIT line, returning from the CPU, will be set HIGH after one WAIT state (500 ns.) This clears the E flip-flop through ICs F and H (zone C7) and processing resumes.

The E flip-flop and PIAs M and N are also cleared with a Power-On Clear ($\overline{POC}$) command from the CPU card during the power up condition. The lower order address lines AØ (LSB), A1 and A2, which comprise the last byte of the channel address, are decoded by PIAs M and N to provide the access pattern shown in Table 3-C. For example, an output command to channel 131 would decode lines A2=LOW, A1=HIGH and AO=HIGH. Thus, PIA-N, Section A, Data Channel is selected.

Table 3-C.   Channel Address vs. PIA Enables

	(A̅2̅) PIA 0 Enabled Binary Address Code		(A2) PIA 1 Enabled Binary Address Code	
	(A̅1̅) Section B	(A1) Section A	(A̅1̅) Section B	(A1) Section A
(A̅0̅) Status Channel Binary Address Code*	128	130	132	134
(A0) Data Channel Binary Address Code*	129	131	133	135

*Decimal Address

To begin conversion, the D one-shot (zone C6) is used to generate the START pulse to the A/D module. The standard configuration of the 88-ADC board uses the <u>CB2</u> line pin 19 (zone B2) of PIA-N to strobe the D one-shot. The proper initialization codes (Program 3-I, page 43) must be received by the PIA.

These codes may be modified as described within the sample program in Section 2-8, although the START pulse always consists of a LOW going transition of CB2.

The START signal can generate one BEGIN CONVERSION command (100ns minimum), but the conversion must be completed and processed before another pulse is applied. The time is dependent on the software being utilized, from ∿65μsec. in STD. CONFIG. up to ∿1 sec. using BASIC only. The STATUS line (P1 pin 8) can be monitored, indicating whether the A/D module is busy or ready to accept another conversion command. However, software processing is asynchronous to the hardware STATUS signal so caution is advised for real time high speed operation. For true monitor capability, the card can be set up as described in Section 2-8(B), Synchronous Mode.

The binary address code for the desired multiplexer channel is latched by PIA-N. The MA0 through MA7 signals (zone B2) can be set to 0 or 1 by generating the proper output code (Table 4-A, page 55) to the PIA. These signals are output on connector P1 for use by the 88-MUX card(s).

The PA0, PA1 and PA2 signals (zone B2) are generated in a similar manner to MA0 through MA7 and these are input to the 8-channel multiplexer, IC U, on the 88-ADC board. These signals from PA0, PA1 and PA2 select one of eight input channels, AX0 through AX7, which are input via connector P2 (refer to Table 4-B, page 63). Input protection for the 88-MUX is provided by diodes D1 through D16 (zone D1), resistors R16 through R23 (zone D2), resistors R24 through R28 and transistor Q2. Voltages larger than the supply voltages for the multiplexer IC U are "clamped" by this circuitry.

3-6. 88-MUX 24-CHANNEL MULTIPLEXER (Figure 3-3)

The CMOS 4051 Multiplexers (zones B7, B5 and B2) are controlled by means of the A, B, C and EN inputs. MUX-A is enabled for channels 0 through 7, MUX-B is enabled for channels 8 through 15, and MUX-C for channels 16 through 23. The $\overline{EN}$ signal pin 6 allows coupling of one of eight channels through the proper MUX IC to its output pin 3. Pins 3 of the three multiplexer ICs A, B and C go directly to the output buffer amplifier and to P1 pin 5, the MUX 1 output signal. The A, B and C signal pins 11, 10 and 9, respectively, select the binary code for the particular channel desired. Refer to the table in Figure 3-4, zone B1 and B2.

3-7. PIA INITIALIZATION AND DATA INTERPRETATION

It may also be useful to refer to Section 2-8 before reading this section.

In order to read the 88-ADC card, the PIAs must be initialized for data flow direction and control signal flags. Program 3-I is an example of 8K BASIC PIA initialization for an 88-ADC board strapped at channel 128. Note that the channel and data numbers are in decimal.

Program 3-I. PIA Initialization

```
 80  OUT  130,0
 90  OUT  131,255        Initialize PIA 0-B Section for 24 Channel
100  OUT  130,4                                        MUX Selection
110  OUT  128,0
120  OUT  129,255        Initialize PIA 0-A Section for 8 Channel
130  OUT  128,4                                        MUX Selection
140  OUT  134,0                                        and/or Strobe A/D
150  OUT  135,0          Initialize PIA 1-B Section for Most Significant
160  OUT  134,4                                        8 Bits of A/D
170  OUT  132,0
180  OUT  133,0          Initialize PIA 1-A Section for Least Significant
190  OUT  132,4                                        Bits of A/D
```

*For each PIA section, the first CH. # represents the Control/Status
Channel, 130 in line 80, and the second CH.# represents either the Data
Channel, 131 in line 90, or the Direction Channel, depending on the
status word at that time. For example, if bit 3 of the status word is
LOW, channel #131 represents the Direction Register and if bit 3 is
HIGH, channel #131 represents the actual Data Channel. Normally, the
Direction Register will be written into only once in the program
during initialization. From then on, the only channel accessed will be
the actual Data Channel.

After processing lines 80 through 190, initialization is complete and the multiplexer channel can be set up as follows:

| 8-Channel MUX | 24-Channel MUX |

200 OUT 131, CH.   CH. = (0-7)   :   OUT 129, CH.   CH. = (0-96)

The second half of statement 200 (OUT 129, X) also strobes the A/D module to begin a conversion. After approximately 50 microseconds, the conversion is complete and the A/D module is waiting to be read by the CPU:

210 MS = INP (133) : LS = INP (135)

The first instruction reads the <u>eight most significant</u> bits, the second reading the <u>four least significant</u> bits. By adding the voltage factors for the four least significant bits with masking and "weighting" the following statement can be written:

220 V = ((16*MS + ((LS/16) and 15)*VI/4095) - BIAS

where VI = input voltage span (5, 10 or 20 volts) and BIAS = 0 for unipolar, 5 for (-5 to +5 volts) or 10 for (-10 to +10 volts). Statement 220, when combined with statement 210, will calculate an equivalent voltage (V) corresponding to the total bit count and total voltage span desired. For example, for a (0 to +10 volt) range, VI = 10.0 and BIAS = 0, and the voltage in volts is read out directly.

For only eight significant bits, statement 220 can be rewritten as follows:

220 V = (16 * MS * VI/4095) - BIAS

resulting in a corresponding increase in processing speed due to the fact that only one input instruction is required and the computations are greatly simplified.

altair 8800
CONVERSION SYSTEM
SECTION IV
TROUBLESHOOTING

4-1. INTRODUCTION

Section IV is designed to aid in the location of malfunctions that could be encountered after the Altair 88-ADC and 88-MUX boards are installed in the 8800a or 8800b computer. Before installation of the board, it should be visually inspected according to the visual inspection check list. The troubleshooting tests will vary slightly, depending on whether the 8-channel or 24-channel multiplexer is utilized.

> ### WARNING
> Always disconnect power when removing the board, cutting or resoldering PC lands and removing or installing ICs.

4-2. VISUAL INSPECTION CHECK LIST

Before the 88-ADC or 88-MUX boards are installed, it is important to check the component assembly and etching of lands. Although the boards should be assembled correctly, an extensive inspection may eliminate possible malfunctions.

1. General

   Carefully examine the board for the following:

   a. leads that have not been soldered

   b. solder bridges

   c. cold solder connections

   d. errors such as hairline opens in lands

2. Component Check

   Using the silkscreen diagram (Figure 4-1 or 4-2) as a guide, check the following:

   a. proper polarity of capacitors

   b. proper polarity of diodes

   c. correct color codes on all resistors

   d. proper pin placement and good solder connections
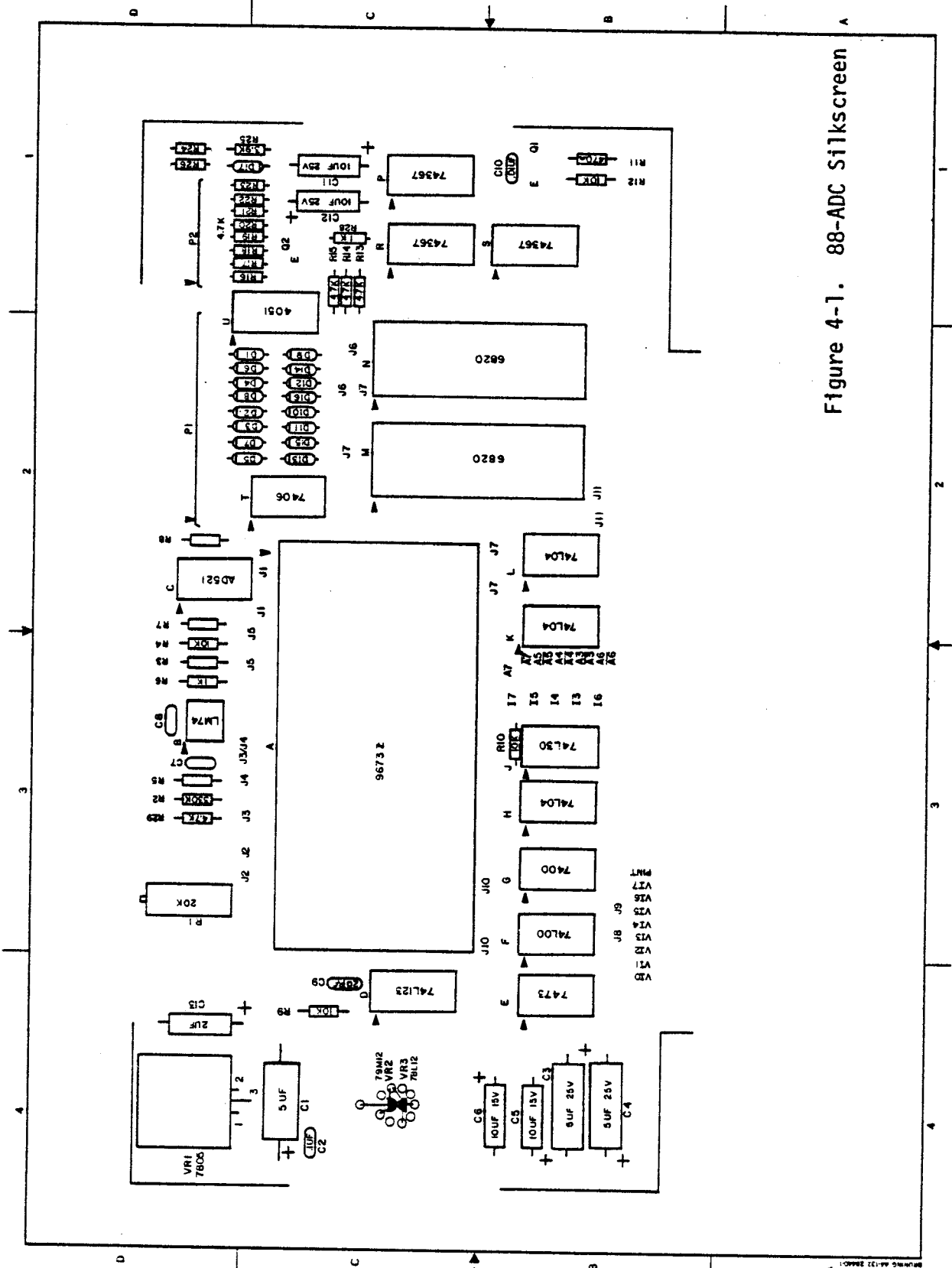
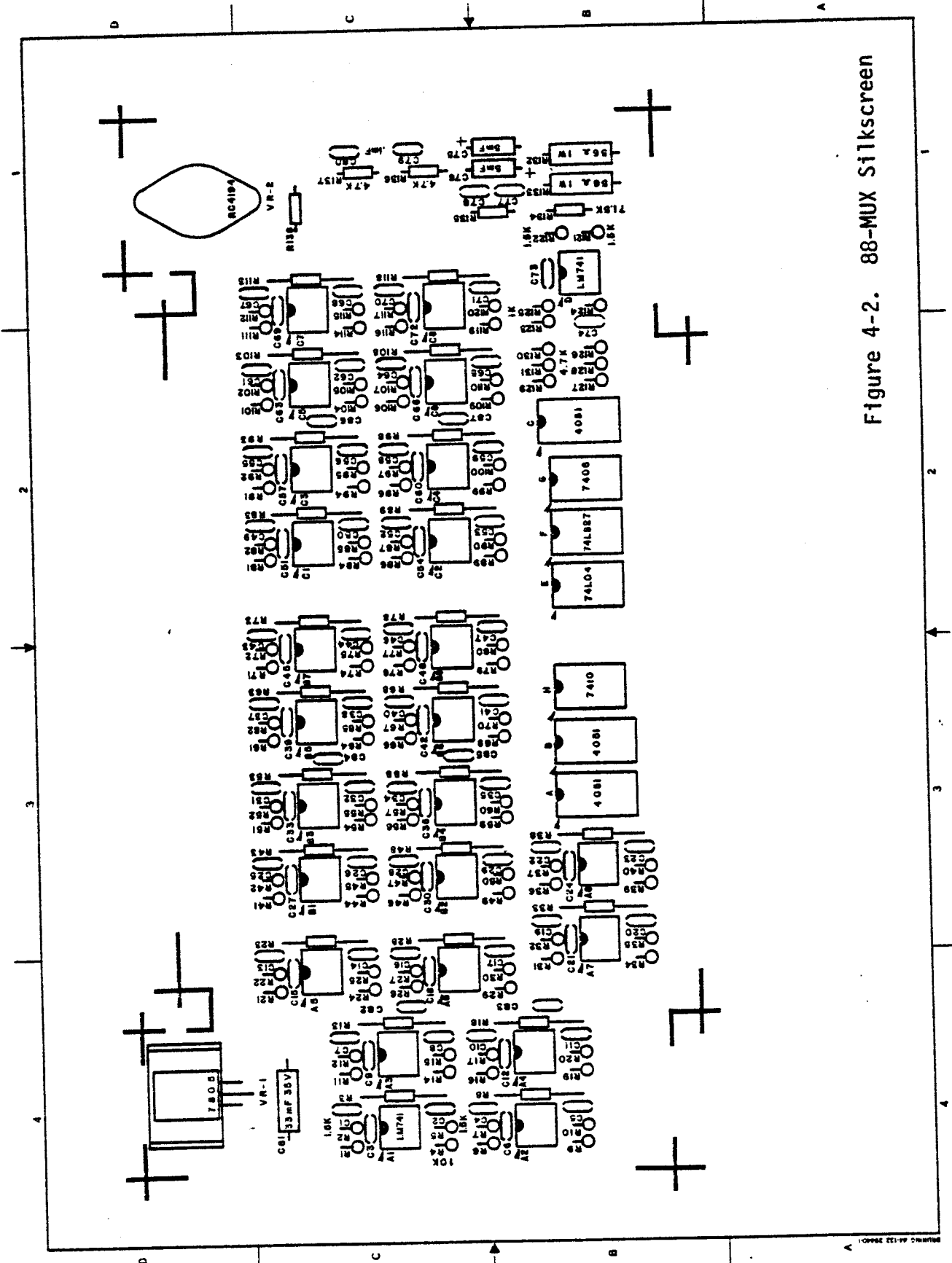   e. proper placement of all components

Figure 4-1. 88-ADC Silkscreen

Figure 4-2. 88-MUX Silkscreen

4-3. GENERAL CHECK

The following items are important factors to be considered when troubleshooting the overall system:

a. Has the system worked previously?
   A PC assembly error (such as a solder short) is less probable for a setup that has operated prior to this check, unless the board has since been modified.

b. Does the program match the system configuration?
   Note that depending on whether the 8-channel or 24-channel MUX is accessed, the program contents are slightly different. Also, is the addressing of the A/D correct?

c. Improper voltages?
   Too high a voltage will saturate the input buffer amplifier. If the A/D card is jumpered incorrectly, the A/D module itself can be saturated, resulting in an unvarying output near full scale. "Floating" inputs to the 8-channel MUX will also appear as saturated. If this is an undesirable feature, unused inputs to the cable should be grounded. Also, note that time-variant voltages can cause unusual results since the computer runs asynchronous to them.

d. Is the problem on one or all channels?
   This is a very significant factor when troubleshooting. All channels except one, point strongly toward the multiplexer section rather than the A/D.

e. UNDER NO CIRCUMSTANCES SHOULD THE A/D MODULE ITSELF BE TAMPERED WITH.
   If the module is suspect, please return the entire card with a description of the problem for a complete factory checkout.

4-4. PRELIMINARY CHECK

After visual inspection and installation of the board(s), check the address and data lines for shorts and opens. All the preliminary checks are implemented with the machine On and in the Stop mode. Each of the 16 address switches on the front panel should be in the down position initially and switched to the up position individually while positioning the EXAMINE/EXAMINE NEXT* switch on the front panel to EXAMINE for each address switch setting. Observe that the corresponding LED is On. After all the switches are up, return them individually to the down position, and observe that the adjacent LED is OFF. If one LED fails during this check, or if several LEDs fail at the same time, there are possible address problems on the board(s). The board should be removed and a resistance check made on the bus pins corresponding to the address lines showing the incorrect indications. If the resistance reading indicates there is a short or open in the circuit, trace the land from the bus until the problem is isolated.

Data lines are checked in much the same manner. Address switches A0-A7 correspond to data lights D0-D7. These address switches are initially in the down position. Place A0 up and position DEPOSIT/ DEPOSIT NEXT** switch on the front panel to DEPOSIT and observe that the D0 LED is On. Place each of the address switches individually HIGH while positioning DEPOSIT/DEPOSIT NEXT switch on the front panel to DEPOSIT NEXT and observe that each corresponding LED comes On. Return all front panel address switches to the LOW position. Position EXAMINE/ EXAMINE NEXT switch on the front panel to EXAMINE to recall data stored in the first address. Repeatedly place the EXAMINE/EXAMINE NEXT switch on the front panel to EXAMINE NEXT. This will enable the machine to read the data that was stored in the successive memory locations to verify data was deposited.

If one LED fails during this check, or if more than one LED fails at the same time, there is a possible data problem on the board(s).

* If the board(s) is being used with the 8800a, the front panel will read EX NEXT.

** If the board(s) is being used with the 8800b, the front panel will read DEP NEXT.

4-5. MUX ISOLATION TEST (8 Channel or 24 Channel MUX System)

a. Remove the 8800-302 cable from the 88-ADC connector P1 if a 24-channel system (88-MUX) is utilized. For an 8-channel multiplexer system, remove IC U from the 88-ADC board. Refer to the CMOS Special Handling Precautions on page 32.

b. Connect a stable voltage source, preferably a flashlight battery (1.5 volt), between pins 1(+) and 2(gnd) of connector P1.

c. Enter Program 4-I to loop on one channel.

Program 4-I. MUX Isolation Test

This program will read up to 96 channels with an 88-MUX
system, up to 8 channels with the on-board 8-channel MUX,
or directly through the 88-ADC without a multiplexer.
SA is the number of samples desired at each channel.

```
10   REM TO READ ONLY ONE CHANNEL CHANGE 70 : I = (DESIRED CH.#) AND
20   REM DELETE STATEMENT 240
30   REM CH.# IS THE LAST CHANNEL YOU WANT TO TEST
50   INPUT"ENTER VI";VI
60   INPUT"ENTER BIAS";BIAS
65   INPUT"CH.#";CN
68   INPUT"ENTER SAMPLES";SA
70   I=0
72   PRINT:PRINT"CH.#";I
75   FOR J=0 TO SA
80   OUT130,0
90   OUT131,255
100  OUT130,4          OUT 130, 46
110  OUT128,0
120  OUT128,255        OUT 129, 255
130  OUT128,4          OUT 128, 46
140  OUT134,0
150  OUT135,0
160  OUT134,4 22       OUT 134, 22
170  OUT132,0
180  OUT133,0
195  OUT132,4 22       OUT 132, 22
200  OUT131,I:OUT129,I
210  MS=INP(133):LS=INP(135)
220  V=((16*MS+((LS/16)AND 15))*VI/4095)-BIAS
230  PRINTV;
235  NEXT J
OK
```

SELECTED V. SPAN	VI=	BIAS=
0 ← 5v	5	0
0 ← 10v	10	0
-5 → +5v	10	5
-10 → +10v No MUX	20	10

d. If the computer now prints the correct answer, the problem is within the cable, the multiplexer itself or the channel code output by the 88-ADC to the 88-MUX.
For problems related to the multiplexer, proceed to the following sections, depending on which system you have:
8-Channel system - Section 4-15
24-Channel system - Section 4-6

e. If the computer still does not print the correct answer, proceed to Section 4-10. This section is concerned with problems relating to the A/D module.

4-6. <u>CABLE CHECK (24-Channel System)</u>

a. Visually check the cable assembly carefully for misalignment and make sure it is firmly seated. Refer to Figure 2-2a, 24-channel MUX Cable Layout (page 12).

b. Check for broken or bent pins (shorts) and broken wires.

```
┌─────────────────────────────────────────┐
│                 WARNING                  │
│ Pins on this connector are fragile and will │
│ break if improperly handled.            │
└─────────────────────────────────────────┘
```

c. It may be necessary to remove and re-seat the connector and repeat Program 4-I.

4-7. <u>A/D CHANNEL CODE CHECK</u>

If the system still fails, the A/D channel code must be checked. These signals (MA0 through MA7) are output from the 88-ADC (IC N) as standard logic levels and should follow the standard binary code which is dependent on the channel number input to Program 4-I.

a. Referring to Table 4-A, check these signals at the 100-pin edge connector on the top of the 88-MUX card.

b. If the code is correct, proceed to Section 4-8.

c. If the code is not correct, substitute IC M for IC N.

d. If the code is now correct, replace the bad PIA. If the code is still incorrect, refer to Section 4-13, PIA Check.

Table 4-A. Binary Channel Code

SELECTED CHANNEL #	MA0 (pin 16)	MA1 (pin 17)	MA2 (pin 18)	MA3 (pin 20)	MA4 (pin X)	MA5 (pin V)	MA6 (pin U)	MA7 (pin T)
0 '	L	L	L	L	L	L	L	L
1	H	L	L	L	L	L	L	L
2	L	H	L	L	L	L	L	L
3	H	H	L	L	L	L	L	L
4	L	L	H	L	L	L	L	L
5	H	L	H	L	L	L	L	L
6	L	H	H	L	L	L	L	L
7	H	H	H	L	L	L	L	L
8	L	L	L	H	L	L	L	L
9	H	L	L	H	L	L	L	L
10	L	H	L	H	L	L	L	L
11	H	H	L	H	L	L	L	L
12	L	L	H	H	L	L	L	L
13	H	L	H	H	L	L	L	L
14	L	H	H	H	L	L	L	L
15	H	H	H	H	L	L	L	L
16	L	L	L	L	H	L	L	L
17	H	L	L	L	H	L	L	L
18	L	H	L	L	H	L	L	L
19	H	H	L	L	H	L	L	L
20	L	L	H	L	H	L	L	L
21	H	L	H	L	H	L	L	L
22	L	H	H	L	H	L	L	L
23	H	H	H	L	H	L	L	L
Corresponding Signal Names	A	B	C	BEN	CEN			

H = HIGH level (True) = +(2 - 4)v.D.C.

L = LOW level (False) = +(.2 - .6)v.D.C.

4-8. 88-MUX CHECK (4051)

If the channel code is correct, and the problem has been isolated to the 88-MUX, it is necessary to check the multiplexer ICs A, B and C.

    a. By repeating Program 4-I and referring to Table 4-A, the correct code should be seen on each multiplexer IC (A, B or C).

    b. Depending on the channel group selected, only one MUX IC should have pin 6 LOW (enabled). The other multiplexer ICs (pin 6) should be HIGH (disabled).

    c. Pins 9, 10 and 11 should correspond to inverted signals A, B and C as shown in Table 4-A.

    d. If these codes are correct, proceed to Section 4-9.

    e. If these codes are not correct, replace ICs G, F or E. Insure that the connector is properly seated and aligned and that all wires are intact.

4-9. 88-MUX INPUT BUFFERS

The final check of the 88-MUX is the input buffer itself. Note that there are 24 identical amplifier circuits which are "on line" at all times. The outputs of each group of 8 terminate at MUX A, B or C.

    a. Each buffer circuit can be monitored at its respective MUX IC pin (1, 2, 4, 5, 12, 13, 14, 15) by applying input signal voltages to the cable. Failure at any pin isolates that particular buffer circuit.

    b. After isolating the respective buffer circuit, check for correct signal level at input pin 3 of the appropriate (741) operational amplifier.

    c. If the signal is not present, check the cable and connector for the respective buffer circuit to locate a possible break or short.

    d. If the signal is present but the amplifier does not output the correct level, check for bent or broken components on the respective buffer circuit.

    e. If the failure is still present, replace the (741) amplifier.

This completes the 24-Channel MUX troubleshooting section.

4-10. POWER SUPPLY VOLTAGES ON THE 88-ADC BOARD

The problem is possibly on the 88-ADC. It is first necessary to check the supply voltages.

    a. Monitor the following voltages directly on the A/D module pins, being careful not to short any wires together.

Voltages	A/D Module Pins
+5v ± .5v DC	pin 29
+12v ± .5v DC	pin 27
-12v ± .5v DC	pin 25

    b. If the voltages are correct, proceed to Section 4-11.

    c. If the voltages are not correct, check for 88-ADC board mis-alignment, power supply failure or regulator failure (79M12, 78L12 or 7805).

4-11. A/D MODULE START PULSE

If the power supply voltages are correct, check the A/D START signal with a scope.

    a. IC D pin 13 should pulse HIGH for approximately 150ns each time the 88-ADC board is read by Program 4-I (loop on one channel).

    b. The output pulse should be measured on the A/D module pin 34.

    c. If the pulse is correct, proceed to Section 4-12.

    d. If the output pulse is missing, check the input of IC D pin 1 for a LOW going pulse occurring at each program.

    e. If the input pulse is present but the output pulse has improper timing, replace or check R9, C9 or IC D.

    f. If the input pulse is missing, substitute IC M for IC N and look for the proper input pulse at D1.

    g. After performing step (f), a good pulse indicates a bad PIA-N or poor contact in the socket. If this is not the case, refer to Section 4-13, PIA Check.

4-12. INPUT BUFFER CIRCUIT

    a. Connect a stable voltage, preferably a battery, to connector P1 pin 2 (+) and pin 1 (gnd).

    b. The input buffer IC B should track the battery voltage. The output should appear at IC B pin 6.

c. Improper tracking indicates a bad input buffer or shorted/
    broken resistors R3, R4, or R6.

d. Voltage present at this point follows through jumpers J1 and
    J5. Refer to Table 4-A.

e. Insure that the voltage level is within the acceptable range
    for the jumpering scheme being used.

f. If the signal level at the module input pin is correct and the
    problem still persists, proceed to Section 4-13.

4-13. <u>PIA CHECK</u>

The following checkout procedure assumes that the A/D module has
correct voltages present at the power supply pins and tracks the input
voltage correctly at module pins 5 or 6. It also assumes negative
results when IC M is substituted for IC N if there is an improper channel
code or missing A/D strobe.

a. Insure that input and supply voltages are present. Temporarily
    ground pin 1 of IC D and check for a HIGH at pin 2 of IC D and
    run Program 4-I. This should force one conversion pulse to the
    88-ADC.

b. If PIA-M and its associated control circuitry is functioning
    properly, the computer should print the correct voltage for
    one trial each time pin 1 is grounded. If the card now prints
    the correct voltage, IC M is probably working correctly. Since
    IC M and IC N are similar in operation, verify that signals
    appearing at IC M also appear at IC N. Verify the following
    connections from PIA-M to PIA-N, respectively. Read the resis-
    tance with an ohmmeter by placing the probe tips on the <u>IC pin
    itself</u>.

<u>IC M</u>		<u>IC N</u>
pin 21	to	pin 21
pins 24-36, respectively	to	pins 24-36, respectively
pin 23	to	pin 23

Example: There should be continuity between pin 21 on IC M and
          pin 21 on IC N.

c. Check for ground on pin 23 of IC N.

d. Check for +5 volts to pin 20 and a good ground connection at pin 1 on both PIAs.

e. The Reset line pin 34 of both PIAs should be HIGH. If these are incorrect, check IC L pins 8 and 10.

f. If the proper voltage is output in step (b), and steps (c) through (e) show no faults, the associated "CPU Input Cycle" control circuit and PIA-M are probably operating correctly. The problem may be in the data bus output lines (DO0 through DO7) or in the control circuitry associated with PIA-N. Failure to print the correct voltage in step (b) may indicate control circuitry problems or a bad PIA. Substitute IC M and repeat step (b), then proceed to Section 4-14 to check the control circuitry.

4-14. CONTROL CIRCUITRY CHECK

a. Address "Board" Selection Test

1) Program 3-I (page 43) must be run first. Single step through Program 4-II. IC J pin 8 should be seen to "toggle" (alternating LOW and HIGH).

Program 4-II. Output Program To the 88-ADC Board

Location	Data
000	076
001	001
002	323
003	201*
004	303
005	000
006	000

* Channel number for card addressed at 200(octal)

2) If pin 8 does not toggle, check address jumpers and ICs J
   and K.

3) If J8 toggles properly, proceed to the Output Test.

b. Output Test

1) Single step through Program 4-II and observe the following:

Test Point	Toggled Signal ("Actuated" State)
J8	LOW
H8	HIGH (inverted J8)
G8	LOW
R1	LOW
R15	LOW
S15	LOW
M21	LOW
N21	LOW
G6	HIGH (inverted G8)
M24	HIGH (inverted G8)
N24	HIGH (inverted G8)

2) When G8 goes LOW, data on the D∅ through D7 lines of both
   PIAs should correspond to the binary coded data output in
   location 001 of Program 4-II.

3) Change the data in this location and step through Program
   4-II. Verify that the data changes correspond on pins 26
   through 33 of both PIAs.

Example 1: For location 001, Data = 001.
           D∅ line pin 33 of both PIAs should go HIGH when G8
           goes LOW. All other lines (D1 through D7) should
           be LOW at this time.

Example 2: For location 001, Data = 003.
           D∅ and D1 lines pins 32 of both PIAs should go
           HIGH when G8 goes LOW. All other lines (D2 through
           D7) should be LOW at this time.

4) Check Data to make sure each bit can be set HIGH and LOW
   independently on the output cycle of both PIAs.

c. Input Test

1) Program 3-I (page 43) must be run first. Single step through Program 4-III.

2) Observe the following:

Test Point	Toggled Signal ("Actuated" State)
J8	LOW
H8	HIGH (inverted J8)
G11	LOW
S1	LOW
P1	LOW
G6	HIGH (inverted G11)

Program 4-III. Input Program From the 88-ADC Board

Location	Data
000	333
001	204*
002	303
003	000
004	000

* Channel number for card addressed at 200(octal)

3) Carefully remove PIAs M and N and perform the following test:

(a) Temporarily ground one of the DØ through D7 lines on the PIA. socket.

(b) Data on the corresponding data bus <u>input</u> line, DIØ - DI7, should go LOW when G11 goes LOW.

(c) Sequentially ground each of the eight data lines and verify the proper response on the bus lines.

Example: Ground DØ pin 33 of PIA-M. When G11 goes LOW, P9 should also go LOW. All other lines should be HIGH (P3, P5, P7, S3, S5 and S9).

d. <u>E Pulse and WAIT State Tests</u>

    1) While running (not single stepping) Program 4-III, check for a 500ns. HIGH pulse at G3 and pin 25 of both PIAs. If the pulse is not present, replace IC G and/or IC H.

    2) Repeat step (1), utilizing Program 4-II. Check for the same pulse.

    3) While running Program 4-II, check for a 500ns. LOW pulse at E13, P13, H4, F8 (inverted) and F6.

This completes the A/D troubleshooting section.

4-15. <u>8-CHANNEL MULTIPLEXER SYSTEMS</u>

a. First check the allowable input voltage ranges shown in Table 2-A, page 13. Input voltages will be "clamped" to these limits. Note that large out-of-spec voltages may damage the circuitry.

b. Check the cable inputs and note that the ground pin 25 on the DB-25 connector (P2-6 on the 88-ADC) should be used as the signal reference point rather than some other system ground terminal.

c. If the voltage at any input pin of IC U is larger than either supply voltage at pin 16 or 7, the input clamping diodes and/or associated components are not functioning properly.

d. Make sure connector P1 pins 1 and 2 are not shorted together. No external terminations should be required at P1 when using the 8-channel system.

4-16. A/D CHANNEL CODE (88-ADC)

a. Enter Program 4-I to loop on one channel and check for the correct binary code at IC U pins 9, 10 and 11. Refer to Table 4-B.

Example 1: Program selection of channel 0 forces pins 9, 10 and 11 HIGH.

Example 2: Channel 3 forces pins 10 and 11 LOW while pin 9 goes HIGH.

Table 4-B. A/D Channel Code

CHANNEL NUMBER	IC-U pin-9	IC-U pin-10	IC-U pin-11	SIGNAL LINE ENABLED
0	H	H	H	AX0
1	H	H	L	AX1
2	H	L	H	AX2
3	H	L	L	AX3
4	L	H	H	AX4
5	L	H	L	AX5
6	L	L	H	AX6
7	L	L	L	AX7

b. The output of IC U pin 3 should track the "enabled" signal line (AX0-AX7). Connect a stable supply (such as a 1.5 volt battery) to P2 pin 10 (+) and pin 6 (-). IC U pin 3 should output a voltage corresponding to the battery voltage when channel 0 is enabled.

c. If the correct address code is seen at pins 9, 10 and 11 and the input voltage is within limits (but pin 3 does not track the input signal), replace IC U. Refer to the CMOS Special Handling Precautions on page 32.

This completes the 8-Channel Multiplexer troubleshooting.

altair 8800
CONVERSION SYSTEM
SECTION V
APPLICATIONS

5-1. GENERAL

This section contains four possible systems that can be implemented using the 88-ADC and 88-MUX boards.

5-2. System 1

The first system is a true "system monitor," incorporating the 88-ADC and 88-MUX boards. The input signals are derived from temperature sensors, strain gauges, light detectors or virtually any type of analog voltage transducers. Since the amplifier gain and scaling is independent for each channel sampled (24-channel multiplexer system only), a combination of sensors can be utilized. Refer to Figure 5-1.
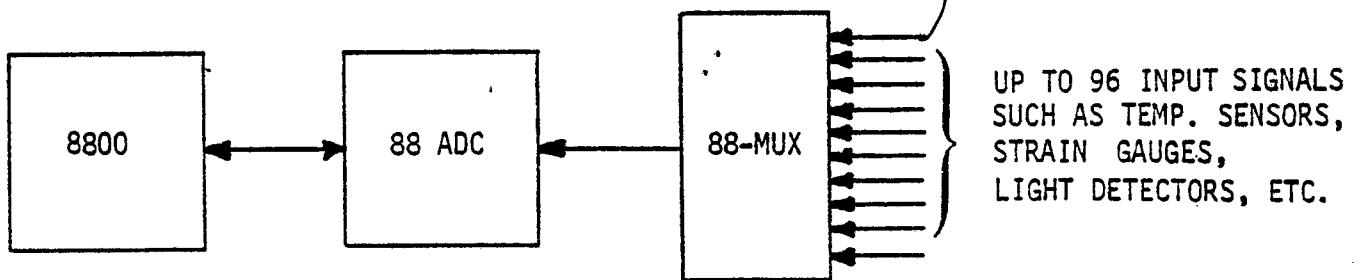
```
+--------+        +--------+        +--------+      }  UP TO 96 INPUT SIGNALS
|        |        |        |        |        |      }  SUCH AS TEMP. SENSORS,
|  8800  | <----> | 88 ADC | <----- | 88-MUX |      }  STRAIN  GAUGES,
|        |        |        |        |        |      }  LIGHT DETECTORS, ETC.
+--------+        +--------+        +--------+
```

Figure 5-1. System Monitor

5-3. System 2

    System 2 is similar to System 1, but requires only an 88-ADC board. It computes the "X" and "Y" coordinates simulated by a pair of potentiometers. This system may be useful for many computer games which utilize joystick type controls. Since the 88-ADC can resolve 1 part in 4096 coordinate "increments," extremely good accuracy can be obtained for sophisticated systems using only one 88-ADC board. Refer to Figure 5-2.
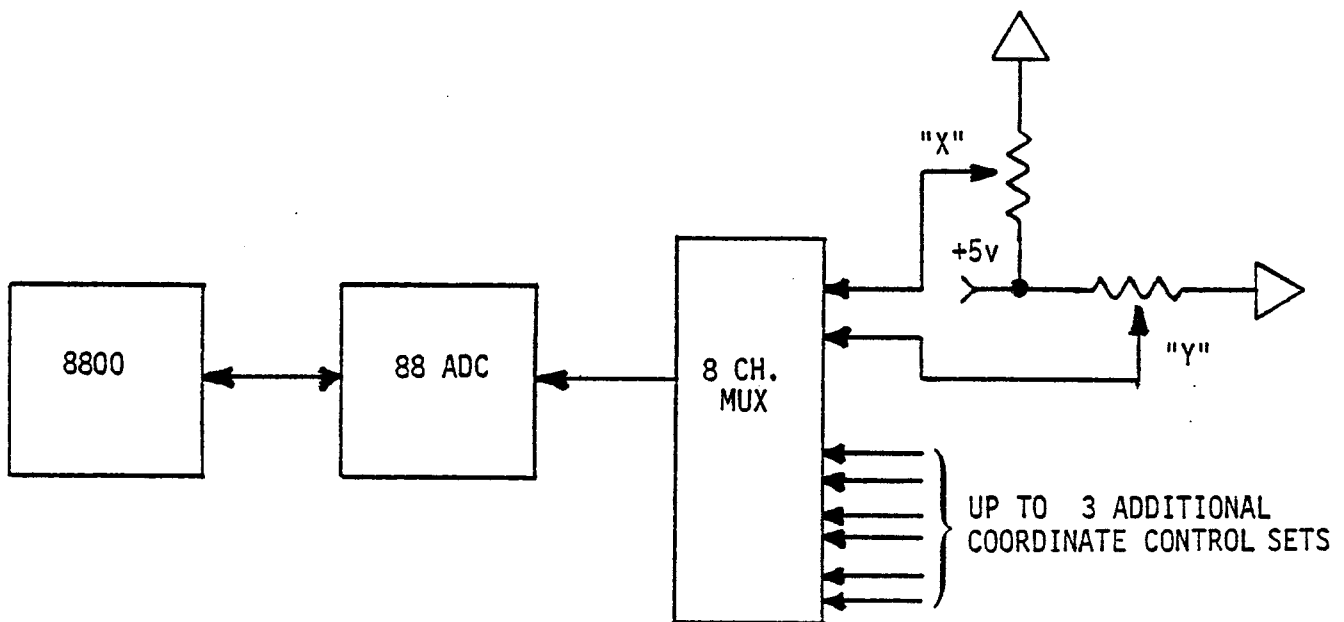
Figure 5-2. Digital Coordinate System

5-4. System 3

It is possible to use the 88-ADC and 88-MUX system as an automatic circuit tester. The 4PIO board is utilized as an output signal generator to key control voltages (standard logic level) on or off through the various subassemblies of some type of electronic device. Optionally, an 88-PCI (Process Control board) can be used in place of the 4PIO, allowing high voltage control signals and complete isolation. The 88-ADC and 88-MUX monitor key test points to determine proper circuit operation and can actually do quite a thorough troubleshooting checkout of the device in a completely automated mode. Refer to Figure 5-3.
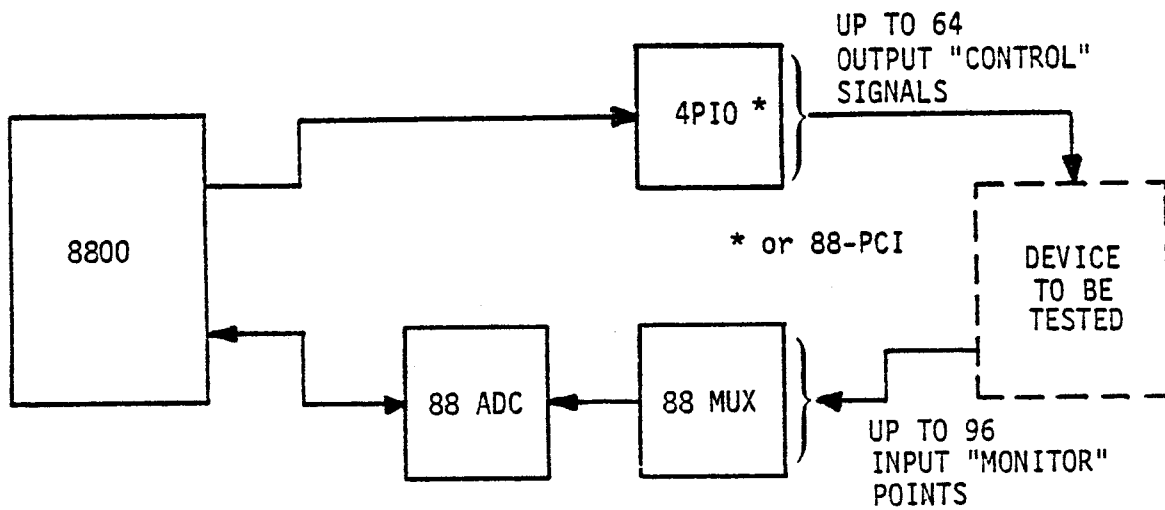

Figure 5-3. Testing System

5-5. System 4

Only the 88-ADC board is required for System 4. Figure 5-4 shows how a relatively slow varying voltage can be broken down and "digitized." Prime considerations for this system are:

1) how fast the input signal varies
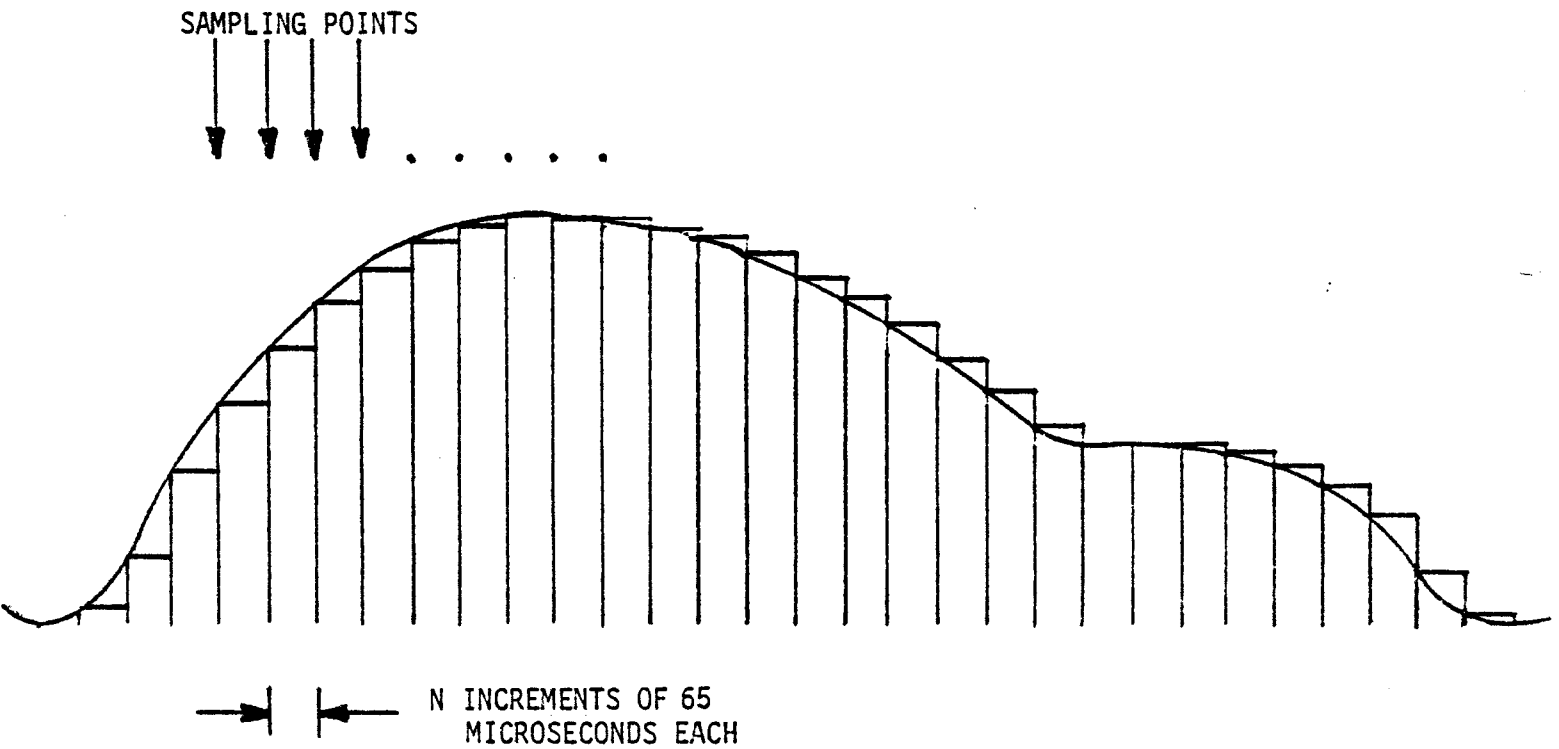2) how fast the processing software can be made

SAMPLING POINTS

N INCREMENTS OF 65
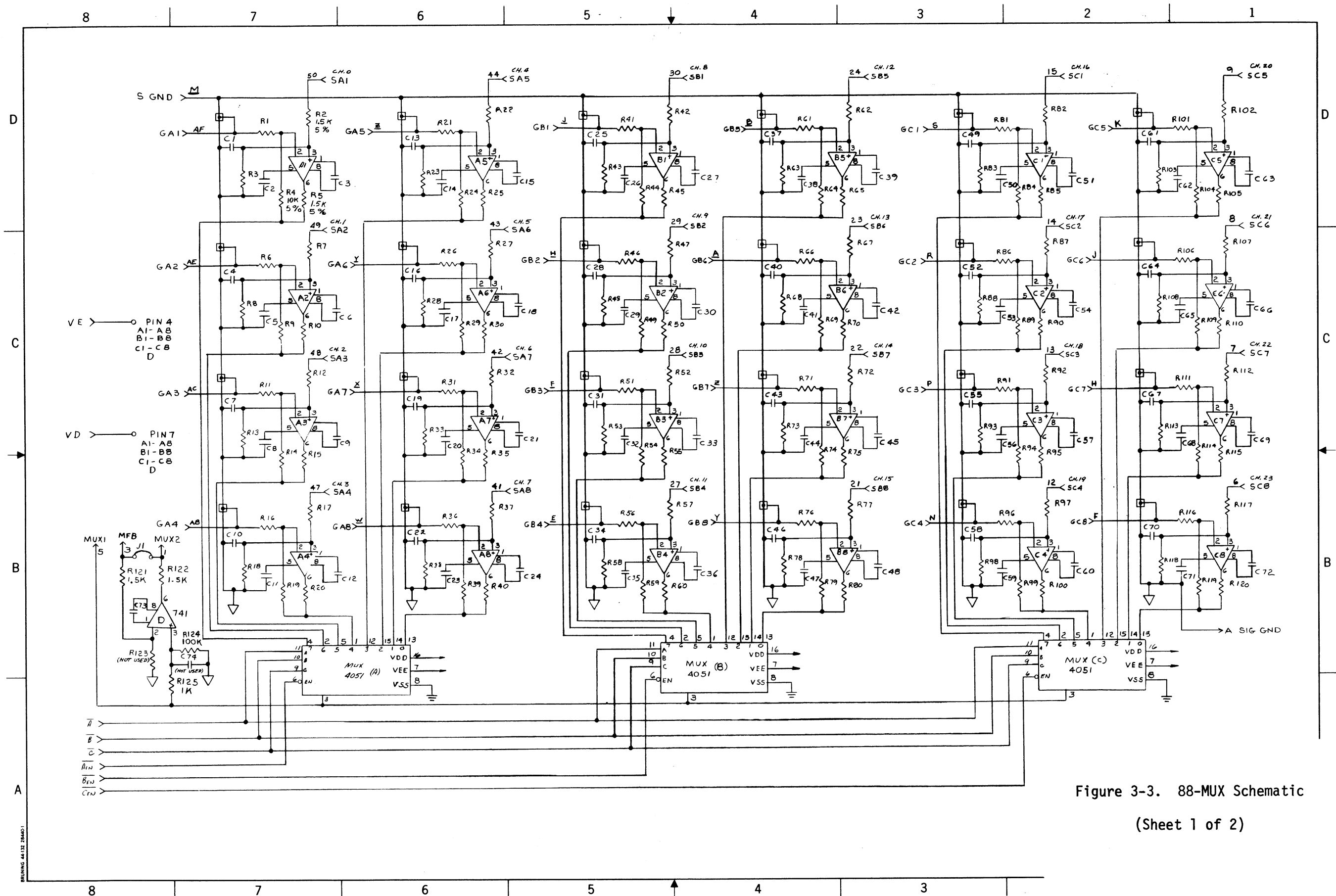MICROSECONDS EACH

Figure 5-4. "Digitized" Voltage

Figure 3-3. 88-MUX Schematic

(Sheet 1 of 2)