88-2

serial INPUT/OUTPUT board

theory of operation

88-2 SERIAL INPUT/OUTPUT BOARD OPERATION

The 88-2SIO board is designed around an ACIA (an asynchronous communications interface adaptor). The ACIA (6850 ICs D and E) contains both the control register and the status register, so that most options are software selectable. The only two options under hardware control are the address select and the baud-rate select. Baud-rate select can also be altered under software control. Each board contains up to two ACIAs or "ports".

BACKGROUND THEORY

NOTE: See block diagram on page 3.

The ALTAIR 8800 allows for up to 256 addresses reserved for Input/Output devices. The "IN" and "OUT" instructions to the central processing unit (CPU) distinguish I/O addresses from memory addresses, thus enabling the CPU to maintain full memory capability during I/O operations.

"IN" and "OUT" instructions work as follows: Each instruction contains two bytes and requires three machine cycles to execute. During machine cycles 1 and 2 (M1, M2) bytes 1 and 2 of the instruction are fetched from memory by the CPU. Byte 1 is the instruction code ("IN" = 333, "OUT" = 323), and byte 2 is the device address (0-377).

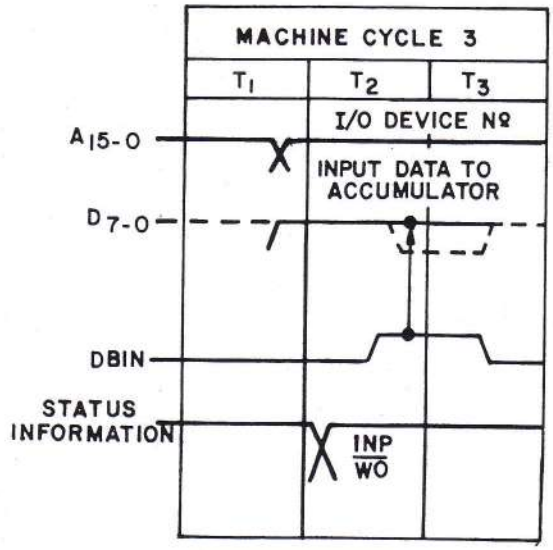
During machine cycle 3 (M3), data is transferred as follows: During the first clock period (T1) of M3, the I/O device address (byte 2 of the instruction) is placed on the "address" buss. Only 8 bits are used for I/O device addresses so that the address appears on both the lower lines (A0-A7) and the upper lines (A8-A15). The status signals of T2 distinguish device address operations from memory operations. During T2, the status information is latched and sent to the system buss. The status signal for the "IN" instruction is "SINP" and the status signal for the "OUT" instruction is "SOUT". Except for the I/O status signal, T3 of M3 appears identical to a memory operation.

Data is strobed into the accumulator with PDBIN for "IN" operations. The accumulator is placed on the data buss and strobed out with $\overline{\text{PWR}}$ for "OUT" operations. The device and interface are responsible for assuring that data is on the buss when the CPU requires it and that the device receives data during $\overline{\text{PWR}}$ in an "OUT" operation.

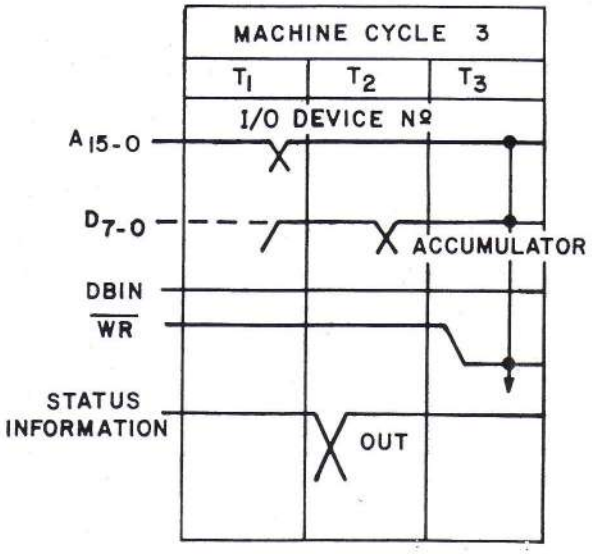
TIMING DIAGRAMS

88-2SIO Board

INPUT INSTRUCTION



OUTPUT INSTRUCTION



ADDRESS SELECTION

The 88-2SIO board provides six address lines that enable address selection. These six lines provide 64 possible addresses which are selected in increments of four. The four addresses are the data transfer and control/status channels of Port 0 and Port 1. To illustrate, the first board includes addresses 0-3, the second 4-7, etc. up to addresses 252-255. Note that address 255 is the front panel sense switch and should not be used.

The address selection chart on pages 21 and 22 of the Assembly Manual shows the correct strapping for any desired address. The jumpers represent address lines A2-A7. Address lines A0 and A1 cause register selection and port selection respectively. These two address lines are software controlled and select registers and ports according to the following chart. This example shows selection for address 0.

ADDRESS		PORT #	OUTPUT FUNCTION	INPUT FUNCTION
A0	A1			
0	0	1	Control Register	Status Register
1	0	1	Output Data	Input Data
0	1	2	Control Register	Status Register
1	1	2	Output Data	Input Data

If, for example, address 68 is selected via the jumpers, the four addresses for the board are as follows:

Address	Function
68	1st Port, Control/Status
69	1st Port, Data In/Out
70	2nd Port, Control/Status
71	2nd Port, Data In/Out

If "OUT, 70" or 323 Byte 1
106 Byte 2 (octal 106 = 70 decimal)

were executed, the accumulator would be written into the control register of the second port on the 2SIO board, which is strapped at location 68.

SOFTWARE OPTIONS

Each port has an 8-bit control register that allows port configuration under software control. Each bit is defined below.

7	6	5	4	3	2	1	0
In Interrupt	Out Interrupt		Transmission Bits			Clock Divide And Reset	

NOTE: Data bit low = 0
Data bit high = 1

The first two data bits, 0 and 1, control the internal clock divide circuit and the master reset according to the following chart:

BIT 1	BIT 0	FUNCTION
0	0	÷ Clock by 1
0	1	÷ Clock by 16
1	0	÷ Clock by 64
1	1	Master Reset

Normal operations output bits 0 and 1 as equal to "1", and reset the ACIA. Next, bits 0 and 1 are output as equal to 1 and 0 respectively, since the normal incoming clock frequency is 16 times the baud rate. (i. e. When any one of the eight baud rates that appear on the silk-screened board is desired, the ÷ 16 mode should be used.)

In order to select any one of the five additional baud rates, use the ÷ 64 mode (data bits 0 and 1 are equal to 0 and 1 respectively). Next, select the associated baud rate from the following chart:

÷ 16 ÷ 64

DESIRED BAUD RATE	SELECTED BAUD RATE
27.5	110
37.5	150
75.0	300
450	1800
600	2400

Note that the selected baud rate is four times greater than the desired baud rate, since the incoming frequency is 16 times the baud rate and is divided by 64 in the ACIA (64 ÷ 16 or 4).

The next three bits of the control register determine word length, parity, and number of stop bits. Consult your I/O device manual for the configuration required. Then, set the bits according to the following table.

DATA BIT			FUNCTION		
4	3	2	# of Data Bits	# of Stop Bits	Parity
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	2	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

The last three bits of the register control interrupts and I/O device handshake, as shown below:

DATA BIT			FUNCTION
7	6	5	
X	0	0	$\overline{RTS}$ = low, transmitting interrupt disabled.
X	0	1	$\overline{RTS}$ = low, transmitting interrrupt enabled.
X	1	0	$\overline{RTS}$ = high, transmitting interrupt disabled.
X	1	1	$\overline{RTS}$ = high, transmits a break level on the transmit data output, Transmit interrupt disabled.
0	X	X	Receive interrupt disabled.
1	X	X	Receive interrupt enabled.

X = does not matter.

The following table shows the initialization for a Teletype with 8 data bits, 2 stop bits and no parity. Both receive and transmit interrupts are enabled. This example illustrates the initialization when I/O address = 0.

OCTAL CODE	FUNCTION
076	Reset port
003	
323	
000	
076	Set up for 8 data bits, ÷ 16 mode, $\overline{RTS}$ = low, transmit and receive interrupts enabled.
261	
323	
000	

STATUS REGISTER

Information on the status of the port is available by reading the ACIA Status Register. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the port.

Receive Data Register Full (RDRF), Bit 0 - Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after a read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 - The Data Carrier Detect bit will be high when the $\overline{DCD}$/input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read status and read data or master reset have occurred, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 - The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send Status bit.

Framing Error (FE), Bit 4 - Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 - Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE), Bit 6 - The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request (IRQ), Bit 7 - The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low, the IRQ bit will be high to indicate the interrupt or service request status.

SPECIAL NOTE: MITS software assumes that the 2-SIO board is addressed at location 20 when used to interface the loading device (tape reader, etc.) A new bootstrap loader labeled "2SIO (for versions 3.2 and later only)" is located in the back of the software manuals. Octal address 005 of the 2SIO boot will initialize the 2SIO port for your particular device. The octal codes 021 or 025 correspond to the address 005. Both of these codes set the clock divide to ÷ 16. Interrupts should not be enabled.

Note that if the 2-SIO boot loader is used, first start the program (push STOP/RUN switch to RUN), then start the reader.

ELECTRONIC THEORY

Selection

Address lines A7-A2 are inverted/buffered through ICs Q and S, then fed to pads A7-A2, IC R and Pin 5 of IC S. The outputs of R and S6 are fed to pads A7-A2. If the incoming address matches the selected address (pads F7-F2), 08 goes low and S8 goes high, thus enabling P1, P9, and P4. If an "IN" or "OUT" instruction is executed, either SINP or SOUT forces P2 high and P3 and $\overline{CS2}$ of D and E go low, partially enabling the ports. Port and register selection are completed by Address lines A1 and A0, according to the following chart:

A0	A1	PORT NUMBER	REGISTER
0	0	0	Control/Status
1	0	0	Data
0	1	1	Control/Status
1	1	1	Data

Port inputs Rs and CS1 are register select and chip select, respectively.

To read or write a register, the E pulse (ENABLE) must be present. The E pulse is generated each machine cycle by either $\overline{PWR}$ or PDBIN to insure proper timing.

Write ("OUT" Instruction)

A CPU write to a port forces SOUT high and $\overline{PWR}$ low. SOUT forces $\overline{CS2}$ low (see "Selection", above). P6 is also forced low, thus enabling the tristate data output drivers via A1 and B1 (see CPU schematic for logic diagram of the 8T97). R/W is pulled low for a write operation (R/W is Read/Write). $\overline{PWR}$ completes the write by generating an E pulse.

Read ("IN" Instruction)

A CPU read from a port forces SINP and PDBIN high. SINP pulls $\overline{CS2}$, A15, B15, and C1 low to enable the port and the data input drivers. SINP also clocks flip-flop V to force PRDY low, thereby forcing the CPU into a wait state for 500 nanoseconds.

During this time, the CPU forces PWAIT high, clearing V and pulling PRDY high again. The wait state is generated to allow address setup time for the port and occurs only during an input.

$\overline{POC}$, power-on-clear, insures that V will be cleared when power is first applied.

SERIAL I/O INTERFACE OPERATION

1. RS-232

Inputs: The 1489's (ICs I and J) convert the incoming signal to standard TTL levels.

Input voltage, minimum swing = ± 3 Volts
Maximum swing = ± 30 Volts

Outputs: The 1488 (IC N) converts the TTL levels to a ±9 Volt minimum swing at a current limited output of approximately 10 milliamps.

2. TTL

Inputs: *1 unit load, logic low = -.5 Volts to .8 Volts
logic high = 2 Volts to 5.5 Volts

Outputs: *10 unit loads, logic low = .4 Volts maximum
logic high = 2.4 Volts minimum

* 1 unit load = 40 microamps high/1.6 milliamps low

3. TTY

(Refer to page 2 of the Schematic).

Input: (Refer to top circuit)

The transmit distributor contacts are fed to Y2 and Y3. These contacts, which are normally closed, allow current flow through R4 and R5, causing a negative voltage at the anode of diode D3. Thus, D3 will not conduct, and the input of gate K is pulled low by resistor R3 (jumper Y1 to K7 is assumed to be present). The output of gate K, therefore, goes high to provide an off condition or "marking" state to the port. When the contacts open due to data transmission, the anode of diode D3 is pulled to +15 Volts. D3 conducts, and the input to gate K is pulled to approximately 4 Volts via the divider resistors R3 and R4. Capacitor C3 is used for contact debounce. Thus, the output of gate K goes low and represents a transmitted data bit.

Output: (Refer to Transistor Q1 circuit)

The port output line (D5) is normally high, causing a low at the base of Q1. The emitter of Q1 is pulled to approximately 1.2 Volts, through diodes D1 and D5, and thereby forward biases Q1 to cause a current flow through resistor R7, Q1, and the device. This is called the marking state. When a data bit is transmitted, the base of Q1 is pulled high by resistor R6. Q1 then turns off, providing a very high impeadance at the device. This represents a valid data bit.

88-2SIO

PARTS LIST

JANUARY, 1976

Bag 1

1	6850	101098
1	74L00	101080
1	74L02	101072
3	7404	101022
4	74L04	101073
1	74L30	101082
1	7473	101027
1	7805	101074
1	93L34	101077
3	8T97	101040
1	1488	101112
1	1489	101113
1	34702	101099

Bag 2

2	100 ohm ½w	101924
10	220 ohm ½w	101925
6	470 ohm ½w	101927
6	1.5kohm ½w	101946
4	2.7kohm ½w	101929
1	10M ohm ½w	102079

Bag 3

2	56pf 20v	100317
6	1mf 10v	100306
3	33mf 16v	100326
15	.1mf 10v	100348

Bag 4

2	IN4742 Z	100722
4	EN2907	102804
14	IN914	100705

Bag 5

1	16 Pin Socket	102103
1	24 Pin Socket	102105
1	Female Connector 09-50-7101	101768
10	Terminal 08-50-106	101769
1	Right Angle Male Connector 09-66-1101	101812
1	25 DBP (male)	102111
1	25 DBS (female)	102112
1	cover (plastic)	101739
1	Crystal 2.4576 MHZ	101741
1	Connector -100 pin	101864
2	Card Guides	101714

Bag 6

3	#6-32 x ½" Screw	100918
1	#6-32 Hex Nut	100933
1	#6 Lock Washer	100942
1	Heat Sink (large)	101870
1	20" 12 Conductor Cable	103058
4	36" 26 ga. white	103060

MISC:

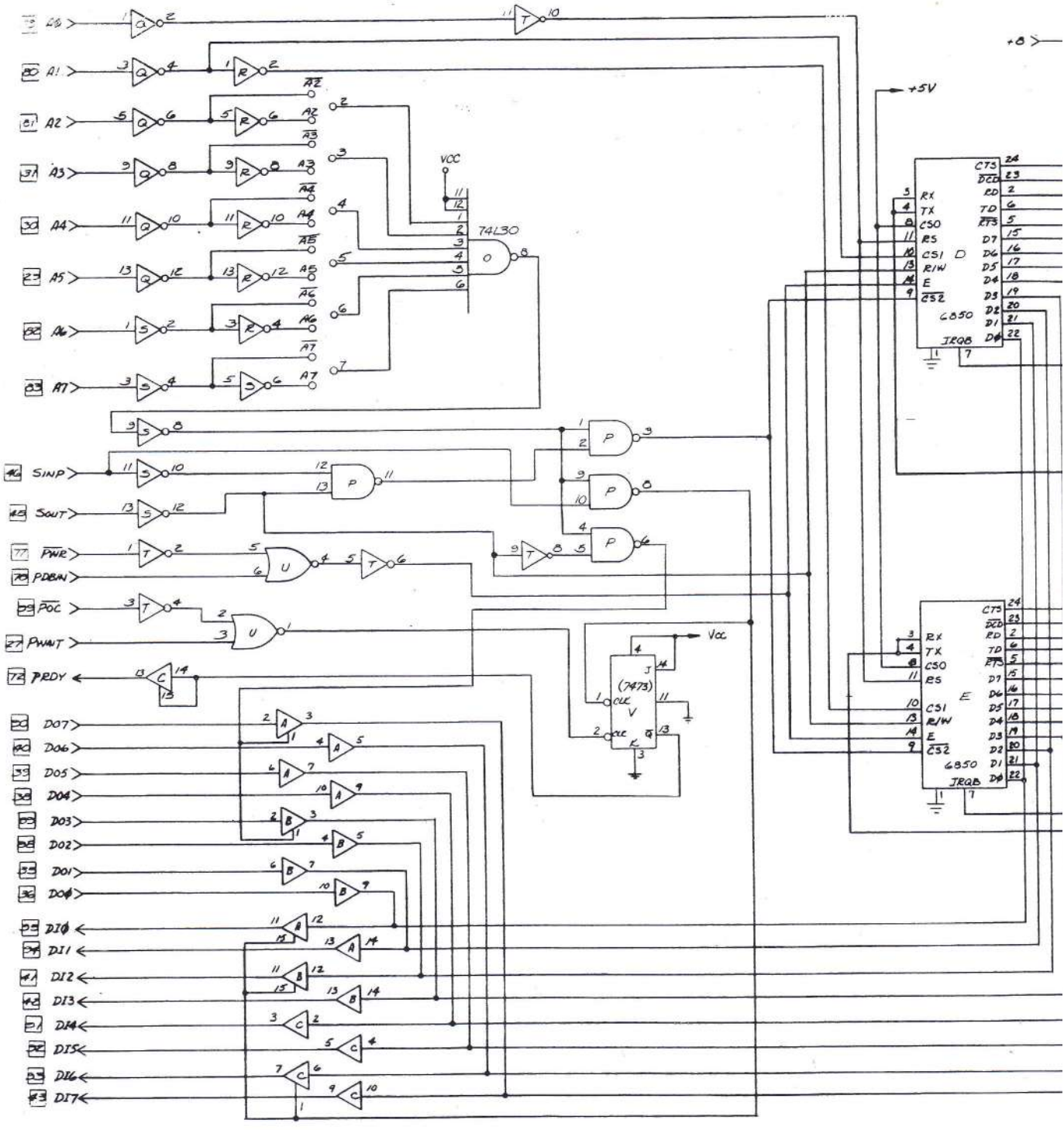
1	Manual	101524
1	2SIO PC BD	100180

NOTICE!!

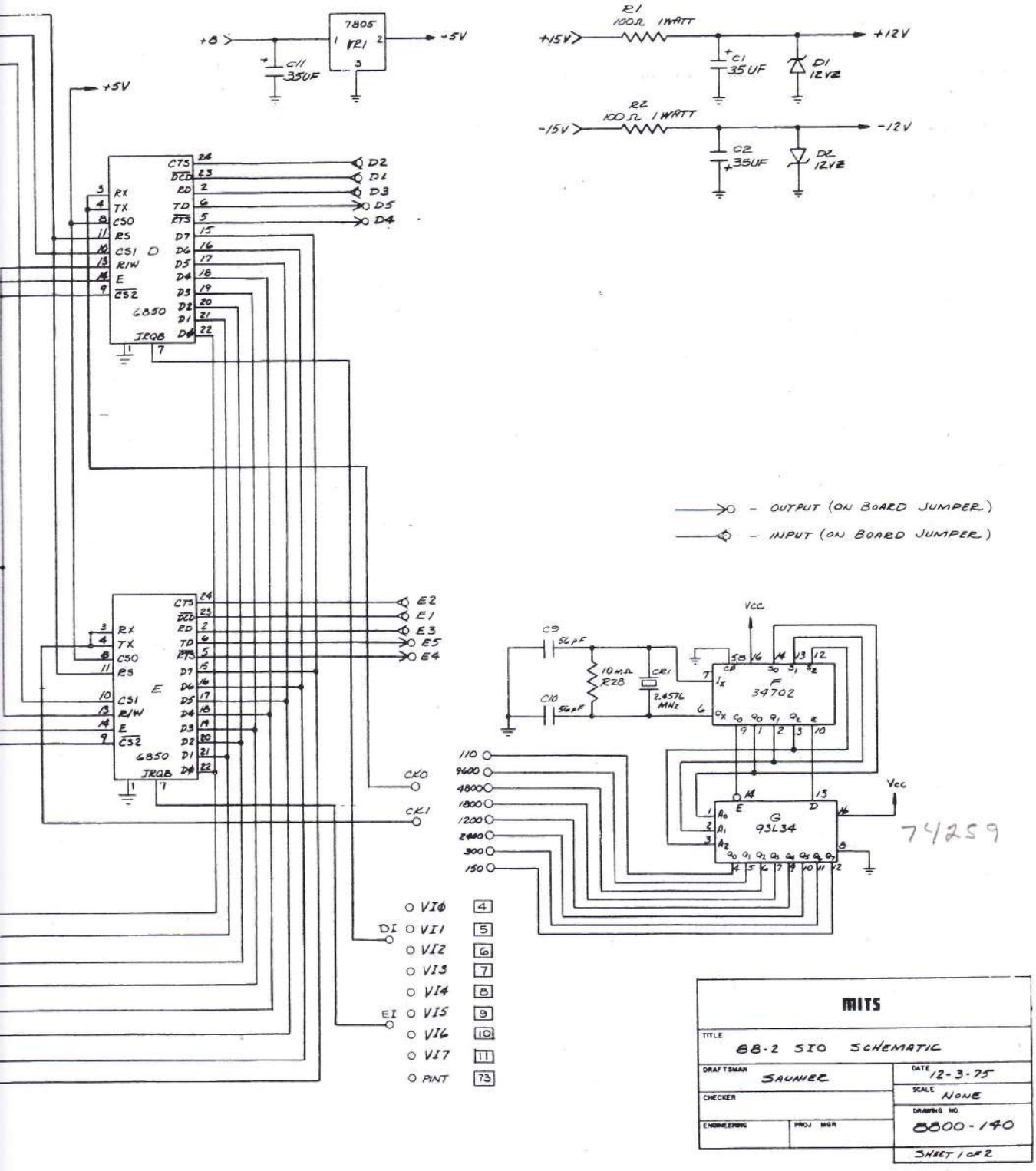
The following refers to the operation of the 88-2SIO Board:

1. If the $\overline{\text{Data}}$ $\overline{\text{Carrier}}$ $\overline{\text{Detect}}$ and $\overline{\text{Clear}}$ $\overline{\text{to}}$ $\overline{\text{Send}}$ inputs are not connected, they must be jumpered to Ground.

2. When using the 2-SIO Board to connect a device that is to be used for loading MITS software, start the bootstrap loader before starting the loading device (paper tape reader, etc.).


+5V
VCC
74L30
SINP
SOUT
PWR
PDBN
POC
PWINT
PRDY
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
6850
IRQB
(7473)

2510

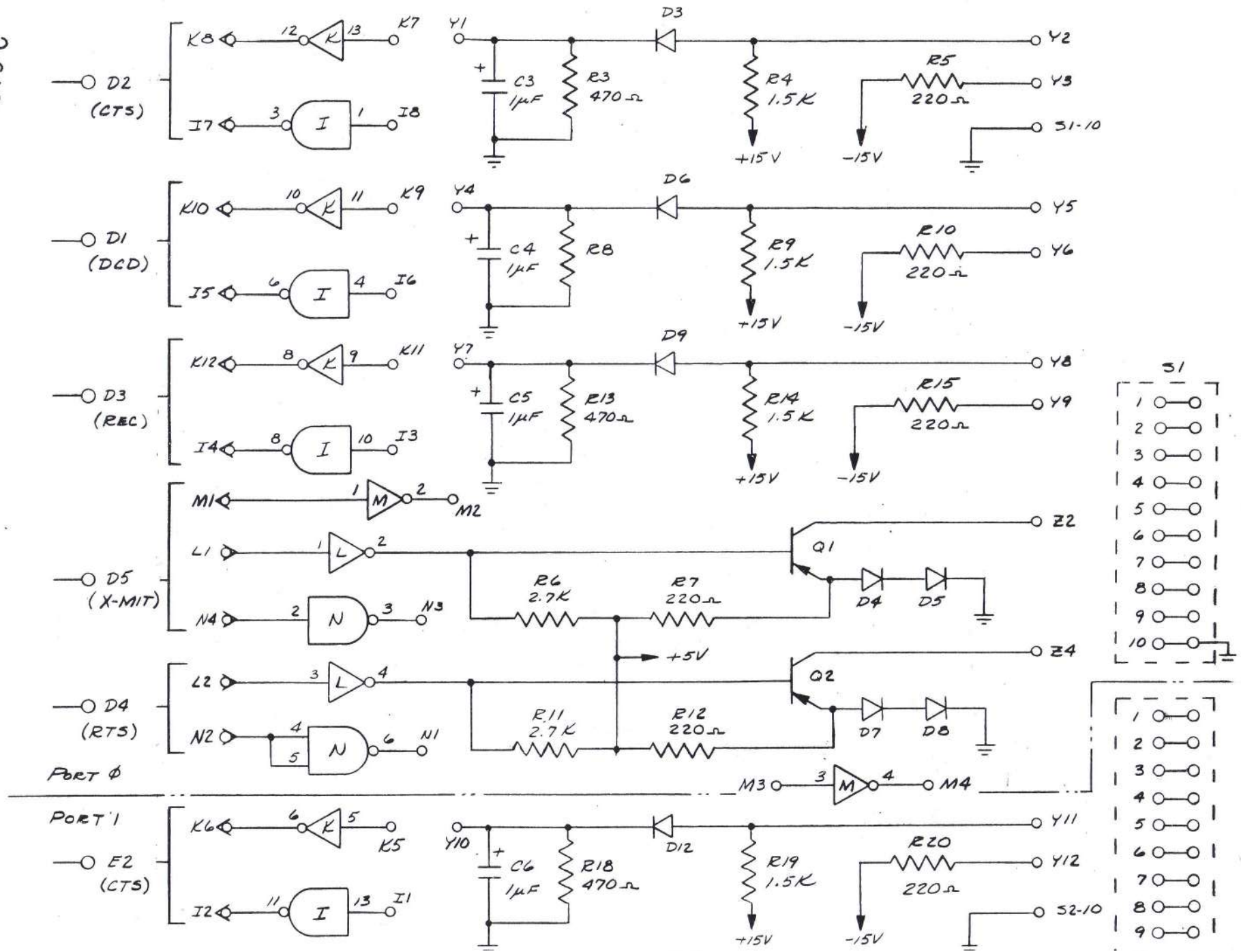


→○ - OUTPUT (ON BOARD JUMPER)

○→ - INPUT (ON BOARD JUMPER)

11

MITS	
TITLE: 88-2 SIO SCHEMATIC	
DRAFTSMAN: SAUNIER	DATE: 12-3-75
CHECKER	SCALE: NONE
ENGINEERING / PROJ MGR	DRAWING NO: 8800-140
	SHEET 1 OF 2


D2 (CTS)
D1 (DCD)
D3 (REC)
D5 (X-MIT)
D4 (RTS)
PORT 0
PORT 1
E2 (CTS)
K8
K7
I7
I8
K10
K9
I5
I6
K12
K11
I4
I3
M1
M2
L1
N4
N3
L2
N2
N1
K6
K5
I2
I1
C3 1μF
R3 470Ω
R4 1.5K
R5 220Ω
C4 1μF
R8
R9 1.5K
R10 220Ω
C5 1μF
R13 470Ω
R14 1.5K
R15 220Ω
R6 2.7K
R7 220Ω
R11 2.7K
R12 220Ω
C6 1μF
R18 470Ω
R19 1.5K
R20 220Ω
D3
D6
D9
D12
D4
D5
D7
D8
Q1
Q2
+15V
-15V
+5V
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
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Y10
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Y12
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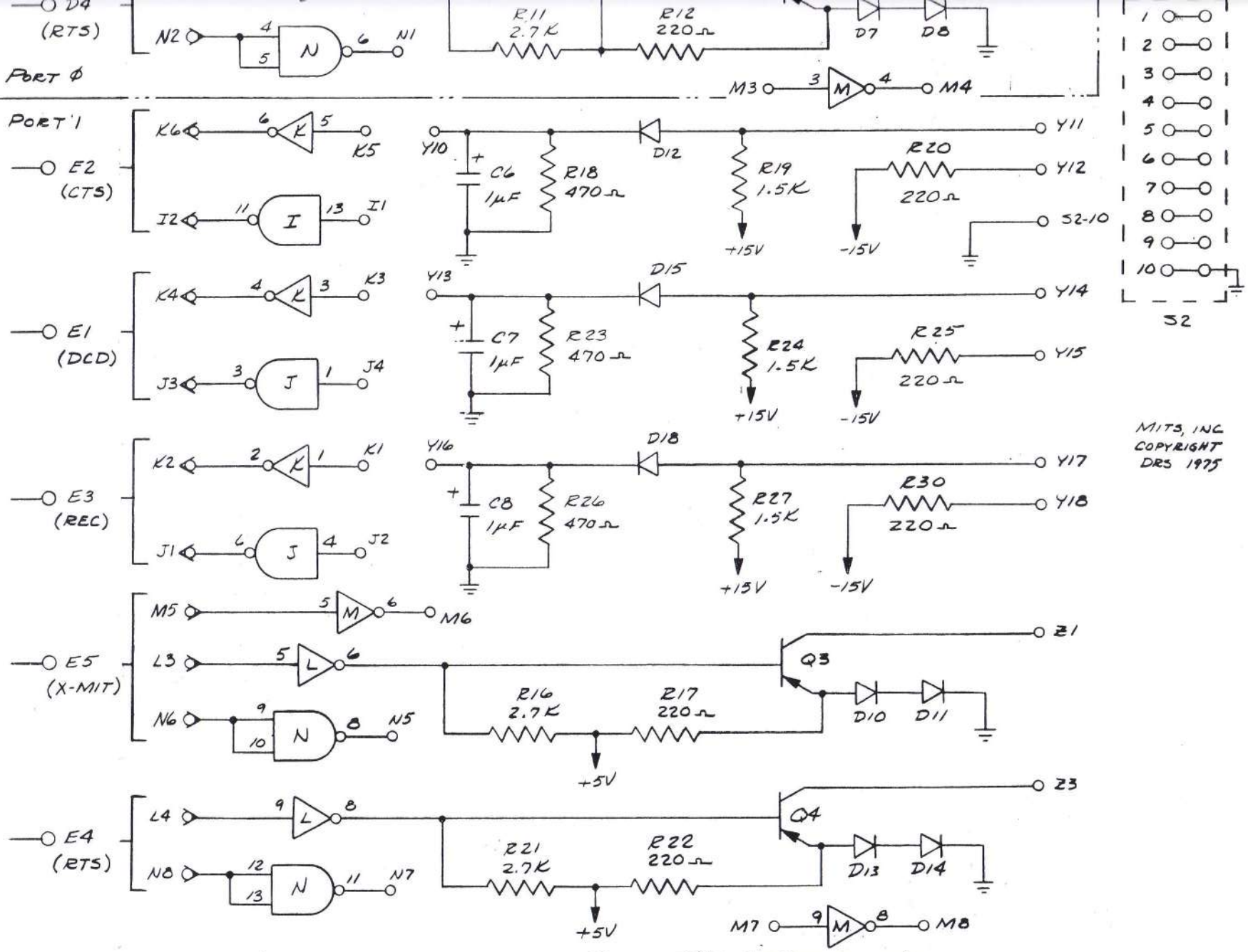
Z4
M3
M4
J1
J2
J1-10
J2-10



88·2

serial INPUT/OUTPUT board

assembly procedure

SOCKET INSTALLATION

The 88-2 Serial Input-Output board (88-2SIO) may be configured for one or two I/O ports. Each port requires one 24-pin socket. One 16-pin socket for the 4702 IC must also be installed.

The 24-pin socket(s) will be placed in positions D and E, and the 16-pin socket will be placed in position F, as indicated by the component layout on page 4. If your board is to be configured for only one port, install D.

Referring to the parts chart on page 3 and the component layout on page 4, use the following procedure to install each socket.

1. Be certain that the socket pins are straight. If any of the pins are bent, CAREFULLY straighten them with the tip of a small screwdriver.

2. Set the socket into place, and secure it with a piece of masking tape.

3. Turn the board over and solder each pin to the foil pattern of the back of the board. Be sure that EACH pin is soldered, and be careful not to leave any solder bridges.

4. Turn the board over again, and remove the masking tape.

5. After each socket is installed, check the corresponding socket off of the parts list on page 4.

IC INSTALLATION

There are from 19-21 integrated circuits to be installed on the 88-2SIO board. From two to three of the ICs have been provided with sockets (D, E, F) and must not be installed at this time.

NOTE: The three ICs provided with sockets are extremely static-sensitive. Do not install these ICs (D, E, F) until after the entire board is assembled.

The following ICs should be installed now: A, B, C, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, and V. Note, one 1489 IC, "I", will be installed only if the 88-2SIO board is configured for two I/O ports.

To prepare ICs for installation:

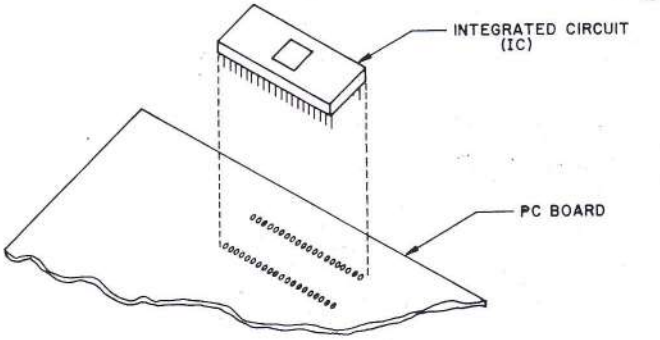
Referring to the component layout on page 4, remove the IC with the correct part number from its holder. If there are any bent pins, straighten them with a needle-nose pliers. Ensure that you choose the IC with the correct part number as you install each one.

All ICs are damaged easily and should be handled carefully. Always try to hold the IC by the ends, touching the pins as little as possible.

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the 88-2SIO board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Orientation Chart included with your manual for the identification of Pin 1.

Install the ICs according to the following procedure:

1. After the IC is correctly oriented, start the pins on one side of the IC into their respective holes on the silk-screened side of the PC board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.



2. Start the pins on the other side of the IC into their holes in the same manner. When all of the pins have been started, set the IC into place by gently rocking it back and forth until it rests as closely as possible to the board. After you are certain that the IC is perfectly straight and as close to the board as possible, tape it in place with a piece of masking tape.

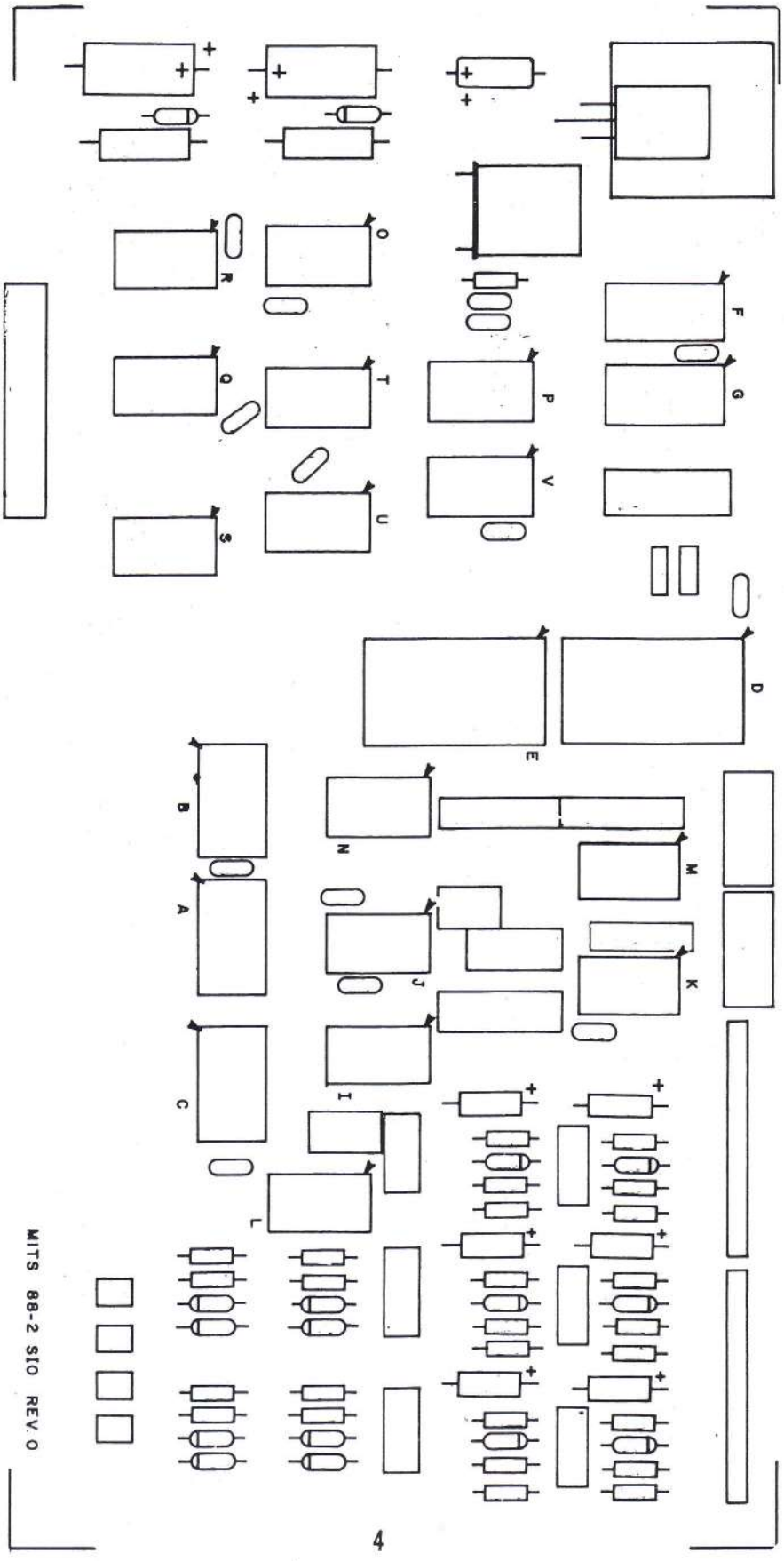
3. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder EACH pin, and be careful not to leave any solder bridges.

4. Turn the board over again, and remove the piece of masking tape.

5. After each IC is installed, check the corresponding IC off of the parts list provided on this page.

SOCKETS AND ICS		
Silk Screen Designation	Part	Number
( ) A	IC	8T97
( ) B	IC	8T97
( ) C	IC	8T97
( ) D	24-pin Socket	
( ) E*	24-pin Socket	
( ) F	16-pin Socket	
( ) G	IC	93L34
( ) I	IC	1489
( ) J*	IC	1489
( ) K	IC	7404
( ) L	IC	7404
( ) M	IC	7404
( ) N	IC	1488
( ) O	IC	74L30
( ) P	IC	74L00
( ) Q	IC	74L04
( ) R	IC	74L04
( ) S	IC	74L04
( ) T	IC	74L04
( ) U	IC	74L02
( ) V	IC	7473

* Designates parts to be installed only if 88-2SIO is configured for two I/O ports.


MITS 88-2 SIO REV.0

RESISTOR INSTALLATION

There are 29 resistors to be installed on the 88-2SIO board.

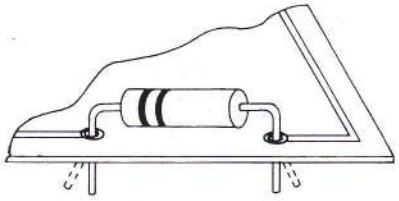
NOTE: Resistors are color-coded according to their value. The resistors in your kit will have four bands of color. The fourth band in both cases will be gold or silver, indicating the tolerance. In the following instructions, only the three bands of color to one side of the gold or silver band are significant. Be sure to match these three bands of color with those called for in the instructions as you install each resistor.

Referring to the parts chart on page 6 and the component layout on page 7, install each resistor according to the following procedure.

1. Match the color bands designated on the parts chart with the resistor position indicated by the component layout.

2. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the 88-2SIO board.

3. Insert the resistor into the correct holes from the silk-screened side of the board. Push the resistor down until it almost touches the foil pattern.



RESISTOR

4. Holding the resistor in place, turn the board over and bend the leads slightly outward.

5. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

6. After making sure that there are no solder bridges, check the resistor off of the parts list.

RESISTORS

( ) R1, Brown-Black-Brown, 1/2 W

( ) R2, Brown-Black-Brown, 1/2 W

( ) R3, Yellow-Purple-Brown, 1/4 or 1/2 W

( ) R4, Brown-Green-Red, 1/4 or 1/2 W

( ) R5, Red-Red-Brown, 1/4 or 1/2 W

( ) R6, Red-Purple-Red, 1/4 or 1/2 W

( ) R7, Red-Red-Brown, 1/4 or 1/2 W

( ) R8, Yellow-Purple-Brown, 1/4 or 1/2 W

( ) R9, Brown-Green-Red, 1/4 or or 1/2 W

( ) R10, Red-Red-Brown, 1/4 or 1/2 W

( ) R11, Red-Purple-Red, 1/4 or 1/2 W

( ) R12, Red-Red-Brown, 1/4 or 1/2 W

( ) R13, Yellow-Purple-Brown, 1/4 or 1/2 W

( ) R14, Brown-Green-Red, 1/4 or 1/2 W

( ) R15, Red-Red-Brown, 1/4 or 1/2 W

( ) R16, Red-Purple-Red, 1/4 or 1/2 W

( ) R17, Red-Red-Brown, 1/4 or 1/2 W

( ) R18, Yellow-Purple-Brown, 1/4 or 1/2 W

( ) R19, Brown-Green-Red, 1/4 or 1/2 W

( ) R20, Red-Red-Brown, 1/4 or 1/2 W

( ) R22, Red-Red-Brown, 1/4 or 1/2 W

( ) R23, Yellow-Purple-Brown, 1/4 or 1/2 W

( ) R24, Brown-Green-Red, 1/4 or 1/2 W

( ) R25, Red-Red-Brown, 1/4 or 1/2 W

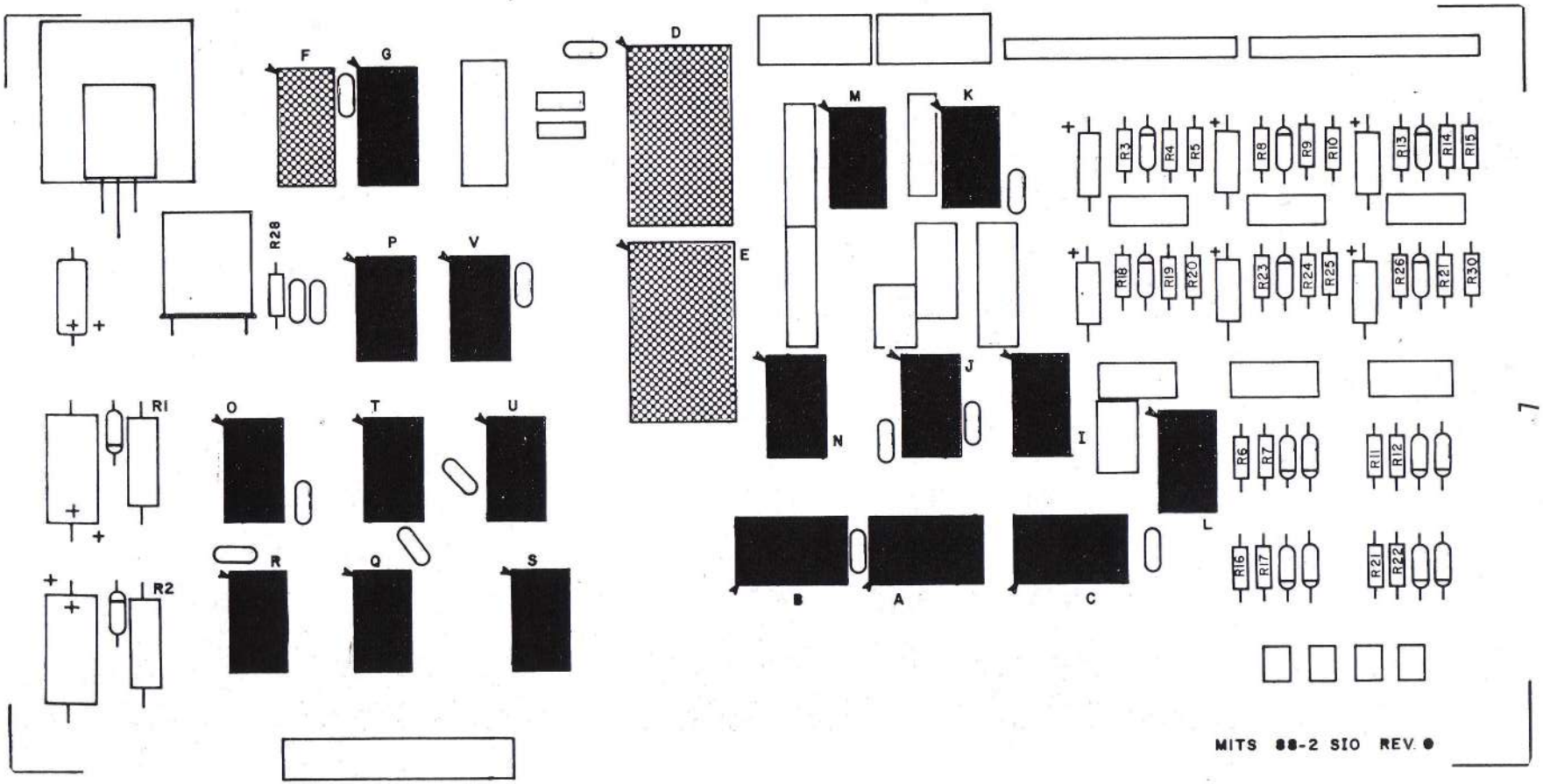
( ) R26, Yellow-Purple-Brown, 1/4 or 1/2 W.

( ) R28, Brown-Black-Blue, 1/4 or 1/2 W

( ) R30, Red-Red-Brown, 1/4 or 1/2 W

NOTE: The component layout shows two resistors labeled R21. Resistor R21, located in the bottom right-hand corner of the layout, next to R22, is color-coded Red-Purple-Red and is 1/4 or 1/2 W. Resistor R21, located in the middle right of the layout, next to R30, is color-coded Brown-Green-Red and is 1/4 or 1/2 W.

Screened blocks indicate partially-installed components.



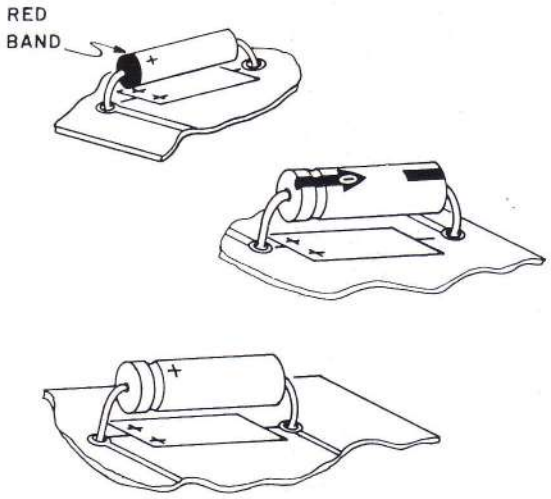
CAPACITOR INSTALLATION

The 88-2SIO Board requires two 56 pf capacitors (C9, C10), twelve .1 µf capacitors (labeled SC) and nine electrolytic capacitors of varying values (C1-C8, C11).

Nine of the capacitors are designated electrolytic, because their polarity requirements must be noted before installation.

The polarity markings of each electrolytic capacitor for the 88-2SIO board will appear as one of the following types:

ELECTROLYTIC CAPACITOR



If the marking is the arrow type, a negative sign will appear in the tip of the arrow. Orient the capacitor so that the arrow points to the negative polarity side. If the marking is one of the other two types, orient the capacitor so that the positive signs match the positive polarity side. Polarity is designated on the silk-screened side of the 88-2SIO board.

Referring to the component layout on page 10 and the parts chart on page 9, install each electrolytic capacitor (C1-C8, C11) as follows:

1. Referring to the parts chart, choose an electrolytic capacitor with the value that matches the part number.

2. Bend the two leads of the capacitor at right angles to match their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board. Be sure to orient the capacitor correctly.

3. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the two leads to the foil pattern, and clip off any excess lead lengths.

4. After making sure that there are no solder bridges, check each electrolytic capacitor off of the parts list as you install it.

Use the following procedure to install each of the two 56 pf capacitors (C9, C10) and each of the twelve .1 µf capacitors (labeled SC).

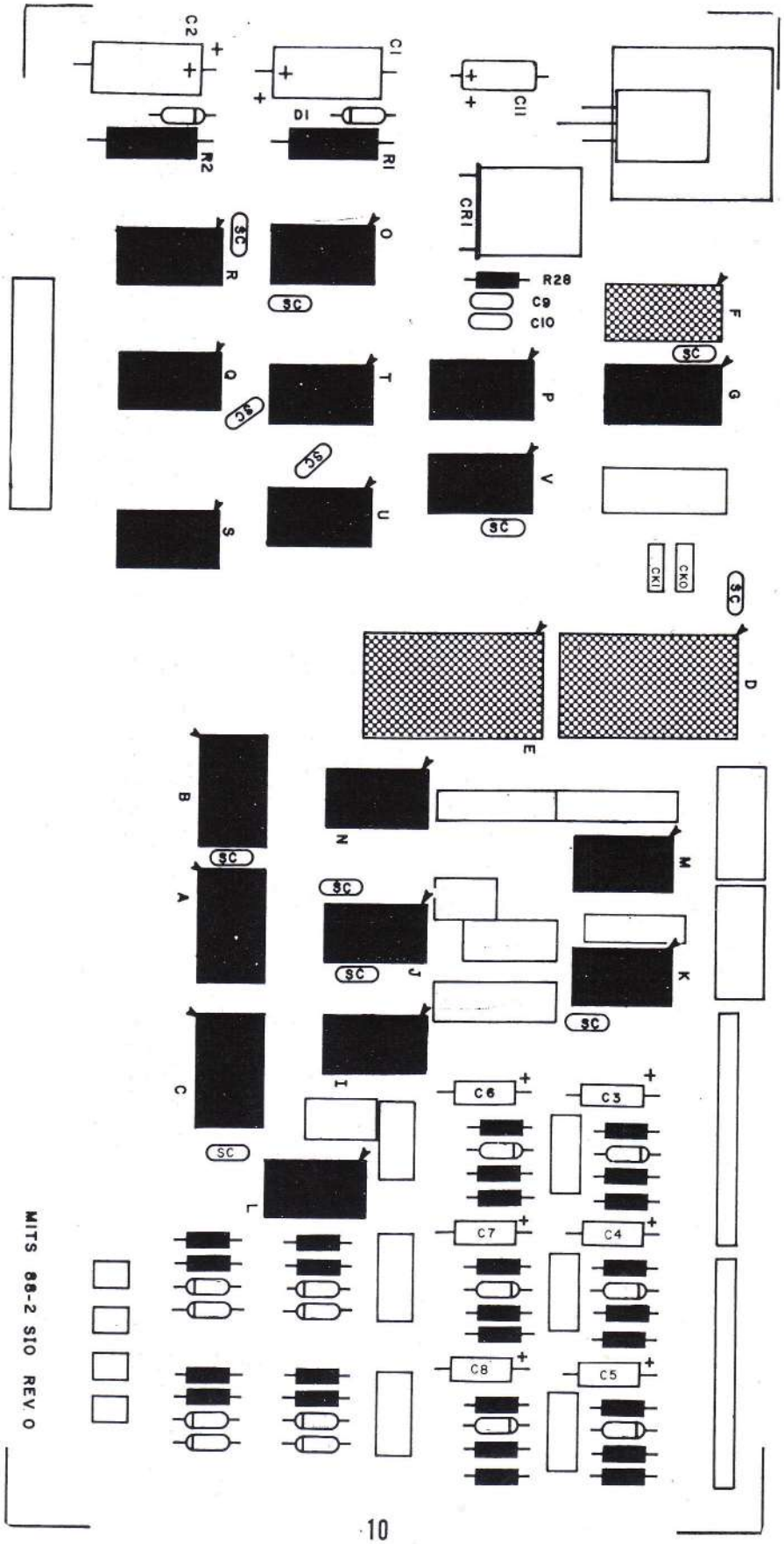
1. Using needle-nose pliers, straighten the two leads as necessary to fit their respective holes on the 88-2SIO board.

2. Insert the capacitor into the correct holes from the silk-screened side of the board. Push the capacitor down until the ceramic insulation almost touches the foil pattern.

3. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil pattern and clip off any excess lead lengths.

4. Be sure that there are no solder bridges, and check each capacitor off of the parts list on this page after it is installed.

CAPACITORS
( ) C1, electrolytic, 33 µf.
( ) C2, electrolytic, 33 µf.
( ) C3, electrolytic, 1 µf.
( ) C4, electrolytic, 1 µf.
( ) C5, electrolytic, 1 µf.
( ) C6, electrolytic, 1 µf.
( ) C7, electrolytic, 1 µf.
( ) C8, electrolytic, 1 µf.
( ) C9, 56 pf.
( ) C10, 56 pf.
( ) C11, electrolytic, 33 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.
( ) SC, .1 µf.


C2
C1
C11
D1
R2
R1
CR1
R28
C9
C10
SC
R
O
F
G
Q
T
P
S
U
V
CK1
CKO
D
E
B
N
M
A
J
K
C
I
C6
C3
L
C7
C4
C8
C5
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DIODE INSTALLATION

There are two 12 volt zener diodes and 14 1N914 diodes to be installed on the 88-2SIO board.

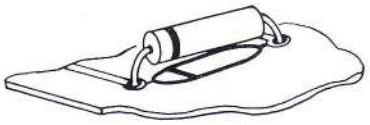
NOTE: Diodes are marked with a band to indicate the cathode end. The diode must be oriented so that the banded end corresponds with the band printed on the 88-2SIO board. Failure to orient diodes correctly may result in permanent damage to your unit.

Referring to the parts chart on this page and the component layout on page 12, install each diode according to the following instructions.

1. Refer to the diode parts chart to be certain that you choose the diode with the part number that correctly corresponds to its position on the component layout.

2. Bend the leads of the diode at right angles to match the correct holes on the board.

3. Be certain that the banded end of the diode matches the band on the silk-screened side of the board.

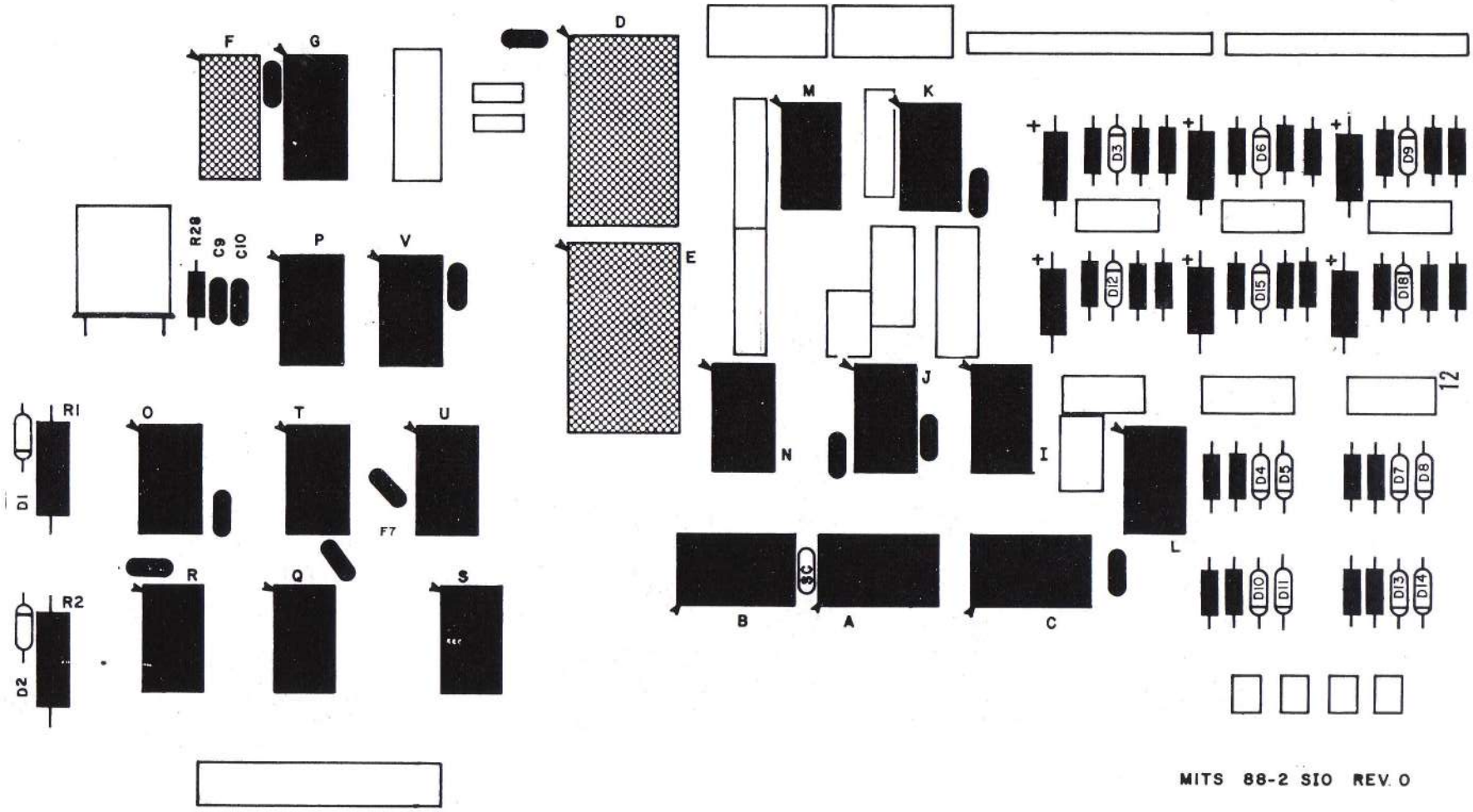


DIODE

Insert the diode into the correct holes from the silk-screened side, of the board. Turn the board over, and bend the leads slightly outward.

4. Solder the two leads to the foil pattern on the back side of the board. Clip off any excess lead lengths. Check each diode off of the parts list as it is installed.

DIODES
( ) D1, 12 volt zener
( ) D2, 12 volt zener
( ) D3, 1N914
( ) D4, 1N914
( ) D5, 1N914
( ) D6, 1N914
( ) D7, 1N914
( ) D8, 1N914
( ) D9, 1N914
( ) D10, 1N914
( ) D11, 1N914
( ) D12, 1N914
( ) D13, 1N914
( ) D14, 1N914
( ) D15, 1N914
( ) D18, 1N914



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TRANSISTOR INSTALLATION

There are four EN2907 transistors to be installed on the 88-2SIO board.

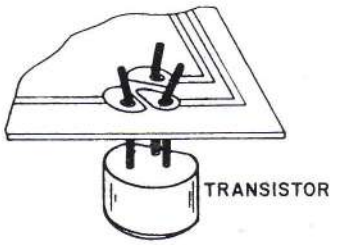
NOTE: Before installing each transistor, ensure that you check the part number before soldering it into place. Some transistors are identical in physical appearance, but differ in electrical characteristics. If the part number on your transistors does not match the number EN2907, it may be that you have a substitution. In this case, refer to the Transistor Identification Chart included with this manual to be certain that it is a correct substitution.

Referring to the parts chart and component layout on this page and the Transistor Identification Chart on the next page, install each transistor (Q1-Q4) according to the following procedure.

1. After ensuring that the part number is correct, note the shape of the transistor. The transistor is rounded with one flat edge. The lead nearest the flat edge is called the emitter. The correct hole for the emitter is opposite the Q1, Q2, Q3, or Q4 marking and is labeled E on the component layout.

2. Orient the transistor so that the emitter aligns with the correct hole on the board. Insert the transistor from the silk-screened side of the board. The other two leads should fit into their respective holes easily. It should not be necessary to bend the leads, and they should not cross over each other.

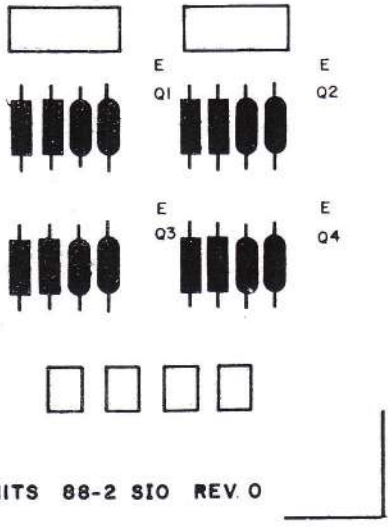
3. Holding the transistor in place, turn the board over, and bend the three leads slightly outward.



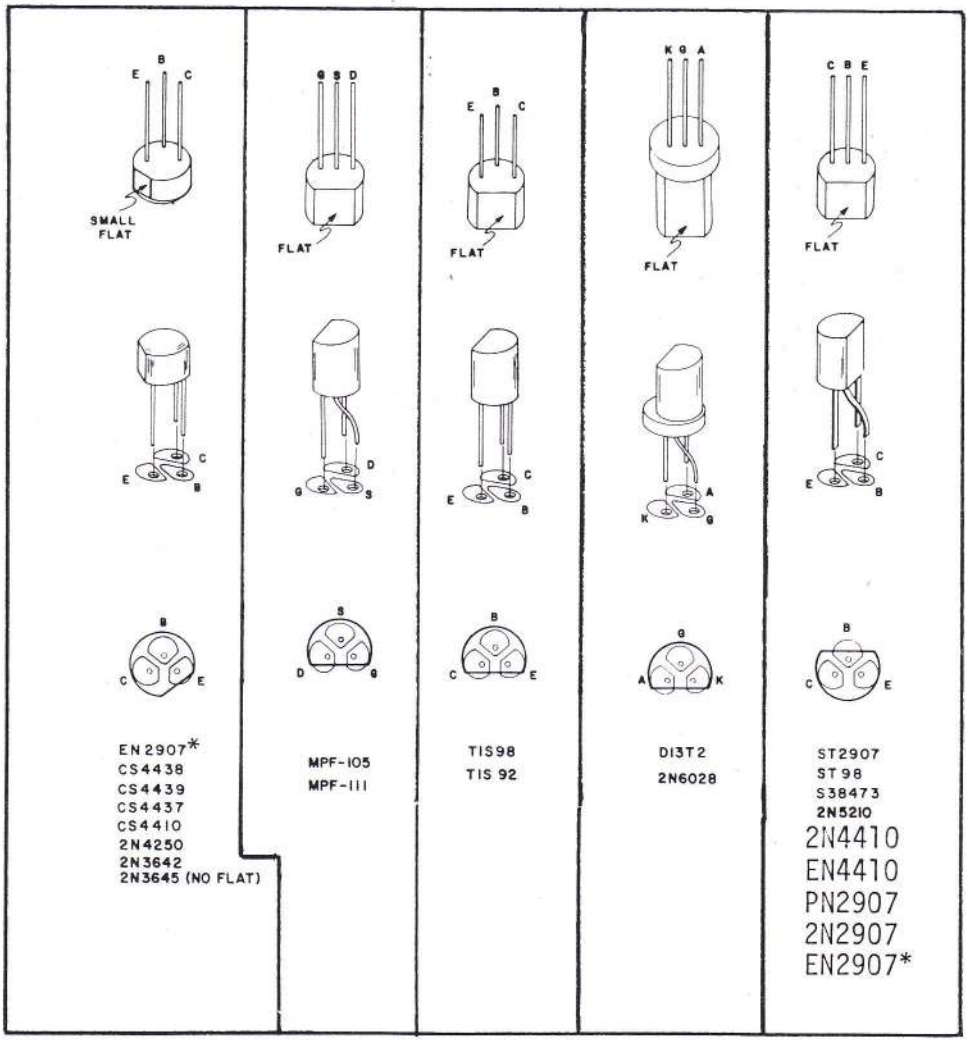
4. Solder the leads to the foil pattern on the back side of the board. Clip off any excess lead lengths.

5. Check each transistor off of the parts list, after it is installed.

TRANSISTORS
( ) Q1, EN2907
( ) Q2, EN2907
( ) Q3, EN2907
( ) Q4, EN2907



TRANSISTOR IDENTIFICATION CHART



IN THE ILLUSTRATION ABOVE THE OUTLINE OF EACH TYPE OF TRANSISTOR IS SHOWN OVER THE PADS ON THE CIRCUIT BOARD WITH THE CORRECT DESIGNATION FOR EACH OF THE THREE LEADS. USE THIS INFORMATION TOGETHER WITH THE INFORMATION IN THE ASSEMBLY MANUAL FOR THE CORRECT ORIENTATION OF THE TRANSISTORS AS YOU INSTALL THEM.

THE FOLLOWING IS A LIST OF POSSIBLE SUBSTITUTIONS: IF ANY OTHERS ARE USED YOU WILL RISK DAMAGING YOUR UNIT:

2N4410 = EN4410 = CS4410 = CS4437, CS4438, TIS98, ST98, S38473 (NPN)

EN2907 = 2N2907 = PN2907 = ST2907, CS4439 (PNP)

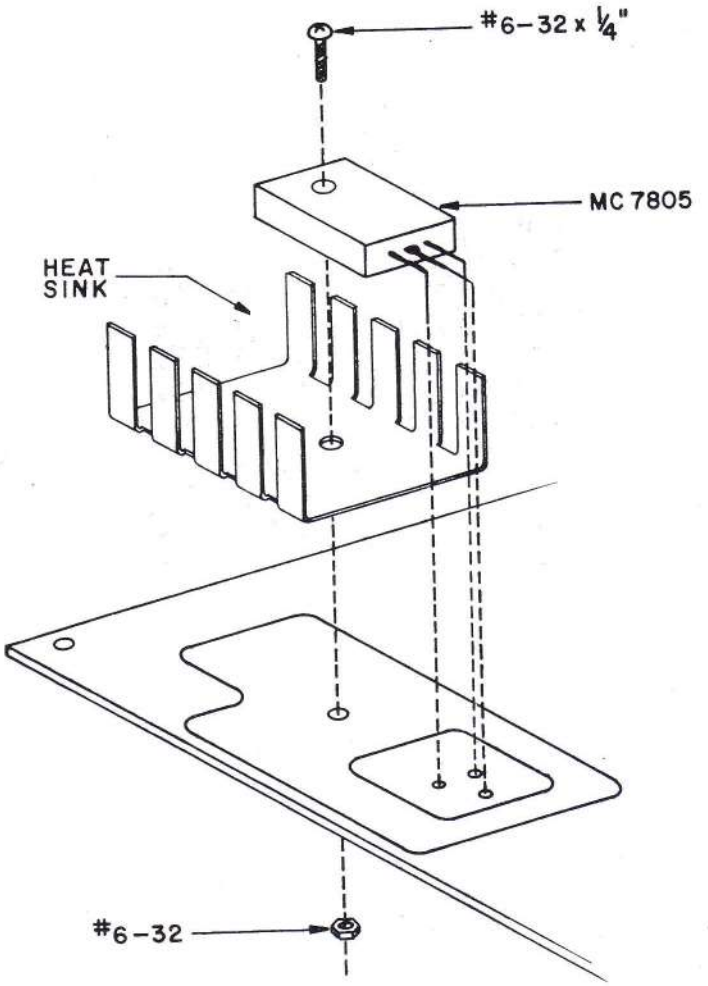
WHEN MAKING SUBSTITUTIONS, REFER TO THE ILLUSTRATION TO DETERMINE THE CORRECT ORIENTATION FOR THE THREE LEADS.

*Configuration of the leads on EN2907 may vary.

VOLTAGE REGULATOR INSTALLATION

There is one 5-volt regulator to be installed on the 88-2SIO board.

1. Set the voltage regulator in place on the board and align the mounting holes. (See drawing below.)



2. Use a pencil to mark the point on each of the three leads where they line up with their respective holes on the board.

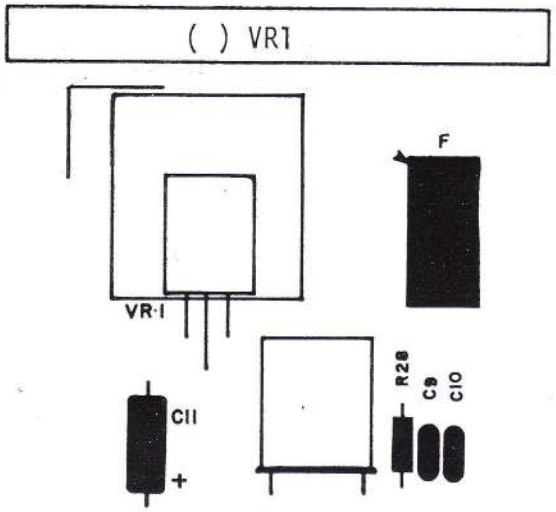
3. Using needle-nose pliers, bend each of the three leads at a right angle on the points where you made the pencil marks.

NOTE: Use heat-sink grease when installing this component. Apply the grease to all surfaces which come in contact with each other.

4. Referring to the preceding drawing, set the regulator and heat sink in place on the silk-screened side of the board. Secure the regulator and heat-sink as shown by the drawing, holding the regulator in place as you tighten the nut.

5. Turn the board over and solder the three leads to the foil pattern on the back side of the board. Be sure not to leave any solder bridges.

6. Clip off any excess lead lengths, and place a checkmark in the blank provided below.



CRYSTAL INSTALLATION

There is one 2.4576 crystal (CR1) to be installed on the 88-2SIO board.

Referring to the component layout on this page, install the crystal according to the following procedure.

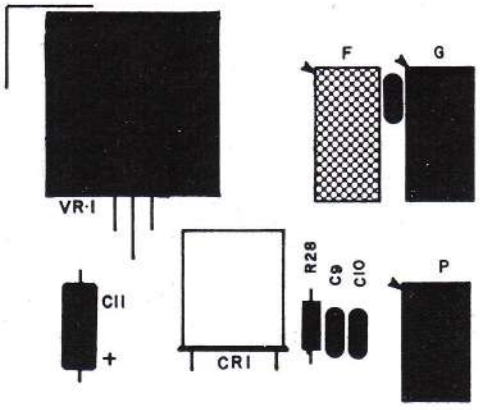
1. Use needle-nose pliers to bend the leads on the crystal at right angles.

2. Insert the leads into the correct holes, until the crystal lays against the board.

3. Holding the crystal in place, turn the board over and bend the leads slightly outward.

4. Solder the leads to the foil pattern and clip off any excess lead lengths. After the crystal is installed, place a checkmark in the blank provided below.

( ) CR1, 2.4576 MHz



HARDWIRE CONNECTIONS

The 88-2SIO board offers several options, depending upon your needs. The board must be hardwired for Address Select, Baud Rate Selection, and for interconnection to the I/O device. Each port may be hardwired for one of three signal interconnects: RS-232 voltage levels; TTL voltage levels; or a TTY 20 milliamp current loop. All hardwire connections must be made with insulated wire.

NOTE: The insulated wire for the 88-2SIO board comes in three-foot lengths. You must cut the wires into lengths appropriate to jumper the pads you are connecting. Each end of the wires you cut must be stripped in order to make adequate lead lengths.

Referring to the component layout on page 20 and the Address Selection Chart on pages 21-23, connect the address selection jumpers as follows:

1. Choose the address selection you want to use according to the Address Selection chart. Be sure that the octal address group that you choose is not used by any other I/O board.

2. Connect pads F2-F7 to A2 or $\overline{A2}$-A7 or $\overline{A7}$ according to the pattern indicated by the Address Selection Chart to obtain the octal addresses 000-003, it is necessary to connect pads F2 to $\overline{A2}$, F3 to $\overline{A3}$, F4 to $\overline{A4}$, F5 to $\overline{A5}$, F6 to $\overline{A6}$, and F7 to $\overline{A7}$.

3. Bend the leads of the insulated wire to fit the corresponding holes. Insert the leads into the correct holes from the silk-screened side of the board.

4. Turn the board over and solder the leads to the foil pattern on the back side of the board. Clip off any excess lengths.

The 10-pin Molex signal-type interconnections may be wired for one of three voltage levels: RS-232 voltage levels; TTL voltage levels; or TTY 20 milliamp current loop. The chart on page 28 indicates which signals are controlled by the wires 1-10 located under S1 and S2.

Referring to the component lavout on page 20 and the Interconnect charts on pages 24 and 25, make the connections according to the following instructions.

NOTE: The wires necessary for interconnection include D1-5, located above IC M; I1-8, located below IC K; J1-4, located above IC J; K1-12, located to the left of IC K and above IC J; L1-4, located to the right of IC I; M1-8, located to the left of IC M; N1-8, located above IC N; S1 and S2 (1-10) located in the top right of IC K; Y10-18, located to the right of IC I; Z1-4, located in the bottom right-hand corner of the silk screen; and, if you are wiring the 2SIO board for two ports, E1-5, located above IC K.

1. Choose which option you wish to implement. Refer to the Interconnect charts, and jumper the pads according to the chart which applies to your selection.

2. Bend the leads of the insulated wire to fit the corresponding holes. Insert the leads into the correct holes from the silk-screened side of the board.

3. Turn the board over and solder the leads to the foil pattern on the back side of the board. Clip off any excess lengths.

Eight baud rates may be connected on the 88-2SIO board: 110; 9600; 4800; 1800; 150; 300; 2400; 1200. Baud rate inputs for port 0 or IC D is CK0 and input for port 1 or IC E is CK1. Either one or both ports may be connected to any one of the eight baud rates silkscreened on the board.

Referring to the component layout on page 20, make the connections according to the following instructions.

1. Choose the baud rates and ports you wish to interconnect.

2. Bend the leads of the insulated wire to fit the corresponding holes. Insert the leads into the correct holes from the silk-screened side of the board.

3. Turn the board over and solder the leads to the foil pattern on the back side of the board. Clip off any excess lengths.

INTERRUPT

The 88-2SIO board is designed to provide the capability for interrupt at eight levels via the 88-Vector Interrupt, at one level via the interupt request line provided on the 88-2SIO board, or no interrupt at all. Any one of these three options may be implemented.

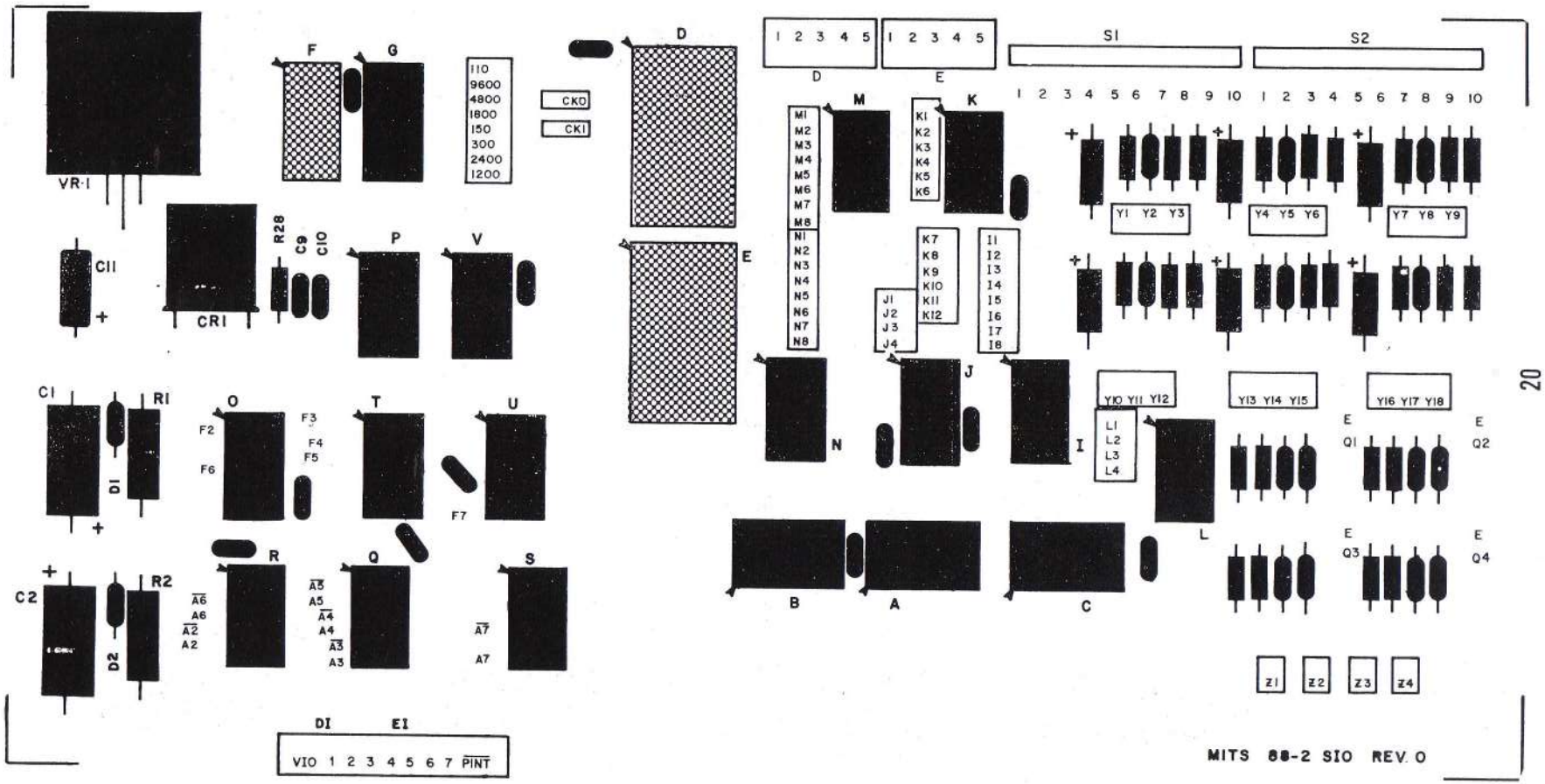
NOTE: The processor is capable of handling only one interrupt signal. If the single level interrupt request line of the 88-2SIO board is implemented, no other board can be hardwire connected to the processor for interrupt. Refer to the Theory of Operation section for further explanation of interrupt functions.

If you choose to implement the single interrupt system, refer to the component layout on page 20 and connect the jumper wires as follows:

1. Choose which interrupt request line (DI, EI) you want to use. DI corresponds to Port 0 and EI corresponds to Port 1.

2. Connect the chosen interrupt request line or lines to the pad marked $\overline{\text{PINT}}$. Bend the leads of the insulated wire as necessary and insert them into the correct holes from the silk-screened side of the board. All interrupt request leads must be inserted in the hole marked $\overline{\text{PINT}}$.

3. Turn the board over and solder the leads to the foil pattern on the back side of the board. Clip off any excess lengths.



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The four octal addresses noted in the chart below represent the control and data channels of Ports 0 and 1. Even-numbered addresses indicate control channels and odd-numbered addresses indicate data channels. The first two addresses are Port 0 and the second two are Port 1, so that for addresses 000-003, 000 is the control channel of Port 0; 001 is the data channel of Port 0; 002 is the control channel of Port 1; and 003 is the data channel of Port 004.

I/O ADDRESS SELECTION CHART

Address Octal	Connections					
000-003	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
004-007	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2
010-013	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$
014-017	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2
020-023	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$
024-027	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2
030-033	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$
034-037	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	A2
040-043	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
044-047	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2
050-053	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$
054-057	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	A2
060-063	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$
064-067	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	A2
070-073	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	$\overline{A2}$
074-077	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	A2
100-103	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
104-107	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2
110-113	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$
114-117	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	A2
120-123	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$
124-127	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	A2

Address Octal	Connections					
130-133	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	$\overline{A2}$
134-137	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	A2
140-143	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
144-147	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	A2
150-153	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	$\overline{A2}$
154-157	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	A2
160-163	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	$\overline{A2}$
164-167	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	A2
170-173	$\overline{A7}$	A6	A5	A4	A3	$\overline{A2}$
174-177	$\overline{A7}$	A6	A5	A4	A3	A2
200-203	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
204-207	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2
210-213	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$
214-217	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2
220-223	A7	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$
224-227	A7	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2
230-233	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$
234-237	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	A2
240-243	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
244-247	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2
250-253	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$
254-257	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	A2
260-263	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$
264-267	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	A2
270-273	A7	$\overline{A6}$	A5	A4	A3	$\overline{A2}$
274-277	A7	$\overline{A6}$	A5	A4	A3	A2
300-303	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
304-307	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2

Address Octal	Connections					
310-313	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$
314-317	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	A2
320-323	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$
324-327	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	A2
330-333	A7	A6	$\overline{A5}$	A4	A3	$\overline{A2}$
334-337	A7	A6	$\overline{A5}$	A4	A3	A2
340-343	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$
344-347	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	A2
350-353	A7	A6	A5	$\overline{A4}$	A3	$\overline{A2}$
354-357	A7	A6	A5	$\overline{A4}$	A3	A2
360-363	A7	A6	A5	A4	$\overline{A3}$	$\overline{A2}$
364-367	A7	A6	A5	A4	$\overline{A3}$	A2
370-373	A7	A6	A5	A4	A3	$\overline{A2}$
374-377	A7	A6	A5	A4	A3	A2

SIGNAL TYPE INTERCONNECT

RS-232 VOLTAGE LEVELS (±12 Volt Levels)

	PORT 0		PORT 1	
Signal	Jumper	Jumper	Jumper	Jumper
1. Receive	D3 to I4	I3 to S1-7	E3 to J1	J2 to S2-7
2. Transmit	D5 to N4	N3 to S1-8	E5 to N6	N5 to S2-8
3. Ground*	--	S1-4 to S1-10	--	S2-4 to S2-10
4. Clear to Send (CTS)	D2 to I7	I8 to S1-1	E2 to I2	I1 to S2-1
5. Data Carrier Detect (DCD)	D1 to I5	I6 to S1-2	E1 to J3	J4 to S2-2
6. Request to Send [(RTS), also can be used for Data Terminal Ready]	D4 to N2	N1 to S1-3	E4 to N8	N7 to S1-3

* If Receive, Transmit, and Ground are all that your I/O device requires, ignore the other signal connections.

TTL VOLTAGE LEVELS

	PORT 0		PORT 1	
Signal	Jumper	Jumper	Jumper	Jumper
1. Receive	D3 to K12	K11 to S1-9	E3 to K2	K1 to S2-9
2. Transmit	D5 to M1	M2 to S1-5	E5 to M5	M6 to S2-5
3. Ground*	--	S1-4 to S1-10	--	S2-4 to S2-10
4. CTS	D2 to K8	K7 to S1-1	E2 to K6	K5 to S2-1
5. DCD and/or Data Terminal Ready	D1 to K10	K9 to S1-2	E1 to K4	K3 to S2-2
6. RTS, also can be used for Data Terminal Ready	D4 to M3	M4 to S1-3	E4 to M7	M8 to S2-3

* If Receive, Transmit, and Ground are all that your I/O device requires, ignore the other signal connections.

SIGNAL TYPE INTERCONNECT

TTY 20 MILLIAMP CURRENT LOOP

	PORT 0				PORT 1			
Signal	Jumper	Jumper	Jumper	Jumper	Jumper	Jumper	Jumper	Jumper
1. Receive	D3 to K12	K11 to Y7	Y8 to S1-6	Y9 to S1-7	E3 to K2	K1 to Y16	Y17 to S2-6	Y18 to S2-7
2. Transmit	D5 to L1	--	--	Z2 to S1-5	E5 to L3	--	--	Z1 to S2-5
3. Ground*	--	--	--	S1-4 to S1-10	--	--	--	S2-4 to S2-10
4. CTS	D2 to K8	K7 to Y1	Y2 to S1-8	Y3 to S1-9	E2 to K6	K5 to Y10	Y11 to S2-8	Y12 to S2-9
5. DCD and/or Data Terminal Ready	D1 to K10	K9 to Y4	Y5 to S1-1	Y6 to S1-2	E1 to K4	K3 to Y13	Y14 to S2-1	Y15 to S2-2
6. RTS, also can be used for Data Terminal Ready	D4 to L2	--	--	Z4 to S1-3	E4 to L4	--	--	Z3 to S2-3

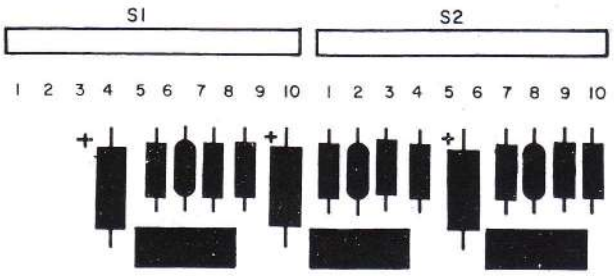
* If Receive, Transmit, and Ground are all that your I/O device requires, ignore the other signal connections.

WAFER CONNECTOR INSTALLATION

There are one or two 10-pin male connector(s) to be installed on the 88 2-SIO board. Referring to the component layout on this page install the 10-pin male connector(s) according to the following procedure.

1. Referring to the drawing below, insert the 10-pin wafer connector into the correct holes on the board from the silk-screened side. Be sure to insert the side with the shorter, straight pins, and be certain that the long pins are facing down, or toward the board's components.

2. Holding the connector in place, turn the board over and solder the 10 pins to the foil pattern on the back side of the board.



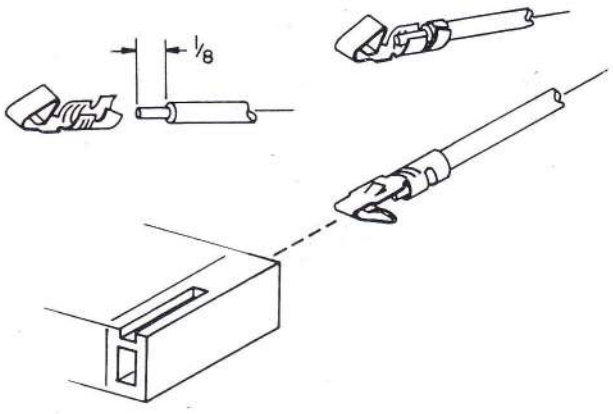
I/O CONNECTOR WIRING

There are one or two 10-pin female connector(s) and multi-conductor cable(s) to be installed on the 88 2SIO board. The number of connectors depends upon the number of I/O ports on your board. Referring to the component layout on page 26 wire the connector(s) and cable(s) together according to the following procedure. Make connections for Port 0 via S1 and Port 1 via S2.

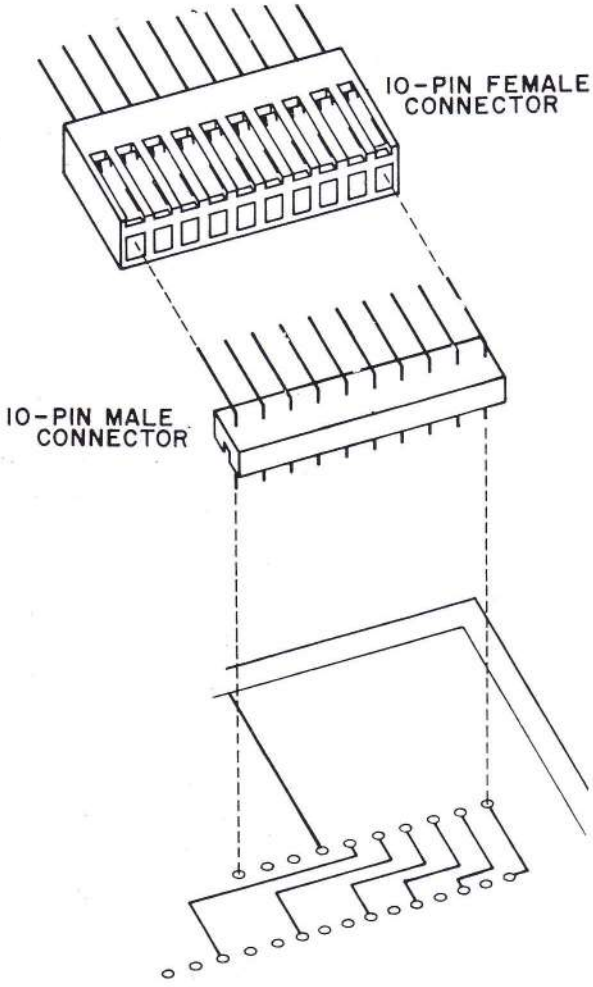
1. Using a small sharp knife, strip 1 1/4" of cable sheath from one end and two inches of cable sheath from the other end of the 10 conductor cable. Do this by cutting a circle around the sheath, being very careful not to cut into the insulation of the wires inside, and pulling the end off of the wires.

2. On the end with 1 1/2" of wires exposed, strip 1/8" of insulation from the ends of each of the 10 wires and tin the exposed portion by applying a thin coat of solder.

3. Referring to the drawing below, install one of the connector pins onto the end of each of the necessary wires. Do this by crimping the wire into place; then soldering the end to the pin itself.



4. Referrring to the drawing below and the chart on page 28, insert the pins one at a time into the female connector. As you insert each pin, note the color of the wire and label the same wire on the opposite end with the designation indicated by the chart. It is very important that you maintain the wire orientation indicated by the chart.



NOTE: If you are wiring the 88-2SIO port(s) for TTY or RS-232, you may wire each of these devices for standard interconnection. Refer to the chart and diagram on pages 29 and 30 for these wiring instructions.

SIGNAL CONNECTIONS

10-PIN MOLEX TO DEVICE

	Pin Number									
	1 2	3	4	5	6 7	8 9	10
TTY	DCD (no polarity)	Request to Send (+)	Ground	Transmit (+)	Receive (no polarity)	Clear to Send (no polarity)	Ground

	Pin Number									
	1	2	3	4	5	6	7	8	9	10
TTL	Clear to Send	DCD	RTS	Ground	Transmit				Receive	Ground

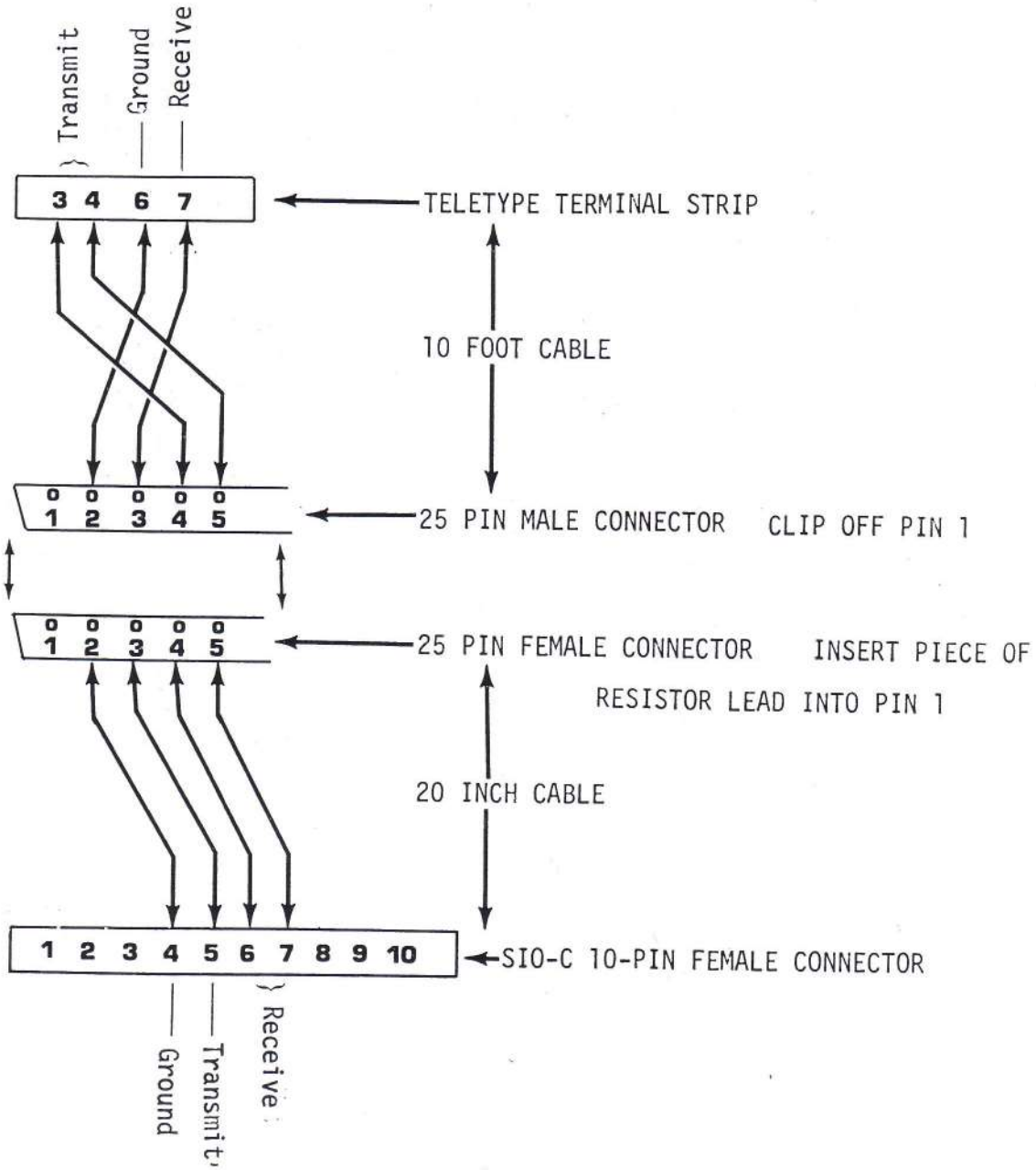
	Pin Number									
	1	2	3	4	5	6	7	8	9	10
RS-232	CTS	DCD	RTS	Ground			Receive	Transmit		Ground

THE FOLLOWING CHART INDICATES THE NORMAL INTER-CONNECTIONS TO BE MADE IF YOU WANT TO WIRE YOUR BOARD FOR RS-232 COMPATIBILITY.

SIGNAL DESCRIPTION	PIN NUMBER
Receive	2
Request to Send	4
Clear to Send	5
Transmit	3
Carrier Detect	8
Data Terminal Ready	20
Signal Ground	7

TTY INTERCONNECTIONS

THE FOLLOWING DIAGRAM ILLUSTRATES THE NORMAL INTERCONNECTIONS BETWEEN THE 88-2SIO BOARD AND A FULL DUPLEX, 20 MILLIAMP CURRENT-LOOP TELETYPE (KSR33 OR ASR-33).



BOARD INSTALLATION

The 24-pin 6850 IC(s) (D, E) and the 16-pin 4702 IC (F) may be installed now.

1. Review the "MOS IC Special Handling Procedures" on page 5 of the ALTAIR 8800 Assembly Manual. Note, failure to carefully follow the instructions of the "MOS Special Handling Procedures" may result in permanent damage to static-sensitive ICs.

2. Insert the 6850 IC and the 4702 IC into the sockets on the 88-2SIO board. Handle the IC(s) carefully, and use as little pressure as possible when inserting the IC(s).

Install the edge connector provided with the board according to the procedure described on page 64 in the assembly manual "EXPANDER BOARD 8800 M/BD ASSEMBLY".

Press the 88-2SIO board into the edge connector. The board should be oriented so that the silk-screened side faces the right side of the unit viewed from the front panel. Mount the 25-pin connector(s) in the space(s) provided on the ALTAIR back panel.