# InterSystems™

# Series II Microcomputer Catalog

## INTELLIGENT COMPUTER PRODUCTS FOR INTELLIGENT USERS


WINTER, 1980

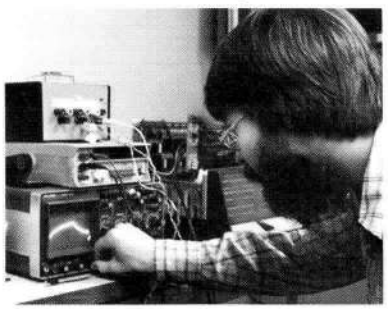
# ABOUT OUR COMPANY

Ithaca Intersystems Incorporated was born from a simple idea: to build and support intelligent computer products for intelligent users. We're not a

computer company for everyone. Our aim is to provide demanding users—programmers, scientists, researchers, educators, students and OEMs—with high-performance, low-cost computing power through the use of high technology.

Our approach is always user-centered—creating elegant solutions to information processing problems in data collection, analysis, synthesis, process control, etc., that are faster, more flexible and economical...as well as expandable for the future. You see it in everything we do. In the 'intelligent' front panel of our DPS-1 mainframe. In the self-contained modular approach of all our products, where each board is optimized for maximum performance in *any* system. And in software that includes our universally-acclaimed Z-80 Pascal.

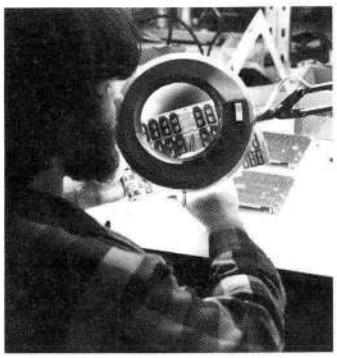
The latest result of this approach is an entirely new generation of advanced 8- and 16-bit small computer products, built around the IEEE S-100 Bus Standard, which we helped pioneer. A new line of products not only more flexible and powerful than existing S-100 computers, but also many existing *minicomputers,* as well. Compatible with most present S-100



systems, they allow small system users to upgrade at competitive prices, without facing obsolescence when 16-bit operation or other refinements are desired in the future. We've also created the first *mainframe* designed from the outset for full IEEE S-100 operation. And that's only the beginning.

We call these new products Series II, and they are available either as a complete computer system for turn-key operation, as modules for inclusion in OEM systems, or for use in existing S-100 machines.

As Ithaca Audio, our company was known as a leading source of innovative hardware and software for S-100 systems. Now, as Ithaca Intersystems, we're producing the broadest, most



versatile line of IEEE S-100 boards today. Offering small computer users a way to improve the performance of their present systems now...without obsoleting their investment in the future. And a way to step into the future today, with a system that's ready for tomorrow.

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## ABOUT THIS CATALOG

*Aside from acquainting you with Intersystems and its products, our aim is to offer a convenient reference tool on the IEEE S-100 Bus, its configuration and operation.*

*We welcome your questions, as well as your comments and suggestions about how our catalog—and products—can serve you even better in the future.*

# The S-100 Bus System– an overview

Since the introduction of the S-100 Bus in 1975, more computers of this type have been sold than any other bus-structured machine. However, until recently, there was no exact agreement among manufacturers on the timing and position of all S-100 signals.

Now, with the adoption of the IEEE S-100 Bus Standard, there is a uniform basis for system architecture, as well as the foundation for a new, more powerful generation of small computer components and systems.

**Architecture**

All communications between IEEE S-100 modules take place on a single, unified bus which connects memory elements, I/O interface and control elements to the central processor. For maximum throughput, address, data and control information are transmitted via independent lines.

Twenty-four address bits provide for memory expansion to 16 megabytes of directly-addressable main memory or virtual storage. Direct addressing means advanced memory management systems previously available only on large machines are now accessible to microcomputer users.

In an IEEE S-100 system, 16 data lines are operated either as uni-directional lines (during 8-bit transfers) or bi-directional lines (during 16-bit transfers). This results in a number of important benefits, including easy upgrading from 8- to 16-bit operation; the ability to use 8-bit and 16-bit CPUs within the system at the same time and the flexibility of utilizing sophisticated 8-bit peripherals (e.g. DMA disks) with 16-bit processors.

**Operation**

S-100 is a psuedo-synchronous bus. This means it is considered to be in an idle state until the beginning of the cycle, when the processor first places the address of the desired memory location or I/O interface on the address lines; then follows with control signals that indicate the address is valid and a signal indicating if the transfer is to be 8- or 16-bit. The addressed module then interprets the control signals and responds either by accepting data transmitted (a write) or by transmitting data to the processor (a read) in the proper 8- or 16-bit format.

If faster data transfer is required, the I/O interface module may use the Direct Memory Access (DMA) technique. During DMA operation, the I/O device interface actually generates the bus address and control signals in exactly the same way as the processor. It gains control by asserting its own priority on four special DMA request lines unless another DMA device of higher priority is present. As a result, priority is automatically given to the highest-priority DMA device requesting the bus. The processor then issues a DMA grant as soon as the current bus operation is complete, rather than waiting to complete the current instruction.

Up to 16 DMA devices may be operating in a Series II system at a time. In other words, *up to 16 high-speed peripherals*—floppy disks, hard disks, number crunchers—*simultaneously working without interference.* Or up to 16 CPUs, each solving a piece of a problem, for increased throughput.

Intersystems' Series II S-100 system also provides a fully vectored, prioritized interrupt scheme, with eight primary and

*nearly unlimited* secondary interrupts. Every interrupt stimulus can have its own vector and interrupt service routine, eliminating the need to poll I/O devices to find the source of an interrupt.

For greater flexibility, the priority of an I/O device is independent of position on the bus—and completely programmable. The processor can enable or disable interrupts for a particular device—or all interrupts in the system—via individual control and status registers.

Interrupts are initiated by a peripheral asserting one of eight interrupt request signals on the bus. After concluding the current instruction, the processor responds to the highest-priority interrupt by issuing an interrupt grant. The asserting peripheral responds by placing a vector on the bus which the processor interprets as a pointer to the starting address of the corresponding interrupt service routine. Each peripheral may also contain on-board interrupt prioritization in addition to the 8 system interrupts—and these also may be masked or changed at will.

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**For more information:**
As leaders in IEEE S-100 bus design, manufacture and support, we'll be happy to provide more information about the IEEE S-100 Bus Standard, our Series II boards and systems, or any other aspect of hardware or software design. Please write or call our Application Engineers.

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**INTERSYSTEMS SERIES II:**
**Ready for tomorrow;**
**more performance today.**

Computer technology isn't standing still: if anything, its pace of growth and innovation is increasing. And large buses housed in strong metal boxes are not enough to guarantee versatility and long, useful life when you have to completely replace your computer boards in order to upgrade to a 16-bit system (or even just a more versatile 8-bit system) in the future.

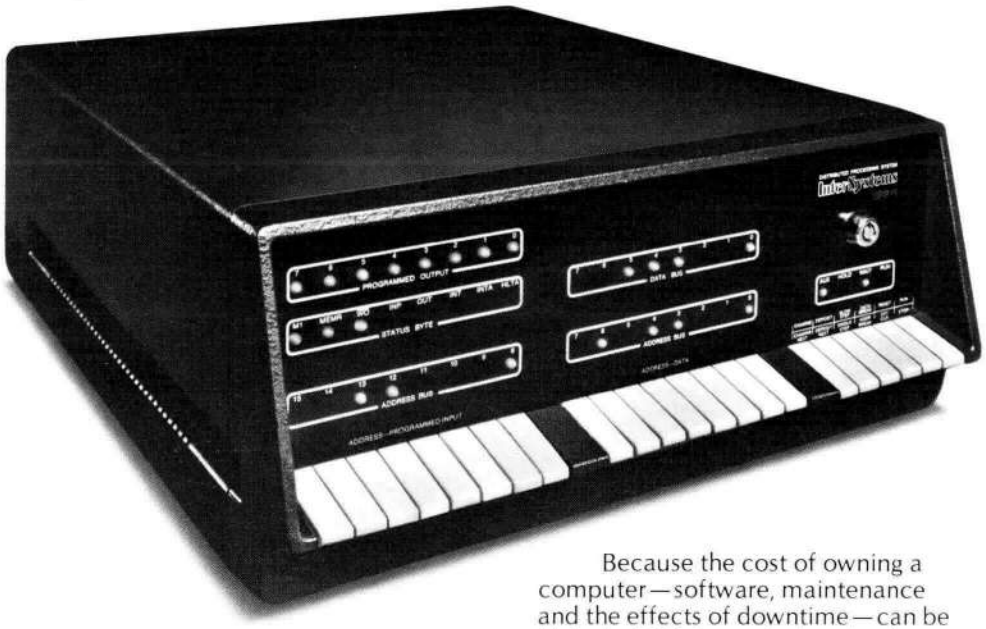
Intersystems Series II is an intelligent solution to the problem of expansion without obsolescence: a high-performance modular system designed for 8- and/or 16-bit operation. Every Series II board is compatible with any IEEE S-100 module, regardless of manufacturer, as well as almost all earlier S-100 products and systems. Enabling you to integrate them with a wide variety of mainframes and peripherals available from more than one hundred manufacturers producing S-100 products.

All Series II boards are designed and tested for reliable operation up to 4MHz and beyond. Each module is burned in for a minimum of 150 hours assuring long-term, trouble-free operation.

**Series II features include:**

- Internationally-standardized bus
- Full IEEE compatibility for 8- or 16-bit operation
- Full 24 address bits for up to 16 megabytes of direct-access or virtual memory
- Full DMA, for more efficient data management
- *True* obsolescence insurance
- Improved architecture for greater system throughput
- Cleaner, more conservative design for increased reliability
- Sophisticated diagnostics, for faster debugging, easier maintenance, lower costs
- Advanced software, including sophisticated compilers for more efficient programming
- And much, much more

# THE DPS-1 MICROCOMPUTER MAINFRAME: Heart of the Series II System



- Versatile front-panel computer mainframe—also available without panel for OEM and other applications
- Reliable 4MHz operation
- Hardware breakpoints
- Full IEEE S-100 bus
- Includes Intersystems MPU-80 —world's most advanced Z80 CPU
- Twenty-slot shielded, dynamically-terminated motherboard
- Heavy-duty, 25-amp power supply

## Description

Extremely modular, the DPS-1, like the entire Series II system, was designed to be a lasting investment, not something you will outgrow in a year or two. Our large 20-slot backplane and 25-amp power supply means always enough room for memory, peripherals or that special interface. And Intersystems' advanced IEEE S-100 bus structure guarantees compatibility with literally hundreds of boards, including the advanced 16-bit processors—a Series II exclusive.

Because the cost of owning a computer—software, maintenance and the effects of downtime—can be high, the DPS-1 was designed to be extremely reliable and maintainable. One of the computer's twenty slots contains the most advanced diagnostic tool we know of for any system of this size—the DPS Front Panel.

Unlike similarly-priced "Black Box" computers that can be difficult to repair without special equipment or spare boards, the DPS-1 can not only tell you if something is wrong, but *where* the fault is and *how* to fix it. Because a Series II System is both more reliable and less costly to repair, *it is less costly to own.*

The front panel, with its molded dress panel, integral switches, and binary readout, has been designed with simplicity and diagnostic capability in mind. Binary format has been deliberately chosen instead of the more fashionable hexadecimal or octal display to facilitate trouble shooting and "testability." But the versatility of the DPS-1 front panel doesn't stop here. It helps debug software, too. Because our front panel doesn't stop at Examine. Examine Next, Deposit, and Deposit Next either. For example, in addition to Single Step, we provide a Slow Step function. Watch a program execute at any speed from .1 to 1000 instructions per second. Unique built-in hardware breakpoints solve problems software breakpoints can't—like tracing real-time interrupt driven software, and DMA (Direct Memory Access) peripherals. Coupled with your lab oscilloscope, this creates a logic analyzer that finds elusive faults easily.

Each front-panel function is remarkably easy to use and may be combined to perform sophisticated tests you'll use and appreciate for years to come.

Like the front panel, the DPS-1 Motherboard is completely state-of-the-art. Twenty card slots allow nondisruptive expansion of your computing capabilities from just a few cards to a full-blown system customized to your computing requirements. Fully shielded and terminated, the bus includes low impedance grounds between each line and active signal termination to virtually eliminate crosstalk, reflections and other bus noise.

The modular power supply is top-quality too. Bus voltages are individually fused and backed up by a common AC fuse. A convenient Key Switch controls all system power, including the auxilliary power outlet on the rear panel.

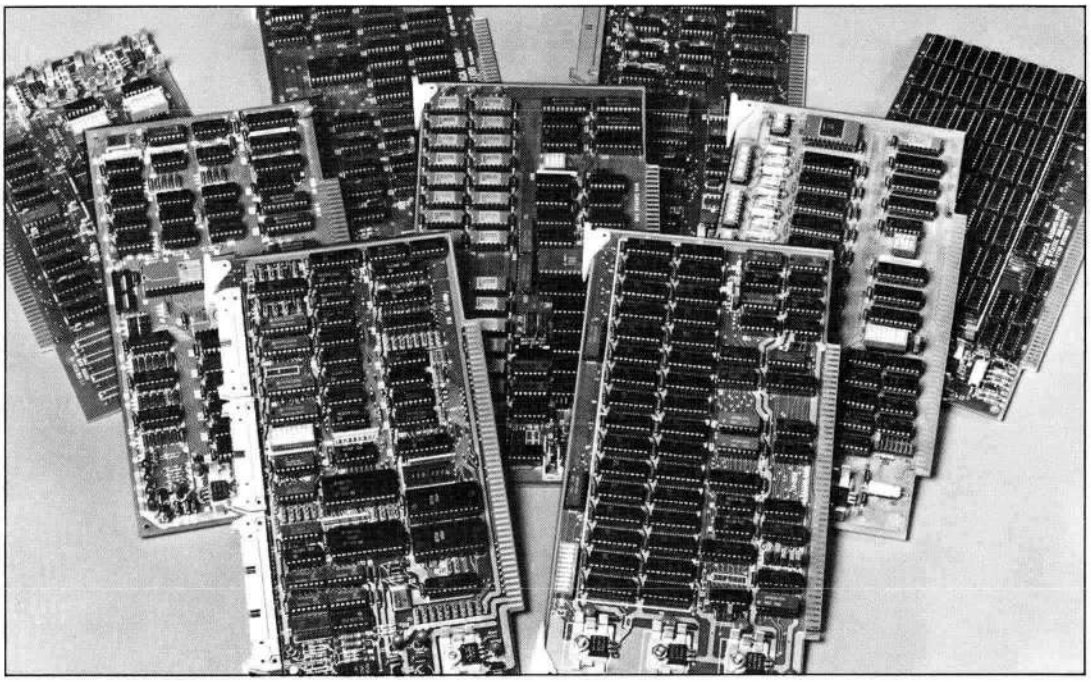
And this power supply won't quit at 15 or 20 amps. It delivers the FULL rated 8 volts at 25 amps continuous load, even with low line voltages.

This handsome, rugged mainframe is constructed of heavy-duty aluminum. The key to the cabinet's strength is its dual-side-channel construction. As attractive as they are practical, these channels act like "I Beams" to maximize the chassis rigidity. So much so, you can stand on it without flexing the top.

The DPS-1 mainframe is just one in the Intersystems Series II family of 8- and 16-bit products. Each of these provides unprecedented quality and flexibility at moderate cost. Every product stresses elegance of design, excellence of manufacture and comprehensive support.

**Model No.** . . . . . **DPS-1**
**Order Part No.** . . . . . **900-0001**

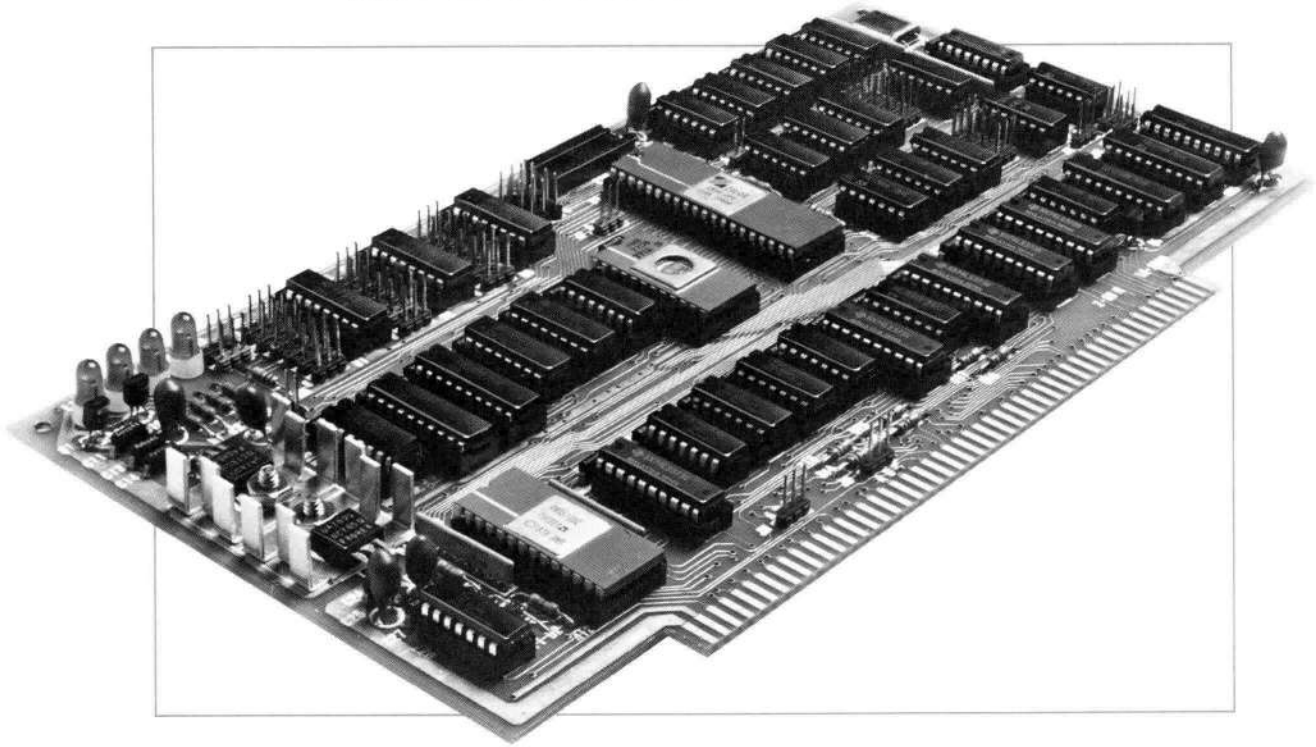
# Series II Computer Cards



Intersystems offers the widest variety of computer modules conforming to the IEEE S-100 Bus Standard. All are designed for high-performance, low-cost computing in a wide variety of systems, including IEEE S-100 OEM products, earlier S-100 systems and of course our DPS-1 mainframe. All cards are manufactured to the highest industrial standards, burned-in for a minimum of 150 hours.

- The widest variety of truly IEEE S-100 compatible cards.
- Reliable operation to 4MHz and beyond
- Fully 8- and 16-bit compatible
- User-selectable functions are all DIP switch or jumper-addressable, eliminating soldering
- All cards include built-in extractors to make insertion and removal faster and safer
- All Series II cards are delivered assembled, tested and burned in at high temperature, for long, trouble-free life.

# The CPU: Our 4MHz MPU-80™



The MPU-80 is a lot more than just an advanced S-100 CPU. Designed around Zilog's high speed 4MHz Z80A, it implements all of the powerful new features of IEEE S-100 while still maintaining upward compatibility with existing hardware.

All Permanent Bus Master signals are generated by the MPU-80. Bus arbitration logic permits up to 16 bus slaves—other CPUs or DMA devices—to be supported simultaneously, making possible for the first time a remarkably flexible S-100 distributed processing system where the computer can work simultaneously on different parts of a problem or run multiple jobs at once.

Our ingenious Memory Map™ feature extends the address space of the Z80 to a full megabyte, more than enough memory for all but the very largest problems. And unlike older bank-select schemes which merely switch whole blocks of RAM in and out, Memory Map 'windows' allow simultaneous access to multiple pages, enhancing versatility.

**MPU-80 Extended Addressing**

Because the Z80 microprocessor generates only 16 address bits—for a total memory space of 64K bytes—and many applications require more than this amount of memory, the MPU-80 includes memory mapping hardware to expand the address range of the Z80 to 1 megabyte (20 address bits).

Two special blocks of memory, each 4K bytes, can be assigned anywhere in the first 64K page (Fig. 1), usually for convenience addresses BØØØ-CFFF. These blocks are then used, either separately or together as one 8K block, as windows to map any other page into page 0, making it possible to either access data directly, or move it between pages. When moving large amounts of code, the high speed Z80 Block Move instruction is employed for even higher speed.

This arrangement permits the MPU-80 to generate real addresses at the processor board, a design much preferred to bank-select schemes, resulting in a system which greatly simplifies memory and peripheral board design, and which is extremely important for future compatibility with the new 16-bit processors and Memory Management hardware.

All eight bus interrupts are prioritized by an on-board Vectored Interrupt Controller, completely programmable for almost unlimited versatility. Interrupts may be masked, rotated, delayed—all under software control. No other board offers this flexibility, making the MPU-80 the undisputed leader in real-time interrupt-driven processing.

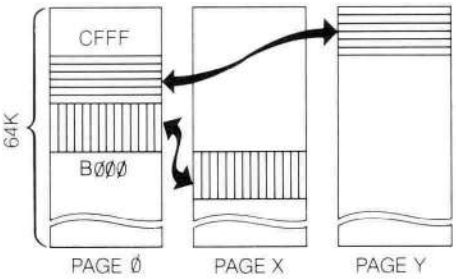



*Figure 1. Memory Management in independent mode as usually supplied. Page 0 map is user-selectable to any 4K block.*

Other features include an optional, jumper-selectable automatic jump to any 1K memory address, room for one 2708 or 2716 EPROM, and switch-selectable 2/4 MHz operation.

All MPU options, including the user-selectable jump, EPROM addressing, and 2/4 MHz operation, are jumper-selectable for set-up ease.

And like the entire Series II line, the MPU-80 is fully-compatible with all Intersystems' products—both 8- *and* 16-bit.

The MPU-80 comes with a listing for our powerful MBUG monitor. The monitor is also available in PROM, for use in the socket provided.

**Model No. . . . . MPU-80**
**Order Part No. . . . . 813-2010**

# Series II Memory

There are two types of RAM—Static and Dynamic.

Dynamic RAM costs less per bit because more memory can be put into an IC chip, but there is the additional fixed overhead for refresh circuitry. Hence for larger systems, 65K bytes or greater, dynamic RAM is preferred, while smaller systems usually are more cost-effective with the simpler static RAM.

Unlike older Dynamic RAM boards, which often experienced problems, Series II Dynamic RAM—thanks to Intersystems' priority arbitration scheme—operates exactly the same as a static board, including the ability to work with a front panel and perform infinite-length DMA.

Because customers have differing memory requirements, Intersystems offers the best of both types of RAM.

**DATA TRANSFER ON THE S-100 BUS**

The S-100 data bus supports both byte parallel (8-bit) and word parallel (16-bit) data transfers, hence allowing both 8-bit and 16-bit processors to use the same memory boards, or even to co-exist in a single system. For 8-bit data transfers the 16 data lines are grouped into two uni-directional 8-bit buses, the Data In Bus and the Data Out Bus. For 16-bit data transfers, the two uni-directional buses are ganged to form a single 16-bit bi-directional data path.

An additional status line has been assigned to control the grouping of the data lines, called Sixteen Request (sSXTRQ). This line is asserted when the proccessor requests a 16-bit data transfer on the bus. 8-bit processors do not generate this line, and hence the data transfer proceeds in byte mode.

**Memory Organization**

To be capable of both 8-bit and 16-bit parallel transfers memory is organized as two banks of 8-bit memory, one bank for the most-significant-byte of the 16-bit word, and one bank for the least-significant-byte. These banks may be activated either together or separately, depending on the condition of the sixteen request status line. This basic memory organization is shown in figure 2.

Memory in S-100 systems is always addressed as bytes. And since a word is composed of two bytes, the least significant address bit, AO, is not considered in address decoding for word (16-bit) references. For byte references however, the AO bit selects either the most significant byte or the least significant byte within the addressed word. See figure 3.

**Word Transfers**

For word, or 16-bit, data transfers the processor asserts the word memory address on address lines A1-A23 (A15 for short address systems), and the Sixteen Request line.

If the Sixteen Request line is not asserted, the memory reference is conducted as a single byte transfer. The processor asserts the memory word address on address lines A1-A23, and selects the proper byte within the word by asserting the AO line.

According to the IEEE specification, if AO is False (electrically low) the most significant byte within an addressed word is selected; if AO is true, the least significant byte is selected.

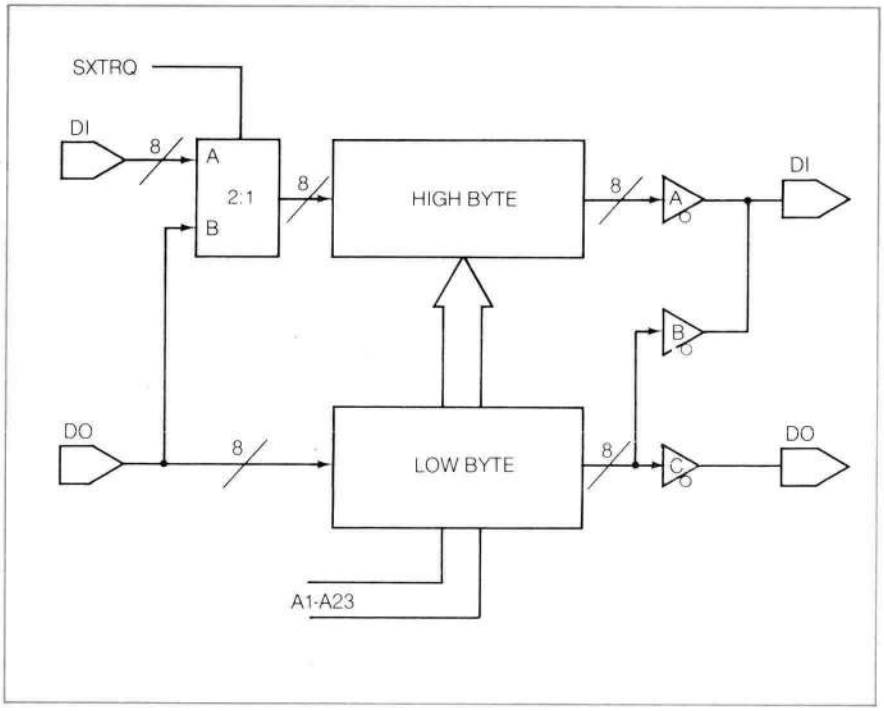
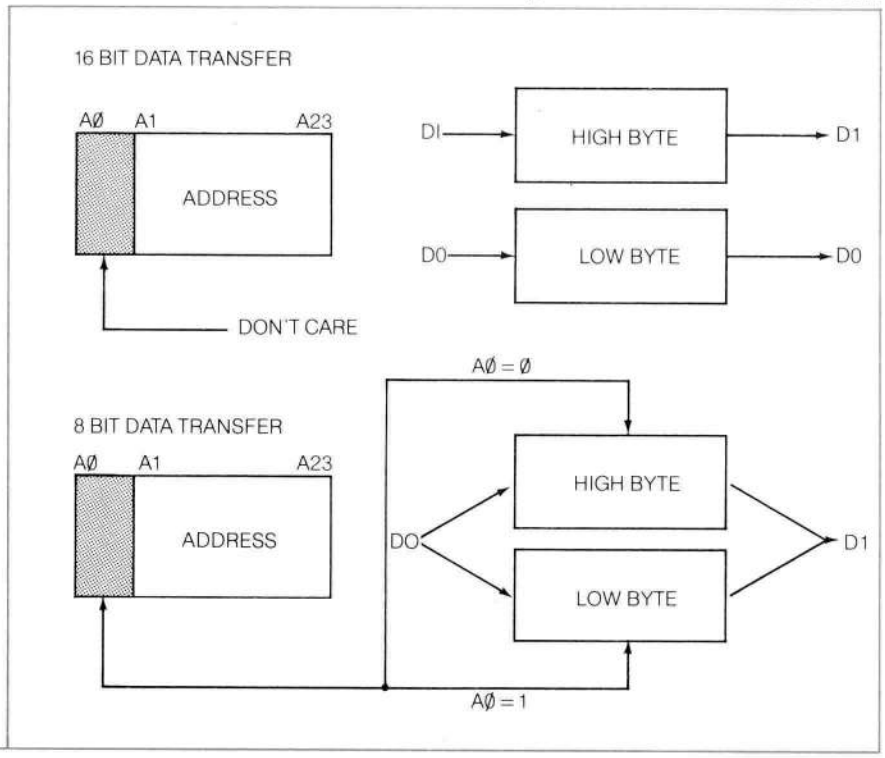
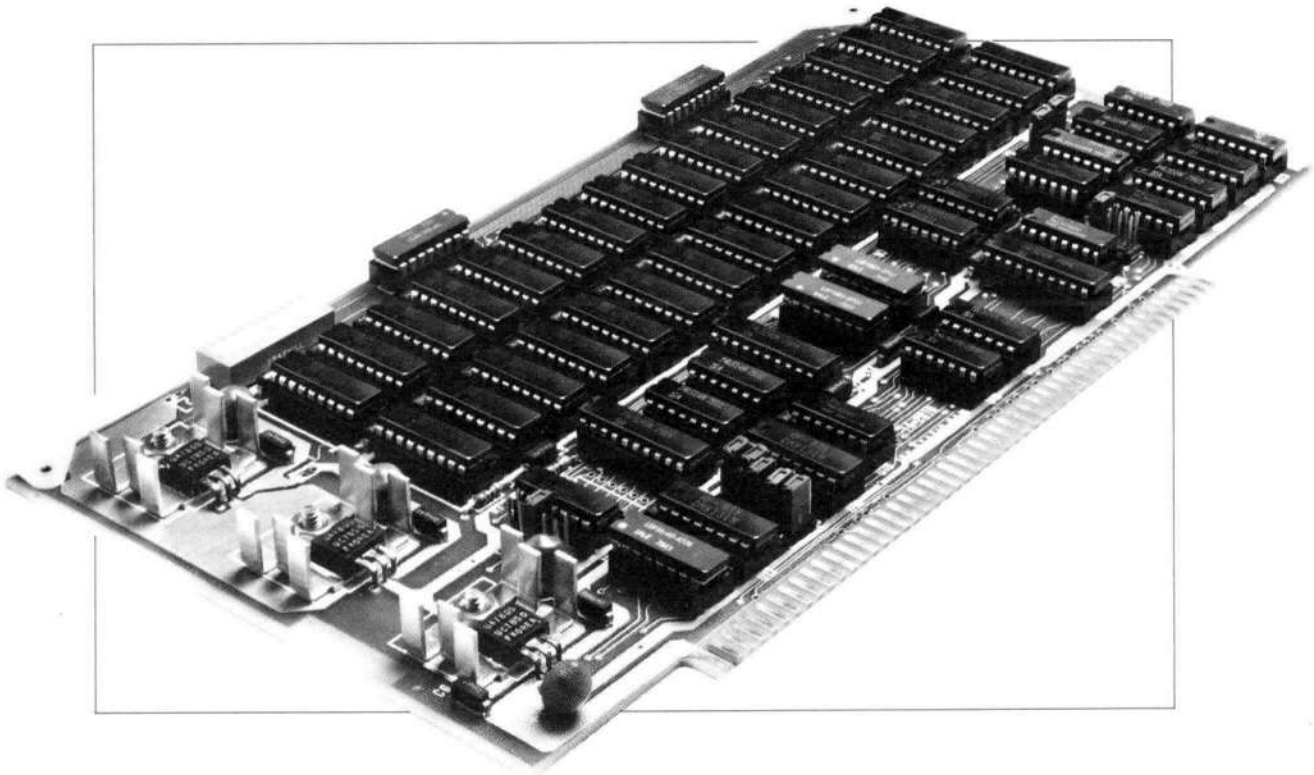



*Figure 2. 8/16 Bit Memory Organization.*

*Figure 3. 8/16 Bit Address and Data Usage.*



# 16 KSR 16K Static RAM



Available in either high speed 250 ns (4MHz) or lower cost 450 ns (2MHz) speed, the 16KSR can take advantage of the new ultra-low-power edge-triggered RAMs. Pin-compatible with the industry standard 4044 RAM, these parts offer the advantage of ultra-low power—resulting in one of the lowest-power 16K boards available.

No more expensive than most competing non-IEEE RAM boards, the 16KSR includes all the features of our Series II line—24 address lines for memory expansion to 16 megabytes, 8/16 data bits for full upward compatibility with 16-bit processors, selectable wait states and, of course, full buffering.

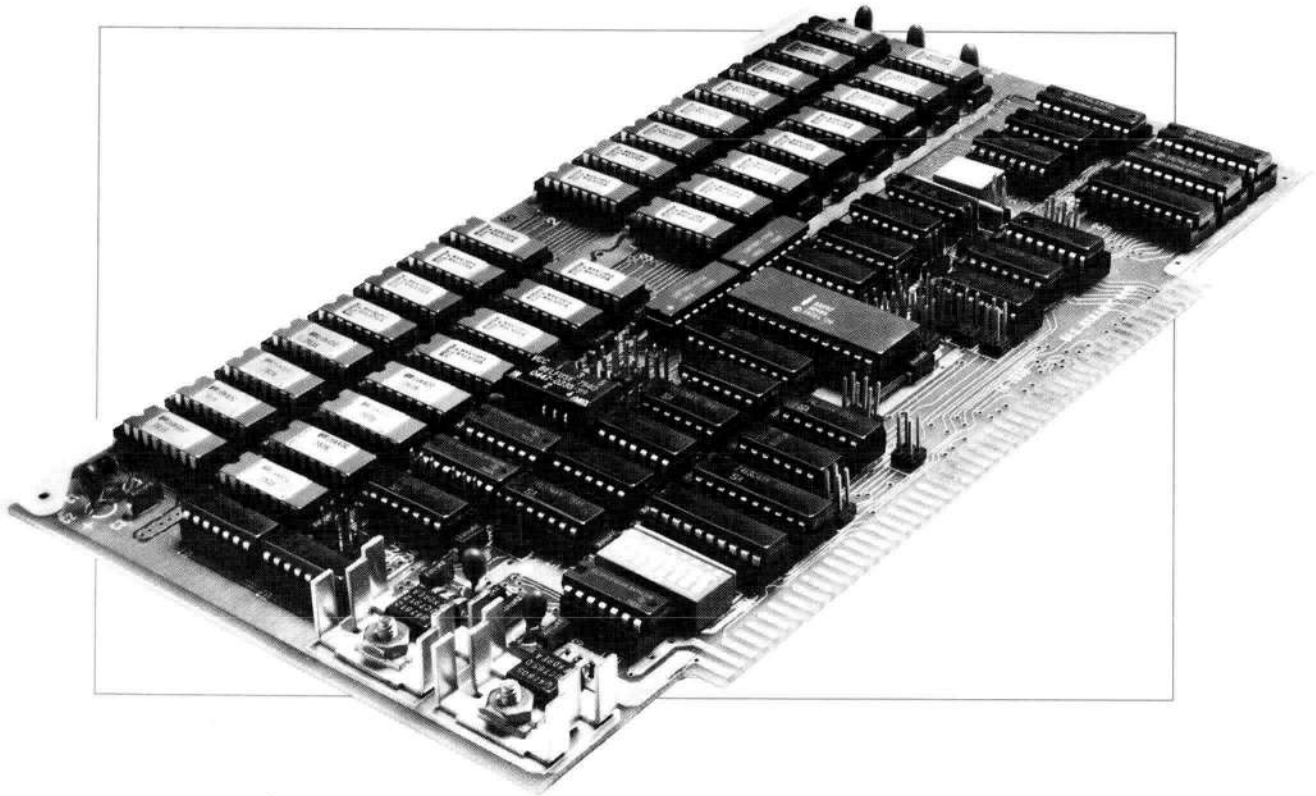
## Features/Specifications

| | |
|---|---|
| Access Time | 250 ns Model 16KSR-4<br>450 ns Model 16KSR-2 |
| Addressing | 16 or 24 address bits<br>DIP switch selectable |
| Data | 8 or 16 bit automatic |
| Buffering | Full IEEE Standard |
| Wait States | 0, 1, 2 or 3 jumper selectable |

**Model No. . . . . 16KSR-4**
**Order Part No. . . . . 860-2010**

**Model No. . . . . 16KSR-2**
**Order Part No. . . . . 814-2010**

# 64KDR 64K Dynamic RAM



This new 64 kilobyte RAM card is simply the most advanced S-100 memory card available. Organized as four blocks of 16K, this is *the only dynamic RAM board that can claim full IEEE S-100 compatibility* including:

- 24 address lines
- 8/16 bit data operation
- front panel compatibility
- arbitrated refresh for full unlimited DMA
- 4MHz operation

This Series II RAM extends our tradition of *true* obsolescence insurance to include upward compatibility with any S-100 CPU, including our soon-to-be-released advanced MPU/8000™ 16-bit processor.

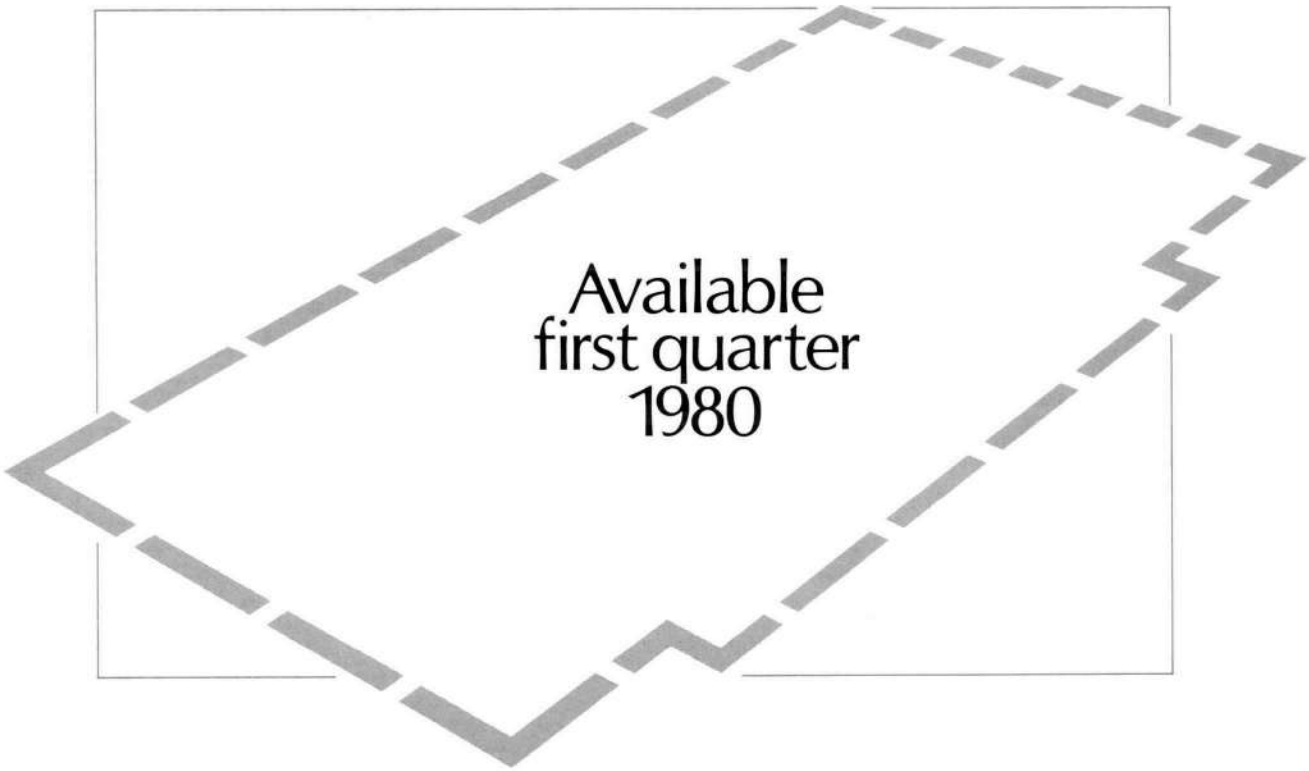
Incredibly reliable, the 64KDR looks to the user exactly like a static RAM module. Other designs limit DMA operations to short bursts—or forbid them entirely—but not the model 64KDR. Our proprietary refresh arbitration design permits unlimited DMA and full front-panel operation. The first dynamic RAM board as reliable as a static, this sophisticated board represents the best memory value available today.

## Features/Specifications

| | |
|---|---|
| Access Time | 250 ns Model 64KDR-4 |
| Addressing | 16 or 24 address bits<br>DIP switch selectable |
| Data | 8 or 16 bit automatic |
| Buffering | Full IEEE Standard |
| Wait States | 0, 1, 2 or 3 jumper selectable |

**Model No.** . . . . . **64KDR**
**Order Part No.** . . . . . **816-2030**

# FDC-2 Double-Density DMA Disk Controller




Double-Density MFM recording and Direct Memory Access team up in the FDC-2 to store twice as much data (to 1 megabyte/disk), at twice the transfer rate (250K bytes/sec), while requiring only 6% of the processor overhead of earlier designs. Because data is moved quickly with almost no processor interaction, system throughput dramatically increases, and therefore more processing power is available to the user.

While all disk controllers claim a data rate of 256K bytes/sec., few controllers can exploit it *fully*. Because the FDC-2 requires less processor overhead, it can transfer a full 2 cylinders with a single command—almost 40K bytes in just a second. In fact, the FDC-2 is itself a processor—microprogrammed to execute all the complex disk operations.

The FDC-2 is compatible with both single- and double-density IBM formats, and includes a dual-level PLL data separator for ultra-reliable decoding, and software-programmable single/double-density operation.

Up to four 5¼" minifloppy or 8" floppies, single- or double-sided, can be accommodated.

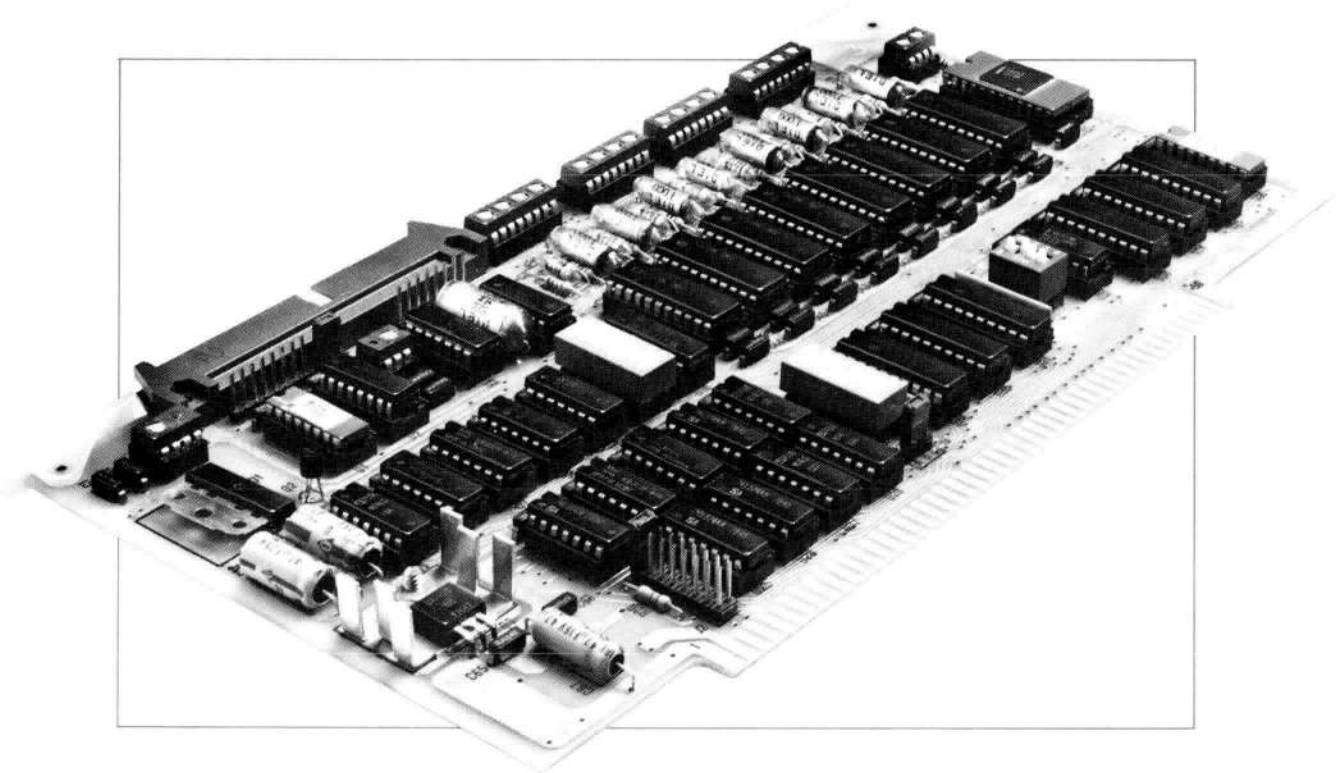
A special head-load circuit is included for extended media life, and a power-down write current switch inhibits power-down transients that could endanger data. A bootstrap monitor is included in a 1K 2708 PROM.

### Features/Specifications

| | |
|---|---|
| Transfer Rate | 39,936 bytes/sec |
| Data Rate | 125K/sec single density<br>256/K sec double density |
| # drives | 4 single or double sided;<br>5¼" or 8" |
| Transfer method | DMA<br>24 address lines (full 16 megabyte range)<br>8 data bits |
| Connector | Shugart SA800 or equivalent |
| Recording format | 3740 FM or 3740 MFM |
| Total bytes/disk | 315K single density<br>630K double density |
| Data bytes/disk | 256K single density<br>512K double density |
| Onboard PROM | 2708 1K PROM |

**Model No.** . . . . . **FDC-2**
**Order Part No.** . . . . . **815-2020**

# ADDA Analog-To-Digital/Digital-To-Analog Converter



The ADDA converter board permits the digital computer to have direct access to, and control over, analog signals. Analog inputs are digitized for processing by the computer using a high-speed 10-bit monolithic Analog-to-Digital (A/D) converter with an accuracy of better than .025%. Digital data from the computer is converted to analog voltages by monolithic Digital-to-Analog (D/A) converters.

This board frees the user from the laborious task of manually entering data. Applications include digitizing graphs, reading settings on potentiometers and other rotary controls, driving pen-plotters, taking data directly from instrumentation, etc.

The ADDA board will convert up to eight channels of single-ended analog data in polled or interrupt-driven modes at rates up to 30KHz (30,000 samples per second). The user has complete control over how many and which channels are being digitized through the on-board control register. The user may instruct the A/D to take a sample on the existing channel, or take a sample on a new channel. In addition, the user may set a real-time clock (RTC) to automatically take samples regularly—at a specified frequency as well as performing a number of other programmable functions.

The ADDA board contains eight independent latched D/As, eliminating refreshing. Settling time is 5$\mu$s for an output rate of 200kHz. An auxiliary digital output is available which operates as a square-wave generator that is user-programmable in frequency.

## An important word about "accuracy"

Many manufacturers specify accuracy in terms of the converter they employ, rather than the more honest *board-level* accuracy, which includes all the errors inherent in the system, e.g., multiplexer noise, sample-and-hold jitter and droop, and quantization error. All Intersystems products specify *board-level* error; in fact, the ADDA actually employs a 10-bit converter, leaving 2 guard bits, to assure all specifications are met, even over the full temperature range.

## Specifications

**A/D Section**

| | |
|---|---|
| Channels | Eight single-ended multiplexed |
| Conversion time | 25$\mu$s typical<br>30$\mu$sec maximum |
| A/D accuracy | 10 bits (8+2 guard bits) |

**D/A Section**

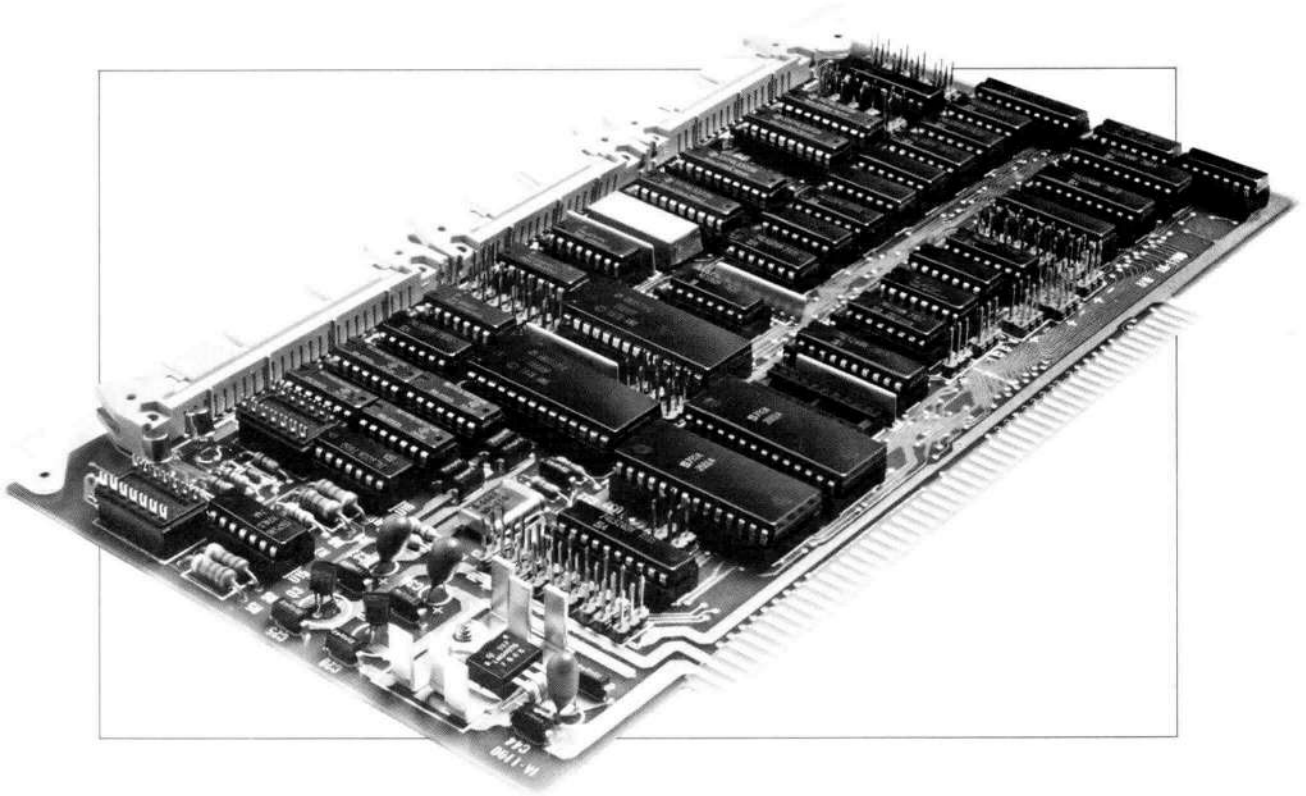
| | |
|---|---|
| Channels | Eight single-ended independent |
| Settling time | 5$\mu$s |
| Accuracy | 8 bits |
| Real time clock (RTC) | 32 bits, plus Clock Out line for optional square-wave output |

**Interrupt Modes**

| | |
|---|---|
| Mode 1 | Interrupt when A/D finishes conversion |
| Mode 2 | Interrupt when RTC times out |

**Model No.** . . . . . **ADDA**
**Order Part No.** . . . . . **810-1170**

# VIO Input/Output Interface



VIO is a multipurpose communications interface that is both easy to program and incredibly flexible. It includes enough buffered, protected ports to support all but the most I/O intensive systems. And, because the board's architecture has been carefully thought out, VIO incorporates a number of extra features, as well as great flexibility.

The VIO provides two fully implemented serial ports, individually selectable for RS 232 or current loop operation, and programmable from 50 to 19,200 baud. Both the widely-accepted asynchronous and the more specialized high-speed synchronous modes are supported, including both byte- and bit-level standard protocols.

Buffered, latched parallel ports, two in and two out, include handshaking, both a strobe and ready line, for ease of interfacing. Plus a VIO exclusive—8 bit-addressable control lines—each selectable as an input or output. No longer will it be necessary to slice up a port to provide a single control bit! All status and error lines may be either polled or, for real-time applications, assigned to any one of sixteen on-board interrupt priorities, with its corresponding unique restart address. Ports are conveniently mass-terminated, for easy hook-up.

## Specifications

**Serial I/O Ports**

| | |
|---|---|
| I/O Ports | Two |
| Baud rates | Independently-software-selectable 50 to 19,200 baud |
| RS232/current loop | Jumper-selectable |

**Parallel I/O Ports**

With strobe and acknowledge lines; both with jumper-selectable polarity

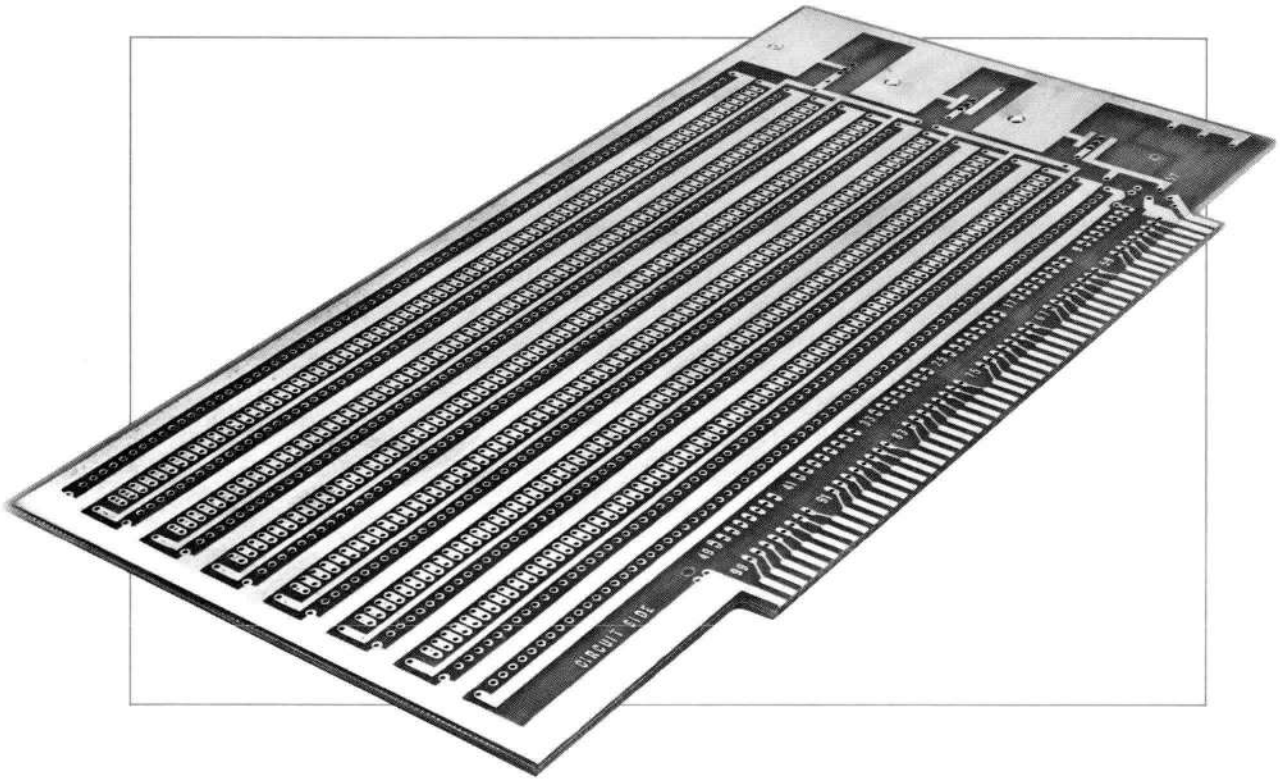
| | |
|---|---|
| Output ports | Two |
| Input ports | Two |
| Control ports | 8- Independently-selectable |

**Interrupts**

| | |
|---|---|
| Number of interrupt priorities | 16 |
| Number of interrupt responses | 16 |
| Addressing | 8-bit I/O or 16-bit memory mapping |

| **Model No.** | **VIO-Ø** | **VIO-1** |
|---|---|---|
| | **W/O Interrupt** | **W/ Interrupt** |
| **Order Part No.** | **811-1190** | **850-1190** |

# Prototype Board



## Introduction

From building up a simple experiment to testing complex circuitry, the Intersystems Prototype Board offers you a reliable, faster, more efficient way of developing your own designs:

- Capacity: 70 14-pin sockets
- Accepts any size socket: 8, 14, 16, 18, 20, 22, 24, 28, 40, 64 pin
- Six wire-wrap positions provide easy access to the edge connector
- Optional split power rail
- Selectable voltage regulators
- Fully bused ground plane

**Description**

Horizontal IC rows accept any size IC sockets and maximize usable space for convenient wire-wrapping. Easy access to the S-100 bus is achieved through wire-wrap socket locations connected directly to the edge connector. Three voltage regulator positions are furnished: one regulator provides +5 volts, the remaining two are available for your special voltage requirements. The optional on-board split power rail gives you the flexibility to separately bus up to two of these voltages, eliminating circuit noise commonly associated with conventional voltage distribution.

Developed by our Engineering Group for their own S-100 development work, we now make this quality board available to you. Manufactured from top grade epoxy glass with full plated-through holes and gold plated edge connectors the board will meet your most demanding wire-wrapping requirements.

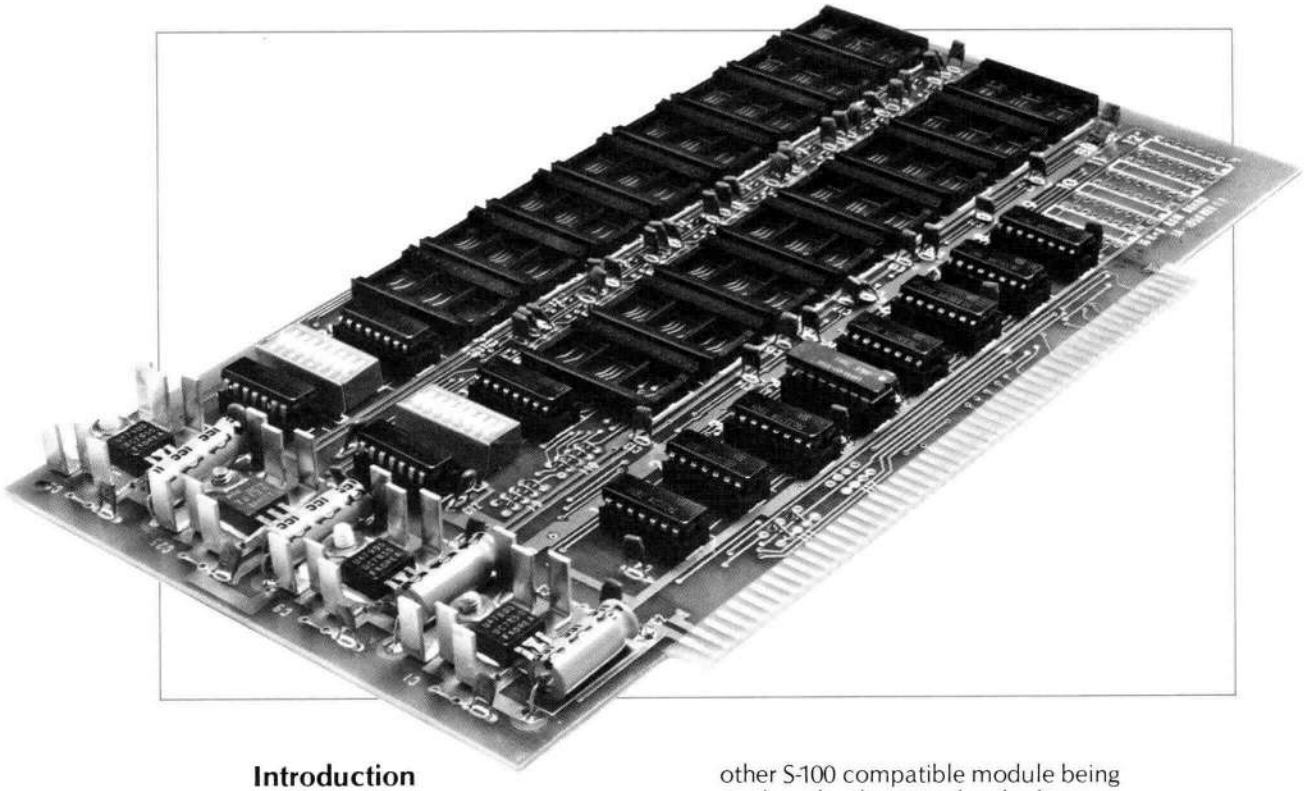
**Model No.** . . . . . **WW-1**
**Order Part No.** . . . . . **702-1030**

# SECTION III: SERIES I BOARDS

While not completely IEEE S-100, Series I boards are all upward-compatible with our Series II line. Because of their low cost, they are well-suited to applications which don't require full 24-bit addressing and 8-/16-bit operation.

At present, Intersystems has well over 15,000 Series I boards in the field, proof of the performance, versatility and value they offer.

## 2708/2716 EPROM Board



### Introduction

The Intersystems 2708/2716 EPROM Board is a low-cost, versatile microcomputer memory module. Designed to utilize EPROM memory chips, the module is indispensable for permanent storage of dedicated programs in a controller. It is also an inexpensive method for storing often-used software in more general system applications.

- Accepts up to 16 of either 2708 or 2716 EPROMS or compatible ROMS
- Addressable to any 16K boundary: EPROMS addressable by DIP switch to any 1K (2K with 2716) location
- Only EPROMS installed need be enabled. Unused locations may be allocated for RAM
- Selectable wait states: 0, 1, 2, 3 or 4
- All S-100 lines fully buffered

### Description

The 2708/2716 EPROM Board provides up to 32K of READ ONLY MEMORY storage, more than any other S-100 compatible module being marketed today. It is also the first to accept either the 2708 1K *or* 2716 2K EPROMS.

Each chip on the board is individually controlled by a DIP switch in order that memory space is never allocated to unused ROM. Up to 4 wait states are provided to allow use with the Intersystems 4MHz Z-80 Central Processor or to take advantage of the low cost slower chips.

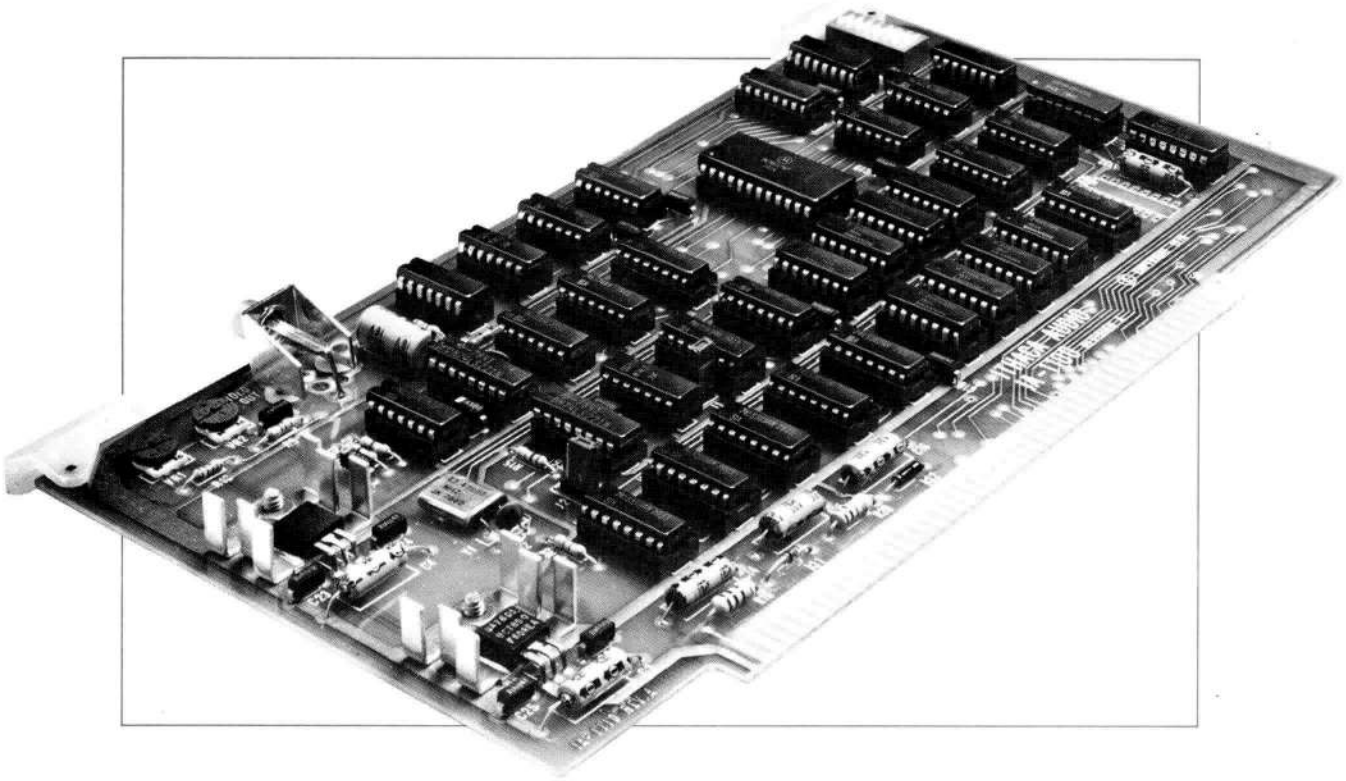
### Specifications

Capacity: 16K bytes (32 K bytes using 2716's)

Power Requirements:
(fully loaded)
+8 volts @ 320mA
+16 volts @ 750mA
−16 volts @ 500mA

**Model No.** . . . . . **2708/16**
**Order Part No.** . . . . . **803-1050**

# Video Display Board



## Introduction

At Intersystems, design and reliability are synonymous. Our Display Board is no exception, engineered to the most conservative S-100 timing and DC specifications to insure full compatibility with your S-100 system:

- 16 lines of 64 characters each
- Full upper/lower case ASCII character set, numbers, symbols, and Greek letters
- Characters are composed of 7 x 9 dot matrix in an 8 x 10 field
- Selectable display modes, normal or reverse video, blinking cursor.
- Memory addressable to any 1K page
- Software driver simulates TTY, provides full cursor control (up, down, forward, back, home and flashing), scrolling and paging
- Compatible with CP/M or Intersystems' K3 Operating System
- All S-100 lines fully buffered

## Description

The easy-to-read, 16-line by 64-character format can be displayed on an inexpensive video monitor or a modified TV set. This moderately dense display enables you to expand your computer to include a full terminal at a minimal cost.

Ultra high-speed operation is provided by a 1024 byte buffered memory. Each memory location corresponds to a unique location on the screen making it possible to update any character in the display instantaneously.

The large versatile character font includes all 128 upper/lower case ASCII characters, numbers, and special symbols. The typeface consists of a 7 x 9 dot matrix displayed in either normal or reverse video for easy character recognition and screen legibility.

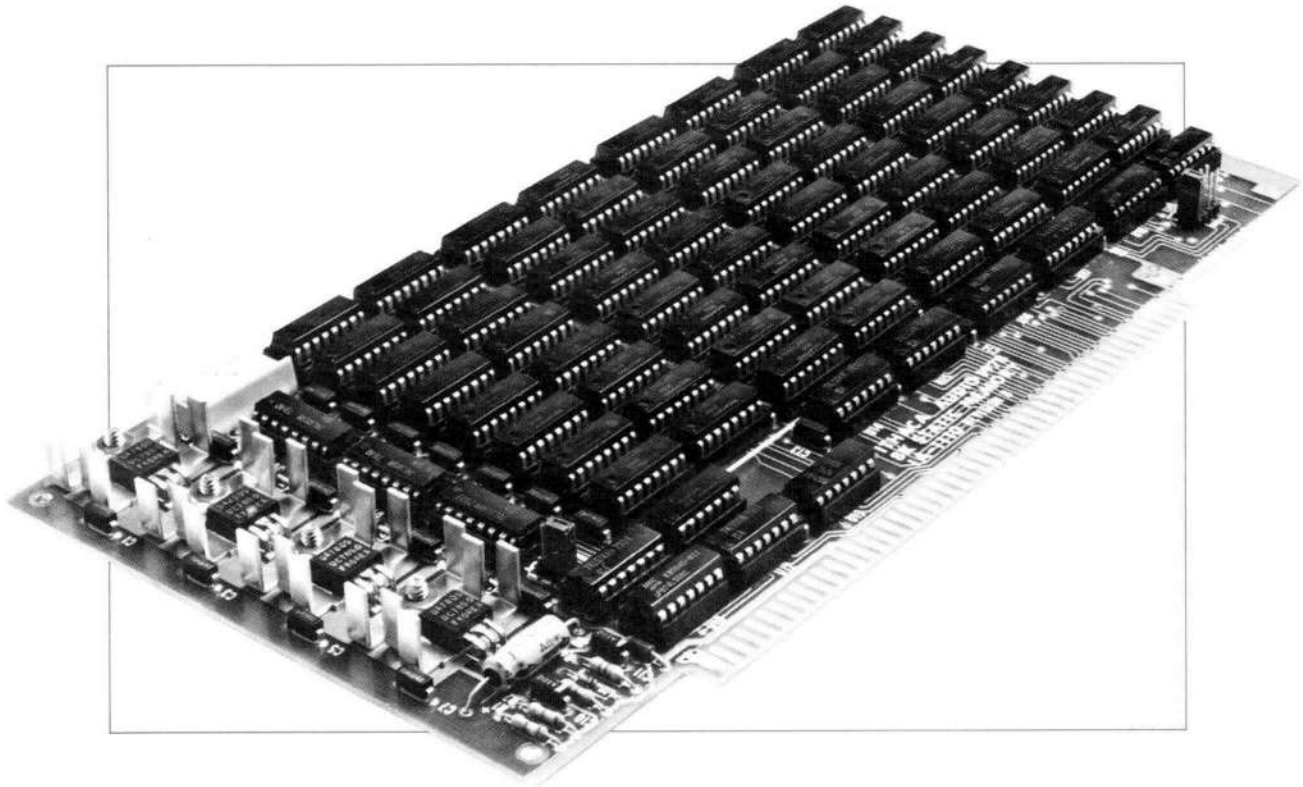
Combine these features with the supplied software driver and you have a versatile operator console complete with programmable cursors, scrolling and paging functions. Additional capabilities range from controlling multiple remote displays to data manipulation and complex text editing.

## Specifications

Display Memory: 8 low power 2102 static RAMs
Refresh: 50 or 60Hz, jumper-selectables
Output: EIA Standard video
Power Requirements:
+8 volts @ 950mA
+16 volts @ 55mA
−16 volts @ 150mA

**Model No. . . . . VIDEO BOARD**
**Order Part No. . . . . 804-1100**

# 8K Static RAM Memory Board



## Introduction

The Intersystems 8K Static RAM Board is a high speed, fully buffered 8K Random Access Memory module designed to use 2102 type memory.

- Memory protect/unprotect
- Power-on-clear
- Selectable 0, 1, 2, 3 wait states
- 8192 8 bit words
- Addressing: Two independent 4K halves selectable by DIP switch
- Fully buffered address, control and data lines

## Description

Featuring fully buffered address, control and data lines, the 8K Static RAM Board minimizes bus loading and protects the memory chips. DIP switch controlled addressing provides selection of two independent 4K pages. Memory protect/unprotect is software controlled and is initialized by power-on-clear. Provision for up to 3 wait states permits the user to take advantage of slower-running memory if desired.

## Specifications

Capacity: 8192 bytes (64 2102 type 1K x 1 Static RAMs).

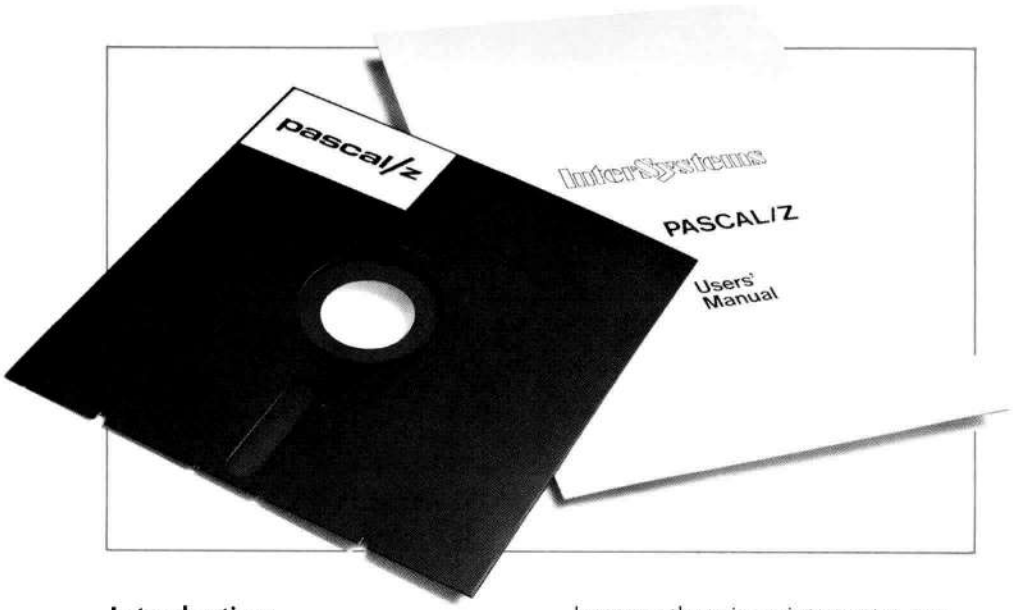
Power Requirements:
+8 volts @ 1.4 Amps with 2102L1PC or 2102LHPC

**Model No. . . . . 8KSR-4**
**Order Part No. . . . . 855-1110**

**Model No. . . . . 8KSR-2**
**Order Part No. . . . . 805-1110**

# SOFTWARE

## PASCAL/Z




### Introduction

Created by Nicholas Wirth in 1971, Pascal was designed as a model for high level teaching languages. Good programming techniques are encouraged by a structure which essentially rules out reckless GOTOs and insists upon the use of efficient top down coding techniques. Easy to learn, Pascal is also flexible enough to be well-suited for any educational, scientific or business application. In fact, most computer research employs Pascal, and it is certain to be the prime media for research into future advanced software systems.

### Description

Pascal/Z is a highly optimized native code compiler. Unlike a pseudo-code (P-code) compiler, Pascal/Z does not require a special intermediate language or run time interpreter; instead the compiler generates Z80 macro-assembly code directly. Eliminating this extra step results in object code that is not only very compact but extremely fast. Execution speed averages better than five times that of identical code run under P-code implementations, and because there is no interpreter, run time modules may be as small as 2K.

All programs compiled under Pascal/Z generate code which is both ROMable and Re-entrant, absolutely essential to any advanced multi-tasking operating system. Furthermore, Pascal/Z has been heavily optimized for execution speed by recognizing and exploiting commonly encountered special cases. Arithmetic operations such as multiplication by 1, 2, 4 or 8 or Boolean operations such as A + O or Ax1 are automatically detected and specially handled for greatest speed. In addition, calculations such as evaluation of operations upon constants, including range checking of array subscripts, are done during compile rather than execution time. This fact alone can result in peak speeds 40 times greater than competing compilers during many common kinds of array number crunching.

As problems become more complex, programs grow larger and it becomes imperative that compilers provide debug facilities to assist the programmer in verifying his code. Pascal/Z provides 3 such features: the IMBED, TRACE and ERROR options.

IMBED permits us to create an assembly listing from the Pascal program with each Pascal statement imbedded as a comment. This unique feature means, for the first time a programmer is actually able to view the assembly language expansion of each Pascal statement alongside the source itself. Since research indicates that in many programs 15% of the code is executed 80% of the time, programmers can quickly spot their mistakes and bottlenecks and correct them. Only Intersystems Pascal/Z permits systems analysts to view their code in this way.

TRACE is usually invoked along with IMBED. When enabled, the compiler prints out the statement numbers as they are encountered during execution. Using this along with the expanded listing, program flow can easily be followed and common routing errors detected.

Other options that may be selected by the user include error checking for all multiply and divide operations, range and index checking, stack overflow flag, and control/C checking.

This last feature bears some further explanation. Used to stop program execution from the console, control/C checking is totally under program command. A programmer has complete control over when a user is permitted to prematurely terminate a program's operation. This is vital to the correct operation of a polled operating system.

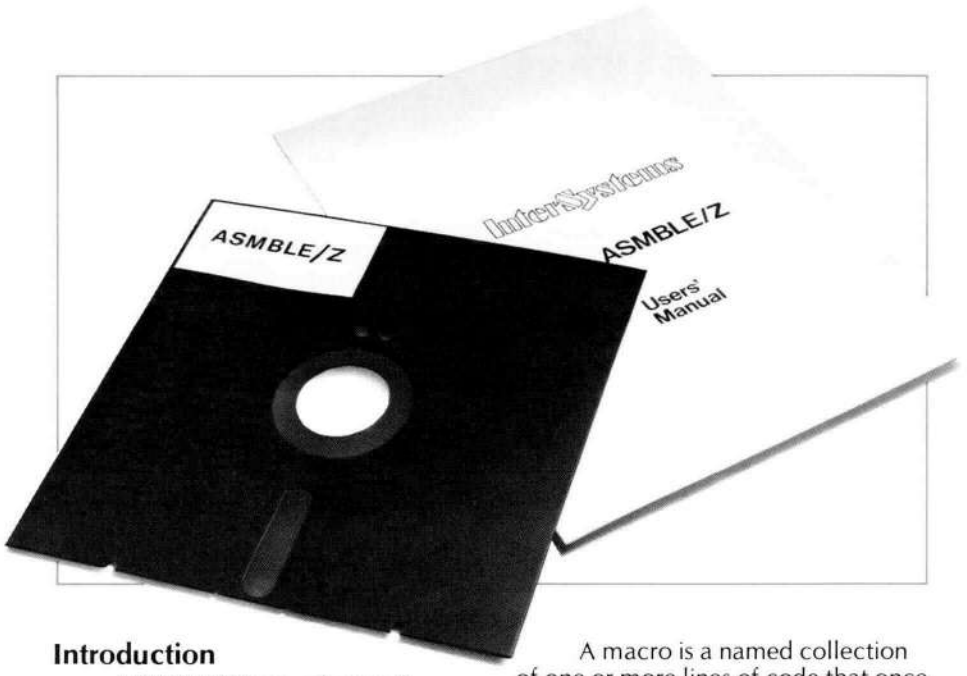
Pascal/Z closely follows the Pascal Users Manual and Report. The temptation to add nonstandard functions or other extensions that would lull the programmer into creating code that might not be transportable or impair the goal of machine independent code has been resisted. The only additions are options to call external routines, to print the symbolic value of enumeratic types and an ELSE clause to the case statement.

Distributed on a standard CP/M disk, Pascal/Z includes the compiler and ASMBLE/Z macroassembler in object and the library file in both commented source and object form. All the routines necessary to customize Pascal/Z to an operating system other than CP/M are well commented and documented. Support includes updates for one year upon return of the original Pascal disk.

**Model No.** . . . . . **Pascal/Z**
**Order Part No.** . . . . . **620-0300**

# SOFTWARE

## ASMBLE/Z




### Introduction

ASMBLE/Z is an advanced source code macroassembler that permits the user a host of programing conveniences while still maintaining a close correspondence to the actual machine language of the computer. ASMBLE/Z may be used directly by the user or in conjunction with other Intersystems software such as Pascal/Z to create extremely compact high speed Z80 programs.

### Description

ASMBLE/Z is an enhanced version of ASMBLE, the standard assembler supplied with Intersystems operating systems. ASMBLE/Z produces either an absolute binary or hex code listing. Devices and file names for the input and output files to be generated may be specified. If a listing is specified the symbol table will be alphabetized.

In addition to the standard features of ASMBLE;—labels, symbolic program counter, conditional assembly and unique relative jump format—ASMBLE/Z includes a powerful macro structure.

A macro is a named collection of one or more lines of code that once defined, may be inserted into a program one or more times simply by typing the macro's name in place of an instruction. Both dummy and real arguments may be used, and dummy arguments are then replaced with the proper real argument when the macro is later called. Macro definitions may contain another macro definition, to create larger more complex structures and finally, a macro may contain a call to another macro up to 16 nesting levels.

Conditional assembly supports both the IT and ELSE statements up to 255 nesting levels.

ASMBLE/Z requires 10K and a standard CP/M operating system.

**Model No.** . . . . . **ASMBLE/Z**
**Order Part No.** . . . . . **606-0106**

**DOMESTIC -- QUANTITY ONE**

**12 - 15 - 79**

| ORDER NO | DESCRIPTION -- MODEL NO. | PRICE |
|---|---|---|
| | **MICROCOMPUTERS -- MAINFRAMES** | |
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| | **OPTION** | |
| 813 - 2000A | Monitor Prom for Z80 Model no. M-BUG | 25 |
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| 860 - 2010 | 16K Static RAM Board; 250ns Access Time low power Model no. 16KSR-2 | 495 |
| 814 - 2010 | Same as above only 450ns Access time Model no. 16KSR-4 | 475 |
| | **I/O SERIES II** | |
| 811 - 1190 | 4 Parallel, 2 Serial I/O Board; without interrupts Model no. VIO-Ø | 295 |
| 850 - 1190 | Same as above with interrupts Model no. VIO-1 | 395 |
| | **OPTION** | |
| | Order 1 cable A and 2 cable B's | |
| 810 - 1170 | 8 Bit Analog to Digital and Digital to Analog Board; Model no. ADDA | 495 |
| | **OPTION** | |
| | Order 1 cable A | |

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