InterSystems Sixty-Four Kilobyte Dynamic Memory

for the S-100 Bus

Manual Revision 0

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Congratulations!

You have chosen one of InterSystems new Series II memory boards, the most flexible and reliable memory units for the S-100 bus.

As with all InterSystems Series II products, these memory units have been designed to take advantage of all the extensions and specifications of the new IEEE S-100 bus specification, and yet remain compatible with the majority of pre-standard S-100 boards.

This owner's manual has been prepared to acquaint you with your memory unit and to serve as an aid in achieving its optimum use. In Section 1, the general design and features of the unit are discussed. In Section 2, specific instructions are given for the configuration of the board in your system. Section 3 contains technical reference information, and the last sections contain the parts list and schematic.

If you have any problems with the memory unit in your system, give us a call at (607) 257-0190; our technical support personnel will be glad to assist you.

Section 1

Introduction and General Information

1.1 Features

1.2 Service Information

- Receiving Inspection
- Warranty Information
- Replacement Parts
- Factory Service
- Contacting InterSystems

1.3 Data Transfer on the S-100 Bus

- Memory Organization
- Word Transfers
- Byte Transfers

1.1 Features

The InterSystems 64K Dynamic RAM board is the first S-100 dynamic memory board to take full advantage of the recent IEEE specification. Its features include:

* Byte or Word Data Transfer. Whether you're using an 8 bit processor or one of the new 16 bit processors, the board's data bus automatically adjusts to the requested word width. You can even run a 16 bit processor and an 8 bit Direct Memory Access Controller concurrently in the same bus.

* Standard or Extended Addressing. The memory board may be addressed in either the standard 16 bit address space (64K), or in the extended 24 bit address space (16 megabytes).

* Onboard arbitration and sequencing logic. This circuitry allows continuous DMA transfers of any size and error-free operation during waits, halts, or resets.

* High Speed Operation. The board may be configured for either 2 mHz or 4 mHz operation without wait states. All timing is completely IEEE S-100.

* Precise delay line timing. There are no one shots, oscillators, or RC delays.

* Uses both transparent and default refresh.

* Compatible with front panels.

* Designed to use either 4115 or 4116 type memory chips.

* Phantom and Error. These new S-100 lines assist in bootstrapping and memory protection.

* Low Power/Low Heat Design. Low power not only means less drain on the system power supply, but higher reliability and longer chip life as well.

* Damped Array. All lines driving the memory array include small series damping resistors, reducing array noise and improving reliability.

* Wait State Generator. One wait state may optionally be generated on the board for M1 or any board access.

1.2 Service Information

Receiving Inspection

When your InterSystems Memory Module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We advise that you save the shipping container for use in returning the module to InterSystems, should it become necessary to do so.)

Any apparent damage should be reported to InterSystems at once. Please write us describing the problem so that we can take appropriate action.

Warranty Information

In brief, your assembled and tested InterSystems Memory Module, and all parts supplied, are warranted against defects in materials and workmanship for a period of 1 year from the date of purchase. Refer to Appendix I for the complete Statement of Warranty.

Replacement Parts

If you find a bad component on your Memory Module, a memory chip for example, return it to us with a letter. We will replace it and return it with a "no charge" invoice if the unit is under warranty. Out-of-warranty parts prices may be confirmed by telephone.

Factory Service

InterSystems provides a factory repair service for all of its products. Before returning the module to InterSystems, first obtain a Return Authorization Number from our Technical Service Dept. This may be done by calling us, sending us a TWX, or by writing to us. After the return has been authorized, proceed as follows:

1) Write a letter describing the problem.

2) Describe your system to us, list boards by manufacturer and name.

3) Include Xerox copies of the schematics of boards by manufacturers other than InterSystems.

4) Include the Return Authorization Number.

5) Pack the above information in a container suitable to the method of shipment.

6) Ship prepaid to InterSystems.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

Contacting InterSystems:

The following apply for both correspondence and service.

Ithaca InterSystems Inc.
1650 Hanshaw Rd.
P.O. Box 91
Ithaca N.Y. U.S.A.
14850

Telephone (607) 257-0190
TWX 510 255-4346

In Europe:

Ithaca InterSystems Ltd.
58 Crouch Hall Rd
London N8 8HG. U.K.

Telephone 01-341-2447
Telex 299568

1.3 Data Transfer on the S-100 Bus

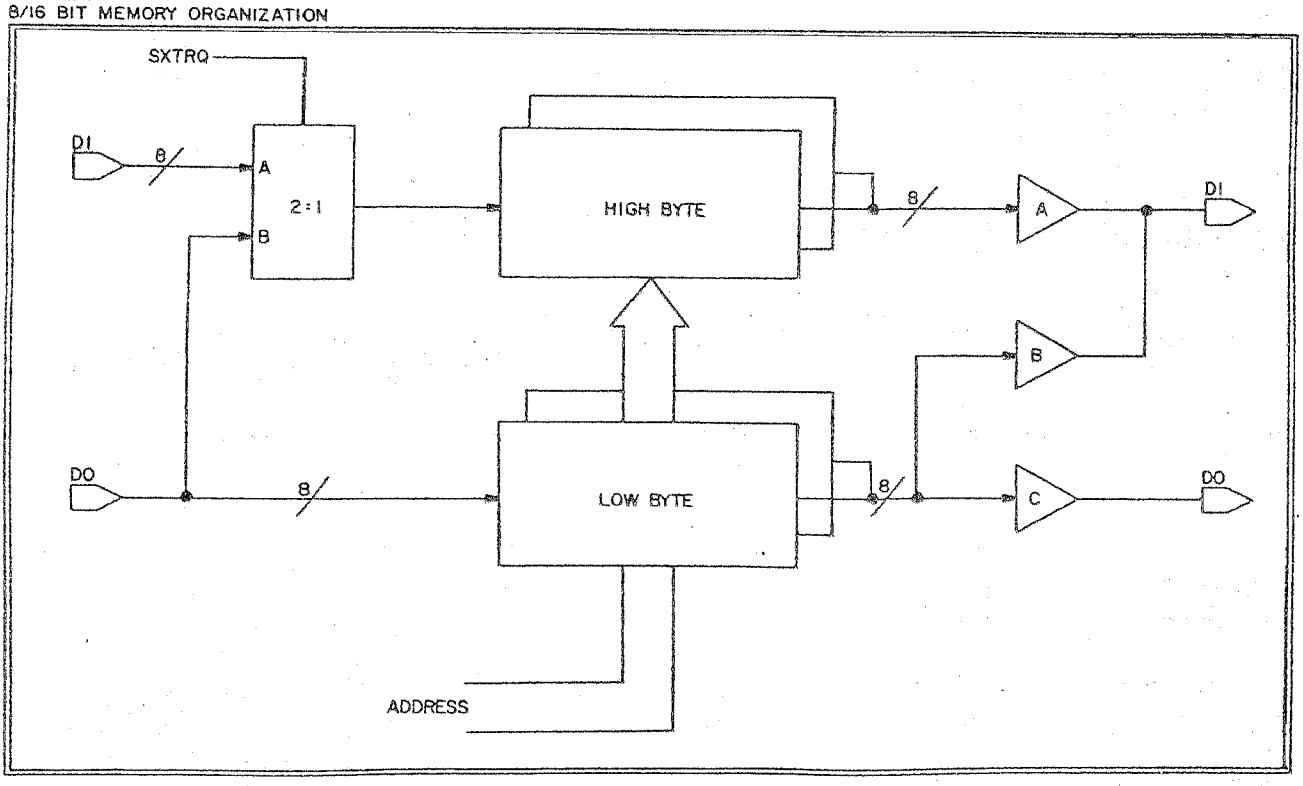
The S-100 data bus supports both byte-parallel (8 bit) and word-parallel (16 bit) data transfers, hence allowing both 8 bit and 16 bit processors to use the same memory boards, or even to co-exist in a single system. For 8 bit data transfers the 16 data lines are grouped into two uni-directional 8 bit busses, the Data In Bus and the Data Out Bus. For 16 bit data transfers, the two uni-directional busses are ganged to form a single 16 bit bi-directional data path.

An additional status line has been assigned to control the grouping of the data lines, called Sixteen Request (sSXTRQ). This line is asserted when the processor requests a 16 bit data transfer on the bus. Eight bit processors do not generate this line, and hence the data transfer proceeds in byte mode.

Memory Organization

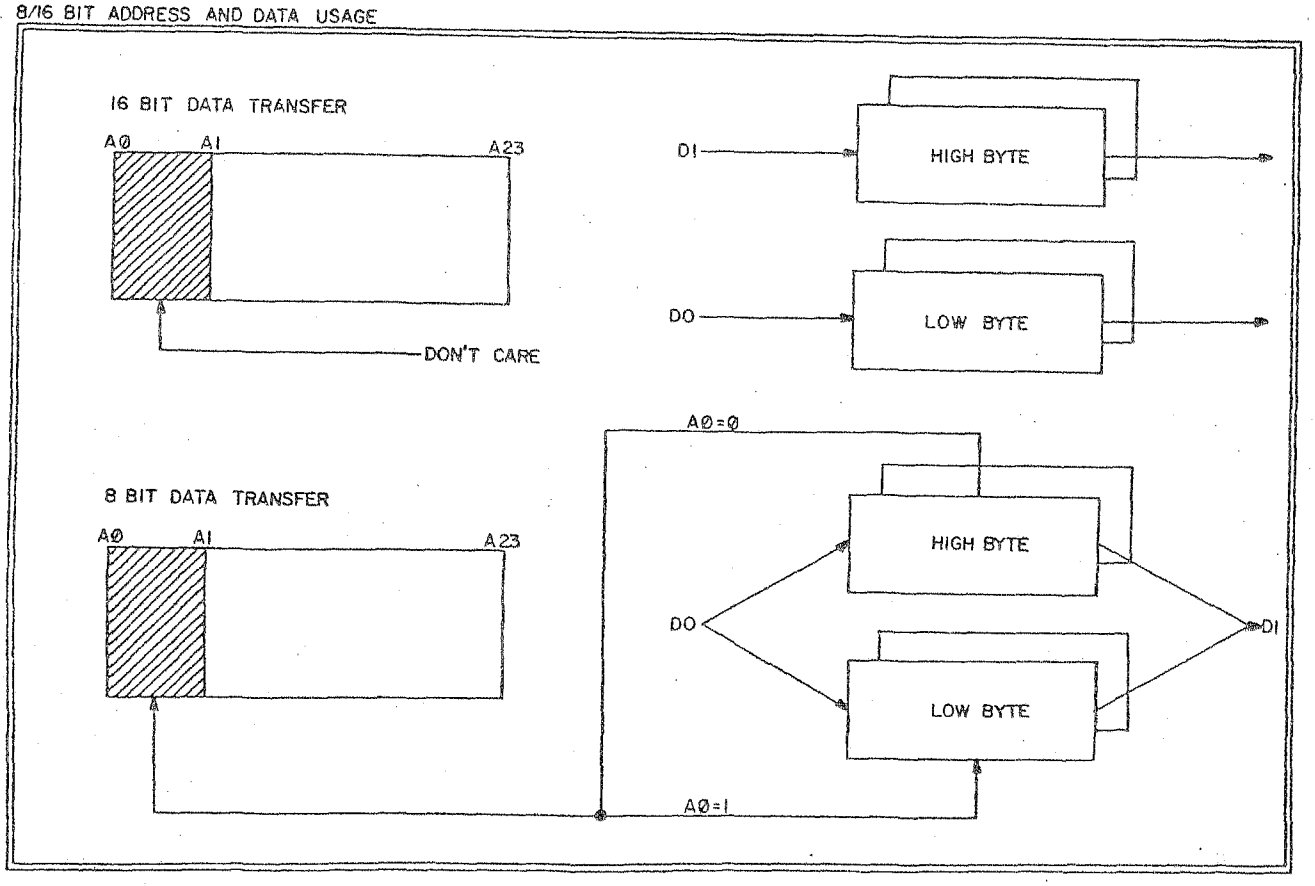
To be capable of both 8 bit and 16 bit parallel transfers memory is organized as four banks of 8 bit memory, two banks for the most significant byte of the 16 bit word, and two banks for the least significant byte. These banks may be activated either together or separately, depending on the condition of the sixteen request status line and board jumpers. Using 4116 type memory chips, each bank is 16,384 x 8 bits. Using 4115 type memory chips, each bank is 8,192 x 8 bits. This basic memory organization is shown in Figure 1.

FIGURE 1
8/16 BIT MEMORY ORGANIZATION



Memory in S-100 systems is always addressed as bytes. And since a word is composed of two bytes, the least significant address bit, A0, is not considered in address decoding for word (16 bit) references. For byte references, however, the A0 bit selects either the most significant byte or the least significant byte within the addressed word. See figure 2.

FIGURE 2
8/16 BIT ADDRESS AND DATA USAGE

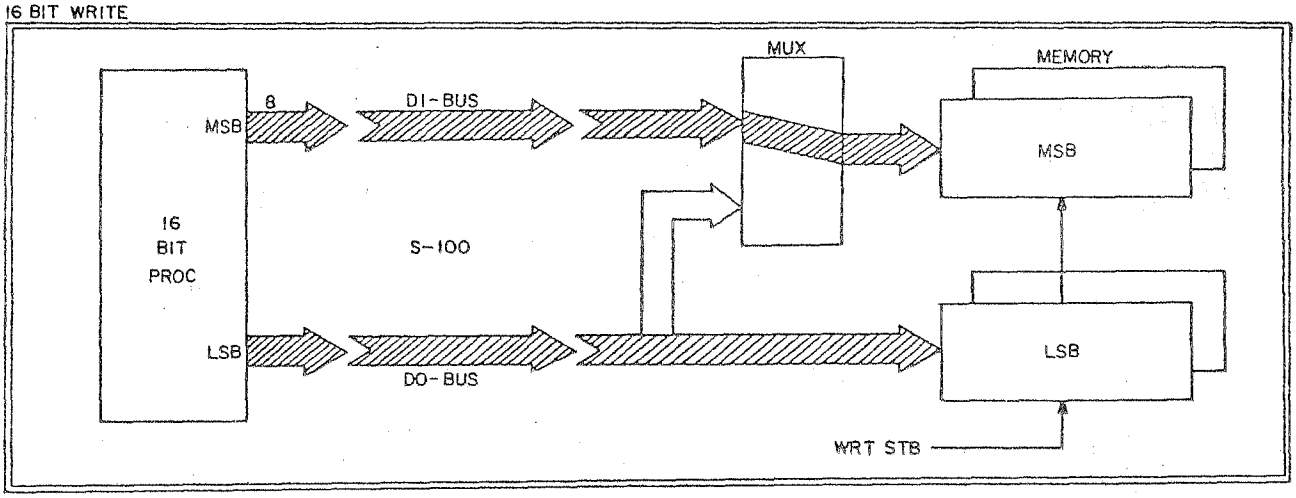


Word Transfers

For word, or 16 bit, data transfers the processor asserts the word memory address on address lines A1-A23 (A15 for short address systems), and the Sixteen Request line.

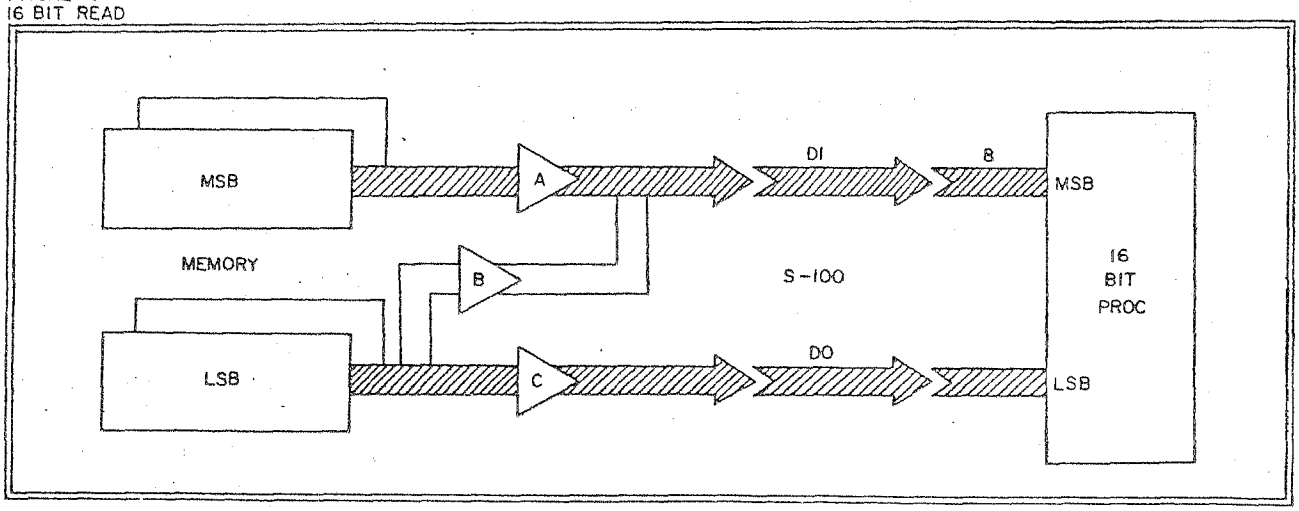
During a write operation, data is output from the processor on the 16 data lines. The least significant data byte is routed to the data lines of the least significant memory bank via the DO lines. The 2 to 1 multiplexer on the data input lines of the most significant bank is selected such that the most significant data byte, asserted by the processor on the DI lines, is routed to the data input lines of the most significant bank. The write strobe from the processor writes the data into both banks simultaneously. See Figure 3. (See Appendix II regarding the polarity of A0).

FIGURE 3
16 BIT WRITE



The 16 bit read operation follows a converse path. Data to be input to the processor is routed from the memory array banks to buffer-latches A and C (Figure 4) and then to the data lines on the bus during the read strobe. Again the data from the most significant byte is routed via the DI bus, and data from the least significant byte via the DO bus.

FIGURE 4
16 BIT READ

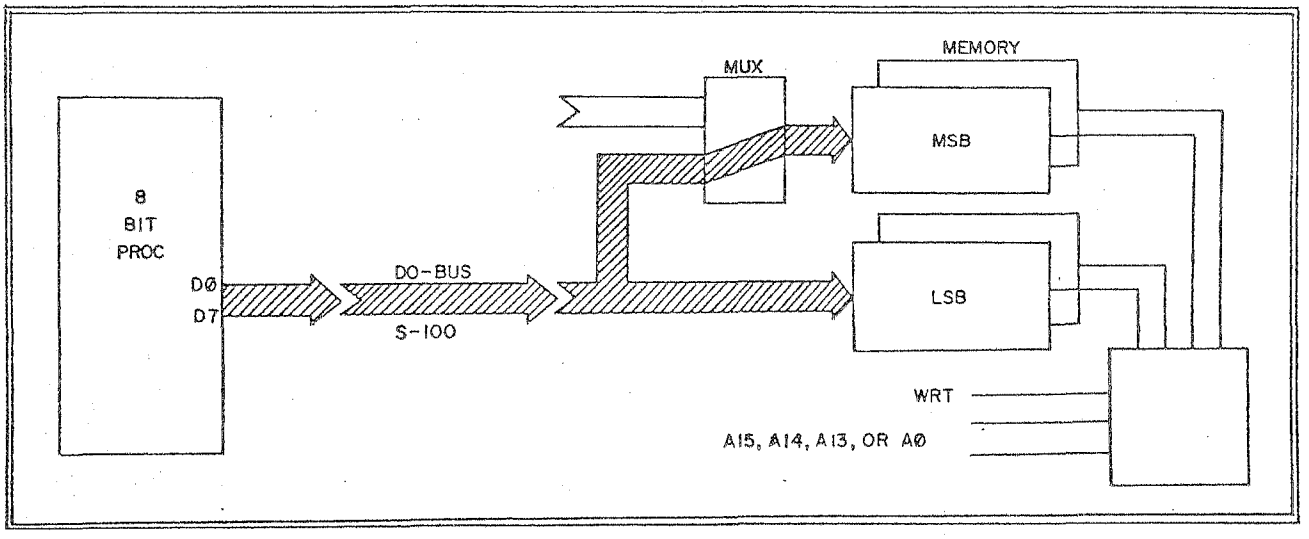


Byte Transfers

If the Sixteen Request line is not asserted, the memory reference is conducted as a single byte transfer.

Figure 5 shows the data path for an 8 bit write operation. Data is asserted by the processor on the Data Out Bus, where it is connected to the data input lines of all four memory banks; the data input lines of the least significant bank are connected directly to the DO lines, and the data input lines of the most significant bank are connected to the DO lines through the 2 to 1 multiplexer controlled by the Sixteen Request line.

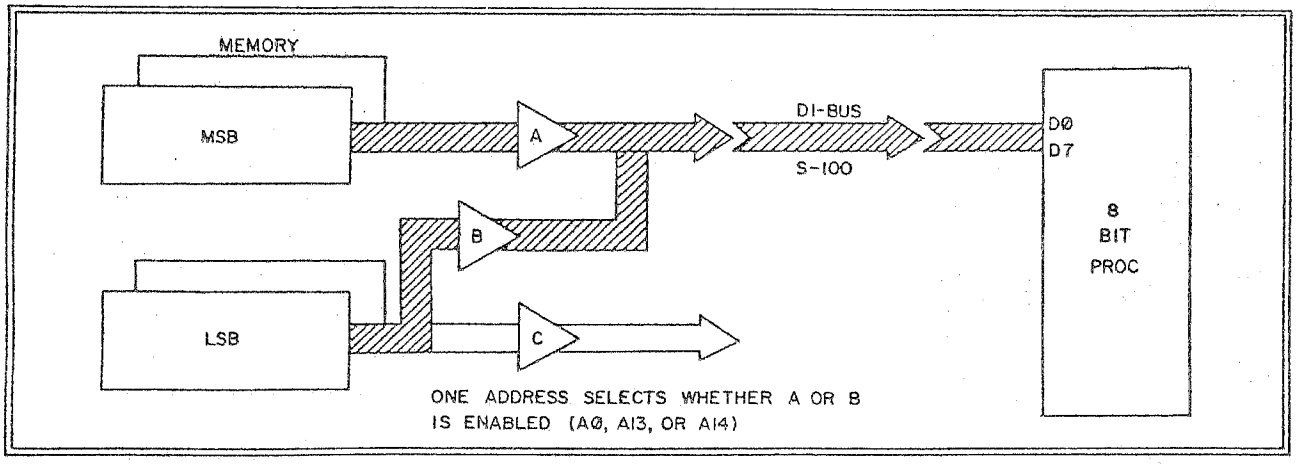
FIGURE 5
8 BIT WRITE



Two address bits are decoded to select which bank will be written into.

The 8 bit read operation is illustrated in Figure 6. Again, two address bits are decoded to enable one of the four banks. Only one of the buffers, A or B, will be enabled, depending on the condition of an address bit. The A0 bit is used to select the least or most significant banks if 16 bit transfers are used. In this case, even and odd bytes are in different banks. If the A14 or A13 bits are used, each bank contains a contiguous block of bytes, both even and odd. This allows the board to be populated with memory chips, one bank at a time. The selected buffer gates the correct byte onto the Data In Bus, where it is input by the processor.

FIGURE 6
8 BIT READ



Section 2

Board Setup and Installation

2.1 SW1, Bank Enabling

2.2 SW2, Extended Addressing

2.3 Jumper Summary

2.4 Jumper Reference and Definitions

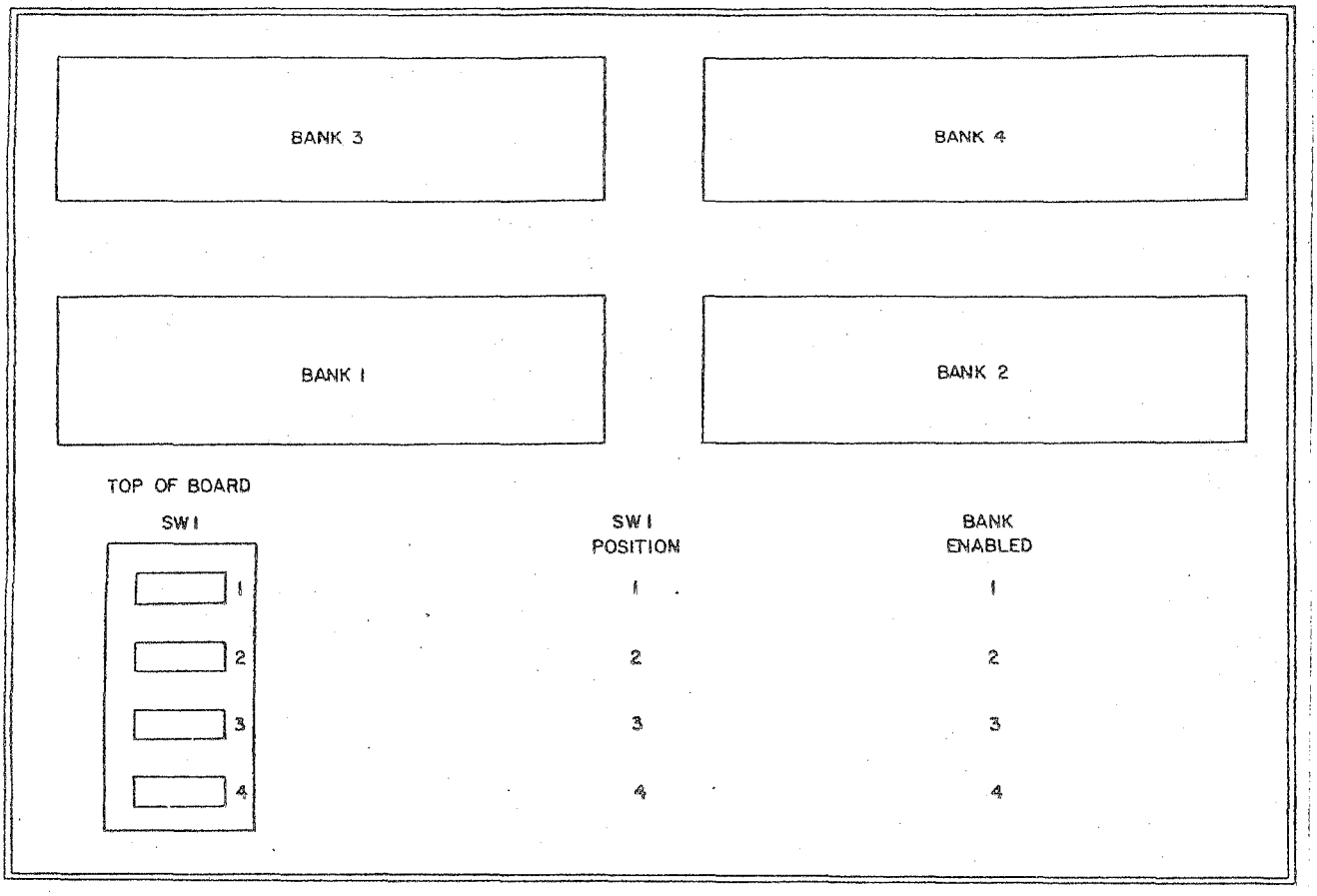
2.5 Installing the board and Checkout

2.0 Board Setup

This section of the manual describes how to set the memory board up for operation in your system, how to install the board, and what to do if the board does not work properly.

2.1 SW1 SW1 is used to enable the individual memory banks. Closing (shorting) a DIP switch in SW1 enables one bank. A bank is turned off (no read or write operations) when its respective DIP switch is left open. A turned off bank is refreshed.

FIGURE 7



During 16 bit transfers, Banks 1 and 2 or Banks 3 and 4 are decoded simultaneously. Therefore the switches must be turned on as pairs: 1-2, 3-4. If only 8 bit transfers are used, the bank decoding circuitry can be set by jumpers so that odd numbers of banks can be used. Table I gives the byte and word addresses contained in each bank for the different jumper-selectable modes of operation of the RAM board. As an example of the use of this table, suppose that

you want to operate the board with 4115 type memory chips and you only need additional 8 bit memory from 48K to 56K. First refer to the Jumper Section of this manual and configure the RAM board for the type of processor in your system and for 4115 type memory. From Table I, you find under the heading "4115 8 bit transfers only" that with jumper J18 set to the C position, bank 3 is decoded from 48K to 56K. Therefore, referring to Figure 7, you close SW1 position 3 to enable bank 3. In this case, only Bank 3 needs memory chips. The other banks can be disabled by leaving the other switches in SW1 open and other memory or memory-mapped boards can occupy the address spaces 0 - 48K and 56K - 64K.

Table I

Byte and Word Locations

4116 8/16 bit transfers

Banks 1 and 2: 0-32767 (32k) bytes or 0-16383 words.
Banks 3 and 4: 32768 (32k)-65535 (64k) bytes of 16384-32767 words.
(Even bytes in banks 1 and 3).*

4116 8 bit transfers only

Bank 1: 0-16383 (16k) bytes.
Bank 2: 16384 (16k)-32767 (32k) bytes.
Bank 3: 32768 (32k)-49151 (48k) bytes.
Bank 4: 49152 (48k)-65535 (64k) bytes.

4115 8/16 bit transfers

J18-B

Banks 1 and 2: 0-16383 (16k) bytes or 0-8191 words.
Banks 3 and 4: 16384 (16k)-32767 (32k) bytes or 8192-16383 words.
(Even bytes in banks 1 and 3).*

J18-C

Banks 1 and 2: 32768 (32k)-49151 (48k) bytes or 16384-34575 words.
Banks 3 and 4: 49152 (48k)-65535 (64k) bytes or 24576-32767 words.
(Even bytes in banks 1 and 3).*

4115 8 bit transfers only

J18-B

Bank 1: 0-8191 (8k) bytes.
Bank 2: 8192 (8k)-16383 (16k) bytes.
Bank 3: 16384 (16k)-24575 (24k) bytes.
Bank 4: 24576 (24k)-32767 (32k) bytes.

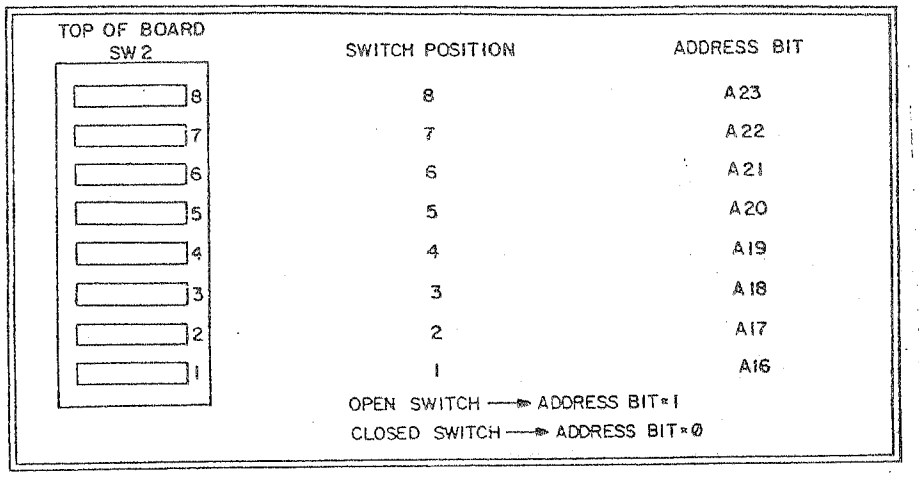
J18-C

Bank 1: 32768 (32k)-40959 (40k) bytes.
Bank 2: 40960 (40k)-49151 (48k) bytes.
Bank 3: 49152 (48k)-57343 (56k) bytes.
Bank 4: 57344 (56k)-65535 (64k) bytes.

* See appendix II regarding the polarity of A0.

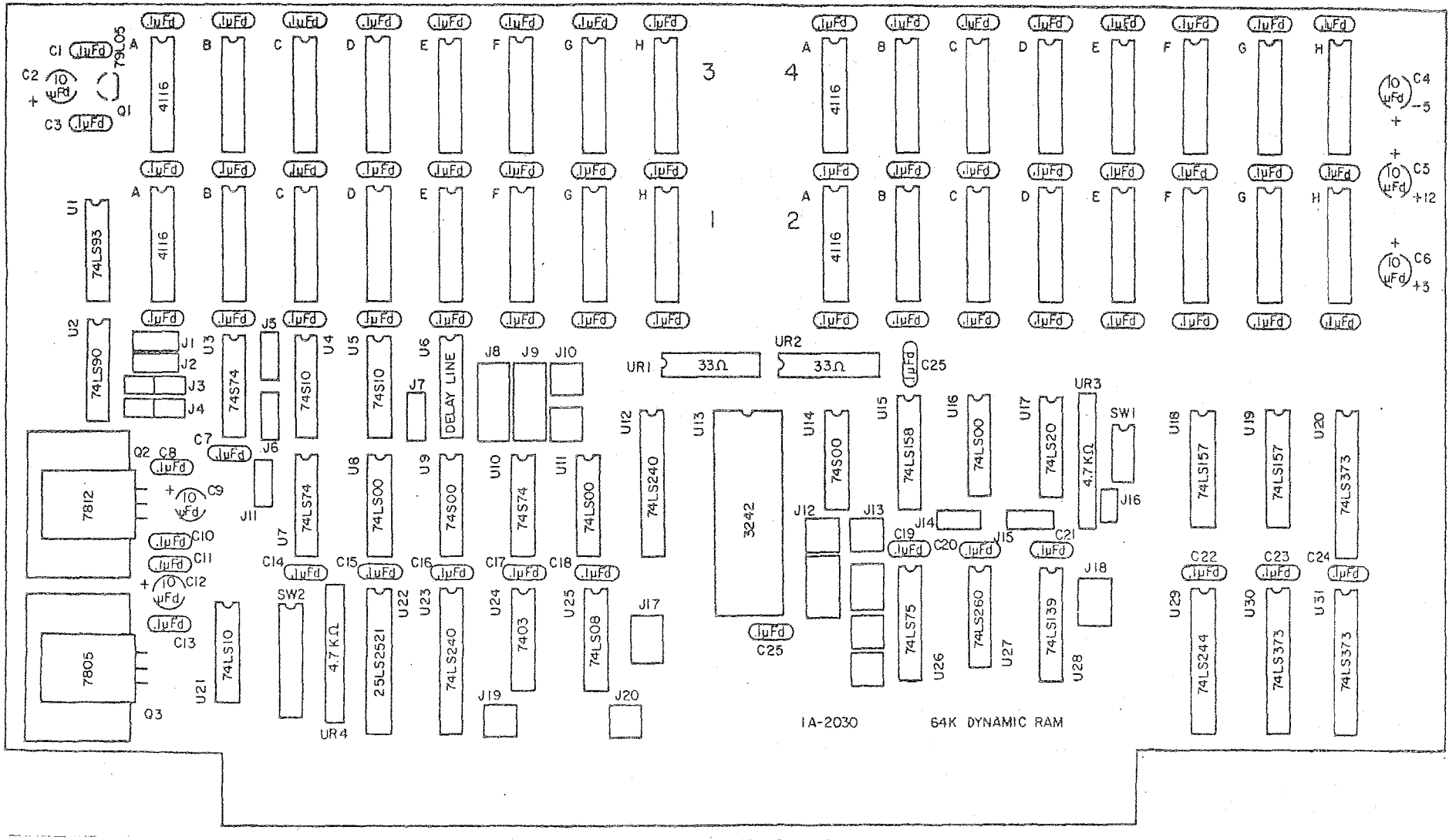
2.2 SW2 While SW1 is used to enable the 8 or 16K banks in a 64K memory space, SW2 is used to enable the operation of the RAM board in one of 256 possible 64K memory segments. This provides a total address range of 16 megabytes. The four RAM banks are decoded in the same 64K segment. In systems using only 16 address lines (64K space), SW2 is disabled by setting jumper J19 to the A position. In systems using the extended 24 bit address bus, SW2 is enabled by setting J19 to B. The eight DIP switches in SW2 are set to the starting binary address of the desired 64K segment.

FIGURE 8



For example, the second 64K segment, 65K - 128K, would have a starting binary address of 00000001. Therefore switch position 1 would be opened and the other seven positions would be closed.

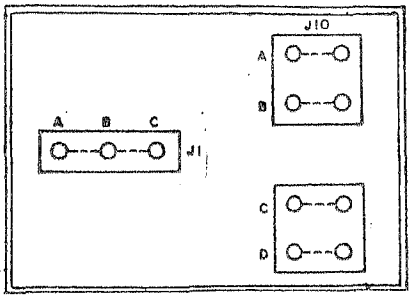
FIGURE 9


IA-2030
64K DYNAMIC RAM
4116
74LS93
74LS90
74S74
74S10
74LS10
74LS74
74LS00
74S00
74S74
74LS00
74LS240
3242
74LS158
74LS00
74LS20
4.7KΩ
74LS157
74LS157
74LS373
74LS373
74LS244
74LS373
74LS139
74LS260
74LS75
74LS08
7403
25LS2521
74LS240
74LS10
7812
7805
DELAY LINE
33Ω
33Ω
.1μFd
10 μFd

2.3 Jumper Summary

There are twenty jumper areas on the 64K RAM board. They are used to set up the board for different processors and processor speeds, and to select the method of memory organization and addressing. Each jumper area consists of from 1 to 4 boxes. Each box contains a group of plated-through holes spaced 0.1" apart. Figure 9 shows the board location of the boxes. To configure a jumper area, one connection per box is made between adjacent plated-through holes. The connection is either made by a printed circuit trace on the solder side of the board or by a shunt that slides onto 0.040 inch square posts that are soldered into the plated-through holes. To change a connection made by a printed circuit trace, the trace must be cut between the plated-through holes. All of the possible connections within a jumper area are given letter names and are called "jumper positions." The letter names run A B C... from left to right or from top to bottom depending upon the orientation of the jumper. As an example, Figure 10 shows two of the jumpers on the board.

FIGURE 10



The J1 jumper area is composed of a single box with three plated-through holes. There are two possible shunt positions. The position between holes A and B is named J1:A-B. The position between holes B and C is named J1:B-C. The J10 jumper area is composed of two boxes containing a total of eight plated-through holes. The two possible shunt positions per box are marked with dotted lines in the Figure. The position between the top pair of holes is named J10-A. The position between the bottom pair is named J10-D.

Table II summarizes how to set the jumpers for some common combinations of processors and operating modes. Appendix III of this manual will extend Table II by including additional types of processor boards.

Table II

CPU*	1	2	3	4	5	6
J1	A-B	A-B	B-C	A-B	A-B	A-B
J2	A-B	A-B	B-C	B-C	B-C	B to grd
J3	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
J4	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
J5	A-B	A-B	B-C	A-B	B-C	A-B
J6	B-C	B-C	A-B	B-C	A-B	A-B
J7	B-C	B-C	B-C	B-C	B-C	B-C
J8	A	A	E	A	C	C
J9	D	D	D	A	D	D
J10 Top	A	A	A	B	B	A
J10 Bottom	D	D	C	C	C	C
J11	A-B	A-B	A-B	A-B	A-B	B-C
J12 Top	A	B	B	A	A	A
J12 Bottom	C	E	F	C	C	D
J13 Top	B	B	B	B	B	A
J13	E	D	D	E	E	C
J13	G	F	F	G	G	G
J13 Bottom	I	H	H	I	I	I
J14	B-C	B-C	A-B	B-C	A-B	B-C
J15	B-C	B-C	A-B	B-C	A-B	B-C
J16	Open	Open	Open	Open	Open	Open
J17	C	C	C	C	C	B
J18	A	B	B	A	A	A
J19	A	A	A	A	B	B
J20	B	B	B	B	B	A

* CPU Type

1 InterSystems Z80 Rev. 1.3, 4mHz., 4116, 64k, 8 bit.

2 InterSystems Z80 Rev. 1.3, 4mHz., 4115-40, 32k, 8 bit.

3 8080, 2 mHz., 4115-41, 32k, 8 bit.

4 Intersystems Z80II, No Extended Addressing, No Wait States, Partial Latch Mode, 4116, 64k, 8 bit.

5 InterSystems Z80II, Extended Addressing, M1 Wait State on CPU, Full Latch Mode, IEEE Mode, 4116, 64k, 8 bit.

6 InterSystems Z8000 or Z80II, IEEE Mode, 4116, 64k, 8/16 bit.

2.4 Jumper Reference and Definitions

If your system's configuration is not included in Table II or Appendix III, then you will have to set the jumpers individually. This section explains the function of each jumper box and lists the options that can be selected by each jumper position. This section also includes a short list of definitions of terms used to describe the jumper functions, and groups related jumper areas together under their functions. When configuring the RAM board for the following options, refer to the listed jumper areas:

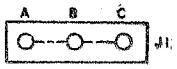
4115/4116:	J12, J13, J18
4115-40/4115-41:	J12
8 bit only/8 and 16 bit operation:	J12, J13
Wait states:	J10, J17
Front Panel operations:	J20
Extended Addressing:	J19

Definitions

Processor cycle:	An S-100 bus cycle composed of 3 or more bus states, such as a read, write, or I/O cycle.
Instruction Fetch cycle:	A processor cycle where the next program instruction is read from memory.
RAM Board cycle:	The timing sequence performed by the RAM board during one read, write, or refresh.
External cycle:	A read or write RAM board cycle. An external cycle is started or triggered by S-100 bus signals.
Refresh cycle:	A RAM board cycle used to restore data to nondegraded voltage levels.
Transparent Refresh:	A refresh cycle triggered by S-100 bus timing so that the refresh cycle does not overlap an external cycle.

Default Refresh:	A refresh cycle triggered by counters on the RAM board without regard to the type of processor cycle.
RAS Precharge Time:	The time between the end of a RAS pulse and the start of another.
External-Refresh Request Arbitration:	The decision that is made to service either an external or a refresh cycle request signal first.
pSYNC:	An S-100 control signal that indicates the start of a processor cycle.
sSXNREQ:	An S-100 status line. Driven low when a bus master requests a 16 bit data transfer.
sMEMR:	An S-100 status line. Indicates a memory read cycle.
sM1:	An S-100 status line. Indicates an instruction fetch cycle.
MWRITE:	An S-100 control signal that is used to strobe data into memory.

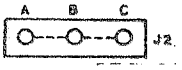
Jumper Reference

J1: 

J1 selects the default refresh rate.

A-B Processor speed:
2mHz, default refresh every 32 us.
4mHz, default refresh every 16 us.

B-C Processor speed:
2mHz, default refresh every 16 us.
4mHz, default refresh every 8 us.

J2: 

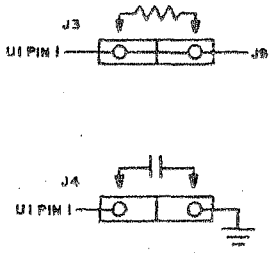
J2 selects a signal (M1, shifted M1, or grd) which is used to enable the start of a transparent refresh cycle during an External Clear pulse. This allows a transparent refresh cycle to occur immediately after the RAS precharge time of instruction fetch cycles. Shifted M1 is selected when M1 would not stay high until the RAS precharge time.

A-B Shifted M1 selected, normally used at 4mHz and with a CPU that does not latch the M1 status line.

B-C M1 selected, normally used at 2mHz or with CPUs that latch the M1 status line.

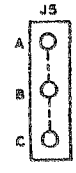
B-Grd Disables transparent refresh.

J3-J4:



J3 provides space for a resistor. J4 provides space for a capacitor. The board is normally delivered with J3 shorted and J4 open. The resistor and the capacitor are used to delay the clock into the refresh counter. The purpose of this delay is to prevent a default Refresh request signal from occurring at exactly the same time as an external cycle request. This could cause an arbitration error. The RC delay is normally not needed because jumper J9 provides four different times for default requests to occur.

J5:

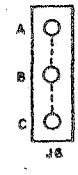


An external cycle during write can be started either at the beginning of the MWRITE pulse or earlier in the processor's write cycle during the pSYNC pulse. Starting a write cycle during pSYNC allows the write cycle to end earlier and the next cycle to start earlier.

A-B MWRITE does not start an external cycle. J14:B-C must be closed and J15:B-C may need to be closed.

B-C MWRITE will start an external cycle. J14:A-B should be closed.

J6:



The Z80 outputs M1 status very early in its cycle. The board can perform an M1 lookahead trigger to provide more access time during instruction fetch cycles.

A-B M1 lookahead trigger disabled. The trigger will occur during pSYNC.

B-C M1 lookahead trigger enabled. The trigger will occur on the first clock transition of $\phi 2$ after the M1 status line goes active high. J10:A-B should be set so that U3 p6 goes low in the middle of the Z80's T1 state. The M1 lookahead trigger will only provide more access time if the M1 status is not latched and is output considerably earlier than pSYNC.

J7:

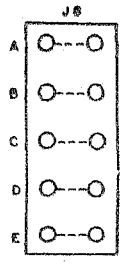
J7 is used to select one of two taps on the delay line. The selected tap determines the length of the Stop Cycle signal. This determines the minimum time when RAS is high, the RAS precharge time. J7 should normally be set to select the longest time. The

shorter time should be selected only if there is a possibility of another external cycle starting before the current external cycle has ended. The worst case pattern for this to occur is a long cycle during write followed by an M1 lookahead trigger cycle. This condition should only occur at greater than 4mHz operation. It can also be avoided by modifying the long cycle (see J10, J15), not using the M1 lookahead trigger, or adding wait states.

A-B Short precharge. Use 4116-2.

B-C Long precharge.

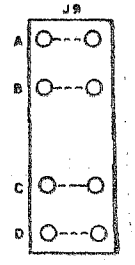
J8:



J8 is used to select when during the pSYNC pulse the external cycle should start. An external cycle cannot start until the address is stable on the S-100 bus and the user may desire not to start a cycle until the status is stable.

Shunt Position	Cycle Start
A	Rising edge of pSYNC.
B	Positive STVAL during pSYNC.
C	Negative STVAL during pSYNC.
D	Positive ϕ2 during pSYNC.
E	Negative ϕ2 during pSYNC.

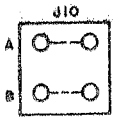
J9:



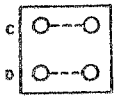
J9 selects a clock input for the refresh counters U1 and U2. A variety of clocks are provided so that the counter will not change state and possibly request a default refresh cycle at exactly the same time as an external cycle request. If default refresh and external cycle request were to occur at the same time, an arbitration error could result. The refresh count is disabled during and after pSYNC by the shifted pSYNC signal, U10 p9. Therefore an arbitration error can only occur for an M1 lookahead trigger or an unqualified pSYNC trigger (J8-A). U1 counts on the falling edge of the clock signal. Do not select opposite polarity of ϕ2 as is used to clock the M1 lookahead circuit. If J8-A is used, then select a clock whose falling edges do not coincide with the rising edge of pSYNC. Some processor boards do not output a 2 or 4 mHz ϕ1 clock signal on S-100 line 25. Instead the line has been defined to be a status valid strobe that occurs once per cycle. Do not use the ϕ1 or $\overline{\phi 1}$ taps if this is the case. Jumpers J3 and J4 can also be used to delay the selected clock signal.

Shunt Position	Edge Used to Clock U1
A	Falling edge of ϕ2.
B	Falling edge of ϕ1 (pSTVAL).
C	Rising edge of ϕ1.
D	Rising edge of ϕ2.

J10 Top half:



The upper half of J10 is used to select the proper polarity of the 02 signal to clock U3 p3. This flip flop is used to create the Shifted M1 signal. The Shifted M1 signal is used as an external trigger (see J6) and as an input to the refresh counters (see J2). When used with a Z80, J10 should be set so that Shifted M1 goes active high during the middle of the T1 state.



Position Selected

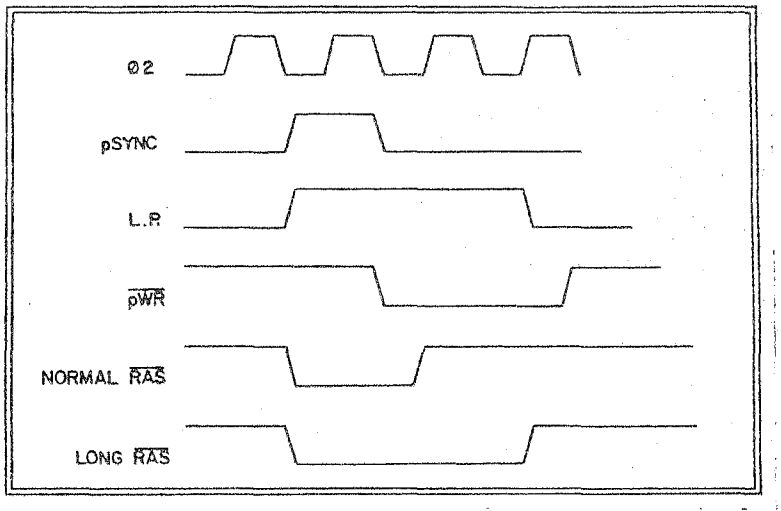
A U3p3 clocked by falling edge of ϕ2.
B U3p3 clocked by rising edge of ϕ2.

J10 Bottom half:

The lower half of J10 is used to select the proper polarity of the ϕ2 signal to clock U10 p11. The flip flop is used to create the Lengthened pSYNC signal. The Lengthened pSYNC signal goes active at the start of pSYNC and stays active until the selected edge of ϕ2 after pSYNC. Lengthened pSYNC is used for three operations:

(1) During a write cycle, RAS must stay low for a minimum of 70 ns after the start of the write strobe for 200 ns memory chips and 85 ns for 250ns chips. Some processors output the write strobe very late in their cycles, and if the memory board's cycle is started during pSYNC, then the write strobe can be missed by RAS. The Lengthened pSYNC signal is used to lengthen RAS so that it overlaps write.

FIGURE 11



(2) If a default refresh request wins an arbitration, then the processor must be placed in a wait state until the external cycle can be serviced. This method will fail if the wait request from the arbitration circuitry occurs too late in the

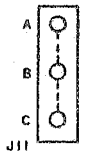
cycle to produce a wait state. This is prevented by gating off the refresh count during the Lengthened pSYNC pulse.

(3) The Lengthened pSYNC pulse is gated through U24 to request a wait state during conditions selected by J17.

C Lengthened pSYNC goes inactive on the first rising edge of 02 after pSYNC.

D Lengthened pSYNC goes inactive on the first falling edge of 02 after pSYNC.

J11: J11 selects whether an external trigger signal can clock U3 p11 to create an External Cycle Request when the Board Select signal is off.

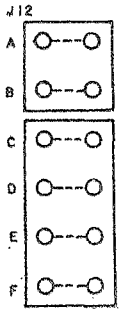


A-B Board Select not used to enable External Cycle Request. Use if address is stable before status.

B-C An External Cycle trigger will not cause an External Cycle Request unless the Board Select signal is high. Only memory read or write cycles to enabled memory banks will generate a memory cycle.

J12: J12 positions A and B select the S-100 address that is output to pin 10 of all RAMs during CAS.

A 8/16 bit mode or 8 bit mode with 4116 type memory, A13 selected.



B 8 bit mode with 4115 type memory, A0 selected

J12 positions C, D, E and F select the S-100 address or the logic level that is output to pin 5 of all RAMs during CAS.

C 8 bit mode, 4116, A0 selected.

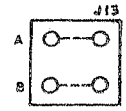
D 8/16 bit mode, 4116, A14 selected.

E 8 or 8/16 bit mode, 4115-40, +5V selected, Grd output.

F 8 or 8/16 bit mode, 4115-41, Grd selected, +5V output.

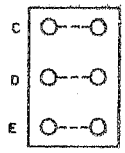
J13: J13 selects status and address signals that are used to decode which RAM banks will be selected.

A sSXNREQ used. RAM banks selected as pairs when sSXNREQ is active low.



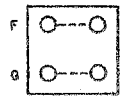
B sSXNREQ not used. RAM banks selected singly.

C 8/16 bit transfer mode. Maps even and odd bytes into separate banks. A0 selected.



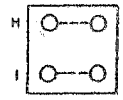
D 8 bit mode, 4115 type memory, A13 selected.

E 8 bit mode, 4116 type memory, A14 selected.



F 4115 type memory, A14 selected.

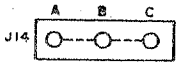
G 4116 type memory, A15 selected.



H 4115 type memory, A15 selected.

I 4116 type memory, Status Enable selected.

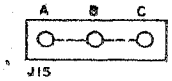
J14: J14 selects whether an external cycle trigger will be generated for every pSYNC or during pSYNC AND sMEMR. See J5.



A-B pSYNC AND MEMR produces trigger.

B-C pSYNC produces trigger.

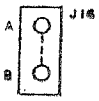
J15: J15 selects whether a long cycle will be enabled during sMEMR. The long cycle is used so that during a 4mHz S-100 write cycle, the memory board's cycle can be started during pSYNC and ended sooner than a memory cycle that was started during the MWRITE pulse. This provides more time for the next cycle. See J10 (Lower half).



A-B No long cycles.

B-C Long cycles during sMEMR.

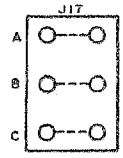
J16: J16 is used to disable the S-100 Error line input. If this line is not driven, bus crosstalk can cause the memory board to be disabled at the wrong time.



J16 Open Error not used.

J16 Closed Error used.

J17: J17 enables the wait state generator.



A Wait state on any board cycle.

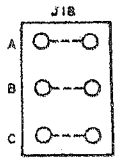
B Wait state during M1 cycles.

C No wait states.

J18: J18 selects signals that are used to enable the RAM banks.

J13-H shunted 4115 mode.

J18-A Don't use.



J18-B Board selected for A15=0.

J18-C Board selected for A15=1.

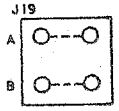
J13-I shunted 4116 mode.

J18-A Board always selected. Use if board is triggered before status is valid.

J18-B Don't use.

J18-C Board selected when status is correct. The S-100 status must be valid before the board is triggered.

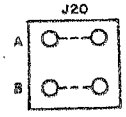
J19: J19 selects whether the output of the extended address comparator, U22, is gated into the board select signal.



A The board decodes a 64K address space.

B The board decodes a 16 Mbyte address space.

J20: J20 selects the signals that are used to decode a front panel deposit.



A Deposit = XRDY AND MWRITE.

B Deposit = DBIN AND MWRITE.

2.5 Installing the Board and Checkout

Once you have selected the board address and set the jumpers, you can install the board in your system. With the system power off, insert the board into the S-100 bus, taking care not to skew the card fingers with respect to the edge connector (it is possible with some card edge connector sockets to skew the board such that the gold fingers on the board seat between the brushes of the socket). Turn on the system power and run a memory test program such as TSTMEM, which is supplied with all InterSystems Disk Operating Systems, over the address space covered by the new memory board. Your memory board has been extensively tested and burned in before shipment from the InterSystems plant, and should work the first time. If you do have trouble, however, here are some pointers: Power down the system. Check the following:

(1) Is the board seated in the edge connector properly?

(2) Has one of the chips on the board been jarred loose in shipping?

(3) Are the jumpers set properly. If your CPU was not listed and you guessed at this, try another position.

(4) Try adding a wait state. Is the board the right speed for your system? If the jumpers are set improperly, the board may appear to need a wait state.

(5) How's your power supply? Check the +8 volt line on the bus (pins 1 and 51). If it's less than 7.5 volts, this could be the problem.

(6) Is one of your old boards generating bus line 58? This line, now the IEEE line indicating a 16 bit data transfer request, may have been assigned a special function by a manufacturer of pre-IEEE S-100 boards.

If none of the above solve your problem, or if you need any assistance whatsoever, give us a call at (607) 257-0190. If you desire to debug the board yourself, try the following:

(1) Assume that only one memory chip is bad. Run a memory test program. The program should indicate the address and bad bit(s) of any byte or word that fails the test. Refer to Section 2.1 and Table I of this manual to locate the memory chip that corresponds to an address given by the memory test program.

(2) Rock a suspected chip in its socket. Check for bent pins. Try the memory test program again.

(3) Replace a suspected chip. Be careful to orient the new chip correctly. Try the memory test program again.

(4) If a substituted chip also tests bad, if many different chips are indicated as being bad, or if the memory test program won't even run with the RAM board in the system, then it is likely that there is either a mistake in the jumpering or circuitry of the RAM board.

Read the technical section of this manual, recheck the jumpering, and if necessary follow the steps in the 3.11 Repair Section.

Technical Reference Section

3.1 Memory Organization

- Write Data Paths
- Read Data Paths
- RAS Decoding

3.2 Board Selection

3.3 Block Diagram

3.4 Refresh Cycle

3.5 External Cycle

3.6 External-Refresh Request Arbitration

3.7 Delay Line Timing Circuitry

- RAS Enable
- Refresh Enable
- Refresh Active
- D1
- Row Enable
- External Cycle
- D2
- $\overline{CAS}$
- D3-D4
- D5
- Stop Cycle
- External Clear

3.8 Wait State Generator

3.9 Conflict Resolver Circuit

3.10 Front Panel Deposit

3.11 Repair

3.12 Timing Diagrams

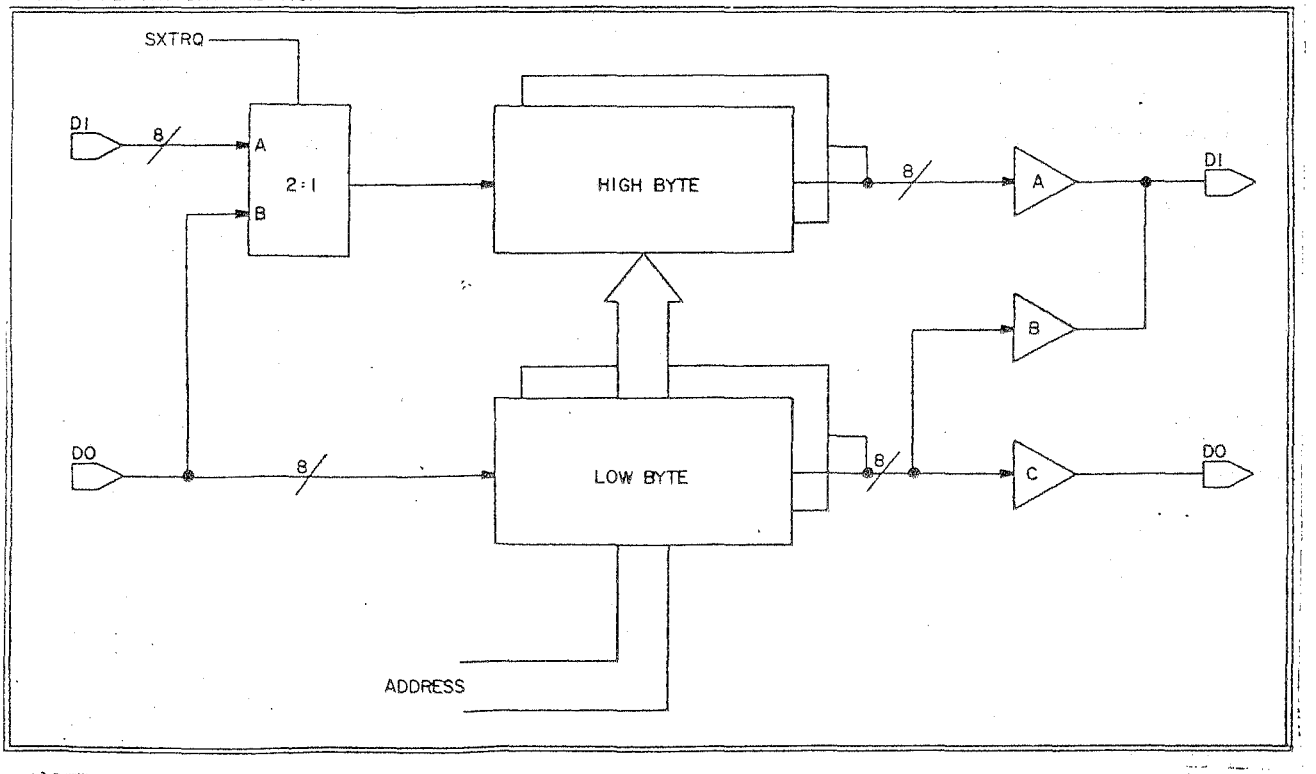
3.0 Technical Reference

This section describes the operation and repair of the circuitry of the InterSystems 64K RAM board. It is intended for maintenance personnel rather than the general user and contains no user information not available elsewhere in the manual.

3.1 Memory Organization

The memory data paths are shown in Figure 11. These paths can be switched on and off to configure the RAM board for 8 bit, 16 bit, read or write operations.

FIGURE 12
8/16 BIT MEMORY ORGANIZATION

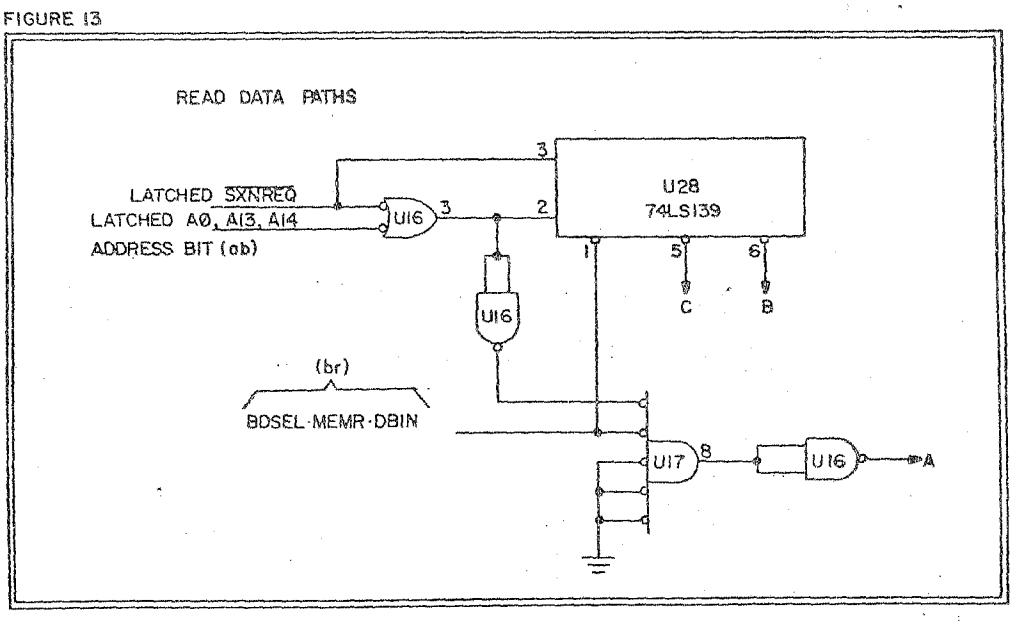


Write Data Paths: The SXNREQ status line controls the 2:1 data multiplexers U18 and U19. During an eight bit transfer, SXNREQ is high and the Data Out, DO, bus is gated to all four banks. During sxiteen bit transfers, the Data Out bus is gated to banks 1 and 3. For both 8 and 16 bit writes, only a bank receiving a RAS pulse will be written into. The latch-buffers U20, U30, and U31 are off during a write.

Read Data Paths:

During 16 bit reads, the A and C buffer-latches are enabled simultaneously while the B buffer is never enabled. During 8 bit reads, the polarity of the address bit (ab) selects between the A and B buffer-latches. Each buffer-latch is connected to two banks. Only the bank to be read receives a RAS pulse. The other bank remains tristated. (See Appendix II regarding the polarity of A0).

FIGURE 13



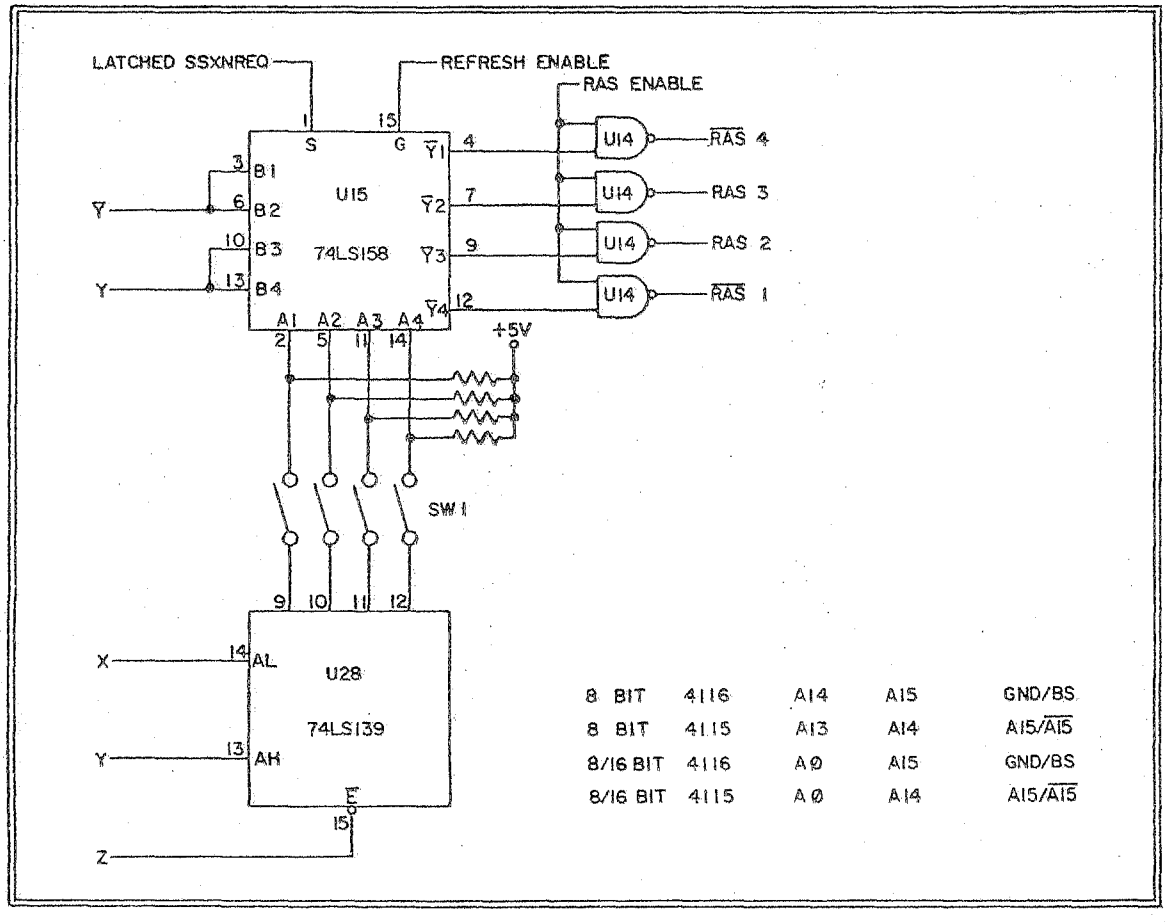
(br)	$\overline{\text{sSXTREQ}}$	(ab)	$\overline{A}$	$\overline{B}$	$\overline{C}$
1	0	X	0	1	0
1	1	0	0	1	1
1	1	1	1	0	1
0	X	X	1	1	1

X = Don't Care.

RAS Decoding:

The RAS Decoding is the same for read and write operations. During 8 bit transfers, RAS is gated to one bank. During 16 bit transfers, RAS is gated to a pair of banks: 1 and 2, or 3 and 4. Both types of decoding, 1 of 4 or 2 of 4, are done simultaneously and then U15, a 2 to 1 multiplexer, selects which decoding method to use depending upon the polarity of the sSXNREQ status line. A positive output from U15 selects the NAND gate(s) in U14 that will turn on when the delay line circuitry generates a RAS Enable signal. During a Refresh cycle, all four banks require a RAS pulse. When the Refresh Enable signal goes active high, the U15 outputs are all set high, selecting all four gates in U14.

FIGURE 14



During 16 bit transfers, U15 p1 is high and the B inputs of the multiplexer are selected. If Y is low, then RAS 1 and 2 are enabled. If Y is high, RAS 3 and 4 are selected. For example, if 4115 memory chips are being used, Y=A14 and banks 1 and 2 will be the low order banks spanning 0 - 16K bytes and 32 - 48K bytes. The Board Select signal will contain the A15 bit information and will determine which range to use.

During 8 bit transfers, U15 p1 is low and the A inputs of the multiplexer are selected. The A inputs are driven by U28, a 1 of 4 decoder, through switches in SW1. If a switch in SW1 is open, the respective bank is never enabled in 8 bit mode. In 4115 mode, neither A15 or $\overline{A15}$ is used to enable U28 (bit Z). this maps the selected bank into the top or bottom half of a 64K memory segment. The X and Y address bits are decoded to select which bank will be enabled.

Address Bit X Y Z	Signal at SW1 1 2 3 4	Bank Selected
- - 1	1 1 1 1	None
0 0 0	0 1 1 1	1
0 1 0	1 0 1 1	2
1 0 0	1 1 0 1	3
1 1 0	1 1 1 0	4

For example, in 8/16 bit mode, X=A0. (See Appendix II regarding the polarity of A0). This maps bytes with odd addresses into banks 1 and 2, and banks with even addresses into banks 3 and 4.

3.2 Board Selection

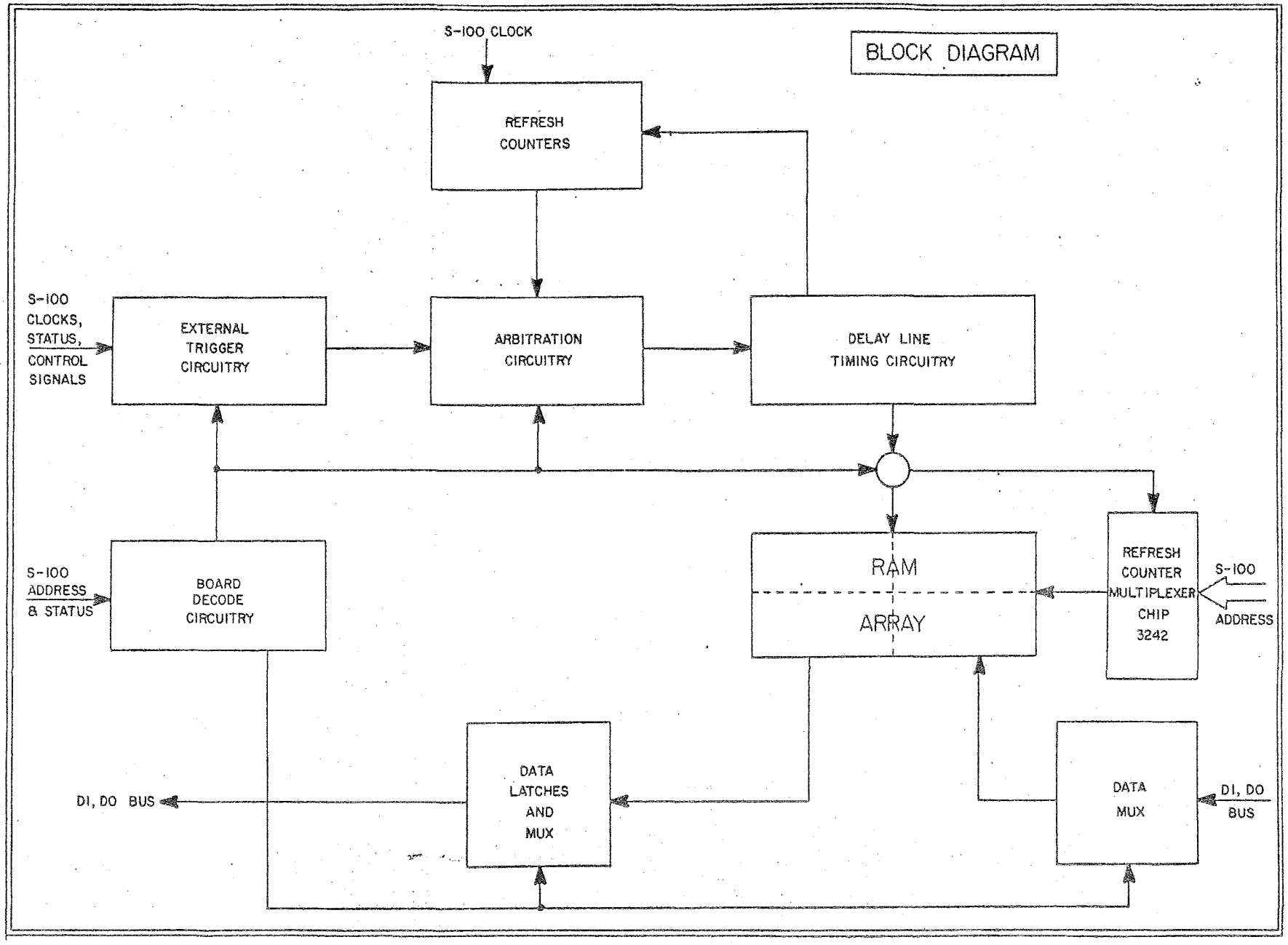
The board is selected (U25 p8 high) when a bank that is enabled by SW1 is decoded by U28 and the following signals are in the specified states:

Signal Name	S100 #	Condition
sOUT	45	0
sINP	46	0
sHLTA	48	0
sINTA	96	0
$\overline{\text{PHANTOM}}$	67	1
$\overline{\text{ERROR}}$	98	1 if J16 closed
Extended Address Comparator	U22p19	0 if J19 A-B closed

The Board Select signal is used to enable wait state requests, the write strobe into the memory array, and $\overline{\text{SIXTN}}$, the sixteen acknowledge signal. When jumper J11:B-C is closed, the External Trigger Request signal is also enabled by Board Select.

3.3 Block Diagram

FIGURE 15


BLOCK DIAGRAM
S-100 CLOCK
REFRESH COUNTERS
S-100 CLOCKS, STATUS, CONTROL SIGNALS
EXTERNAL TRIGGER CIRCUITRY
ARBITRATION CIRCUITRY
DELAY LINE TIMING CIRCUITRY
S-100 ADDRESS & STATUS
BOARD DECODE CIRCUITRY
RAM
ARRAY
REFRESH COUNTER MULTIPLEXER CHIP 3242
S-100 ADDRESS
DI, DO BUS
DATA LATCHES AND MUX
DATA MUX
DI, DO BUS

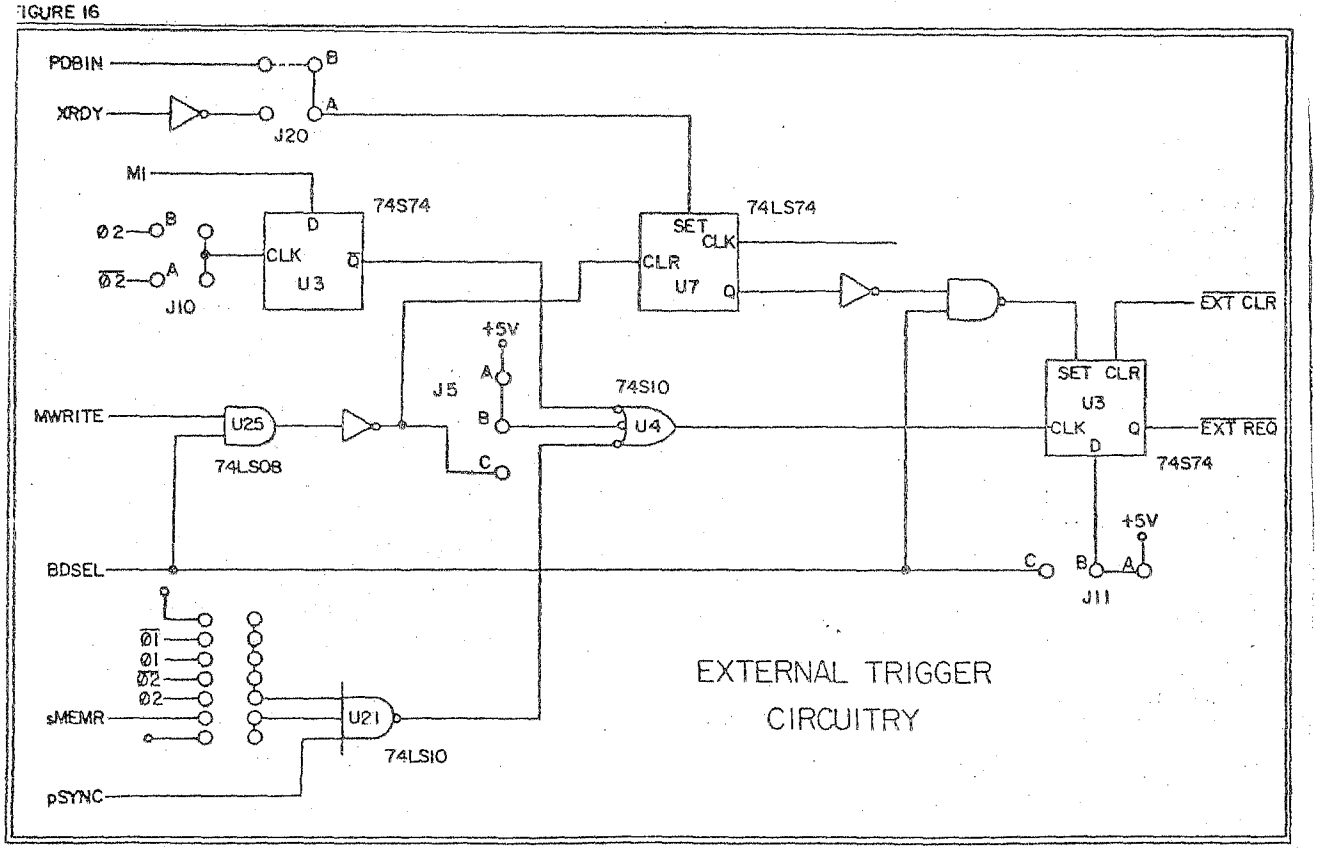
3.4 Refresh Cycle

Each memory cell must be refreshed at least once every 2 msec. This is accomplished by performing a RAS-only refresh cycle on each of the 32 memory chips simultaneously. During a refresh cycle, the output of a 7 bit refresh-address counter is multiplexed onto the RAM chips' address lines by U13. Then a 1/4 sec RAS pulse is gated to each RAM chip. The refresh counter is incremented after each refresh.

A refresh cycle can be started in two ways. In transparent refresh, a refresh cycle is started after each external cycle when the M1 (instruction fetch) status line is high. In default refresh, a counter composed of U1 and U2 times out 16 usec after the last refresh cycle and starts a refresh cycle. The counter is cleared by any refresh cycle so that while instruction fetch cycles are being executed, the default mode never occurs.

It is possible for a default refresh cycle to conflict with an external cycle request. For this reason, arbitration circuitry has been included on the board. During and for a short time after the pSYNC pulse, the arbitration can fail because of the ready set up time requirements of the processor. For this reason, the counter composed of U1 and U2 is disabled by gate U8 p3 for this time period.

FIGURE 16



3.5 External Cycle

Before starting an external read or write cycle, the memory board requires a stable address on the S-100 bus. In order to maximize the memory access time, the memory board's cycle should be started soon after the address becomes stable. However, the address lines stabilize at different times for different processors. Therefore, to optimize memory access times for different processor types, several jumpers are provided for the user to select the best trigger points. A list of the different trigger points and their associated jumpers follows. Refer to the Jumper Section for a detailed explanation of the jumper functions.

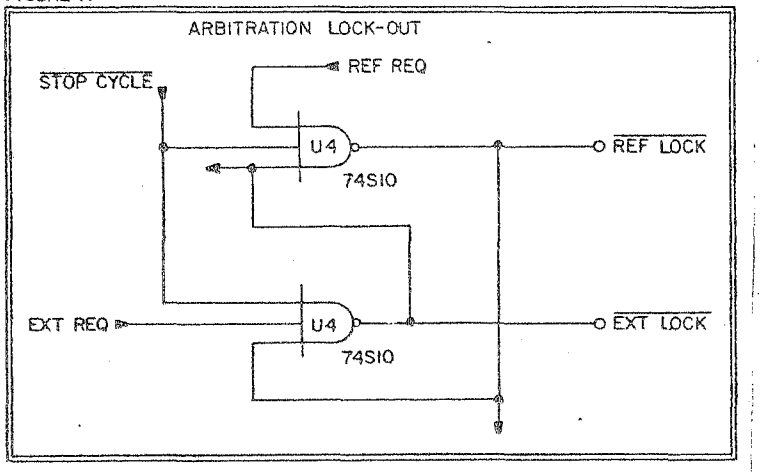
M1 Lookahead trigger	J6, J10
Front Panel Deposit trigger	J20
MWRITE trigger	J5
pSYNCH trigger	J8, J14

The triggers can be generated by a CPU, DMA device, or a front panel. The various trigger signals are latched by a flip flop to produce the External Cycle Request signal on p9 of U3.

3.6 External-Refresh Request Arbitration

The External Cycle Request signal and the onboard generated Refresh Cycle Request signal are input into a gated set-reset lock-out circuit composed of two sections of IC U4. This circuit acts as an arbitrator that allows only one of the cycle request signals to pass through to the delay line timing circuitry. The earliest cycle request signal will win the arbitration. The arbitration circuit will remain locked in that state until a Stop Cycle signal clears it. If the External Cycle Request signal wins an arbitration, the External Lock signal is set low and the next refresh cycle is delayed. If the Refresh Cycle Request signal wins an arbitration, the Refresh Lock signal is set low and the external cycle is delayed while the refresh occurs. The S-100 bus master is placed into a wait state until it can be serviced.

FIGURE 17

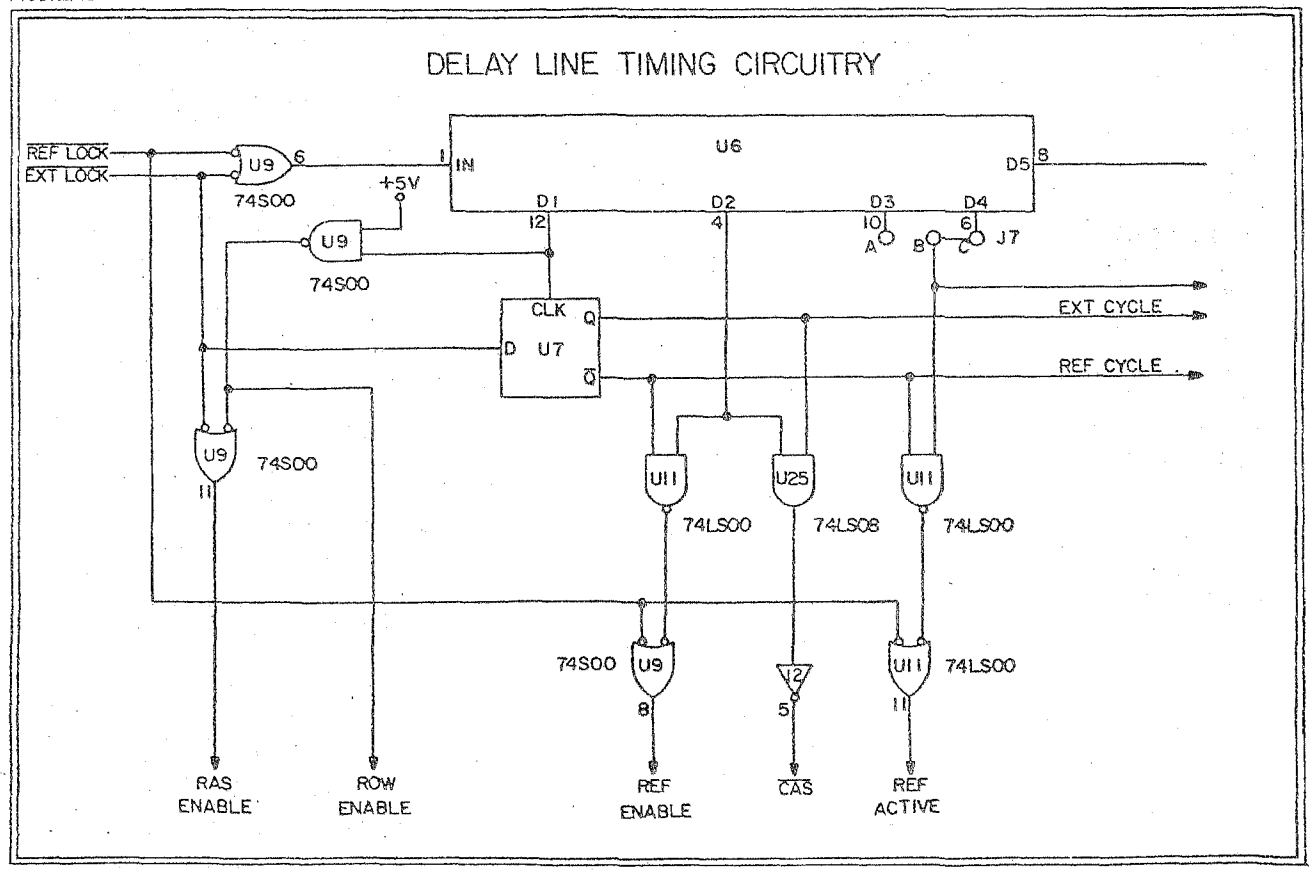


The $\overline{\text{Stop Cycle}}$, $\overline{\text{Ref Lock}}$, and $\overline{\text{Ext Lock}}$ signals are normally high and Ref. Req and Ext Req are normally low. When one of the Req signals goes active high, the corresponding Lock signal goes low. This prevents the other $\overline{\text{Lock}}$ signal from going low.

.7 Delay Timing Circuitry

he $\overline{\text{Ref}}$ $\overline{\text{Lock}}$ and $\overline{\text{Ext}}$ $\overline{\text{Lock}}$ outputs of the arbitration circuit are ORed ogether and input to the delay line, U6 pl. The delay line has five utputs at 35, 60, 150, 175, 235 ns. The delayed leading edge of the input ignal is used to generate the $\overline{\text{Stop}}$ cycle signal which gates off the rbitration circuit. This allows the delay line to define the negative edge f its input pulse. Thus a positive pulse with a well-defined length ppears at each delay line tap shifted in time by the delay at each tap. hese pulses, identified by the tap number, and the $\overline{\text{Ref}}$ $\overline{\text{Lock}}$ and $\overline{\text{Ext}}$ Lock ignals, are gated together to produce the control signals for the RAM rray.

FIGURE 18



The control signals' functions and generation are presented in the following list, in chronological order:

RAS Enable = $\overline{\text{Ext}}$ $\overline{\text{Lock}}$ + Row Enable

During an external cycle, RAS Enable goes active high one Schottky gate delay after arbitration. During a refresh cycle, RAS Enable goes active three Schottky gate delays plus a 35 ns delay after arbitration. The additional time during refresh is used to establish a stable refresh address. The RAS Enable signal is used to enable the 74S00 gates that drive the RAS signal.

$$\text{Refresh Enable} = \overline{\text{Ref}}\ \overline{\text{Lock}} + \overline{\text{D2.Ref Cycle}}$$

During a refresh cycle the Refresh Enable signal goes active high one Schottky gate delay after arbitration. It stays active until after $\overline{\text{RAS}}$ goes inactive. The Refresh Enable signal drives all of the RAS select lines active high through U15 and causes the address multiplexers in U13 to output the refresh address.

$$\text{Refresh Active} = \overline{\text{Ref Lock}} + \overline{\text{D4.Ref Cycle}}$$

Refresh Active identifies when a refresh cycle is active. It goes active high one LS gate delay after arbitration and goes low as the $\overline{\text{Stop}}$ $\overline{\text{Cycle}}$ signal to the arbitration flip flop ends. If the $\overline{\text{Ext}}$ $\overline{\text{Lock}}$ signal goes active low while the Refresh Active signal is active high, then the Q output of flop flop U18 will be set active high. This will place the current bus master into a wait state if the memory board is selected. The wait state will last until the external cycle is serviced.

D1

D1 is a positive pulse at the first tap of the delay line. It is delayed 35 ns from the Input. D1 is inverted to produce Row Enable. D1 is also used to clock flip flop U7. U7 produces two status signals, Ext Cycle and Ref Cycle, which indicate the current cycle type.

$$\text{Row Enable} = \overline{\text{D1}}$$

Row Enable is used to drive the address multiplexers in U13. Row Enable is normally held high. When it goes low the column address is multiplexed into the memory array unless the Refresh Enable signal is active high. The Refresh Enable input overrides the state of the Row Enable signal.

$$\text{Ext Cycle} = \overline{\text{Ref Cycle}}$$

These status signals latch the condition of the arbitration flip flop at the beginning of the D1 pulse.

D2

D2 is a positive pulse at the second tap of the delay line. It is delayed 60 ns from the input. During an External Cycle, D2 is used to generate the $\overline{\text{CAS}}$ pulse and control the data latches U20, U30 and U31. The latches store data at the end of the D2 pulse. During a Refresh Cycle, D2 is used to keep the Refresh Enable signal active until the RAS goes inactive.

$\overline{CAS}$ = $\overline{D4.Ext\ Cycle}$: Column Address Strobe

ıe column address is strobed into the memory chips on the falling edge of ıe $\overline{CAS}$ pulse. $\overline{CAS}$ is gated off during a Refresh Cycle. U26, a 74LS75, is ıtched during $\overline{CAS}$. This prevents noise on the bus from propagating through ıe memory board circuitry.

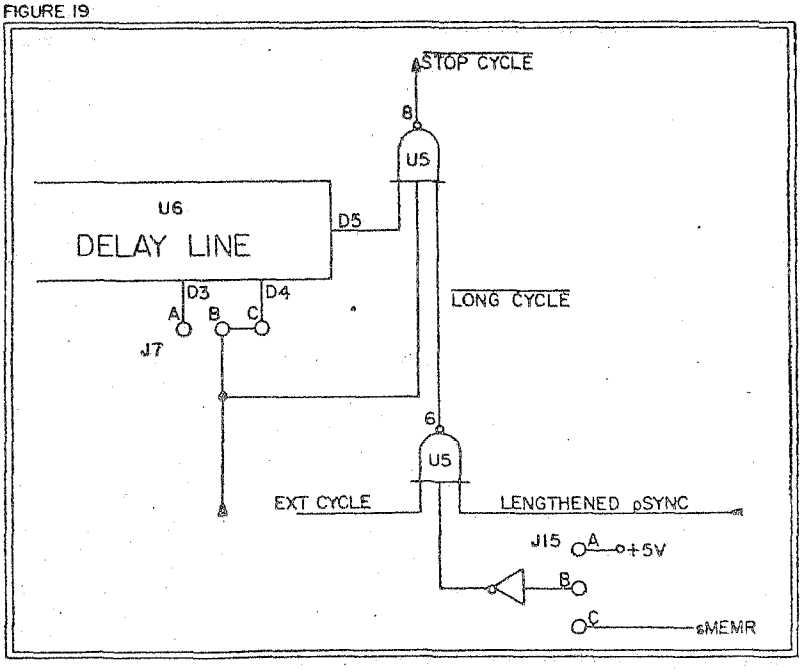
D3-D4

ıe D3 or D4 tap is selected by jumper. Both are positive pulses that are ɛlayed by 150 ns and 175 ns respectively from the input. The selected ignal defines the length of the $\overline{Stop\ Cycle}$ signal which clears the rbitration flip flop.

D5

he D5 tap is a positive pulse that is delayed 235 ns from the input. A elay line timing cycle can be either a long cycle or a short cycle. Only on-memory read cycles can be long cycles. During a short cycle, the D5 ignal defines the start of the $\overline{Stop\ Cycle}$ signal.

FIGURE 19



$\overline{Stop\ Cycle}$ = D4.D5.$\overline{Long\ Cycle}$

The Stop Cycle signal is used to clear the arbitration flip flop, to set the Refresh Request active high after an external cycle during an S-100 M1 cycle, and to set the Refresh Request low after a refresh cycle. During a short cycle, $\overline{Long\ Cycle}$ is always high. $\overline{Stop\ Cycle}$ goes active low as soon as D4 and D5 go high. This clears the arbitration flip flop and the delay line input then goes low. After the D4 delay time, the D4 signal goes low

and this drives $\overline{\text{Stop Cycle}}$ high. The arbitration flip flop is now released and a new cycle can start. The $\overline{\text{Stop Cycle}}$ pulse width provides the minimum RAS precharge time needed by the memory chips.

A $\overline{\text{Long cycle}}$ is created during a non-sMEMR external cycle if J15:B-C is closed. The Shifted pSYNC signal goes active high at the start of pSYNC and stays high until the rising or falling (J10) edge of $\phi 2$. $\overline{\text{Long Cycle}}$ goes active low while Shifted pSYNC is high and holds off the start of $\overline{\text{Stop Cycle}}$. Once $\overline{\text{Stop cycle}}$ goes active low it is terminated in the normal manner and has the same pulse width as a short cycle. The $\overline{\text{long cycle}}$ is used to extend the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths so that they overlap the processor write strobe. This feature is only used when write cycles are triggered during pSYNC and not when cycles are triggered by the MWRITE signal.

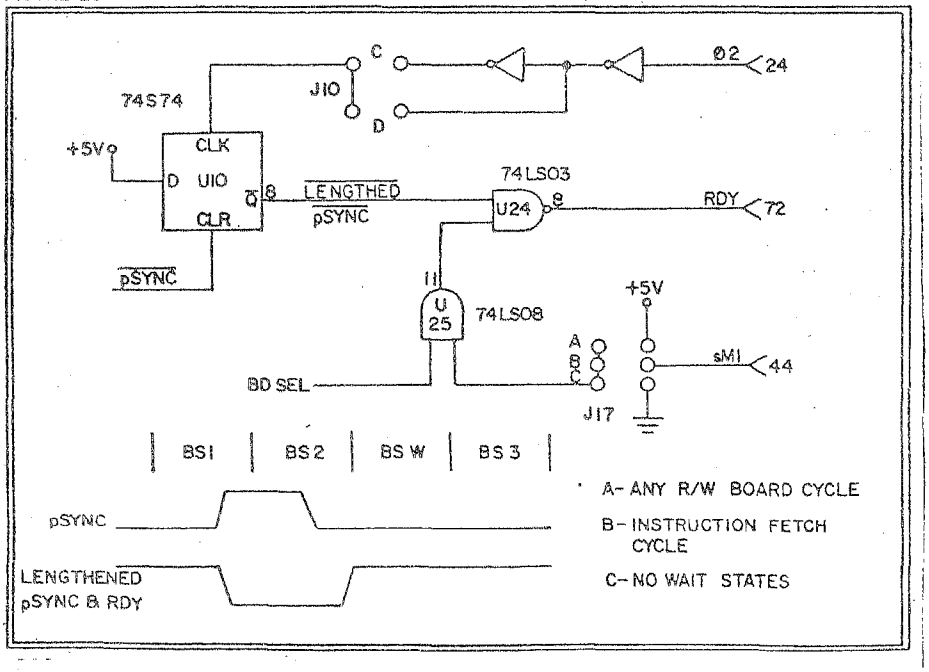
$$\overline{\text{External Clear}} = \overline{\overline{\text{Stop Cycle}}}.\text{External Cycle}$$

$\overline{\text{External Clear}}$ is used to clear the External Request flip flops and the wait request flip flop, U10 p4. It is also inverted and used to set the Refresh Request line to active high during an M1 cycle. This causes a refresh cycle to follow every instruction fetch cycle. This produces the feature known as Transparent Refresh.

3.8 Wait State Generator

The onboard wait state generator can be jumpered to generate one wait state per instruction fetch (M1) or for every read or write board cycle. The generator is only enabled when the board is selected.

FIGURE 20

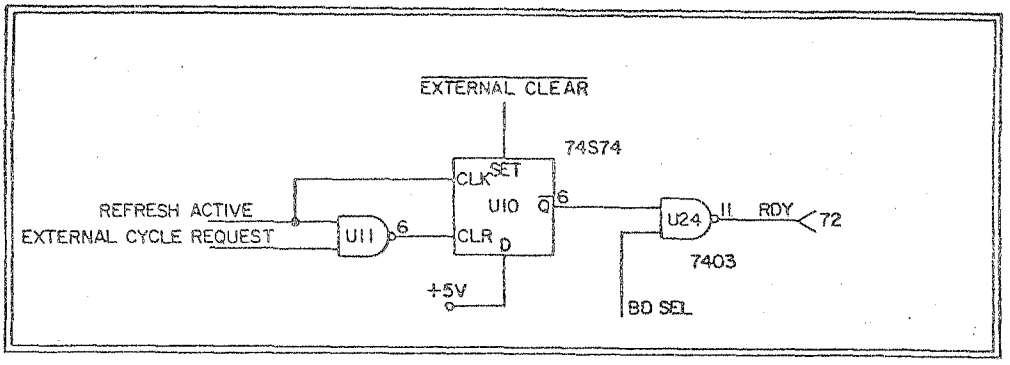


The flip flop U10 is used to assure that the RDY line will remain low during all of BS2. J10 should be jumpered so that U10 is clocked at the end of BS2 so that two wait states are not generated. J17 is jumpered to enable the desired type of wait state.

3.9 Conflict Resolver Circuit

The conflict resolver circuit is used to prevent errors when external and default refresh cycles occur simultaneously. If an external cycle request occurs during a refresh cycle (Refresh Active signal high), U11 p6 goes low, clearing the U10 flip flop, and U10 p6 goes active high. If the RAM board is selected, the RDY line goes low, placing the bus master in a wait state.

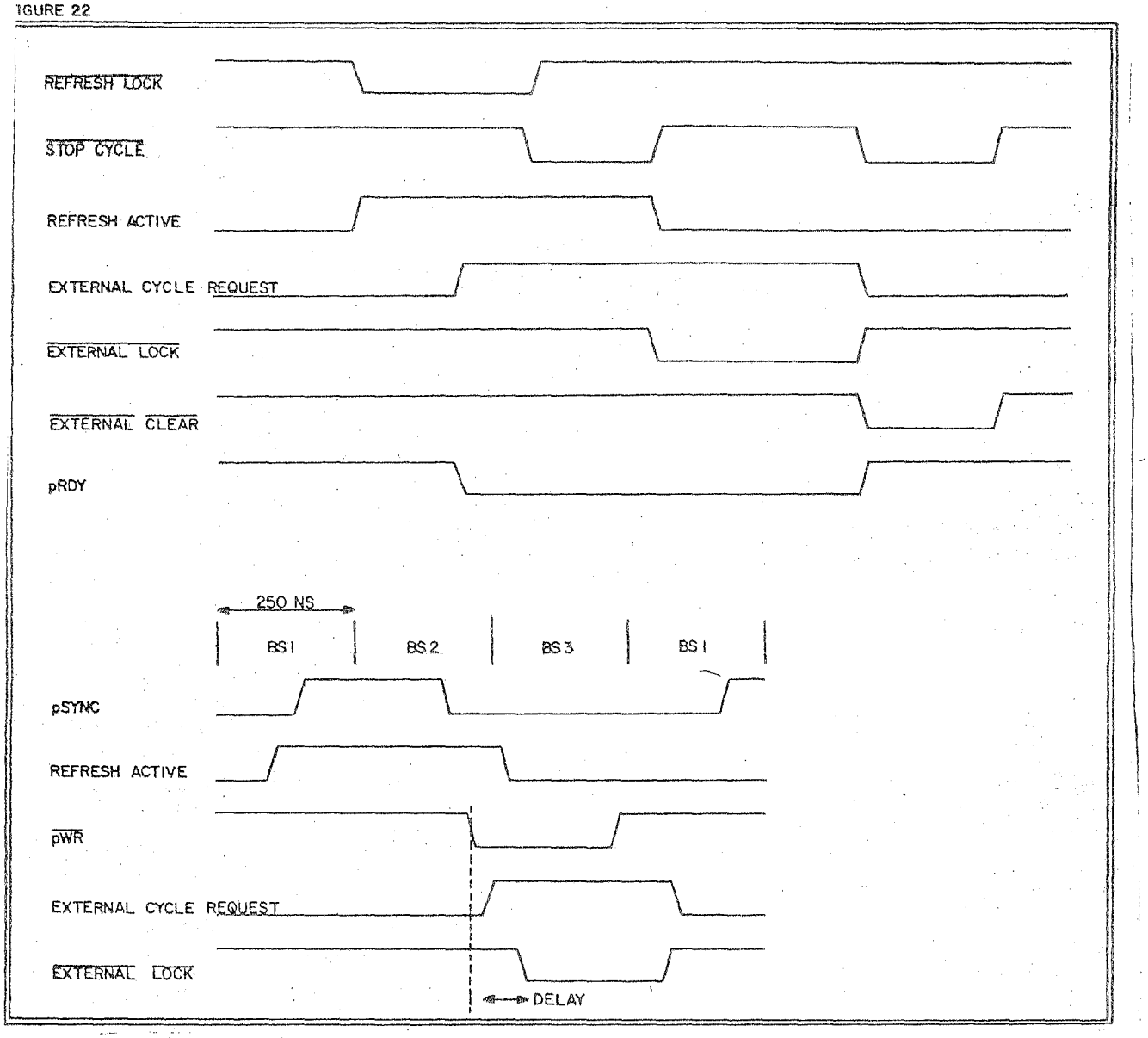
FIGURE 21



The bus master remains in the wait state while the refresh cycle is completed and the delayed external cycle is serviced. As the external cycle is termainted by External Clear, the U10 flip flop is set, driving its Q output low, removing the wait request. U10 is clocked by Refresh Active so that after power-up the flip flop will be clocked to the correct state.

This method will work as long as the RDY signal goes active early enough to place the processor or DMA controller into a wait state. If the External Cycle Request goes active after the RDY line is sampled and while the board is executing a refresh cycle, the external cycle will be delayed and an error can occur either during the present or the next external cycle. To prevent this from occurring, the count to a default refresh is gated off during and for a time after pSYNC by U8 p3 and the long cycle feature allows the board to be jumpered so that a write cycle can start during pSYNC instead of being triggered by MWRITE -MWRITE usually goes active after the RDY line is sampled. As an example, Figure 22 shows a write cycle being delayed because a refresh cycle had been triggered in the middle of the BS1 state. Note that in this case, the delay could be eliminated by clocking U1 on the edge of 02 that corresponds to the beginning of BS1. Note also that because the RAM board can be jumpered so that it executes external cycles when it is not selected (J11:A-B), a delayed and deselected external cycle can prevent the proper triggering of the next selected external cycle. A solution can be to change the trigger times, jumper J11:B-C, change the clock input to U1, or to add a wait state.

IGURE 22

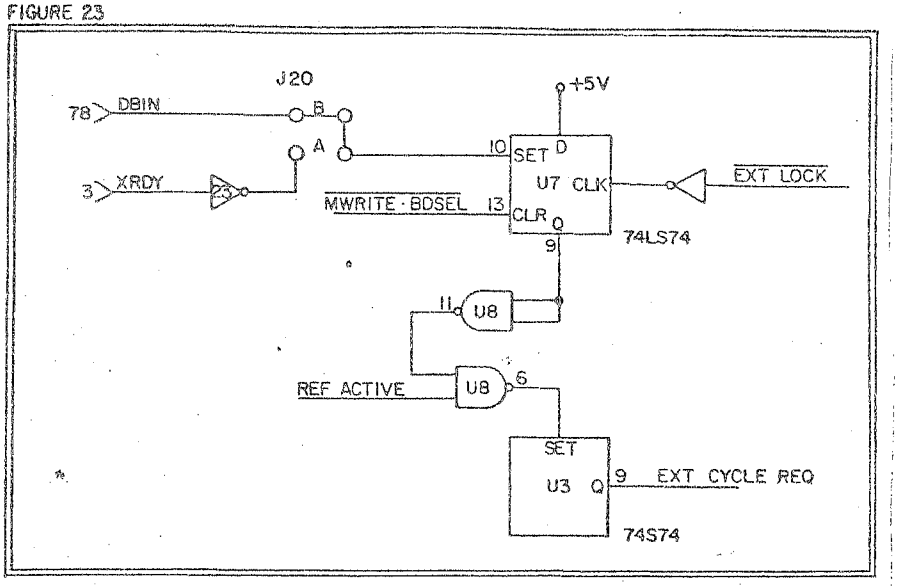


3.10 Front Panel Deposit

A front panel deposit normally consists of a read-write-read operation so that the user can see the contents of a memory location before and after the deposit. The first read is accomplished by latching the data from the previous cycle with U20, U30 and U31. The write operation requires special trigger circuitry on the RAM board because most front panels do not emulate processor write cycles. They often do not, for example, generate pSYNC

during a deposit. The second read operation also requires special circuitry to make the RAM board generate a read cycle after the MWRITE deposit pulse. The write-read cycles are generated and sequenced by the circuitry in Figure 23.

FIGURE 23



With J20:B shunted, U7 p9 normally stays high because the flip flop is set whenever DBIN is low. An MWRITE pulse due to a processor cycles does not clear the flip flop because DBIN remains low and the set input overrides the clear input. During a front panel deposit, however, DBIN stays high while MWRITE is active. This condition clears the flip flop and U7 p9 goes low. At the next refresh cycle, U8 p6 goes low. This sets the External Cycle request line active low and an External Cycle starts as soon as the refresh cycle is over. If MWRITE is still high, the External cycle will be a write cycle. One write cycle will occur for each refresh cycle during the MWRITE pulse. After the MWRITE pulse goes low, the U7 p9 Q output will remain active low until it is clocked high by one additional external cycle that is triggered after a refresh cycle. Since MWRITE is low, this last external cycle is a read cycle.

The actual deposit is a read-write-write...write-read sequence. This method assumes that DBIN stays high during the deposit and that the deposit MWRITE pulse is long compared to the default refresh rate (8 or 16 sec). It will work with Altair A, IMSAI, Cromemco, and InterSystems front panels. For DMA and other front panels, the J20:B-A position is provided to decode a front panel deposit as MWRITE.XRDY. also, if the DMA front panel emulates a processor's cycle, the RAM board's normal trigger circuitry should trigger a write cycle.

3.11 Repair

The following is a suggested sequence to follow to repair the board.

(1) If possible, use a memory test program to locate a bad memory chip or bad connection in the array. The memory test program should indicate the address and bad bit(s) of any byte or word that fails the test. The chip that is so indicated should be rocked in its socket and examined for bent-under pins. If necessary, the suspected chip should be replaced with another chip. If the replacement chip fails the memory test, use an oscilloscope to compare the pins of the suspected chip with another chip in the same bank. All of the signals and voltage levels should be the same except for the data in and out pins.

Refer to the board addressing section of this manual to locate the chip that corresponds to the address given by the memory test. The right-most chip in each bank is the least significant bit. The left-most chip is the most significant bit.

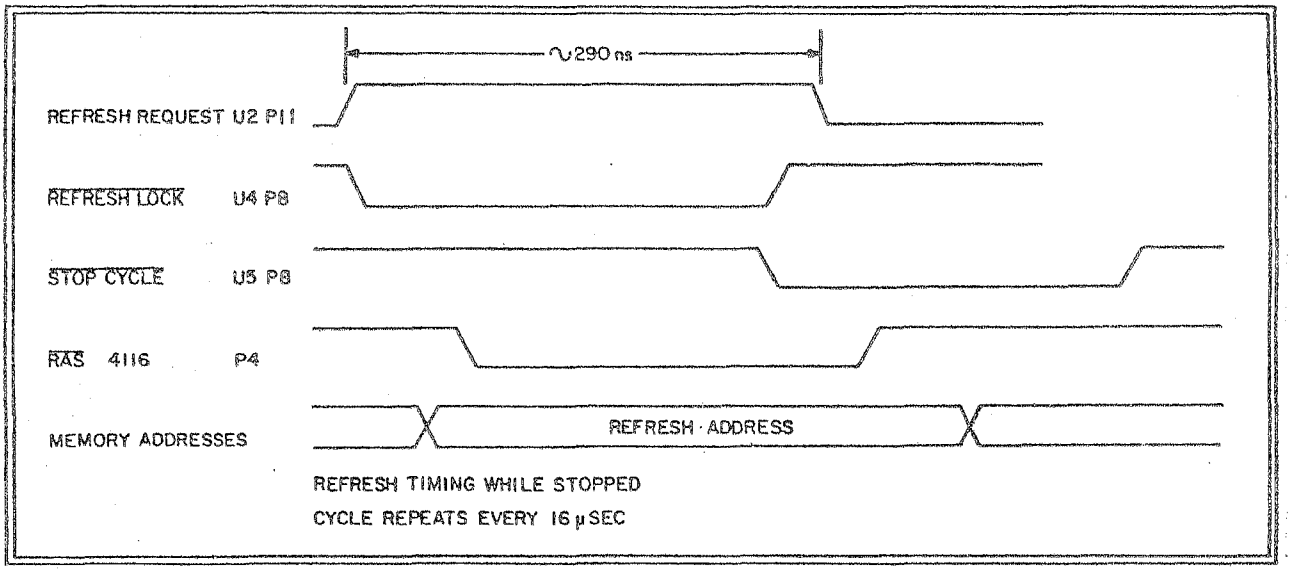
(2) If a memory test cannot be run, or if it reports errors in many chips, then it is likely that there is a timing error in the board. First check out simple things like the alignment of the memory board in the S-100 connector, the power supply voltages, the jumper and switch settings, and the integrated circuits for proper type, orientation, and bent-under pins.

(3) Try adding a wait state by closing jumper J17:A. Data access time from a trigger, using tRAC = 200 ns memory, is approximately 250 ns. If the memory board will only work with the wait state, then either the jumpers that select the trigger timing are set improperly or the processor board does not allow enough access time.

(4) With the computer in Stop mode, use an oscilloscope to check the refresh operation. There should be a 1/4 microsecond negative going RAS pulse every 16 microseconds on pin 4 of all of the memory chips. Pin 15, CAS, should be high. The refresh address count transitions should be apparent on each address line. The address transitions should occur approximately 30 ns before and after the RAS pulses.

If there are no RAS pulses, first check the counters U1 and U2. There should be a positive pulse, Refresh Request, of approximately 300 ns every 16 microseconds at U2 p11. Since there shouldn't be any external cycle requests while the computer is stopped, the Refresh Request signal will immediately win an arbitration. Therefore, the Ref Lock signal, U4 p8, should go low soon after Refresh Request goes high.

FIGURE 24



If none of these pulses are present, check to see if the Stop Cycle signal is being generated at U5 p8. The following tests require an InterSystems front panel.

(5) Close the Continuous NOP switch on the front panel. Trigger your oscilloscope on the positive edge of pSYNC. With all positions of SW1 closed, and using Transparent Refresh, 8-bit operation, you should see:

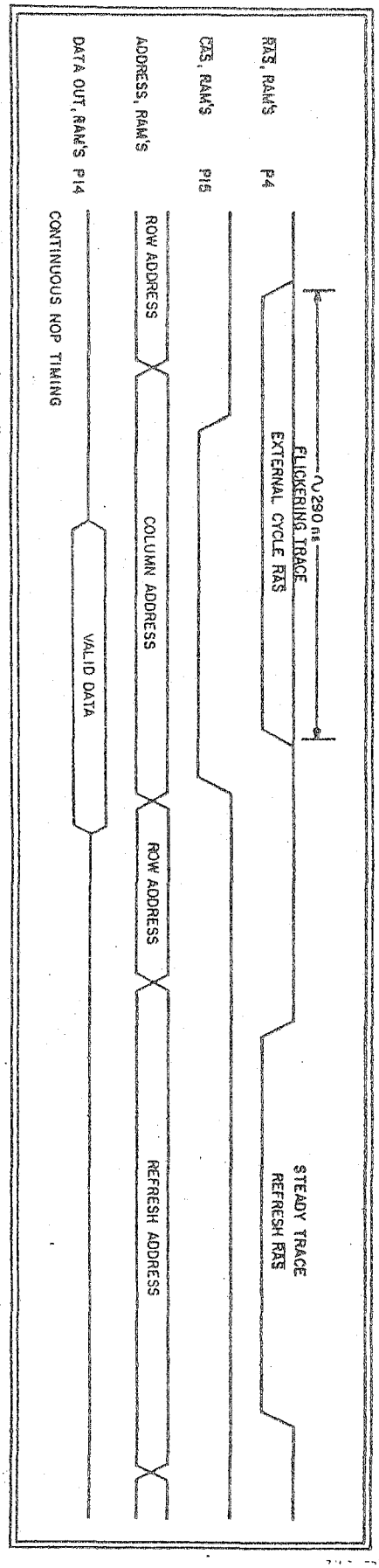

RAS, RAM'S
P4
CAS, RAM'S
P15
ADDRESS, RAM'S
DATA OUT, RAM'S P14
CONTINUOUS NOP TIMING
~290 ns
FLICKERING TRACE
EXTERNAL CYCLE RAS
STEADY TRACE
REFRESH RAS
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
REFRESH ADDRESS
VALID DATA

FIGURE 25

Check for address signals that are between 0.8V and 2.7V (shorted TTL drivers) or that never change (3242 outputs shorted to a power or grd bus).

There are two types of $\overline{RAS}$ pulses displayed. The longer 290 ns pulse is due to an external read cycle and flickers because an external cycle $\overline{RAS}$ is only gated to a decoded RAM bank. The shorter 250 ns $\overline{RAS}$ pulse is due to a Transparent Refresh cycle and doesn't flicker because it is gated to all banks.

If the external $\overline{RAS}$ pulse does not appear, see if U3 p9, External Request, is high. If not, check the external trigger, U3 p11. The external trigger waveform depends upon the jumpering used. If the M1 lookahead trigger is used (J6:B-C), then the external trigger signal should go high at the middle of T1 and stay high for 2 or 2.5 clock periods. If J6:A-B is made, then the external trigger should look like pSYNC (J8:A) or like pSYNC ANDed with one of the clocks: $\phi 1$, $\overline{\phi 1}$, $\phi 2$, $\overline{\phi 2}$ (J8:B,C,D,E). Make sure that the external trigger signal has only one rising edge per pSYNC pulse.

If the refresh $\overline{RAS}$ pulse does not appear, check pins 6 and 7 of U2. They should both be high after the external RAS pulse during an instruction fetch cycle. This condition sets the output of U2, Refresh Request, high. As soon as the $\overline{Stop\ Cycle}$ signal returns to high, the Refresh Request signal wins the arbitration and a refresh cycle starts.

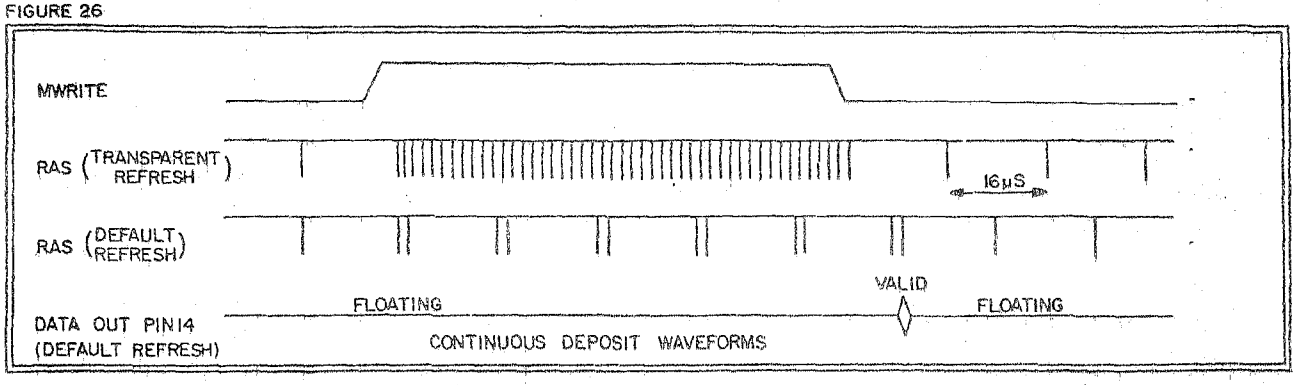
The data access time for an instruction fetch cycle can also be checked while the processor is continuously NOPing. Connect the vertical input of an oscilloscope to pin 14, Data Out, of any RAM chip. The output data pin can be seen to be floating until approximately 175 ns after the falling edge of the external RAS pulse. Then the output data will stabilize to either a 1 or 0 level. By comparing the start of valid data to the DBIN strobe, the data set-up time available to the processor can be measured.

(6) If all of the timing appears to be correct, but the memory still doesn't work, the board select, bank decoding and data lines should be checked.

Examine a memory location in a selected bank. The Board Select signal at U25 p8 should be high. Try to deposit various patterns into the memory. A front panel deposit causes the memory board to generate a write cycle after each refresh cycle during the MWRITE deposit pulse. The last write cycle is followed by a read cycle that latches the data that has just been written into RAM onto the output data latches. Either transparent or default refresh will occur during a front panel write.

Use the front panel Continuous Deposit function to produce a stable display on an oscilloscope.

FIGURE 26



Observe Data-In, pin 2, on a RAM chip in the selected bank. As the appropriate front panel data switch is raised or lowered, pin 2 (Data-In) should go to the same value during the last CAS pulse, and the value of pin 14 during CAS should be latched onto the bus by a 74LS373. If the correct data is on the RAM chip's pin 14, but is not on the bus, check the three latch enable lines.

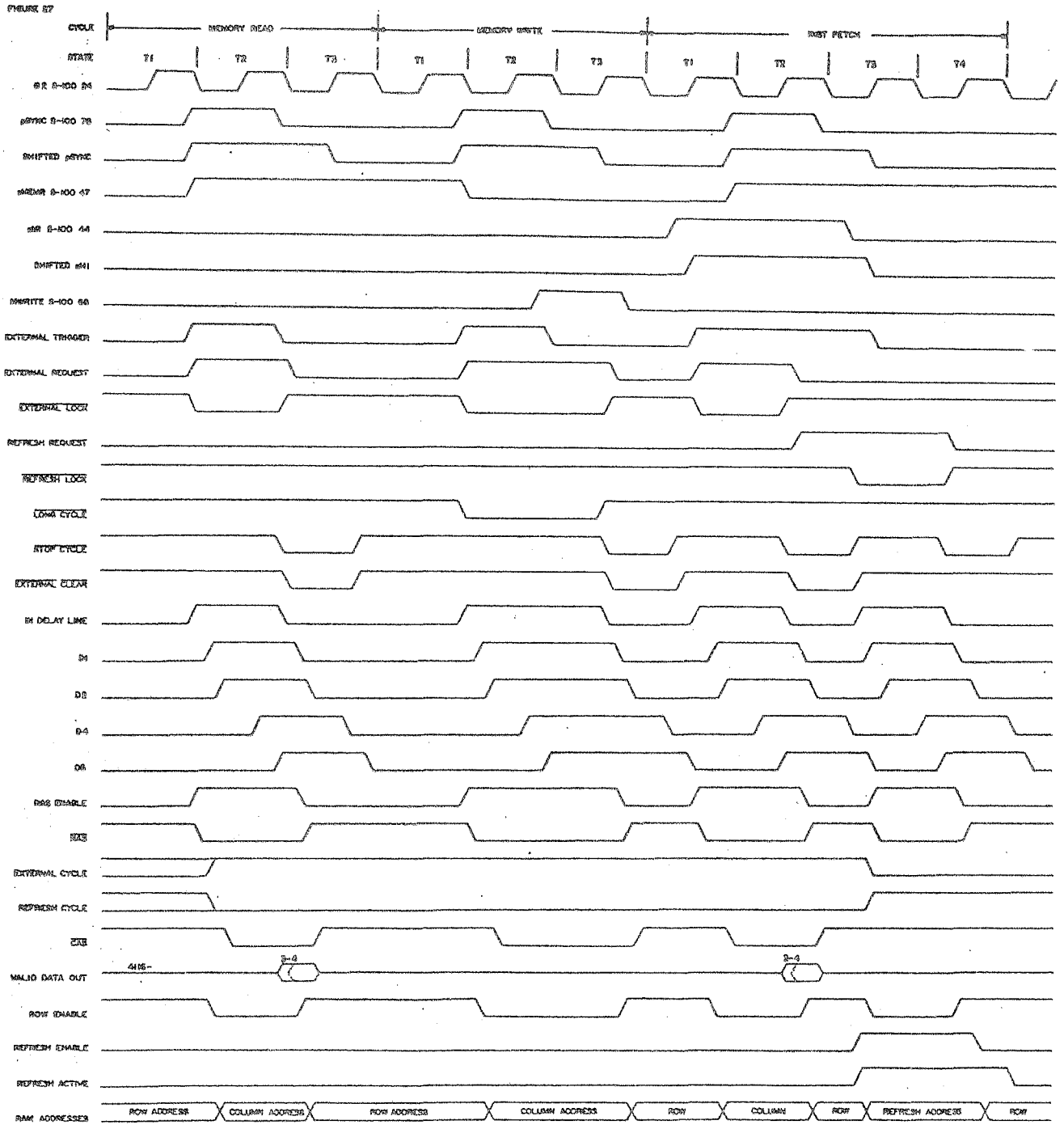
(7) Check the arbitration circuitry by disabling the transparent refresh (connect J2:B to ground). Run the following program starting at zero; C3, 00, 00. The S-100 RDY line (72) should occasionally go low, indicating that an arbitration is taking place. The number of arbitrations depends upon the type and speed of the processor. Note that the average time between arbitrations is greater than the refresh rate because some refresh cycles don't conflict with the external cycles.

(8) The RAM board arbitrates between refresh and external cycles. It does not arbitrate between external cycles. If the External Clear signal is active low due to the last cycle when a new cycle produces an External Trigger, then an error will occur. Check that U3 p13 is never low during a valid rising edge at U3 p11. There are two worst cases that should be checked.

Check the case of a long write cycle (J15:B-C) followed by an M1 cycle.

Check whether a deselected external cycle that has been delayed by a default request arbitration can prevent a proper trigger. See Section 3.9.

3.12 Timing Diagrams



5.0 Parts List and Replacement

Memory 4115 or 4116*

U1	74LS93
U2	74LS90
U3	74LS74
U4	74S10
U5	74S10
U6	Delay Line
U7	74LS74**
U8	74LS00
U9	74LS00
U10	74LS74
U11	74LS00
U12	74LS240
U13	3242
U14	74S00
U15	74LS158
U16	74LS00
U17	74LS20
U18	74LS157
U19	74LS157
U20	74LS373
U21	74LS10
U22	25LS2521
U23	74LS240
U24	7403
U25	74LS08
U26	74LS75
U27	74LS260
U28	74LS139
U29	74LS244
U30	74LS373
U31	74LS373

Q1	79L05
Q2	7812
Q3	7805
UR1	33-39 ohm, 7 Resistor DIP
UR2	33-39 ohm, 7 Resistor DIP
UR3	4700 ohm, 8 Resistor SIP
UR4	4700 ohm, 8 Resistor SIP
C2	1 uF dipped tantalum, 25v
C4	10 uF dipped tantalum, 10v
C5	10 uF dipped tantalum, 20v
C6	10 uF dipped tantalum, 10v
C9	10 uF dipped tantalum, 25v
C12	10 uF dipped tantalum, 25v

Other capacitors 0.1 uF, 25v bypass.

* Trac = 200 ns.

** Selected Part 26 ns. setup for pin 2,
15 ns. propagation delay from clock pin 3.

Appendicies

6.1 Warranty

6.2 A0 Polarity

ITHACA INTERSYSTEMS LIMITED WARRANTY

All equipment manufactured by ITHACA INTERSYSTEMS shall be guaranteed against defects in materials and workmanship for a period of ninety (90) days from date of delivery to the Buyer by the Seller, and the Seller agrees to repair or replace, at its sole option, any part which proves to be defective and attributable to any defect in materials or workmanship.

EXCEPT FOR THE WARRANTIES THAT THE GOODS ARE MADE IN A WORKMANLIKE MANNER AND IN ACCORDANCE WITH THE SPECIFICATIONS SUPPLIED, SELLER MAKES NO WARRANTY EXPRESS OR IMPLIED, AND ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE WHICH EXCEEDS THE FOREGOING WARRANTY IS HEREBY DISCLAIMED BY SELLER AND EXCLUDED FROM ANY AGREEMENT.

Buyer expressly waives its rights to any consequential damages, loss or expense arising in connection with the use of or the inability to use its goods for any purpose whatsoever.

No warranty shall be applicable to any damages arising out of any act of the Buyer, his employees, agents, patrons or other persons.

In the event that a unit proves to be defective, and after authorization by Seller, the defective part and/or unit, as authorized, must be securely packaged and returned Freight Prepaid by the Buyer to ITHACA INTERSYSTEMS for repair. Upon receipt of the unit, ITHACA INTERSYSTEMS will repair or replace, at its sole option, the defective part or product and return such part/product Freight Prepaid to the Buyer.

The remedies set forth herein are exclusive and the liability of Seller to any contract or sale or anything done in connection therewith, whether in contract, in tort, under any warranty, or otherwise, shall not, except as expressly provided herein, exceed the price of the equipment or part on which said liability is based.

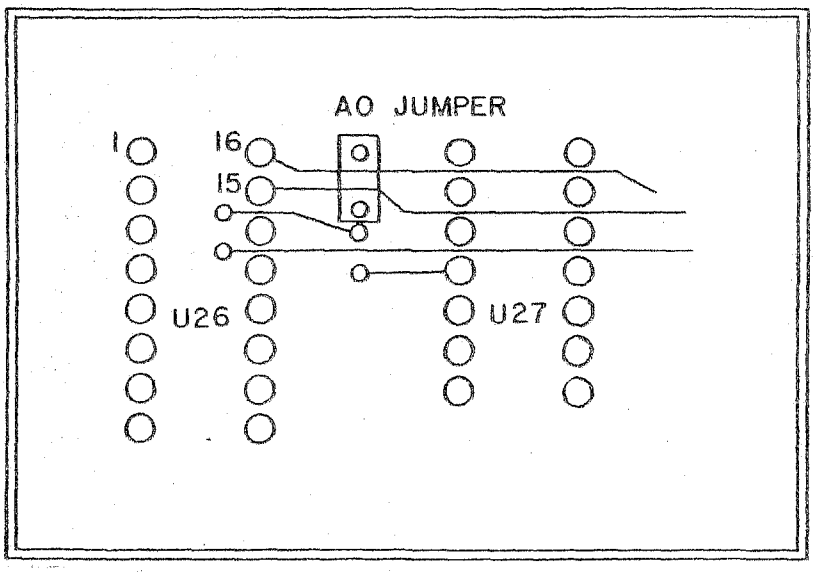
This warranty is given solely to the original Buyer. No employee or representative of Seller is authorized to change this warranty in any way or grant any other guaranty or warranty.

5.2 A0 Polarity

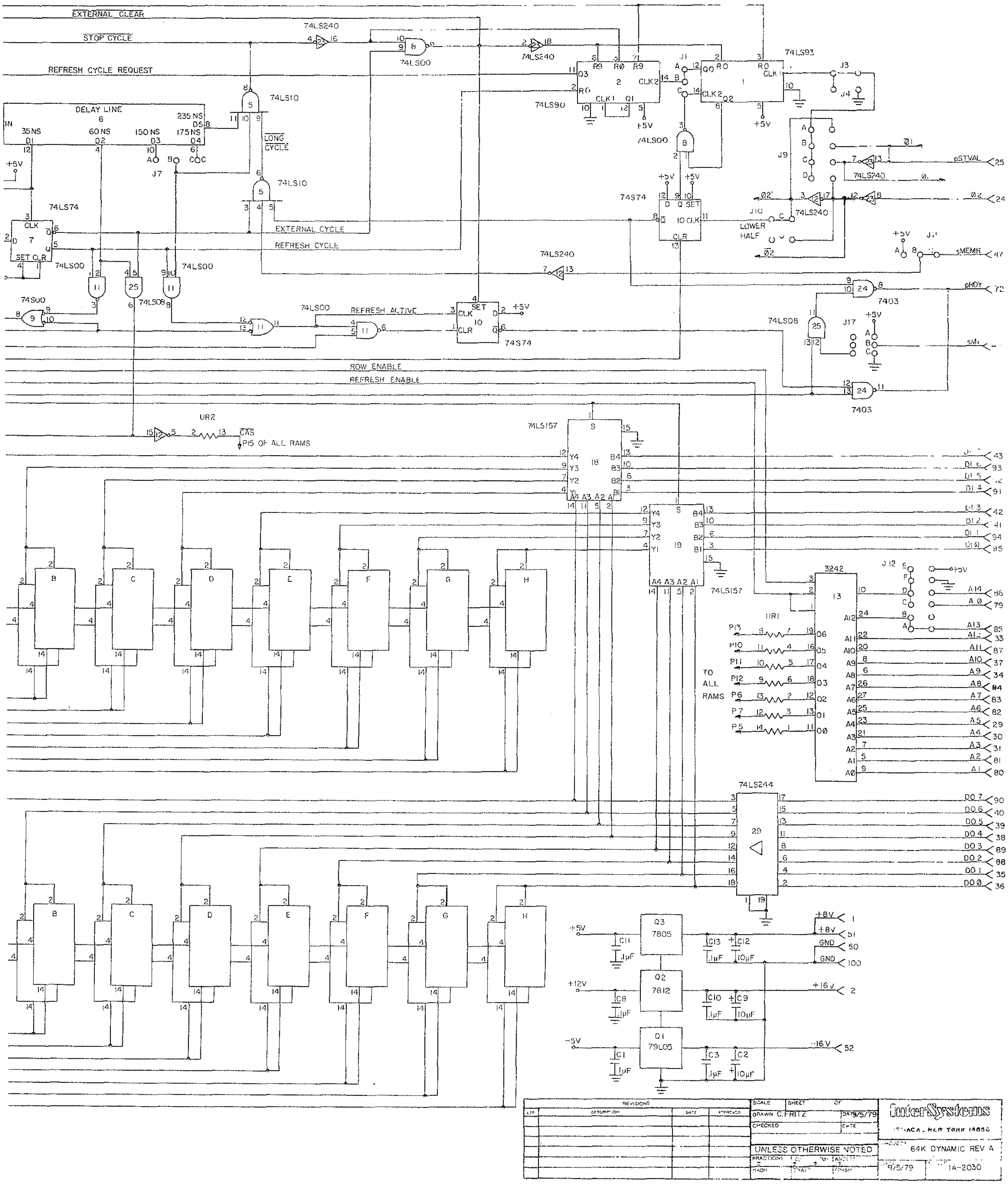
The current IEEE specification concerning which polarity of the A0 line selects which byte within an addressed word may change in the near future, and hence an unlabelled jumper has been included on the board which will change the polarity of the A0 line.

The jumper is located between ICs U26 and U27. See Figure 28. To make the change, cut the PC trace on the solder side of the board that goes from pin 15 of U26 to the upper plated-through hole of the jumper, then solder a short piece of wire to the upper and lower plated-through holes.

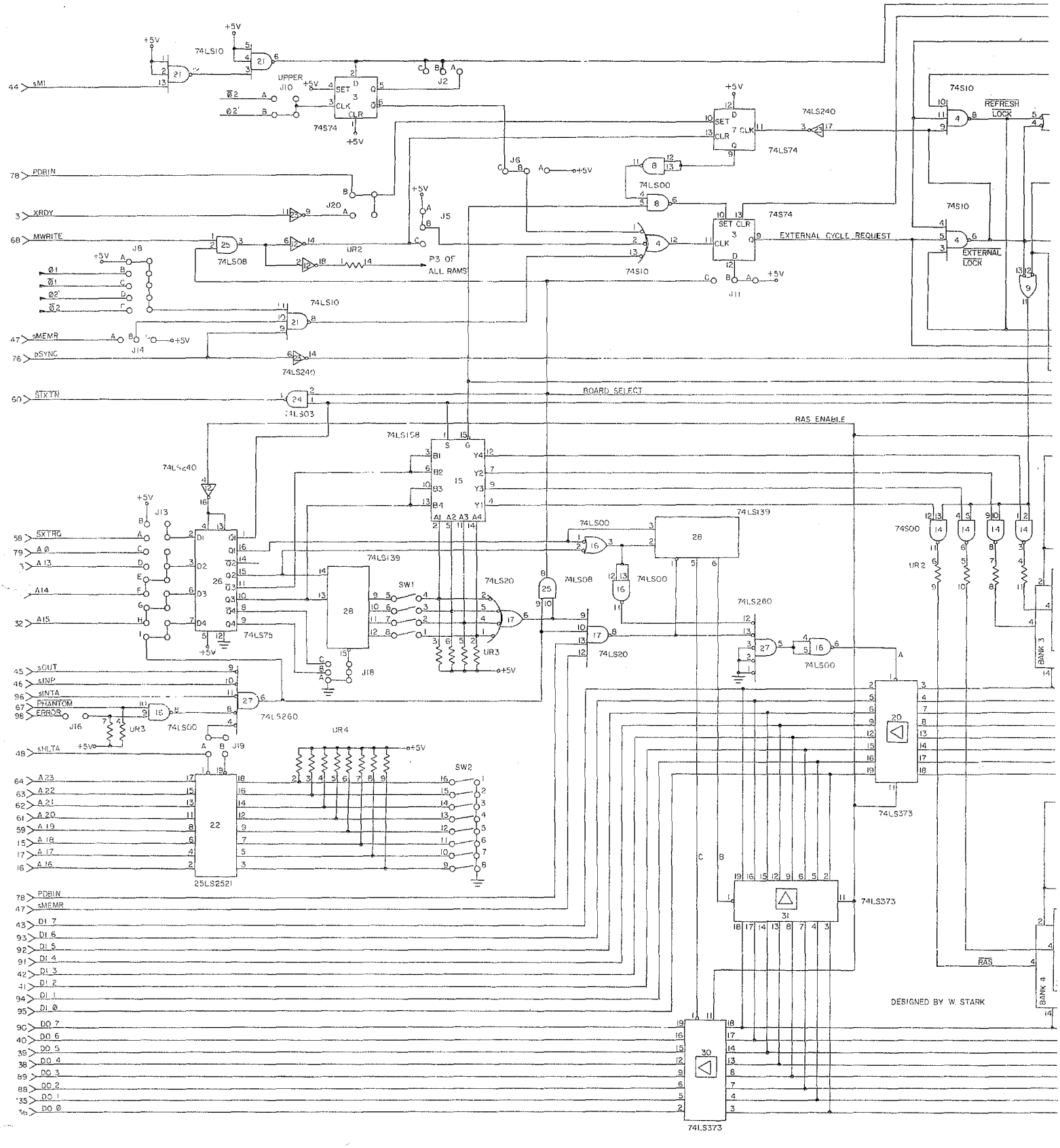
FIGURE 28



Note that the A0 specification is only important in systems that mix 8-bit and 16-bit transfers. This modification should only be made when A0 is selected (J13:C). Otherwise, while the board will still work, the bank ordering in Table I will be incorrect.



EXTERNAL CLEAR
STOP CYCLE
REFRESH CYCLE REQUEST
DELAY LINE
35 NS
60 NS
150 NS
175 NS
235 NS
LONG CYCLE
EXTERNAL CYCLE
REFRESH CYCLE
REFRESH ACTIVE
ROW ENABLE
REFRESH ENABLE
74LS240
74LS00
74LS10
74LS74
74LS08
74S00
74S74
74LS90
74LS93
74LS157
74LS244
7403
3242
LOWER HALF
pSTVAL
pRDY
sMEMR
CAS
P15 OF ALL RAMS
TO ALL RAMS
7805
7812
79L05
+5V
+12V
-5V
+8V
+16V
-16V
GND
InterSystems
ITHACA, NEW YORK 14850
REVISIONS
DRAWN C. FRITZ 9/5/79
CHECKED
UNLESS OTHERWISE NOTED
64K DYNAMIC REV A
9/5/79
1A-2030


74LS10
74LS74
74LS240
74LS00
74LS08
74LS04
74LS03
74LS158
74LS139
74LS20
74LS260
74LS75
74LS373
25LS2521
74S10
74S00
UPPER
REFRESH
LOCK
EXTERNAL
EXTERNAL CYCLE REQUEST
BOARD SELECT
RAS ENABLE
RAS
P3 OF
ALL RAMS
SW1
SW2
UR2
UR3
UR4
BANK 3
BANK 4
DESIGNED BY W. STARK
sM1
XRDY
MWRITE
PDBIN
sMEMR
pSYNC
sXTXTN
sXTRQ
A0
A13
A14
A15
sOUT
sINP
sINTA
PHANTOM
ERROR
sHLTA
A23
A22
A21
A20
A19
A18
A17
A16
DI 7
DI 6
DI 5
DI 4
DI 3
DI 2
DI 1
DI 0
DO 7
DO 6
DO 5
DO 4
DO 3
DO 2
DO 1
DO 0