THE ITHACA INTERSYSTEMS

256 KDR

QUARTER MEGABYTE DYNAMIC RAM BOARD
for the S-100 BUS

Edition 1

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1.0 INTRODUCTION AND GENERAL INFORMATION

The Ithaca Intersystems 256KDR memory board uses 64K dynamic RAM's to put a quarter megabyte of memory on a 5 by 10 inch board, conserving space and power in a mainframe. The 256KDR board is completely compatible with the IEEE 696 S-100 bus standard and supports both 8-bit (byte) and 16-bit (word) parallel data transfers.

This manual provides information about the general design and features of the memory board, instructions for configuring the board for specific installations, and the schematic drawing and parts list for the board.

1.1 256KDR FEATURES

The Intersystems 256KDR board features include:

* 64K Dynamic RAM chips. Seven bit refresh.

* Byte or word data transfer. Whether used with an 8-bit processor or a 16-bit processor, the board's data bus automatically adjusts to the needed word length. A 16-bit processor and an 8-bit DMA controller can be run concurrently on the same bus.

* Parity error checking. Parity is generated and checked during all read cycles and checked during write cycles if parity is generated by the bus master.

* Extended Addressing. The memory board is addressed in the extended 24-bit address space (16 megabytes).

* Arbitration and sequence logic. Continuous DMA transfers of any size and error free operation during waits, halts, or resets.

* High speed operation. The board is capable of 2 MHz, 4 MHz, or 6 MHz operation.

* Precise delay line timing. There are no one shots, oscillators, or RC delays.

* Operates with either the early or the late write strobe. No jumpering is needed.

* Uses both transparent and default refresh.

* Front panel compatibility.

* Phantom and Error. These S-100 lines assist in bootstrapping and memory protection.

* Wait state generator. One wait state may optionally be generated.

* Low power/low heat design. Low power means less drain on the power supply, higher reliability, and longer chip life.

* Simplified board setup procedure. The board has only four jumpers.

1.2 DATA TRANSFER ON THE S-100 BUS

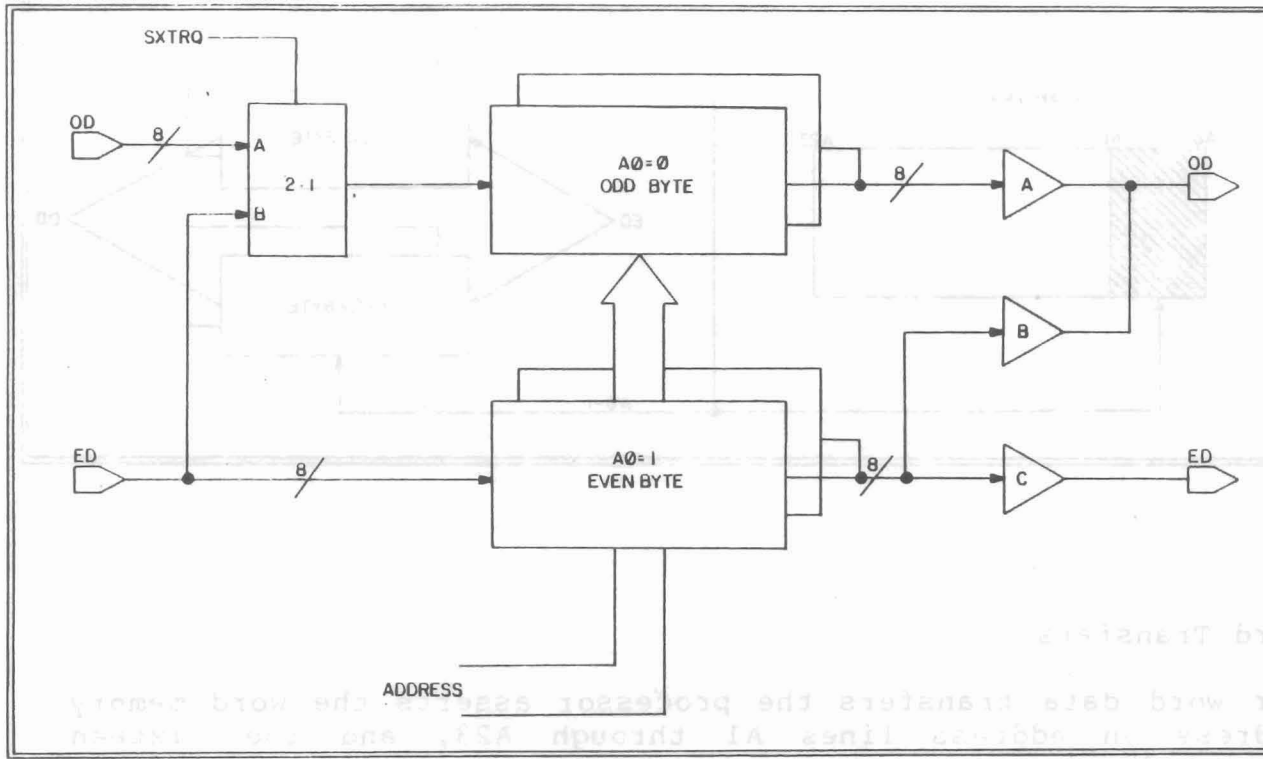
The S-100 data bus supports both 8-bit (byte) and 16-bit (word) parallel data transfers. For byte data transfers, the 16 data lines are grouped in two uni-directional 8-bit busses, the Odd Data (OD) bus for data going into the CPU, and the Even Data (ED) bus for data going into memory. For word data transfers, the two uni-directional busses are ganged to form a single 16-bit bi-directional bus.

A status line, called Sixteen Request (sSXTRQ), is assigned to control the grouping of the data lines. The line is asserted when a 16-bit processor requests a 16-bit data transfer on the bus. Eight bit processors do not assert this line and are, therefore, limited to 8-bit data transfers.

Memory Organization

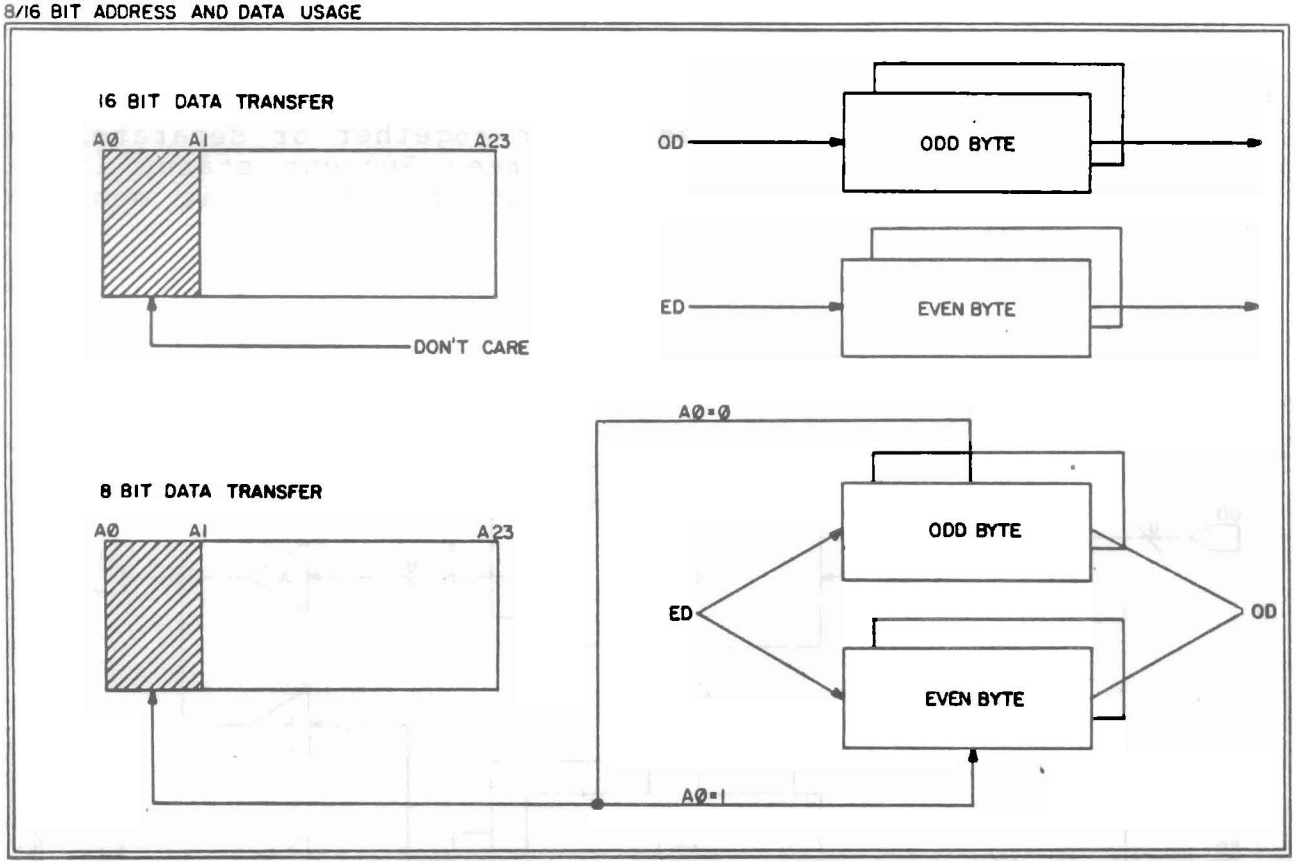
To be capable of both byte and word parallel transfers, memory is organized as four banks of 8-bit memory. Each bank contains 65,536 bytes of memory. Two banks are devoted to the Even Byte of the 16-bit word, and two banks are devoted to the Odd Byte. The banks are activated either together or separately, depending on the condition of the Sixteen Request status line and address line A0. Figure 1 illustrates the basic memory organization of the 256KDR board.

FIGURE 1
8/16 BIT MEMORY ORGANIZATION



Memory in S-100 bus systems is addressed as bytes. For byte memory transfers, the A0 bit determines which byte within an addressed word is selected. During 16-bit memory transfers the A0 bit is not considered because both bytes of the addressed word are transferred. Refer to Figure 2.

FIGURE 2
8/16 BIT ADDRESS AND DATA USAGE

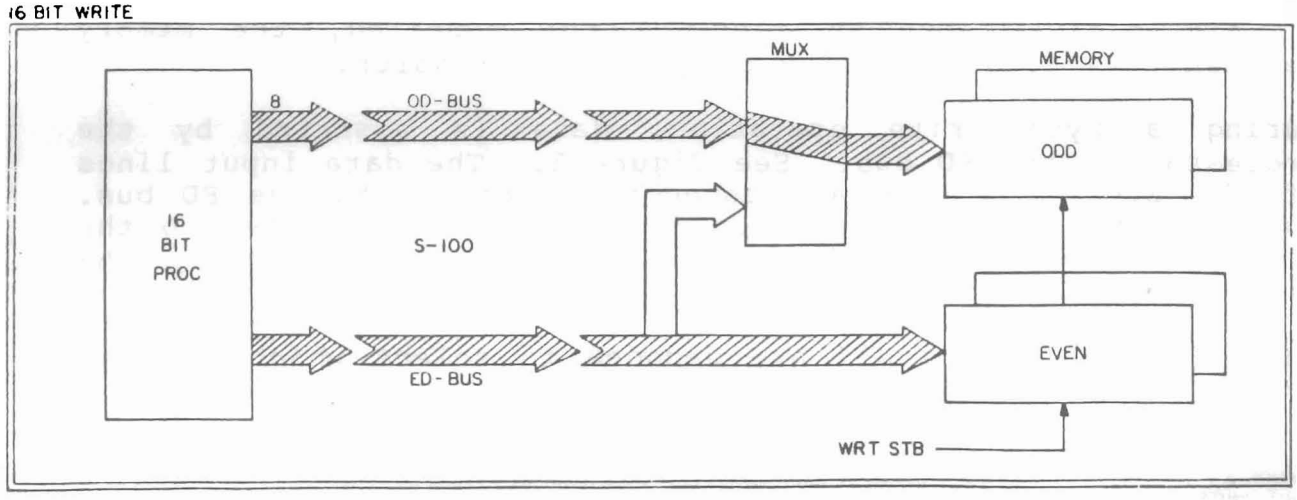


Word Transfers

For word data transfers the processor asserts the word memory address on address lines A1 through A23, and the Sixteen Request line.

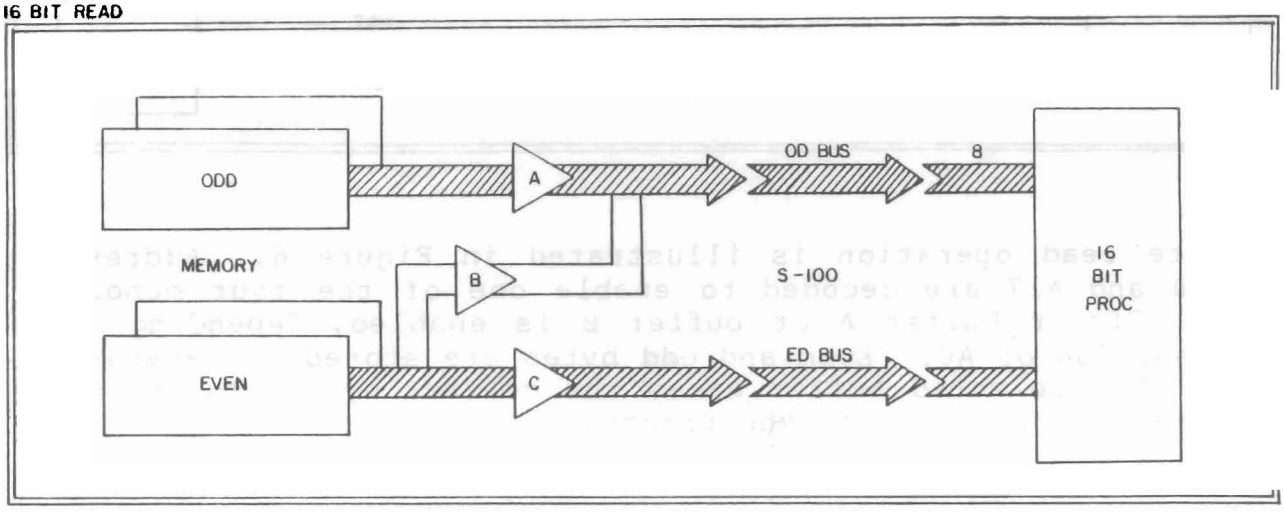
During a write operation, data is output on the 16 data lines by the processor. The Even Byte is routed to the Even Byte memory bank on the ED bus. The Odd Byte is routed to a 2-to-1 multiplexer on the OD bus. The 2-to-1 multiplexer is selected such that the Odd Byte is routed to the data input lines of the Odd Byte memory bank. The write strobe from the processor writes the data into both banks simultaneously. Refer to Figure 3.

16 BIT WRITE



During a read operation, data to be input to the processor is routed from the memory array banks to buffer-latches A and C (Figure 4) and then to the data lines during the read strobe. The Even Byte is routed on the ED bus and the Odd Byte is routed on the OD bus.

FIGURE 4
16 BIT READ



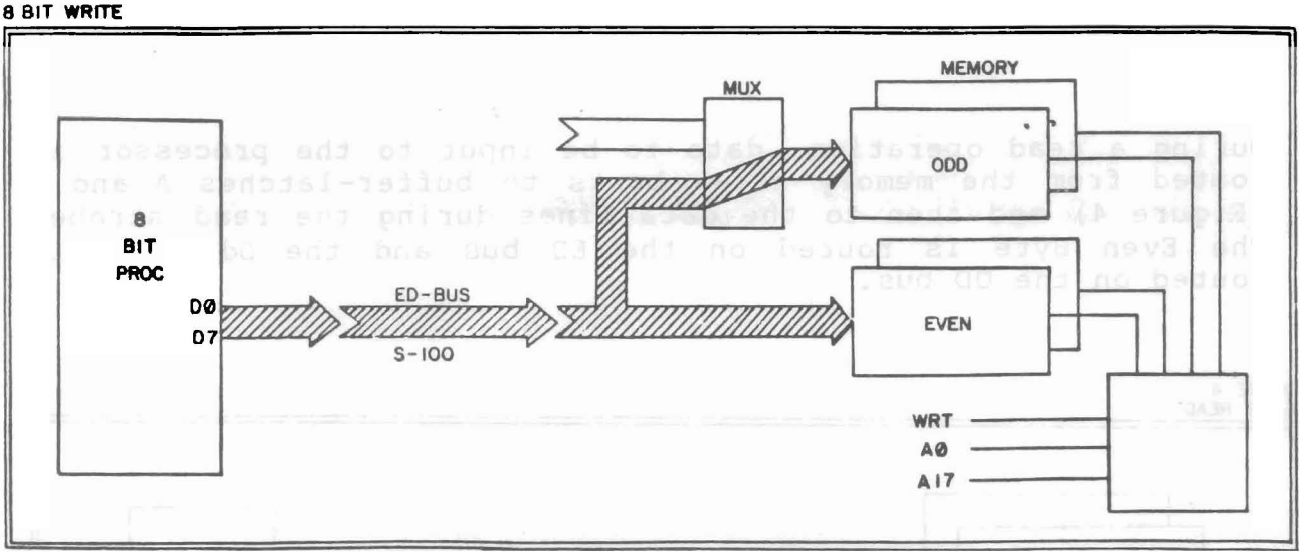
Byte Transfers

If the Sixteen Request line is not asserted, the memory reference is conducted as a single byte transfer.

During a byte write operation, data is asserted by the processor on the ED bus. See Figure 5. The data input lines of the Even Byte bank are connected directly to the ED bus. The data input lines of the Odd Byte bank are connected to the ED lines through the 2-to-1 multiplexer controlled by the Sixteen Request line.

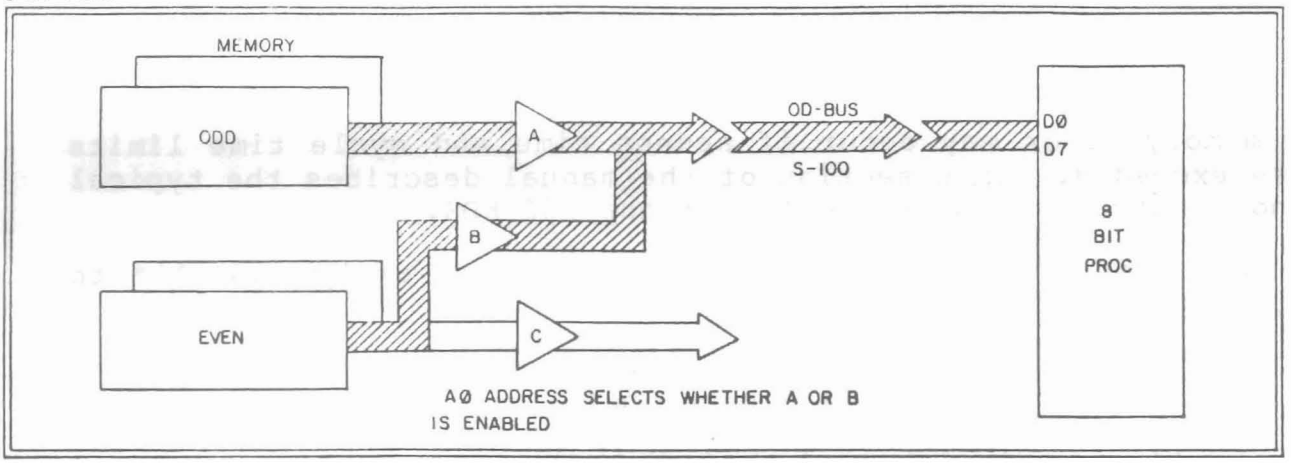
Address bits A0 and A17 are decoded to select which bank of memory is written to.

FIGURE 5
8 BIT WRITE



The byte read operation is illustrated in Figure 6. Address bits A0 and A17 are decoded to enable one of the four memory banks. Either buffer A or buffer B is enabled, depending on the condition of A0. Even and odd bytes are stored in separate banks. The selected buffer gates the correct byte onto the OD bus, where it is input by the processor.

FIGURE 6
8 BIT READ



1.3 BYTE AND WORD LOCATIONS

8/16 Bit Transfers

Banks 1 and 4: 0-131071 (128K) bytes
0-65535 words.

Banks 2 and 3: 131072 (128K)-262143 (256K) bytes
65536-131071 words.

Odd Bytes in banks 3, and 4, (see Figure 7 for bank locations).

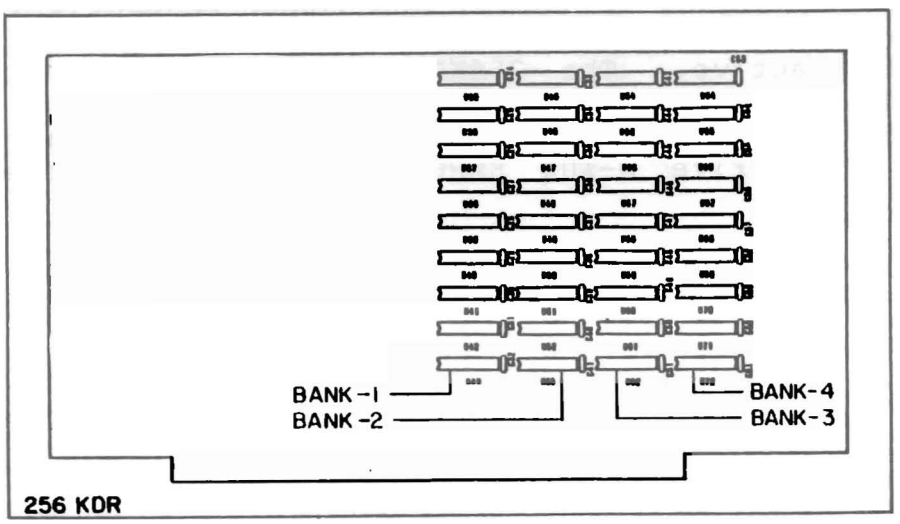


Figure 7 256 KDR memory organization

1.4 256 KDR CRITICAL TIMING

A memory error may occur if access time and cycle time limits are exceeded. This section of the manual describes the typical and worst case timing limits for the 256 KDR.

Access Time - Measured from the falling edge of bus pSTVAL* to bus data.

Typical	216 nanoseconds
Worst Case	274 nanoseconds

Cycle Time - Minimum time between external triggers that does not cause a memory error.

External to External Cycle Time

Typical	388 nanoseconds
Worst Case	417 nanoseconds

Transparent Refresh Cycle Time

Typical	661 nanoseconds
Worst Case	716 nanoseconds

1.5 PARITY

The 256KDR supports the Intersystems parity scheme: S-100 lines 65 and 66 are assigned to PARITY and PAREN* respectively. The PARITY line contains ODD parity when the device driving the bus drives PAREN* active. The 256KDR generates ODD parity and asserts PAREN* during all read cycles. Parity is checked during write cycles if parity is generated by the bus master. The 256KDR can drive S-100 ERROR* active in response to a detected error.

2.0 BOARD SETUP

This section of the manual describes how to prepare the memory board for operation, how to install the board, and what to do if the circuit board does not work properly.

2.1 SW1

SW1, an eight position DIP switch, is set to enable the operation of the 256KDR board in one of 64 possible 256K memory segments over a 16 megabyte address range. (All four RAM banks are decoded in the same 256K segment.)

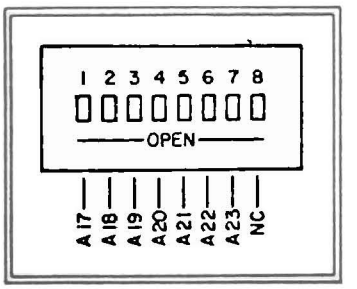


Figure 8 SW1

Switches SW1-2 through SW1-7 represent address bits A18 through A23 respectively of the starting binary address of the desired 256K segment. For example, the second 256K segment, 256K-511K, has a starting binary address of 000001. SW1-2 is opened, and SW1-3 through SW1-7 are closed. See Figure 8.

2.2 JUMPER CONFIGURATION SUMMARY

There are four jumper areas (refer to Figure 9) used to configure the 256KDR board for different processors. Each jumper area box contains a group of plated-through holes spaced 0.1" apart. To configure a jumper area, one connection per box is made between adjacent plated-through holes by a shunt that slides onto 0.040" square posts that are soldered in the holes. Possible connections within a jumper area are designated by letter names. The letter names run A, B, C,... from left to right or from top to bottom.

The following 256KDR jumper configurations are used to prepare the board to operate with Intersystems processors:

256KDR Jumpers	Z80 II (MPU-80)	Z80 III	Z8000 (MPU-8000)
J1	B-C	B-C	B-C
J2	A-B	A-B	A-B
J3	B-C	B-C	A-B
J4	B-C	B-C	B-C

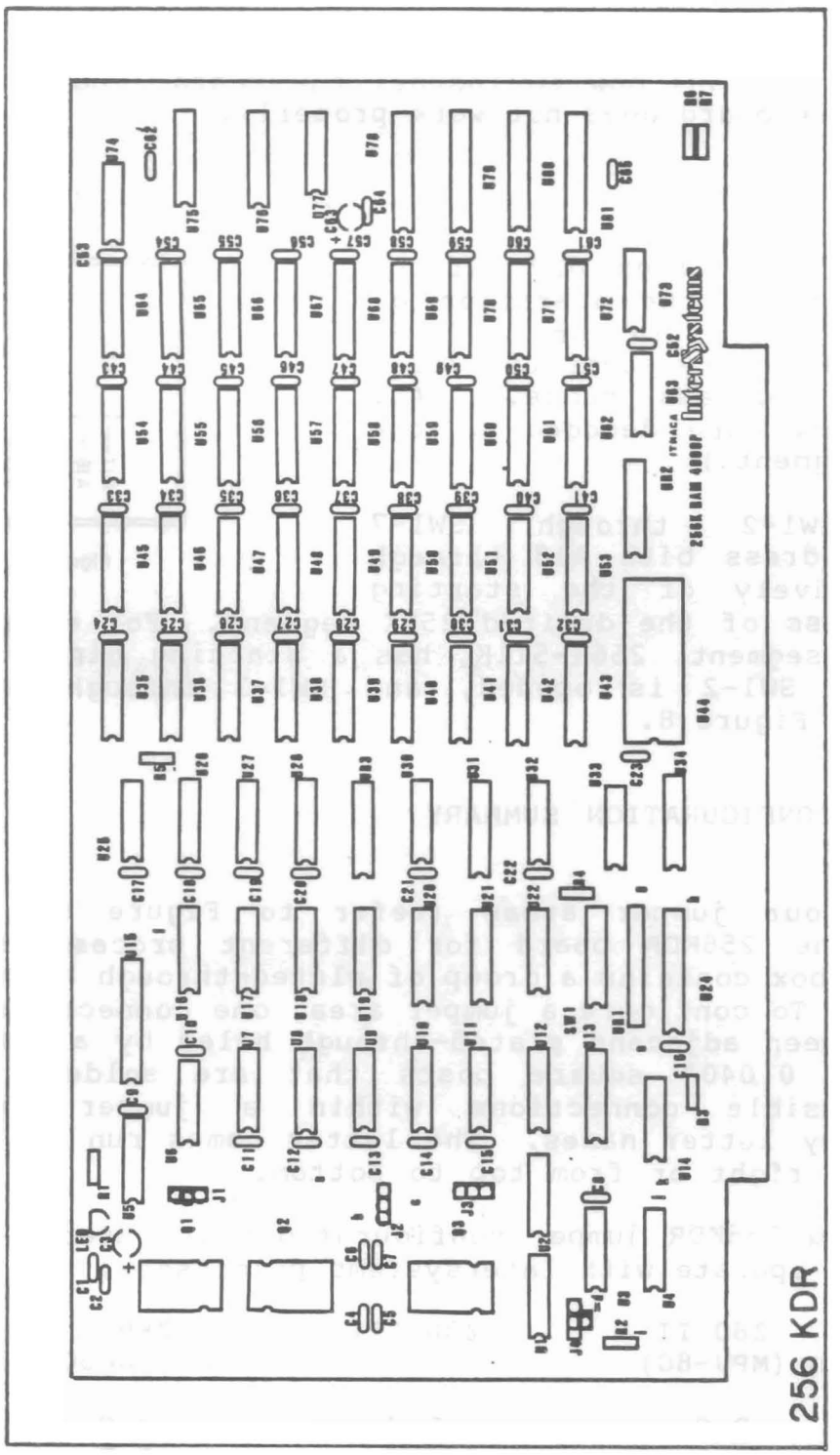
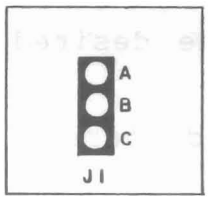


Figure 10 **256 KDR**

2.3 JUMPER REFERENCE

J1

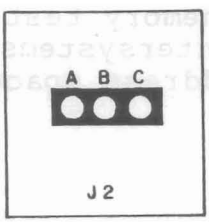


J1 selects the phase of bus clock Phi used to synchronize the input clock of refresh counter U2. Two clock edges are provided to prevent a default refresh request occurring at same time as the External Cycle Request (which might cause an arbitration error).

A-B Refresh request occurs on the falling edge of Phi

B-C Refresh request occurs on the rising edge of Phi

J2

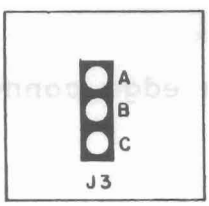


J2 enables the MI trigger circuit to provide more access time during MI cycles. This mode is only used with Z80's that don't delay the start of MI status signal.

A-B No MI trigger

B-C MI trigger enabled

J3

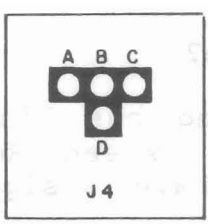


J3 enables a transparent refresh cycle to occur immediately after the RAS precharge time of instruction fetch cycles. (Z80 processors only.)

A-B No transparent refresh

B-C Transparent refresh enabled

J4



J4 determines when wait states are requested by the board.

A-B One wait state on all cycles

B-C One wait state when refresh and board select are asserted. Drives pRDY earlier than conflict circuit.

B-D No wait state is requested

2.4 BOARD INSTALLATION AND CHECKOUT

Consider the following steps when installing the 256KDR board:

* Check that SW1 is set to select the desired board address.
* Check that the jumpers are configured correctly.
* Check that socketed IC's are firmly seated.
* Turn off power to the system.
* Insert the board so that the card connector fingers are correctly aligned with the brushes of the bus socket.
* Turn the system power on and run a memory test (such as MEM, which is supplied with Intersystems Disk Operating Systems) over the board address space.

2.5 FAULT ISOLATION

The memory board was extensively tested and burned-in before being shipped, and should work the first time. If the memory board does not operate properly, turn the system power off and consider the following:

* Is the board properly seated in the edge connector?
* Is one of the socketed IC's loose?
* Are the jumpers set properly?
* Should a wait state be added?
* Is the +8 volt line within tolerance?
* Is a board in the system generating bus line 58? IEEE line 58 is designated the Sixteen Request line. Pre-IEEE S-100 boards may have assigned a different function for line 58.

Contact Ithaca Intersystems if the above suggestions do not serve to isolate the problem.

If so inclined, use the following procedure to debug a defective board.

1) Assume that only one memory chip is bad. Run a memory test program. The program shows the address and bad bit(s) of any byte or word that fails the test. Refer to section 1.3 to locate the memory chip that corresponds to the address.

2) Rock a suspected chip in its socket. Check for bent pins. Rerun the memory test.

3) Replace a suspected chip. NOTE: Orient the new chip correctly. Rerun the memory test

4) If the substituted chip tests bad, if several chips are indicated as being bad, or if the memory test program does not run with the 256KDR board, then it is likely that the problem is either incorrect jumpering or a defective circuit board.

CAS	CAS is the column address strobe that latches the eight column-address bits on the input pins of the memory chip.
Default Refresh	A refresh cycle triggered by counters on the RAM board without regard to the processor cycle.
External Cycle	A read or write RAM board cycle started or triggered by S-100 bus signals.
External Refresh Request Arbitration	The decision made to service either an external or a refresh cycle request signal first.
Instruction Fetch Cycle	Processor cycle where next program instruction is read from memory.
MWRITE	S-100 control signal that strobes data into memory.
Phi	Phi is the master timing signal for the S-100 bus, driven by bus master
Processor Cycle	An S-100 bus cycle composed of three or more bus states, such as a read, write, or I/O cycle.
pSYNC	S-100 control signal indicating the start of a processor cycle.
RAM Board Cycle	Ram board timing sequence during one read, write, or I/O cycle.
RAS	RAS is the Row Address Strobe that latches the eight row-address bits on the input lines to the memory chips.
RAS Precharge Time	The time between the end of one RAS pulse and the start of another.
Refresh Cycle	A RAM board cycle used to restore data to nondegraded voltage levels.

sMEMR	S-100 status line indicating a memory read cycle.
sMI	S-100 status line indicating the instruction fetch cycle.
sSXTRQ	S-100 status line driven low when the bus master requests a 16-bit data transfer.
Transparent Refresh	A refresh cycle triggered by S-100 bus timing so that the refresh cycle does not overlap an external cycle.

5.0 MANUAL APPLICABILITY AND BOARD REVISION

This manual applies specifically to boards identified as 4000 P and 1119-01. Boards are identified in the lower right hand corner.

6.0 APPENDIX

6.1 A0 POLARITY

The Ithaca Intersystems 256KDR board is manufactured in accordance with the most recent IEEE specification proposal concerning which polarity of the A0 line selects which byte within an addressed word as described in section 1.2 of this manual.

A jumper appears on the board which allows the board to be reconfigured to operated in systems developed in accordance with prior specifications. Jumper "g" is located between circuit board IC's UR1 and U33, to the right of SW1. See Figure 10. To configure the board for non-standard installations, cut the printed circuit trace between jumper "g" holes A and C, and between B and D. Next, solder a short piece of insulated wire from jumper "g" hole A to hole D, and another piece of insulated wire from hole B to hole C.

Note that the A0 specification is only important in systems that mix 8-bit and 16-bit transfers.

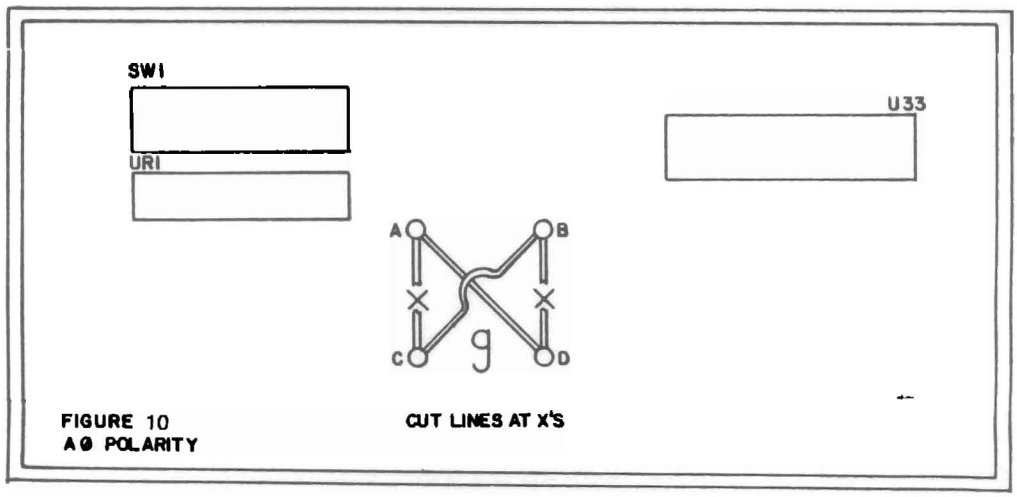


FIGURE 10
A0 POLARITY