Hardware Manual

InterSystems™

Ithaca Intersystems Inc.

Micros for bigger ideas.

The Ithaca InterSystems HDA I

HARD DISK ADAPTER BOARD for the S-100 Bus

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HDA I
HARD DISK ADAPTER

1.0 INTRODUCTION

The Ithaca InterSystems HDA I circuit board serves as an interface between the S-100 Bus and a hard disk controller. The hard disk controller used with InterSystems disk modules can control four disk drive units, providing all the special timing the drives require.

This manual provides information about the general design and features of the Hard Disk Adapter board, instructions for configuring the board for specific installations and the parts list for the board.

1.1 PHYSICAL DESCRIPTION

The HDA I is a standard 5 by 10 inch (12.7 by 25.4 cm), S-100 bus, plug-in circuit board. The circuit card is connected to a system hard disk controller board through the HDA I 50-pin top edge connector.

1.2 FEATURES

* DMA data transfers available for maximum data transfer rate with minimum processor overhead.
* Parity check of data transfers on both the S-100 Bus and the hard disk controller bus.
* Optional DMA (one) wait state generation.
* Vectored interrupt generation.
* 8-bit or 16-bit I/O addressing select.

1.3 BASIC FUNCTION

The basic function of the HDA I circuit card is to transfer information between the S-100 bus and a system hard disk controller. Two kinds of information are transferred: status and command information, and the data being stored.

8-bit data is transferred between the S-100 bus and the hard disk controller board in two ways: polled data transfer and DMA data transfer. Polled data transfer is used to transfer commands to the HDA I, and some controller/hard disk statuses. Various status bits are available at a port on the HDA I that the CPU checks until the HDA I indicates it is ready for a transfer. The CPU then writes a byte to or reads a byte from another port on the HDA I. Commands to the HDA I are always accomplished this way. Some controller/hard disk statuses are returned this way.

DMA (direct memory access) data transfer is available to transfer stored data and some status information. DMA data transfers offer an advantage in speed and is particularly useful in multi-tasking, multi-user systems.

Data transfers that are normally carried on via DMA can also be done by polling, if desired.

Parity

The HDA I card supports the Ithaca InterSystems parity scheme. In this arrangement S-100 lines 65 and 66 are assigned to PARITY and PAREN* respectively. These lines are defined in the IEEE S-100 standard as NDEF (not to be defined). The PARITY line contains odd parity when the device driving the S-100 data bus drives PAREN* active. The HDA I drives PAREN* active as required and generates parity on the PARITY line.

Jumper J5 is set to enable (B-C) or disable (A-B) parity.

1.4 CONTROLLER BUS

The HDA I circuit board is connected to the hard disk controller by the controller bus, a 50-conductor ribbon cable. Figure 1 is a pin assignment chart for the bus. On InterSystems equipment, the hard disk controller board is located in the disk drive module. The cable is attached between the HDA I 50-pin top edge connector (Figure 2), on the board and the appropriate hard disk drive module. The signals on the controller bus are listed below.

Pin No.	Signal	Notes
All odd	Ground	
2	DATA 0*	C/A
4	DATA 1*	C/A
6	DATA 2*	C/A
8	DATA 3*	C/A
10	DATA 4*	C/A
12	DATA 5*	C/A
14	DATA 6*	C/A
16	DATA 7*	C/A
18	ODDPARITY	C/A
20-34	Not Used	1
36	BUSY*	C
38	ACKNOWLEDGE*	A
40	RESET*	A
42	MESSAGE*	C
44	SELECT*	A
46	DATA / CONTROL*	C
48	REQUEST*	C
50	WRITE / READ*	C

Notes:

1 Even no. pins only
A Line driven by HDA I
C Line driven by hard disk controller board.

Figure 1 HDA I top connector pin assignments

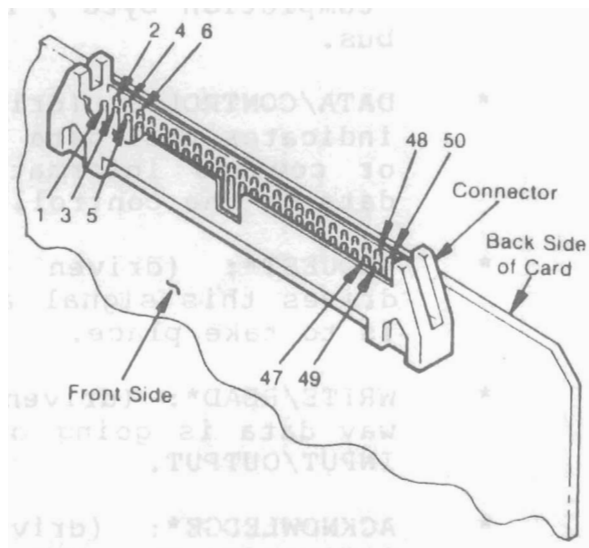


Figure 2 Top edge connector pin locations

* DATA0* through DATA7*: eight bi-directional data bits, driven by either the controller board or the HDA I. The bus carries inverted data.

* ODDPARITY: (driven by either the controller board or the HDA I) carries the the odd parity bit during data transfers.

* BUSY*: (driven by controller) when inactive, indicates the controller is waiting; when active, the controller is busy.

* MESSAGE*: (driven by controller) indicates the end of a command. When active, a byte called the "completion byte", is placed on the controller data bus.

* DATA/CONTROL*: (driven by controller) when low, indicates that data on the controller bus is status or command information; when high, indicates that data on the controller bus is actual disk data.

* REQUEST*: (driven by controller) the controller drives this signal active whenever a data transfer is to take place.

* WRITE/READ*: (driven by controller) indicates which way data is going on the data bus. Also known as INPUT/OUTPUT.

* ACKNOWLEDGE*: (driven by the HDA I) when low, indicates the HDA I is finished with a data transfer.

* RESET*: (driven by the HDA I) when asserted, returns the controller to a pre-defined state. The signal is connected to the S-100 RESET* line.

* SELECT*: (driven by the HDA I) asserted at the beginning of a command sequence to poll the controller.

Controller Bus Timing

The hard disk controller board is the master on the controller bus. When the controller is ready to read or to write a byte, it asserts REQUEST* and then waits for the HDA I to assert ACKNOWLEDGE*.

During a READ (from the controller to the HDA I) cycle the controller places data on the bus before REQUEST* goes active. The HDA I drives ACKNOWLEDGE* active when finished with the data. This occurs at the end of the S-100 bus cycle when the CPU actually reads the data, or at the end of the DMA cycle. After the controller sees ACKNOWLEDGE* active, it deasserts REQUEST*.

During a WRITE (to the controller, from the HDA I) cycle, the controller asserts REQUEST* when it is ready to receive data. The HDA I drives ACKNOWLEDGE* active when it has latched the data into its controller data bus drivers. This occurs at the end of the S-100 bus cycle when the CPU is writing data, or in a DMA cycle, at the end of pDBIN. The data must remain stable until the controller deasserts REQUEST*.

The REQUEST*/ACKNOWLEDGE* timing is fundamental to all data transfers between the HDA I and the controller. The WRITE/READ*, DATA/COMMAND*, and MESSAGE* status are valid before REQUEST* goes high, and remain so until ACKNOWLEDGE* goes inactive. WRITE/READ* and DATA/COMMAND* describe the type of data transfer, and MESSAGE* indicates if the data transfer is to be the last in the command cycle.

When the HDA I initiates a command to the controller the following handshake procedure takes place. The system checks the BUSY* status on the controller bus by reading a port on the HDA I card. BUSY* must be inactive before the HDA I begins its command. (The BUSY* status is active if the controller has not finished a previous command or if there is an error.) The HDA I then asserts DATA0 and SELECT*. The controller responds (after at least 690 nanoseconds) by asserting BUSY*. When BUSY* goes active, the HDA I deasserts SELECT* and DATA0. Further activity follows the REQUEST*/ACKNOWLEDGE* protocol.

1.5 HDA I REGISTER MAP

The HDA I registers are I/O mapped as described below:

Write Ports

Port	Function
00	Write Command to Controller. Data is written to this port when transferring data via polled operation instead of DMA transfer.
01	Assert SELECT*. SELECT* is asserted whenever data is written to this port. SELECT* remains asserted until the controller asserts BUSY*.
02	Enable Latch. D0 equal to logic ONE = DMA enable. D1 equal to logic ONE = Interrupt enable.
03	Not Used
04	Address Counter. A0 through A7
05	Address Counter. A8 through A15
06	Address Counter. A16 through A23
07	Parity Error Reset. Writing to this port resets the status port parity error report bit to ZERO.

Read Ports

Port	Function
00	Read Controller Data (Controller Status). During polled data transfers, data is read from this port.
01	Read Controller Status. Status register described below:

D0	REQUEST*
D1	DATA/COMMAND*
D2	WRITE/READ*
D3	BUSY*
D4	MESSAGE*
D5	PARITY ERROR*
D6	ACKNOWLEDGE
D7	Not Used

02	Reset Controller
03	Unreset Controller

2.0 BOARD SETUP

This section of the manual describes how to prepare the HDA I board for operation and install it in a system.

2.1 SW1 AND SW2

DIP switches SW1 and SW2 are set to select the HDA I circuit board I/O port address space. See Figure 3. The HDA I is set to occupy any eight port I/O space with an 8H boundary base address; i.e., 00H, 08H to F8H for eight bit I/O addressing, or 0000H, 0008H, 0018H, for sixteen bit I/O addressing (selected by J6). Switches SW1-4 through SW1-8 select address lines A3 through A7 respectively for 8-bit and 16-bit I/O address selection. Switches SW2-1 through SW2-8 select address lines A8 through A15 respectively 16-bit addressing. An open switch corresponds to an address bit = 1.

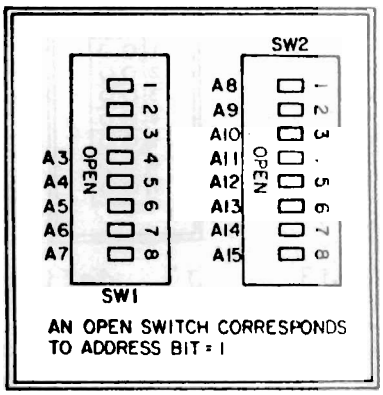


Figure 3 SW1 and SW2

2.2 JUMPER CONFIGURATION

There are five jumper areas on the HDA I board, used to set up the board for different installations. Each jumper area box contains a group of plated-through holes spaced 0.1" apart. To configure a jumper area, one connection per box is made between adjacent plated-through holes, either by a circuit solder trace on the solder side of the board, or by a shunt that slides onto square posts that are soldered in the holes. To change a connection made by a solder trace, the trace must be cut between jumper holes. Possible connections within jumper areas are designated by letter names. The letter names run A, B, C, ... from right to left, or from top to bottom. Figure 3 shows the location of jumpers on the board.

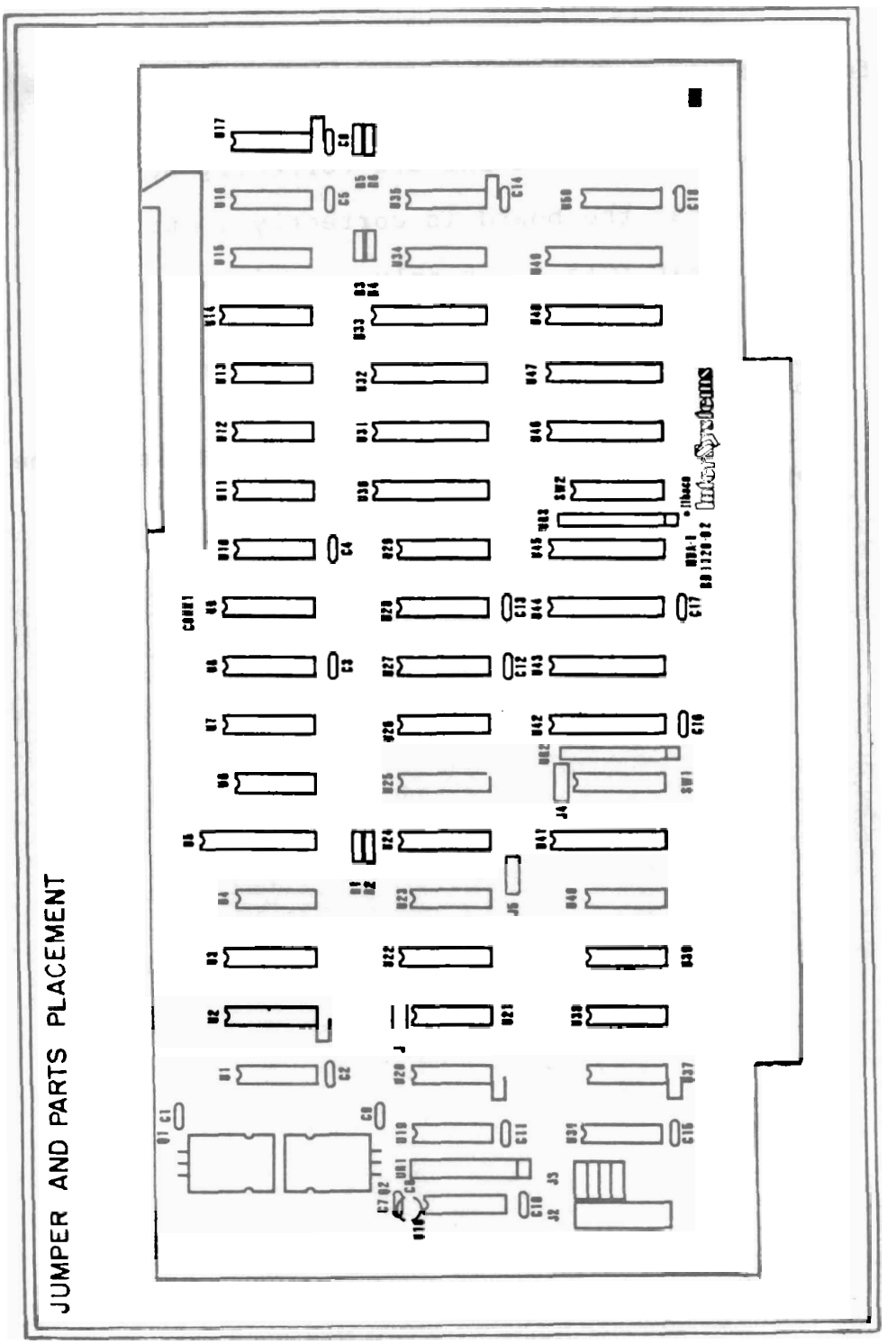


Figure 4 HDA I board

2.3 BOARD INSTALLATION

Use the following procedure when installing the HDA I board:

* Check that SW1 and SW2 are correctly set.
* Check that the board is correctly jumpered.
* Check that IC's are firmly seated in sockets.
* Insert the board with the card connector fingers correctly aligned with the brushes of the bus socket.
* Firmly connect the controller bus cable to the card top connector.

3.0 PARTS LIST

Placement	Part
U1	74LS00
U2	74LS279
U3	74LS175
U4	74LS27
U5	74LS240
U6	74LS00
U7	74LS279
U8	74LS138
U9	74LS139
U10	74LS08
U11-12	7438
U13	74LS280
U15	7406
U16	74LS04
U17-18	7438
U19	74LS21
U20	74LS32
U21	74LS08
U22	74LS75
U23	7407

Placement	Part
U24-29	74LS191
U30	74LS240
U31-32	74LS373
U33	74LS244
U34	74ALS74
U35	74LS51
U36	74LS21
U37	74LS11
U38	74LS08
U39	74LS04
U40	74LS125
U41	74LS244
U42	25LS2521
U43-44	74LS244
U45	25LS2521
U46	74LS244
U47	74LS240
U48-49	74LS244
U50	74LS32

CAPACITORS

C1-7, 9-18	.1 uf DP
C8	33 uf

RESISTORS AND RESISTOR NETWORKS

R1, 4, 5	220 Ohm
R2, 3, 6	330 Ohm
UR1	15 K 9 POS
UR2,3	4.7 K 9 POS

REGULATOR

7805

HARD DISK ADAPTER

4.0 MANUAL APPLICABILITY AND BOARD REVISION

Edition 1.1 of the HDA I manual applies specifically to boards identified as BD 1120-03. Edition 1.1 of the manual is essentially the same as Edition 1 except that 1.1 describes jumper J5.

Edition 1 of the HDA I manual applies specifically to HDA I boards identified as BD 1120-02.

For boards identified as BD 1120-01, the following provision applies

Jumper Reference

J4 J4 selects the noise lockout signal for the interrupt arbitration circuit. Position A-B is the InterSystems standard.

J5 J5 selects the source of pSTVAL*.
J5 A-B: pSTVAL* = NOT(pSYNC AND NOT PHI)
J5 B-C: pSTVAL* = delayed pSYNC (InterSystems standard)

J6 J6 configures the board for either 8-bit or 16-bit addressing. J6 A-B: 8-bit, J6 B-C: 16-bit.

FORMATTING THE HARD DISK FROM MONITOR

When, in the course of human events, it becomes necessary to reformat track 0 of the hard disk, the following may prove helpful.

If you are attempting to format a disk attached to a 2nd HDA in the ıs, increment all port addresses by eight.

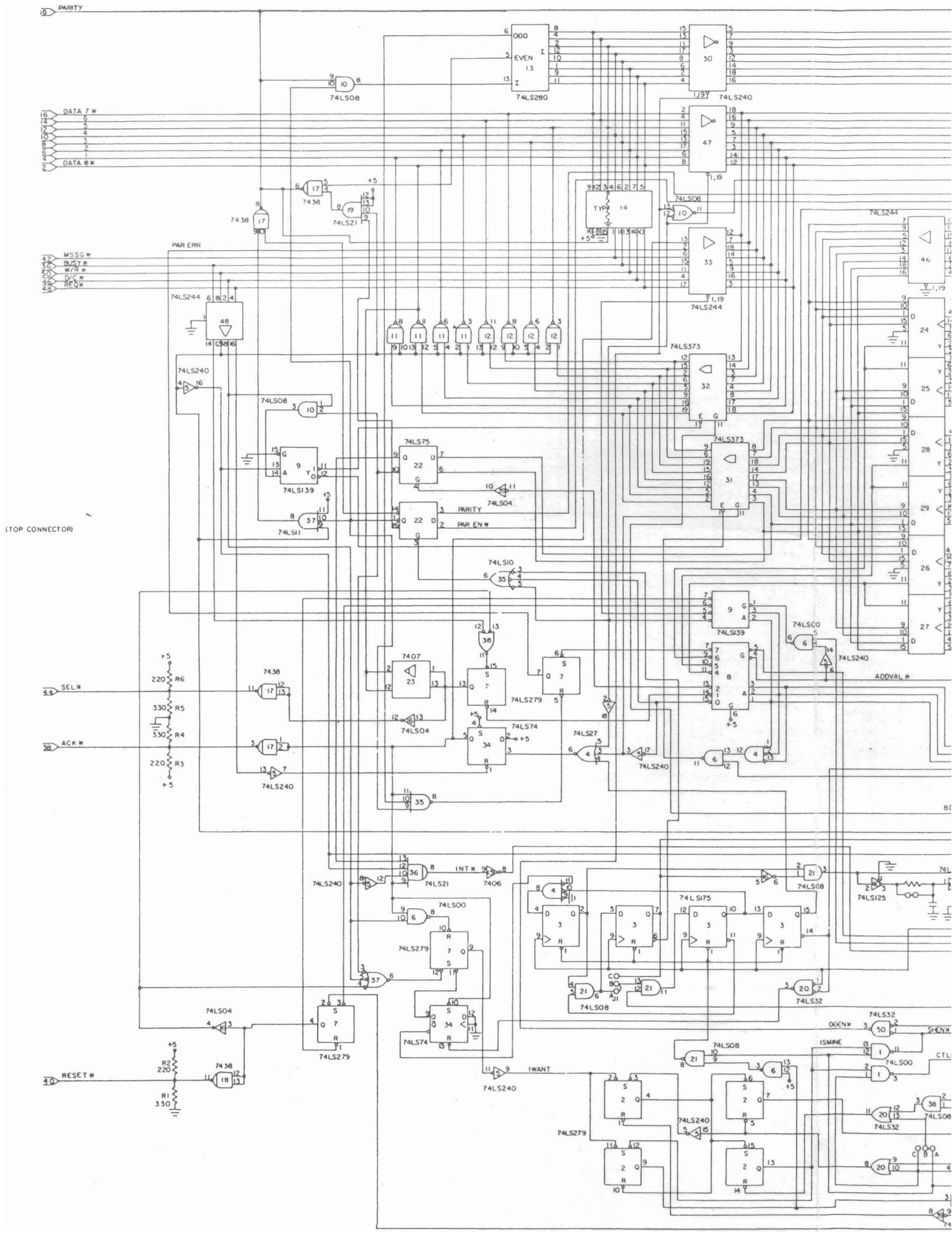
ıter the monitor. Type in the following commands.

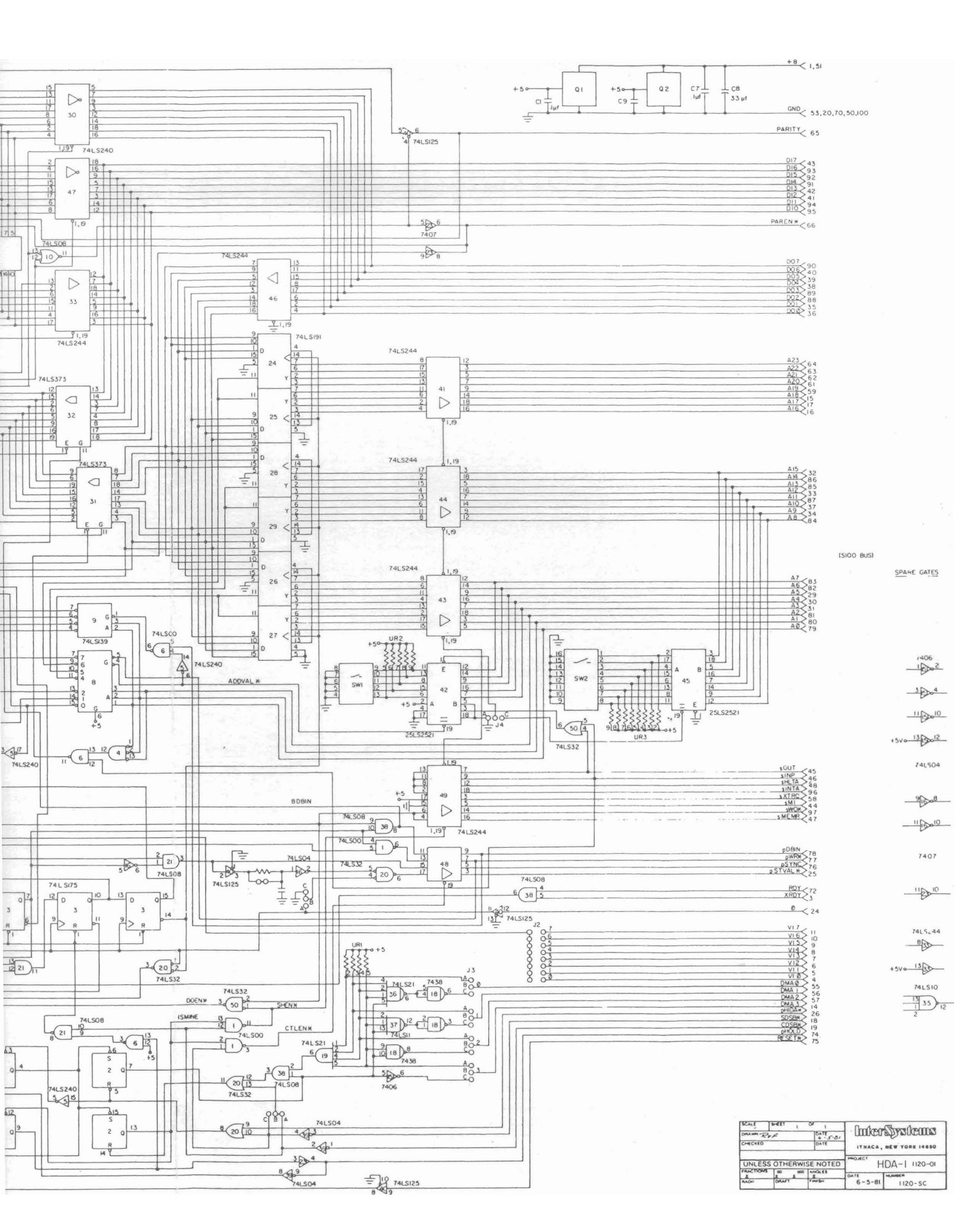
Command	Computer Response
I82 (CR)	anything
I83 (CR)	anything
O82,1 (CR)	No Response
O87,0 (CR)	No Response
O81,0 (CR)	No Response
I81 (CR)	B4 - If you do not get a B4, start over.
O80,6 (CR)	No Response
O80,0 (CR)	No Response
O80,0 (CR)	No Response
O80,0 (CR)	No Response
O80,8 (CR)	No Response - If interleave isn't 8 for this drive, substitute correct value.
O80.0 (CR)	No Response
I80	0 - If not zero, finish next step and start over.
I80	0 - If not zero, start over.
I81	anything.

NORMAL SECTOR ZERO

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4000	lp	lp	lp	lp	lp	lp	00	00	56	45	52	20	31	ld	d1	d1
4010	d1	d1	d1	d1	DL	DL	DL	DL	DL	DL	DL	DL	DL	DL	DL	DL
4020	DL	DL	DL	DL												

lp - load parameters
ld - # of logical drives on this hard drive
d1 - define limits command for OMTI 10A and 20A
DL - define limits command for OMTI 20C


PARITY
DATA 7 *
DATA 0 *
MSSG *
BUSY *
W/R *
D/C *
REQ *
PAR ERR
(TOP CONNECTOR)
SEL *
ACK *
RESET *
74LS280
74LS240
74LS08
74LS244
74LS373
74LS75
74LS139
74LS04
74LS11
74LS10
74LS279
74LS74
74LS27
74LS00
74LS21
74LS175
74LS32
74LS125
74LS00
7438
7407
7406
ADDVAL *
INT *
IWANT
DDEN *
ISMINE
SHEN *
CTL
R1 330
R2 220
R3 220
R4 330
R5 330
R6 220



SCALE	SHEET 1 OF 1	InterSystems	
DRAWN	DATE 4-5-81	ITHACA, NEW YORK 14850	
CHECKED	DATE		
UNLESS OTHERWISE NOTED		PROJECT HDA-1 1120-01	
FRACTIONS ±	00 ± .000 ±	ANGLES ±	DATE 6-5-81
FINISH	DRAFT		NUMBER 1120-SC