

VIDEO DISPLAY BOARD

IA-1100

Instruction Manual

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FEATURES

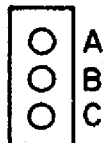
- * 16 lines of 64 characters each
- * Full upper/lower case ASCII character set, numbers, symbols, and Greek letters
- * Characters are composed of 7 x 9 dot matrix in an 8 x 10 field
- * Selectable display modes, normal or reverse video, blinking character
- * Memory addressable to any 1K page
- * Software driver simulates TTY, provides full cursor control (up, down, forward, back, home, and flashing), scrolling and paging
- * Convenient composite video out connector, RCA phono plug
- * 50 - 60 Hz jumper option, compatible with European requirements
- * Compatible with CP/M or Ithaca Audio's K3 Operating System
- * All S-100 lines fully buffered

ASSEMBLY INSTRUCTIONS

BOARD ASSEMBLY

- 1) Install sockets for U1 through U35, U37, and UR1 (U36 is a spare position). Be sure you don't accidentally solder an IC socket in the upper right hand corner of the board. A DIP switch is normally mounted in this position. DO NOT INSTALL ANY IC's UNTIL AFTER THE POWER SUPPLY HAS BEEN CHECKED OUT.
- 2) Install an eight position DIP switch (SPST) in the upper right hand corner of the board. This location is not designated with any IC number. Position # 1 on top.
- 3) Install a .001 uf (1000 pf) at 15 volts (or higher) capacitor in locations C1 and C7.
- 4) Install .01 to .1 uf bypass capacitors in locations C8, C10, C11, C12, C18, C19, and C21. These are simply bypass capacitors and their exact value is not critical, although they should be at least .01 uf at 15 volts.
- 5) Install a 10 pf at 15 volts (or higher) capacitor in location C2.
- 6) Install a 10 uf at 15 volts (or higher) electrolytic capacitor in locations C3, C4, C14, C15, and C16. A tantalum capacitor is ideal but ordinary aluminum electrolytics are perfectly adequate. With the board facing you and the edge connector down, C3 and C4 are installed with their positive end on your right. C14, C15, and C16 should be installed with their positive end on your left.
- 7) Install a .1 uf at 15 volts (or higher) capacitor in locations C5, C6, and C20.
- 8) Install a 100 uf at 12 volts (or higher) electrolytic capacitor in location C9. The positive end should face down.
- 9) Install a 470 pf at 15 volts (or higher) capacitor in location C17.
- 10) Install a 1 to 10 uf electrolytic capacitor at 10 volts (or higher) in location C22. The positive end should face up.
- 11) Install a 390 ohm 1/4 watt resistor in locations R1 and R2.
- 12) Install a 4.7K ohm DIP resistor pac in location UR1 (R6 thru R12). Install a 4.7K ohm, 1/4 watt resistor in location R3, R4, R14 and R23.
- 13) Install a 2.7K ohm 1/4 watt resistor in locations R5 and R13.
- 14) Install a 10K ohm 1/4 watt resistor in locations R15 and R22.

- 15) Install a 100 ohm 1/2 watt resistor in location R16.
- 16) Install a 330 ohm 1/4 watt resistor in location R17.
- 17) Install a 270 ohm 1/4 watt resistor in location R18.
- 18) Install a 75 ohm 1/4 watt resistor in location R19.
- 19) Install a 1000 ohm 1/2 watt resistor in location R20.
- 20) Install a 5.6 megohm 1/4 watt resistor in location R21.
- 21) Install a 7805 (LM340T-5) in locations Q1 and Q2. The voltage regulators should be greased but no heat sink is needed since the current drain on each regulator is well under 1/2 amp.
- 22) Install a 50K ohm trimpot in locations UR1 and UR2. The trimpots are .1 inch in-line miniatures, such as D2C503 ALLEN-BRADLEY.
- 23) Install the crystal in location Y1. The crystal should be 13.478 MHz if jumper J1 is installed (recommended) and 12.636 MHz if jumper J1 is not installed. Strap the crystal down by soldering a wire across the crystal in the mounting holes provided.
For explanation of J1, refer to page 5.
- 24) Install a 12 volt zener diode in location -1. The cathode band end should be on the left.
- 25) Install a 5.5 volt zener diode in location -2. The cathode band end should also be on the left.
- 26) Install J2.



A - B 60Hz
B - C 50Hz

- 27) Install RCA phono jack, female receptive, such as IEM RJP5116-1 or S&K SQ 3931 in the upper left edge. Insert output cable with male RCA plug.

At this point the board should be completely populated but no ICs should be installed. Insert the card into the computer and measure the voltages on pins 1, 2 and 3 of U12. The voltages should be -5.5, +5 and +12 plus or minus 5% respectively. If the voltages do not check out, examine the zener diodes and Q1. Make sure the diodes are installed properly and check to see if there are any shorts. Measure the voltage on pin 16 of U30. It should be 5 volts plus or minus 5%. When all the voltages check out, the integrated circuits may be installed.

DIP SWITCH SELECTION

POSITION 1: (Top of Board) When switch is on (shorted), normal video is displayed (white on black). When switch is off, reverse video is displayed.

POSITION 2: When switch is on, a solid cursor block is displayed. When switch is off, a blinking cursor block is displayed.

POSITION 3: Determines A15 of board address. On 0, Off 1.

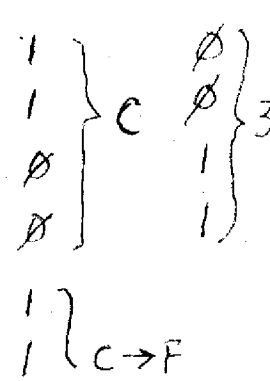
POSITION 4: Determines A14 of board address. On 0, Off 1.

POSITION 5: Determines A13 of board address. On 0, Off 1.

POSITION 6: Determines A12 of board address. On 0, Off 1.

POSITION 7: Determines A11 of board address. On 0, Off 1.

POSITION 8: Determines A10 of board address. On 0, Off 1.



CIRCUIT DESCRIPTION

The IA-1100 can be broken down into essentially five functional blocks: 1) Master timing and sync generation; 2) screen memory; 3) character generation; 4) cursor; 5) and computer interface.

MASTER TIMING

Two inverter gates (U7) connected as a feedback pair with a series resonant crystal (Y1) form a crystal controlled oscillator. This oscillator (typically 13.478 MHz or 12.636 MHz) defines the period for one dot and is referred to as the DOT CLOCK. Since the IA-1100 uses a high resolution 7 x 9 character generator, it is required that 9 DOT CLOCK periods form a complete character along the horizontal. Seven dots are displayed and two dots provide space between characters. U26 provides this character timing by dividing the DOT CLOCK by nine. U26 is preset to 7 by its own carry to provide the proper division. Two outputs are supplied by U26; the LOAD CLOCK, which is an active low signal of one DOT CLOCK duration, and the CHARACTER CLOCK, which is high for 4 and low for 5 DOT CLOCK periods. The positive going edge of the LOAD CLOCK and the CHARACTER CLOCK occur simultaneously.

The CHARACTER CLOCK is counted by U11 and U18. This pair of binary counters is preset to 31 hex (or 37 hex) and count to 90 hex. Thus they count either 96 or 90 CHARACTER CLOCKS. The choice of either 96 or 90 CHARACTER CLOCKS is provided by jumper J1. When it is installed U18 and U11 count 96 CHARACTER CLOCKS and a 13.478 MHz crystal must be used. When the jumper is left out, 90 CHARACTER CLOCKS are counted and a 12.636 MHz crystal must be used.

The preset of U11 and U18 define the left hand margin of the display. Counts 40 hex through 7F hex define the 64 successive displayed character positions and counts 80 hex through 8F hex define the right hand margin. The outputs of U18 provide the 4 lowest order address bits (A0, A1, A2, and A3) to the screen memory. The QA and QB outputs from U11 provide the two higher order address bits (A4 and A5). The QC output from U11 controls the horizontal margin blanking. When QC is low, the screen is blanked; when it is high, characters can be displayed. The QD output from U11 provides the horizontal sync advance and will be discussed later in this section.

When U11 reaches a count of 9, the output of nand gate U9 presets U11 and U18 back to a count of 31 hex (or 37 hex) and the horizontal cycle repeats itself.

At the same time the preset of U11 and U18 occurs, the ROM counter U25 is incremented. The ROM counter counts the horizontal scan lines that make up a row of characters and supplies the line number to the character generator ROM. The ROM counter is preset to a count of 15 and counts from 0 to 11. Therefore it counts 13 horizontal lines per character. U13, U14, and U15 decode the output from the ROM counter and supply it with a load pulse when it reaches a count of 11. This load pulse is used to preset the ROM counter to 15.

The load pulse which presets the ROM counter also increments the row counters U27 and U28. The row counters count the number of rows which are displayed and supply the screen memory with the four highest order address lines (A6, A7, A8, and A9). The row counters are preset to zero

and count to 19. When count 19 is reached, nand gate U17 supplies U27 and U28 with a load pulse and presets them back to count zero.

The row counters also supply the signals that provide vertical margin blanking. When U27 and U28 reach a count of 16, they provide a signal which blanks the screen (QA output of U27). This blanking is needed so only 16 rows are displayed and no "Wrap Around" occurs. This same signal is also used to create the vertical sync advance.

The vertical sync advance line is used to trigger a dual monostable multivibrator U16. One-half of U16 is used to generate a user adjustable delay pulse. The width of this pulse is adjusted by VR1. This pulse is then used to trigger the other half of U16 which provides a vertical sync pulse (typically 700us). By setting VR1 the user can then adjust the vertical sync timing with respect to the video output, thus allowing the vertical position to be "adjusted" to the particular monitor used.

The horizontal sync advance line, mentioned earlier, is used in much the same way as the vertical sync advance line. The QD output from U11 is used to trigger one-half of a monostable, U8, which generates a delay determined by VR2. This delayed generator is used to trigger the other half of U8 which provides the horizontal sync pulse (typically 3us). By setting VR2 the user can then adjust the horizontal sync timing with respect to the video output, thus allowing the horizontal positioning to be "adjusted" in much the same manner as the vertical.

SCREEN MEMORY

The screen memory (U20, U21, U22, U23, U31, U32, U33, and U34)

consist of eight 250ns 2102's. All of the screen memory chips are held enabled (pin 13 low). Memory addressing is provided by four tri-state buffers (U19, U29, U30 and U35) which select addressing from one of two possible sources: external address from the computer or internal character address from U11, U18, and U28. The computer always has priority with respect to the screen memory and the write enable input (pin 3) to the screen memory chips is active only when the computer is doing a screen write operation.

CHARACTER GENERATION

The outputs from the screen memory are connected to the character inputs of U12, the character generator ROM. This ROM has seven character address inputs, four row select inputs, and seven data outputs. The row select inputs, as mentioned earlier, are connected to the row counter U25. The data outputs are connected to U5, a synchronous parallel-in serial-out shift register.

U5 is loaded by the LOAD CLOCK and shifted by the DOT CLOCK. The serial output line of U5 (pin 13) is connected to an exclusive-or gate (U4). This gate performs an exclusive-or operation between the shifted serial output and the cursor control circuitry to provide an "inverted video" cursor block.

The output of the previously mentioned exclusive-or gate is then routed to U2, a four input nand gate. This gate combines all of the blanking signals (horizontal blanking, vertical blanking, and board-enable blanking) with the video.

The output of U2 is sent through another exclusive-or gate, U4,

which allows the entire screen to be inverted (black on white). This option is provided by the first position on the dip switch. When the switch is on, normal video (white on black) is displayed. When the switch is off, reverse video (black on white) is displayed.

The output of the inverted video exclusive-or gate is connected to U1, the video output gate. U1 combines the video signal with the horizontal and vertical sync pulses that are generated by the previously mentioned one-shots, U8 and U16. R17, R18, and R19 set the voltage ratios of the video level and the sync level. The final video output is coupled through the output capacitor, C9.

CURSOR

A CMOS inverter, U6, is connected as a self oscillating RC feedback oscillator. The .5 second period of this oscillator is set by R21 and C20. The output of this oscillator is connected to R22 and then inverted by another gate in U6. The input to this gate can be shorted to ground by switch position 2 on the dip switch, thus allowing the cursor to appear as a solid inverted video block or as a hardware blinking inverted video block (when the switch is on, the cursor is solid - when it is off, it will blink).

The output of the gate described above is connected to the reset line on U3, a "D" type flip-flop. U3 is used to clock the data from bit 7 of the screen memory to the previously described video inversion exclusive-or gate, U4. When the output of U6 is low, U3 is held in a reset state and no video inversion occurs. When the output of U6 is high, video inversion can occur if bit 7 of the screen memory is high, thus the cursor

will appear to blink.

Any character in the screen memory can appear as an inverted video cursor simply by setting bit 7 of that character location high.

DEBUG INSTRUCTIONS

1) Visual Check: CAREFULLY (95% of problems come from these errors)

- 1.1 Pins bent under sockets
- 1.2 Pins folded out
- 1.3 Solder splashes
- 1.4 Cold solder, missing solder

INSERT BOARD: Remove all other boards: Turn on machine

2) Check Voltages:

- 2.1 plus 5 volts at plus of C3
- 2.2 plus 5 volts at plus of C4
- 2.3 minus 3.3 volts at minus of C16
- 2.4 plus 12 volts at plus of C15

3) Timing Chain

It is not possible to debug the timing chain without an oscilloscope. If there is no scope available, return board to factory. See instructions in warrantee.

3.1 Character Clock: See Fig. 1

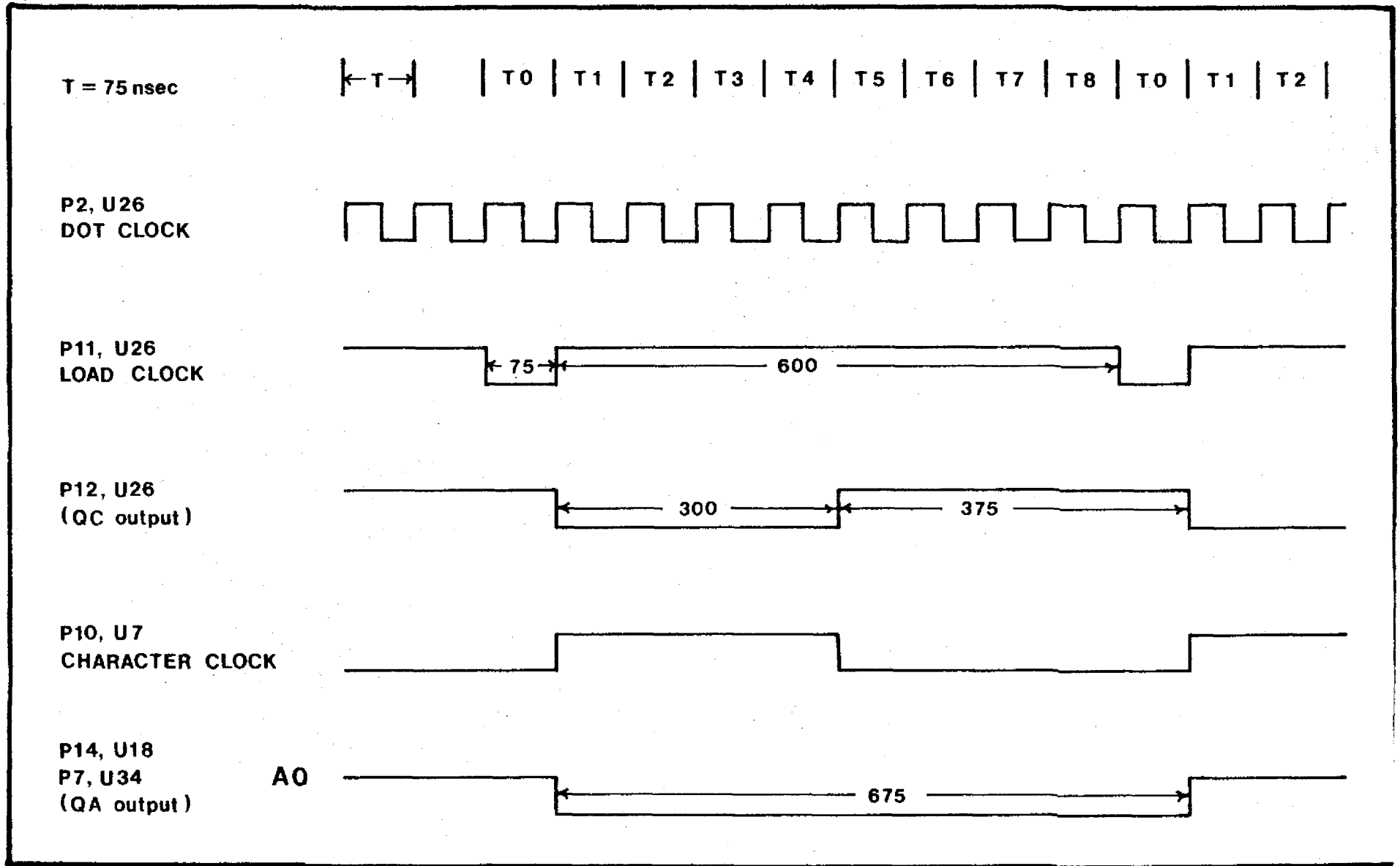
- A) Dot Clock: Check at IC 26 pin 2
This signal is a square wave with period of 75 nsec
- B) Load Clock: Check at IC 26 pin 11
74 nsec low, 600 nsec high
- C) Character Clock: Check at IC 7 pin 10
300 nsec high, 375 nsec low
- D) A0 at IC 18 pin 14
Square wave with period of 1.35 usec

Also check at IC 34 pin 7
- E) (not on Fig. 1)
A1 at IC 18 pin 13
Square wave with period of 2.7 usec

Also check at IC 34 pin 5
- F) A2 at IC 18 pin 11
Square with period of 10.8 usec

Also check at IC 34 pin 15
- G) A3 at IC 18 pin 11
Square with period of 10.8 usec

Also check at IC 34 pin 14



CHARACTER CLOCK TIMING
(all times in (nsec) nanoseconds)

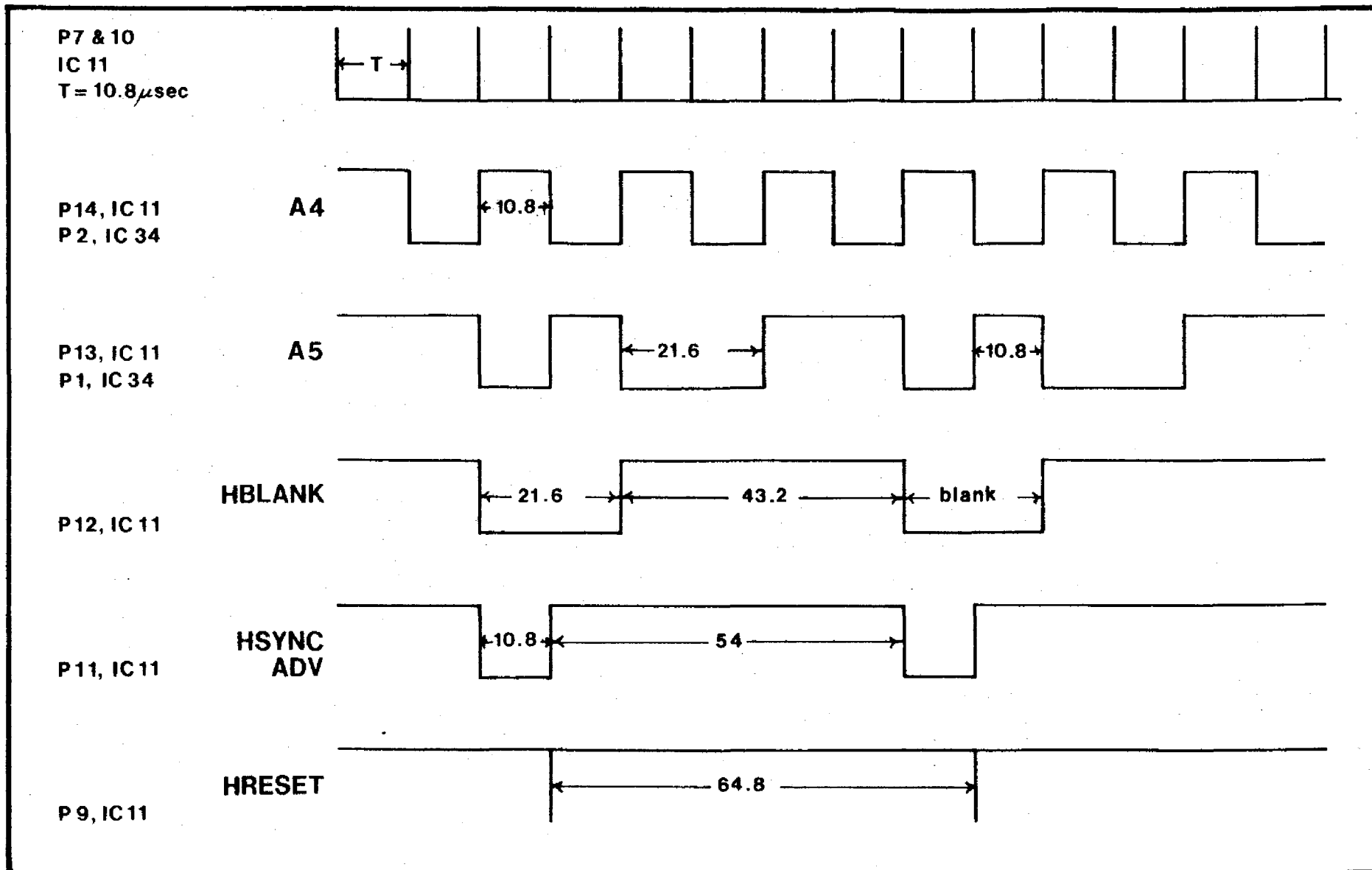
FIG. 1

3.2 Horizontal Timing: See Fig. 2

- A) High count enable at IC 11 pins 7 and 10
Narrow high going pulse with period of 10.8 usec
- B) A4 at IC 11 pin 14
Square wave with period of 21.6 usec

Also check at IC 34 pin 2
- C) A5 at IC 11 pin 13
See Fig. 2 for timing

Also check at IC 34 pin 1
- D) Horizontal screen blank at IC 11 pin 12
43.2 usec high, 21.6 usec low
Screen blanked while low
- E) Horizontal Sync Adv at IC 11 pin 11
10.8 usec low, 54 usec high
- F) Horizontal Reset at IC 11 pin 9
Narrow negative pulse with period of 64.8 usec

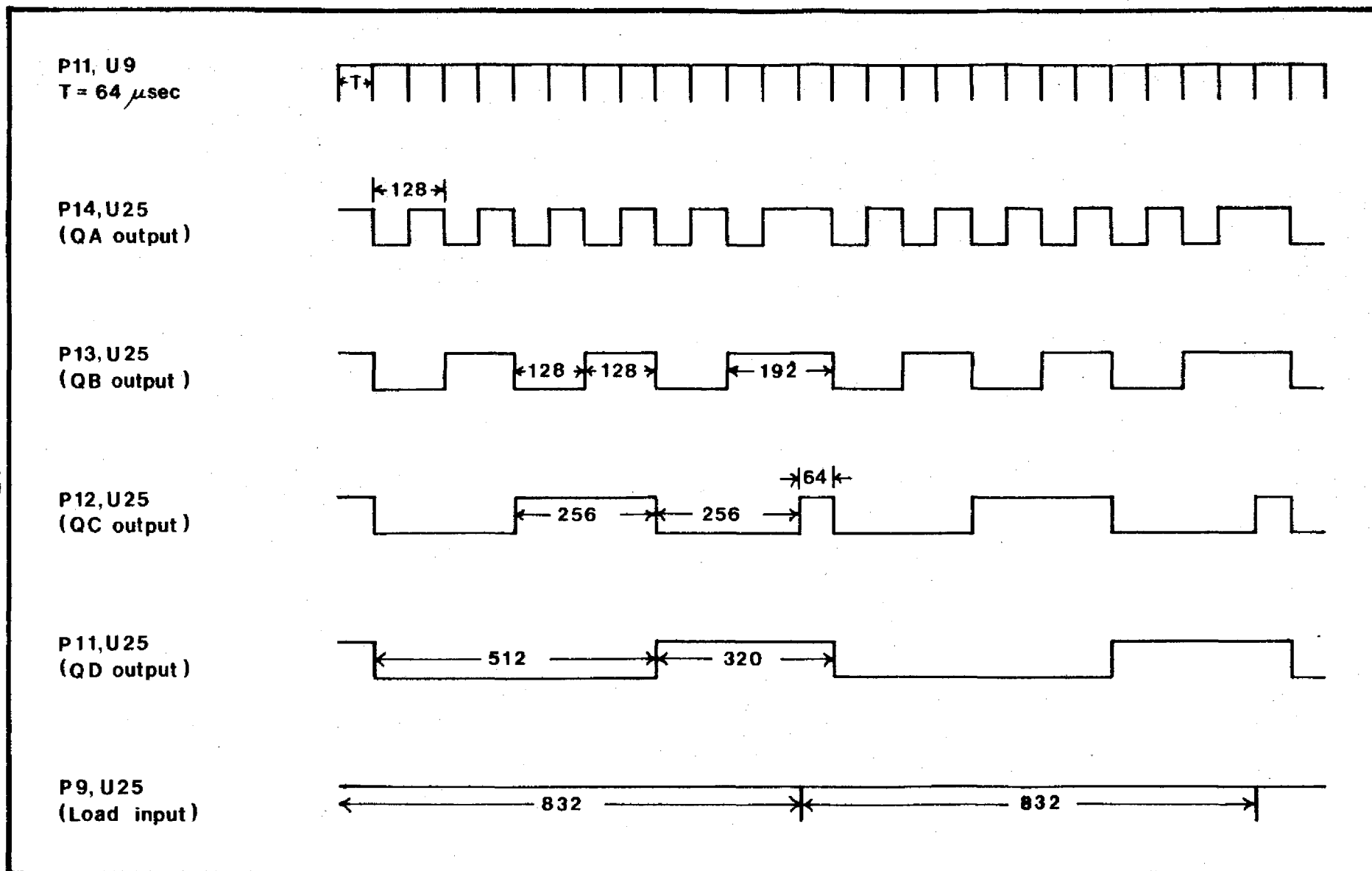


HORIZONTAL TIMING
(all times in (μsec) microseconds)

FIG. 2

3.3 Line Counter: See Fig. 3

- A) Line Clock at IC 9 pin 11
Narrow negative going pulse with period of 64 usec
- B) Line Bit 0 (QA output) at IC 25 pin 14
See Fig. 3 for Timing
- C) Line Bit 1 (QB output) at IC 25 pin 13
See Fig. 3 for Timing
- D) Line Bit 2 (QC output) at IC 25 pin 12
See Fig. 3 for Timing
- E) Line Bit 3 (QD output) at IC 25 pin 11
See Fig. 3
- F) Line Reset (load input) at IC 25 pin 9
Narrow negative pulse with period of 832 usec



LINE COUNTER TIMING
(all times in (μsec) microseconds)

FIG. 3

3.4 Row Counter: See Fig. 4

- A) Row Clock at IC 25 pin 9
Negative pulse with period of .83 msec

- B) A6 (Q0 output) at IC 28 pin 14
Square wave with period of 1.664 msec

Also check at IC 34 pin 4

- C) A7 (Q1 output) at IC 28 pin 13
Square wave with period of 3.328 msec

Also check at IC 34 pin 16

- D) A8 (Q2 output) at IC 28 pin 12
See Fig. 4

Also check at IC 34 pin 6

- E) A9 (Q3 output) at IC 28 pin 11
6.656 msec high, \approx 10 msec low

Also check at IC 34 pin 8

- F) Vertical Sync Adv at IC 27 pin 14
13.312 msec low, 3.32 msec high

- G) Row Counter Reset (load input) at IC 27 pin 9
IC 28 pin 9
Negative pulse with period of 16.64 msec

4) Video

- A) Access Blanking: At IC 2 pin 12
Should be high unless board is Accessed

- B) Open switch at Position 1
Check IC 4 pin 11 for presence of high frequency video signal

- C) Close switch at Position 1
Video should invert

P9, U25
T = 0.83msec



P14, U28
P4, U34
(Q0 output)



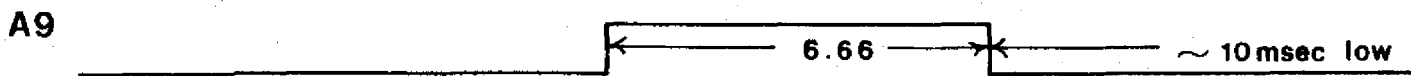
P13, U28
P16, U34
(Q1 output)



P12, U28
P6, U34
(Q2 output)



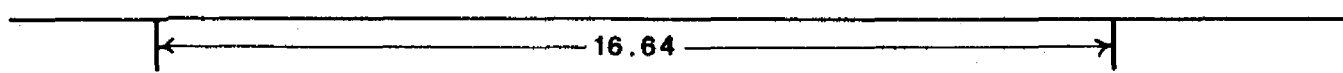
P11, U28
P8, U34
(Q3 output)



P14, U27
(Q0 output)



P9, U27 28
(Load input)



ROW COUNTER TIMING
(all times in (msec) milliseconds)

FIG. 4

5) Sync: See Fig. 5

- A) Horizontal delay at IC 8 pin 4
Pulse width should vary with adjustment of HPOS control VRZ
from 750 nsec to 8 usec
- B) Horizontal sync at IC 4 pin 1
low 60 usec, high 4.5 usec
- C) Vertical Delay at IC 16 pin 4
Pulse width should vary with VPOS control (VR1)
from 200 usec to 3 msec
- D) Vertical Sync at IC 4 pin 2
Low 16.6 msec, high 190 usec
- E) Composite Sync at IC 4 pin 3

6) Bus Access

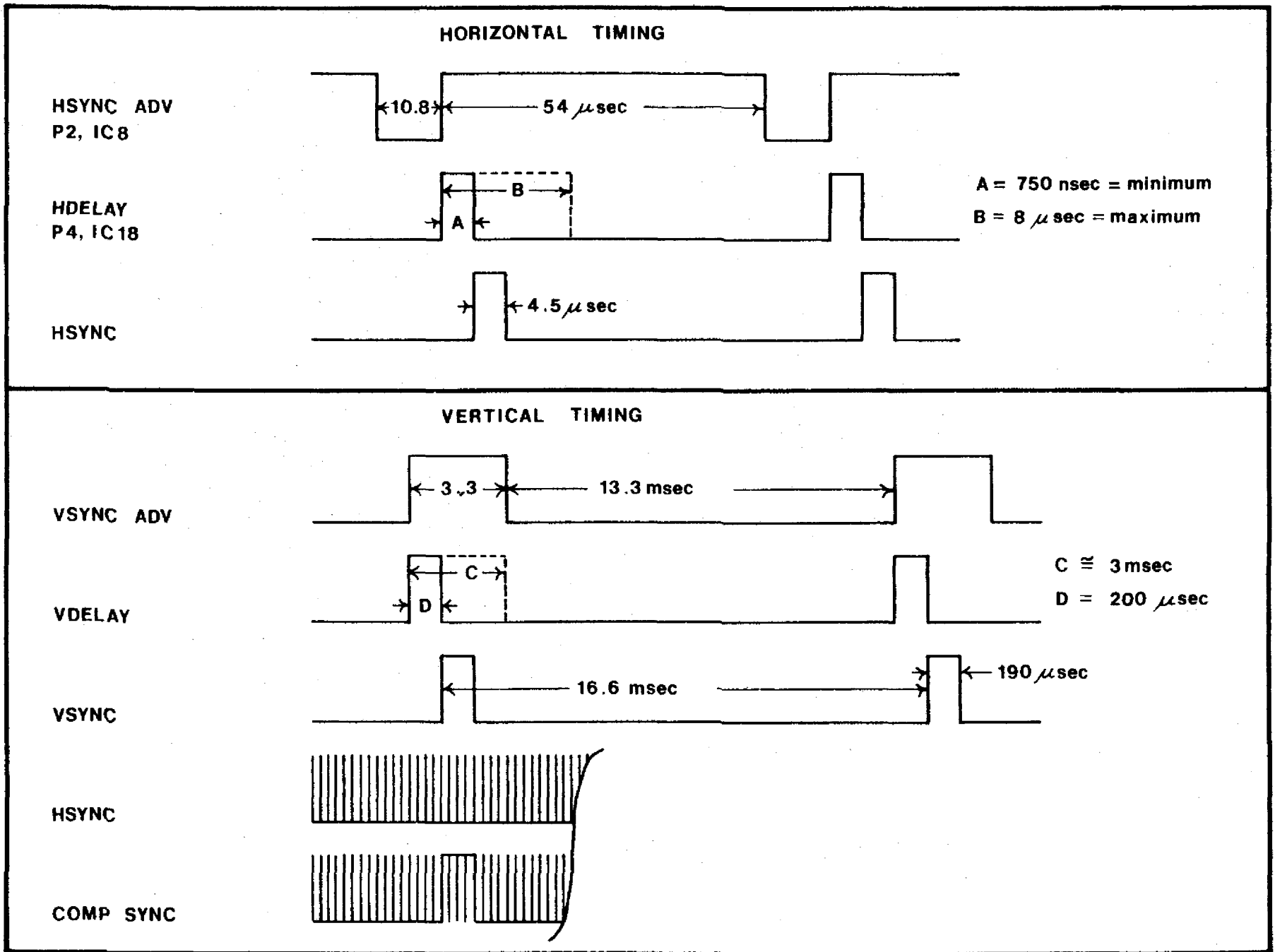
Plug a CPU into the computer and connect the front panel.
Close switches at Positions 3 thru 8.
Turn on and hit rest and examine location 0

- A) ENABLE at IC 37 pin 9
Should be low
- B) ACCESS BLANK at IC 10 pin 8
Should be low
- C) ADDRESS MUX

at IC 19 pin 1 - should be high
at IC 19 pin 15 - should be low
- D) Deposit each data bit, one at a time.
These should then appear on the front panel data lights.
- E) Check IC 34 pins 8, 6, 16, 4, 1, 2, 15, 14, 5, 7
All should be low
- F) Examine location 03FF
Repeat step E but all should be high

7) Cursor

- A) Cursor Blink at IC 6 pin 13
Square wave with period of 1 sec
- B) Open switch at Position 2
Deposit FF at location 0
Connect video monitors
Cursor should blink



SYNC TIMING

FIG. 5

A E000

E000		0005	*		
E000		0010	*		
E000		0015	*SOFTWARE VIDEO DRIVER FOR IA-1100, VBI-R, & VDM		
E000		0020	*		
E000		0025	*CHANGE SCROLLING SPEED BY TYPING A NUMBER DURING OUTPUT		
E000		0030	* (1(FAST))-9(SLOW))		
E000		0035	*		
E000		0040	*STOP DISPLAY BY TYPING SPACE BAR, RESTART BY TYPING		
E000		0045	* ANY OTHER CHARACTER		
E000		0050	*		
E000		0055	*CALL ROUTINE AT 'STRT' WITH CHARACTER IN ACCUMULATOR		
E000		0060	*		
E000		0065	*NOTE: A SCREEN CLEAR (CTRL-L) MUST BE FIRST CHARACTER SENT		
E000		0070	* TO DRIVER UPON SYSTEM INITIALIZATION TO SET UP SCREEN		
E000		0075	* AND PROPER SCROLLING		
E000		0080	*		
E000		0085	*MAY BE PLACED IN PROM IF SCRATCHPAD RAM IS PROVIDED		
E000		0090	* FOR "VDMF" AND "NEWSP". ALSO, THIS DRIVER USES		
E000		0095	* ABOUT 16 BYTES OF THE USER'S STACK.		
E000		0100	*		
E000		0105	*MAY 4, 1978 REF: DR. DOBB'S JOURNAL, V#2, ISSUE 10, P. 13		
E000		0110	*		
E000	E5	0115	STRT	PUSH H	#SAVE SYSTEM REGISTERS
E001	D5	0120		PUSH D	
E002	C5	0125		PUSH B	
E003	F5	0130		PUSH PSM	#CHARACTER IN ACCUM.
E004	2A D2 E0	0135		LHLD VDMP	#GET SCREEN POSITION POINTER
E007	FE 00	0140		CPI 0DH	#IS IT A CARRIAGE RETURN?
E009	CA 28 E0	0145		JZ CR	#YES, SCROLL, OUTPUT A CR
E00C	FE 5F	0150		CPI 5FH	#IS IT AN UNDERLINE(BACKSPACE)?
E00E	CA 22 E0	0155		JZ BS	#YES, MOVE CURSOR BACK
E011	FE 0C	0160		CPI 0CH	#IS IT A CTRL-L (FORM FEED)
E013	CA B0 E0	0165		JZ CLEAR	#YES-ERASE ENTIRE SCREEN
E016	FE 20	0170		CPI 20H	#DON'T DISPLAY CONTROL CHARACTERS
E018	DA 6D E0	0175		JC SPEED	#EXIT TO CHANGE SPEED
E01B	77	0180		MOV M:A	#IT MUST BE DATA
E01C	23	0185		INX H	#UPDATE SCREEN POSITION
E01D	36 A0	0190		MVI M:0A0H	#PUT CURSOR ON SCREEN
E01F	C3 34 E0	0195		JMP LINDV	#TEST FOR LINE OVERFLOW
E022	36 20	0200	BS	MVI M:20H	#REMOVE CURSOR
E024	2B	0205		DCX H	#BACK UP POINTER
E025	C3 1D E0	0210		JMP BS-5	
E02B	36 20	0215	CR	MVI M:20H	#CHAR IS A CARRIAGE RETURN
E02A	7D	0220		MOV A:L	#UPDATE NEXT CHAR POSITION
E02B	E6 00	0225		ANI 000H	
E02D	C6 40	0230		ADI 40H	#SETTING UP FOR NEW LINE
E02F	6F	0235		MOV L:A	#ADDRESS OF NEW LINE
E030	3E 00	0240		MVI A:0	
E032	8C	0245		ADC H	
E033	67	0250		MOV H:A	
E034	22 D2 E0	0255	LINDV	SHLD VDMP	#SAVE POINTER FOR NEXT CHAR
E037	3E 7F	0260		MVI A:7FH	
E039	A5	0265		ANA L	
E03A	C2 6D E0	0270		JNZ SPEED	#EXIT
E03D	36 20	0275		MVI M:20H	
E03F	21 C0 CF	0280		LXI H:0CFC0H	#SET UP DATA LINE (LINE 16)

*Change
to FF*

-22-

35 32 00 58

D3

E042	22	D2 E0	0285	SULD	VDMF
E045	21	40 CC	0280	LXI	H:0CC40H
E048	11	00 CC	0285	LXI	D:0CC00H
E04B	01	C0 03	0300	LXI	E:03C0H
E04E	7E		0305	SCROL	MOV A:M
E04F	12		0310	STAX	D
E050	23		0315	INX	H
E051	13		0320	INX	D
E052	0B		0325	DCX	B
E053	AF		0330	XRA	A
E054	B8		0335	CMP	B
E055	C2	4E E0	0340	JNZ	SCROL
E058	B9		0345	CMP	C
E059	C2	4E E0	0350	JNZ	SCROL
E05C	21	C0 CF	0355	LXI	H:0CFC0H
E05F	36	20	0360	ERASE	MVI M:20H
E061	23		0365	INX	H
E062	7D		0370	MOV	A:L
E063	E6	3F	0375	ANI	3FH
E065	C2	5F E0	0380	JNZ	ERASE
E068	21	C0 CF	0385	LXI	H:0CFC0H
E06B	36	A0	0390	MVI	M:0A0H
E06D	CD	D6 E0	0395	SPEED	CALL STATS
E070	C4	B4 E0	0400	CNZ	GETIT
E073	3A	D4 E0	0405	LDA	NEWSP
E076	67		0410	MOV	H:A
E077	2E	80	0415	MVI	L:80H
E079	2B		0420	DELAY	ICX H
E07A	7C		0425	MOV	A:H
E07B	B7		0430	ORA	A
E07C	C2	79 E0	0435	JNZ	DELAY
E07F	F1		0440	POP	PSW
E080	C1		0445	POP	B
E081	D1		0450	POP	D
E082	E1		0455	POP	H
E083	C9		0460	RET	
E084	CD	DB E0	0465	GETIT	CALL DATA
E087	FE	3A	0470	CPI	'9'+1
E089	D2	A6 E0	0475	JNC	WAIT
E08C	FE	31	0480	CPI	'1'
E08E	DA	A6 E0	0485	JC	WAIT
E091	F5		0490	PUSH	PSW
E092	E6	0F	0495	ANI	0FH
E094	C5		0500	PUSH	B
E095	4F		0505	MOV	C:A
E096	AF		0510	XRA	A
E097	37		0515	STC	
E098	0D		0520	LESS	DCR C
E099	CA	A0 E0	0525	JZ	FOUND
E09C	17		0530	RAL	
E09D	C3	98 E0	0535	JMP	LESS
E0A0	C1		0540	FOUND	POP B
E0A1	32	D4 E0	0545	STA	NEWSP
E0A4	F1		0550	POP	PSW
E0A5	C9		0555	RET	
E0A6	FE	20	0560	WAIT	CPI 20H
E0A8	C0		0565	RNZ	
E0A9	CD	D6 E0	0570	WAIT2	CALL STATS
E0AC	CA	A9 E0	0575	JZ	WAIT2
E0AF	C9		0580	RET	
E0B0	21	00 CC	0585	CLEAR	LXI H:0CC00H
E0B3	3E	AA	0590	MVI	A:NFLAG

#SAVE POINTER
#15 LINES OF SCREEN DATA
#STOP OF SCREEN SET UP
#TO SCROLL 15 LINES
#START SCROLLING UP

#COUNT DOWN
#CLEAR STATUS WORD
#15 LINES SCROLLED?
#NOT YET COMPLETE

#STILL NOT COMPLETE
#RESET DATA LINE TO LINE 16
#PUT BLANK ON SCREEN

#LINE NOT YET ERASED
#RESET DATA LINE TO LINE 16
#PUT CURSOR ON SCREEN
#LOOK AT KEYBOARD STATUS
#IF BUSY, GET ASCII DATA
#LOAD NEW SPEED BYTE
#CHANGE SPEED WITH ASCII 1-9

#DELAY ROUTINE FOR VARIABLE
OUTPUT SPEED

#JUMP FOR MORE TIME
#GET READY TO RETURN TO USER PROGRAM

#INPUT ASCII FROM KEYBOARD
#IS CHAR AN ASCII 1-9?
#TOO BIG

#TOO SMALL

#REMOVE ASCII BIAS
#SAVE TEMPORARILY
#SAVE DELAY NUMBER
#CLEAR ACCUMULATOR
#INITIALIZE DELAY CARRY BIT
#DECREASE DELAY NUMBER
#STOP ROTATING DELAY BIT
#SHIFT DELAY BIT LEFT
#NEXT ROUND
#RESTORE REGISTERS

#IS IT A SPACE BAR?
#NO-CONTINE
#WAIT TILL A KEY IS PRESSED
BEFORE CONTINUING

#CLEAR SCREEN

84 up

85

change

change

1001

E0B5 32 FF CF	0595	STA	SCREEN	!SAVE FLAG IN LAST SCREEN LOCATION
E0B8 3E 20	0600	CLER1 MVI	A:20H	
E0BA 77	0605	MOV	M:A	
E0BB 23	0610	INX	H	
E0BC 3A FF CF	0615	LDA	SCREEN	
E0BF FE 20	0620	CPI	20H	
E0C1 C2 B8 E0	0625	JNZ	CLER1	!CONTINUE CLEARING
E0C4 21 C0 CF	0630	DQNT LXI	H:0CFC0H	!RESET DATA LINE TO LINE 16
E0C7 36 A0	0635	MVI	M:0A0H	!RESTORE CURSOR TO SCREEN
E0C9 22 D2 E0	0640	SHLD	VDMF	!SAVE SCREEN POINTER
E0CC AF	0645	XRA	A	
E0CD D3 CB	0650	OUT	0CBH	!CLEAR VDM-1 STATUS LATCH
E0CF C3 6D E0	0655	JMP	SPEED	
E0D2	0660	VDMF	DS	
E0D4 00 00	0665	NEWSP	DH	
E0D6	0670	NFLAG	EQU	0AAH
E0D6	0675	SCREEN	EQU	0CFFFH
E0D6	0680	*		
E0D6	0685	*THESE ARE AUXILIARY ROUTINES FOR I/O THAT ARE		
E0D6	0690	* NORMALLY PART OF THE CALLING PROGRAM, THEY ARE		
E0D6	0695	* USED HERE FOR INPUT OF SCROLLING SPEED FROM		
E0D6	0700	* THE KEYBOARD		
E0D6	0705	*		
E0D6	0710	STAT	EQU	0D5H
E0D6	0715	KBD	EQU	0D4H
E0D6 DB D5	0720	STATS	IN	STAT
E0D8 E6 B0	0725	ANI	B0H	!INPUT FROM STATUS PORT
E0DA C9	0730	RET		!LOOK AT STATUS BIT ONLY
E0DB DB D4	0735	DATA	IN	KBD
E0DD E6 7F	0740	ANI	7FH	!INPUT FROM DATA PORT
E0DF C9	0745	RET		!STRIP PARITY

SYMBOL TABLE

RS	E022	CLEAR	E0B0	CLER1	E0B8	CR	E028	DATA	E0DB	DELAY	E079
DQNT	E0C4	ERASE	E05F	FOUND	E0A0	GETIT	E0B4	KBD	00D4	LESS	E098
LINOV	E034	NEWSP	E0D4	NFLAG	00AA	SCREEN	CFFF	SCROL	E04E	SPEED	E06D
STAT	00D5	STATS	E0D6	STRT	E0C0	VDMF	E0D2	WAIT	E0A6	WAIT2	E0A9

CF ~
CF
G1

E0D3
{E0D4
E0D5}

REVISIONS LIST

IA-1100 Video Display Board

- Rev. 0 Initial Release
- Rev. A The board has been improved with the addition of a 50/60 Hz jumper option and a composite video jack.

PARTS LIST

INTEGRATED CIRCUITS

U1	7406
U2, U17	74LS20
U3, U10	74LS74
U4	74LS86
U5	74166 or 74LS166
U6	4049
U7	74LS04
U8, U16	74LS221
U9, U14	74LS00
U11, U18, U25, U26, U27, U28	74LS163
U12	6571A or 6574 (Motorola)
U13	74LS10
U15	74LS32
U19, U24, U29, U30, U35	74LS367
U20, U21, U22, U23,	
U31, U32, U33, U34	21F02 (250ns - 2102)
U37	8131

CAPACITORS

C1, C7001 uf (1000 pf) ceramic
C2	10 pf ceramic
C3, C4, C14, C15, C16	10 uf electrolytic
C5, C6, C201 uf ceramic
C8, C10, C11, C12,	
C18, C19, C2101 to .1 uf ceramic
C9	100 uf electrolytic
C17	470 pf ceramic
C22	1 to 10 uf electrolytic

All capacitors should have a working voltage of 15 volts or higher.

PARTS LIST CONTINUED

RESISTORS

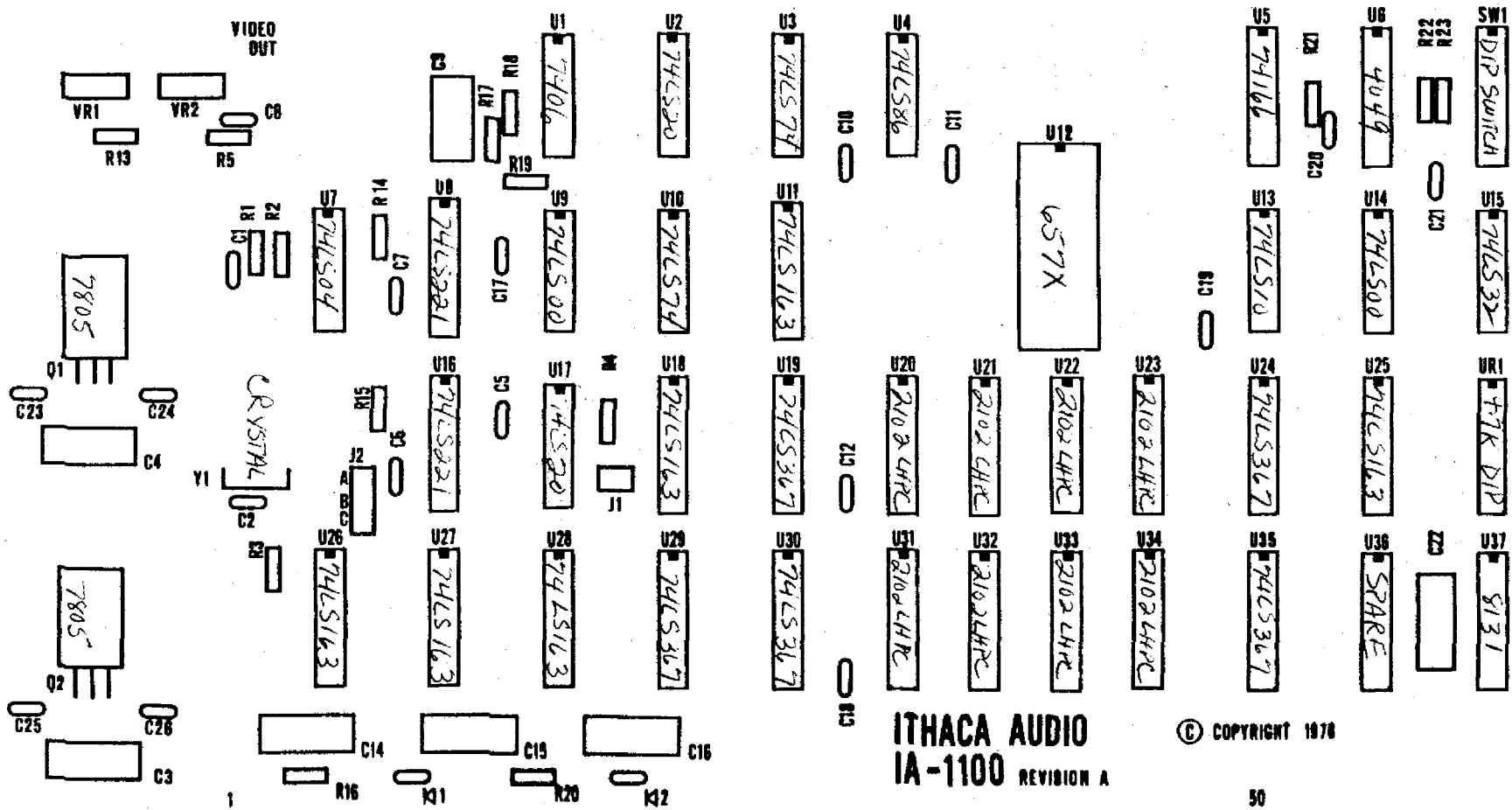
R1, R2.	300 ohms, .25 watts
UR1	4.7K ohms, DIP res. pac
R3, R4, R14, R23.	4.7K ohms, .25 watts
R5, R13	2.7K ohms, .25 watts
R15, R22.	10K ohms, .25 watts
R16	100 ohms, .5 watts
R17	330 ohms, .25 watts
R18	270 ohms, .25 watts
R19	75 ohms, .25 watts
R20	1000 ohms, .5 watts
R21	5.6 meg. ohms, .25 watts
VR1, VR2.	50K ohm trimpot

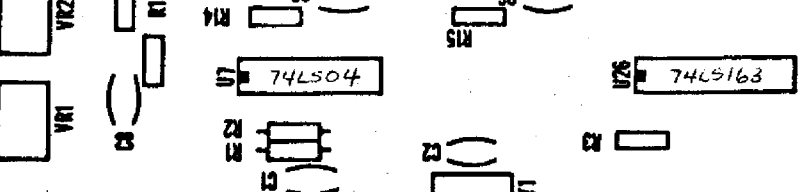
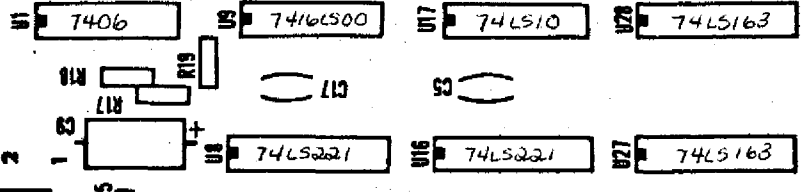
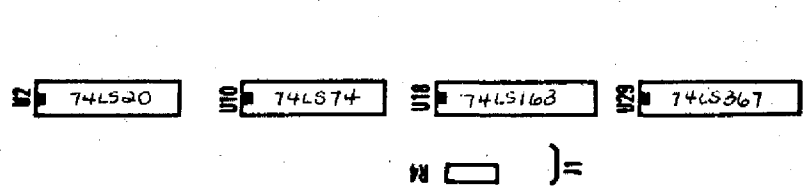
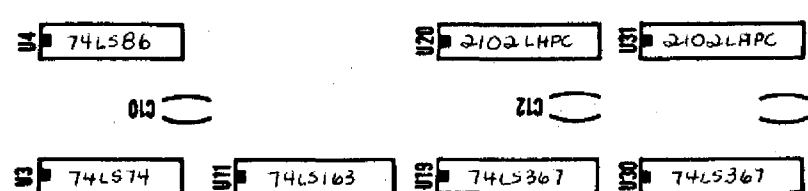
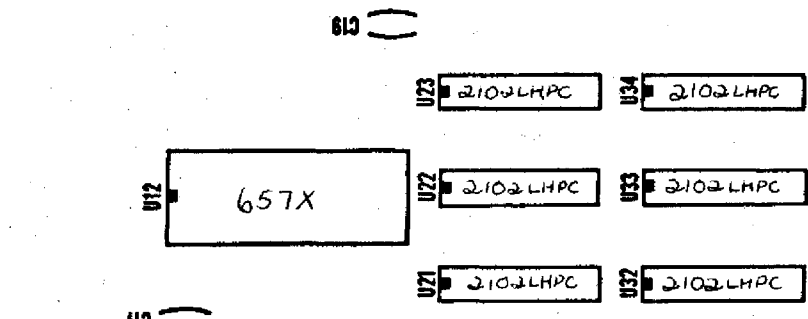
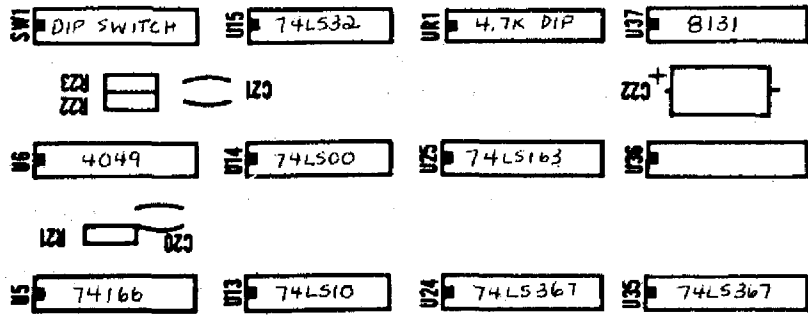
Note: R6 - R12 have been replaced by UR1.

MISCELLANEOUS PARTS

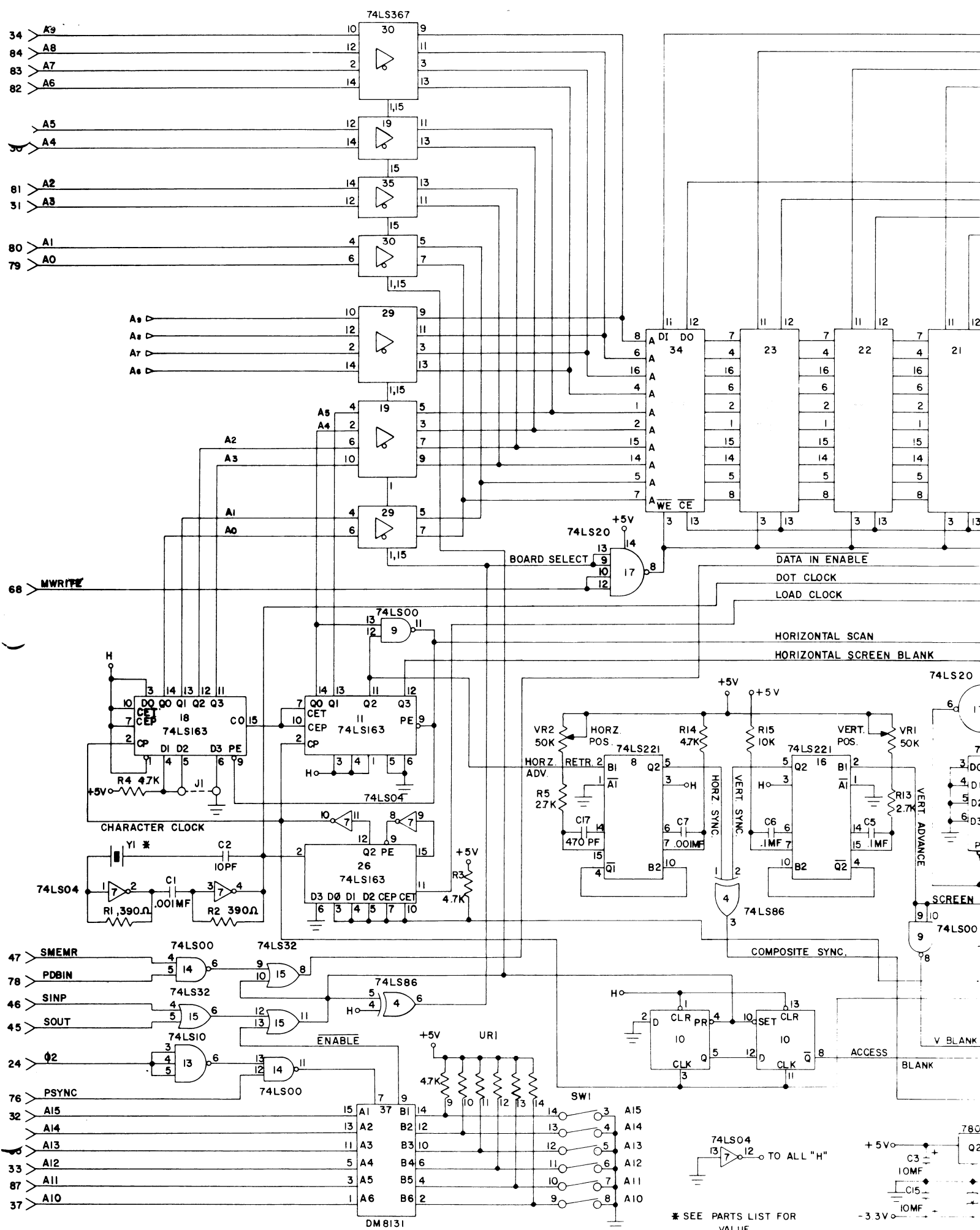
Q1, Q2.	7805 (LM340T-5) voltage regulators
Y1.	13.478 or 12.636 series resonant crystal
D1.	12 volt zener diode, 1 watt
D2.	3.3 volt zener diode, 1 watt

- 1 SPST eight position DIP switch
- 25 sixteen-pin IC sockets
- 11 fourteen-pin IC sockets
- 1 twenty-four pin IC socket
- 1 video output cable with male RCA connector
- 1 RCA phono jack (female receptor)
(such as IEH PJP5116-1 or SIK Electronics SQ 3081)

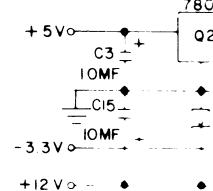


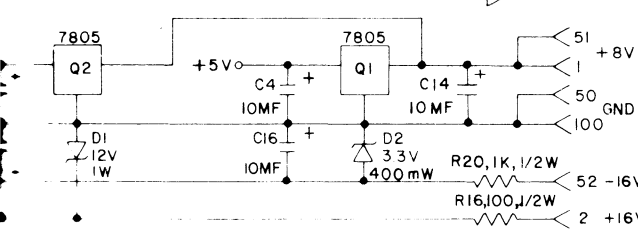
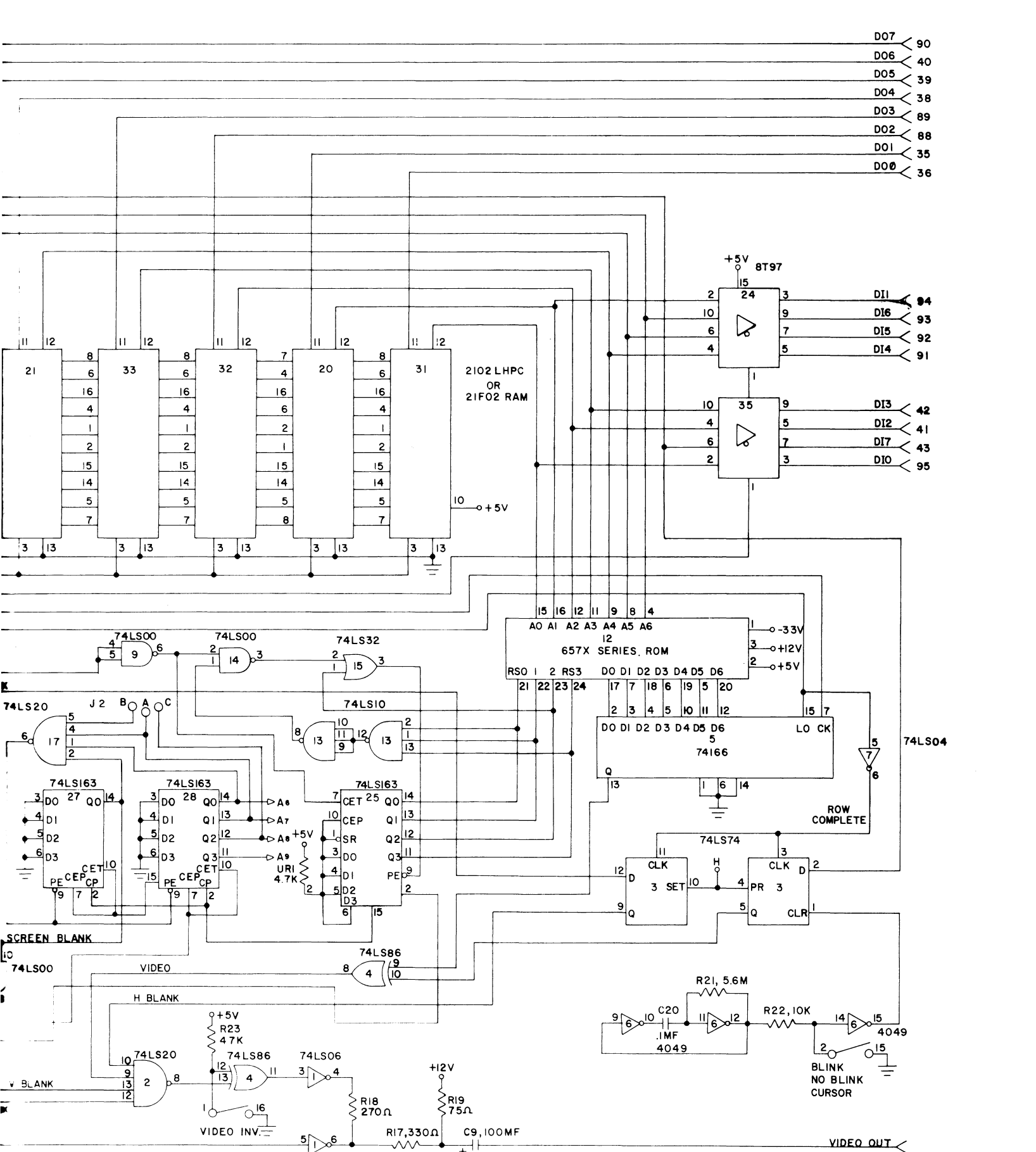


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* SEE PARTS LIST FOR VALUE





SCALE	SHEET	OF
DRAWN	J L AMEIGH	DATE 10/11/78
CHECKED	A B FALLEN	DATE
MATERIAL		
UNLESS OTHERWISE NOTED		
FRACTIONS	00	000
±	±	±
RADII	DRAFT	FINISH

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PROJECT	
VIDEO DISPLAY REV A	
DATE	NUMBER
5/1/79	IA-1100 REV A

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