# IMS INTERNATIONAL

# MODEL 451

# Z80 PROCESSOR BOARD

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## GENERAL DESCRIPTION

The Model 451 Processor is the Central Process ng Unit (CPU) of the IMS International Series 5000 and 8000 Computer Systems. The Model 451 provides control for the system.

Control is accomplished by the Z-80A CPU LSI (Large Scale Integration) Micro Processor device. This is a fully Parallel 8-bit, Bi-Directional, Bus Oriented Processing Unit with a 16-bit address capability, allowing up to 64 Kbytes of directly addressable memory. The Z-80A CPU has a 1 usec instruction cycle time.

The Model 451 processor consists of a single Printed Circuit Board that can occupy any slot in the Series 5000 or 8000 Computer Systems. It interfaces with the rest of the system through the address, data, and control lines of the S-100 Bus System.

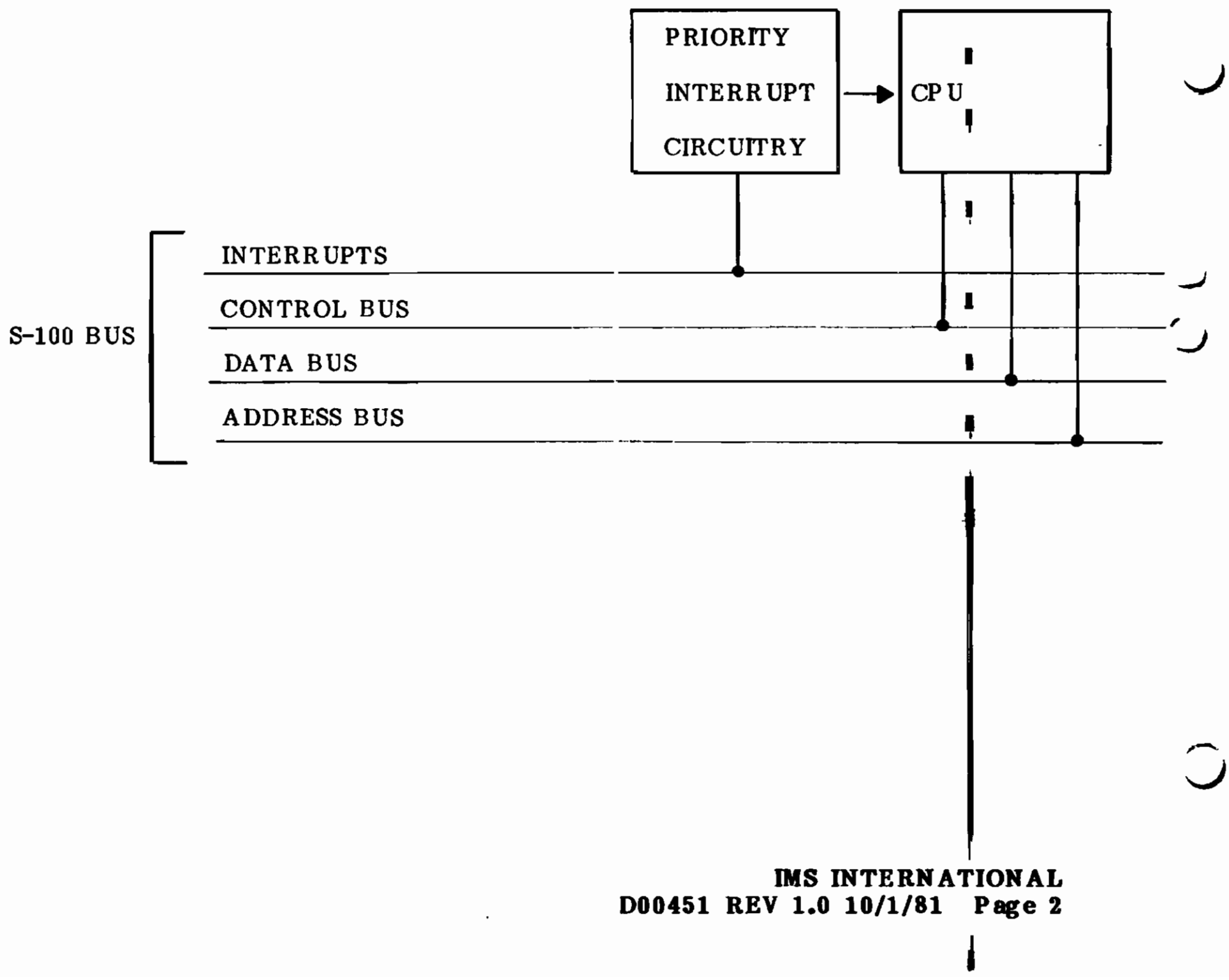
The 451 Processor Board consists of the following functional divisions (See Figure 1).

- Z-80 8-bit Microprocessor Device (CPU)
- Priority Vectored Interrupt Circuitry
- S100 Bus Interface

## SPECIFICATIONS

- Word Size: Address 16-bits
- Data 8-bits
- Directly Addressable Memory: 64Kbytes
- Clock Frequency: 4 MHz
- PCB Dimensions: 5.25" x 10"
- Power Requirements: +8 @ 700 ma

**FIGURE 1 - Z80 CPU BLOCK DIAGRAM**



## Z-80A CPU MICROPROCESSOR

The Z-80 Processor is a Bi-Directional, Bus-Oriented, 8-bit Parallel LSI device with a 16-bit address capability, allowing up to 64 Kbytes of directly addressable memory. The Z-80 contains six 8-bit, general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The Z-80 has an external stack feature wherein any portion of memory may be used as a last-in/first-out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the six general-purpose registers. The 16-bit stack pointer contains the address of the next available location in the external memory. The program counter is a 16-bit register that contains the program address. The flag register contains six bits of condition code information which indicate the results of the ALU (Arithmetic Logic Unit) operation; Negative (N), Zero (Z), Overflow (V), Carry from Bit 7 (C), and Half-Carry from Bit 3 (H). These are used as testable conditions for the conditional branch instructions. This stack feature allows the ability to provide priority vectored interrupts.

The minimum instruction time for the Z-80 Microprocessor is 1 usec. Separate 16-bit address and 8-bit bi-directional data lines are used to facilitate easy interface to memory and I/O.

Memory and I/O interface control signals may be used to suspend processor operation and force the address and data lines to a high impedance state (Tri-State) allowing Direct Memory Access (DMA) and multi-processor operation.

The Z-80 provides 158 variable length instructions (see Z-80 instruction set). In addition to performing basic processing functions, the processor is capable of responding to Real-Time Program Interrupts, Automatic Restart in response to the RESET/Power-On RESET signals, and Direct Memory Access operations.

## HARDWARE SUMMARY

The instruction set of the 451 is that of the Z-80A Microprocessor Device. The Processor has a 1 usec instruction cycle time, the ability to provide priority vectored interrupts, and the capability for 256 bi-directional I/O ports.

## FUNCTIONAL OVERVIEW

The S-100 bus interface consists of three separate sets of lines:

1. Address Lines
2. Data Lines
3. Control Lines

**ADDRESS** - The 16 address lines (A0-A15) allow each of 65,536 bytes of memory to be uniquely addressed.

The address lines are utilized by either the Microprocessor or Direct Memory Access (DMA) device, such as the Disk Controller. These lines are decoded by each memory module so that only one memory location is addressed by an exclusive bit pattern.

**DATA** - The data lines are further sectioned into two sets of lines:

1. Input Data
2. Output Data

The input data lines (DI0-DI7) carry the binary data in parallel from the memory to the 451 Processor.

The output lines (DO0-DO7) carry the binary data in parallel from the 451 Processor to memory.

**CONTROL** - The remaining bus lines perform various control functions:

1. Timing
2. Synchronization
3. Data Direction
4. Status

**TIMING AND SYNCHRONIZATION** - These control lines are:

| | |
|---|---|
| pSYNC | pHLDA |
| pSTVAL | RDY |
| pDBIN | XRDY |
| pWR | CLOCK |
| pWAIT | O CLOCK |

The 16 MHz oscillator provides the base frequency for the microprocessor. From this circuit O CLOCK at 4MHz and CLOCK at 2MHz are derived for use on the S-100 bus.

**STATUS** - The status signals and the correspording data bits are as follows:

| BIT | STATUS TERM |
|---|---|
| D0 | sMEMR |
| D1 | sINP |
| D2 | sM1 |
| D3 | sOUT |
| D4 | sHLTA |
| D5 | |
| D6 | sWO |
| D7 | sINTA |

The eight status lines are placed on the bus by the microprocessor to be selectively used by the memory and I/O board to obtain information as to the nature of the cycle.

**INTERRUPTS** - The vectored priority interrupt system consists of eight interrupt lines. Refer to the 440 I/O Board documentation for a description of these lines.

The interrupt function is to indicate to the CPU that there are peripheral devices that need to be serviced. When the priority requirements are fulfilled, the CPU goes into the Interrupt Service Routine and responds to the device requesting the interrupt.

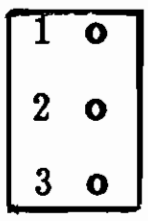
## MODEL 451 P1 SIGNAL LIST

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | +8V | 51 | +8V |
| 2 | | 52 | |
| 3 | XRDY+ | 53 | SSWDSB- |
| 4 | VI0- | 54 | |
| 5 | VI1- | 55 | |
| 6 | VI2- | 56 | |
| 7 | VI3- | 57 | |
| 8 | VI4- | 58 | |
| 9 | VI5- | 59 | |
| 10 | VI6- | 60 | |
| 11 | VI7- | 61 | |
| 12 | NMI- | 62 | |
| 13 | | 63 | |
| 14 | | 64 | |
| 15 | | 65 | |
| 16 | | 66 | |
| 17 | | 67 | |
| 18 | SDSB- | 68 | MWRT+ |
| 19 | CDSB- | 69 | |
| 20 | GND | 70 | GND |
| 21 | | 71 | RUN+ |
| 22 | ADSB- | 72 | RDY+ |
| 23 | DODSB- | 73 | INT- |
| 24 | O CLOCK | 74 | HOLD- |
| 25 | pSTVAL- | 75 | RESET- |
| 26 | pHLDA+ | 76 | pSYNC+ |
| 27 | pWAIT+ | 77 | pWR- |
| 28 | | 78 | pDBIN+ |
| 29 | A5+ | 79 | A0+ |
| 30 | A4+ | 80 | A1+ |
| 31 | A3+ | 81 | A2+ |
| 32 | A15+ | 82 | A6+ |
| 33 | A12+ | 83 | A7+ |
| 34 | A9+ | 84 | A8+ |
| 35 | DO1+ | 85 | A13+ |
| 36 | DO0+ | 86 | A14+ |
| 37 | A10+ | 87 | A11+ |
| 38 | DO4+ | 88 | DO2+ |
| 39 | DO5+ | 89 | DO3+ |
| 40 | DO6+ | 90 | DO7+ |
| 41 | DI2+ | 91 | DI4+ |
| 42 | DI3+ | 92 | DI5+ |
| 43 | DI7+ | 93 | DI6+ |
| 44 | sM1+ | 94 | DI1+ |
| 45 | sOUT+ | 95 | DI0+ |
| 46 | sINP+ | 96 | sINTA+ |
| 47 | sMEMR+ | 97 | sWO- |
| 48 | sHLTA+ | 98 | |
| 49 | CLOCK | 99 | POC- |
| 50 | GND | 100 | GND |

# CONFIGURING THE 451 Z-80 CPU BOARD

## Wait State Select

JA



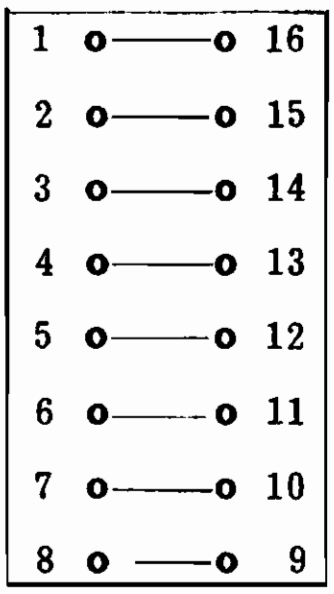

No shunts = No memory wait state

Shunt JA 1-2 = Provides one wait state

Shunt JA 2-3 = Provides two wait states

## Power On Address Select

JB




A15 Shunt Off = 1 Shunt on=0

A14 All Shunts Off = Power on Address X'FF00'

A13 All Shunts On = Power on Address X'0000'

A12

A11 Standard Configuration = Power on Address X'0000'

A10

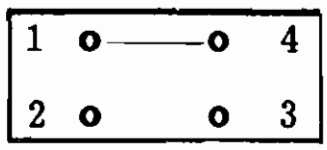
A9

A8

## CPU Clock Select

Cut etch jumper to change CPU clock

JC

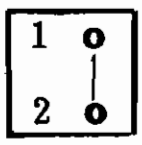



4MHz

2MHz

## Address Mirror Select

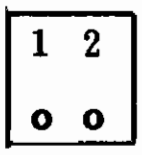
JD




Cut etch jumper for no address mirror

## MWRITE + ENABLE

JE




Shunt JE 1-2 = Puts MWRITE + Signal on S100-Bus - Pin 68

| REV | DESC. OF CHANGE | ECO NO. | DATE | BY |
|---|---|---|---|---|
| A | FINAL RELEASE | 10001 | 072981 | RJV |
| B | SHT 4: IC "00" PIN 13 IS: +5V WAS: BUSACK- | 10013 | 081481 | RJV |

+5
C4 39 PF
R2 220
R1 22
R3 1.2K
Q1 2N3906
ØZ-
2A 04
12AB
Z80
Φ
D7+ D6+ D5+ D4+ D3+ D2+ D1+ D0+
D7 D6 D5 D4 D3 D2 D1 D0
WAIT- INT-
WAIT INT
NMI-
BUSRQ-
RESET
A15+ A14+ A13+ A12+ A11+ A10+ A9+ A8+ A7+ A6+ A5+ A4+ A3+ A2+ A1+ A0+
HALT- MREQ- IØRQ- RD- WR- BUSACK- MI- RFSH-
PNMI- 12
PHØLD- 74
11B 244
1K 10C +5
11B 244
BUSRQ-
1K 10C +5
R7 33K
CR1
CR2
PRESET- 75
11C 240
C13 6.6UF 25V
+5
4B 74
PR D Q C Q CL
RESET-
4C 244
99 PSC-
11C 240
49 CLK-
2A 04
ØZ+
ØZ-
4B 74
4C 244
24 PHZ2+
12C 02
4C 244
23 PHZ1+
3B 161
PE P3 P2 P1 P0 CEP CET CP
TC Q3 Q2 Q1 Q0 R
4MHZ 8MHZ
JC
Y1 16.00 MHZ
R5 680
R6 2.7K
CV 4024 Ø
2B
2A 04

1. ALL RESISTORS ARE 1/4W ± 5%
2. ALL DIODES ARE SILICON SWITCHING

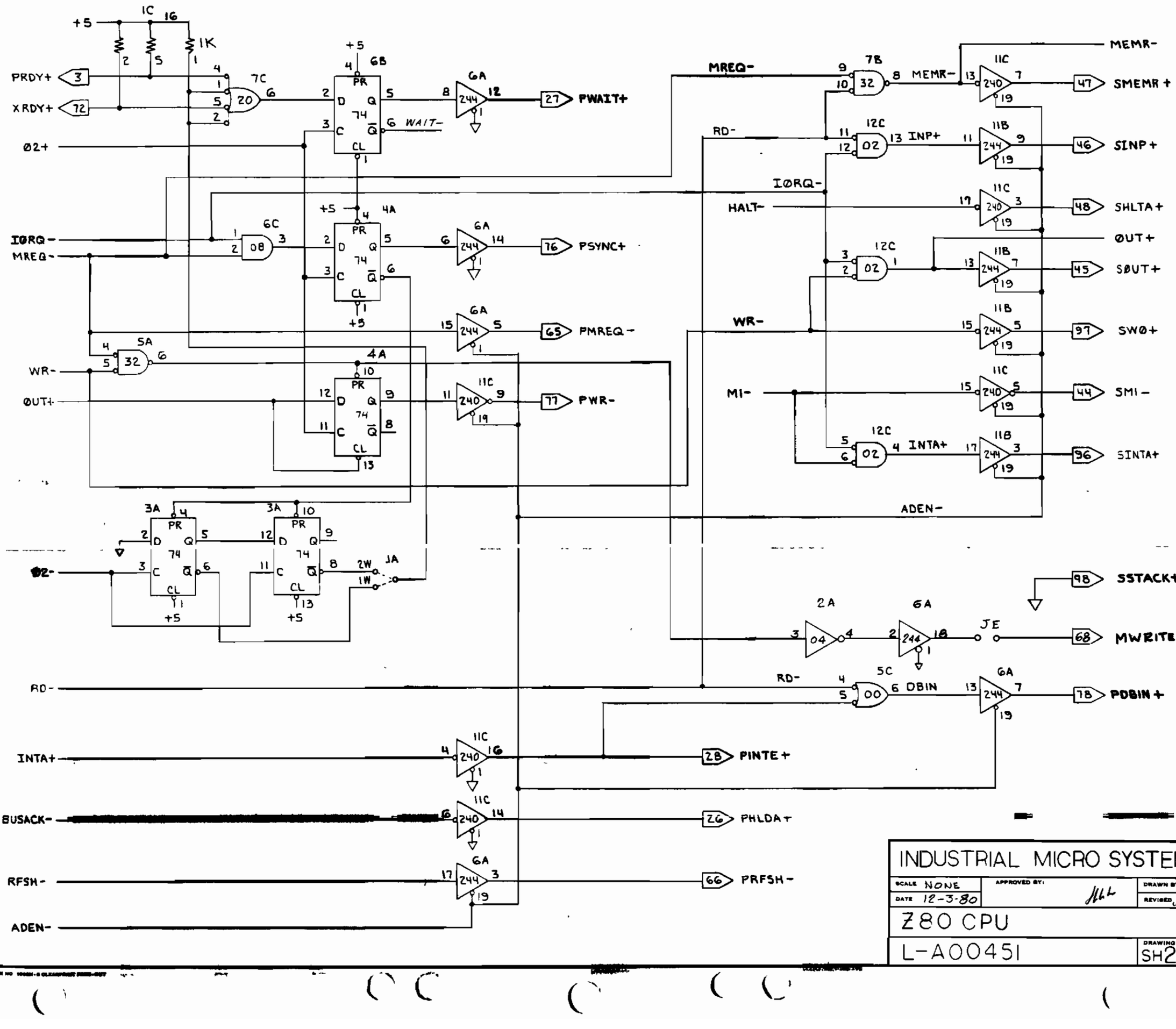
INDUSTRIAL MICRO SYSTEMS

| | | |
|---|---|---|
| SCALE NONE | APPROVED BY: | DRAWN BY RJV |
| DATE: 12-3-80 | | REVISED JULY 29, '81 |

Z80 CPU

L-A00451

DRAWING NUMBER SHT 1 OF 4




INDUSTRIAL MICRO SYSTEMS

| | | |
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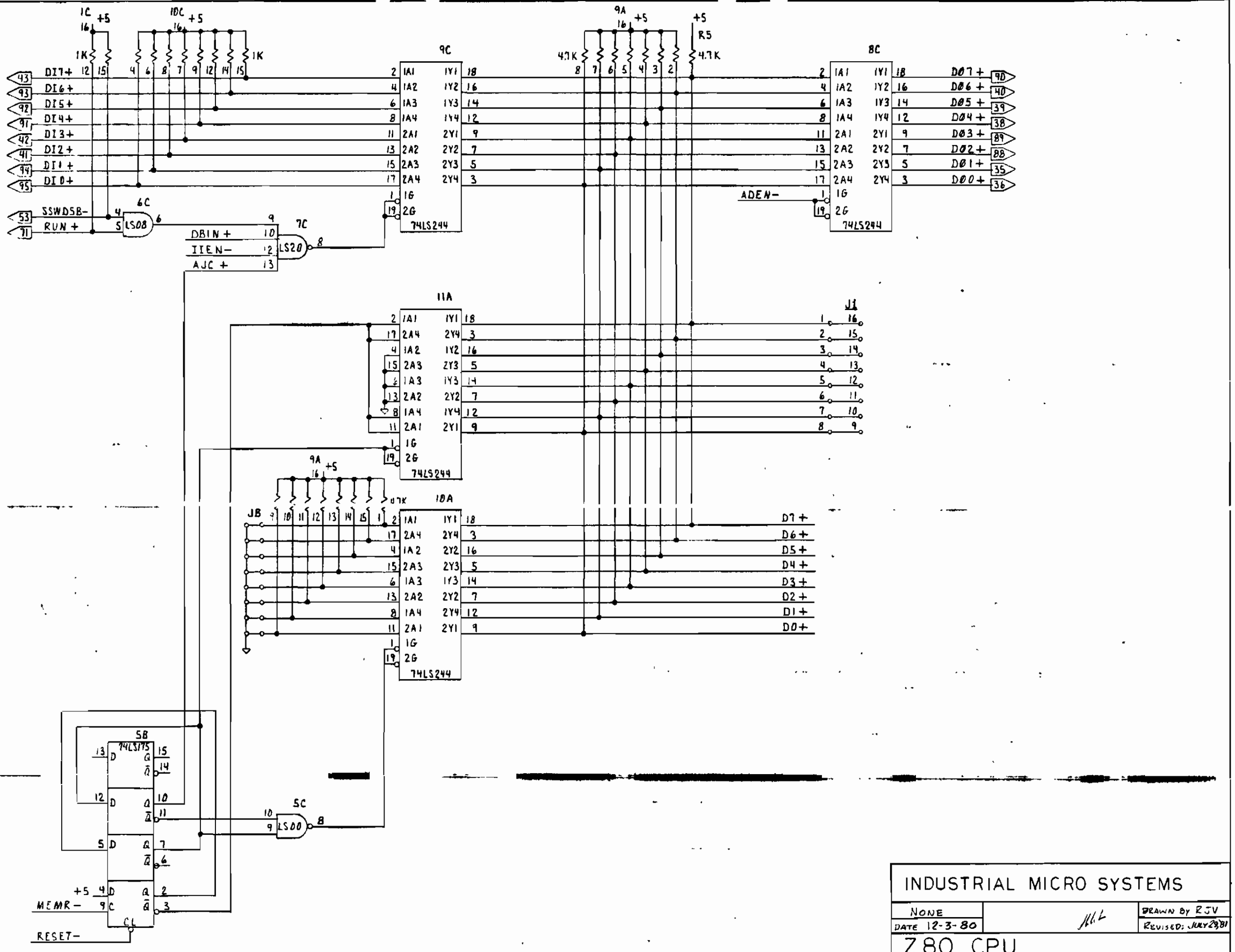
| DATE 12-3-80 | | REVISED July 29, 81 |

Z80 CPU

L-A00451

DRAWING NUMBER SH 2 OF 4

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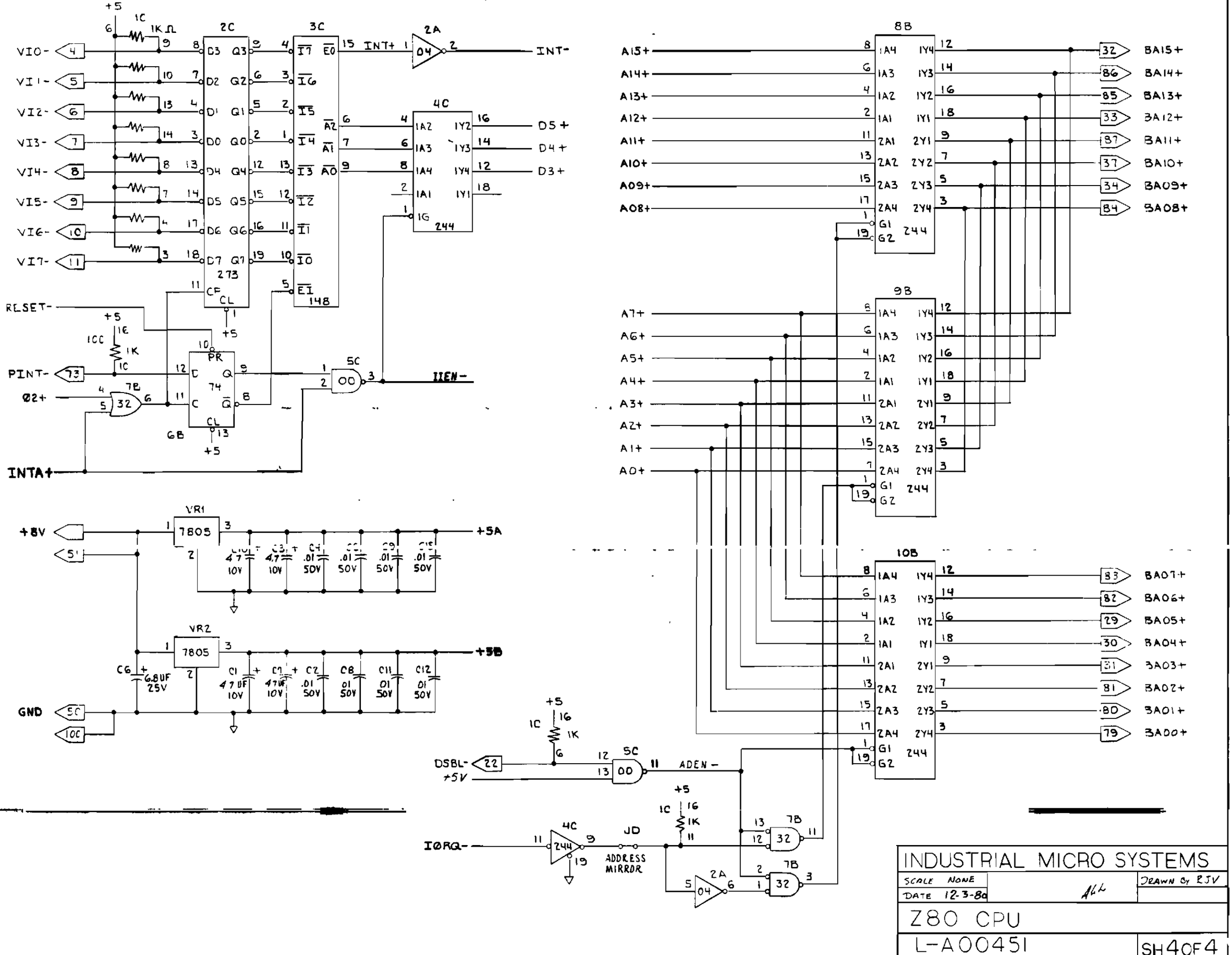
| INDUSTRIAL MICRO SYSTEMS | | |
| NONE<br>DATE 12-3-80 | MLL | DRAWN BY RJV<br>REVISED: JULY 29 81 |
| Z80 CPU | | |
| L-A00451 | | SH 3 OF 4 |




| | | |
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| INDUSTRIAL MICRO SYSTEMS | | |
| SCALE NONE | ALL | DRAWN BY RJV |
| DATE 12-3-80 | | |
| Z80 CPU | | |
| L-A00451 | | SH 4 OF 4 |