CENTRAL PROCESSING UNIT 803439

MAINTENANCE

CONTENTS

ILLUSTRATIONS

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1. GENERAL

1.01 This manual provides a physical and functional description and the operating theory necessary for effective field service of the Central Processing Unit (CPU) 803439. The CPU is supplied in the Dynabyte 5100/5200 Computer Units.

Features

1.02 The CPU is designed for operation in the Dynabyte S-100 Bus. Features of the CPU include:

- A Z80 microprocessor.
- Switch-optioned Power-On-Jump to any 4K byte boundary.
- Two software baud rate selectable I/O ports.
- I/O ports may be either RS-232C or 20 mA current loop interface.

- One TTL 8-bit parallel I/O port with Strobe and Data Ready lines.
- Solder masked pc board.
- Each CPU carries 30-day warranty on parts and labor.
- Each CPU pc assembly (PCA) is burned in for a minimum of 72 hours.

1.03 Operational features of the Dynabyte S-100 Bus are described functionally in both the 5100 and 5200 Computer Technical Manuals. Table 7-1 in this manual summarizes the Dynabyte S-100 Bus pins by assignment and function.

1.04 Dynabyte maintains hardware and software compatibility with the Dynabyte S-100 Bus only. The CPU may not operate with all S-100 Bus computers. Contact Dynabyte, Inc., for specific applications.

2. PHYSICAL DESCRIPTION

2.01 The CPU is an integrated plug-in unit incorporating all the necessary components for a high-speed S-100 Bus processor including I/O ports. This printed circuit assembly (PCA) contains:

(1) A Z-80 microprocessor.

(2) A 8 MHz crystal-controlled clock for timing signals.

(3) A latch to hold status information.

(4) Line drivers and receivers connected to the S-100 Bus.

(5) Voltage regulators for powering the CPU logic.

Figure 2-1 illustrates the CPU.

2.02 The PCA measures 5 x 10 inches. A 100-pin edge connector mates with the S-100 Bus connector of the 5100/5200 Computer motherboard. This connector is offset by 5/8 inch from the pc board centerline, i.e., the PCA cannot be inserted into the motherboard backwards.

2.03 Distinctive white silkscreened marking has been provided on the component side of the PCA.

(1) The card name, Dynabyte part number and a location for the serial number have been marked on the pc board. Some early CPUs have the serial number etched on the pc board.

(2) Component reference designators are marked where practical. They facilitate locating the individual part on the schematic or replaceable parts list. Refer to Part 7.

The CPU integrated circuits and some major components derive their reference designators from the row-column matrix silkscreened onto the pc board. Refer to Figure 2-1. Rows are A to C and columns are 1 to 15. An integrated circuit located at the lower right corner is C15.

2.04 The PCA has three on-board regulators located at A1, B1 and C14.

(1) B1 provides +12 Vdc and is provided with an insulated heat sink.

(2) A1 provides +5 Vdc and is provided with an insulated heat sink.

(3) C14 provides −5 Vdc and is provided with an insulator.

If it becomes necessary to change one of these regulators, coat the mating surface with a thermal conductive cream. Secure the regulator to the surface with a screw and nut.

NOTE

The PCA should never be inserted or removed from the bus when the ac line is connected to the computer.

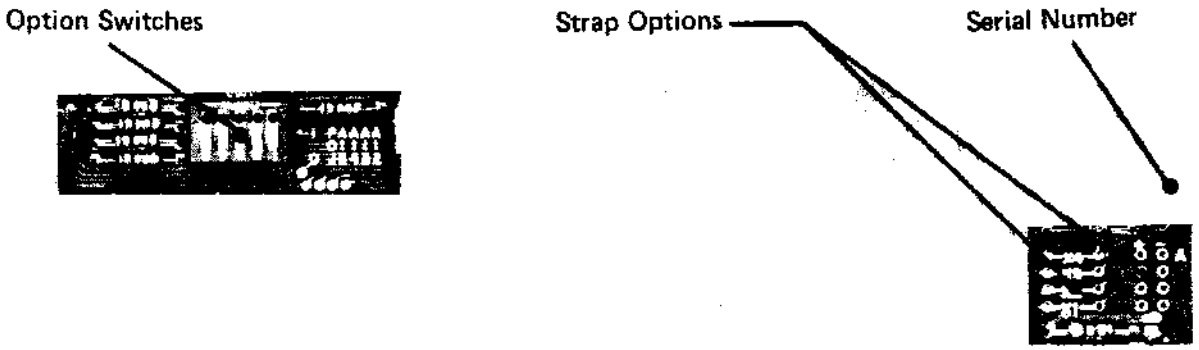

Figure 2-1 – Central Processing Unit – 803439

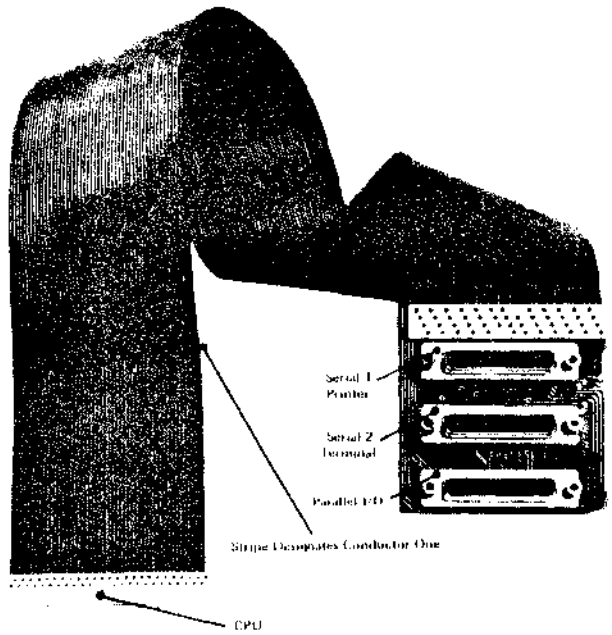

Figure 2 2 - CPU Port I/O Cable – 800285

2.05 The three groups of I/O port signals are exchanged with the external data terminals over a 50-conductor connector located along the top edge. The CPU I/O Cable, 800285, mates with this connector and extends the signals to the rear panel of the 5100/5200 Computer Unit. This is a 50-conductor flat cable.

IMPORTANT

Multi-conductor I/O cables are polarized with a painted strip on conductor one. This conductor is terminated at Pin One of the connector. This marking convention serves to polarize mating connectors.

Power-On-Jump Option

2.06 A five-position DIP switch located at A7 and designated SW1 performs two functions:

(1) Positions 1 to 4 set the high order four-bit address when Power-On-Jump option is enabled. A15, A14, A13 and A12 correspond to 5 to 2 silkscreened next to the switch.

(2) Position 5 enables the Power-On-Jump feature. The switch is open in Dynabyte Disk Storage Systems.

3. FUNCTIONAL DESCRIPTION

3.01 The basic function of a Central Processing Unit (CPU) within a computer system is to accept data and instructions, perform the operations and deliver data back out.

3.02 Figure 3-1 illustrates CPU 803439 in block diagram and should be used in conjunction with the CPU logic diagram in Part 7 for the description which follows. Table 3-1 tabulates the S-100 Bus signals used by the CPU.

NOTE

*A * suffix to a signal name indicates a logical NOT and active low.*

Timing

3.03 CLOCK – An 8 MHz crystal-controlled oscillator establishes the timing reference for the CPU and the S-100 Bus.

(1) 1U is the timing reference for UART 1. The UART divides this signal down to a software-controlled data communication line rate of from 110 to 76,800 baud.

(2) 2U is the timing reference for UART 2. Its function is similar to (1) above.

(3) CLOCK is a 2 MHz 40% — 60% duty cycle clock supplied to the S-100 Bus.

(4) 4 MHZ PHASE 2 is the master timing signal supplied to the S-100 Bus.

(5) Φ is supplied to the microprocessor. Refer to Figure 3-2.

Microprocessor

3.04 The principle element of the CPU is the *Microprocessor (μP)*. It addresses other CPU elements over an internal 16-Bit Address Bus.

(1) *Address Buffers* – are tri-state devices which connect to the S-100 Address Bus, A0 — A15.

(2) *UART1, UART2 and Control* — for data communication port addressing.

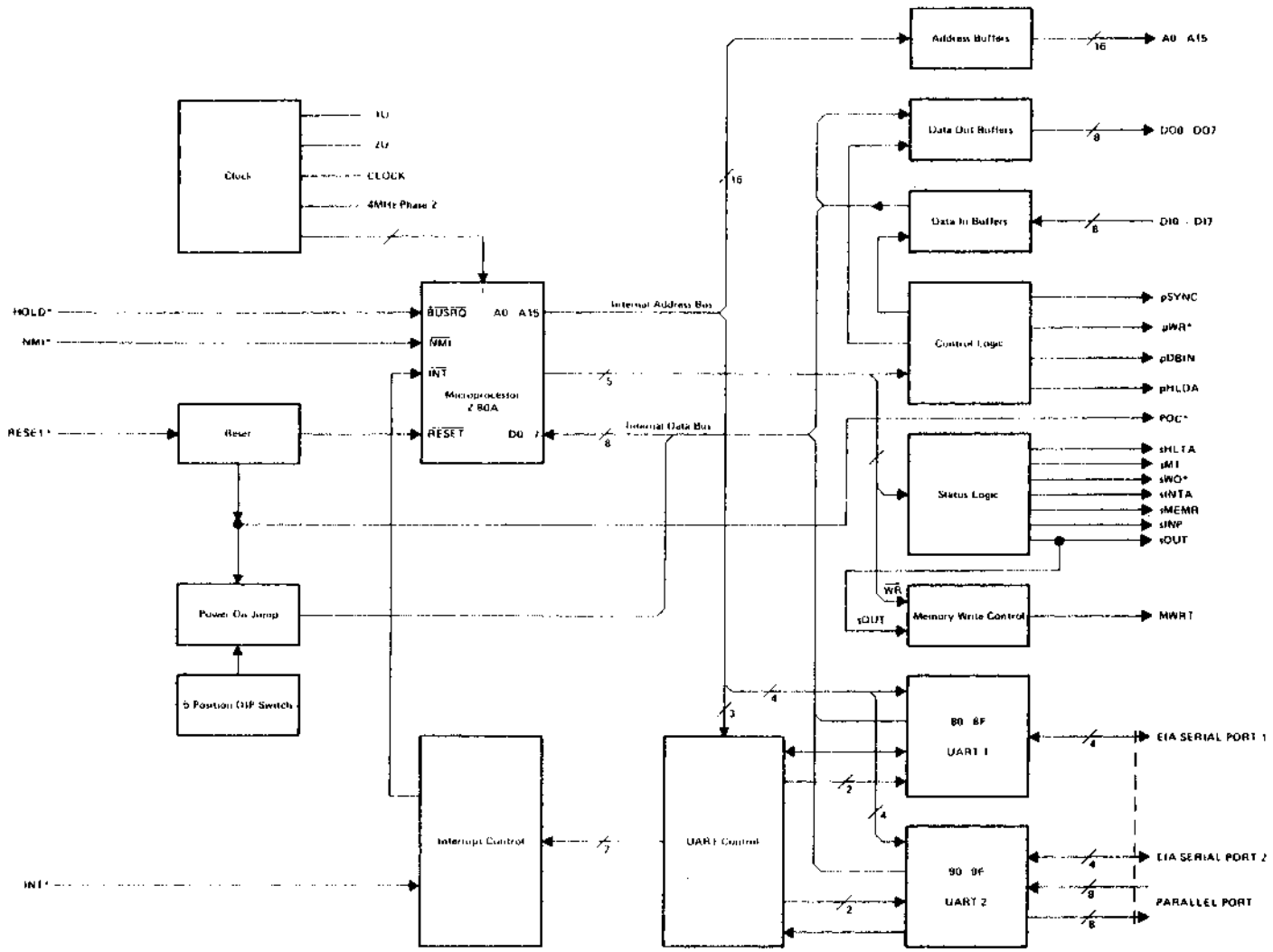

Figure 3-1 — Central Processing Unit Functional Block Diagram

Communications are handled by an 8-Bit bi-directional data bus. The internal data bus is tri-state.

(3) *Data In Buffers* — connect to S-100 Bus Data In Lines DI0 — DI7.

(4) *Data Out Buffers* — connect to S-100 Bus Data Out Lines DO0 — DO7.

(5) *UART 1, UART 2* — for data communications.

(6) *Power-On-Jump* — where it conveys the jump address when this feature is enabled. Refer to 3.07.

The μP initiates five control signals to the S-100 Bus from *Control Logic* during processing operations. The *Control Logic* consists of data latches.

(7) pSYNC identifies the beginning of a processing cycle. Refer to Figure 3-2.

(8) pWR* signifies the presence of valid data on the Data Out Bus, DO0 — DO7.

(9) pDBIN requests data from the Data In Bus, DI0 — DI7.

(10) pHLDA is used in conjunction with HOLD* to coordinate bus master transfer operations.

(11) MWRT is the write to memory.

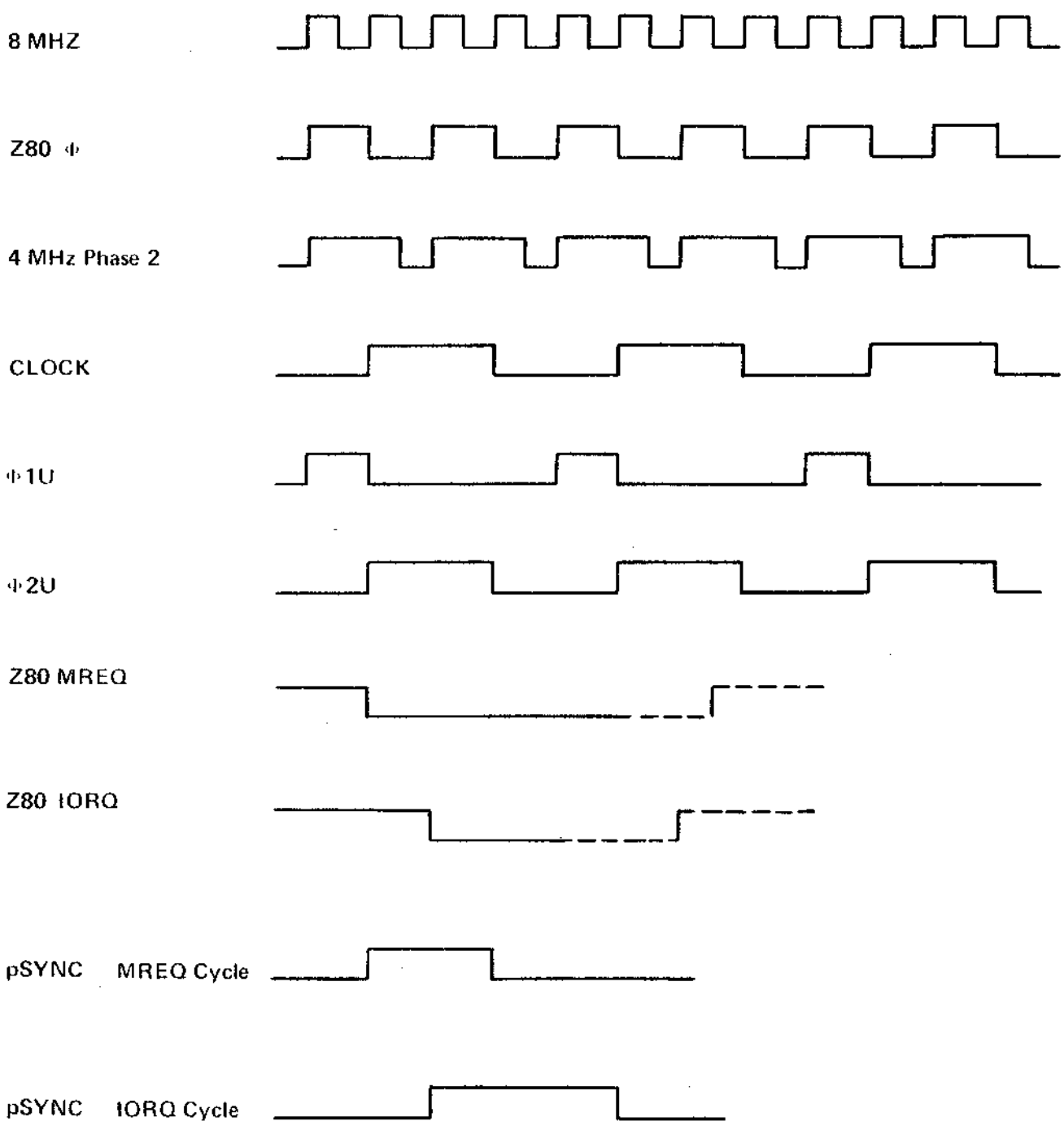

Figure 3-2 – Central Processing Unit Timing

In addition, the μP supplies seven status lines to the S-100 Bus from *Status Logic* during processing operations. The *Status Logic* consists of latches.

(12) sHLTA acknowledges a HLT instruction has been executed.

(13) sM1 indicates the current cycle is an op-code fetch.

(14) sWO* identifies a bus cycle which transfers data from the CPU to a device.

(15) sINTA identifies the bus input cycle(s) that may follow an accepted interrupt request presented on S-100 Bus INT* Line.

(16) sMEMR identifies the bus input cycle(s) which transfer data from memory to the CPU which are not interrupt acknowledge instruction fetch cycle(s).

(17) sINP indicates the data transfer bus cycle is from an input device.

(18) sOUT indicates the data transfer bus cycle to an output device.

3.05 Two S-100 Bus lines are input directly to the μP.

(1) HOLD* is the Hold Request line and is used by temporary bus masters to request control of the bus from the CPU. Refer to 3.04 (10) above.

(2) NMI* is the non-maskable interrupt. It has priority over the maskable interrupts. Refer to 3.14.

Reset

3.06 The *Reset* may be activated in either of two ways.

(1) An S-100 Bus request reset is received. The RESET line goes low, e.g., when the computer operator keys the Front Panel RESET.

(2) AC power is applied to the computer system.

A Power On Clear (POC) is issued from *Reset* to the S-100 Bus POC* line and the CPU *Power On Jump* circuit. POC* is the master reset line for the Dynabyte system.

Power-On-Jump

3.07 Option switches on the CPU provide a starting address for the CPU after a POC* is issued. The *Power On Jump* provides for the μP to jump to any high-order 4-Bit address enabled and set by the *5-position DIP Switch*. This starting address is output to the μP over the internal data bus.

Input Output Ports

3.08 *UART Control* monitors status and supplies controls to two input output (I/O) ports on the CPU.

(1) UART 1 -- address 80H to 8FH is a serial port.

(2) UART 2 -- address 90H to 9FH can be configured to be a serial port and a 8-Bit parallel port.

Both of these ports have their operating parameters, e.g., baud rate, parity check, serial or parallel operation through software. The Operating System initializes the I/O ports when the system is reset.

3.09 Two serial data communications configurations are supported by the UARTs.

(1) 20 mA current loop.

(2) EIA RS-232C Data In, Out and Signal Common. Terminal Ready is monitored at Pin 5 of the DB-25S connector. All these lines are at RS-232C voltage levels. Modem control and status lines are at TTL levels.

Table 7-3 tabulates the Rear Panel DB-25S receptacle pin assignments for these ports.

3.10 CPU strap options provide for setting four modem control lines to RS-232C high or low. These are labeled on Figure 7-1, CPU schematics, as:

(1) RTS1*

(2) DTR1*

Table 3-1 - S-100 Bus Signals Used By The CPU

Name	Pin	Function
4 MHZ PHASE 2	24	The master timing signal for the bus.
A1 — A15	Various	Address bits 0 through 15.
ADSB*	22	The control signal to disable the 16 address signals.
CLOCK	49	2 MHz (0.5%) 40% — 60% duty cycle. Not required to be synchronous with any other bus signal.
DI0 — DI7	Various	Data in bits 0 through 7.
DO0 - DO7	Various	Data out bits 0 through 7.
DODSB*	23	The control signal to disable the 16 address signals.
MWRT	68	A bus memory write signal. pWR•sOUT* (logic equation). This signal must follow pWR* by not more than 30 ns.
NMI*	12	Nonmaskable interrupt.
POC*	99	The Master Reset signal. The Power-On-Clear signal for all devices. When this signal goes low, it must stay low for at least 10 ms.
RESET*	75	Requests the reset of all bus master devices. Connects to the Front Panel Reset Switch and activates POC*.
VI2*	6	Vectored interrupt line 2.
pDBIN	78	The control signal that request data on the DI bus.
pHLDA	26	A control signal used in conjunction with HOLD* to coordinate bus master transfer operations.
HOLD*	74	The control signal used in conjunction with pHLDA to coordinate bus master transfer operations.
pINT*	73	The primary interrupt request line.
pSYNC	76	The control signal identifying the beginning of a processor cycle.
pWR*	77	The control signal signifying the presence of valid data on DO bus.
sHLTA	48	The status signal which acknowledges that a HLT instruction has been executed.
sINP	46	The status signal identifying the data transfer bus cycle from an input device.

Table 3-1 — S-100 Bus Signals Used By The CPU (Continued)

Name	Pin	Function
sINTA	96	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt requested present on INT*.
sM1	44	The status signal which indicates that the current cycle is an op-code fetch.
sMEMR	47	The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).
sMREQ*	65	The status signal identifying bus cycles which reference memory read, write or refresh.
sOUT	45	The status signal identifying the data transfer bus cycle to an output device.
sRFSH*	66	The status signal identifying the current address on A0 — A6 is a dynamic memory refresh address.
sWO*	97	The status signal identifying a bus cycle which transfers data from a bus master to a slave.

(3) RTS2*

(4) DTR2*

Part 5 explains the installation procedure.

3.11 An 8-Bit parallel I/O port is also supported by *UART 2*. The input lines are:

(1) IN0 — IN7, the Data In lines,

(2) READY*

(3) SENSE

(4) PORT*

(5) OUTBUSY*

The output lines are:

(6) OUT0 — OUT7, the Data Out lines,

(7) OUT STROBE

(8) FLAG1 OUT*

(9) FLAT2 OUT*

3.12 Ten interval timers are part of the two UARTs. Each timer may be counted down from a programmed count of 1 to 255. Each count is 64 μs, resulting in intervals of 64 μs to 16.32 ms. At zero an interrupt pending bit is set and under program control can generate an interrupt to the μP.

3.13 Pin 55, Real Time Clock, of the S-100 Bus is monitored. RTC is at the ac line frequency. It's sine wave undergoes wave shaping and is supplied to *UART 1* sense input. The sense input can be programmed to set a status bit or cause an interrupt in synchronism with the ac line frequency. The Operating System may use this for time-of-day applications.

Interrupts

3.14 In addition to INT*, the maskable interrupt, and NMI*, the non-maskable interrupt, supplied from the S-100 Bus, the UARTs provide the CPU with sixteen individually maskable interrupts. Group 1 includes:

(1) Timer 1

(2) Timer 2

(3) Real Time Clock

(4) Timer 3

(5) Serial 1 Receive Data Available

(6) Serial 1 Transmitt Buffer Empty

(7) Timer 4

(8) Timer 5 or CTS2* Line.

Group 2 includes:

(9) Timer 6

(10) Timer 7

(11) Parallel Port Int. or S-100 Bus VI2*

(12) Timer 8

(13) Serial 2 Receive Data available

(14) Serial 2 Transmit Buffer empty

(15) Timer 9

(16) Timer 10 or Parallel Port Input Bit 7

Timer 5 and Timer 10 interrupt are under program control and can be changed from the timer to the signal external to UART. The 16 interrupt conditions are listed in order of priority within their group. Group 2 has priority over Group 1 interrupts.

3.15 Table 3-2 lists the I/O ports by address and provides a brief description of the bit functions.

Table 3-2 – CPU I/O Port Address and Function

Port	Name	Bit	Function
80H	Input Serial 1 Receive Data	7-0	Contain the data byte received by Serial 1.
81H	Input Device Status		
	Terminal Ready	7	A high indicates an RS-232C high level at Pin 5 of DB-25S Serial 2. A low indicates an RS-232C low level.
		6	A high in Bit 6 indicates a TTL high level at Pin 6 of DB-25S connector Serial 2. A low indicates a TTL low level.
	Terminal Ready	5	Same as Bit 7 above except for Serial 1.
		4	Same as Bit 6 above except for Serial 1.
	Ready*	3	A high indicates that Pin 10 of DB-25S parallel I/O connector has been strobed high to low. Bit 2 of Port 87 resets IN-RDY and therefore must be a low before the strobe. A low indicates Ready* has been sent.
	Sense	2	A high indicates that Pin 11 of DB-25S connector parallel I/O is at a TTL high. A low indicates a TTL low.
	Out Busy*	1	A high indicates that Pin 23 of DB-25S connector parallel I/O is a TTL low. A low indicates a TTL high.
	Real Time Clock	0	Alternately high and low at the ac line frequency rate.
82H	Input Group 1 Interrupt Address	7-0	This port reads the highest priority Group 1 interrupt currently requesting CPU attention. This address is the restart instruction Op-Code that will be executed by the CPU when and if interrupts are enabled and interrupt acknowledge is returned by the CPU. The following table lists port contents in order of priority, highest first.

Data	Requestor	Restart
C7	Timer 1	RST 0
CF	Timer 2	RST 1
D7	Real Time Clock	RST 2
DF	Timer 3	RST 3
E7	Serial 1 Receive Data Available	RST 4
EF	Serial 1 Transmit Buffer Empty	RST 5
F7	Timer 4	RST 6
FF	Timer 5 or CTS 2	RST 7

Table 3-2 – CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
			This port can be used to service interrupts by polling. After reading, the highest priority interrupt is reset. If none are pending 0FFH will be read. When interrupts re-enabled and unmasked, the indicated restart instruction will be executed.
83H	Input Serial 1 Status		
	Start Bit Detect (SBD)	7	A high indicates that Serial 1 has received the start bit of an incoming character. This bit remains high until the entire character is received or until a reset command is issued. This bit is used for testing.
	Full Bit Detect (FBD)	6	This bit is identical to bit above except that it indicated the first data bit in an incoming character instead of the start bit.
	Interrupt Pending (IPB)	5	A high indicates that one or more Group 1 interrupts have been requested and are unmasked. This bit is high when a Group 1 hardware interrupt is requested of the CPU. This bit is used to service interrupts via polling.
	Transmit Buffer Empty (TBE)	4	A high indicates that Serial 1 Transmit Buffer is ready to accept a character. The Serial Transmitter is buffered and the user may load a new character even before the previous character is totally transmitted. TBE is set high by the reset command and can request a Group 1 interrupt.
	Received Data Available (RDA)	3	RDA is set high when the Serial 1 Receiver buffer is loaded with a new character and remains high until the buffer is read or a reset Serial 1 command is received. If the buffer is not read before the next character is received, the new character will overwrite the old and set the overrun error flag. RDA can request a Group 1 interrupt.
	Serial Received (SRB)	2	Monitors the Serial 1 Data Input Signal which provides break character detection. A high indicates a high at the Serial Data Input and a low indicates a low.
	Overrun Error (ORE)	1	A high indicates that a new character has been loaded into the Serial 1 receiver buffer before the old character was read. The old character is lost. ORE is cleared each time Port 83H is read or when a reset Serial 1 command is received.

Table 3-2 — CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
	Frame Error (FEB)	0	A high indicates that an incorrect number of stop bits have been received on Serial 1. FEB is cleared each time Port 83H is read or when a reset Serial 1 command is received.
84H	Output Signal Serial 1 Command		Bits 5 — 1 are latched.
		7	Unused.
		6	Unused.
	Test (TB5)	5	TB5 is a test bit that should be low at all times. TB5 is latched between outputs to Port 84H.
	High Baud (HBR)	4	A high multiplies the Serial 1 standard baud rate by 8 and divides the standard count rate by 8. A low sets the standard baud rate and count. HBR is latched between outputs to Port 84H.
	INTA Enable (INE)	3	A high will enable Group 1 unmasked interrupts to gate a restart instruction to the processor during interrupt acknowledge time. A low INE will cause no restart instruction to be gated even though an interrupt has been generated. An interrupt with no gated restart instruction will default to RST7. INE is latched between outputs to Port 84H.
	INT7 Select (INT7)	2	A high connects an Interrupt 7 (RST7) request to the low to high transition of RS-232C signal Serial 2 Terminal Ready. A low at IN7 connects Interrupt 7 to Timer 5 zero count. IN7 is latched between outputs to Port 84H.
	Break (BRK)	1	A high will cause Serial 1 Transmitter to send a Break character (continuous spacing). A low will set Serial 1 to normal operation. If RST and BRK are both high, RST will override (see below). BRK is latched between outputs to Port 84H.
	Reset (RST)	0	A high will: (1) Clear Serial 1 receive register and set low: SBD, FBD, RDA, ORE and FEB. Receive buffer will contain last received character. (2) Serial 1 transmitter data output is set high (marking) and TBE is set high.

Table 3-2 – CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
			(3) All Group 1 interrupts are cleared except TBE and Timers 1 through 5 are inhibited. (4) If BRK and RST are high together, RST will override. RST is not latched.
85H	Output Serial 1 Baud Rate		
	Stop Bits	7	A high selects one stop bit and a low selects two stop bits for Serial 1.
	Rate	6-0	A high in Bit 6 through Bit 0 selects the indicated Serial 1 baud rate as standard or high depending on HBR of Port 84H. If more than one bit is high, the highest rate will prevail.
		6	9,600 or 76,800 baud
		5	4,800 or 38,400 baud
		4	2,400 or 19,200 baud
		3	1,200 or 9,600 baud
		2	300 or 2,400 baud
		1	150 or 1,200 baud
		0	110 or 880 baud
86H	Output Serial 1 Transmit Data	7-0	Loaded with the data byte to be transmitted on Serial 1.
87H	Output Device Control Word		All bits are latched between Port 87H outputs.
		7	A high will output a TTL low at Pin 4 of DB-25S connector Serial 2. A low will output a high.
		6	A high will output a TTL low at Pin 20 of DB-25S connector Serial 2. A low will output a high.
		5	Same as Bit 7 above for Serial 1.
		4	Same as Bit 6 above for Serial 1.
	Reset In-Ready	3	A high will reset the parallel ready edge triggered latch. A low will allow ready to go high on the high-to-low transition of Pin 10 of DB-25S parallel I/O.
	Out Strobe	2	A high will output a TTL low at Pin 24 of DB-25S parallel I/O. A low will output a TTL high.

Table 3-2 – CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
	Flag 2 Out*	1	A high will output a TTL low at Pin 25 of DB-25S parallel I/O. A low will output a TTL high.
	Flag 1 Out*	0	A high will output a TTL low at Pin 12 of DB-25S parallel I/O. A low will output a TTL high.
88H	Output Group 1 Interrupt Mask		Each bit of the Group 1 interrupt mask corresponds to one of the eight Group 1 interrupts. A high will enable and a low will inhibit that interrupt. The interrupt request is latched independently of the mask and therefore will remain active if masked until a reset occurs or the mask is changed and the interrupt acknowledged.
	Timer 5 or Serial 2 Terminal Ready	7	
	Timer 4	6	
	TBE (Serial 1)	5	
	RDA (Serial 1)	4	
	Timer 3	3	
	Real Time Clock	2	
	Timer 2	1	
	Timer 1	0	
89H	Output Timer 1 Count	7-0	This port is loaded with the count to start Timer 1. The count is then decremented by one every 64 microseconds until zero. At zero an interrupt is requested at the priority level of the timer if it is unmasked. Maximum time interval is 255 x 64 μs = 16.32 ms. Loading a zero will cause an immediate interrupt request. A count may be changed any time. If the HBR bit of Port 84H is high, the count rate is 8 μs instead of 64 for Timers 1 through 5.
8AH	Output Timer 2 Count	7-0	Same as Port 89H for Timer 2.
8BH	Output Timer 3 Count	7-0	Same as Port 89H for Timer 3.

Table 3-2 – CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
8CH	Output Timer 4 Count	7-0	Same as Port 89H for Timer 4.
8DH	Output Timer 5 Count	7-0	Same as Port 89H for Timer 5.
8EH		7-0	Not used.
8FH		7-0	Not used.
90H	Input Serial 2 Receive Data	7-0	Contain the data byte received from Serial 2.
91H	Input Parallel Card Data	7-0	Contain the data byte received from the Parallel Input Port.
92H	Input Group 2 Interrupt Address	7-0	This address is the restart instructions op-code that will be executed by the CPU when and if interrupts are enabled and interrupt acknowledge is returned by the CPU. The following table lists port contents in order of priority, highest first: Data – Requestor – Restart C7 Timer 6 RST 0 CF Timer 7 RST 1 D7 Port Interrupt RST 2 DF Timer 8 RST 3 E7 Serial 2 Receive Data Available RST 4 EF Serial 2 Transmit Buffer Empty RST 5 F7 Timer 9 RST 6 FF Timer 10 or parallel input Bit 7 RST 7 This port can be used to service interrupts by polling. After reading the highest priority interrupt is reset. If none are pending 0FFH will be read. When interrupts are enabled and unmasked, the indicated restart instruction will be executed.
93H	Input Serial 2 Status		
	Start Bit Detect (SBD)	7	A high indicates that Serial 2 has received the start bit of an incoming character. This bit remains high until

Table 3-2 -- CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
			the entire character is received or until a reset command is issued. This bit is used for testing.
	Interrupt Pending (IPB)	5	A high indicates that one or more Group 2 interrupts have been requested and are unmasked. This bit is high when a Group 2 hardware interrupt is requested of the CPU. This bit is used to service interrupts via polling.
	Transmit Buffer Empty (TBE)	4	A high indicates that Serial 2 Transmit Buffer is ready to accept a character. The Serial Transmitter is buffered and the user may load a new character even before the previous character is totally transmitted. TBE is set high by the reset command and can request a Group 2 interrupt.
	Received Data (RDA)	3	RDA is set high when the Serial 2 receiver buffer is loaded with a new character and remains high until the buffer is read or reset Serial 2 command is received. If the buffer is not read before the next character is received, the new character will overwrite the old and the overrun error flag. RDA can request a Group 1 interrupt.
	Serial Received (SRB)	2	Monitors the Serial 2 data input signal which provides break character detection. A high indicates a high (marking) at the serial data input and a low (spacing) indicates a low.
	Overrun Error (ORE)	1	A high indicates that a new character has been loaded into the Serial 2 receiver buffer before the old character is lost. ORE is cleared each time Port 93H is read or when a reset Serial 2 command is received.
	Frame Error (FEB)	0	A high indicates that an incorrect number of stop bits have been received on Serial 2. FEB is cleared each time Port 39H is read or when a reset Serial 2 command is received.
94H	Output Serial 2 Command		
		7	Not used.
		6	Not used.
	Test (TB5)	5	TB5 is a test bit that should be low at all times. TB5 is latched between outputs to Port 94H.

Table 3-2 – CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
	High Baud (HBR)	4	A high multiplies the Serial 2 standard baud rate by 8 and divides the standard count rate by 8. A low sets the standard baud rate and count. HBR is latched between outputs to Port 94H.
	Inta Enable (INE)	3	A high will enable Group 2 unmasked interrupts to gate a restart instruction to the processor during interrupt acknowledge time. A low in INE will cause no restart instruction to be gated even though an interrupt has been generated. An interrupt with no gated restart instruction will default to RST7. NE is latched between outputs to Port 94H.
	Int7 Select (IN7)	2	A high connects an interrupt 7 (RST7) request to the low to high transition of parallel port bit 7. A low of IN7 connects interrupt 7 to timer 10 zero count. IN7 is latched between outputs to Port 94H.
	BREAK (BRK)	1	A high will cause Serial 2 transmitter to send a break character (continuous spacing). A low will set Serial 2 to normal operation. If RST and BRK are both high, RST will override (see below). BRK is latched between outputs to Port 94H.
	RESET (RST)	0	A high will: (1) Clear Serial 2 receive register and set low: SBD, FBD, RDA, ORE and BEF. Receiver buffer will contain last received character 2. (2) Serial 2 transmitter data output is set high (marking) and TBE is set high. (3) All Group 2 interrupts are cleared except TBE and Timers 6 through 10 are inhibited. (4) If BRK and RST are high together, RST will override. RST is not latched.
95H	Output Serial 2 Baud Rate		
	Stop Bits	7	A high selects one stop bit and a low selects two stop bits for Serial 2.
	Rate	6-0	A high in bit 6 through bit 0 selects the indicated Serial 2 baud rate as standard/high depending on the HBR of Port 94H. If more than one bit is high, the highest rate will prevail.

Table 3-2 – CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
		6 5 4 3 2 1 0	9,600 or 76,800 baud 4,800 or 38,400 baud 2,400 or 19,200 baud 1,200 or 9,600 baud 300 or 2,400 baud 150 or 1,200 baud 110 or 880 baud
96H	Output Serial Transmit Data	7-0	Loaded with the data byte to be transmitted on Serial 2.
97H	Output Parallel Port Data	7-0	Data output on this port will appear latched at TTL levels at the parallel port DB-25S connector.
98H	Output Group 2 Interrupt Mask		Each bit of the Group 2 interrupt mask corresponds to one of the eight Group 2 interrupts. A high will enable and a low will inhibit that interrupt. The interrupt request is latched independently of the mask and, therefore, will remain active if masked until a reset occurs or the mask is changed and the interrupt acknowledged or polled.
	Timer 10 or Parallel Bit 7	7	
	Timer 9	6	
	TBE (Serial 1)	5	
	RDA (Serial 1)	4	
	Timer 8	3	
	Port Interrupt or V12	2	
	Timer 7	1	
	Timer 6	0	
99H	Output Timer 6	7-0	This port is loaded with the count to start Timer 6. The count is then decremented by one every 64 μs until zero. At zero an interrupt is requested at the priority level of the timer if it is unmasked. Maximum time interval is:

Table 3-2 — CPU I/O Port Address and Function (Continued)

Port	Name	Bit	Function
			255 x 64 μs = 16.32 ms Loading a zero will cause an immediate interrupt request. A count may be changed any time. If the HBR bit of Port 94H is high, the count rate is 8 μs instead of 64 for Timers 6 through 10.
9AH	Output Timer 7 Count	7-0	Same as Port 99H for Timer 7.
9BH	Output Timer 8 Count	7-0	Same as Port 99H for Timer 8.
9CH	Output Timer 9 Count	7-0	Same as Port 99H for Timer 9.
9DH	Output Timer 10 Count	7-0	Same as Port 99H for Timer 10.
9EH		7-0	Not used.
9FH		7-0	Not used.

4. SPECIFICATIONS

4.01 Table 4-1 summarizes the CPU, 803439, functional and physical performance specifications. Minor deviations from these specifications which do not affect the computer system operation are excluded from the Dynabyte, Inc. warranty.

Table 4-1 – Central Processing Unit 803439 Specifications

PARAMETER	CHARACTERISTICS
Processor Section	
Microprocessor	Z-80A
Clock Rate	4 MHz
Instruction Set	158
Interval Timer	
Number	10
Time Unit	64 μs per count 8 μs per count under program control
Range	1 to 255 units (8 μs – 16.32 ms)
Interrupt	Interrupts on count 0 under program control.
Real Time Clock	
Frequency	Ac line synchronous
Indication	Sets status bit or causes interrupt
Interrupts	
Number	16
Priority, highest	Timer 6 Timer 7 Port interrupt Timer 8 Serial 2 Receive Data available Serial 2 Transmit Data available Timer 9 Timer 10 or Parallel Port Input Bit 7 Timer 1 Timer 2 Real Time Clock Timer 3 Serial 1 Receive Data available Serial 1 Transmit Buffer empty Timer 4
Priority, lowest	Timer 5
Levels of Interrupt Masking	
Level 1	Masks all interrupts
Level 2	Individual masking or interrupts
Off-Card Interrupts	One maskable One unmaskable

Table 4-1 – Central Processing Unit 803439 Specifications (Continued)

PARAMETER	CHARACTERISTICS
Input/Output Section	
Serial Ports	2
Rates	110, 150, 300, 800, 1200, 2400, 4800, 9600, 19,200, 38,400, 76,800 baud
Rate Selection	Software programmable
Connector	DB-25S, refer to Table 7-2 for pin assignments
Data In	RS-232C
Data Out	RS-232C
Signal Common	RS-232C
Data In	20 mA current loop
Data Out	20 mA current loop
Parallel Port	1
Input	8 bits
Ready flag	Edge triggered
Sense	1 bit
Output	8 bits
Strobe	1 bit
Flags	2
Connector	DB-25S, refer to Table 7-2 for pin assignments
Power Requirements	
+16 Volt Bus	Regulated to +12 Vdc
+ 8 Volt Bus	Regulated to + 5 Vdc
–16 Volt Bus	Regulated to –12 Vdc
Operating Temperature	10° to 32°C (50° to 95°F)
Relative Humidity	20% to 80%
Dimension, width	25.4 cm (10.0 in.)
, depth	1.5 cm (0.6 in.)
, height	12.7 cm (5.0 in.)
, Weight	328.9 g (11.6 oz.)

5. INSTALLATION

5.01 Refer to the 5100/5200 Computer Unit Technical Manual for unpacking, inspection and return of material procedures.

NOTE

Always check the PCA options agree with the individual system equipment configuration before turning on the Dynabyte computer system.

Options

5.02 Power-On-Jump is enabled by SW1 on the CPU. This feature should not be optioned in Dynabyte Disk Operating Systems. In these applications the switches should be set as shown in Figure 2-1. The switch functions by position are silkscreened on the pc board to the right of the switch. Closing switch position:

(1) Sets high order Address Bit 12.

(2) Sets high order Address Bit 13.

(3) Sets high order Address Bit 14.

(4) Sets high order Address Bit 15.

(5) Enables the Power-On-Jump to the address set in positions 1 to 4.

5.03 RS-232C Levels — CPU modem control lines labled:

(1) RTS1*

(2) DTR1*

(3) RTS2*

(4) DTR*

on CPU schematic, Figure 7-1, can be strapped high (+5 Vdc) or low (–5 Vdc) to meet individual installation requirements. Refer to Figure 2-1 for the procedure which follows.

STEP	PROCEDURE
1	Using a sharp blade, cut one or more Traces at the silkscreened "X" on the pc board. The silkscreened numbers correspond to the control lines listed above. This opens the line(s) between the lines driver(s) and the output line(s).
2	Install an insulated #22 strap between the hole marked (+) or (–) to the hole next to the cut trace. This pulls the control line high or low.
3	Repeat Step 2 to the next cut line.

5.04 The CPU can be installed in any of the 12 card cage positions. As a matter of cabling convenience, it should be installed as shown in Figure 2-3 of the 5100/5200 Computer Unit Technical Manual.

STEP	PROCEDURE
1	Install the CPU Port I/O Cable 800285 to the Rear Panel of the 5100/5200 Computer Unit. The Connector PC Assembly is secured to the rear panel by the six 4-40 DB-25S connector nuts.
2	Install the CPU into the card cage. **NOTE** *The 50-conductor I/O cables are polarized with a stripe on conductor 1.*
3	Connect the Port I/O Cable to the CPU. Be sure the cable connector Pin 1 mates with P1 silkscreened onto the CPU pc board.

6. MAINTENANCE

6.01 The CPU 803439 is a result of several years of design, development and modern electronic manufacturing. The pc assembly is designed around the latest semiconductors and integrated circuits. All components operate at relatively low power and components dissipating power are heat sinked. Each CPU is burned in at the Dynabyte factory for 72 hours before shipment.

6.02 No routine maintenance should be performed to the CPU.

Customer Support Service

6.03 Maintenance and procedures described in this manual should be performed in accordance with local instructions and the individual user's maintenance plan. Maintenance and repair of the CPU during the warranty period should be limited to returning the pc assembly to Dynabyte, Inc. The Dynabyte Customer Support staff is available by telephone for assistance in troubleshooting and recommendations for repairs. All communications and material should be directed to:

DYNABYTE, INC.
Customer Support
521 Cottonwood Drive
Milpitas, CA. 95035
(408) 263-1221
Telex 346-359

The 5100/5200 Technical Manual, Part 6, outlines the procedure for returning material.

NOTE

Dynabyte Authorized Service Centers (ASC) are staffed with factory-trained technicians that are supplied with technical manuals and routinely receive service bulletins and design change information on Dynabyte equipment.

7. REFERENCE

S-100 Bus

7.01 Table 7-1 tabulates the Dynabyte S-100 Bus pins by assignment and function.

Schematics and Replaceable Parts Lists

7.02 Figure 7-1 will furnish the user with the schematic diagram for the CPU 803439. Table 7-2 is the replaceable parts list for the CPU indexed by reference designator appearing on the schematic. Enough information is furnished so the maintenance technician should be able to purchase replaceable parts from a local supplier or make a substitution if necessary. CPUs as completed assemblies, ROMs and other special parts should be ordered directly from Dynabyte Customer Support Service.

Engineering Change Notices

7.03 Dynabyte makes changes to drawings and products through engineering change notices (ECN)s. Before a change to a product is approved or made:

(1) The implications to systems in the field are determined,

(2) Rework instructions are included for the equipment in the field when appropriate.

Dynabyte Customer Support Services receives copies of all ECNs and advised Dynabyte Authorized Service Centers through seminars and periodic bulletins.

7.04 There are no pertinent ECNs effecting the CPU at the publication date.

Table 7-1 – Dynabyte S-100 Bus Pin Assignments

Pin No.	Signal – Type	Active Level	Description
1	+8 Volts (B)		Instantaneous minimum greater than 7 Volts, instantaneous maximum less than 25 Volts, average maximum less than 11 Volts.
2	+16 Volts (B)		Instantaneous minimum greater than 14.5 Volts, instantaneous maximum less than 35 Volts, average maximum less than 21.5 Volts.
3	XRDY (S)	H	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. See pin 72.
4	VI0* (S)	L OC	Vectored interrupt line 0.
5	VI1* (S)	L OC	Vectored interrupt line 1.
6	VI2* (S)	L OC	Vectored interrupt line 2.
7	VI3* (S)	L OC	Vectored interrupt line 3.
8	VI4* (S)	L OC	Vectored interrupt line 4.
9	VI5* (S)	L OC	Vectored interrupt line 5.
10	VI6* (S)	L OC	Vectored interrupt line 6.
11	VI7* (S)	L OC	Vectored interrupt line 7.
12	NMI* (S)	L OC	Nonmaskable interrupt.
13	Dynabyte Reserved		
14	Dynabyte Reserved		
15	Dynabyte Reserved		
16	Dynabyte Reserved		
17	Dynabyte Reserved		
18	SDSB* (M)	L OC	The control signal to disable the 8 status signals.
19	CDSB* (M)	L OC	The control signal to disable the 5 control output signals.
20	Dynabyte Reserved		
21	Dynabyte Reserved		

Table 7-1 -- Dynabyte S-100 Bus Pin Assignments (Continued)

Pin No.	Signal – Type	Active Level	Description
22	ADSB* (M)	L OC	The control signal to disable the 16 address signals.
23	DODSB* (M)	L OC	The control signal to disable the 16 address signals.
24	4 MHz Phase 2 (B)		The master timing signal for the bus.
25	Dynabyte Reserved		
26	pHLDA (M)	H	A control signal used in conjunction with HOLD* to coordinate bus master transfer operations.
27	Dynabyte Reserved		
28	Dynabyte Reserved		
29	A5 (M)	H	Address bit 5.
30	A4 (M)	H	Address bit 4.
31	A3 (M)	H	Address bit 3.
32	A15 (M)	H	Address bit 15 (most significant).
33	A12 (M)	H	Address bit 12.
34	A9 (M)	H	Address bit 9.
35	DO1 (M)	H	Data out bit 1.
36	DO0 (M)	H	Data out bit 0.
37	A10 (M)	H	Address bit 10.
38	DO4 (M)	H	Data out bit 4.
39	DO5 (M)	H	Data out bit 5.
40	DO6 (M)	H	Data out bit 6.
41	DI2 (S)	H	Data in bit 2.
42	DI3 (S)	H	Data in bit 3.
43	DI7 (S)	H	Data in bit 7.
44	sM1 (M)	H	The status signal which indicates that the current cycle is an op-code fetch.

Table 7-1 – Dynabyte S-100 Pin Assignments (Continued)

Pin No.	Signal – Type	Active Level	Description
45	sOUT (M)	H	The status signal identifying the data transfer bus cycle to an output device.
46	sINP (M)	H	The status signal identifying the data transfer bus cycle from an input device.
47	sMEMR (M)	H	The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).
48	sHLTA (M)	H	The status signal which acknowledges that a HLT instruction has been executed.
49	CLOCK (B)		2 MHz (0.5%) 40 - 60% duty cycle. Not required to be synchronous with any other bus signal.
50	GND (B)		Common with pin 100.
51	+8 Volts (B)		Common with pin 1.
52	–16 Volts (B)		Instantaneous maximum less than –14.5 Volts, instantaneous minimum greater than –35 Volts, average minimum greater than –21.5 Volts.
53	Dynabyte Reserved		
54	Dynabyte Reserved		
55	Dynabyte Reserved		
56	Dynabyte Reserved		
57	Dynabyte Reserved		
58	Dynabyte Reserved		
59	Dynabyte Reserved		
60	Dynabyte Reserved		
61	Dynabyte Reserved		
62	Dynabyte Reserved		
63	Dynabyte Reserved		
64	Dynabyte Reserved		

Table 7-1 – Dynabyte S-100 Pin Assignments (Continued)

Pin No.	Signal – Type	Active Level	Description
65	sMREQ* (M)	L	The status signal identifying bus cycles which reference memory read, write or refresh.
66	sRFSH* (M)	L	The status signal identifying the current address on A0 - A6 is a dynamic memory refresh address.
67	PHANTOM*	L OC	A bus signal which disables memory during disk controller ROM access.
68	MWRT (B)	H	A bus memory write signal. pWR•sOUT* (logic equation). This signal must follow pWR* by not more than 30 ns.
69	Dynabyte Reserved		
70	Dynabyte Reserved		
71	Dynabyte Reserved		
72	RDY (S)	H OC	See comments for pin 3.
73	INT* (S)	L OC	The primary interrupt request bus signal.
74	HOLD* (M)	L OC	The control signal used in conjunction with pHLDA to coordinate bus master transfer operations.
75	RESET* (B)	L OC	Requests the reset of all bus master devices. Connects to the Front Panel Reset Switch and activates POC*.
76	pSYNC (M)	H	The control signal identifying the beginning of a processor cycle.
77	pWR* (M)	L	The control signal signifying the presence of valid data on DO bus.
78	pDBIN (M)	H	The control signal that requests data on the DI bus.
79	A0 (M)	H	Address bit 0 (least significant).
80	A1 (M)	H	Address bit 1.
81	A2 (M)	H	Address bit 2.
82	A6 (M)	H	Address bit 6.
83	A7 (M)	H	Address bit 7.
84	A8 (M)	H	Address bit 8.

Table 7-1 – Dynabyte S-100 Pin Assignments (Continued)

Pin No.	Signal – Type	Active Level	Description
85	A13 (M)	H	Address bit 13.
86	A14 (M)	H	Address bit 14.
87	A11 (M)	H	Address bit 11.
88	DO2 (M)	H	Data out bit 2.
89	DO3 (M)	H	Data out bit 3.
90	DO7 (M)	H	Data out bit 7.
91	DI4 (S)	H	Data in bit 4.
92	DI5 (S)	H	Data in bit 5.
93	DI6 (S)	H	Data in bit 6.
94	DI1 (S)	H	Data in bit 1.
95	DI0 (S)	H	Data in bit 0 (least significant for 8-bit data).
96	sINTA (M)	H	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on INT*.
97	sWO* (M)	L	The status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	Dynabyte Reserved		
99	POC* (B)	L	The Master Reset signal. The Power-On-Clear signal for all devices. When this signal goes low, it must stay low for at least 10 ms.
100	GND (B)		System ground and common to Pin 50.

NOTES:

(1.) Signal Type
- (B) Bus
- (M) Bus Master
- (S) Bus Slave
- * Logical NOT

(2.) Active Level
- H High
- L Low
- OC Open Collector

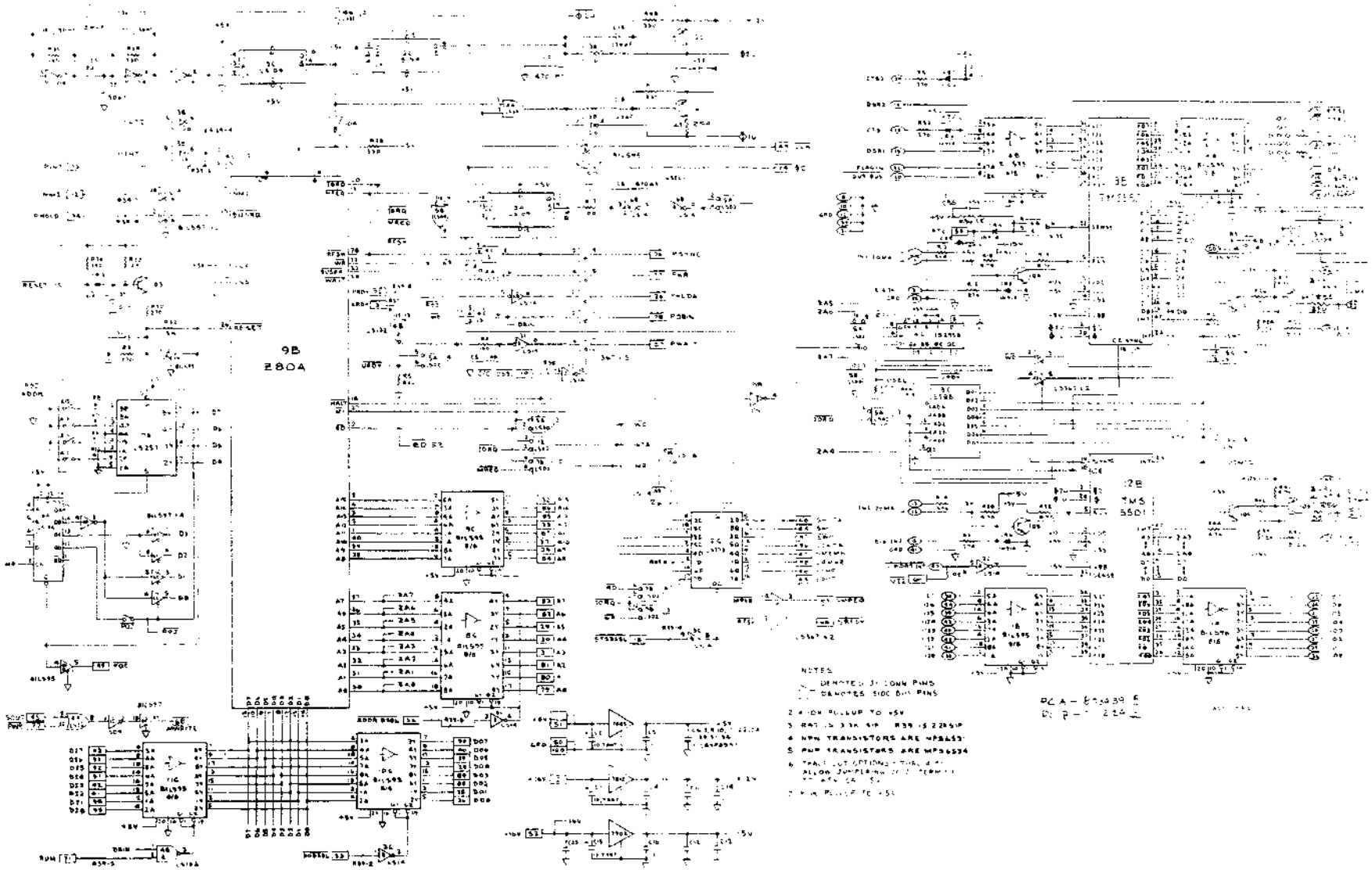

Figure 7-1 -- Central Processing Unit Logic Diagram

Table 7-2 – Central Processing Unit Replaceable Parts List

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
	PCA: CPU	DYNABYTE	803439	803439
	CABLE: CPU I/O	DYNABYTE	800285	800285
	PCA: INTERCONNECT	DYNABYTE	803420	803420
C 01	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 02	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 03	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 04	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 05	C: FXD CER 10% 1KV .001UF	CENTRALAB	DD102	703312
C 06	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 07	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 08	C: FXD CER 10% 1KV 470PF	CENTRALAB	DD471	703348
C 09	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 10	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 11	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 12	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 13	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 14	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 15	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 16	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 17	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 18	C: FXD CER 10% 1KV 120PF	CENTRALAB	DD121	703330
C 19	C: FXD CER 10% 1KV 120PF	CENTRALAB	DD121	703330
C 20	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 21	C: FXD CER 10% 1KV 470PF	CENTRALAB	DD471	703348
C 22	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 23	C: FXD CER 10% 1KV .001UF	CENTRALAB	DD102	703312
C 24	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 26	C: FXD CER 10% 1KV .001UF	CENTRALAB	DD102	703312
C 27	C: FXD CER 10% 1KV 120PF	CENTRALAB	DD121	703330
C 29	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 31	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 32	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 33	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 34	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 35	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 36	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294

Table 7-2 — Central Processing [illegible] Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
C 37	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
CR 01	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 02	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 03	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 04	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 05	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 06	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 07	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 08	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
J 01	CONNECTOR: 50-CONDUCTOR	AP PRODUCT	929838-01-25	703204
Q 01	TSTR: PNP SWITCH	NATIONAL	MPS6534	702934
Q 02	TSTR: PNP SWITCH	NATIONAL	MPS6534	702934
Q 03	TSTR: NPN SWITCH	NATIONAL	MPS6531	702916
Q 04	TSTR: NPN SWITCH	NATIONAL	MPS6531	702916
Q 05	TSTR: NPN SWITCH	NATIONAL	MPS6531	702916
Q 06	TSTR: PNP SWITCH	NATIONAL	MPS6534	702934
Q 07	TSTR: NPN SWITCH	NATIONAL	MPS6531	702916
Q 08	TSTR: PNP SWITCH	NATIONAL	MPS6534	702934
Q 09	TSTR: NPN SWITCH	NATIONAL	MPS6531	702916
R 01	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 02	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 03	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 04	R: FXD CF 5% 0.25W 100 OHM	ROHM	R25J101	703024
R 05	R: FXD CF 5% 0.25W 820 OHM	ROHM	R25J821	703060
R 06	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 07	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 08	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 09	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 10	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 11	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 12	R: FXD CF 5% 0.25W 100 OHM	ROHM	R25J101	703024
R 13	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 14	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620

Table 7-2 — Central Processing Unit Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
R 15	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 16	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 17	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 18	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 19	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 20	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 21	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 22	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 23	R: FXD CF 5% 0.25W 3.3K OHM	ROHM	R25J332	701566
R 24	R: FXD CF 5% 0.25W 1.5K OHM	ROHM	R25J152	701674
R 25	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 26	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 27	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 28	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 29	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 30	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 31	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 32	R: FXD CF 5% 0.25W 1.5K OHM	ROHM	R25J152	701674
R 33	R: FXD CF 5% 0.25W 12K OHM	ROHM	R25J123	703096
R 34	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 35	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 36	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 37	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 38	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 39	R: FXD SIP 7 X 2K OHM	BECKMAN	785-1-R2K	703114
R 40	R: FXD CF 5% 0.25W 3.3K OHM	ROHM	R25J332	701566
R 41	R: FXD CF 5% 0.25W 1.5K OHM	ROHM	R25J152	701674
R 42	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 43	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 44	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 45	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 46	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 48	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 49	R: FXD CF 5% 0.25W 820 OHM	ROHM	R25J821	703060
R 50	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 51	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 52	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078

Table 7-2 — Central Processing Unit Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
R 53	R: FXD CF 5% 0.25W 270 OHM	ROHM	R25J271	716620
R 54	R: FXD CF 5% 0.25W 47 OHM	ROHM	R25J470	703132
R 55	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
R 56	R: FXD CF 5% 0.25W 330 OHM	ROHM	R25J331	703042
SW 01	SWITCH: 5-POSITION SPST DIP	GRAYHILL	76SB05	703258
U A03	IC: DUAL J-K FLIP FLOP	TI	SN74LS109N	703564
U A04	IC: QUAD 2-IN OR	TI	SN7432N	703546
U A05	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U A06	IC: 4-BIT SHIFT REGISTER	TI	SN74LS195N	703600
U A07	IC: QUAD 2-IN MUX NON-INV	TI	SN74LS257N	703618
U A08	IC: 8-BIT MICROPROCESSOR	ZILOG	Z-80A	703762
U A10	IC: 5-BIT SHIFT REGISTER	TI	SN74LS96N	703726
U A12	IC: UART	TI	TMS5501NL	703780
U A13	IC: UART	TI	TMS5501NL	703780
U A14	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U B03	IC: HEX INVERTER BUFFER OC	TI	SN7406N	703492
U B04	IC: QUAD 2-IN NAND SCHMIDTT	TI	SN74LS132N	703582
U B05	IC: QUAD 2-IN NAND	TI	SN74LS00N	703438
U B06	IC: HEX INVERTER	TI	SN47LS04N	704014
U B07	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U B10	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U B14	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U C01	IC: HEX INVERTER	TI	SN74S04N	703474
U C02	IC: DUAL J-K FLIP FLOP	TI	SN74LS109N	703564
U C03	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U C04	IC: TRIPLE 3-IN AND	TI	SN74LS11N	703510
U C05	IC: HEX BUS DRIVER	TI	SN74LS367N	703672
U C06	IC: SYNCH 6-BIT BINARY MULT	TI	SNLS97N	703744
U C07	IC: HEX BUS DRIVER	TI	SN74LS367N	703672
U C08	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U C09	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U C10	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U C11	IC: 4-BIT SHIFT REGISTER	TI	SN74LS95N	703708
U C12	IC: OCTAL D LATCH	TI	SN74LS373N	703690
U C13	IC: READ ONLY MEMORY	DYNABYTE	803781	803781

Table 7-2 — Central Processing Unit Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
U C14	IC: 4-BIT SHIFT REGISTER	TI	SN74LS295N	703654
U C15	IC: TRIPLE 3-IN AND	TI	SN74LS11N	703510
VR 01	IC: REGULATOR +5V	TI	7805C	703168
VR 02	IC: REGULATOR +12V	TI	7812C	701998
VR 03	IC: REGULATOR -5V	TI	7905C	703186
Y 01	XTAL: 8-MHZ 10 PPM	NDK	HC 18U	703222

Table 7-3 – CPU Serial and Parallel I/O Port Pin Assignments

Pin	Definitions		
	Serial 1	Serial 2	Parallel I/O
1	Vacant	Vacant	IN 0
2	Data In (EIA)	Data In (EIA)	IN 1
3	Data Out (EIA)	Data Out (EIA)	IN 2
4	Out Port 87 Bit 5	Out Port 87 Bit 7	IN 3
5	Terminal Ready (EIA)	Terminal Ready (EIA)	IN 4
6	In Port 81 Bit 4	In Port 81 Bit 6	IN 5
7	Signal Common	Signal Common	IN 6
8	Vacant	Vacant	IN 7
9	Vacant	Vacant	Signal Common
10	Vacant	Vacant	Ready*
11	Data Out (+20 ma)	Data Out (+20 ma)	Sense
12	Vacant	Vacant	Flag 1 Out*
13	Vacant	Vacant	Port Int*
14	Vacant	Vacant	Out 0
15	Vacant	Vacant	Out 1
16	Vacant	Vacant	Out 2
17	Vacant	Vacant	Out 3
18	Data Out (–20 ma)	Data Out (–20 ma)	Out 4
19	Vacant	Vacant	Out 5
20	Out Port 87 Bit 4	Out Port 87 Bit 6	Out 6
21	Data In (+20 ma)	Data In (+20 ma)	Out 7
22	Vacant	Vacant	Signal Common
23	Vacant	Vacant	Out Busy*
24	Vacant	Vacant	Out Strobe
25	Data In (–20 ma)	Data In (–20 ma)	Flag 2 Out*

NOTES:

(1.) * Logical NOT.