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XXU

Reference Manual

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XXU

Reference Manual

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Rev. A

This manual was produced using a Cromemco System One computer running under the Cromemco Cromix-Plus Operating System. The text was edited with the Cromemco Cromix-Plus Screen Editor. The edited text was proofread by the Cromemco SpellMaster Program and formatted by the Cromemco Word Processing System Formatter II. Camera-ready copy was printed on a Cromemco 3355B printer.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

LIST OF APPENDICES

INTRODUCTION

Cromemco's XXU processor board provides a bold leap in microcomputer processing power, exceeding previously offered microcomputer speed by a factor of three or more. By integrating a 16.7 MHz MC68020 microprocessor, a 16.7 MHz MC68881 floating-point coprocessor and a 16 KByte two-set associative data and instruction cache onto one S-100/IEEE-696 card, the XXU offers performance heretofore unavailable in a general purpose microcomputer. Using Cromemco's 2048KZ memory boards, which feature Cromemco's exclusive double-word transfer extension to the S-100/IEEE-696 bus, data can be moved on the bus at rates as great as 8.33 megabytes per second. This is more than double the transfer rate of previous Cromemco products.

The XXU also provides a real-time clock/calendar with battery backup and a diagnostic/boot ROM. The clock has an accuracy adjustable to within seconds per month. The combination of battery backup and high degree of accuracy eliminates the tedium of entering time and date every time the system is booted. The diagnostic/boot ROM makes it possible to test the basic system hardware prior to booting. This enables configuration or hardware problems to be detected and signaled to the user.

Table 1-1: XXU SPECIFICATIONS

Processor: Coprocessor:	MC68020 - 16.7 MHz MC68881 - 16.7 MHz (jumper option present to utilize faster coprocessors when available)
Cache Configurations:	256 byte internal instruction cache (on-chip) 16 Kbyte 2-set associative instruction/data cache (on-board)
Cache Operating Mode:	Zero wait state read Two wait state write-through ("quick write")
Memory Address Span:	16 Megabytes
I/O Address Span:	16 Megabytes
Memory and I/O Access:	Dynamic bus sizing permits access to slave device of any width
Power-on or Reset:	Diagnostic/bootstrap ROM permits direct boot to many devices
LED Fault Indicator:	Encodes catastrophic hardware problems (See 68020 Cromix-Plus Manual, 68020 UNIX Manual or System 400/20 Manual)
Time-of-Day Clock:	Accurate to seconds per month. Backup battery life approximately 5 years (with power off)
Power Requirements:	+16 Volts at 1.8 Amps
Operating Environment:	0 to 55 Degrees C

SETUP AND INSTALLATION

Switch Settings

There are no switches on the XXU.

Jumper Selectable Options

The XXU board has three jumper locations as shown in Figure 1-1. Jumper JP1 selects the clock source for the MC68881 coprocessor. As shipped, the MC68881 clock input is the same 16.7 MHz signal used by the MC68020. When available, a higher speed coprocessor can be used by cutting the trace between pads 2 and 3 of JP1 and installing a jumper between pads 1 and 2. Then install the auxiliary oscillator at location IC23 and replace the 16.7 MHz MC68881 with the higher speed version.

Jumpers JP2 and JP3 are for test purposes only and should be left open.

Variable Capacitor Adjustment

C2 is a variable capacitor for adjusting the accuracy of the real-time clock. If an adjustment is necessary, locate the arrow on the adjusting screw of C2. To slow down the clock, turn the screw so that the arrow is moved closer to the maximum capacitance position (arrow pointing toward the battery). To speed up the clock, turn the arrow away from the battery. Move the screw only a small amount, approximately a tenth of a turn at a time. Wait at least several hours to see if additional adjustment is necessary.

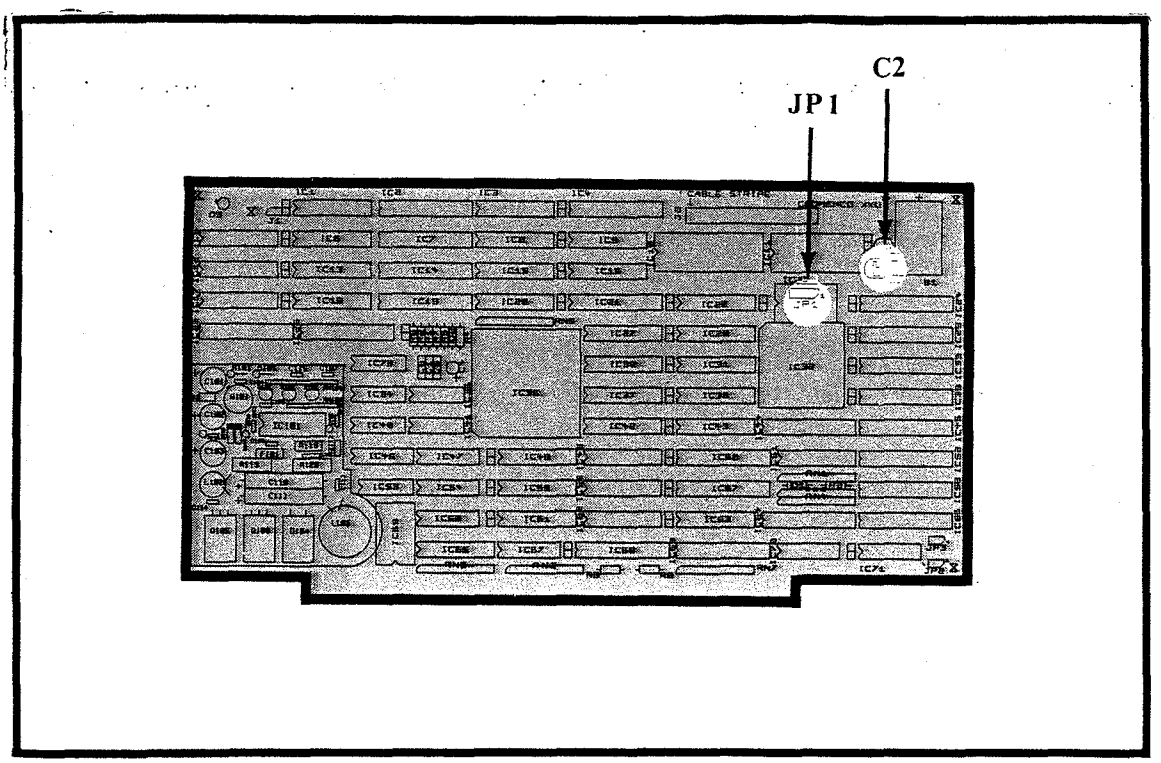

Figure 1-1. JUMPER AND ADJUSTABLE CAPACITOR LOCATIONS ON THE XXU

Cabling

If an XMU is being used in the system, connect the 34-conductor ribbon cable provided between the XXU and the XMU. Be sure that the red cable stripe is oriented correctly to the cable stripe arrow on the board.

Battery Replacement

When XDOS reports that the system clock has failed or when battery voltage falls below about 2.8V, it is time to replace the battery. Be certain to use an identical lithium battery as some manufacturers use a cathode material that results in an initial battery voltage exceeding the maximum voltage specification of the initial real-time clock chip.

THEORY OF OPERATION

S-100 Bus Operation

The XXU is designed to be compatible with most of the existing Cromemco S-100 boards. Bus timing constraints are actually slightly relaxed when compared to the XPU.

The XXU supports the use of an extension to the S-100 protocol in which a 32-bit word can be transferred in one bus cycle. Two new bus signals: **sMURQ*** and **MUAK***, form a "handshaking" scheme which allows the XXU to make 32-bit requests and transfer long words with acknowledging slave devices.

The XXU supports only vertical memory configuration. The S-100 signal **PHANTOM*** (also known as **MEM_DISABLE***) is grounded on the XXU, thereby disabling 64KZ memories and forcing 256KZ memories to work only in the vertical mode.

The state machine on the XXU automatically compensates for MC68020 data requests for data widths greater than the addressed slave device can transfer. If a long word transfer is attempted with a word-wide device, the state machine causes two word-wide bus cycles to take place. Four bus cycles would be performed for byte-wide slave devices. Thus a programmer need not be concerned with the width of the slave device being addressed.

The XXU periodically (about every 16 microseconds) provides an opportunity for dynamic memory cards to refresh their data. The XXU performs a pseudo-opcode fetch cycle (a read cycle with **sM1** asserted) and pauses briefly thereafter, allowing these memory cards to perform a refresh cycle on their RAMs.

Cache Description

Because the MC68020 requires data at a much faster rate than a bus based system can provide, it is imperative to provide a zero wait-state storehouse of locally available data. In order to achieve highest performance, this local storage area (cache) must contain instructions and data that the processor is likely to reuse. The cache is filled automatically as the program executes. By tracking the data's source location in main memory, it is possible to load the cache with instructions and data from many different places in main memory. This enables cache operation to be completely transparent to the user, except for the dramatic increase in processor performance.

The XXU board can load main memory long words into cache at one of two different places or sets. The logical address from the MC68020 is divided into two parts. Address bits A12-2 are used to address in parallel, two RAM arrays known as Tag RAMS. A12-2 also address two sets of cache RAMs that hold the data or instructions for the processor.

The Tag RAMs store the address bits A23-13 and Function Code FC2 of any main memory location previously loaded into the cache. These RAMs are known as Tag RAMs since they contain a marker or tag for the location in main memory where this cache entry is located. Since there are two RAM arrays, two tags are output. If

either one of these tags matches the bits A23-13 and FC2 of the current processor read cycle, then the data in the set associated with that tag is the operand or instruction that the processor is requesting. It can then be provided to the processor without incurring any wait states. A match as described above is known as a cache read "hit". If neither tag matches, a read "miss" occurs and the data must be fetched from main memory and loaded into the cache.

Writes are handled in a slightly different manner, although the matching mechanism is as described above. If a write hit occurs, the byte or bytes being written out by the processor are updated in the cache and also written out to main memory. This technique of keeping main memory current is known as "write through". Write misses are performed to main memory without involving the cache. Once the cache is updated, the XXU employs the quick-write feature. The address and data for this particular write cycle are stored in registers external to the processor. The processor is then informed that the cycle is complete. This permits the MC68020 to continue operating from its internal or external cache if the next instuctions or operands are found there.

At the same time the XXU state machine completes the write cycle on the S-100 bus. This overlap of operation can permit the processor to complete up to ten or more instructions while the state machine finishes the write cycle to the slave device. Such overlap is especially effective when performing graphics operations, as the two-port memories frequently request many wait states.

Flushing the Cache

Certain system operations, such as DMA transfers from hard disk, can change main memory without updating the cache. When this occurs, the cache must be cleared or "flushed" so that it will be reloaded from main memory. Two resetable RAM chips called Valid RAMs, track which cache entries correspond to main memory and are therefore valid. Two RAMs are used so that supervisor and user information can be tracked separately.

Either or both of these Valid RAMS may be cleared under software control by the operating system, or by the hardware when a DMA write is detected. In the case where it is known that a DMA device always writes to only supervisor or user space, an unnecessary flush of the space not involved can be avoided. Consult the description of the Flush Control bit in Appendix A for details.

It should be noted that during DMA the MC68020 can continue executing out of cache. The quick-write feature permits the processor to continue during DMA until a read miss occurs or a second write cycle is requested.

MC68020 Address Space Mapping

The XXU uses Function Codes FC2-0, A31 and A30 to determine whether a cycle is one of the following:

- Memory
- Internal I/O
- External I/O
- Interrupt acknowledge

- Coprocessor
- Special

If an XMU is present and active, it also affects the space of each cycle.

Table 1-2 describes how this mapping is performed. External I/O indicates cycles that are performed on the S-100 bus to I/O devices. Internal I/O cycles are those to the ports on the XXU; no S-100 control signals are issued during these cycles. Internal I/O port assignments are described in Appendix A.

FC=2,3,5 or 6[3] Logical Address A31, A30	XMU Not Active		XMU Active	
	Super	User	Super	User
11	Ext. I/O	Ext. I/O	XMU says: Memory / I/O; Memory/ROM[2] / Ext. I/O	XMU [1]
10	Int. I/O	Ext. I/O	Int. I/O	XMU [1]
01[4]	Memory/ROM[2] Access mapped to user	Memory	XMU says: Memory / I/O; Memory/ROM[2] / Ext. I/O; Access mapped to user	XMU [1]
00	Memory/ROM[2]	Memory	XMU says: Memory / I/O; Memory/ROM[2] / Ext. I/O	XMU [1]

Notes: 1. "XMU" means XMU determines if access is to memory or external I/O.

2. "Memory/ROM" means: a. A16=0 ROM_ON software control bit is 0.
   b. A16=1 Memory

3. If FC = 0, 3, or 4, the cycle is aborted

4. When A31 & 30 = 01, a supervisor access is mapped into user space, for example, the external cache and the XMU behave as though FC2 = 0.

Table 1-2: XXU MAPPING

The MC68881 Floating-point Coprocessor is assigned coprocessor ID number 1. All other coprocessor cycles are aborted with **BERR***. MC68020 Breakpoint and Access Level Control cycles are also aborted.

MC68020 Interrupt Acknowledge cycles at level 1 are performed on the S-100 bus. All interrupt acknowledge cycles above level 1 are autovectored. The XXU does not provide translation for the interrupt vectors as did the XPU and DPU. **For this reason the system administrator must take care not to address any interrupting devices with fixed vector assignments (eg. the TU-ART, and PRI) at locations where they will generate interrupt vectors outside of the MC68020 user defined area. Only vectors above 40H should be used.**

Operation with the XMU

An XMU can be connected to the XXU to provide mapping and protection for 68020 Cromix-Plus or UNIX. The XXU state machine automatically adjusts the operation of the XXU when the XMU is active. Such adjustments include waiting for XMU approval before performing quick-writes and not interrupting XMU table walks with refresh cycles.

LED

The XXU contains a red LED. The LED is used by the XXU Resident Operating System (XDOS) to signal, via a flashing code, problems encountered during its power-on diagnostic tests. Please consult the sections devoted to XDOS in the 68020 Cromix-Plus System Administrator's Guide, the Introduction to UNIX System V.2 or the System 400/20 Manual for details.

Appendix A

PORT ASSIGNMENTS ON THE XXU

Internal I/O Port Characteristics

Internal I/O ports may be accessed only when the MC68020 is in supervisor mode. Any attempt by user mode operations to access internal I/O are mapped to external I/O space. (See Table 1-2.) All internal I/O ports are byte wide, but may be referenced with longer operands as the MC68020 dynamic bus sizing will automatically read or write as many bytes as necessary.

An internal I/O port address is as follows:

A31	A30	A29-A7	A6-A0	
1	0	xxx	port#	xxx are "don't care" bits, but should be 0.

The following description of the ports gives bit assignments for read and write operations.

Port#

00	Out:	Control	(At Power On or reset, this port is cleared all zeroes.)
		D7-D5	Unused. Always write as zeroes.
		D4	SEPARATE SUPER and USER. D4=0 causes all external cache entries to be loaded into supervisor space. D4=1 separates the external cache into supervisor and user spaces. (See Cache Description.)
		D3	ROM ON*. D3=0 enables the Diagnostic/bootstrap ROM. (See Table 1-2.)
		D2	CACHE ON. D2=1 turns on the external cache.
		D1	FREEZE CACHE. D1=1 prohibits any new entries from being loaded into the external cache. Any entries already loaded will be used if the cache is on. Flushing occurs normally.
		D0	DMA FLUSH CONTROL. When D0=0 both supervisor and user spaces of the external cache are flushed, whenever a DMA write occurs. If D0=1, no automatic cache flushing occurs.

00	In:	Status	
		D7-D0	These bits read back as written above.
01	Out:	Flush	
		D7-D2	Unused. Always write as zeroes.
		D1	FLUSH SUPERVISOR. Writing a 1 in this bit flushes the supervisor space of the external cache.
		D0	FLUSH USER. Writing a 1 in this bit flushes the user space of the external cache.
01	In:	unused	
02	Out:	Clear NMI latch	
		D7-D0	Don't care. A write to this port clears the NMI latch.
02	In:	unused	
03	Out:	LED Control	
		D7-D1	Unused. Always write as zeroes.
		D0	LED ON. D0=1 turns on the LED Diagnostic light.
20-3F	In/Out:	Real-Time Clock	
			Consult Intersil's technical literature for the ICM7170 Real-Time Clock for the port assigments of this chip.

APPENDIX B

SCHEMATIC AND PART LIST

Part list for XXU
020-0176
List by Part Number

R3	75	001-0006	QTY.	1
R8,9	180	001-0009	QTY.	2
R6,7	330	001-0012	QTY.	2
R2	560	001-0015	QTY.	1
R1	1K	001-0018	QTY.	1
R120	RES 20,3W,WIREWOUND	001-0046	QTY.	1
R4,5	2K	001-0054	QTY.	2
R115	RES 16.9K .2SP	001-0158	QTY.	1
R118	RES 3.9 1/2W	001-0192	QTY.	1
R119	RES .05,3W WIREWOUND	001-0232	QTY.	1
R101	RES 820 .2SP	001-2182	QTY.	1
R114	RES 3.3K .2SP	001-2233	QTY.	1
RN1,2,3,4,5,6	1K	003-0011	QTY.	6
RN7	10K	003-0024	QTY.	1
RN102	RNET CUSTOM 7P,SIP	003-0076	QTY.	1
RN101	RNET CUSTOM 10P,SIP	003-0077	QTY.	1
C107	CAP .022UF,50V	004-0036	QTY.	1
CAP	DECUP	004-0061	QTY.	28
C112	CAP .047,50V .2SP	004-0061	QTY.	1
C101,102,103	CAP AL 470,6.3V	004-0091	QTY.	3
C4	47uF	004-0111	QTY.	1
C110,111	CAP PYCB, 3UF,50V	004-0130	QTY.	2
C114	CAP CRDC 100PF,50V	004-0137	QTY.	1
C106,113	CAP CRDC 220PF	004-0138	QTY.	2
C109	CAP .001UF,50V	004-0141	QTY.	1
C5	0.1uF	004-0143	QTY.	1
C105,115	CAP CRDC .1UF,10V	004-0143	QTY.	2
C108	CAP CRDC 1UF,50V	004-0147	QTY.	1
C6	47pF	004-0152	QTY.	1
C104	CAP .01UF,25V	004-0153	QTY.	1
C2	CAP 5-30 PF	004-0160	QTY.	1
C3	18pF	004-0169	QTY.	1
C1	220pF	004-0180	QTY.	1
L101	IND 22UH	007-0000	QTY.	1
L103	IND 35UH	007-0024	QTY.	1
L102	IND 30UH	007-0025	QTY.	1
D102,105	DIODE 1N5231B	008-0006	QTY.	2
D1	1N5225	008-0014	QTY.	1
D3	TIL209	008-0019	QTY.	1
D2	1N5711	008-0033	QTY.	1
D101	DIODE 1N752,5.6	008-0056	QTY.	1
D103	DIODE UES 1002	008-0071	QTY.	1
D104	DIODE IR10TQ040	008-0072	QTY.	1
Q103	TRANS 2N3904	009-0001	QTY.	1

Q102,104	TRANS 2N3906	009-0002	QTY.	2
Q105	TRANS D45VH10	009-0035	QTY.	1
Q106	TRANS D44VH10	009-0047	QTY.	1
Q101	TRANS SCRS2600	009-0048	QTY.	1
IC60	74LS279	010-0039	QTY.	1
IC34	74LS74	010-0055	QTY.	1
IC35	74LS14	010-0061	QTY.	1
IC67	74LS148	010-0189	QTY.	1
IC101	SG3524	010-0326	QTY.	1
IC40,53	74F74	010-0337	QTY.	2
IC41	74F04	010-0374	QTY.	1
IC70,71	74F251	010-0389	QTY.	2
IC61	74AS760	010-0446	QTY.	1
IC1,6,13,18	74F521	010-0447	QTY.	4
IC3,8,15,63	74ALS541	010-0448	QTY.	4
IC46	74LS592	010-0449	QTY.	1
IC68	74ALS873	010-0450	QTY.	1
IC44,57,64,69	74ALS646	010-0451	QTY.	4
IC9	74AS573	010-0452	QTY.	1
IC62,66	74ALS573	010-0453	QTY.	2
IC54	74F169	010-0454	QTY.	1
IC29	74AS843	010-0455	QTY.	1
IC4	74AS841	010-0456	QTY.	1
IC47	74F174	010-0477	QTY.	1
IC72	74ALS35	010-0478	QTY.	1
IC21	74ALS996	010-0481	QTY.	1
IC11	7170	011-0121	QTY.	1
IC27,28,30,31 IC37,38,42,43	7C168_35	011-0123	QTY.	8
IC2,7,14,19	7C128_25	011-0124	QTY.	4
IC25,26	9150_25	011-0125	QTY.	2
IC32	MC68881	011-0139	QTY.	1
IC36	MC68020	011-0127	QTY.	1
SC4	4-40X1/4 PAN HD SLOT CAD SCREW	015-0076	QTY.	1
STDF1	4-40X3/16X7/16 HX THRDED STDF	015-0083	QTY.	1
SC1,2,3	SCREW 6-32X3/8,NYL/STEEL	015-0183	QTY.	3
NT1	NUTPLATE	016-0300	QTY.	1
HTSK	XXU	016-0398	QTY.	1
SCKT 24,33,39,45,50,52,58,65	8 PIN	017-0000	QTY.	12
SCKT 24,33,39,45,50,52,58,65	16 PIN	017-0002	QTY.	12
SCKT 5,12,16,17 20,22,48,49,51,55,56	20 PIN	017-0004	QTY.	11
SCKT 11	24 PIN	017-0005	QTY.	1
SCKT 10	28 PIN	017-0071	QTY.	1
SCKT 23,59	COMP LEAD SCKT	017-0327	QTY.	4
J2	XMM	017-0091	QTY.	1
SCKT 32	SCKT PGA 68	017-0361	QTY.	1
SCKT 36	SCKT PGA 114	017-0426	QTY.	1
F101	FUSE 7A,125V,AXIAL	018-0039	QTY.	1
SLPD	SILPAD, 3 REG	021-0185	QTY.	1

MNT1	TO 5 MNT. PAD	021-0186	QTY.	1
IC59	16.667MHZ	026-0046	QTY.	1
Y1	32.768KHZ	026-0044	QTY.	1
B1	3V	101-0006	QTY.	1

Programmable ICs

IC16 CPU_SPACE	PAL16L8_15	502-0159	010-0445	QTY.	1
IC17 VALID	PAL16R4	502-0160	010-0419	QTY.	1
IC56 RTC_SEL	PAL16R4_15	502-0161	010-0443	QTY.	1
IC48 FLUSH	PAL16L8	502-0162	010-0422	QTY.	1
IC49 IODECODE	PAL16L8	502-0163	010-0422	QTY.	1
IC51 DATA	PAL16L8_15	502-0164	010-0445	QTY.	1
IC55 DMA	PAL16R4	502-0165	010-0419	QTY.	1
IC5 TAG_CTL	PAL16L8_15	502-0166	010-0445	QTY.	1
IC12 HIT	PAL16L8_15	502-0167	010-0445	QTY.	1
IC22 DATA_CTL	PAL16L8_15	502-0168	010-0445	QTY.	1
IC20 CYCLES	PAL16L8_15	502-0169	010-0445	QTY.	1
IC10 XDOS	XDOS	502-0170	011-0140	QTY.	1
IC24 STARTER	PAL22V10A	502-0171	010-0480	QTY.	1
IC50 SIZER	PAL22V10A	502-0172	010-0480	QTY.	1
IC33	XXU ST.MACH.0	502-0214	010-0417	QTY.	1
IC39	XXU ST.MACH.1	502-0215	010-0417	QTY.	1
IC45	XXU ST.MACH.2	502-0216	010-0417	QTY.	1
IC52	XXU ST.MACH.3	502-0217	010-0417	QTY.	1
IC58	XXU ST.MACH.4	502-0218	010-0417	QTY.	1
IC65	XXU ST.MACH.5	502-0219	010-0417	QTY.	1

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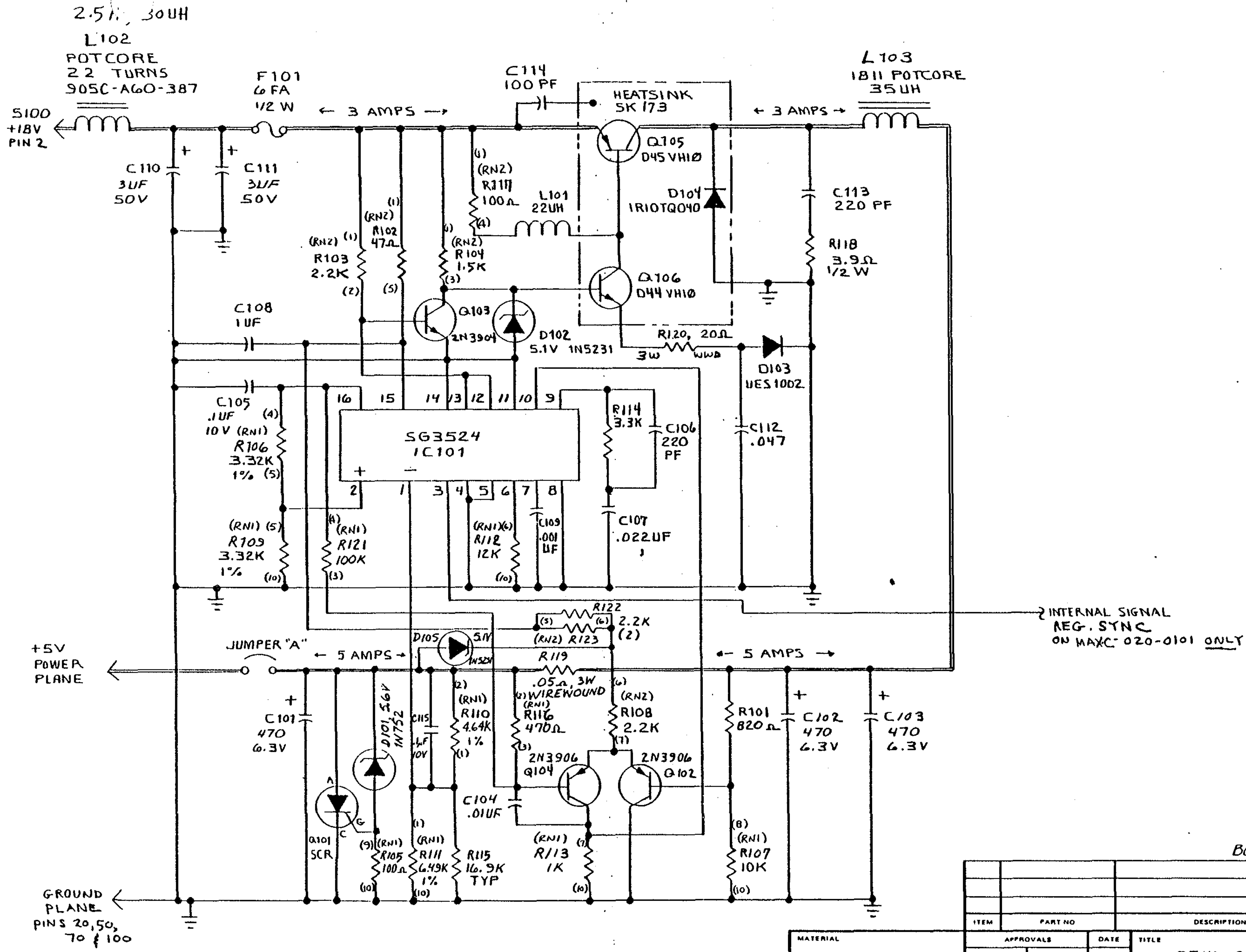
REVISIONS				



BOARD REV. B

ITEM	PART NO	DESCRIPTION	MANUFACTURER

MATERIAL	APPROVALS	DATE	TITLE
	DESIGNER		25W S100 BOARD SWITCHING POWER SUPPLY
FINISH	DRAFTSMAN		
	CHECKER		

Cromemco incorporated

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

SIZE	PRODUCT	DWG. TYPE	ID NUMBER	REV
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SCALE — SHEET 3 OF 3

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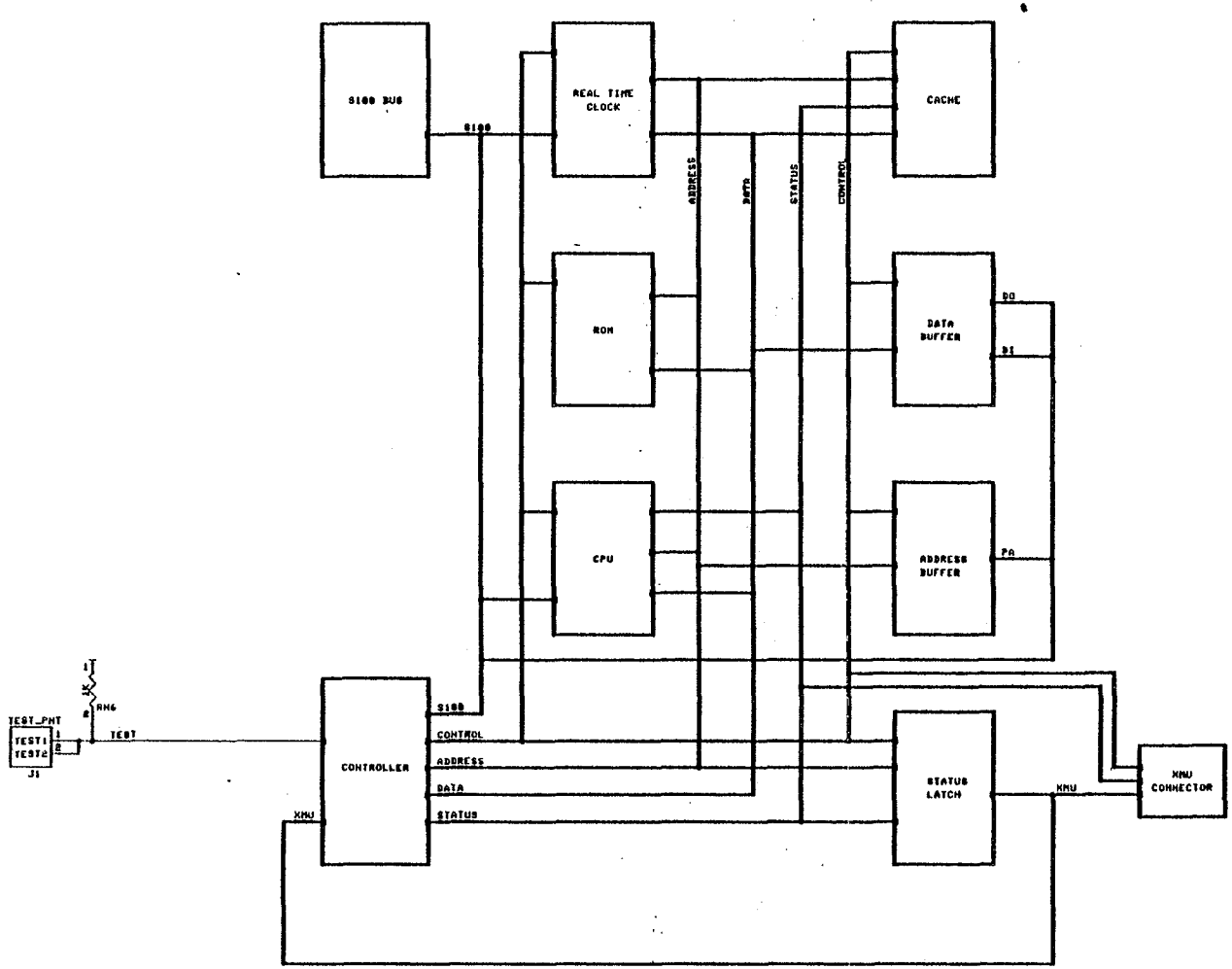
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D1
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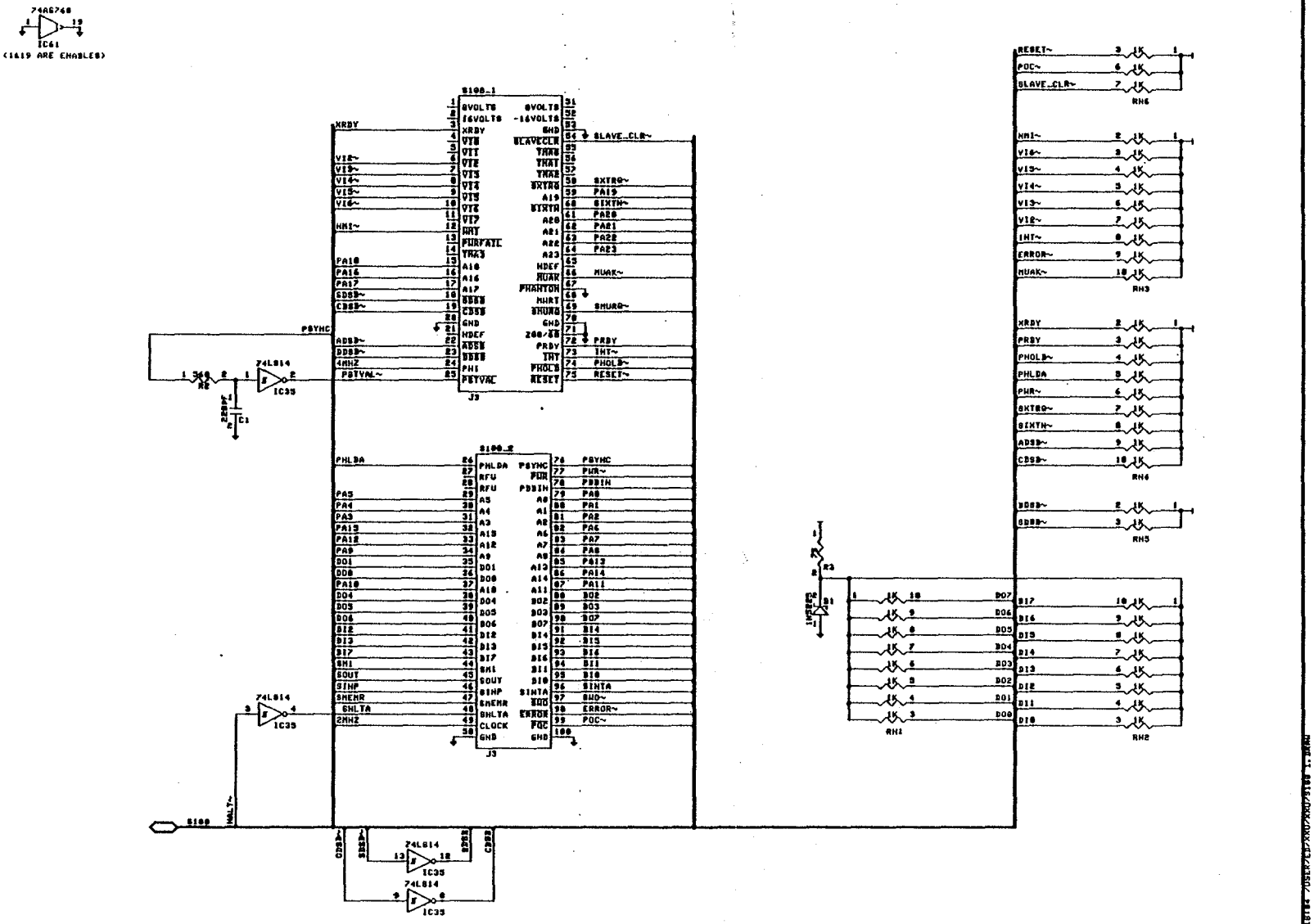
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PA6
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PA8
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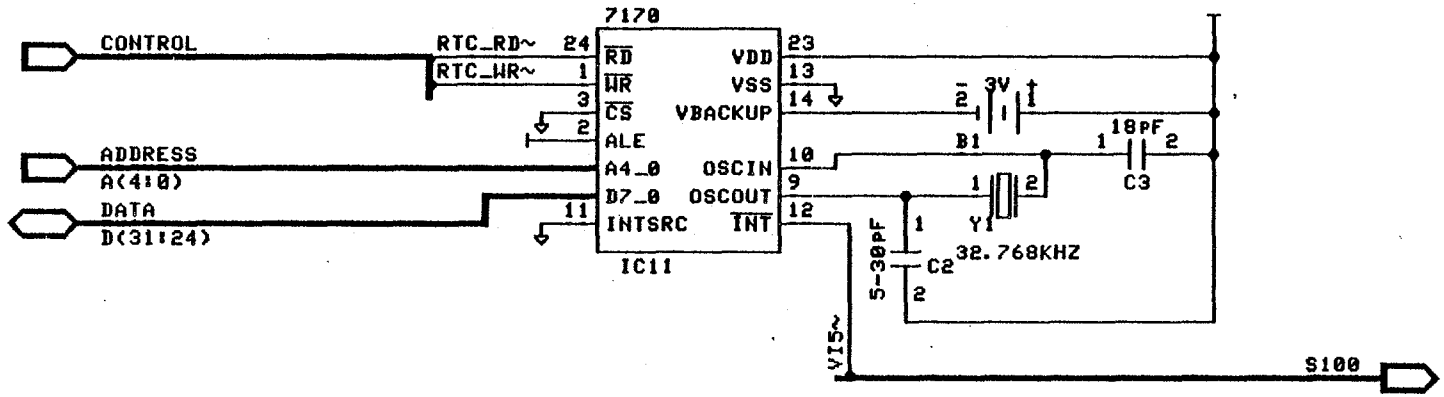
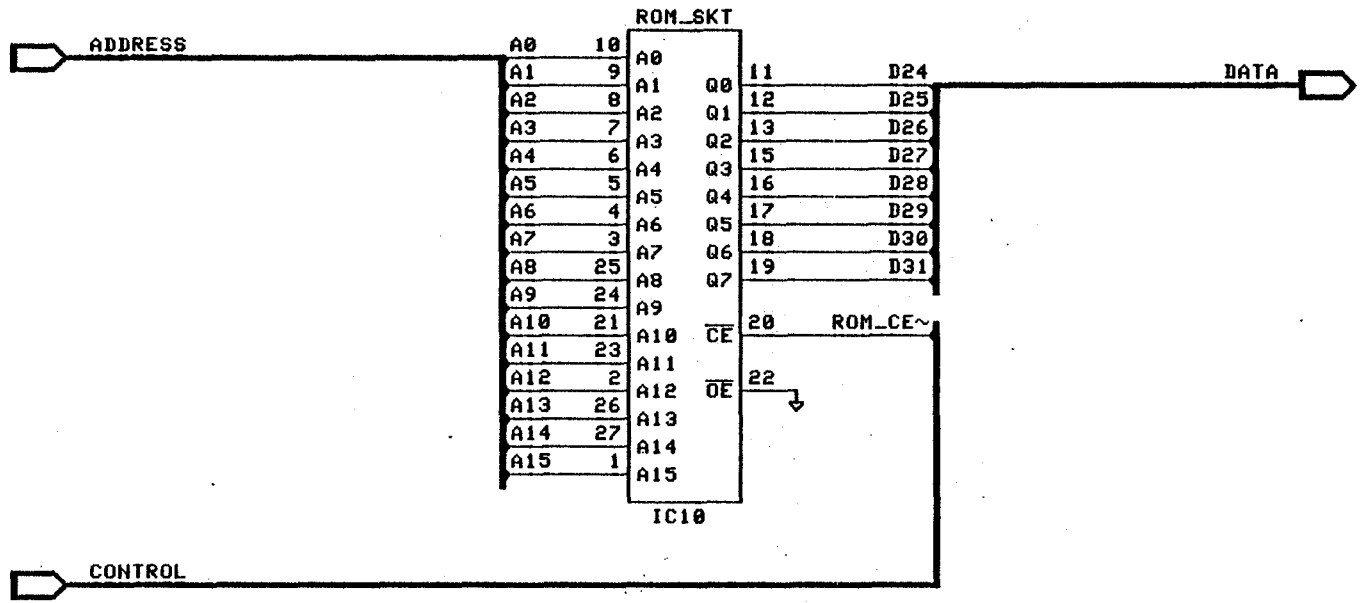
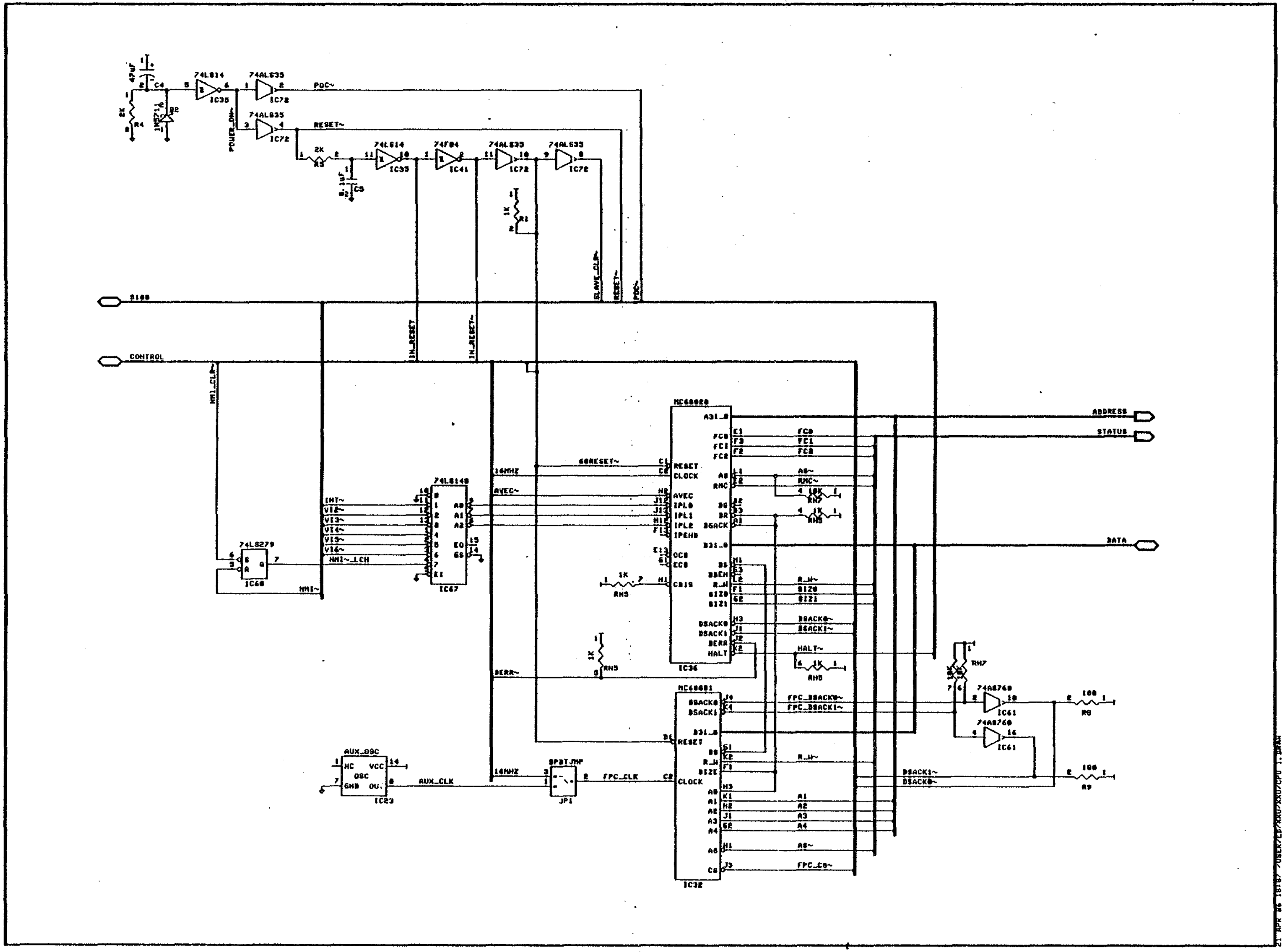
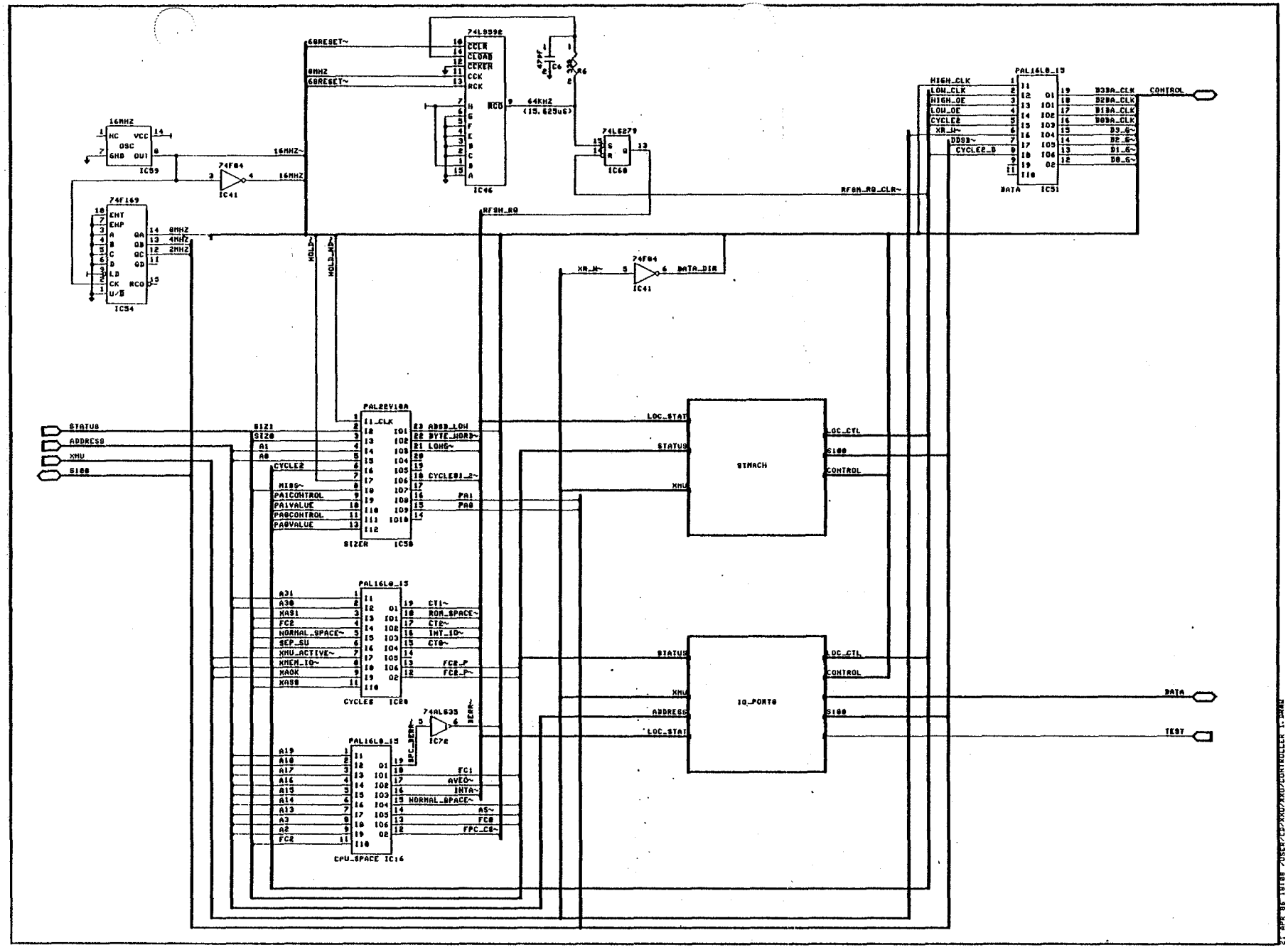
1K

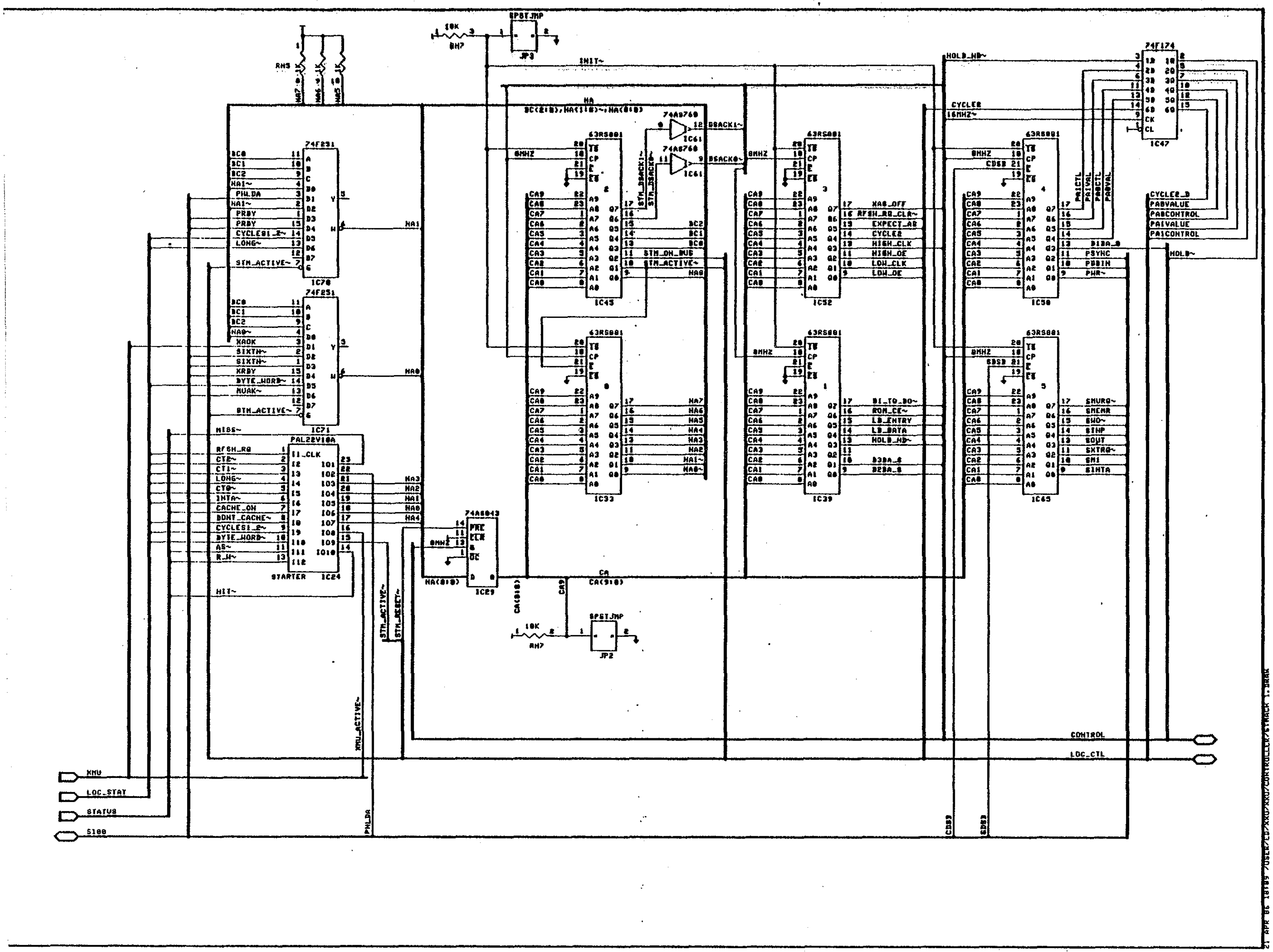




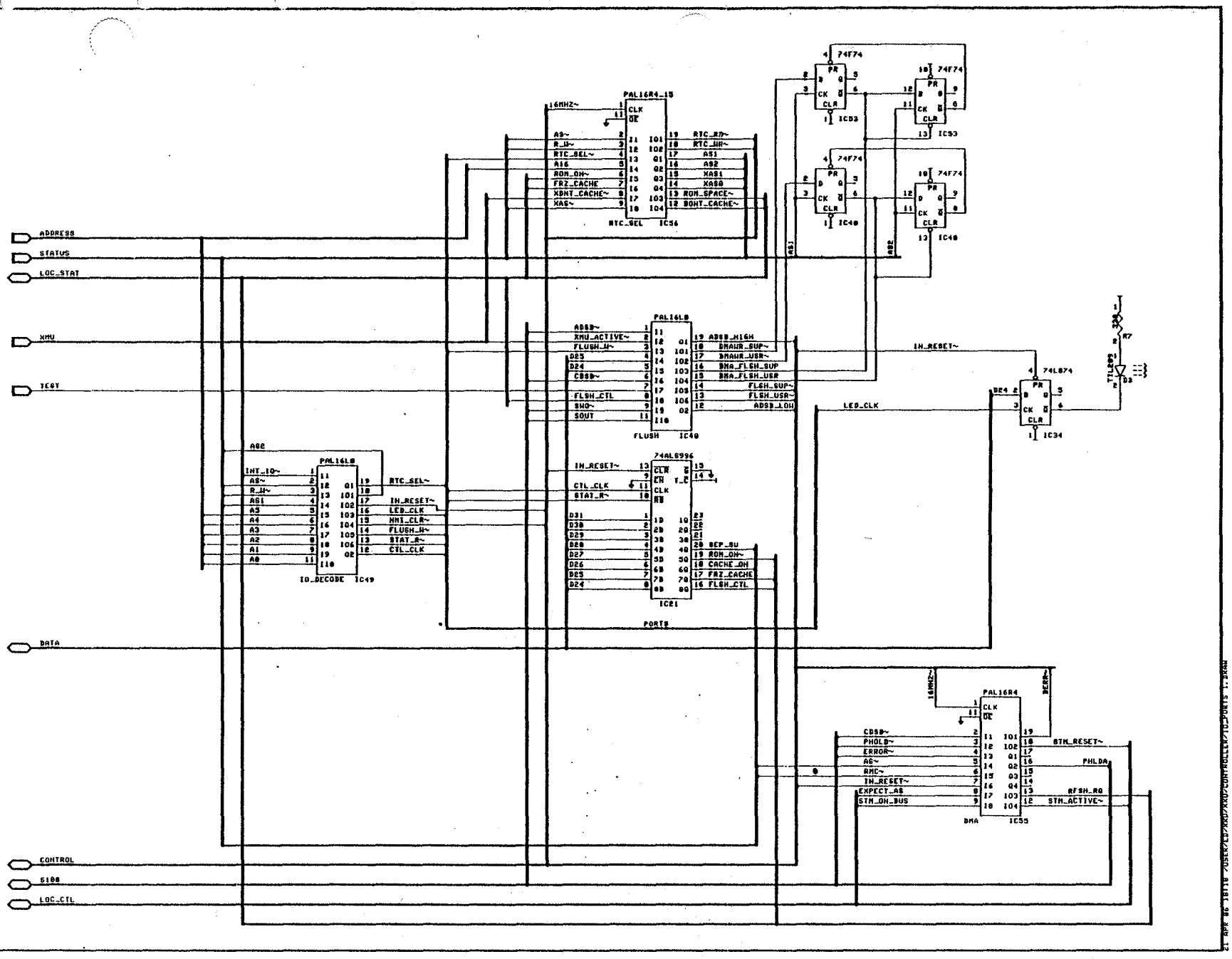


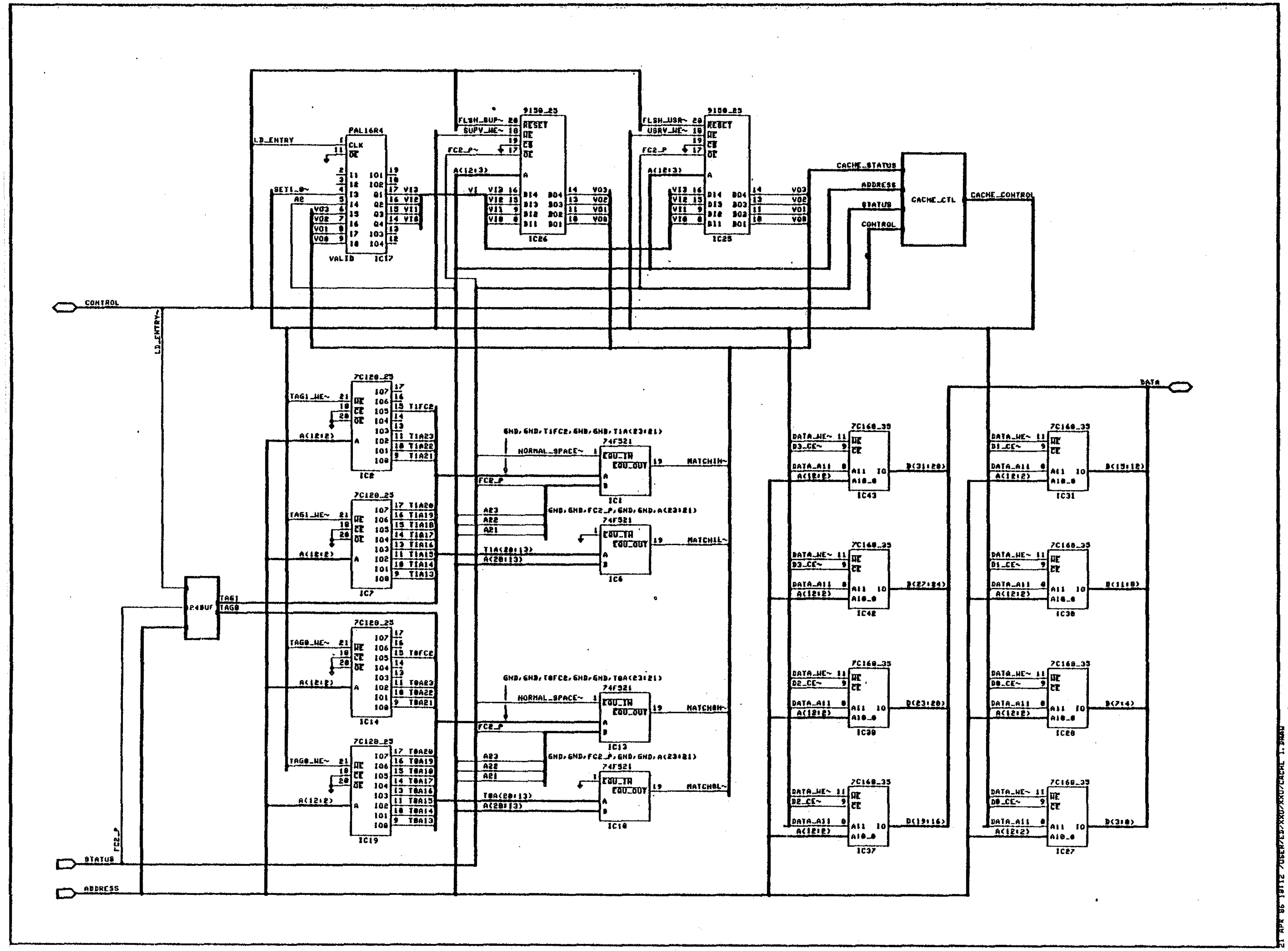
21 APR 86 10:07 /USER/ED/XXU/XXU/CPU 1.DRAW


74LS398
IC46
74LS279
IC60
16MHZ
IC59
74F04
IC41
74F169
IC54
PAL16L8_15
IC51
PAL22V10A
SIZER
IC58
PAL16L8_15
CYCLES
IC28
74ALS35
IC72
PAL16L8_15
CPU_SPACE IC16
SYNACH
IO_PORTS
STATUS
ADDRESS
XMU
S100
DATA
TEST
CONTROL
60RESET~
8MHZ
64KHZ
(15.625uS)
16MHZ~
RFSH_RQ
RFSH_RQ_CLR~
HOLD~
HLDA~
XR_W~
DATA_DIR
LOC_STAT
LOC_CTL
SIZ1
SIZ0
A1
A0
CYCLE2
M1OS~
PAICONTROL
PAIVALUE
PA0CONTROL
PA0VALUE
ABSB_LOH
BYTE_WORD~
LOW8~
CYCLES1_2~
PA1
PA0
A31
A30
XA31
FC2
NORMAL_SPACE~
SCP_SU
XMU_ACTIVE~
XMEM_IO~
XA0K
XA30
CTI~
ROM_SPACE~
CTE~
INT_IO~
CTO~
FC0_P
FC0_P~
A19
A18
A17
A16
A15
A14
A13
A3
A2
FC2
BPC_BERR~
BERR~
FC1
AVEO~
INTA~
AS~
FC0
FPC_C0~
HIGH_CLK
LOW_CLK
HIGH_OE
LOW_OE
CYCLE2
XR_W~
DD0B~
CYCLE2_0
B3BA_CLK
B2BA_CLK
B1BA_CLK
B0BA_CLK
B3_0~
B2_0~
B1_0~
B0_0~

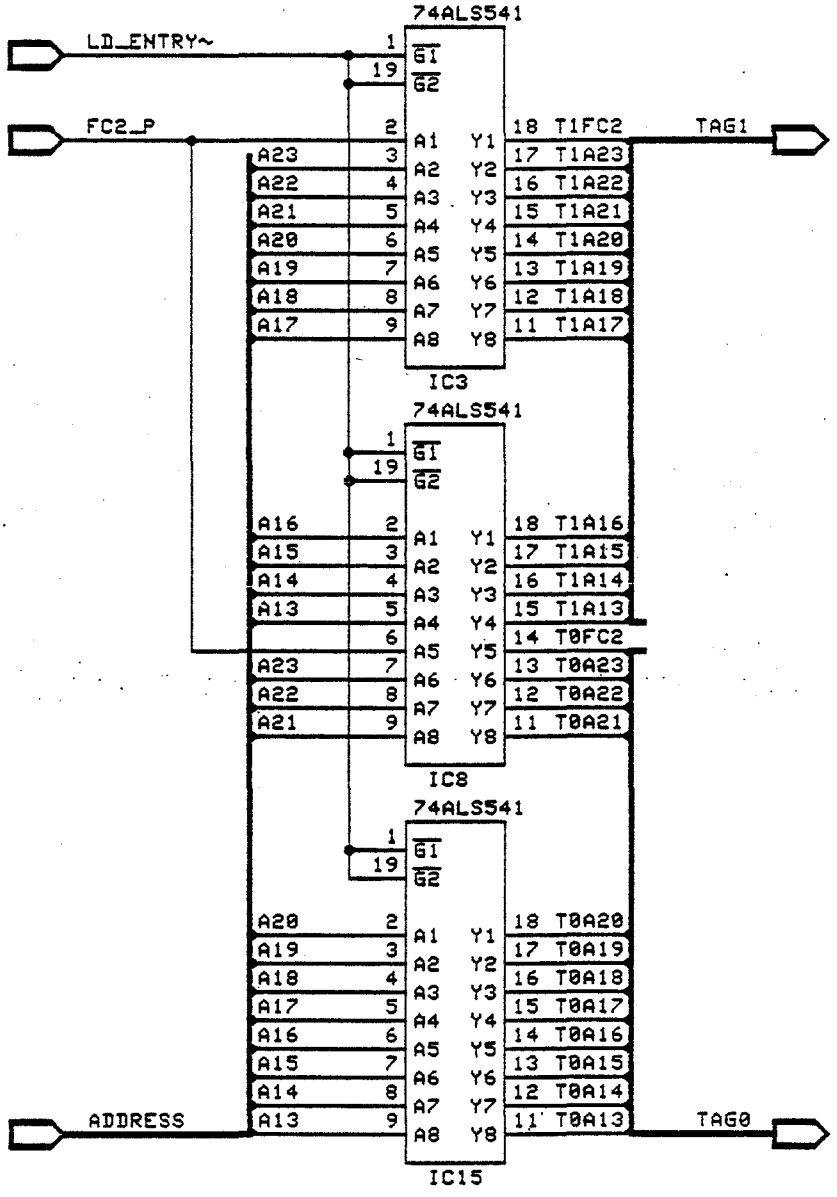


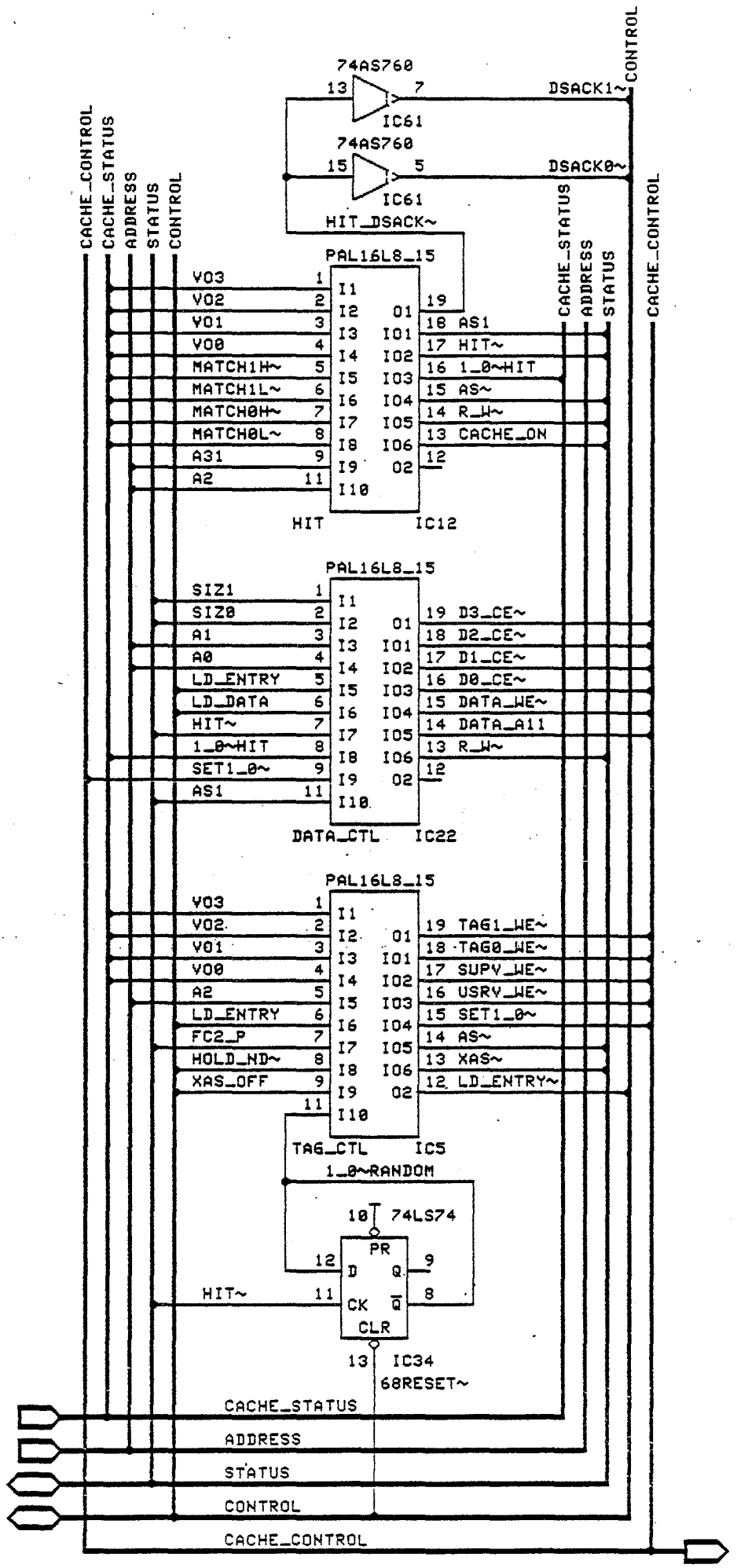
74F251
IC70
74F251
IC71
PAL22V10A
STARTER
IC24
74AS043
IC29
74AS760
IC61
63RS081
IC45
IC33
IC52
IC39
IC50
IC65
74F174
IC47
SPST JMP
JP3
JP2
10K
RN7
RN5
INIT~
HOLD_HD~
CYCLE2
16MHZ~
8MHZ
DSACK1~
DSACK0~
STM_ACTIVE~
STM_RESET~
XMU_ACTIVE~
HIT~
MISS~
PHLDA
CONTROL
LOC_CTL
XMU
LOC_STAT
STATUS
S100
XA0_OFF
RFSH_RQ_CLR~
EXPECT_A0
HIGH_CLK
HIGH_OE
LOW_CLK
LOW_OE
BI_TO_BO~
ROM_CE~
LD_ENTRY
LD_DATA
PSYNC
PDBIN
PWR~
SMWRO~
SMEMR
SHO~
SINP
SOUT
SXTRQ~
SM1
SINTA
CYCLE2_D
PA0VALUE
PA0CONTROL
PA1VALUE
PA1CONTROL
HOLD~


ADDRESS
STATUS
LOC_STAT
XMU
IEGT
DATA
CONTROL
S100
LOC_CTL
PAL16R4_15
16MHZ~
RTC_SEL
IC56
74F74
IC53
IC40
PAL16L8
FLUSH
IC40
74ALS996
PORTB
IC21
74LS74
IC34
IN_RESET~
LED_CLK
PAL16L8
IO_DECODE
IC49
PAL16R4
BMA
IC55
PHLDA
BFSH_RQ
STM_RESET~
STM_ACTIVE~



PAL16R4
IC17
VALID
LD_ENTRY
SET1_0~
9150_25
IC26
IC25
FLSH_SUP~
SUPV_WE~
FLSH_USR~
USRV_WE~
RESET
FC2_P~
FC2_P
A(12:3)
CACHE_STATUS
ADDRESS
STATUS
CONTROL
CACHE_CTL
CACHE_CONTROL
7C128_25
IC2
IC7
IC14
IC19
TAG1_WE~
TAG0_WE~
A(12:2)
74F521
IC1
IC6
IC13
IC18
NORMAL_SPACE~
EQU_IN
EQU_OUT
MATCH1H~
MATCH1L~
MATCH0H~
MATCH0L~
244BUF
TAG1
TAG0
7C168_35
DATA_WE~
DATA_A11
IC43
IC42
IC38
IC37
IC31
IC30
IC28
IC27
D(31:28)
D(27:24)
D(23:20)
D(19:16)
D(15:12)
D(11:8)
D(7:4)
D(3:0)
DATA
CONTROL
STATUS
ADDRESS
21 APR 86 19:12 /USER/LD/XXD/XXD/CACHE_1.DRAW





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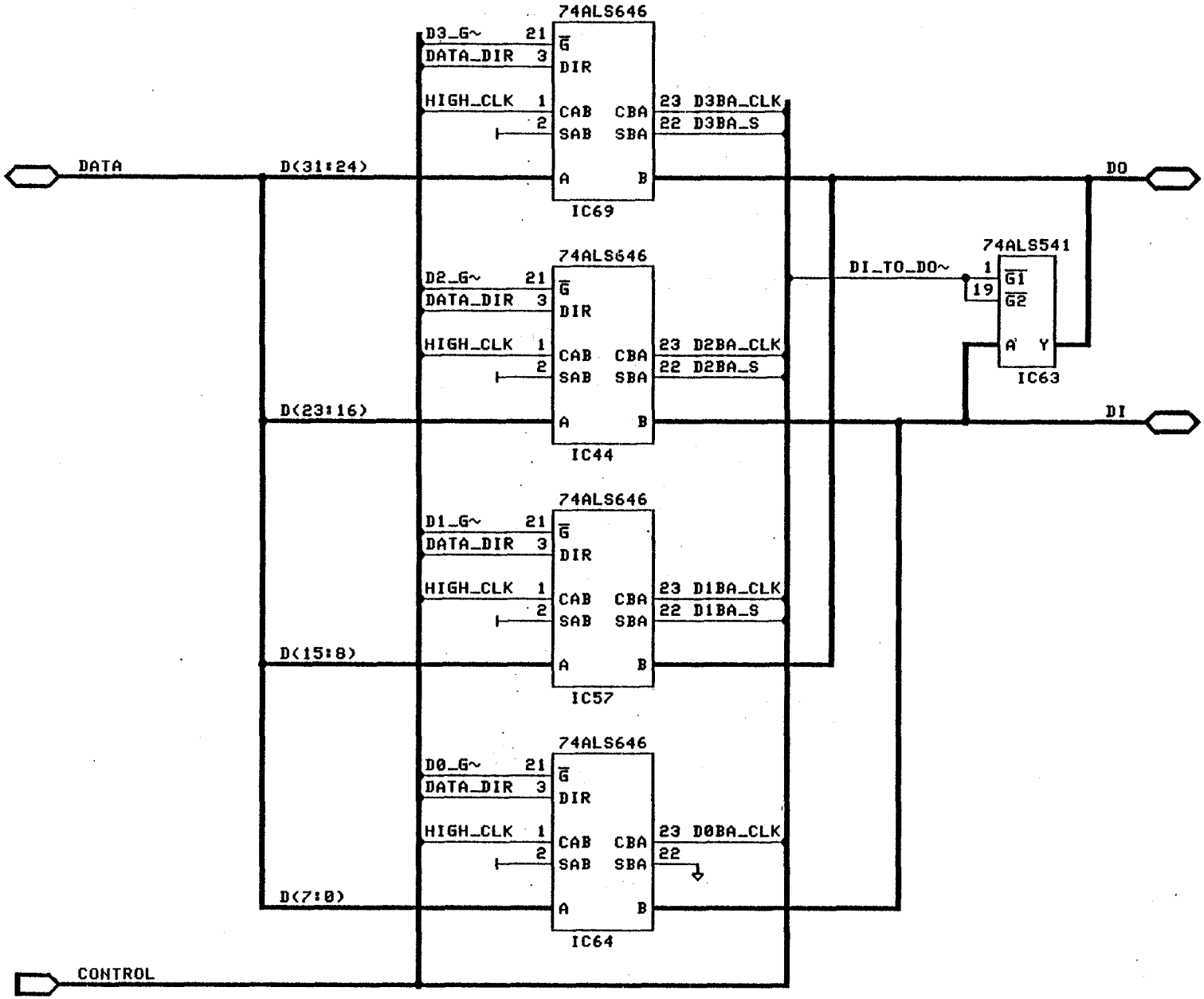

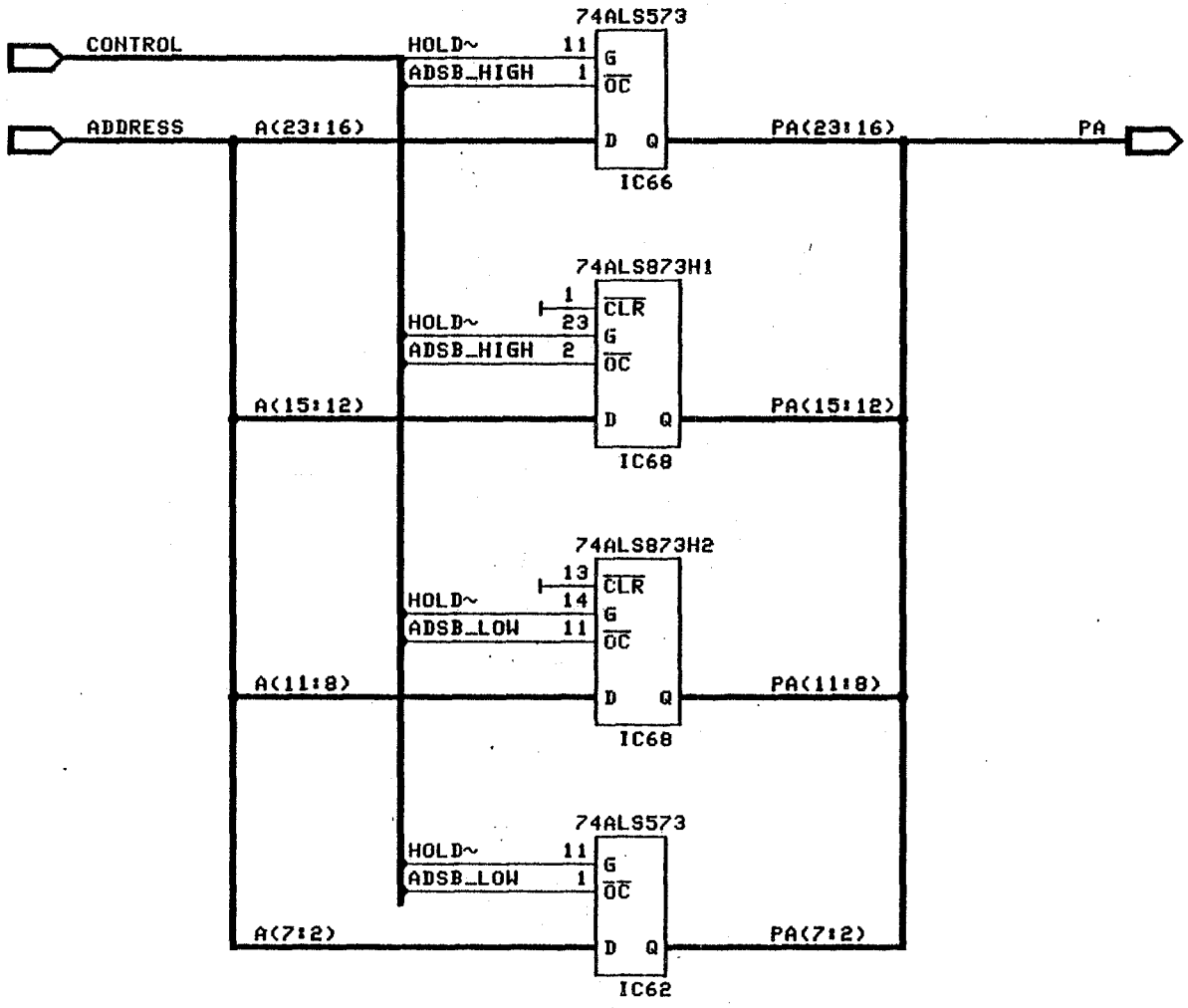

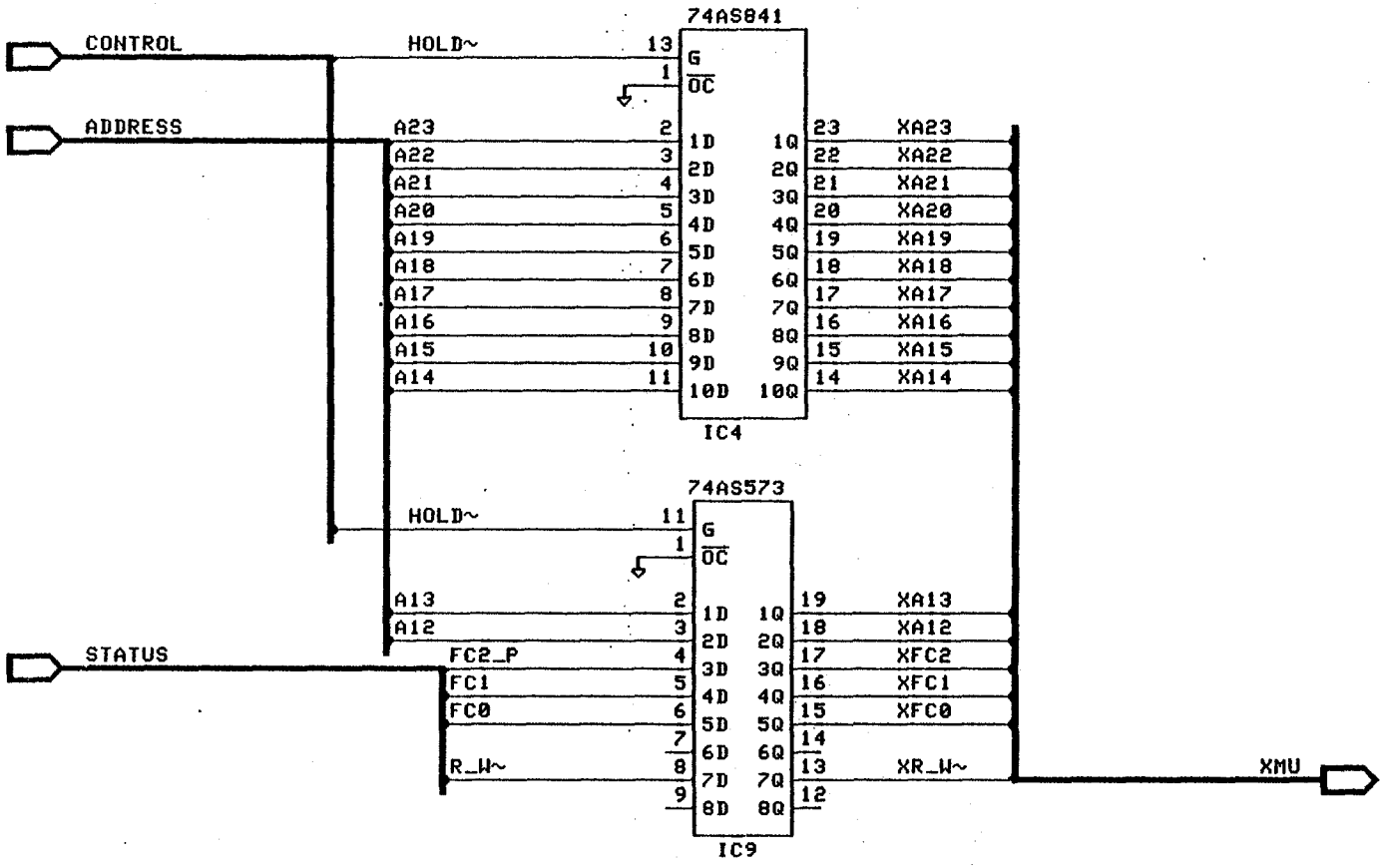

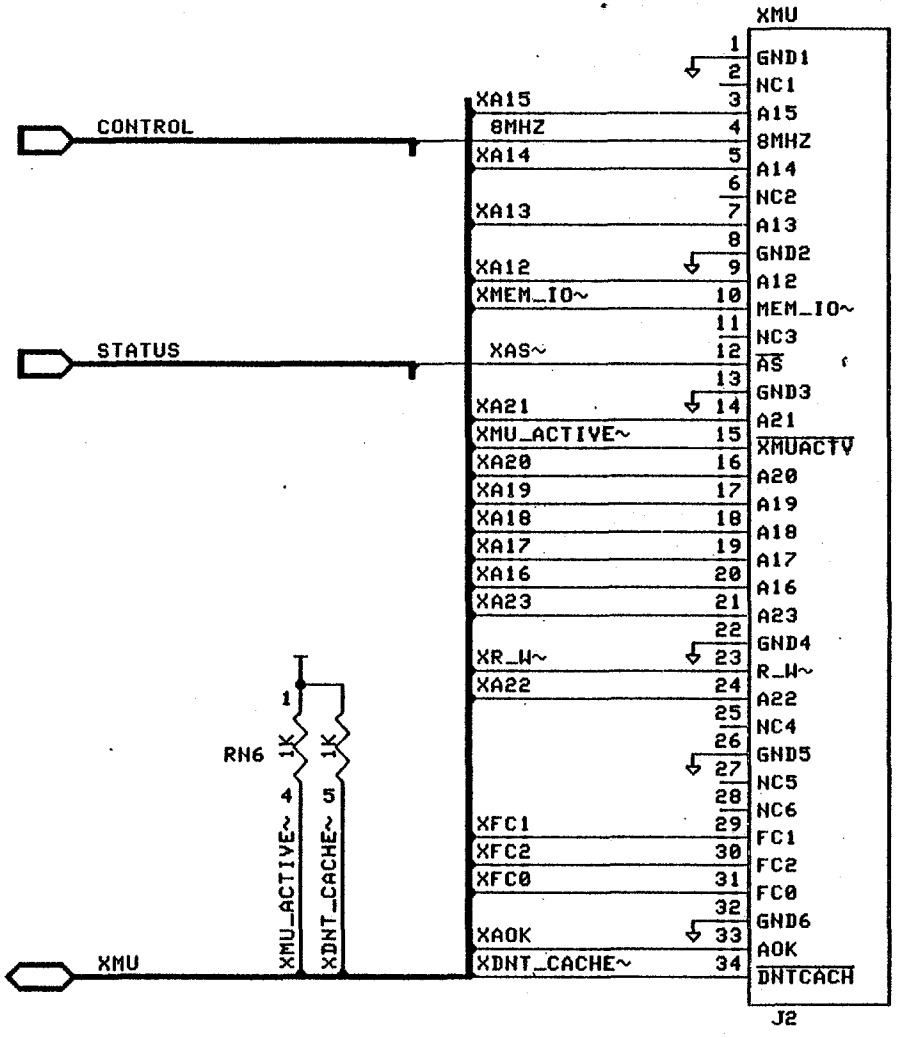

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