

Cromemco

XMM

Installation Manual

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Installation Manual

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LIMITED WARRANTY

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Chapter 1

THE XMM MEMORY MANAGER

The Cromemco XMM Memory Management board provides S-100 bus systems with an efficient, highly flexible means of sharing up to 16 megabytes of memory among several programs.

In conjunction with Cromemco's XPU dual processor board and UNIX System V Operating System, the XMM allocates memory in 4K-byte pages for up to 16 concurrent processes. Page references and modifications are logged so that, if memory must be released for use by another process, the operating system can either erase the least-used page (if it has not been modified) or copy it out to a disk.

The XMM translates (or maps) each logical address generated by a program into a physical address chosen by the operating system. This logical-to-physical address translation, performed by a high-speed table lookup, effectively isolates the ongoing processes from the hardware and from each other. Each program appears to have the entire system to itself, and software errors are unlikely to spread from one program to another.

Each page or segment (128 pages) of memory can be shared by several users, with varying degrees of access, or held exclusively by the supervisor or a single user. Code and data can be separated in memory to prevent faulty instructions, such as attempts to execute data. Sensitive data can be restricted to read-only access, and special programs, such as compilers, can be made accessible for execution yet remain unexaminable to all but the supervisor.

In addition to page usage, the XMM keeps track of where each page resides, and will interrupt the processor if a requested page is not in main memory (page fault). These features support the development of virtual memory software, which allows a program to run with only part of its code in memory, while the remaining pages of code are swapped to and from the disk as needed.

Table 1-1 lists the XMM's operational specifications.

Table 1-1: XMM SPECIFICATIONS

Addressable Memory:	16 megabytes
Clock Rate:	10MHz
I/O Port Address:	FCh
Boards Supported:	All Cromemco 16-bit memory boards
Bus:	S-100/IEEE-696
Power Requirements:	+18 volts @ 1.4 amps
Operating Environment:	0 to 55 degrees C

INSTALLING THE XMM BOARD

Switch Settings

None.

Jumper-Selectable Options

Port Address - The port address of the XMM board is factory-set at FCh by a jumper at A1 (Figure 1-1). If necessary, a different address can be selected by adding the appropriate combination of jumpers at A1 through A7.

Cables

XPU Cable - Insert the XMM in an S-100 bus slot (as described in your system manual) next to the XPU board. Install the XPU cable (Cromemco part number 519-0062) from the 34-pin connector at the top of the XMM board (Figure 1-1) to the corresponding connector on the XPU. The red cable stripe must be to the left on both boards (as seen from the component side).

MEMORY MAPPING

The XMM divides the 16-megabyte memory space, provided by the 24 address lines of the MC68000/68010, into 4,096 pages of 4K bytes each. The pages are grouped into 32 segments of 128 pages (1/2 megabyte) each. Every memory reference is translated (mapped) into one of the 4K-byte pages in physical memory.

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 1. The XMM Memory Manager

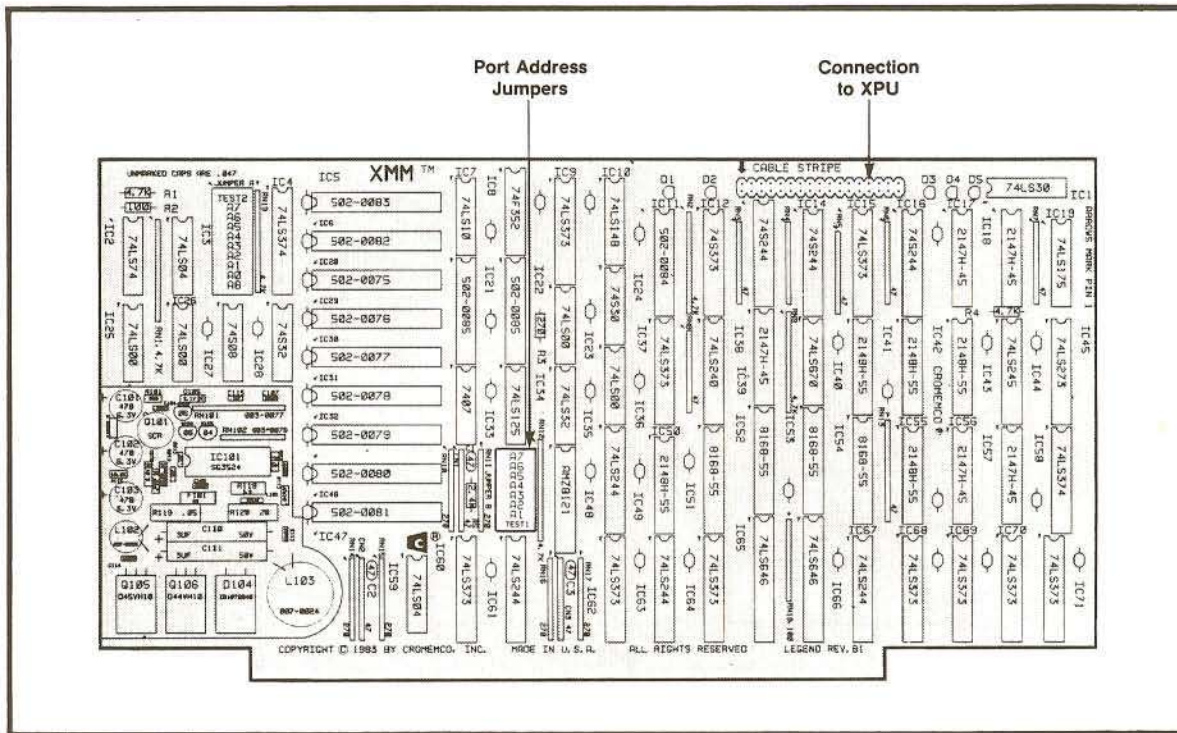


Figure 1-1: THE XMM BOARD

MC68000/68010 Processor - Figure 1-2 depicts the basic translation process for the MC68000/68010 processor. Logical address lines A23 through A12 are sent directly to the XMM via the overhead cable from the XPU. The segment number (0-31), determined by bits A23 through A19, points to a record in the segment table for the current process (each process has its own segment table). An entry in each record of the segment table points to the page table (the Translation Lookaside Buffer, or TLB) for that segment. The local page number (0-127), determined by bits A18 through A12, points to a record in the page table holding the base address of a 4K-byte page in physical memory. In effect, the XMM takes a 12-bit logical page number (the combined segment and local page number) and converts it to a 12-bit physical page number. The physical page number (0-4095), along with the byte number from bits A11 through A0, constitutes the complete physical address where the data is stored.

The byte number is not translated, but goes directly from the XPU to the S-100 bus.

The address translation proceeds only after the legality of the access is verified. For each memory access, the MC68000/68010 processor defines the three variables of access type: user or supervisor, code or data, read or write. The operating system initializes an access control table, listing every combination of access type, page type, and segment type as either legal or illegal. The XMM automatically checks this table before each translation.

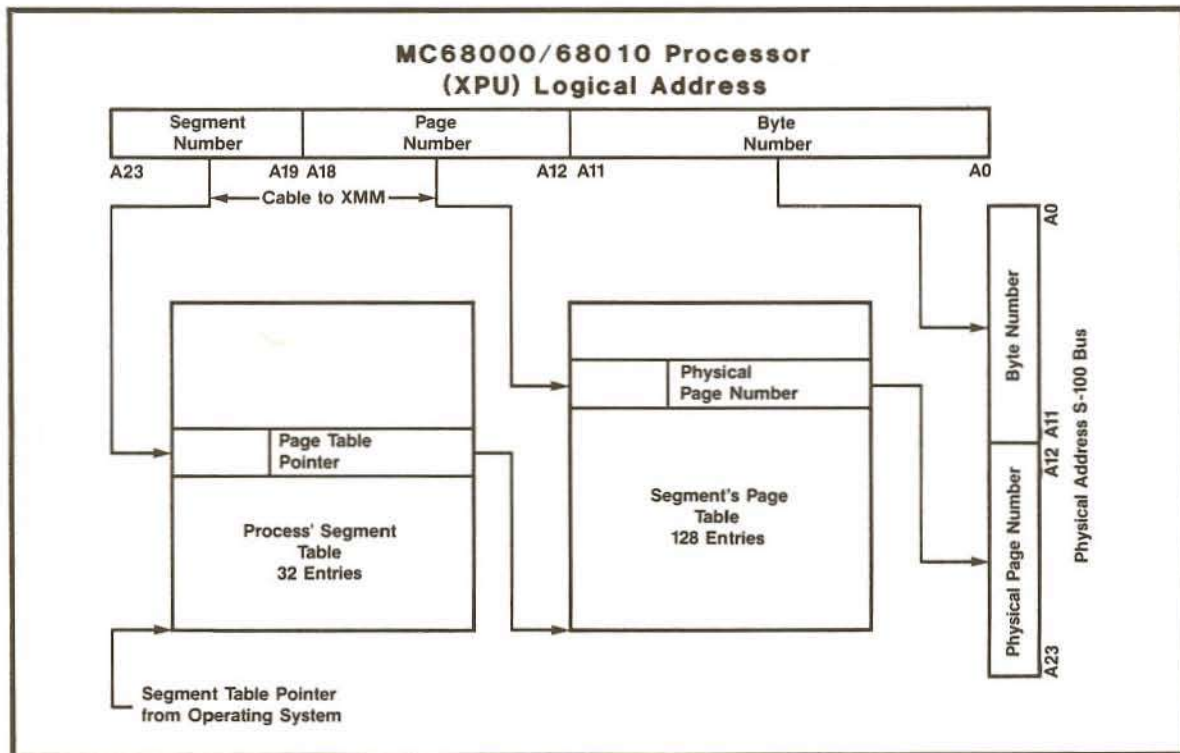


Figure 1-2: LOGICAL-TO-PHYSICAL ADDRESS TRANSLATION

Z80A Processor - Memory mapping for the Z80 processor is simpler than for the MC68000/68010. Since the Z80's 16 address lines limit it to 16 pages (64K) of memory, separate page and segment tables are unnecessary. The logical page number (0-15), determined by bits A15 through A12, selects the physical page number directly from the page table (actually a segment table used as a page table). The Z80 pages can be anywhere in the 16-megabyte address space. Memory protection, however, is not provided because, unlike the MC68000/68010 processor, the Z80 does not define access types.

The XMM assumes that all Z80 pages are resident in main memory and accessible to all users in any mode.

Input and Output - All I/O references are mapped to the top 64K bytes of memory (FF0000h to FFFFFFFh). When an address translates into this range, the XMM notifies the XPU to perform an I/O cycle rather than a memory cycle.

For more information on the XMM board, refer to the Cromemco XMM Technical Reference Manual, part number 023-2010.

Chapter 2

XMM/XPU SIGNAL DEFINITIONS

The 34-conductor cable linking the XMM and XPU conveys both control and address signals for memory mapping. This chapter defines the control signals. The pin assignments for all of the XMM/XPU signals are shown in Table 2-1. An asterisk indicates that the signal is active low; signals without the asterisk are active high.

Signals for Z80 Mapping

Memory Request - The Z80 MREQ* signal indicates the start of a Z80 memory cycle. The XMM uses this signal to adjust the timing of mapped Z80 cycles to correspond to unmapped cycles.

M1* - The Z80 M1* signal indicates the start of either an instruction fetch cycle or an interrupt acknowledge cycle. The XMM uses this signal to adjust the timing of mapped Z80 cycles to correspond to unmapped cycles.

Input/Output Request - The Z80 IOREQ* signal is true whenever an I/O or interrupt acknowledge cycle is performed. The XMM uses this signal to adjust the timing of mapped cycles to correspond to unmapped cycles.

Z80 Ready - The ZRDY signal from the XMM notifies the XPU that the Z80 cycle may proceed. During mapping, Z80 cycles are delayed to allow time for translation of address bits A15 through A12 to S-100 address bits A23 through A12.

Signals for MC68000/68010 Mapping

Clock - The 10MHZ clock signal from the XPU synchronizes the XMM and XPU boards. This signal provides the basic timing for all XMM operations.

CPU Transfer Enable - The EN68000/68010 signal notifies the XMM that the XPU is about to switch from the Z80 processor to the MC68000/68010 processor.

MC68000/68010 Control Signals - AS*, R/W*, and FC0-2 are the Address Strobe, Read/Write, and Function Code control signals from the MC68000/68010 processor. They describe the type of cycle being performed by the MC68000/68010.

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 2. XMM/XPU Signal Definitions

XMM-Active* - The XMM-Active* signal is true while the XMM board is enabled. This signal forces the XPU to disable the drivers for address lines A23 through A12 and to examine the AOK and MEM/IO* lines to determine the type and validity of the cycle being executed.

Memory/IO - The MEM/IO signal from the XMM notifies the XPU to run either a memory cycle or an I/O cycle. This signal can occur only if the XMM has been enabled.

Address OK - The AOK signal from the XMM prevents the XPU from starting an S-100 bus cycle until the address has been translated and proven valid. This signal can occur only if the XMM has been enabled.

Table 2-1: XPU/XMM SIGNALS

Pin	Signal	Source	Definition
1	GND	BOTH	Ground
2	MREQ*	XPU	Z80 Memory Request Control Line
3	A15	XPU	MC68000/68010/Z80 Address Line 15
4	10MHZ	XPU	10MHz Master Clock
5	A14	XPU	MC68000/68010/Z80 Address Line 14
6	M1*	XPU	Z80 M1 Cycle Control Line
7	A13	XPU	MC68000/68010/Z80 Address Line 13
8	GND	BOTH	Ground
9	A12	XPU	MC68000/68010/Z80 Address Line 12
10	MEM/IO*	XMM	MC68000/68010 Memory or I/O Cycle
11	IOREQ*	XPU	Z80 I/O Request Control Line
12	AS*	XPU	MC68000/68010 Address Strobe Control Line
13	GND	BOTH	Ground
14	A21	XPU	MC68000/68010 Address Line 21
15	XMM-ACTIVE*	XMM	XMM turned on and mapping
16	A20	XPU	MC68000/68010 Address Line 20
17	A19	XPU	MC68000/68010 Address Line 19
18	A18	XPU	MC68000/68010 Address Line 18
19	A17	XPU	MC68000/68010 Address Line 17
20	A16	XPU	MC68000/68010 Address Line 16
21	A23	XPU	MC68000/68010 Address Line 23
22	GND	BOTH	Ground
23	R/W*	XPU	MC68000/68010 Read/Write Cycle Control Line
24	A22	XPU	MC68000/68010 Address Line 22
25	ZRDY	XMM	Z80 Cycle may proceed (delayed during mapping)
26	GND	BOTH	Ground
27	GND	XMM	Ground
28			Unused
29	FC1	XPU	MC68000/68010 Function Code Bit 1 Control Line
30	FC2	XPU	MC68000/68010 Function Code Bit 2 Control Line
31	FC0	XPU	MC68000/68010 Function Code Bit 0 Control Line
32	GND	BOTH	Ground
33	AOK	XMM	MC68000/68010 address translation permitted and complete
34	EN68010	XPU	Control will transfer from Z80 to MC68000/68010

Appendix A

LED CODES

There are five LED's near the top of the XMM board (refer to Figure 1-1). The yellow diode, D1, flashes on each Z80 address translation. The green diode, D2, flashes on each MC68000/68010 address translation. The red diodes, D3-D5, indicate errors, as shown in the following table (a "1" means that the diode is ON). The LED's stay on after an error until reset by the software.

D5	D4	D3	Error
0	0	0	No errors
0	1	0	Page fault
0	1	1	Illegal access
1	0	0	TLB loading error
1	0	1	TLB loading error after segment clear
1	1	0	Page table fault
1	1	1	Segment not mapped

Refer to the Cromemco XMM Technical Reference Manual for a discussion of these errors.

Appendix B
XMM PARTS LIST

**Integrated
 Circuits**

Designation	Cromemco Description	Part No.
IC1	74LS30	010-0059
IC2	74LS74	010-0055
IC3	74LS04	010-0066
IC4	74LS374	010-0133
IC5	Microcode V02R0	502-0083
IC5-6	Sekt 8 pin	017-0000
	Sekt 16 pin	017-0002
IC6	Microcode V02R2	502-0082
IC7	74LS10	010-0063
IC8	74F352	010-0354
IC9	74LS373	010-0102
IC10	74LS148	010-0189
IC11	Sekt 20 pin	017-0004
	Pal TLB Active	502-0084
IC12	74S373	010-0085
IC13-14	74S244	010-0342
IC15	74LS373	010-0102
IC16	74S244	010-0342
IC17-18	2147H-45	011-0103
	Sekt 18 pin	017-0003
IC19	74LS175	010-0042
IC20	Sekt 8 pin	017-0000
	Sekt 16 pin	017-0002
IC21-22	Microcode V02R1	502-0075
	Sekt 20 pin	017-0004
IC23	PLA Microcode	502-0085
	74LS00	010-0069
IC24	74S30	010-0356
IC25-26	74LS00	010-0069

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**Integrated
 Circuits** (Continued)

Designation	Cromemco Description	Part No.
IC27	74S08	010-0166
IC28	74S32	010-0090
IC29	Microcode V02R3	502-0076
IC30	Microcode V02R5	502-0077
IC31	Microcode V02R7	502-0078
IC32	Microcode V02R6	502-0079
IC29-32	Sekt 8 pin	017-0000
	Sekt 16 pin	017-0002
IC33	7407	010-0104
IC34	74LS125	010-0127
IC35	74LS32	010-0058
IC36	74LS00	010-0069
IC37	74LS373	010-0102
IC38	74LS240	010-0038
IC39	2147H-45	011-0103
	Sekt 18 pin	017-0003
IC40	74LS670	010-0260
IC41-43	2148H-55	011-0105
	Sekt 18 pin	017-0003
IC44	74LS245	010-0120
IC45	74LS273	010-0107
IC46	Microcode V02R8	502-0080
IC47	Microcode V02R4	502-0081
IC46-47	Sekt 8 pin	017-0000
	Sekt 16 pin	017-0002
IC48	AMZ8121/AM25LS2521	010-0328
IC49	74LS244	010-0100
IC50	2148H-55	011-0105
	Sekt 18 pin	017-0003
IC51-54	2168/8168/IMS1420	011-0104
	Sekt 20 pin	017-0004
IC55	2148H-55	011-0105
IC56-57	2147H-45	011-0103
IC55-57	Sekt 18 pin	017-0003
IC58	74LS374	010-0133
IC59	74LS04	010-0066
IC60	74LS373	010-0102
IC61	74LS244	010-0100
IC62	74LS373	010-0102
IC63	74LS244	010-0100
IC64	74LS373	010-0102
IC65-66	74LS646	010-0355
IC67	74LS244	010-0100
IC68-71	74LS373	010-0102
IC101	SG3524	010-0326

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**Diodes/
 Transistors**

Designation	Cromemco Description	Part No.
D1	LED Yellow	008-0076
D2	LED Green	008-0020
D3-5	LED Red	008-0019
D101	1N752A	008-0056
D102	1N5231B 5.1V	008-0006
D103	UES1002 100V	008-0071
D104	IR10TQ040	008-0072
D105	1N5231B 5.1V	008-0006
Q101	SCR S2600	009-0048
	Mounting Pad	021-0186
Q102	2N3906	009-0002
Q103	2N3904	009-0001
Q104	2N3906	009-0002
Q105	D45VH10	009-0035
Q106	D44VH10	009-0047
Q104-106	3-Regulator silpad	021-0185

Capacitors

Designation	Cromemco Description	Part No.
C1-3	47 pf mono 100V	004-0000
C101-103	470 uf vari 6.3V	004-0091
C104	.01 uf tgs 100V	004-0037
C105	.1 uf tant 10V	004-0030
C106	220 pf crdc 1000V	004-0013
C107	.022 uf crdc 50V	004-0036
C108	1 uf mono 25V	004-0070
C109	.001 uf crdc 1000V	004-0022
C110-111	3 uf 50V	004-0130
C113	220 pf crdc 1000V	004-0013
C114	100 pf crdc 1000V	004-0008
C115	.1 uf tant 10V	004-0030
-o-	.047 uf tant 50V	004-0061

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**Capacitor
 Networks**

Designation	Cromemco Description	Part No.
CN1-3	47 pf 8 pin	005-0000

Resistors

Designation	Cromemco Description	Part No.
R1	4.7 kohm 1/4	001-0024
R2	100 ohm 1/4	001-0007
R3	270 ohm 1/4	001-0011
R4	4.7 kohm 1/4	001-0024
R5	2.4 kohm 1/4	001-0022
R101	820 ohm 1/4	001-0017
R114	3.3 kohm 1/4	001-0041
R115	16.9 kohm 1/4 1%	001-0158
R118	3.9 ohm 1/2	001-0192
R119	.05 ohm 3W	001-0232
R120	20 ohm 3W	001-0046

**Resistor
 Networks**

Designation	Cromemco Description	Part No.
RN1-2	4.7 kohm 9R 10P	003-0014
RN3-6	47 ohm 4R 8P	003-0047
RN7	470 ohm 7R 8P	003-0012
RN8	47 ohm 4R 8P	003-0047
RN9	4.7 kohm 9R 10P	003-0014
RN10-11	270 ohm 4R 8P	003-0003
RN12	4.7 kohm 9R 10P	003-0014
RN13	47 ohm 5R 10P	003-0078
RN14-17	270 ohm 4R 8P	003-0003
RN18	100 ohm 7R 8P	003-0036
RN19	4.7 kohm 9R 10P	003-0014
RN101	Power supply 10P	003-0077
RN102	Power supply 7P	003-0076

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Inductors

Designation	Cromemco Description	Part No.
L101	22 uH	007-0000
L102	30 uH	007-0025
L103	35 uH	007-0024

Miscellaneous

Designation	Cromemco Description	Part No.
	4-40x1/4 slot screw	015-0076
	4-40x3/16/7/16 standoff	015-0083
	4-40x5/16 phil screw	015-0182
	6-32x3/8 nylon screw	015-0183
	Heatsink	016-0290
	Nutplate	016-0300
	Sekt 34 pin connector	017-0091
Jumper A	Sekt 20 pin	017-0004
Jumper A	Shunt 20 pin	017-0362
F101	Fuse 6A axial	018-0038
	XMM PC Board	020-0108

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2. the return authorization number
3. a description of the problem, and
4. proof of the date of retail purchase

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