Cromemco®

WDI-II

Instruction Manual

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Chapter 1

GENERAL INFORMATION

INTRODUCTION

This manual contains information needed to install, select options, program, control, and understand the operation of the Cromemco WDI-II Winchester Disk Interface printed circuit board. This board will be referred to as the WDI-II throughout this manual. Cromemco instruction manuals and other related information will be referred to as required.

This chapter includes the WDI-II specifications, a board description, a list of documentation referenced in this manual, and a list of WDI-II/software compatibility, including diagnostic programs recommended by Cromemco.

Chapter 2, Getting Started, describes the WDI-II user selected options. For situations where a WDI-II is installed in an existing system, WDI-II installation information is also included.

Chapter 3, I/O Characteristics, covers the board interface characteristics of the system S-100 Bus and the hard disk drives.

Chapter 4, Programming and Program Control, describes programming the WDI-II microcircuits, registers, and counters, as well as program control considerations for these circuits. This manual is not intended as a complete reference guide to programming and controlling these circuits. More information may be found in the manufacturer's data book, referred to in this book as necessary.

Chapter 5, Principles of Operation, covers circuit operation in terms of the major operating capabilities of the WDI-II board and the individual circuits.

Chapter 6, Replacement Parts, provides information needed to order replacement parts for the WDI-II, including a complete parts list.

SPECIFICATIONS

The specifications for the WDI-II are contained in Table 1-1.

Table 1-1: SPECIFICATIONS

Modes and Functions:	Hard Disk Data Transfer Memory-to-Memory Data Transfer Extended Addressing
Disk Drive Compatibility:	Cromemco Hard Disk Drives H5, HD11 and HD22
Disk Drive Capacity:	6 Maximum
Bus:	S-100
Power Requirements:	+8 VOLTS @ 1.4 Amps -18 VOLTS @ 0.1 Amps
Operating Environment:	0 to 55°C

DESCRIPTION

The WDI-II provides an interface between the system S-100 Bus and a hard disk drive. The WDI-II circuits, together with the operating system, format and control data transfer between the system main memory and the disk surface media. High speed memory-to-memory data transfers may be made between addressed locations in system main memory. The extended address function allows extended addressing using address-as-data information received from the S-100 Bus.

The WDI-II is installed in one of the S-100 Bus connectors. The disk drive(s) connect to the WDI-II through one or more flat ribbon cables. Memory-to-memory data transfer and extended address functions require only that the WDI-II be inserted into an S-100 Bus connector. Refer to Chapter 2 for additional installation information.

USER SELECTED OPTIONS

There are two types of user selected options available for the WDI-II. Interboard functions may be selected using interconnecting cables, and intraboard functions may be selected using onboard jumpers. Refer to Chapter 2 for information explaining option selection methods.

The interboard options set up priorities between boards for system bus requests and system interrupts. WDI-II bus requests are generated by the Address Generator (DMA). WDI-II interrupts are generated by the Address Generator, CTC (Counter/Timer Circuit), and the PIO (Parallel Input/Output) controller circuits.

The intraboard (WDI-II onboard) options are 1) system bus request priority selection similar to interboard bus request priority selection, 2) base address selection in the Address Decoder circuit, and 3) CPU selection in the ϕ2 Clock Input circuit.

SYSTEM COMPATIBILITY

Hardware

The WDI-II is designed for S-100 Bus systems. All Cromemco systems are hardware compatible with the WDI-II. Only the HDD-22, HDD-11, and HD5 Hard Disk Drives are compatible with the WDI-II.

Software

Cromemco recommends that the WDI-II be used only with operating systems and programs capable of driving the WDI-II directly. The WDI-II will operate directly with the following operating systems and programs.

1. Cromemco Cromix Multi-user Multi-tasking Operating System--Version 11.07 and above. For more information refer to the Cromix manual.

2. Cromemco CDOS Single User Operating System--Version 02.44 and above. For more information refer to the CDOS manual.

3. Cromemco INIT Disk Initialization Program--Version 02.23 and above. This program allows the user to initialize the diskette. For more information refer to the CDOS manual.

4. Cromemco HDTEST Hard Disk Testing Program-Version 00.10 and above. This program exercises the hard disk drive and displays any detected errors on the console terminal. Refer to the Cromemco System Diagnostic Software manual.

5. Cromemco HDIAG Hard Disk Diagnostic Program-Version 00.13 and above. This program is used for executing special hard disk drive operations such as reading or writing data, declaring alternate tracks, saving data from bad tracks, verifying that all data can be read, and initializing all or part of the hard disk. Refer to the Cromemco System Diagnostic Software manual.

REFERENCE MATERIAL

Table 1-2 provides a list of the instruction manuals and other written information to which reference is made in this manual.

Table 1-2: LIST OF REFERENCE MATERIAL

LIST OF REFERENCE MATERIAL	
1.	Cromemco Cromix Multi-User Multi-tasting Operating System Instruction Manual--Part Number 023-4022.
2.	Cromemco CDOS Single User Operating System Instruction Manual--Part Number 023-0036.
3.	Cromemco System Diagnostic Software Instruction Manual--Part Number 023-6013.
4.	Cromemco Z-2H and HDD Hard Disk Systems Instruction Manual--Part Number 023-5020.
5.	Cromemco ZPU Central Processing Unit Instruction Manual--Part Number 023-0012.
6.	Zilog Microcomputer Components Data Book--March 1981.
7.	7710 Hard Disk User's Manual (HDD11 and 22)--Part Number 023-6027.
8.	HD5 Product Description Manual for 5" Hard Disk Drive--Part Number 023-6028.

Chapter 2

GETTING STARTED

INTRODUCTION

This chapter provides information about system installation and user selected options for the WDI-II. System installation explains how the WDI-II, if received separately from the system in which it is to be used, is installed in the system and connected to the disk drive. Both interboard and intraboard (onboard) user selected options are available.

The operating system, through the WDI-II, can control one of up to six hard disk drives in a system. Refer to the Cromemco Cromix or CDOS Operating System manuals for hard disk drive addressing information.

SYSTEM INSTALLATION

The WDI-II may be a part of a Cromemco System Zero, One, Two, or Three. In any of these systems, the WDI-II board should be installed firmly in one of the S-100 Bus circuit board connectors.

The WDI-II, with accompanying cables and hard disk drive, may be received either as a part of a complete system or separately, to be installed in an existing system.

The hard disk drive may be installed either within the system cabinet or externally. If the hard disk drive is installed within the system cabinet, one cable (Cromemco Part Number 519-0033) is required to connect the WDI-II to the hard disk drive. If the hard disk drive is installed outside the cabinet, a cable with two rear panel connectors (Cromemco Part Number 519-0037) is installed within the cabinet. External cables (Cromemco Part Number 519-0036) then serve to connect the hard disk drive(s) to these system cabinet rear panel connectors. Refer to the Cromemco Z-2H and HDD manual for more information.

NOTE: The WDI-II will not function properly if the ZPU clock switch is set for 2 MHz operation. Refer to the Z-2H and HDD manual for more information.

USER SELECTABLE OPTIONS

The interboard options are selected using interconnecting cables. The intraboard or onboard options are selected using jumpers. Explanations and instructions for the selection of each option are included in the following paragraphs. Figure 2-1 shows where each cable connector or circuit board solder pad is located on the WDI-II board.

CPU Selection

The WDI-II, as received from the factory, is ready for use in a system using a DPU central processor. The CPU selection circuit traces can be cut and new jumpers installed for other CPUs. The jumper locations for each CPU are shown in Figure 2-2.

Interboard Interrupt Priority Selection

Figure 2-3 illustrates how interboard interrupt priorities are selected. Figure 2-4 shows a closeup of connector J1. A Priority Interrupt Cable (Cromemco Part Number *519-0029*) may be used to establish interrupt priorities between circuit boards. These cables interconnect all of the boards that are part of the interrupt priority chain. Note that the Interrupt (INT*) signals from each board form a wired-or output to the system CPU. This signal tells the CPU that one of the boards has issued an interrupt request.

The circuit board with the highest interrupt priority has no connection at the Interrupt Enable Input (IEI). An onboard pull-up resistor to the +5 volt supply places a high on the input to the circuit generating the interrupt. A high on any of the circuit board Interrupt

Enable Outputs (IEO) indicates that an interrupt was issued either by the board with the high output or another board with a higher interrupt priority. A low on IEO indicates that the higher priority boards did not issue an interrupt request or that the interrupt has already been serviced.

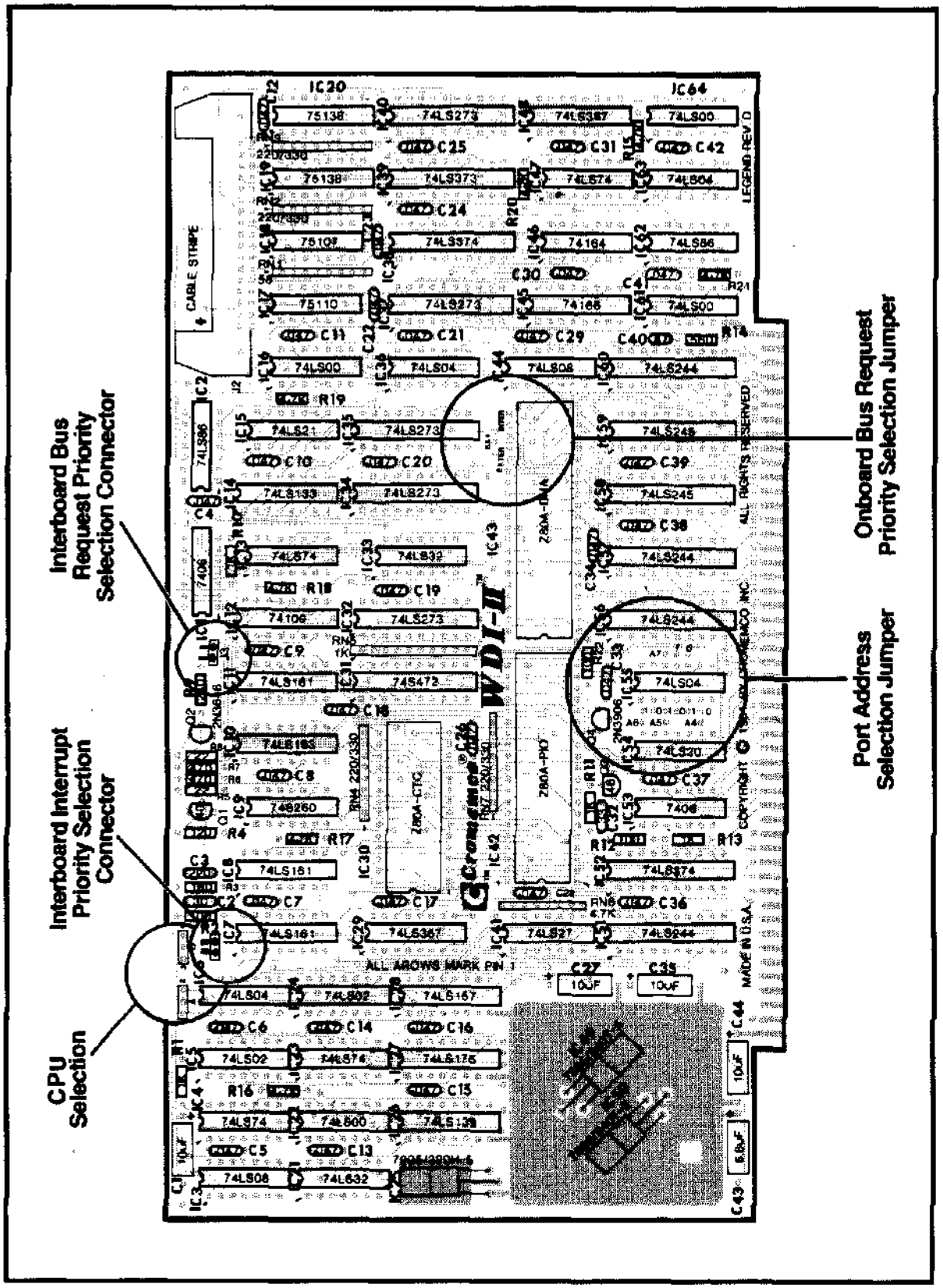


Figure 2-1: OPTION CABLE CONNECTOR AND JUMPER PAD LOCATIONS

NOTE: Cromemco software does not require the use of this option on the WDI-II.

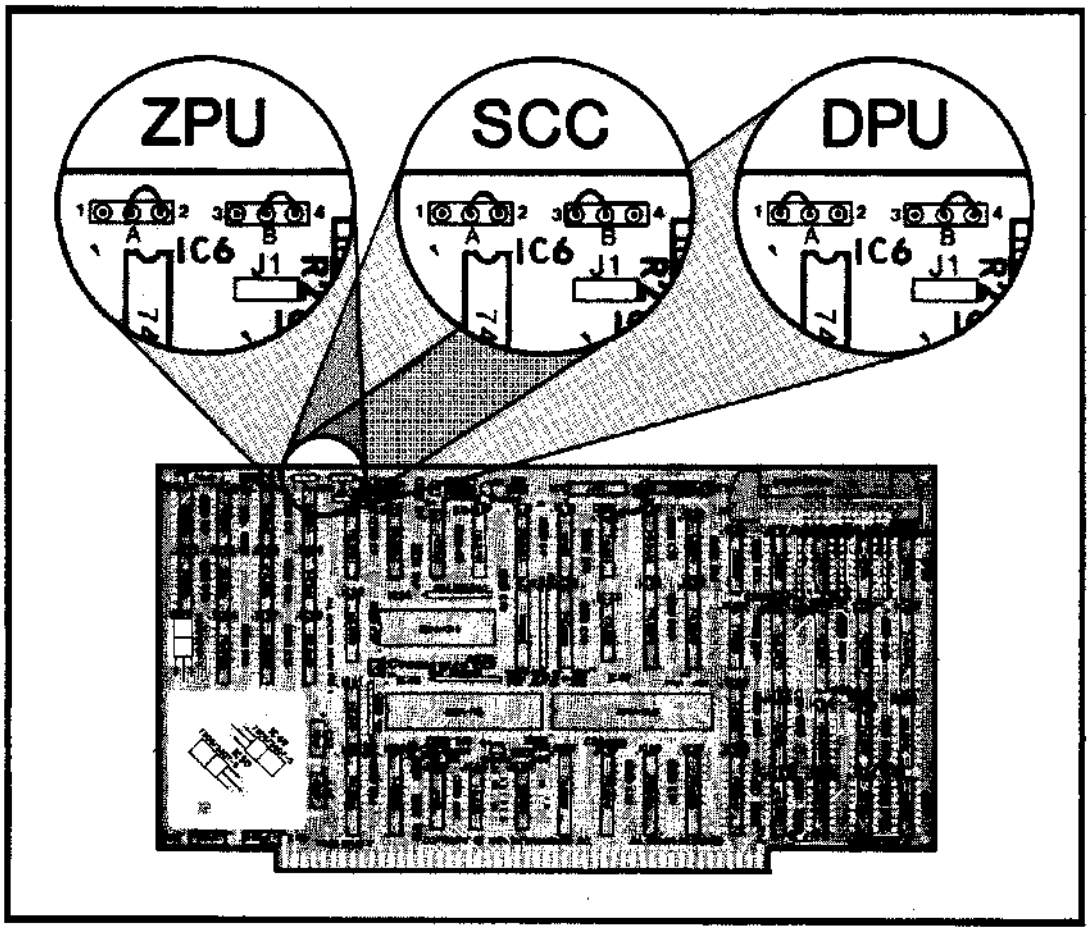


Figure 2-2: CPU SELECTION

Interboard Bus Request Priority Selection

All boards with a DMA controller have the ability to control the address and data buses and may be connected in a daisy chain arrangement, as illustrated in Figure 2-5. A closeup view of the WDI-II connector is shown in Figure 2-6.

The highest priority board's bus acknowledge input (BAI*) is connected directly to the system CPU hold acknowledge (pHLDA) output. A high on pHLDA indicates that the system bus is released for DMA control. A low on bus acknowledge output (BAO*) indicates that a higher priority DMA has not issued a bus request or that the DMA has issued a bus request but has already been

serviced. At this time, the board with a high on the bus acknowledge input (BAI*) has priority and is currently being serviced. A high on BAO* indicates that the bus has not been released by the system CPU or that a higher priority DMA has requested the bus and, as of this time, has not been serviced. See also **Onboard Bus Request Priority Selection** as follows.

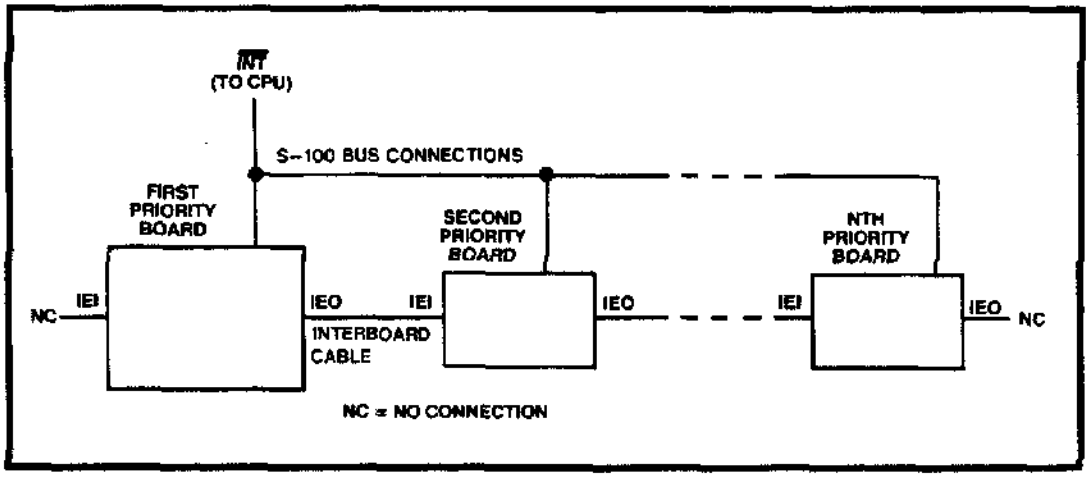


Figure 2-3: INTERBOARD INTERRUPT PRIORITY SELECTION

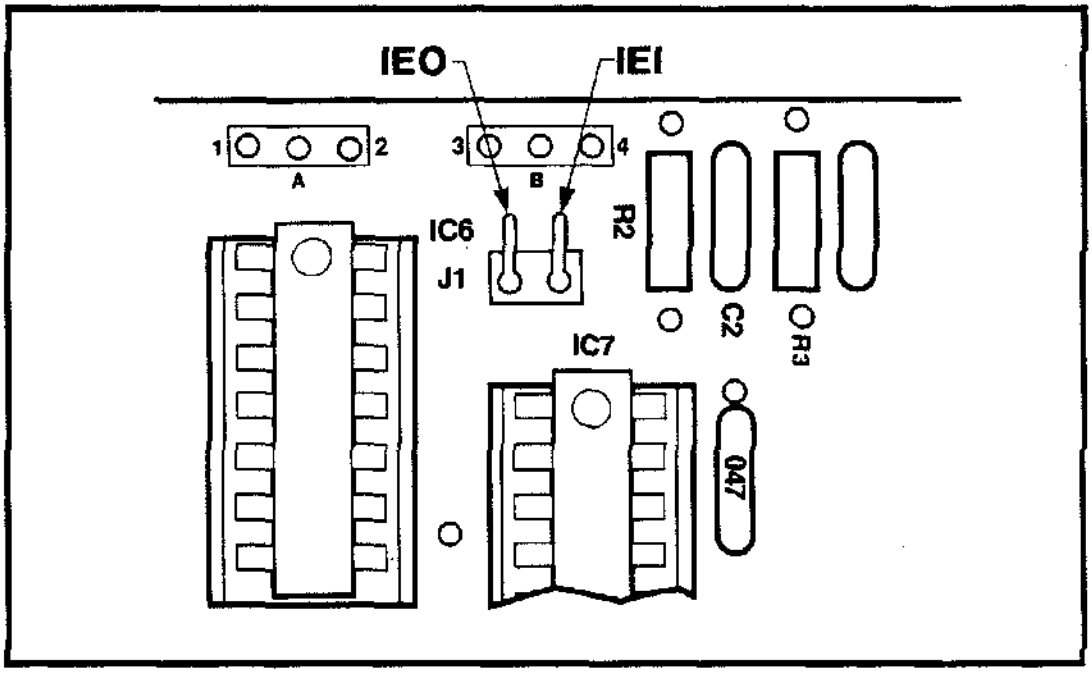


Figure 2-4: INTERBOARD INTERRUPT PRIORITY SELECT CONNECTOR J1

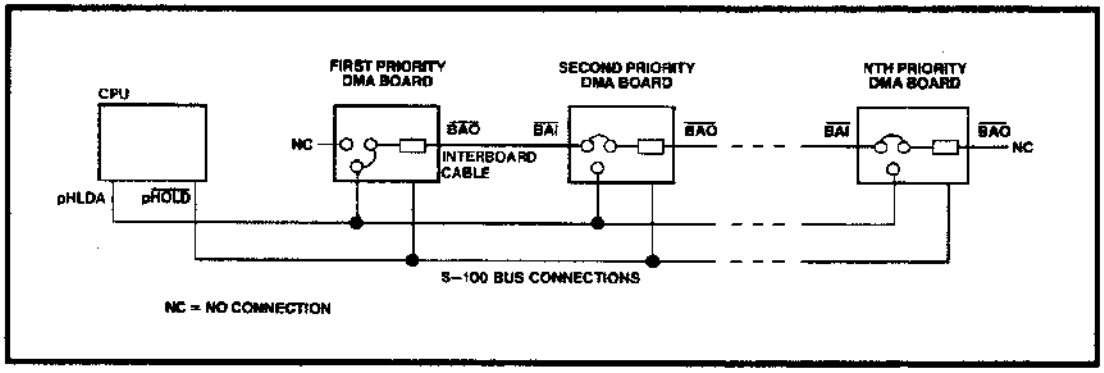


Figure 2-5: INTERBOARD BUS REQUEST PRIORITY SELECTION

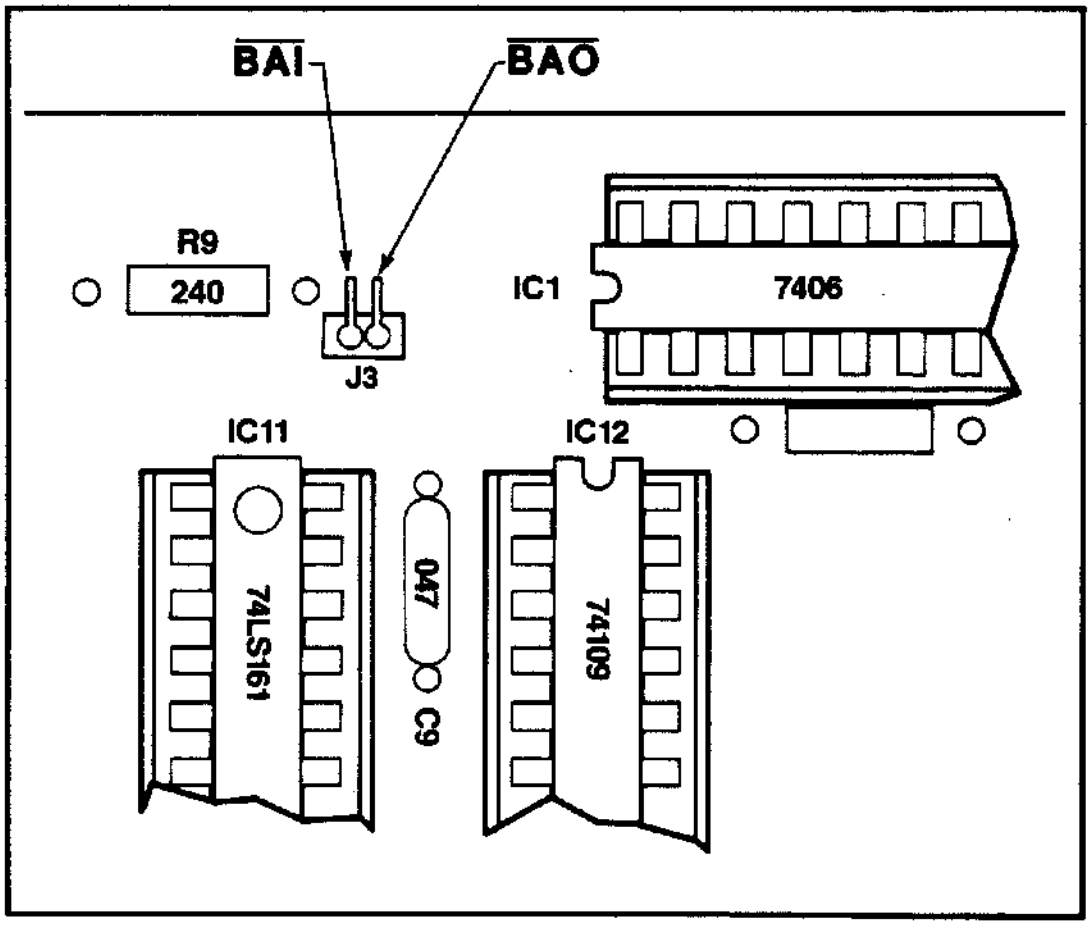


Figure 2-6: INTERBOARD BUS REQUEST PRIORITY SELECT CONNECTOR

Onboard Bus Request Priority Selection

On the WDI-II, the bus request priority jumper indirectly connects the pHLDA signal to the BAI* input of the Address Generator (DMA). If the WDI-II has the highest interboard bus request priority, the jumper is connected from BAI* to internal (INTER). The printed circuit traces are shipped this way from the factory. If the WDI-II does not have the highest interboard interrupt priority, the trace must be cut and a jumper inserted between BAI* and external (EXTER). Refer to Figure 2-7. See also, **Interboard Bus Request Priority Selection** and Figure 2-5.

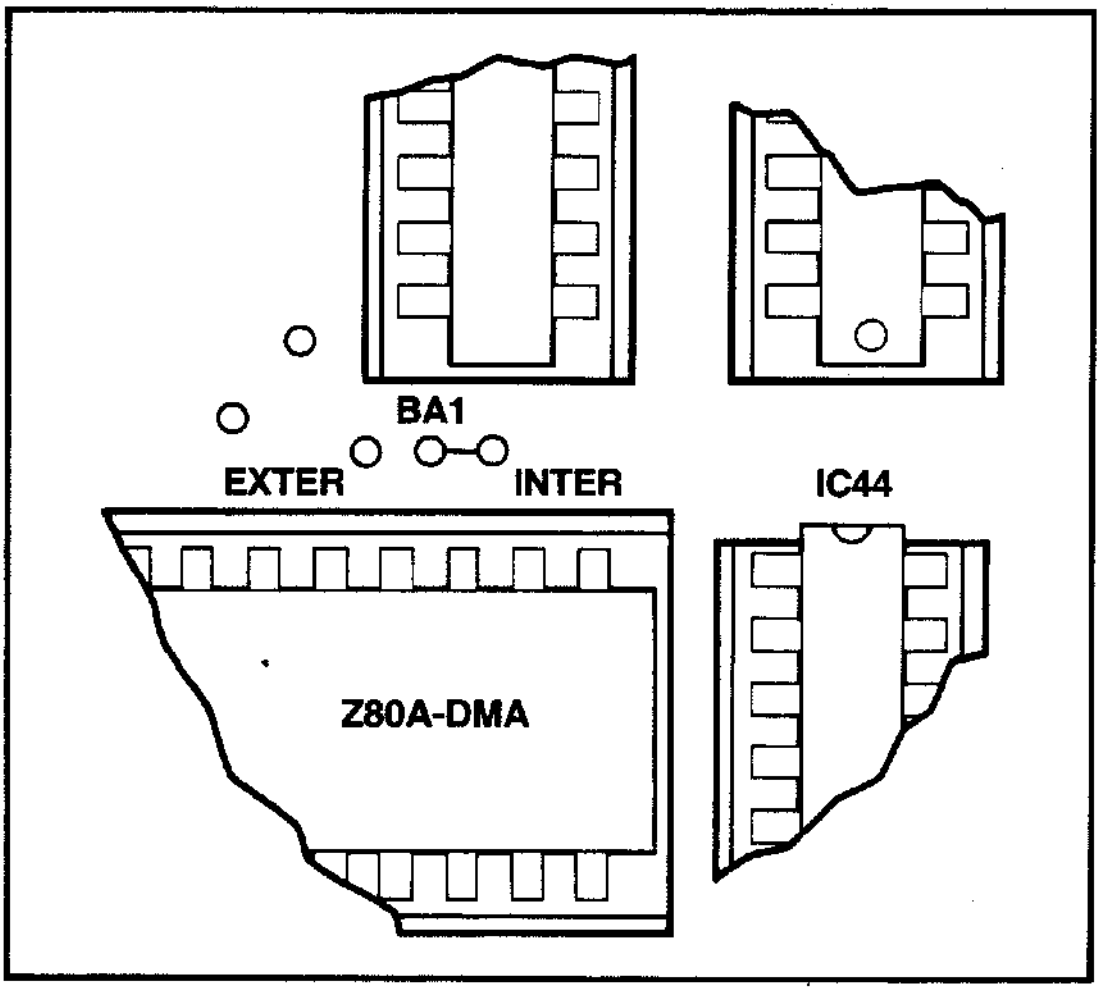


Figure 2-7: BUS REQUEST PRIORITY SELECTION JUMPER

Port Address Selection

The WDI-II board is shipped from the factory with E set as the base address. Figure 2-8 shows the original jumper locations. If the base address is to be changed, one or more of the traces must be cut. Jumpers must be inserted as indicated by Table 2-1. A **1** shows that a jumper should be inserted, and a **0** indicates that the jumper is omitted.

Table 2-1: BASE ADDRESS SELECTION

Base Address	Binary Equivalent			
	A7	A6	A5	A4
0Xh	0	0	0	0
1Xh	0	0	0	1
2Xh	0	0	1	0
3Xh	0	0	1	1
4Xh	0	1	0	0
5Xh	0	1	0	1
6Xh	0	1	1	0
7Xh	0	1	1	1
8Xh	1	0	0	0
9Xh	1	0	0	1
AXh	1	0	1	0
BXh	1	0	1	1
CXh	1	1	0	0
DXh	1	1	0	1
EXh	1	1	1	0
FXh	1	1	1	1

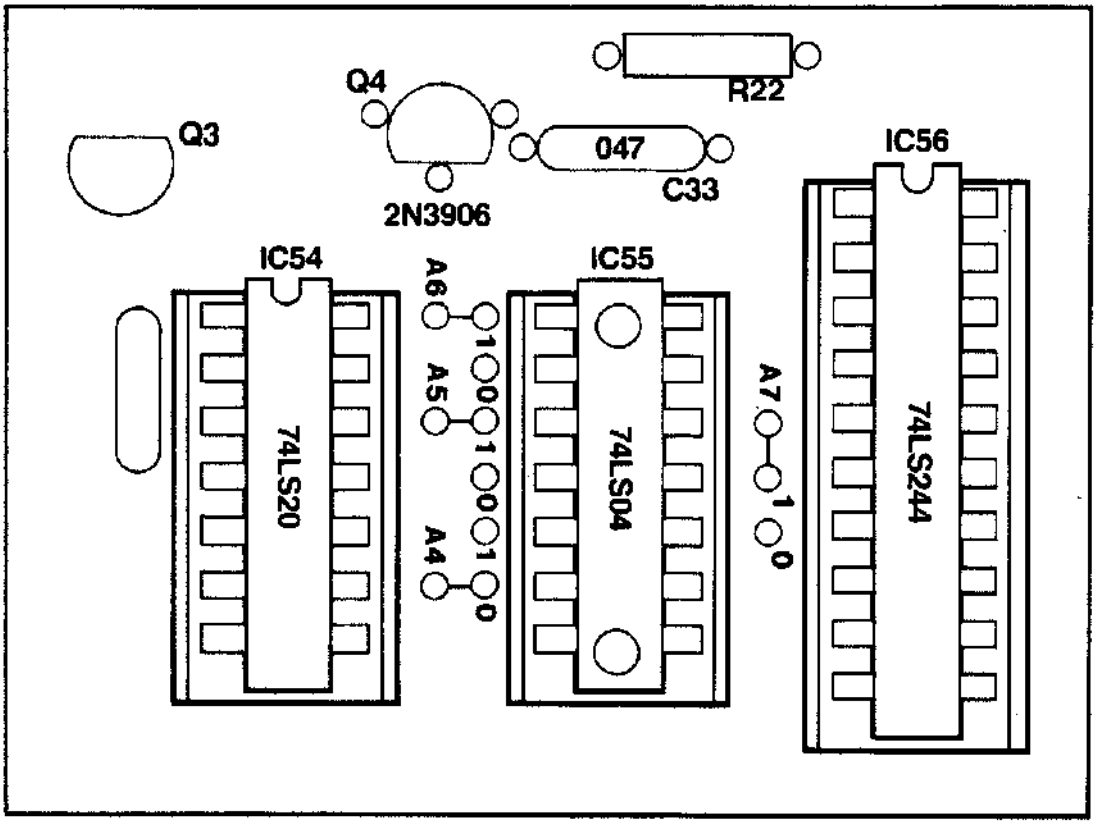


Figure 2-8: PORT ADDRESS SELECTION JUMPERS

Chapter 3

I/O INTERFACE CHARACTERISTICS

INTRODUCTION

The WDI-II and the system are connected with the standard 100-pin printed circuit board connector. The WDI-II appears to the operating system as a 16-port I/O peripheral. Refer to the Cromemco ZPU manual for more information pertaining to the S-100 Bus. Refer also to the CDOS or Cromix Operating Systems manuals for information pertaining to I/O drivers and addressing.

I/O ADDRESSING

As received from the factory, the addresses of the 16 I/O ports of the WDI-II are E0h through EFh. While the base address **E** can be changed, it is recommended that the number remain **E** unless a situation arises requiring the change. This assures compatibility with Cromemco software. Table 3-1 lists the I/O addresses of the WDI-II. The following paragraphs provide more detailed information on addressing. For information on programming and program control of the WDI-II microcircuits and board functions, refer to **Programming and Program Control** in Chapter 4.

Address E0h

This address enables the Extended Address Latch. This allows addresses in the form of data from the S-100 Bus to be latched onto the extended address lines A16-A23.

Address E1h

This address enables the Command/Status Bus registers. These lines carry command and status information for selecting, controlling and verifying proper operation of one of several hard disk drives. These signals are used throughout the Disk Data Transfer mode.

Addresses E2h and E3h

These addresses are not used at this time.

Addresses E4h through E7h

These addresses select one-of-four PIO (Parallel Input/Output) Controller modes. In the command modes, the internal registers interface the operating system to WDI-II circuits as required in the Disk Data Transfer mode. In the data (operational) modes, the internal registers interface with the WDI-II circuits.

Address E8h

This address selects the DMA controller microcircuit. The DMA mode is software selected and determines the WDI-II interface mode. Once the DMA mode is selected, the controller microcircuit enters the operational phase. In the Disk Data Transfer mode, the DMA takes control of the S-100 Bus. The DMA, in turn, is controlled by other WDI-II circuits. In the Memory-to-Memory Transfer mode, as soon as the CPU allows, the DMA takes control of the S-100 Bus and begins operation.

Addresses E9h through EBh

These addresses may also be used to select the DMA microcircuit. It is, however, recommended that E8h be used exclusively for DMA control to maintain compatibility with current Cromemco software. Addresses E9h through EBh are reserved for future WDI-II operating mode expansion.

Addresses ECh through EEh

These addresses select one-of-three CTC (Counter/Timer Circuit) channels. CTC operation is related to disk drive control and to finding data and reading and writing it to exact disk locations.

Address EFh

This address may be used to select CTC channel 3. Note, however, that channel 3 is not used in any of the WDI-II operating modes at this time.

Table 3-1: WDI-II I/O PORT ASSIGNMENTS

Address (Hexadecimal)	Control Signals[1]	Use
E0	$\overline{\text{PIO0 SEL}}$,A0,A1[2]	Selects Extended address Latch
E1	$\overline{\text{PIO0 SEL}}$,A0,A1[2]	Selects Command/Status Bus
E2,E3		Not Used
E4-E7	$\overline{\text{PIO1 SEL}}$	Selects Parallel Input/Output Controller microcircuit
E8	$\overline{\text{DMA SEL}}$	Selects Direct Memory Access microcircuit
E9-EB	$\overline{\text{DMA SEL}}$	Same as E8[3]
EC-EF	$\overline{\text{CTC SEL}}$	Selects Counter Timer Circuit[4]

Notes:

1. Refer to Schematic.
2. Clocked by S-100 Bus $\overline{\text{RD}}$ signal.
3. Address use not recommended.
4. Selection of address EFh serves no useful purpose.

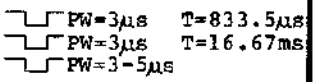
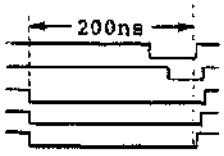
DISK DRIVE INTERFACE

A hard disk drive located within the system cabinet is connected directly to the WDI-II circuit board with a special interconnecting cable. Hard disk drives outside the system cabinet are connected to each other and to the WDI-II cable connectors on the cabinet rear panel using separate interconnecting cables. Refer to the Cromemco Z-2H and HDD manual for more information.

If the WDI-II circuit board, cables, and hard disk drives are received from the factory or dealer separately from the computer, they will have to be installed before they are usable. Refer to Chapter 2 for installation information.

Each connection between the WDI-II and the hard disk drive(s) has a specific purpose. Table 3-2 shows the connector pin number, the signal name, and indicates the active true state or pulse characteristics. Figure 3-1 is a simplified block diagram that shows the disk drive interface. The following paragraphs list each signal name and indicate the effect each has on hard disk drive operation.

Table 3-2: WDI-II/DISK DRIVE CONNECTIONS

Pin [1,2] Name	Signal on J2-Pin #	Signal Transition or Active State
Address, Selected Unit		
-3	5	low
-2	6	low
-1	9	low
-0	10	low
Data (Read/Write) Differential		
+	7	
-	8	
Servo Clock, Differential[4]		
+	11	
-	12	
Disk Position		
Sector	15	 PW=3µs T=833.5µs
Index	16	PW=3µs T=16.67ms
Seek Complete	17	PW=3-5µs
Fault	18	low
Command Strobe	19	 200ns
Command Acknowledge	25	
Command Read/Write	20	
Command Select 0	21	
Command Select 1	22	
Command/Stauts Bus[3]		
-6	27	low
-7	28	low
-4	29	low
-5	30	low
-2	31	low
-3	32	low
-0	33	low
-1	34	low

Notes:

1. J2-Pins 1, 2, 13 and 14 are grounds.
2. Unassigned lines, J2-pins 3, 4, 23, 24 and 26 are all grounded at J2.
3. Command/Status Bus Signals must remain low while command control signals CMD STB, CMD AK, CMD R/W, CMD SEL 1, and CMD SEL 2 are active.
4. SYS CLK is the 5.184 MHz disk drive clock signal. When the Command/Status Bus READ GATE is true, SYS CLK is synchronized to the data transitions. Otherwise, SYS CLK is locked to the servo surface INDEX pulse through the phase locked oscillator.

Address, Selected Unit

The bit pattern on SELECTED UNIT ADDRESS* indicates which disk drive has been selected to participate in a data exchange with the system main memory.

Clock, Differential Systems

The ± SYS CLOCK signal is generated within the disk drive from either synchronization data placed on the disk media servo surface at the factory or the data transitions recorded on the disk media. The first example synchronizes the data in the write-to-disk mode while the latter synchronizes the data being read from the disk. During operation, the WDI-II Formatter uses the clock signal to synchronize the transmission of data between the WDI-II and disk drive.

Command/Status Bus

This bus carries an 8-bit byte which passes command (control) or status information between the system and the disk drive unit. One-of-eight bytes is selected. For more information, refer to **Programming Control Through WDI-II Microcircuits, Registers and Counters** in Chapter 4.

Command/Status Bus Control Signals

These signals select and control the information that is transmitted on the Command/Status Bus.

Command acknowledge (CMD ACK*) indicates to the operating system (with a low) that a command has been received or that status information is on the Command/Status Bus.

Command Read/Write (CMD R*/W) selects the Command or Status mode (four-of-eight bytes).

Command Select 1 and 2, (CMD SEL 1 and CMD SEL 2), select one-of-four bytes in either the Command or Status mode.

Command Strobe (CMD STROBE*), with a momentary low, indicates that a command is being sent to the hard disk drives. The command may be used to control the drive unit's mechanical operation or to indicate that the unit should place status information on the Command/Status Bus.

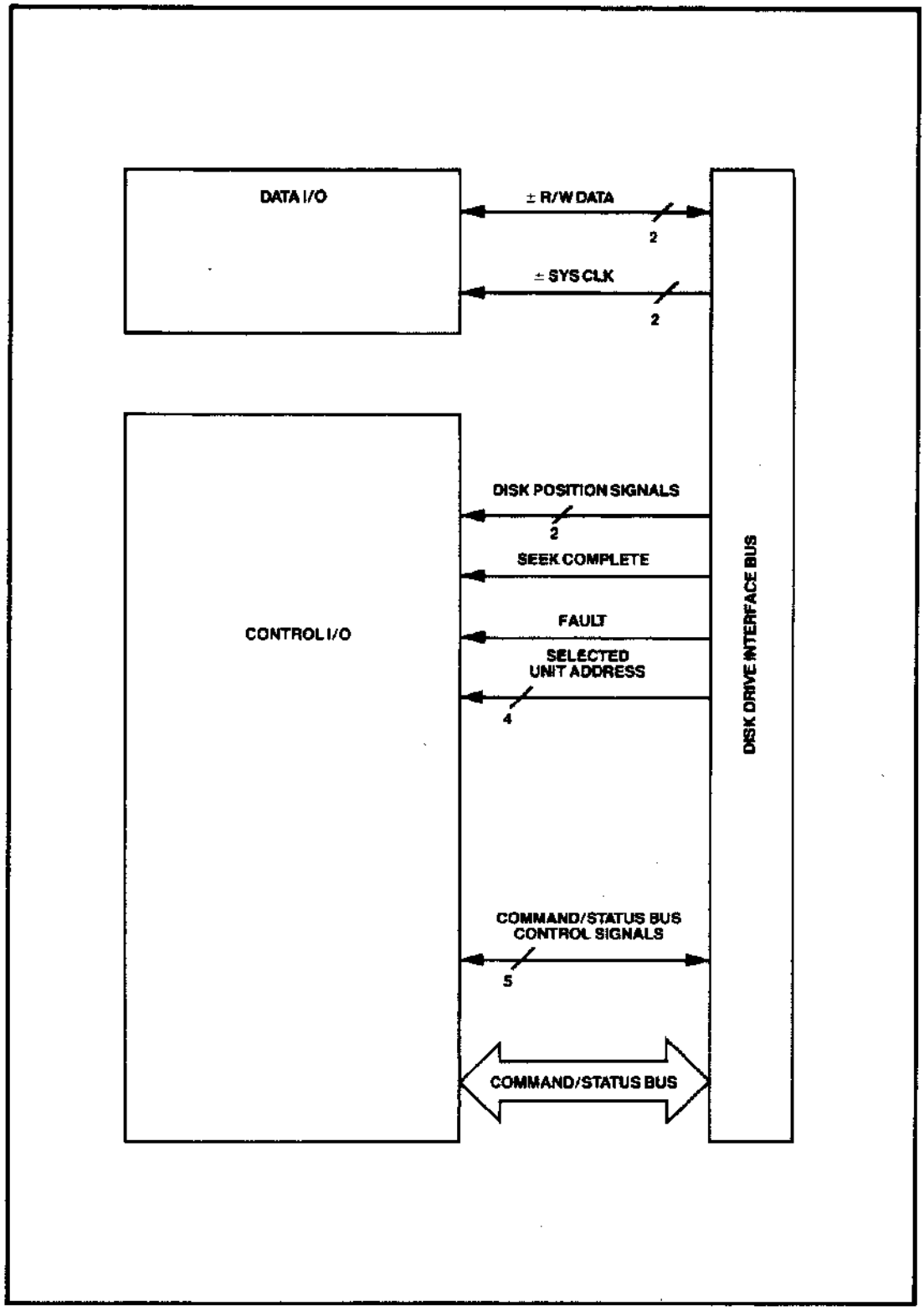


Figure 3-1: DISK DRIVE INTERFACE

Data, Differential Read/Write

A ±R/W DATA signal on these lines indicates that data is being transmitted to or received from the hard disk drive.

Disk Position Signals

The following pulses are written to the disk servo surface at the factory. In practice they are accessed in a read only mode.

INDEX* is a pulse generated once for each rotation of the disk. It is a reference that indicates the position of the disk at a given instant. It may be used to locate or place information on the disk media, or monitor the speed of the disk.

SECTOR* is a pulse generated once for each sector on the disk. It functions as a reference and may be used the same way as the Index pulse.

Seek Complete

Seek Complete* is generated when the read/write head has located the target track that it has been seeking.

Fault

Fault* goes low whenever a fault associated with control of the addressed hard disk drive unit occurs.

Chapter 4

PROGRAMMING AND PROGRAM CONTROL INFORMATION

INTRODUCTION

This section includes information to aid in programming and controlling the modes and functions of the WDI-II. Programming and program control information on overall board operation is included, followed by information on microcircuit programming and the onboard registers and counters. The final portion of this chapter concerns programming control through WDI-II microcircuits, registers and counters.

PROGRAMMING AND PROGRAM CONTROL

The WDI-II appears to the operating system as a 16-port addressable peripheral. Under program control, the different operating modes and functions of the WDI-II may be implemented as desired. Selecting the Disk Data Transfer Mode causes the WDI-II circuits to interface the system S-100 Bus and the selected hard disk drive. Selecting the Memory-to-Memory Data Transfer Mode causes the Address Generator (DMA) to control main memory data transfer at a rate up to 10 times faster than a conventional program controlled data transfer. The Extended Address Function allows addresses in the form of data, received from the S-100 Bus, to be placed on the extended address lines.

The onboard microcircuits must be programmed at the beginning of most WDI-II operations. The PIO (Parallel Input/Output) Controller falls into this category because it plays a major role in the two main WDI-II modes of operation. The DMA (Direct Memory Access) Controller also requires immediate programming because it determines the WDI-II mode of operation. The CTC (Counter/Timer Circuit) is involved in various timing and control functions occurring throughout the Disk Data Transfer mode, and thus must be reprogrammed at various times in order to accomplish all of its assigned tasks. During each WDI-II operation, the microcircuits are selected and placed into their operating modes, allowing them to perform their programmed function(s). For more information on the operation of the microcircuits with the other WDI-II circuits, refer to Chapter 5.

Disk Data Transfer Mode

A particular series of program controlled steps must occur to implement disk data transfer. It is possible to perform some of these out of the order shown. However, this sequence is recommended to prevent problems in implementing this mode of operation.

Microcircuit Programming--At the beginning of the Disk Data Transfer Mode, the PIO is programmed to provide the required hardware interface. Then the DMA is programmed for the search continuous mode and other related parameters required for the disk data transfer. For more information pertaining to PIO and DMA programming, refer to the section on microcircuit programming later in this chapter.

In the Disk Data Transfer Mode, the Formatter controls DMA operation. More information about this may be found in the sections entitled **Disk Data Transfer Synchronizer** and **Formatter** in Chapter 5.

Initial Program Control of the READ and WRITE Commands--Under program control, the READ (from disk) and *WRITE (to disk) commands on the Command/Status Bus* are initially held inactive until later.

Controlling the Disk Drive Operation--To implement the disk data transfer, the system must control the hard disk drive unit. Selecting the disk drive allows the operating parameters of that unit to be polled by the operating system through the Command/Status Bus Registers. The operating system then responds with the appropriate commands to bring the disk drive under control.

Choosing the Disk Location for the Data Transfer--The disk data transfer location where data is to be written to or read from the disk media must be chosen. The disk location is chosen in terms of disk surface, track and sector. The particular disk surface is selected in terms of the addressed read/write head; the data track is selected by the addressed cylinder. The operating system may verify the addresses by requesting a status check on each.

Determining Instantaneous Sector Position--Instantaneous sector position must be determined to enable WDI-II timing circuits to transfer data to or from the correct

sector. This is a dynamic transfer condition and must be done properly to avoid destroying data in the write-to-disk mode or reading incorrect data in the read-from-disk mode. Instantaneous sector position may be established by programming the CTC Channel 0 counter to one. The counter will decrement to zero upon receiving an INDEX* pulse from the disk drive unit, and the operating system can poll CTC Channel 0 to determine exactly when this occurs. Instantaneous sector position may also be determined or double checked by reading the header data currently under the read/write head. When a sector pulse is received, the header read mode is immediately implemented. The header contains data that indicates the selected disk surface, track and sector. For more information, refer to the **Header Read** paragraph in this chapter.

Using Instantaneous Sector Position to Determine when to Implement the Final Pre-Data Transfer Events--When the instantaneous disk location is determined, CTC Channel 1 is immediately programmed to one less than the difference between the sector currently under the read/write head and the sector where the data transfer will occur. *The counter decrements by one as each* sector pulse is received. When the zero count is reached, the zero count ZC1 is output. At this point, the head is above the sector just preceding the data transfer sector.

Implementation of Final Pre-Data Transfer Events--When the read/write head position is above the sector immediately preceding the data transfer sector, the final series of events leading to the actual data transfer must be implemented. These events are:

1. CTC Counter 1 is reprogrammed to count $\phi 2$ clock pulses for an 8us time period (12us for 5" disk drives).

2. By operating system control, place the READ or WRITE command on the Command/Status Bus. The command is latched into the Command/Status Bus register.

3. By operating system control, activate the PIO B0 port, DISK OP*. This enables the Formatter via the ± SYS CLK and the Control Signal Switching and Synchronization circuit. The READ or WRITE command is gated to the disk drive where it is called the READ or WRITE GATE enable signal.

4. Program DMA RDY/START through PIO B2 to the Disk Data Transfer Synchronizer, providing the "first byte" trigger. Operation from this point on is completely under the control of the WDI-II hardware circuits.

For more information about the continued operation of the WDI-II circuits in this mode, refer to **Principles of Circuit Operation** found in Chapter 5. The Disk Data Transfer Synchronizer circuit description provides information on the operation of the control circuits in conjunction with the Formatter and the Address Generator (DMA). Refer also to the Formatter Enable/Start circuit description which takes the 8 or 12us timing signal TO1 from the CTC and enables or starts the Formatter operation.

Write-to-Disk Mode--The data to be written to the disk must be placed in system main memory in sequential order as follows:

```
  1 Synchronization Byte
  4 Header Bytes
512 Data Bytes
```

Part of the DMA programming indicates the location of this data in memory and how much data is to be written to the disk. In this mode, 517 bytes is always transferred from system main memory to one sector on one track. Data transfer from main memory to the disk occurs one byte at a time controlled by the Formatter. Refer to Chapter 5 for more information.

The write-to-disk mode may be followed up by data transfer error checking. This is done by immediately entering the read-from-disk mode and comparing the recorded error check bytes against those calculated by the WDI-II circuits.

Read-from-Disk Mode--As far as the operating system is concerned, only the 4 header bytes, or the 4 header bytes and the 512 data bytes, are output to the system main memory. Once started, data transfer is a continuous flow from the disk to main memory.

The hardware performs an error check on the header and data information in this mode. The CRC (Cyclic Redundancy Check) error verification data bytes are inserted on the disk by the Formatter in the write-to-disk mode. They are then checked against the number calculated from the data read from the disk in

the read-from-disk mode. The error check signal is output to the system program through PIO B7 CRC ERROR. This signal is held until the next CRC check is made. *For more information on hardware operation in this mode,* refer to Chapter 5.

1. **Header Read**--In order to perform a header read only, the DMA circuit must be programmed to read only 4 data bytes. After reading the bytes, the error check is made to assure that the header data transfer was accurate.

   The header read may be used to determine the disk surface, the track, and the sector currently under *the carriage head. With the sector information,* the system program may enable CTC Counter 1 to count sector pulses until the disk position is reached which ensures correct disk data transfer. Refer to the paragraphs entitled **Disk Data Transfer Mode** for more information.

2. **Data Read**--In order to read the data from the disk, the DMA must be programmed to read 516 bytes, including the header and data bytes. Error checks assure that the complete transmission of data was accurate.

Memory-to-Memory Data Transfer Mode

In the Memory-to-Memory Data Transfer Mode, the DMA is programmed to the transfer mode, allowing transfer of data from one location to another in system main memory using the DMA as a temporary data storage location. This mode begins operating immediately after the DMA is programmed. The DMA outputs a bus request (BUSRQ*) signal to the system CPU. The CPU acknowledges the bus request with a bus acknowledge (BUSAK*) signal and turns control over to the DMA. Control is retained until the data transfer is completed. For more information on DMA programming in this mode, refer to the microcircuit programming information in this chapter.

Extended Address Function

The Extended Address Function requires no initial programming of WDI-II circuits. Refer to Chapters 3 and 5 for more information.

MICROCIRCUIT PROGRAMMING

The following paragraphs provide a brief overview of programming the WDI-II microcircuits. For a more detailed discussion, refer to the Zilog Microcomputer Components Data Book.

DMA (Direct Memory Access) Controller Programming

The DMA microcircuit contains seven groups of write registers programmed to control the various operating functions. Each group includes a base or control register and usually several subservient registers controlling individual DMA functions. The write registers are:

- WR0 Port A Base (1 byte), Starting Address (2 bytes), and data Block Length (2 bytes) Registers.
- WR1 Port A Base and Variable Timing Registers (1 byte each).
- WR2 Port B Base and Variable Timing Registers (1 byte each).
- WR3 Byte Match Base, Mask and Match Registers (1 byte each).
- WR4 Port B Base (1 byte), Starting Address (2 bytes), and the Interrupt, Pulse, and Interrupt Vector Registers (1 byte each).
- WR5 DMA Control (1 byte).
- WR6 DMA Control and DMA Read Mask (status control) Registers (1 byte each).

The read registers output the status of the DMA and the various internal registers controlled by the Read Mask Register. The read registers are:

RR0	DMA Status
RR1/RR2	Byte Counter Status
RR3/RR4	Port A Address Counter Status
RR5/RR6	Port B Address Counter Status

The write registers are programmed from left to right in sequence, as shown in Figure 4-1. The starting address counters may either count up, down, or they may be fixed. They are multiplexed to the WDI-II Address Bus in a sequence dependent on the operation being performed.

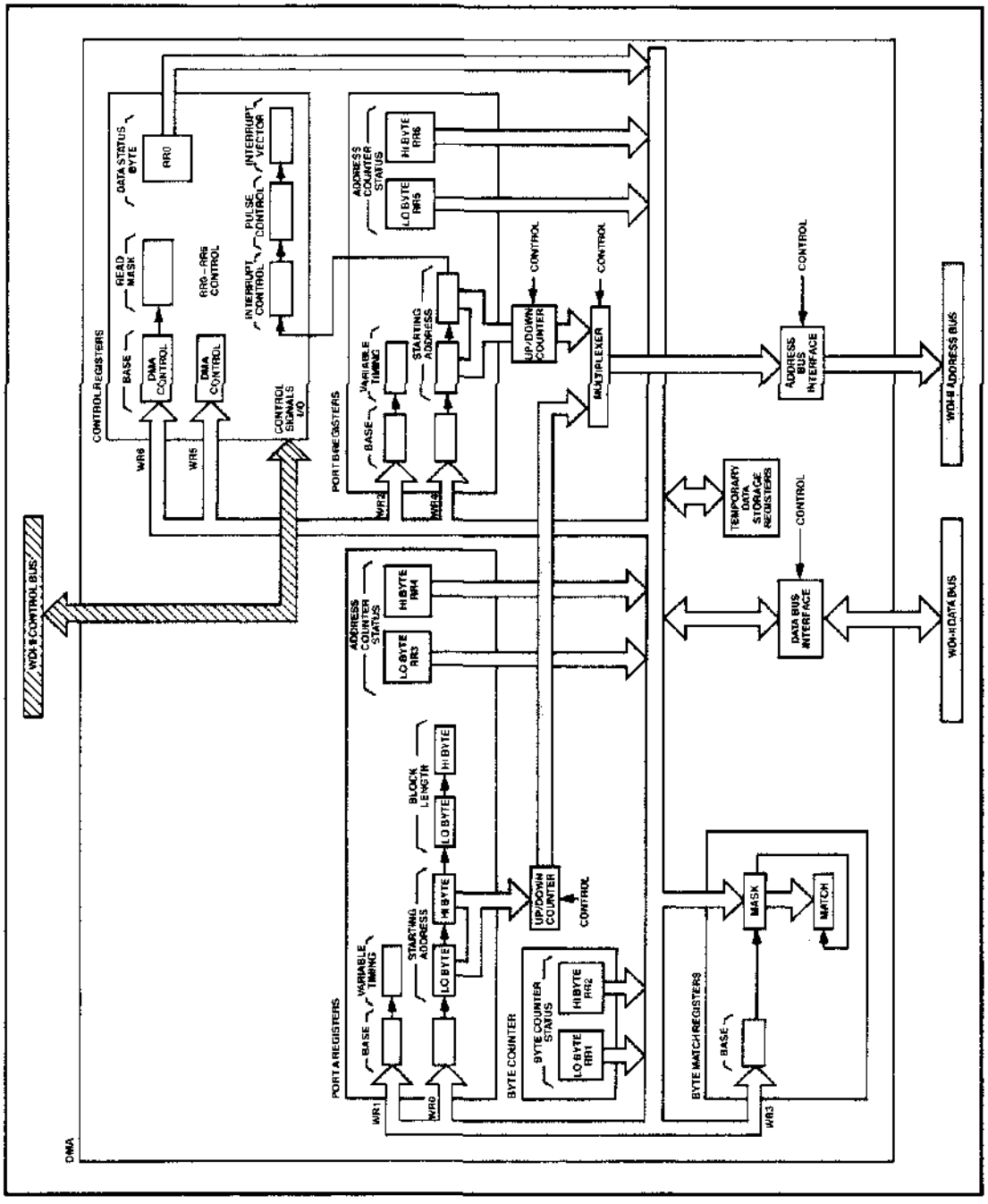


Figure 4-1: DMA SIMPLIFIED BLOCK DIAGRAM

The DMA has two programmable operations pertinent to WDI-II operation.

DMA Search--Enter the WDI-II Disk Data Transfer mode by selecting address E8h. Program the DMA as follows:

1. Select the data byte search mode.

2. Mask all bits of the Mask Byte so no search match can be made. (This makes the search continuous.)

3. Select the continuous data transfer mode. This allows hardware control of the DMA, assuring orderly data transfer during simultaneous operation with other WDI-II circuits.

4. Program the DMA with main memory address locations as follows:

    a. the beginning address.
    b. the block length of data to be transferred.

NOTE: This programming list for the DMA is by no means exhaustive. Refer to the Zilog Data Book for more information.

In operation, the following events occur:

1. The DMA asks for and receives control of the S-100 Bus from the system CPU.

2. The Formatter halts DMA operation until the first data byte is ready to be transferred. The DMA is then released.

3. The DMA outputs the beginning address and tries to match the first data byte. Hardware control circuits hold the address until the data transfer is completed.

4. The Formatter indicates to the DMA that the next byte is ready. Steps 1 through 4 are repeated until all the bytes are transferred.

5. The DMA relinquishes bus control to the CPU and the data transfer ends.

DMA Transfer--To enter the WDI-II Memory-to-Memory Data Transfer Mode, program the DMA in the following manner:

1. Select the data transfer operation.

2. Select the continuous data transfer mode.

3. Select the DMA ready input inhibit.

4. Program the DMA with main memory data byte address locations as follows:

    a. the beginning address.
    b. the number of data bytes to be transferred.

NOTE: This list of DMA programming steps is by no means exhaustive. Refer to the Zilog Data Book for more information.

In operation, the following events take place:

1. The DMA asks for and receives control of the S-100 Bus from the system CPU.

2. The DMA outputs the beginning source address. The data byte from main memory is temporarily stored in an internal DMA data register.

3. The DMA outputs the beginning destination address and the data byte is transferred to that main memory location.

4. Steps 2 and 3 are repeated for each subsequent data byte until all are transferred.

5. Data transfer ends and the DMA relinquishes S-100 Bus control to the CPU.

PIO (Parallel Input/Output) Controller Programming

The PIO is a programmable, dual port, parallel I/O device. The PIO input and output lines may be programmed to operate individually or as a group. Preselected logical combinations of line transitions may optionally generate interrupts. Once the PIO mode and I/O operation have been defined, the PIO interfaces the operating system to the hardware on the WDI-II board. Since the PIO is hardware committed to the WDI-II board, the data flow of each line must conform to that shown in Figure 4-2.

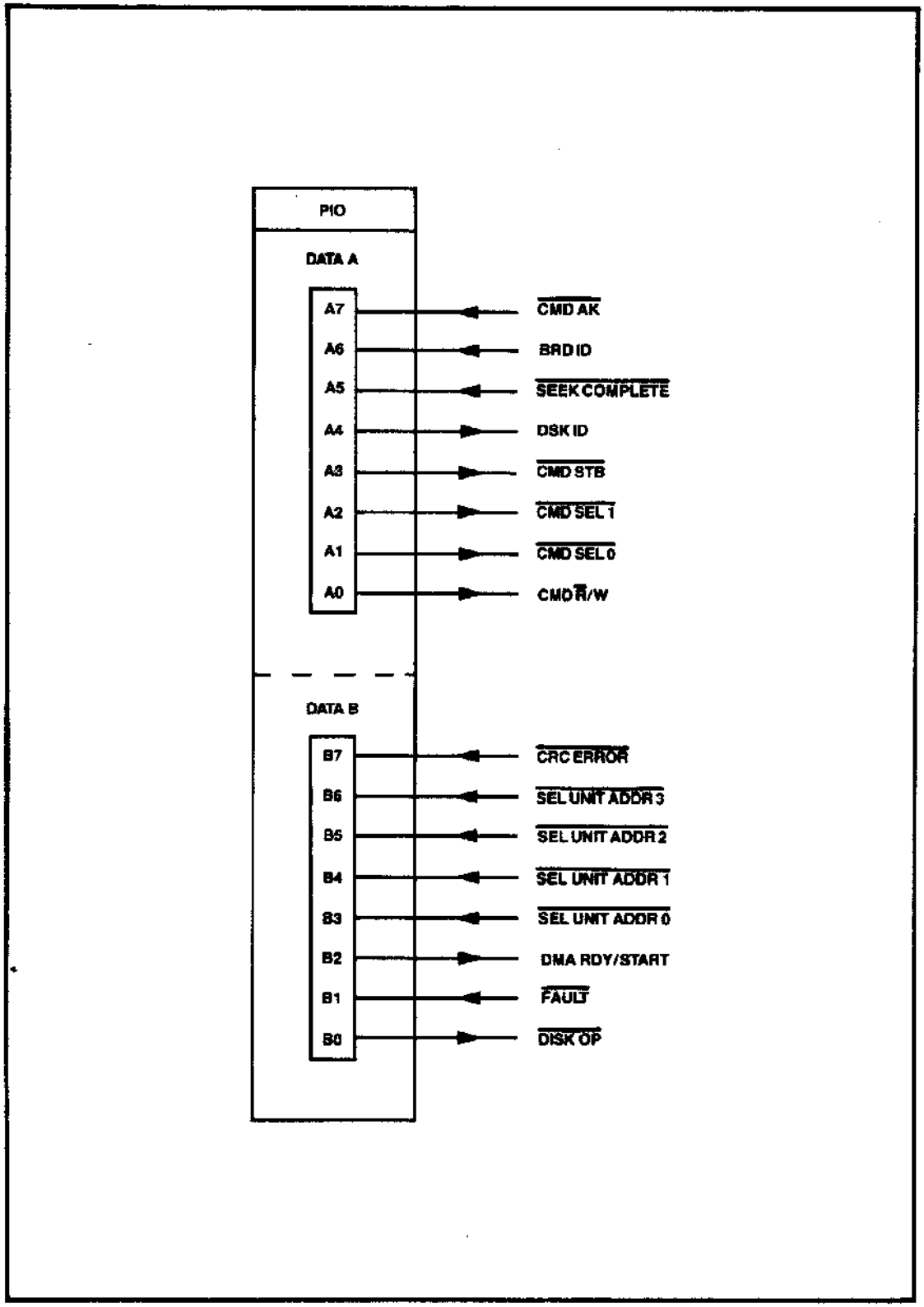


Figure 4-2: PIO I/O SIGNAL FLOW DEFINITION

In the case of the WDI-II circuits, PIO Ports A and B (selected by addresses E6h and E7h respectively) are programmed to the Bit Input/Output mode. Control bytes select the mode and the bit input and output definition. The format of these control bytes are shown in Figure 4-3.

Although the PIO Interrupts are not used in the present WDI-II configuration, the potential does exist. Refer to Figure 4-4 for a generalized sequence of programming steps.

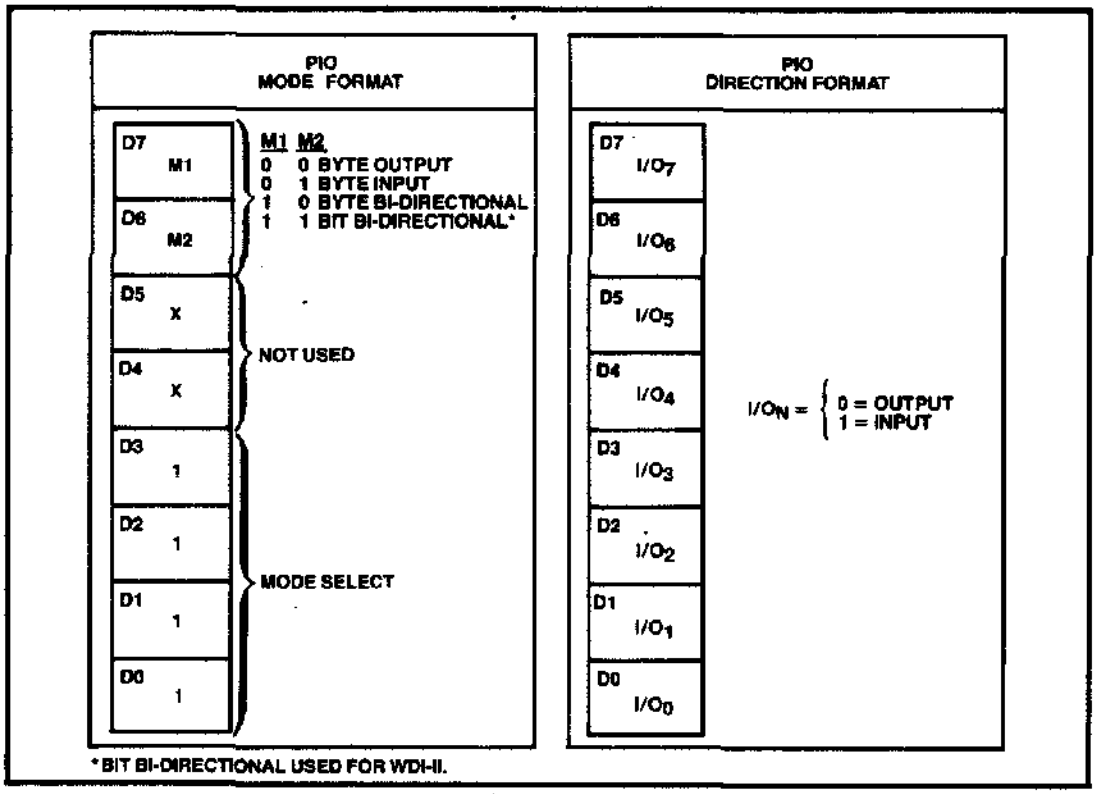


Figure 4-3: PROGRAMMED PIO CONTROL BYTE FORMAT

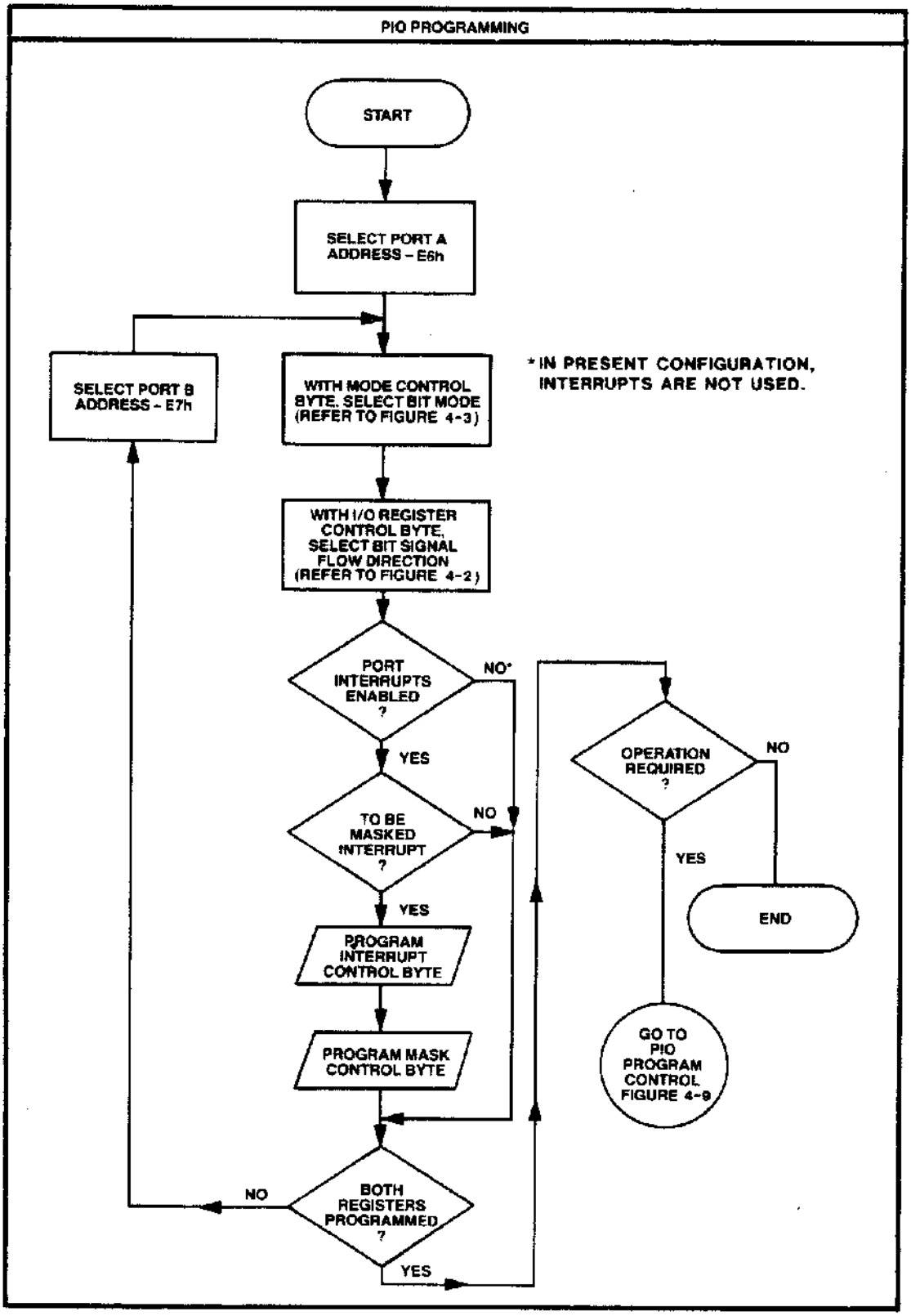


Figure 4-4: PIO PROGRAMMING SEQUENCE

An interrupt byte selects the logic conditions and levels which generate the interrupt. The logic function may be an *AND* or an OR. In the former case, all inputs must be active to generate the interrupt. In the latter, only one input must be active. The active levels must be either all highs or lows. Any or all of the input bits may be masked by programming the Mask Control Byte.

CTC (Counter/Timer Circuit) Programming

The CTC is used in both the counter and timer modes for controlling the operation of a disk drive during the Disk Data Transfer Mode. The four channels are mapped into the WDI-II I/O Port Assignments shown in Table 3-1. The mode of operation, counting rate, and interrupt behavior of each channel are programmed by outputting control bytes to the addressed channel (port). Each channel is initialized by writing a mode control byte and a time constant byte to each port as shown in Figure 4-5. A simplified representation of the CTC is shown in Figure 4-6. Refer to Figure 4-7 for a simplified diagram of CTC programming.

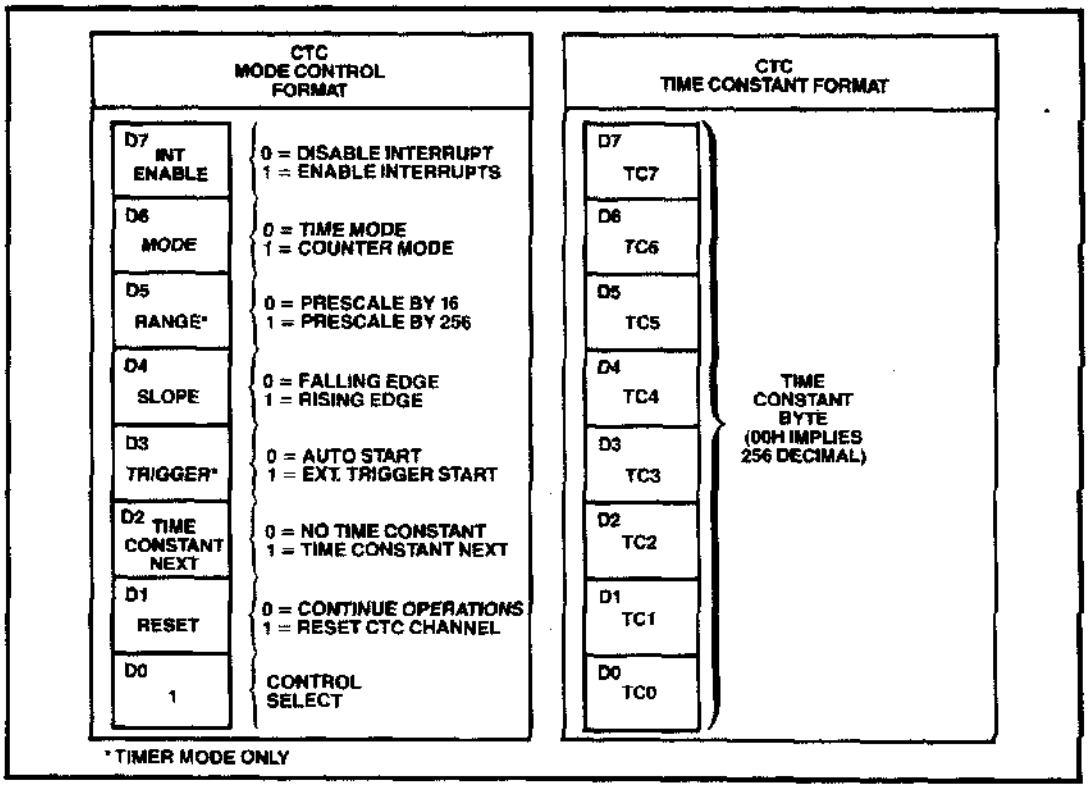


Figure 4-5: *PROGRAMMED CTC CONTROL BYTE FORMATS*

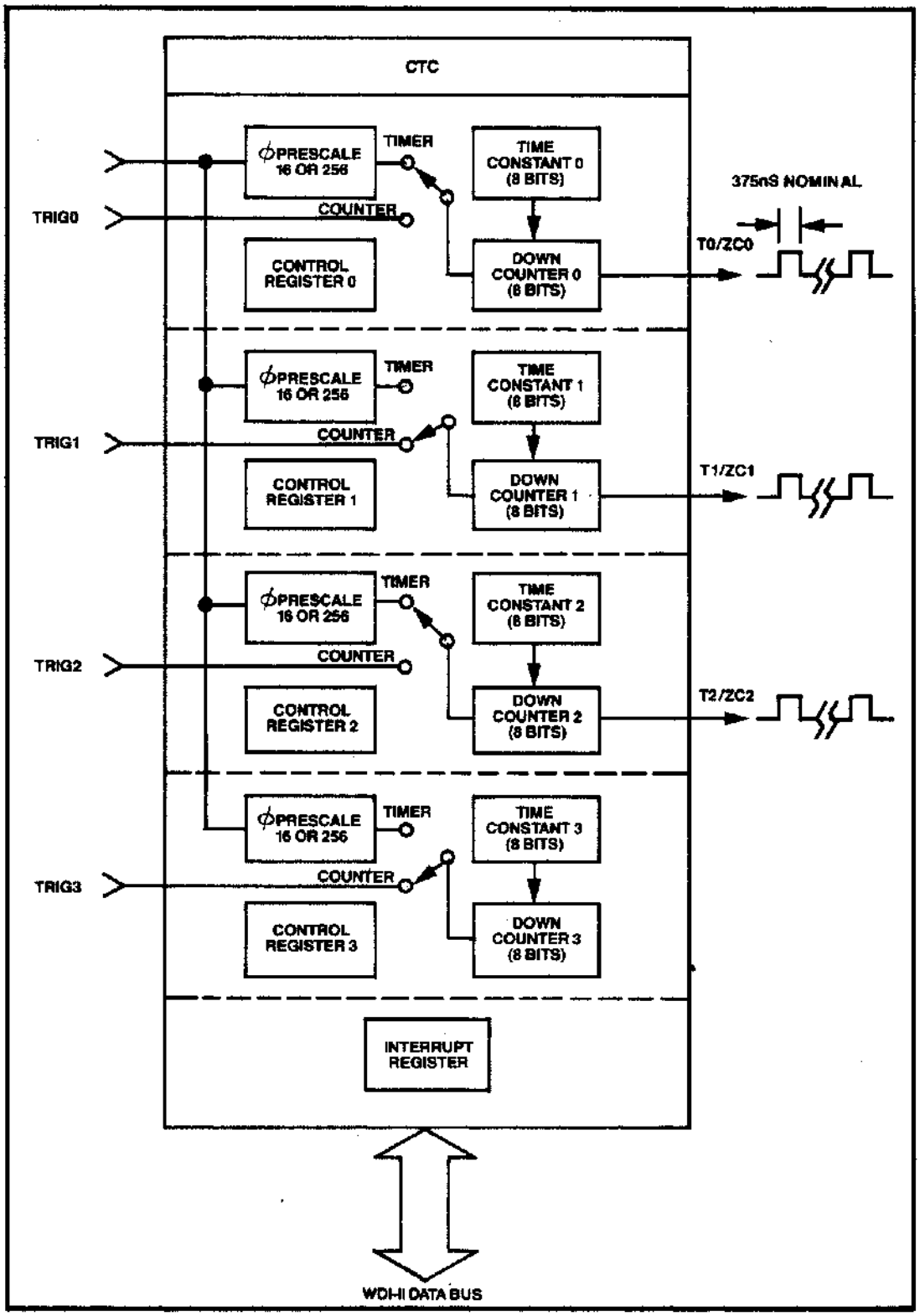


Figure 4-6: SIMPLIFIED CTC INTERNAL STRUCTURE

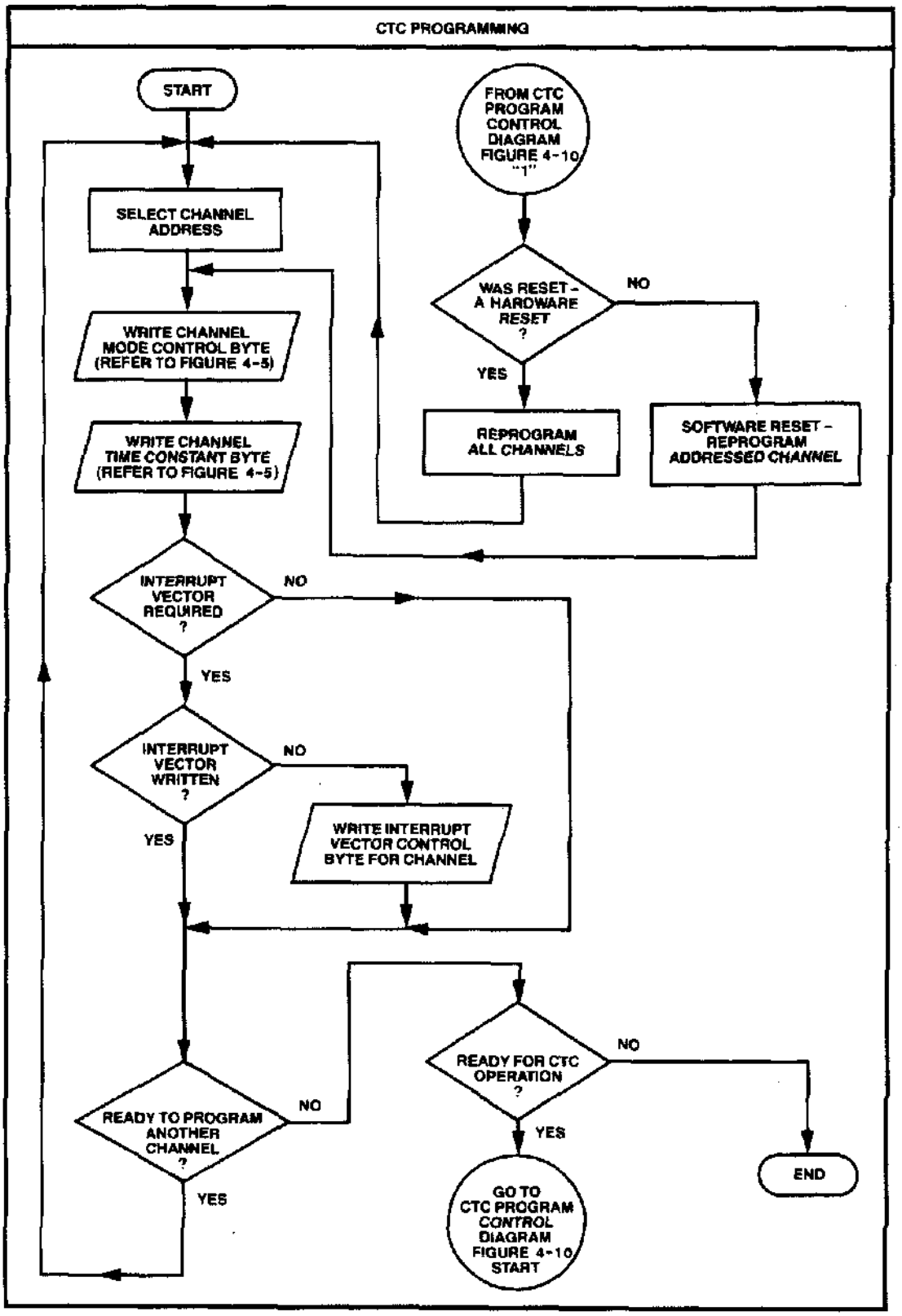


Figure 4-7: CTC PROGRAMMING SEQUENCE

The timing element of each CTC channel is an 8-bit down counter. Three of the four channels have a hardware time out or zero count output. A counter is preloaded with the programmed 8-bit time constant from which it counts down to zero. Upon reaching zero, a 375ns positive-going pulse is output from the Zero Count pin. The time constant is automatically reloaded and the counting continues uninterrupted.

Bit 6 of the mode control byte programs the addressed CTC channel to the timer or count mode. In the timer mode, the clock input $\phi 2$ (a 4 MHz signal) is connected in parallel with each channel. $\phi 2$ is prescaled by 16 if bit D5 is reset, or by 256 if D5 is set. Bit 4 causes the counter to decrement on the clock falling or rising edge. In the timer mode, the time constant and prescaler are both preloaded in determining the total count time. This is expressed as follows:

```
        t=(p*K)/4
where   t=time in us
        p=prescaled value (programmed to 16 or 256)
        k=time constant (programmed from 1 to 256; 256
          is programmed as 00h)
        4=4 MHz  φ2 Clock Frequency
```

For example:

```
  If t=8 us,
then p=16,
 and K=2.
```

Each of the three CTC channels, when used as a counter, is driven by a control signal from the disk drive. In Channels 0 and 1 it is a servo control signal. For more information refer to the sections on the individual signals, SEEK COMPLETE*, INDEX* and SECTOR*.

PROGRAMMING CONTROL THROUGH WDI-II MICROCIRCUITS, REGISTERS AND COUNTERS

The following paragraphs explain how the operating system controls the WDI-II board functions and subsequently the hard disk drives. Operating system control is discussed in terms of WDI-II microcircuits, registers and counters. Figure 4-8 shows the connections between the WDI-II and disk drive. Table 3-2 provides information on disk drive signals and interfacing. For more detailed information on the disk

drives, including disk data transfer timing diagrams, refer to the appropriate disk drive manual. For more information on error messages, refer to the appropriate disk drive manual or the system manual.

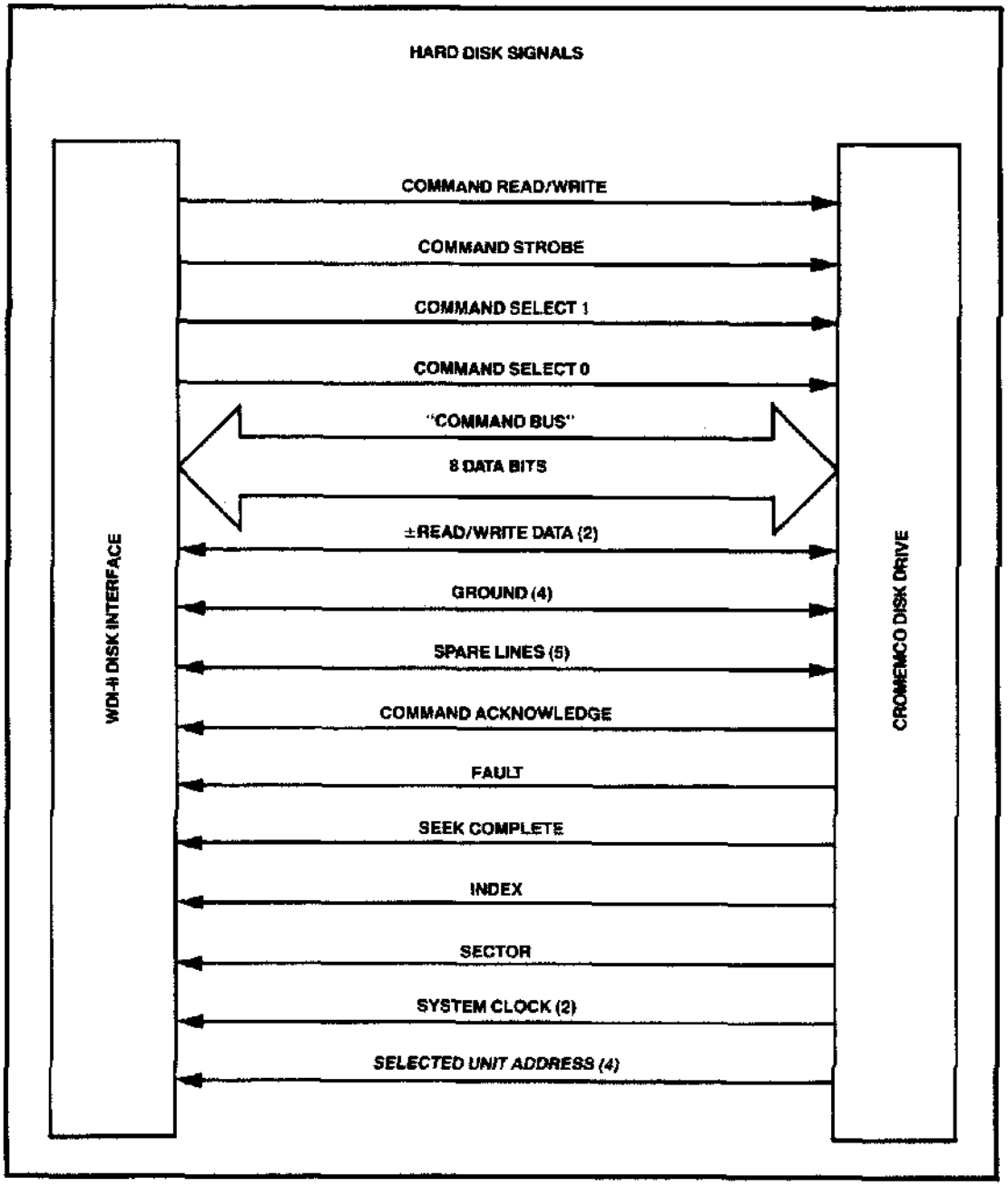


Figure 4-8: WDI-II/DISK DRIVE INTERFACE BUS

Command/Status Bus

Selecting address E0h enables the Command/Status Bus. One-of-eight command or status bytes may be selected. Four are disk drive command bytes while the remaining four bytes transmit disk drive status information. As shown in Table 4-1, one byte addresses several functions. Refer to PIO bits A0, A1, A2, A3 and A7 for Command/Status Bus control signal information.

NOTE: All signals on the Command/Status Bus are active low. Refer to Table 4-1 for more information.

Table 4-1: HARD DISK DRIVE COMMAND/STATUS BUS SIGNALS

	COMMAND/STATUS BUS CONTROL SIGNALS			COMMAND/STATUS BUS SIGNALS								
	R/W	SEL 1	SEL 0	BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRIVE COMMANDS	0	0	0	0	UAS3[1]	UAS2	UAS1	UAS0	HAS1[3]	HAS0	CAS9	CAS8
	0	0	1	1	CAS7[2]	CAS6	CAS5	CAS4	CAS3	CAS2	CAS1	CAS0
	0	1	0	2	SERVO OFFSET REVERSE	SERVO OFFSET FORWARD			DIAGNOSTIC		READ GATE	WRITE GATE
	0	1	1	3							RE-ZERO	FAULT CLEAR
DRIVE STATUS	1	0	0	4	SPEED ERROR	ILLEGAL ADDRESS	R/W FAULT	SERVO ERROR	RE-ZEROING	SEEKING	ON CYLINDER	UNIT READY
	1	0	1	5	GUARD BAND			WRITE PROTECTED	PLO ERROR	POR		R/W UNSAFE
	1	1	0	6	CAV7[5]	CAV6	CAV5	CAV4	CAV3	CAV2	CAV1	CAV0
	1	1	1	7	UAV3[6]	UAV2	UAV1	UAV0	HAV1[4]	HAV0	CAV9	CAV8

NOTE:
1. UAS0-3 = UNIT ADDRESS SELECT
2. CAS0-9 = CYLINDER ADDRESS SELECT
3. HAS0-1 = HEAD ADDRESS SELECT
4. HAV0-1 = HEAD ADDRESS VERIFY
5. CAV0-9 = CYLINDER ADDRESS VERIFY
6. UAV0-3 = UNIT ADDRESS VERIFY
7. SPACE = UNUSED BIT (NORMALLY AT LOGICAL ZERO)
8. NEGATIVE TRUE LOGIC:
   LOGICAL 1 = 0 TO 0.7V
   LOGICAL 0 = 2.4 TO 5.0V

Disk Drive Unit Address Select/Verify and Related Commands--Unit Address Select (UAS) 0-3 byte 0 bits 4-7 are used to address a specific disk drive. Unit Address Verify (UAV) 0-3 byte 7 bits 4-7 may be used to verify that the correct drive has been selected. ILLEGAL ADDRESS byte 4 bit 6 indicates that an illegal or nonexistent address for the hard disk drive has been issued. When a unit address is issued, all disk drives will check the address but only one should respond.

CAUTION

Cromemco recommends that no more than seven drives be connected to the WDI-II/Disk Drive Interface Bus at one time.

Head Address Select/Verify--Head Address Select (HAS0 and HAS1) byte 0 bits 2 and 3 are used to address a specific head in the addressed disk drive. Head Address Verify HAV0 and HAV1 byte 7 bits 2 and 3 are used to verify that the disk drive has received the correct head address. Depending on the disk drive, either 1 or up to 3 separate heads may be selected for the data transfer. The fourth head accesses disk location information in a read only mode. The signals accessed are the INDEX* and SECTOR* that have been prerecorded on the disk servo surface as reference signals for controlling disk drive operation.

Cylinder Address Select/Verify and Related Commands--Cylinder Address Select CAS0-9, byte 1 in its entirety and byte 0 bit 0 and bit 1, are used to address a specific cylinder (track location) on the disk. Cylinder Address Verify CAV0-9, all of byte 6 and byte 7 bit 0 and bit 1, may be used to verify that the disk drive unit has received the correct cylinder address. SEEKING byte 4 bit 2 is active while the head is being moved to the correct track. The ON CYLINDER signal, byte 4 bit 1, indicates that the head has arrived at the correct track (cylinder).

Servo Command and Status Signals--SERVO ERROR byte 4 bit 4 indicates that the selected drive has detected a seek error condition. This may be due to the following:

1. The SEEKING (cylinder) process has not been completed.

2. REZERO is incomplete.

3. An invalid address (UAS, CAS, or HAS) has been selected.

4. The head is over a GUARD BAND.

For SEEK and REZERO, the REZERO or POR (Power On Reset) command must be reissued to enable disk drive operation. Issuing FAULT CLEAR will clear SERVO ERROR.

SERVO OFFSET FORWARD and SERVO OFFSET REVERSE byte 2 bit 6 and bit 7 cause the head to move forward (toward) or reverse (away from) the disk drive spindle. The head

moves in 400 micro inch increments. A new command must be reissued for each subsequent movement. ON CYLINDER goes false until the offset position is reached.

NOTES:

1. Servo offset commands may be used in an error recovery mode.

2. Servo offset commands will affect disk drive operation immediately. This means that only the CMD STB is needed. CMD AK has no effect. (This occurs only in Command/Status Bus byte 2.)

Diagnostic--DIAGNOSTIC byte 2 bit 3 causes the disk drive to ignore a R/W UNSAFE signal while other byte 2 drive commands are active.

Write (to disk) and Read (from disk) Control Signals--The commands WRITE GATE byte 2 bit 0 and READ GATE byte 2 bit 1 are normally inactive until the final phases of the disk data transfer operation when one or the other is programmed for the active state. At this time, the WDI-II circuits allow the READ or WRITE GATE signal to pass to the disk drive, enabling the disk drive for the forthcoming data transfer. Other WDI-II circuits begin the actual data transfer when the proper disk sector location is reached. The command mode is held while waiting for the WRITE or READ GATE command to be sent to the disk drive by holding the CMD STB signal true. When the WRITE or READ GATE signal is passed to the disk drive, the drive responds immediately without waiting to output the CMD AK signal.

R/W (Read/Write) FAULT byte 4 bit 5 indicates that multiple head selection, write current is flowing but either no write data exists, or the WRITE GATE has not been enabled.

R/W UNSAFE byte 5 bit 0 indicates that the FAULT signal is true.

WRITE PROTECT byte 5 bit 4 indicates that writing to the disk is not allowed. This may be because a FAULT signal is active or the disk drive is set to the write protect mode. Refer to the appropriate disk drive instruction manual for more information.

Rezero/Rezeroing--REZERO byte 3 bit 2 causes the head to move to track 000; the head and cylinder registers are reset to zero while ON CYLINDER, SERVO ERROR and R/W FAULT are cleared. A SEEK COMPLETE pulse is generated at the end of REZERO. REZEROING byte 4 bit 3 is active during the REZERO operation.

Fault Clear--FAULT CLEAR byte 3 bit 0 resets the FAULT status flip-flop.

Guard Band--GUARD BAND byte 5 bit 7 indicates the read/write head is outside the data track area.

PLO (Phase Locked Oscillator) Error--PLO ERROR byte 5 bit 3 indicates that the disk drive phase locked oscillator is not synchronized with the clock pulses from the servo control surface.

POR (Power-On Reset)--POR byte 5 bit 2 indicates a 12 to 15s delay. This allows the disk drive motor to reach proper operating speed. The disk drive logic circuits are reset by POR during this time.

Speed Error--SPEED ERROR byte 4 bit 7 indicates that the disk speed is not within tolerance. Refer to the disk drive instruction manual for more information.

Unit Ready--UNIT READY byte 4 bit 0 indicates that no FAULT exists. The disk drive unit is ready to read, write or seek.

Extended Address Function--The system program enables this function by using address E1h. Data inputs DO0 through DO7 from the S-100 Bus are enabled. The RD* signal from the S-100 Bus clocks data from the WDI-II Data Bus, through the Extended Address Latch and onto the S-100 Bus Extended Address Lines (A16-A23). Addresses E2 and E3 are not used.

PIO (Parallel Input/Output Controller) Control

Addresses E4h through E7h are used in programming and controlling the operation of the PIO. E4h and E5h are used to select the PIO data (operational) modes while E6h and E7h select the command (programming) modes. In

the command modes, the I/O functions of the registers are selected by the system program. In the data modes, the programmed functions are enabled, in effect becoming part of the WDI-II circuit board hardware. The command modes should be programmed at the beginning of WDI-II board operation. The data modes are then selected, as required, during the execution of the Disk Data Transfer mode. Refer to Figure 4-9 for a simplified program control sequence for the PIO.

Port A Data Mode--Address E4h selects the Data Mode for Port A of the PIO. The port I/O is 8 bits wide and interfaces the operating system to the hard disk drive(s) through the Command/Status Bus. Each individual bit and its purpose follow. For more information about bits A0, A1, A2, A3 and A7, refer to the section entitled **Command/Status Bus** in this chapter. Refer also to Table 4-1, Table 3-2, and the Z-2H and HDD manual.

A0 Command Read/Write--CMD R*/W provides operating system control of the Command or Status mode. The Command mode is selected with a logical true, the Status mode with a logical false.

A1 and A2, Command Select 0 and 1--CMD SEL 1* and CMD SEL 2* provide operating system selection of one-of-eight Command/Status Bus bytes in conjunction with A0. Four bytes may be selected in the command mode and four bytes in the status mode.

A3 Command Strobe--CMD STB* is used in conjunction with A7 to provide handshaking between the S-100 Bus and the disk drive unit. In the command mode, A3 is issued by the operating system at least 200ns after the command byte is placed on the Command/Status Bus. A3 signals the disk drive that the Command/Status Bus information is valid. In the status mode, A3 signals the disk drive that the operating system is ready to receive status information.

A4 Drive Identifier--Under program control, DRV ID indicates the disk size of the addressed disk drive. In conjunction with A6, this signal also indicates the model of the WDI Winchester Disk Interface board (WDI or WDI-II). A logic true output from A4 indicates that a 5" disk drive is being used; a logic false indicates an 8" disk drive.

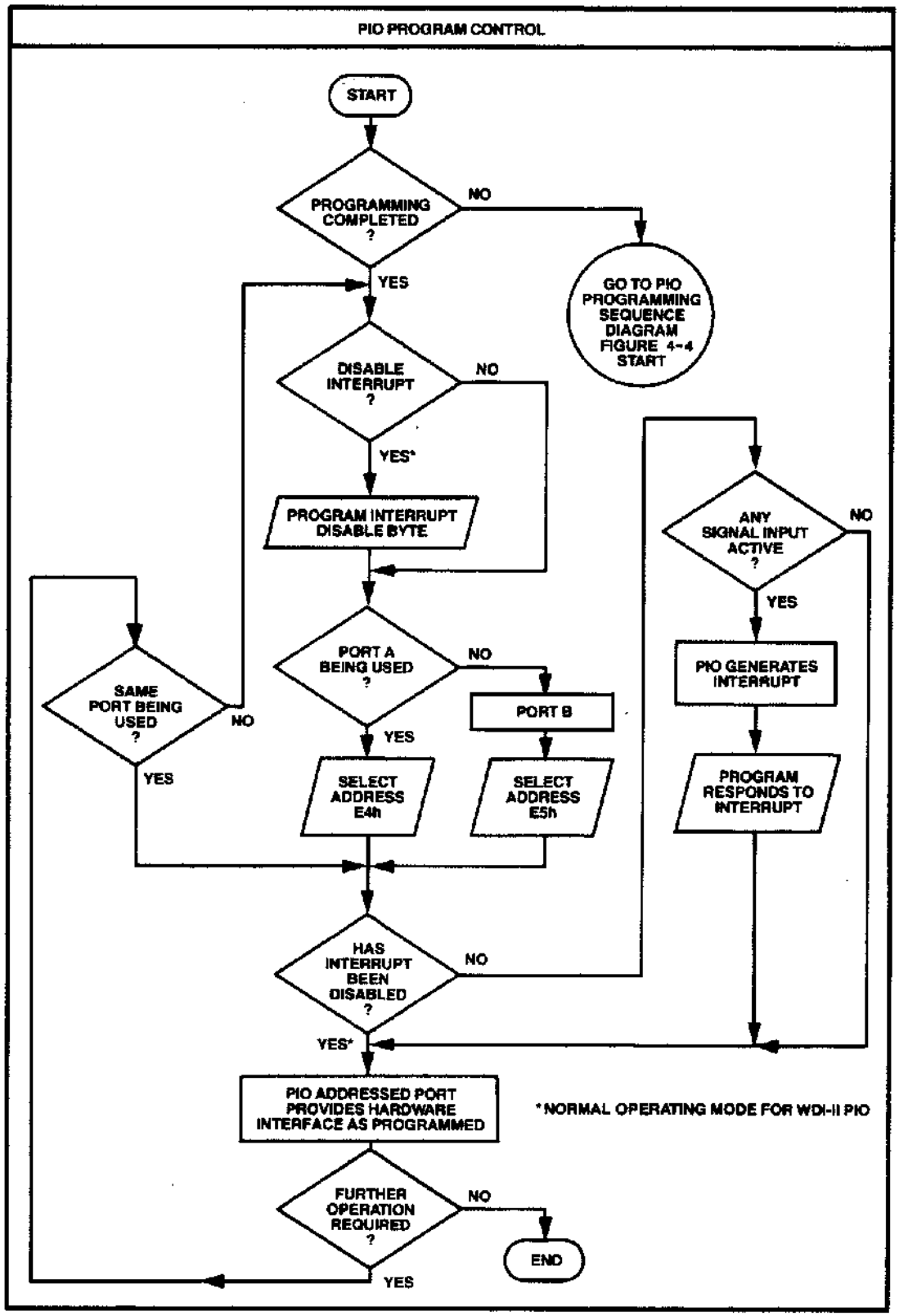


Figure 4-9: PIO PROGRAM CONTROL

A5 Seek Complete--SEEK COMPLETE* pulses at the completion of the head carriage movement. This signal is input to the CTC and PIO microcircuits, and this can trigger a counter and/or be polled immediately by the operating system.

A6 Board Identifier--BRD ID will always be the same state as A4 if the WDI-II is the interface board.

A7 Command Acknowledge--CMD AK* is used in conjunction with A3 to provide handshaking between the S-100 bus and the hard disk drive. In the command mode, this signal indicates that the disk drive has received and latched the command byte. The operating system can now have the WDI-II release A3. In the status mode, the disk drive indicates that the status byte is valid; that is, the operating system should read this byte and then release the command strobe. Note that A7 is issued by the selected drive only.

Port B Data Mode--Address E5h selects the Port B Data Mode of the PIO. The port I/O is made up of 8 bits of data interfacing the operating system to the WDI-II circuits and a disk drive. Each individual bit and its purpose follow.

B0 Disk Operation--DISK OP* has two primary purposes that relate to disk data transfer.

1. It provides the "first byte" trigger which initializes the appropriate WDI-II circuits for the coming data transfer.

2. It controls the pulse synchronized READ or WRITE GATE signals issued to the disk drive units.

B1 Fault--FAULT* indicates to the system that at least one of several possible problems exist in the disk drive unit. These are:

1. multiple heads selected,

2. write current with no write data,

3. write current without WRITE GATE enabled,

4. WRITE GATE active with no ON CYLINDER signal,

5. disk drive phase locked oscillator synchronization error indicated by PLO ERROR,

6. head forced off track, or

7. disk drive internal SEEK or REZERO time out.

FAULT* inhibits the write-to-disk mode when active. The Command/Status Bus may be polled to determine the fault. REZERO clears FAULT*.

B2 DMA Ready/Start--DMA RDY/START is issued by the system to the Disk Data Transfer Synchronizer which generates the DMA RDY signal. The bus request (BUSRQ*) is output by the DMA to the system CPU when DMA RDY is received.

B3-B6 Select Unit Address 0 through 3--SEL UNIT ADDR 0* through SEL UNIT ADDR 3* indicate which disk drive has been selected. The same information can be obtained on the Command/Status Bus using UAS0 through UAS3, and it is recommended that UAS0 through 3 be used rather than these signals. Refer to the Z-2H and HDD manual for information pertaining to selection of disk drive addresses.

B7 CRC Error--An active CRC ERROR signal indicates to the system program that an error has occurred in transferring data to or from the disk.

Port A Programming Mode--Address E6h selects the Port A programming mode. PIO Port A is programmed for operation as stated under **Port A Data Mode.** Programming is received from the S-100 Bus under the control of the operating system drivers. Refer to Figure 4-4 for a simplified diagram of PIO programming requirements.

Port B Programming Mode--Address E7h selects the Port B programming mode. PIO Port B is programmed for operation as stated under **Port B Data Mode.** Programming is received from the S-100 Bus under the control of operating system drivers. Refer to Figure 4-4 for a simplified diagram of PIO programming requirements.

DMA Control

Address E8h selects the DMA microcircuit. The DMA is programmed for one of two operations. During disk data transfer, the DMA is programmed for the search continuous mode, and for memory-to-memory transfer, it is programmed for the transfer mode. The DMA is placed in the Command (programming) or Data (operating) modes under software control. Refer to the section entitled **Microcircuit Programming** for more information.

Addresses E9h through EBh will also select the DMA microcircuit but it is recommended that E8h be used exclusively for this purpose. E9h through EBh are then reserved for future operating mode expansion. Using E8h for DMA Control will ensure software compatibility with future hardware configurations.

CTC Control

Each of these addresses, ECh through EFh, enables one-of-four counters that is part of the CTC microcircuit. In the present configuration, only Channels 0-2 are used. Each is used in the disk data transfer operation. Refer to Figure 4-10 for a simplified CTC program control sequence.

Channel 0 is addressed by **ECh** and is used in the counter mode only. It is programmed to a value of 1. When the INDEX pulse from the disk drive servo control surface is received by the TRIG1 input, the operating system learns of this event by monitoring the CTC data lines. For more information, refer to the paragraphs under **CTC Programming** in this chapter. Note that the INDEX* pulse is also connected to A5 of the PIO. This counter, in the timer mode, could be used to check the rotational speed of the disk.

Channel 1 is addressed by **EDh** and is used in both the counter and timer modes. In the counter mode, the channel is programmed to count sectors, determining when disk data transfer is to start. The counter is then immediately programmed for the timer mode with a predetermined time period. The timer ensures a specific passage of time before the beginning of the next event in the disk data transfer. When time is up, the time out TO1 signal from the CTC triggers the next event.

Channel 2 is addressed by **EEh** and is used in the counter mode only. It is used exactly like the counter of Channel 0. The signal input is the SEEK COMPLETE* signal from the disk drive, which indicates that the cylinder seeking process has been completed.

EF Counter 3 is not used in the operation of the WDI-II circuit board.

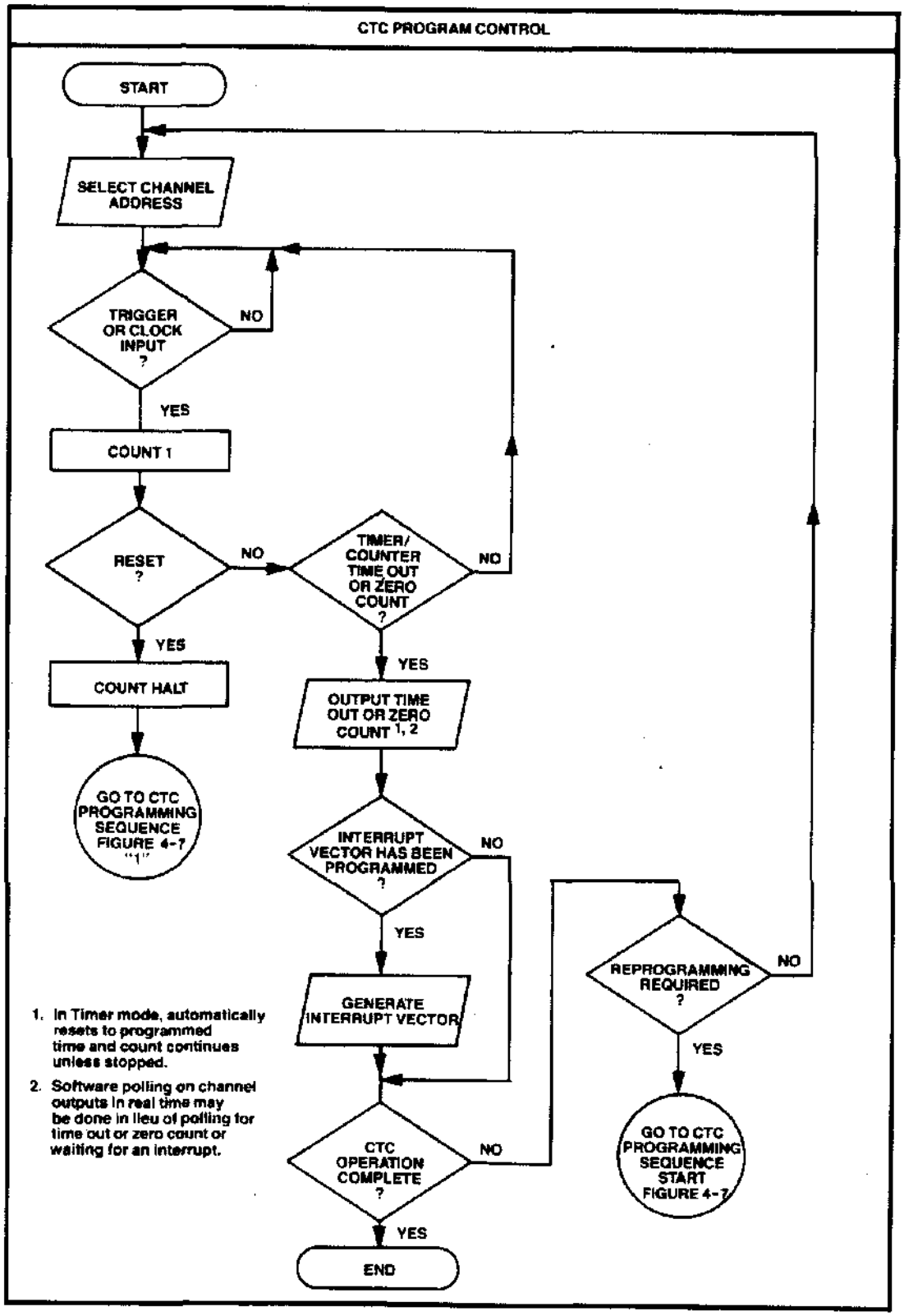


Figure 4-10: CTC PROGRAM CONTROL

Chapter 5

PRINCIPLES OF OPERATION

INTRODUCTION

This chapter explains the operating principles of the WDI-II.

PRINCIPLES OF OPERATION

The primary purpose of the WDI-II is to provide an interface between the S-100 Bus and a hard disk drive. This facilitates the exchange of data between the system main memory and the hard disk surface media. A secondary purpose that is often very important, is to transfer data rapidly between main memory locations. The board may also be used to place "extended addresses" onto the appropriate S-100 Bus signal lines.

Operating Modes

The operating system causes control, status, address, and data information to be exchanged with the WDI-II or to be passed on to the hard disk drive. The operations and functions that the WDI-II performs are selected under operating system control by programming and selectively enabling the operation of the registers contained within the WDI-II microcircuits. These operations and functions are explained in greater detail in the following paragraphs.

Disk Data Transfer Mode

The DMA is programmed with the starting addresses of the memory location source or memory location destination, and with the data block length (number of data bytes to be transferred). It is also programmed to respond to the DMA Ready signal.

The WDI-II performs three main functions in the Disk Data Transfer Mode.

1. The WDI-II converts data from the format used in system main memory to the format required by the disk in the write-to-disk mode; it also converts the data from the disk format to the system main memory format in the read-from-disk mode.

2. The WDI-II transfers disk drive status information to the operating system and operating system commands to the disk drive.

3. The WDI-II reconciles timing differences in the data transfer between the S-100 Bus and the disk drive.

In performing these functions, the WDI-II circuits execute many operations. The Address Decode circuit, under operating system control, enables the individual circuits that perform each operation. The Address and Data Bus Buffers control address and data signal transfer between the S-100 Bus and WDI-II circuits. The Control Bus Buffers interface Z-80 compatible control signals between the system Z-80 microprocessor and the WDI-II Z-80 compatible microcircuits. The Formatter converts the data to the proper format, as required by the S-100 Bus or the disk, and controls DMA operation to ensure correct data transfer. The Address Generator function, performed by the DMA, addresses each location in main memory to or from the data that is to be transferred. The control and status circuits, which include the CTC, PIO and Command/Status Bus, interface the system and the disk drives. This allows the operating system to control the disk drives.

Other timing and control circuits are found on the WDI-II. Particularly important is the Disk Data Transfer Synchronizer circuit. The description later in this chapter includes information about the interaction of the control circuits that allow the transfer of data to and from the disk media.

In the write-to-disk mode, data transfer occurs as follows. First, a synchronization byte, four identification bytes and 512 data bytes are written to the system main memory. Then, under Formatter control, a preamble of zeros is written to the disk. This is followed by seven header bytes, 512 data bytes, two CRC error check bytes and the postamble zeros. The header bytes include the synchronization byte (01h), the four identification bytes, two CRC error check bytes and a byte of trailing zeros. The identification bytes are the addressed head identifier (1 byte), the addressed track (cylinder) identifier (2 bytes), and the addressed sector identifier (1 byte). Refer to the appropriate disk drive instruction manual for more information on disk data formatting.

Data flow from system main memory is halted while the preamble zeros, CRC bytes, trailing zero and postamble zeros are being written to the disk. Data flow from the memory is restarted by the Formatter as required. The first two CRC bytes are calculated from the identification bytes only. The last two CRC bytes are calculated from the data bytes.

Because of the physical characteristics of the data on the disk, data transfer from the disk must be done in one continuous stream. Therefore, in the read-from-disk mode, data transfer to the system main memory occurs in a group of four identification bytes or in a group of 516 bytes that includes the four identification bytes and 512 data bytes. The zeros, synchronization, and CRC bytes are either ignored or used by the WDI-II circuits for information spacing on the disk media, control, or error checks.

Memory-to-Memory Transfer Mode

In this mode, the DMA is programmed for the memory location source starting address, the memory location destination starting address, and the data block length (number of data bytes to be transferred). The DMA is also programmed to ignore the DMA Ready signal. Once programmed, the DMA immediately issues bus request (BUSRQ*). The system CPU acknowledges the bus request with bus acknowledge (BUSAK*) and gives S-100 Bus control to the DMA. At this point, the DMA takes control and transfers that data as quickly as it can. Normally this works out to be from 1/4 to 1/10 the time taken in a microprocessor controlled data transfer. Control of the bus is held by the DMA until the end of the data block is reached, at which time the DMA returns control of the bus to the system.

Extended Address Function

This operation is referred to as a board function rather than a mode because it requires no preprogramming. Data lines DO0 through DO7 from the S-100 Bus are enabled so that addresses in the form of data may be placed on the WDI-II data bus lines. From there the addresses are clocked onto the S-100 Bus address lines A16-A23.

PRINCIPLES OF CIRCUIT OPERATION

Address Decoder

This circuit consists of IC21B, IC26B, IC54B, IC55A, IC55B, IC55C, and IC55E. With the jumpers in the positions shown on the schematic, the circuit decodes addresses E0h through EFh as found on S-100 Bus address lines A0 through A7. The base address (A4-A7) is decoded by IC54 as defined by the jumper locations. A2 and A3 of the offset address are decoded by IC26 to select one of four circuits. In addressed order, the circuits are:

1. The Command/Status Bus circuits IC19, IC20, IC39 and IC40, the Extended Address Latch IC52 and their decoder IC21 and IC26 as addressed by E0h and E1h and enabled by PIO0 SEL*;

2. The PIO (Peripheral Input/Output) Controller IC42 as addressed by E4h through E7h and enabled by PIO1 SEL*;

3. The DMA (Direct Memory Access) Controller IC43 as addressed by E8h and enabled by DMA SEL*;

4. The CTC (Counter/Timer Circuit) IC30 as addressed by ECh through EEh and enabled by CTC SEL*.

Address lines A0 and A1 select the operating modes of most of these circuits. Refer to the individual circuit operation descriptions for more information pertaining to circuit mode and selection.

Address and Data Bus Buffers

These circuits buffer the S-100 Bus connections to the WDI-II. The buffers enable or inhibit address and data flow to ensure that the required signals are passed between the S-100 Bus and the WDI-II at the correct time.

The Address Buffers (IC56 and 57) connect the Address Generator (DMA) address outputs to the S-100 Bus in the Disk Data and Memory-to-Memory Transfer Modes.

Data flowing from the S-100 Bus to the WDI-II circuits is received through IC58 via the DO0 through DO7 lines as long as the system microprocessor maintains control of system operation. This occurs while the WDI-II

Extended Address Function is operating or during the disk data write-to-disk mode.

In the disk data read-from-disk mode and Memory-to-Memory Data Transfer Mode, the DMA has control of data transfer. In these modes, data exchanged with the S-100 Bus is output through IC58 and input through IC59.

Control Bus Buffers

IC29, IC51 and IC60 buffer the control signals between the S-100 Bus and the Z-80 compatible microcircuits. Other associated circuits, such as IC41 and IC53, control the buffers or provide inputs and outputs to the S-100 Bus.

The DMA and DMA* signals control the Control Bus Buffers and their associated circuits. Since the state of these signals depends on the state of BUSRQ* and BUSAK*, the Control Bus Buffers are enabled and inhibited as required by DMA operation.

Control Signal Switching and Synchronization

IC23, IC27 and IC28 select and synchronize the control signals required by the computer system, the DMA Controller, and related WDI-II circuits in the Disk and Memory-to-Memory Data Transfer Modes.

Disk Data Transfer Mode--During disk data transfer, the DISK OP signal is active (high). The IC28 multiplexer inputs B1 and B2 are coupled to Y1 and Y2 respectively.

The DMA RDY signal, clocked through IC23B, is coupled to IC23A from IC28 B1 to Y1. The Q* output of IC23A presets the input of the Control Signal Switching and Synchronization and Disk Data Transfer Synchronizer circuits. The Q output of IC23A is coupled to the S-100 Bus to provide synchronization with system circuits (see S-100 Bus signals pSYNC and pRDY) and with the WDI-II CTC and the Formatter Parallel to Serial Converter circuit.

The WRITE (to disk) signal is passed from the B2 input of IC28 to the Y2 output. This signal is passed through latch IC27 and other gates and inverters to control lines on the S-100 Bus.

Memory-to-Memory Transfer Mode--In this mode, signals from the S-100 Bus or the DMA are input to multiplexer IC28. The A1 to Y1 signal from the S-100 Bus is used during the programming mode of the DMA (refer to **DMA Controller Programming** in Chapter 4). An active signal (low) from the DMA in operating mode indicates that the address on the S-100 Address Bus is valid.

The A2 to Y2 signal RD* from the S-100 Bus tells the DMA that the system wishes to read the status bytes from the DMA read registers (programming mode). This same signal, coming from the DMA (operating mode), means that a DMA controlled read from system main memory is taking place.

Synchronization--IC23 and IC27 provide synchronization of the control signals as these flip-flops and the latch are clocked by the ϕ2 system clock.

Direct S-100 Bus/WDI-II Control Signals

It is important to realize that there are some signals controlling the interfacing of the S-100 Bus and WDI-II that are completely independent of the buffered and controlled circuits. Among these are SINTA, SOUT, pDBIN, pHOLD*, pHLDA, SINP, and SMI. They provide direct communication between the system and the WDI-II interface. These signals control the board in the various operational modes. With the **Address Decoder**, they select the WDI-II mode of operation.

ϕ2 Clock Input Circuits

The ϕ2 S-100 Bus clock signal is normally input to IC6F, IC33A and their associated components. These circuits invert and increase the duty cycle of ϕ2 to produce a symmetrical waveform. This symmetrical signal is then coupled directly to the Control Signal Switching and Synchronization circuit. The clock signal is also inverted and coupled to the Disk Data Transfer Synchronizer, the clock driver/translator (Q1 and Q2) which drives the non-TTL clock inputs of the DMA, CTC and PIO microcircuits, and is coupled to the Formatter Enable/Start circuit. Although the Formatter Enable/Start circuit is TTL compatible, the clock will still operate properly since it is within TTL specifications.

If the system CPU is on a circuit board other than the Cromemco ZPU, the jumper location must be moved so that the input is connected to the WDI-II circuits through IC3A. Refer to the schematic and the jumper selection information in Chapter 2.

Address Generator

The DMA circuit is the Address Generator used in the Disk Data and Memory-to-Memory Data Transfer Modes. When data is transferred between system main memory locations or the hard disk drives, the DMA outputs one or more addresses to the system, selecting the data transfer main memory location.

Disk Data Transfer--In the Disk Data Transfer Mode, the DMA is programmed for the search continuous mode of operation. This means that when enabled, the DMA is given control of the S-100 Bus. Other control requirements will have been programmed into the DMA by this time. The DMA will try to find a match between the current data byte and the programmed Match Byte, and since the Mask Byte is programmed to never allow a data match, the search is continuous.

During the disk data transfer, the DMA RDY output of the Disk Data Transfer Synchronizer controls DMA operation. Operation is continuous, except when the DMA RDY line is forced inactive by the Formatter. The DMA continues searching until the programmed block of data has been transferred. In the write-to-disk mode, this will always be 517 bytes. In the read-from-disk mode, a header read is 4 bytes and the data read (which is all the data contained on the track within a sector) is 516 bytes. Refer to the **Disk Data Transfer Synchronizer** paragraphs for an operational description of the disk data transfer control circuits. Refer to Chapter 4 for further information on DMA programming and programmed operation.

Memory-to-Memory Transfer--In the Memory-to-Memory Transfer Mode, the DMA circuit is given control of the S-100 Bus. The control requirements have already been programmed into the circuit. The Data and Address *Buffers are enabled by the DMA until the data transfer* is completed. The DMA outputs the BUSRQ*, MEMR*, RD*, WR* and IORQ* signals to control the data transfer. Refer to Chapter 4 for further information on DMA programming and programmed operation.

When the system issues the pRESET* signal, the DMA is reset by the +5V being removed from the DMA VDD input at pin 11.

DMA Bus Request Priority--After the DMA has issued a bus request (BUSRQ*) (pHOLD*) signal, the system microprocessor will return a bus acknowledge (BUSAK*) (pHLDA) signal to the DMA bus acknowledge input (BAI*). This occurs only after the microprocessor has completed its current task. If the WDI-II is the first priority bus request circuit, the jumper will remain in the position shown on the schematic. The S-100 Bus pHLDA signal comes into the DMA BAI* first, meaning that this bus request will be serviced before any other. If the bus request priority is less than that of other circuit(s), the jumper connected to the DMA BAI* is placed in the other position, tied to the next higher priority circuit board bus acknowledge output (BAO*) line. The higher priority board's bus request will then be serviced before the WDI-II DMA. The BAO* line is tied directly to the BAI* within the DMA which serves to inhibit the lower priority circuits from being serviced before the WDI-II DMA interrupt. Refer to Chapter 2 for more information.

Disk Data Transfer Synchronizer

The Disk Data Transfer Synchronizer, made up of IC12B, IC13B and IC16C, is the key circuit in the disk data transfer operation. It synchronizes the data transmission between the system main memory (via the DMA) and the disk media (via the Formatter). It also ties together the control exerted by the Control Signal Switching and Synchronizing circuit and the Formatter Enable/Delay circuit on the data transfer operation.

The DMA RDY/START signal (from PIO B2) triggers the synchronizer "first byte". As a result, the DMA RDY signal is output to the DMA's RDY input and to the D input of IC23B in the Control Signal Switching and Synchronization circuit.

DMA Response to the DMA RDY Signal--The DMA responds by issuing a bus request (BUSRQ*) (pHOLD*) signal to the system microprocessor. The microprocessor returns a bus acknowledge (BUSAK*) (pHLDA) signal to the DMA when it releases bus control to the DMA. The BUSRQ* and BUSAK* signals generate the DMA signal initiating Formatter operation through the Formatter Enable/Start circuit.

Control Signal Switching and Synchronization Circuit Response to DMA RDY--DMA RDY is clocked through IC23B and is passed through Multiplexer IC28 from the B1 input to the Y1 output. This signal is selected by the DISK OP signal at the S (select) input. Then DMA RDY is clocked through IC23A. Note that it takes 2 clock pulses for DMA RDY to reach the outputs of IC23A. The Q* output resets IC23A (the input of the Control Signal Switching and Synchronization circuit) and IC12 and IC13 of the Disk Data Transfer Synchronizer circuit. This effectively resets or initializes these circuits for transfer of the "first byte" of data.

DMA and Disk Data Transfer Synchronizer Response to Setting the Disk Data Transfer Synchronizer Flip-Flops--When IC12 is set, the DMA RDY signal is removed from the DMA. The DMA BUSRQ* goes inactive, returning bus control to the system and the DMA signal to the Formatter Enable/Start circuit goes inactive.

With IC13 set, the Disk Data Transfer Synchronizer circuit is initialized for continuing DMA data transfer under Formatter control.

Formatter Enable/Start and Formatter Response to the DMA Signal Being Made Active and then Inactive--The DMA signal is input to AND gate IC44B. The Q output of IC47 is normally high; the high applied to the D input of IC47A is clocked on the first $\phi 2$ clock pulse. The Formatter enable (FRMTR EN) signal enables Formatter operation for one count, effectively initializing the circuit. When the DMA signal is removed, the Formatter resets the counters and then waits for the signal to begin data transfer. For more information on the operation of these circuits, refer to the appropriate circuit description.

Summary of Disk Data Transfer Synchronization Operation--The net effect of disk data transfer synchronization is that all of the circuits involved in the disk data transfer are initialized and ready to begin the data transfer. The circuits involved are the Address Generator and Formatter, controlled by the Disk Data Transfer Synchronizer, Control Signal Switching and Synchronization Circuit, and the Formatter Enable/Start Circuit. The data transfer will begin when the Formatter Enable/Start circuit receives the time out T01 signal from CTC IC30. For more information on the generation and effect of this signal and the individual operation of each of the circuits taking part in the

disk data transfer operation, refer to the circuit description under the appropriate circuit title. Refer also to **Disk Data Transfer Mode** in Chapter 4.

Formatter

The Formatter changes the data being transferred to the format required by either the magnetic disk memory storage system or the system main memory. The Formatter accomplishes this as follows:

1. It converts the data to either the serial or parallel format acceptable to the disk or main memory respectively;

2. It outputs a DMA control signal to the Disk Data Transfer Synchronizer so that

    a. the DMA operation controlling data flow to and from main memory and synchronized to the system $\phi 2$ clock may be synchronized to

    b. the Formatter, controlling data flow to and from the disk and synchronized to the disk drive SYSTEM clock;

3. It calculates and records the error check of the data written to the disk and then recalculates the error check signal of the data read from the disk and compares it to the error check bytes recorded with the data;

4. It controls all of these operations on a byte by byte basis so that the data transfer is ordered and error free.

The Formatter is enabled upon receipt of either the WRITE (to disk) signal in the write-to-disk mode or the Formatter Enable/Start (FRMTR EN/START) signal in the read-from-disk mode. Actual data transfer begins when the Formatter Enable/Start circuit issues the FRMTR EN/START in the write-to-disk mode or receives the synchronization byte from the disk in the read-from-disk mode.

Formatter Control--After the Formatter is enabled, the next differential clock pulse (± SYS CLK) from the disk drive IC12A causes the CLR to Byte Counter IC7, IC8, IC11 and Bit Counter IC10 to go inactive and enables ROM IC31. The Bit Counter outputs a carry on the first clock pulse. This increments the Byte Counter and outputs the request byte (RQ BYTE) signal to the Disk Data Transfer Synchronizer circuit when the DMA ready enable (DMA RDY EN) signal from the Formatter control circuits enables gate IC16C. As the Byte Counter increments once for each data byte transferred, it outputs control signals to the ROM IC31. The ROM contains several tables of control information which are dependent on several parameters. Among these are 1) the particular byte being transferred, 2) the mode of data transfer, (the write-to-disk or read-from-disk mode), and 3) the disk format (either a 5" or 8" drive). Note that the Byte Counter outputs at IC31 pins 1-5 and 16, the WRITE (to disk) signal at pin 18 and the Disk Identification (DISK ID) signal at pin 19 are all ROM input control signals. The ROM output (Formatter control) signals are latched into IC32 where they are output to various sections of the Formatter.

Parallel to Serial Converter--In the write-to-disk mode, the disk write enable (DISK WR EN) signal enables the parallel input latch IC37. A pulse (controlled by DMA RDY) from the Control Signal Switching and Synchronization circuit causes the data from the system main memory to be latched into IC37. The Bit Counter controls the shift register IC45 load or shift operation, which is synchronized to the ± SYS CLK by flip-flop IC13. The data from the latch is loaded into the shift register. Then, under control of the shift clock enable (SHFT CLK EN) signal, the data is clocked out to the TTL-to-Differential Converter IC17. The differential read/write data (± R/W DATA) signal output from IC17 is in the format required by the disk drive. Note that IC17 is enabled by the WRITE (to disk), check load enable (CHK LD EN) and PRESET signals to the CRC (Cyclic Redundancy Check) circuit IC34 and IC35. The latter two signals pass though IC36A and IC16C respectively and join at IC16A to enable IC17.

Serial to Parallel Converter--In the read-from-disk mode, data is received from the disk drive by the Differential-to-TTL Data Converter IC18. The latch of the Serial to Parallel Converter is enabled by the READ (from disk) and DMA signals. Data is shifted into IC46

by the ± SYS CLK under the control of the SHFT CLK EN signal. Data is synchronously latched onto the data bus under the control of the Bit Counter.

Formatter Synchronization--The Formatter is synchronized to the disk drive ± SYS CLK. The clock signal is input to the Formatter though IC18. From there it branches to various locations in the Formatter as required. The control section receives the clock signal directly. Note that this signal is applied to the Bit and Byte Counters, the Formatter Control Output Latch and the Formatter Enable/Start flip-flop IC12A. The SHFT CLK EN signal gates the synchronizing clock signal to shift registers IC45 and IC46 through IC16D. The CRC CLK EN gates ± SYS CLK through IC33C to the CRC circuits. Note also that the DISK OP signal enables the ± SYS CLK input into the Formatter through IC18.

Data Error Checking--Error checking requires two separate operations in each of the two main disk data transfer modes. In the write-to-disk mode, the data written to the disk is applied to the CRC Calculator circuits IC1C, IC2A, IC2B and IC2C through IC15B. These circuits are tied to CRC Shift Registers IC34 and IC35, which store the two calculated CRC bytes. Note that as the calculations are made, the individual bits are saved as they are shifted through the gate and input circuits and back into the registers. The calculated CRC bytes are shifted out of the registers and onto the disk through IC16A at the appropriate time. Check/load enable (CHK/LD EN) controls the calculation or write-to-disk function while the shift register clock gate is always active during CRC operations. The clock is controlled by CRC clock enable (CRC CLK EN*).

In the read-from-disk mode, the CRC error calculations are the same as those in the write-to-disk mode. The compare function, however, is performed by inputting the 2 CRC data bytes through IC2C and synchronously shifting the 16 calculated bits (2 bytes), effectively comparing them. If the data transfer is without error, the outputs of the shift register will all be high at the end of the operation. This leaves the CRC Comparator IC14 and IC15 with a low at the CRC ERROR output. Note that in this mode, CHK/LD EN continually enables IC15C and inhibits IC16A. When the comparison is complete, the CRC CLK EN* inhibits the shift register clocks. This serves to hold the CRC ERROR signal at IC14-pin 9. This low is coupled to B7 of the PIO. The operating system can poll the PIO to check the CRC ERROR status.

CTC (Counter/Timer Circuit)

The CTC has four internal programmable counter/timer channels. Three of these are used in the WDI-II Disk Data Transfer Mode while the fourth is not used in any of the present operating modes. Channel 0, 1 and 2 counters all operate in a down counter mode. They are triggered on the disk drive outputs INDEX*, SECTOR*, and SEEK COMPLETE* respectively. Interrupts are serviced in Channel 0, 1 and 2 order. An interrupt is generated whenever one of the counters/timers reaches the zero count/time out. Channel 1 is the only channel used as a timer. In the timer mode, Channel 1 counts 250ns pulses from the $\phi 2$ clock. At the completion of the Counter 1 Timer mode, an output from TO1 (at pin 22) clocks the Formatter Enable/Start circuit which outputs the multiplex control, sending the READ or WRITE signal to the disk drive. This signal also sets up the final timing operation in the Formatter Enable/Start circuit, enabling or starting the Formatter operation. For more information refer to the individual circuit operation.

PIO (Parallel Input/Output) Controller Circuit

The PIO is a two port programmable input/output interface controller. For the WDI-II, it is programmed in the Bit Mode, meaning that each of the 16 available bits are programmed to be inputs or outputs. The inputs may be programmed to generate an interrupt if one or all of the inputs change.

NOTE: The interrupt function is not used in the current operating system control of PIO operation.

Once the PIO is programmed, it is in the data mode where it interfaces the operating system with the WDI-II circuits. The Port A bits are used primarily to control the Command/Status Bus. Port B interfaces other disk drive signals and initiates the disk data transfer operation. For more information, refer to the programming and program control information found in Chapter 4. Also refer to the circuit descriptions of related circuits in this chapter.

Command/Status Bus Circuits, PIO0 Decoder and Extended Address Latch

When addresses E0h or E1h are selected, PIO0 SEL* and A1 enable the PIO0 Decoder IC26. Note that address A1=A2=A3=0. Address E0h selects the Extended Address Latch IC52 because A0=0 (high). The RD* signal from the S-100 Bus is passed through IC26 to IC52-pin 11 and functions as the Extended Address Latch clock.

Address E1h selects the Command/Status Bus status mode. With A0=1 (low) and RD* inactive (high), a high is output to the enable input of IC39. An active signal from PIO A0 to IC19 and IC20-pins 12 completes enabling of the status mode of the Command/Status Bus circuits, allowing operating system controlled polling of disk drive status through the PIO.

Address E1h also selects the Command/Status Bus command mode. A0=1 and is therefore a low which passes RD* through IC26 to IC40-pin 11. RD* effectively functions as the clock for the Command/Status Bus command mode and is output to IC40-pin 11 as RD* continually changes state. Note that in the case of the READ and WRITE lines, gates IC44B and 44C, controlled by the Formatter Enable/Start circuit, interrupt signal flow. An active signal from PIO A0 completes enabling of the command mode and allows operating system control of the disk drive circuits. Refer to the programming and program control information in Chapter 4 for more information on the use of these gates and circuits.

Formatter Enable/Start and READ/WRITE Multiplex Circuits

When the disk data transfer mode is selected, the DISK OP output from PIO A0 is set low by the system program. This output is inverted, enabling gates IC61C and IC61D. Either the READ (from disk) or WRITE (to disk) signal is enabled. The signal is output to the appropriate circuits for control purposes.

In the Formatter Enable/Start circuit, DISK OP releases flip-flop IC47. The TO1 signal from CTC Channel 1 (8 or 12us timer) causes IC47 to output a high at Q. This enables either the READ or WRITE GATE Command/Status Bus command signal, which is immediately implemented by the disk drive. Because the Address Generator (DMA) has control of the S-100 Bus at this point, the output of IC47A is immediately applied to the D input of IC47B.

There is a delay of up to 250ns on implementation of the Formatter Enable/Start (FRMTR EN/START) signal as IC47B waits for the next $\phi 2$ clock pulse.

DISK OP is also output to the Formatter and the Control Signal Switching and Synchronizer circuits as a control signal. Refer to the descriptions of these circuits for more information. Refer also to the **Disk Data Transfer Synchronizer** paragraphs for a general discussion of the operation of these circuits during disk data transfer.

On- and Off-Board Interrupt Priorities

The interrupt (INT*) control lines of the Address Generator (DMA), CTC and PIO are all tied directly to the pINT* of the S-100 Bus. This signal indicates immediately to the system CPU that one of the above named components has issued an interrupt request. The interrupt priority on the WDI-II is established by hardwiring between the three microcircuits. Note that IEI (Interrupt Input) of the PIO is tied directly to the board IEI at J1. This means that the PIO has the highest interrupt priority on the board. IEO (Interrupt Output) of the PIO is tied to IEI of the CTC, therefore, the CTC has second priority. Since the CTC IEO is tied to the DMA IEI, it obviously has the lowest priority. Note that the IEO of the DMA is tied through a gate to the board J1 IEO line.

Circuit board interrupt priority is established in the same way as the onboard priorities. If nothing is attached to the IEI input at J1, the line is held high and the WDI-II has the highest board interrupt priority. If a connection is made to the IEI input, the board connected has higher priority. A board connected to the IEO output has lower interrupt priority.

Chapter 6

REPLACEMENT PARTS

INTRODUCTION

This chapter contains information for ordering parts. The following table is the list of replacement parts.

Part locations can be found by referring to Figure 6-1, WDI-II Component Location Diagram.

ORDERING INFORMATION

To order a part listed in the replacement parts list, include the Cromemco part number, the description and the quantity required. All parts may be ordered through your Cromemco dealer. Most of the parts are also available through the manufacturer.

Parts List

Designation	Description	Cromemco Part No.
Integrated Circuits		
IC1	7406	010-0028
IC2	74LS86	010-0052
IC3	74LS08	010-0064
IC4	74LS74	010-0055
IC5	74LS02	010-0068
IC6	(non TI) 74LS04	010-0066
IC7-8	74LS161	010-0044
IC9	74S260	010-0094
IC10	74LS163	010-0128
IC11	74LS161	010-0044
IC12	74109	010-0013
IC13	74LS74	010-0055
IC14	74LS133	010-0327
IC15	74LS21	010-0060
IC16	74LS00	010-0069
IC17	75110	010-0175
IC18	75107	010-0176
IC19-20	75138	010-0194
IC21	74LS32	010-0058
IC22	74LS00	010-0069
IC23	74LS74	010-0055
IC24	74LS02	010-0068
IC25	7905/320T-5	012-0000
IC26	74LS139	010-0118
IC27	74LS175	010-0042
IC28	74LS157	010-0046
IC29	74LS367	010-0108
IC30	Z80A-CTCAPS	011-0038
IC31	74933	502-0033
IC32	74LS273	010-0107
IC33	74LS32	010-0058
IC34-35	74LS273	010-0107
IC36	(non TI) 74LS04	010-0066
IC37	74LS273	010-0107
IC38	74LS374	010-0133
IC39	74LS373	010-0102
IC40	74LS273	010-0107
IC41	74LS27	010-0112
IC42	Z80A-PIOAPS	011-0039
IC43	Z80A-DMAAPS	011-0041
IC44	74LS08	010-0064
IC45	74166	010-0238
IC46	74164	010-0007
IC47	74LS74	010-0055

Designation	Description	Cromemco Part No.
IC48	74LS367	010-0108
IC49-50	7805/340T-5	012-0001
IC51	74LS244	010-0100
IC52	74LS374	010-0133
IC53	7406	010-0028
IC54	74LS20	010-0095
IC55	(non TI) 74LS04	010-0066
IC56-57	74LS244	010-0100
IC58-59	74LS245	010-0120
IC60	74LS244	010-0100
IC61	74LS00	010-0069
IC62	74LS86	010-0052
IC63	(non TI) 74LS04	010-0066
IC64	74LS00	010-0069
Transistors		
Q1	2N3640	009-0023
Q2-3	2N3646	009-0000
Q4	2N3906	009-0002
Capacitors		
C1	10 uf tant	004-0032
C2	30 pf disk	004-0003
C3	220 pf disk	004-0013
C4-26	.047 uf axial	004-0061
C27	10 uf tant	004-0032
C28-31	.047 uf axial	004-0061
C32	33 pf disk	004-0048
C33-34	.047 uf axial	004-0061
C35	10 uf tant	004-0032
C36-39	.047 uf axial	004-0061
C40	47 pf mono	004-0000
C41-42	.047 uf axial	004-0061
C43	6.8 uf tant	004-0034
C44	10 uf tant	004-0032
Resistors		
R1	1 K	001-0018
R2	100	001-0007
R3	180	001-0009
R4	120	001-0073
R5	22	001-0001
R6-7	470	001-0014
R8	22	001-0001

Designation	Description	Cromemco Part No.
R9	240	001-0072
R10-11	1 K	001-0018
R12	100	001-0007
R13	1 K	001-0018
R14	560	001-0015
R15-21	4.7 K	001-0024
R22	100	001-0007
Resistor Networks		
RN1	56, 8 pin	003-0038
RN2-4	220/330, 8 pin	003-0037
RN5	1K, 10 pin	003-0058
RN6	4.7K, 8 pin	003-0009
RN7	220/330, 8 pin	003-0037
Miscellaneous		
	1 header, 34 pin	017-0249
	2 sockets, 40 pin	017-0006
	1 socket, 28 pin	017-0071
	2 sockets, 16 pin	017-0002
	1 socket, 2 pin	017-0009
	2 2-56X3/8 screw	015-0003
	4 6-32X1/2 screw	015-0044
	1 6-32X1/2 nylon screw	015-0108
	1 nylon washer, white	015-0024
	5 6-32 hex nut	015-0013
	2 2-56 hex nut	015-0014
	5 #6 lock washers	015-0020
	1 large heat sink	021-0017

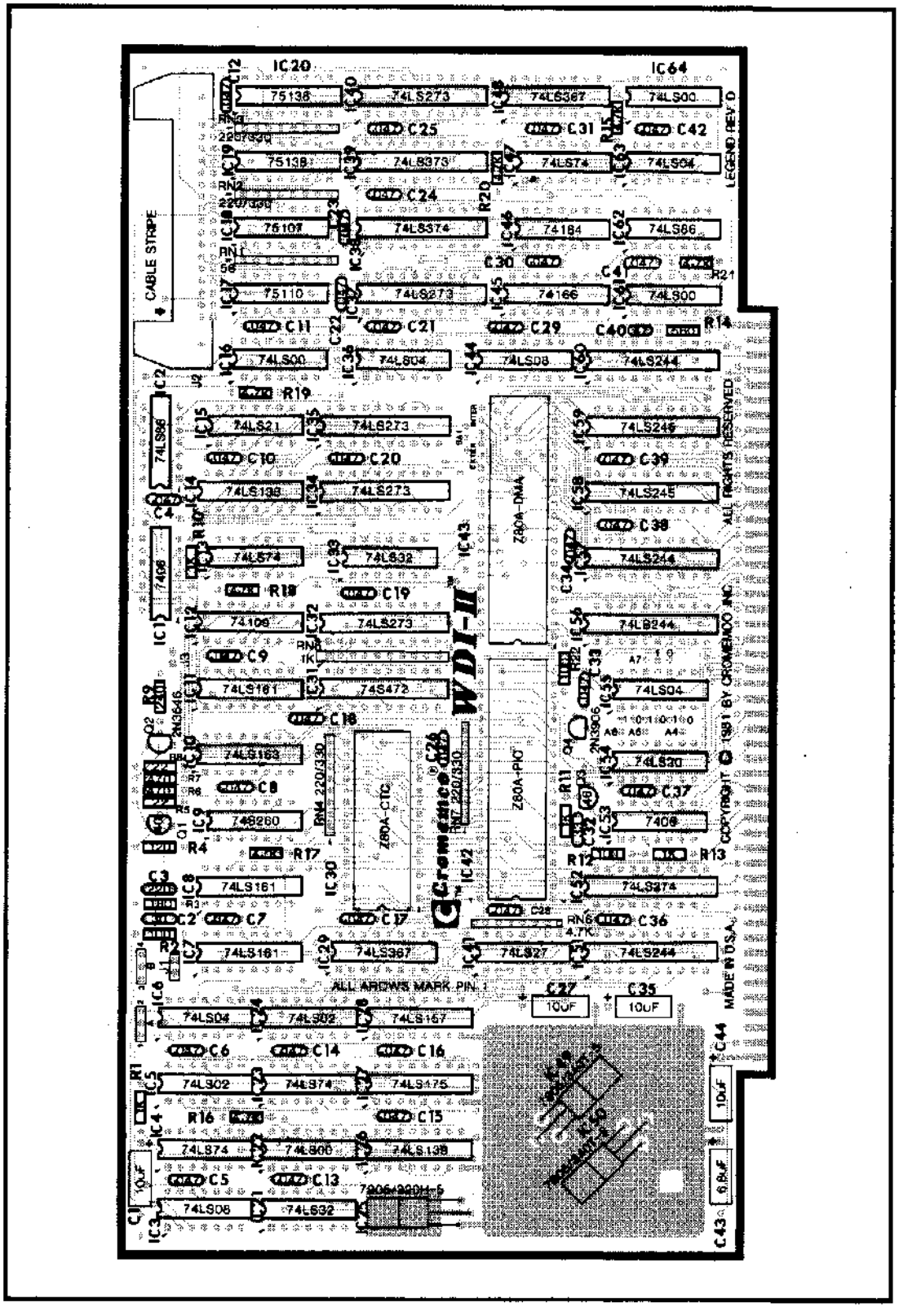


Figure 6-1: WDI-II COMPONENT LOCATION DIAGRAM

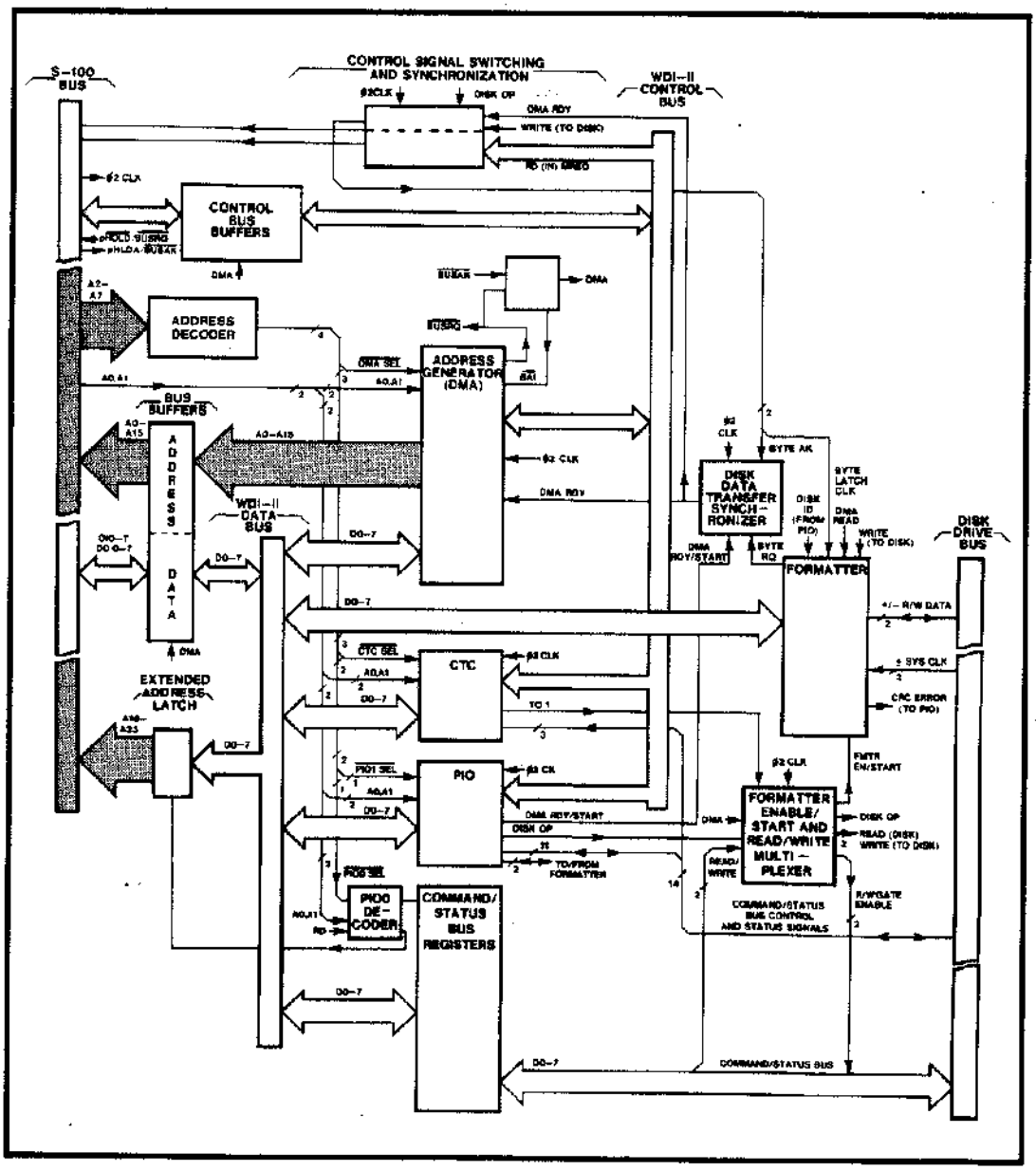


Figure A-1: WDI-II BLOCK DIAGRAM

Appendix B
LIMITED WARRANTY

Cromemco, Inc. ("Cromemco") warrants this product against defects in material and workmanship to the original purchaser for ninety (90) days from the date of purchase, subject to the following terms and conditions.

What Is Covered By This Warranty

During the ninety (90) day warranty period Cromemco will, at its option, repair or replace this Cromemco product or repair or replace with new or used parts any parts or components, manufactured by Cromemco, which prove to be defective, provided the product is returned to an Authorized Cromemco Dealer as set forth below.

How To Obtain Warranty Service

You should immediately notify IN WRITING your Authorized Cromemco Dealer or Cromemco Inc of problems encountered during the warranty period. In order to obtain warranty service, first obtain a return authorization number by contacting the Authorized Cromemco Dealer from whom you purchased the product. Then attach to the product:

1. Your name, address and telephone number,
2. the return authorization number,
3. a description of the problem, and
4. proof of the date of retail purchase.

Ship or otherwise return the product, transportation and insurance costs prepaid, to the Authorized Cromemco Dealer. If you are unable to receive warranty repair from the Authorized Cromemco Dealer from whom you purchased the product, you should contact Cromemco Customer Support at: Cromemco, Inc., 280 Bernardo Ave., Mountain View, Ca. 94043.

What Is Not Covered By This Warranty

Cromemco does not warrant any products, components or parts not manufactured by Cromemco.

This warranty does not apply if the product has been damaged by accident, abuse, misuse, modification or misapplication; by damage during shipment; or by improper service. This product is not warranted to operate satisfactorily with peripherals or products not manufactured by Cromemco. Transportation and insurance charges incurred in transporting the product to and from the Authorized Cromemco Dealer or Cromemco are not covered by this Warranty.

THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER ORAL OR WRITTEN, EXPRESS OR IMPLIED. ANY IMPLIED WARRANTIES, INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO NINETY (90) DAYS FROM THE DATE OF PURCHASE OF THIS PRODUCT. CROMEMCO SHALL NOT BE LIABLE FOR INCIDENTAL AND/OR CONSEQUENTIAL DAMAGES FOR THE BREACH OF ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING DAMAGE TO PROPERTY AND, TO THE EXTENT PERMITTED BY LAW, DAMAGES FOR PERSONAL INJURY, EVEN IF CROMEMCO HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. SOFTWARE, TECHNICAL INFORMATION AND FIRMWARE IS LICENSED "AS IS" AND WITH ALL FAULTS. THE AGENTS, DEALERS, AND EMPLOYEES OF CROMEMCO ARE NOT AUTHORIZED TO MAKE MODIFICATIONS TO THIS WARRANTY, OR ADDITIONAL WARRANTIES BINDING ON CROMEMCO ABOUT OR FOR PRODUCTS SOLD OR LICENSED BY CROMEMCO. ACCORDINGLY, ADDITIONAL STATEMENTS WHETHER ORAL OR WRITTEN EXCEPT SIGNED WRITTEN STATEMENTS FROM AN OFFICER OF CROMEMCO DO NOT CONSTITUTE WARRANTIES AND SHOULD NOT BE RELIED UPON.

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES OR LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATION OR EXCLUSION MAY NOT APPLY TO YOU.

THIS WARRANTY AND THE STATUTE OF LIMITATIONS SHALL RUN CONCURRENTLY WITH ANY ACCEPTANCE PERIOD. THIS WARRANTY IS NOT TRANSFERABLE. NO SUIT, LITIGATION, OR ACTION SHALL BE BROUGHT BASED ON THE ALLEGED BREACH OF THIS WARRANTY OR IMPLIED WARRANTIES MORE THAN ONE YEAR AFTER THE DATE OF PURCHASE IN THOSE JURISDICTIONS ALLOWING SUCH A LIMITATION, OTHERWISE NO SUCH ACTION SHALL BE BROUGHT MORE THAN ONE YEAR AFTER THE EXPIRATION OF THIS WARRANTY.

THIS WARRANTY SHALL NOT BE APPLICABLE TO THE EXTENT THAT ANY PROVISION OF THIS WARRANTY IS PROHIBITED BY ANY FEDERAL, STATE OR MUNICIPAL LAW WHICH CANNOT BE PREEMPTED. THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS WHICH VARY FROM STATE TO STATE.

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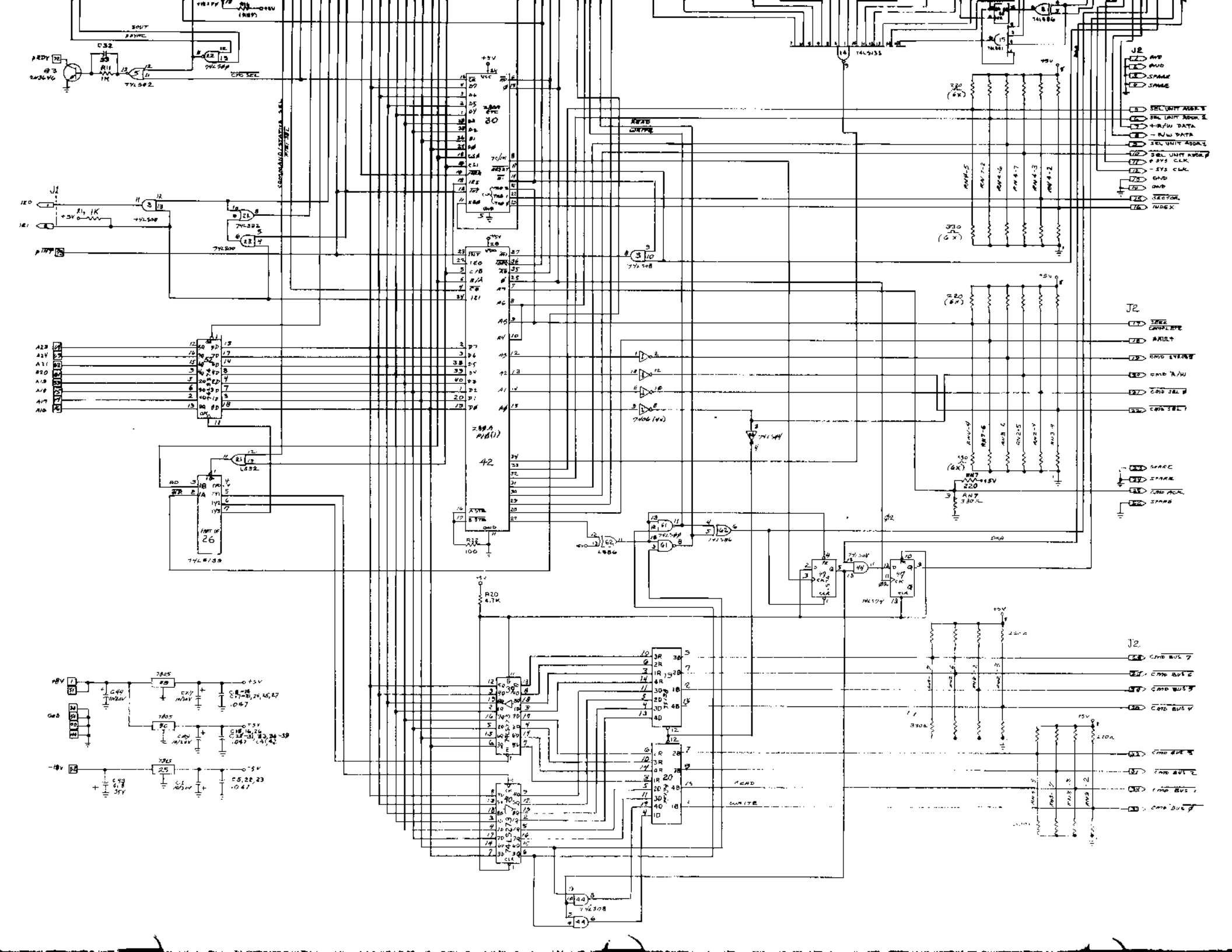

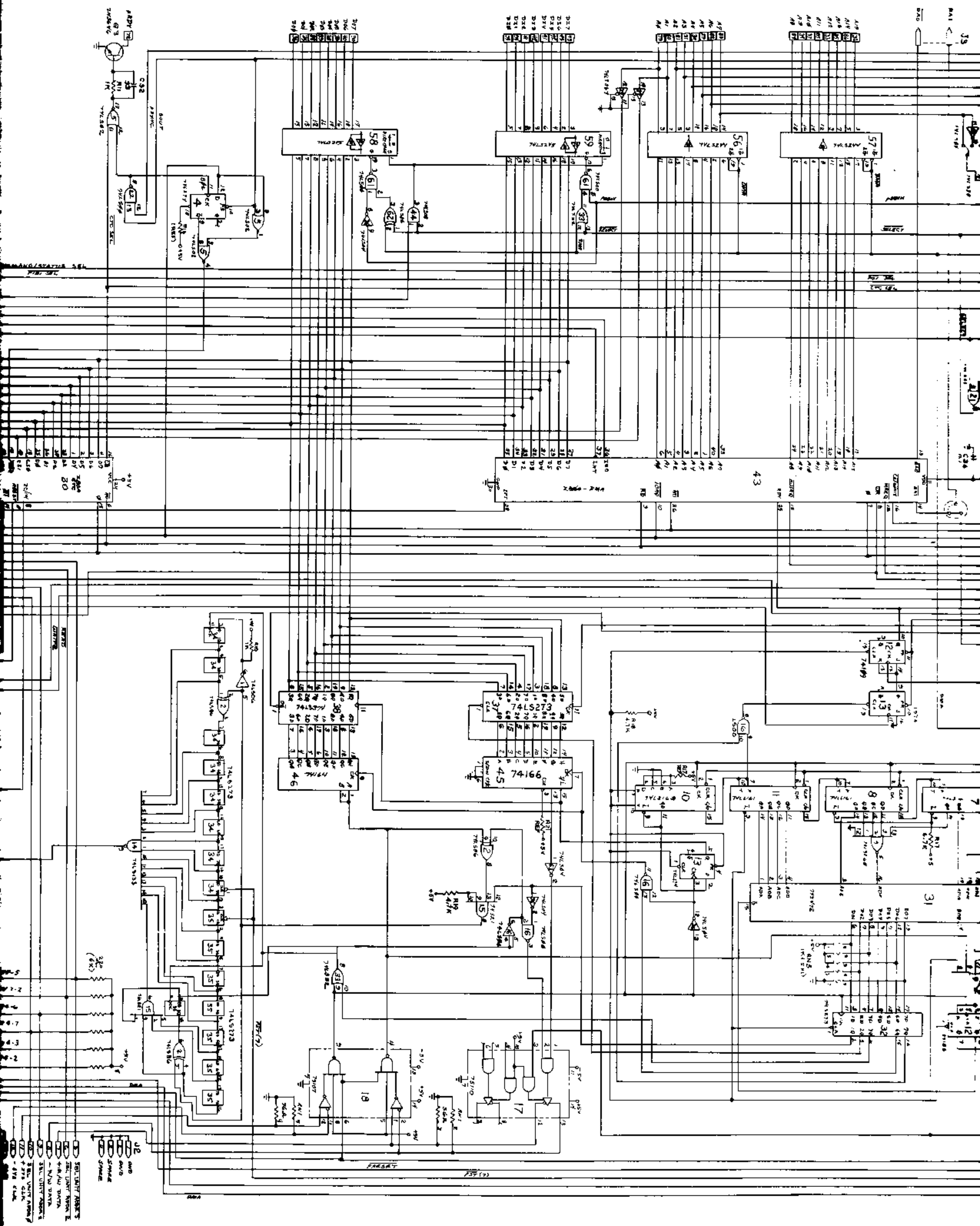
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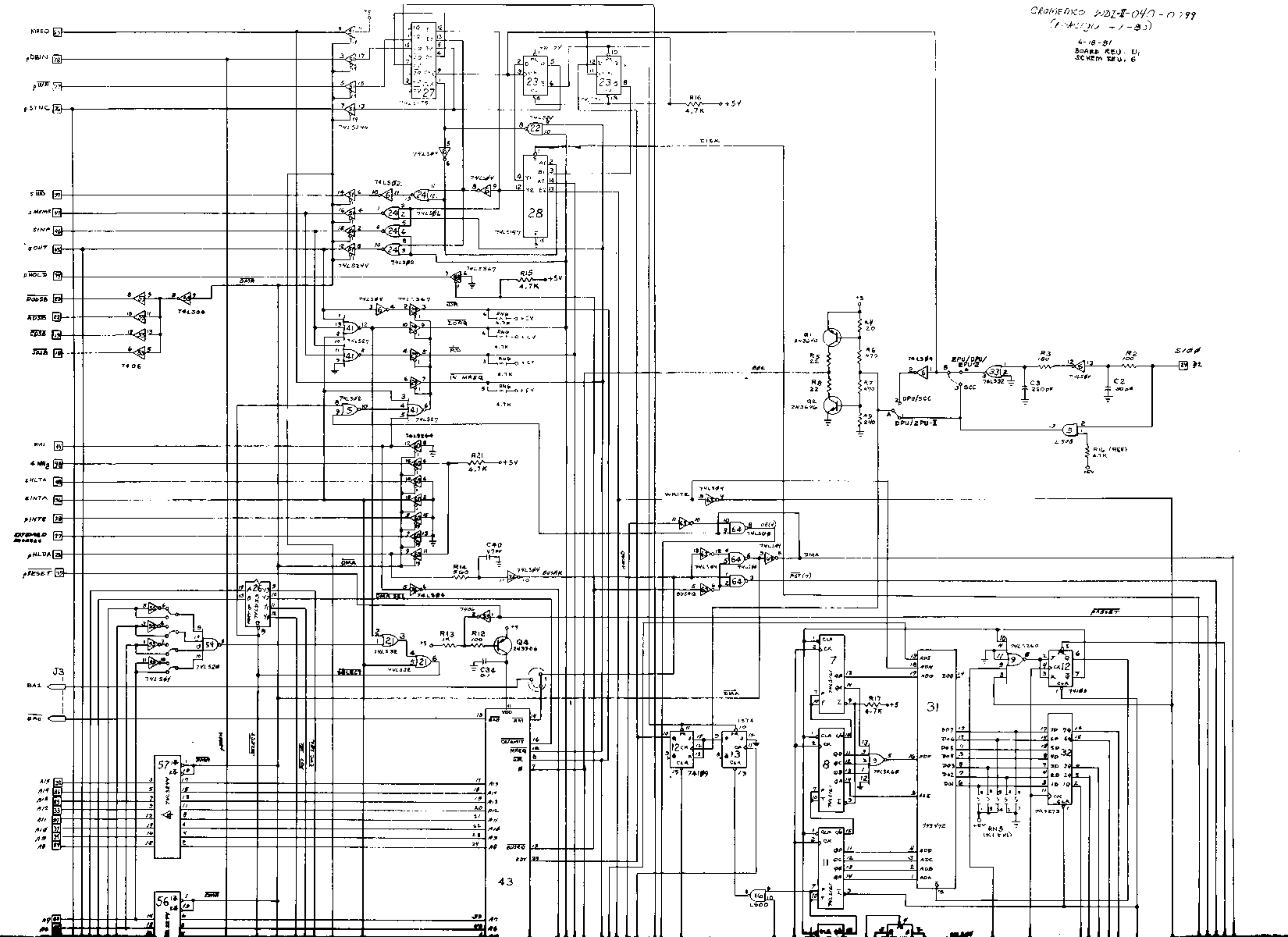
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