Twenty Dollars

Cromemco

48KTP

Two Port Memory

Instruction Manual

Cromemco™

48KTP Two Port Memory

INSTRUCTION MANUAL

THIS BOARD IS NOT INTENDED FOR USE AS A SYSTEM MEMORY BOARD

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1. INTRODUCTION

The Cromemco model 48KTP Two Port Memory board is specially designed for use with Cromemco systems employing a model SDI graphics interface. Together with a high resolution RGB color monitor such as the Cromemco RGB-19, these boards turn any Cromemco microcomputer into a highly sophisticated graphics system with features unparalleled in the industry.

One or two 48KTP RAM boards can be added to each SDI system as a means of storing picture information. Each 48KTP is capable of storing an entire 48K nybble-mapped or bit-mapped image. The 48KTP is not, however, designed to store SDI images in 12K format.

The basic SDI system configuration without the 48KTP RAM boards is shown in Figure 1.

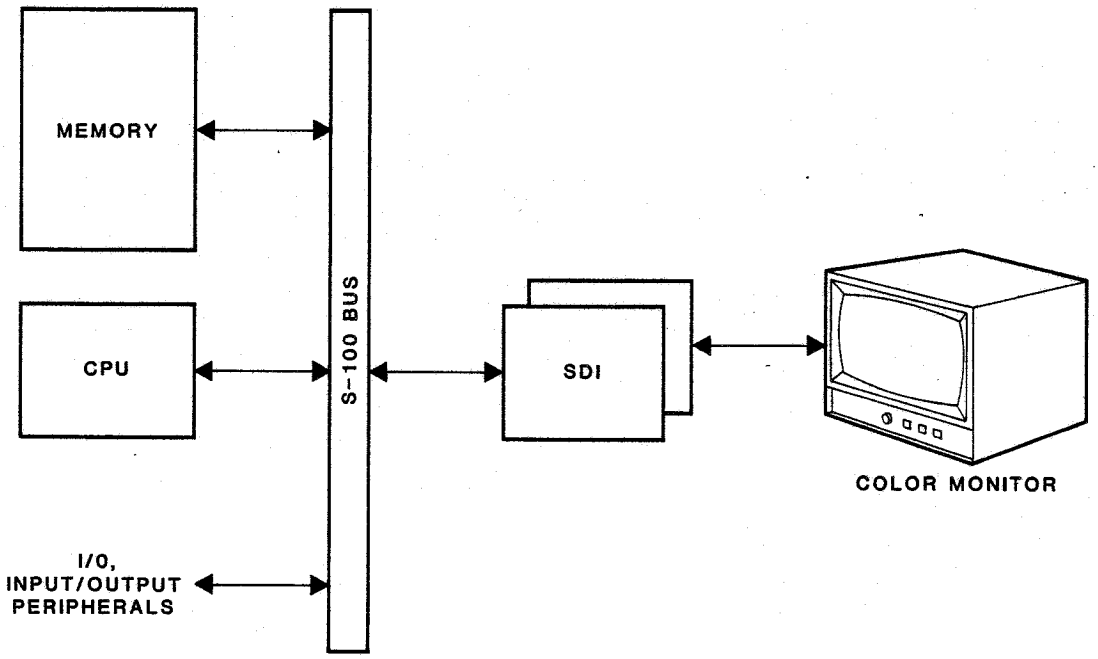


Figure 1 - The Basic SDI System

In this configuration the SDI scans main memory for a digitized image. When reading the picture information from main memory, the SDI must disable the ZPU for a large percentage (up to 92%) of the time. This greatly reduces execution efficiency because the ZPU must share the S-100 address and

data bus lines with the SDI.

This situation is remedied with the 48KTP. The 48KTP has two sets of address and data lines (two ports) which give it the ability to process the SDI's memory refresh requests while the ZPU simultaneously and independently executes a user program. The **second port** of the 48KTP is a 50 pin connector on the top edge of the card. This allows a direct connection of the SDI with the 48KTP which bypasses the S-100 bus. The ZPU accesses the 48KTP through the S-100 bus (the **main port**) as though the SDI were not present.

One or two 48KTP boards can be employed in a single SDI system. The system configuration with two 48KTPs is shown in Figure 2.

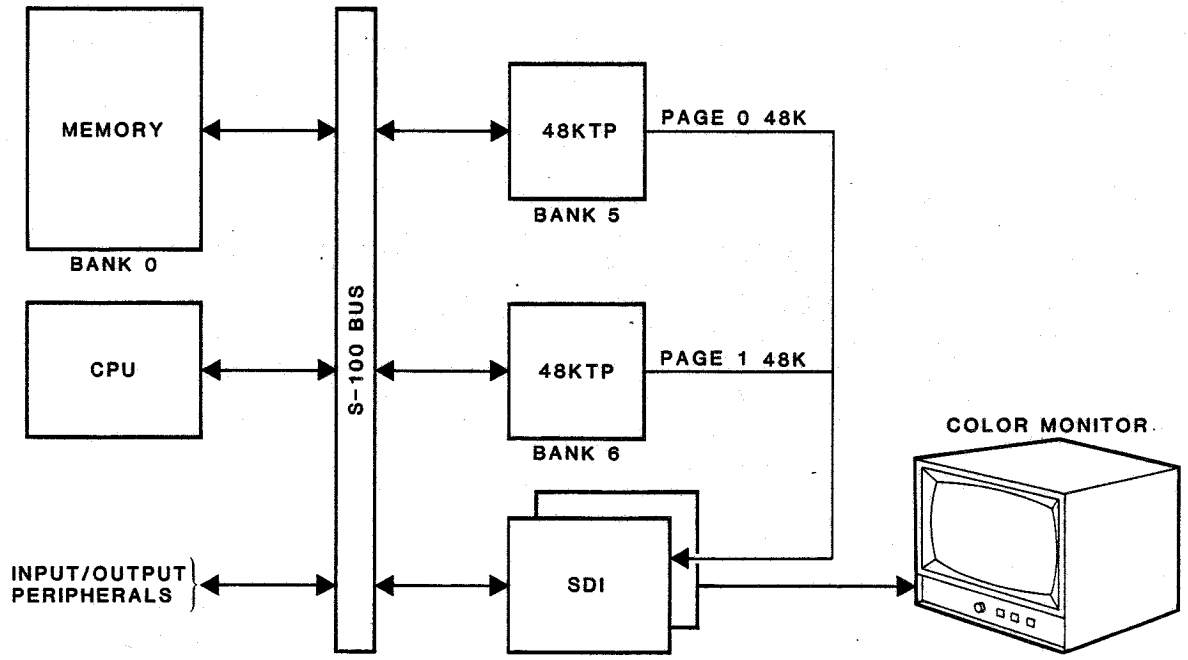


Figure 2 - An SDI System with Two 48KTP Boards

2. BOARD DESCRIPTION

The 48KTP is a two port dynamic memory board. It incorporates 4116 (16K x 1) dynamic RAM chips (or the equivalent) into its main 48K block of user memory. Also on board is all the logic necessary to service read and write requests from the host (S-100 bus) and read requests from the SDI (second port). More technical information can be found in the section on General Theory of Operation.

The 48KTP contains two external connectors on the edge opposite the S-100 plug. These connectors, a 50 pin connector and 26 pin connector, allow a **top edge** interface to the SDI. By connecting the 48KTP to the SDI-D with 50 and 26 conductor ribbon cables, data and timing information can be communicated between the two boards. The address requests to the 48KTP as well as the picture data to the SDI are passed via the 50 conductor cable. Timing information is supplied to the 48KTP by the SDI-D through the 26 conductor cable.

There are 2 switch groups on board the 48KTP. SW-2 indicates to the host which banks the 48KTP appears in. SW-1 establishes information regarding the relationship between the 48KTP and the SDI as well as address information and other features. One bit on this switch, for example, determines which page of image memory the 48KTP occupies with respect to the SDI. The SDI can support two 48K pages, page 0 and page 1. The selection of frame buffer page is independent of bank selection.

3. STANDARD SYSTEM CONFIGURATION & INSTALLATION

For most applications (and in particular when using Cromemco software) a standard system configuration with regard to bank placement and switch settings should be observed. In this configuration, the main user bank (hereafter referred to as host memory) appears in bank 0. If one page of 48KTP memory is used it should appear in bank 5 and from the point of view of the SDI appear as page 0. If a second page of 48KTP memory exists, this board should be set to bank 6 and appear to the SDI as page 1. Both 48KTP boards (if two are present) should be addressed from 4000H to FFFFH, i.e., the upper 48K of memory. Finally, because of the 48KTP's special memory disable feature, the host bank, bank 0, should be set to appear also in bank 5, if one 48KTP is present, or banks 5 and 6, if two 48KTP's are present. This apparent memory overlap is allowed because the 48KTP disables all memory which lies in its bank and memory block while the 48KTP is being written into. This system configuration is summarized in Figure 3 and Table 1. The switch settings for this configuration are shown in Figure 4.

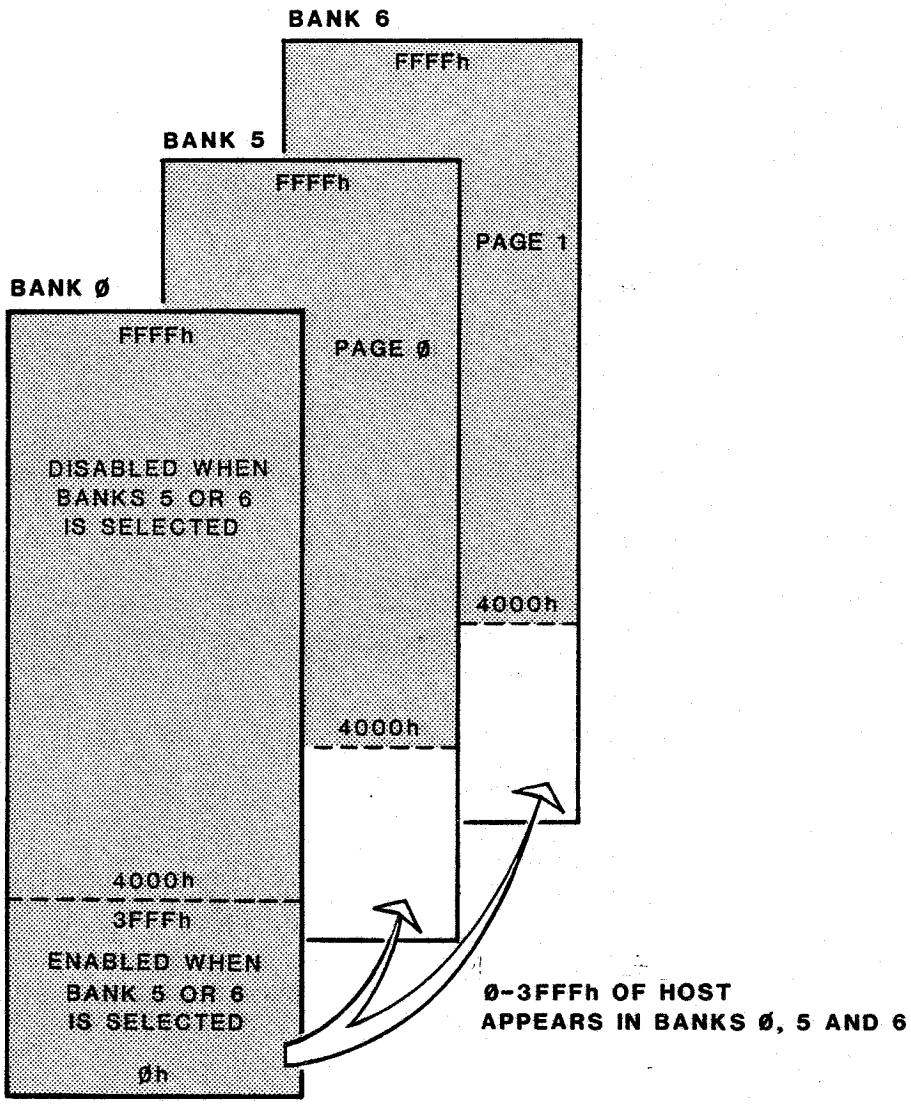


Figure 3 - System with Two 48KTPs

Table 1
Standard System Configuration with Two 48KTPs

	Size	Appears in banks:	Addressed as:	Appears to SDI as:
Host memory	64K	0,5,6	0-FFFFh	------
1st 48KTP	48K	5	4000h-FFFFh	page 0
2nd 48KTP	48K	6	4000h-FFFFh	page 1

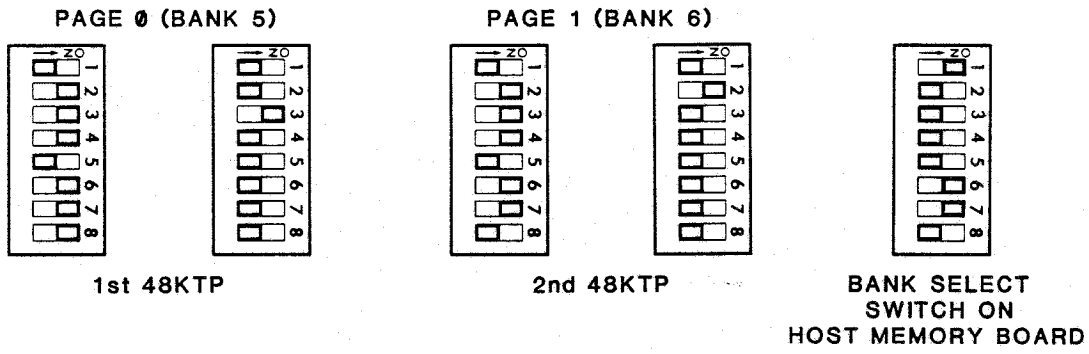


Figure 4 - Switch Settings

From the point of view of the graphics programmer, the host memory from 4000h to FFFFh will appear only in bank 0. Thus, when it is necessary to switch to bank 5 or bank 6 in order to manipulate the image memory, that portion of the program which handles the bank select and subsequent image manipulation must be located in host memory below 4000h. This is because host addresses 0-3FFFh appears in banks 5 and 6 also, so that when these banks are selected any program segment which appears in this address range will continue to operate. A typical organization of software for the SDI/48KTP system is shown in Figure 5.

Installation of the 48KTP

1. Verify that the SDI board set is properly installed in the system (see SDI manual for switch settings and installation instructions). Make sure that the SDI-D has two vacant board slots adjacent it on its side opposite the DMA-V.

2. Copy the switch settings of figure 4 onto the (both) 48KTP and also onto the bank select switch of the host memory card(s).

3. Connect 1 plug of a 50 pin ribbon cable to connector J-1 of the 48KTP, leaving the other plug free. If two 48KTP's are present, use a single cable/3 plug ribbon connector and plug this cable into each 48KTP leaving the third plug free.

4. In a similar fashion as step 3 connect a 26 conductor ribbon cable to one or both 48KTP connector J-2, leaving an end free.

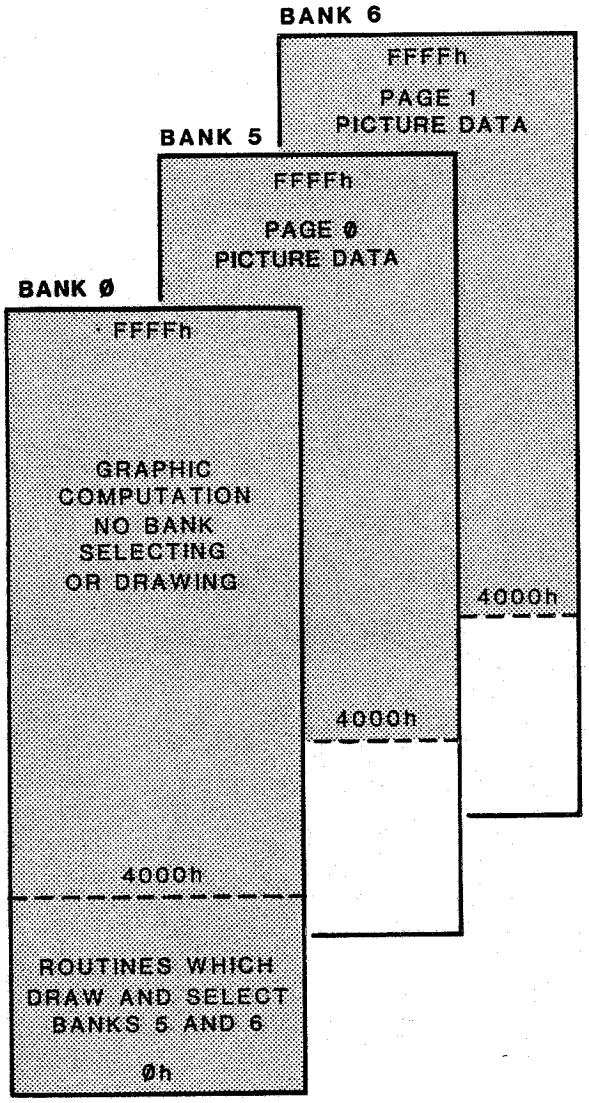


Figure 5 - Organization of the SDI and 48KTP

5. Insert both 48KTPs into the system in the vacant slots adjacent the SDI-D board, with the free cable ends toward the SDI-D.

6. Plug the 50 conductor cable free end into connector J-2 of the SDI-D, and the 26 conductor cable free end into connector J-4 of the SDI-D.

The 48KTP boards are now installed in the system. The system card cage will appear as in Figure 6.

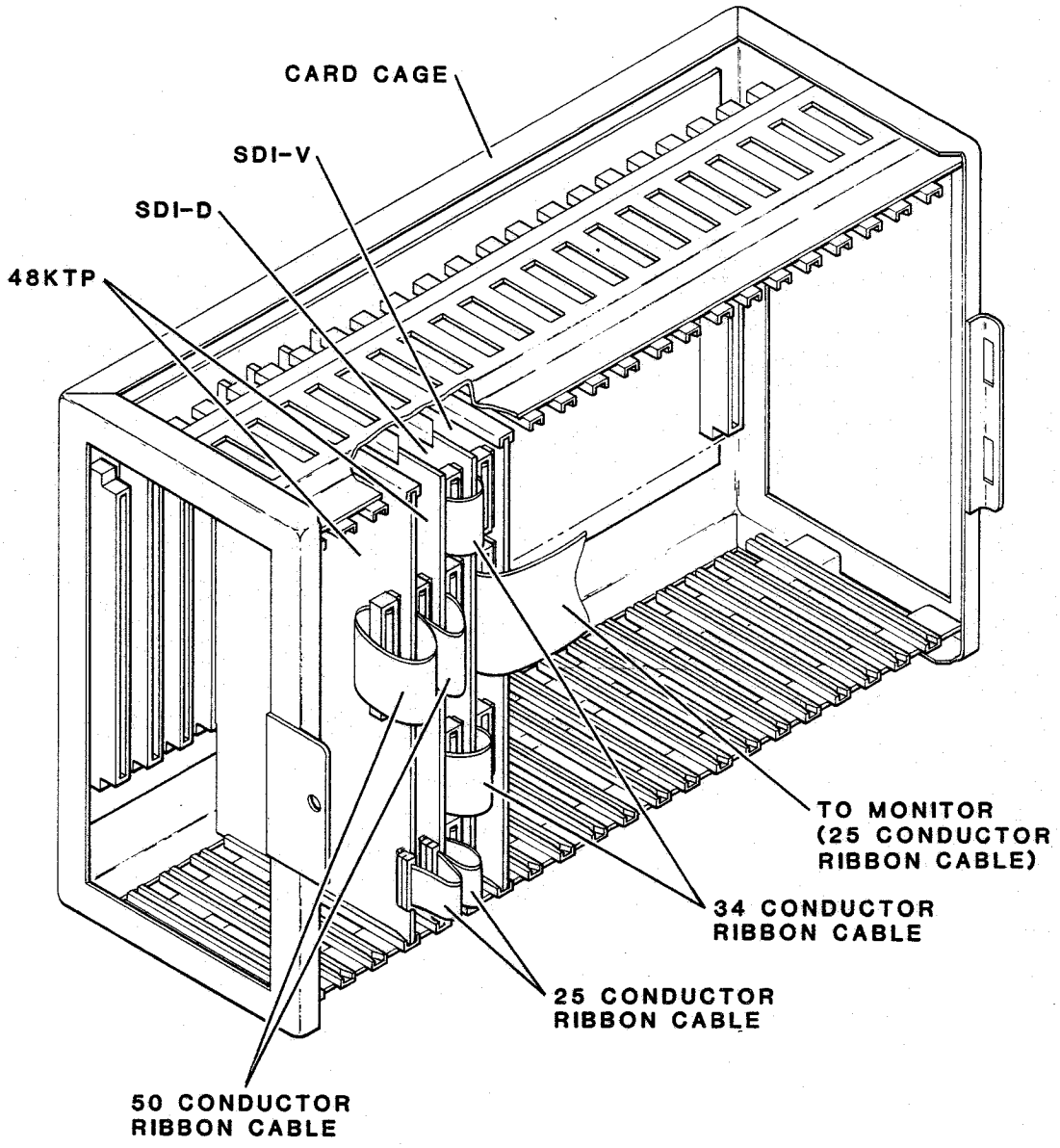


Figure 6 - SDI and 48KTPs in Card Cage

4. SWITCH SETTINGS

This section describes the use of each 48KTP switch in detail. Reference is made to the previous section if a standard Cromemco graphics system configuration is employed. An outline of the 48KTP board showing the location of the 2 switch groups is shown in Figure 7.

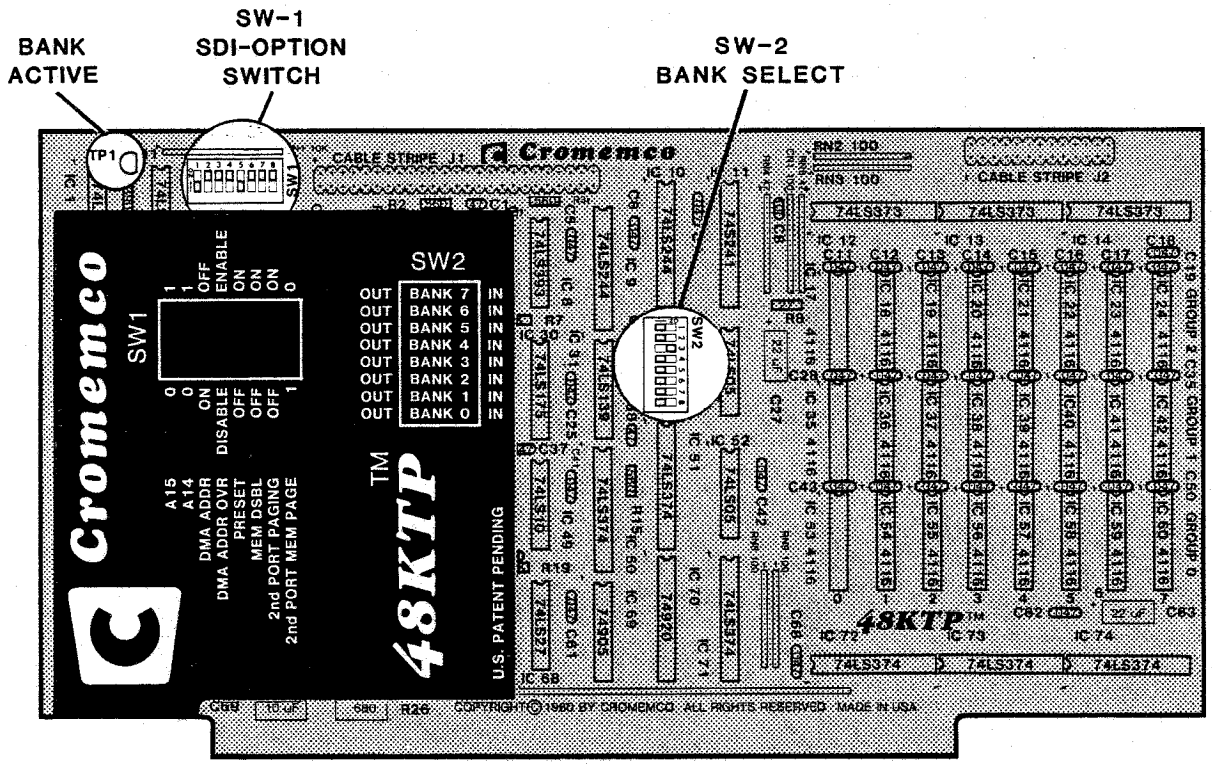


Figure 7 - 48KTP Switch Locations

Switch Group SW-1

Bits 1 and 2 (A15 and A14): These bits determine the base address of the 48KTP. Normally their setting is:

A15 = 0
A14 = 1

indicating a base address of 4000h. The 48KTP then appears from 4000h to FFFFh. If set to base address 0, the 48KTP will appear from 0h to BFFFh.

The base address of the 48KTP can be on any 16K boundary . If the base address is such that not all of the 48K can fit in the available memory above the base address (i.e., [FFFFh - base] < 48K), the remainder will wrap around to 0 and continue from that point. As an example, consider the case in which the base address is set to 8000h. The picture information will start at 8000h (left side of

image) and be stored in consecutive locations, increasing to the top of memory, and wrapping around so that the last portion of picture information (right side of image) will be stored in memory from 0 to 4000h. Refer to Figure 8.

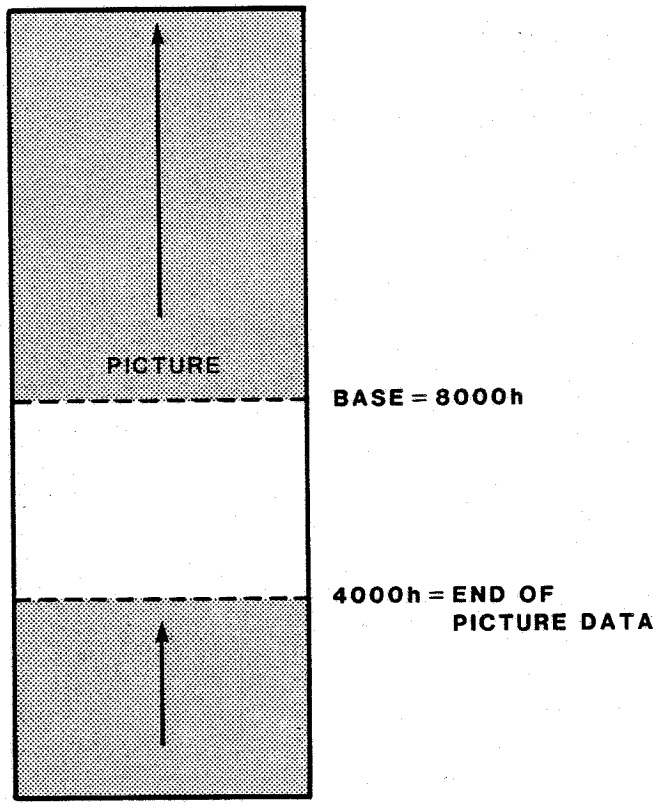


Figure 8 - "Wrap Around" Base Address

Bits 3 and 4 (host DMA controls): The recommended setting of these switches is bit 3 = off and bit 4 = on. In this case the 48KTP ignores **all** host DMA requests regardless of bank.

Two alternative situations which one might desire are:

1) 48KTP responds to a host DMA request if it is in the selected bank, otherwise it will not respond. (bit 3 = off, bit 4 = off).

2) 48KTP responds to **all** host DMA requests regardless of bank (bit 3 = on, bit 4 = on).

These possibilities are summarized in Table 2.

Table 2 - Host DMA Options

Bit 4 DMA override enable	Bit 3 DMA on/off	Effect
Off	No Effect	48KTP behaves like "normal" host memory
On	Off	48KTP ignores all host DMA requests (Recommended)
On	On	48KTP responds to all host DMA requests

Bit 5 (preset): if this switch is on, the 48KTP will be active after reset. If off, the board will be off (unselected). **Off** is the standard position for this switch.

Bit 6 (phantom enable): this bit controls the ability of the 48KTP to disable memory which resides in the same bank. If phantom enable is on, then a host read or write request to the 48KTP will cause the S-100 MEMDISBL line to become active. This will disable all other memory boards from being accessed by the host. Note that the following Cromemco boards do not have the MEMDISBL feature: old 8KBS, 4KZ, and 16KPR. This switch allows memory overlap in banks 5 and 6 (the "dual port banks") which is unavoidable if a 64KZ RAM board is used for page 0 host memory. When this switch is in the "off" position, no MEMDISBL pulse is generated. In such cases, a portion of the host memory **must** be configured in 16K or smaller blocks. The 16K block which does not overlap the 48KTP addressing (usually 0-3FFFh), must be set to banks 0 **and** 5 (and/or 6). This assures that some program memory will still be visible to the ZPU after a bank 5 (or 6) selection is made. All other host memory which does overlap the 48KTP addressing (usually from 4000h to FFFFh) must be in bank 0 **only.**

Bits 7 and 8 (second port paging): in order to have the 48KTP respond to a **particular** page request from the SDI, bit 7, page enable, must be in the "on" position. If bit 7 is in the "off" position, the 48KTP will not differentiate between page 0 and page 1 requests and thus respond to all 48KTP accesses which emanate from the second port.

When bit 7 is in the "on" position the 48KTP will respond to either page 0 access or page 1 access from the second port (SDI). The determination of which page the RAM responds to is fixed by bit 8 - page 0 or 1. Page 0 is selected by bit 8 in the on position. Page 1 is selected by bit 8 in the off position.

Switch Group S-2

This switch group determines the bank(s) in which the 48KTP resides. Normally the 48KTP making page 0 will be in bank 5, and the 48KTP making page 1 will be in bank 6. The bank-switch correspondence is shown in Table 3.

Table 3

Switch Number	Bank
1	7
2	6
3	5
4	4
5	3
6	2
7	1
8	0

5. CONNECTIONS BETWEEN THE 48KTP AND SDI

The 48KTP contains provisions for 2 separate cable connections to the SDI. The two pin groups on the card edge, labelled J-1 and J-2 are shown in Figure 9.
The connector J-1 is the main data and address transmission line to the SDI. The SDI sends address requests to the 48KTP through this connection, and the 48KTP responds by sending data back to the SDI, also through J-1. Since some of the address information is simulated on board the 48KTP, address lines EA0 to EA7 are used by the

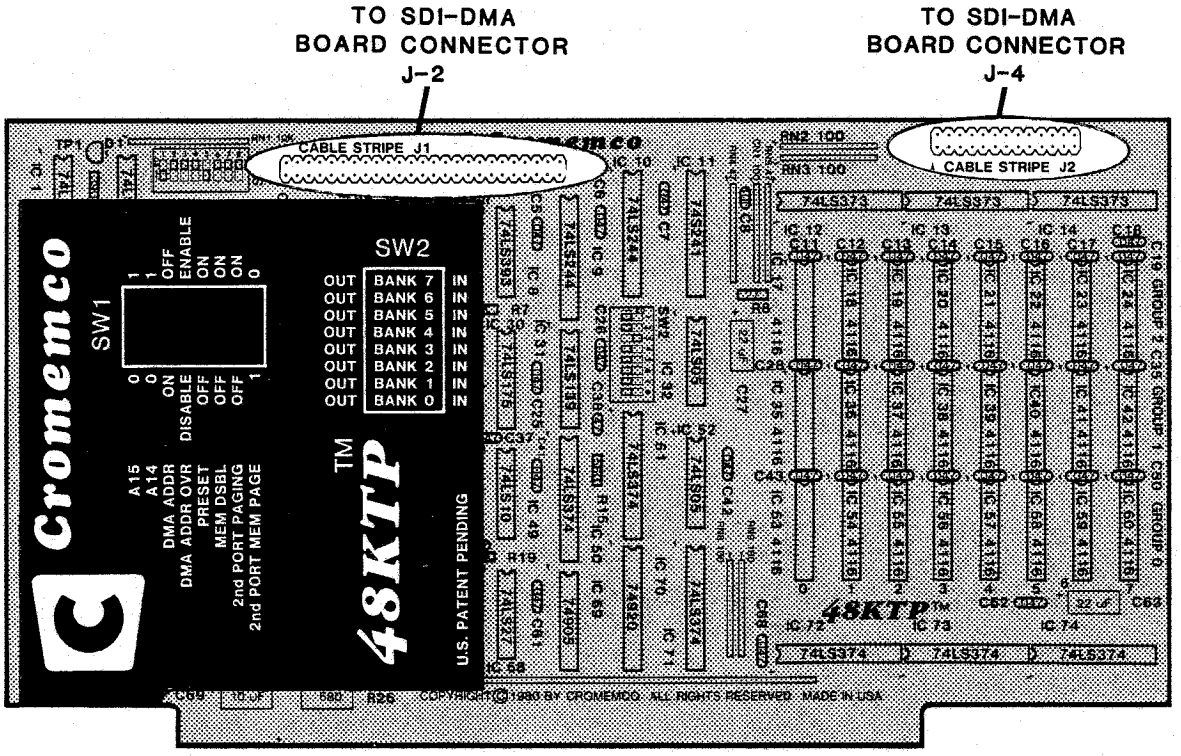


Figure 9 - Cable Connections to the 48KTP

48KTP. The details are shown in Figure 10.

The connector J-2 supplies the 48KTP with two timing signals from the SDI: HG, the horizontal gate, and QCK the 14.31818 mhz (NTSC) or 17.734479 mhz (P.A.L.) clock which drives the entire graphics interface.

6. GENERAL THEORY OF OPERATION

The 48KTP is a Two Port dynamic memory board. It consists of three 16K x 8 bit sections which are built from 4116 (or equivalent) 16K x 1 dynamic memory chips. The 48KTP has an access time of 250 nsec and a cycle time of 405 nsec. The SDI shares cycles with the host (ZPU) so that every other 405 nsec cycle is dedicated to the SDI, while the remaining cycles are dedicated to the host. Figure 11 shows the waveform generated by an on board Johnson Counter.

J-1 PIN DESCRIPTION*

1.	}	2.	}
3.	}	4.	} N.C.
5.	} N.C.	6.	}
7.	}	8.	}
9.	}	10.	GND
11.	EDI0	12.	EDI1
13.	EDI2	14.	EDI3
15.	EDI4	16.	EDI5
17.	EDI6	18.	EDI7
19.	GND	20.	EA0
21.	EA1	22.	EA2
23.	EA3	24.	EA4
25.	EA5	26.	EA6
27.	EA7	28.	}
29.	}	30.	}
31.	}	32.	}
33.	}	34.	} N.C.
35.	} N.C.	36.	}
37.	}	38.	}
39.	}	40.	}
41.	ER0	42.	ER1
43.	ER2	44.	}
45.	PG1	46.	} N.C.
47.	} N.C.	48.	}
49.	}	50.	GND

*Key:

EDI = data, EA = address, ER = read, PG1 = page 1, GND = ground, N.C. = no connection.

J-2 PIN DESCRIPTION

1.	}	2.	QCK
3.	} GND	4.	} N.C.
5.	}	6.	}
7.	}	8.	HG
9.	} N.C.	10.	}
11.	}	12.	}
13.	}	14.	}
15.	GND	16.	} N.C.
17.	N.C.	18.	}
19.	GND	20.	}
21.	GND	22.	}
23.	} N.C.	24.	}
25.	}	26.	GND

Figure 10 - Second Port Connections

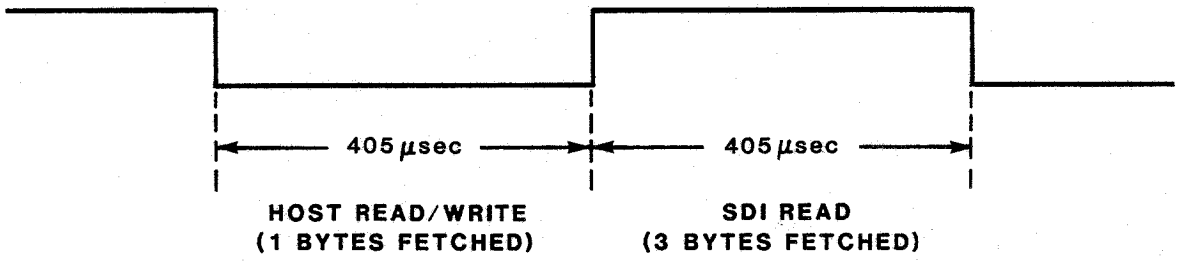


Figure 11 - Johnson Counter - I.C. 16, pin 15

This counter, which has a period of 810 nsec and a 50% duty cycle divides the memory cycles into second port cycles and main port (S-100) cycles. When the Johnson Counter (I.C. 16, pin 15) is low, the host has access to the RAM through main port. When this pin is high, the SDI reads via the second port.

SECOND PORT READ

During the 405 nsec cycle which is dedicated to the SDI, a memory read through the second port takes place. The address for this read is defined by a combination of an on board address simulator/refresh counter and address bits EA0-EA7 supplied to the board from the SDI. Please refer to Figure 12. EA1-EA7 determine CAS for second port read. RAS for second port read is determined by the address simulator along with bit EA0 from the SDI. Together, the address simulator and bit A0 also serve to refresh the dynamic RAM on the 48KTP. One complete cycle of the address simulator generates addresses for a single horizontal scan (1 HG pulse). Then, with bit EA0 acting as the MSB of RAS, the complete RAS cycle of 256 locations is cycled through every 2 HG pulses (127 usec). This is well within the required refresh time of the 4116 RAM chips.

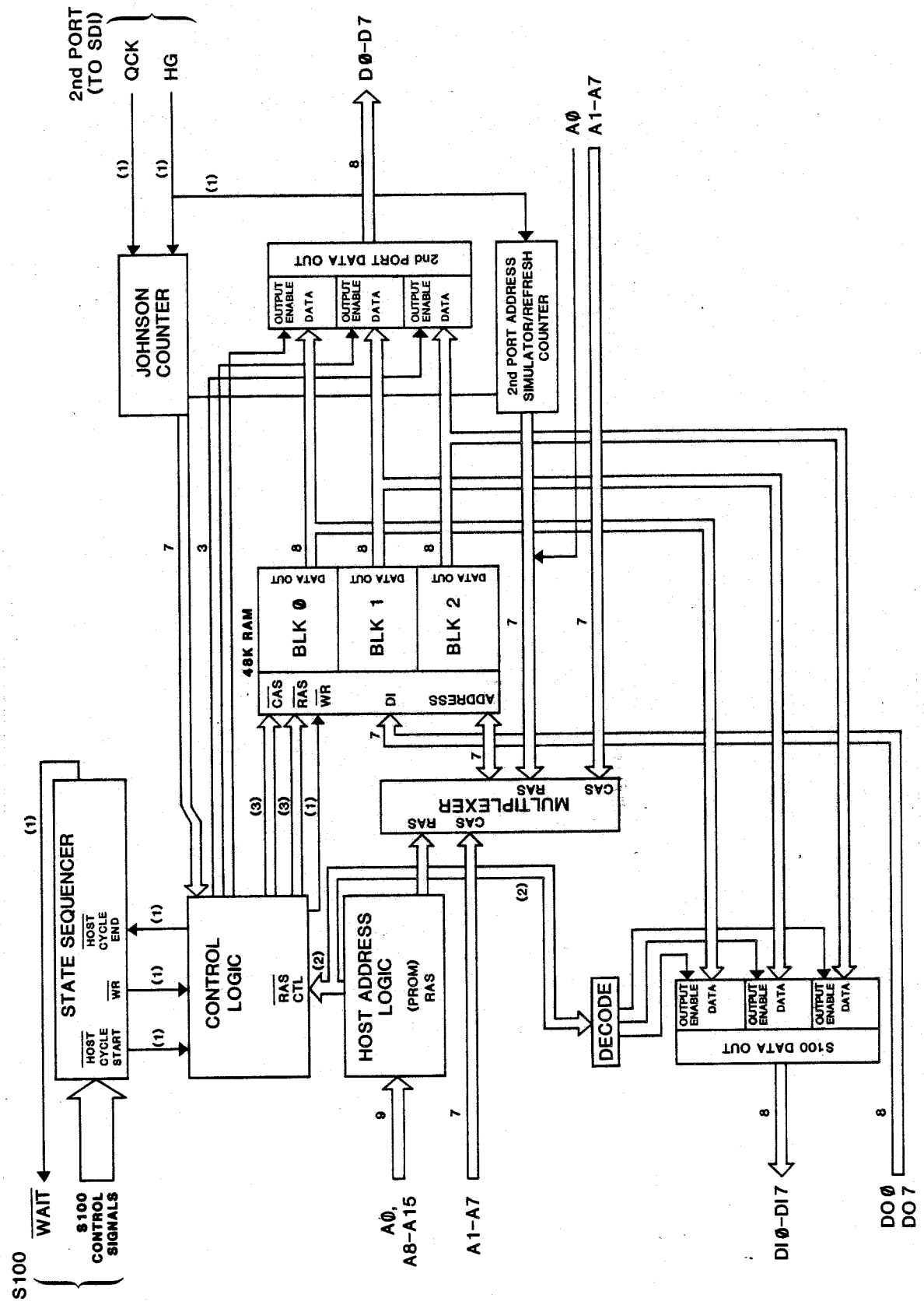


Figure 12 - 48KTP Block Diagram

When second port RAS and CAS are stable, these selection lines are sent to all three 16K sections and three separate bytes are read simultaneously and latched into I.C. 12, 13, and 14 of the 48KTP. Reading three bytes for the second port each cycle gives an average of 1 byte every (810/3) nsec or 270 nsec which is the rate at which the SDI requires data.

HOST ACCESS

The 405 nsec host access window may or may not be accompanied by a host request. If no host request occurs, then a cycle without RAS is generated and data is not gated onto the host data bus. If a host request is present, a 16K memory block is selected in accordance with the host address given. This address does not generate RAS and CAS in a straightforward fashion as an on board PROM is used in the RAS generation process. This is illustrated in Figure 11. The selected 16K block is given RAS and then all three blocks are given CAS. If the host access is a **write**, the data is written into the 16K memory block which received RAS. If the host access is a **read**, then after the data has become valid, all three of the host data latches (I.C. 72, 73, and 74) are gated and the latch that contains the read (selected) data is enabled onto the DI bus for the host to read.

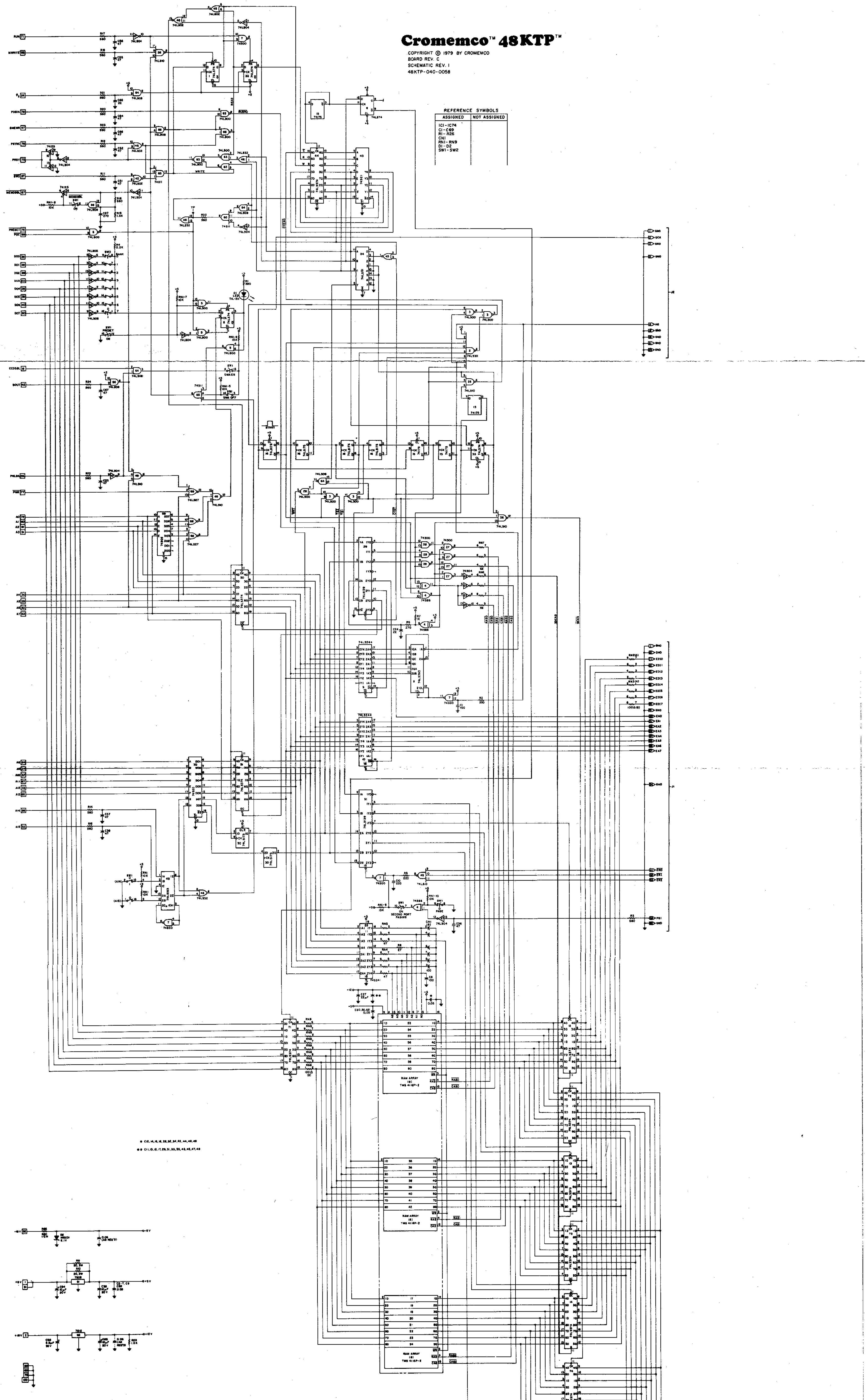
WAIT STATES

The 48KTP will, depending upon the type of access and the circumstances, request WAIT states of the host system during a memory access. WAIT states are needed because of the 48KTP's dedicated memory access periods and necessarily long cycle time of 810 nsec. The result of this is that only one host access can occur every 810 nsec.

The circumstances under which WAIT states will occur are as follows:

1. when two writes occur within 810 nsec. of each other, i.e., push qq

2. during all reads.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BOARD REV. C
SCHEMATIC REV. 1
48KTP-040-0058
REFERENCE SYMBOLS
ASSIGNED
NOT ASSIGNED
IC1-IC74
C1-C69
R1-R26
CN1
RN1-RN9
D1-D2
SW1-SW2