ADD ANALOG CAPABILITY TO YOUR COMPUTER WITH THE CROMEMCO D + 7A I/O

by Roger H. Edelson

This month I will report on the Cromemco D + 7A I/O card (freely translated that's One Digital Plus Seven Analog Inputs/Outputs) and the associated Joystick Console. The D + 7A I/O will be covered first, because without an analog channel you can't make use of the Joystick Console.

The Cromemco D + 7A I/O card allows you to input and output analog signals as easily as you would digital ones. One digital and seven analog input/output ports are provided, with five port address jumper wires used to select the starting port address of the board. The lowest port address is the location of the digital I/O port with the next higher seven locations setup for the seven analog I/O ports. Cromemco suggests selection of port 030 (octal) as the digital port with ports 031 through 037 as the seven analog ports.

Let us begin our review of the D + 7A I/O board with the single parallel digital I/O channel. Figure 1 provides the schematic diagram of Revision 3 of the board. Quad D flip-flops, Z1 and Z2 (74175's), are used as output latches and drivers. The Quad 2-Line to 1-Line Data Selectors/Multiplexers (Z25 and Z33 — 74LS157's) are used to place the digital word supplied by the computer on the input lines of the Quad D flip-flops. Being very sneaky, Cromemco, which has inverted DO7 (for reasons which will be explained later) has corrected this inversion by using the Q output of Q_A on Z_1 — verry tricky. The parallel digital input is buffered by the omnipresent 74367 Hex Buffers (the same animal as the possibly more familiar 8T97 series Hex Buffers). Input STB is used to strobe these buffers and is generated by Z12 (a 7442 BCD/Decimal Decoder). This strobe is produced by a Port 0 Iput command — that's port 030 if you have used the suggested port locations given by Cromemco. The strobe (or clock) to the digital output latches is generated by a port 0 output command. The digital channel is really nothing special, and only accounts for a small slice of the board space, but it does provide a convenient means of getting a digital word in and out of the computer. The real heart of this card is the seven analog input/ouput channels.

The Cromemco D + 7A I/O board provides seven multiplexed channels of analog input/output including conversion to and from digital words. The analog-to-digital (A-to-D) conversion is performed by a successive approximation technique. As implemented in the D + 7A I/O card an 8-bit multiplying digital-to-analog converter (MC 1408L-8) and an 8-bit successive approximation register (SAR) are used to provide an approximately ± 0.5% D-to-A/A-to-D converter.

Let's follow the functional operation of the analog/ digital conversion section, beginning with the analog output cycle, because it is the easiest.

Stripped to its basics, the digital-to-analog output conversion consists of applying eight bits of digital data to the input of the MC1408L-8 D-to-A converter. This produces a current of between 0 and 2ma. (depending on the value of the digital word) into pin 4. A balancing current, equal to ½ of the full-scale chip current) is sup-

plied by the A/D zero network to provide a zero-set and bi-polar operation. The result of these currents operating on resistor R_{11} is to produce a voltage in the range of ± 2.56 volts to be applied to the analog output hold circuitry. These circuits are simply an operational amplifier connected as a voltage follower with a voltage holding capacitor on the input. An RCA 3140 BiMOS operational amplifier is used for this circuit to provide the characteristics needed for good operation. The 3140 device combines a MOS/FET input with a bipolar output (hence the name) to achieve low input currents with a high output drive capability. The typical electrical characteristics of the RCA 3140 are shown in Table 1. With ± 5 volt supplies the input current should run around 22 amp. Using a 0.0022µfd. holding capacitor, the analog output droop caused by this current is given by $V/t = I/C$. Using the values provided this gives $22 \times 10^{-12}/0.0022 \times 10^{-6}$, or approximately 10 mv per second droop because of the amplifier (a ½-bit or approximately .1% FS error in one second). Additional components of output droop are caused by output leakage current of the multiplexer switch and the capacitor and board leakages. While on the subject of the holding capacitor, the manual and the schematic both indicate that these components should be mylar. This is required both for leakage considerations and to minimize errors caused by dielectric relaxation. Unfortunately the capacitors supplied with my kit look suspiciously like ceramic types — a no-no. Cromemco does not provide a specification for analog output accuracy nor droop, other than to indicate that the refresh rate should be 1 Hz or faster.

Table I.

TYPICAL ELECTRICAL CHARACTERISTICS

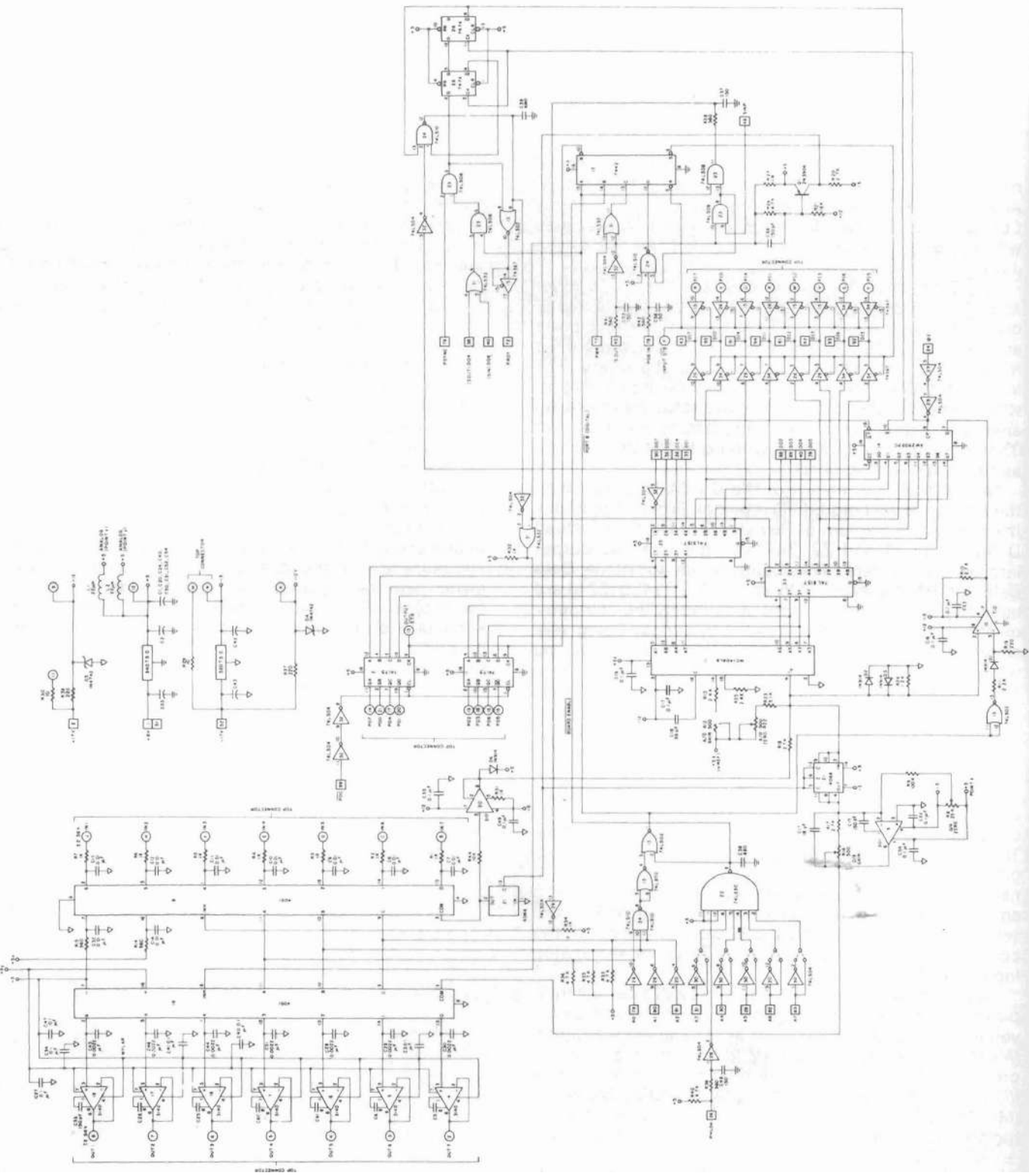| CHARACTERISTIC		TEST CONDITIONS $V^+ = +15V$ $V^- = -15V$ $T_A = 25°C$	LIMITS			UNITS
			CA3140B	CA3140A	CA3140	
Input Offset Voltage Adjustment Resistor		Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}	43	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	1.5	TΩ
Input Capacitance	C_I		4	4	4	pF
Output Resistance	R_o		60	60	60	Ω
Equivalent Wideband Input Noise Voltage	e_n	BW = 140 kHz $R_S = 1$ MΩ	48	48	48	µV
Equivalent Input Noise Voltage	e_n	f = 1 kHz R_S L f = 10 kHz 100Ω	40 12	40 12	40 12	nV/√Hz
Short Circuit Current to Opposite Supply Source I_{OM}^+ Sink I_{OM}^-			40 18	40 18	40 18	mA mA
Gain Bandwidth Product	f_T		4.5	4.5	4.5	MHz
Slew Rate	SR		9	9	9	V/µs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low			220	220	220	µA
Transient Response Rise Time Overshoot	t_r	$R_L = 2$ kΩ $C_L = 100pF$	0.08 10	0.08 10	0.08 10	µs %
Settling Time 1 mV at 10 V p-p (See Fig. 17) 10 mV	t_s	$R_L = 2$ kΩ $C_L = 100$ pF Voltage Follower	4.5 1.4	4.5 1.4	4.5 1.4	µs

Figure 1. Cromemco D + 7A I/O™ Schematic

The drive capability of the analog output is about 30 ma source and a 12ma sink; adequate enough for most applications. Again, Cromemco does not provide a specification for this function, I determined the value from the characteristics of the RCA 3140. The slew rate of the 3140 is fast enough (9 V/μsec.) but its settling time is 4.5μsec. for a 1 mv. error. For this reason, 11 wait states (5.5μsec.) have been provided before allowing another command to be performed.

The actual operational cycle of the analog output begins when the CPU sends PSYNC and SOUT at the start of an analog output cycle in coincidence with a port address in the range 31 to 37, Z28 P5 goes high to indicate this event. Gating logic then causes PRDY to be pulled to a logic 0, causing the CPU to enter a wait state. One 02 cycle later, Z28 P8 goes low instructing the successive approximation register (SAR) to begin operation on the next 02 rising edge. The SAR then begins operation and holds down its CC output for an additional 8 02 cycles. During analog output, the SAR is used only as a timing device to generate a sufficient number of wait states to cause proper circuit operation. Its other outputs are ignored. The logic gating holds down PRDY until the SAR has completed operation and released its CC output. A total of 5.5μsec. of wait states are produced at 2MHz.

As a result of SOUT going to a logic 1, Z32 P12 goes to a logic 0. This signal switches most of the circuitry between input and output modes. In particular, pin 1 of Z25 and Z33 go low, selecting the A inputs, and Q1 produces +5V at the control inputs of Z21, turning its sections ON.

With Z25 and Z33 switched to their A inputs, the 8 data bits flow from the DO bus to the inputs of the D/A converter Z11. This causes a current to be pulled by the I/O output, pin 4, towards the -12V supply, with its magnitude proportional to the binary number at its inputs A1-A8. Resistors R12 and R13 provide the full scale reference current for the D-to-A converter, while R22 and R23 produce a half scale offset so that the code 10000000 at the D-to-A converter input produces 0 volts output. Inverter Z32 complements DO7 so that 0 volts output occurs for the code 00000000 on the DO bus, thereby giving 2's complement operation. This allows bipolar operation of the D-to-A converter with binary numbers the CPU can generate. Now we see the reason for inverting 007.

Since the CMOS transmission gate Z1 is ON, a resistance of about 30 ohms connects the D/A converter output to pin 2 of Z9. This amplifier then produces whatever voltage is needed at its pin 6 (in the range ± 2.56) so that the current though R16 and R17 exactly balances the D-to-A converter output current. The output voltage at Z9 P6 then goes to the output S/H multiplexer Z18 P3. The output port address bits A0-A2 direct the multiplexer Z18 to connect Z9 P6 to one of the .0022 voltage hold capacitors with a CMOS transmission gate. Current then flows to charge the selected holding capacitor to the desired output voltage. Charging is enabled only during the wait states of an analog output function. Voltage follower amplifiers with MOS inputs copy the holding capacitor voltages to the analog output pins, thereby preventing drift due to loading.

The analog input uses a successive approximation A-to-D conversion technique. Figure 2 provides a functional block diagram of this type of converter. The comparator is used as the decision element to control the state of the eight bits of the successive approximation register. When the conversion cycle starts, the SAR first sets its Q7 output to a logic 0 and outputs Q0 through Q6 to a logic 1. This causes the D-to-A to sink a current equal to one-half the full scale value of approximately 2mA. At the end of the first clock period, the SAR
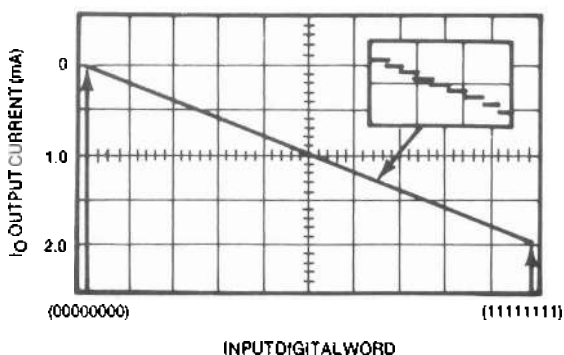
Figure 2.

checks the output of the comparator Z10. If the analog input voltage is negative, the SAR leaves bit Q7 clear. Otherwise, it is set. At the same time, the SAR also sets Q6 to a logic 0. It then waits one clock cycle before using the comparator output to set the state of Q6, and clears Q5. In a similar manner, the successive approximation procedure continues until all bits Q0-Q7 have been set and subsequently tested. This procedure corresponds to the use of a set of 2 pan balance scales with binary weight values to weigh an object, and is the fastest procedure operating on only one bit at a time. Other procedures are available which operate on more than one bit at a time, at the expense of circuit complexity, and dual slope A-to-D convertors will provide more accuracy at the expense of time. The successive approximation technique is a good trade-off between circuit complexity and conversion time. At the end of the conversion cycle the SAR outputs contain the digital representation of the analog voltage.

The heart of this A-to-D converter is the Motorola MC1408L-8 Eight Bit Multiplying Digital-To-Analog converter. Figure 3 provides a look at the block diagram of the MC1408L-8 and the D-to-A Transfer Characteristics. As can be seen from Table 2 (the electrical characteristics of the chip) this device provides a ± 0.19% relative accuracy (to full scale). This accuracy is degraded by the scaling circuitry used on the board. Again, Cromemco does not provide an accuracy specification. The MC1408L-8 possesses a very fast settling time (300nsec to within ½ LSB). This allows a bit to be set every clock period, at a 2 MHz clock rate.
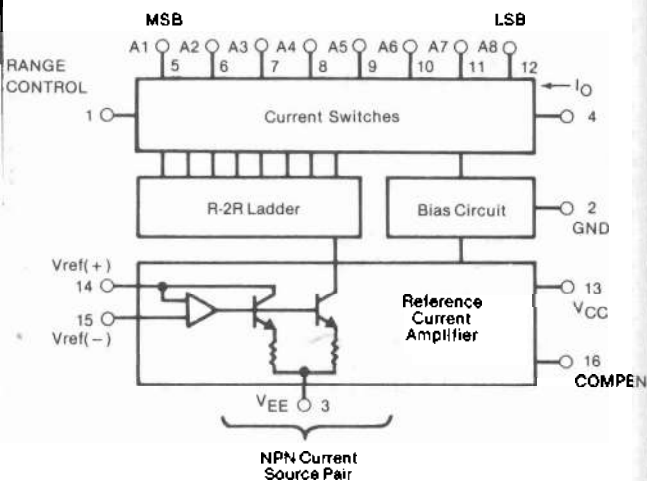

Figure 3.

The MC1408L-8 consists of a reference current amplifier, an R-2R ladder network, and eight high-speed current switches. To use the device all that is necesary is to supply a reference voltage to pin 14 (done from +5X through the A/D gain network) and a reference resistor (R25) to pin 15. The switches are non-inverting, therefore a high state on the digital input line turns them on. High speed current steering switches are used in the selection of the current specified by the R-2R ladder. This ladder divides the reference amplifier current into binary-related components which are fed to the switches.

Let's take a look at the analog input cycle. At the start of the cycle the CPU sends PSYNC and SINP in coincidence with an analog port address. Z28 detects this event and initiates a cycle in a manner similar to the analog output sequence. In this case, however, the SAR output is connected by the multiplexers Z25 and Z33 to the D-to-A converter's data inputs.

The input port command for channels 1 to 7 is taken from A0 through A2 by the analog multiplexer Z8 and used to connect an analog input to the voltage follower Z20. In this case, Z21 is an open circuit. Voltage follower Z20 has a very low input current requirement in combination with a fast slewing capability. This prevents loading of the signal sources and allows full accuracy for source impedances of up to 10K ohms. Output from the voltage follower goes through R18 to inject current into the summing node at Z11 P4 and Z10 P2. After the 2-clock cycle time delay generated by Z28 to allow for settling of the input circuit, the SAR begins the conversion process which we have already discussed. At the end of the conversion cycle, the SAR outputs

contain the desired data word. The CC output goes to a logic 0, signalling the end of the conversion process and allowing the CPU to proceed. The CPU then inputs Q0 through Q7 as its data. Q7 is complemented to produce a 2's complement binary code and allow straightforward bipolar operation.

Let's now take a look at the D + 7A I/O mechanized as a kit. The card is of the same high quality material and construction as I have come to expect from the Cromemco kits. The board is high quality glass with all the etch tinned. The edge board connectors are gold plated for reliability. The solder masking and the component marking are excellent. The solder masking in particular is detailed enough to prevent many of the easily-made solder splash problems. The board in places looks unfortunately as if it were laid out by an engineer. This does not affect operation, and is probably necessary to assure good noise characteristics and reliable operation, but it is esthetically somewhat unappealing.

Construction is straightforward requiring only about 2½ hours from unpacking to board cleaning, a step which Cromemco fails to mention — but is extremely important in any analog board. Some small problems showed up during assembly:

1) Some of the IC's should be temporarily inserted when installing the 0.0022 µfd. capacitors, particularly IC 18. This must be done or you will find it very difficult to get the IC inserted after the capacitors have been soldered in place. IC's 23 and 34 are also tight because of the two capacitors C38 and C39. Resistor R13 must be inserted before the potentiometer R12.

2) The board pads are not always correctly spaced,

Table II.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15V$, $V^- = 15V$, $T_A = 25°C$ Unless Otherwise Specified

CHARACTERISTIC	LIMITS									UNITS
	CA3140			CA3140			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $|V_{IO}|$	—	0.8	2	—	2	5	—	5	15	mV
Input Offset Current, $|I_{IO}|$	—	0.5	10	—	0.5	20	—	0.5	30	pA
Input Current, I_I	—	10	30	—	10	40	—	10	50	pA
Large-Signal	50 k	100 k	—	20 k	100 k	—	20 k	100 k	—	V/V
Voltage Gain, A_{OL} ●	94	100	—	86	100	—	86	100	—	dB
Common-Mode	—	20	50	—	32	320	—	32	320	µV/V
Rejection Ratio, CMRR	86	94	—	70	90	—	70	90	—	dB
Common-Mode Input-Voltage Range, V_{ICR}	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection $\Delta V_{IO}/\Delta V$	—	32	100	—	100	150	—	100	150	µV/V
Ratio, PSRR	80	90	—	76	80	—	76	80	—	dB
Max. Output V_{OM}^+	+12	13	—	+12	13	—	+12	13	—	V
Voltage ■ V_{OM}^-	−14	−14.4	—	−14	−14.4	—	−14	−14.4	—	
Supply Current, I^+	—	4	6	—	4	6	—	4	6	mA
Device Dissipation, P_D	—	120	180	—	120	180	—	120	180	mW
Input Current, I_I ▲	—	10	30	—	10	—	—	10	—	nA
Input Offset Voltage V_{IO} ▲	—	1.3	3	—	3	—	—	10	—	mV
Large-Signal	20 k	100 k	—	—	100 k	—	—	100 k	—	V/V
Voltage Gain, A_{OL} ▲	86	100	—	—	100	—	—	100	—	dB
Max. Output V_{OM}^+	+19	+19.5	—	—	—	—	—	—	—	V
Voltage, * V_{OM}^-	−21	−21.4	—	—	—	—	—	—	—	
Large-Signal	20 k	50 k	—	—	—	—	—	—	—	V/V
Voltage Gain, A_{OL} ‡ *	86	94	—	—	—	—	—	—	—	dB

● At $V_O = 26V_{p-p}$, +12V, −14V and $R_L = 2k\Omega$.
■ At $R_L = 2k\Omega$.
▲ At $T_A = -55°C$ to $\pm 125°C$, $V^+ = 15V$, $V^- = 15V$, $V_O = 26V_{p-p}$, $R_L = 2k\Omega$.
* At $V^+ = 22V$, $V^- = 22V$.
‡ At $V_O = +19V$, −21V, and $R_L = 2k\Omega$.

Figure 4. Circuit Schematic

or the 0.1 μfd capacitor lead spacing, making it difficult to seal some of these capacitors.

3) No layout drawing is provided. The component marking on the board, as indicated earlier, is excellent making assembly a not difficult task. But I like a layout drawing also — it can't cost that much.

These gripes are really very minor and don't affect the kit in any way. They really don't much slow down construction either.

One nice feature — my CA3140 IC leads were already shaped, which made light work of inserting these devices. Again, though Cromemco doesn't mention it, don't forget to clean the solder resin off your board. This step is a must to reduce the board leakage current and achieve high-quality A-to-D operation.

After assembly of the board it is necessary to calibrate the analog/digital/analog channels. The calibration procedure begins with the A-to-D channel. Known voltages must be applied to the analog input and the A/D gain (R12) and A/D zero (R22) are adjusted until the digital value is correct. While this is straightforward, (even though R12 and R22 interact requiring an iterative procedure) the instructions require an input of +2.54 v and -2.56 volts — values not likely to be found lying around everyone's computer room. A variable power supply and a digital voltmeter will do the job — if you have one.

A possible alternative would be to set the analog input to 0 volts (short it) and adjust the R22 until the output of the selected digital port is "0". Then apply any known—or measured—voltage (a battery, etc.) and set the A-to-D gain (R12) until the digital value is the representation of the analog voltage supplied (remember, each bit = 20mv). Reversing the battery will provide a negative voltage to check both polarities. It may be necessary to readjust R22 to get the correct negative digital value. Remember, as the D + 7A I/O uses two's complement representation, 10000000 (80_H) is equal to -2.56V and FF_H (11111111) is not "-0" but actually -20mv. For this reason the negative full scale value is 20 mv. greater than the positive full scale (bit 8, the sign bit, provides the extra -20mv.). Figure 5 gives an example of some of the 8-bit two-s complement representation of analog voltages.

After the analog input channel has been calibrated the analog output is calibrated. An accurate voltmeter is all that is required for this simple operation. Using the program supplied by Cromemco R16 (D-to-A) gain is adjusted for full scale positive output. The program is then modified and the D-to-A zero pot. (R8) is adjusted for a zero output. This procedure may have to be repeated once or twice as these controls interact also.

Besides providing the digital and analog I/O channels at the top edge board connector (gold plated for reliability) Cromemco has also brought out several power supply voltages. Analog and digital grounds are separated to avoid placing digital return currents in the analog ground returns. Figure 6 shows the top connector pin assignments. Cromemco has also thoughtfully provided the female counterpart to the top-edge connector. This connector is equipped with a nice handle for easy insertion and removal.

01111111	+ 2.54 volts
0000001	+ 0.02 volts
00000000	0 volts
11111111	− 0.02 volts
10000000	− 2.56 volts

Figure 5.

The D + 7A I/O card is a well-thought-out addition to your computer, which will expand the capabilities of your present installation and allow you to handle analog signals as easily as digital. Some of the more popular applications for this card would be oscilloscope graphics, process control, music or voice synthesis, and joystick interfaces. In line with the last mentioned application, Cromemco provides a Joystick Console (JS-1) which is set up to interface with the D + 7A I/O card.

As can be seen in the schematic, the JS-1 provides four switches as digital inputs, two pots (with mechanical trim adjustments) arranged as a two-axis joystick as analog inputs, and an emitter follower driving a 45-ohm speaker as one analog output. The digital switches operate to provide + 5 volt in their open condition and ground in the energized state. The emitter follower is AC coupled with a time constant of about 50msec.

Construction is extremely easy. However, I don't much care for unsupported components. I wish Cromemco had provided a standoff for the 10K resistors. Initial checkout is also a snap. The instructions are more than adequate.

With the JS-1 Cromemco also provides the software for Dazzle-Doodle™, a program which is designed to allow the user to draw full-color pictures on the screen of an ordinary TV under joystick control. The hardware required is a D + 7A I/O to interface the joystick, and a Cromemco TV Dazzler™ for the TV display interface. The computer must supply 2K of static RAM for picture element storage, and another approximately 128 bytes of program storage.

Cromemco also provides software support for the joystick console including Dazzle-Doodle, Track, Chase!, and Spacewar, complete with documentation. Each of these games is available on paper tape with the documentation for $15 a piece.

The JS-1 provides an easy and lowcost way to provide an analog input to your D + 7A I/O card. When these two units are combined, it is easier to enter analog inputs into your computer than digital — and in some cases more fun.

CONNECTOR PIN ASSIGNMENTS

COMPONENT SIDE		PIN No.	PIN No.	SOLDER SIDE	
ANALOG GROUND		A	1	ANALOG GROUND	
ANALOG INPUT	7	B	2	ANALOG OUTPUT	7
	6	C	3		6
	5	D	4		5
	4	E	5		4
	3	F	6		3
	2	H	7		2
ANALOG INPUT	1	J	8	ANALOG OUTPUT	1
-12V REGULATED		K	9	+12V REGULATED	
ANALOG GROUND		L	10	ANALOG GROUND	
-17V UNREGULATED		M	11	+17V UNREGULATED	
-5V REGULATED		N	12	+5V REGULATED	
INPUT STB		P	13	OUTPUT STB	
PARALLEL INPUT BIT	7	R	14	PARALLEL OUTPUT BIT	7
	6	S	15		6
	5	T	16		5
	4	U	17		4
	3	V	18		3
	2	W	19		2
	1	X	20		1
PARALLEL INPUT BIT	0	Y	21	PARALLEL OUTPUT BIT	0
DIGITAL GROUND		Z	22	DIGITAL GROUND	

PC
BOARD

Figure 6.

The Cromemco JS-1 joystick console is a general purpose I/O device designed specifically for use with mini and micro-computers. A Cromemco D + 7A analog interface can be used to interface one of two JS-1 consoles to any computer using the S-100 Microcomputer Bus.

Each joystick console includes a two-axis joystick, four push button switches, and an audio amplifier and speaker in an attractive, finished enclosure. A 12-conductor cable is included to connect the console to the top edge connector of the D + 7A interface.

When using one JS-1 console with the D + 7A interface Cromemco recommends the following port assignments:

Joystick X axis — analog input port 031 (19H)
Joystick Y axis — analog input port 032 (1AH)

SW1 — D0 input port 030 (18H)
SW2 — D1 input port 030 (18H)
SW3 — D2 input port 030 (18H)
SW4 — D3 input port 030 (18H)

Speaker — analog output port 031 (19H)

When using two JS-1 consoles the following port assignments for the second console are recommended:

Joystick X axis — analog input port 033 (1BH)
Joystick Y axis — analog input port 034 (1CH)

SW1 — D4 input port 030 (18H)
SW2 — D5 input port 030 (18H)
SW3 — D6 input port 030 (18H)
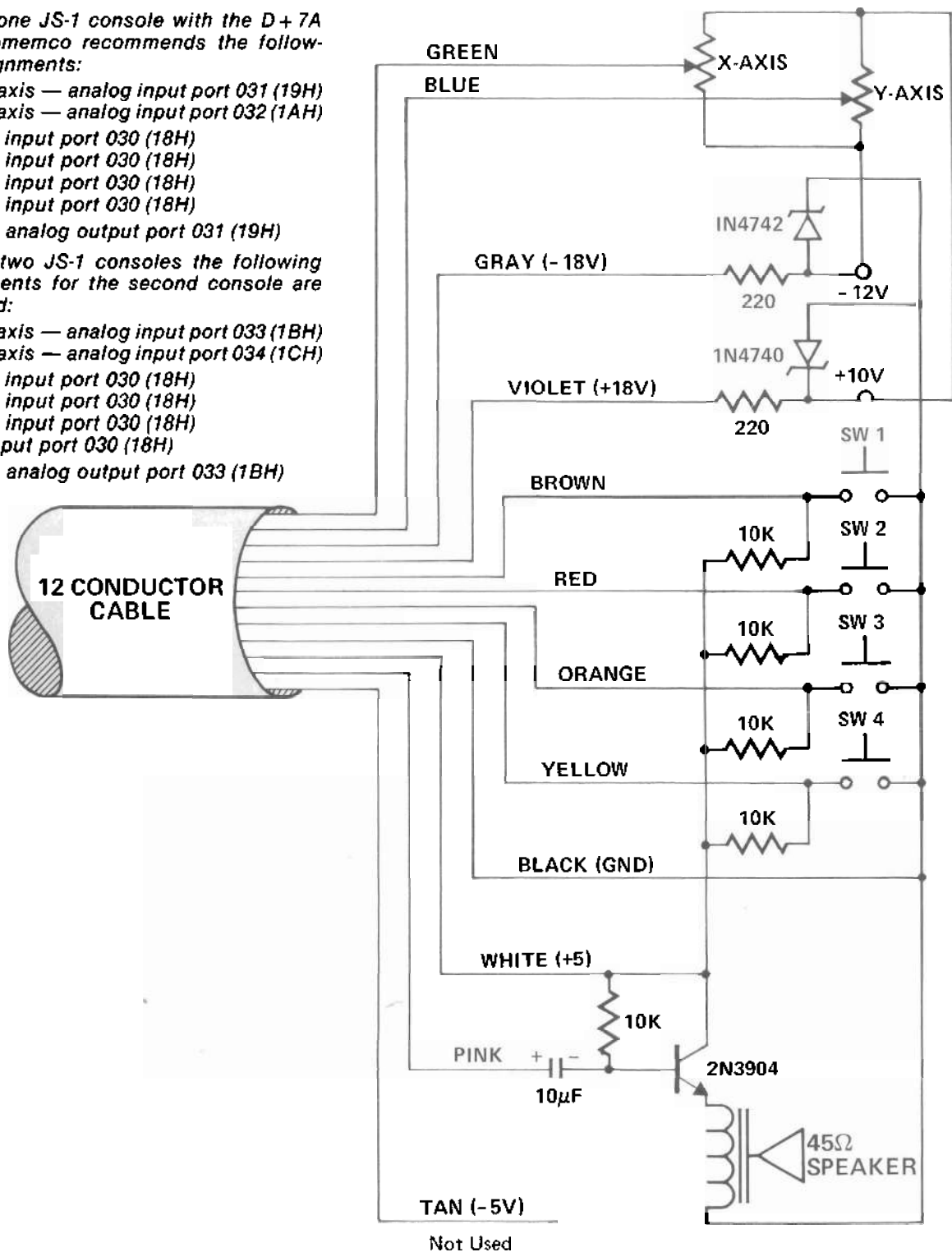SW4 — D7 input port 030 (18H)

Speaker — analog output port 033 (1BH)

Figure 7. The Schematic Diagram of the JS-1