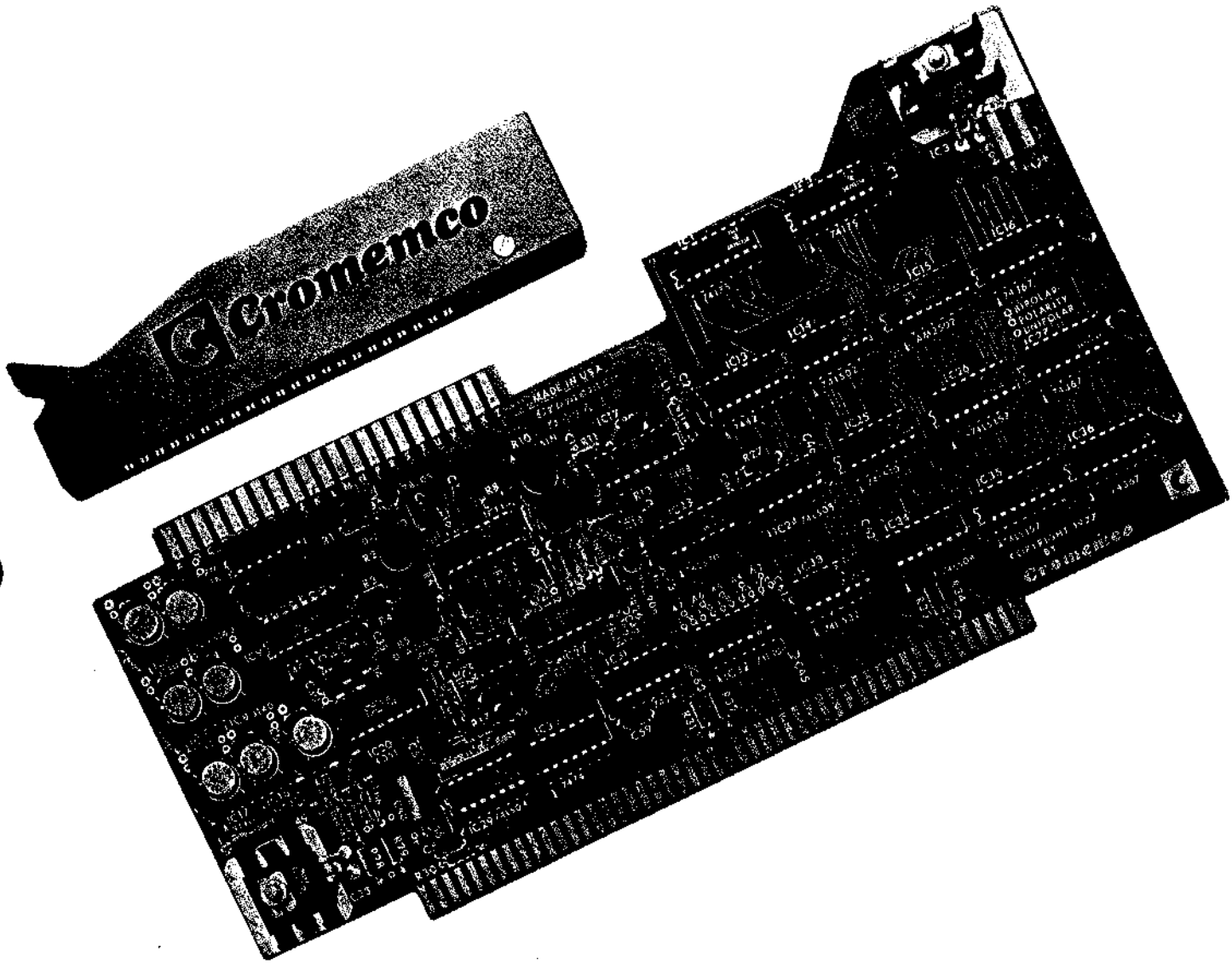
CROMEMCO D+7A I/O



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Cromemco
incorporated
Specialists in computers and peripherals
280 Bernardo Ave., Mountain View, CA 94041

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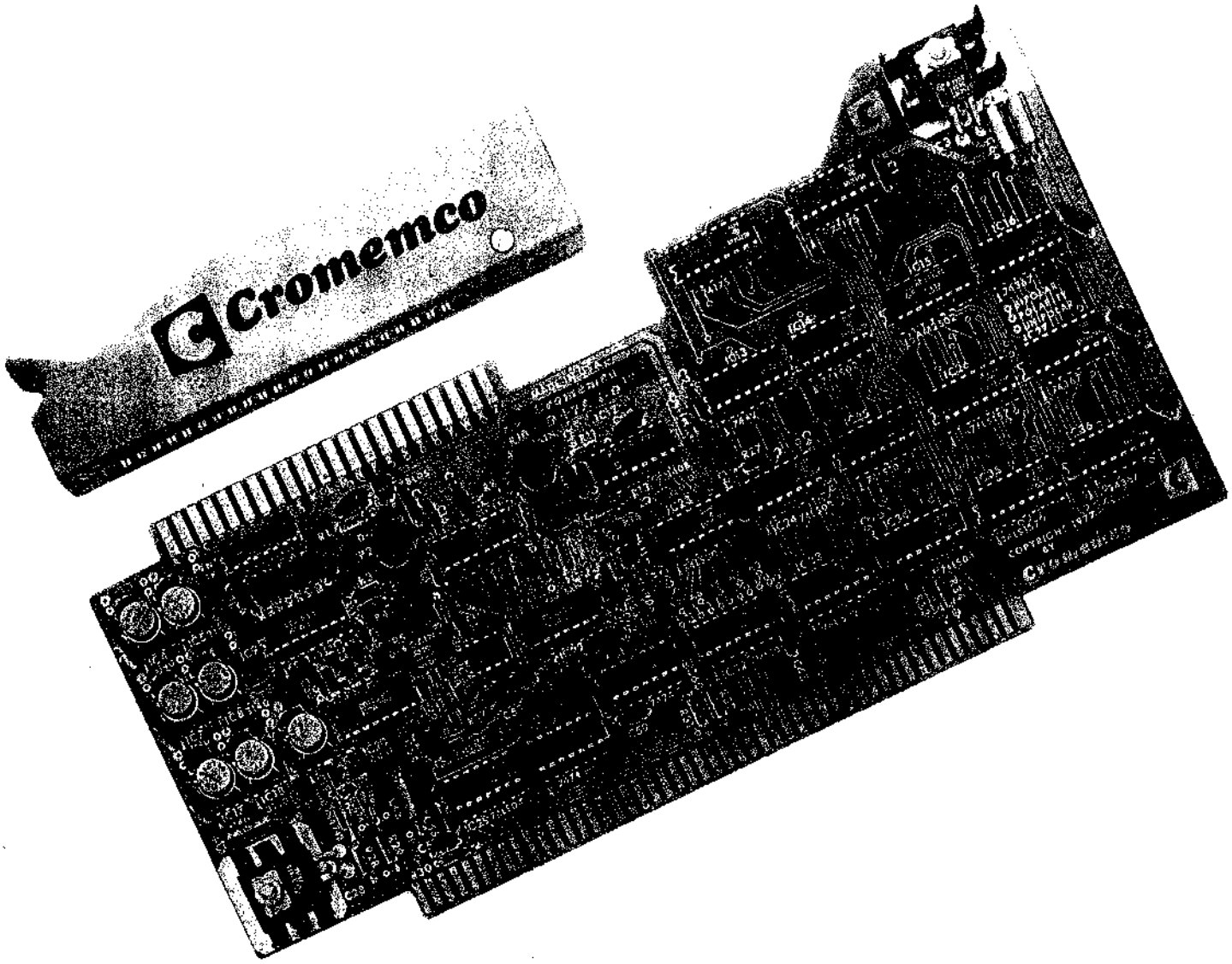

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INTRODUCTION

The Cromemco D+7A I/O Module is a fast and easy way to input and output both analog and digital signals from a computer. This high performance module gives seven channels of 8-bit analog-to-digital conversion and seven channels of digital-to-analog conversion with a fast conversion time of 5.5 microseconds. The D+7A I/O Module makes it easy to use a computer for applications ranging from process control and digital filtering to speech and music synthesis. Using the D+7A I/O Module, analog data can be input from joysticks, measurement instruments, machine tools, control systems, motors, recorders, plotters, and a large number of other devices.

The D+7A I/O Module plugs directly into an industry standard S-100 microcomputer bus. There are eight I/O ports on the D+7A I/O Module card, one digital and seven analog. Five port address jumpers on the board are used to select the addresses of these ports.

This manual describes the operation of the D+7A I/O Module in detail, and explains how it is used. A summary of the technical specifications of the D+7A I/O Module is given in Table 1.

Table 1
Technical Specifications
D+7A A/D & D/A Interface

TECHNICAL SPECIFICATIONS D+7A A/D & D/A INTERFACE

ANALOG INPUT PORTS:
- Number of input ports: 7
- Input voltage range: -2.56 to +2.54 volts
- Input bias current: 2 microamps max.
- 20 Megohms ‖ .001 μF, 1 kHz sample rate.
- 2 Megohms ‖ .001 μF, 10 kHz sample rate.
- Resolution: 8 bits.
- Conversion time: 5.5 microseconds
- Accuracy: ±20 millivolts

ANALOG OUTPUT PORTS:
- Number of output ports: 7
- Output voltage range: -2.56 to +2.54 volts
- Output impedance: 0.25 ohm.
- Maximum load current: 1.5 mA
- Resolution: 8 bits
- Conversion time: 5.5 microseconds
- Accuracy: ± 20 millivolts
- Drift rate: Less than 10 mV/sec at 25°C

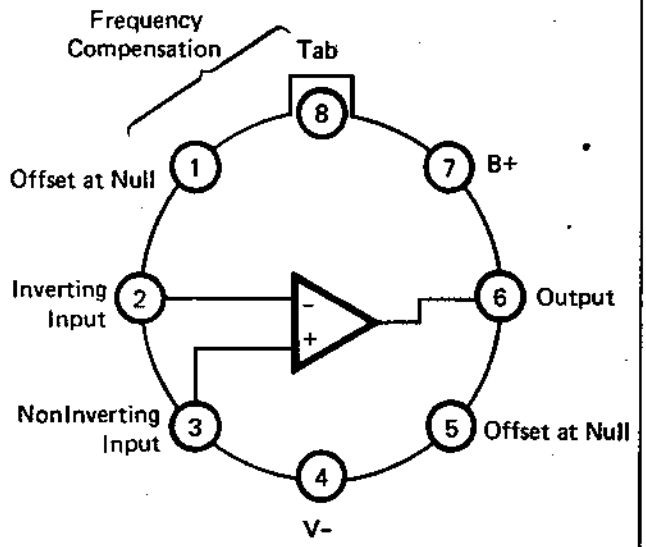
PARALLEL I/O PORT:
- Input port: 8 bits
- Output port: 8 bits
- Input load: one TTL equivalent
- Output drive: 10 TTL loads

GENERAL INFORMATION:
- Bus: S-100.
- Power requirements:
  - +8 volts @ 0.4 A
  - +18 volts @ 30 mA
  - -18 volts @ 60 mA

ASSEMBLY INSTRUCTIONS

If you purchased your D+7A as a kit you will find the assembly to be straightforward. To facilitate assembly, the location and value of every component is printed directly on the PC card. The components are simply inserted in the locations shown in figure 3 and soldered into position. Be sure to use a low-wattage soldering iron and high-quality rosin-core solder.

Figure 1 IC Case

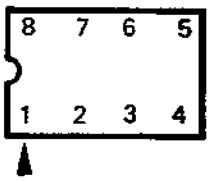


Note: Pin 4 Connected to Case

Table 2 Resistor Color Codes

10	brown-black-black	1.5K	brown-green-red
100	brown-black-brown	2.2K	red-red-red
150	brown-green-brown	2.4K	red-yellow-red
180	brown-gray-brown	2.7K	red-violet-red
220	red-red-brown	4.7K	yellow-violet-red
470	yellow-violet-brown	5.1K	green-brown-red
560	green-blue-brown	10K	brown-black-orange
1K	brown-black-red	18K	brown-gray-orange
1.2K	brown-red-red	100K	brown-black-yellow

Figure 2 TO-5 IC Installation



1. Install all IC sockets. Note that IC sockets must be used for all IC's except voltage regulators (IC3, IC6, and IC28.)

2. Install all resistors. The resistor color codes are shown in Table 2.

3. Install calibration potentiometers R2, R5, R10, R12. NOTE: R2 is 25K, and the other three are 500 ohms.

4. Install resistor network RN2. Note that pin 1 is leftmost, as indicated by the arrow on the PC board.

5. Install all six diodes in place taking care that the banded (cathode) end of each diode is properly oriented.

6. Install transistor Q1 (2N3906) and install IC6 (78L05). Note that the flat surface of each of these parts faces the top of the PC board.

7. Install voltage regulator IC's 3 and 28. A heatsink should be placed between the regulator and the PC board and the assembly secured with 6-32 hardware. Note that IC3 is a LM340T-5 or 7805 part. IC28 is a LM320T-5 or 7905 part. BE CAREFUL NOT TO INTERCHANGE THESE TWO IC's.

8. Install the two inductors L1 and L2.

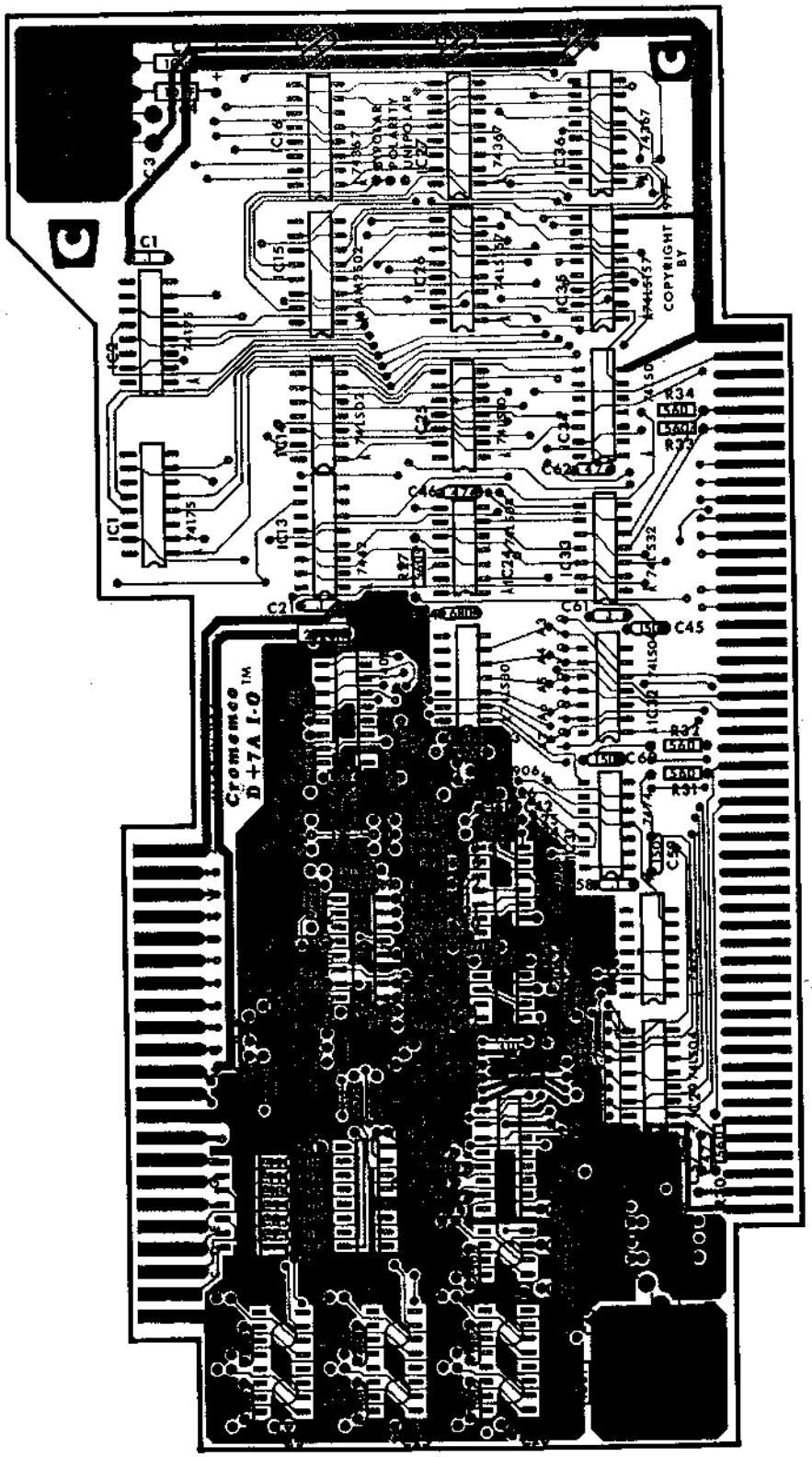
9. Install all capacitors as marked on the PC board. Note that the "+" end of each of the tantalum capacitors must be oriented properly. Capacitors C31, C32, C33, and C34 are mounted side-by-side but should NOT be in physical contact with one another.

10. Install all IC's and RN1 in their sockets taking care to see that pin one of each part is oriented as indicated by the arrow on the PC board. When installing IC's in the metal TO-5 style case, note that the metal tab denotes pin 8 of the IC as shown in figure 1.

The leads of the TO-5 style IC's should be shaped into two rows of four and inserted into the IC socket in the order shown in figure 2.

11. Carefully inspect your work. Make certain that the IC's are all properly oriented and that every pin of every IC is properly engaged in its socket. Carefully inspect your soldering for cold solder joints or accidental solder bridges.

Figure 3 Parts Location Diagram



CALIBRATION PROCEDURE

Two potentiometers are used for calibration of the A/D converter (R12 and R10) and two potentiometers are used for calibration of the D/A converter (R2 and R5). Calibration of the A/D converter must be done before calibration of the D/A converter.

The analog I/O channels use two's complement notation for ease of representing both positive and negative voltages. The least significant bit represents a 20 millivolt increment. The analog voltage range on both input and output is from -2.56 volts to +2.54 volts. For example, the following 8-bit codes are used to represent these analog voltages:

01111111	+2.54 volts
00000001	+0.02 volts
00000000	0 volts
11111111	-0.02 volts
10000000	-2.56 volts

To calibrate the A/D converter, known voltages must be applied to any one of the seven analog input channels (e.g., analog channel 7, port 037, on contact B of the top edge connector). You should enter and execute on your computer the following program to input from analog port 037 and output to digital port 030:

Address	Data	Description
000 000	333	Input
000 001	037	from port 037
000 002	323	Output
000 003	030	to port 030
000 004	303	Jump
000 005	000	000
000 006	000	000

Apply a -2.56 volt signal to contact B of the top edge connector and adjust R12 for an output address of 1000000 on pins 14 to 21. Now apply a +2.54 volt signal to contact B of the top edge connector and adjust R10 for an output address of 0111111 on pins 14 to 21 of the digital output port. Since R10 and R12 interact, you may need to repeat the above procedure once or twice.

To calibrate the D/A converter, a voltmeter must be used to measure the output voltage at any one of the seven analog output ports (say analog port 037, on contact "2" on the top edge connector). Now enter and execute the following program:

Address	Data	Description
000 000	076	Move into accumulator
000 001	177	177
000 002	323	Output
000 003	037	to port 037
000 004	303	Jump
000 005	000	000
000 006	000	000

While the above program is executing, adjust R5 for an output voltage of +2.54 volts on contact 2. Now modify the above program so that the second byte, 177, is replaced by "000". Execute this modified program and adjust R2 so that the output voltage on pin 2 is zero. Calibration is now complete.

OPERATING INSTRUCTIONS

All input and output signals are connected to the edge connector on the top of the D+7A I/O Module. The connector pin assignments are shown on Table 3 below.

Table 3
Connector Pin Assignments

CONNECTOR PIN ASSIGNMENTS

COMPONENT SIDE	PIN No.		PIN No.	SOLDER SIDE
ANALOG GROUND		A	1	ANALOG GROUND
ANALOG INPUT	7	B	2	ANALOG OUTPUT 7
	6	C	3	6
	5	D	4	5
	4	E	5	4
	3	F	6	3
	2	H	7	2
ANALOG INPUT	1	J	8	ANALOG OUTPUT 1
-12V REGULATED		K	9	+12V REGULATED
ANALOG GROUND		L	10	ANALOG GROUND
-17V UNREGULATED		M	11	+17V UNREGULATED
- 5V REGULATED		N	12	+ 5V REGULATED
INPUT STB		P	13	OUTPUT STB
PARALLEL INPUT BIT 7		R	14	PARALLEL OUTPUT BIT 7
	6	S	15	6
	5	T	16	5
	4	U	17	4
	3	V	18	3
	2	W	19	2
	1	X	20	1
PARALLEL INPUT BIT 0		Y	21	PARALLEL OUTPUT BIT 0
DIGITAL GROUND		Z	22	DIGITAL GROUND

PC BOARD

The digital ports and analog ports are accessed as input and output ports of the computer system. In the standard configuration, the port assignments in Table 4 are used.

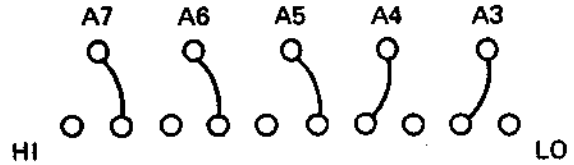
Provision has been made on the D+7A I/O Module for changing port assignments. This may become necessary if particular port addresses are already used or if more than one D+7A I/O Module is used in the computer at one time. The traces just above IC32 set the five high order bits of the port address. In the standard configuration, PC board traces connect the five bits as shown in figure 4.

If other port addresses are desired, the traces must be cut and jumper wires used to select the desired address.

Table 4
Port Assignments

Parallel	Octal address	Hex address
Parallel port	030	18
Analog port 1	031	19
Analog port 2	032	1A
Analog port 3	033	1B
Analog port 4	034	1C
Analog port 5	035	1D
Analog port 6	036	1E
Analog port 7	037	1F

Figure 4
Port Address Selection

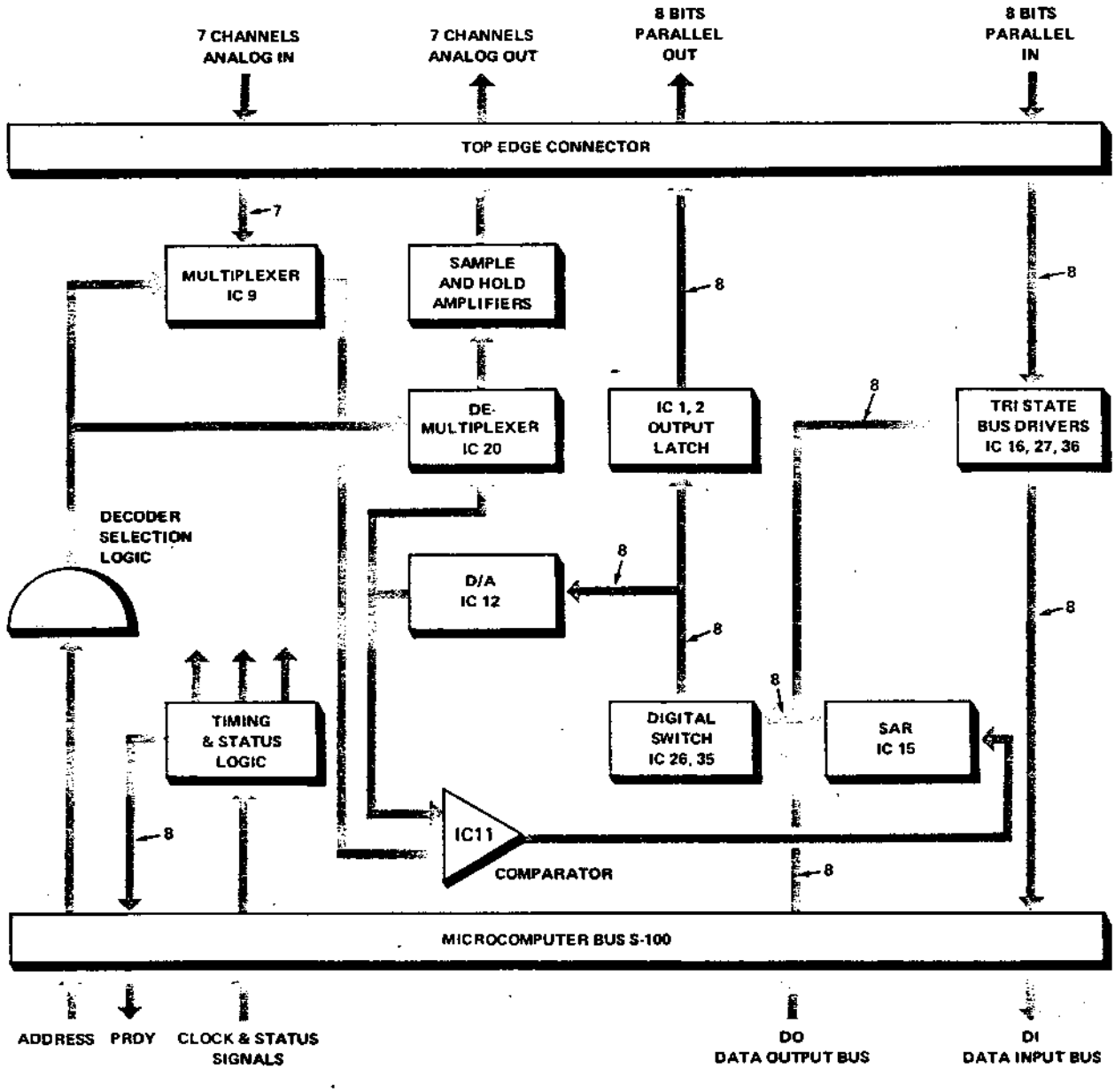


THEORY OF OPERATION

Introduction

The D+7A interface is able to perform four functional operations: 1) analog output, 2) analog input, 3) digital output, and 4) digital input. A simplified block diagram is shown in figure 5. A detailed schematic diagram is shown in figure 10. When referring to the schematic diagram note that numbers in square boxes refer to S-100 bus contacts on the bottom edge connector of the D+7A card. Numbers or letters in circles refer to contacts on the top I/O connectors of the D+7A card.

Figure 5 D+7A I/O Block Diagram



Analog Output

Analog output begins with an 8-bit data output word appearing on the S-100 DO (data output) bus. These 8-bits of data are routed through an 8-channel digital switch (IC's 26,35) to the input of an 8-bit digital-to-analog (D-to-A) converter (IC 12). The output of the D-to-A converter is switched to one of seven sample-and-hold output amplifiers by a demultiplexer switch (IC 20). The output of the sample-and-hold amplifiers (IC's 4,5,7,8,17,18,19) are brought to the top edge connector contacts of the D+7A card.

When the CPU sends PSYNC and SOUT (at the start of an analog output cycle) in coincidence with a port address (in the range 31 to 37), IC30 output pin 6 goes high to indicate this event. Gating logic then causes PRDY to be pulled to a logic 0, causing the CPU to enter a wait state. One $\overline{CLK}$ cycle later, IC31 output pin 8 goes low thereby instructing the successive approximation register (SAR), IC 15, to begin operation on the following $\overline{CLK}$ rising edge. The SAR then begins operation and holds down its $\overline{CC}$ output for an additional 8 $\overline{CLK}$ cycles. During analog output, the SAR is used only as a timing device to generate a sufficient number of wait states to cause proper circuit operation. Other outputs are ignored. The logic gating holds down PRDY until the SAR has completed operation and released its $\overline{CC}$ output, causing IC31 pin 5 to go low on the next Ø2 positive edge. A total of 5.5 μs of wait states are produced at 2MHz and a total of 5.0 μs of wait states are produced at 4MHz.

As a result of SOUT going to a logic 1, IC34 pin 12 goes to a logic Ø. This signal switches most of the circuitry between input and output modes. In particular, pin 1 of IC26 and pin 1 of IC35 go low, selecting the A inputs, and Q1 produces +5V at the control inputs of IC22, turning its sections ON.

With IC26 and IC35 switched to their A inputs, the eight data bits flow from the D0 bus to the inputs of the D/A converter IC12. This causes a current to be pulled by the I_O output, pin 4, towards the -12V supply, with the magnitude proportional to the binary number at inputs A1-A8. Resistors R10 and R11 provide the full scale reference current for the D/A converter. Resistors R12 and R14 produce a half scale offset so that the code address 10000000 at the D/A converter input produces a 0 volt output. Inverter IC34 complements DO7 so that a 0 volt output occurs for the code 00000000 on the DO bus, thereby giving two's complement operation. This allows bipolar operation of the D/A converter with binary numbers generated by the CPU.

Since the CMOS transmission gate IC22 is ON, a resistance of about 30 ohms connects the D/A converter output to pin 2 of IC10. This produces whatever voltage is needed at its output pin 6 (in the range ±2.56) so that current through R5 and R7 exactly balances the D/A converter output current. The output voltage at IC10 output pin 6 then goes to the output of multiplexer IC20 pin 3. The output port address bits AØ-A2 direct the multiplexer IC20 to connect IC10 pin 6 to one of the 0.0022 voltage hold capacitors of the CMOS transmission gate. Current then flows to charge the selected holding capacitor to the desired output voltage. Charging is enabled only during the wait states of an analog input function. Voltage follower amplifiers with MOS inputs copy the holding capacitor voltages to the analog output pins, thereby preventing drift due to loading. Residual voltage drift primarily results from CMOS multiplexer leakage currents. Because of the drift, the analog outputs in use must be refreshed at a 1Hz or faster rate by OUTPUT instructions.

Analog Input

One of seven analog input channels is selected by the input multiplex switch, IC 9. The signal on this channel is connected to one input of an analog comparator, IC 11. The other input to the analog comparator is derived from the output of the D-to-A converter, IC 12. A successive approximation shift register (SAR, IC 15) receives the output of the analog comparator and outputs a successively larger or smaller digital word to the D/A converter based on the comparator output. When conversion is complete the 8-bit output of the SAR is put on the data input (DI) bus through bus drivers IC 27 and IC 36.

At the start of an analog input cycle, the CPU sends PSYNC and SINP in coincidence with an analog port address. IC30 detects this event and initiates a cycle in a manner similar to the analog output sequence. In this case, however, the SAR output is connected by multiplexers IC26 and IC35 to the D/A converter's data inputs.

The input port command for channels 1 to 7 is taken from AØ through A2 by the analog multiplexer

C9 and used to connect an analog input to the voltage follower IC21. In this case, IC22 is an open circuit. Voltage follower IC21 has a very low input current requirement in combination with a fast slewing capability. This prevents loading of the signal sources and allows full accuracy for source impedances of up to 10K ohms. Output from the voltage follower goes through R20 to inject current into the summing node at IC12 pin 4 and IC11 pin 2. After the time delay generated by IC31, to allow for settling of the input circuit, the SAR begins the conversion process.

When the conversion cycle starts, the SAR, IC15, first sets the Q7 output bit to a logic Ø and the QØ through Q6 output bits to a logic 1. This causes the D/A to sink a current equal to 127/256 of the full scale value of approximately 2mA. At the end of the first clock period, the SAR checks the output of the comparator IC11. If the analog input voltage is negative, the SAR leaves bit Q7 clear. Otherwise, it is set. At the same time, the SAR also sets bit Q6 to a logic Ø. It then waits one clock cycle before using the comparator output to set the state of bit Q6 and clears bit Q5. In a similar manner, the successive approximation procedure continues until all bits QØ-Q7 have been set and subsequently tested. This procedure corresponds to the use of a set of balance scales using binary weight values to weigh an object and is the fastest procedure operating on only one bit at a time.

At the end of the conversion cycle, the SAR outputs contain the desired data word. The $\overline{CC}$ output goes to a logic Ø, signalling the end of the conversion process and allowing the CPU to proceed. The CPU then inputs bits QØ-Q6 and $\overline{Q7}$ as its data. Q7 is complemented to produce a two's complement binary code and allow straightforward bipolar operation.

Digital Output

When the digital output from the CPU to port Ø occurs, data flows from the DO bus through IC26 and IC35, bus buffers, to the port latches IC1 and IC2. Decoder IC13 then uses $\overline{PWR}$ to generate an output strobe and latch the data into IC1 and IC2.

The digital output data is available on contacts 14 through 21 of the top edge connector. The output strobe signal is available on contact 13 of this connector.

Digital Input

When digital input from port Ø to the CPU occurs, IC13 generates an input strobe to the tristate bus drivers IC16, IC27, and IC36. The digital input data is then passed directly to the DI bus.

Digital input data is applied to the D+7A I/O Module on contacts R through Y of the top edge connector. An input strobe signal is available on contact P of this connector.

TECHNICAL SPECIFICATIONS

Computer

Known computibility with ALTAIR, IMSAI, and CROMEMCO machines using 8080 and Z80 CPU's at 2 or 4 MHZ.

Digital Port

Standard TTL signal levels
Input 8 bits – one TTL equivalent load
Output 8 bits – can drive up to 10 TTL loads
Logic levels
  >+2.0V – logic 1
  <+0.8V – logic Ø

Strobes – output is normally a logic 1 state
  Trailing edge of a pulse to logic Ø state indicates occurrence of data transfer.
  Separate input and output strobes.
  Output 8 data bits are latched.

Analog Port

(after calibration; typical values)

Signal levels for standard configuration:
  +2.54V – 01111111 - .02V – 11111111
  + .02V – 00000001 -2.54V – 10000001
  0.0V – 00000000 -2.56V – 10000000
  Two's complement code
Data Input.
  Absolute Maximum allowed ±5.0V
  Input impedance
    Z_{in} = 20MΩ ‖ .001μf, 1KHZ sample rate
    Z_{in} = 2MΩ ‖ .001μf, 10 KHZ sample rate;
  Recommended source impedance R_S<10KΩ
  Input bias current $|I_B|$ <2 μA and flows into inputs
  Accuracy ± 1 LSB
  No missing codes
Data Output.
  Maximum load current $|I_L|$ ≤1.5mA
  $R_L$min ≥ 2KΩ
  Output impedance Z_{out} <.25Ω, F ≤10KHZ
  Accuracy ± 1 LSB when refreshed
  Drift rate $\left|\frac{dv}{dt}\right|$ <10mV/sec at 25°C

Source Impedance Effects

The analog inputs have a DC input impedance and bias current that are a function of the sampling rate for the port under consideration. At a 10KHZ sampling rate, R_{IN}=2MΩ and I_B=-.2μA. These values vary inversely with the sampling rate. To prevent loss of gain accuracy and zero offset, a maximum source impedance of 10KΩ is recommended for most applications. If the signal port will be digitized at the maximum rate of 100KHZ or so, the signal source should have R_S < 100Ω. This requirement also stems, in part, from frequency response limitations imposed by the 1KΩ resistor and 0.001μf capacitor on each analog input. These components give some protection to the multiplexer in general purpose applications and may be omitted if the user is especially careful about static voltage, discharges, and overvoltage inputs. Usually only the capacitor must be removed. This is recommended for best accuracy on high frequency inputs. If sampling rates of 100HZ or less are used, the analog inputs may be treated as an essentially infinite input impedance and used accordingly.

Input Accuracy

Since the analog input has a very high input impedance, and is commutated among the input ports with a low impedance multiplexer, all input channels track very closely when attached to a common voltage source. They normally differ by an unmeasurable quantity. The only factor disturbing tracking is the source impedance effect as described above.

Output Accuracy

As with inputs, the analog outputs use a common set of hardware down to the point where the demultiplex, sample and hold, and voltage follower activity occurs. Accordingly, the primary causes of inaccuracy are pedestal error in charging the output capacitor and offset in the voltage follower. The pedestal error has a dynamic dependence on the magnitude of voltage change for the output in question. Under worst case conditions, the pedestal error may be as much as ±3 LSB's (60mv) for a full scale voltage change of 5.12V

For smaller step changes the pedestal error diminishes rapidly in size, since it is a 2nd order phenomenon. Pedestal error can be practically eliminated by doing two outputs of the same value in succession when large changes occur.

Also, during steady state operation there is a static error caused by the demultiplexer switching transients. This causes a nonlinearity evidenced by the full scale positive output being slightly high (~20mv) when the zero and full scale negative outputs are correct. This error term is a function of the internal demultiplexer construction.

Offset voltage in the voltage follower for each analog output adds directly to the output for that channel. Typically, this is less than 8 mv (< 1/2 LSB) for the CA3140 devices, so no offset adjustment is provided on a per channel basis. In applications requiring careful channel matching, the CA3140's may have to be rearranged or selected to give the desired performance. Alternately, offset adjustment pots can be added according to the manufacturer's data sheet.

Output Drift

Since the analog outputs use a sample and hold to retain the output voltage after each output action, periodic refreshing of the capacitor voltage is necessary. The typical drift rate is < 10mv/sec at 25°C, requiring refresh at a rate of 1HZ or faster. In continuous control situations this usually doesn't cause a problem since the feedback iteration rate is faster. Incidentally, 10mv/sec drift corresponds to a total leakage of 20×10^{-12} amperes from the capacitor. Therefore, cleanliness of the printed circuit board is essential for good operation. The drift rate exhibits a strong dependence on temperature, increasing rapidly at high temperatures.

If problems with excessive drive occur, first try interchanging the associated CA 3140 with one from a good port location. If the drift is not reduced, then exchange the input and output CD4051 multiplexer IC's. The input multiplexer location is much more tolerant of leakage currents. Persistent problems with drift indicate either a defective holding capacitor or contamination on the capacitor or associated printed circuit board area.

Bipolar/Unipolar Operation

The D+7A I/O Module is normally used for analog voltages in the range of -2.56 to +2.54 volts. Since both positive and negative voltages are included in this range this is referred to as "bipolar operation." Bipolar operation is selected by a trace on the printed circuit board connecting the "polarity" pad to the "bipolar" pad.

If you desire unipolar operation (0 to 2.54v or 0 to -2.56) this is also possible. Simply sever the trace connecting "polarity" to "bipolar" and in its place install a jumper from "polarity" to "unipolar." See Table 5 for proper resistor values with this mode of operation.

Table 5
Input Scaling Component Values

MODE	R22	R5	R7 & R20	R12	R14	VOLTAGE
BIPOLAR	OMIT	500	2.7 K	500	5.1 K	-2.56 to 2.54
+ UNIPOLAR	100K	200	1.3 K	20K	39 K	0 to 2.54
- UNIPOLAR	OMIT	200	1.3 K	200	2.4 K	-2.56 to 0

APPLICATIONS INFORMATION

Setting the Analog Voltage Range

In its standard configuration the D+7A I/O Module is designed to be used with analog voltage levels from -2.56 volts to +2.54 volts. Minor modification can be made to accommodate other voltage ranges. Bipolar (both positive and negative voltages) or unipolar (voltages of just one polarity) operation can be selected by a jumper wire. Normally bipolar operation is selected by the printed circuit board trace connecting "polarity" to "bipolar. ' Unipolar operation is selected by cutting this trace and installing a jumper wire between "polarity ' and "unipolar" on the printed circuit board.

In either unipolar or bipolar operation the analog inputs and outputs may be scaled to select the desired voltage range.

Input Scaling

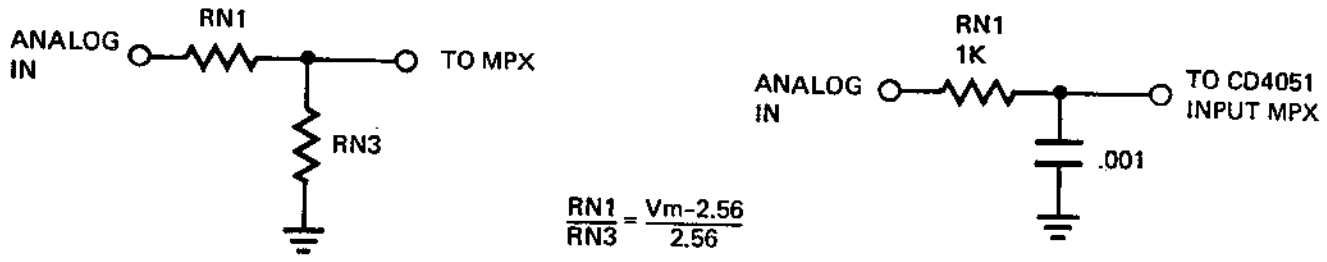
The nominal input voltage range is -2.56V to +2.54V. This can be altered for unipolar operation or larger bipolar voltage ranges. The component values of Table 5 tell what resistor values to alter for unipolar operation. Note that the input voltage range must lie between ±2.56V to prevent saturation problems in the multiplexers and buffer amplifiers. However, resistor dividers may be added at the appropriate points to permit input ranges to ±100V and output ranges to ±10V. The only restriction is that all inputs and outputs must be of the same type, i.e., unipolar or bipolar, as this is determined by the bipolar/unipolar jumper wire selection.

When the nominal maximum converter input is 2.56 volts, the input bypass capacitor may be replaced by a resistor RN3. The resistors RN1 and RN3 then form a voltage divider to reduce the maximum input Vm to 2.56 volts according to the equation in figure 6. The PCB layout allows substitution of a resistor DIP network for the capacitors if all inputs are to be similarly scaled. When all inputs are scaled to the same sensitivity, the A/D gain and offset adjustments may be used to alter the basic ADC range. This permits use of standard resistor values for RN1 and RN3.

In order to preserve the ADC accuracy in critical gain matched applications, the input divider RN1 and RN3 must be metal film devices with a ±0.1% tolerance. Most engineering applications will allow use of 1% resistors. Type RN55C metal film resistors are preferred. This gives an absolute channel input accuracy of ±2% worst case. Hobby and error feedback applications may permit use of 5% tolerance resistors.

It is recommended that the parallel combination of RN1 and RN3 be kept below 10K ohms. This may be easily done by always using RN3=10K ohms. Then for Vm=10 volts, use RN1=28.7K ohms as the nearest common 1% value. When using this divider, be careful that its equivalent 40K ohm input impedance does not seriously load the signal source.

Figure 6 Input Scaling



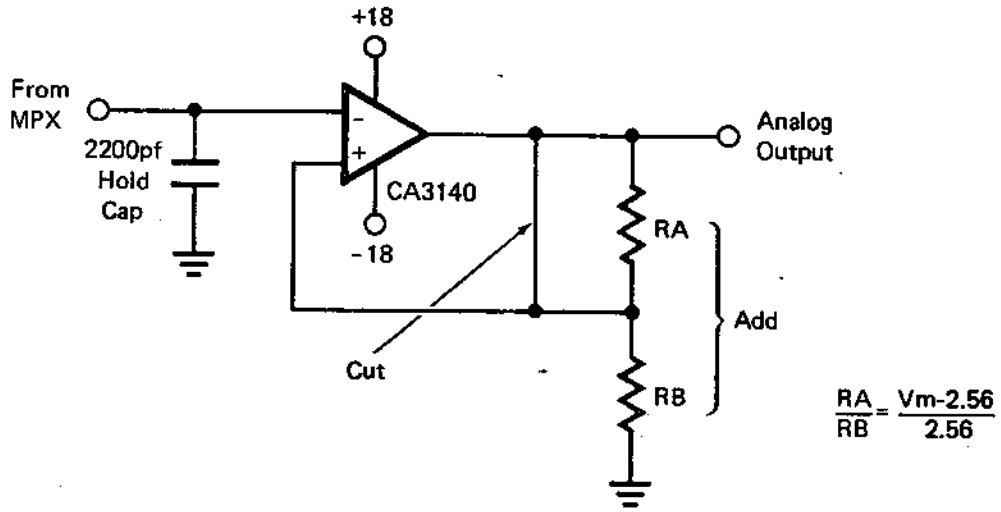
Output Scaling

The sample and hold output amplifiers are presently configured as unity gain voltage followers for ±2.56 V maximum output. If greater output is desired, such as ±10V, two changes must be made. First the amplifiers are connected to the +18 and -18 voltage busses for power to allow larger output swings. Second, a feedback voltage divider as shown in figure 7 permits gain in the voltage follower.

Changing the amplifiers to ±18V power requires cutting the power traces on the PCB and installing appropriate jumpers. Pads are provided for installation of resistors RA and RB. A trace on the PCB solder side must be cut to permit RA to function.

The equations for RA and RB are identical to the input divider equations, and similar resistor values are required. Again, 10K ohms is a good nominal value for RB, making RA=28.7 ohms for Vm=±10V maximum output.

Figure 7 Output Scaling



Using the D+7A With Cromemco Dazzler

If the Cromemco Dazzler is being used to display a picture when the D+7A I/O Module is used to input or output analog data, a small modification must be made to REV B and REV B-1 series of the Dazzler to avoid flashes in the picture. The modification is simply to remove pin 10 of Dazzler IC 29 (a 7400 IC). No modification is required to REV C Dazzlers.

Using the D+7A With Joystick Console

Cromemco is pleased to announce a new joystick console (model JS-1) designed specifically to interface to your computer using the D+7A I/O Module. In fact two such consoles can be completely interfaced using just one D+7A I/O Module. Each console consists of a two-axis joystick, four push-button control switches, and a speaker with amplifier. The schematic diagram of the joystick console is shown in figure 8. A wiring connection diagram, figure 9, shows exactly how two joystick consoles can be connected to the top edge connector of the D+7A I/O Module.

Figure 8 Joystick Schematic Diagram

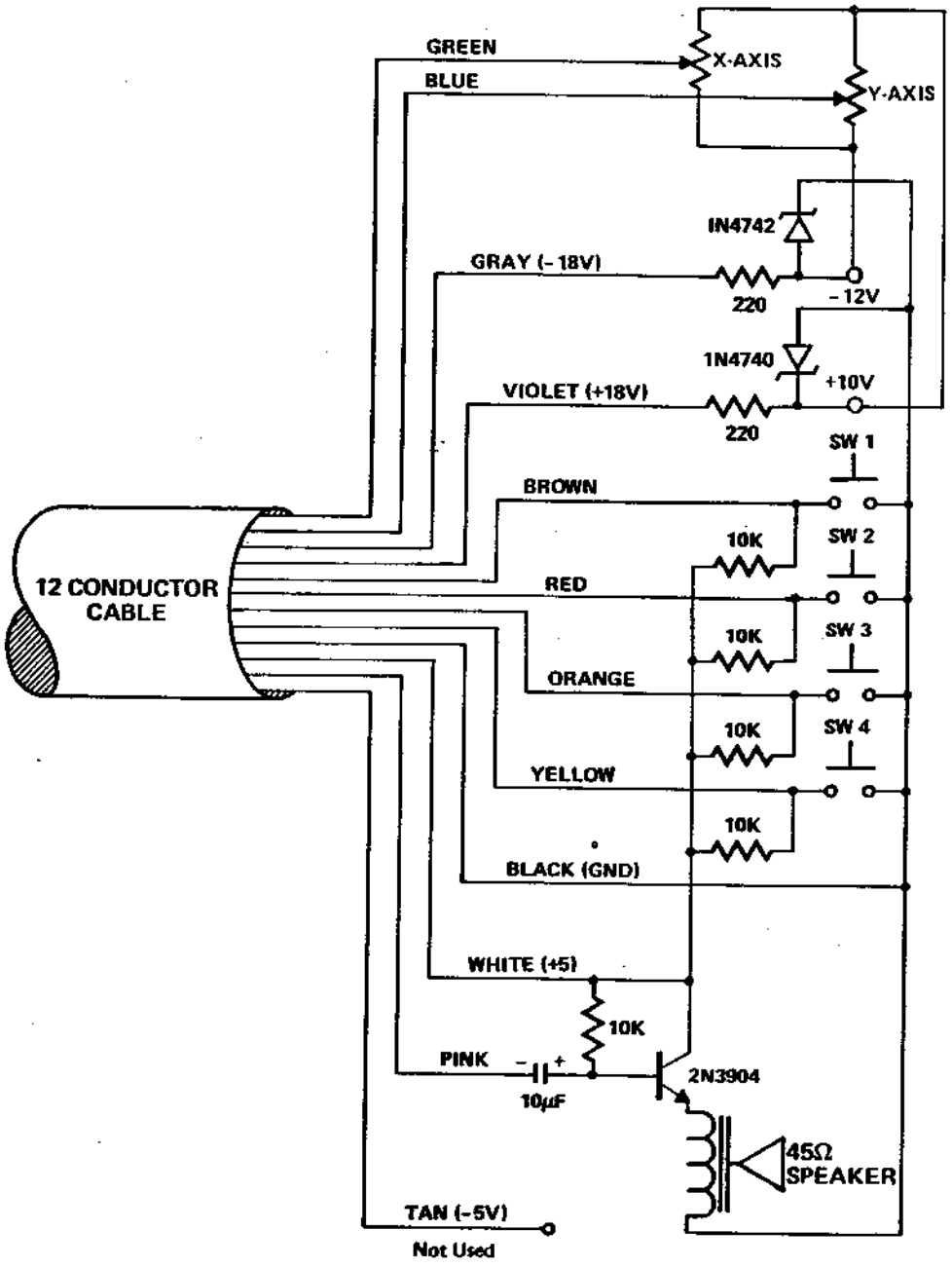
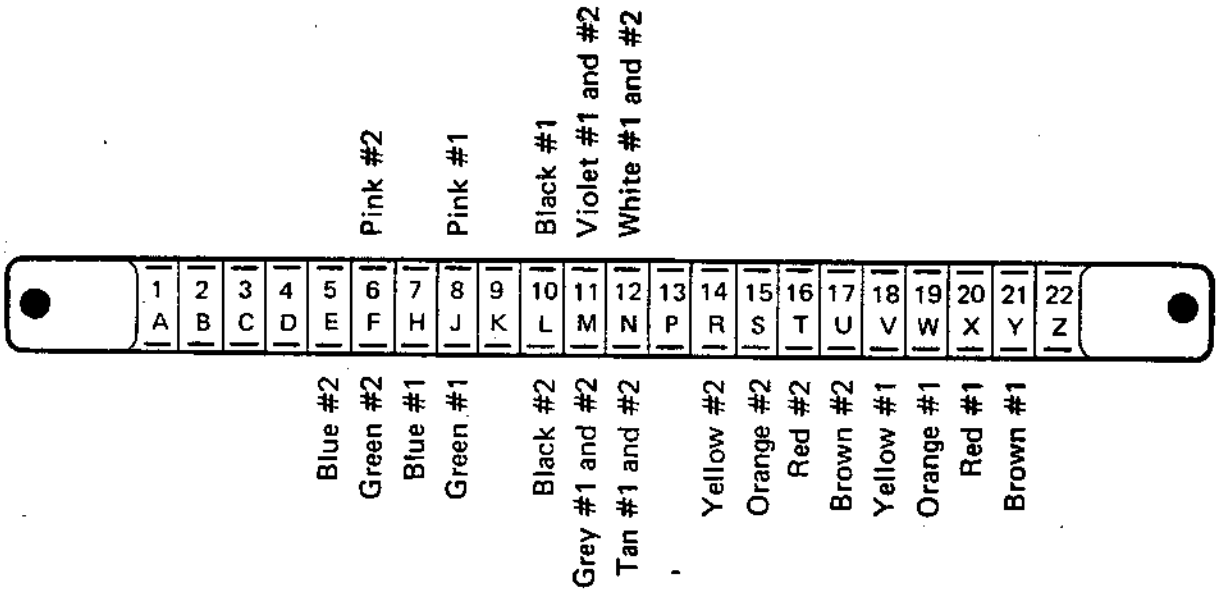


Figure 9 Joystick Wiring Diagram



Either one or two JS-1 consoles may be interfaced to a computer using the Cromemco D+7A interface. The diagram above shows how to connect two joystick consoles (#1 and #2) to the top edge connector of the D+7A interface card. The colors correspond to the color of the wires in the 12-conductor cable from each joystick.

PARTS LIST

1) Voltage Regulators and Hardware
IC 3 – LM340T-5.0 (7805)
IC 6 – 78L05
IC28 – LM320T-5.0 (7905)
2 – 6-32 x 3/8 screws
2 – 6-32 nuts
2 – #6 lock washers
2 – Heatsinks

2) IC Sockets
12 – 14 pin
16 – 16 pin
2 – 8 pin

3) Integrated Circuits
IC 1 – 74175
IC 2 – 74175
IC 4 – 3130 or 3140
IC 5 – 3130 or 3140
IC 7 – 3130 or 3140
IC 8 – 3130 or 3140
IC 9 – 4051
IC 10 – LM301
IC 11 – 72710 or 72810
IC 12 – MC1408L8
IC 13 – 7442
IC 14 – 74LS02
IC 15 – AM2502PC
IC 16 – 74367
IC 17 – 3130 or 3140
IC 18 – 3130 or 3140
IC 19 – 3130 or 3140
IC 20 – 4051
IC 21 – 310
IC 22 – 4066
IC 23 – 74LS30
IC 24 – 74LS08
IC 25 – 74LS10
IC 26 – 74LS157
IC 27 – 74367
IC 29 – 74LS04
IC 30 – 7474
IC 31 – 7474
IC 32 – 74LS04
IC 33 – 74LS32
IC 34 – 74LS04
IC 35 – 74LS157
IC 36 – 74367

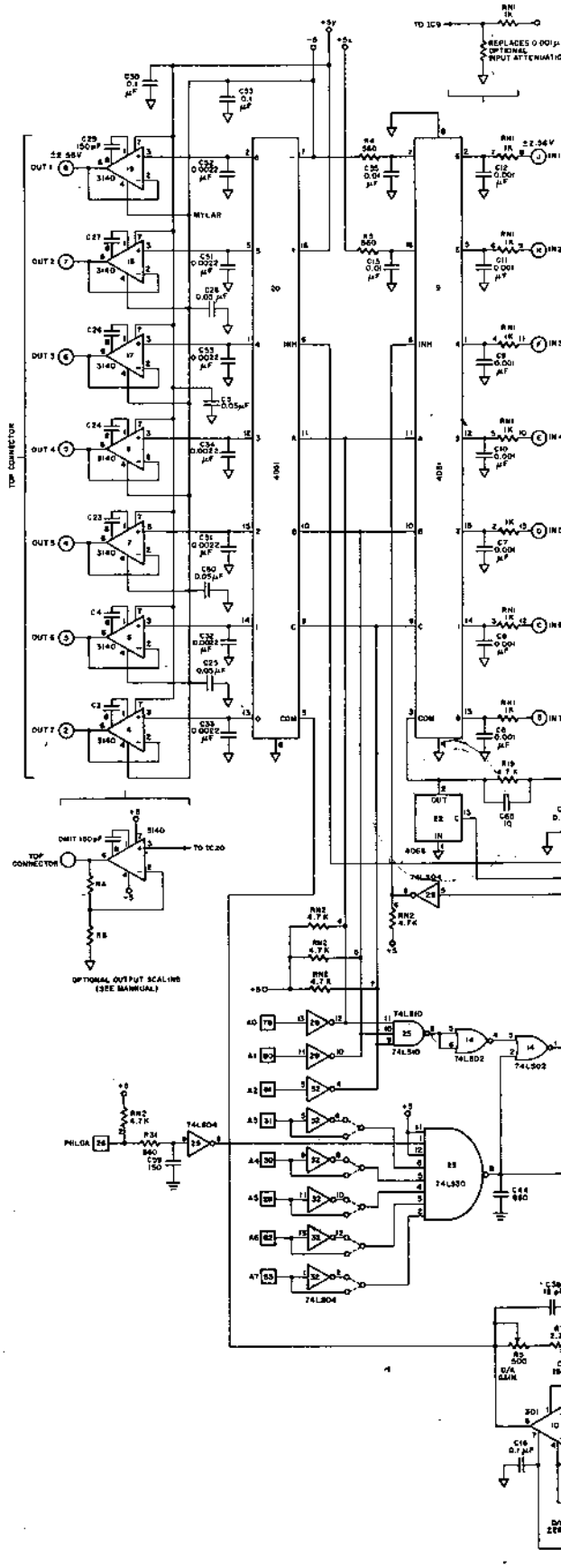
4) Resistors and Discrete Semiconductors
R1 – 470
R2 – 25k pot
R 3 – 560
R 4 – 560
R 5 – 500 pot
R 6 – 100K
R 7 – 2.7k
R 8 – 2.2k
R 9 – 2.7k
R 10 – 500 pot
R 11 – 2.4k
R 12 – 500 pot
R 13 – 2.4k
R 14 – 5.1k
R 15 – 10
R 16 – 10
R 17 – 18k
R 18 – 1k
R 19 – 4.7k
R 20 – 2.7k
R 21 – 220
R 22 – omit for bipolar operation
R 23 – 1.2k
R 24 – 2.7k
R 25 – 4.7k
R 26 – 1k
R 27 – 560
R 28 – 220
R 29 – 220
R 30 – 560
R 31 – 560
R 32 – 560
R 33 – 560
R 34 – 560
R 35 – 1.5k
RN 1 – 14 pin dip 7 resistors 1k
RN 2 – 8 pin sip, 7 resistors, 4.7k
D 1 – 1N914
D 2 – 1N914
D 3 – 1N914
D 4 – 1N914
D 5 – 1N4742
D 6 – 1N4742
Q 1 – 2N3906

5) Capacitors
C 1 – 0.1
C 2 – 10 uF tantalum
C 3 – 150
C 4 – 150
C 5 – .05
C 6 – .001
C 7 – .001
C 8 – .001
C 9 – .001
C 10 – .001
C 11 – .001
C 12 – .001
C 13 – .01
C 14 – .05
C 15 – 0.1
C 16 – 0.1
C 17 – .05
C 18 – .05
C 19 – .01
C 20 – 0.1
C 21 – 0.1
C 22 – 0.1
C 23 – 150
C 24 – 150
C 25 – .05
C 26 – 150
C 27 – 150
C 28 – .05
C 29 – 150
C 30 – 0.1
C 31 – .0022
C 32 – .0022
C 33 – .0022
C 34 – .0022
C 35 – .01
C 36 – .05
C 37 – 150
C 38 – 18
C 39 – 0.1
C 40 – 0.1
C 41 – 0.1
C 42 – 150
C 43 – 0.1
C 44 – 680
C 45 – 150
C 46 – 47
C 47 – 0.1
C 48 – 10 uF tantalum
C 49 – 10 uF tantalum
C 50 – .05
C 51 – .0022
C 52 – .0022
C 53 – .0022
C 54 – 0.1
C 55 – 0.1
C 56 – 0.1
C 57 – 47
C 58 – 0.1
C 59 – 150
C 60 – 150
C 61 – 0.1
C 62 – 47
C 63 – 0.1
C 64 – 10uF tantalum
C 65 – 10 Pf

6) Inductors
L1 – 22uH
L 2 – 22uH

7) Connector Assembly
Dual 22 contact connector, hood, assembly hardware.

8) Miscellaneous
Printed circuit board.
Instruction manual.



MODE	R22	R5	R7 & R20	R12	R14	VOLTAGE RANGE
BIPOLAR	OMIT	500	2.7K	500	4.7K	−2.56 TO + 2.56
+UNIPOLAR	100K	200	1.5K	20K	39K	0 TO + 2.56
−UNIPOLAR	OMIT	200	1.5K	200	2.4K	−2.56 TO 0

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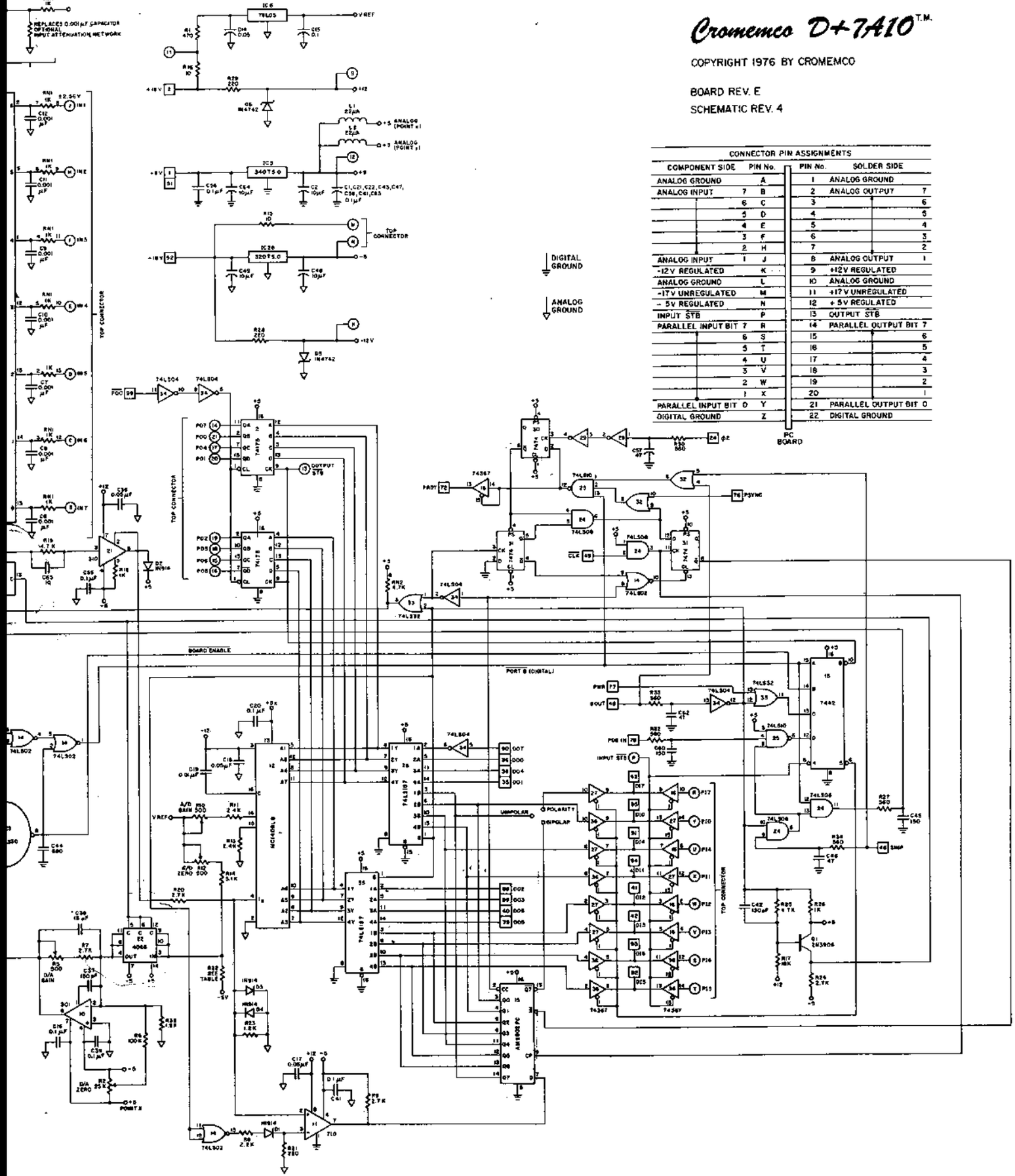
BOARD REV. E

SCHEMATIC REV. 4



CONNECTOR PIN ASSIGNMENTS				
COMPONENT SIDE	PIN No.		PIN No.	SOLDER SIDE
ANALOG GROUND		A	1	ANALOG GROUND
ANALOG INPUT	7	B	2	ANALOG OUTPUT 7
	6	C	3	6
	5	D	4	5
	4	E	5	4
	3	F	6	3
	2	H	7	2
ANALOG INPUT	1	J	8	ANALOG OUTPUT 1
-12 V REGULATED		K	9	+12 V REGULATED
ANALOG GROUND		L	10	ANALOG GROUND
-17 V UNREGULATED		M	11	+17 V UNREGULATED
- 5 V REGULATED		N	12	+ 5 V REGULATED
INPUT STB		P	13	OUTPUT STB
PARALLEL INPUT BIT 7		R	14	PARALLEL OUTPUT BIT 7
	6	S	15	6
	5	T	16	5
	4	U	17	4
	3	V	18	3
	2	W	19	2
	1	X	20	1
PARALLEL INPUT BIT 0		Y	21	PARALLEL OUTPUT BIT 0
DIGITAL GROUND		Z	22	DIGITAL GROUND

PC BOARD