Five Dollars

Cromemco

16KTP

Two Port Memory

Instruction Manual

Cromemco®

16KTP TWO PORT MEMORY

Instruction Manual

**THIS BOARD IS NOT INTENDED
FOR USE AS
A SYSTEM MEMORY BOARD.**

CROMEMCO, Inc.
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Mountain View, CA. 94043

Part No. 023-2003

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This manual was produced on a Cromemco System Three computer utilizing a Cromemco HDD-22 Hard Disk Storage System running under the Cromemco Cromix™ Operating System. The text was edited with the Cromemco Cromix Screen Editor. The edited text was proofread using the Cromemco SpellMaster™ Program and then formatted using the Cromemco Word Processing System Formatter II. Final camera-ready copy was printed on a Cromemco 3355A printer.

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Chapter 1

INTRODUCTION

The Cromemco 16KTP Two Port Memory board is designed to be used with Cromemco systems that use a Cromemco SDI graphics interface. Together with a high resolution RGB color monitor such as the Cromemco RGB-13, these boards turn a Cromemco microcomputer into a highly sophisticated graphics system.

One to six 16KTP RAM boards can be added to each SDI system as a means of storing picture information. Each 16KTP is capable of storing an entire 12K nybble-mapped or bit-mapped image. Alternatively, 3 16KTPs may be used to store an entire 48K image.

The basic SDI system configuration without the 16KTP RAM boards is shown in Figure 1.

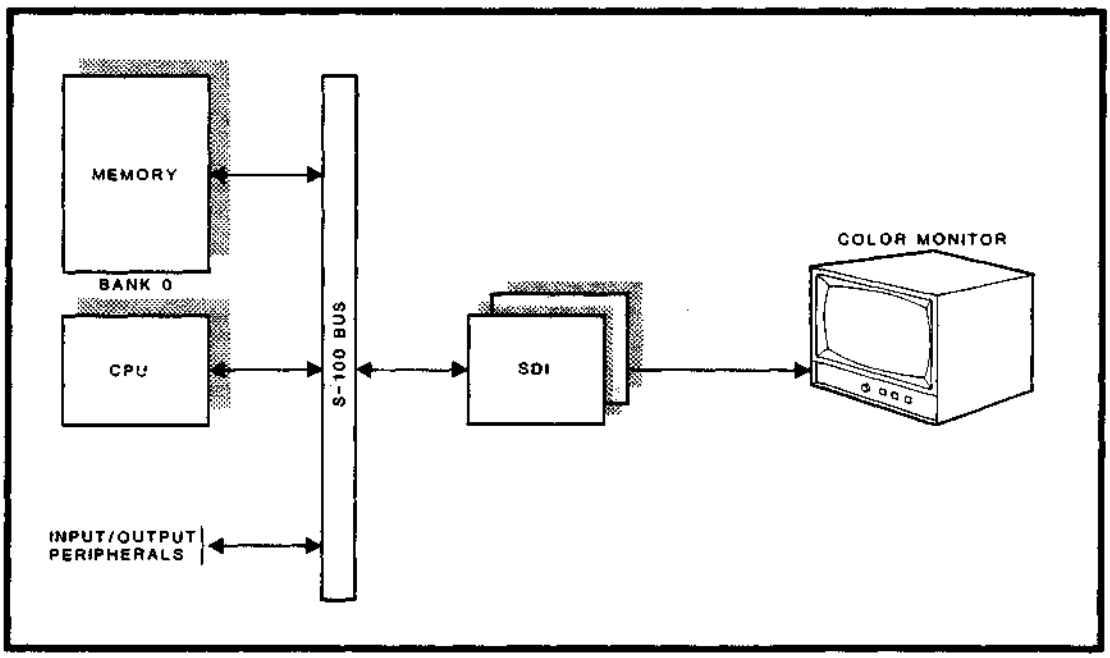

Figure 1: THE BASIC SDI SYSTEM

In this configuration the SDI scans main memory for a digitized image. When reading the picture information from main memory, the SDI must disable the ZPU up to 92% of the time. This greatly reduces execution efficiency because the ZPU must share the S-100 address and data bus lines with the SDI.

This situation is remedied with the 16KTP. The 16KTP has two sets of address and data lines (two ports) which give it the ability to process the SDI's memory refresh requests while the ZPU simultaneously and independently executes a user program. The **second port** of the 16KTP is a 50 pin connector on the top edge of the card. This allows a direct connection of the SDI with the 16KTP which bypasses the S-100 bus. The ZPU accesses the 16KTP through the S-100 bus (the **main port**) as though the SDI were not present.

One to six 16KTP boards can be employed in a single SDI system. The system configuration with six 16KTPs is shown in Figure 2.

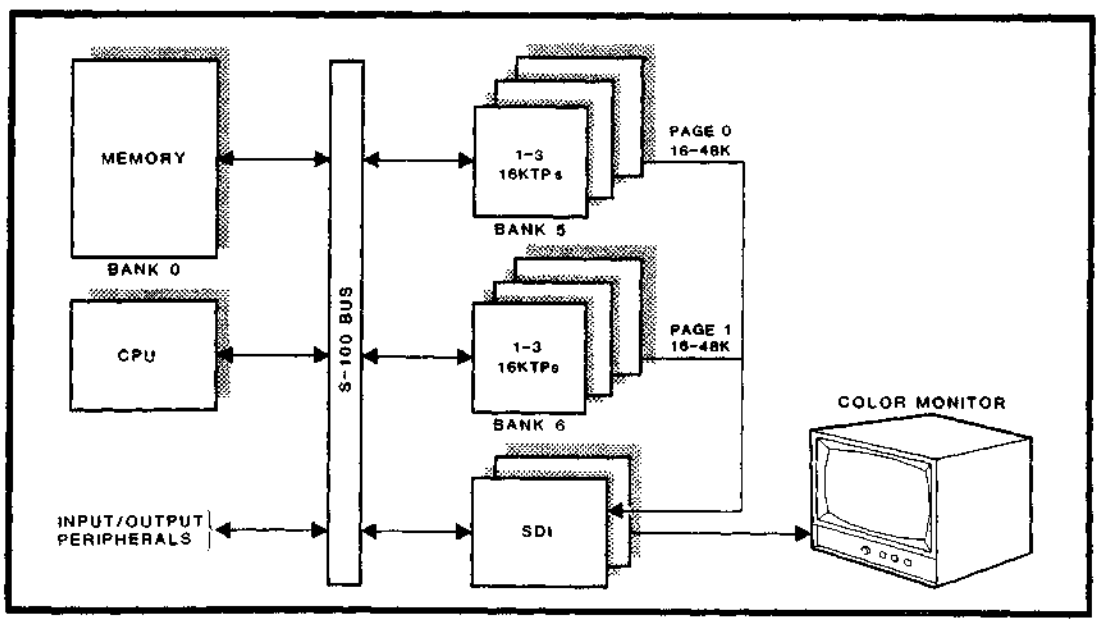

Figure 2: AN SDI SYSTEM WITH 1-16 KTP BOARDS

Chapter 2

BOARD DESCRIPTION

The 16KTP is a two port static memory board. It incorporates 200ns (4K x 1) static RAM chips in its 16K block of user memory. Also on board is all the logic necessary to service read and write requests from the host (S-100 bus) and read and write requests from the SDI (second port).

The 16KTP contains an external connector on the edge opposite the S-100 plug. This connector, a 50 pin connector, allows a **top edge** interface to the SDI. By connecting the 16KTP to the SDI-D with 50 conductor ribbon cable, data and timing information can be communicated between the two boards. The address requests to the 16KTP as well as the picture data to the SDI are passed through the 50 conductor cable.

There are 3 switch groups on board the 16KTP. SW-2 indicates to the host which banks the 16KTP appears in. Switches SW-1 and SW-3 establish information regarding the relationship between the 16KTP and the SDI as well as address information and other features. These switches, for example, determine which page of image memory the 16KTP occupies with respect to the SDI and what 16K block of memory the board is addressed as. The SDI can support two 48K pages, page 0 and page 1. The selection of frame buffer page is independent of bank selection.

Chapter 3

STANDARD SYSTEM CONFIGURATION

For most CDOS applications (and in particular when using Cromemco CDOS software) a standard system configuration with regard to bank placement and switch settings should be observed. In this configuration, the main user bank (hereafter referred to as host memory) appears in bank 0. If one page of memory (consisting of 3 16KTPs) is used, it should appear in bank 5 and from the point of view of the SDI appear as page 0. If a second page of memory is used, these boards should be set to bank 6 and appear to the SDI as page 1. Both 48K pages (if two are present) should be addressed from 4000h to FFFFh, i.e., the upper 48K of memory. This means that when 3 16KTPs are used to comprise a single page, their base addresses should be 4000h, 8000h and C000h respectively. Finally, because of the 16KTPs special memory disable feature, the host memory, bank 0, should be set to also appear in bank 5, if SDI page 0 is present, or banks 5 and 6, if both SDI pages (0 and 1) are present. This apparent memory overlap is allowed because the 16KTP disables all memory which lies in its bank and memory area while the 16KTP is being written into or read from. This system configuration is summarized in Figure 3 and Table 1. The switch settings for this configuration are shown in Figure 4.

For the Cromix Operating System, the only switch settings which change are those that set the Host address. Instead of the cards appearing in banks 5 and 6 at addresses 4000 (Block 0), 8000 (Block 1) and C000 (Block 2); for Cromix they must be at addresses 0000 (Block 0), 4000 (Block 1) and 8000 (Block 2). The switch changes affect SW-3, 1 and 2 only.

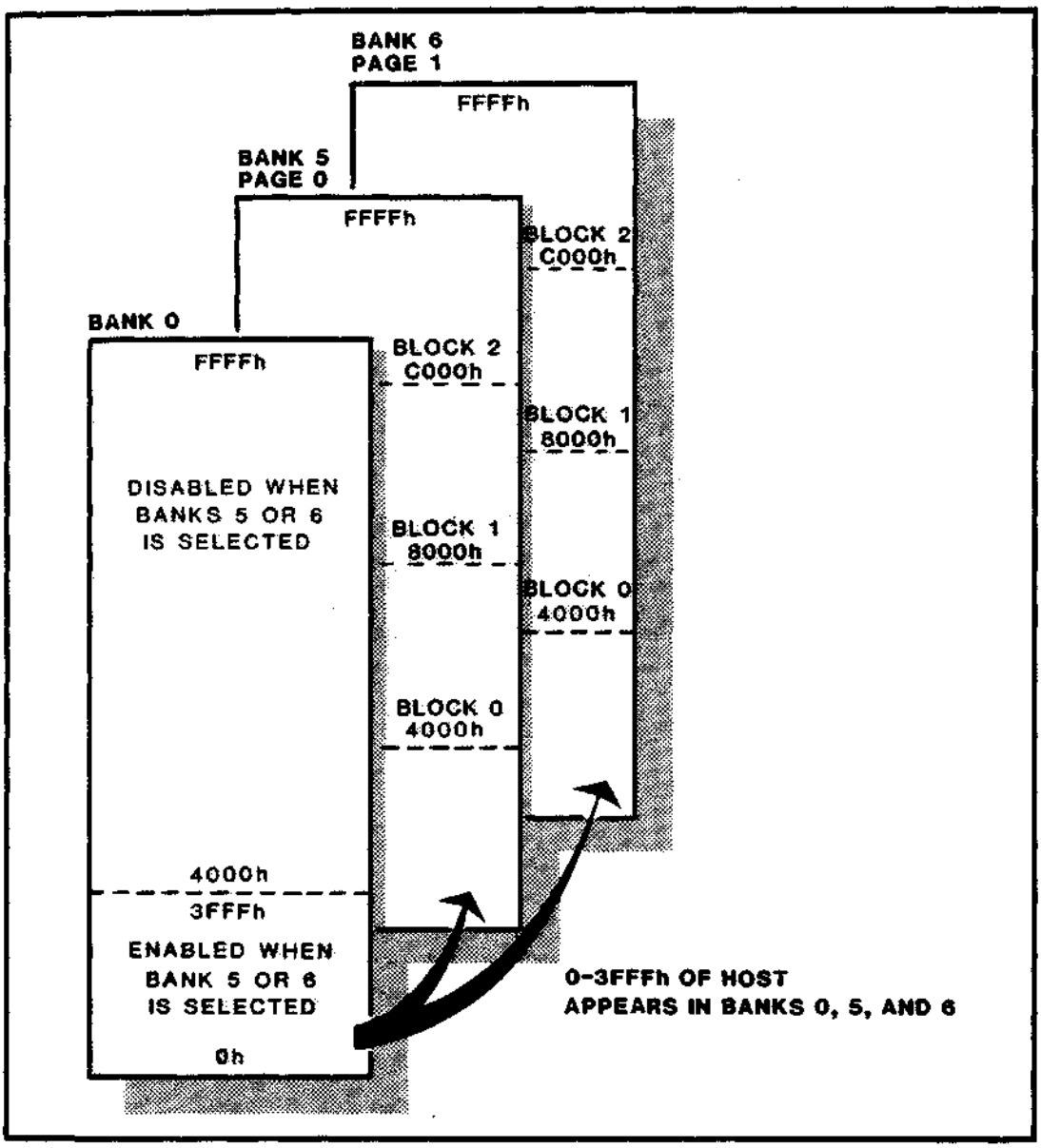

Figure 3: CDOS SYSTEM WITH SIX 16KTPs

Table 1

STANDARD SYSTEM CONFIGURATION WITH TWO 16KTPs

	Size	Appears in banks:	Addressed as:	Appears to SDI as:
Host memory	64K	0,5,6	0-FFFFh	------
1st 16KTP	16K	5	4000h-7FFFh	page 0 block 0
2nd 16KTP	16K	5	8000h-BFFFh	page 0 block 1
3rd 16KTP	16K	5	C000h-FFFFh	page 0 block 2
4th 16KTP	16K	6	4000h-7FFFh	page 1 block 0
5th 16KTP	16K	6	8000h-BFFFh	page 1 block 1
6th 16KTP	16K	6	C000h-FFFFh	page 1 block 2

From the point of view of the graphics programmer, the host memory from 4000h to FFFFh will appear only in bank 0. Thus, when it is necessary to switch to bank 5 or bank 6 in order to manipulate the image memory, that portion of the program which handles the bank select and subsequent image manipulation must be located in host memory below 4000h. This is because host addresses 0-3FFFh appear in banks 5 and 6; when these banks are selected any program segment which appears in this address range will continue to operate. A typical organization of software for the SDI/16KTP system is shown in Figure 3.

.1 INSTALLATION OF THE 16KTP

1. Verify that the SDI board set is properly installed in the system (refer to the SDI manual for switch settings and installation instructions).

2. Copy the switch settings of Figure 4 onto all of the 16KTPs and also onto the bank select switch of the host memory card(s).

3. Connect 1 plug of a 50 pin ribbon cable to connector J-1 of the 16KTP, leaving the other plugs free. If more than one 16KTP is present, use a single cable/multi plug ribbon connector and plug this cable into each 16KTP leaving at least one plug free.

4. Insert all 16KTPs into the system in the vacant slots adjacent the SDI-D board, with the free cable ends toward the SDI-D.

5. Plug the 50 conductor cable free end into connector J-2 of the SDI-D.

The 16KTP boards are now installed in the system.

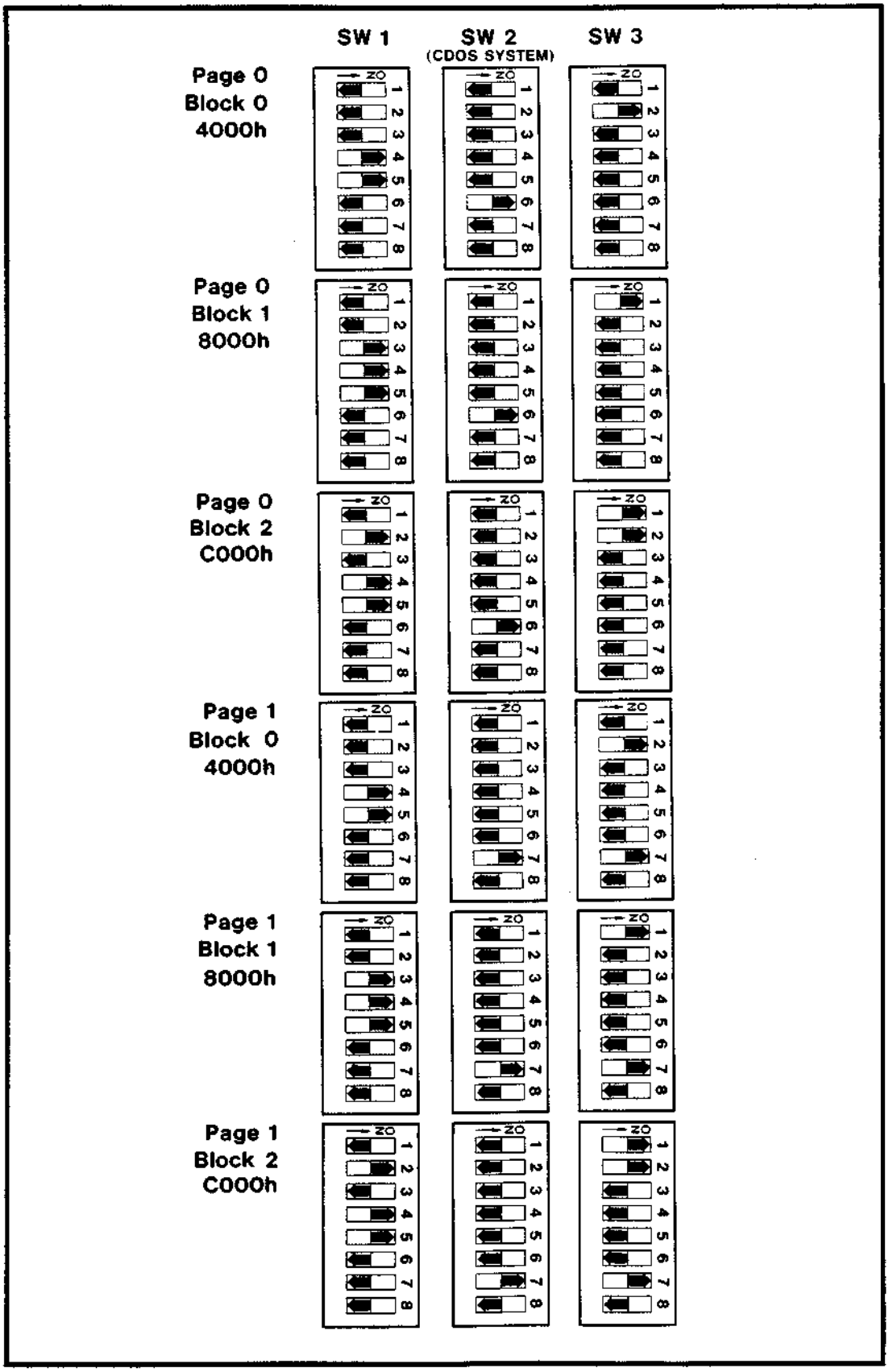

Figure 4: STANDARD SWITCH SETTINGS FOR THE 16KTPs AND HOST MEMORY

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SWI

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Bit

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Chapter 4

SWITCH SETTINGS

This section describes the use of each 16KTP switch in detail. Reference is made to the previous section if a standard Cromemco graphics system configuration is employed. An outline of the 16KTP board showing the location of the three switch groups is shown in Figure 5.

SWITCH GROUP SW-1

Bit 1 (preset)

If this switch is on, the 16KTP will be active after reset. If off, the board will be off (unselected). Off is the standard position.

Bits 2 and 3 (second port block)

These bits determine which of the 4 16K blocks the 16KTP will reside in from the second port point of view.

Bit 2 (MSB)	Bit 3 (LSB)	Block
0	0	0
0	1	1
1	0	2
1	1	3 (not used)

0 = switch "OFF"
1 = switch "ON"

Bit 4 (memory access priority)

This bit, in conjunction with SW1-8, determines the circumstances under which the ORRQ (override request) signal of the second port will be asserted by the 16KTP. If the second port controlling device chooses to ignore the ORRQ signal, then the Host cannot gain access to the 16KTP and must wait (PRDY will become not ready, or low).

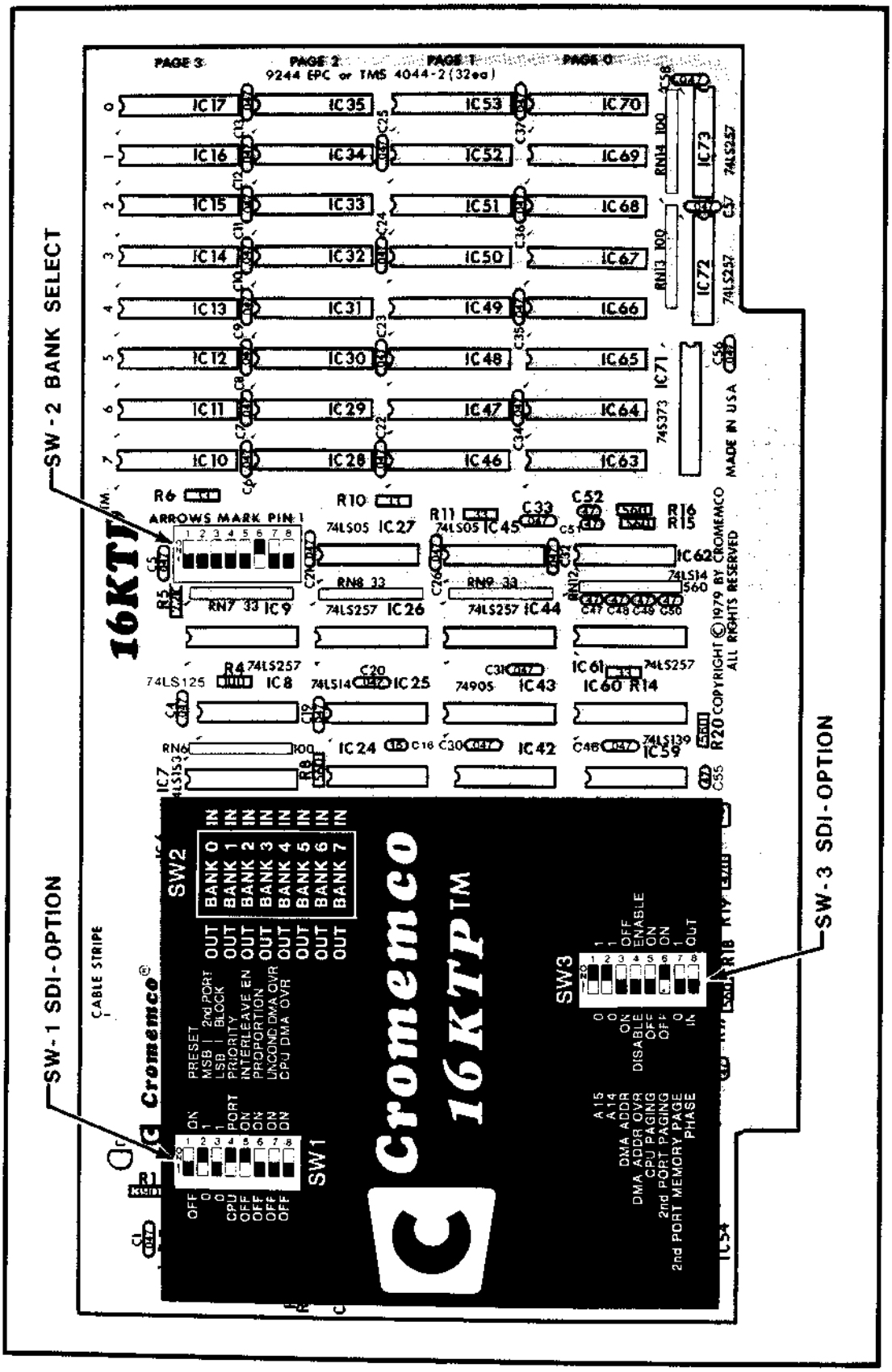

Figure 5: 16KTP SWITCH LOCATIONS

SW1 8	BIT 4	ORRQ Asserted On
OFF	OFF	All Host accesses.
OFF	ON	Nothing. ORRQ disabled.
ON	OFF	All Host accesses.
ON	ON	Host DMA accesses only.

Bit 5 (interleave enable)

When on, this bit allows the interleaving of picture data from the second port. That is, when used with the SDI, data may be read from this board, or another board which is identically addressed but occupying a different page. Usually in the on position, this bit enables the SDI to perform its windowing function.

Bit 6 (proportion)

For 8080 systems. Leave "OFF".

Bit 7 (unconditional DMA override)

If SW-1 bit 8 (see below) is "ON", then this switch when "ON" disables the second port during Host DMA into or out of the 16KTP. Applies to Host DMA accesses only.

Bit 8 (CPU or DMA override)

The bit (switch) when "ON", enables the functioning of SW1-4 and SW1-7. If "OFF", SW1-7 is effectively "OFF".

.2 **SWITCH GROUP S-2**

This switch group determines the bank(s) in which the 16KTP resides. Normally the 16KTP designated page 0 will be in bank 5, and the 16KTP designated page 1 will be in bank 6. The bank-switch correspondence is shown in Table 2.

Table 2: BANK-SWITCH CORRESPONDENCE

Switch Number	Bank
1	0
2	1
3	2
4	3
5	4
6	5
7	6
8	7

4.3 SWITCH GROUP S-3

Bits 1 and 2 (A15 and A14)

These bits determine the base address of the 16KTP as viewed from the host. The options are:

Bit 1 (A15)	Bit 2 (A14)	Base Addr.
0	0	0000h
0	1	4000h
1	0	8000h
1	1	C000h

0 = switch "OFF"
1 = switch "ON"

Bits 3 and 4 (host DMA controls)

The standard operation of the 16KTP is with both of these bits in the off (0) position. In this case the 16KTP responds to a host DMA request if it is in the selected bank, otherwise it will not respond.

Two alternative situations are:

1. 16KTP ignores **all** host DMA requests regardless of bank (bit 3 = off, bit 4 = on).

2. 16KTP responds to **all** host DMA requests regardless of bank (bit 3 = on, bit 4 = on).

SW1 BIT 8	4	ORRQ Asserted On
OFF	OFF	All Host accesses.
OFF	ON	Nothing. ORRQ disabled.
ON	OFF	All Host accesses.
ON	ON	Host DMA accesses only.

Bit 5 (interleave enable)

When on, this bit allows the interleaving of picture data from the second port. That is, when used with the SDI, data may be read from this board, or another board which is identically addressed but occupying a different page. Usually in the on position, this bit enables the SDI to perform its windowing function.

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Two alternative situations are:

1. 16KTP ignores **all** host DMA requests regardless of bank (bit 3 = off, bit 4 = on).

2. 16KTP responds to **all** host DMA requests regardless of bank (bit 3 = on, bit 4 = on).

These possibilities are summarized in Table 3.

Table 3: HOST DMA OPTIONS

Bit 4 DMA override enable	Bit 3 DMA on/off	Effect
Off	No Effect	16KTP behaves like "normal" host memory
On	Off	16KTP ignores all host DMA requests
On	On	16KTP responds to all host DMA requests

Bit 5 (CPU paging)

Bits 6 and 7 (second port paging and second port page select)

In order to have the 16KTP respond to a particular page request from the SDI, bit 6, page enable, must be in the "on" position. If bit 6 is in the "off" position, the 16KTP will not differentiate between page 0 and page 1 requests and thus will respond to all accesses from the second port when of the correct block.

When bit 7 is in the "on" position the 16KTP will respond to either page 0 access or page 1 access from the second port (SDI). The determination of which page the RAM responds to is fixed by bit 7 - page 0 or 1. Page 0 is selected by bit 8 in the OFF position. Page 1 is selected by bit 8 in the ON position.

Bit 8 (Phase)

Don't wonder, leave "OFF".

Chapter 5

CONNECTIONS BETWEEN THE 16KTP AND THE SDI

The 16KTP contains provisions for a separate cable connection to the SDI. The pin group on the card edge, labelled J-1, is shown in Figure 6.

The connector J-1 is the main data and address transmission line to the SDI. The SDI sends address requests to the 16KTP through this connection, and the 16KTP responds by sending data back to the SDI, also through J-1. The details are shown below.

1. GND	2. EDO0*
3. EDO1*	4. EDO2*
5. EDO3*	6. EDO4*
7. EDO5*	8. EDO6*
9. EDO7*	10. GND
11. EDI0	12. EDI1
13. EDI2	14. EDI3
15. EDI4	16. EDI5
17. EDI6	18. EDI7
19. GND	20. EA0
21. EA1	22. EA2
23. EA3	24. EA4
25. EA5	26. EA6
27. EA7	28. EA8
29. EA9	30. EA10
31. EA11	32. EA12
33. EA13	34. GND
35. SREQ0	36. SREQ1
37. SREQ2	38. SACK 0
39. SACK 1	40. SACK 2
41. ER0	42. ER1
43. ER2	44. ORRQ
45. PG1	46. ORACK
47. EW0*	48. EW1*
49. EW2*	50. GND

* SDI-D not connected to these lines.

SECOND PORT CONNECTOR J-1 PIN FUNCTION DESCRIPTIONS

Pin	Functions
2-9	EDO0-7 The second port write data bus.
11-18	EDI0-7 Second port read data bus
20-33	EA0-13 Second port address bus. These lines are the same as address lines A0-A13. The memory block (i.e., the 16KTP being accessed) is determined through pins 35-37.
35-37	SREQ0-2 These low active lines select the 16KTP being accessed. They are decoded so that only one is active at any given time.
38-40	SACK 0-2 This signal is generated by the second port memory device after receiving a SREQ0-2 signal with ORACK high. The SACK signal states that the selected two port memory device (in this case, a 16KTP) has switched over to its second port and that the second port memory cycle can start immediately. From the reception of this signal, it is 220ns minimum until the end of the memory cycle.
41-43	ER0-2 These low active lines enable second port read data onto the second port bus from the selected Two Port RAM. They enable the data buffer.
45	PG1 This line selects either the first 48K of second port memory when low (PAGE0) or the second 48K of memory (PAGE1) when high.
44,46	ORRQ, ORACK These lines work in conjunction with SW-1 on the DMA board of the SDI board set. If the override enable switch of SDI-D SW-1 is on, then an override request on pin ORRQ generated by the 16KTP will cause the SDI to temporarily stop driving the Two Port RAM. The second port signal ORRQ, is generated in accordance with the setting of switch 1 bits 4 and 8 (see Section 4.1, SW1). The ORACK line

is used by the controlling second port device to signal that an override is O.K. This is done by driving the line low. If ORACK is not taken low, then the HOST DMA device must WAIT because the HOST WAIT line will become active (low), or the DMA device will not read or write its data correctly. The ORRQ line should be pulled up to 5v through a 10K ohm resistor on the second port controlling device.

47-49 EW0-2

These low active lines allow the second port device to write a byte into the addressed RAM location of the selected block (0, 1 or 2). The EW0-2 signal must not go low before the respective SACK0-2 signal has been received from the 16KTP.

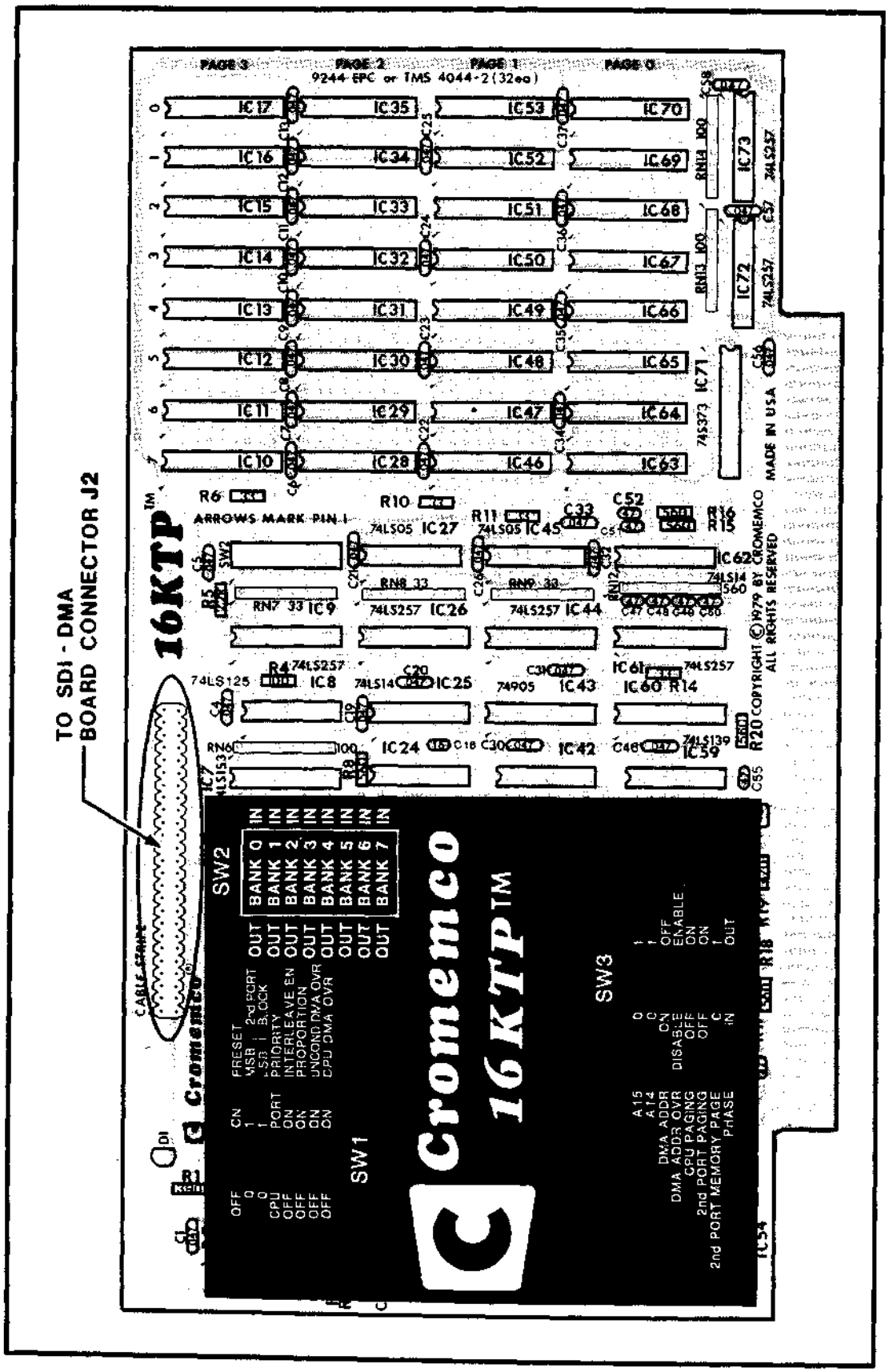

Figure 6: CABLE CONNECTIONS TO THE 16KTP

PARTS LIST

Designation	Description	Cromemco Part No.
Integrated Circuits		
IC1	74S241	010-0088
IC2	74LS08	010-0064
IC3	74S04	010-0123
IC4	74LS00	010-0069
IC5	74LS74	010-0055
IC6-7	74LS153	010-0048
IC8	74LS125	010-0127
IC9	74LS257	010-0124
IC10-17	9244/9044	011-0013
IC18	7805/340T-5	012-0001
IC19	74S32	010-0090
IC20	74LS74	010-0055
IC21	74LS164	010-0043
IC22	74S02	010-0122
IC23	74LS27	010-0112
IC24	74LS32	010-0058
IC25	74LS14	010-0061
IC26	74LS257	010-0124
IC27	74LS05	010-0065
IC28-35	9244/9044	011-0013
IC36	7805/340T-5	012-0001
IC37	NON TI 74LS04	010-0066
IC38	74LS74	010-0055
IC39-40	74LS00	010-0069
IC41	74LS10	010-0063
IC42	74LS27	010-0112
IC43	16 pin shunt	017-0069
IC44	74LS257	010-0124
IC45	74LS05	010-0065
IC46-53	9244/9044	011-0013
IC54	7805/340T-5	012-0001
IC55	74LS14	010-0061
IC56	74LS151	010-0049
IC57	74S86	010-0125
IC58	74LS20	010-0095

Designation	Description	Cromemco Part No.
IC59	74S02	010-0122
IC60	74LS139	010-0118
IC61	74LS257	010-0124
IC62	74LS14	010-0061
IC63-70	9244/9044	011-0013
IC71	74S373	010-0085
IC72-73	74LS257	010-0124
IC74	74S08	010-0166
IC75	74125	010-0011
Transistors/ Diodes		
Q1	2N3646	009-0000
D1	led til-211	008-0020
Capacitators		
C1-13	.047 uf axial	004-0061
C14	10 uf tant	004-0032
C15-17	.047 uf axial	004-0061
C18	15 pf mono	004-0044
C19-26	.047 uf axial	004-0061
C27	10 uf tant	004-0032
C28-37	.047 uf axial	004-0061
C38	10 uf tant	004-0032
C39	15 pf mono	004-0044
C40-43	47 pf mono	004-0000
C44-46	.047 uf axial	004-0061
C47-52	47 pf mono	004-0000
C53	10 uf tant	004-0032
C54	22 pf mono	004-0041
C55	47 pf mono	004-0000
C56-58	.047 uf axial	004-0061
Resistors		
R1	390	001-0013
R2	10 K	001-0030
R3	270	001-0011
R4	100	001-0007
R5	2.2 K	001-0021

Designation	Description	Cromemco Part No.
R6	33	001-0071
R7	330	001-0012
R8	560	001-0015
R9	27	001-0047
R10-11	33	001-0071
R12	560	001-0015
R13	330	001-0012
R14	33	001-0071
R15-16	560	001-0015
R17	10 K	001-0030
R18	560	001-0015
R19	470	001-0014
R20-21	560	001-0015
R22	1.5 K	001-0020
R23	10 K	001-0030
R24	390	001-0013
Resistor Networks		
RN1-2	100, 8 pin	003-0001
RN3-5	10K, 8 pin	003-0025
RN6	100, 8 pin	003-0001
RN7-9	33, 8 pin	003-0000
RN10	560, 8 pin	003-0006
RN11	10K, 8 pin	003-0025
RN12	560, 8 pin	003-0006
RN13-14	100, 8 pin	003-0001
Miscellaneous		
	1 connector, 50 pin	017-0033
	2 sockets, 20 pin	017-0004
	32 sockets, 18 pin	017-0003
	11 sockets, 16 pin	017-0002
	27 sockets, 14 pin	017-0001
	1 heat sink	016-0060
	3 silicon pads	021-0109
	2 2-56x5/8 screws	015-0113
	3 6-32x7/16 screws	015-0129
	3 6-32 hex nuts	015-0074
	2 3/8x3/16 spacers	015-0114
	2 #2 nylon washers	015-0115

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You should immediately notify IN WRITING your Authorized Cromemco Dealer or Cromemco of problems encountered during the warranty period. In order to obtain warranty service, first obtain a return authorization number by contacting the Authorized Cromemco Dealer from whom you purchased the product. Then attach to the product:

1. Your name, address and telephone number,
2. the return authorization number,
3. a description of the problem, and
4. proof of the date of retail purchase.

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Cromemco 16 KTP™

SCHEMATIC REV. 4

BOARD REV. F

16 KTP-040-0015

REFERENCE SYMBOLS

ASSIGNED	NOT ASSIGNED
IC1-IC75	
D1	
C1-C59	
R1-R29	
RN1-RN14	
Q1	

NOTE (UNLESS OTHERWISE SPECIFIED)
1. RESISTANCE VALUES ARE IN OHMS
2. CAPACITANCE VALUES ARE IN pF