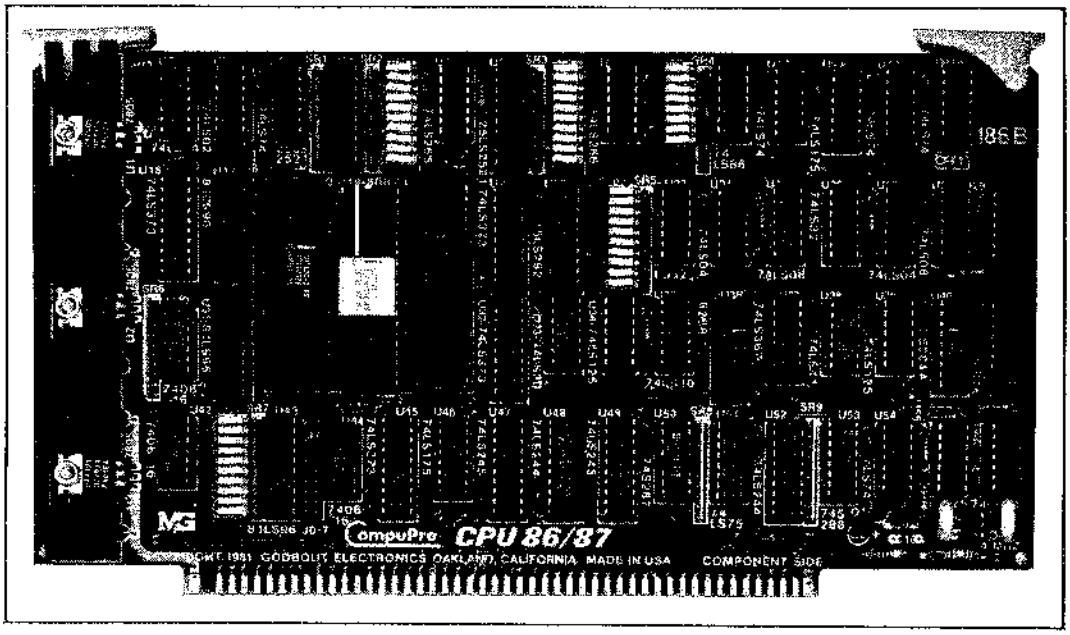
CompuPro®
A GODBOUT COMPANY

CPU 86/87™

Technical Manual

IEEE 696/S-100



16 BIT 8086

8087 MATH CO-PROCESSOR

80130 "SUPPORT SILICON"

$20.00

A197

CUSTOMER SERVICE INFORMATION

IF YOU NEED ASSISTANCE ALWAYS CONTACT YOUR COMPUPRO SYSTEM CENTER/DEALER FIRST

CompuPro products are available Assembled Tested with a 1 year limited warranty, or qualified under the Certified System Component (CSC) high-reliability program (200 hour burn-in, 2-year limited warranty, and direct exchange program for the boards in the event of malfunction)

Our paramount concern is that you are satisfied with any CompuPro product, so please follow the procedures below to help us serve you better.

If any product fails to operate properly, always contact your COMPUPRO SYSTEM CENTER/DEALER FIRST. If your dealer is unable to solve the problem, contact us at (415) 786-0909 for a **R**eturn **M**aterial **A**uthorization **(RMA)** number, and then return the board to us for service. Carefully package your board. Make sure the RMA number is on the outside of the package and on all literature. Include the RMA number, with a *copy of your invoice*, your name, shipping (street) address and a note describing the problem as fully as possible and ship to:

COMPUPRO — RMA #_____
3339 ARDEN ROAD
HAYWARD, CA 94545.

LIMITED WARRANTY

COMPUPRO warrants this computer product to be in good working order for a period of one (1) year (two years CSC, six months for disk drives) from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, COMPUPRO will, at its option, repair or replace this product at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of COMPUPRO. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse, or unauthorized modification of the product.

If you need assistance, or suspect an equipment failure, always contact your COMPUPRO System Center or dealer first. COMPUPRO's System Center technicians are factory trained to provide prompt diagnosis and repair of equipment failures. If you prefer, or if you are not satisfied by the actions taken by your System Center/dealer, you may return the product to COMPUPRO for warranty service. Please call COMPUPRO at (415) 786-0909 to obtain further information (obtain a return authorization number). Or, write to COMPUPRO at 3506 Breakwater Court, Hayward, California 94545, Attn., Warranty Service. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location (System Center or COMPUPRO) and to use the original shipping container or equivalent. Contact your COMPUPRO System Center/dealer or write to COMPUPRO at the above address for further information.

ALL EXPRESS AND IMPLIED WARRANTIES FOR THIS PRODUCT INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO A PERIOD OF ONE (1) YEAR FROM THE DATE OF PURCHASE, AND NO WARRANTIES, WHETHER EXPRESS OR IMPLIED, WILL APPLY AFTER THIS PERIOD. SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS MAY NOT APPLY TO YOU.

IF THIS PRODUCT IS NOT IN GOOD WORKING ORDER AS WARRANTED ABOVE, YOUR SOLE REMEDY SHALL BE REPAIR OR REPLACEMENT AS PROVIDED ABOVE. IN NO EVENT WILL COMPUPRO BE LIABLE TO YOU FOR ANY DAMAGES, INCLUDING ANY LOST PROFITS, LOST SAVINGS OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OF OR INABILITY TO USE SUCH PRODUCT, EVEN IF COMPUPRO OR A COMPUPRO FULL SERVICE SYSTEM CENTER HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY OTHER PARTY.

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR CONSUMER PRODUCTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU.

THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS WHICH MAY VARY FROM STATE TO STATE.

CompuPro®

CPU 86/87

Technical Manual

IEEE 696/S-100

CPU 86/87 TECHNICAL MANUAL
Copyright 1982 CompuPro
Hayward, CA 94545

File Name CPU 86/87.MAN
Document #11866
Board No. 186, Revision B

First editon: September 1982
Second printing: December 1983
Third printing: January 1984

DISCLAIMER - CompuPro makes no representations or warranties with respect to the contents hereof and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Further, CompuPro reserves the right to revise this publication and to make any changes from time to time in the content hereof without obligation of CompuPro to notify any person of such revision or changes.

Trademarks: CPU 86/87, CompuPro.
Tri-state, National Semiconductor, Inc.

All rights reserved. No part of this publication may be reproduced or transmitted in any form, or by any means, without the written permission of CompuPro. Printed and assembled in the United States of America.

CONTENTS

Switch Settings for Standard CompuPro Systems or
How to Get Your CPU 86/87 Up and Running in Under 5 Minutes,
Without Reading the Manual 1

HARDWARE SECTION
About CPU 86/87 3
Switch Settings and Option Selection 3
DIP Switch S1 4
DIP Switch S2 (and Part of S4) 4
DIP Switch S3 5
DIP Switch S4 6
DIP Switch S5 7
Jumpers 7
Installing an 8087 Math Co-Processor 8
Using Memory Manager 9
Brief Summary of Running
the 8086/80130 with Vectored Interrupts. 10
Using the 80130 Interrupts and Interval Timers 11
Interrupt Controller Internals 11
Interrupt Initialization 11
ICWs 1 and 2 12
ICW1 12
ICW2 13
ICW3 13
ICW4 13
ICW 5 and 6 14
OCW1 14
OCW2 15
OCW3 15
Reading Interrupt Mask Register 16
80130 Interrupt Inputs 16
80130 Interrupt Outputs 16
Counter Timer Internals 17
Description of Timer Modes 17
Sending Data to Timer 17
Reading Count Value 18

THEORY OF OPERATION 19

HARDWARE DESCRIPTION
Parts List 22
Component Layout 23
Logic Diagram 24-32

CUSTOMER SERVICE / WARRANTY INFORMATION . . . . . back page

HOW TO GET YOUR CPU 86/87 UP AND RUNNING IN UNDER 5 MINUTES, WITHOUT READING THE MANUAL

This section is for those of you who are running this CPU board in a standard single user CompuPro configuration and do not intend to deviate from that standard configuration. You should be able to set the switches and jumpers as shown below and never have to change them again (unless you change your system configuration).

If you want to know all the details about what these switches and jumpers do, you will have to read the rest of this manual.

SWITCH SETTINGS

DIP SWITCH S1 - Turn all paddles of dip switch S1 OFF.
DIP SWITCH S2 - Turn all paddles of dip switch S2 OFF.
DIP SWITCH S3 - Turn paddles 1,5,6 and 8 of dip switch S3 OFF.
Turn paddles 2,3,4 and 7 of dip switch S3 ON.
DIP SWITCH S4 - Turn paddles 1 and 2 of dip switch S4 OFF.
Turn paddles 3 through 10 of dip switch S4 ON.
DIP SWITCH S5 - Turn all paddles of dip switch S5 OFF.

JUMPERS

Make sure there is a shorting plug installed at jumper location J8. J8 is located near the top left-hand corner of the board. There should be no shorting plugs installed at jumper locations J0 through J7, which are located near the bottom left hand corner of the board.

SWITCH SETTINGS FOR OTHER COMPUPRO BOARDS

Follow the switch settings as outlined in the software manual, with the following exception: If you have an "F" revision DISK 1 (denoted by the part number 171F) or later, or a DISK 1A, consult the manual for how to get the 86 only boot. Move the shorting plug at jumper location J17 from the "A" position (which is the way it was probably shipped from the factory) to the "B" position. J17 is located just to the right of the EPROM.

If you have an "E" revision DISK 1 (denoted by the part number 171E) or earlier, contact the dealer where you purchased the CPU 86/87 for an upgrade EPROM that contains the 8086 boot code.

If you are using MP/M 8-16 with your CPU 86/87, make sure you change the SYSTEM SUPPORT 1 board as follows. (These instructions are also included in your MP/M 8-16 documentation.)

1) Carefully pull IC U28 from its socket. (IC U28 is located on the right hand side of the board.)

2) Bend out pin 4 so that when the IC is replaced, pin 4 will not make contact with the socket or anything else.

3) Replace IC U28 back in its socket and verify that every pin except pin 4 is back in its hole.

Bring up a CP/M system and put a copy of your MP/M 8-16 disk in the B drive. Use the MPMGEN command as follows:

```
A>B:MPMGEN  B:MPMLDRFY.86
copysys Version x.x
Destination Drive name (or return to terminate):B
Function complete.
Destination Drive name (or return to terminate):<cr>
A>
```

Your MP/M 8-16 disk will now have a loader for the CPU86/87. You may proceed with the rest of the manual.

NOTE: If you are going to use the CPU 86/87 board, you will not be able to run any 8 bit software. Therefore, the file "SW!.CMD" should be removed from your system disk.

BOOTING UP THE SYSTEM

If all the switches and jumpers in the system are set correctly (make sure your drives are jumpered per the DISK 1 manual if they are other than CompuPro drives), you should be ready to boot up the system. Make sure that all the boards are plugged squarely into the motherboard, replace the mainframe's cover, and turn on the power to the computer, terminal and disk drives. The light on your "A" drive should be flashing about twice per second. If it is not flashing, stop! Read the DISK 1 manual's troubleshooting section and correct the problem before proceeding. If the light is flashing, insert the CP/M or MP/M Disk #2 diskette into the A drive and close the drive door. CP/M-86 or MP/M 86 should sign on. CP/M-86 and MP/M 8-16 Disk #1 will not boot with the CPU 86/87.

ABOUT THE CPU 86/87

The **CPU 86/87** from CompuPro is one of the most advanced 16 bit processors available for the IEEE 696/S-100 Bus. Based on Intel's high performance 8086 16 bit processor, it also includes sockets for the 8087 high speed math co-processor and 80130 Operating System Firmware component. Through a special arrangement with Intel, CompuPro has supplied this board with a "ROM-less" version of the 80130 so that the user may retain full use of that part's interrupt and timer capabilities without paying for software that may not be needed. The CPU 86/87 has been designed to accept the ROM part, in case you desire that feature.

The CPU 86/87 includes circuitry that allows it to handle 8 and 16 bit memory and I/O devices that conform to the IEEE 696/S-100 protocol for 8 and 16 bit transfers. Both 8 and 16 bit types may be mixed in a system, the CPU 86/87 will dynamically adjust itself to the proper bus width. The CPU 86/87 is fully compatible with DMA devices that adhere to the IEEE 696/S-100 standard protocols (like the DISK 1A, DISK 2, DISK3 etc.).

The CPU 86/87 currently operates at 8 and 10 MHz clock speeds, but was designed to accommodate faster clocks as faster CPUs are introduced.

A special clock switching circuit allows the use of specially designed slave processors to share the bus with the CPU 86/87. Use of an 8 bit slave CPU would provide equivalent operation to our CPU 8085/88 dual processor board, thus providing a simple way to execute libraries of existing 8 bit software, as well as CompuPro's exclusive MP/M 8-16.

The CPU 86/87 includes power-on-jump capabilities that allow it to begin program execution on any 4K boundary in the lower 1 megabyte of address space.

When you couple high speed operation with the power of the 8086/8087 pair, the CPU 86/87 is truly a processor board for advanced computing systems of the eighties. Thank you for choosing a CompuPro product.

SWITCH SETTINGS AND OPTION SELECTION

This section gives you a detailed description of all the switch and jumper settings for the CPU 86/87. To set the board up for use in a standard CompuPro system configuration, refer to your CompuPro "CP/M-86 Technical Manual and Installation Procedures".

DIP SWITCH S1

Use dip switch S1 to select the memory address for the ROM internal to the 80130 chip. Since this board is supplied with a "ROM-less" part, the setting of these switches is unimportant until you want to use an 80130 with some code in it. The ROM space occupies 16K bytes and the CPU 86/87 allows it to reside on any 16K boundary in the 16 megabyte address space available on the IEEE 696/S-100 bus. Select the address with dip switch S1 as follows:

Paddle #	Address Bit	
1	A23	
2	A22	
3	A21	
4	A20	ON = "0"
5	A19	
6	A18	
7	A17	OFF = "1"
8	A16	
9	A15	
10	A14	

To minimize power dissipation, turn all these paddles OFF. Note: There is also a master memory enable switch (paddle 1 of dip switch S3) which should be turned OFF to keep this address from interfering with system memory.

DIP SWITCH S2 (and part of S4)

Use all the paddles of dip switch S2 and two of the paddles from dip switch S4 to select the I/O address where the 80130 component resides. The 80130 I/O registers occupy a block of 16 port addresses out of the possible 65,536 I/O port locations that the 8086 can address. The CPU 86/87 allows the part to be addressed to any 16 port boundary in the 65,536 port locations addressable. Set this address with dip switch S2 and part of dip switch S4 as follows:

S4 Paddle #	Address Bit	
1	A15	
2	A14	

S2 Paddle #	Address Bit	
1	A13	
2	A12	
3	A11	ON = "0"
4	A10	
5	A9	OFF = "1"
6	A8	
7	A7	
8	A6	
9	A5	
10	A4	

The standard port address for this part is FFF0-F hex. To set the standard port address, turn all paddles of S2 and paddles 1 and 2 of S4 OFF. Note: There is a master I/O enable switch for this part (paddle 2 of S3) and this should be set accordingly.

DIP SWITCH S3

Use dip switch S3 to select some of the various options on the CPU 86/87 board. The individual paddle's functions are:

Paddle 1 - Memory Enable: When this paddle is turned ON, the 16K byte memory space (selected by dip switch S1) used by the 80130 is enabled. When this paddle is turned OFF, the memory space is disabled. Since this board is supplied with a "ROM-less" version of the 80130, leave this paddle OFF.

Paddle 2 - I/O Enable: When this paddle is turned ON, the 16 byte I/O address space (selected by dip switches S2 and S4) used by the 80130 is enabled. When this paddle is turned OFF, the I/O address space is disabled. Currently any interrupt driven CompuPro software uses the system support board to arbitrate interrupts. Thus, this paddle should be turned ON so that the operating system will program the 80130 into a repressed and passive state.

Paddle 3 - Wait State Enable: When this paddle is turned ON, the on-board wait state generator is enabled. One wait state will be inserted into every I/O cycle, or every memory and I/O cycle, depending on the setting of paddle 4 (I/O Wait Only Enable). When this paddle is turned OFF, no on-board wait states will be generated. Note: Turning this paddle on or off during program execution may cause a program crash.

Paddle 4 - I/O Wait Only Enable: When this paddle is turned ON in conjunction with paddle 3 (Wait State Enable) ON, one wait state will be inserted into every I/O cycle. When this paddle is turned OFF in conjunction with paddle 3 (Wait State Enable) ON, one wait state will be inserted into every CPU cycle, memory and I/O. If paddle 3 (Wait State Enable) is OFF, paddle 4 will have no effect, (no wait states will be generated). Note: Turning this paddle on or off during program execution may cause a program crash.

It is recommended that paddles 3 and 4 both be turned ON to cause a wait state to be inserted into every I/O cycle. This will minimize problems with slow I/O boards. After system operation is verified, paddle 3 may be turned off, but if the system then becomes "flaky", turn paddle 3 on again. Note that running the system with I/O wait states usually will not measurably degrade the system's performance.

Paddles 5 and 6 - Unused. These paddles are not used and should be turned OFF.

Paddle 7 - MWRT Enable: When this paddle is turned ON it enables the S-100 bus signal MWRT to be generated by the CPU 86/87. When this paddle is turned OFF, the MWRT signal is not generated by the CPU 86/87. The MWRT signal should then be generated elsewhere in the system. In a normal CompuPro single user system configuration, this paddle should be turned ON.

Paddle 8 - ϕDSB* Enable: When this paddle is turned ON, it allows the master bus clock (ϕ) to be disabled by a temporary bus master asserting the ϕDSB* signal on bus line 21. When this paddle is turned OFF, this feature is disabled. This new S-100 bus line has been defined by CompuPro for use with our slave processor boards or special DMA peripherals. For now, leave this paddle OFF. The manual supplied with a board that utilizes this line will instruct you to turn on the paddle. For a description of how the ϕDSB* line is implemented, see the Theory Of Operation Section of this manual.

DIP SWITCH S4

Use paddles 1 and 2 of this dip switch (in conjunction with dip switch S2) to select the I/O address of the 80130. For a description of paddles 1 and 2, see the section on dip switch S2 above.

Use the remaining paddles to select the I/O port address for the memory manager. The lower byte of the port address is "hard-wired" to FD hex, but the upper byte is selectable by this dip switch as shown below:

Paddle #	Address Bit	
3	A15	
4	A14	
5	A13	ON = "0"
6	A12	
7	A11	
8	A10	OFF = "1"
9	A9	
10	A8	

The CompuPro standard port address for the memory manager is 00FD hex. To set dip switch S4 for this standard address, turn paddles 3 through 10 ON.

For a description of what the memory manager does, see the "Using the Memory Manager" section of this manual.

DIP SWITCH S5

Use dip switch S5 to select the power-on-jump/jump-on-reset options of the CPU 86/87. Select the address where the 8086 will jump to at power-on and reset with paddles 1 through 8. Paddle 9 selects whether the 8086 does a jump at power-on only, or with every RESET in addition to power-on. Paddle 10 enables or disables the power-on-jump feature.

The 8086 normally begins execution at address 0FFFF0 hex, but the power-on-jump feature allows execution to begin at any 4K address boundary in the lower 1 megabyte of address space by "jamming" a long jump instruction into the processor. Select the address with paddles 1 through 8 of dip switch S5 as shown below:

Paddle #	Address Bit	
1	A19	
2	A18	
3	A17	ON = "0"
4	A16	
5	A15	
6	A14	OFF = "1"
7	A13	
8	A12	

Paddle 9 - Jump-On-Reset Enable: When this paddle is turned ON in conjunction with paddle 10 (Power-On-Jump Enable) ON, the power-on-jump sequence is executed at power-on and every time a RESET occurs on the bus (usually caused by pushing the RESET button). When this paddle is turned OFF in conjunction with paddle 10 (Power-On-Jump Enable) ON, the power-on-jump sequence will only be executed at power-on. A RESET occurring on the bus will cause the normal 8086 reset operation (execution at 0FFFF0 hex) to occur. If paddle 10 (Power-On-Jump Enable) is turned OFF, the setting of paddle 9 will have no effect.

Paddle 10 - Power-On-Jump Enable: When this paddle is turned ON, the power-on-jump circuitry is enabled. When this paddle is turned OFF, the power-on-jump circuitry will be disabled and a normal 8086 reset sequence will occur.

The standard CompuPro system configuration does not require the use of the power-on-jump feature of the CPU 86/87, so all paddles of dip switch S5 should be turned OFF if this board is being used in the standard configuration.

JUMPERS

Jumpers J0 through J7 are located near the lower left-hand corner of the board and are used to select the various interrupt configurations possible with the CPU 86/87. They are arranged as shown in the diagram following:

```
    Left-hand Side                                  Right-hand Side

S-100 VI7* (pin 11) <------o (J7) o------< 8087 Interrupt Output
S-100 VI6* (pin 10) <------o (J6) o------< S-100 INT* (pin 73)
S-100 VI5* (pin 9)  <------o (J5) o------< 80130 Interrupt Output
S-100 VI4* (pin 8)  <------o (J4) o------< 80130 "Delay" Output
S-100 VI3* (pin 7)  <------o (J3) o------< 80130 "Baud" Output
S-100 VI2* (pin 6)  <------o (J2) o------< 80130 "Systick" Output
S-100 VI1* (pin 5)  <------o (J1) o------< S-100 INT* (pin 73)
S-100 VI0* (pin 4)  <------o (J0) o------< 8087 Interrupt Output
```

These jumpers have been arranged to provide the "most standard" interrupt configurations by the use of shorting plugs. The 8087 interrupt output is positioned so that it may be easily hooked up as the lowest (VI7*) or the highest (VI0*) vectored interrupt priority by installing a shorting plug at jumper locations J7 or J0 respectively. If no interrupt controller is to be used (not recommended), the 8087 interrupt output may be hooked directly to the S-100 master interrupt line INT* by installing a shorting plug between the right-hand sides of J7 and J6, or J1 and J0. If a vectored interrupt other than VI7* or VI0* is desired, select it by hooking wire-wrap wire from the right-hand side of either J7 or J0 to the left-hand side of any of jumpers J6-1.

The master interrupt output from the 80130 would normally be hooked to the S-100 master interrupt line INT* by installing a shorting plug between the right-hand side of jumpers J5 and J6.

The timer outputs from the 80130 (Delay, Baud and Systick) are arranged to be jumpered to vectored interrupt lines VI4* through VI2* respectively by the use of shorting plugs. If other arrangements are desired, they may be "scramble-wired" with the use of wire-wrap wire. Hook the right-hand side of the timer output jumper to the desired VI* line available at the left-hand side of the jumpers.

The standard CompuPro system configuration requires no jumpers on J0 through J7.

Jumper J8 is located near the top left-hand corner of the board. A shorting plug should be installed at this location if there is no 8087 on the board. The shorting plug should be removed if an 8087 is installed.

* * * * * * INSTALLING AN 8087 MATH CO-PROCESSOR * * * * * *

The CPU 86/87 is designed to accept an 8087 math co-processor chip made by Intel. Currently, the fastest 8087 available runs at 5 MHz. This means that the 8086 must also run at 5 MHz. CPU 86/87 boards are shipped from CompuPro running at either 8 or 10 Mhz depending on the version you ordered. If you ordered the CPU 86/87 from CompuPro with an 8087 installed, we shipped your board

running at 5 Mhz, and we verified that the 8087 was operational. If you ordered the CPU 86/87 without the 8087 chip, but now would like it installed, you may return the board to CompuPro for an upgrade. This is the recommended procedure, as it ensures that the hardware will be working correctly. If you want to install your own 8087, be aware that you will have to unsolder some components and solder in some new ones. If you do this badly, it will void your warranty. Also, even if you do the job neatly, but it doesn't work when you're finished, we are going to charge you to find the problem. Don't expect help over the phone, either.

For the brave among you, here is the procedure: Carefully unsolder capacitors C9 and C10, crystal X1 and inductor L1. Replace crystal X1 with a 15 MHz crystal. Replace capacitor C9 with a 220 pfd silver mica capacitor. Replace capacitor C10 with a 120 pfd silver mica capacitor. Replace inductor L1 with a 1 uH inductor. Carefully plug the math chip into socket U19. Remove jumper J8. Hope that it works.

Again, we strongly suggest that you return the CPU 86/87 to the factory for an 8087 upgrade.

* *

USING THE MEMORY MANAGER

The memory manager on the CPU 86/87 is a simple 4 bit parallel port that allows control of the upper four extended address lines (A23-20) on the S-100 Bus.

The data appearing in the upper four data bits of an I/O write to the memory manager's port address will be present on the address lines at the next CPU cycle. The lower four data bits will be ignored.

The use of the port seems deceptively simple. In fact, there are several things to watch out for. The first is that the page running the code that bumps the memory manager will vanish as soon as the write occurs. This means that the new page must contain known code so that the 8086 can continue. How do you get it there? It's like the chicken and the egg. The CPU cannot put the code there itself. However, you can use the DISK1 to read a sector (or more) there directly, since it can transfer to the full 24 bit range. Or the MPX-1 can be used to put or move code to the extended page. The standard MPX-1 ROM code has a function to move data between extended pages.

Secondly, since the 8086 is pipe-lined machine, the actual write to the memory manager port may occur after the next several instructions are fetched. This can cause problems if the 8 or so bytes following the output instruction are not identical in both pages. Make sure they are!

BRIEF SUMMARY OF RUNNING
THE 8086/80130 WITH VECTORED INTERRUPTS

1) Decide who is going to control your interrupts. You have the option of using the 80130 in the 8086 board or the 8259s in the System Support board. Whenever both boards are present, the unused controller(s) must be put in a benign state (all 8 or 16 interrupts masked) since the interrupt chips come up in undefined states - most likely ready to interrupt in some obscure manner.

   If you use the System Support board as your interrupt controller it may be easiest to just remove the 80130 chip from the 8086 board. In this case, do not jumper J0-J7 since the interrupt line drivers (U44) with open inputs will have active inverted outputs that will activate the interrupt lines.

   Using the timers and/or baud rate generator of the 80130 chip to drive the System Support interrupts requires programming the 80130's interrupt controller into a dormant state. Here the 8086 board I/O select switch (Switch 3 paddle 2) must be on for software access to the 80130. In jumpering J0-J7 be careful not to jumper to the 80130's interrupt output (right side of J5).

   Although the following is for using 80130 to control interrupts, it is for the most part applicable to the 8259s.

2) There are two physical considerations - turn Switch 3 paddle 2 on - again this allows you to select the 80130. Also jumper the right sides of J5 and J6 together. This connects the INT output of the 80130 to S-100 bus pin 73 (INT*) and thus to the INT input of the 8086.

3) Next you have to program the 80130. Read the following section as it does much to clarify an inherently obtuse situation. The comments on the 8259 in the System Support manual are also useful. Note that Initialization Control Word 2 (ICW2) sets the base address of your vector table. 80H gives a starting address of 200H.

4) Operational Control Word 1 (OCW1) must be given to enable (unmask) as many of the 8 interrupts as you want. 00H enables all eight vectored interrupts.

5) As you set up the table, remember the order of the bytes is low Instruction Pointer, high IP, low Code Segment, high CS. Don't assume what CS will be - copy it from the processor at run time.

6) After you have received an interrupt, you have to do two things if you ever want to get another. One thing is, you have to execute an enable interrupts instruction. The other is to send out the specific OCW2 to acknowledge to the 80130 that the interrupt has been handled.

USING THE 80130 INTERRUPTS AND INTERVAL TIMERS

The 80130 supplied with the CPU 86/87 board contains no ROM code, but you can still use the interrupt controller and interval timers built into the part. The CP/M-86 software supplied by CompuPro for the CPU 86/87 contains special code to initialize the interrupt controller to a benign state (all interrupts masked). This section of the manual assumes that you are familiar with interrupts and interval timers. If not, we refer you to the Intel Data Catalog - read the sections on the 8259A and the 8253/54. Also, the 8086 Family Handbook has an exceptional application note on the 8259A and interrupts in general (it's AP-59). If you happen to have a CompuPro System Support Manual, much of the data and concepts are covered there as well. This section is only intended to give you the raw data about the internals of the 80130, and is not a tutorial. The following is not a complete description, but is intended to be as guidelines.

INTERRUPT CONTROLLER INTERNALS

As mentioned above, this section is not going to attempt to explain how interrupts work. The interrupt section of the 80130 is very similar to the 8259A when operating in the 8086 mode. The 80130 accepts two types of command words to set its various operational modes. Between three and six of these words must be sent to the chip before it may be used. These are called "Initialization Command Words" or abbreviated ICWs. Once the initial ICW sequence is sent, it need not be sent again. After the ICW sequence, two "Operational Command Words" (OCWs) must be sent to complete the initial programming sequence. OCWs are used during normal interrupt operation for things such as interrupt masking, end-of-interrupt and reading the interrupt status. OCWs may be sent any time after the ICWs are sent.

NOTE: The following examples assume that the 80130 is addressed at I/O port locations FFF0 through FFFF hex.

Interrupt Initialization

Whenever a command is written to address FFF0H with D4=1, the data is interpreted by the 80130 as Initialization Command Word 1 (ICW1). ICW1 starts an internal initialization sequence during which the following events automatically occur:

a) The edge sense circuits are reset, which means that following the initialization sequence, an interrupt request (IR) input must make a low-to-high transition (high-to-low on the S-100 Bus) to generate an interrupt, until the IR input is programmed as level sensitive input (which it must be to meet the S-100 vectored interrupt specs).

b) The interrupt mask register is cleared, meaning that all IR inputs are enabled.

c) Status read is set to allow reading of the Interrupt Request Register (IRR).

d) The Interrupt Acknowledge circuitry is reset and prepared for the first INTA cycle.

ICWs 1 and 2

Issuing ICW1, ICW2 and ICW4 is the minimum amount of programming needed by the 80130 priority interrupt controller (PIC). ICW1 contains bits that indicate whether the 80130 can expect to see ICW3, ICW5 and ICW6 sent or not. Once ICW1 has been written, the following writes to I/O address FFF2H must be the sequence of ICW2, ICW3, ICW4, ICW5 and ICW6 (unless $\overline{\text{ICW3}}$, ICW5 and ICW6 are not needed, as specified in ICW1). The 80130 is ready to accept interrupts after the last ICW is sent. Note that ICW3, ICW5 and ICW6 are never sent in the implementation of the 80130 on the CPU 86/87.

ICW2 contains the bits T7-3 of the vector supplied to the 8086 during the second INTA cycle. The remaining bits (T2-0) are determined by the interrupt level being acknowledged and are supplied automatically by the 80130.

ICW1:

ICW1 is specified by writing to I/O port address FFF0H with D4 set to "1". The meaning of the bits of ICW1 are as follows:

Bits 7 and 6: Unused and may be any value.

Bit 5: Should always be set to "0". This tells the 80130 not to expect ICW6.

Bit 4: Should always be "1". Indentifies ICW1.

Bits 3 and 2: These bits should always be sent with bit 3 = "1" and bit 2 = "0". This tells the 80130 that all the IR inputs are level sensitive (to be compatible with the S-100 bus spec), and not to expect ICW5.

Bit 1: Should always be set to "1". This tells the 80130 that there are no other slave interrupt controllers on the board.

Bit 0: Should always be "1".

These really don't leave you leave you much choice as to what value to send for ICW1, does it? The value to send is: 1BH.

ICW2:

ICW2 is specified by writing to I/O port address FFF2H immediately after writing ICW1 above. The meaning of the bits in ICW2 are as follows:

Bits 7 through 3: These bits specify the five most significant bits of the vector byte supplied by the 80130 to the CPU during an INTA cycle. Bit 7 is the most significant and Bit 3 is the least significant. These are equivalent to bits T7-3 as referred to in the 8259A and 8086 documentation.

In brief, here is how the bits specify an address:

The 8086 responds to interrupts by sending out two INTA cycles. The first is a "dummy" cycle, but one byte of vector information is read by the 8086 during the second INTA cycle. Bits T7-3 are sent during this time on D7-3. T2-0 (D2-0) are dependent upon the IR level being acknowledged, which the 80130 supplies.

The 8086 takes this byte and multiplies it by 4 (shifts left twice) giving a 10 bit "vector" with the two least significant bits = "0". This vector is used to point to a memory location, with all higher address bits = "0". Since the lower two bits are "0", this address will point to any one of 256 four byte blocks starting at physical address 0. The 8086 picks up IP and CS bytes from these four locations and branches to the interrupt service routine.

Hence, T7-T3 may be thought of as corresponding to address bits A9-5. Address bits A4-2 are supplied by the 80130 and A1 and A0 always = "0".

Bits 2 through 0: Unused and may be any value.

ICW3:

ICW3 is not used in the CPU 86/87 configuration for the 80130.

ICW4:

ICW4 is always required by the 80130 and is used to select between the Special Fully Nested and Fully Nested modes. For a complete description of what these modes are, see the 8259A literature

referenced above. The 80130 as implemented on the CPU 86/87 will normally use the fully nested mode.

ICW4 is written to I/O address FFF2H immediately following ICW2 above. The meaning of the various bits of ICW4 are as follows:

Bits 7 through 5: Unused, but should be set to "0".

Bit 4: Used to select between the Special Fully Nested Mode and the Fully Nested Mode. When set to "1", selects the Special Fully Nested Mode. When set to "0", selects the Fully Nested Mode. Normal operation of the 80130 on the CPU 86/87 requires the Fully Nested Mode, so set this bit to "0".

Bit 3: Should always be set to "1". (Selects the buffered mode, but is actually ignored by the 80130.)

Bit 2: Should always be set to "1". (Selects the 80130 as the master, but is actually ignored by the 80130.)

Bit 1: Should always be set to "0". (Selects the normal end of interrupt mode, but is actually ignored by the 80130.)

Bit 0: Should always be set to "1". (Selects the 8086 mode, but is actually ignored by the 80130.)

Note: The above bits that are "ignored" by the 80130 are "hard-wired" internally to select the modes as described above. However, they should always be written as described.

ICW5 and ICW6

ICW5 and ICW6 are not used in the CPU 86/87 configuration of the 80130.

OCW1

OCW1 is used to set and clear the interrupt mask bits in the Interrupt Mask Register. When a bit is set to "1", it masks or inhibits its respective IR input. When a bit is set to "0", that IR input is unmasked or enabled.

OCW2 is written to I/O address FFF2H any time after the ICWs are sent. The mask bit to IR input correlation is as follows:

Bit 7: "1" masks IR7, "0" enables IR7.
Bit 6: "1" masks IR6, "0" enables IR6.
Bit 5: "1" masks IR5, "0" enables IR5.
Bit 4: "1" masks IR4, "0" enables IR4.
Bit 3: "1" masks IR3, "0" enables IR3.
Bit 2: "1" masks IR2, "0" enables IR2.
Bit 1: "1" masks IR1, "0" enables IR1.
Bit 0: "1" masks IR0, "0" enables IR0.

Masking an IR channel does not affect other channels in operation.

OCW2

Use OCW2 to issue end of interrupt (EOI) commands to the 80130. The 80130 operates only in the specific EOI mode, which means that each interrupt's service routine must send an EOI command to the 80130 when that routine is completed. The EOI sent must be the specific EOI for that interrupt level.

OCW2 is written to I/O address FFF0H any time after the ICWs are sent. The meaning of the bits in OCW2 are as follows:

Bits 7 through 5: Should always be sent with bit 7 = "0", bit 6 = "1" and bit 5 = "1". This selects the specific EOI mode. The 80130 actually ignores these bits, but they should be sent as described anyway.

Bits 4 and 3: Both bits should always be set to "0". This selects OCW2.

Bits 2 through 0: These bits contain a binary code that indicates which IR level gets the EOI as shown in the table below:

Bit 2	Bit 1	Bit 0	IR level that gets EOI
0	0	0	IR0
0	0	1	IR1
0	1	0	IR2
0	1	1	IR3
1	0	0	IR4
1	0	1	IR5
1	1	0	IR6
1	1	1	IR7

Note: One point that causes a lot of confusion for people writing interrupt service routines is the need for sending an EOI. Without the EOI, that IR level and all those of a lower priority will never be interrupted again.

OCW3

OCW3 is used to read two of the registers internal to the 80130. Those registers are the Interrupt Request Register (IRR) and the In-Service Register (ISR).

The IRR contains 8 bits which correspond to the IR inputs that have not yet been serviced. It is essentially an image of the IR inputs with bit 7 corresponding to IR7 and bit 0 corresponding to IR0. The bits in the register are "1" when an interrupt is pending.

The ISR register contains information as to which interrupt is being serviced. Bit 7 corresponds to IR7 and bit 0 corresponds to IR0. A bit is "1" if that level is "in-service".

Reading the IRR or ISR is performed by sending an OCW3 that selects one of the two registers for reading. Any I/O reads following OCW3 made to I/O address FFF0H will then yield the appropriate register's data. Note that the 80130 "remembers" the last register requested, so subsequent reads of the same register do not require OCW3 to be sent again.

OCW3 is sent by writing to I/O address FFF0H. The meaning of the bits of OCW3 is shown below:

Bits 7 through 5: Unused. Can be any value.

Bits 4 and 3: Bit 4 should always be sent as "0" and bit 3 should always be sent as "1". This selects OCW3.

Bits 2 and 1: Unused. Can be any value.

Bit 0: Used to select between the IRR and ISR. When set to "0" selects the IRR for reading. When set to "1", selects the ISR for reading.

Reading Interrupt Mask Register

The interrupt mask register may be read at any time by performing an I/O read to address FFF2H.

80130 Interrupt Inputs

The 80130 interrupt inputs are hard-wired to the S-100 bus vectored interrupt lines as shown below:

```
S-100 VI7* >----------> 80130 IR7
S-100 VI6* >----------> 80130 IR6
S-100 VI5* >----------> 80130 IR5
S-100 VI4* >----------> 80130 IR4
S-100 VI3* >----------> 80130 IR3
S-100 VI2* >----------> 80130 IR2
S-100 VI1* >----------> 80130 IR1
S-100 VI0* >----------> 80130 IR0
```

80130 Interrupt Outputs

For a complete discussion of the 80130 interrupt outputs, see the section of this manual entitled "Jumpers" in the "Switch Settings and Option Selection" section.

That completes the description of the 80130 interrupt controller. The next section describes the internals of the interval timer section of the 80130.

COUNTER TIMER INTERNALS

The interval timer section of the 80130 is basically a "hard-wired" 8254 (which is very similar to the 8253). This section is not intended to tell you everything there is to know about these parts or interval timers in general, but will just tell you about the 80130 implementation of them. For more information, refer to the 8254 and 8253 data sheets in the Intel Component catalog. The 8253 data sheet is also reprinted in the System Support 1 manual, if you happen to have a copy.

Description of Timer Modes

Timer 0 - is hard-wired to the Rate Generator mode (Mode 2). Upon loading the last byte of Timer 0's count register (CR), the timer will start counting down. When it reaches zero, the SYSTICK output will go low for one clock cycle. The CR will automatically be reloaded and counting will start again.

Timer 1 - Timer 1 is hard-wired to the Interrupt on Terminal Count mode (Mode 0). The DELAY output will be set low upon initialization and will remain low until the CR is loaded. The timer will then start counting down, and when it reaches zero the DELAY output will go high and will remain high until the CR is reloaded.

Timer 2 - is hard-wired to the Square Wave Generator mode (Mode 3). After the CR is loaded the BAUD output will contain a square wave at a frequency dependent on the count value. The output will be low for half the value and high for the other half.

Sending Data to Timers

Loading the CR of each timer consists of the following sequence:

1) Write the timer initialization byte to the timer control port (FFFEH).

2) Write the LSB of the count value to the appropriate timer data port.

3) Write the MSB of the count value to the timer data port. Counting then starts.

There are three timer initialization bytes, one for each timer. The timer initialization byte is always written to I/O address FFFEH (the timer control port). The three timer initialization bytes are as follows:

Timer 0 = 00111010
Timer 1 = 01110000
Timer 2 = 10110110

The count values are sent to each timer's data port. The LSB is always sent first, followed by the MSB. It is not possible to write the count value in a single 16 bit operation. The timer's data port I/O addresses are as follows:

Timer 0 = FFF8H
Timer 1 = FFFAH
Timer 2 = FFFCH

Reading Count Value

To read the current value of any of the count registers, it is necessary to send the timer a special "latch count" command. This does not stop the timer from counting, but stores the current count value in a latch so that the CPU doesn't read the counter data just as it's changing (which could result in erroneous data).

Each timer has its own "latch count" command byte that is sent to the timer control port (FFFEH). The commands are:

Latch Count Command for Timer 0 = 00000000
Latch Count Command for Timer 1 = 01000000
Latch Count Command for Timer 2 = 10000000

After the latch count command is sent to the timer control port, the latched data may be read from the appropriate timer's data port (see above for addresses). The LSB is always read first, followed by the MSB. After both bytes are read, the latch holding the data will be unlatched and begin tracking the count registers again.

THEORY OF OPERATION

This section of the manual will explain, in general, how the circuitry on the CPU 86/87 works. In the following discussion, it will be helpful to refer to the schematic diagrams contained in the appendix of this manual.

The CPU 86/87 is based on the Intel 8086 CPU. The clock for the CPU is generated by the 8284A clock generator IC (U40). It uses an external oscillator consisting of two inverters, crystal X1, capacitor C9 and inductor L1. The crystal is a third overtone type, and is three times the desired processor frequency. For example, to run the CPU at 8 MHz, a 24 MHz crystal would be used. If the crystal value is changed, the value of C9 must also be changed.

The clock output of the 8284A is sent unbuffered to the 8086, 8087 and 80130 to keep the rise and fall times within spec. Terminating resistors R7 and R18 minimize undershoot and reflections. Inverters are used to provide the CLK* and CLK signals for the rest of the board. The CLK signal is buffered by a Tri-state™ buffer to form bus ϕ. The Tri-state enable is driven by the inverting output of flip flop U41b. The D and CLR inputs to this flip-flop are driven by the newly defined bus line ϕDSB* on pin 21 of the S-100 bus. This line will be driven low by a temporary master coincident with the CDSB* signal (which is just after the rising edge of the clock). This will immediately cause the bus clock to be Tri-stated. Pull-up R17 makes sure that it floats to the high state, but the temporary master should be driving the clock now anyway. When the temporary master relinquishes the bus, it will drive CDSB* high and float its clock high. Flip-flop U41b will then be free to enable the CPU 86/87's clock , but not until after the next rising edge of it. This ensures that there are no slices on the clock line.

The 8086 (U20) and the 8087 (U19) have most of their common pins wired together. The exceptions are the RQ/GT* lines. When there is no 8087 installed, J8 connects the RQ/GT* line to the 8086 directly. When the 8087 is installed, J8 is removed and the RQ/GT* line goes through the 8087 and then to the 8086. This ensures that DMA requests are handled correctly if the 8087 is in control of the bus.

The 8288 system controller IC (U36) is used to generate the read and write strobes, the ALE signal, and the direction and data buffer control signals DT/R* and DEN. ALE is used to latch the address information from the CPU into the address latches U21,32 and 45. These also provide the buffering for the S-100 bus address lines. ALE is also used by U15b to generate the pSYNC signal. The pSTVAL* signal is a function of pSYNC and CLK*.

The MRDC*, IORC* and INTA* signals are ANDed by a section of U38 to form a generalized read strobe, which eventually becomes pDBIN. Similarly, the MWTC* and IOWC* signals are ANDed by a section of

U25 to form a generalized write strobe, which eventually becomes pWR*.

All these "p" signals are buffered by U37 and go out to the bus.

The S-100 status lines are generated by a 74S288 bipolar PROM. The three status lines from the CPU (S0*-S2*) are latched by U51. The outputs of U51 go to 3 of the address inputs of the PROM. The PROM then decodes the proper status and puts it out on its data output lines O1-7. Data output O8 is used to inhibit generation of a wait state by flip-flop U6b. Wait states will be allowed only if the right cycle type is occurring (determined by the two wait state switches connected to the other two address inputs to the PROM).

The S-100 status lines are buffered by U52.

The sXTRQ* line is generated by the OR of the latched BHE* signal LBHE* and A0. If LBHE* and A0 are low, and it's not an interrupt acknowledge cycle, a sixteen request will be generated. If SIXTN* goes low, indicating that a 16 bit transfer can occur, the output of U35 will go high, causing the ONECYCLE signal to be true. This signal tells the CPU to complete the 16 bit transfer at full speed. If the SIXTN* signal stays high, U35's output will be low causing the ONECYCLE signal to be false. This starts a process whereby the CPU 86/87 will halt the 8086 and read or write two bytes serially. This is performed by the state machine consisting of U12, U13 and U14, which generates the signals STBINH, FORCE, and FLIP. These are used to sequence the logic on the board to run the two bus cycles.

The data bus is buffered, multiplexed and latched (depending on what is required) by U16, 47, 48 and 49. The control of these buffers and latches is performed by a 256x4 bipolar PROM (U50). The direction inputs of U47 and 49 (the main data bus buffers) are connected directly to the DT/R* line from the 8288. A section of U35 is used to disable the PROM entirely, which gives us a few more input terms. All buffers will be disabled when DODSB*, or ACK* (the signal specifying that an access to the 80130 is occurring) is true, and DEN is false. The rest of the inputs to the PROM control when the various buffers are enabled. The LA0, LBHE* and DT/R* signals control the basic 16 bit cycles, while the FLIP and TWOCYCLE signals control the buffers during a byte serial transfer. The POJ* signal disables the buffers if the power-on-jump signal is active. The INTAK signal routes the byte data correctly during interrupt acknowledge cycles.

The 80130 interface is mostly straight-forward decoding logic, with U9, U10 and part of U8 providing the IOCS* signal and U7 and U8 providing the MEMCS* signal. These are the I/O chip select and Memory chip select signals, respectively. The 80130 address/data and status lines connect to the equivalent 8086 lines similar to the 8087. The ACK* output signifies that an access to the 80130 is occurring.

The memory manager circuitry is merely a 4 bit I/O port whose address is decoded by U33 and U22. U46 is a 4 bit latch whose output passes through to U45 which keeps the address from appearing on the bus until the next ALE and also buffers it.

The S-100 bus uses a HOLD/HLDA protocol for DMA requests, but the 8086/87 use a RQ/GT protocol when in their max mode. U4, U5, and U6a provide the HOLD/HLDA to RQ/GT* conversion. When HOLD* is asserted, a pulse one clock cycle wide is issued on the RQGT* line. When a GT pulse is issued by the CPU on RQGT*, U6a will be set low, causing pHLDA to be asserted. When HOLD* goes away another pulse will be issued on RQGT* causing the processor to assume control of the bus again. One clock cycle after the last pulse, pHLDA goes false.

Three sections of U56, crystal X2 (4 MHz) and U41a provide a 2 MHz clock for the S-100 CLOCK signal on pin 49. A separate oscillator was used so that CLOCK will always be 2 MHz independent of the CPU frequency.

The power fail circuit causes a POC* to be issued upon the rising edge of PWRFAIL*. This insures that the system will recover just as if the power had come on for the first time, and prevents problems that might occur if the power dips for a short period causing PWRFAIL* to be asserted, but the power doesn't really stop.

PARTS LIST

INTEGRATED CIRCUITS

U1-U3	7805
U4	74LS74
U5	74LS02
U6	74LS74
U7	25LS2521
U8	74LS266
U9	25LS2521
U10	74LS266
U11	74LSR86
U12	74LS74
U13	74LS175
U14	74LS74
U15	74LS74
U16	74LS373
U17	81LS96/98
U18	80130 ROM-less
U19	8087 OPTIONAL
U20	8086
U21	74LS373
U22	25LS2521
U23	74LS32
U24	74LS04
U25	74LS08
U26	74LS32
U27	74LS04
U28	74LS08
U29	74LS02
U30	7416
U31	81LS96/98
U32	74LS373
U33	74LS30
U34	74LS125A
U35	74LS10
U36	8288
U37	74LS367A
U38	74LS11
U39	74LS125A
U40	8284A-1
U41	74LS74
U42	7416
U43	81LS96/98
U44	7416
U45	74LS373
U46	74LS175
U47	74LS245
U48	74LS244
U49	74LS245
U50	74S287 (G193)
U51	74LS75
U52	74LS244
U53	74S288 (G192)
U54	74LS74
U55	74LS125A
U56	74F04

RESISTORS

R1-R4	1.5K Ohm
R5	4.7K Ohm
R6	10K Ohm
R7	18 Ohm
R8	560 Ohm
R9-R10	10K Ohm
R11	270 Ohm
R12	2.2K Ohm
R13	2.7K Ohm
R14-R16	1K Ohm
R17	1.5K Ohm
R18	18 Ohm
SR1-SR5	4.7 Ohm or 5.1K Ohm
SR6	1.5K Ohm
SR7	4.7 Ohm or 5.1K Ohm
SR8-SR9	1.5K Ohm

CAPACITORS

C1-C6	10 uF
C7	.01 uF
C8	18 uF
C9	Silver Mica
31	By-pass

DIODE

D1	1N914

TRANSISTOR

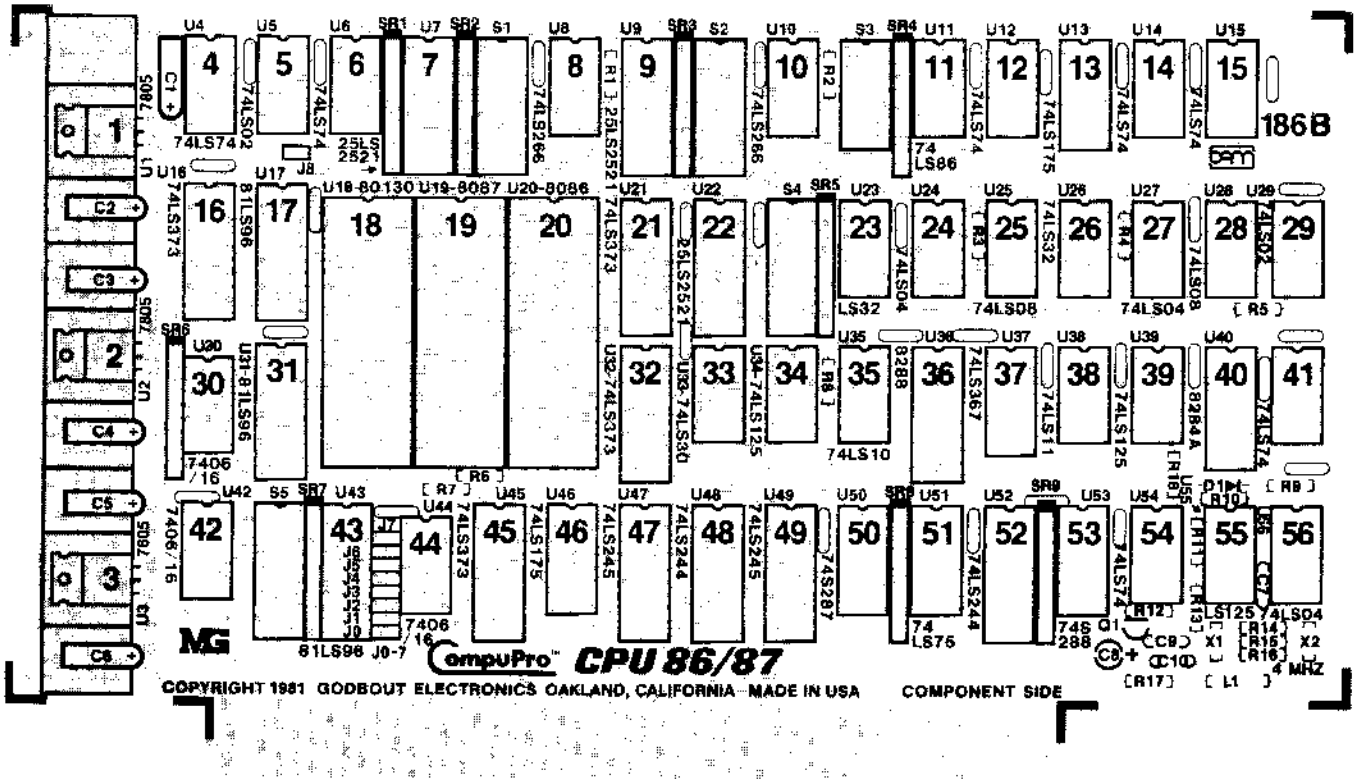
Q1	2N3904

SWITCHES

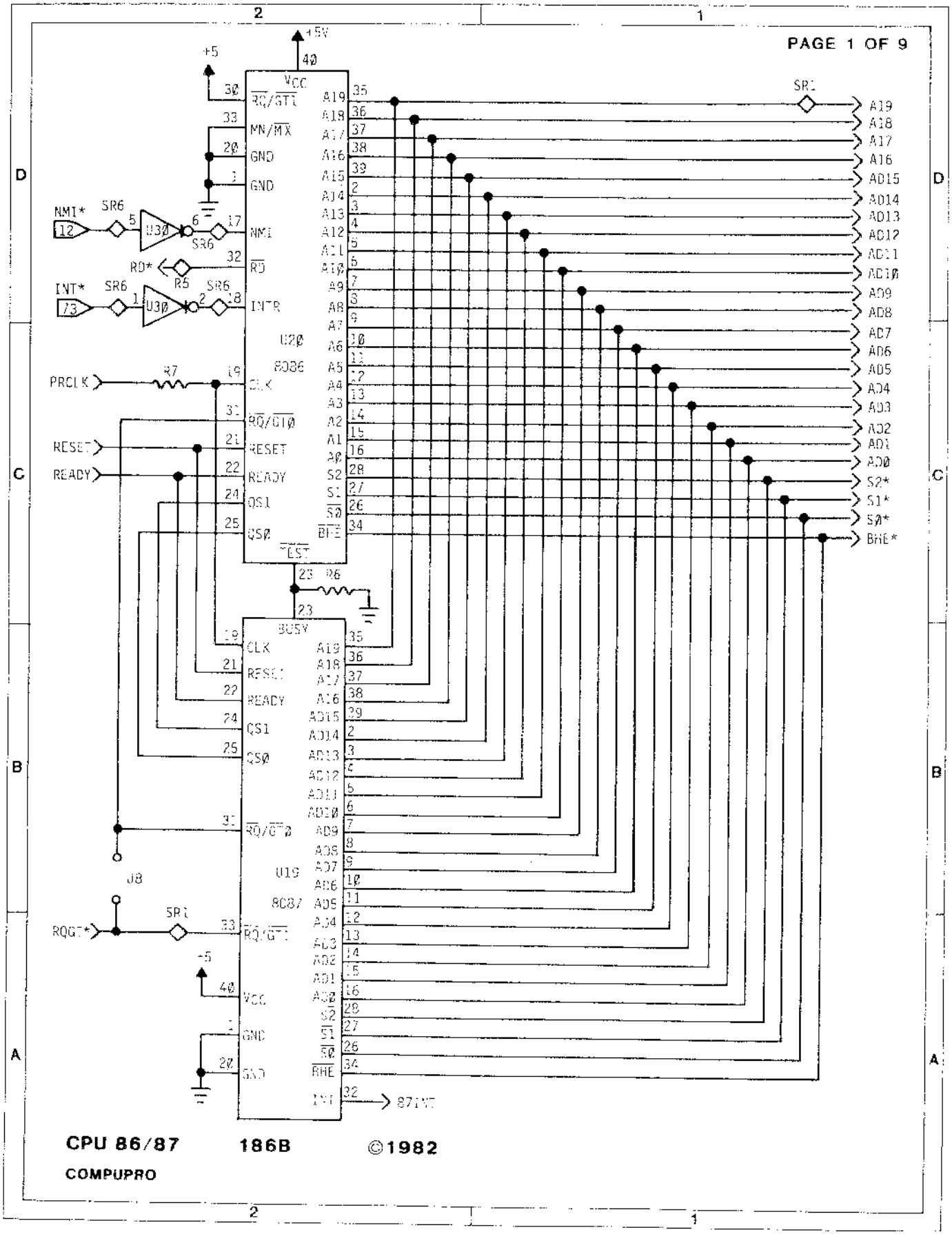
S1-S2	10 position
S3	8 position
S4-S5	10 position

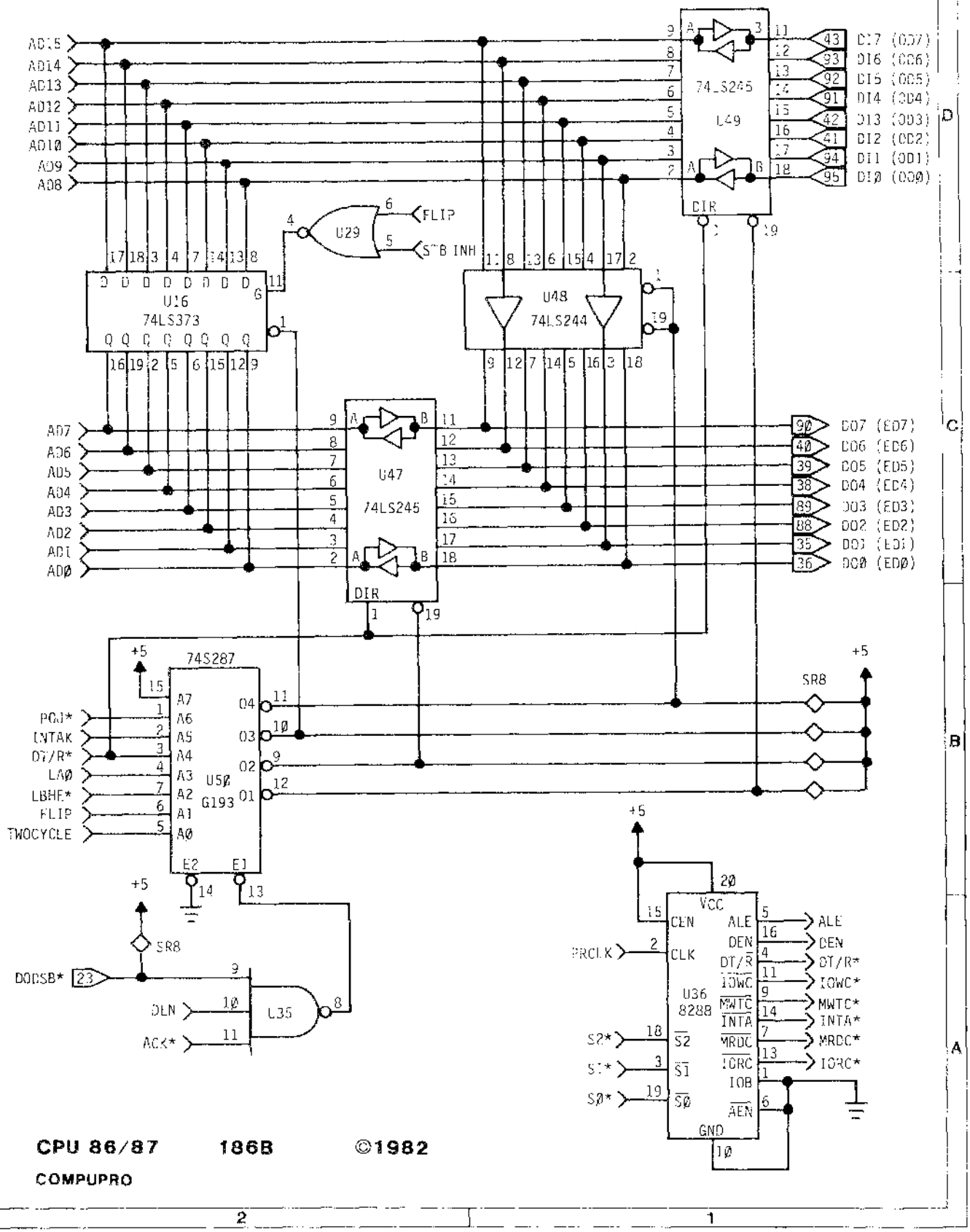
JUMPERS

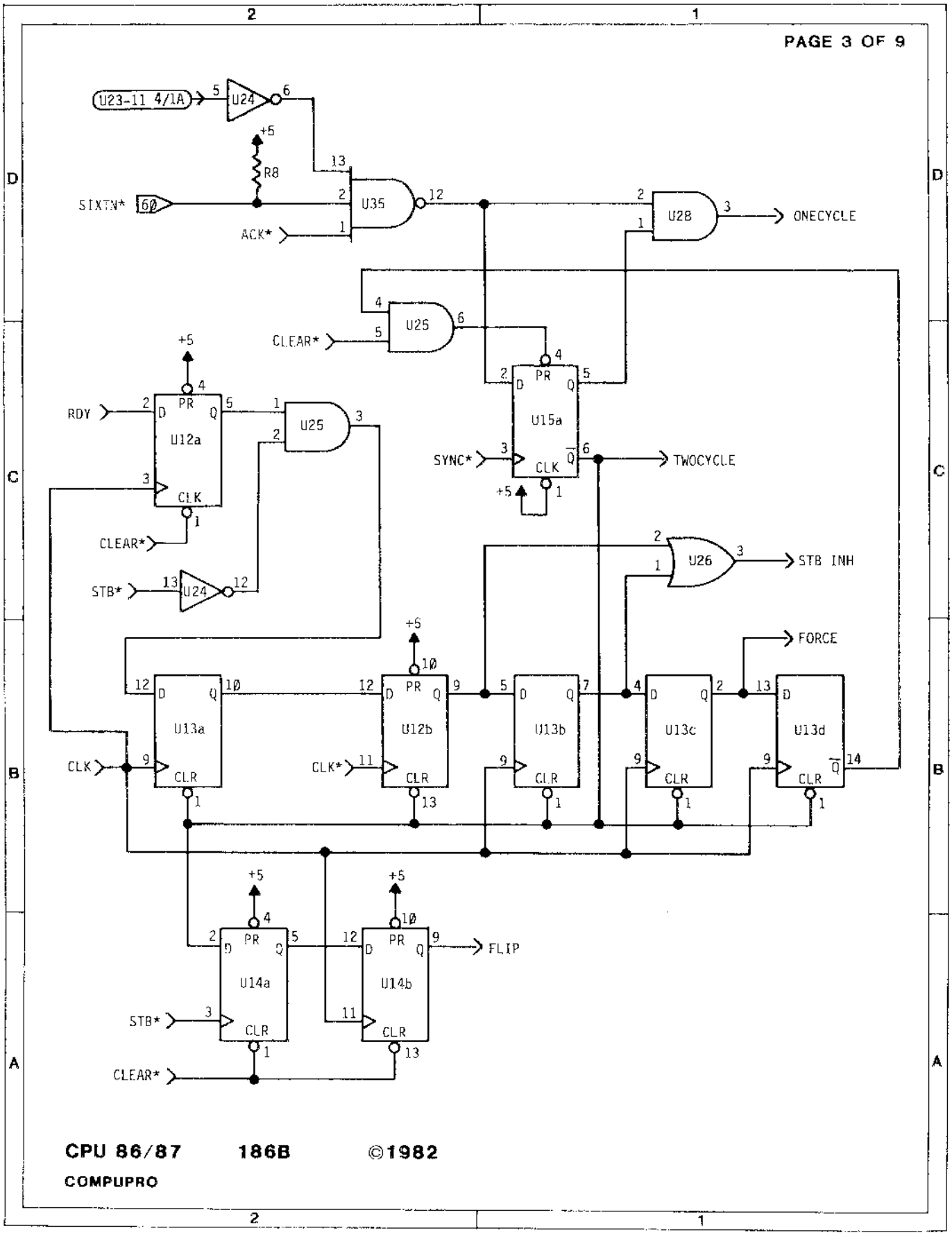
J0-J7	8x2 position
J8	2 position



COMPONENT LAYOUT

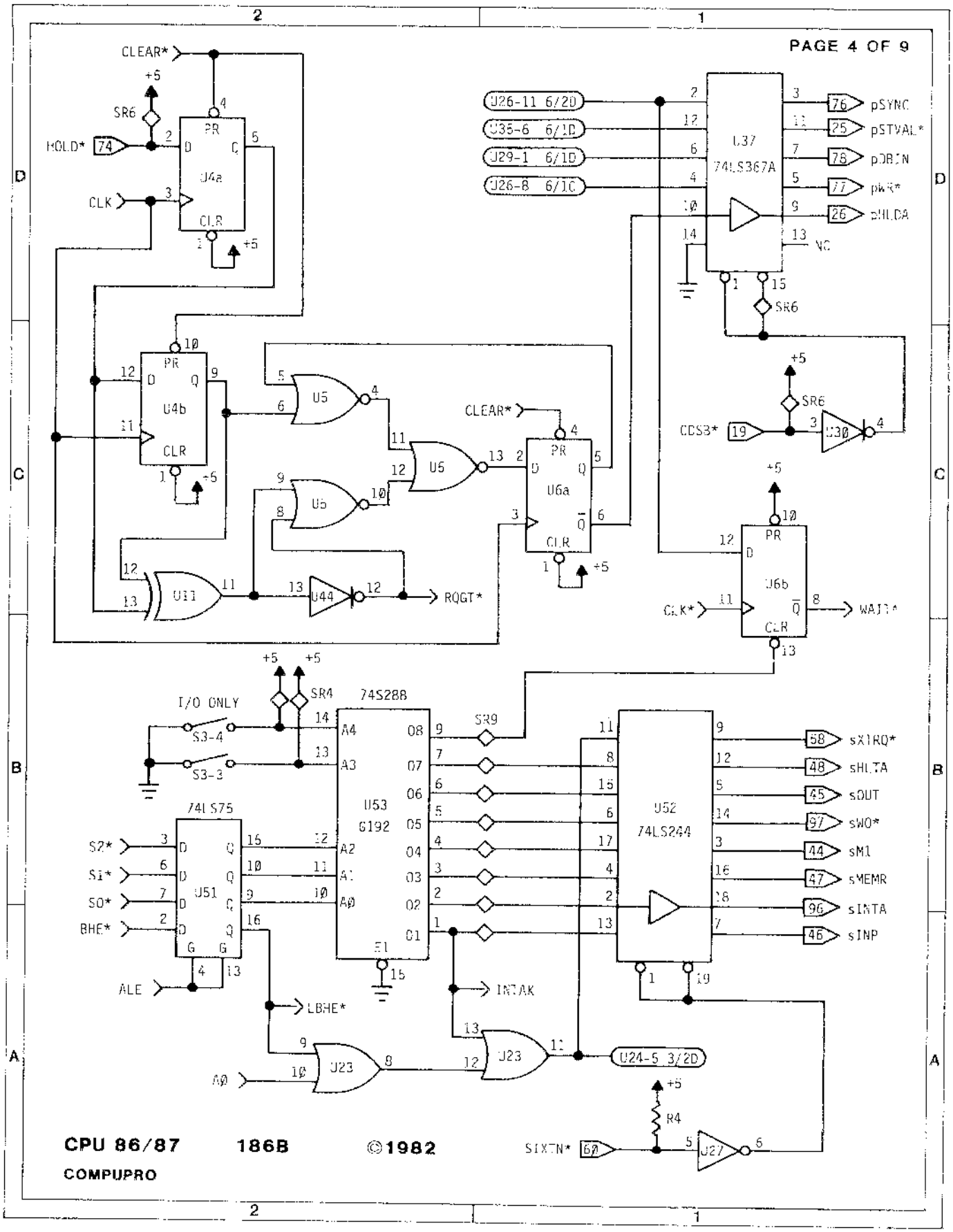

PAGE 1 OF 9
+5V
+5
VCC
RQ/GT1
MN/MX
GND
NMI
RD
INTR
U20
8086
CLK
RQ/GT0
RESET
READY
QS1
QS0
TEST
BUSY
U19
8087
RQ/GT1
BHE
INT
87INT
NMI*
INT*
RD*
PRCLK
RQGT*
SR1
SR6
U30
R5
R6
R7
J8
A19
A18
A17
A16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
S2*
S1*
S0*
BHE*
CPU 86/87
186B
©1982
COMPUPRO

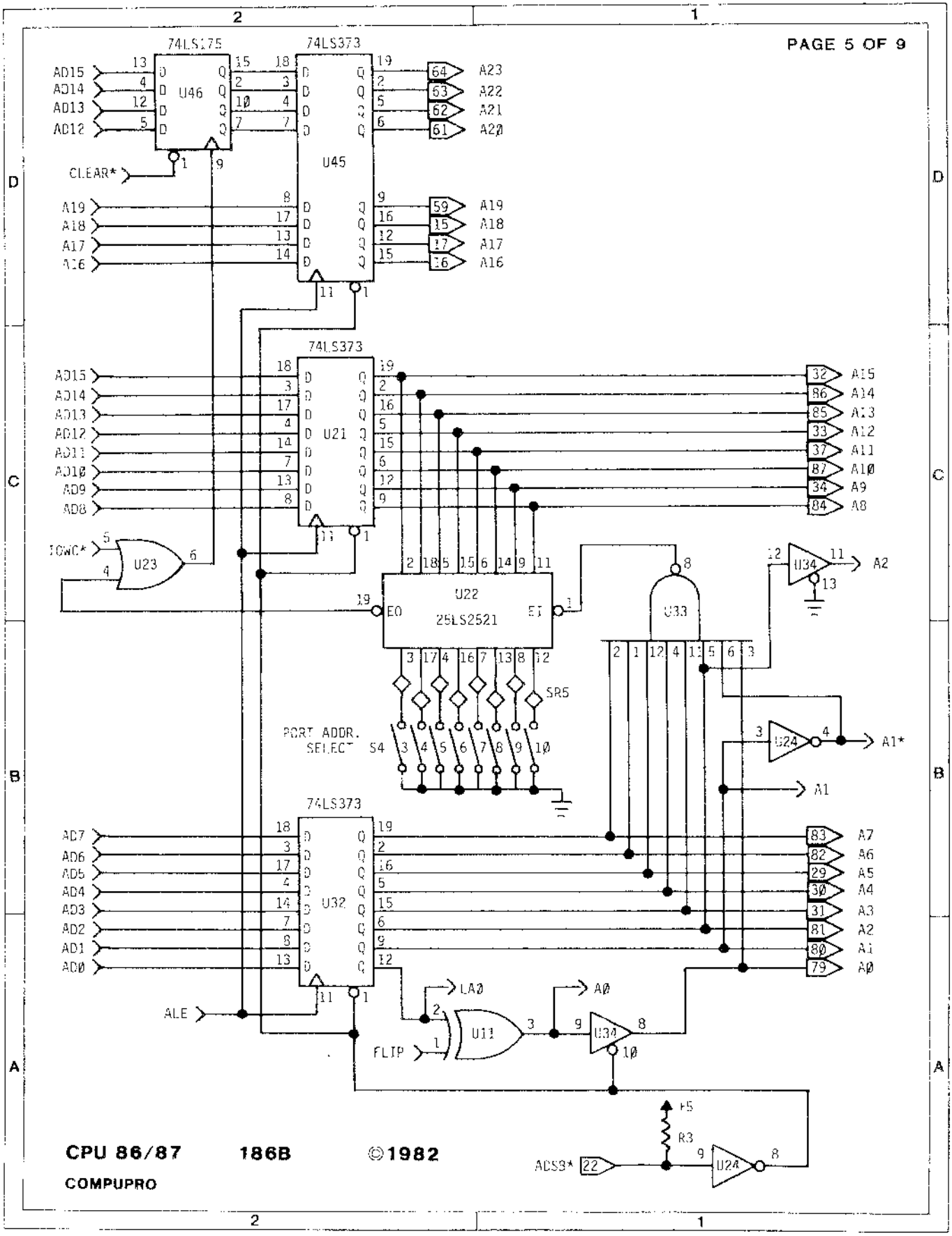

AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
74_S245
U49
DIR
DI7 (OD7)
DI6 (OD6)
DI5 (OD5)
DI4 (OD4)
DI3 (OD3)
DI2 (OD2)
DI1 (OD1)
DI0 (OD0)
U29
FLIP
STB INH
U16
74LS373
U48
74LS244
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
U47
74LS245
DO7 (ED7)
DO6 (ED6)
DO5 (ED5)
DO4 (ED4)
DO3 (ED3)
DO2 (ED2)
DO1 (ED1)
DO0 (ED0)
+5
74S287
U50
G193
PCU*
INTAK
DT/R*
LA0
LBHE*
FLIP
TWOCYCLE
SR8
DODSB*
DEN
ACK*
U35
PRCLK
U36
8288
CEN
CLK
ALE
DEN
DT/R*
IOWC*
MWTC*
INTA*
MRDC*
IORC*
IOB
AEN
S2*
S1*
S0*
GND
Vcc
CPU 86/87 186B ©1982
COMPUPRO



CPU 86/87 186B ©1982

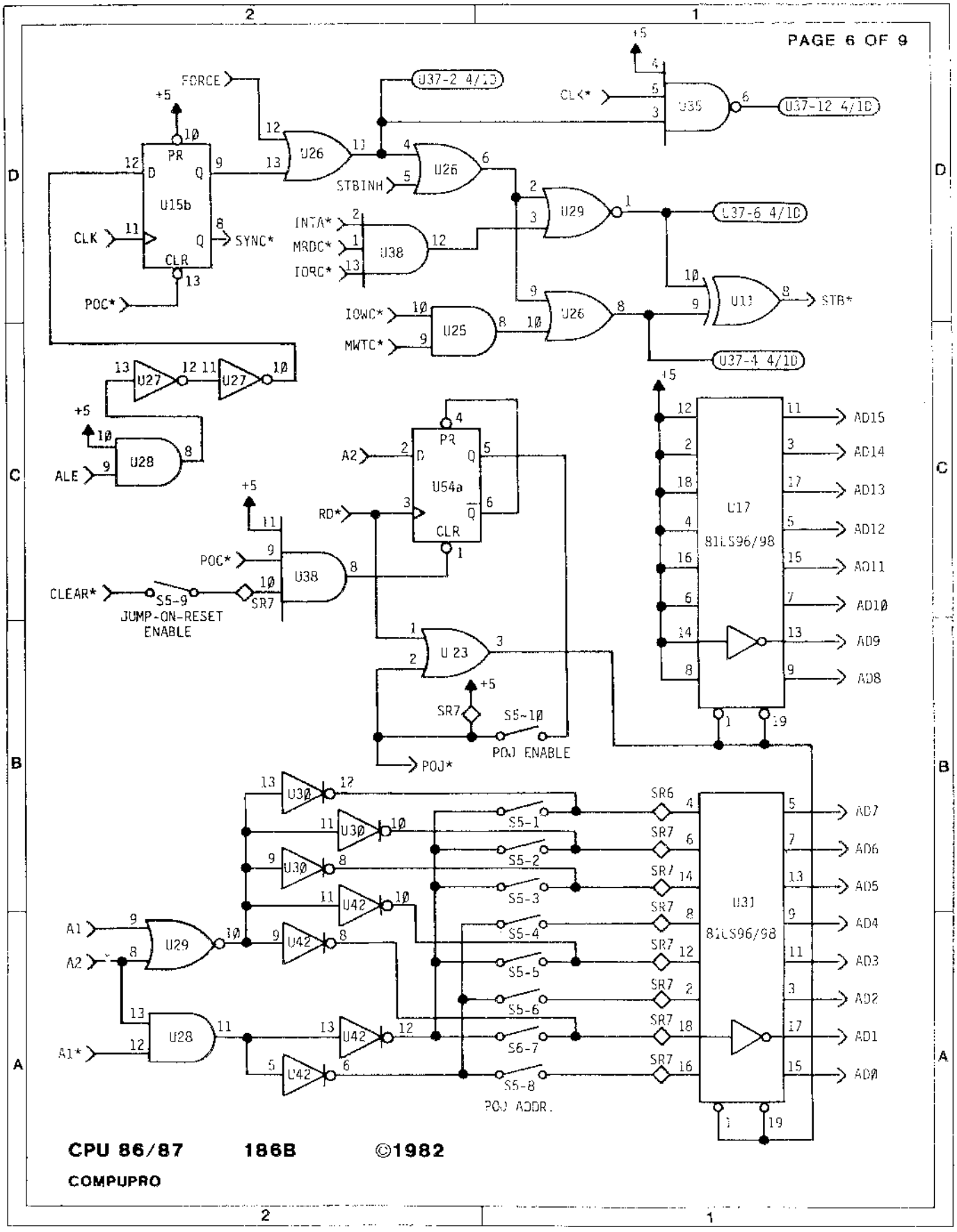
COMPUPRO


CLEAR*
+5
SR6
HOLD*
74
U4a
PR
CLR
CLK
U26-11 6/2D
U35-6 6/1D
U29-1 6/1D
U26-8 6/1C
U37
74LS367A
pSYNC
pSTVAL*
pDBIN
pWR*
pHLDA
NC
U4b
U5
U6a
U6b
RQGT*
WAIT*
CDS3*
U30
I/O ONLY
S3-4
S3-3
SR4
74S288
U53
6192
SR9
U52
74LS244
sXIRQ*
sHLTA
sOUT
sWO*
sM1
sMEMR
sINTA
sINP
74LS75
U51
S2*
S1*
S0*
BHE*
ALE
LBHE*
INTAK
A0
U23
U24-5 3/2D
R4
SIXTN*
60
U27
CPU 86/87
186B
©1982
COMPUPRO



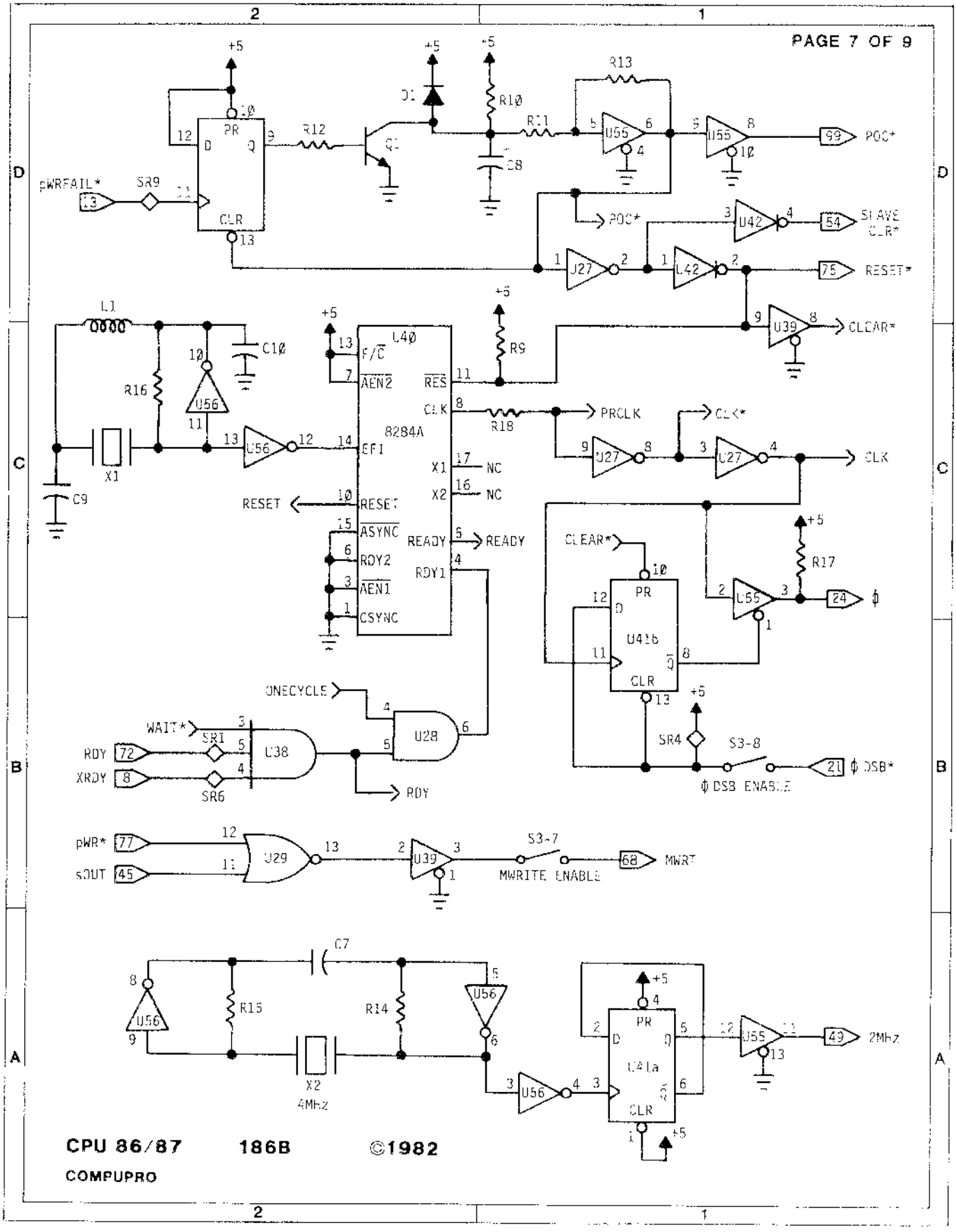
CPU 86/87 **186B** **©1982**

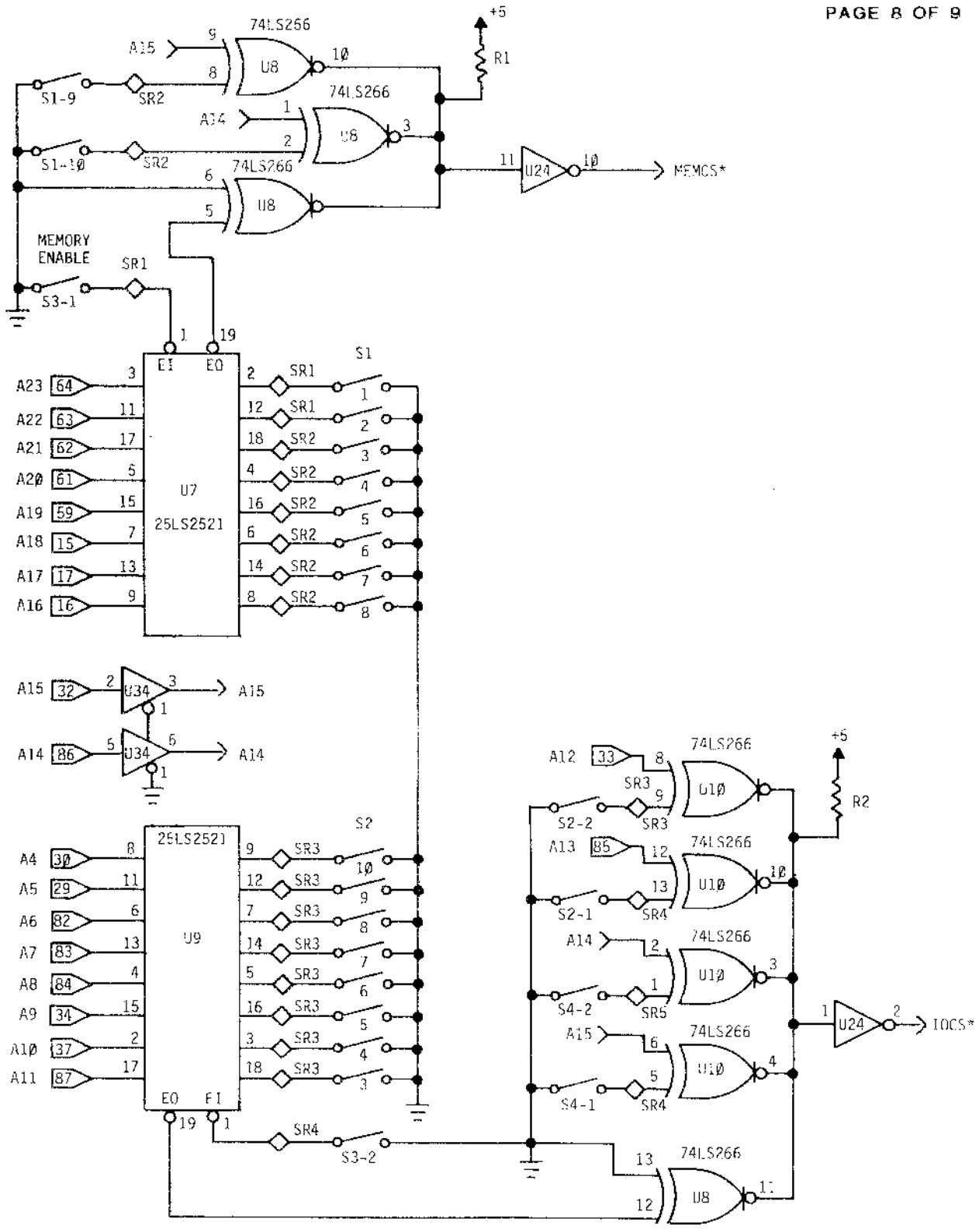
COMPUPRO



CPU 86/87 186B ©1982

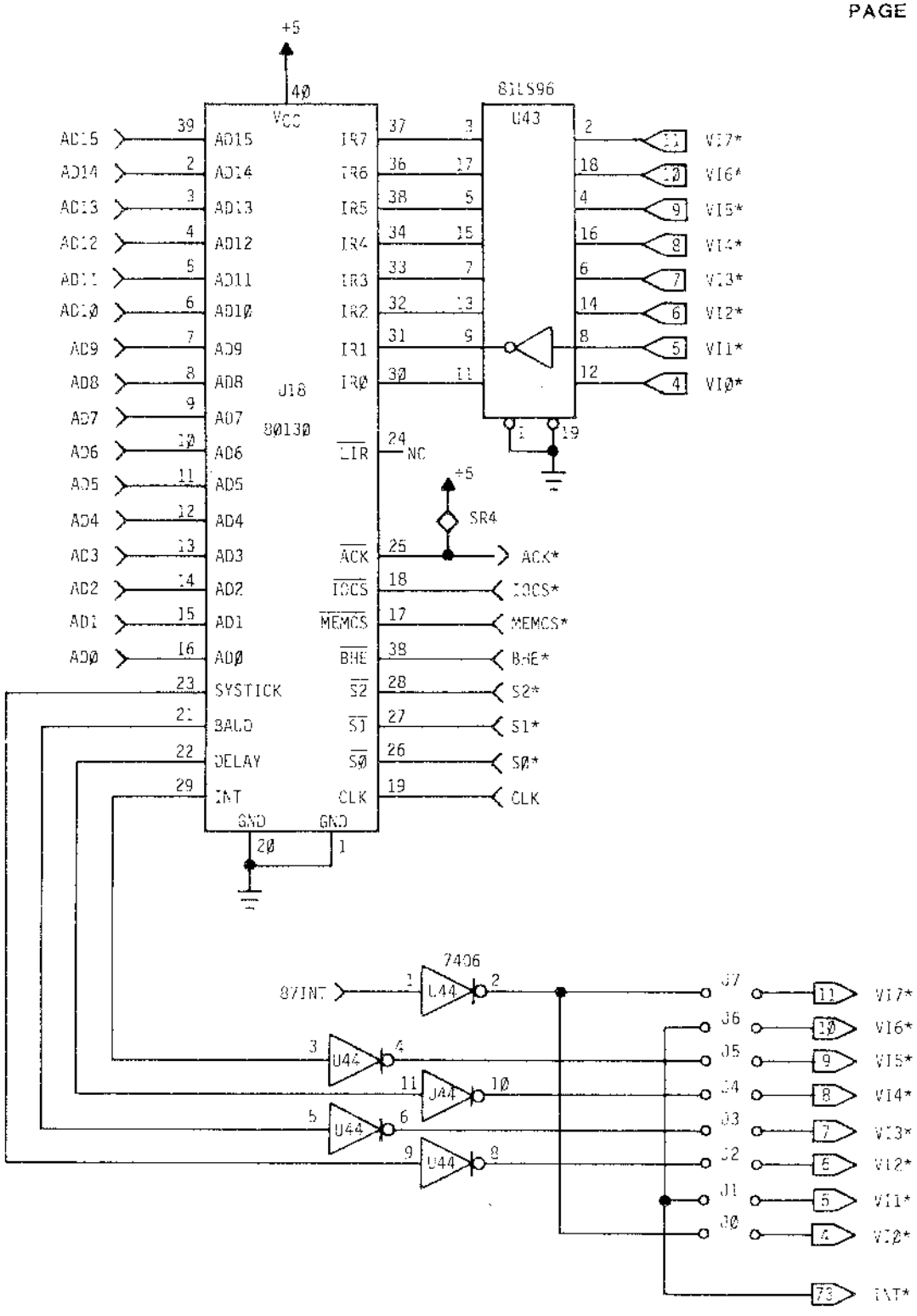
COMPUPRO


PAGE 7 OF 9
+5
pWRFAIL*
SR9
PR
CLR
R12
R10
R11
R13
C8
U55
U42
U27
U39
POC*
SLAVE CLR*
RESET*
CLEAR*
L1
C10
R16
X1
C9
U56
L40
8284A
F/C
AEN2
RES
CLK
EFI
X1
X2
NC
RESET
ASYNC
READY
RDY2
AEN1
RDY1
CSYNC
R8
R18
PRCLK
CLK*
CLK
ONECYCLE
WAIT*
SR1
SR6
RDY
XRDY
U38
U28
U41b
R17
SR4
S3-8
ϕ DSB*
ϕ DSB ENABLE
pWR*
sOUT
U29
S3-7
MWRT
MWRITE ENABLE
C7
R15
R14
X2
4MHz
U41a
2MHz
CPU 86/87
186B
©1982
COMPUPRO



CPU 86/87 186B ©1982

COMPUPRO



CPU 86/87 **186B** **©1982**

COMPUPRO

CPU 86/87

A *GODBOUT* COMPANY
3506 Breakwater Court, Hayward, CA 94545