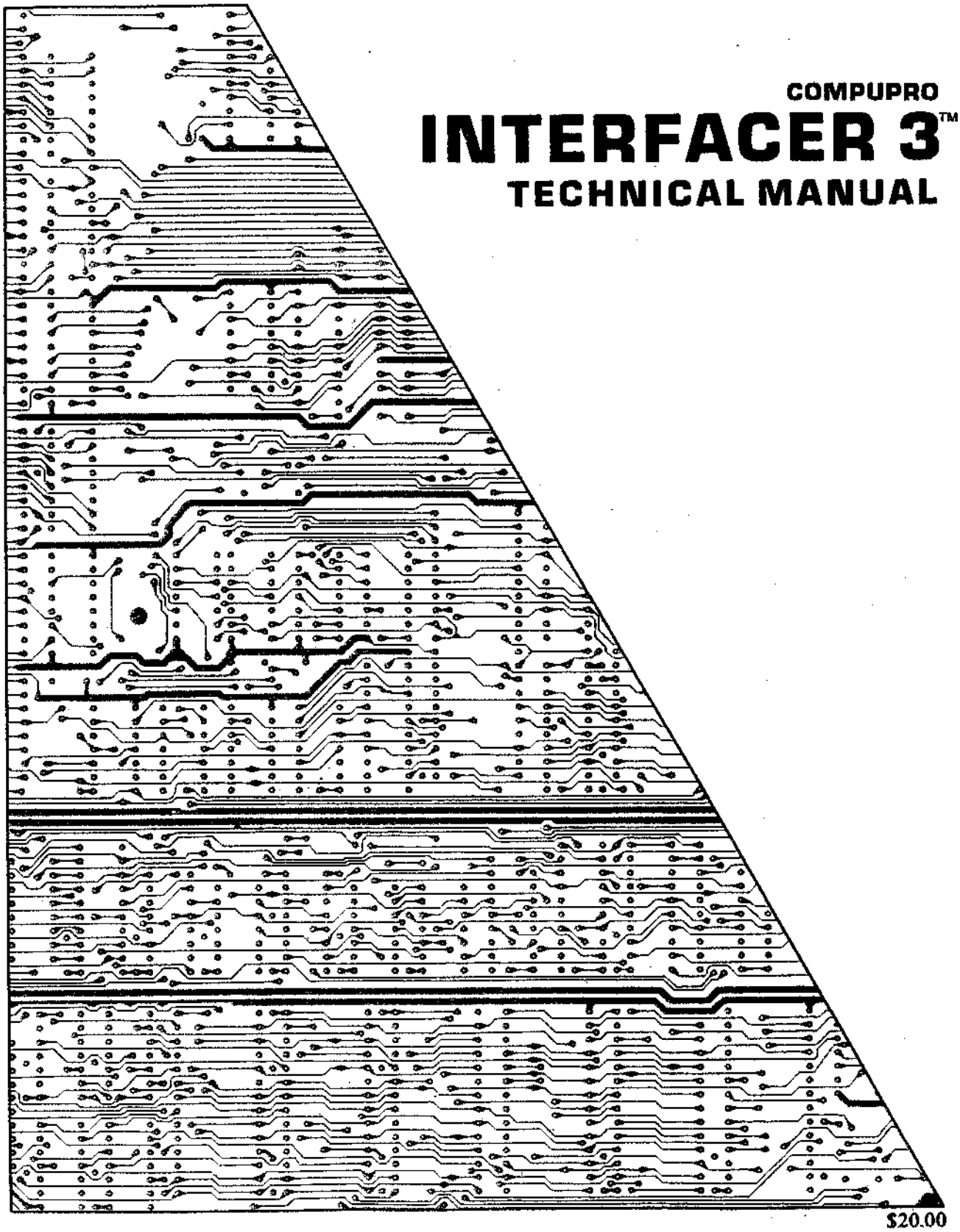
VIASYN™



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INTERFACER 3™

TECHNICAL MANUAL

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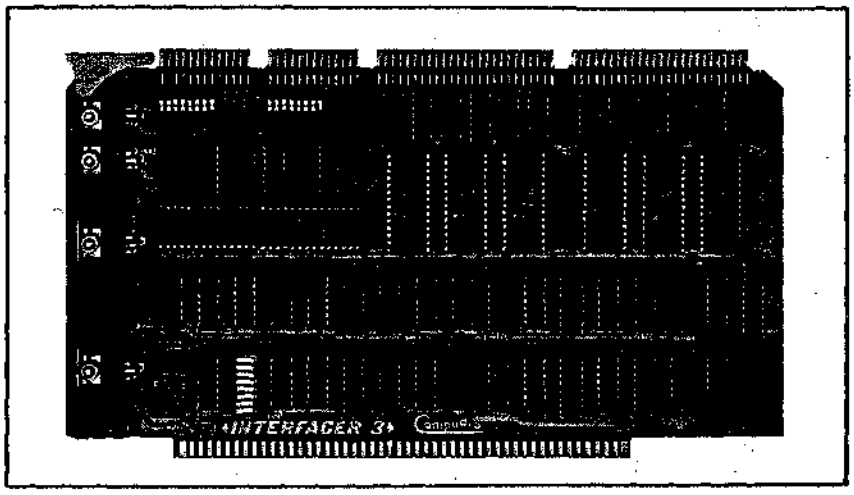
INTERFACER 3

Technical Manual

IEEE 696/S-100



8 CHANNEL SERIAL I/O BOARD
RS-232 with full handshake

INTERFACER 3 TECHNICAL MANUAL

Hayward, CA 94545

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INTERFACER 3 TECHNICAL MANUAL

connected in either DTE mode or DATA COMMUNICATION EQUIPMENT (DCE) mode. This allows direct connection to all types of RS-232 equipment including modems. In addition, these two channels are capable of high speed synchronous operation using internal or external clocks.

PORT MAP

The INTERFACER 3 interface uses a block of eight port addresses for communication between it and the host processor. The address of the first port is switch selectable to any address which is a multiple of eight. The ports will be referred to as relative ports 0 - 7.

RELATIVE PORT	FUNCTION
0	USART Data Register (R/W)
1	USART Status Register (R) SYN1/SYN2/DLE Register (W)
2	USART Mode Register (R/W)
3	USART Command Register (R/W)
4	Transmit Interrupt Status Register (R) Transmit Interrupt Mask Register (W)
5	Receive Interrupt Status Register (R) Receive Interrupt Mask Register (W)
6	Not used
7	User Select Register (write only)

PORT ADDRESSING

DIP switch S1, positions 1 thru 6 are used to select the base address of the eight port block in a binary fashion as shown below:

SWITCH POSITION	ADDRESS BIT	
1	PORT DISABLE WHEN "ON"	
2	A7	
3	A6	"ON" = "0"
4	A5	"OFF" = "1"
5	A4	
6	A3	

EXAMPLE: To address this board at addresses 10H thru 17H for CompuPro operating systems, position 1 and 5 would be "OFF" and positions 2 thru 4 and positions 6 would be "ON".

EXAMPLE: To address this board at addresses 38H thru 3FH, positions 1, 4, 5, and 6 would be "OFF" and positions 2 and 3 would be "ON".

USER/BOARD SELECTION

To select a particular channel and to select which board that channel will be on (when running more that 8 users), requires the use of the User Select Port and two board select switches. The five bit User Select Register determines which of 32 possible users will be selected at a particular time. The two board select switches determine whether a board will respond to users 0 thru 7, 8 thru 15, 16 thru 23, and 24 thru 31. A particular user (0-31) is selected by outputting the five bit number that represents that user. The diagram shown below will describe the relation between the board select switches and the User Select Register.

USER SELECT REGISTER

DATA BIT	NAME	FUNCTION
D0	US0	USER SELECT 0 (LSB)
D1	US1	USER SELECT 1
D2	US2	USER SELECT 2 (MSB)
D3	BS0	BOARD SELECT 0 (LSB)
D4	BS1	BOARD SELECT 1 (MSB)
D5		NOT USED
D6		NOT USED
D7		NOT USED

Since each INTERFACER 3 will support 8 users, we will refer to these eight as RELATIVE USER 0-7. These eight ports are physically configured with relative user 0 on the extreme right side of the board and relative user 7 on the extreme left side. To determine the exact user number, the RELATIVE USER number must be added to the USER OFFSET number. The RELATIVE USER number corresponds to the three bits above called USER SELECT 0-2, and the USER OFFSET number corresponds to the two bits above called BOARD SELECT 0 and 1. These five bits determine the exact user number.

US2	US1	US0	RELATIVE USER NUMBER
0	0	0	USER 0
0	0	1	USER 1
0	1	0	USER 2
0	1	1	USER 3
1	0	0	USER 4
1	0	1	USER 5
1	1	0	USER 6

BOARD SELECT SWITCHES		BOARD SELECT BITS		USER OFFSET
S1-8	S1-7	BS1	BS0	
ON	ON	0	0	0
ON	OFF	0	1	8
OFF	ON	1	0	16
OFF	OFF	1	1	24

EXAMPLE: To address the INTERFACER 3 to respond to users 0 thru 7, switches S1-7 and S1-8 would be "ON". To select a particular user in the group from 0 to 7, BS1 and BS0 must be "0" for the board to respond. To select user 5, a 05H must be sent to the user select port.

EXAMPLE: To address the INTERFACER 3 to respond to users 16 thru 23, switch S1-7 would be "ON", and switch S1-8 would be "OFF". To select a particular user in the group from 16 to 23, BS1 must be a "1" and BS0 must be "0" for the board to respond. To select user 18, a 12H must be sent to the user select port.

WAIT STATE SELECTION

The INTERFACER 3 was designed to run in very fast microcomputer systems by allowing up to two wait states to be added when accessing the USART registers. Since the user select and interrupt control registers are capable of higher speed operation than the USART registers, no wait states are inserted even when they are enabled on the board.

The three vertical pins at J17 control the enabling of one or two wait states. With the black pin shunt connecting pins "A" and "C", one wait state will be inserted. With the pin shunt connecting pins "B" and "C", two wait states will be inserted. If the pin shunt is left removed, no wait states will be inserted.

CABLES

The INTERFACER 3 is designed to use two each of two different cables assemblies. Relative users 0-5 use a custom 50 conductor cable and relative users 6 and 7 use standard 26 conductor cables identical to those used on the INTERFACER 1 and INTERFACER 2.

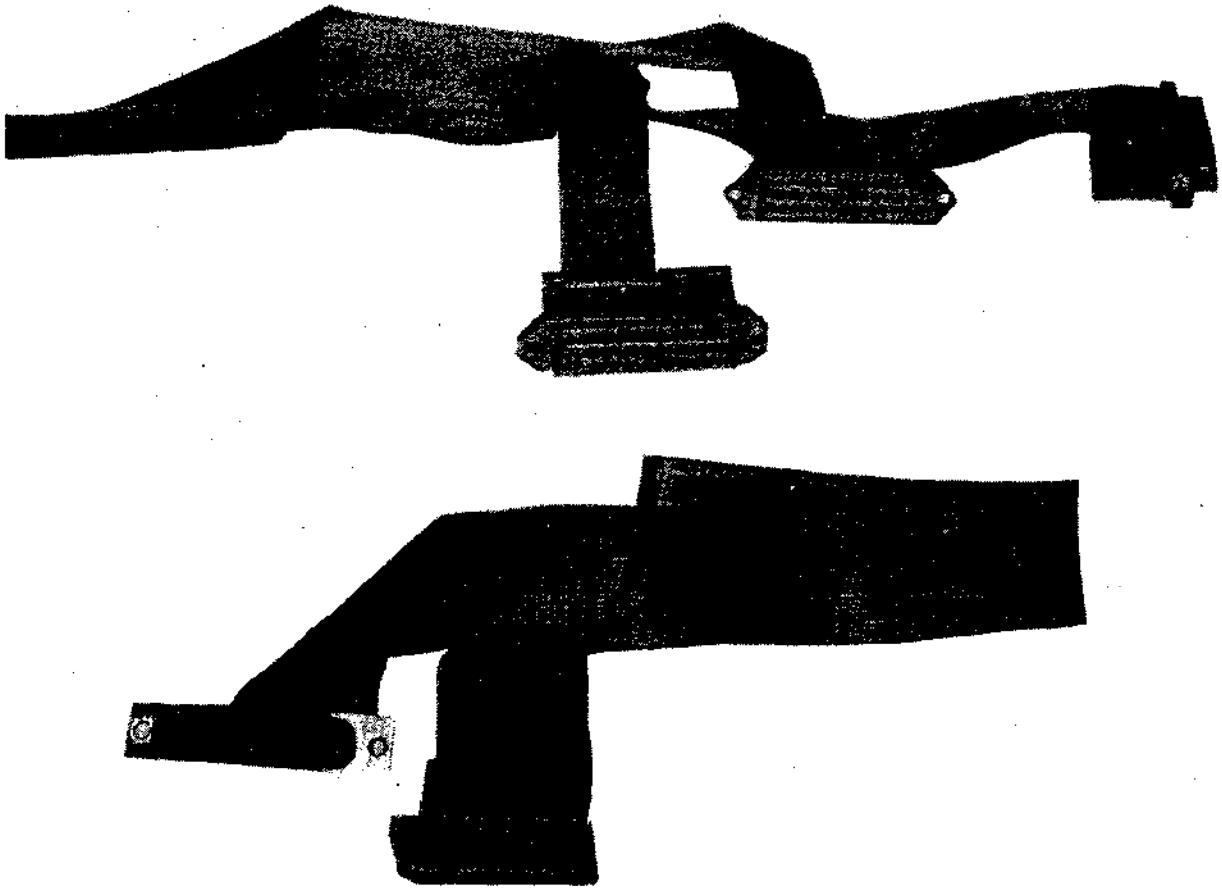
Relative users 0-2 (50 pin connector on the far right) and relative users 3-5 (50 pin connector in middle of board) use a custom three-user cable (see photo A page 7). This cable consists of a female 50 pin insulation displacement connector that splits into thirds and connects to three female DB-25 connectors. The actual cable has positions 1-16 (pin 1 on the far left side of the connector) on the first DB-25, positions 17-32 on the second DB-25, and positions 33-50 on the third DB-25.

NOTE: The pin numbers on the circuit diagram show the pin numbers on the DB-25 connector and not the 50 pin connector.

Relative user 7 (26 pin connector on the far left) and relative user 6 (26 pin connector to the right of user 7) use standard RS-232 I/O

cables (see photo B below). This cable consists of a female 26 pin insulation displacement connector that mates to a female DB-25 (the 26th conductor is not used).

NOTE: The pin numbers on the circuit diagram show the pin numbers on the DB-25 connector and not the 26 pin connector.



SLAVE CLEAR/POWER-ON-CLEAR OPTION

The INTERFACER 3 is designed to be cleared by either pRESET* or SLAVECLR*. In some older non-IEEE 696 processor boards, POC* does not generate SLAVECLR* and pRESET*. On these systems this board might not be cleared upon power-up. By cutting the trace at J18 between "B" and "C", and installing a jumper between holes "A" and "C", this board will be cleared by POC* instead of SLAVECLR*.

USING INTERRUPTS

The INTERFACER 3 has a simple but elegant interrupt structure that allows considerable flexibility. Each USART generates both a transmit and receive interrupt, for a total of 16 distinct interrupts for the board. A transmit interrupt indicates that the USART transmit register is empty and it is ready to accept a character. A receive interrupt indicates that data is available from the receiver data register. Each of these interrupts may be masked "OFF" or "ON" by altering the INTERRUPT CONTROL REGISTERS as described below. Each of these interrupts are open collector, and may be individually tied to any of the eight vectored interrupt lines (VI0-VI7). The status of each interrupt line may be sampled by reading the INTERRUPT STATUS REGISTERS as described below.

Since each of the 16 interrupts generated on the INTERFACER 3 may be tied to any of the eight vectored lines, almost any type of priority scheme may be implemented. All transmit interrupts are brought out on one side of jumper socket J15, and all receive interrupts are brought out on one side of jumper socket J16. On the opposite side of each socket, each of the eight vectored interrupt lines are brought out. By using the provided headers, any USART interrupt may be connected to any VI line. The pin-out of J15 and J16 are shown below.

INTERRUPT	J15		VI LINE	J16		INTERRUPT
TxINT 0 -----	9	8	--- VI0 ---	9	8	----- RxINT 0
TxINT 1 -----	10	7	--- VI1 ---	10	7	----- RxINT 1
TxINT 2 -----	11	6	--- VI2 ---	11	6	----- RxINT 2
TxINT 3 -----	12	5	--- VI3 ---	12	5	----- RxINT 3
TxINT 4 -----	13	4	--- VI4 ---	13	4	----- RxINT 4
TxINT 5 -----	14	3	--- VI5 ---	14	3	----- RxINT 5
TxINT 6 -----	15	2	--- VI6 ---	15	2	----- RxINT 6
TxINT 7 -----	16	1	--- VI7 ---	16	1	----- RxINT 7

EXAMPLE: If you want to generate an interrupt on vectored interrupt line VI3 when data becomes available from relative user 6, solder a wire between pins 2 and 12 of J16.

EXAMPLE: If you want to generate an interrupt on vectored interrupt line VI6 when data becomes available from relative users 0,1,2, and 7, solder a wire to connect pins 1,6,7,8 and 15 of J16.

EXAMPLE: If you want to generate an interrupt on vectored interrupt line VI0 when relative user 2 is ready to accept a character, solder a wire to connect pins 8 and 11 of J15.

CHANNEL 6/7 INTERRUPT OPTION

Relative channels 6 and 7 are capable of generating a third interrupt called TxEMT/DSCHG*. This interrupt occurs when the transmitter has completed serialization of the last character loaded or a change has occurred in the state of the DSR or DCD RS-232 status lines. Additional information on this line may be found in the 2651 data sheet in this manual.

The TxEMT/DSCHG* output from the 2651 may be jumpered to generate either a transmit or receive interrupt. Due to the wire-OR capability of the interrupt outputs from the 2651, when jumpered, the transmit interrupt will become TxRDY OR TxEMT/DSCHG or the receive interrupt will become RxRDY OR TxRDY/DSCHG. Therefore, when jumpered, you must check the status register to determine what condition caused the interrupt.

The following table will demonstrate where to install the shorting plug to generate the appropriate interrupt.

CHANNEL NUMBER	TO CAUSE A TxEMT/DSCHG INTERRUPT ON THE: TxRDY LINE	RxRDY LINE
6	INSTALL J14	INSTALL J13
7	INSTALL J4	INSTALL J3

INTERRUPT CONTROL REGISTERS

Two registers are provided for individually masking the transmit and receive interrupts from the bus. On power-up or reset, all interrupts are disabled on the INTERFACER 3. To gain access to these registers, a user channel must be enabled on the particular board to be altered. (You cannot alter any interrupt register on the board set for users 0 thru 7 unless you have selected one of those eight users) To enable a particular Transmit or Receive interrupt, a "1" must be sent to the proper bit of the register. The registers are configured so that Data Bit 0 will mask relative user 0, D1 will mask relative user 1, and so on with D7 masking relative user 7. This is true for both the Transmit Interrupt Control Register (relative port 4) and the Receive Interrupt Control Register (relative port 5).

EXAMPLE: To enable all Transmit interrupts on a particular INTERFACER 3, send a 0FFH to relative port 4.

EXAMPLE: To enable the transmit interrupt on relative users 1, 4 and 6, send a 52H to relative port 4.

EXAMPLE: To disable all Receive interrupts on a particular INTERFACER 3, send a 00H to relative port 5.

EXAMPLE: To enable the Receive interrupt on relative users 2, 3 and 7, send a 8CH to relative port 5.

INTERRUPT STATUS REGISTERS

Two registers are provided for checking the status of pending transmit and receive interrupts. To gain access to these registers, a user channel must be enabled on the particular board to be altered. (You cannot read any interrupt register on the board set for users 0 thru 7 unless you have selected one of those eight users) If a Transmit or Receive interrupt is pending, a "1" will be present in the proper bit of the status register. The registers are configured so that Data Bit 0 contains the status of relative user 0, D1 contains the status of relative user 1, and so on with D7 containing the status of relative

user 7. This is true for both the Transmit Interrupt Status Register (relative port 4) and the Receive Interrupt Status Register (relative port 5). Remember, these status registers are read only! Writing into these registers will alter the Interrupt Control Mask. In addition, the status of a channel's interrupts are available even if those interrupts are masked "OFF". The Interrupt Control Register does not affect the reading of the status from a register.

EXAMPLE: If all Transmit interrupts on a particular INTERFACER 3 are asserted, you will read a 0FFH at relative port 4.

EXAMPLE: If transmit interrupts are pending on relative users 1, 4 and 6, you will read a 52H from relative port 4.

EXAMPLE: If there are no Receive interrupts pending on a particular INTERFACER 3 (no data available), you will read a 00H from relative port 5.

EXAMPLE: If Receive interrupts are pending on relative users 2, 3 and 7, you will read a 8CH from relative port 5.

USART INITIALIZATION

The serial channels on the INTERFACER 3 are implemented with a 2651 type USART from either National Semiconductor or Signetics. Several of the USART parameters and channel control functions are programmed by writing into or reading from certain registers in the 2651. They are:

1. The baud rate.
2. The word length.
3. Whether or not a parity bit is generated.
4. Whether the parity is even or odd (if generated).
5. The number of stop bits.
6. Enabling and disabling the transmitter and receiver.
7. Setting and testing the RS-232 handshake lines.
8. Synchronous or asynchronous operation.

In addition, the normal status indication and data transfer functions are also handled through the USART's registers.

A table of the various registers and where they appear in the I/O port map is shown in a previous section and in the following tables.

"READ" or "INPUT" Ports

Relative Port Address	UART Register Function
00 hex	Data Port, read received data.
01 hex	Status Port, read UART status info.
02 hex	Mode Registers, read current UART mode.
03 hex	Command Register, read current command.

"WRITE" or "OUTPUT" Ports

Relative Port Address	UART Register Function
00 hex	Data port, write transmit data.
01 hex	SYN1/SYN2/DLE register, write sync bytes.
02 hex	Mode registers, write mode bytes.
03 hex	Command register, write command byte.

USART INITIALIZATION SEQUENCE

When bringing up the USART in asynchronous mode, the following sequence of events must occur:

1. Set Mode Register 1
2. Set Mode Register 2
3. Set Command Register
4. Begin normal USART operation

When bringing up the USART in transparent synchronous mode, all of the following sequence of events must occur. If bringing up the USART in non-transparent synchronous mode, step 5 may be omitted.

1. Set Mode Register 1
2. Set Mode Register 2
3. Set SYN1 Register
4. Set SYN2 Register
5. Set DLE Register
6. Set Command Register
7. Begin normal USART operation

DATA REGISTERS

The UART data registers are straight-forward in their operation. You write a byte to the data register when you want to transmit that byte to an external serial device and you read the byte in the data register to receive a byte from an external serial device. The UART will automatically add the proper start and stop bits when transmitting and will remove them when receiving.

STATUS REGISTER

The status register is used to determine the current state of the UART. Each bit of the status register has a different meaning depending on whether it is high or low. (High means a logic one or high level and low means a logic zero or low level.) The following

table describes the meaning of the status bits:

STATUS REGISTER FORMAT TABLE

STATUS REGISTER FORMAT

BIT NUMBERS

SR-7	SR-6	SR-5	SR-4	SR-3	SR-2	SR-1	SR-0
DATA SET READY 0 = DSR INPUT IS HIGH 1 = DSR INPUT IS LOW	DATA CARRIER DETECT 0 = DCD INPUT IS HIGH 1 = DCD INPUT IS LOW	FE/SYN DETECT ASYN: 0 = NORMAL 1 = FRAMING ERROR SYNC: 0 = NORMAL 1 = SYN CHARACTER DETECTED	OVERRUN 0 = NORMAL 1 = OVERRUN ERROR	PE/DLE DETECT ASYNC: 0 = NORMAL 1 = PARITY ERROR SYNC: 0 = NORMAL 1 = PARITY ERROR OR DLE CHARACTER RECEIVED	TxEMT/DSCHG 0 = NORMAL 1 = CHANGE IN DSR OR DCD, OR TRANSMIT SHIFT REGISTER IS EMPTY	RxRDY 0 = RECEIVE HOLDING REGISTER EMPTY 1 = RECEIVE HOLDING REGISTER HAS DATA	TxRDY 0 = TRANSMIT HOLDING REGISTER BUSY 1 = TRANSMIT HOLDING REGISTER EMPTY

NOTE 1: BAUD RATE FACTOR IN ASYNCHRONOUS MODE APPLIES ONLY IF EXTERNAL CLOCK IS SELECTED. FACTOR IS 16x IF INTERNAL CLOCK IS SELECTED.

MODE REGISTERS

When bringing up the UART, its two mode registers must be set with various bit patterns that will determine the operating modes. There are two registers, however they occupy only one I/O port address. This is accomplished with internal sequencing logic that allows you to write the first register (Mode Register 1) and then the second register (Mode Register 2). It is important to write to Mode Register 1 first.

The meanings of the various bits in the mode registers are described on the next page.

MODE REGISTER 1 AND 2 FORMAT TABLES

MODE REGISTER 1 FORMAT

BIT NUMBERS

MR1-7	MR1-6	MR1-5	MR1-4	MR1-3	MR1-2	MR1-1	MR1-0
SYNC: NO. OF SYN CHARACTERS 0 = DOUBLE SYN 1 = SINGLE SYN	SYNC: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT	PARITY TYPE 0 = ODD 1 = EVEN	PARITY CONTROL 0 = DISABLED 1 = ENABLED	CHARACTER LENGTH 00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		MODE AND BAUD RATE FACTOR[1] 00 = SYNCHRONOUS 1x RATE 01 = ASYNCHRONOUS 1x RATE 10 = ASYNCHRONOUS 16x RATE 11 = ASYNCHRONOUS 64x RATE	

ASYNC:
STOP BIT LENGTH
00 = INVALID
01 = 1 STOP BIT
10 = 1½ STOP BITS
11 = 2 STOP BITS

MODE REGISTER 2 FORMAT

BIT NUMBERS

MR2-7	MR1-6	MR2-5	MR2-4	MR2-3	MR2-2	MR2-1	MR2-0
NOT USED		TRANSMITTER CLOCK 0 = EXTERNAL 1 = INTERNAL	RECEIVER CLOCK 0 = EXTERNAL 1 = INTERNAL	BAUD RATE SELECTION 0000 = 50 BAUD 0001 = 75 BAUD 0010 = 110 BAUD 0011 = 134.5 BAUD 0100 = 150 BAUD 0101 = 300 BAUD	0110 = 600 BAUD 0111 = 1200 BAUD 1000 = 1800 BAUD 1001 = 2000 BAUD 1010 = 2400 BAUD 1011 = 3600 BAUD	1100 = 4800 BAUD 1101 = 7200 BAUD 1110 = 9600 BAUD 1111 = 19200 BAUD	

This completes the description of the Mode Registers. Remember that you must always write both mode registers, with Mode Register 1 first.

COMMAND REGISTER

The Command Register is used to set the operating mode (sync or async), enable or disable the receiver and/or transmitter, force a "break" condition, reset the error flags and control the state of the RTS and DTR outputs.

COMMAND REGISTER TABLE

COMMAND REGISTER FORMAT

BIT NUMBERS

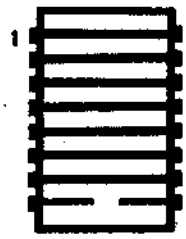
CR-7	CR-6	CR-5	CR-4	CR-3	CR-2	CR-1	CR-0
OPERATING MODE 00 = NORMAL OPERATION 01 = ASYNC: AUTOMATIC ECHO MODE SYNC: SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		REQUEST TO SEND 0 = FORCES $\overline{RTS}$ OUTPUT HIGH 1 = FORCES $\overline{RTS}$ OUTPUT LOW	RESET ERROR 0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REGISTER (FE, OE, PE/DLE DETECT)	ASYNC: FORCE BREAK 0 = NORMAL 1 = FORCE BREAK SYNC: SEND DLE 0 = NORMAL 1 = SEND DLE	RECEIVE CONTROL (R x EN) 0 = DISABLE 1 = ENABLE	DATA TERMINAL READY 0 = FORCES $\overline{DTR}$ OUTPUT HIGH 1 = FORCES $\overline{DTR}$ OUTPUT LOW	TRANSMIT CONTROL 0 = DISABLE 1 = ENABLE

SERIAL MODE JUMPERS

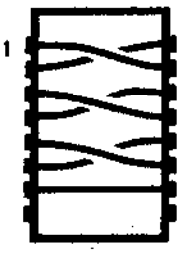
The INTERFACER 3 board with its serial programming jumpers allows the user to adapt relative channels 6 and 7 to all standard RS-232 pin configurations. In RS-232 mode, these jumpers may be set so that this board operates in a "master" mode where it behaves as the Data Terminal Equipment (DTE), or it may be set so that the board operates in a "slave" mode where it behaves as the Data Communication Equipment (DCE). Since almost all CRT terminals and serial interface printers operate as the "master" or as the Data Terminal Equipment, then the INTERFACER 3 board must operate as the "slave" or Data Communication Equipment. (For this reason, relative channels 0 - 5 are set to operate in this mode.) For example, to connect the INTERFACER 3 to a terminal like an Televideo or a Hazeltine, relative channels 0 - 5 will connect directly and relative channels 6 and 7 require that serial mode jumpers (J1 and J2) should be set in "slave" mode as shown on the following table. To connect relative channels 6 and 7 to a modem is a different set-up because modems are set to operate as "slaves". When connected to a modem, the serial mode jumpers (J1 and J2) of the INTERFACER 3 should be set in the "master" mode as shown on the following table.

PROGRAMMING JUMPERS

SLAVE MODE, J1/J2: for connections to CRT terminals, printers, etc.



MASTER MODE, J1/J2: for connection to MODEMS.



RS-232C CONTROL LINES

The RS-232 control and data lines are defined as shown below. The EIA RS-232 standard defines a signal line at greater than +3V (+12V typical) to be "SPACING" and a signal line at less than -3V (-12V typical) to be "MARKING".

PIN#	CIRCUIT	DIR.	NAME	DESCRIPTION
1	AA			PROTECTIVE GROUND
2	BA	TO DCE	TxD	TRANSMITTED DATA
3	BB	TO DTE	RxD	RECEIVED DATA
4	CA	TO DCE	RTS	REQUEST TO SEND
5	CB	TO DTE	CTS	CLEAR TO SEND
6	CC	TO DTE	DSR	DATA SET READY
7	AB			SIGNAL GROUND
8	CF	TO DTE	DCD	REC'D LINE SIGNAL DET.
15	DB	DCE SOURCE	TSET	TRANS. SIG. ELE. TIMING
17	DD	DCE SOURCE	RSET	REC'D SIG. ELE. TIMING
20	CD	TO DCE	DTR	DATA TERMINAL READY

Five hardwired RS-232 handshaking signals are provided for interfacing to equipment needing these lines as shown below. Output lines may be set either "MARKING" or "SPACING" and their state may be altered by software commands as described in the USART INITIALIZATION Section under Command Register.

OUTPUT LINES

NAME	RS-232 LINE	DB25 PIN CONNECTION
DTR	CD	20 OR 6 *
RTS	CA	4 OR 5 *

INPUT LINES

NAME	RS-232 LINE	DB25 PIN CONNECTION
DSR	CC	6 OR 20 *
CTS	CB	5 OR 4 *
DCD	CF	8

*NOTE: Non-starred pin numbers indicate the DB25 pin number for relative channels 0 - 5 and when the Serial Mode Jumpers of relative channels 6 and 7 are set for "master" mode. The starred pin numbers indicate the DB25 pin number on relative channels 6 and 7 when the Serial Mode Jumpers are set for "slave" mode.

SYNCHRONOUS MODE CLOCK DRIVER/RECEIVERS

Relative channels 6 and 7 can either transmit or receive the synchronous signal timing element signals. The typical configuration requires that the DATA COMMUNICATION EQUIPMENT (DCE) be the source of the of the synchronous transmit and receive clocks. The INTERFACER 3 is capable of independently transmitting or receiving either of the clocks in either DCE or DTE modes. The following table will describe how the pin shunts should be set for transmitting or receiving the clocks.

CHANNEL NUMBER	RECEIVE SYNC CLOCK		TRANSMIT SYNC CLOCK	
	TRANSMIT	RECEIVE	TRANSMIT	RECEIVE
6	INSTALL J11	INSTALL J12	INSTALL J9	INSTALL J10
7	INSTALL J7	INSTALL J8	INSTALL J5	INSTALL J6

EXAMPLE: If you want relative channel 7 to transmit both its transmit and receive sync clocks, install pin shunts on J7 and J5.

EXAMPLE: If you want relative channel 6 to receive both its transmit and receive sync clocks, install pin shunts on J10 and J12.

THEORY OF OPERATION

The INTERFACER 3 can be roughly divided into seven subsections for describing its operation. These sections include: The S-100 Bus Drivers, the I/O Port Decode Logic, the Strobe Generation Logic, the Wait State Logic, the Interrupt Control/Status Logic, the USART, and the RS-232 Level Conversion Logic.

S-100 BUS DRIVERS

The separate data input and output data buses of the S-100 bus are converted to a bi-directional data bus by octal drivers U44 and U58. Data from the S-100 bus is driven onto the internal data bus by U58 only when sOUT goes high, indicating an output operation. The internal data bus is driven onto the S-100 bus when DOEN* goes low, indicating that a valid board select (SEL) and pDBIN are high (NAND-U45).

All S-100 bus signals are buffered onto the board if the line would otherwise have more than 1 LSTTL load. Address lines A0, A1, A2, and pDBIN are buffered onto the board by 2/3 of hex buffer U48, and the lines sOUT, sINP, pWR*, O, and pSTVAL* are inverted using portions of U29, U43, and U50.

I/O PORT DECODE LOGIC

The eight port block that the INTERFACER 3 occupies is decoded by six open collector X-OR gates (U46 and U47). Five of these gates decode address lines A3-A7 by comparing against positions 2-6 of switch S1, and the last section compares sOUT and sINP* to determine if an I/O operation is occurring. When all compare conditions are satisfied, ASEL goes high. Closing position 1 of S1 will ground ASEL and disable the board completely.

A valid board select (SEL*) is generated (by 1/3 of U32), when ASEL goes high along with USEL (indicating that this boards select number is active) and A1 and A2 are not both high (indicating the USER SELECT PORT is not selected). SEL* is disabled by 1/3 of U32 when the USER SELECT PORT is enabled so that conflicts between up to four boards does not occur.

A USER SELECT write occurs when ASEL, A1, A2, sOUT, and STROBE go high. This generates OUT0* (U32) which clocks the least significant five bits on the bus (D0-D4) into hex latch U34. The three low order bits of U34 are decoded into eight chip enables (CE0* - CE7*) by U35 when SEL is high and A2 and ESTROBE* are low. The two high order bits of U34 are compared to switch positions 7 and 8 of S1 by 1/2 of U47 (X-NOR) to decode a current user board select signal USEL. Access to registers on the board requires that USEL be high before access is gained.

The four interrupt read and write strobes are generated by decoder U49 when A2 is high and SEL* and STROBE* are low. A0, A1, and sINP* determine which output becomes active at the proper time.

STROBE GENERATION LOGIC

In order to gain additional access time in an I/O cycle for the 2651 USARTs, the INTERFACER 3 generates early strobes based on valid status. S-100 bus strobes pDBIN and pWR* are gated together (U30) and inverted to generate STROBE and STROBE*. These signals indicate that a bus strobe is occurring. The interrupt registers and user select port have their data gated by STROBE because they are TTL and capable of very high speed operation. Since the 2651 type USART is a MOS device and has an access time of approximately 250 nS, an early strobe is generated so that wait states are avoided whenever possible. A status valid signal, ESTATVAL*, is generated whenever pSYNC is high and pSTVAL* is low. ESTATVAL* clears "D" flop U33a to generate ESTROBE*, which becomes one term of the USART chip enable decoder U35. The termination of STROBE* causes a "1" to be clocked into U33a and terminate ESTROBE*.

WAIT STATE LOGIC

To allow operation with high speed processors, a wait state generator allows the addition of one or two wait cycles. U31 forms a two bit shift register clocked by O*. A wait state is left pending after STROBE goes low, and when STALL1* or STALL2* and A2 are low (U30), and SEL is high (U45), WAIT* is generated. STALL1* is clocked out on the next rising edge of O* after STROBE goes high, and STALL2* is clocked out the following cycle. The pRDY* line is pulled low by U48 when WAIT* goes low. When neither STALL1* or STALL2* is connected on J17, no wait states will be generated.

INTERRUPT CONTROL/STATUS LOGIC

The interrupt logic consists of two 8-bit latches for enabling interrupts onto the bus, two 8-bit buffers for reading current interrupt status, and sixteen 2-input open collector NAND buffers for driving the interrupts on the bus.

Two 8-bit latches are formed by four 4-bit latches (U38, U41, U52, and U55) for generating the interrupt enable mask. The Q outputs become the RxINTENx and TxINTENx interrupt enables for selectively masking "OFF" individual interrupts. Upon power-up or reset, these latches are cleared by CLR* so that all interrupts are disabled.

The TxRDY and RxRDY interrupt outputs from the 2651 USARTs are inverted to form active high interrupt signals. These interrupt signals are fed to one input of the open collector NAND buffer, with the corresponding interrupt enable fed to the other input. The resulting interrupt outputs (TxINTx and RxINTx) are capable of driving

the VI0-7 lines directly, and are brought out to J15 and J16 for jumpering to the appropriate line.

Two 8-bit buffers are formed from four quad tri-state buffers (U37, U42, U51, and U56) for gating the current USART interrupts (TxRDYx and RxRDYx) onto the bus as status information. Since the buffers use Tx and Rx RDY instead of Tx and Rx INT lines, the status of disabled interrupts are displayed as well as enabled interrupts.

Relative channels 6 and 7 allow jumpering the TxEMT/DSCHG interrupt from the USART to either the TxRDY or RxRDY interrupt outputs. This is possible since the outputs from the 2651 are open drain and may be wire-ORed.

USARTS

The 2651 type USART is quite sophisticated in that it can run in both asynchronous as well as synchronous modes. In addition, the part has an internal baud rate generator, RS-232 status and control bits, up to three interrupt outputs, and the capability of transmitting as well as receiving baud clocks.

The chip enable (CE) and read/write (R*/W) lines are operated by initially determining whether a read or a write will occur (sINP* to R*/W) and then strobing the part with CE*. Address lines A0 and A1 determine which of four registers will be selected and CLR resets the USART.

The baud rate clock BAUDCLK is generated by a 5.0688 MHz crystal oscillator formed from three inverters (U29) and crystal X1.

RS-232 LEVEL CONVERSION LOGIC

Each USART has a full compliment of RS-232 handshaking lines for devices that require them. Industry standard 1488 and 1489 receivers and transmitters are used throughout for highest performance. In addition to the data lines TxD and RxD, each channel has a RTS and DTR output and a CTS, DSR, and DCD input. All three RS-232 status lines have pullup resistors to +12V so that floating inputs are pulled high.

Relative channels 0 - 5 have the RS-232 lines set for direct connection to CRT terminals and printers. Relative channels 6 and 7 may be set for both DCE and DTE modes by wiring new jumpers for J1 and J2.

Relative channels 6 and 7 are capable of sending and receiving both the transmit and receive baud clocks for running in synchronous mode. An RS-232 driver and a receiver are provided for RxC and TxC, and either one may be jumpered in.

SAMPLE TEST PROGRAM FOR RUNNING IN ASYNCHRONOUS MODE

```
*
*
*                INTERFACER 3 TEST PROGRAM
*
* This program will initialize all 2651s for asynchronous operation
at 9600 baud with 8 data bits, one stop bit, no parity. This program
will echo all characters received on any user channel (from 0 to 31)
and if any user sends a ^C, the program will terminate and return back
to CP/M.

NOTE: This program assumes that the console device is either an
INTERFACER 1 or 2 addressed at ports 0 and 1.
*
*
base    equ     18h
udata   equ     BASE+0h  ;data port in and out
ustat   equ     BASE+1h  ;status register port
mode    equ     BASE+2h  ;mode register port
commr   equ     BASE+3h  ;command register port
txreg   equ     BASE+4h  ;tx int register
rxreg   equ     BASE+5h  ;rx int register
user    equ     BASE+7h  ;port to select user
exit    equ     0        ;CP/M reentry point
tbmt    equ     01h      ;transmitter buffer empty
dav     equ     02h      ;data available
*
*
*
        org     100h
Start   mvi     a,0ffh   ;init user
Loop    inr     a        ;next user
        cpi     20H      ;check for final uart
        jz      echo     ;start echo routine
        out     user     ;select uart
        mov     b,a      ;save user in b
        call    init     ;init the uart
        mov     a,b      ;restore user
        jmp     loop     ;next
Init    mvi     a,0CEh   ;set up the 2651
        out     mode     ;send to mode register 1
        mvi     a,7Eh    ;9600 baud, internal clocks
        out     mode     ;SEND BYTE TO M.R. 2
        mvi     a,27h    ;could be 07h (no 1420)
        out     commr
        ret
Echo    mvi     a,0FFh   ;mask value
        out     txreg    ;set tx int reg
        out     txreg    ;set rx int reg
Loop1   inr     a        ;next user
        out     user     ;select uart
        mov     b,a      ;save user in b
                call     cstat   ;check for data
```

```
        cpi     0AAh    ;data if aa
        cz      ok      ;do echo loop
        mov     a,b     ;restore user
        jmp     loop1   ;next
Ok      call    inloop  ;get data
        call    oloop   ;output data
        ret
Cstat   in      ustat   ;look for key entry
        ani     dav     ;check status
        jz      nodat   ;no data
        mvi     a,0AAh  ;data char
        ret
Nodat   mvi     a,0     ;no data char
        ret
Inloop  in      ustat   ;look for key entry
        ani     dav     ;check the status
        jz      inloop  ;wait for key entry
        in      udata   ;get key entry
        ani     7Fh     ;mask parity off
        cpi     03h     ;has a ^c been hit?
        jz      done    ;return to CP/M
        mov     e,a     ;save input in E reg.
        ret
Oloop   in      ustat   ;check ready for output
        ani     tbmt    ;check status
        jz      oloop   ;wait for ready
        mov     a,e     ;get data
        out     udata   ;output character
        ret
Done    jmp     exit    ;return to cp/m
        end
```

```
*
*
*          INTERFACER 3 SYNCHRONOUS TEST PROGRAM
*
*
* This program will take characters typed on the console and transmit
them synchronously at 19.2K baud out of relative user 6 to relative
user 7, and then back out of 7 to 6 and back to the console. When a
control C (^C) is hit on the console, the program will terminate and
re-enter CP/M.

NOTE: This program assumes that the console device is an INTERFACER 1
or 2 at ports 0 and 1. It does not use direct BIOS entry points. The
synchronous clock jumpers should be set as described in the example in
the SYNCHRONOUS MODE CLOCK DRIVER/RECEIVER section. The
SERIAL MODE JUMPERS should be set so that channel 7 is in master mode
and 6 is in slave mode.
*
*
base    equ   10h
udata   equ   base+0h ;data port in and out
ustat   equ   base+1h ;status register port
mode    equ   base+2h ;mode register port
commr   equ   base+3h ;command register port
txreg   equ   base+4h ;tx int register
rxreg   equ   base+5h ;rx int register
user    equ   base+7h ;port to select user
exit    equ   0       ;CP/M reentry point
cstat   equ   01h     ;console status port
cdata   equ   00h     ;console data port
tbmt    equ   01h     ;transmitter buffer empty
dav     equ   02h     ;data available
*
*
*
        org   100h
START   mvi   a,0ffh  ;mask value
        out   txreg   ;set tx int reg
        out   rxreg   ;set rx int reg
INIT6   mvi   a,6h    ;init user 6
        out   user    ;select uart
        mvi   a,08cH  ;set up the 2651
        out   mode    ;send to mode register 1
        mvi   a,0fh   ;19200 baud, external clocks
        out   mode    ;send to mode register 2
        mvi   a,0a5h  ;synch character
        out   ustat   ;send to synch reg
        mvi   a,67h   ;synch strip mode
        out   commr   ;send to command register
        mvi   a,0a5h  ;dummy synch character
        out   udata   ;poke in butt to start
INIT7   mvi   a,7h    ;init user 7
        out   user    ;select uart
        mvi   a,08cH  ;set up the 2651
```

```
        out     mode    ;send to mode register 1
        mvi     a,3fh   ;19200 baud, internal clocks
        out     mode    ;send to mode register 2
        mvi     a,0a5h  ;SYN1 character
        out     ustat   ;send to synch reg
        mvi     a,67h   ;synch strip mode
        out     commr   ;send to command register
        mvi     a,0a5h  ;dummy synch character
        out     udata   ;poke in butt
CONIN   in      cstat   ;look for key entry
        ani     dav     ;check status
        jz      conin   ;no data
        in      cdata   ;get char
        ani     7fh     ;mask parity off
        cpi     03      ;has a ^c been hit?
        jz      done    ;return to CP/M
        mov     l,a     ;save in l
OUT6    mvi     a,6     ;user 6
        out     user    ;select
OUT6L   in      ustat   ;look for ready
        ani     tbmt    ;check the status
        jz      out6l   ;wait for ready
        mov     a,l     ;restore character
        out     udata   ;output char
IN7     mvi     a,7     ;user 7
        out     user    ;select
IN7L    in      ustat   ;get status
        ani     dav     ;check for char
        jz      in7l    ;no char
        in      udata   ;get char
        mov     l,a     ;save char
OUT7    in      ustat   ;check ready for output
        ani     tbmt    ;check status
        jz      out7    ;wait for ready
        mov     a,l     ;get data
        out     udata   ;output character
IN6     mvi     a,6     ;user 6
        out     user    ;select
IN6L    in      ustat   ;get status
        ani     dav     ;check for char
        jz      in6l    ;no char
        in      udata   ;get char
        mov     l,a     ;save char
CONOUT  in      cstat   ;check ready for output
        ani     tbmt    ;check status
        jz      conout  ;wait for ready
        mov     a,l     ;get data
        out     cdata   ;output character
        jmp     conin
DONE    jmp     exit    ;return to cp/m
        end
```

```
;       CompuPro INTERFACER 3 equates.

GBI3:   EQU     10h             ;INTERFACER 3 BASE
GBUD:   EQU     GBI3+0          ;Uart data port
GBUS:   EQU     GBI3+1          ;Uart status port
GBUM:   EQU     GBI3+2          ;Uart mode port
GBUC:   EQU     GBI3+3          ;Uart command port
GBUSR   EQU     GBI3+7          ;User select register
I3DAV:  EQU     02H             ;INTERFACER 3 DAV
I3TBMT: EQU     01H             ;INTERFACER 3 TBMT

;       C O N S O L E   I N I T I A L I Z A T I O N
;
;       This routine performs the initialization
;       required by the INTERFACER 3 USART.
;

sTINIT  MVI     A,0             ;select user "0"
        OUT     GBUSR           ;output to select user
        MVI     A,0EEH          ;8 bits, no parity, 2 stops
        OUT     GBUM            ;Set up mode register 1
        MVI     A,07EH          ;9600 baud
        OUT     GBUM            ;Set up mode register 2
        MVI     A,027H          ;dtr low, no break,
                                ;no reset, rts low
        OUT     GBUC            ;Set up command port
        RET

;       C O N S O L E   S T A T U S
;
;       This routine samples the Console status and returns
;       the following values in the A register.
;
;       EXIT    A = 0 (zero), means no character
;               currently ready to read.
;
;               A = FFh (255), means character
;               currently ready to read.

sCONST  IN      GBUS            ;Input from port
        ANI     I3DAV           ;Mask data available
        RZ                      ;If data not available
        ORI     0FFH
        RET

;       C O N S O L E   I N P U T
;
;       Read the next character into the A register,
;       clearing the high order bit. If no character
;       currently ready to read then wait for a character
;       to arrive before returning.
;
```

```
;       EXIT    A = character read from terminal.

sCONIN  IN      GBUS            ;Get status from uart
        ANI     I3DAV
        JZ      sCONIN
        IN      GBUD
        ANI     7Fh
        RET

; C O N S O L E   O U T P U T
;
; Send a character to the console.  If the console
; is not ready to receive a character wait until
; the console is ready.
;
; ENTRY     C = ASCII character to output to console.

sCONOUT IN      GBUS            ;Get uart status
        ANI     I3TBMT          ;Test if buffer empty
        JZ      sCONOUT
        MOV     A,C
        OUT     GBUD
        RET

;       End     GBcbioI3.asm
```

National Semiconductor

October 1980

INS2651 Programmable Communications Interface

General Description

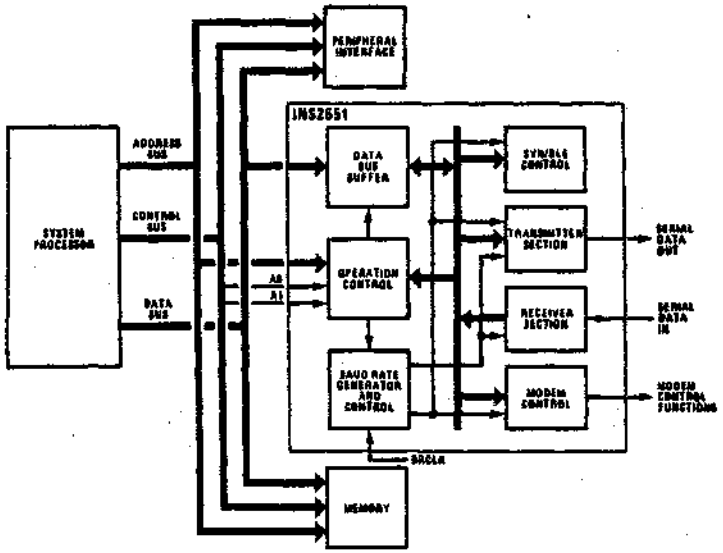
The INS2651 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as a serial data input/output interface in a bus structured system. The functional configuration of INS2651 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communications signal presently in use.

The INS2651 can be programmed to receive and transmit either synchronous or asynchronous serial data. The INS2651 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS2651 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the INS2651, as well as error conditions (parity, overrun, or framing).

Features

- Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Selectable 1 or 2 SYNC Characters
  - Transparent or Non-Transparent Mode
  - Automatic SYNC or DLE-SYNC Insertion
  - SYNC or DLE Stripping
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - 3 Selectable Clock Rates (1x, 16x, or 64x the Baud Rate)
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
- Baud Rates
  - DC to 0.8 M Baud (Synchronous)
  - DC to 0.8 M Baud (1x, Asynchronous)
  - DC to 50 k Baud (16x, Asynchronous)
  - DC to 12.5 k Baud (64x, Asynchronous)
- Internal or External Baud Rate Clock
  - 16 Internal Rates (50 to 19,200 Baud)
- Double Buffering of Data
- TTL Compatible
- No System Clock Required
- Direct Plug-In Replacement for Signetics 2651

INS2651 General System Configuration



Absolute Maximum Ratings

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Voltages with Respect to Ground	−0.5 V to +6.0 V

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.*

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%, GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage		0.25	0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	2.8		V	I_{OH} = −100 μA
I_{IL}	Input Load Current			10	μA	V_{IN} = 0 V to 6.5 V
I_{LD}	Data Bus Leakage Current			10	μA	V_{OUT} = 4.0 V
I_{LO}	Open Drain Leakage Current			10	μA	V_{OUT} = 4.0 V
I_{CC}	Power Supply Current		65	150	mA	

Capacitance

T_A = +25°C; V_{CC} = GND = 0 V

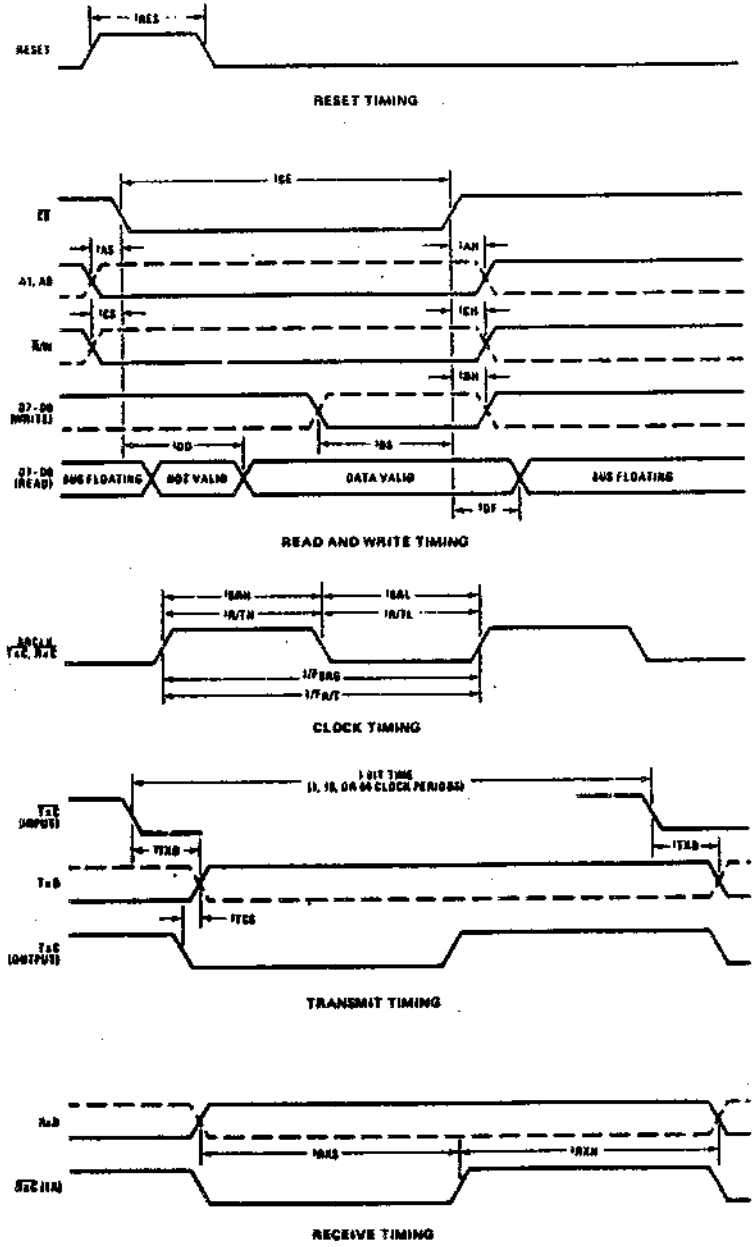
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			20	pF	f_c = 1 MHz
C_{OUT}	Output Capacitance			20	pF	Unmeasured pins to ground
$C_{I/O}$	I/O Capacitance			20	pF	

AC Electrical Characteristics

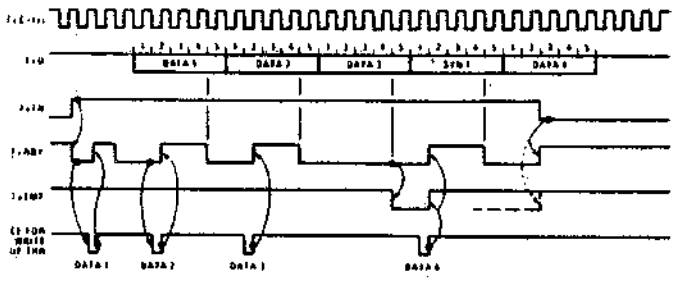
T_A = 0°C to +70°C; V_{CC} = +5.0V ± 5%, GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
BUS PARAMETERS						
t_{CE}	Chip Enable Pulse Width	300			ns	
t_{AS}	Address Setup Time	20			ns	
t_{AH}	Address Hold Time	20			ns	
t_{CS}	R/$\overline{W}$ Control Setup Time	20			ns	
t_{CH}	R/$\overline{W}$ Control Hold Time	20			ns	
t_{DS}	Data Setup Time for Write	225			ns	
t_{DH}	Data Hold Time for Write	50			ns	
t_{DD}	Data Delay Time for Read			250	ns	C_L = 100pF
t_{DF}	Data Bus Floating Time for Read			150	ns	C_L = 100pF
OTHER TIMINGS						
t_{RES}	RESET Pulse Width	1000			ns	
f_{BRG}	Baud Rate Generator Input Clock Frequency	1.0	5.0688	5.073	MHz	
t_{BRH}	Baud Rate Clock High State	70			ns	
t_{BRL}	Baud Rate Clock Low State	70			ns	
$f_{R/T}$	$\overline{TxC}$ or $\overline{RxC}$ Input Clock Frequency	DC		0.769	MHz	
$t_{R/T\,H}$	$\overline{TxC}$ or $\overline{RxC}$ Clock High State	650			ns	
$t_{R/T\,L}$	$\overline{TxC}$ or $\overline{RxC}$ Clock Low State	650			ns	
t_{TxD}	TxD Delay from Falling Edge of $\overline{TxC}$			850	ns	C_L = 100pF
t_{TCS}	Skew Between TxD Changing and Falling Edge of $\overline{TxC}$ Output		0	0	ns	C_L = 100pF
t_{RxS}	Rx Data Setup Time	300			ns	
t_{RxH}	Rx Data Hold Time	300			ns	

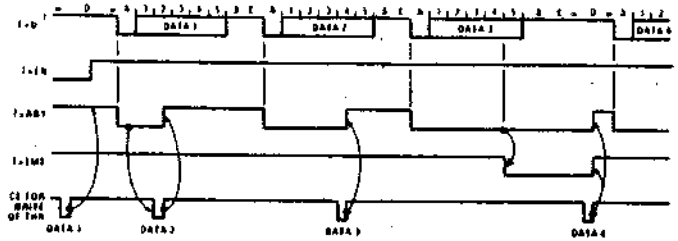
Timing Waveforms



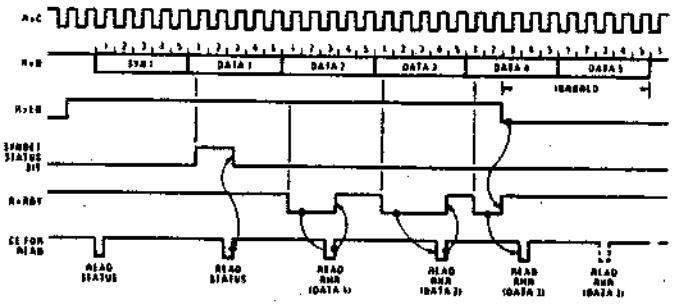
Timing Waveforms (cont'd.)



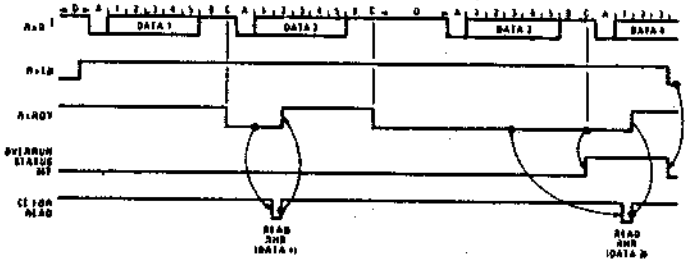
SYNCHRONOUS MODE



ASYNCHRONOUS MODE

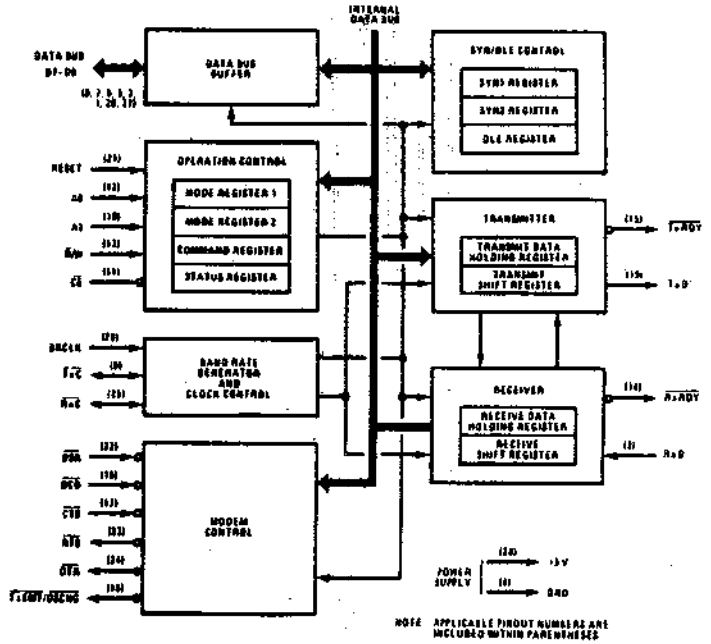


SYNCHRONOUS MODE



ASYNCHRONOUS MODE

INS2651 Block Diagram



INS2651 Functional Pin Definitions

The following describes the function of all the INS2651 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Reset (RESET), Pin 21: When high, performs a master reset on the INS2651. This signal asynchronously terminates any device activity and clears the Mode, Command, and Status Registers. The device assumes the idle state and remains in this mode until initialized with the appropriate control words.

Address Lines (A1–A0), Pins 10, 12: Address lines used to select internal Mode and Command registers.

Read/Write ($\overline{R}$/W), Pin 13: Controls the direction of data bus transfers. A high input allows data from the CPU to be loaded into the addressed register. A low input causes the contents of the addressed register to be present on the data bus.

Chip Enable ($\overline{CE}$), Pin 11: When low, indicates that control and data lines to the device are valid and that the specified operation should be performed. When high, places the device in the TRI STATE® condition.

Baud Rate Generator Clock (BRCLK), Pin 20: 5.0688 MHz clock input to the internal Baud Rate Generator. Not required if external receiver and transmitter ($\overline{TxC}$ and $\overline{RxC}$) clocks are used.

Receiver Data (RxD), Pin 3: Serial data input to the receiver.

Data Set Ready ($\overline{DSR}$), Pin 22: General-purpose input which, when low, indicates either the Data Set Ready or Ring condition. Its complement is stored as Status Register bit 7. A change in state of this input causes a low output on $\overline{TXEMT/DSCHG}$.

Data Carrier Detect ($\overline{DCD}$), Pin 16: When low, enables the receiver to operate. The complement of this input is stored as Status Register bit 6, and an input change of state causes a low output on $\overline{TXEMT/DSCHG}$.

Clear to Send ($\overline{CTS}$), Pin 17: When low, enables the transmitter to operate. When high, holds the TxD output in MARK condition.

V_{CC}, Pin 26: +5-volt supply

Ground, Pin 4: 0 volt reference

OUTPUT SIGNALS

Transmitter Ready ($\overline{TxRDY}$), Pin 15: A low on this output, which is open-drain, indicates that Transmit Holding Register (THR) is ready to accept a data character from the CPU. This output, which is the complement of Status Register bit 0, goes high when the data character is loaded and is valid only when the transmitter is enabled. The $\overline{TxRDY}$ output can be used as an interrupt to the system.

Receiver Ready ($\overline{RxRDY}$), Pin 14: A low on this output, which is open-drain, indicates that the Receive Holding Register (RHR) has a character ready for input to the CPU. This output, which is the complement of Status Register bit 1, goes high either when the Receiver Holding Register is read by the CPU or when the receiver is disabled. The $\overline{RxRDY}$ output can be used as an interrupt to the system.

Transmitter Empty or Data Set Change ($\overline{TxEMT/DSCHG}$), Pin 18: A low on this output, which is open-drain, indicates that either the transmitter has completed serialization of the last character loaded by the CPU or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. If the TxEMT condition does not exist, this output goes high when the Status Register is read by the CPU. Otherwise, the Transmit Holding Register must be loaded by the CPU for this line to go high. The $\overline{TxEMT/DSCHG}$ output can be used as an interrupt to the system. This output is the complement of Status Register bit SR2.

Transmitter Data ($\overline{TxD}$), Pin 19: Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) when the transmitter is disabled.

Data Terminal Ready ($\overline{DTR}$), Pin 24: General-purpose output normally used to indicate Data Terminal Ready. The $\overline{DTR}$ output is the complement of Command Register bit 1.

Request to Send ($\overline{RTS}$), Pin 23: General-purpose output normally used to indicate Request to Send. The $\overline{RTS}$ output is the complement of Command Register bit 5.

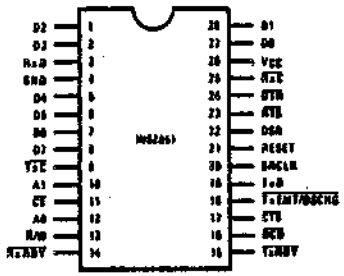
INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus, Pins 29, 27, 9, 7, 6, 5, 2, 1: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS2651 and the CPU. Data, control words, and status information are transferred via the Data Bus.

Receiver Clock ($\overline{RxC}$), Pin 25: If external receiver clock is programmed, this input controls the rate at which a data character is received. The frequency of the $\overline{RxC}$ input is a multiple (1x, 16x, or 64x) of the Baud Rate. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1x the programmed Baud Rate.

Transmitter Clock ($\overline{TxC}$), Pin 9: If external transmitter clock is programmed, this input controls the rate at which a data character is transmitted. The frequency of the $\overline{TxC}$ input is a multiple (1x, 16x, or 64x) of the Baud Rate. Transmitter Data is clocked out of the INS2651 on the falling edge of the $\overline{TxC}$ input. If internal transmitter clock is programmed, this pin becomes an output at 1x the programmed Baud Rate.

Pin Configuration



INS2651 Programming

The system software determines the operative conditions (mode selection, clock selection, data format, and so forth) of the INS2651 via internal Mode Registers 1 and 2, and the Command Register. Prior to initiating data communications, the INS2651 operational mode must be programmed by performing write operations to these 8 bit registers via the Data Bus. The device can be reprogrammed at any time during program execution. However, the receiver and transmitter should be disabled if the change has an effect on the reception or transmission of a character.

The internal registers of the INS2651 are accessed by applying signals to the $\overline{CE}$, R/$\overline{W}$, A1, and A0 inputs as specified in table 1.

Table 1. Guess My Name

$\overline{CE}$	A1	A0	R/$\overline{W}$	Function
1	X	X	X	TRI-STATE Data Bus
0	0	0	0	Read Receive Holding Register
0	0	0	1	Write Transmit Holding Register
0	0	1	0	Read Status Register
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers 1 and 2
0	1	0	1	Write Mode Registers 1 and 2
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

In the case of multiple registers (SYN1/SYN2/DLE Registers and Mode Registers 1 and 2), successive read or write operations will access the next higher register. For example, if A1 equals 0, A2 equals 1, and R/$\overline{W}$ equals 1, the first write operation loads SYN1 Register. The next write operation loads SYN2 Register, and the third loads the DLE Register. Read and write operations are performed on the Mode Registers in a similar manner. If more than the required number of accesses is made, the internal register pointer returns to the first register. The pointers are reset to the first registers either by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

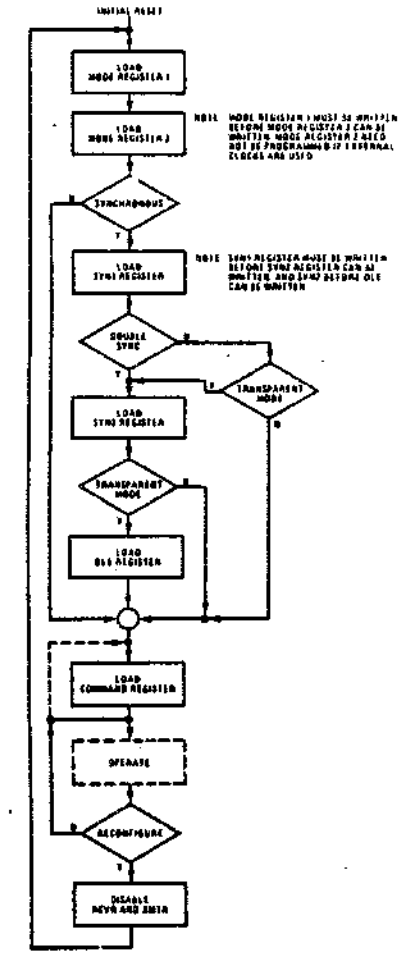
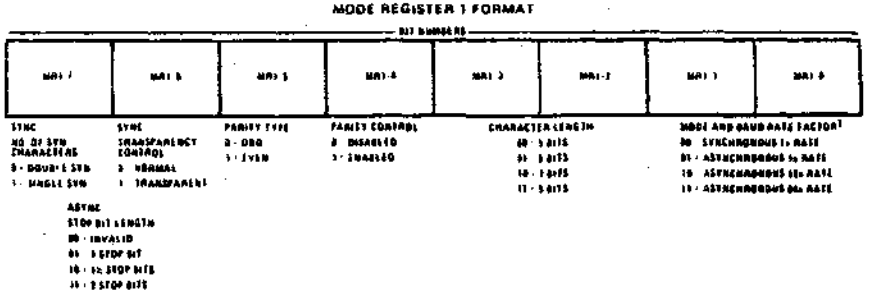
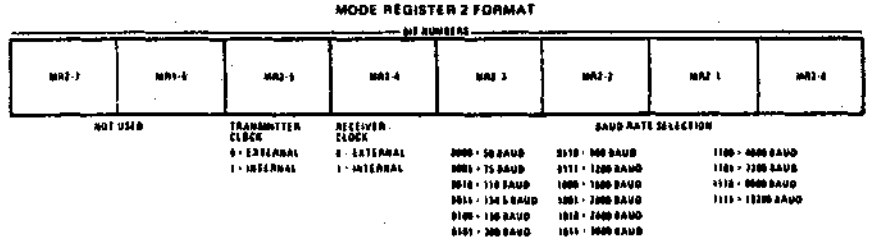
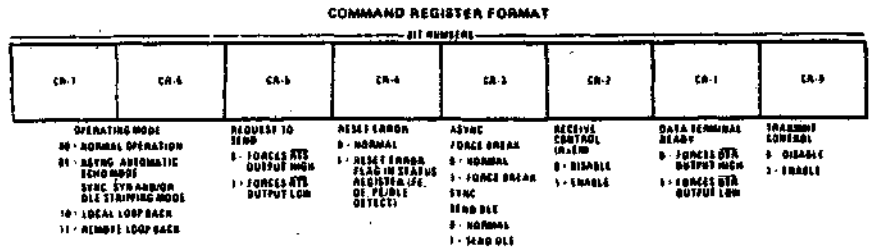
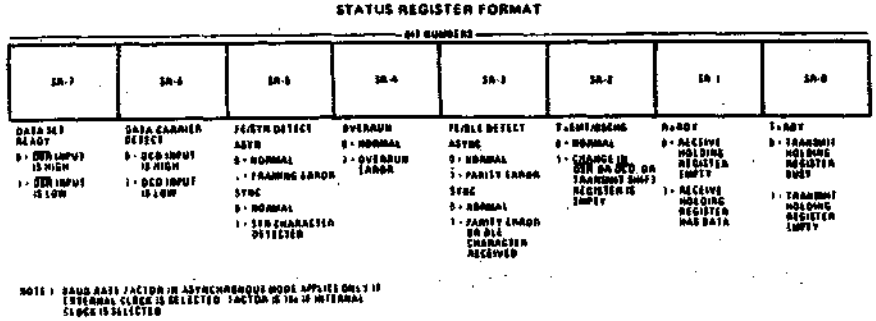


Figure 1. Initialization Flowchart









NOTE 1: BAUD RATE FACTOR IN ASYNCHRONOUS MODE APPLIES ONLY IF EXTERNAL CLOCK IS SELECTED. FACTOR IS 16x IF INTERNAL CLOCK IS SELECTED.

Table 2. Baud Rate Generator Characteristics (Crystal Frequency = 5.0688 MHz)

Baud Rate	Theoretical Frequency 16x Clock (kHz)	Actual Frequency 16x Clock (kHz)	Percent Error	Duty Cycle (%)	Divisor
50	0.8	0.8	–	50/50	6336
75	1.2	1.2	–	50/50	4224
110	1.76	1.76	–	50/50	2880
134.5	2.152	2.1523	0.016	50/50	2355
150	2.4	2.4	–	50/50	2112
300	4.8	4.8	–	50/50	1056
600	9.6	9.6	–	50/50	528
1200	19.2	19.2	–	50/50	264
1800	28.8	28.8	–	50/50	176
2000	32.0	32.081	0.253	50/50	158
2400	38.4	38.4	–	50/50	132
3600	57.6	57.6	–	50/50	88
4800	76.8	76.8	–	50/50	66
7200	115.2	115.2	–	50/50	44
9600	153.6	153.6	–	48/52	33
19200	307.2	316.8	3.125	50/50	16

Note: 16x clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1x and duty cycle is 50%/50% for any baud rate.

INS2651 Operation

GENERAL

The transmitter section of the INS2651 performs parallel-to-serial conversion of data supplied to it from the system data bus.

The receiver section of the INS2651 performs serial-to-parallel conversion of data received from the MODEM or input/output device. Both the transmitter and receiver are double buffered, allowing a full character time in which to service Transmit Ready ($\overline{T_xRDY}$) and Receive Ready ($\overline{R_xRDY}$) interrupts.

The character size (5, 6, 7, or 8 bits) is program selectable. Parity check/generation and the baud rate may also be defined by the program. Note that the character size is exclusive of the start/stop and parity bits.

SYNCHRONOUS MODE

The transmitter starts transmitting a continuous bit stream once the transmitter is enabled and the Clear to Send ($\overline{CTS}$) input is low. If the system is late in supplying a character to the transmitter, then the transmitter will send the SYN character (or SYN1, two characters if in double SYNC mode) as an idle fill in the Non-Transparent mode, or the DLE-SYN1 character pair as an idle fill in the Transparent mode. If this condition occurs, the $\overline{T_xEMT/DSCHG}$ output goes low.

The receiver enters a character synchronization mode as soon as the receiver is enabled and the Data Carrier Detect ($\overline{DCD}$) input goes low. Either one or two consecutive SYN characters must be recognized by the receiver. The number of SYN characters is program selectable, and data is sent to the processor only after synchronization. The SYN character(s) in the Transparent mode (or DLE-SYN1 characters in the Non-Transparent mode) are stripped off the data stream after synchronization. This feature is program selectable.

An overrun error will occur if the processor is late in servicing the received character. When this condition occurs, the character in the receiver buffer is written over by the character causing the overrun, and the overrun status bit is set.

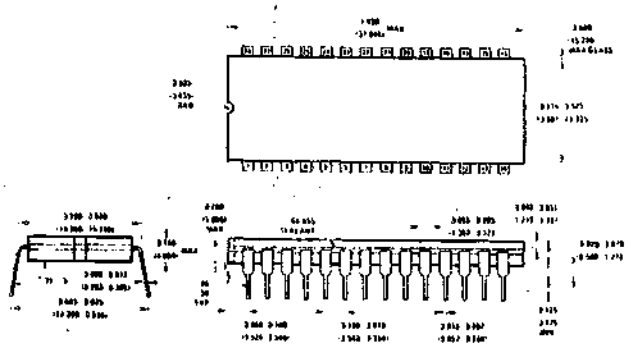
ASYNCHRONOUS MODE

Once transmission is initiated, the transmitter supplies the start bit, odd, even, or no parity bit, and the proper number of stop bits as specified by the program. If the next character is presented to the transmitter, it is sent immediately after transmission of the stop bit of the present character. Otherwise the Mark (logic high) condition is sent. The transmitter can be programmed to send a Space (logic low) condition instead of the Mark condition.

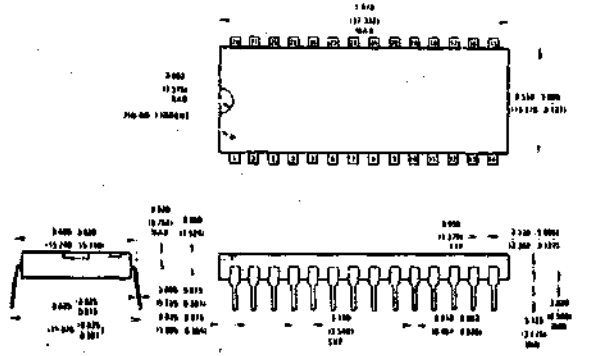
Once the receiver is enabled, reception of a character is initiated by recognition of the start bit. The Start/Stop and Parity bits are stripped off while assembling the serial input into a parallel character. If a break condition is detected then the receiver sends a character of all zero bits and a Framing Error status bit to the processor.

Succeeding all-zero or break characters are not assembled and presented to the system. The Receive Data (R_xD) input must return to a marking condition before character assembly is resumed. The overrun condition is checked in the same manner as in the Synchronous mode.

Physical Dimensions

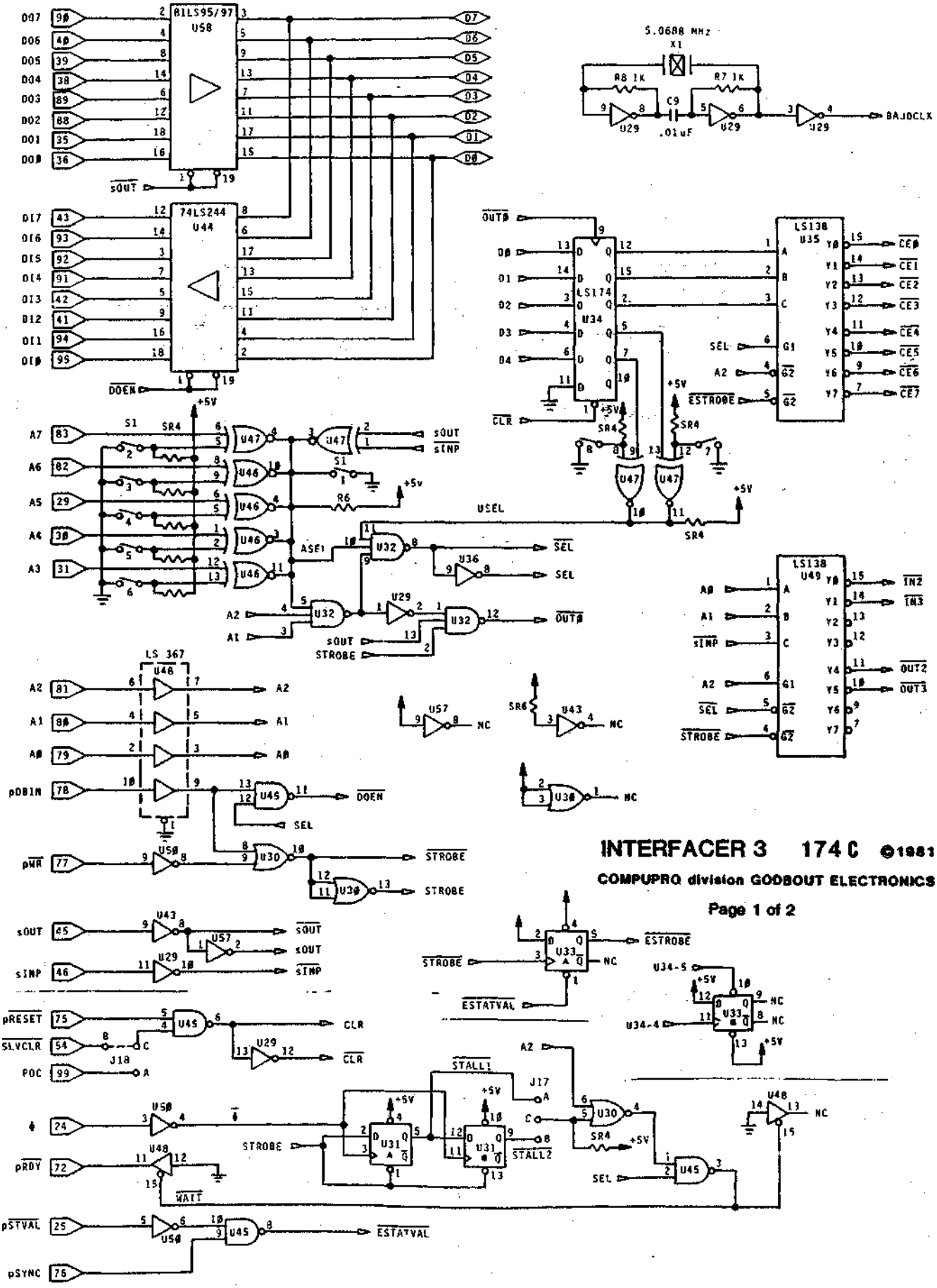


28-Lead Ceramic Dual-In-Line Package (Cer Dip (J))
Order Number INS2651J

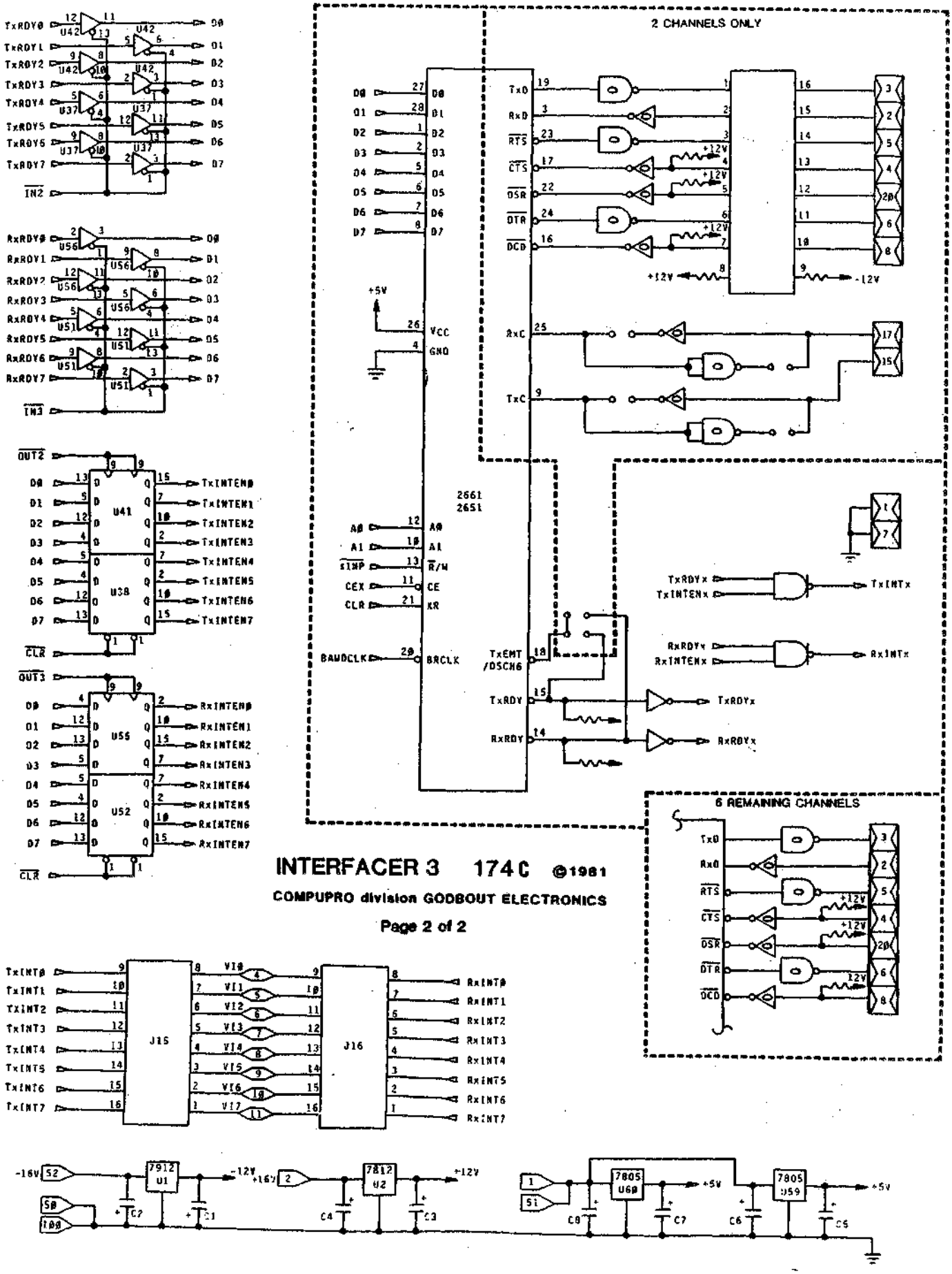


28-Lead Plastic Dual-In-Line Package (N)
Order Number INS2651N

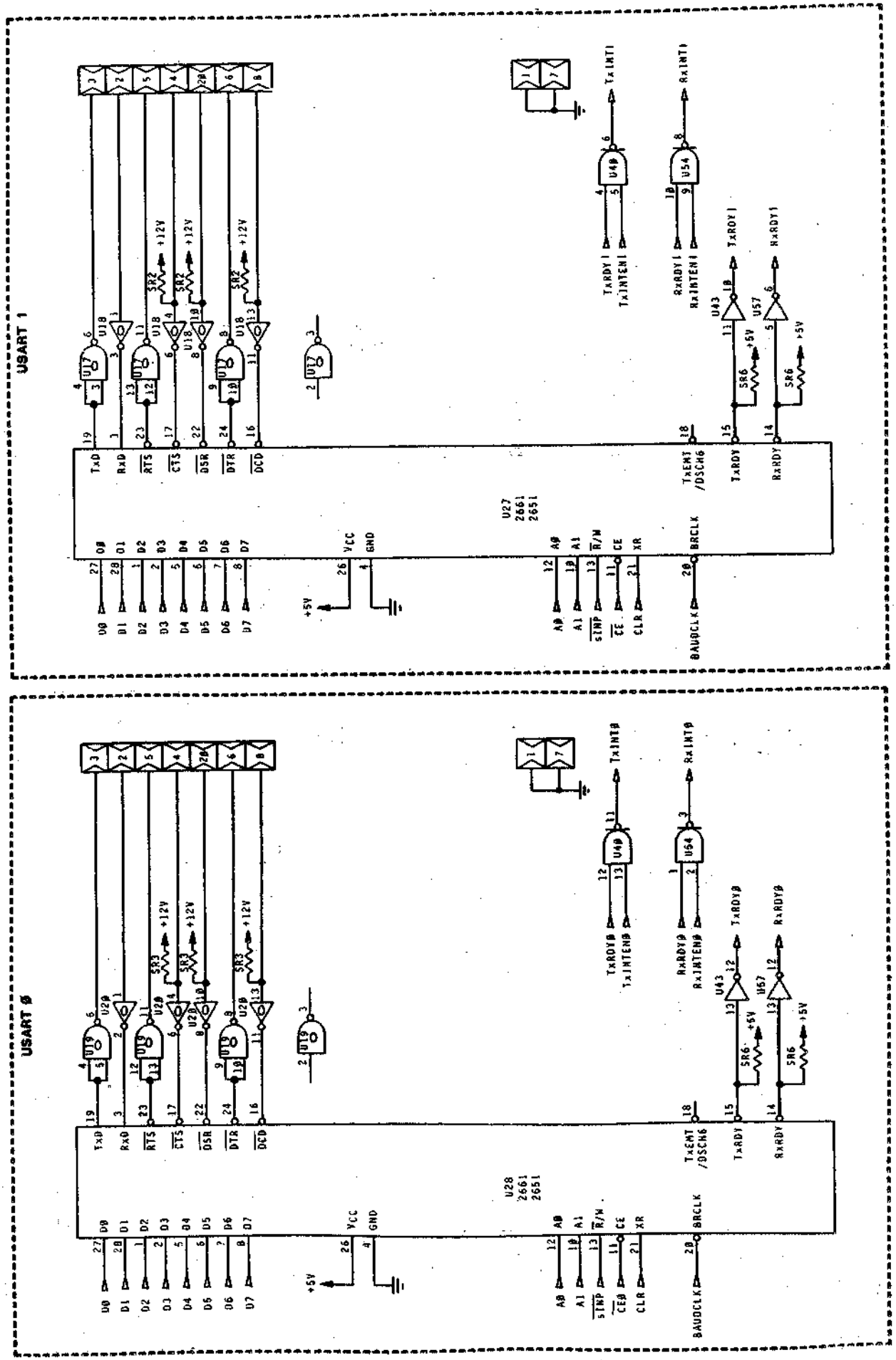
LOGIC DIAGRAM

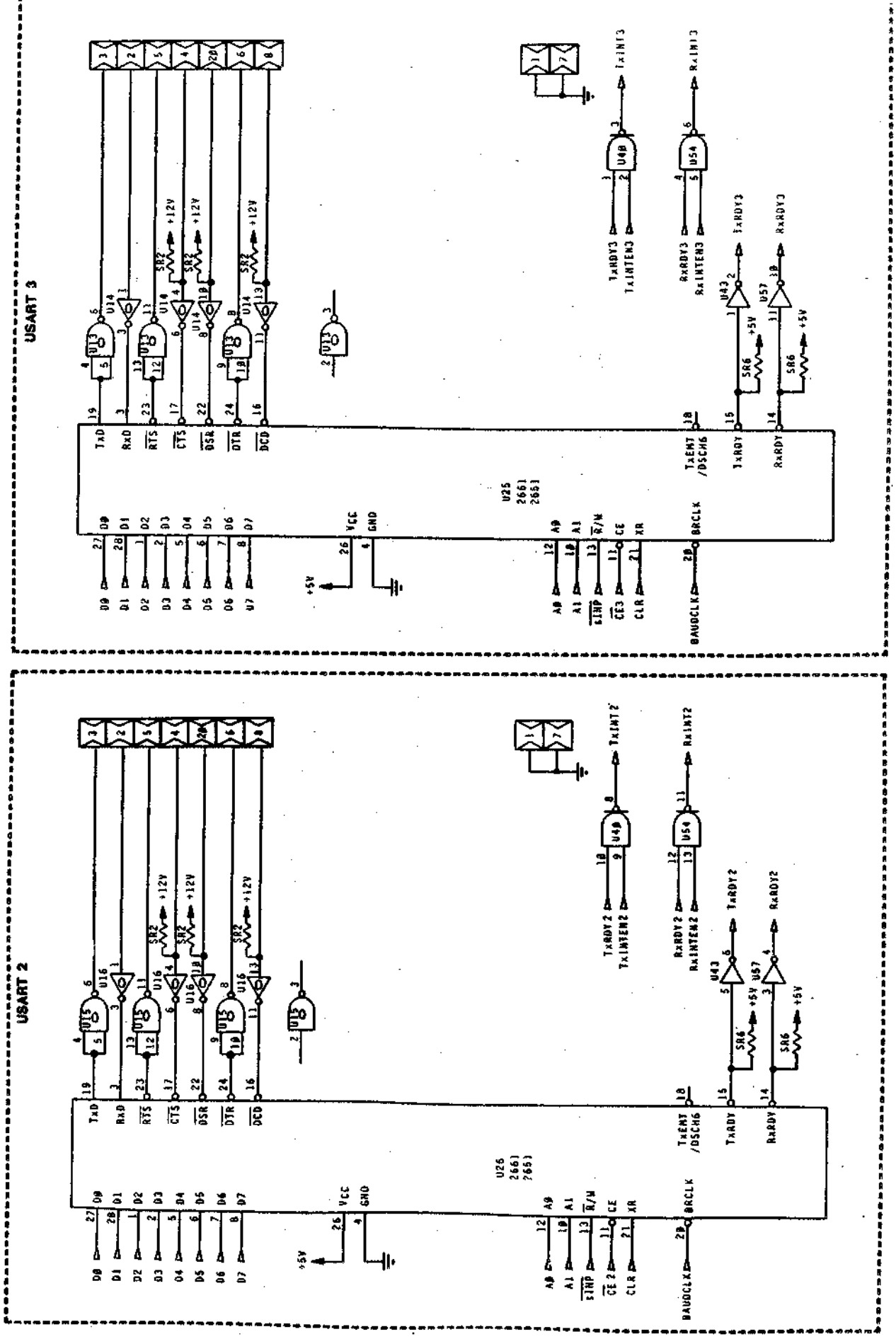


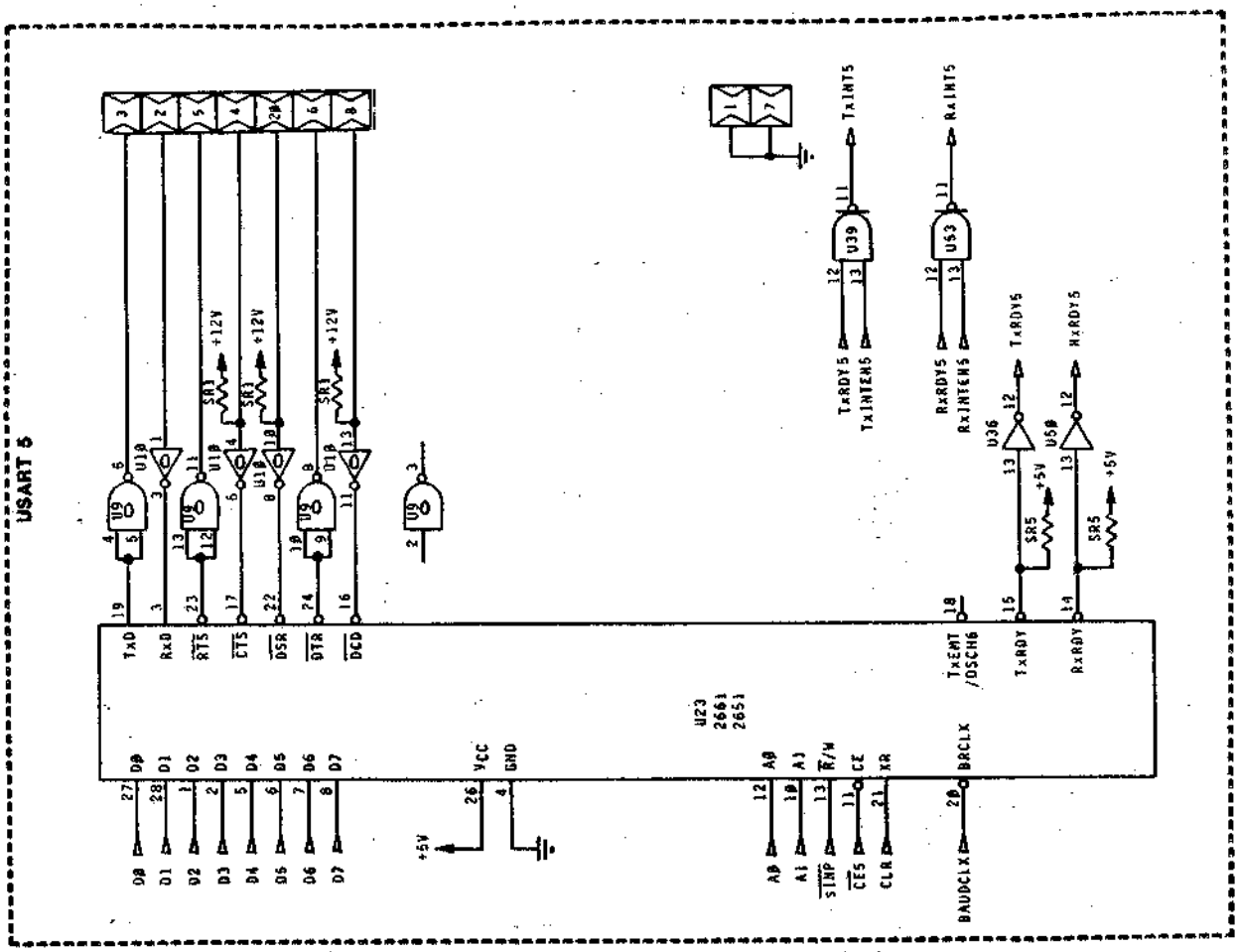
See pages 34 - 37 for pin numbers of each USART Channel

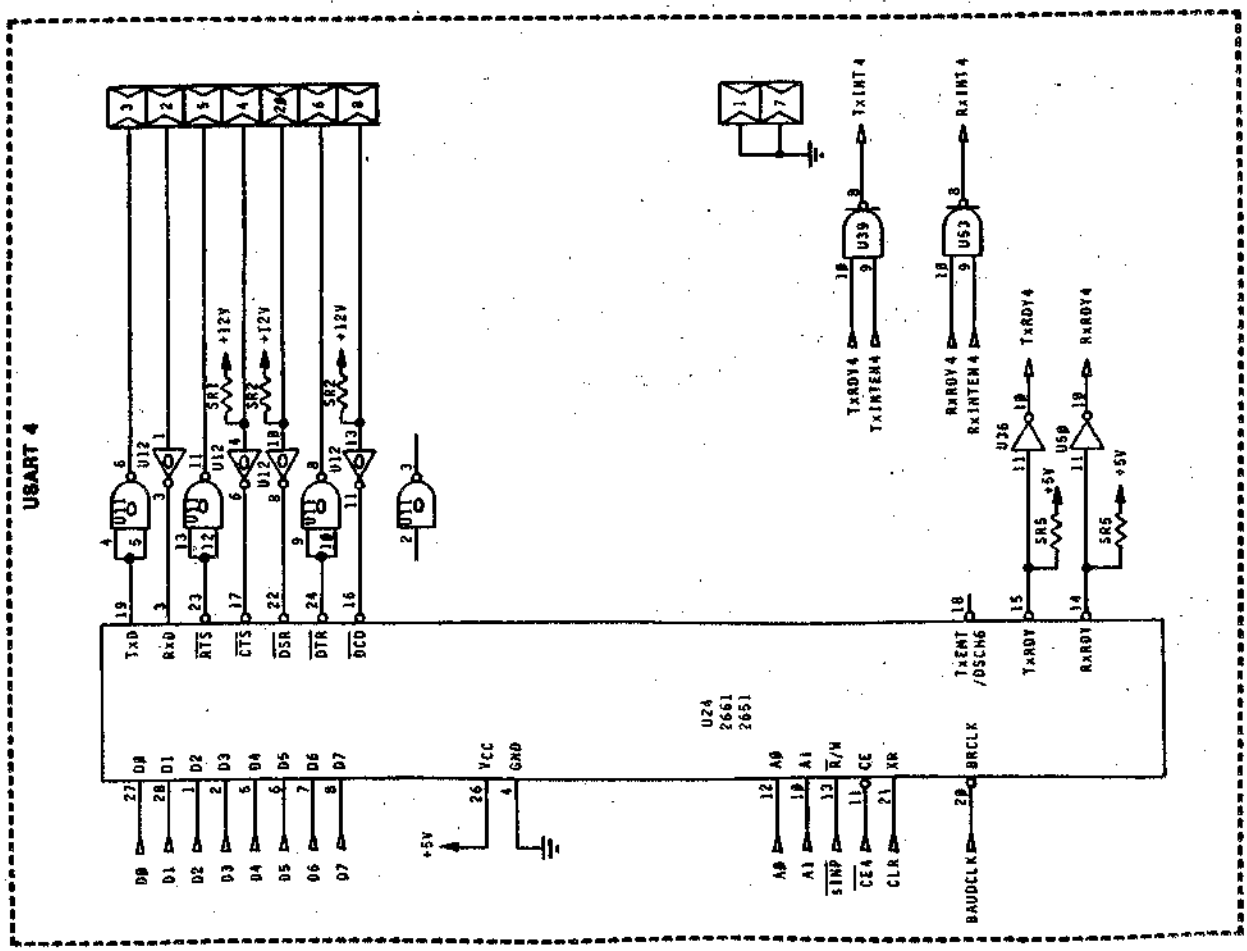


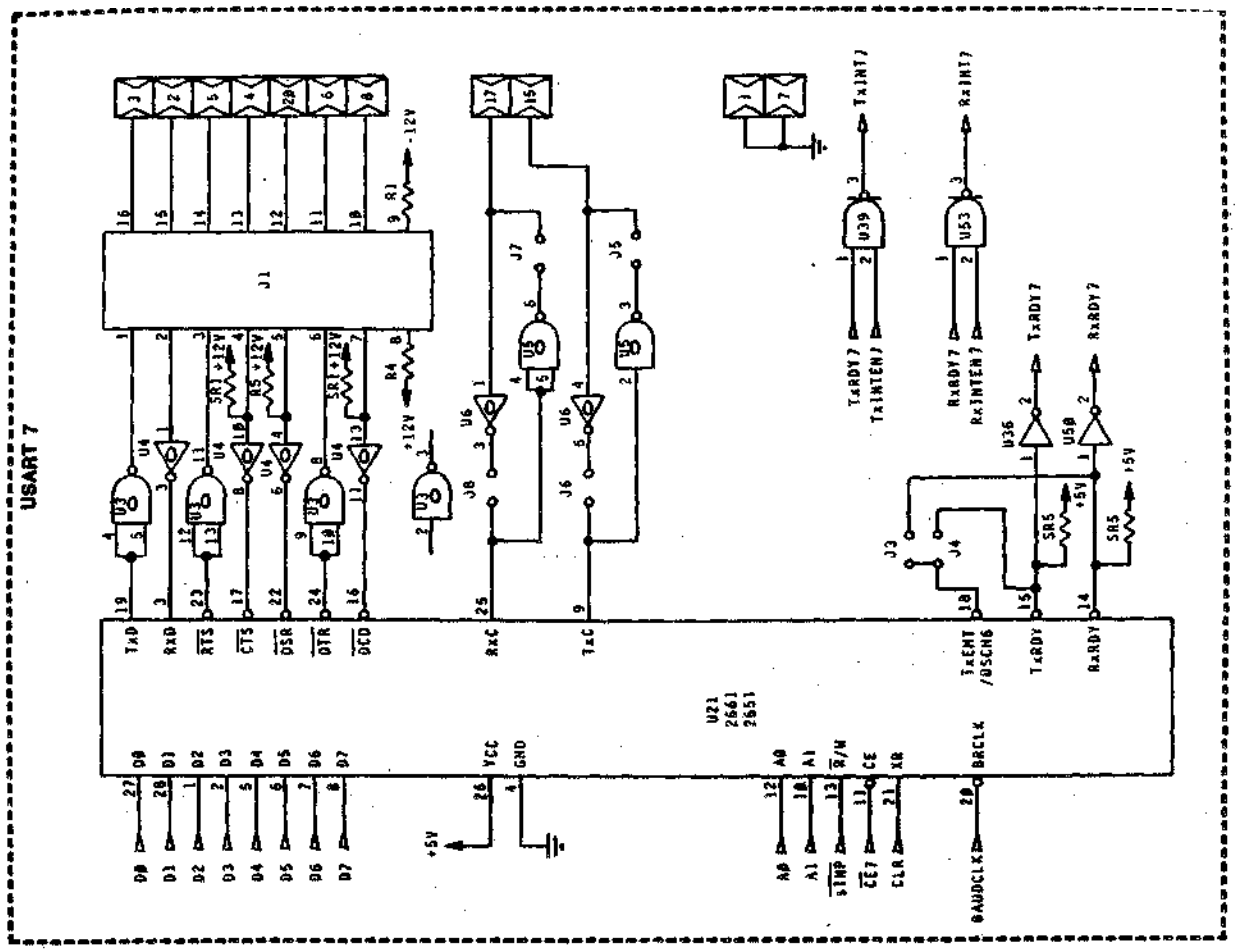
USARTs

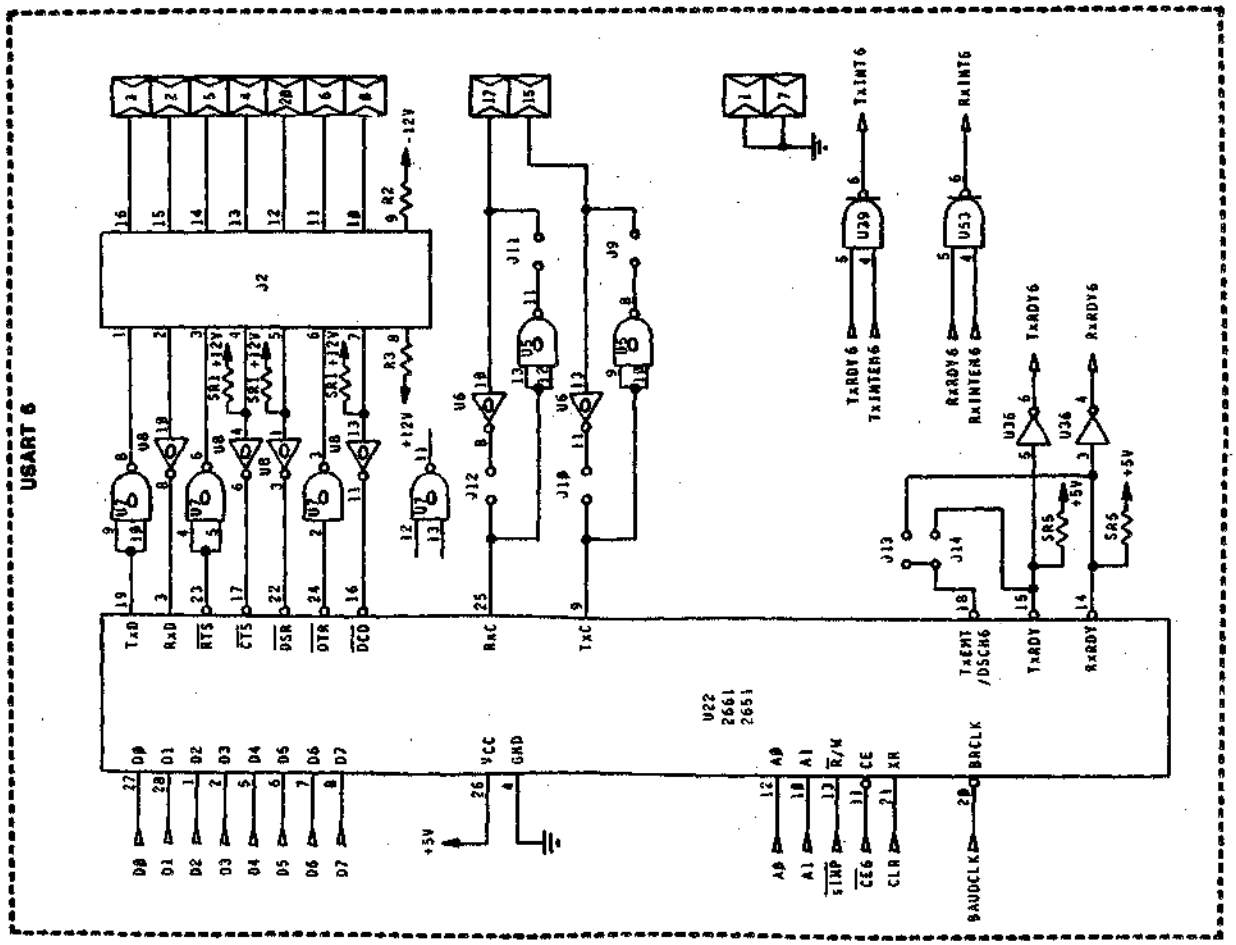

USART 1
USART Ø
U27
2661
2651
U28
2661
2651
TxD
RxD
RTS
CTS
DSR
DTR
DCD
D0
D1
D2
D3
D4
D5
D6
D7
VCC
GND
A0
A1
R/W
CE
XR
BRCLK
TxEMT
/DSCHG
TxRDY
RxRDY
SINP
CLR
BAUDCLK
+5V
+12V
TxINT1
RxINT1
TxINTØ
RxINTØ
TxRDY1
TxINTEN1
RxRDY1
RxINTEN1
TxRDYØ
TxINTENØ
RxRDYØ
RxINTENØ


USART 3
USART 2
TxD
RxD
RTS
CTS
DSR
DTR
DCD
D0
D1
D2
D3
D4
D5
D6
D7
VCC
GND
+5V
+12V
A0
A1
R/W
CE
CLR
BRCLK
BAUDCLK
TxRDY
RxRDY
TxRDY3
RxRDY3
TxINT3
RxINT3
TxRDY2
RxRDY2
TxINT2
RxINT2


USART 5
TxINT5
RxINT5
TxRDY5
TxINTEN5
RxRDY5
RxINTEN5
TxRDY
RxRDY
TxEMT /OSCH6
BRCLK
BAUDCLK
U23
2661
2651
+12V
+5V
GND
Vcc


USART 4
TxINT4
RxINT4
TxRDY4
TxINTEN4
RxRDY4
RxINTEN4
TxRDY
RxRDY
TxEMT /OSCH6
BRCLK
BAUDCLK
U24
2661
2651
+12V
+5V
GND
Vcc


USART 7
J1
U21
2661
2651
TxD
RxD
RTS
CTS
DSR
DTR
DCD
RxC
TxC
TxEMT
/DSCHG
TxRDY
RxRDY
VCC
GND
BRCLK
BAUDCLK
TxINT7
RxINT7
TxRDY7
RxRDY7
+5V
-12V


USART 6
J2
U22
2661
2651
TxD
RxD
RTS
CTS
DSR
DTR
DCD
RxC
TxC
TxEMT
/DSCHG
TxRDY
RxRDY
VCC
GND
BRCLK
BAUDCLK
TxINT6
RxINT6
TxRDY6
RxRDY6
+5V
-12V

PARTS LIST & COMPONENT LAYOUT SECTION

PARTS LIST

SEMICONDUCTORS	
U1	7912
U2	7812
U3	1488
U4	1489
U5	1488
U6	1489
U7	1488
U8	1489
U9	1488
U10	1489
U11	1488
U12	1489
U13	1488
U14	1489
U15	1488
U16	1489
U17	1488
U18	1489
U19	1488
U20	1489
U21-U28	2651/61
U29	74LS04
U30	74LS02
U31	74LS74
U32	74LS10
U33	74LS74
U34	74LS174
U35	74LS138
U36	74LS04
U37	74LS125
U38	74LS175
U39-40	74LS38
U41	74LS175
U42	74LS125
U43	74LS04
U44	74LS244
U45	74LS00
U46-U47	74LS266R

SEMICONDUCTORS	
U48	74LS367
U49	74LS138
U50	74LS04
U51	74LS125
U52	74LS175
U53-U54	74LS38
U55	74LS175
U56	74LS125
U57	74LS04
U58	81LS95/97
U59-60	7805

RESISTORS	VALUE
R1-R5	4.7K
R6	1.8K
R7-R8	1.2K
SR1-6	5.1K

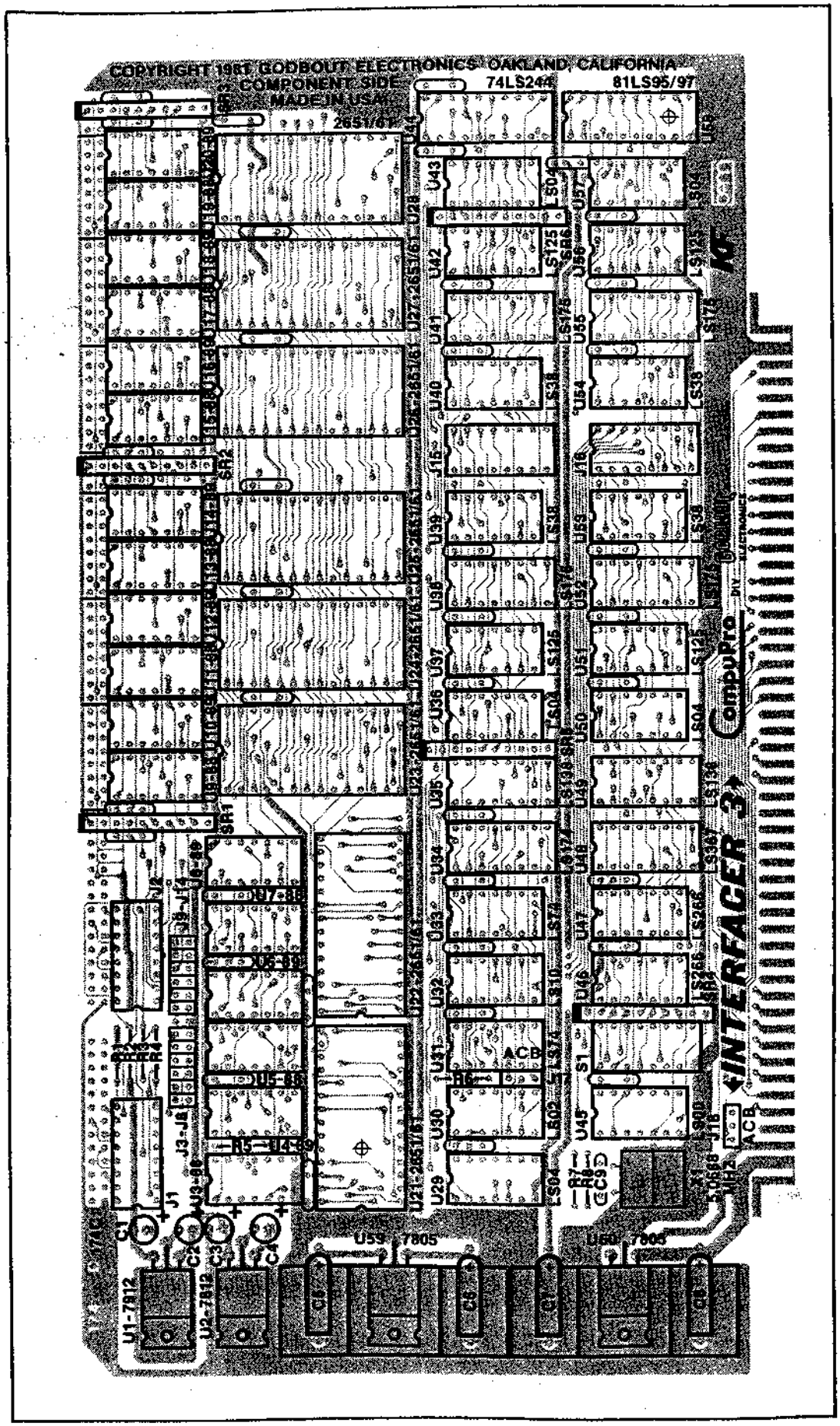
CAPACITORS	VALUE
C1-C4	2.7 uF
C5-C8	39 uF
C9	.01 uF
(39)	.01 uF

CRYSTAL	VALUE
X1	5.0688 MHz

SWITCHES	
S1	8-Position DIP

CONNECTORS	
JA,JB	26 Pin Transition
JC,JD	50 Pin Transition

JUMPERS	
J1-J2	16 Pin DIP Shunt
J3-J14	12 Pin Post Assembly
J5-J16	16 Pin DIP Header
J17	3 Pin Post Assembly
(10)	Post Shunt



COMPONENT LAYOUT

LIMITED WARRANTY

Viasyn Corporation warrants this computer product to be in good working order for a period of one (1) year, (two (2) years for CSC boards and six (6) months for drives) from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, VIASYN will, at its option, repair or replace the product at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of VIASYN. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse, or unauthorized modification of the product.

If you need assistance, or suspect an equipment failure, always contact your System Center or dealer first. System Center technicians are factory trained to provide prompt diagnosis and repair of equipment failures. If you are not satisfied by the actions taken by your System Center/dealer, please call VIASYN at (415) 786-0909 to obtain a **R**eturn **M**aterial **A**uthorization (**RMA**) number, or, write to VIASYN at 3481 Arden Road, Hayward, California 94545, Att.: RMA. Be sure to include a copy of the original bill of sale to establish purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location and to use the original shipping container or equivalent. Contact your System Center/dealer or write to VIASYN at the above address for further information.

ALL EXPRESSED AND IMPLIED WARRANTIES FOR THIS PRODUCT, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO THE ABOVE LISTED PERIODS FROM THE DATE OF PURCHASE, AND NO WARRANTIES, WHETHER EXPRESSED OR IMPLIED, WILL APPLY AFTER THIS PERIOD.

IF THIS PRODUCT IS NOT IN GOOD WORKING ORDER AS WARRANTED ABOVE, YOUR SOLE REMEDY SHALL BE REPAIR OR REPLACEMENT AS PROVIDED ABOVE. IN NO EVENT WILL VIASYN BE LIABLE TO YOU FOR ANY DAMAGES, INCLUDING ANY LOST PROFITS, LOST SAVINGS OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OF OR INABILITY TO USE SUCH PRODUCT, EVEN IF VIASYN OR A SYSTEM CENTER/DEALER HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY OTHER PARTY.

IF THIS PRODUCT IS OUT OF WARRANTY, PLEASE CALL THE VIASYN RMA DEPARTMENT TO OBTAIN THE FLAT RATE LABOR QUOTATION FOR FACTORY SERVICE.

Viasyn Corporation
26538 Danti Court
Hayward, California 94545
Telephone (415) 786-0909
TWX 510-100-3288

Note: This warranty supersedes all previous warranties, and all other warranties are now obsolete.