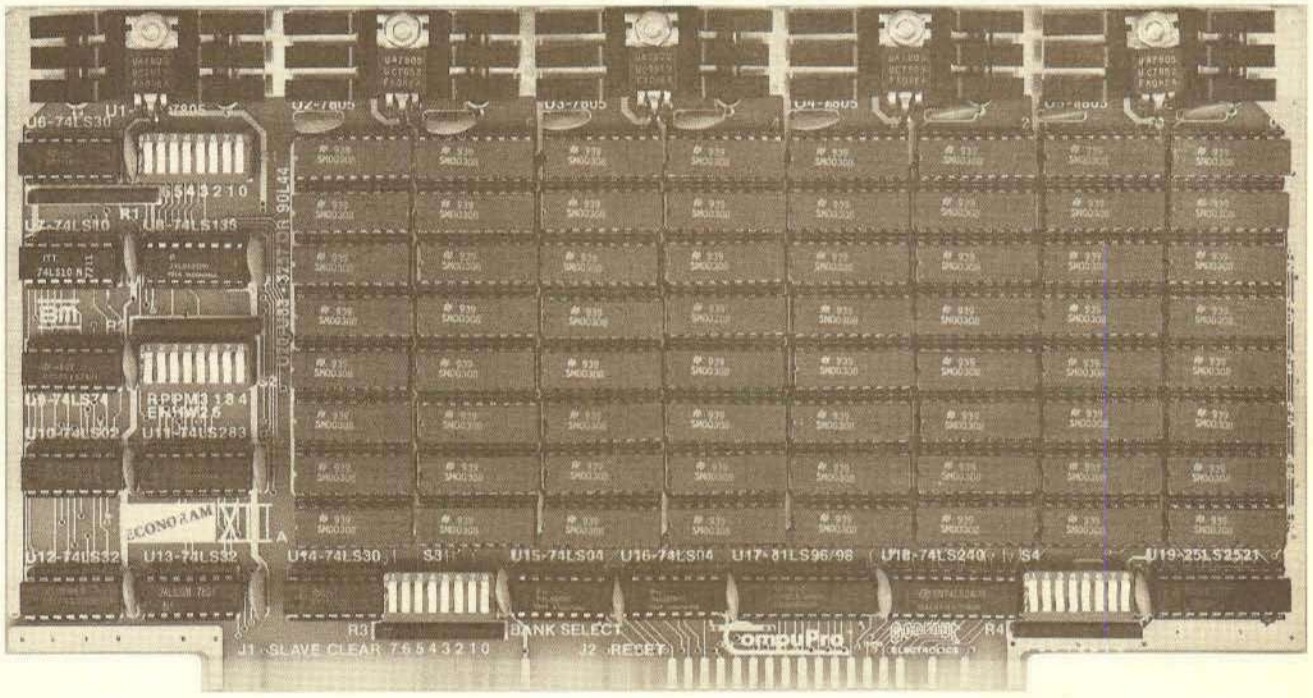
ECONORAM XIIIa™
USER'S MANUAL



IEEE • S-100
32K Bank Select Memory
using MM5257/90L44 • 5 MHz

147 mac

CompuPro™ from GODBOUT

2/80

Table of contents

ABOUT ECONORAM XIIIa

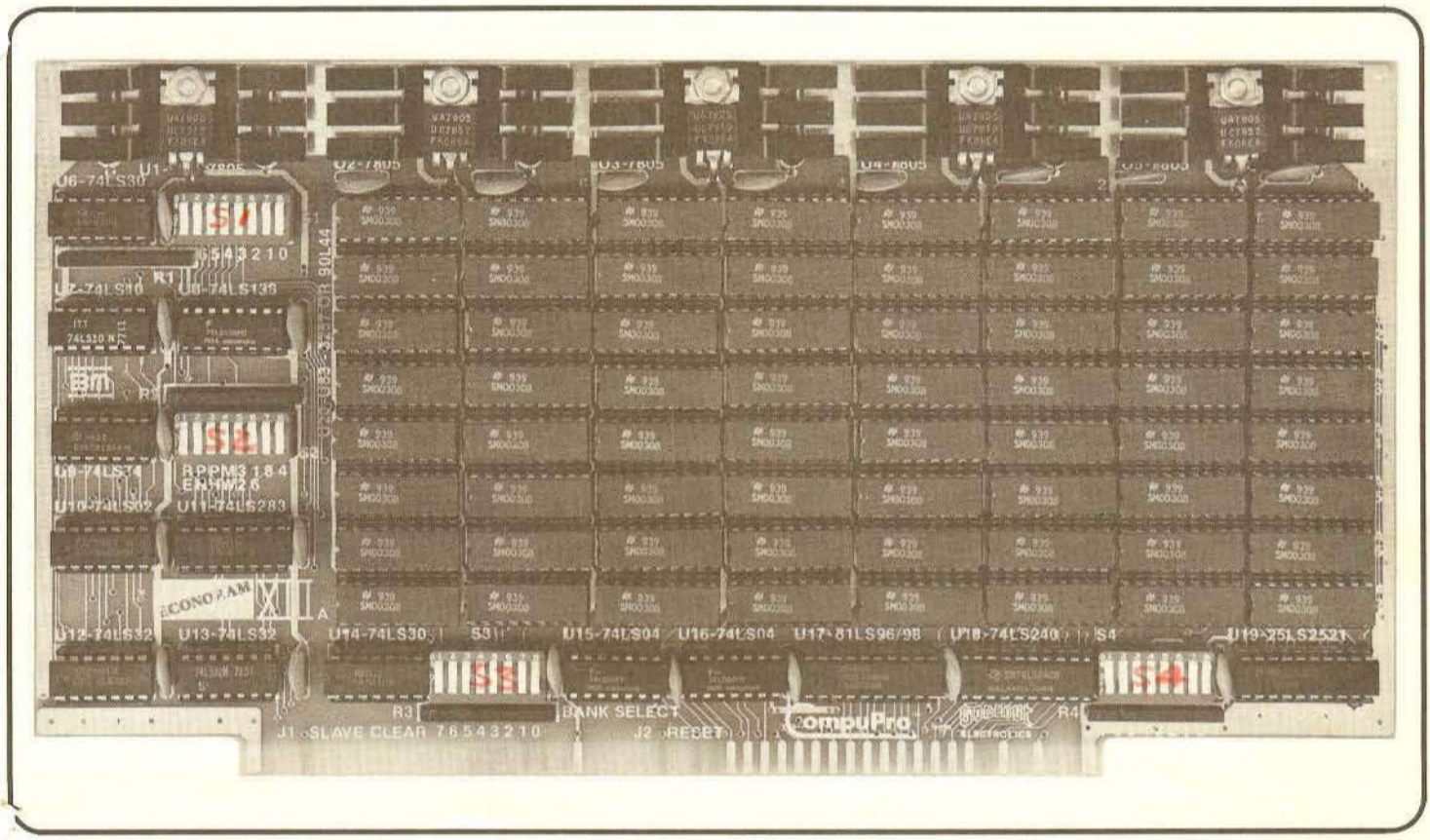
Congratulations on your decision to purchase **ECONORAM XIIIa**, a 32K x 8 memory board designed specifically for electrical and mechanical compatibility with the IEEE S-100 buss standard. The S-100 buss is the professional level choice for commercial, industrial, and scientific applications. This buss provides for ready expansion and modification as the state of the computing art improves. We believe this board, along with the rest of the S-100 portion of the **CompuPro** family, is one of the best memory boards available for that buss.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developments. In recognition of this fact, we also make this board available in "UNKIT" form for those who enjoy the challenge of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing the **CompuPro ECONORAM XIIIa**...welcome to the club!

TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered...there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement. The individual memory ICs used on this board are grouped together to form a single 32K X 8 block of memory, addressable on any 4K boundary using the on-board Dip switch (no jumpers required). Additional features include a write protect switch; a write strobe selection switch which allows use of this memory in systems with or without a front panel (MWRITE strobe); allowance for use of the PHANTOM* line; thorough capacitor bypassing of supply lines to suppress transients; plus on-board regulation and heatsinking for reliably cool operation. All this and sockets for all ICs go onto a double sided, solder-masked printed circuit board with a complete component-layout legend.



BANK SWITCHING THEORY

The purpose behind Bank Switching is to allow the Microcomputer user to access and write to more than the typical 64K that most Micros can directly address. To allow this, the **ECONORAM XIIIa** allows chunks of memory to be selectively enabled and disabled by outputting a data bit (user selectable) to a I/O Port (also user selectable). For example, if the bank is specified as port 40H, and the data bit is bit 0, by outputting a one in data bit 0 to port 40H, the bank will be enabled. Alternately, by outputting a zero to data bit 0 the bank will be disabled, and the board will not be electrically part of your system.
NOTE: Care should be taken to first disable an enabled bank before enabling the disabled bank to insure that no memory conflicts occur.

BANK PORT ADDRESSING

S4 1 2 3 4 5 6 7 8 Bank Selection

A7 A6 A5 A4 A3 A2 A1 A0 ON=1 OFF=0

EXAMPLE:

POSITIONS 1-8 ON = PORT FFH

POSITIONS 1-8 OFF = PORT 00H

POSITIONS 1-4 ON \
POSITIONS 5-8 OFF/ = PORT F0H

BANK ENABLE/DISABLE BIT ASSIGNMENT

Once the Bank Port has been selected, one data bit (or more) must be selected to enable or disable the bank. S3 is used to select these data bits as shown below:

1 2 3 4 5 6 7 8 ON= "1"

S3

D7 D6 D5 D4 D3 D2 D1 D0 OFF= "0"

To disable the bank all 0's must be output to the data bits which have been turned ON. To enable the bank again, a "1" must be output to any of the data bits that have been turned ON. Note that it requires all 0's to be sent to the selected data bits to disable, but only one "1" bit will enable the bank again.

POWER-ON ENABLE/DISABLE

When initial power is applied, and upon receiving a slave reset this board will be either ENABLED or DISABLED depending on the switch setting of S2 positions 1 & 2. To have the board enabled on power-on turn position 2 (PR) ON, and position 1 OFF. To disable board on power-on turn position 2 OFF and position 1 (RE) ON. Do not have both switches ON because the board will come up randomly enabled or disabled.

MEMORY ADDRESS ASSIGNMENT

This board is one large 32K block addressable on any 4K boundary. The dipswitch S2, positions 5-8 are used for selecting the starting address of the block. The starting address is set by "adding" the values shown below the switch when the position is ON. EXAMPLE: To start at 20K, turn ON positions 6 and 8 (16+4). To start at 52K, turn ON positions 5, 6, and 8 (32+16+4). With all switches (5-8) OFF the block will start at 0H.

DISABLING 4K BLOCKS

Because this board is sold partially populated also, the memory rows can be disabled. S1 is used to delete 4K Blocks from the memory space. This is particularly useful for disk operations which may require ROM at E900 or E000. By turning on the appropriate position on S1 the 4K Block associated with that position is removed from the system.

S1 POSITION 1 2 3 4 5 6 7 8 ON = DISABLED

BLOCK 7 6 5 4 3 2 1 0 OFF = ENABLED

The legend on the right side of the board (A0-A7) corresponds with the positions shown above. FOR EXAMPLE: To populate the board to only 16K, put the RAM chips in rows A0-A3 and turn on positons 5-8 of S1. This will disable rows A4-A7. S2 is still used to select the starting address of the block. Problem: To populate the board with 28K in the upper half of the memory map and leave a hole at E000 (for disk ROM). Set the address switches to start at 8000 (S2-7 ON, 5, 6, & 8 OFF), turn S1-2 ON to disable row A6, and put the RAM chips in all rows but A6. You can leave RAM chips in a disabled row with no problems if you choose to.

REFERENCE TABLE

SWITCH S1	1	2	3	4	5	6	7	8	ON=DISABLED
BLOCK	(7)	6	5	4	3	2	1	0	OFF=ENABLED

-S1 is used to selectively blank out individual 4K blocks within the main 32K block.

SWITCH S2	1	2	3	4	5	6	7	8	ON=ENABLED
LABEL	P R	R E	P H	M W	3 2	1 6	8	4	OFF=DISABL

-PR enabled causes the board to be enabled on power up or reset.
-RE enabled causes the board to be disabled on power up or reset.
-PH enabled puts the board under the control of the phantom line 67.
-MW enabled grounds the MWRITE line and causes the board to respond to PWR*.
-32, the decimal number that, when enabled, must be summed together to obtain the starting address for the board.
-16 See "32".
-8 See "32".
-4 See "32".

SWITCH S3	1	2	3	4	5	6	7	8	ON=RESPOND
LABEL	7	6	5	4	3	2	1	0	OFF=NORESP

-Positions 1 through 8 correspond to data bits 7 through 0 respectively. S3 is used to select which bit(s) the bank select responds to.

SWITCH S4	1	2	3	4	5	6	7	8	ON = "1"
LABEL	7	6	5	4	3	2	1	0	OFF = "0"

- Positions 1 through 8 correspond to address lines 7 through 0 respectively. S4 selects bank select port address and should reflect the binary equivalent of the desired address.

PHANTOM LINE

Switch S2-3 allows the **ECONORAM XIIIa** to be removed from memory space by a low level on PHANTOM* (Bus Pin 67). With S2-3 ON, memory will disappear when PHANTOM* is asserted. With S2-3 OFF, the board is unaffected by PHANTOM*. NOTE: Since some manufacturers are not conforming to the proposed IEEE S-100 buss standard, insure that your system is using the PHANTOM* line properly before using this feature on your **ECONORAM XIIa**.

MEMORY TESTING

If the memory board seems to be working properly, the MEMORY TESTING ROUTINE can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 32K from 4000 hex to BFFF hex. This may be changed by entering a different starting address at "STRT" (3001-3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical informaton is stored and the routine enters a software "HALT" that is a "jump to here" at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure information:

3069*	"FDE"	= D,E pair...D is the fill character, and E is the test character
306B*	"FHL"	= H,L pair...the failure address
306D*	"FOUT"	= the data expected
306E*	"FIN"	= the data read

* address from MEMORY TESTING ROUTINE

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference betwen "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

MEMORY TESTING ROUTINE

```
3000 21 00 A0          0010 STRT LXI  H,A0C0H
3003 3E A0             0020 END  MVI  A,0A0H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP  DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP  SHLT
3080                   0680 *
```

CIRCUIT DESCRIPTION

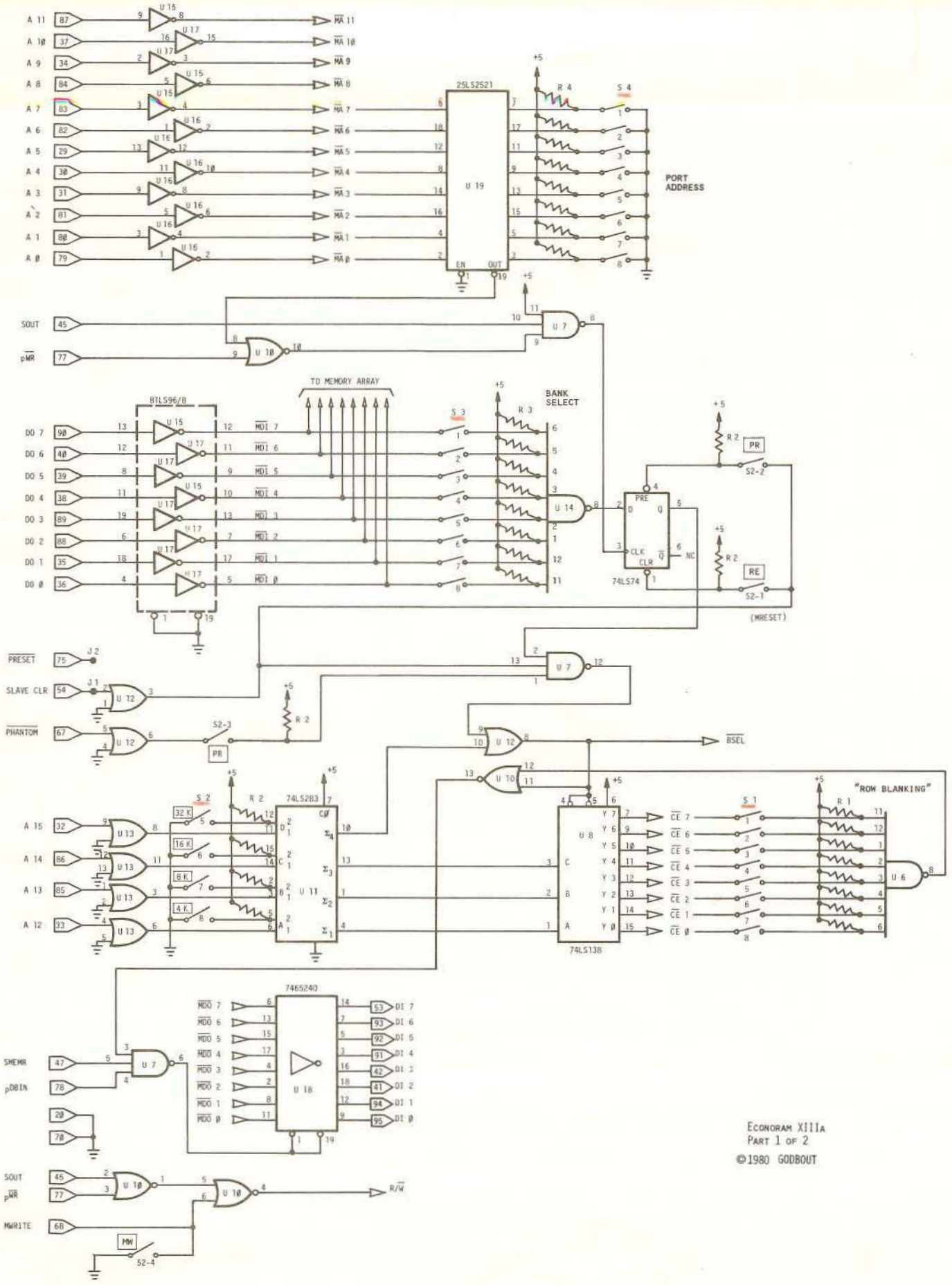
The heart of **ECONORAM XIIIa** is the MM5257/90L44 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts. These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 8 of these rows together produces a total memory storage of 32K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array). Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to write data into the memory, or read data from the memory. The schematics show the address circuitry along with the other **ECONORAM XIIIa** circuitry. Each memory IC requires 12 address lines (A0-A11) to access any one of the 4096 bits available in the IC. These address lines are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address lines (A12-A15) which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array). When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read on to the data buss from memory passes through 8 TRI-STATE inverting buss drivers; when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state. This board can be used in a system with more than 64K of memory, and because of this there must be a method to disable the entire board and remove it from the system memory map. Since the CPU can only access 64K of memory with its 16 address lines, the method chosen was to use an I/O port to ENABLE/DISABLE the board. Switch S4 is used to select the I/O port for the board and when the correct port is decoded by U19, U9 latches in the data bit(s), if any bit selected by switch S3 is high, the board will be enabled at the address selected by switch S2 positions 5-8. Conversely if all bits selected by S3 are low upon receiving the output instruction the board will be disabled. The board can be set up to be turned ON or OFF with Preset or Power-on by using switch S2 positions 1 and 2.

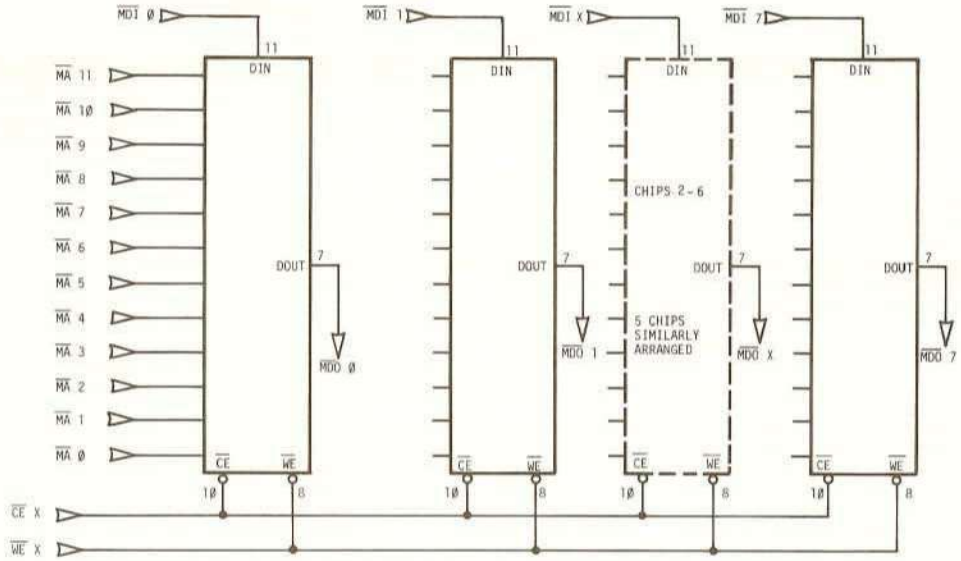
U8 is used to select the row of memory enabled during read/write. Switch S1 and NAND gate U6 are used with U8 to select 4K chunks of memory to be removed anywhere on the board. The appropriate position of S1 will disable the corresponding block if it is turned on.

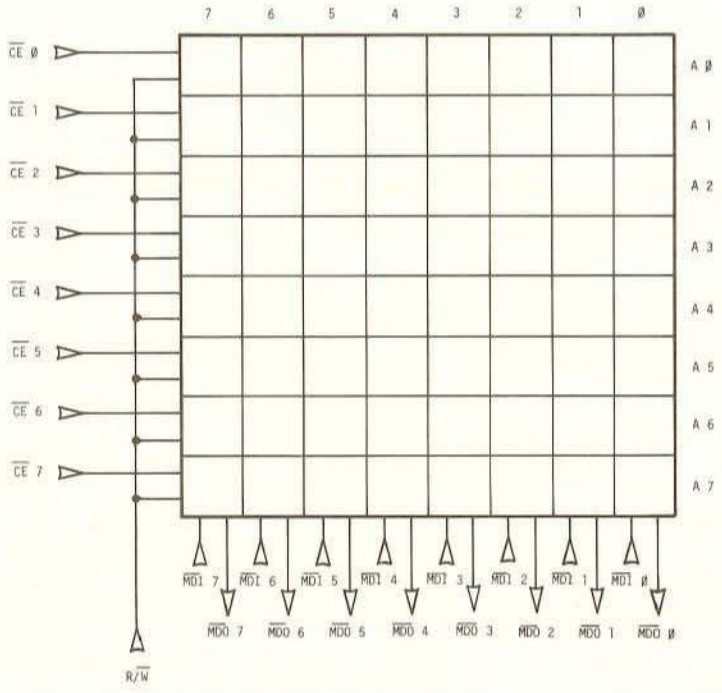
An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4 MHz, or 5 MHz with an 8085 CPU over the full temperature range (0-70 C ambient) and draw less than 3.5 Amps. Also, our typical measured currents were less than 3.0 Amps, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

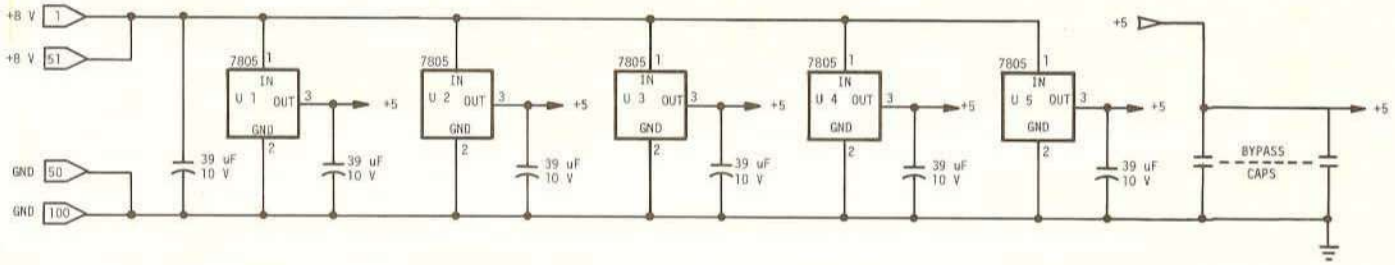
It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.


25LS2521
U 19
PORT ADDRESS
TO MEMORY ARRAY
81LS96/8
BANK SELECT
74LS74
(MRESET)
74LS283
74LS138
"ROW BLANKING"
7465240
U 18
SMEMR
pDBIN
MWRITE
R/W
BSEL
PRESET
SLAVE CLR
PHANTOM
SOUT
pWR
Econoram XIIIa
Part 1 of 2
©1980 GODBOUT





ECONORAM XIIIA
PART 2 OF 2
© 1980 GODBOUT



Parts List

☐ (1) ECONORAM XIIIa circuit board

INTEGRATED CIRCUITS (note: the following parts may have letters suffixes and prefixes along with the key numbers given below.)

☑ (64)	MM5257N-3L	4Kx1 static RAM	
☑ (1)	74LS02	quad 2 input NOR	(U10)
☑ (2)	74LS04	hex inverter	(U15, U16)
☑ (1)	74LS10	triple 3 input NAND	(U7)
☐ (2)	74LS30	8 input NAND	(U6, U14)
☐ (2)	74LS32	quad 2 input OR	(U12, U13)
☑ (1)	74LS74	dual "D" flip flop	(U9)
☐ (1)	74LS138	decoder	(U8)
☑ (1)	74LS240	octal buss driver	(U18)
☐ (1)	74LS283	4 bit adder	(U11)
☐ (1)	25LS2521	octal comparator	(U19)
☐ (1)	81LS96/98	octal buss driver	(U19)
☑ (5)	7805	5 volt regulator	(U1-U5)

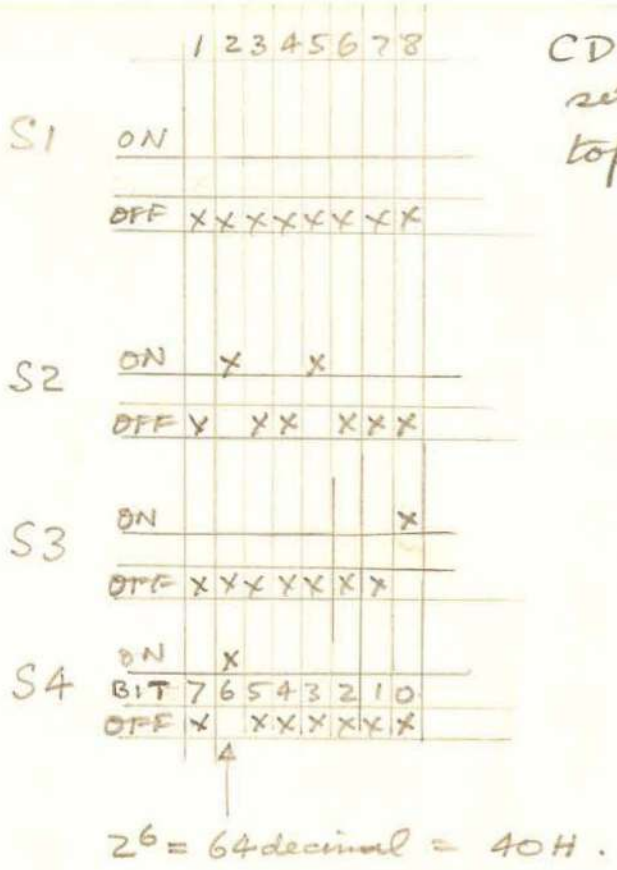
OTHER ELECTRONIC COMPONENTS

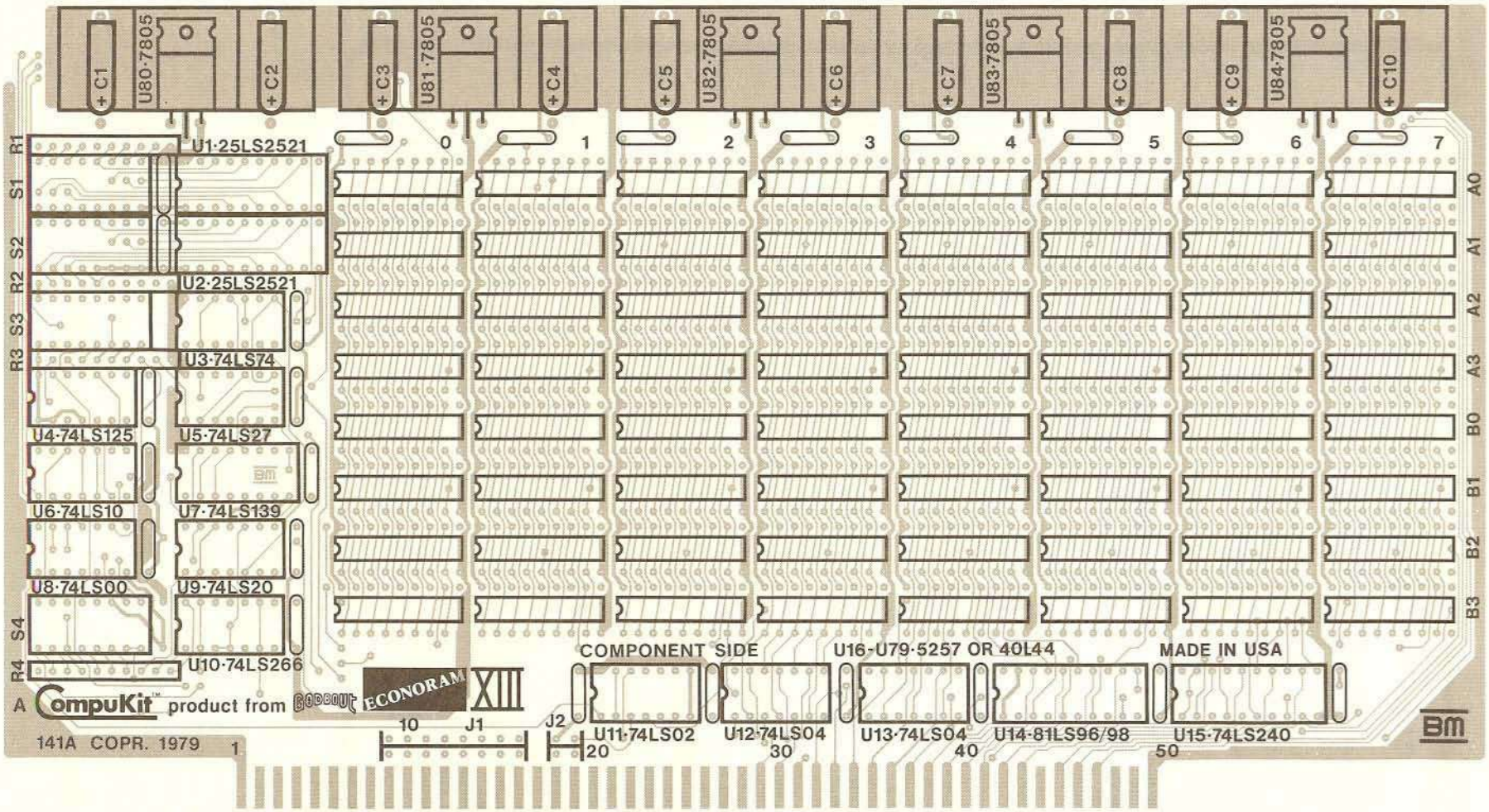
☐ (4)	SIP resistor packs	(R1-4)*
☐ (6)	39uf Tantalum Capacitors	(C1-C6)
☑ (20)	Ceramic bypass Capacitors *	21

MECHANICAL COMPONENTS

☑ (78)	Low Profile Sockets *	
☐ (4)	Dip Switch, 8 position	(S1-S4)*
☐ (5)	TO-220 Heat Sinks	
☑ (5)	Sets 6-32 Hardware	

* supplied already soldered on the board





Component Layout

UP

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuPro product. If this product fails to operate properly, it may be returned to us for service; see warranty information below.

If you need further information feel free to write us at:

P.O. Box 2355, Oakland Airport, CA 94614.

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone for taking orders, (415) 562-0636. If you have any problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). We cannot return calls or accept collect calls.

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $10.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

Prices and specifications are subject to change without notice, owing to the volatile nature and pricing structure of the electronics industry.