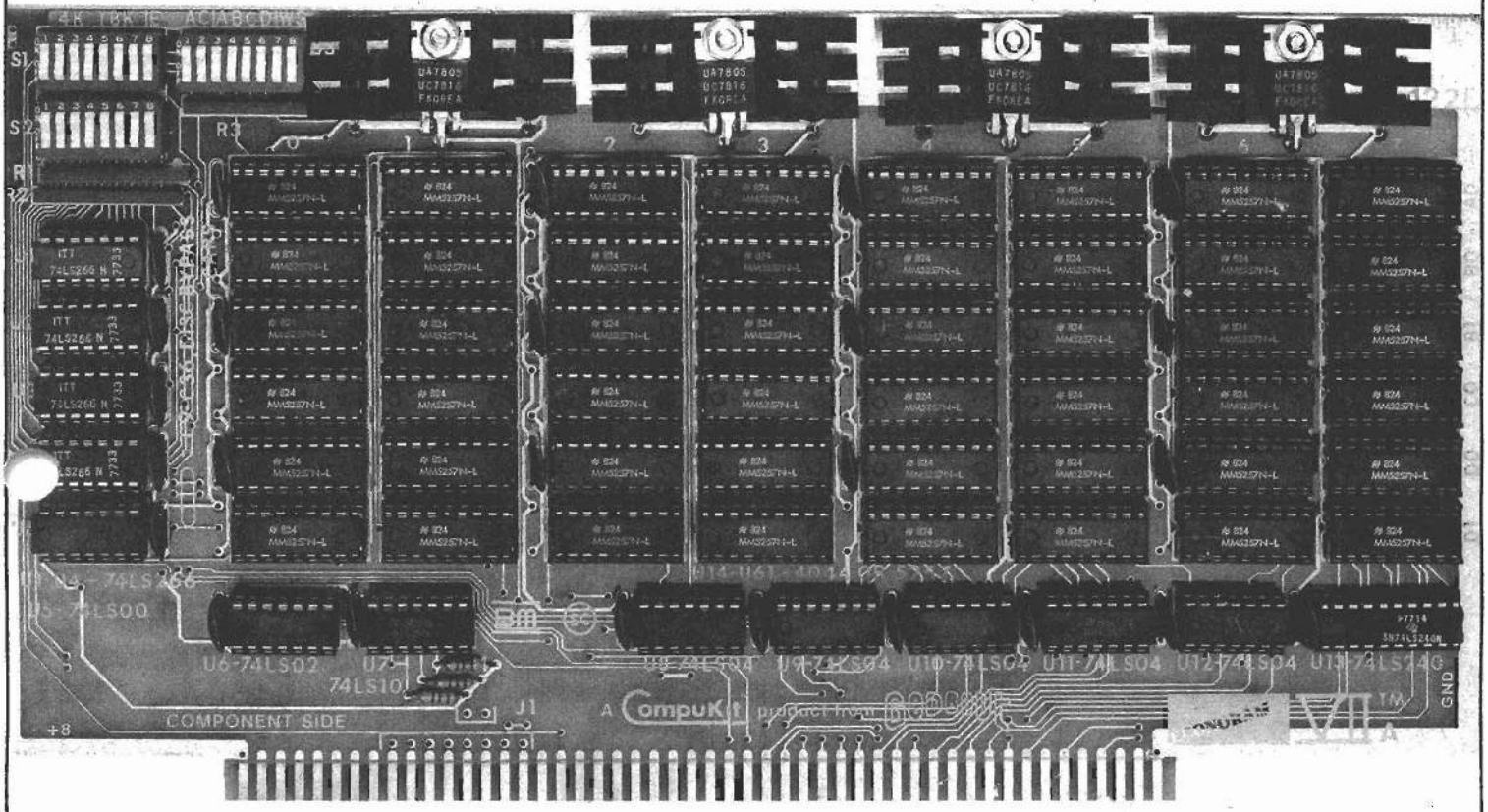
ECONORAM VII A T.M.
USER'S MANUAL



24K x 8 static memory · S-100
using MM5257/TMS40L44 · 4MHz

A CompuKit T.M. product from GODBOUT

Rev 3/79

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ABOUT ECONORAM VII

Congratulations on your decision to purchase ECONORAM VII, a 24K x 8 memory board designed specifically for electrical and mechanical compatibility with the S-100 buss standard. The S-100 buss currently is one of the most popular in the industry and by far the most prolific; we believe this board, with the rest of the S-100 portion of the ECONORAM family, is one of the best memory boards available for that buss.

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting. Completion of the assembly should take from one to four hours, depending on previous assembly experience, and upon completion, you will discover -- as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works, and works.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONORAM VII . . . welcome to the club.

TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered. There is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement.

The individual memory ICs used on this board are grouped together to form four larger blocks of memory, two 4K X 8 and two 8K X 8. The 4K blocks may be addressed on any 4K boundary, and the 8K blocks on any 8K boundary by setting the starting locations with the on-board dip switch (no jumpers required). Additional features include write protect switches for each of the four blocks; a write strobe selection switch which allows use of memory in systems with or without a front panel (MWRITE strobe); allowance for use with or without the PHANTOM line; thorough capacitor bypassing of supply lines to suppress transients plus on-board regulation and heat-sinking for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend.

Parts List

Upon receipt of your kit, check your parts against the list below.

- ☑ (1) Econoram VIIA circuit board

INTEGRATED CIRCUITS (note: the following parts may have letter suffixes and prefixes along with the key numbers given below.)

- ☐ (48) MM5257N-3L or TMS 40L44 (U14 - U61)
- ☑ (1) 74LS00 nand gate (U5)
- ☑ (1) 74LS10 3-input nand gate (U7)
- ☑ (1) 74LS02 nor gate (U6)
- ☑ (5) 74LS04 hex inverters (U8 - U12)
- ☑ (1) 74LS240 TRI-STATE® inverters (U13)
- ☑ (4) 74LS266 ex-nor o.c. (U1 - U4)
- ☑ (4) 7805 positive 5V regulators (U62 - U65)

OTHER ELECTRONIC COMPONENTS

- ☑ (3) S.I.P. resistor packs (R1 - R3)*
- ☑ (3) 4 K 2.7K 1/4 watt resistors (red-violet-red; R4 - R6)
- ☑ (8) 39uF tantalum capacitors (C1 - C8)
- ☑ (25) ceramic disk bypass capacitors*

MECHANICAL COMPONENTS

- ☑ (61) low profile sockets*
- ☑ (3) dipswitch (S1 - S3)*
- ☑ (4) TO-220 heat sinks
- ☑ (4) 6-32 bolts
- ☑ (4) 6-32 lockwashers
- ☑ (4) 6-32 hex nuts
- ☑ (1) instruction booklet

*supplied already soldered to board.

ASSEMBLY PROCEDURES

Proper operation of your kit depends on good soldering technique, along with correct identification and handling of the various parts used during construction. Read this manual *thoroughly* before plugging in your soldering iron.

SOLDERING TECHNIQUES. The Econoram Board is *solder-masked.* In case you are not familiar with solder-masked boards, they are similar to standard PC boards, but are screened with a solder-resistant coating. This mask is screened over the entire board, except where there are solder connections to be made; since solder does not comfortably hold to or flow over the resist, the chances of getting a bridge between tight, adjacent traces are decidedly minimized.

However, soldering a solder-masked board requires a bit of care. All soldering is performed on the *solder* side of the board; we recommend keeping all component leads straight up at all times, not bent over as with some other types of boards (see figure 1). When soldering, bring the iron tip in at an angle, against the board pad and component lead; then feed in a tiny bit of solder at opposite ends of the lead (see figure 2). This makes a good joint with no excess solder. *NOTE: Use of any type of solder other than rosin core solder invalidates the warranty. Do not use any type of solder paste or corrosive flux under any conditions.*

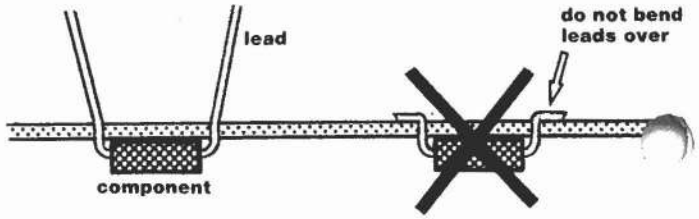


Figure 1.

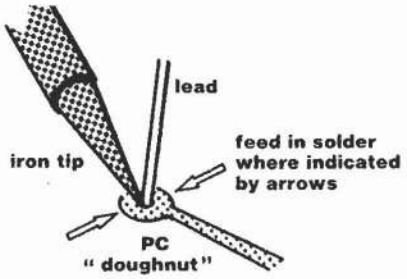


Figure 2.

IDENTIFICATION OF PARTS. There are many ICs used in this kit; each one must be oriented correctly for proper operation. Most ICs have a dot near one corner that indicates pin 1 (see figure 3); sometimes this dot appears in conjunction with a deeply cut notch or circle. Other types indicate the pin 1 end of the IC by a deep notch, or a notch within a shallow circle (see figure 4). In case of doubt, place the IC in front of you so that any identifying numbers read from left to right; pin 1 is almost always in the lower left-hand corner (figure 5).

Additionally, the 8 tantalum capacitors must be correctly identified as to the (+) and (-) ends. The (+) end is the rounded end and is also identified with a (+) mark on the body (see figure 6).

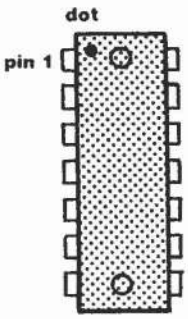


Figure 3.

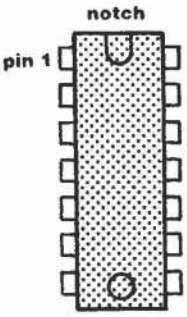


Figure 4.

Figure 5.

HANDLING OF PARTS. All integrated circuits may be damaged by static electricity discharges; however, MOS ICs - such as the memory ICs included with your kit - are most susceptible to this problem. You can easily accumulate a static charge on your body in the thousands-of-Volts range (say, by walking across a rug on a dry day). If you then touch the pins of an IC, those thousands of Volts flow into the IC and can damage the internal structure. To prevent this from happening, leave the ICs in their protective foil until needed; then, before plugging in each IC, touch the protective foil with your finger to drain off any residual charge. Also, avoid wearing clothing that is prone to generating static electricity during construction (such as sweaters, certain types of acrylic fabrics, and so on).

Another caution concerns the mounting of resistors. These are small, somewhat fragile parts, and excessive force used while bending the leads may cause damage or crack the part. Either use a commercial lead bender (available from Godbout's and many other electronic vendors), or use needlenose pliers to grasp the lead close to the body of the resistor and then bend the lead downward (see figure 7).

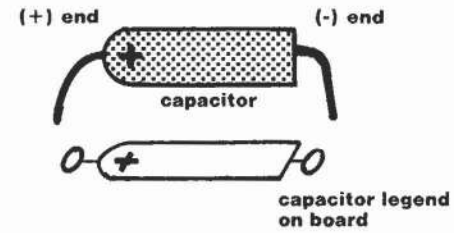


Figure 6.

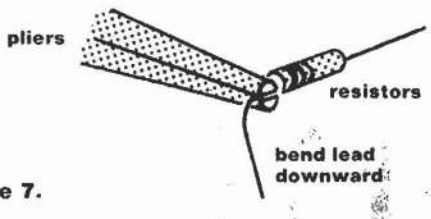
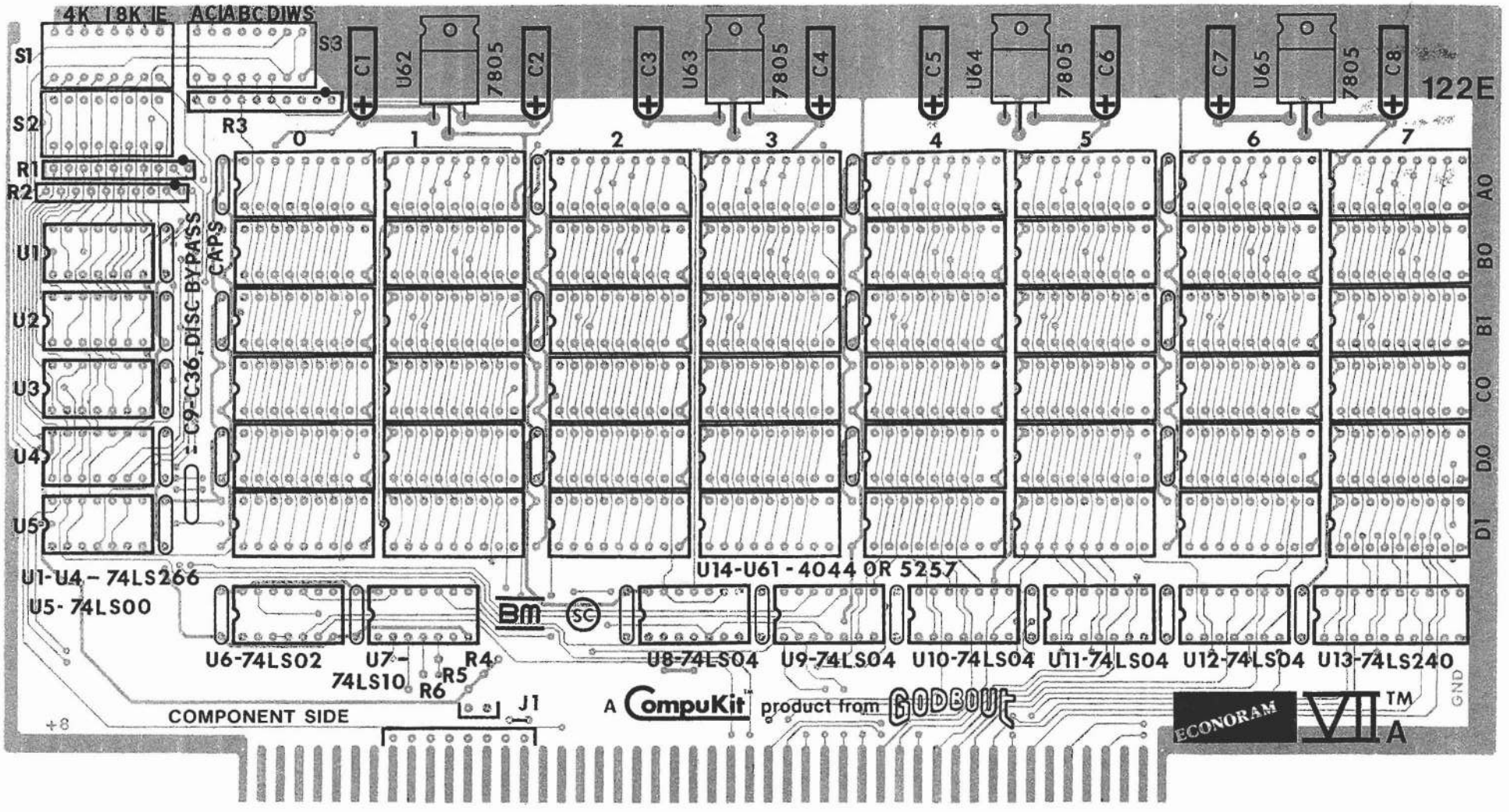


Figure 7.



Component Layout

UP

CONSTRUCTION

Keeping the preceding information in mind, it is now time to mount the various components and install the ICs into their sockets. Orient the board as shown in the component layout. Then, referring to this layout, follow the steps below in the order given.

☑ **1.** Bend leads, mount and solder the resistors in place as indicated.

☑ **2.** Bend leads, mount and solder the 8 tantalum capacitors in place as indicated, carefully observing the orientation of the (+) end.

☑ **3.** Mount the 4 regulators and the regulator heat sinks in place. Referring to Figure 8, observe that the heat sinks mount on top of the board, and then, the regulators mount on top of the heat sinks. If desired, a small dab of heat sink compound may be added between the regulator cases and heat sinks to improve thermal transfer from regulator to sink. Again referring to Figure 8, bend all regulator leads as shown, then bolt the heat sink regulator assemblies into place using the provided nut, bolt, and lockwasher hardware. After these assemblies are in place, solder the regulator leads on the solder side of the board.

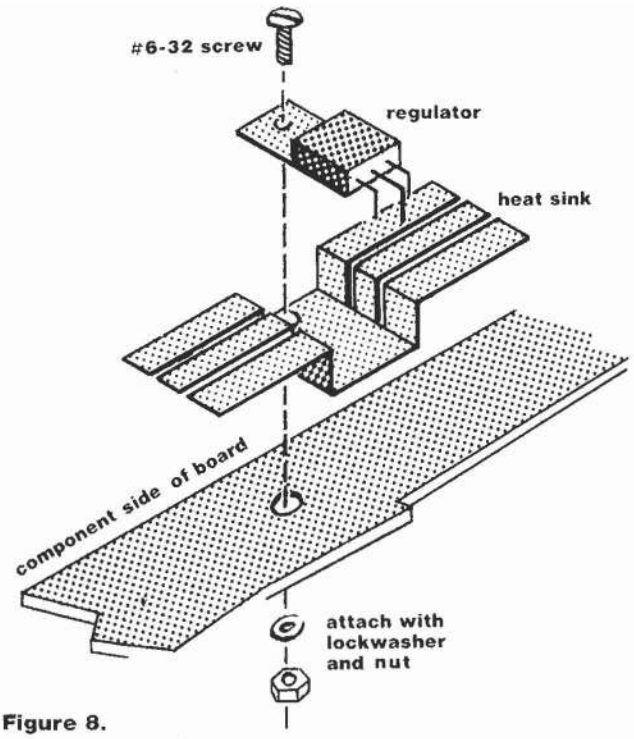


Figure 8.

☑ **4.** Observe the 8 pole dip switches. The side with the number 1-8 faces the upper edge of the board (see Figure 9). Mount the switch in place, then solder. *(Note: may be already soldered in place.)*

☑ **5.** Before proceeding, check your work so far by testing the board for any shorts between supply lines and ground. Referring to Figure 10, use a voltmeter to test for a shorted condition at the test points indicated on the regulator.

Perform this test at each regulator. If you find a short circuit at any of these points, carefully check over your board for the cause of the short. If all readings are satisfactory, proceed with construction of the board.

☐ **6.** Prepare to plug in all ICs in accordance with the component layout, Page 5. All ICs should have the pin 1 end facing towards the left side of the board. Any numbers or other markings on the IC should be right side up with the board oriented as shown in the component layout. If any of the writing is upside-down, the IC may not be correctly inserted.

A common problem with boards returned for repair is improper insertion of the IC. Sometimes a lead from the IC will bend *under* the part instead of going into the socket contacts. We recommend inserting each IC halfway, and verifying visually that all pins are indeed going into the socket. Then, push the IC in the rest of the way.

Keeping the preceding in mind, insert the support ICs first and then insert all memory ICs.

☐ **7.** Check your work over carefully for errors in construction, improperly inserted ICs, or improper polarity of the tantalum capacitors. If all is well, assembly of your board is now complete.

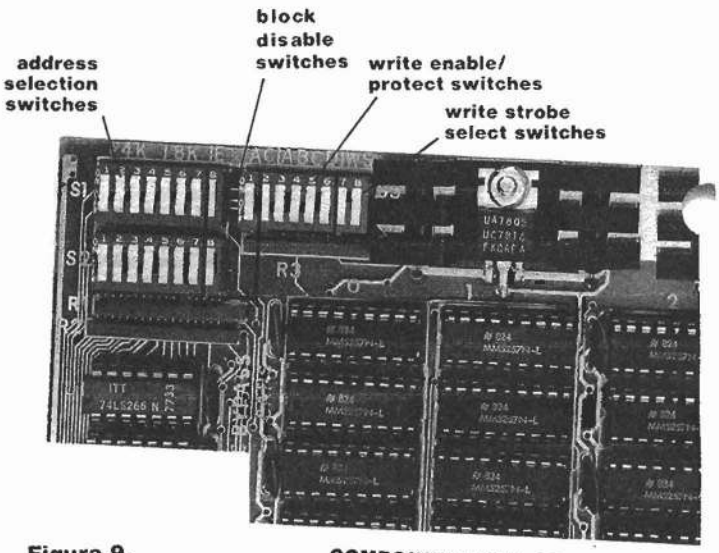


Figure 9. COMPONENT SIDE OF BOARD

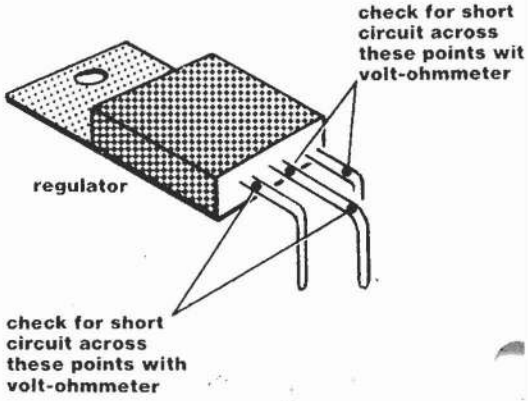


Figure 10.

MEMORY ADDRESS CONFIGURATION

This board is configured as two 4K blocks addressable on 4K boundaries and two 8K blocks independently addressable on 8K boundaries. Switches S1 and S2 each select one 4K and one 8K block. (switch S1 : block A - 4K and block B - 8K, switch S2 : block C - 4K and block D - 8K) as follows:

4K		8K	
SWITCH POSITION	STARTING ADDRESS	SWITCH POSITION	STARTING ADDRESS
1 2 3 4		5 6 7	
Ø Ø Ø Ø	ØØØØ	Ø Ø Ø	ØØØØ
Ø Ø Ø 1	1ØØØ	Ø Ø 1	2ØØØ
Ø Ø 1 Ø	2ØØØ	Ø 1 Ø	4ØØØ
Ø Ø 1 1	3ØØØ	Ø 1 1	6ØØØ
Ø 1 Ø Ø	4ØØØ	1 Ø Ø	8ØØØ
Ø 1 Ø 1	5ØØØ	1 Ø 1	AØØØ
Ø 1 1 Ø	6ØØØ	1 1 Ø	CØØØ
Ø 1 1 1	7ØØØ	1 1 1	EØØØ
1 Ø Ø Ø	8ØØØ		
1 Ø Ø 1	9ØØØ		
1 Ø 1 Ø	AØØØ		
1 Ø 1 1	BØØØ		
1 1 Ø Ø	CØØØ	Ø = OFF	
1 1 Ø 1	DØØØ		
1 1 1 Ø	EØØØ	1 = ON	
1 1 1 1	FØØØ		

In addition, position 8 on each switch enables (OFF) or disables (ON) the associated 8K block. Positions 1 and 2 of switch S3 disable/enable the 4K blocks A and C respectively.

MEMORY PROTECT SWITCHES

Switch S3 positions 3-6 are write enable switches. Conversely they may be used for manual write protection of the memory. Each position 3, 4, 5 and 6 is associated wih one memory block A, B, C and D respectively. Any combination of these four swtiches may be ON write enabling or OFF write protecting the particular block.

WRITE STROBE SELECT SWITCHES

Switch S3 positions 7 and 8 select write strobe. S3-8 ON causes $\overline{\text{PWR}}$ to qualify the memory for write commands. S3-7 ON causes MWRITE to qualify the memory for write commands. In normal operations with systems which have front panels ie., Altair, Imsai etc., or others which generate $\overline{\text{MWRITE}}$ with or without front panels use MWRITE. All others use $\overline{\text{PWR}}$. Positions 7 and 8 both ON at the same time will ground MWRITE on the buss. This condition must be avoided if MWRITE is present.

MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine (page 11) can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 24K from 4000 hex up to AØØØ hex. This may be changed by entering a different starting address at "STRT" (3001 - 3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical information is stored and the routine enters a software "HALT", that is a "jump to here' at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure info:

3069*	"FDE"	= D, E pair . . . D is the fill character and E is the test character
306B*	"FHL"	= H, L pair . . . the failure address
306D*	"FOUT"	= the data expected at this address
306E*	"FIN"	= the data read from, the address

* address from *Memory Testing Routine Listing.*

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference between "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

PHANTOM LINE

In response to increasing numbers of users who have requested inclusion of "PHANTOM LINE", buss pin 67 which is often used for implementing power on jump features. This board is designed for use with active or inactive PHANTOM lines.

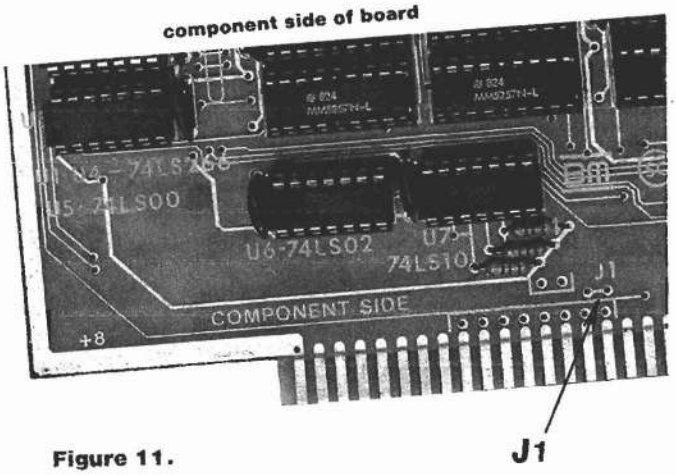


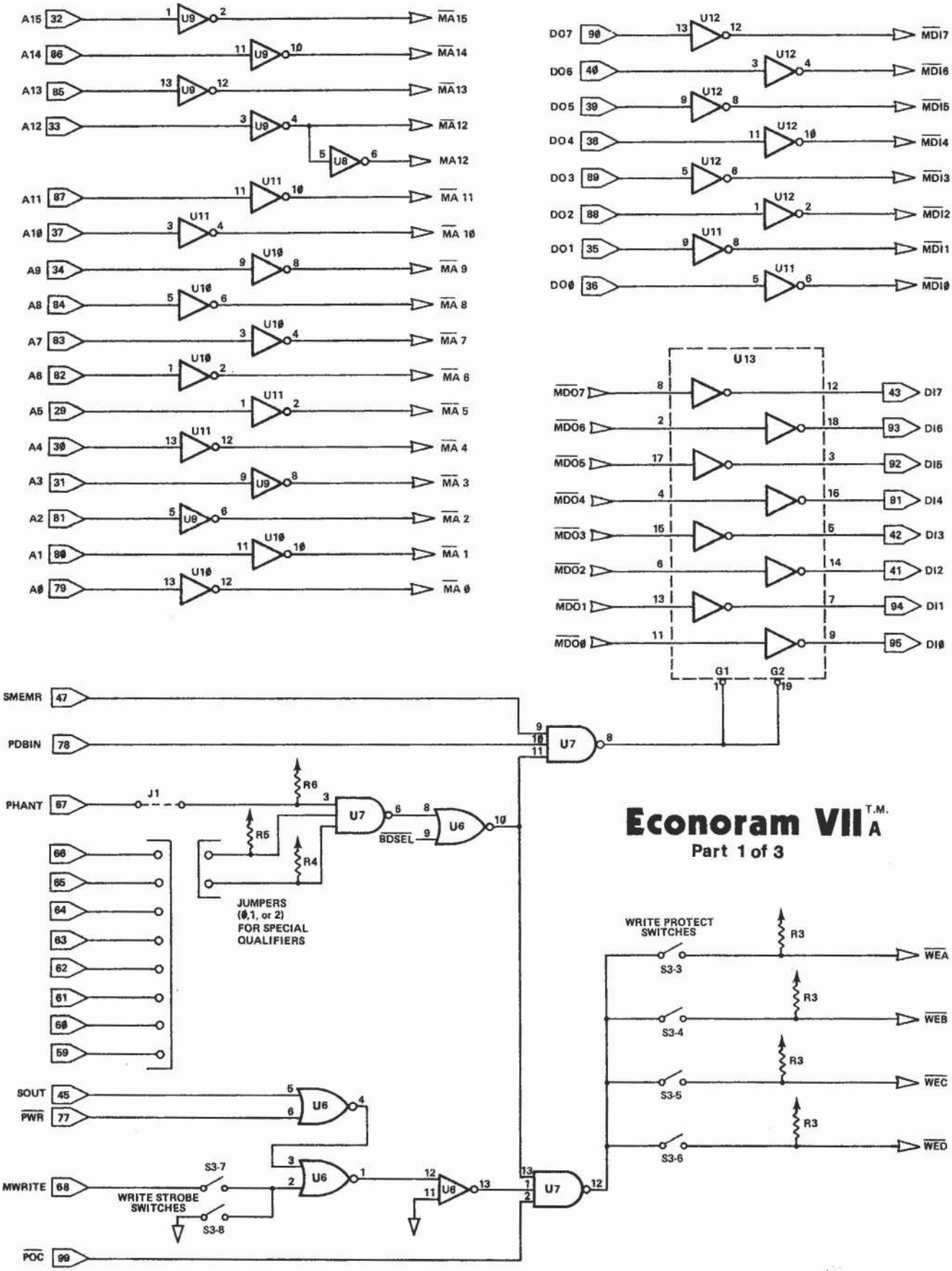
Figure 11. **J1**

CAUTION

Some manufacturers use PHANTOM line (buss pin 67) for a refresh signal. This will conflict with the PHANTOM feature, and cause boards with PHANTOM to fail. If your system has this conflict it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards.

The PHANTOM feature may be disabled by cutting the trace on the back of the PC board between pads for J1. It may be reactivated at any time simply by installing a jumper at J1 (see Figure 11).

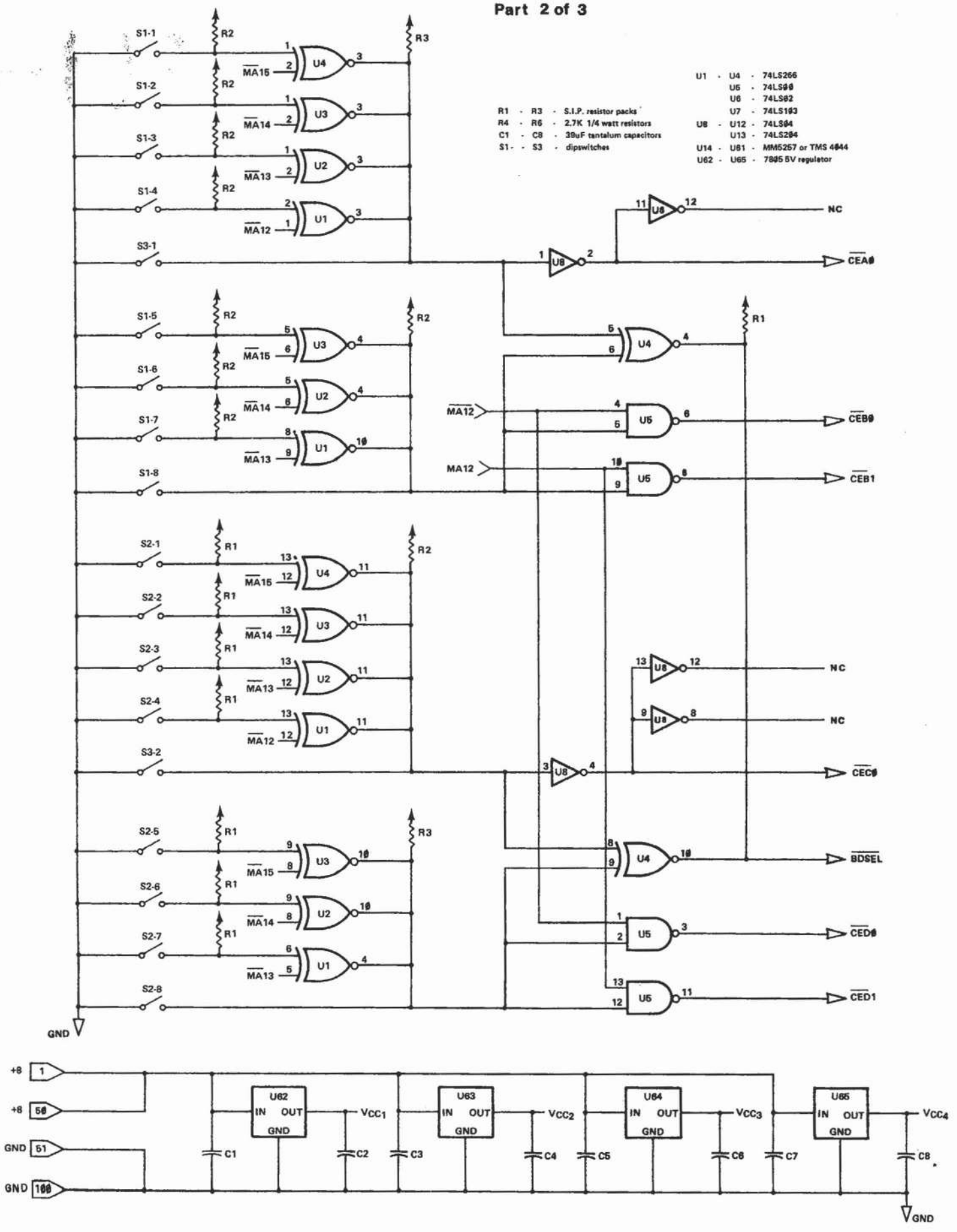
If you want the PHANTOM feature, the conficting refresh signal may be eliminated (IF NOT USED ELSEWHERE IN THE SYSTEM) by cutting the trace connected to buss pin 67 on the CPU board. *BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES.*

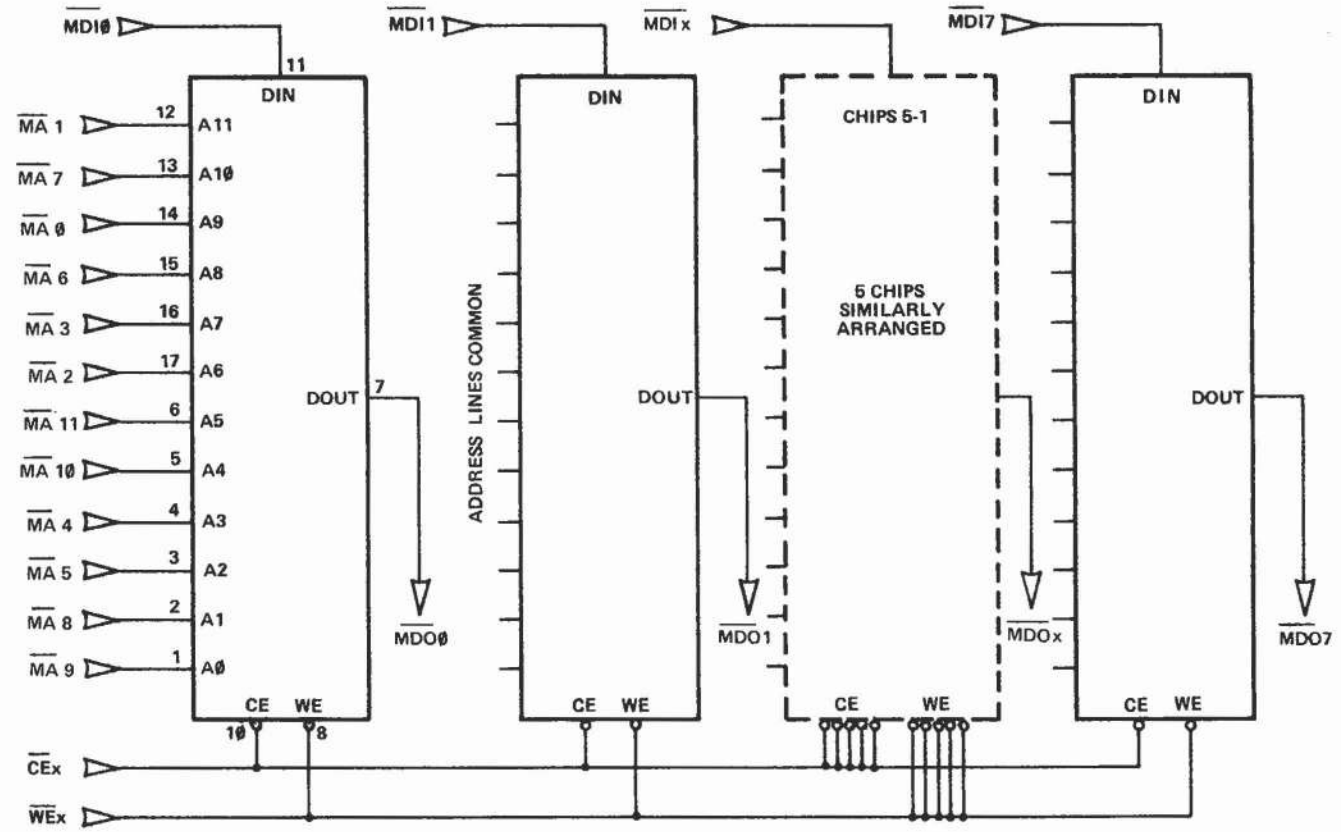


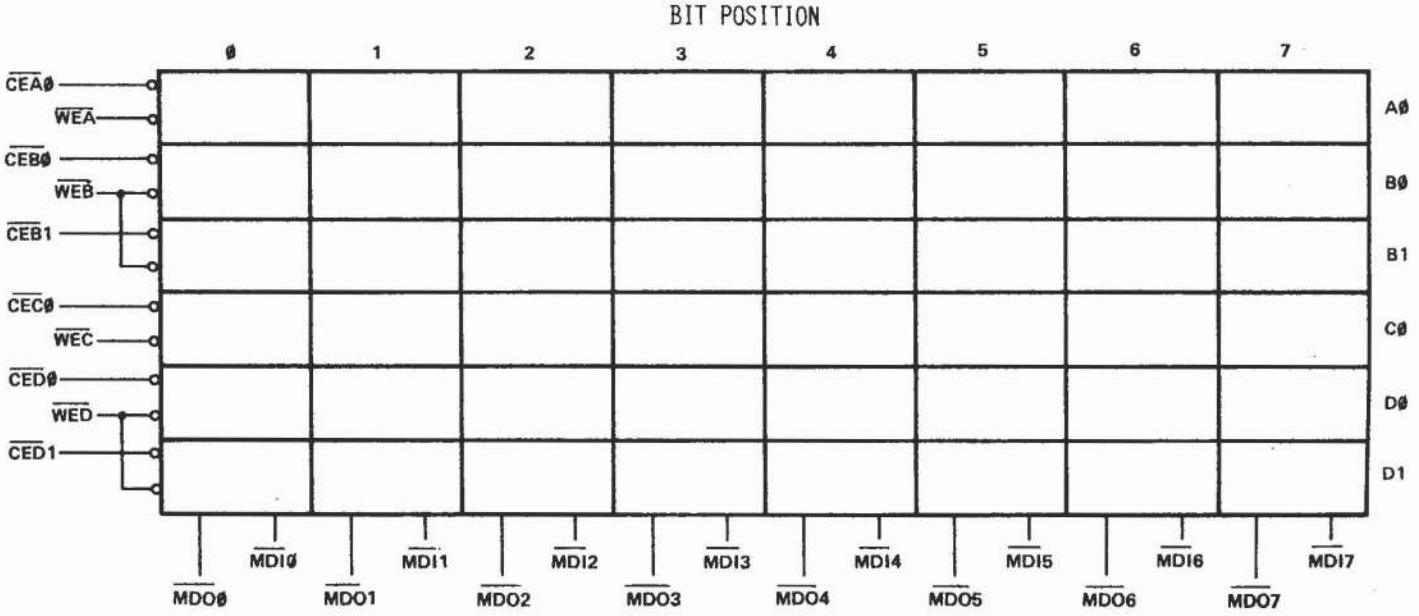
Econoram VII A T.M.

Part 1 of 3

Part 2 of 3


R1 - R3 - S.I.P. resistor packs
R4 - R6 - 2.7K 1/4 watt resistors
C1 - C8 - 39uF tantalum capacitors
S1 - S3 - dipswitches
U1 - U4 - 74LS266
U5 - 74LS00
U6 - 74LS02
U7 - 74LS193
U8 - U12 - 74LS04
U13 - 74LS284
U14 - U81 - MM5257 or TMS 4044
U62 - U65 - 7805 5V regulator
S1-1
S1-2
S1-3
S1-4
S3-1
S1-5
S1-6
S1-7
S1-8
S2-1
S2-2
S2-3
S2-4
S3-2
S2-5
S2-6
S2-7
S2-8
R1
R2
R3
MA15
MA14
MA13
MA12
U1
U2
U3
U4
U5
U8
NC
CEA0
CEB0
CEB1
CEC0
BDSEL
CED0
CED1
GND
+8
GND
U62
U63
U64
U65
IN OUT GND
VCC1
VCC2
VCC3
VCC4
C1
C2
C3
C4
C5
C6
C7
C8


MDI0
MDI1
MDIx
MDI7
DIN
DOUT
CHIPS 5-1
5 CHIPS SIMILARLY ARRANGED
ADDRESS LINES COMMON
MA 1
MA 7
MA 0
MA 6
MA 3
MA 2
MA 11
MA 10
MA 4
MA 5
MA 8
MA 9
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CE
WE
MDO0
MDO1
MDOx
MDO7
CEx
WEx


BIT POSITION
0
1
2
3
4
5
6
7
CEA0
WEA
CEB0
WEB
CEB1
CEC0
WEC
CED0
WED
CED1
A0
B0
B1
C0
D0
D1
MDI0
MDI1
MDI2
MDI3
MDI4
MDI5
MDI6
MDI7
MDO0
MDO1
MDO2
MDO3
MDO4
MDO5
MDO6
MDO7

MEMORY TESTING ROUTINE

Figure 13.

```
3000 21 00 40          0010 STRT LXI  H,4000H
3003 3E A0             0020 END  MVI  A,0A0H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP   DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP SHLT
3080                   0680 *
```

CIRCUIT DESCRIPTION

The heart of Econoram VII is the MM5257/TMS4044 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts.

These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 6 of these rows together produces a total memory storage of 24K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array).

Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to *write* data into the memory, or *read* data from the memory.

The schematics on pages 8 and 9 show the address circuitry along with the other Econoram VII circuitry. Each memory IC requires 12 address bits (A0-A11) to access any one of the 4096 bits available in the IC. These address bits are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array).

When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read on to the data buss from memory passes through 8 TRI-STATE® inverting buss drivers; when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state.

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4MHz over the full temperature range (0° - 70° C ambient) and to draw less than 2500 mA (2.5 amps). Our typical measured currents were less than 1210 mA at cold start-up, rapidly decreasing to around 1600-1900 mA, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

THANK YOU

This board is the result of much time, work and experience on the part of a number of people.

We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time. If we can be of any help to you in applying this board, or if you have any questions, please let us know. As always, we solicit your comments, letters, and new product suggestions.

HAPPY COMPUTING!

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuKit product. If this product fails to operate properly, it may be returned to us, see warranty information below.

If you have any questions about assembly, performance, specifications or need further information feel free to write us at:

P.O. Box 2355, Oakland Airport, CA 94614.

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone, for taking orders, (415) 562-0636. If you have problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). Unfortunately, we cannot return calls, or accept collect calls.

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *must* be returned for replacement.

If a defective part or design error causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $10.00.

We are not responsible for damage caused by use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

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