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MODEL 2832
HARD DISK CONTROLLER
and HARD DISK SUBSYSTEM
Reference Manual

California Computer Systems

42000081-01 Rev. A

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CCS MODEL 2832

HARD DISK CONTROLLER

and

HARD DISK SUBSYSTEM

Reference Manual

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000836

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The CCS Model 2832 Hard Disk Controller is designed to control a hard disk subsystem of up to four 10 megabyte or 20 megabyte Winchester-technology disk drives. Consisting of two PC boards, the 2832 features the Microcomputer Systems Corporation MSC-9016 Disk Controller Module, with DMA capability provided by a Z-80 DMA Controller. CCS's unique implementation of the DMA Controller ensures optimum data transfer rates. A number of user-configurable options provide compatibility with a variety of operating environments.

1.2 USING THIS MANUAL

This manual is intended primarily as a reference for system designers, programmers, and troubleshooters. It includes information on option configuration, software requirements, and hardware design. System designers and integrators will find board set-up instructions in Chapter 2 and installation instructions in Section 1.4. For programmers, Chapter 3 includes complete instructions for programming the MSC-9016 Disk Controller Module as well as a discussion of the programming requirements arising from the unique implementation of the Z-80 DMA Controller. Chapter 4 consists of a detailed examination of the hardware design and operation of the 2832, and is meant to be read in conjunction with frequent references to the schematics in Appendix B. Included in Appendix A are a parts list and various technical

tables and illustrations. Chapter 4 and the appendices will will be of interest primarily to troubleshooters.

Throughout this manual, low-active signals are indicated by an asterisk after the signal name/mnemonic (e.g., pWR*) or by a bar over the name/mnemonic.

1.3 SPECIFICATIONS

SYSTEM BUS	S-100: Meets IEEE 696 Standard
DRIVE BUS	Plug-Compatible with Fujitsu M2301/02B Up to Four Drives per Controller
DISK CONTROLLER	MSC-9016
DMA CONTROLLER	Z-80A DMA
DMA TRANSFER RATE	Up to 957 KB/sec Memory-to-Disk Up to 873 KB/sec Disk-to-Memory
USER OPTIONS	Base Address at Any Multiple of 8 Mode 2 Interrupt Priority Level DMA Priority Level 256 Byte or 512 Byte Sectors

1.4 INSTALLATION

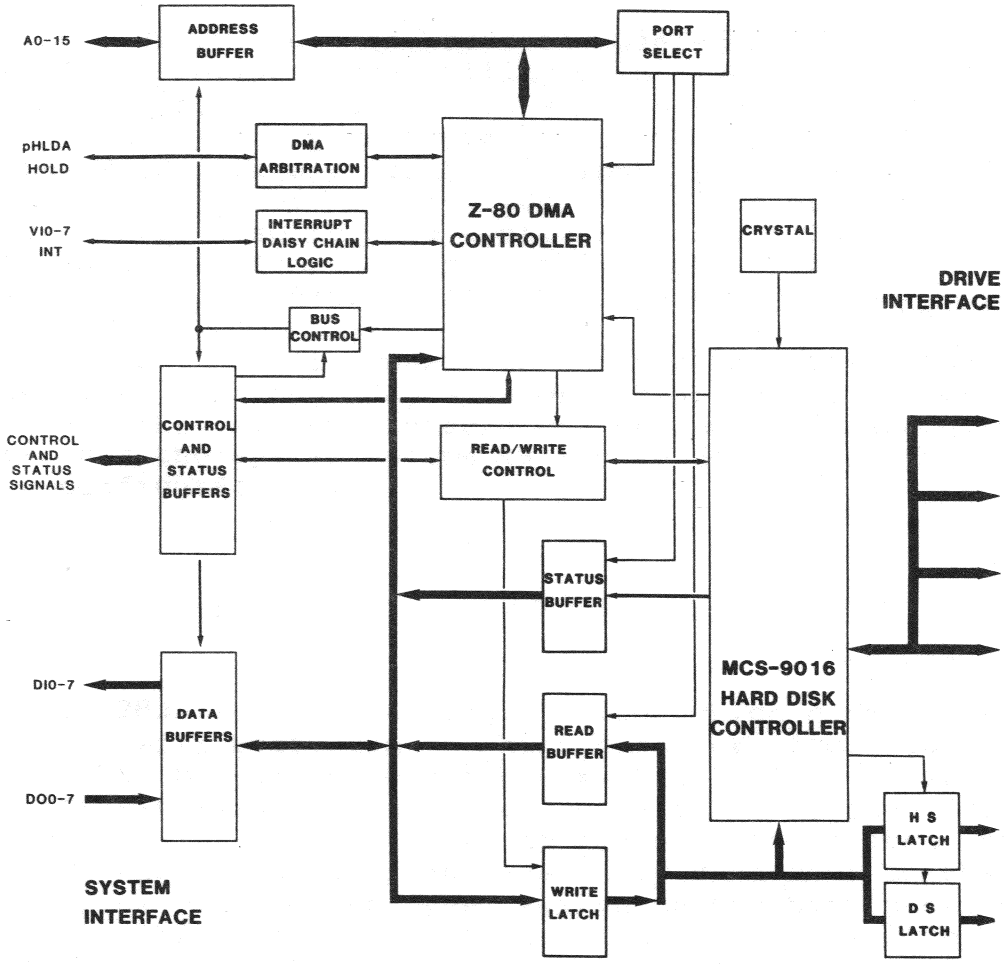
Always turn off power to the system before installing any board. For best operation, boards should be installed in the following order: CPU, memory, disk controllers, I/O, terminator.

The 2832 includes a toggle switch to control whether the system boots from hard disk or floppy. This switch should be mounted on the mainframe's back panel. If the back panel does not have a 1/4 inch hole for this purpose, we recommend that you drill one, though it is also possible to mount the switch in one of the unused connector slots. Plug the connector at the end of the switch cable onto the BOOT Jumper pins before you install the board in the mainframe.

From three to six cables must be installed for each 2832. A short 40-pin cable plugs to the J4 connectors of each board. The long 50-pin cable runs from J3 of board 2 (labeled A

CABLE) to the 5Ø-pin connector slot at the back of the mainframe. Finally, separate 2Ø-pin radial cables for each drive in the subsystem must run from the drive connectors on board 2 to the corresponding drive connector slots at the back of the mainframe.

1.5 2832 BLOCK DIAGRAM



1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
ØBH	x	x	x	x	x	ØØH	Ø1H	none

Table 3-13. Diagnostic Command

CHAPTER 2

USER OPTIONS

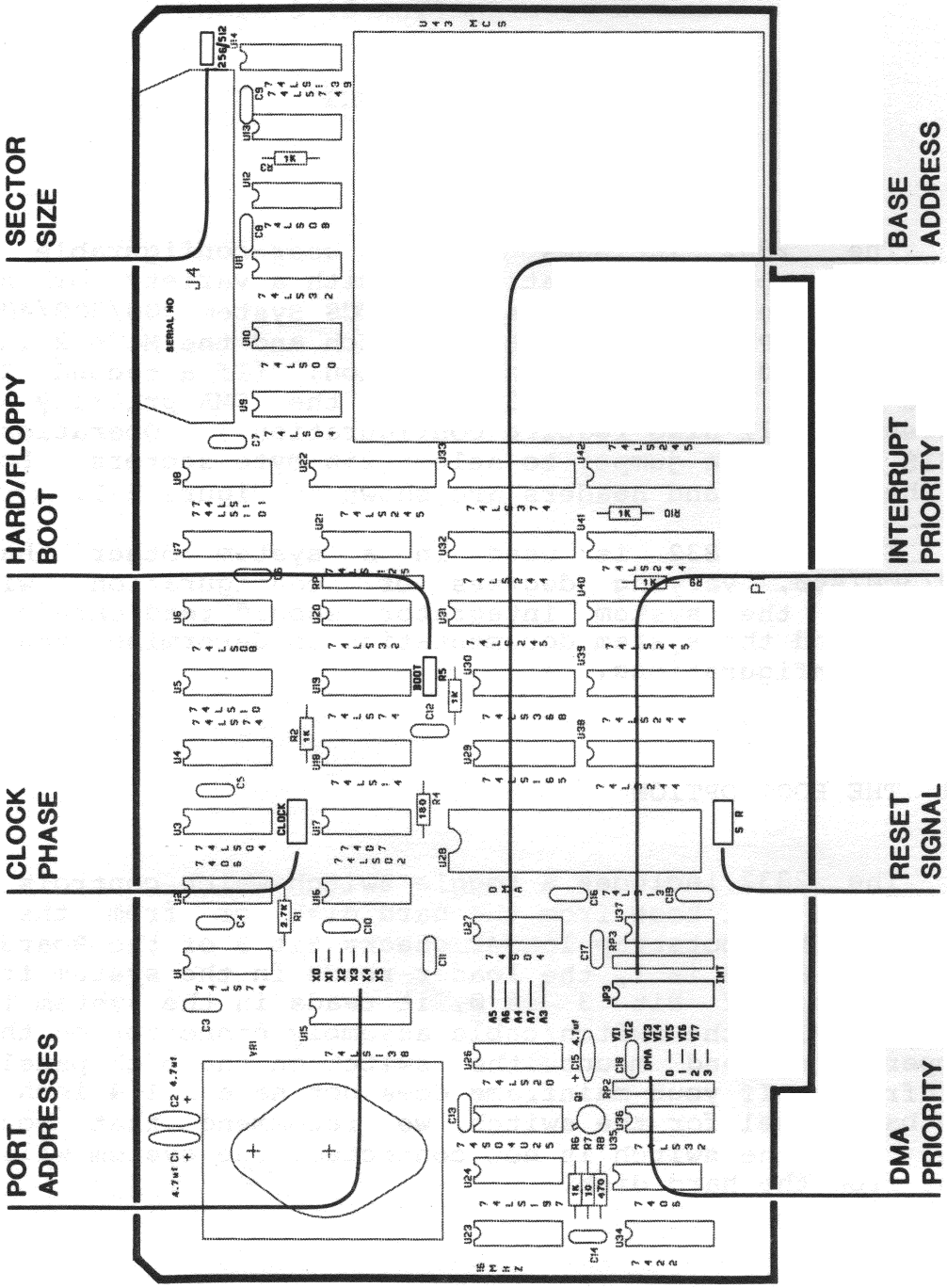
The 2832 includes several user-configurable options designed to provide compatibility with a variety of systems. It is pre-configured for use in a CCS System 200/300/400 under C/PM or M/PM; only the Boot Switch and the Mode 2 Interrupt Priority Header require configuration. (If a second 2832 is added to a System 200/300/400, the DMA priority and port addresses will also require configuration.) Operation under OASIS requires a jumper to select 256-byte sectors. Locations of the jumpers and headers are shown in Figure 2-1.

If the 2832 is used in a system other than a CCS 200/300/400, varying degrees of configuration will be required; the system integrator should read carefully this chapter and the system documentation to determine the proper option configurations.

2.1 THE BOOT OPTION

The 2832 includes a toggle switch which controls whether the system will boot from the hard disk or from the floppy disk. The bootstrap loader checks Bit 3 of the Board Status Port. If Bit 3 is 1, the loader reads in the system from the hard disk; if Bit 3 is Ø, it reads in the system from the floppy. Plug the switch/cable assembly connector on the BOOT Jumper pins and mount the switch on the back panel of the mainframe. If your mainframe does not have a 1/4 inch hole in the back panel for the switch, we recommend that you drill one. If the switch is not connected, the system will always boot from the hard disk.

Figure 2-1. JUMPER AND HEADER LOCATIONS



2.2 ADDRESS SELECTION

The 2832's addressable registers occupy three I/O ports. The eight-port block in which the registers reside and their positions within the block are separately selected. As shipped, the 2832 is configured for the following addresses:

FØH	DMA Controller Port
F1H	Disk Controller Data Port
F2H	Disk Controller Command Port

Jumpers A7-A3, located between U26 and U27, are hardwired to select the eight-port block FØ-F7H. To select a different block, cut traces and install jumpers in A7-A3 (circuit side of board) as required to match bits 7-3 of the base address in binary. A7-A4 select a 1 if the right pair of pads are closed or a Ø if the left pair of pads are closed; A3 is the opposite (1=left, Ø=right).

The X5-XØ Jumpers allow the 2832's registers to be mapped to the first three (Ø-2) or the second three (3-5) ports in the eight-port block. (Other arrangements are possible but not recommended.) The board is hardwired to map the registers to the first three ports (traces across XØ, X1, and X2 on the component side). To move the registers to the second three ports, cut the XØ, X1, and X2 traces and install jumpers in X3, X4, and X5.

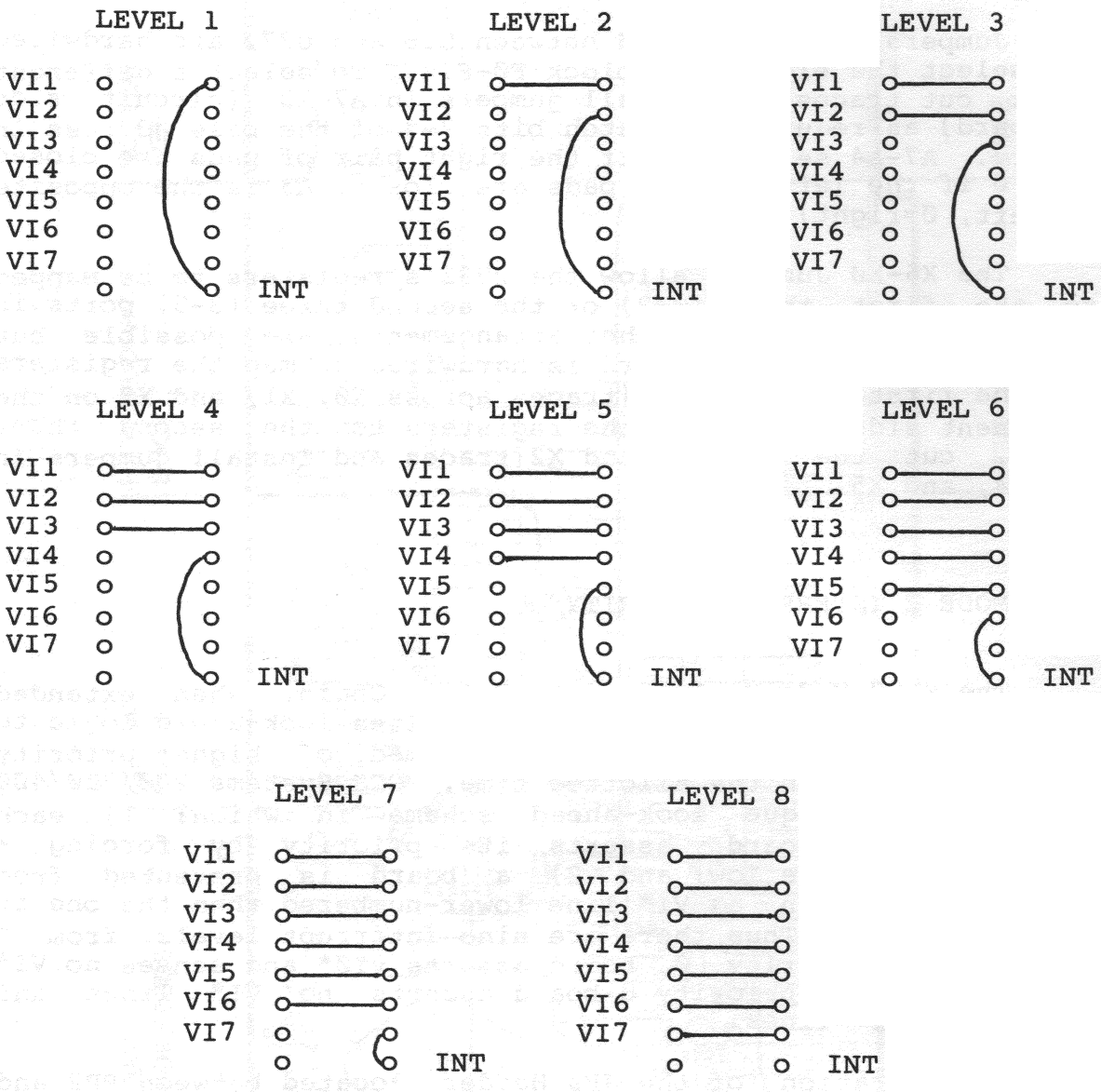
2.3 MODE 2 INTERRUPT PRIORITY

The Z-8Ø Mode 2 Interrupt Daisy Chain, when extended beyond four peripheral devices, requires look-ahead logic to ensure that all devices will be informed of higher-priority interrupts within the allotted time. CCS Systems 2ØØ/3ØØ/4ØØ implement a unique look-ahead scheme in which: 1) each participating board asserts its priority by forcing a different VI* line low; and 2) a board is prevented from interrupting when a VI* line lower-numbered than the one it asserts is low. Thus there are nine interrupt levels, from Ø to 8; the priority Ø board asserts VIØ* and senses no VI* lines, while the priority 8 board asserts no VI* lines and senses all VI* lines.

Configuration of the JP3 Header, located between RP2 and RP3, determines which VI* line the 2832 will assert and which VI* line(s) it will sense. This header is configured slightly

different than other CCS System Board Interrupt Priority Headers. To configure the header, tie the pin labeled INT to the RIGHT-column pin of the row corresponding to the desired priority level; then tie all lower-numbered VI pins straight across. Figure 2-2 shows the header configurations for all priority levels.

Figure 2-2. MODE 2 INTERRUPT PRIORITY CONFIGURATIONS



The priority scheme shown below should be appropriate for the majority of systems. The System Processor is hardwired for Level Ø; it is the only board whose priority is fixed. Gaps are allowed in the daisy chain; however, no priority level may be occupied by more than one board.

```
        Level Ø:  282Ø System Processor
        Level 1:  28Ø5 Clock/ROM/Terminator
        Level 2:  283Ø Six-Channel Serial I/O
        Level 3:  2719 2 Parallel/2 Serial I/O
        Level 4:  2831 Arithmetic Processor
        Level 5:  2833 GPIB Interface
        Level 7:  2822 Floppy Disk Controller
 ----->  Level 8:  2832 Hard Disk Controller
```

2.4 DMA PRIORITY

The DMA arbitration logic resolves simultaneous bus requests by two or more temporary bus masters by giving bus control to the highest priority device. The DMA priority level, from Ø to 15 (ØØØØb to 1111b) with 15 being highest, is determined by the DMA Jumpers, located below C18 between RP2 and JP3. The 2832 is hardwired for the highest DMA priority, 15. To select a different priority, determine the priority level in binary, then install a jumper plug for each bit (3-Ø, with 3 the most significant) which is a Ø.

2.5 SECTOR SIZE

The 2832 is hardwired to select a 512-byte sector size. To select a 256-byte sector size, as required for OASIS, install a jumper plug over the pair of header pins labeled 256/512, located above U14.

2.6 RESET SIGNAL

The Reset Jumper is located beneath U28. If the 2832 is used in a system which does not automatically assert SLAVE CLR* when RESET* is asserted, cut the trace between the pads labeled S and install a jumper between the pads labeled R. This is not necessary with CCS systems. If you are uncertain

whether the Reset Jumper requires reconfiguration for a specific non-CCS system, consult the system documentation or call the system manufacturer.

2.7 CLOCK PHASE

In some systems, including those featuring the CCS 2810 CPU board, the CPU clock and the system clock on bus pin 24 are of opposite phase. Z-80 devices in a system must all have clocks of the same phase to work together. The Clock Jumper allows the user to invert the phase of the system clock. If the 2832 is used in a system in which the bus clock and processor clock are of opposite phase, cut the trace between the rightmost pair of pads of the Clock Jumper (on the component side of the board) and install a jumper between the leftmost pair of pads.

CHAPTER 3

PROGRAMMING INFORMATION

3.1 PROGRAM ACCESSIBLE REGISTERS

As shipped from the factory, the 2832 is configured for the following port addresses:

DMA Control	FØH
Disk Data	F1H
Disk Control	F2H

When the CPU is the bus master, it reads from the Disk Control Port and checks the READY bit, then writes a dummy byte to the Disk Control Port to put the 9Ø16 in the command mode. Then the eight bytes of the command are written to the Disk Data Port. Depending on the command given, the appropriate data or status transfer then takes place through the Disk Data Port.

To read from or write to the disk using DMA, the Disk Data Port need not be directly addressed; both commands and data may be passed through the DMA Controller. The DMA Controller is initialized through the DMA Control Port, then a dummy byte written to the Disk Control Port to put the 9Ø16 into the Command Mode. If the command has been put at the front of the data buffer, it can then be transferred as part of the DMA operation. In this case the data buffer must be 8 bytes longer than the amount of data to be transferred, i.e., 52Ø bytes rather than 512 bytes if the sector size is 512 bytes. The 9Ø16 will determine whether data is transferred from buffer to disk or disk to buffer depending on the command it receives. Of course it is also possible to write the command to the Disk Data Port before initializing the DMA Controller, passing data only during the DMA. In this case the buffer need not be longer than the sector size.

Board Status can be read from the Disk Control Port. The Board Status byte has the following format:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
SECSZ	1	1	1	BOOT	READY	DRQ	DAV

SECSZ (SECTOR SIZE) = 1 indicates 256-byte sectors selected; SECSZ = Ø indicates 512-byte sectors selected.

BOOT = 1 indicates a boot from floppy disk; BOOT = Ø indicates a boot from hard disk.

READY = 1 indicates that the 9Ø16 is idle (9Ø16 output BSY inactive); READY = Ø indicates that the 9Ø16 is processing or acting on a command and should not be written to.

DRQ (DATA REQUEST) = 1 indicates that the 9Ø16 is ready to accept a data byte from the host (9Ø16 output LDI* active).

DAV (DATA AVAILABLE) = 1 indicates that the 9Ø16 is ready to output a data byte to the host (9Ø16 output DOUT* active).

3.2 PROGRAMMING THE DMA

3.2.1 General Instructions

The general principles of programming the Z-8Ø DMA chip are discussed in CCS's Z-8Ø FAMILY PROGRAMMING REFERENCE MANUAL, included with CCS Systems 2ØØ/3ØØ/4ØØ or available separately from CCS, and in numerous other publications, including those below:

AN INTRODUCTION TO MICROCOMPUTERS, Osborne and Associates, Inc. (Berkeley, CA: 1978).
ZILOG MICROCOMPUTER COMPONENTS DATA BOOK, Zilog, Inc. (Cupertino, CA: 198Ø).
MOSTEK MICROCOMPUTER DATA BOOK, Mostek Corporation (Carollton, TX: 1979).

3.2.2 CCS'S Implementation of the Z-8Ø DMA

CCS's implementation of the Z-8Ø DMA chip allows the maximum data transfer rates possible with the MCS-9Ø16. As a result, the programming options available with the Z-8Ø DMA are limited. Of the four DMA modes supported by the DMA chip, the 2832 supports only the Search For Match Byte mode. In the unsupported Data Transfer modes, the Z-8Ø DMA chip controls the data bus, generating the necessary bus read/write strobes. It thus requires two bus cycles to transfer a byte of data: one to read it from the source, and another to write it to the destination. On the 2832, however, the data bus during DMA is controlled by circuitry which is external to the DMA chip and which generates one read or write cycle per byte transfer depending on the direction of the data transfer. Thus the Z-8Ø DMA chip must be programmed in the one-cycle Search For Match Byte mode.

The following programming principles apply to CCS's application of the DMA chip on the 2832:

1. The DMA chip must be programmed in the Search For Match Byte mode only.

2. Of the four modes of bus access, three are supported: Single Byte, Burst, and Continuous. (The Transparent mode is not supported.) In the Continuous mode, the maximum data transfer rates of the 9Ø16 are theoretically obtainable: up to 957 kilobytes per second to disk and 873 kilobytes per second from disk.

3. The source address register must be loaded with the source address in memory for DMA reads and with the destination address in memory for DMA writes. It is never necessary to specify the disk controller as either source or destination for DMA transfers.

4. No match byte should be specified; the DMA chip will transfer data until the end of block is reached.

5. Only transfers to and from memory are supported; I/O transfers are not supported.

6. The Byte Count must be programmed for the exact number of bytes to be transferred, not one byte less.

7. RDY must be programmed active high.

3.3 DISK OPERATION COMMANDS

There are twelve commands, each requiring that eight bytes be written to the 2832. The format and order of the bytes are as follows:

	Task Byte	D7	D6	D5	D4	D3	D2	D1	DØ
1	Command Code	Ø	Ø	Ø	Ø	n	n	n	n
2	Drive Select	Ø	Ø	Ø	Ø	DS3	DS2	DS1	DSØ
3	Cylinder Address	A15	A14	A13	A12	A11	A1Ø	A9	A8
4	Cylinder Address	A7	A6	A5	A4	A3	A2	A1	AØ
5	Head Address	Ø	Ø	Ø	Ø	n	n	n	n
6	Sector Address	Ø	Ø	n	n	n	n	n	n
7	ØØH	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
8	Ø1H	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1

The Command Code and Cylinder, Head, and Sector Addresses are all binary values. The Drive Select byte should have a 1 in the bit corresponding to the drive to be selected; all other bits must be Ø. Not all commands require each byte; however, pad bytes must be sent for the unneeded bytes to maintain the eight-byte message length. (Pad bytes are indicated by an "x" in Tables 3-1 through 3-13.) Commands should be written to the Disk Control Port only when the disk controller is not busy and is ready for input.

3.3.1 DISK COMMAND DESCRIPTIONS

Code Ø--SEEK. The seek command moves the heads of the selected drive to the specified absolute cylinder on a formatted disk.

1 CODE	2 DRV	3 4 CYLINDER		5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
ØØH	ØnH	MSB	LSB	x	x	ØØH	Ø1H	none

Table 3-1. Seek Command

Code 1--READ ONE SECTOR. This command results in one sector of data being transfered from the disk drive to the host system. The 2832 positions the heads (implied seek), verifies the ID field, reads the sector, and corrects data errors prior to transferring the data. Data may be read at the Disk Data Port or transferred via DMA directly into memory. Note: If a Hard ECC error is encountered, no data is transferred. Therefore, if the processor is waiting for an interrupt from the DMA Controller at the completion of the data transfer, the system will hang.

1 CODE	2 DRV	3 CYLINDER		4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø1H	ØnH	MSB	LSB		ØnH	nnH	ØØH	Ø1H	256/512 in

Table 3-2. Read Sector Command

Code 2--WRITE ONE SECTOR. This command results in one sector of data being transferred from the host system to the disk. The disk controller module transfers one sector of data from the host into its internal buffer, positions the heads, verifies the ID field, and writes the data to disk. Data may be written to the Disk Data Port or transferred directly from memory to the disk controller via DMA.

1 CODE	2 DRV	3 CYLINDER		4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø2H	ØnH	MSB	LSB		ØnH	nnH	ØØH	Ø1H	256/512 out

Table 3-3. Write Sector Command

Code 3--FORMAT ONE TRACK--The Format command causes the ID and data fields to be initialized on the specified track. The data field is initialized with a preset pattern of B6DB6D. The head parameter in the command selects the head used; the cylinder parameter is used to write the ID field.

1 CODE	2 DRV	3 4 CYLINDER		5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø3H	ØnH	MSB	LSB	ØnH	x	ØØH	Ø1H	none

Table 3-4. Format Track Command

Code 4--RECALIBRATE. This command causes the heads to return to Track ØØ.

1 CODE	2 DRV	3 4 CYLINDER		5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø4H	ØnH	x	x	x	x	ØØH	Ø1H	none

Table 3-5. Recalibrate Command

Code 5--STATUS. This command causes one byte of status information regarding the previous task to be output during the next read of the Board Data Port.

1 CODE	2 DRV	3 4 CYLINDER		5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø5H	x	x	x	x	x	ØØH	Ø1H	1 in

Table 3-6. Status Command

The status byte should be interpreted as follows:

Byte	Meaning
ØØ	No Error
Ø1	Invalid Command
Ø2	Drive Not Ready
Ø3	Seek Timeout (2 seconds)
Ø4	Invalid Track ØØ Indication from Drive
Ø5	All ID Fields Bad on Track
Ø6	Target Sector Not Found
Ø7	No Sector Found and ID ECC Error (Target)
Ø8	Position Error (Seek Error)
Ø9	Defective Module or Support Signals
ØA	Drive Fault Active
ØB	Index/Sector Timeout
ØC	Command Parameter Error
ØD	Uncorrectable ECC Error
1x	Correctable ECC Error (x = Ø to BH, indicating length of corrected burst error)
2Ø	Write Alternate Error
21	Invalid Alternate Sector Assignment
22	Alternate Sector Already Assigned
23	Direct Access to Alternate Sector
24	Defective Processor
25	Defective Buffer Memory
26	Defective ECC Circuitry
27	Defective Program Memory
28	Illegal Sector Pulse During Diagnostic
29	Illegal Interleave Table Parameter

Table 3-7. Status Byte Definitions

Code 6--READ LONG. The Read Long command transfers one sector plus the four ECC (Error Correction Code) Bytes from the disk to the host. During this command, the module positions the heads (implied seek), verifies the ID field, reads the sector, and transfers the sector plus ECC bytes to the host. The module does not try to correct the data field if an ECC error occurs, allowing this command to be used to verify the ECC function of the module.

1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø6H	ØnH	MSB	LSB	ØnH	nnH	ØØH	Ø1H	26Ø/516 in

Table 3-8. Read Long Command

Code 7--WRITE LONG. The Write Long command transfers one sector plus four ECC Bytes from the host to the disk. During this command, the module transfers one sector plus the ECC bytes from the host to its internal buffer, positions the head (implied seek), verifies the ID field, and writes the data and ECC to disk. The appended polynomial should be: $X^{32}+X^{23}+X^{21}+X^{11}+X^{2}+1$.

1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø7H	ØnH	MSB	LSB	ØnH	nnH	ØØH	Ø1H	26Ø/516 out

Table 3-9. Write Long Command

Code 8--WRITE ALTERNATE SECTOR. This command is used to reassign a defective sector to an alternate sector on the track. During this command, the module transfers the sector of data from memory to the internal buffer, positions the heads (implied seek), and formats the ID fields to signify the defective and alternate assignment, then writes the data into the alternate sector. Note that if the rest of the track already holds data, it must be preserved by reading and rewriting all sectors after this command has been executed.

1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø8H	ØnH	MSB	LSB	ØnH	nnH	ØØH	Ø1H	256/512 out

Table 3-1Ø. Write Alternate Command

Code 9--SET INTERLEAVE. This command transfers to the module the interleave table correlating the logical to physical sector assignments. After CLEAR or a diagnostic command, the Module defaults to no interleave. The number of bytes of the Interleave Table is equal to the number of sectors per track (21 if 512 bytes per sector; 38 if 256 bytes per sector) and should take the following form:

```
Byte Ø      Physical location of logical sector Ø
Byte 1      Physical location of logical sector 1
Byte 2      Physical location of logical sector 2
.           .
.           .
Byte N      Physical location of last logical sector, N
```

1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
Ø9H	x	x	x	x	x	ØØH	Ø1H	21/38 out

Table 3-11. Set Interleave Command

Code A--WRITE CHECK. This command is identical to the Read Sector command, except that no data is transferred. It is used to verify that the previously written data can be read without ECC errors.

1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
ØAH	ØnH	MSB	LSB	ØnH	nnH	ØØH	Ø1H	none

Table 3-12. Write Check Command

Code B--DIAGNOSTIC. This command causes the Module to execute a self-test that checks its internal processors, data buffers, ECC circuitry, and Program memory. Execution of a Status command will give the results. If the Diagnostic command does not complete within 3Ø seconds, an error condition is preventing communication. After the test is complete, the module will be in a clear state.

1 CODE	2 DRV	3 CYLINDER	4	5 HD	6 SCT	7	8	NUMBER OF DATA BYTES
ØBH	x	x	x	x	x	ØØH	Ø1H	none

Table 3-13. Diagnostic Command

CHAPTER 4

HARDWARE DESIGN

The 2832 Hard Disk Controller provides the circuitry necessary for controlling the Winchester hard disk drives in CCS's System 400 series. Featuring a Z-80 DMA Controller, the 2832 is capable of direct, single-cycle disk-to-memory and memory-to-disk transfers at data rates approaching 1 megabyte per second. DMA arbitration logic allows the 2832 to be set to any priority level in systems with more than one DMA device, provided that the other DMA devices also implement the IEEE DMA arbitration logic. The 2832 also participates in CCS's special implementation of the Z-80 Mode 2 Interrupt Daisy Chain.

4.1 DESCRIPTION OF MAJOR LOGICAL COMPONENTS

4.1.1 THE 9016 DISK CONTROLLER

Microcomputer Systems Corporation's MSC-9016 module performs most of the tasks involved in controlling a Memorex or Fujitsu hard disk drive: sector reads and writes; sector data buffering; error detection (up to 22 bit burst-errors) and error correction (up to 11 bit burst-errors); alternate sectoring and variable sector interleaving; self-diagnostic tests; and automatic retries (up to four) on seeks, sector verifications, hard ECC read errors, and alternate sector writes. Figure 4-1 illustrates the major components of the MSC-9016; Table 4-1 identifies the chip's inputs and outputs. A data sheet on the MSC-9000 series is available from:

MICROCOMPUTER SYSTEMS CORPORATION
P.O Box 512
Sunnyvale, CA 94086

Table 4-1. 9016 Signals

PIN	MNEMONIC	SIGNAL AND FUNCTION
1	LDI*	Load Data In output. Used to gate host data into module if RDY* active.
2	DOUT*	Data Out output. Indicates valid data on bus: for host if RDY* active, drive if DCV* active.
4	CLR*	Clear input. Clears the module.
7	SL512	Select 512 input. Selects 512 bytes/sector if high, 256 bytes/sector if low.
8,9	DC0,DC1	Disk Control 0,1 outputs. Encode which disk status or control signals are on the bus.
13	CMD*	Command Mode input. When BSY active, causes module to enter command mode. May go low anytime after first command byte is received.
16	RDY*	Ready output. Signifies when data can be transferred and STB activated.
17	BSY	Busy output. Indicates when module is processing or executing a command.
18	DCV*	Disk Control Valid output. Indicates DC0,DC1 valid.
19	CLK	Clock input. 4 MHz.
22	STB	Handshake input. Strobes data into module (LDI* low); acknowledges that host has received data (DOUT* low).
24	PSTN	Position input. Pulse for defining rotational position of disk.
25	RGTE	Read Gate output to disk drive.
26	RDTA	Read Data input. NRZ serial data from disk.
27	WGTE	Write Gate output to disk drive.
28	WDTA	Write Data output. Serial data for disk.
29	INDX	Index input. Index pulse from drive.
30	PLO	PLO Clock input. PLO Clock from drive for strobing read and write data.
31-8	DTA0-7	Data 0-7. Bidirectional, tri-state data bus.

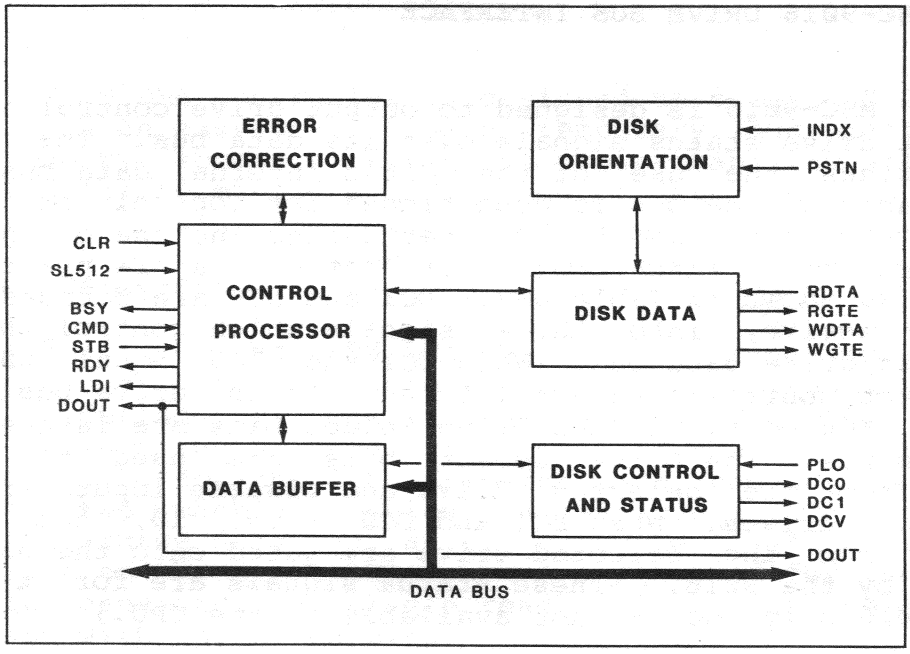


Figure 4-1. 9016 Block Diagram

4.1.2 MSC-9016 SYSTEM BUS INTERFACE

Before it performs one of its twelve operations, the 9016 must receive an eight-byte command telling it which operation to perform and giving it the necessary operating parameters. (If less than eight bytes of information are required, pad bytes must be sent.) The 9016 enters the command mode when its CMD* input is forced low and its BSY output is low. The RDY* output signifies when the 9016 is ready to accept or output data (including commands and status). The outputs LDI* and DOUT* are the chip's read and write signals; LDI* signifies that the 9016 expects to receive data, while DOUT* signifies that the 9016 has data ready for either the host or a disk. The 9016's STB input is used for data transfer handshaking; it strobes data into the module when LDI* is active and acknowledges that the host has received data when DOUT* is active.

4.1.3 MSC-9Ø16 DRIVE BUS INTERFACE

The MSC-9Ø16 is designed to output drive control signals and input drive status signals over its data bus. The output DCV* defines the use of the 9Ø16's internal data bus; when DCV* is active, the bus is conditioned for control or status bits. Outputs DC1 and DCØ further define the use of the data bus by indicating which control or status bits are present on the bus, as shown in Table 4-2. DC1 and DCØ are decoded, when DCV* is active, into three signals which control the disk controller/drive data bus. When DC1 and DCØ equal ØØ, the Head Select/Control bits are latched onto the drive bus. When DC1 and DCØ equal Ø1, the Drive Select bits are latched onto the drive bus. The Drive Select bits are used to enable inputs from the selected drive and disable inputs from the de-selected drives. When DC1 and DCØ equal 1Ø, the status signals from the selected drive are gated onto the data bus and read by the 9Ø16. (These status signals are for the use of the 9Ø16 only and are not available to the CPU.)

Table 4-3 summarizes the contents of the data bus for given states of DC1 and DCØ when DCV* is active.

DC1,DCØ = ØØ Head Select/ Control Out	DC1,DCØ = Ø1 Drive Select Out	DC1,DCØ = 1Ø Status In	DC1,DCØ = 11 Does Not Occur

Table 4-2. Drive Bus Multiplexing

Data Bits	DC1,DCØ = ØØ Head Select/ Control	DC1,DCØ = Ø1 Drive Select	DC1,DCØ = 1Ø Status
DØ	Head Ø	Select Ø	Track ØØ
D1	Head 1	Select 1	Write Fault
D2	Head 2	Select 2	Seek Complete*
D3	Head 3	Select 3	Drive Readv*
D4	Step		
D5	Direction		
D6	Fault Clear		
D7			

Table 4-3. Data Bus Contents When DCV*=Ø

4.1.4 THE Z-8Ø DMA CONTROLLER

The Z-8Ø DMA Controller is designed to provide Z-8Ø-based systems with an easy-to-interface temporary bus master for direct memory access. Extensive programmability allows the DMA Controller to manage a wide range of data searches and/or transfers. Table 4-4 defines the DMA Controller inputs and outputs. The device includes logic to support the Z-8Ø Mode 2 Interrupt Daisy Chain.

The 2832 uses the Z-8Ø DMA chip in a unique application designed to provide the fastest possible data transfer rates. Normally, during DMA operations, the system bus control signals reflect the RD* and WR* outputs of the DMA controller. When programmed for the data transfer mode, the DMA Controller generates two machine cycles: a read cycle (RD* active) to obtain the source data and a write cycle (WR* active) to transfer it to the destination; when programmed for the search mode, it generates a single read cycle to get the data for comparison with the match byte.

CCS has designed the 2832 so that the data bus and read/write signals are controlled by the 9Ø16 rather than by the DMA Controller, allowing either a read cycle or a write cycle to be generated when the DMA Controller is in the search mode. (The DMA chip still controls the address bus and pSYNC.) Because the data does not pass through the DMA Controller, but instead is transferred directly between the 9Ø16 and memory, only one cycle is needed for each byte transfer, significantly increasing the data transfer rate.

The S-1ØØ bus provides for arbitration of simultaneous bus requests by dedicating four lines, DMA3*-DMAØ*, for DMA priority assertion by up to 16 temporary bus masters. If a temporary master desires the bus and no other temporary master has requested or controls the bus (pHLDA and HOLD* both inactive), it places its unique 4-bit priority number on the bus and asserts HOLD*--the higher the binary number it asserts (low state = 1), the higher its priority. On the rising edge of pHLDA, the lower-priority temporary masters stop asserting HOLD* and their priority bits and wait for the next sequence of arbitration, which occurs when the current temporary bus master releases the bus. (It is after bus release by a temporary master that simultaneous bus requests are most likely to occur.) The highest-priority temporary bus master takes control of the bus, continuing to assert HOLD* and pHLDA until it finishes its operations and relinquishes the bus. After the falling edge of pHLDA, the arbitration process is repeated if necessary.

Table 4-4. DMA Controller Signals

PIN	MNEMONIC	SIGNAL AND FUNCTION
1-6 17-24 39-40	A15-A0	Address outputs. Used during DMA to address source and destination.
7	CLK	System clock input.
8	WR*	Bidirectional Write signal used as input only. Strobes control word into DMA Controller.
9	RD*	Bidirectional Read signal. As input, enables read of DMA Controller status. As output, strobes both read and write data during DMA (search mode).
10	IORQ*	As an input controlled by CPU, I/O Request indicates (when CE* is low) a control word write to or status read from the DMAC. As an output, IORQ* indicates during DMA a valid I/O address on A7-A0.
12	MREQ*	Memory Request output. Low when A15-A0 hold a valid source or destination address.
14	BAI*	Bus Acknowledge In input. Signals that bus control has passed to the DMA Controller.
15	BUSRQ*	Bidirectional Bus Request. Used only as an output to request bus control from the CPU.
16	CE*	Chip Enable input. Enables reading from and writing to the DMA during I/O cycles.
25	RDY	Ready input. Programmable active high or low. Used by disk controller to indicate that it is ready for a DMA operation.
26	M1*	M1 cycle input. Used in decoding RETI instruction for interrupt arbitration. M1* and IORQ* both low indicates an interrupt acknowledge by the CPU.
27-29 31-35	D0-7	Bidirectional Data pins.
37	INT*	Interrupt Request output.
38	IEI	Interrupt Enable In input. DMA Controller can interrupt only when this signal is high. Used to let higher-priority devices disable DMA interrupts.
39	IEO	Interrupt Enable Out output. Goes low when INT* or IEI is low. Used to disable interrupts by lower-priority devices.

4.1.5 THE INTERRUPT DAISY CHAIN

DMA Controller pins IEI, IEO, and INT* provide for the daisy-chaining of interrupts. The DMA Controller can respond to an Interrupt Acknowledge only if its IEI (Interrupt Enable In) is high. If either IEI is low or the device has forced INT* low, IEO (Interrupt Enable Out) is forced low. The daisy chain is implemented by connecting the IEO of a device to the IEI of the next-lower-priority device. The highest-priority device's IEI is tied high; the lowest-priority device's IEO is not connected. The highest-priority device requesting an interrupt puts its interrupt vector on the bus when the CPU acknowledges the interrupt.

The 2832, like all other CCS System 200/300/400 boards capable of generating interrupt requests, uses the S-100 Vectored Interrupt lines in a fast look-ahead scheme for extended Z-80 Mode 2 Interrupt Daisy Chains. Without look-ahead (i.e., in a simple daisy chain in which a device receives interrupt arbitration information only from the next higher-priority device in the chain), the daisy chain can be no more than four Z-80 devices long; if the chain is longer, the ripple-through time will be too great for the lowest-priority device to be notified of an interrupt request by the highest-priority device before the CPU acknowledges the interrupt. Look-ahead circuitry combines parallel and serial daisy chain logic to ensure that each device is no more than four devices from the highest-priority device, allowing daisy chains of 30 or more devices.

4.1.6 DATA BUFFERS

The buffers between the DI and DO buses and the 2832's internal data bus are bi-directional 74LS245's. Bi-directionality is required because when the DMA Controller is a slave the board inputs over the DO lines and outputs over the DI lines, while when the DMA Controller is the bus master it inputs over the DI lines and outputs over the DO lines. The DI buffer lets data onto the board only during DMA Reads; it lets data off the board when: 1) the CPU is reading from one of the board's three ports; OR 2) the CPU acknowledges an interrupt and the DMA Controller has the highest-priority interrupt pending. The DO buffer lets data off the board only during DMA Writes; it lets data on the board at all times EXCEPT when: 1) the DI buffer is enabled (letting data either on or off the board); OR 2) a DMA Write is in progress.

It is important that the DO buffer let data onto the board when the board is idle so that when the DMA Controller is waiting for a higher-priority interrupt to be serviced before putting its own interrupt request on the bus, it can monitor the DO lines for the RETI instruction which indicates that the interrupt in progress is ending. It is assumed that the system processor board connects the DI and DO buses internally so that the instruction input to the CPU on the DI bus is made available to peripheral boards on the DO bus. The CCS 282Ø System Processor meets this requirement.

4.1.7 CLOCKS

The clock for the DMA chip is supplied by the system clock. The phase can be altered by a jumper, allowing the user to compensate for a bus clock which is inverted in relation to the CPU clock. (In a Z-8Ø-based system, the CPU and peripheral clocks must be synchronized.) The clock for the disk controller chip, however, is independently controlled by an on-board 16 MHz crystal oscillator, ensuring a 4 MHz clock for the 9Ø16 independent of the system clock, which in some cases might be 2 MHz.

4.2 2832 OPERATION

4.2.1 DISK CONTROLLER COMMAND AND STATUS OPERATIONS

The Command Port, to which disk controller commands are written and from which disk controller status is read, is located at the board's base address + 2. A write to this address clocks (on the rising edge of pWR*) a flip-flop, which outputs a low to the 9Ø16's CMD* input if the 9Ø16's BSY output is inactive. This conditions the 9Ø16 to receive the eight bytes needed to specify a command. The command bytes themselves are written to the Data Port.

A read from the Command Port enables the Status Buffer, gating four bits of controller/host interface status onto the data bus to be read by the CPU. The Board Status bits are defined in Section 3.1.

4.2.2 DATA TRANSFERS: CPU BUS MASTER

When the CPU is the bus master, command bytes, 9Ø16 internal status, and data are all transferred through the Data Port, located at the base address + 1. The CPU determines whether the 9Ø16 is ready to receive or transmit data by polling status bits DATRQ and DATAV, described above. Addressing the Data Port clocks a flip-flop when pDBIN (processor read cycle) or pWR* (processor write cycle) goes inactive; the flip-flop outputs a high to the 9Ø16's STB input, which strobes data into the module (processor write cycle) or acknowledges that data has been received (processor read cycle). In processor write cycles, the command or data byte is latched on the trailing edge of the write pulse. During processor read cycles, status or data from the 9Ø16 is gated onto the data bus for the duration of pDBIN active.

4.2.3 DMA BUS REQUEST ARBITRATION

When the 9Ø16 is ready for data to be loaded in (LDI* active) or has data ready to output (DOUT* active), it forces the DMA's RDY input high to indicate that a DMA operation should begin. When the DMA Controller finds RDY high, it immediately asserts BUSRQ*, requesting control of the system bus.

The 2832 follows the IEEE specifications for the S-1ØØ bus in the implementation of the DMA bus request arbitration logic. If another temporary master has the bus (HOLD* or pHLDA active) when the DMA Controller asserts BUSRQ*, the arbitration logic keeps the 2832's priority bits off the bus. If, however, both HOLD* and pHLDA are inactive, the assertion of BUSRQ* causes HOLD* to be forced low and the board's priority bits to be gated onto the bus.

If another device is requesting control of the bus at the same time, it will also put its priority onto the bus. The 2832 compares its priority to the priority on the bus on a bit-serial basis, starting with the highest-order bit. A bit is 1 if the corresponding DMA* lines is pulled low. When the 2832 arbitration logic finds a 1 on the bus where it has a Ø, it removes all lower-order bits to prevent ORing of the priority codes. (Without this feature, one board putting 1Ø1Ø on the DMA* lines while another board put out 11ØØ would cause 1110 to appear on the bus, and both boards would drop out in favor of the illusory board with priority 1110.) When the DMA* lines settle they will thus encode the priority of the

highest-priority board requesting the bus. If the 2832 sees its priority on the bus when pHLDA is asserted by the processor, the BAI* input to the DMA Controller is forced low, and the 2832 takes control of the bus.

Bus transfer must occur in an orderly fashion. Shortly after the 2832 wins the DMA arbitration, it disables the CPU's address and data buses. At the same time, it asserts its control and status signals. At this point, both the CPU and the 2832 are putting control and status signals on the bus as specified in the IEEE 696 S-100 bus standards (pHLDA true; pSYNC, pSTVAL*, pDBIN, pWR* false). Finally, the 2832 disables the CPU's control and status outputs and takes complete control of the bus. When the 2832 relinquishes the bus, the process is reversed; after the removal of HOLD* (by BUSRQ* going inactive), the CPU control and status signals are enabled first, followed by the address and data buses.

4.2.4 BUS CONTROL DURING DMA

When the DMA Controller becomes the bus master, it controls the address bus but exercises relatively little control over the status and control buses. The status signals sOUT, sINP, sINTA, and sM1 are always set false during DMA (all transfers being between disk and memory), while pHLDA is held true. Only pSYNC is controlled solely by the DMA Controller, coming true for one clock cycle at the beginning of each DMA operation.

The signals pWR*, pDBIN, sWO*, and sMEMR, which indicate the direction of data transfer, are all controlled by the 9016, with the DMA chip's RD* output used to qualify the timing. (WR* is not used because the DMA Controller is always programmed in the Search mode, in which there are no write cycles.) The LDI* and DOUT* outputs of the 9016 determine which signals will go active. When RD* and LDI* are active, pDBIN is asserted to indicate to the addressed memory that it is to gate data onto the bus. When RD* and DOUT* are active, pWR* is asserted to indicate to the addressed memory that valid data is on the bus. The states of sMEMR and sWO* are similarly controlled by DOUT* and LDI* respectively.

4.2.4.1 DMA READS

When the 2832 logic asserts pDBIN (both 9Ø16 output LDI* and DMA output RD* active), it also inverts the same signal to clock, at the end of the read pulse, the Strobe Flip-Flop. The Strobe Flip-Flop forces the 9Ø16's STB input high, strobing memory data into the module. The data present on the bus when pDBIN goes inactive is latched to ensure that it will be valid when the 9Ø16 reads it. Data stays latched until the 9Ø16 removes the LDI* signal.

4.2.4.2 DMA WRITES

When the 2832 logic asserts pWR* (both 9Ø16 output DOUT* and DMA output RD* active), it also enables the buffer that passes data from the 9Ø16 onto the data bus. (The data is immediately valid because pWR* is not generated until after DOUT* goes active.) On the rising edge of pWR*, the buffer is disabled and the Strobe Flip-Flop is clocked, forcing STB high. When data is being passed from the 9Ø16, STB acts as an acknowledge signal, telling the module that the data has been taken and causing it to remove DOUT*. The Strobe Flip-Flop is in turn reset by the removal of DOUT*.

4.2.4.3 DMAING 9Ø16 COMMANDS

9Ø16 commands may be transferred as part of the DMA transfer if they are first loaded into the bottom eight bytes of the buffer, whether the actual DMA transfer is a read from or write to disk. After 9Ø16 input CMD is asserted, LDI* goes high until eight bytes (the command) are received. Because LDI* active causes a DMA read if the DMA Controller is the bus master, the first eight bytes of the buffer are automatically loaded into the 9Ø16. The 9Ø16 then asserts DOUT* or LDI* according to the command it has received and data is either read from the buffer to the disk or written from the disk to the buffer.

4.2.5 INTERRUPT REQUESTS

The 2832's priority level in the interrupt daisy chain is determined by the configuration of the Interrupt Daisy Chain Header. The DMA Controller's IEI input is forced low if VIØ* (the System Processor's priority assertion line) or any VI*

line tied across the header (and controlled by a higher-priority board's interrupt logic) is pulled low. This disables output of the interrupt vector by the 2832 if a higher-priority device has requested an interrupt. If its IEI input is not pulled low, the DMA Controller can request an interrupt by pulling bus line INT* low. (However, to prevent interrupts by the DMA Controller before the 9Ø16 has finished its part of the task, INT* is held high as long as the 9Ø16's BUSY signal is active.) The INT pin of the header should be tied to the VI* line corresponding to the board's priority level. When either of the DMA Controller's IEO and IEI pins is low, the board's VI* line will be pulled low to disable interrupts by lower-priority boards in the daisy chain.

APPENDIX A

TECHNICAL INFORMATION

A.1 USER-REPLACEABLE PARTS: 2832, BOARD 1

QTY	REF	DESCRIPTION	CCS PART #
Integrated Circuits			
1	U15	74LS138 3-to-8 decoder	48200022-01
1	VR1	LM323 +5 V regulator	48200107-01
1	U37	74LS13 dual 4-in NAND	48200120-01
3	U11,20,36	74LS32 quad 2-in OR	48200013-01
2	U6,12	74LS08 quad 2-in AND	48200006-01
1	U14	74LS139 dual 2-to-4 dec	48200023-01
4	U32,38,39,41	74LS244 octal buffers	48200035-01
1	U16	74LS02 quad 2-in NOR	48200002-01
2	U3,9	74LS04 hex inverters	48200004-01
2	U25,27	74S04 hex inverters	48200043-01
1	U10	74LS00 quad 2-in NAND	48200001-01
1	U2	7406/7416 hex inver, OC	48200048-01
1	U17	7407/7417 hex buff, OC	48200051-01
2	U5,7	74LS10 tri 3-in NAND	48200008-01
1	U8	74LS11 tri 3-in AND	48200125-01
2	U18,34	74LS14 hex inverter	48200009-01
1	U26	74LS20 dual 4-in NAND	48200010-01
1	U35	7422 dual 4-in NAND, OC	48200128-01
1	U21	74LS125 quad 3-st buff	48200126-01
1	U29	74LS165 8 bit shift reg	48200030-01
4	U1,4,13,19	74LS74 dual D flip-flop	48200015-01
1	U24	74LS197 binary counter	48200033-01
4	U22,31,40,42	74LS245 oct transceiver	48200127-01
1	U30	74LS368 hex driver	48200040-01
1	U33	74LS374 oct D flip-flop	48200042-01
1	U28	Z-80A DMA Controller	48200085-01
1	U43	MCS-9016 Disk Cont	48200094-01
1	U23	Xtal, DIP, 16MHz	48200118-01
Capacitors			
16	C3-14,16-19	.1uf Mono, 50VDC, 20%	15900001-01
3	C1,2,15	4.7uf Tant, 35VDC, 20%	15500003-01
Resistors			
1	R1	2.7K ohm, 1/4 Watt, 5%	47000023-01
1	R7	10 ohm, 1/4 Watt, 5%	47000001-01
1	R4	180 ohm, 1/4 Watt, 5%	47000014-01
1	R8	470 ohm, 1/4 Watt, 5%	47000029-01
6	R2,3,5,6,9,10	1K ohm, 1/4 Watt, 5%	47000003-01
3	RP1-3	SIP Network, 4.7K x 7	47400004-01

QTY	REF	DESCRIPTION	CCS PART #
Sockets			
1	XJP3	16 pin DIP	21400015-01
1	XU28	40 pin DIP	21400020-01
Miscellaneous			
1	Q1	Transistor, 2N2222	48000001-01
1	J4	Conn, 2 x 20 pin	21000026-01
1		Header, 16 pin DIP	21600001-01
1		Header Cover, 16 pin	14100001-01
1		Jumper Plug	21300021-01
2	JP2	Header, 1 x 4	21000009-01
1		Header, 1 x 2	21000007-01
1		Header, 1 x 2 Molex	21300027-01
1	XVR1	Heatsink, TO-3	76000003-01
1	XVR1	Heatsink Insulator	76000004-01
2		Screw, 6-32 x 3/8	28000006-01
2		Nut, 6-32 KEP	28100004-01
2		Board extractor	74000001-01
2		Roll pin	28300001-01
1		Cable Assy, 40 pin	60900022-01

A.2 USER-REPLACEABLE PARTS: 2832 BOARD 2

QTY	REF	DESCRIPTION	CCS PART #
Integrated Circuits			
1	VR1	78Ø5 +5 V regulator	48200109-Ø1
4	U2,1Ø,16,17	75114 dual diff drvr	48200123-Ø1
4	U3,9,14,15	74115 dual diff rcvr	48200124-Ø1
3	U4,5,7	7406/7416 hex inver, OC	48200048-Ø1
1	U6	74LS273 oct D flip-flop	48200037-Ø1
1	U8	74LS32 quad 2-in OR	48200013-Ø1
1	U12	74LS240 oct buff, inver	48200034-Ø1
1	U11	74LS175 quad D flip-fl	48200031-Ø1
2	U1,18	74LS244 octal buffer	48200035-Ø1
Capacitors			
12	C1-12	.1uf Mono, 5ØVDC, 20%	15900001-Ø1
2	C13,14	4.7uf Tant, 35VDC, 20%	15500003-Ø1
Resistors			
4	RP1-4	SIP Net, 15Ø ohm x 7	47400001-Ø1
Miscellaneous			
4	J1,2,5,6	Conn, 2 x 1Ø	21000025-Ø1
1	J3	Conn, 2 x 25	21000027-Ø1
1	J4	Conn, 2 x 2Ø	21000026-Ø1
1	XVR1	Heatsink, TO-22Ø	76000001-Ø1
1		Screw, 6-32 x 3/8	28000006-Ø1
1		Nut, 6-32 KEP	28100004-Ø1
2		Board extractor	74000001-Ø1
2		Roll pin	28300001-Ø1
1		Cable Assy, 5Ø pin A	60100009-Ø1
1		Cable Assy, 2Ø pin	60900001-Ø1

A.3 CABLE CONNECTOR PIN-OUTS

A.3.1 INTERBOARD CABLE

DD2	1	o	o	2	GND
DD3	3	o	o	4	GND
DD4	5	o	o	6	GND
DD5	7	o	o	8	GND
DD6	9	o	o	1Ø	GND
DD7	11	o	o	12	GND
RDDATA	13	o	o	14	GND
WGTE	15	o	o	16	GND
WRDATA	17	o	o	18	GND
INDEX	19	o	o	2Ø	GND
DD1	21	o	o	22	GND
DDØ	23	o	o	24	GND
SECTOR	25	o	o	26	GND
RGTE	27	o	o	28	GND
DATAIN*	29	o	o	3Ø	GND
PLOCLK	31	o	o	32	GND
DOUT*	33	o	o	34	GND
RSI*	35	o	o	36	GND
DSG*	37	o	o	38	GND
CMDG*	39	o	o	4Ø	GND

A.3.2 DRIVE Ø-3 CABLES

INDEX*	1	o	o	2	GND
RDY*	3	o	o	4	GND
SECTOR*	5	o	o	6	GND
SEEKCOM*	7	o	o	8	GND
WRDATA+	9	o	o	1Ø	WRDATA-
GND	11	o	o	12	WRCLK+
WRCLK-	13	o	o	14	GND
PLOCLK+	15	o	o	16	PLOCLK-
GND	17	o	o	18	RDDATA+
RDDATA-	19	o	o	2Ø	GND

A.3.3 A CABLE

GND	1	o	o	2	HSØ*
GND	3	o	o	4	HS1*
GND	5	o	o	6	HS2*
GND	7	o	o	8	HS3*
GND	9	o	o	1Ø	
GND	11	o	o	12	
GND	13	o	o	14	
GND	15	o	o	16	DSØ*
GND	17	o	o	18	DS1*
GND	19	o	o	2Ø	DS2*
GND	21	o	o	22	DS3*
GND	23	o	o	24	DIR*
GND	25	o	o	26	STEP*
GND	27	o	o	28	FLTCLR*
GND	29	o	o	3Ø	WGTE*
GND	31	o	o	32	TRKØ*
GND	33	o	o	34	WRTFLT*
GND	35	o	o	36	RGTE*
	37	o	o	38	
	39	o	o	4Ø	
	41	o	o	42	
	43	o	o	44	
	45	o	o	46	
	47	o	o	48	
	49	o	o	5Ø	

A.4 S-100 BUS CONNECTOR PINOUTS

+8V	1	o	o	51	+8V
	2	o	o	52	
	3	o	o	53	
VIO*	4	o	o	54	SLAVE CLR*
VI1*	5	o	o	55	DMA0*
VI2*	6	o	o	56	DMA1*
VI3*	7	o	o	57	DMA2*
VI4*	8	o	o	58	
VI5*	9	o	o	59	
VI6*	10	o	o	60	
VI7*	11	o	o	61	
	12	o	o	62	
	13	o	o	63	
DMA3*	14	o	o	64	
	15	o	o	65	
	16	o	o	66	
	17	o	o	67	
SDSB*	18	o	o	68	
CDSB*	19	o	o	69	
	20	o	o	70	
	21	o	o	71	
ADSB*	22	o	o	72	RDY*
DDSB*	23	o	o	73	INT*
o2	24	o	o	74	HOLD*
	25	o	o	75	RESET*
pHLDA	26	o	o	76	pSYNC
	27	o	o	77	pWR*
	28	o	o	78	pDBIN
A5	29	o	o	79	A0
A4	30	o	o	80	A1
A3	31	o	o	81	A2
A15	32	o	o	82	A6
A12	33	o	o	83	A7
A9	34	o	o	84	A8
DO1	35	o	o	85	A13
DO0	36	o	o	86	A14
A10	37	o	o	87	A11
DO4	38	o	o	88	DO2
DO5	39	o	o	89	DO3
DO6	40	o	o	90	DO7
DI2	41	o	o	91	DI4
DI3	42	o	o	92	DI5
DI7	43	o	o	93	DI6
sM1	44	o	o	94	DI1
sOUT	45	o	o	95	DI0
sINP	46	o	o	96	sINTA
sMEMR	47	o	o	97	sWO*
	48	o	o	98	
	49	o	o	99	
GND	50	o	o	100	GND

A.5 DRIVE BUS SIGNALS

A.5.1 CONTROL SIGNALS (Multiplexed)

SIGNAL NAME	DESCRIPTION
Drive Inputs	
HEAD SELECT Ø-3	These signals are used to select which head is active.
DRIVE SELECT 1-4	When active, a DRIVE SELECT line selects which of four drives is active.
STEP	Each pulse of this signal causes the head to be stepped one track.
DIRECTION	When active with STEP, this signal determines which direction the head steps. If DIRC is high, the head steps toward the center; if it is low, the head steps toward the perimeter.
FAULT CLEAR	The Write Fault Latch in the drive is reset by this signal.
WRITE GATE	This signal gates write current to the currently-selected head.
READ GATE	This signal allows the selected head to be read from.
Drive Outputs	
WRITE FAULT	When active, this signal usually indicates that WRITE GATE* occured inappropriately. It is active until reset by FAULT CLEAR.
TRACK Ø	This signal indicates that all heads of the currently-selected drive are positioned over Track ØØ.

A.5.2 READ/WRITE SIGNALS (Radial)

SIGNAL NAME	DESCRIPTION
Drive Inputs	
WRITE DATA	The write data is transmitted in the NRZ format using balanced transmission lines.
WRITE CLOCK	The write clock signal from the controller is synchronized with the write data internally to the drive.
Drive Outputs	
INDEX	This signal pulses low 1.7 us once every revolution of the disk.
READY	When active, this signal indicates the drive is up to speed and ready for disk operations
SECTOR	This signal pulses low 1.7 us for every sector. It does so by counting bytes and going active when the number of bytes per sector is reached.
READ DATA	The read data in NRZ format is transmitted synchronously with the PLO clock and over balance transmission lines.
PLO CLOCK	When READ GATE is false, PLO CLOCK is synchronized with signal from the clock track. When READ GATE is true, the PLO CLOCK is synchronized to READ DATA.
SEEK COMPLETE	When the head is positioned over the requested track, this signal is true.

APPENDIX B

SCHEMATICS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

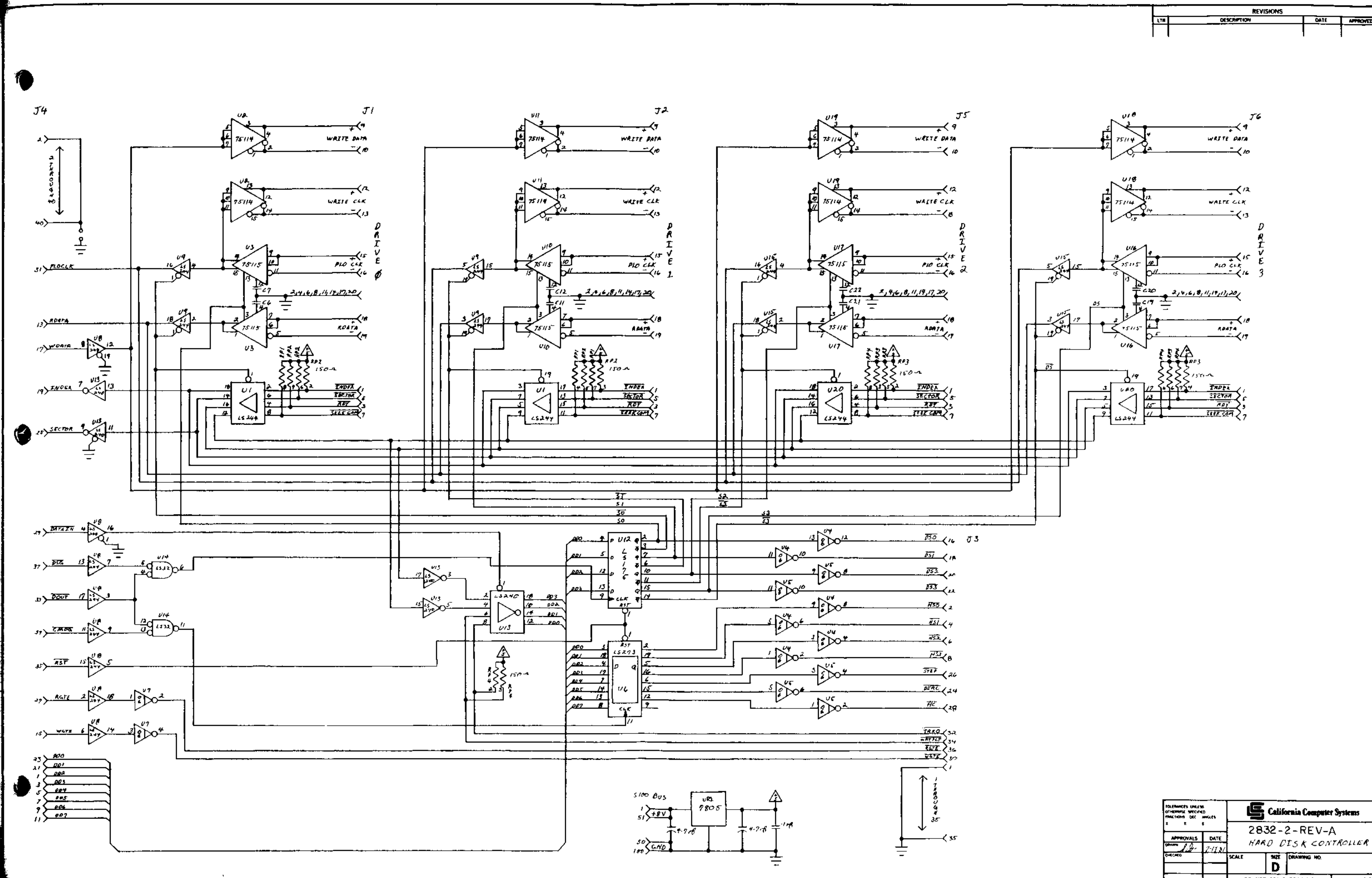
P1

P1

J4

J4

TOLERANCES UNLESS OTHERWISE SPECIFIED: FRACTIONS ±; DEC ±; ANGLES ±°	California Computer Systems
APPROVALS / DRAWN / CHECKED / DATE	2832-1-REV-A
	HARD DISK CONTROLLER
	SCALE / SIZE D / DRAWING NO
	DO NOT SCALE DRAWING / SHEET 1 of 2



California Computer Systems

2832-2-REV-A

HARD DISK CONTROLLER

SIZE D

DO NOT SCALE DRAWING

APPENDIX A

TECHNICAL INFORMATION

C.1.2 DRIVES

The Winchester drives used in the CCS System 400 are the Fujitsu 2301B two-platter or 2302B four-platter drives or equivalent drives from another manufacturer. These drives have unformatted capacities of 11.7 and 23.4 Megabytes respectively. The disks and heads operate in a sealed plastic enclosure, ensuring high reliability. No user maintenance is required.

A PC Board on the bottom of the drive includes several jumpers and switches which must be configured to match the system hardware and software. In factory-configured systems, the jumpers and switches are set for the system and should not be altered unless the operating system is changed or drives are added. Instructions are given in the System 300 and 400 User's Guide and in Section C.2 of this manual.

C.1.3 POWER SUPPLY

Each drive is served by a separate power supply designed specifically for Winchester-type disk drives: the Condor FNBB-120W or equivalent. Outputs of +24, +5, and -5 Volts are regulated to a .05% tolerance, with overvoltage protection for the 5 Volt outputs. The power supply also features short circuit and overload protection. Configuration of the power supply for either 115 or 230 Volts AC is done at the factory.

SPECIFICATIONS

AC INPUT	115/230 Volts + 10%, 47-440 Hz
DC OUTPUT	3.3 (5.5 Amps Peak) at +24 V. 7.0 Amps at +5 V. 1.2 Amps at -5 V.
REGULATION	±.05% for a 10% line change ±.05% for a 50% load change
OVERVOLTAGE PROTECTION	6.2 ±0.4 V
OUTPUT RIPPLE	3.0 mv PK-PK max, 0.4 mv RMS
TRANSIENT RESPONSE	30 usec for 50% load change
TEMPERATURE RATING	32 to 122 F. (0 to 50 C.)

C.1.4 SERVICE

If your drive subsystem should require service while under warranty, do not disassemble the unit and attempt to make repairs; doing so could void your warranty. Follow the instructions regarding service that accompany the CCS Limited Warranty card.

C.1.5 LOCK SWITCH

```
**************************************************************
*                                                            *
*  WARNING:   DO NOT TURN ON POWER TO THE DRIVES UNLESS YOU  *
*     ARE SURE THAT THE LOCK SWITCHES ARE SET TO "FREE".     *
*                                                            *
**************************************************************
```

Before powering on your hard disk drives, remove the front panel (it snaps on and off). At the lower edge of each drive you will see the end of a white plastic toggle switch. These are the Lock Switches. They should be in the leftmost position (LOCK) when the drive is received, and must be set to the rightmost (FREE) position before the drive is powered on. Turning on a drive with the switch in the LOCK position will damage the drive.

C.1.6 AIR FLOW

The fan at the back of the mainframe will keep the drives and power supplies cool as long as you let it. Always leave room for air flow in front of and behind the chassis, and vacuum the filter regularly (about once a month under normal conditions).

If you have a single-drive unit, make sure that air flow is blocked through the part of the grill in front of the empty half of the chassis; otherwise, most of the air will be drawn through the empty section and the drive may not be properly cooled.

C.1.7 CABLES

Each hard disk unit includes one 50-pin cable plus a 20-pin cable for each drive. Plug one end of the 50-pin cable into the top 50-pin connector at the back of the hard disk chassis. Plug one end of the 20-pin cable(s) into the appropriate 20-pin connector(s); the top connector is for Drive 0, and the bottom is for Drive 1. Be sure to match pin 1 marks (usually a V-shaped indentation on the connector molding). The other ends of the cables plug into the corresponding connectors at the back of the mainframe; see your Systems 300 and 400 User's Guide for the connector locations.

C.2 HARD DISK SUBSYSTEM EXPANSION

C.2.1 ADDING A SECOND DRIVE

Two-platter and four-platter Winchester drives are available from CCS, allowing the user to move easily from a single-drive to a double-drive subsystem. Included with each drive are a power supply with wiring harnesses, a drive mounting bracket, and mounting hardware. Consult the current CCS Systems Price List for the product numbers of the available kits.

To install a second drive in a single-drive unit, follow the procedures listed below.

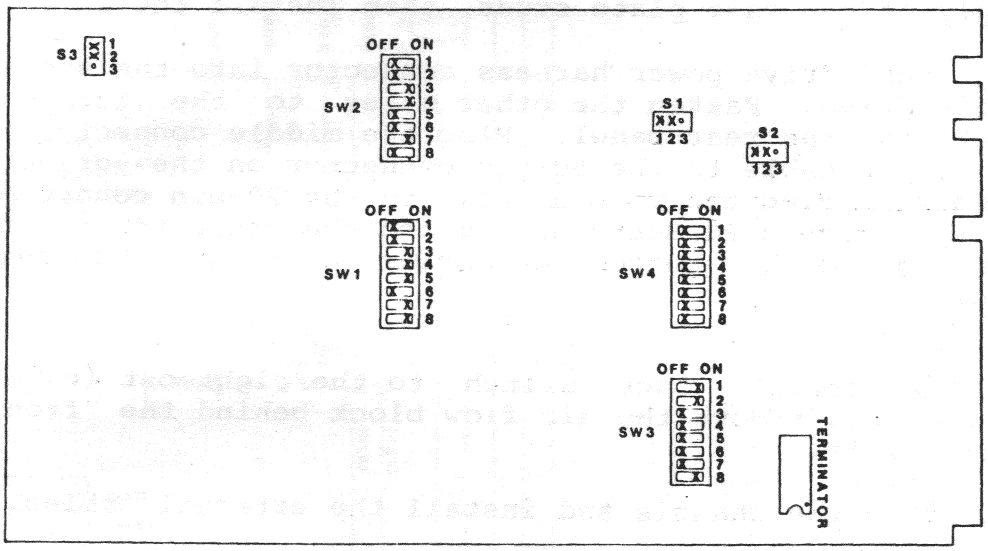
1. Before installing the drive, make sure that the PC Board is configured correctly. Except for switches SW2-7, SW2-8, SW3-5 through SW3-8, and termination, all drives are configured the same. Only Drive 0 should be terminated. Make certain that pins 1 and 2 of S1 are jumpered on all drives; if this jumper is not set correctly when the drive is powered on, the drive will be damaged. SW3-5 through SW3-8 are Drive Select Switches. Set one switch to ON to select the drive number; set the others to OFF.

SW3-8	DRIVE 0
SW3-7	DRIVE 1
SW3-6	DRIVE 2
SW3-5	DRIVE 3

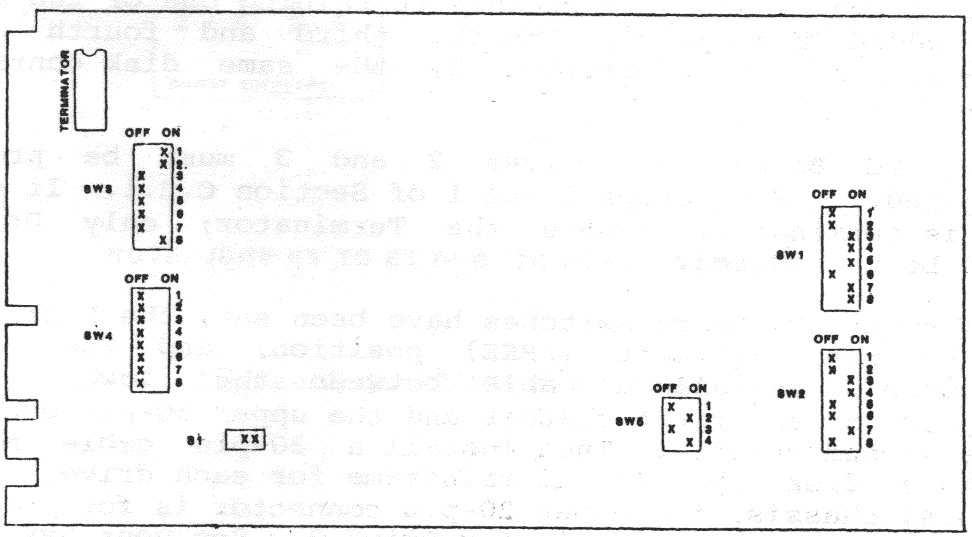
SW2-7 and SW2-8 select the sector size:

SW2-7 ON, SW2-8 OFF	512 bytes/sector (CP/M, MP/M)
SW2-7 OFF, SW2-8 ON	256 bytes/sector (OASIS)

Figure C-1 shows the settings for Drive 0 in a CP/M or MP/M system.



NON LSI-VERSION



LSI-VERSION

NOTE: REMOVE ALL TERMINATOR RESISTERS FROM ALL DRIVES EXCEPT THE LAST DRIVE CONNECTED TO THE 50 PIN CABLE

Figure C-1. DRIVE PC BOARD SWITCH AND JUMPER SETTINGS

2. Snap off the front panel. Remove the cover, which is secured by two screws at the front and four at the back.

3. When you are sure that the PC Board jumpers and switches are correctly set, mount the drive bracket and power supply on the base plate studs, then install the drive.

4. Plug the drive power harness connector into the socket on the drive. Fasten the other wires to the terminal block on the rear panel. Plug the middle connector on the 50-pin cable to the 50-pin connector on the drive's PC Board. Plug the 20-pin cable to the 20-pin connector on the drive's PC Board and fasten the connector at the other end to the bottom connector slot on the rear panel.

5. Set the drive's Lock Switch to the rightmost (FREE) position and remove the air flow block behind the front panel grille.

6. Reassemble the chassis and install the external cables.

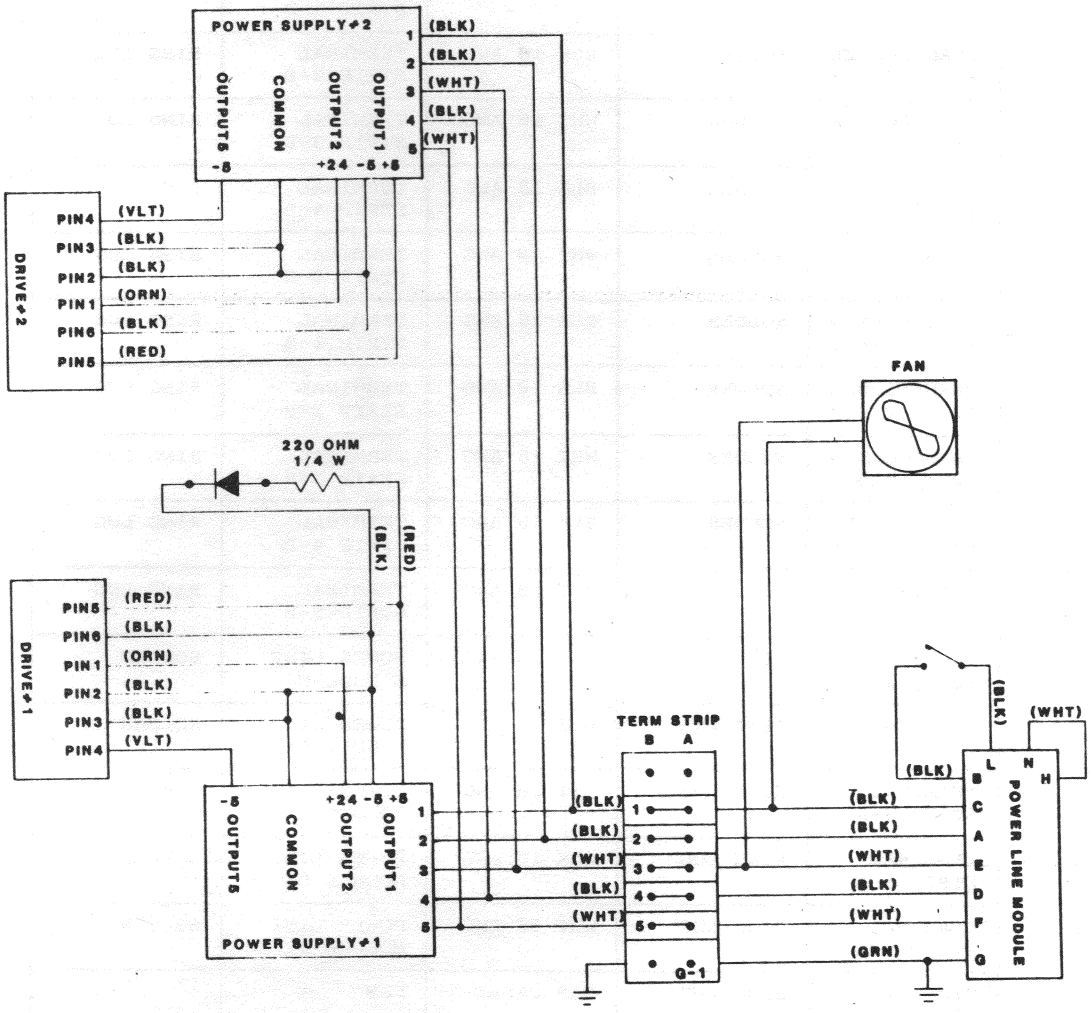
C.2.2 DAISY-CHAINING A SECOND DRIVE CHASSIS

A second hard disk chassis containing one or two drives can be added to a system, with the third and fourth drives daisy-chained and controlled by the same disk controller board.

The PC Boards of Drives 2 and 3 must be properly configured. See Steps 2 and 1 of Section C.2.1. If either drive is terminated, remove the Terminator; only Drive 0 should be terminated.

When the PC Board switches have been set, the Lock Switch set to the rightmost (FREE) position, and the chassis reassembled, install a cable between the lower 50-pin connector of the first chassis and the upper 50-pin connector of the second chassis. Then install a 20-pin cable between the hard disk chassis and mainframe for each drive. On the hard disk chassis, the upper 20-pin connector is for Drive 2 and the lower connector is for Drive 3. See your System 300 and 400 User's Guide for locations of the mainframe connectors.

C.2.3 WIRING INFORMATION



NOTE: JUMP E1 TO E2 IN BOTH POWER SUPPLIES

Figure C-2. WIRING DIAGRAM

Table C-1. WIRING CHART

FROM	TERMINATION	DESCRIPTION	TO	TERMINATION
TRANSFORMER #1 TAB 1	SOLDER	BLK 18 AWG	TERMINAL STRIP 1-B	RING LUG
TRANSFORMER #1 TAB 2	SOLDER	BLK 18 AWG	TERMINAL STRIP 2-B	RING LUG
TRANSFORMER #1 TAB 3	SOLDER	WHT 18 AWG	TERMINAL STRIP 3-B	RING LUG
TRANSFORMER #1 TAB 4	SOLDER	BLK 18 AWG	TERMINAL STRIP 4-B	RING LUG
TRANSFORMER #1 TAB 5	SOLDER	WHT 18 AWG	TERMINAL STRIP 5-B	RING LUG
TRANSFORMER #2 TAB 1	SOLDER	BLK 18 AWG	TERMINAL STRIP 1-B	RING LUG
TRANSFORMER #2 TAB 2	SOLDER	BLK 18 AWG	TERMINAL STRIP 2-B	RING LUG
TRANSFORMER #2 TAB 3	SOLDER	WHT 18 AWG	TERMINAL STRIP 3-B	RING LUG
TRANSFORMER #2 TAB 4	SOLDER	BLK 18 AWG	TERMINAL STRIP 4-B	RING LUG
TRANSFORMER #2 TAB 5	SOLDER	WHT 18 AWG	TERMINAL STRIP 5-B	RING LUG
TERMINAL STRIP 1-A	RING LUG	BLK 18 AWG	POWER LINE MODULE C	SOLDER
TERMINAL STRIP 2-A	RING LUG	BLK 18 AWG	POWER LINE MODULE A	SOLDER
TERMINAL STRIP 3-A	RING LUG	WHT 18 AWG	POWER LINE MODULE E	SOLDER
TERMINAL STRIP 4-A	RING LUG	BLK 18 AWG	POWER LINE MODULE D	SOLDER
TERMINAL STRIP 5-A	RING LUG	WHT 18 AWG	POWER LINE MODULE F	SOLDER
TERMINAL STRIP 1-A	RING LUG	FAN CABLE	FAN	
TERMINAL STRIP 3-A	RING LUG	FAN CABLE	FAN	
POWER LINE MODULE B	SOLDER	BLK 18 AWG	SWITCH CB-1	SLIP-ON
POWER LINE MODULE L	SOLDER	BLK 18 AWG	SWITCH CB-2	SLIP-ON
POWER LINE MODULE N	SOLDER	WHT 18 AWG	POWER LINE MODULE H	SOLDER
POWER LINE MODULE G	SOLDER	GRN 18 AWG	TERMINAL STRIP G-1	RING LUG