Model 2830
6 CHANNEL SERIAL I/O

Reference Manual

California Computer Systems

42000080-01 Rev. A

MODIFIED TO USE PIN 25 (Φ2) RATHER THAN PIN 24 (Φ1) DUE TO 2810 CLOCK PHASE. ALSO MODIFIED TO PICK UP BAUD RATE CLOCK FROM BUS PIN 70 SUPPLIED BY 2719 CTC CHANNEL 2

CCS MODEL 2830

SIX CHANNEL SERIAL I/O

Reference Manual

California Computer Systems
250 Caribbean Drive
Sunnyvale CA 94086

The information contained in this manual is believed to be correct at the time of publication. However, CCS assumes no liability resulting from the use of this publication.

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CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The CCS Model 2830 Six Channel Serial I/O Board employs three Z-80 DARTs (Dual Asynchronous Receiver/Transmitters) and a Z-80 CTC to provide six programmable serial ports with programmable baud rates. Designed to conform to the IEEE 696/D2 specifications for the S-100 bus, the 2830 also features a unique Z-80 Mode 2 Interrupt Daisy Chain look-ahead scheme which significantly reduces the ripple time for long daisy chains, alleviating the need for wait states during Interrupt Acknowledge cycles. The base address of the CTC and the three DARTs is hardware-selectable at any multiple of 16 between 0 and 255. The serial port interfaces, configured for DCE but easily reconfigured for DTE, meet EIA RS-232-C specifications.

1.2 USING THIS MANUAL

This manual is intended to provide information required by a variety of users in a variety of situations; most users will not find it necessary to read the entire manual. Chapter 2 deals with board configuration, and all users should consult this chapter. Chapter 3 discusses the 2830-unique programming requirements of the DARTs and CTC. Chapter 4 is a detailed discussion of the hardware design of the 2830, and is intended to be read in conjunction with frequent references to the Schematic/Logic Diagram in Appendix A. Various technical illustrations and tables are provided in Appendix A.

1.3 SPECIFICATIONS

I/O INTERFACES:

Three Z-8Ø DARTs Provide Six
Asynchronous Serial Ports
Meets EIA RS-232-C Specifications,
Full or Partial Primary Channel
DARTs Replaceable with SIO/Øs for
Synchronous Operation
Jumper-Enabled Handshake Options:
RS-232-C Lines 8, 11, 19
Easy DCE-to-DTE Reconfiguration
Programmable Baud Rates (Z-8Ø CTC)

SYSTEM INTERFACE:

S-1ØØ: Complies with IEEE Task 696.1/D2,
SLAVE AI F6 T3ØØ
Supports Z-8Ø Mode Ø, 1, & 2 Interrupts
Supports IEEE/696 Use of VI* Lines in
CCS-Unique Fast Interrupt Daisy Chain
Look-Ahead Scheme
Jumper-Selectable Board Base Address
Full Buffering of Bus-Driving Outputs,
Schmitt-Trigger Bus Receiver Inputs

POWER:

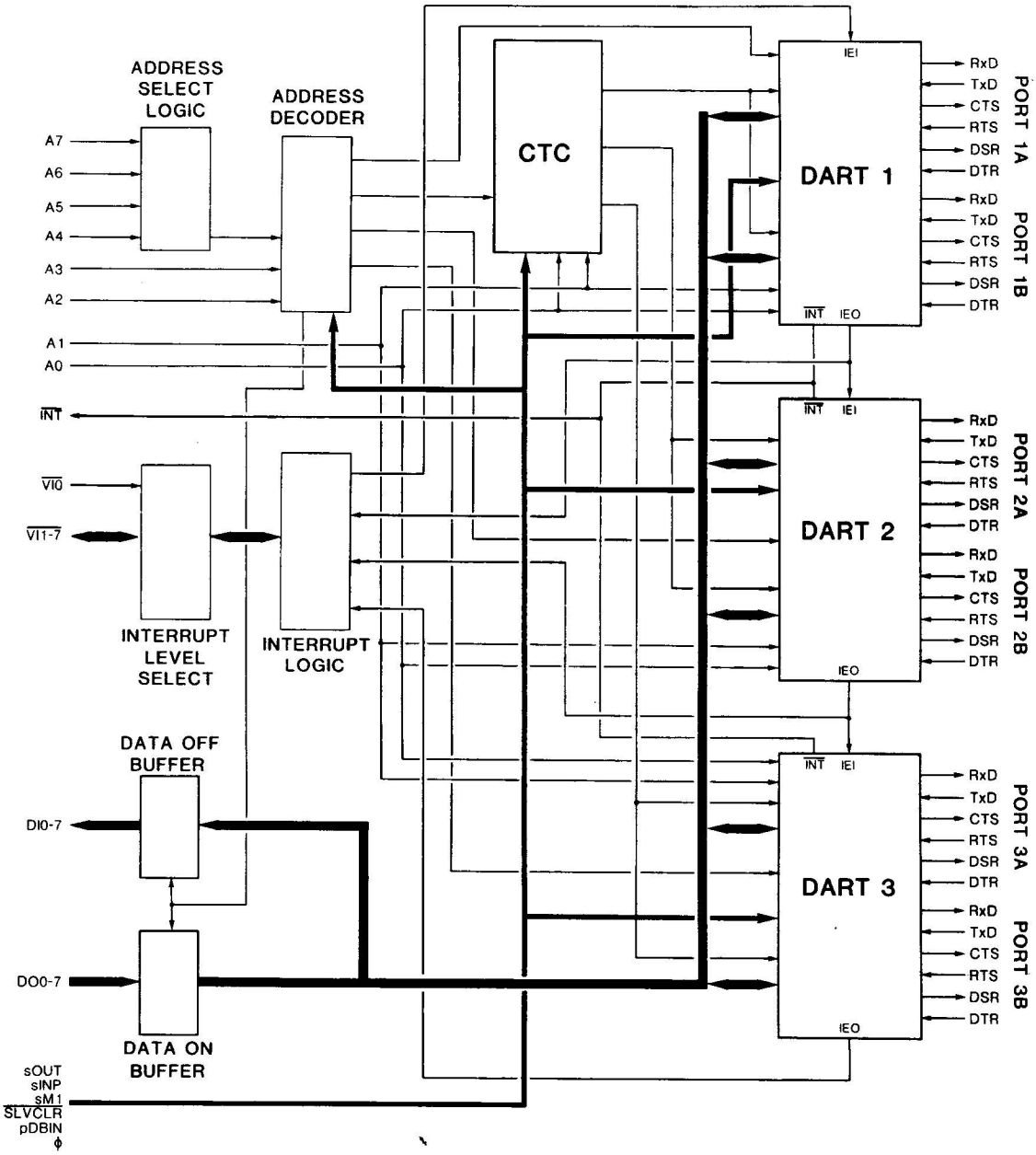
+8 Volts Regulated On-Board to +5 Volts
+16 Volts Regulated On-Board to +12 Volts
-16 Volts Regulated On-Board to -12 Volts

Consumption:	.5Ø Amps at +8 Volts
	.Ø5 Amps at +16 Volts
	.Ø5 Amps at -16 Volts
Heat Burden:	81 gram-calories/minute
	.34 BTU/minute

ENVIRONMENTAL REQUIREMENTS:

Temperature:	Ø to +7Ø C. (32 to 155 F.)
Humidity:	Up to 9Ø% Non-Condensing

1.4 2830 BLOCK DIAGRAM



CHAPTER 2

CONFIGURING THE 2830

Several user-configurable options exist on the 2830: base address, port interface configuration, baud rate source, interrupt priority level, and interface protective ground. Protective ground for the port interfaces requires user-implementation in all systems in which terminals are to be connected to a different power source than the mainframe (including different wall outlets in the same building). When used in the System 200/300/400 in standard configuration, only the protective ground option need be configured. However, in customized systems reconfiguration may be necessary. Instructions are provided in this chapter. Locations of the jumpers and headers on the 2830 are shown in Figure 2-1.

2.1 INSTALLING THE 2830 IN A SYSTEM 200/300/400

To install the 2830 in a CCS System 200/300/400, follow these step-by-step instructions:

1. Ensure that the Port Address Select Jumpers are set to 20H.

2. If you desire an interrupt priority level other than level 2, reconfigure the Interrupt Priority Header as described in Section 2.3.

3. Six I/O cables are supplied with the board. Connect one for each port you plan to bring up, making sure that the triangular pin 1 marks on the board and cable connectors match. See Figure 2-1 for port/connector correspondences.

4. Configure the Protective Ground, if required, as described in Section 2.6.

5. Install the board in the mainframe. For optimum performance, install the boards in adjacent slots in the following order: System Processor, Memory, Fast I/O (Disk Controllers), Slow I/O (including 2830), Termination. ALWAYS POWER DOWN THE SYSTEM BEFORE INSTALLING OR REMOVING BOARDS.

6. Fasten the I/O cable RS-232-C connectors to the back of the mainframe.

7. Install the appropriate cables between the mainframe and your peripherals. For instructions on setting up your peripheral, see your System User's Guide.

2.2 THE PORT ADDRESS SELECT JUMPERS

The settings of these jumpers select the base address of the CTC and I/O ports at any multiple of 16 (10H). These jumpers are set at the factory for a base address of 20H, which is the base address required by the CCS system software packages; thus the first 2830 used in a CCS System 300 or 400 should be left in the factory configuration. When the 2830 is used in other situations, however, a different base address may be desired. (Be sure that any other port address selected does not conflict with other port assignments in the system.) Consult Table 2-1 for the jumper settings for all possible base addresses.

Table 3-3 shows the relative addresses of the CTC Channels and DART data and command/status ports.

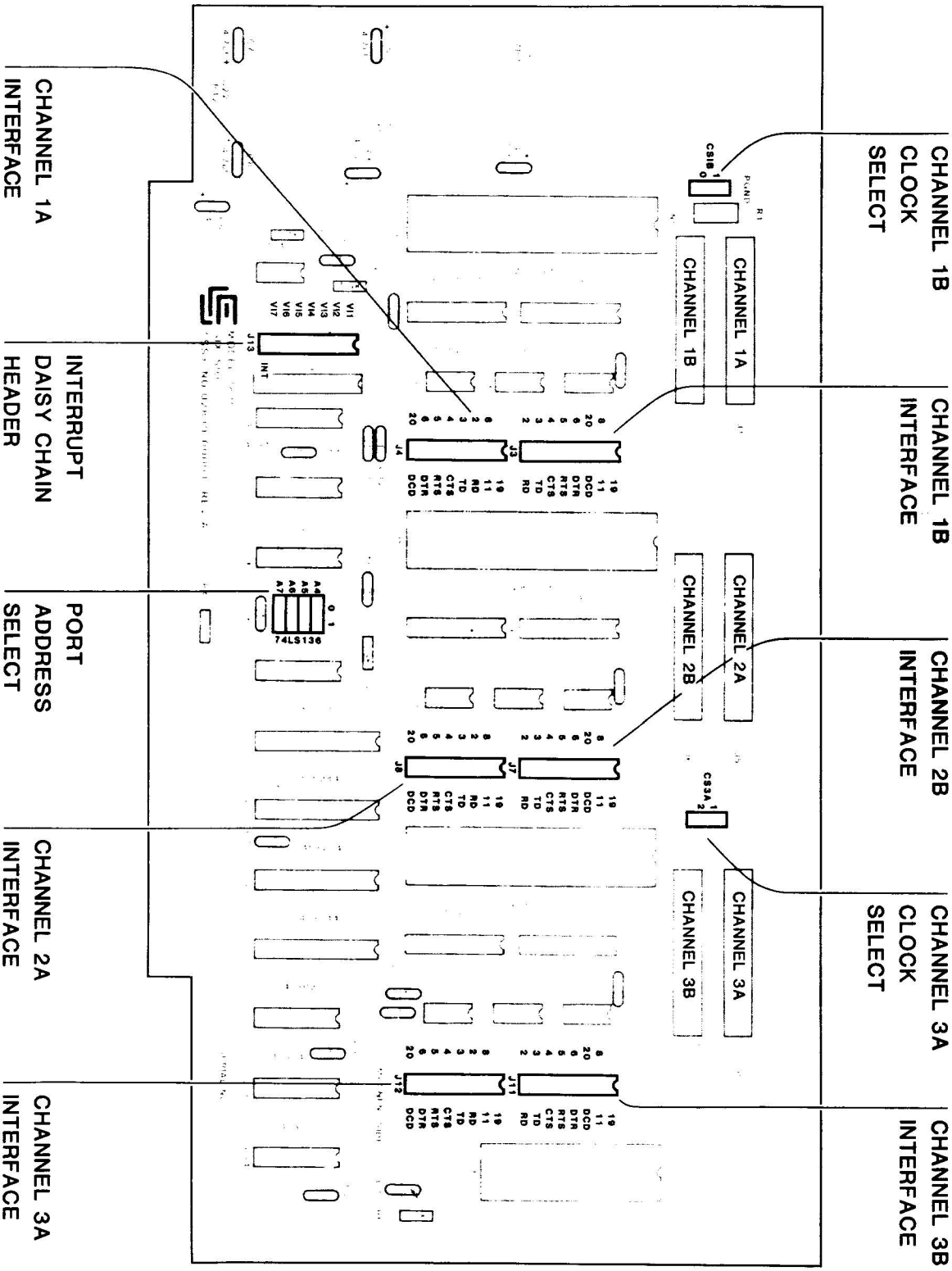


FIGURE 2-1. 2830 JUMPER LOCATIONS

TABLE 2-1. PORT BASE ADDRESSES

JUMPER SETTINGS				BASE	
A7	A6	A5	A4	HEX.	DEC.
0	0	0	0	00	00
0	0	0	1	10	16
0	0	1	0	20	32
0	0	1	1	30	48
0	1	0	0	40	64
0	1	0	1	50	80
0	1	1	0	60	96
0	1	1	1	70	112
1	0	0	0	80	128
1	0	0	1	90	144
1	0	1	0	A0	160
1	0	1	1	B0	176
1	1	0	0	C0	192
1	1	0	1	D0	208
1	1	1	0	E0	224
1	1	1	1	F0	240

FIGURE 2-2. INTERRUPT HEADER

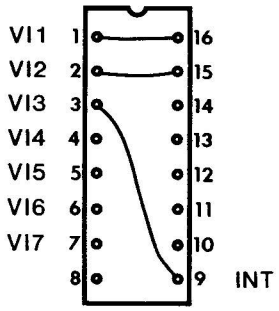
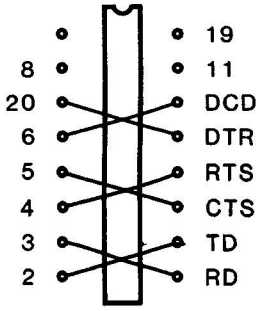


FIGURE 2-3. INTERFACE JUMPERS



2.3 THE INTERRUPT DAISY CHAIN HEADER

2.3.1 STANDARD CONFIGURATION

System 200/300/400 interrupt priorities may be determined at the system implementer's discretion, depending on system components and application. However, the priority scheme shown below is followed in the factory configuration of the interrupt priority headers for each system board, and should be appropriate for the majority of systems. The System Processor is hardwired for Level 0; it is the only board whose priority is fixed.

Level 0: 2820 System Processor
Level 1: 2805 Clock/ROM/Terminator
Level 2: 2830 Six-Channel Serial I/O
Level 3: 2 Parallel/2 Serial I/O
Level 4: 2831 Arithmetic Processor
Level 5: GPIB Interface
Level 6: 2832 Hard Disk Controller
Level 7: 2822 Floppy Disk Controller

Note that gaps are allowed in the priority structure; thus, it is not necessary to reconfigure a level 3 board to level 2 if there is no level 2 board in the system. However, no priority level may be occupied by more than one board. Header reconfiguration will be required if two of the same board are installed in a system. Priority swapping can be accomplished by swapping header plugs, except in the case of the 2832, which has a slightly different header configuration. For example, to put the 2830 at level 3 and the 2818 at level 2, simply exchange the header plugs supplied with the boards.

2.3.2 RECONFIGURATION

A Z-80 Mode 2 Interrupt Daisy Chain, when extended beyond four peripheral devices, requires look-ahead logic to ensure that all devices are properly informed of higher-priority interrupts within the allotted time. CCS Systems 200, 300, and 400 implement a unique look-ahead scheme in which: 1) each board participating in the daisy chain asserts its interrupt priority by forcing a given Vectored Interrupt bus line low; and 2) a board is prevented from interrupting when a lower-numbered VI* line is low. Thus there are nine interrupt priority levels, 0-8; the priority 0 board controls VI0* and senses no lines, while the priority 8 board senses all VI* lines and controls none. The Interrupt Daisy Chain Header, illustrated in Figure 2-2, allows the user to select the interrupt priority level (1-8) of the 2830 by selecting which VI* line(s) the board will be sensitive to and which VI* line it will pull low when an on-board device requests an interrupt.

To configure the header:

1. Tie the pins corresponding to higher-priority (lower-numbered) VI* lines straight across (pin 1 to pin 16, pin 2 to pin 15, etc);

2. Tie the pin corresponding to the 2830's priority-assertion line to the INT pin (pin 9);

3. Leave unconnected all lower-priority VI pins.

Note that the highest priority level to which the 2830 may be assigned is 1. The board is hardwired to sense the VI0* line, which is reserved as the 2820 System Processor's priority-assertion line. Figure 2-2 shows the header configured for interrupt priority level 3.

2.4 SERIAL PORT INTERFACE JUMPERS

The Serial Port Interfaces are hardwired for the DCE configuration (board emulates a modem), but may be reconfigured for DTE (board emulates a terminal). To re-configure, first cut the existing traces which connect the pads straight across (on the component side of the board). Jumper wires may be soldered directly to the jumper pads, but we recommend that you install a 16-pin DIP header with cover. On the header plug, install jumper wires so that pins 3-14 are connected crosswise, as illustrated in Figure 2-3.

Some terminal devices, notably printers, use lines other than RTS, CTS, DTR, and DSR for handshaking. To ensure compatibility with these devices, we have provided pins allowing RS-232-C lines 8 (RLSD), 11 (Unassigned), and 19 (SRTS) to be jumpered to replace other handshake lines as required. Consult your peripheral manual to determine handshaking requirements.

2.5 THE CLOCK SELECT JUMPERS

In the standard configuration, baud rates for DARTs 1, 2, and 3 are determined by CTC Channels Ø, 1, and 2 respectively. The Clock Select 1B and 3A jumper pads allow the user to select CTC Channel 1 as the baud rate source for DART Channel 1B and/or DART Channel 3A. This frees DART Channels 1A and 3B for independent or variable baud rate applications (e.g., use with a modem requiring 11Ø, 3ØØ, and 12ØØ baud at different times). To select Channel 1 as the baud rate source for either DART Channel 1B or DART Channel 3A, cut the trace between the pair of pads labeled Ø (jumper CS1B) or 2 (jumper CS3A) and install a jumper wire between the pair of pads labeled 1.

2.6 PROTECTIVE GROUND

Protective Ground is defined as the supply current return path, not a signal current return path. It is intended to equalize the voltage potential of the terminal and the mainframe, and should be implemented whenever the terminal and the mainframe are connected to different power sources which may have different ground potentials. If all terminals interfaced through the 283Ø are to be connected to the same outlet as the mainframe, the protective ground feature need not be implemented.

Next to the CS1B jumper pads are two jumper pads labeled PGND and SGND. These allow the user to select one of two implementations of the RS-232-C interface Protective Ground signals for all ports. The recommended implementation is to run a green wire from the PGND pad to the mainframe chassis, with an alligator clip or other convenient method for connection. This conforms to the RS-232 design specifications, ensuring that terminal and mainframe have the same potentials. Use this method with CCS-supplied terminals. Some terminals, however, tie Protective Ground and Signal Ground together or use the protective ground as the signal ground. If you are using such a terminal with the 283Ø, you will need to install a 1ØØ ohm, 1/4 Watt resistor (as per EIA standard RS-422-A) between the PGND and SGND pads.

CHAPTER 3

PROGRAMMING INFORMATION

Programming options for the Z-8Ø DART and CTC are quite elaborate. Complete instructions are given in the Z-8Ø Family Programming Guide included in CCS Systems documentation packages. Users of the 283Ø who do not own a copy of the CCS Programming Guide may order a copy or find equivalent programming instructions in a variety of publications, a few of which are listed below. This chapter deals with programming limitations and requirements stemming from the implementation of the Z-8Ø DART and CTC on the 283Ø.

AN INTRODUCTION TO MICROCOMPUTERS, Osborne and Associates, Inc. (Berkeley, CA: 1978).
ZILOG MICRCOMPUTER COMPONENTS DATA BOOK, Zilog, Inc. (Cupertino, CA: 198Ø).
MOSTEK MICROCOMPUTER DATA BOOK, Mostek Corporation (Carollton, TX: 1979).
SGS Z-8Ø MICROCOMPUTER SYSTEM, SGS-ATES Componenti Elettronici SpA (Agrate Brianza, Italy: 1981).

3.1 DART 283Ø-UNIQUE PROGRAMMING CHARACTERISTICS

Table 3-1 shows which DART pins are connected to which RS-232-C lines. The programmer should keep in mind that commmand and status bits in the programming guide are named for the DART pin and not the RS-232-C interface line--for example, the RTS command bit actually controls the CTS interface line when the board is in the standard DCE configuration.

TABLE 3-1. DART/RS-232-C INTERFACING

DART PIN	DART SIGNAL	RS-232-C PIN	RS-232-C SIGNAL
15/26	TxD	3	RD (BB)
12/28	RxD	2	TD (BA)
17/24	RTS	5	CTS (CB)
18/23	CTS	4	RTS (CA)
16/25	DTR	6	DSR (CC)
19/22	DCD	20	DTR (CD)

Programming limitations of the DARTs are few and stem from the fact that some inputs and outputs are not connected: specifically, W/RDYA*, W/RDYB*, RIA*, and RIB*. The specific limitations are listed below.

1. Bit 7 of Command Register 1 (Wait/Ready Enable) should be Ø. Bits 6 and 5 are don't-care bits.

2. Bit 4 of Status Register Ø will always be low. This will not affect External Status Interrupts.

3. Bits 7-6 of Command Register 4 should be programmed as required for the desired baud rate, as indicated in Table 3-2.

3.2 CTC 283Ø-UNIQUE PROGRAMMING CHARACTERISTICS

The CTC on the 283Ø provides programmable clock signals for the DARTs. In the factory configuration, Channel Ø provides the clocks for Ports 1A and 1B, Channel 1 provides the clocks for Ports 2A and 2B, and Channel 2 provides the clocks for Ports 3A and 3B. Channel 3, which has no output, can be used only as a readable real-time clock, the contents of a channel's downcounter being available to the CPU at the channel address. In the factory configuration the address of CTC Channel 3 is 23H.

The specific programming requirements for the CTC on the 283Ø are listed below.

1. The CTC INT*, IEI, and IEO pins are unconnected. Therefore, the Interrupt Vector Register need never be programmed. Command

Register Bit 7 should be Ø to disable interrupts.

2. Channels Ø-2 may be programmed in either the counter mode (2 MHz clock) or the timer mode (4 MHz clock and prescaler of 16 or 64). See Table 3-2 for the programming options for common baud rates. In the CCS System 3ØØ and 4ØØ software, the CTC is programmed in the counter mode.

3.3 PROGRAMMING BAUD RATES

Because of the counter/timer and prescaler options of the CTC and the data rate option of the DART, the CTC/DART combination allows for a wide range of possible baud rates. In some cases there are two or more ways to program the CTC and DART for a given baud rate. Table 3-2 shows all of the programming options for commonly used baud rates.

TABLE 3.2. PROGRAMMING CTC AND SIO/DART FOR SELECTED BAUD RATES

	TIME CONSTANTS						
BAUD RATE	P=1 DR=16*	P=16 DR=1	P=16 DR=16*	P=16 DR=32*	P=16 DR=64*	P=256 DR=1	P=256 DR=16*
50				156	78		
75			208	104	52	208	13
110			142	71		142	
134.5			116	58	29	116	
150			104	52	26	104	
300			52	26	13	52	
600	208		26	13		26	
1200	104	208	13			13	
1800	69	139					
2000	62	125					
2400	52	104					
3600	35	69					
4800	26	52					
7200	17	35					
9600	13	26					
19200		13					

P Prescaler programmed for CTC. If P=1, then the CTC is in the counter mode, clocked by the 2 MHz signal.
DR Data Rate programmed for SIO or DART.
* Available in Async Mode only.

3.4 PORT RELATIVE ADDRESSES

The base address of the 16 ports occupied by the 2830 is selected by the user as described in Chapter 2, but within the 16-port block the relative addresses of the ports are fixed. Table 3-3 shows the relative addresses of the CTC channels and the DART data and command/status ports. The port addresses for the standard configuration of the board when used in a CCS System 300/400 are given in parentheses.

TABLE 3-3. PORT RELATIVE ADDRESSES

CTC	CHANNEL 0 Base (20H)	CHANNEL 1 Base+1 (21H)	CHANNEL 2 Base+2 (22H)	CHANNEL 3 Base+3 (23H)
DART 1	A DATA Base+4 (24H)	A COMMAND Base+5 (25H)	B DATA Base+6 (26H)	B COMMAND Base+7 (27H)
DART 2	A DATA Base+8 (28H)	A COMMAND Base+9 (29H)	B DATA Base+10 (2AH)	B COMMAND Base+11 (2BH)
DART 3	A DATA Base+12 (2CH)	A COMMAND Base+13 (2DH)	B DATA Base+14 (2EH)	B COMMAND Base+15 (2FH)

CHAPTER 4

HARDWARE DESIGN

The 2830 is a software-intensive board. A wide range of capabilities are provided with relatively simple hardware. Three DARTs and a CTC form the heart of the board, providing six asynchronous serial I/O ports with semi-independent programmable baud rates. Additional hardware performs three basic functions: address decoding, bus and interface line buffering, and interrupt daisy chain implementation. The DARTs, the CTC, and the three basic support functions are discussed individually below.

This chapter is intended to be read in conjunction with frequent references to the Schematic/Logic Diagram in Appendix A.

4.1 THE DART

Each Z-80 Dual Asynchronous Receiver/Transmitter provides two extensively programmable asynchronous serial ports capable of serial-to-parallel and parallel-to-serial data conversions in a variety of formats. Such options as word length, parity type or inhibition, interrupt conditions and vector, clock divisor, and stop bit length are under program control. Details of the programming capabilities of the DART are given in the System 200, 300, and 400 Z-80 Family Programming Reference Manual.

DART interfaces are configured for the DART as DCE (Data Communications Equipment), but may be reconfigured for the DART as DTE at the user's discretion; instructions are given in Chapter 2. RS-232-C lines supported by each port include Protective and Signal Grounds, TxD, RxD, CTS, RTS,

DSR, and DTR. Because the DART pins are named assuming that the DART is used as DTE, the RS-232-C lines and the DART pins are oppositely labeled when the DART is used as DCE; see Table 3-1.

Table 4-1 identifies the DART inputs and outputs. RIA*, RIB*, W/RDYA*, and W/RDYB* are unconnected.

4.2 THE CTC

The Z80 Counter/Timer Circuit consists of four separately-programmed channels, each of which can operate in either the timer or the counter mode. In either mode a value programmed into a channel's Time Constant Register is loaded into a downcounter which decrements until it reaches zero, at which point the channel's ZC/TO output pulses high (Channels 0-2 only), an interrupt is generated (this capability is not supported by the 2830 hardware), and the downcounter is reloaded with the Time Constant. The difference between timer mode and counter mode is in the method of decrementing the downcounter. In the timer mode, the downcounter decrements with every 16 or 64 cycles of the system clock (depending on the prescaler selected). In the counter mode, the downcounter decrements with every cycle of the CLK/TRG input, which on the 2830 is controlled by the 2 MHz clock.

The CTC is implemented on the 2830 as a baud rate generator. Channels 0-2 provide 512 different clock rates for each DART in a range wide enough to allow the programming of all common baud rates. Channel 3 is not used and is accessible to the programmer only as a polled-access real-time clock; there is no output from Channel 3 and the CTC's interrupt request output is not connected. Table 3-2 shows how the prescaler and time constant can be programmed to produce common baud rates.

CTC inputs and outputs are described in Table 4-2. ZC/TO outputs 0-3 control all transmitter and receiver clock inputs for DARTs 1, 2, and 3 respectively unless jumper options are implemented (see Section 2.4). All CLK/TRG inputs are controlled by the 2 MHz clock.

TABLE 4-1. DART SIGNALS

SIGNAL	FUNCTION
CE* DØ-7 IORQ* M1* RD*	See Table 4-2 for definitions of these signals.
B/A*	This input, controlled by AØ, determines whether Channel A or Channel B is selected.
C/D*	This input, controlled by A1, determines whether a control or data transfer will occur.
TxDA TxDB	Serial data at TTL levels is output to interface lines RxD.
RxDA RxDB	Serial data at TTL levels is input at these pins via the TxD interface lines.
CTSA* CTSB*	The Clear To Send inputs, connected to the RTS RS-232-C lines, may be programmed as transmitter auto-enable or general-purpose signals.
RTSA* RTSB*	The Request to Send handshaking outputs are connected to the CTS RS-232-C lines.
DCDA* DCDB*	The Data Carrier Detect inputs, connected to the DTR RS-232-C lines, may be programmed as receiver auto-enable or general purpose inputs.
DTRA* DTRB*	The Data Terminal Ready handshaking outputs are connected to the DSR RS-232-C lines.
RIA* RIB*	These pins are not connected on the 2830.
RxCA TxCA RxTxCB	The Channel A and Channel B clocks are controlled by one CTC channel unless jumpered otherwise.
RESET*	A low at this pin resets both DART channels.
CLK	This is the DART's system clock input.
INT* IEI IEO	See Section 4.4 for a discussion of these interrupt daisy chain signals.

TABLE 4-2. CTC SIGNALS

SIGNAL	FUNCTION
CE*	Chip Enable is controlled by the address decode circuitry.
RD*	The Read input determines the direction of data transfer.
IORQ*	The I/O Request input enables data transfer.
M1*	Both M1* and IORQ* low indicates an Interrupt Acknowledge cycle.
CSØ,CS1	The Channel Select inputs select one of four CTC channels. They are controlled by AØ-A1.
CLK/TRG Ø-3	The Clock/Trigger inputs control downcounter decrementing in counter mode. All are controlled by the 2 MHz clock (bus pin 49).
ZC/TO Ø-2	The Zero Count/Timeout pins pulse high when the downcounters reach zero. They control the DART receiver and transmitter clocks.
DØ-7	The bi-directional data pins connect directly to the 2719 internal data bus.
RESET*	Reset low terminates downcounting, disables interrupts, and tri-states DØ-D7.
CLK	This is the CTC's system clock input.
INT* IEI IEO	See Section 4.4 for a discussion of these interrupt daisy chain signals.

4.3 ADDRESS DECODING

The four Z-8Ø peripheral devices on board the 283Ø occupy a block of 16 port addresses whose base is a multiple of 16. The base address is selected by the user with four jumper plugs. These plugs determine whether a high or a low signal is Ex-ORed with each of the bus lines A7-A4. When each of A7-A4 is in the state opposite of that selected by the corresponding jumper, the outputs of the four open-collector Ex-OR gates are all high. The Ex-OR outputs are tied together to control the E (Enable) input of the 3-to-8 Device Select Decoder. The decoder has two other Enable inputs, both active low; the conditions of all three enable inputs must be met for the decoder to be enabled. One of the E* inputs is tied to ground. The other is active when either sINP or sOUT is active--i.e., during I/O read or I/O write cycles. Thus, when A7-A4 address the jumper-selected 16-port block during an I/O cycle the Device Select Decoder is enabled.

Each Z-8Ø device on board--CTC or DART--occupies four port addresses. The Device Select Decoder, used as a 2-to-4 decoder, decodes bus lines A3 and A2 to force one of four outputs low. Each of the four outputs is tied to the CE (Chip Enable) input of one of the Z-8Ø devices, so that whenever the Device Select Decoder is enabled one of the Z-8Ø devices is enabled. The enabled device then decodes A1 and AØ to determine which channel or port is addressed.

4.4 INTERRUPT DAISY CHAIN LOGIC

The 283Ø supports the Z-8Ø Mode 2 Interrupt Daisy Chain as implemented by CCS Systems 2ØØ, 3ØØ, and 4ØØ. (Mode 2 interrupts are discussed in detail in the 282Ø Reference Manual and in the Z-8Ø Family Programming Reference Manual.) The Vectored Interrupt bus lines are used to prioritize the boards participating in the chain. Each board must include look-ahead logic that guarantees that an interrupt request by an on-board device or by a device on a higher-priority board will be passed on to lower-priority boards rapidly enough to be recognized by lower-priority devices before the interrupt is acknowledged; otherwise, two devices might put their interrupt vectors on the bus at the same time.

If an on-board interrupt occurs, the DART(s) having lower priority than the interrupting DART are prevented from interrupting by the normal chip-to-chip IEI-IEO daisy chain,

the interrupt-disable message rippling through the individual chips (input IEI low forcing output IEO low) from high priority to low. An interrupt by a higher-priority board does not ripple through the DARTs, however; each DART's interrupt request logic is immediately disabled when the 2830 interrupt logic senses any higher-priority VI* line going low, thereby significantly reducing response time. In addition, whenever an on-board DART interrupts or the 2830 senses a higher-priority VI* line low, the 2830 forces its priority-assertion VI* line low.

The particular VI* lines the 2830 senses and the VI* line it asserts are determined by the configuration of the Interrupt Daisy Chain Header; see Section 2.2. The 2820 System Processor is always the highest priority (0), but the 2830 can be configured for any other priority from 1 to 8. As shipped from the factory, it is configured for priority level 1.

4.5 BUFFERING

All system bus inputs and outputs are fully buffered, as are the RS-232-C interface lines. Hysteresis drivers and receivers are used for system bus interfacing, ensuring minimum noise on the bus. No load of more than one Low-Power Schottky TTL level is placed on any system bus input. INT* and lower-priority VI* line drivers are open-collector. Port interface drivers and receivers meet EIA RS-232-C specifications.

Except for the Data In and Data Out Buffers, all buffers are permanently enabled. The Data In and Data Out Buffers are alternately tri-stated. Basically, the Data In Buffer is tri-stated and the Data Out Buffer enabled: 1) when the board is addressed during an I/O Read cycle; or 2) during an Interrupt Acknowledge cycle when the 2830 is the highest-priority board requesting an interrupt. At all other times the Data Out Buffer is tri-stated and the Data In Buffer is enabled.

When a device's interrupt has been blocked by the interrupt of a higher-priority device, the lower-priority device monitors the data bus during all instruction fetches, looking for the RETI instruction which signals that servicing of the higher-priority interrupt has been completed and that lower-priority interrupts may now be asserted. To ensure proper monitoring of the CPU instruction fetches by the 2830, the CPU must internally

connect the DI and DO buses. This is necessary because, while the RETI instruction is input to the CPU on the DI lines, the 2830 looks for RETI on the DO lines. The CCS 2820 System Processor Board meets this requirement as long as no peripheral or memory board asserts DODSB during instruction fetch cycles.

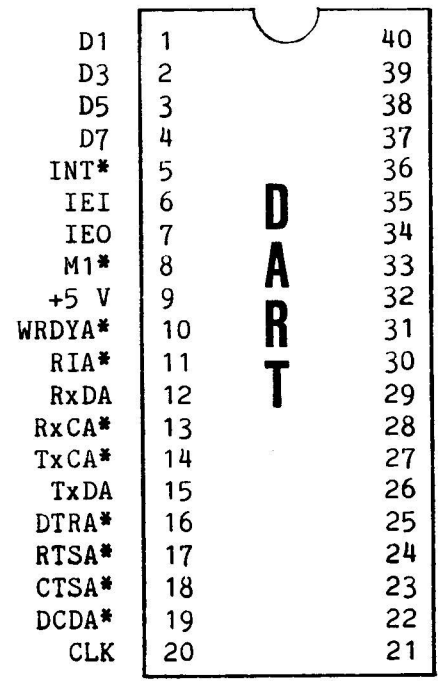
APPENDIX A

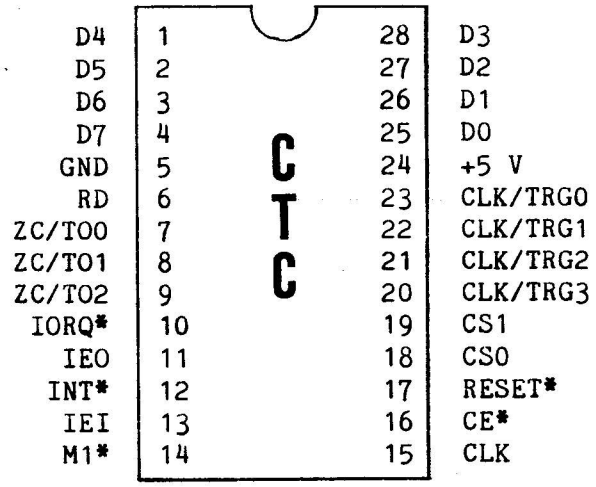
TECHNICAL INFORMATION

A.1 USER-REPLACEABLE PARTS

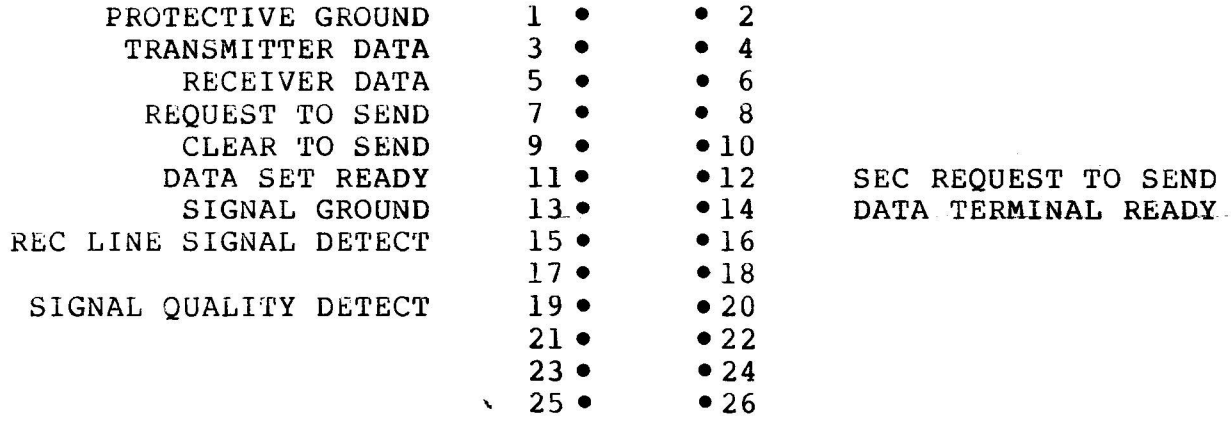
QTY	REF	DESCRIPTION	CCS PART #
Integrated Circuits			
3	U1,5,9	Z-80 DART	48200119-01
5	U2,6,10,16,18	75154 line receiver	48200056-01
9	U3,4,7,8,11,12, 17,19,21	75150 line driver	48200055-01
1	U13	Z-80 CTC	48200084-01
1	U14	7805 +5 V regulator	48200109-01
1	U15	7912 -12 V regulator	48200115-01
1	U20	74LS138 3-to-8 decoder	48200022-01
1	U22	7812 +12 V regulator	48200113-01
1	U23	75453 dual OR driver	48200059-01
1	U24	74LS13 dual 4-in NAND	48200120-01
1	U25	74LS30 8-in NAND	48200012-01
1	U26	74LS08 quad 2-in AND	48200006-01
1	U27	74LS136 quad EX-OR	48200021-01
4	U28-31	74LS244 octal buffers	48200035-01
1	U32	74LS02 quad 2-in NOR	48200002-01
1	U33	74LS04 hex inverters	48200004-01
1	U34	74LS00 quad 2-in NAND	48200001-01
Capacitors			
16	C1-3,10-22	.1uf Mono, 50VDC, 20%	15900001-01
6	C4-9	4.7uf Tant, 35VDC, 20%	15500003-01
Resistors			
1	R2	2.7K ohm, 1/4 Watt, 5%	47000023-01
4	R3-6	1K ohm, 1/4 Watt, 5%	47000003-01
1	RP1	SIP Network, 2.7K x 7	47400002-01
Sockets			
1	XJ13	16 pin DIP	21400015-01
1	XU13	28 pin DIP	21400019-01
3	XU1,5,9	40 pin DIP	21400020-01
Miscellaneous			
6	J1,2,5,6,9,10	Conn, 2 x 13 rt angle	21000005-01
1	J13	Header, 2 x 8	21600001-01
1		Header cover, 2 x 8	14100001-01
1		Header, 2 x 4	21000023-01
4		Header, 1 x 4	21000009-01
4		Jumper shorting plugs	21300021-01
1	XU14	Heatsink, TO-220	76000001-01
3	XU14,15,22	Screw, 6-32 x 3/8	28000006-01
3	XU14,15,22	Nut, 6-32 KEP	28100004-01
2		Board extractor	74000001-01
2		Roll pin	28300001-01
6		Cable, RS-232-C	60900007-01

A.2 DART AND CTC PINOUTS

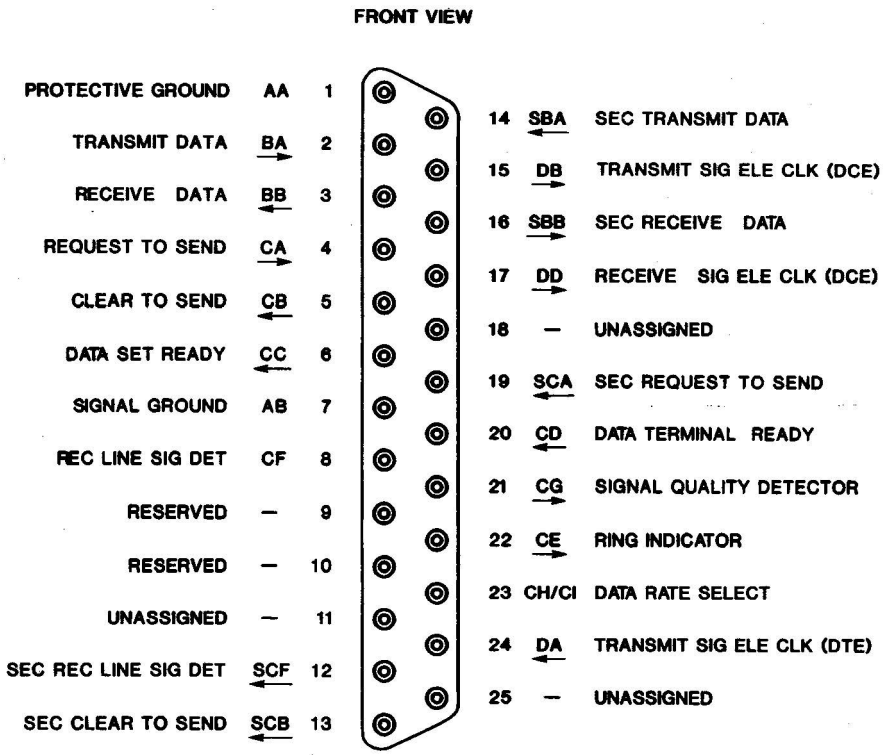




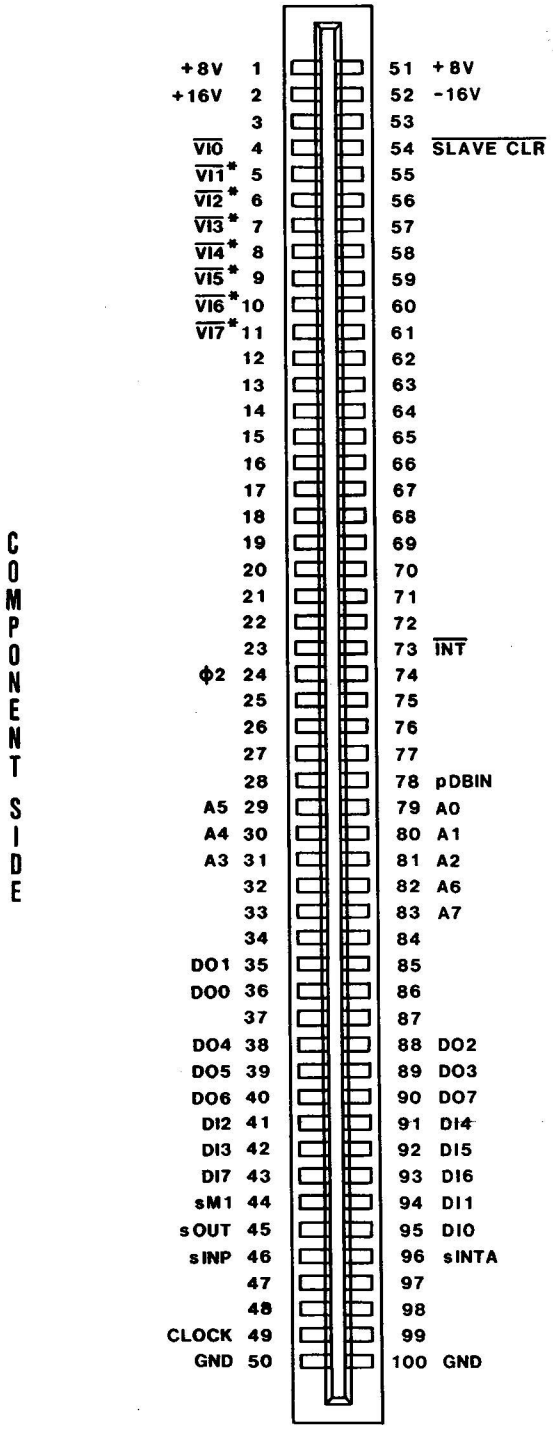
A.3 ON-BOARD INTERFACE CONNECTOR PINOUTS



A.4 RS-232-C CONNECTOR PINOUTS



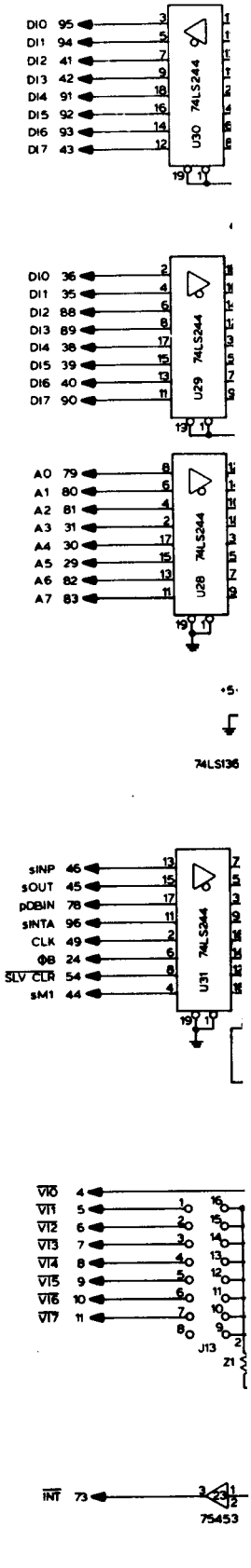
A.5 BUS CONNECTOR PINOUTS



TOP VIEW

*Jumper-enabled signals

A.6 SCHEMATIC/LOGIC DIAGRAM



MODEL 2830
SIX SIO
©CCS 1981
REV A

DIO 95
DI1 94
DI2 41
DI3 42
DI4 91
DI5 92
DI6 93
DI7 43
U30 74LS244
DIO 36
DI1 35
DI2 88
DI3 89
DI4 38
DI5 39
DI6 40
DI7 90
U29 74LS244
A0 79
A1 80
A2 81
A3 31
A4 30
A5 29
A6 82
A7 83
U26 74LS244
sINP 46
sOUT 45
pDBIN 78
sINTA 96
CLK 49
ΦB 24
SLV CLR 54
sM1 44
U31 74LS244
U20 74LS138
U13 Z80A-CTC
U1 Z80A DART
U5 Z80A DART
U9 Z80A DART
74LS00
74LS02
74LS04
74LS08
74LS30
74LS136
74LS13
75453
75154
75150
R1 1K
R2 2.7K
R3 1K
R4 1K
R5 1K
R6 1K
C10 .1uf
C15 .1uf
C21 .1uf
CS1B
CS3A
INT 73

J2
1 AA (1) PROTECTIVE GROUND
12 SCA (19) SECONDARY REQUEST TO SEND
13 AB (7) SIGNAL GROUND
11 CC (6) DATA SET READY
14 CD (20) DATA TERMINAL READY
9 CB (5) CLEAR TO SEND
7 CA (4) REQUEST TO SEND
5 BB (3) RECEIVE DATA
3 BA (2) TRANSMIT DATA
21 NDEF
15 CF (8) RECEIVE LINE SIGNAL DETECT

J1
1 AA (1)
12 SCA (19)
13 AB (7)
11 CC (6)
14 CD (20)
9 CB (5)
7 CA (4)
5 BB (3)
3 BA (2)
21 NDEF
15 CF (8)

J6
1 AA (1)
12 SCA (19)
13 AB (7)
11 CC (6)
14 CD (20)
9 CB (5)
7 CA (4)
5 BB (3)
3 BA (2)
21 NDEF
15 CF (8)

J5
1 AA (1)
12 SCA (19)
13 AB (7)
11 CC (6)
14 CD (20)
9 CB (5)
7 CA (4)
5 BB (3)
3 BA (2)
21 NDEF
15 CF (8)

J10
1 AA (1)
12 SCA (19)
13 AB (7)
11 CC (6)
14 CD (20)
9 CB (5)
7 CA (4)
5 BB (3)
3 BA (2)
21 NDEF
15 CF (8)

J9
1 AA (1) PROTECTIVE GROUND
12 SCA (19) SECONDARY REQUEST TO SEND
13 AB (7) SIGNAL GROUND
11 CC (6) DATA SET READY
14 CD (20) DATA TERMINAL READY
9 CB (5) CLEAR TO SEND
7 CA (4) REQUST TO SEND
5 BB (3) RECEIVE DATA
3 BA (2) TRANSMIT DATA
21 NDEF
15 CF (8) RECEIVE LINE SIGNAL DETECT