000831

# MODEL 2805
# WALLCLOCK/TERMINATOR

## Reference Manual

California Computer Systems

42000089-01 Rev. A

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# CCS MODEL 2805

# WALLCLOCK/TERMINATOR

## Reference Manual


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# CHAPTER 1

# INTRODUCTION

## 1.1 GENERAL DESCRIPTION

The CCS Model 2805 provides three distinct functions for CCS Systems 200/300/400: a clock/calendar, circuitry for a user-supplied 2K ROM, and bus termination. The clock/calendar counts both date, including day of the week, and time, which is programmable for either a 24-hour or 12-hour (AM/PM) format. Two 1.5 Volt batteries ensure accurate timekeeping by the clock/calendar when the system is powered down. The base address of the clock (interfaced through a Z-80 PIO) may be jumpered to any multiple of 8 between 0 and 255.

The ROM is not presently implemented on the 2805 as shipped from the factory but may be implemented by the user if desired. Reset Glide circuitry, if jumper-enabled, causes the ROM to be the first memory accessed after power-up or reset, no matter where it resides. In addition, the ROM can be turned on and off through software. Whenever the ROM is active, PHANTOM* is forced low to disable other memory sharing the same address. The base address of the ROM may be jumpered to any 2K boundary within 64K.

Designed to conform to the IEEE 696/D2 specifications for the S-100 bus, the 2805 supports the unique Z-80 Mode 2 Interrupt Daisy Chain Look-Ahead Scheme featured in CCS Systems 200/300/400. Bus inputs and outputs are fully buffered, with no more than one Low-Power Schottky load on each input. In addition, the 2805 terminates all necessary bus signals.

## 1.2 USING THIS MANUAL

This manual is intended primarily as a reference for programmers, troubleshooters, and system integraters. Chapter 2 deals with board configuration, and should be consulted before the 28Ø5 is installed in a system. Chapter 3, intended for programmers who wish to write their own drivers for the 28Ø5, provides complete instructions for programming the clock through the PIO. Also included in Chapter 3 is a discussion of possible ROM implementations. Chapter 4, which deals with the hardware design of the 28Ø5, should be read in conjunction with frequent references to the Schematic/Logic Diagram in Appendix A. Appendix A consists of various technical illustrations and tables.

Throughout this manual, low-active signals are indicated by an asterisk after the signal name/mnemonic (e.g., pWR*) or by a bar over the name/mnemonic.

## 1.3 SPECIFICATIONS

| | |
|---|---|
| CLOCK FEATURES: | Counts Seconds, Minutes, Hours, Days of Week and Month, Months, and Years<br>12-Hour (AM/PM) or 24-Hour Format<br>Automatic Adjustment for Leap Year<br>Z-80 Mode 2 Interrupt Capability<br>Jumper-Selectable Base Address<br>Addressable Reference Pulses for Periodic Interrupt Request Generation<br>Crystal-Controlled Clock Input Frequency<br>Battery Back-Up to Maintain Timekeeping When System Is Powered Down<br>Clock Write Protect Switch |
| ROM FEATURES: | Circuitry for 2716 2-Kilobyte EPROM or Equivalent (Not Included)<br>Jumper-Selectable Base Address<br>Automatic Glide to Base Address on Reset<br>PHANTOM* Asserted to Disable System Memory<br>Software On/Off Switch<br>ROM, Reset Glide Disable Jumpers |
| TERMINATION: | Passive Termination of CCS System Bus Lines<br>1K Ohm Pull-Up to Tri-Stated Signals<br>330/390 Ohm Pull-Up to Open-Collector Signals |
| SYSTEM INTERFACE: | S-100: Complies with IEEE Task 696.1/D2<br>Supports Z-80 Mode 2 Interrupts<br>Supports CCS System 200/300/400 Fast Interrupt Daisy Chain Look-Ahead<br>Full Buffering of Inputs and Outputs |
| POWER: | Consumption: .90 Amps at +8 Volts<br>Dissipation: 105 Gram-Calories/Minute<br>.45 BTU/Minute<br>(Divide by 3 If Termination Removed) |
| ENVIRONMENTAL: | Temperature: 0 to 70 C. (32 to 155 F.)<br>Humidity: Up to 90%, Non-Condensing |

# CHAPTER 2

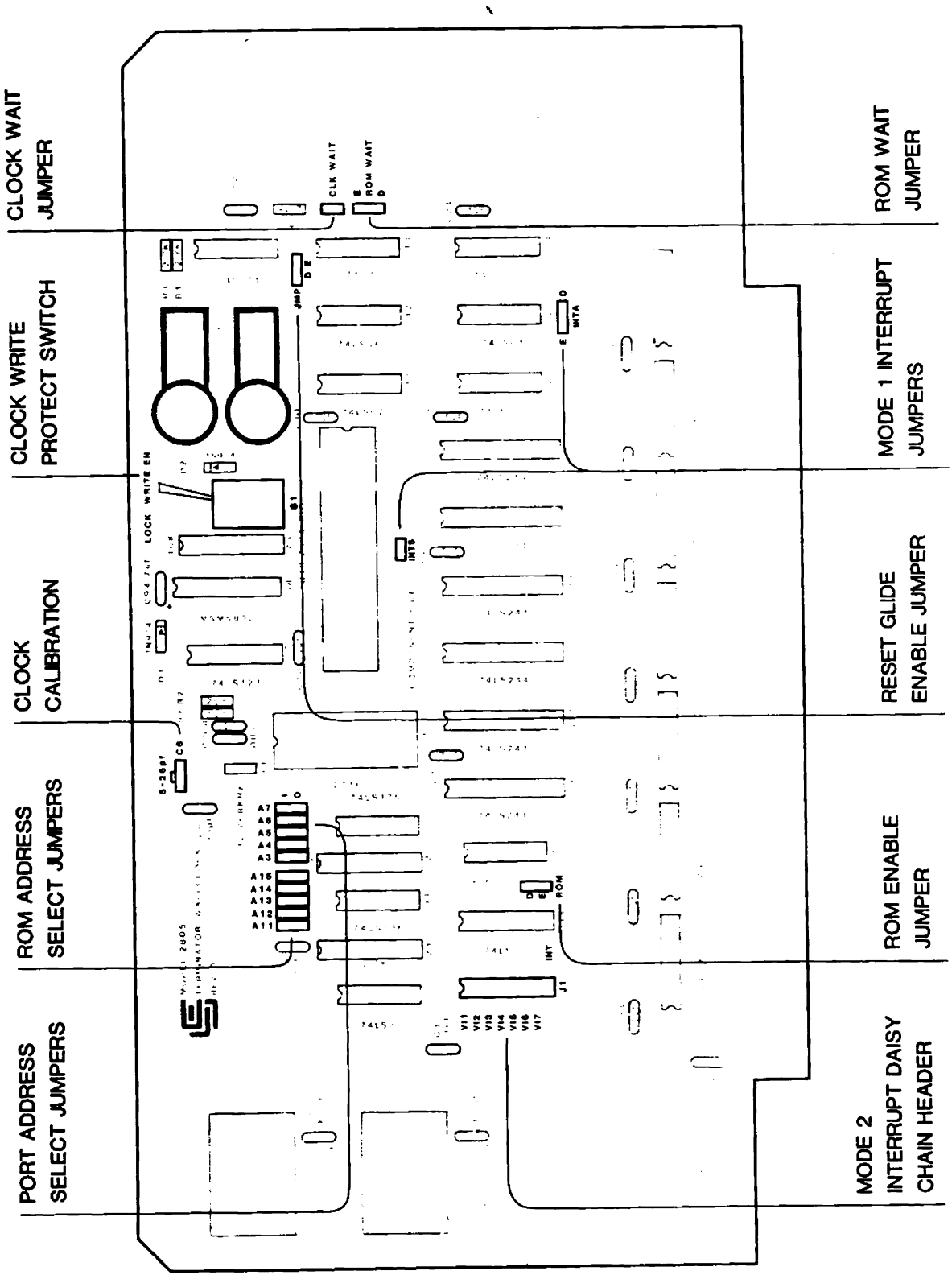
# CONFIGURING THE 2805

The 2805 features several user-configurable options: Boot ROM and Clock base addresses, Mode 2 interrupt priority level, ROM disabling, Reset Glide disabling, Mode 1 interrupts, clock write-protection, and separate RDY-forced waits when the clock or ROM are addressed. The base addresses, ROM enabling, and Reset Glide enabling are selected using shorting plugs, while the interrupt priority level is determined by the wiring of a DIP header. Wait states and Mode 1 interrupts may be implemented with the installation of jumper wires. Clock write-protection is controlled by a toggle switch. Locations of user options on the 2805 are shown in Figure 2-1. Each option is discussed individually in the sections that follow. Instructions for obtaining and installing batteries, adjusting the clock input frequency, and disabling duplicate termination are also included in this chapter.

## 2.1 CONFIGURING FOR CCS SYSTEMS 200/300/400

As shipped from the factory, the 2805 is configured as fully as possible for use in a CCS System 200/300/400. The I/O and ROM base addresses are set to 38H and F000H respectively, as required by the system software. If the board is sold as part of a factory-integrated system, the Interrupt Priority Header will be configured for level 1; otherwise the header is shipped unconfigured. The ROM Enable and Reset Glide Enable Jumpers are set to the Enable positions. Wait states are not implemented. Batteries are included.

FIGURE 2-1. 2805 USER OPTIONS



## 2.2 INSTALLATION

Always turn off power to the system before installing any board. For best operation, boards should be installed in consecutive slots in the following order: CPU, memory, fast I/O (disk controllers), slow I/O, terminator. Thus the 28Ø5 should be the board farthest from the CPU. If the system already has termination, remove it when you install the 28Ø5, or remove the terminating resistors from the 28Ø5.

## 2.3 WRITE SWITCH

The toggle switch at the top of the board allows write-protection of the clock. The clock may be written to only when this switch is in the WRITE EN position. Writing to the clock is necessary only when the time or date is inaccurate and needs to be reset; once the clock has been set to the proper date and time, there should be no need to write to it. To protect against accidental writes, flip the switch to the LOCK position once you have set the clock.

## 2.4 CLOCK CALIBRATION

All 28Ø5 clocks are checked for accuracy at the factory, but shipping vibrations may in some cases cause a board to be slightly fast or slow when first brought up. Should you find that the board loses or gains time (from a few seconds up to a minute or two in 24 hours), you will need to adjust the variable capacitor C6, which fine-tunes the crystal-controlled clock frequency. DO NOT ADJUST C6 UNLESS YOU HAVE DETERMINED THAT YOUR CLOCK IS KEEPING INACCURATE TIME.

C6 also allows you to correct for another possible cause of diminished accuracy: crystal aging. Over the years, crystals undergo a very slight but detectable change in frequency. Since the 28Ø5 should give years of service, sometime in the future a minor adjustment of C6 will probably be necessary.

Most users who find that their calendar/clock modules need calibration will have to use the adjust-a-little-and-check-the-results method. After determining the amount of time gained or lost per 24 hours, insert a small screwdriver blade into the slot at the top end of C6 and adjust slightly;

a small adjustment can have a significant effect on the clock rate. Wait long enough to determine the effect of the first adjustment, then readjust accordingly. Continue this process until you achieve the accuracy you desire.

For those who have access to a six-digit frequency counter, there is a better way to calibrate the clock. Program the clock to output reference signals (see Chapter 3 for instructions) and monitor pin 9 of U8. Adjust C6 as required so that the frequency of the wave at pin 9 is 1Ø24.ØØ +-.Ø1 Hz.

## 2.5 BATTERIES

The 28Ø5 wallclock will not continue timekeeping when the system is powered down unless two 1.5 Volt batteries are installed. Acceptable, readily-available batteries include:

| | |
|---|---|
| Eveready | E675 |
| Mallory | M675 |
| Burgess | Hg-675 |

To install a battery, loosen the screw that holds the clip, slide the clip to the side, place the battery in the cup with the button side up, slide the clip back over the battery, and tighten the screw.

## 2.6 USER-SELECTABLE OPTIONS

### 2.6.1 THE PORT ADDRESS SELECT JUMPERS

These jumpers, which determine the states of the signals compared with A7, A6, A5, A4, and A3, allow the user to assign the 28Ø5 to any block of eight I/O ports whose base is a multiple of 8. If address bits A7-A3 match the jumper settings, either the PIO is selected (A2=1) or the ROM Software Switch is clocked (A2=Ø, write cycles only). Consult Table 2-1 for the correct jumper settings for all possible port base addresses. Be sure that selected base addresses do not conflict with address assignments for other boards in the system.

### 2.6.2 THE ROM ADDRESS SELECT JUMPERS

These jumpers, which determine the states of signals compared with A15, A14, A13, A12, and A11, allow the user to address the Boot ROM at any 2K boundary within the 64K address space. If address bits A15-A11 match the jumper settings, the ROM is enabled. A1Ø-AØ address one of the 2K locations in the ROM. Consult Table 2-2 for the correct jumper settings for all possible ROM base addresses.

TABLE 2-1. PORT ADDRESSES

| JUMPER SETTINGS | | | | | BASE PORT | |
|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | HEX | DEC |
| 0 | 0 | 0 | 0 | 0 | 00 | 0 |
| 0 | 0 | 0 | 0 | 1 | 08 | 8 |
| 0 | 0 | 0 | 1 | 0 | 10 | 16 |
| 0 | 0 | 0 | 1 | 1 | 18 | 24 |
| 0 | 0 | 1 | 0 | 0 | 20 | 32 |
| 0 | 0 | 1 | 0 | 1 | 28 | 40 |
| 0 | 0 | 1 | 1 | 0 | 30 | 48 |
| 0 | 0 | 1 | 1 | 1 | 38 | 56 |
| 0 | 1 | 0 | 0 | 0 | 40 | 64 |
| 0 | 1 | 0 | 0 | 1 | 48 | 72 |
| 0 | 1 | 0 | 1 | 0 | 50 | 80 |
| 0 | 1 | 0 | 1 | 1 | 58 | 88 |
| 0 | 1 | 1 | 0 | 0 | 60 | 96 |
| 0 | 1 | 1 | 0 | 1 | 68 | 104 |
| 0 | 1 | 1 | 1 | 0 | 70 | 112 |
| 0 | 1 | 1 | 1 | 1 | 78 | 120 |
| 1 | 0 | 0 | 0 | 0 | 80 | 128 |
| 1 | 0 | 0 | 0 | 1 | 88 | 136 |
| 1 | 0 | 0 | 1 | 0 | 90 | 144 |
| 1 | 0 | 0 | 1 | 1 | 98 | 152 |
| 1 | 0 | 1 | 0 | 0 | A0 | 160 |
| 1 | 0 | 1 | 0 | 1 | A8 | 168 |
| 1 | 0 | 1 | 1 | 0 | B0 | 176 |
| 1 | 0 | 1 | 1 | 1 | B8 | 184 |
| 1 | 1 | 0 | 0 | 0 | C0 | 192 |
| 1 | 1 | 0 | 0 | 1 | C8 | 200 |
| 1 | 1 | 0 | 1 | 0 | D0 | 208 |
| 1 | 1 | 0 | 1 | 1 | D8 | 216 |
| 1 | 1 | 1 | 0 | 0 | E0 | 224 |
| 1 | 1 | 1 | 0 | 1 | E8 | 232 |
| 1 | 1 | 1 | 1 | 0 | F0 | 240 |
| 1 | 1 | 1 | 1 | 1 | F8 | 248 |

TABLE 2-2. ROM ADDRESSES

| JUMPER SETTINGS | | | | | BASE ADDR | |
|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | A11 | HEX | DEC |
| 0 | 0 | 0 | 0 | 0 | 0000 | 0K |
| 0 | 0 | 0 | 0 | 1 | 0800 | 2K |
| 0 | 0 | 0 | 1 | 0 | 1000 | 4K |
| 0 | 0 | 0 | 1 | 1 | 1800 | 6K |
| 0 | 0 | 1 | 0 | 0 | 2000 | 8K |
| 0 | 0 | 1 | 0 | 1 | 2800 | 10K |
| 0 | 0 | 1 | 1 | 0 | 3000 | 12K |
| 0 | 0 | 1 | 1 | 1 | 3800 | 14K |
| 0 | 1 | 0 | 0 | 0 | 4000 | 16K |
| 0 | 1 | 0 | 0 | 1 | 4800 | 18K |
| 0 | 1 | 0 | 1 | 0 | 5000 | 20K |
| 0 | 1 | 0 | 1 | 1 | 5800 | 22K |
| 0 | 1 | 1 | 0 | 0 | 6000 | 24K |
| 0 | 1 | 1 | 0 | 1 | 6800 | 26K |
| 0 | 1 | 1 | 1 | 0 | 7000 | 28K |
| 0 | 1 | 1 | 1 | 1 | 7800 | 30K |
| 1 | 0 | 0 | 0 | 0 | 8000 | 32K |
| 1 | 0 | 0 | 0 | 1 | 8800 | 34K |
| 1 | 0 | 0 | 1 | 0 | 9000 | 36K |
| 1 | 0 | 0 | 1 | 1 | 9800 | 38K |
| 1 | 0 | 1 | 0 | 0 | A000 | 40K |
| 1 | 0 | 1 | 0 | 1 | A800 | 42K |
| 1 | 0 | 1 | 1 | 0 | B000 | 44K |
| 1 | 0 | 1 | 1 | 1 | B800 | 46K |
| 1 | 1 | 0 | 0 | 0 | C000 | 48K |
| 1 | 1 | 0 | 0 | 1 | C800 | 50K |
| 1 | 1 | 0 | 1 | 0 | D000 | 52K |
| 1 | 1 | 0 | 1 | 1 | D800 | 54K |
| 1 | 1 | 1 | 0 | 0 | E000 | 56K |
| 1 | 1 | 1 | 0 | 1 | E800 | 58K |
| 1 | 1 | 1 | 1 | 0 | F000 | 60K |
| 1 | 1 | 1 | 1 | 1 | F800 | 62K |

## 2.6.3 THE INTERRUPT DAISY CHAIN HEADER

The Z-80 Mode 2 Interrupt Daisy Chain, when extended beyond four peripheral devices, requires look-ahead logic to ensure that all devices are properly informed of higher-priority interrupts within the allotted time. CCS Systems 200, 300, and 400 implement a unique look-ahead scheme in which: 1) each board participating in the daisy chain asserts its interrupt priority by forcing a given Vectored Interrupt bus line low; and 2) a board is prevented from interrupting when a lower-numbered VI* line is low. Thus there are nine interrupt priority levels, 0-8; the priority 0 board controls VI0* and senses no VI* lines, while the priority 8 board senses all VI* lines and controls none. The Interrupt Daisy Chain Header allows the user to select the interrupt priority level of the 2805 by selecting which VI* line(s) the board will be sensitive to and which VI* line it will pull low when the on-board PIO requests an interrupt.

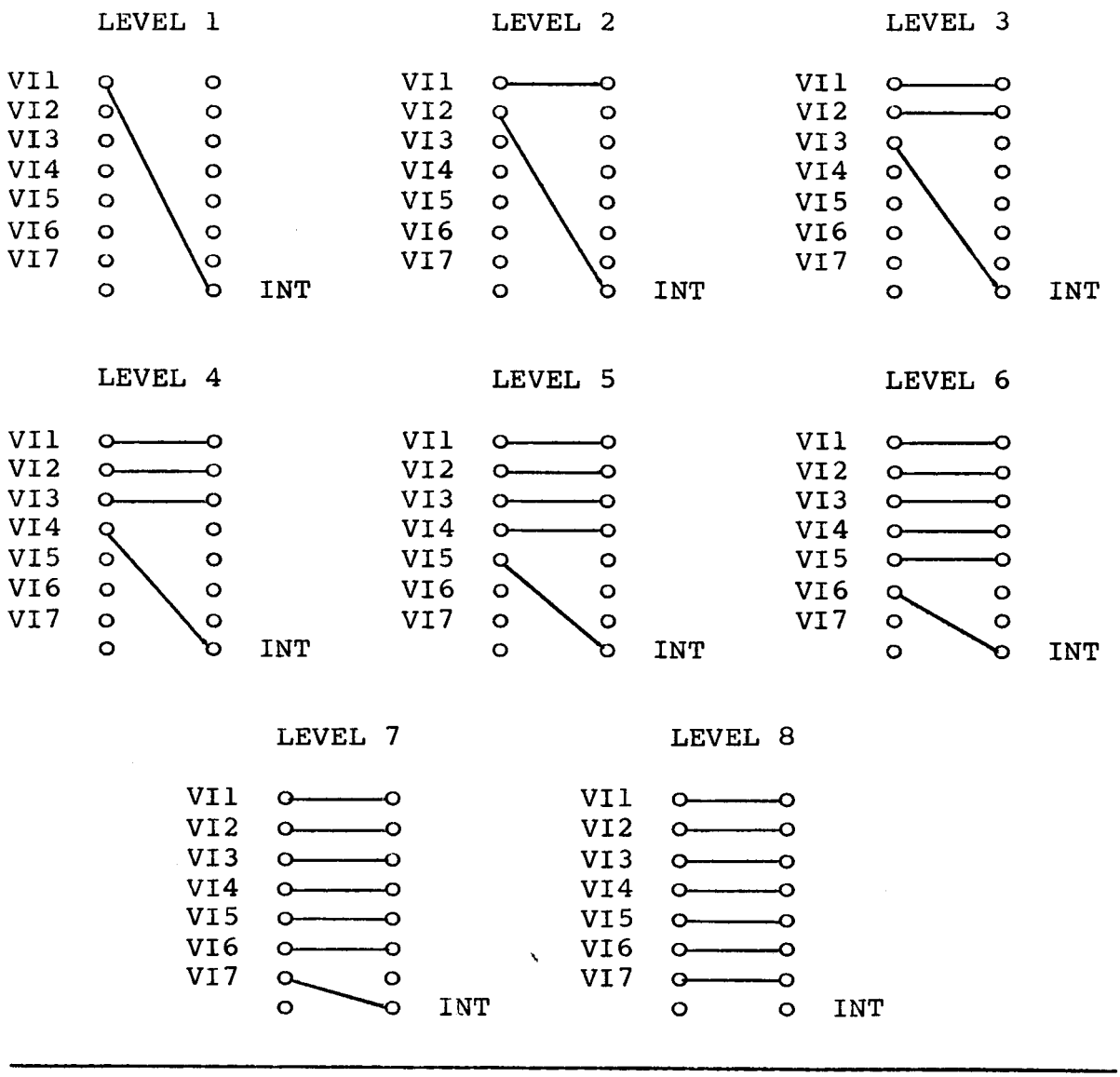
System 200/300/400 interrupt priorities may be determined at the system implementer's discretion, depending on system components and application. However, the priority scheme shown below should be appropriate for the majority of users. The System Processor is hardwired for Level 0; it is the only board whose priority is fixed.

```
        Level 0:  2820 System Processor
-----> Level 1:  2805 Clock/ROM/Terminator
        Level 2:  2830 Six-Channel Serial I/O
        Level 3:  2719 2 Parallel/2 Serial I/O
        Level 4:  2831 Arithmetic Processor
        Level 5:  2833 GPIB Interface
        Level 7:  2822 Floppy Disk Controller
        Level 8:  2832 Hard Disk Controller
```

Note that gaps are allowed in the priority structure; thus, it is not necessary to reconfigure a Level 3 board to Level 2 if there is no Level 2 board in the system. However, no priority level may be occupied by more than one board. Priority swapping of boards in an integrated system can be accomplished by swapping header plugs. For example, to put the 2830 at Level 1 and the 2805 at Level 2, simply exchange the boards' header plugs.

To configure the header, first determine the priority level, then: 1) tie all lower-numbered VI pins straight across; and 2) tie the VI pin corresponding to the 2805's priority level to the pin labeled INT. Note that the lowest level to which the 2805 may be assigned is 1; the board is hardwired to sense the VI0* line, which is reserved as the 2820 System Processor's priority-assertion line. Figure 2-2 shows all possible header configurations.

Figure 2-2. INTERRUPT DAISY CHAIN HEADER CONFIGURATION



### 2.6.4 DISABLING THE ROM AND/OR RESET GLIDE

The Reset Glide circuitry (which guarantees that the ROM is the first memory to respond after power-on or reset) and the ROM itself may be separately jumper-disabled. If the ROM is to be enabled, but not used as a Boot ROM, the Reset Glide should be disabled. If the ROM is disabled, the Reset Glide can be used to glide to a Boot ROM located elsewhere in the system if the 2805 ROM Address Select Jumpers are set to the base address of the Boot ROM. To disable the ROM and/or Reset Glide, set the jumper(s) to the D position.

### 2.6.5 ENABLING WAIT STATES

One method of ensuring the necessary timing delays when addressing the clock is to force the processor to wait until the clock is ready (see Chapter 3). To do so, install a jumper between the pads labeled CLK WAIT. When the jumper is installed, the board's logic forces the RDY bus line low for the duration of the required timing delays.

In some cases it may also be necessary to slow the processor when the ROM is accessed. To cause a single wait state to be included in all machine cycles in which the ROM is accessed, install a jumper between the pads labeled ROM WAIT.

### 2.6.6 MODE 1 INTERRUPT JUMPERS

These jumpers allow you to configure the 2805 for Z-80 Mode 1 interrupts. For Mode 1, install a jumper wire between the pads labeled INTS, cut the INTA E trace, and install a jumper wire between the INTA D pads. This prevents the 2805 from gating an interrupt vector onto the bus during Interrupt Acknowledge cycles and allows the processor to determine whether the 2805 has interrupted by reading PIO bit B4.

## 2.7 DISABLING TERMINATION

In some systems termination may already be present; for example, early versions of the CCS 2220 mainframe terminate the open collector lines. If the 2805 is installed in such a system, duplicate termination should be removed, preferably from the motherboard or other terminating board if possible. On the 2805, resistor packs Z4-Z5 terminate the open collector lines, while packs Z6-Z10 terminate the tri-state lines.

# CHAPTER 3

# PROGRAMMING INFORMATION

This chapter details the programming of the clock through the Z-80 Parallel Input/Output Controller (PIO); it is intended for those who wish to write their own drivers for the 2805. Complete programming instructions for the 5832 Clock/Calendar chip are included, along with a discussion of the unique programming requirements of the PIO as implemented on the 2805. For those unfamiliar with the PIO, general programming information is available in numerous publications, including the CCS Z-80 Family Programming Reference Manual. (Part of the CCS Systems 200/300/400 documentation, the Z-80 Family Programming Reference Manual may also be ordered separately from CCS.) Also included in this chapter is a discussion of possible adaptations of the ROM.

## 3.1 INITIALIZING THE PIO

The addresses of the PIO Channel A and Channel B Data and Command Ports (assuming that the factory-set base address of 38H is used) are given in Table 3-1. Channels A and B should be programmed as follows:

1. PIO Channel A is always programmed for Mode 0, the output mode. To select Mode 0, write 0FH to the Channel A Command Port. To enable interrupts when handshake input ASTB* returns high (one way to ensure the timing delays required by the clock--see Section 3.2), follow by writing 83H to the same port; to disable interrupts, follow by writing 03H.

2. Channel B should be programmed for Mode 3, the control mode, allowing the direction of Bits 3-Ø (connected to clock pins D3-DØ) to be changed as required. To select Mode 3, write CFH to the Channel B Command Port, followed by CFH again to read from the clock or CØH to write to it. (The Write Switch must be in the WRITE EN position when you write to the clock. Once the clock has been set to the proper time, there should be no need to write through Channel B until the clock requires resetting; thus, it is a good idea to flip the Write Protect Switch to LOCK to prevent accidental rewriting of a clock digit.) If periodic interrupts are not desired (see Step 3 below), Channel B may be programmed for Mode 1 after the clock has been set. To select Mode 1, write 4FH to the Channel B Command Port.

3. Writing one of the following byte pairs to the Channel B Command Port enables periodic interrupts if the clock is programmed to generate reference pulses (see Tables 3-2 and 3-3).

97H, FEH : 1Ø24 Hz
97H, FDH : 1 Hz
97H, FBH : 1/6Ø Hz
A7H, F7H : 1/36ØØ Hz

4. If Channel A or Channel B interrupts are enabled, the appropriate Interrupt Vector Register must be programmed. (Unlike other Z-8Ø devices, the PIO has a separate Interrupt Vector Register for each channel.) Any byte with Bit Ø = Ø written to a channel's Command Port programs that channel's Interrupt Vector Register.

TABLE 3-1. PORT ADDRESSES

| ADDRESS | PORT |
|---|---|
| 38H-3BH | ROM On/Off Switch |
| 3CH | PIO Channel A Data |
| 3DH | PIO Channel A Command |
| 3EH | PIO Channel B Data |
| 3FH | PIO Channel B Command |

TABLE 3-2. 5832 CLOCK DATA AND ADDRESSES

| A A A A 3 2 1 Ø | HEX | CLOCK COUNTER | D D D D 3 2 1 Ø |
|---|---|---|---|
| Ø Ø Ø Ø | Ø | Second 1 | X X X X |
| Ø Ø Ø 1 | 1 | Second 1Ø | - X X X |
| Ø Ø 1 Ø | 2 | Minute 1 | X X X X |
| Ø Ø 1 1 | 3 | Minute 1Ø | - X X X |
| Ø 1 Ø Ø | 4 | Hour 1 | X X X X |
| Ø 1 Ø 1 | 5 | Hour 1Ø | A B X X |
| Ø 1 1 Ø | 6 | Day of Week | - X X X |
| Ø 1 1 1 | 7 | Day/Month 1 | X X X X |
| 1 Ø Ø Ø | 8 | Day/Month 1Ø | - C X X |
| 1 Ø Ø 1 | 9 | Month 1 | X X X X |
| 1 Ø 1 Ø | A | Month 1Ø | - - - X |
| 1 Ø 1 1 | B | Year 1 | X X X X |
| 1 1 Ø Ø | C | Year 1Ø | X X X X |
| 1 1 1 1 | F | Reference | D D D D |

X: BCD bit, Ø or 1.
-: Unused bit.
A: Ø for 12 hour, 1 for 24 hour format.
B: Ø for AM, 1 for PM.
C: 1 for 29 days in February.
D: See Table 3-3 for these outputs.

TABLE 3-3. CLOCK REFERENCE OUTPUTS

| PIN | PERIOD | HZ | POLARITY | WIDTH |
|---|---|---|---|---|
| DØ | 1/1Ø24 Sec | 1Ø24 | Sq. Wave | Duty 5Ø% |
| D1 | 1 Second | 1 | Low | 122.1 us |
| D2 | 1 Minute | 1/6Ø | Low | 122.1 us |
| D3 | 1 Hour | 1/36ØØ | Low | 122.1 us |

TABLE 3-4. PIO/CLOCK INTERFACING

| PIO BIT | A 7 | A 6 | A 5 | A 4 | A 3 | A 2 | A 1 | A Ø | B 7 | B 6 | B 5 | B 4 | B 3 | B 2 | B 1 | B Ø |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLOCK PIN/ STATUS SIGNAL | - | H O L D | W R | R D | A 3 | A 2 | A 1 | A Ø | B S Y A | B S Y H | - | - | D 3 | D 2 | D 1 | D Ø |

## 3.2 PROGRAMMING THE CLOCK

Each digit of time or date has its own counter internal to the 5832 and is separately addressed; for example, to read the time (hours, minutes, and seconds), six separate reads are required. Except for the second counters, all digit counters can be written into as well as read; writing to a second counter automatically zeroes it. The addresses of the particular digits are given in Table 3-2.

Any read from or write to the clock requires three steps: establishing HOLD to freeze the counters; reading or writing the data; and removing HOLD. Digits are addressed through PIO Channel A; data is read or written through PIO Channel B. Table 3-4 shows the formats of the byte written to Channel A of the PIO and the byte read from or written to Channel B.

STEP 1: On the first write, Bit 7 is a don't-care bit; Bit 6 must be 1; Bits 5 and 4 must be Ø; Bits 3-Ø should hold the digit address from Table 3-2.

HOLD must be stable for 150 microseconds before the second step of the clock access, the application of RD or WR. There are three ways to ensure the necessary delay. In many systems the most desirable means will be to program the PIO so that an interrupt is generated by the Channel A handshaking input ASTB*. (ASTB* is held low for the required delay time; Channel A interrupts when ASTB* returns high.) Using interrupts allows the processor to perform other tasks during the necessary delays in clock accessing. The second

alternative is to have the processor monitor Bit 6 of Channel B; when B6 returns low, the HOLD delay time has elapsed. The third alternative is to install a RDY Jumper. This forces the CPU into wait states for the duration of the timing delay. (Note: The total duration of HOLD active must always be less than 1 second or the time count will not be accurate.)

STEP 2: When the HOLD delay time has elapsed, the RD or WR signal should be applied to the clock. This step is actually two steps, a write to Channel A and a write to or read from Channel B, the order depending on whether the clock is being read or written to.

a. WRITE: First write the desired new value to the low nibble of Channel B; then rewrite to Channel A the same byte as in Step 2 except with Bit 5 = 1.

b. READ: First rewrite to Channel A the same byte as in Step 2 except with Bit 4 = 1; then read the digit addressed from the low nibble of Channel B.

The delay required following application of RD or WR in order to ensure valid data is 6 microseconds. It can be ensured in the same three ways as the address delay, except that the bit to be monitored by the CPU in the second method is B7. The delay should occur after data is written or before data is read--i.e., between the two substeps described in (a) and (b) above.

STEP 3: After the data is read or written, ØØH should be written to Channel A. This clears the HOLD signal, allowing counters to increment if necessary before the next read or write. If reference pulses have been addressed, write 1ØH instead of ØØH; this maintains RD active, allowing the reference pulses to be output by the clock chip.

## 3.3 ADAPTING THE ROM

The ROM circuitry on the 28Ø5 may be adapted for many purposes; for example, it may be used with a Monitor ROM, or with a ROM storing constants, serial numbers, or other data which may be required by a program. The ROM's base address can be selected at any 2K boundary, as described in Section 2.6.2. If the Reset Glide Jumper is set to E, the ROM on the 28Ø5 will be the first memory accessed after power-on or reset, no matter where it is addressed. However, setting the Reset Glide Jumper to D will disable this feature as well as prevent the ROM from being enabled by power-on or reset. Enabling and disabling of the ROM will thus be entirely under software control. (The ROM Software Switch allows the programmer to enable or disable the Boot ROM by writing to any of ports 38H through 3BH, Bit Ø determining whether the ROM is turned on or off. If Bit Ø = 1, the ROM is enabled; if Bit Ø = Ø, the ROM is disabled.) Whenever it is read, the ROM forces PHANTOM* low to overlay identically-addressed system memory.

# CHAPTER 4

# HARDWARE DESIGN

The 28Ø5 consists of three functionally discreet elements: a clock/calendar, circuitry for a 2K ROM (the ROM must be supplied by the user if desired) and bus termination. The clock is controlled through a Z-8Ø PIO and includes a battery back-up to maintain time-keeping functions when the system is powered down. The ROM circuitry includes Reset Glide circuitry which ensures that the ROM will come up immediately after power-on or reset, whatever its base address. Passive termination is provided for all bus lines used in CCS Systems 2ØØ/3ØØ/4ØØ. General discussions of each functional element follow; they are meant to be read in conjunction with frequent references to the Schematic/Logic Diagram in Appendix A.

## 4.1 THE CLOCK/CALENDAR

The 28Ø5 features an OKI-DATA 5832 clock/calendar chip interfaced through a Z-8Ø PIO. Besides providing two parallel I/O channels for addressing, reading from, and writing to the 5832, the PIO allows the clock to participate in the Z-8Ø Mode 2 Interrupt Daisy Chain. Additional circuitry supports the Interrupt Daisy Chain Look-Ahead Scheme implemented in CCS Systems 2ØØ/3ØØ/4ØØ.)

### 4.1.1 5832 OPERATION

The 5832 Microprocessor Real-Time Clock/Calendar, illustrated in Figure 4-1, provides accurate counting of seconds, minutes, hours, days of week and month, months, and years. The 5832 requires a 32.678 KHz reference frequency. A high at CS (Chip Select) enables the chip. Individual decimal digits of the counts kept by the 5832 are addressed through inputs A3-AØ. When the RD input is high, the addressed digit is output through D3-DØ; when the WR input is high, the addressed digit is re-written through D3-DØ. If neither RD nor WR is high, the D3-DØ pins are tri-stated. A high to the HOLD input puts all counters in a static state, ensuring error-free reads and writes; time-counting is not affected provided that HOLD is high for less than 1 second.

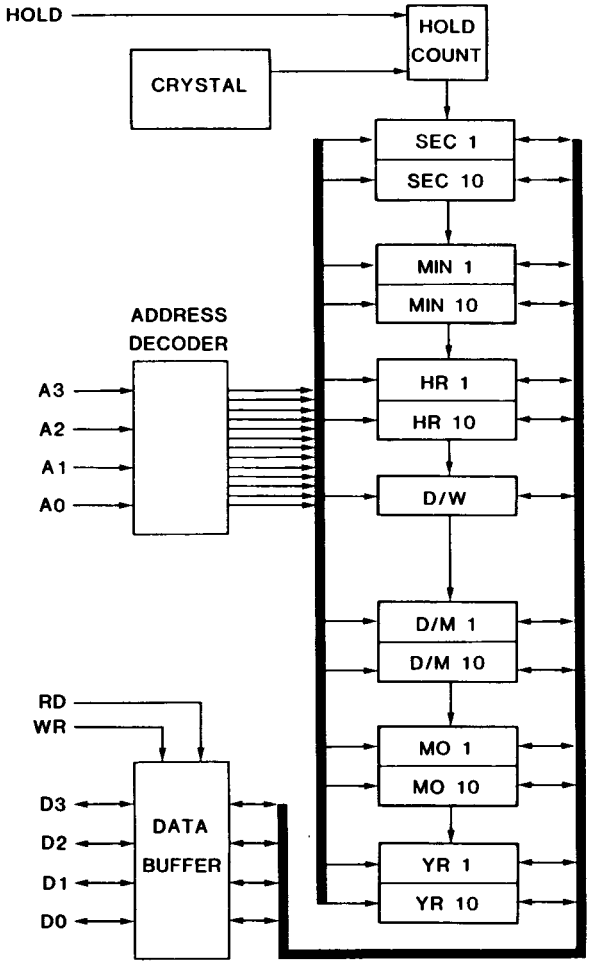



FIGURE 4-1. 5832 BLOCK DIAGRAM

The 5832 can be programmed to generate periodic interrupts. When Clock inputs AØ-A3 and RD are high and HOLD is low, D3, D2, and Dl output reference pulses of 1/36ØØ Hz, 1/6Ø Hz, and 1 Hz respectively (D3 pulses high, D2 and Dl pulse low) and DØ outputs a 1Ø24 Hz square wave. (The low on HOLD is not necessary for the square wave at DØ.) These signals may be used to generate interrupt requests every hour, every minute, every second, or approximately every millisecond. The implementation of these signals on the 28Ø5 is discussed in Section 4.1.2.5.

The 5832 will maintain time-keeping functions as long as VCC is at least +2.2 Volts. Using batteries as a back-up power source for the 5832 thus ensures that the time and date counts will not be lost when the system is intentionally or accidentally powered down. On the 28Ø5 two 1.5 Volt batteries are connected to the VCC input of the clock, which is also connected to +5 Volts. When the system is powered down, the batteries take over supplying current to the clocks, ensuring undisrupted timekeeping.

### 4.1.2 THE PIO

#### 4.1.2.1 PIO Operation

The Z-8Ø Parallel Input/Output Controller provides two parallel channels, consisting of eight data lines and two handshake lines each, which can be independently programmed for operation in one of four modes: output (Mode Ø), input (Mode 1), bi-directional (Mode 2), and control (Mode 3). In Mode 3, each bit is individually programmed as an input or an output, and the handshake lines are disabled. In addition, interrupts can be generated in Mode 3 when any unmasked input changes state. PIO inputs and outputs are defined in Table 4-1.

#### 4.1.2.2 PIO/Clock Interfacing

On the 28Ø5 the PIO is used with Channel A in Mode Ø and Channel B in Mode 3 or Mode 1. Channel A, the command channel, is used to address the clock and to apply the HOLD, RD, and WR signals to the clock as indicated in Table 3-4. (The WR signal is controlled by A5 only if the Write Switch is set to WRITE EN. This allows hardware-disabling of writes to

TABLE 4-1. PIO SIGNALS

| SIGNAL | FUNCTION |
|---|---|
| CE* | When Chip Enable is low, data is read from or written to the PIO during I/O cycles. CE* is controlled by the port address circuitry. |
| B/A* | This input, controlled by A1, determines whether Channel A or Channel B is selected. |
| C/D* | This input, controlled by AØ, determines whether a command or data transfer will occur. |
| DØ-7 | The bi-directional data pins connect directly to the 28Ø5 internal data bus. |
| IORQ* | This pin low and CE* low indicate that a control or data word is to be gated from or onto the data bus. |
| M1* | M1* serves two purposes. If both M1* and IORQ* are active, the CPU is acknowledging an interrupt. If M1* is active and both RD* and IORQ* are inactive, the PIO is reset. |
| RD* | This input determines the direction of data transfer between the CPU and the PIO. |
| A7-Ø<br>B7-Ø | These lines form the bi-directional data ports for each channel. |
| ASTB*<br>BSTB* | The handshake strobe ASTB* is controlled by the delay pulse. BSTB* is not used. |
| ARDY<br>BRDY | The handshake output ARDY is used to initiate the address delay pulse. BRDY is not used. |
| CLK | This is the PIO's clock input. It must be the same as the CPU clock. |
| INT*<br>IEI<br>IEO | These are the interrupt daisy chain signals. |

the clock during normal day-to-day operation. Writing to the clock is necessary only when the time or date has become inaccurate for some reason and must be reset.) Channel B is used for reading and writing data, reading handshake status, and generating periodic interrupts. Pins B7 and B6, the status bits, are always inputs. Pins B4 and B5 are unconnected. Pins B3-BØ are tied to pins D3-DØ of the 5832s. If Channel B is in Mode 3, pins B3-BØ can be defined as either inputs or outputs, allowing data to be either read or written. If Channel B is in Mode 1, B3-BØ are inputs and data can be read but nor written. The ability to mask specific bits in Mode 3 allows enabling of interrupts by a specific reference output when the clock is programmed to output reference pulses; the interrupt capability is lost if Channel B is programmed for Mode 1.

#### 4.1.2.3 Meeting 5832 Timing Requirements

One of the characteristics of low-power CMOS clock chips is relatively slow electrical response. Because of the timing requirements of the 5832, significant delays must follow the assertion of HOLD and the assertion of RD or WR. The necessary delays are timed by two monostable multivibrators. The first produces a 6 microsecond high pulse whenever data is written to Channel A (i.e., when RDYA, Channel A's handshake output, goes high). The second multivibrator operates similarly; when Channel A output A6 (HOLD) goes high, it outputs a 150 microsecond high pulse. The two pulses are NORed to control STBA*, the PIO handshaking signal which may be programmed to generate an interrupt on each rising edge. In addition, the 6 microsecond pulse controls PIO input B6, while the 150 microsecond pulse controls B7. Finally, if the RDY jumper is installed, either pulse active forces the RDY bus line low, causing the processor to wait. Thus there are three ways to make sure that the timing requirements of the 5832 are met: use Channel A handshaking, monitor B6 and B7, or force the processor to wait.

#### 4.1.2.4 Addressing the PIO

The PIO occupies four I/O ports in the lower half of an 8-port block whose base address, determined by jumpers A7-A3, is a multiple of 8. When, during an I/O read or an I/O write, address bits A7-A3 match the A7-A3 jumper settings and A2 is Ø, Port Address Decoder output Y3 going low enables the PIO. Address bit A1 controls PIO input B/A*, selecting the channel; address bit AØ controls input C/D*, determining whether a

command or data register is addressed. Bus line pDBIN, inverted, controls the PIO RD* input.

Due to pin constraints, the PIO has a unique way of being reset: the M1* input is monitored, and if it is active for longer than it would be in an M1 cycle, the PIO resets. Thus the PIO M1* input is forced low when either sM1 or RESET* is active.

4.1.2.5 PIO Interrupts

On the 28Ø5, either PIO channel may be programmed to generate interrupt requests: Channel A when timing delays have elapsed and Channel B when the desired reference pulse occurs. (See Chapter 3 for programming instructions.) The use of the PIO to generate all interrupts by the 28Ø5 allows the board to participate in the Z-8Ø Mode 2 Interrupt Daisy Chain.

The 28Ø5 implements the special Mode 2 Interrupt Daisy Chain Look-Ahead Scheme used in CCS Systems. In this scheme, which guarantees that all interrupting devices will be informed whether they have the highest-priority interrupt pending before the interrupt is acknowledged, the VI* lines are used to prioritize the boards in the daisy chain. A board's priority level corresponds to the VI* line it asserts when it requests an interrupt; each board is blocked from interrupting whenever a lower-numbered VI* line than the one it controls is low.

Configuration of the Interrupt Daisy Chain Header on the 28Ø5 determines the board's priority. If a higher-priority board interrupts, the low on the corresponding VI* line will force the PIO's IEI (Interrupt Enable In) pin low, disabling interrupts by the PIO until it is removed. When IEI is high, the PIO can generate interrupts by forcing its INT* output low. If either IEI or INT* is low, IEO (Interrupt Enable Output) is forced low; applied to the 28Ø5's priority-assertion VI* line, this low disables interrupts by lower-priority boards.

During an Interrupt Acknowledge cycle, if the PIO is the highest-priority device with an interrupt pending, it will put ¬ts interrupt vector on the DI bus. For that reason, logic has been included to enable the Data In Buffer when bus line sINTA is active and the PIO has the highest-priority interrupt pending. (A jumper allows this logic to be defeated if Mode 1 interrupts are desired.)

When a device's interrupt has been blocked by the interrupt of a higher-priority device, the lower-priority device monitors the data bus during all instruction fetches, looking for the RETI instruction which signals that servicing of the higher-priority interrupt has been completed and that lower-priority interrupts may now be asserted. To ensure proper monitoring of the CPU instruction fetches by the 28Ø5, the CPU must internally connect the DI and DO buses. This is necessary because, while the RETI instruction is input to the CPU on the DI lines, the 28Ø5 looks for RETI on the DO lines. The CCS 282Ø System Processor Board meets this requirement as long as no peripheral or memory board asserts DODSB during instruction fetch cycles.

## 4.2 THE BOOT ROM

The Boot ROM, a 2716 2K EPROM, can be located in any 2K block of memory whose base is a multiple of 2K, the base address being determined by jumpers A15-A11. When the jumper settings match address bits A15-A11 during a Memory Read cycle, output by the ROM is enabled.

### 4.2.1 RESET GLIDE CIRCUITRY

No matter where the Boot ROM is located in the 64K of memory, it will be the first memory accessed after power-up or reset due to the Reset Glide circuitry if the Reset Glide Enable Jumper is set to E. RESET* active sets the Reset Glide Flip-Flop (U9a); the resulting low output at Q* pulls down PHANTOM* to disable other memory in the system and enables the Reset Glide Buffer. When the Reset Glide Buffer is enabled, it pulls down bus lines DIØ-7. As a result, the CPU glides through the memory addresses, executing NOP instructions (op code ØØH) and incrementing the Program Counter until it reaches the base address of the Boot ROM. When this occurs, a low is clocked into the Reset Glide Flip-Flop, the Q* output of which goes high, disabling the Reset Glide Buffer. The CPU then executes the code stored in the Boot ROM. PHANTOM* remains asserted as long as the Boot ROM is addressed.

If the Reset Glide Enable Jumper is set to D, the Reset Glide circuitry is disabled and the CPU will begin executing at location ØØØØH after power-up or reset.

### 4.2.2 SOFTWARE CONTROL OF THE ROM

The ROM can be enabled and disabled under program control. As described above, the PIO occupies the upper four addresses in a user-selected 8-address block. Writing to one of the lower four addresses clocks data bit DOØ into the ROM Switch Flip-Flop (U9b). If DOØ is Ø, the ROM is disabled. If DOØ is a 1, the ROM is enabled.

## 4.3 TERMINATION

The 28Ø5 provides passive termination of all but the most rarely used S-1ØØ bus lines. Resistor values were chosen to specifically provide TTL line termination to the 2.7 Volt Thevenin equivalent line voltage at the characteristic TTL line impedance of 36Ø ohms.

## 4.4 BUS BUFFERING

All system bus inputs and outputs used by the clock and BOOT ROM circuitry are fully buffered. Hysteresis drivers and receivers are employed to ensure minimum noise on the bus, with no load of more than one Low-Power Schottky TTL level being placed on any system bus input. PHANTOM*, INT*, and lower-priority VI* line drivers are open-collector. Except for the Reset Glide Buffer and the Data Out and Data In Buffers, all buffers are permanently enabled. Basically, the Data In Buffer is enabled when: 1) pDBIN* is active AND either the clock or the ROM is addressed, OR 2) during an interrupt acknowledge when the PIO has the highest-priorty pending interrupt. At all other times the Data Out Buffer is enabled. The Reset Glide Buffer is discussed in Section 4.2.2.

# APPENDIX A

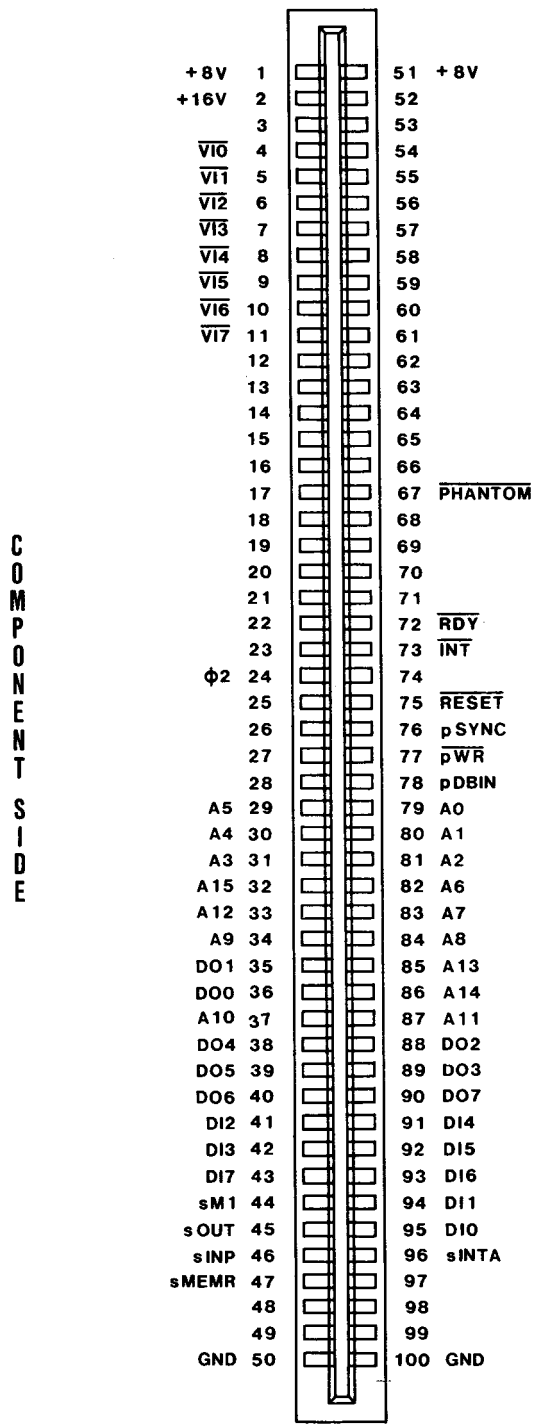
# TECHNICAL INFORMATION

## A.1 USER-REPLACEABLE PARTS

| QTY | REF | DESCRIPTION | CCS PART # |
|---|---|---|---|
| **INTEGRATED CIRCUITS** | | | |
| 1 | U8 | MSM5832 Calendar/Clock Chip | 48200074-01 |
| 1 | U10 | Z-80 PIO | 48200083-01 |
| 1 | U22 | 74LS00 | 48200001-01 |
| 1 | U11 | 74LS02 | 48200002-01 |
| 1 | U23 | 74LS04 | 48200004-01 |
| 1 | U13 | 7407 | 48200051-01 |
| 1 | U12 | 74LS08 | 48200006-01 |
| 1 | U3 | 74LS30 | 48200012-01 |
| 1 | U9 | 74LS74 | 48200015-01 |
| 1 | U7 | 74LS123 | 48200019-01 |
| 1 | U24 | 74LS132 | 48200020-01 |
| 3 | U4,5,15 | 74LS136 | 48200021-01 |
| 1 | U14 | 74LS139 | 48200023-01 |
| 6 | U16-21 | 74LS244 | 48200035-01 |
| 2 | U1,2 | 7805 +5 Voltage Regulator | 48200109-01 |
| **RESISTORS** | | | |
| 1 | R1 | 10K, 1/4 W, 5% | 47000004-01 |
| 1 | R2 | 20K, 1/4 W, 5% | 47000017-01 |
| 3 | R3-5 | 2.7K, 1/4 W, 5% | 47000023-01 |
| 5 | Z6-10 | Network, 330/390 ohm | 47400010-01 |
| 1 | Z3 | Network, SIP, 10K x 7 | 47400017-01 |
| 1 | Z1 | Network, SIP, 2.7K x 7 | 47400002-01 |
| 2 | Z4,5 | Network, SIP, 1K x 16 | 47400008-01 |
| 1 | Z2 | Network, SIP, 1K x 7 | 47400016-01 |
| **CAPACITORS** | | | |
| 1 | C5 | Mica, 33 pf, 500VDC | 15000007-01 |
| 16 | C3,4,10-12,14-24 | Monolythic, .1 uf, 50VDC | 15900001-01 |
| 4 | C1,2,9,13 | Tantalum, 4.7 uf, 35VDC | 15500003-01 |
| 1 | C8 | Disc, .01 uf, 50VDC | 15100004-01 |
| 1 | C7 | Disc, .001 uf, 50VDC | 15100003-01 |
| 1 | C6 | Trimmer, 5-25 uf | 15700001-01 |

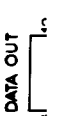
| QTY | REF | DESCRIPTION | CCS PART # |
|---|---|---|---|
| MISCELLANEOUS | | | |
| 1 | Y1 | Crystal, 32.76 KHz | 23000001-01 |
| 2 | D1,2 | Diode, IN914 | 48100001-01 |
| 2 | | Heatsink | 76000001-01 |
| 1 | | Toggle Switch | 51000001-01 |
| 8 | | IC Socket, 16 pin DIP | 21400015-01 |
| 1 | | IC Socket, 24 pin DIP | 21400018-01 |
| 1 | | IC Socket, 40 pin DIP | 21400040-01 |
| 2 | | Battery Clip | 28800002-01 |
| 2 | | Battery Cup | 28800003-01 |
| 2 | | Battery Insulator | 28800005-01 |
| 6 | | Screw, SEM PPH 6-32 x 5/16 | 28000006-01 |
| 6 | | Nut, 6-32 x 1/4 | 28100001-01 |
| 1 | | Header, 16-pin DIP | 21600001-01 |
| 1 | | Header Cover, 16-pin DIP | 14100001-01 |
| 12 | | Header, 1 x 3 | 21000008-01 |
| 12 | | Jumper Plug | 21300021-01 |
| 2 | | PC Board Extractor | 28300001-01 |
| 2 | | Extractor Roll Pin | 74000001-01 |

## A.2 BUS CONNECTOR PINOUTS




TOP VIEW

## A.3 SCHEMATIC/LOGIC DIAGRAM: WALLCLOCK



DATA OUT

DO0 36
DO1 35
DO2 88
DO3 89
DO4 38
DO5 39
DO6 40
DO7 90

U18 74LS244

DATA IN

DI0 95
DI1 94
DI2 41
DI3 42
DI4 91
DI5 92
DI6 93
DI7 43

U19 74LS244

RESET GLIDE BUFFER

U20 74LS244

R3 2.7K

JMP

74LS07

PHANTOM 67

74LS04

74LS00

U22

74LS30

U3

J1

VI0 4
VI1 5
VI2 6
VI3 7
VI4 8
VI5 9
VI6 10
VI7 11

Z1

74LS07

INT 73

74LS07

74LS02

U11

74LS74

CLR D Q PR U9

ROM E D

74LS08

U12

74LS00

U22

74LS04

R4 2.7K

U6 2716

D7 D6 D5 D4 D3 D2 D1 D0

A0 A1 A2 A3 A4 A5 A6 A7 A10 A9 A8

Φ 24
sINTA 96
pDBIN 78
sOUT 45
sINP 46
sM1 44
RESET 75
pWR 77

U21 74LS244

74LS02

U11

74LS24

U24

74LS12

U12

74LS139

U14

PORT ADDR DECODER

74LS07

ROM WAIT

74LS132

U24

74LS04

Z2

74LS136

U4 U4 U4 U5 U5

PORT ADDR

A3 A4 A5 A6 A7

RDY 72

A0 79
A1 80
A2 81
A3 31
A4 30
A5 29
A6 82
A7 83

U16 74LS244

pSYNC 76
sMEMR 47

74LS136

U4 U15 U15 U15 U15

ROM ADDR

A15 A14 A13 A12 A11

A15 32
A14 86
A13 85
A12 33
A11 87
A10 37
A9 34
A8 84

U17 74LS244

Φ
RD
IORQ
M1

CE
B/A
C/D
IEI
IEO
INT

U10 Z80A-PIO

A STB
GND

A RDY

B7
B6

74LS123

U7

C7 .001uf
R1 10K

C8 .01uf
R2 20K

C6 5-25pf
C5 20pf
Y1 32.768KHz

U8 MSM5832

WR RD A0 A1 A2 HOLD D3 D2 D1 D0
A5 A4 A3 A6 B3 B2 B1 B0

CS
VCC

C9 4.7uf
D2 D1 1N4001

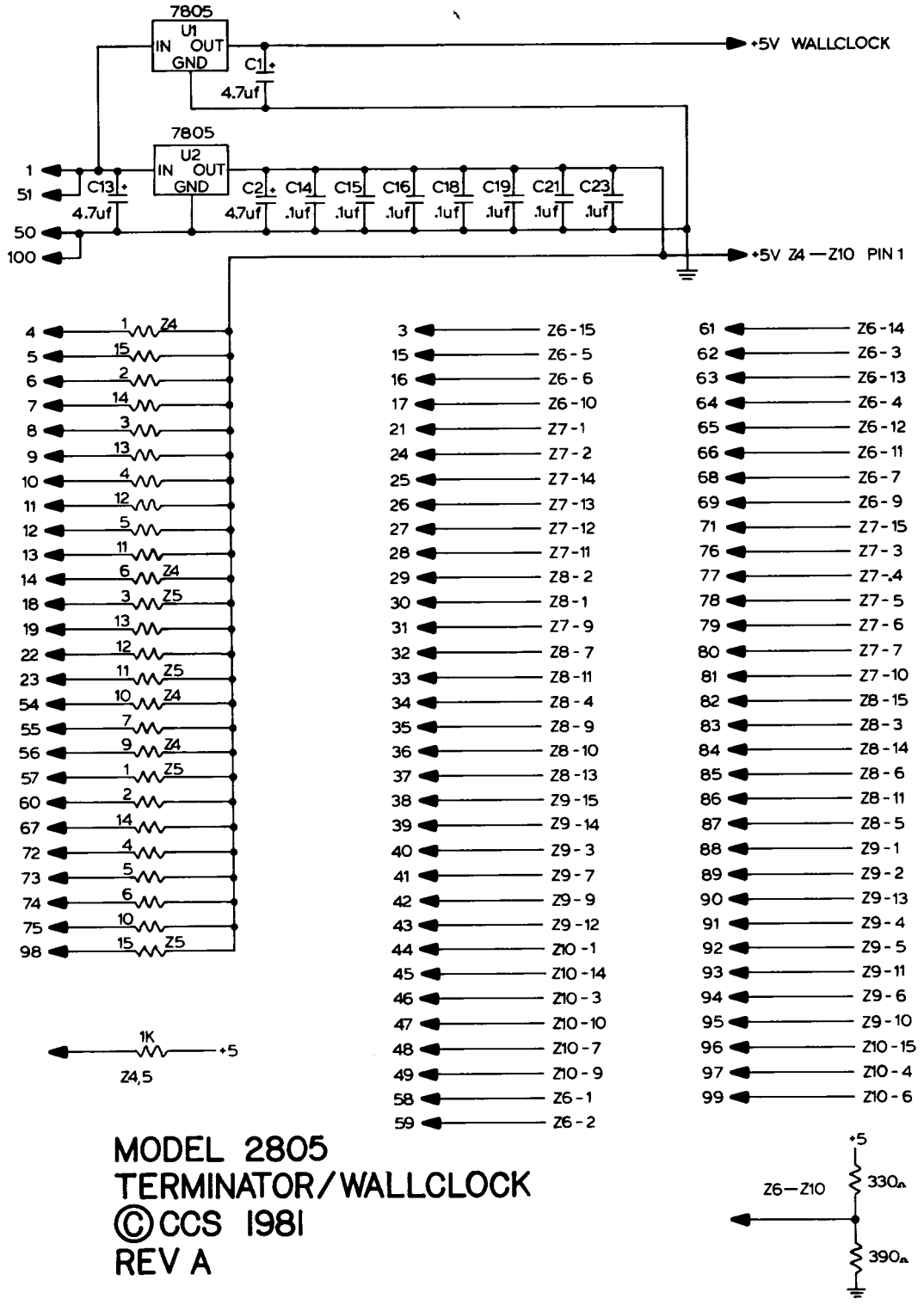
CLK WAIT

R5 2.7K

MODEL 2805
WALLCLOCK / TERMINATOR

REV A

## A.4 SCHEMATIC/LOGIC DIAGRAM: TERMINATION



# ADDENDUM TO 2805 REFERENCE MANUAL, REV. A

## BATTERY INSTALLATION AND MODE 1 JUMPERS

### BATTERIES

Section 2.2 incorrectly states that batteries should be placed in the clips "positive side up." The proper installation is with the negative side (button side) up. No damage will be done to either the batteries or the clock if the batteries are installed upside down, but the clock will of course not be able to draw power from the batteries unless they are correctly installed.

### MODE 1 INTERRUPT JUMPERS

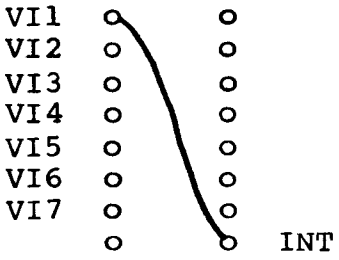
Rev. D 2805 boards include two new jumpers to allow implementation of Z-80 Mode 1 interrupts: INTS, located in the center of the board below the PIO, and INTA, located in the lower right corner below U23. To use the 2805 in Mode 1, cut the E trace of the INTA jumper, install a jumper wire in the D position, and install a jumper wire between the INTS pads.

The INTA jumper wired to D prevents the 2805 from putting an interrupt vector on the bus during Interrupt Acknowledge cycles. The INTS jumper routes the PIO's IEO output to PIO data bit B4, where the processor can monitor it; if B4 (which must be programmed as an input) is low, the 2805 has requested an interrupt.

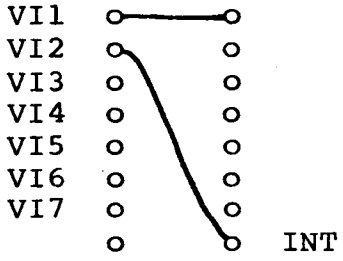
## ADDENDUM: MODE 2 INTERRUPT HEADER CONFIGURATION

The Mode 2 Interrupt Priority Headers on CCS system boards require configuration by the user. The illustrations below, which apply to all system boards except the 2832 Hard Disk Controller, show the proper configuration for each priority level; Level Ø is reserved for the 282Ø System Processor. Gaps are allowed in the priority scheme; for example, a Level 3 board will respond properly even if there is no Level 2 board. However, no priority level may be occupied by more than one board. See your board manuals for suggested priority levels.

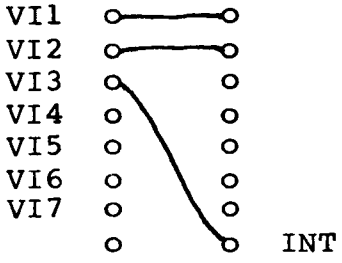
LEVEL 1



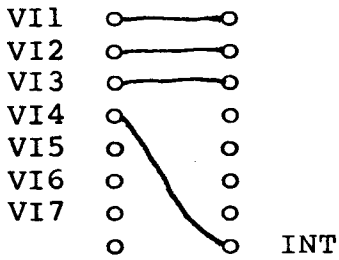

LEVEL 2



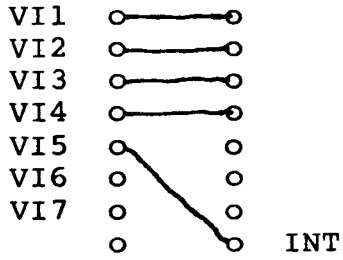

LEVEL 3



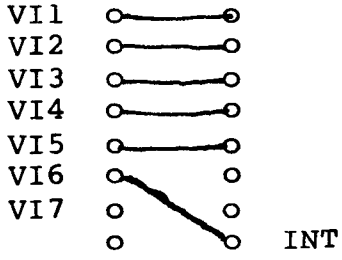

LEVEL 4



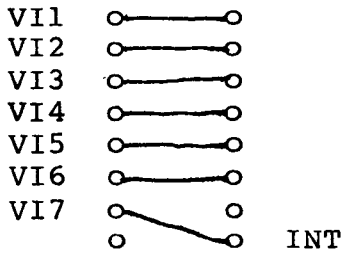

LEVEL 5




LEVEL 6




LEVEL 7




LEVEL 8