MODEL 2066
64K DYNAMIC MEMORY

Reference Manual

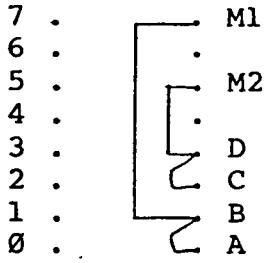
California Computer Systems

CCS 2066 REFERENCE MANUAL

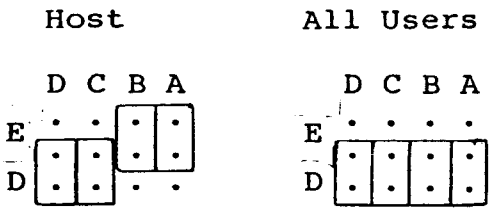
ADDENDUM 1: CONFIGURING FOR CROMIX SYSTEMS

The following figures show the configuration of the Bank Select Header and the Multi-Bank and Reset Enable Jumpers for three 2066 boards used in a two-user Cromix system. All three Bank Select Headers are configured the same.

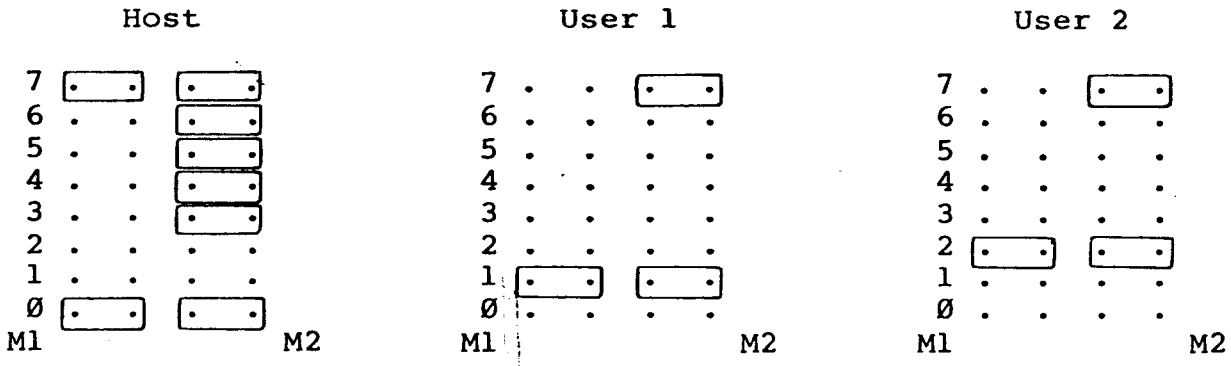
Bank Select Header



Reset Enable Jumpers



Multi-Bank Jumpers



To add a third user, remove the Bank 3 jumper plug from the host's Multi-Bank Jumpers, then configure a fourth 2066 board the same as the third 2066 except with jumper plugs in the Bank 3 row of the Multi-Bank Jumpers instead of the Bank 2 row. Additional users may be added following the same procedure.

CCS MODEL 2066

64K DYNAMIC MEMORY

Reference Manual

Rev. A

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California Computer Systems

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The information contained in this manual is believed to be correct at the time of publication. However, CCS assumes no liability resulting from the use of this publication.

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CHAPTER 1

INTRODUCTION

1.1 GENERAL INFORMATION

The CCS Model 2066 provides 64K of bankable dynamic RAM for system memory expansion up to 512K. Designed for optimum performance in CCS systems, the 2066 conforms to the IEEE specifications for the S-100 bus and is flexible enough to be compatible with most 8080- and Z-80-based S-100 systems. Memory refresh circuitry responds to the bus signals of both types of CPU, and includes a timing function to guarantee that memory will be refreshed during extended wait states.

The 2066 RAM array is divided into four 16K blocks which are independently addressed and banked by the user. (Banking is accomplished using a bank-byte/bank-port scheme. An I/O port is dedicated for bank selection, and whenever a byte is written to that port, each bank is enabled or disabled according to whether the corresponding bit of the bank byte is a 1 or a 0--bit 6 = 1 enables bank 6, for example). Each block may be individually set to be disabled by PHANTOM* and to come up active after reset. In addition, several other options are provided. The 2066, however, requires relatively little configuration by the user. In cases where most users will desire the same configurations, options have been hardwired; thus configuration is necessary only when a non-standard option is selected.

1.2 SPECIFICATIONS

MEMORY

Capacity:	64K in Four 16K Blocks
Type:	4116 (or Equivalent) 16K x 1 Dynamic RAM
Access Time:	200 Nanoseconds
Cell Refresh:	Once Every 2 Milliseconds
Banking Scheme:	Bank Port/Bank Byte

SYSTEM INTERFACE

S-100: Complies with IEEE Task 696.1/D2,
SLAVE F6 T300
16K Block Base Addresses Jumper-Selected
Bank Port and Bank Level Jumper-Selected
Jumper-Selectable Cromix Compatibility

POWER CONSUMPTION

Current Drain:	472 mA at +8 Volts (Regulated On Board to +5 Volts)
	25 mA at +16 Volts (Regulated On Board to +12 Volts)
	2.6 mA at -16 Volts (Regulated On Board to -5 Volts)
Dissipation:	4.25 Watts
	61.7 Gram-Calories/Minute
	.255 BTU/Minute

ENVIRONMENTAL REQUIREMENTS

Temperature:	0°C. to +70°C.
Humidity:	Up to 90% Non-Condensing

1.3 BLOCK DIAGRAM

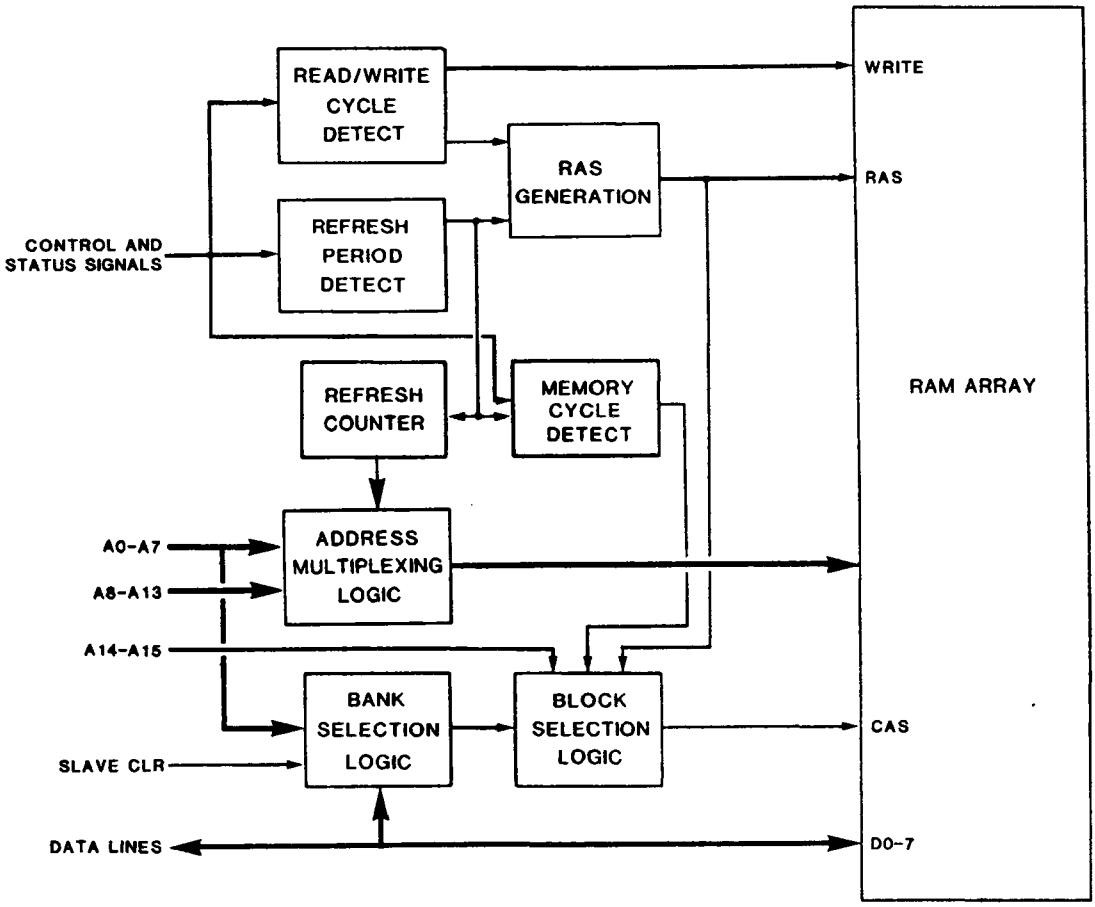


FIGURE 1.1. 2066 BLOCK DIAGRAM

1.4 USING THIS MANUAL

This manual is intended as a reference for those who install, program or troubleshoot the 2066. Chapter 2 deals with board configuration, and should be read before the board is installed in a system. Chapter 3 provides banking configuration instructions for the 2066 if it is used in a CCS system. Chapter 4 is a detailed discussion of the hardware design of the 2066, and is intended to be read in conjunction with a study of the schematic/logic diagram. The schematic/logic diagram and various other technical illustrations and tables are included in Appendix A.

1.5 CAUTIONS

Before installing and testing your 2066, please read the following instructions.

1. ALWAYS power down your mainframe before installing or removing boards.

2. ICs may work loose during shipping. Ensure that all chips are firmly seated before you install the board.

3. Dynamic RAMs are very sensitive to heat. Make sure that your mainframe is properly cooled. Something as seemingly trivial as a dirty fan filter might cause erratic operation of dynamic RAMs.

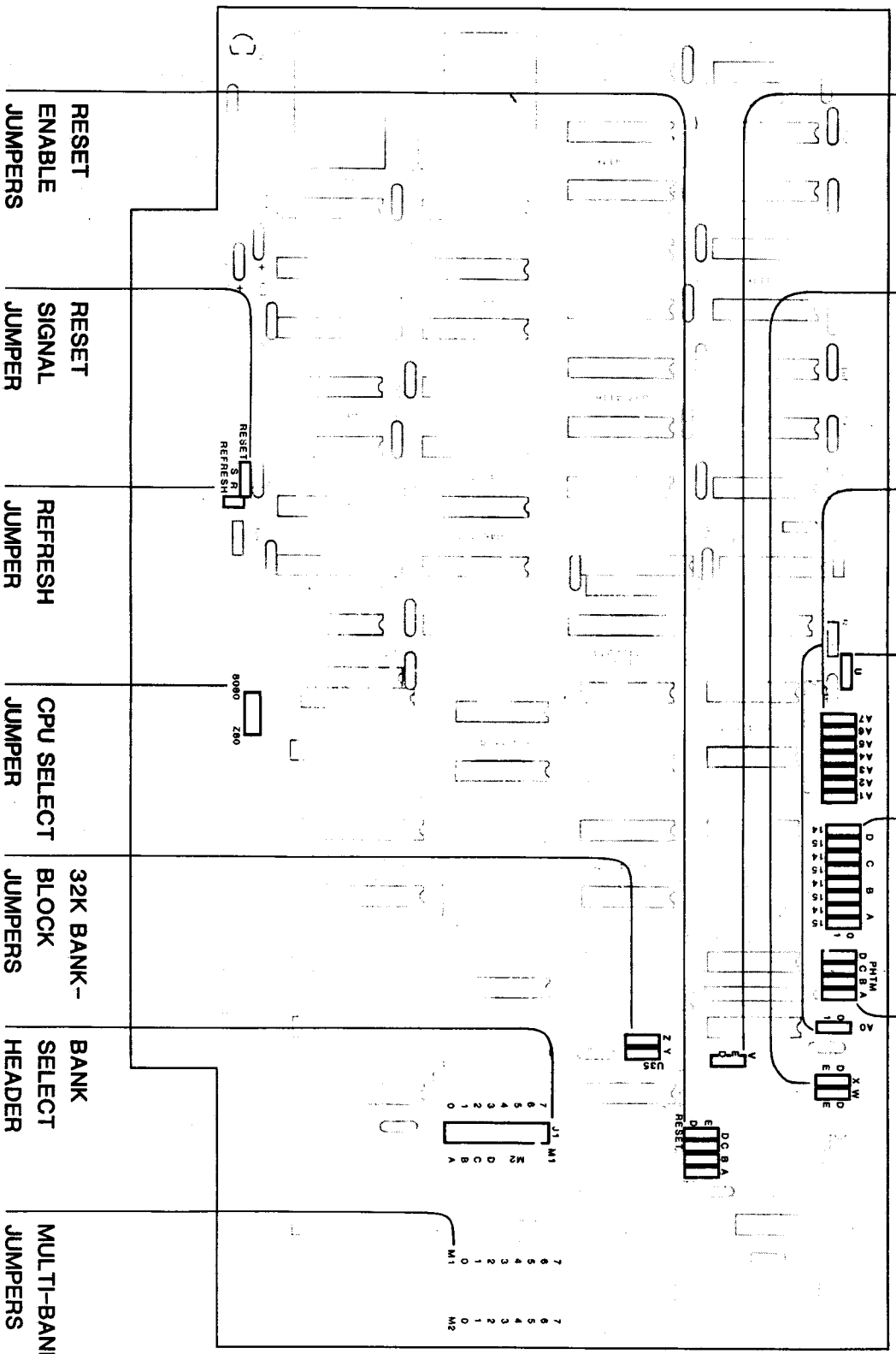
CHAPTER 2

USER-CONFIGURABLE OPTIONS

The 2066 incorporates several user-selectable options designed to provide a flexibly addressed and banked 64K dynamic RAM board compatible with a wide range of systems. The 2066's 64K of RAM is divided into four 16K blocks which are independently addressed, banked, reset-enabled, and PHANTOM-enabled. The hardwired bank port address can be altered by the user. Additional options include emulating Cromix system memory, substituting pDBIN for sMEMR in 8080-based systems, and disabling RAS* generation during M1 cycles.

Options on the 2066 are configured in three ways. One DIP header with cover is used; the user configures the option by soldering wires to the header. In other cases, the user selects an option by placing a shorting plug across the appropriate pair of header pins. In cases where few users will select a non-standard configuration, the standard configuration is hard-wired and the user selects a non-standard configuration by installing a jumper wire between two pads and/or cutting a trace. The locations of the headers and jumpers by which options are configured are shown in Figure 2-1. Each option is discussed individually below.

Users of CCS systems need not concern themselves with the section of this chapter dealing with cut-trace-and-jumper options, which are provided to meet special requirements of non-CCS systems. Specific instructions regarding the setting of the other jumpers for various CCS systems are given in Chapter 3.


WRITE PHANTOM JUMPER
DMA ENABLE JUMPERS
BANK PORT ADDRESS JUMPERS
M1 RAS JUMPER
BLOCK ADDRESS JUMPERS
PHANTOM ENABLE JUMPERS
RESET ENABLE JUMPERS
RESET SIGNAL JUMPER
REFRESH JUMPER
CPU SELECT JUMPER
32K BANK-BLOCK JUMPERS
BANK SELECT HEADER
MULTI-BANK JUMPERS
RESET
REFRESH
8080
Z80
PHTM
RESET
J1
M1
M2

2.1 HEADER-CONFIGURED OPTION

2.1.1 The Bank Select Header

The Bank Select Header, J1, allows the user to select the bank in which each memory block will reside. Pins labeled A, B, C, and D correspond to the four memory blocks; pins labeled 0-7 correspond to the eight banks. In addition, two pins, labeled M1 and M2, allow blocks to be assigned to more than one bank (see Section 2.2.1). To configure the header, tie each of pins A, B, C, and D to one of the bank level or multi-bank pins. More than one block pin may be tied to the same bank level or multi-bank pin; however, only one bank level or multi-bank pin may be tied to each block pin.

If a block pin A-D is left unconnected, the corresponding memory block will be independent of bank selection--i.e., it will be enabled with all banks. The block will be enabled as soon as the system is powered on if its Reset jumper is in the E position. If its Reset jumper is set to D, the block will be enabled after the first write to the bank port and will remain enabled until next system reset.

2.2 SHORTING-PLUG-CONFIGURED OPTIONS

2.2.1 The Multi-Bank Jumpers

A pair of 2 x 8 headers allow the user to enable one or more of the memory blocks with more than one bank. (This feature may be especially desirable in multi-user systems in which different groups of users will share blocks of memory.) Multi-Bank Headers M1 and M2 control Bank Select Header pins M1 and M2. Each Multi-Bank Header consists of eight pairs of pins labeled 0-7 and corresponding to the eight memory banks. To configure a Multi-Bank Header, place shorting plugs across the pairs of pins corresponding to the banks desired. The configuration of the Multi-Bank Jumpers has no effect unless pins M1 and/or M2 of the Bank Select Header are connected.

2.2.2 The Block Address Jumpers

These jumpers select the states of A15 and A14 required to enable each of the memory blocks--i.e., they select the base addresses of the four 16K blocks of RAM on the 2066. Set the jumpers for the desired block base addresses as shown in Table 2-1. As shipped, the board is configured for the following block base addresses: A=00H; B=40H; C=80H; D=C0H.

TABLE 2-1. BLOCK ADDRESS SELECTION

JUMPERS		BASE ADDRESS	
A15	A14	HEX	DEC
0	0	0000H	0K
0	1	4000H	16K
1	0	8000H	32K
1	1	C000H	48K

2.2.3 The Phantom Enable Jumpers

The PHANTOM* bus line is used by some memory devices to disable identically-addressed system memory. These jumpers determine which 16K blocks will be PHANTOM-sensitive--i.e., which blocks will be disabled when PHANTOM* is low. To make a block PHANTOM-sensitive, place a shorting plug over the correspondingly-labeled pair of pins. Leaving a pair of pins open causes the corresponding block to ignore the PHANTOM* signal. In the factory configuration, Block A is Phantom-enabled, while blocks B, C, and D are Phantom-disabled.

2.2.4 The Write Phantom Jumper (V)

This jumper controls whether PHANTOM-sensitive memory will be disabled by PHANTOM* active during read cycles only (soft Phantom) or during both read and write cycles (hard Phantom). If PHANTOM* is to be asserted by a ROM (e.g., a Boot ROM), there is no reason for PHANTOM* to disable RAM during write cycles; in fact, it may be important in some situations that RAM be write-accessible while PHANTOM* is

asserted--for example, if the ROM contents are to be copied into RAM at the same address. If the Write Phantom Jumper is in the D position, PHANTOM-enabled memory will always operate in the soft Phantom mode. (Removing the jumper plug has the same effect as setting the jumper to D.)

If the Write Phantom jumper is in the E position, Phantom-enabled memory operates in the soft Phantom mode until a write to the bank port, then in the hard Phantom mode until the system is reset. This arrangement allows the Boot ROM to copy itself into RAM, then write to the bank port to allow other RAM to overlay the 2066's Phantom-enabled block(s).

2.2.5 The Reset Enable Jumpers

These jumpers determine whether a block of memory will be enabled or disabled by a reset of the board. If a block's Reset jumper is in the E position, the block will come up enabled after power-on or reset regardless of whether its bank is selected. If its Reset jumper is in the D position, the block will be disabled after power-on or reset and will remain disabled until its bank is selected.

2.3 CUT-TRACE-AND-JUMPER OPTIONS

2.3.1 The Bank Port Address Jumper Pads

The 2066 is hard-wired for a bank port address of 40H (i.e., A6 is closed, closed, A1-A5 and A7 are open, and A0 is closed at 0 and open at 1). This is the bank port used by most S-100 systems, including all CCS systems, employing a bank-port/bank-byte memory banking scheme. To configure for a different bank port address, write out the address in binary, then open or close each pair of pads A7-A1 according to the desired address (open selects a 0 in that bit position; closed selects a 1). A0 is configured a little differently, separate jumpers/traces being used to select a 0 and a 1. For A0=0, close 0 and open 1; for A0=1, close 1 and open 0.

If more than eight users are implemented under OASIS, a second bank port is required. CCS dedicates port 41H as the second bank port. The A0 jumper is equipped with a 3 pin

header to facilitate changing the bank port from 40H to 41H. For 41H, cut the trace between the 0 pins (on the back of the board) and install a jumper plug over the 1 pins.

2.3.2 The Reset Signal Jumper Pads

These pads are hard-wired so that the board is reset by the SLAVE CLR* bus line (pin 54). In most systems, SLAVE CLR* is asserted whenever RESET* (pin 75) is asserted; in addition, it may be asserted independently to clear bus slaves only. However, in some systems SLAVE CLR* is not asserted automatically when RESET* is asserted. If the 2066 is used in such a system, the trace labeled S should be cut and a jumper inserted between the pads labeled R.

2.3.3 The CPU Select Jumper Pads

As explained in Chapter 4, differences in sMEMR and pDBIN timing between 8080 and Z-80 CPUs make it impossible for the same signal to be used by the 2066 control logic in both CPU environments. Therefore a jumper has been provided to allow the substitution of pDBIN for sMEMR (the latter being the hardwired option). If you have a Z-80-based system, you will not need to alter the wiring of this jumper. If you have an 8080-based system, cut the trace between the Z80 pads and install a jumper between the 8080 pads.

2.3.4 The 32K Bank-Block Jumper Pads (Y,Z)

Cromemco's Cromix system banks memory in 32K blocks. If the 2066 is to be used with Cromemco memory boards in a Cromix system, it should be configured to emulate Cromemco memory. The 32K Bank-Block jumpers allow Blocks A and B (jumper Z) and Blocks C and D (jumper Y) to be paired for banking purposes, Block AB being banked as Block A and Block CD being banked as Block C.

The 2066 is hard-wired for 16K bank-blocks, and need not be reconfigured for any system presently available except Cromix. To make the board emulate Cromix system memory (i.e., to select 32K bank-blocks), cut the traces between the center pads and the pads toward the blade edge of the board, and

CHAPTER 3

CONFIGURATION FOR CCS SYSTEMS

3.1 CCS SYSTEM 2210 WITH CP/M

The 2210 is an example of single-user system (one 64K board) which uses bank-selection rather than PHANTOM* as a method of selectively enabling/disabling memory. The Boot ROM resides at F000H. After a system reset, the Boot ROM reads in the system loader from the disk. After being read from the disk, the system loader begins executing and immediately outputs a 01H to port 40H, which simultaneously disables the boot ROM and enables any memory assigned to Bank 0. The 2066 board is set up to work in the System 2210 as follows:

BLOCK	BASE	BANK	RESET	PHTM
A	0000H	0*	EN	OFF
B	4000H	0*	EN	OFF
C	8000H	0*	EN	OFF
D	C000H	0*	DIS	OFF

* If the memory blocks are banked in Bank 0, writing any byte other than 01H to port 40H at any time will immediately disable the system memory. This possible problem can be avoided if the memory blocks are not banked, or more properly are made to reside in all banks; this is accomplished by making no connections on the Bank Select Header. Reset-enabled blocks will come up after a reset and stay up permanently. Reset-disabled blocks will not come up until some byte has been written to port 40H, after which they will remain enabled until the next reset regardless of any writes to port 40H.

3.2 CCS SYSTEM 300/400 WITH CP/M

When this single-user system is powered on or reset, the Boot ROM, which resides at F000H, asserts PHANTOM* to disable identically-addressed system memory. (The 2805, on which the Boot ROM is located, includes a power-on glide circuit which causes a "jump" to F000H after power-on or reset.) Thus, for the 2066 to work in this environment, the upper 16K block must be disabled by PHANTOM*. For use in a CCS System 300 or 400 with CP/M, the 2066 should therefore be configured as follows:

BLOCK	BASE	BANK	RESET	PHTM
A	0000H	0*	EN	OFF**
B	4000H	0*	EN	OFF
C	8000H	0*	EN	OFF
D	C000H	0*	EN	ON**

* The note to Section 3.1 applies in this case as well.

** In early versions of the CCS 300/400 the Boot ROM is located on the 2422 and is addressed at 0000H. To use the 2066 in these early systems, set A PHTM to ON and D PHTM to OFF.

3.3 CCS SYSTEM 300/400 WITH MP/M

MP/M boots the same way as CP/M. However, with M/PM there is the additional consideration of the user-shared system load. The operating system must reside in the last 16K of all banks and always be accessible.
Configuration for First Board (Bank 0):

BLOCK	BASE	BANK	RESET	PHTM
A	0000H	0	EN	OFF**
B	4000H	0	DIS	OFF
C	8000H	0	DIS	OFF
D	C000H	ALL*	EN	ON**

* Leaving the D pin of the Bank Select header unconnected causes Block D to occupy addresses C000-FFFFH in all banks.

** The note to Section 3.2 applies in this case as well.

CHAPTER 4

HARDWARE DESIGN

The 2066 provides 64K of dynamic RAM memory divided into four separately addressed, separately banked 16K blocks. Because of the requirements of dynamic RAM and the user-configurable options which give the board its flexibility, the circuitry of the 2066 is rather complex. For the purposes of explanation, the operation of the 2066 can be divided into four main functions: bank selection, block enabling, memory accessing, and memory refreshing. The following descriptions of the circuitry performing these functions are intended to give the reader a general sense of what the logic does and why it does it; the details of the circuitry are presented in the schematic/logic diagram in Appendix A. We recommend that readers of this chapter frequently consult the logic diagram during their reading.

4.1 BANK ENABLING

The 2066 is compatible with systems using a bank-port/bank-byte scheme to provide for memory expansion up to 512K. (See Section 1.1 for an explanation of this bank select scheme.) Each bank consists of up to 64K of memory. Because memory addresses within the banks are identical, no two banks having memory occupying the same addresses can be enabled at the same time. One physical block of memory can occupy the same addresses in more than one bank, however.

4.1.1 Bank Port Addressing

On the 2066 the bank port is user-selected. Jumper settings determine for which address byte A7-A0 the outputs of the open collector address-comparison gates will all be high. The outputs of the address-comparison gates are tied together to form the PORT SELECT line. This line, however, is active whenever A7-A0 match the jumper settings, which means it could be active in M1 and memory cycles as well as in I/O cycles. Therefore PORT SELECT is NANDed with pWR* inverted and sOUT to form the BANK CLOCK* line. BANK CLOCK*, returning high when pWR* goes inactive, clocks the four Bank Enable Flip-Flops A-D (U36,U37).

4.1.2 Bank Selection

The D input to each Bank Select Flip-Flop is independently controlled by the Bank Select Header (J1), a 16-pin DIP header which allows the user to control each flip-flop's D input with a specific bit of the bank byte or with a signal from one of the two Multi-Bank Headers (see Sections 2.1.1 and 2.2.1). The Bank Select Header pins labeled A-D--called "block pins"--control the D inputs of the Bank Select Flip-Flops. The other pins of the header--called "bank pins"--are controlled by the data lines, either directly (pins 0-7 being high when the corresponding data bit is high) or through the Multi-Bank Jumpers (pin M1/M2 being high when one of the selected data bits is high). Whenever the bank pin tied to a block pin is high during a write to the bank port, a high will be clocked into the flip-flop. Likewise, if a block pin is left unconnected, a high will be clocked into the flip-flop, the D input being held high by a pull-up resistor. When a high is clocked into a Bank Select Flip-Flop, its Q output goes high. The Q outputs of the Bank Select Flip-Flops are the BANK SELECTED signals for the four memory blocks.

The BANK SELECTED signal may also be asserted or cleared after a system or peripheral reset, depending on the setting of the block's Reset jumper. A Reset jumper set to E connects the reset signal (controlled by SLAVE CLR* unless RESET* is jumpered in instead) to the corresponding flip-flop's PRESET input, asserting BANK SELECTED after a reset. A Reset jumper set to D connects the reset signal to the flip-flop's CLEAR input, clearing BANK SELECTED after a reset.

Whenever a BANK SELECTED signal is asserted, an LED for that block lights. The LED remains lit as long as the block's

install jumpers between the center pads and the pads toward the top of the board.

The Block A and Block C Reset and DMA Enable jumpers also affect Block B and Block D when 32K bank-blocks are selected. The Block Address and PHANTOM-sensitivity jumpers are not affected by the configuration of the 32K Bank-Block Jumpers.

2.3.5 The DMA Enable Jumper Pads (W,X)

These jumpers, like the 32K Bank-Block jumpers, allow emulation of a Cromix system memory board, and are meant to be set in conjunction with the 32K Bank-Block jumpers. When the Cromix operating system is loaded, an image is written to the lower 16K of each bank which is set to be selected during DMA. Rather than sharing the 16K of memory in which the operating system is stored, each user has his own copy of the operating system. The DMA Enable jumpers allow the 2066 to emulate Cromix system memory and accept a copy of the operating system when it is loaded in.

The DMA Enable jumpers are hard-wired for the D settings (block disabled by DMA), which is standard for non-Cromix systems. Cromix users should cut the traces between the D pads and install jumpers between the E pads.

2.3.6 The REFRESH Jumper Pads

The REFRESH* bus signal indicates when a dynamic memory refresh may be performed transparent to the CPU. Both the CCS CPU boards, the 2820 and the 2810, support this line. However, many systems, especially 8080-based systems, do not support REFRESH*. If your system does not support REFRESH*, you will need to cut the trace between the REFRESH jumper pads. This disconnects the bus line from on-board circuitry, preventing noise or invalid signals on the line from initiating a refresh operation at an inappropriate time. Necessary memory refreshing will be controlled by other bus signals; no degradation of refresh capability will result.

2.3.7 The M1 RAS Jumper Pads (U)

These pads are hard-wired closed. If the 2066 is used with an Alpha-Micro CPU the trace between these pads should be cut. In all other cases the pads should be left closed.

Additional Boards:

The general principles to follow when adding additional boards are: 1) no other memory block should be assigned to addresses C000H-FFFFH; 2) all blocks should be disabled on reset; 3) no block should be assigned to more than one bank. The following shows one possible configuration for three additional 2066 boards.

BLOCK	BASE	BANK	RESET	PHTM
A	0000H	1	DIS	OFF
B	0000H	2	DIS	OFF
C	0000H	3	DIS	OFF
D	0000H	4	DIS	OFF
A	4000H	1	DIS	OFF
B	4000H	2	DIS	OFF
C	4000H	3	DIS	OFF
D	4000H	4	DIS	OFF
A	8000H	1	DIS	OFF
B	8000H	2	DIS	OFF
C	8000H	3	DIS	OFF
D	8000H	4	DIS	OFF

3.4 CCS SYSTEM 300/400 WITH OASIS

OASIS boots up the same as MP/M and CP/M; however, the OASIS operating system resides in the first 16K. Thus the configuration for OASIS is the same as the configuration for MP/M except that the memory in the 0000-3FFFH block, rather than that in the C000-FFFFH block, is shared by all banks.

Configuration of First Board (Bank 0):

BLOCK	BASE	BANK	RESET	PHTM
A	0000H	ALL*	EN	OFF**
B	4000H	0	DIS	OFF
C	8000H	0	DIS	OFF
D	C000H	0	DIS	ON**

* Leaving the A pin of the Bank Select Header unconnected causes Block A to occupy addresses 0000-3FFFH in all banks.

** The note to Section 3.2 applies in this case as well.

Additional Boards:

The general principles to follow when adding additional boards are: 1) no other memory block should be assigned to addresses 0000H-3FFFH; 2) all blocks should be disabled on reset; 3) no block should be assigned to more than one bank. The following shows one possible configuration for three additional 2066 boards.

BLOCK	BASE	BANK	RESET	PHTM
A	4000H	1	DIS	OFF
B	4000H	2	DIS	OFF
C	4000H	3	DIS	OFF
D	4000H	4	DIS	OFF
A	8000H	1	DIS	OFF
B	8000H	2	DIS	OFF
C	8000H	3	DIS	OFF
D	8000H	4	DIS	OFF
A	C000H	1	DIS	OFF
B	C000H	2	DIS	OFF
C	C000H	3	DIS	OFF
D	C000H	4	DIS	OFF

Note: OASIS allows up to 16 banks. To implement more than 8 banks, you will need to dedicate a second bank port for banks 9-16. See Section 2.3.1 for instructions. While MP/M also allows more than eight banks, it is highly unlikely that more than eight banks would be implemented in an MP/M system.

bank is selected regardless of whether on-board memory is actually accessed.

4.2 MEMORY BLOCK ENABLING

The enabling of a memory block depends on several conditions. The block's BANK SELECTED signal, which may be modified by block size and DMA-select circuitry included for Cromix memory emulation, must be active, address comparison outputs must be active, and PHANTOM* must be inactive if the block is Phantom-enabled in the hard mode. When all of these conditions obtain for a given block, that block's BLOCK ENABLE* signal goes active, allowing the RAM chips in the block to be addressed.

4.2.1 Block Size (Cromix Compatibility)

If the 2066 is used with Cromemco memory in a Cromix system, memory block size must be altered from 16K to 32K for banking purposes. Jumper pads have been included on the 2066 to allow this. Normally, each block's BANK SELECTED signal is input to a separate NAND gate, the output of which is the BLOCK ENABLE* signal for that block. However, the Block B and Block D BANK SELECTED inputs may be replaced by the Block A and Block C inputs respectively. Thus Blocks A and B and Blocks C and D may be banked as two 32K blocks, the bank assignments being determined by the A and C block pins of the Bank Select Header. Block size does not affect addressing; the four 16K blocks are still independently addressed.

4.2.2 DMA Select (Cromix Compatibility)

When the 2066 is used in a Cromix system with Cromemco memory boards, provision must be made for enabling of the lower 32K block of each bank during DMA in order to ensure that the operating system may be loaded into the lower 16K of each memory bank. Two jumpers allow the user to select whether pHLDA is ANDed or ORed with the BANK SELECTED lines for Block A and Block C; thus the jumpers determine whether, during DMA, a block is automatically selected or deselected. If a block is selected during DMA, it will respond whenever addressed during DMA regardless of whetner its bank has been

selected previous to the DMA operation; if it is deselected, it cannot be addressed during the DMA operation, but will return to its pre-DMA state when the DMA operation is completed and the permanent bus master regains the bus. If neither side of the jumper is closed, a block will retain its pre-DMA state through the DMA operation.

4.2.3 Block Addressing

Jumpers allow the user to select the base address of each 16K block by determining which combination of address bits A15 and A14 will cause two highs to be input to the block's address comparison gate. When the states of A15 and A14 match the jumper settings for a block, the output of that block's address comparison gate is active.

4.2.4 Phantom-Sensitive Memory

The bus signal PHANTOM* is asserted by another device on the bus to disable identically-addressed memory. On the 2066 each 16K block is independently set as either PHANTOM-sensing or not by the Phantom Enable Jumpers. PHANTOM* active when a Phantom-sensing block is addressed does not automatically stop locations on that block from being accessed, however. If the Write Phantom Jumper is set to D, selecting the soft Phantom mode, PHANTOM* active prevents the Data In Buffer from passing data onto the system DI lines. In this implementation, appropriate when the PHANTOM*-asserting device is a ROM, PHANTOM* active will have no effect on a write to the board, allowing ROm contents to be copied into RAM at the same location if desired.

In some cases, however, the overlaying memory will be RAM, and it will be necessary to block response of Phantom-sensing memory during write cycles as well. This is the hard Phantom mode, selected when the Write Phantom Jumper is in the E position. When the hard Phantom mode is selected on the 2066, the board comes up after power-on or reset in the soft Phantom mode, allowing the Boot ROM to copy itself into RAM at the same location. The hard Phantom mode is initiated by the first write to the bank port, which clocks a low into the Write Phantom Flip-Flop; the board remains in the hard Phantom mode until a system reset sets the Write Phantom Flip-Flop.

4.3 THE RAM ARRAY

Each 4116 dynamic RAM has 16K locations arranged 16K x 1--i.e., each 4116 has a single data input/output. Therefore, each 16K block consists of eight 4116s, each one tied to a different line of the internal bi-directional data bus. To address one of the 16K locations on a chip, a fourteen-bit address is required. In order to minimize the number of pins required, the 4116 employs a multiplexed addressing scheme: a seven-bit row address followed by a seven-bit column address selects the memory location to be accessed. Two inputs, RAS* and CAS* (Row and Column Address Strobes), determine whether the address inputs to an enabled chip will be considered a row address or a column address.

4.3.1 RAS* Generation

Separate flip-flops control RAS* generation for the three memory-access operations Memory Read, Memory Write, and Op Code Fetch (M1). Each flip-flop monitors for a specific situation during which RAS* must be generated. The flip-flops are wired so that a Write RAS condition forces an M1 RAS condition which in turn forces a Read RAS condition. It is the output of the Read RAS Flip-Flop that controls the RAM RAS* inputs and related on-board logic.

The Write RAS Flip-Flop (U13b) is clocked by pWR* going active when MWRITE active indicates a memory write operation. Unless the bus is being transferred from one master to another (i.e., CDSB* and pHLDA the same state), a low will be clocked into the flip-flop, asserting WR RAS* (Q output low). WR RAS* active clears the M1 RAS flip-flop, asserting M1 RAS*.

The M1 RAS Flip-Flop (U13a) is clocked by pSYNC going active during an M1 cycle. Unless a bus transfer is in progress, a low will be clocked into the flip-flop, causing M1 RAS* to be asserted (Q output low). M1 RAS* active low sets the Read RAS Flip-Flop, forcing RD RAS* low. Generation of M1 RAS* can be disabled if necessary (see Section 2.3.7).

The Read RAS Flip-Flop (U10b) is clocked when sMEMR (or pDBIN, if jumpered to replace sMEMR) goes active; unless sM1 is active or the bus is being transferred, a high will be clocked into the flip-flop, asserting RD RAS* (Q* output low). READ RAS* controls directly the RAS* inputs of the RAM chips.

The signals sMEMR and pDBIN are generated somewhat

differently in Z-80 and 8080 CPUs, and the differences are significant enough that neither signal can be used by the 2066 in both environments. In 8080-based systems sMEMR does not always change state between cycles, making it unusable as a clocking signal. In Z-80-based systems, the presence of pDBIN in Interrupt Acknowledge cycles will cause problems. Therefore, a jumper has been provided to allow selection of sMEMR in Z-80-based systems and pDBIN in 8080-based systems. Note that RD RAS* will be asserted during I/O reads as well as during memory reads in 8080-based systems; however, data will be put on the internal bus only if CAS* is also asserted, which does not occur during I/O cycles.

4.3.2 CAS* Generation

The RAS* signal input to the memory chips also clocks the monostable multivibrator (U9b) which generates CAS*. The multivibrator generates two pulses, a high pulse at Q and a low pulse at Q*, the width of the pulses being determined by the values of the external capacitor and resistors. The low pulse is used to turn off RAS* and for additional functions during memory refresh operations; it will be discussed later. The high pulse is used to generate CAS*.

There are two timing requirements to be met by CAS* as it is input to the memory chips: first, it must follow RAS* by a certain amount of time; second, it must be of a certain duration. The second of these requiremnts is met by the width of the CAS* pulse from the multivibrator; the first is met by the gate delays between the generation of the pulse and its being input to the memory chips.

The gates through which the CAS* pulse passes serve more than timing purposes, of course. The first (U30b) blocks CAS* generation during memory refresh operations. The next (U34c) blocks CAS* generation during non-I/O cycles as well as when the addressed block is Phantom-sensitive and PHANTOM* is active. Finally, the pulse, active low at this point, is ORed with the BLOCK ENABLED* lines (U33a-d), ensuring that CAS* is applied only to the addressed block.

4.3.3 RAS* and CAS* Removal

CAS* is originally generated as a pulse and therefore needs no additional logic to provide for its removal at the proper time. RAS*, however, is generated by flip-flops and will remain until removed by additional logic. (Re-clocking of the flip-flop involved may also remove the RAS* signal, but much too late.) To remove RAS* at the proper time, a second multivibrator (U9a) is used. The second multivibrator puts out a low pulse at Q* shortly after being clocked by the falling edge of the low pulse from the CAS multivibrator. This pulse resets the Write RAS* and M1 RAS* Flip-Flops and and clears the Read RAS* Flip-Flop, forcing RAS* inactive. The length of the pulse ensures that the required delay between the removal and reassertion of RAS* is observed.

4.3.4 Address Bus Multiplexing

Generating the Row and Column Address Strobes is only half of addressing a RAM location; it is also necessary to ensure that half of the fourteen address bits are on the internal address bus when each strobe is asserted. (It doesn't really matter which bits are used for the row address and which for the column.) On the 2066, the Row Address Buffers (U67 and U68, pins 11-19) are usually enabled; they are tri-stated only during refresh time and when the inital CAS pulse from U9b is active. The Column Address Buffers (U67 and U68, pins 1-9) remain tri-stated except when CAS is active during a non-refresh cycle. Thus the row address is already present on the bus when RAS* is applied to the memory chips, and remains on the bus until shortly before CAS* is applied, when the column address is gated onto the bus. During refresh time both the Row and Column Address Buffers are tri-stated.

4.3.5 Data Bus Buffering

The S-100 Data In and Data Out lines are buffered and then tied together to form the on-board bi-directional data bus. The Data Out Buffer (U71) is enabled when both MWRITE and pWR* are true--i.e., when valid data is present during a memory write cycle. The Data In Latch (U72) is enabled when six conditions are met: 1) the CAS pulse is active; 2) pDBIN is active; 3) the current cycle is not an I/O cycle; 4) a refresh operation is not in progress; 5) an Interrupt

Acknowledge is not in progress; and 6) one of the memory blocks has been selected and not Phantom-overlain. Data is clocked at the end of the CAS pulse and is held for the duration of sMEMR (or pDBIN in 8080-based systems) active.

4.4 MEMORY REFRESHING

Because the capacitors used in dynamic RAM will leak and lose their charge after a certain period of time, the memory cells must be periodically read and then restored to their proper voltages. This process is called refreshing the memory. The cells of the 4116 chips used on the 2066 must be refreshed every 2 milliseconds. The 4116 employs what is called RAS*-Only Refreshing: when RAS* is applied to a chip for the proper length of time, all cells in the addressed row are refreshed. If the rows are addressed sequentially, refreshing one row every 16 microseconds will guarantee that all cells will be refreshed at least once every 2 milliseconds.

4.4.1 Transparent Memory Refreshing

The desirable way to refresh memory is to make the refresh operation transparent to the CPU--i.e., to refresh the memory in such a way that CPU operation is not affected. The best time to do this is during the second half of an M1 cycle, when the CPU is occupied with internal operations. The Z-80 CPU simplifies memory refreshing by providing a signal, REFRESH*, active during the second half of M1. 8080 CPUs do not provide a refresh signal, so dynamic memory boards designed to work in 8080-based systems must include logic that produces an on-board signal analogous to the Z-80 REFRESH* signal.

The 2066 will work with either Z-80 or 8080 CPUs. The on-board refresh control signals are the outputs of the Refresh Flip-Flop (U10a). If the Z-80 REFRESH* signal is present on bus line 66, the Refresh Flip-Flop will be set by a low at its PRESET* input as long as REFRESH* is active. In the absence of the REFRESH* signal, the Refresh Flip-Flop will still be set during the second half of M1 cycles, in this case by the trailing edge of sMEMR (or pDBIN in 8080-based systems) clocking in sM1 active.

Refresh Flip-Flop outputs Q and Q* are used to generate RAS* and to ensure that the refresh address is put on the bus at the proper time. The high at Q increments the Refresh Address Counter and disables the Row Address Buffers. The low at Q* disables CAS* generation and the Column Address Buffers, enables the Refresh Address Buffers, disables the Data In Buffer, and asserts RAS* by clearing the Write RAS Flip-Flop. Gate delays ensure that the refresh address gated from the Refresh Address Counter onto the internal data bus will be stable before RAS* is applied to the memory chips. RAS* is turned off during refresh operations in the same way as it is in memory access cycles.

4.4.2 Asynchronous Memory Refreshing

During long wait states, more than 16 microseconds may elapse between M1 transparent refreshes, which could lead to the destruction of memory contents. To prevent this, the 2066 includes circuitry which automatically initiates a refresh operation if one does not occur within 16 microseconds of the preceding refresh. A counter (U11) divides the 2 MHz clock from the bus by 4 to produce a clock with 2 microsecond cycles. This clock signal is used to clock an eight-bit shift register (U38). The shift register is cleared after every memory access and refresh by the active low pulse from the Q* output of the CAS Multivibrator (U9a). When the pulse goes high again, the eight shift register outputs pulse high sequentially at 2-microsecond intervals.

Unless the shift register is cleared again during the first 12 microseconds after a clearing signal is withdrawn, the second-to-last pulse (pin QG going high) will be clocked into the Refresh Wait Flip-Flop (U20b), the resulting low at Q* forcing bus line RDY low and thereby causing the CPU to wait while the refresh occurs. When the last pulse (pin QH) goes high, the Refresh Flip-Flop is set, and a refresh operation proceeds as described in Section 4.4.1. The low pulse from the Remove RAS Multivibrator (U9a) clears the Refresh Wait Flip-Flop, allowing RDY to return high.

Asynchronous memory refreshing is disabled during DMA operations by HOLD* active, which disables the counter U11. Disabling asynchronous refreshes during DMA is necessary because the RDY bus signal asserted low by the 2066 during asynchronous refreshes is ignored by many DMA devices. Attempting an asynchronous refresh operation without being able to make the bus master wait until the refresh is finished could cause problems. No asynchronous memory refreshing should be required during DMA operations, however, as either

source or destination memory will be accessed sequentially, providing sufficient transparent refreshing as long as no extended waits occur.

APPENDIX A

TECHNICAL INFORMATION

A.1 USER-REPLACEABLE PARTS

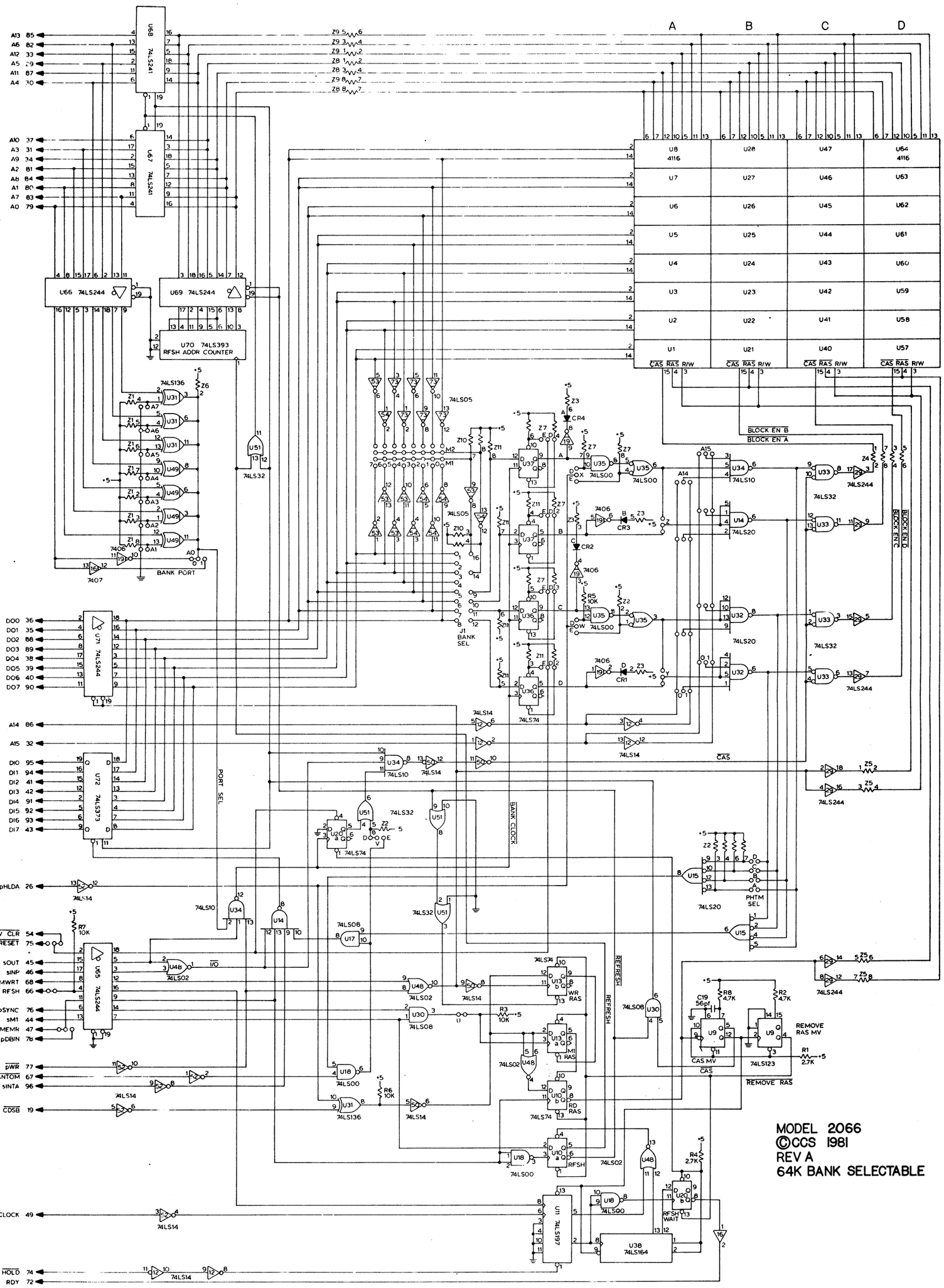
QTY	REF	DESCRIPTION	CCS PART #
INTEGRATED CIRCUITS			
32	U1-8,21-8, 40-7,57-64	4116 RAM, 200 ns	31900-41162
2	U18,35	74LS00	30000-00000
1	U48	74LS02	30000-00002
2	U18,35	74LS00	30000-00000
3	U53,54,73	74LS05	30000-00005
1	U19	7406	30200-00006
1	U16	7407	30000-00007
2	U17,30	74LS08	30000-00008
1	U34	74LS10	30000-00010
3	U12,50,52	74LS14	30000-00014
3	U14,15,32	74LS20	30000-00020
2	U33,51	74LS32	30000-00032
5	U10,13,20, 36,37	74LS74	30000-00074
1	U9	74LS123	30000-00123
2	U31,49	74LS136	30000-00136
1	U38	74LS164	30000-00164
1	U11	74LS197	30000-00197
2	U68,69	74LS241	30000-00241
5	U29,65-7,71	74LS244	30000-00244
1	U72	74LS373	30000-00373
1	U70	74LS393	30000-00393
1		7805 +5V Regulator	32000-07805
1		7812 +12V Regulator	32000-07812
1		79L05 -5V Regulator	32000-17905
CAPACITORS			
46		Mono, .1 uf, 50 VDC, 20%	42034-21046
6	C24,25,35, 40,42,56	Tant, 4.7 uf, 35 VDC, 20%	42804-54756
1	C19	Mica, 56 pf, 500 VDC	42215-55605

QTY	REF	DESCRIPTION	CCS PART #
RESISTORS			
2	R1,4	2.7 Kohm, 1/4 w, 5%	40002-02725
2	R2,6	4.7 Kohm, 1/4 w, 5%	40002-04725
4	R3,5-7	10 Konm, 1/4 w, 5%	40002-01035
4	Z4,5,8,9	Net, 33 ohm x 4, 10%	40931-43305
4	Z1,2,7,11	Net, 4.7 Kohm x 7, 20%	40930-74726
2	Z6,10	Net, 1 Kohm x 7, 20%	40931-71025
1	Z3	Net, 220 ohm x 5, 20%	40931-52205
MISCELLANEOUS			
33		IC Socket, 16 pin	58102-00160
4		LED, 1/4 in, red	37400-00001
1		Header, 2 x 8 DIP	55000-10000
3		Header Strip, 2 x 8	56004-02008
1		Header Strip, 1 x 8	56004-01008
5		Header Strip, 1 x 4	56004-01004
2		Header Strip, 1 x 3	56004-01003
25		Jumper Plug	56200-00001
2		Heat Sink, TO-220	60022-00001
2		Screw, 6-32 x 3/8	71006-32061
2		Nut, 6-32	73006-32001
2		PCB Extractor	60010-00001
2		PCB Extractor Roll Pin	60100-00000

A.2 RAM CHIP IDENTIFICATION TABLE

	BLOCK			
DATA BIT	A	B	C	D
7	U1	U21	U40	U57
6	U2	U22	U41	U58
5	U3	U23	U42	U59
4	U4	U24	U43	U60
3	U5	U25	U44	U61
2	U6	U26	U45	U62
1	U7	U27	U46	U63
0	U8	U28	U47	U64

A.3 SCHEMATIC/LOGIC DIAGRAM


A
B
C
D
U8 4116
U28
U47
U64 4116
U7
U27
U46
U63
U6
U26
U45
U62
U5
U25
U44
U61
U4
U24
U43
U60
U3
U23
U42
U59
U2
U22
U41
U58
U1
U21
U40
U57
CAS RAS R/W
U68 74LS241
U67 74LS241
U66 74LS244
U69 74LS244
U70 74LS393
RFSH ADDR COUNTER
74LS136
74LS32
74LS05
74LS00
74LS10
74LS20
74LS74
74LS244
74LS14
74LS373
74LS02
74LS08
74LS123
74LS164
74LS597
BANK PORT
J1 BANK SEL
BLOCK EN B
BLOCK EN A
PORT SEL
BANK CLOCK
REFRESH
CAS
PHTM SEL
REMOVE RAS
WR RAS
RD RAS
RFSH
RFSH WAIT
CAS MV
REMOVE RAS MV
MODEL 2066
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REV A
64K BANK SELECTABLE