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**OWNER'S MANUAL**

**Model 2065**

**64K Static RAM Module**

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**California Computer Systems**

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**CCS'S MODEL 2065  
64K DYNAMIC RAM  
OWNER'S MANUAL**

**CALIFORNIA COMPUTER SYSTEMS  
250 CARIBBEAN DRIVE  
SUNNYVALE, CA 94086**

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## INTRODUCTION TO THE 2065

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CCS's 2065 64K Dynamic Ram board provides your S-100 system with 64K bytes of reliable, high-speed dynamic RAM. Compatible with most of the major S-100 systems on the market, including those with front panels, it supports DMA operations and requires no wait states with 4 MHz microprocessors.

The 2065 is designed for memory expansion; it allows you to expand your memory up to 512K. Through the bank select system, you can hardware-assign your board to any of eight levels of 64K and then activate the banks under program control. An on-board LED indicates when a bank the 2065 resides in is selected. The 2065's bank select system is compatible with the bank select systems used by Cromemco, North Star, and others.

In addition, the 2065 gives you flexible memory. Any 16K memory block can be completely disabled or can be made independent of the bank select system, allowing it to be enabled any time it is addressed, regardless of which bank is selected. All 64K can also be enabled every time you turn on or reset your system, without the board's bank being software-selected first. An on-board LED indicates when enabled memory on the 2065 is selected.

The 2065 also gives you reliable memory. Its dynamic memory refresh circuitry provides processor-transparent refreshes during normal operations with an 8080 or Z-80™ CPU. (Note: The 2065 requires that a Z-80 CPU output the control signal REFRESH on pin 66 of the system bus.) The refresh circuitry also provides for memory refresh during DMA and extended wait states when normal refresh generation is inhibited.

™Z-80 is a trademark of Zilog, Inc.

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# CHAPTER 1

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## BOARD SETUP

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The 2065 dynamic RAM board has a number of features that must be jumper configured or selected. This chapter discusses each of these features in turn. At the end of the chapter, Figure 1-2 shows the jumper locations, while Figure 1-1 illustrates the recommended jumper configuration for the 2065 when it is used in CCS's System 2210 or with the 2810 Z-80 CPU and 2422 Floppy Disk Controller set. To configure a jumper, place the jumper plug on the pins that select the option you desire.

### 1.1 BANK SELECT JUMPERS

The 2065's 64K of memory can be assigned to any of eight 64K memory banks, allowing memory expansion to 512 Kbytes. Which memory bank is active at any time depends on the Bank Select Byte last output to the Bank Port. Bits 0-7 of the Bank Select Byte correspond to the bank levels 0-7. A bit set to 1 activates its corresponding bank; set to 0, it deactivates the bank. The BANK BYTE SEL jumpers D0-D7 allow you to select which bit of the Bank Select Byte this board will respond to; in other words, they allow you to hardware-assign this board to any bank. For example, placing the jumper plug on the D0 pins assigns your board to bank 0. The output of the Bank Select Byte 00000001b to the Bank Port will then enable the board and light the Bank LED.

The address of the Bank Port is also jumper-selectable. Set jumpers A7-A0 to the desired binary address. For example, both Cromemco and CCS systems address the Bank Port at 40h (01000000b); a 2065 board used in these systems should have A7-A0 set to 01000000. Presuming the board is assigned to bank 0, the following Z-80 instructions would activate the board while simultaneously deactivating any other board:

```
LD  A,00000001B      ;load accumulator with Bank Select Byte
OUT 40H,A           ;output the Bank Select Byte to Bank Port
```

Note that after the OUT instruction, the CPU fetches its next instruction from the address next in sequence, even though it is now fetching its instructions from a different memory bank. Be careful to ensure program continuity after switching banks.

The 2065 board comes with only one jumper plug for jumpers D0-D7, since applications which need 64K of memory assigned to more than one bank are rare. However, you may assign the 2065 to more than one bank if you wish. We recommend that you do not assign memory with overlapping address space to the same bank, since memory conflicts would probably occur.

## 1.2 BLOCK SELECT JUMPERS

The 2065 allows any 16K block to be made independent of the bank select system, so that it is enabled any time it is addressed, regardless of which bank is currently selected. This makes it possible to do time-sharing in which certain blocks are held reserved for an individual user (bank-dependent blocks) and certain blocks are used in common (bank-independent blocks). To make a 16K block bank independent, set its corresponding BLOCK SELECT jumper (Block 1 = 0000-3FFFh) to ME (Memory Enable); to make it bank dependent, set its jumper to BE (Bank Enable). If you remove its jumper plug entirely, the block is disabled.

## 1.3 BANK RESET JUMPER

The bank reset circuitry allows you to disqualify the bank select circuitry whenever the system is turned on or reset. If you enable the reset circuitry, all memory blocks on the 2065 board come up enabled on power-on or reset, regardless of whether they are bank dependent or not. If you disable the reset circuitry, bank-dependent blocks are enabled only if you select the board's bank. To enable the reset circuitry, place the RESET jumper plug at position ON.

## 1.4 PHANTOM ENABLE JUMPER

The input PHANTOM allows an outside memory device capable of generating the signal to selectively overlay any portion of the 2065's memory space. Whenever such a memory device is addressed during a memory cycle, it outputs the PHANTOM signal, disabling the 2065's output bus for that cycle if the PHANTOM jumper is set to ON. The use of the PHANTOM overlay makes it unnecessary to disable a complete 16K block because

it shares part of its memory space with another device; only those locations shared in common will be disabled on the 2065 by the PHANTOM overlay. Whether or not you want to enable the PHANTOM line depends on the boards you have in your system; consult your manuals. To enable the PHANTOM line, set the PHANTOM jumper to position ON.

### 1.5 CPU SELECT JUMPER

We have designed the 2065 board so that its read cycle can be started by either sMEMR or pDBIN. Using sMEMR to start a read cycle often increases memory access time when the board is used with a Z-80 CPU. However, in an 8080 CPU, sMEMR does not change state between two consecutive memory cycles. Thus pDBIN must be used with an 8080 CPU. Setting the CPU SEL jumper so that it selects your type CPU allows the appropriate signal to begin an access cycle during memory reads.

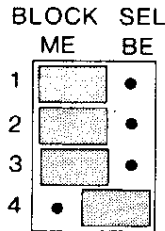
### 1.6 CONFIGURING THE 2065 TO WORK WITH THE 2810 OR 2422

To work with either the 2810 Z-80 CPU or the 2422 Floppy Disk Controller, the 2065 must not conflict with either board's Monitor ROM when it is enabled (both ROMs reside at F000h). At the same time, some low RAM must be available to the Monitor ROMs on system power-on or reset. If your system contains only the 2810, your task is simple: you must permanently disable the last 16K block (Block 4) and enable at least the first 16K (Block 1). If you have, however, CCS's system 2210 (the 2810, the 2422, and CP/M<sup>™</sup> software), you want to be able to re-enable the last 16K once CP/M is booted in and the monitor ROM is disabled. There are several configurations of the 2065 that will achieve this end: all four blocks can be enabled, for example, and PHANTOM can be used to shadow out the RAM while the ROM is active. Another method is supported by the controller-unique software provided with the 2422. When the system loader from the disk starts executing, it disables the Monitor ROM by outputting 01h to port 40h. This write to port 40h can be used also to enable any bank-dependent memory on the 2065. Thus if Block 4 is made bank-dependent and disabled on reset, it will not be enabled until the system loader disables the ROM. Table 1-1 shows the settings of the 2065 jumpers which support this method.

<sup>™</sup>CP/M is a trademark of Digital Research, Inc.

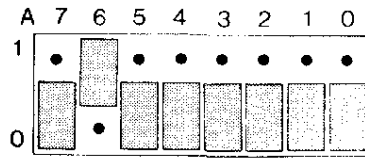
2065 BOARD CONFIGURATION FOR CCS SYSTEM 2210

① BLOCK SELECT



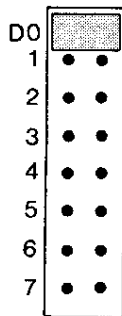
Block 4 bank-dependent; Blocks 1, 2, and 3 bank-independent.

② BANK PORT ADDRESS



Bank port address set to 40h.

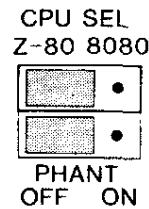
③ BANK BYTE



BANK BYTE SEL

Bank 0 selected.

④ CPU SELECT AND PHANTOM ENABLE



Configured for Z-80 CPU;  
PHANTOM disabled.

⑤ BANK RESET

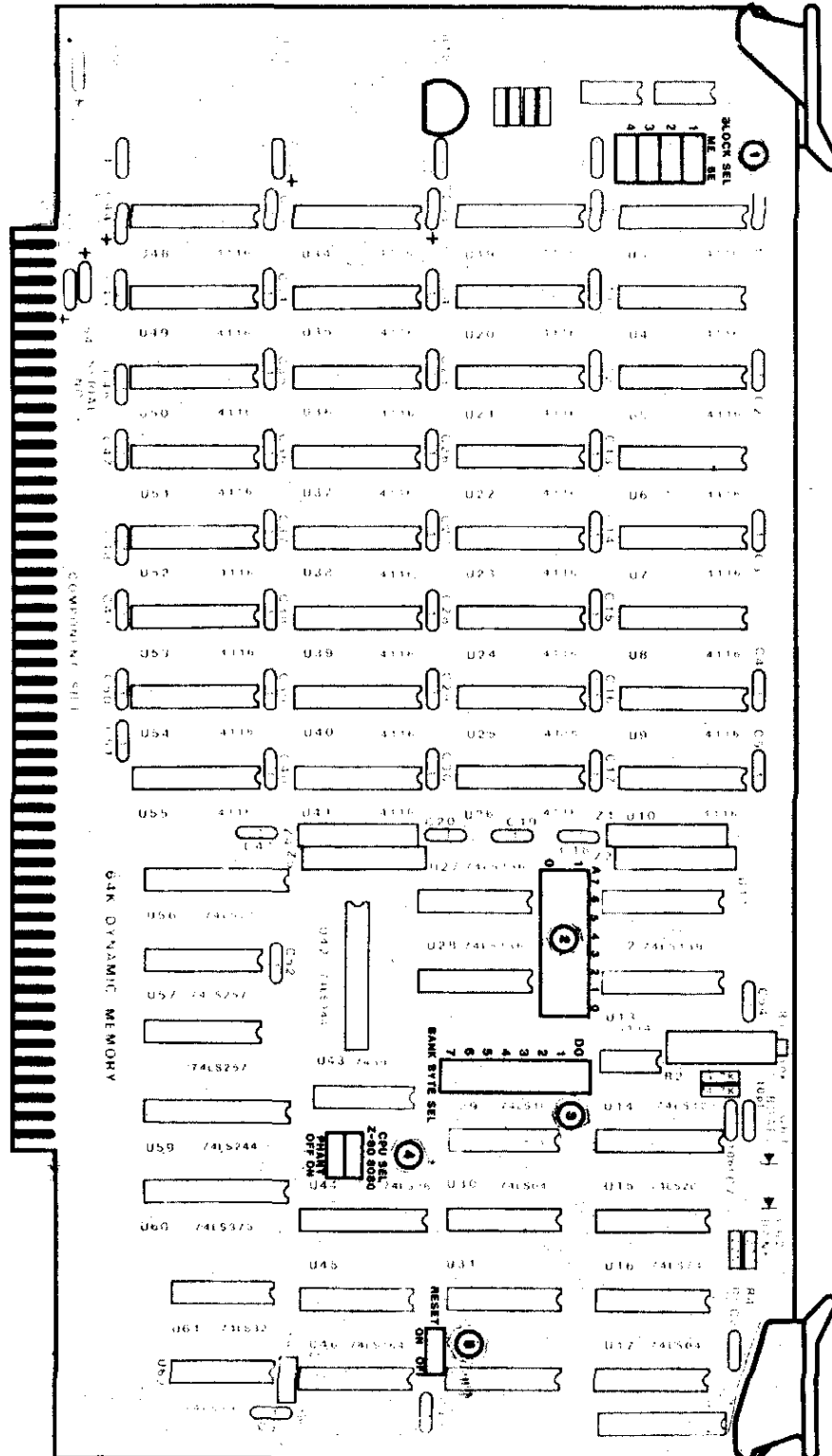


Board bank-disabled on system reset.

TABLE 1-1



FIGURE 1-2 JUMPER LOCATIONS



# CHAPTER 2

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## THEORY OF OPERATION

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In this chapter, active low signals are indicated by either an asterisk after the signal name or a bar over it. We have assumed that you are familiar with the S-100 signals used by the 2065 board; if you are not, you will find short definitions of the signals in the appendix.

### 2.1 THE RAM ARRAY

The memory array consists of four blocks of eight 16K x 1-bit dynamic RAMs. The Data In lines and the Data Out lines of the four chips that share a data bit position are bussed together, creating an internal 8-bit bi-directional data bus. The control and address lines for the eight chips in a 16K block are also tied together, creating one set of control and address lines for the block, while the regulated +5, -5, and +12 volts are distributed equally to all the chips. As a trouble shooting aid, Figure A-1 in the appendix shows which chips respond to a given address and store a given data bit.

### 2.2 ADDRESSING THE MEMORY

#### 2.2.1 THE RAM ADDRESS BUS

The industry standard 16K x 1-bit dynamic RAM used on this board is housed in a 16-pin package to provide high density and low cost. In order for the RAM to be housed in such a small package, the 14 address bits needed to address 16K of memory are multiplexed onto seven address lines. The internal memory of the RAM chips can be thought of as a 128 x 128 matrix, with each location being specified by 7-bit row and column addresses. Address bits A0-A6 form the row

address; bits A7-A13 the column address. The memory chips require that the row address bits be multiplexed first onto RAM address lines. Once the address bits are stable, the control input RAS\* (Row Address Select) is then pulled low to strobe the bits the chips' internal row address registers. After a minimum length of time the address bits on the RAMs' address lines should change to column address bits and the control input CAS\* (Column Address Select) should then be pulled low to strobe the column address bits into the chips' internal column address registers. (See Figure 2-1).

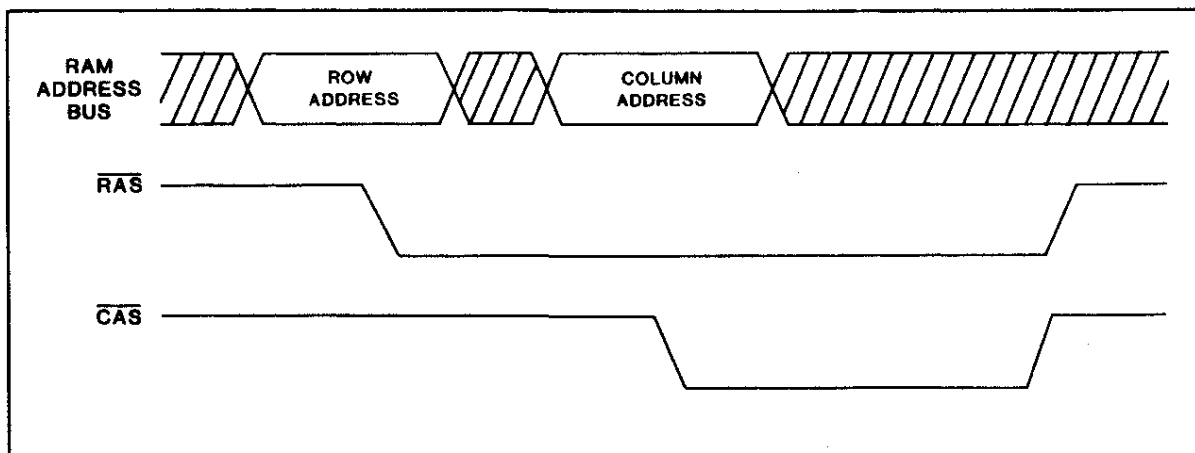


FIGURE 2-1 RAS AND CAS TIMING

On the 2065, the RAM chips' address lines are tied together, creating a 7-bit RAM address bus. The multiplexing of the row and column address bits from the system bus onto the RAM address bus is controlled by an 8-to-4-line multiplexer, U57, and a 6-to-3-line multiplexer, U58. Normally the select lines to these multiplexers are high, selecting the B inputs for output. The B inputs to the multiplexers are address lines A0-A6, or the row address bits. The select lines change state just before CAS\* becomes active, selecting the A inputs for output. The A inputs are address lines A7-A13, or the column address bits. After CAS\* goes inactive, the select lines go high again. The outputs of both multiplexers are set in a high impedance state during Refresh cycles, when the address on the RAM bus comes from the Refresh Address Counter, U43 (see section 2.5.1).

## 2.2.2. BLOCK SELECTION

Address bits A0-A13 are sufficient only to address one memory location out of 16K; address bits A14-A15 are needed to select one location out of 64K. On the 2065 board, they do so by determining for which of the 16K blocks CAS\* will be active. RAS\* could have been used for enabling the addressed block instead of CAS\*, but since CAS\* controls the three-state output buffers on the chips, using CAS\* allows the outputs of four blocks to be tied together. U12a, a 2-to-4 line decoder, decodes A14 and A15 into a CAS\* input for one of the 16K blocks when it is enabled. The bits are decoded as follows:

A14	A15	CAS* ACTIVE FOR BLOCK
0	0	0000 - 3FFF
0	1	4000 - 7FFF
1	0	8000 - BFFF
1	1	C000 - FFFF

Table 2-1 CAS\* Block Selection

Decoder U12a is enabled by the circuitry controlling CAS\* timing (section 2.4.2), which in turn is enabled only when the board is selected during a memory read or write.

## 2.3 ENABLING THE MEMORY

Addressing a memory location within 64K alone is not sufficient to enable the 2065 board. Whether or not the board is enabled depends on the state of the internal signal BOARD SELECT. When this signal is low, the generation of CAS\* is inhibited and the data buffers disabled. Only when it is active high can a memory access cycle be completed. For bank-dependent 16K blocks, the state of BOARD SELECT is dependent on the state of the internal signal BANK SELECT\*. The following two sections discuss the Bank Select and Board Select circuitry.

### 2.3.1 BANK SELECT CIRCUITRY

The selection of a bank takes place during an I/O write to the Bank Select Port. On the 2065, the Bank Select Port's address is sensed by eight exclusive-OR gates which compare the address bits on the low byte address bus with the settings of the Bank Port Select jumpers, A0-A7. Only if the address bits match the settings is the gates' open collector output high. This high is Nanded with sOUT and the inverted pWR\*. If both these signals are also high, a condition which occurs only during an I/O write, the resulting low from the NAND gate pulls the clock input to flip-flop U31b low. As the inverted pWR\* makes its low-to-high transition at the end of the cycle, the output of the NAND gate is pulled high, clocking U31b. The state of the flip-flop's Q\* output, which is the BANK SELECT\* signal, depends on the state of the D input to the flip-flop when it is clocked. The D input to the bank select flip-flop is the open collector output from the bank byte select circuitry. This line is high only when the 2065 board receives a data byte with a high in a bit position that is jumpered on the BANK BYTE SEL jumpers. If the line is high when the flip-flop is clocked, BANK SELECT\* is forced active low and the flip-flop's complementary Q input is forced high, lighting the Bank LED. BANK SELECT\* will maintain its state until the flip-flop is clocked again by a new write to the bank select port or until the system is reset.

Depending on the setting of the RESET jumper, BANK SELECT\* comes up either active or inactive on reset and power-on. Setting the RESET jumper to ON ties EXT CLR to the flip-flop U31b's Preset input. When EXT CLR goes low as a result of system power-on or reset, the flip-flop is preset and Q\*, BANK SELECT\*, is forced low. Setting the RESET jumper to OFF ties EXT CLR to the flip-flop's Clear input. In this case when EXT CLR goes low, the flip-flop is cleared and Q\* is forced high, thus making BANK SELECT\* inactive until the proper bank byte is output to the bank select port as described above.

### 2.3.2 BOARD SELECT CIRCUITRY

The signal BOARD SELECT is the inverted open collector output of four OR gates. One of the inputs to each OR gate comes from a 2-to-4-line decoder, U12b, enabled whenever both sOUT and sINP are inactive. This chip decodes address bits A14 and A15 into four outputs, only one of which goes low when a specific memory block is addressed. The state of the other

input to each of the OR gates depends on the setting of the BLOCK SELECT jumper for the specific memory block. If the BLOCK SELECT jumper is set to BE, making that block bank-dependent, the input to the OR gate is jumpered to the BANK SELECT\* line. Only if BANK SELECT\* is active low can the OR gate be pulled low and BOARD SELECT made active. If the BLOCK SELECT jumper is set to ME, making the block bank-independent, the input is jumpered to ground, making it necessary only to address the block to pull the OR gate low and BOARD SELECT high. A low on the open collector line lights the Board LED.

## 2.4 ACCESSING THE MEMORY

Once a 16K block has been addressed and enabled, a memory access cycle can occur. There are several important timing requirements that must be met during a memory access cycle: RAS\* must be generated when the row address bits are stable on the RAM bus; CAS\* must follow after a minimum delay and after the column address bits are stable; and the data bits must be available to the CPU on the Data In bus at the appropriate time. To minimize gate delays and maximize memory access time, the 2065 uses two flip-flops in parallel to respond to pDBIN and pWR\* (or MWRT) and begin a memory access cycle.

### 2.4.1 RAS GENERATION

A memory access cycle begins when either flip-flop U31a or U16a is clocked. Both these flip-flops' D inputs are tied high. U31a is clocked by pWR\* or MWRT going active; U16a is clocked by either sMEMR or pDBIN going active, depending on the setting of the CPU SEL jumper (section 1.5). The resulting low on the Q\* output of the clocked flip-flop pulls NAND gate U15b high. This signal, inverted and fed through two parallel drivers, becomes the four RAS\* inputs to the RAM blocks. The propagation delays in generating RAS\* ensure that the row address bits will be stable on the RAM address bus when RAS\* goes active low.

The high signal from U15b also triggers a monostable multivibrator, U14b. This chip in turn outputs a high-going pulse, the length of which is determined by the setting of the variable resistor, R1. On the falling edge of the signal, a second multivibrator is triggered, U14a. The 50 ns low-going pulse from this multivibrator clears flip-flops U31a and U16a,

turning off the RAS\* signal. When the output of U14a goes high, the flip-flops are ready to be clocked again, beginning a new RAS\* cycle.

The length of the RAS\* signal is thus determined by the setting of R1. This variable resistor is adjusted for a RAS\* length of 225 ns at the factory and normally should not need further adjustment. If it does, you can look at RAS\* on pin 4 of any RAM chip. On a scope set for negative trigger, time divisions of 50 ns, and volt divisions of 1 volt, RAS\* should appear approximately as shown in Figure 2-2 when the processor is cycling. Note that RAS\* during refresh cycles is slightly longer than the normal RAS\*; disregard the second rising edge of the signal as it appears on the scope. Adjust R1 until RAS\* length is approximately 225 ns.

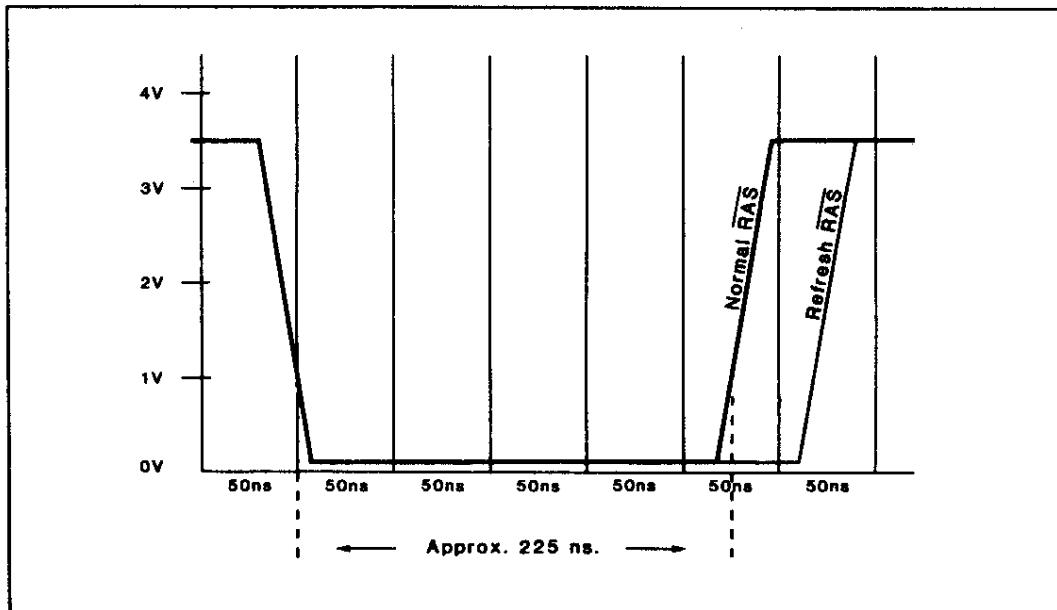


FIGURE 2-2  $\overline{\text{RAS}}$  SIGNAL LENGTH

#### 2.4.2 CAS GENERATION

The high-going signal from U14b also is involved with generating CAS\*. It is NANDed with BOARD SELECT and REFRESH\*; if either BOARD SELECT or REFRESH\* is low, the pulse will be disqualified at this gate. If all three signals to the gate are high, the resulting low from the NAND gate pulls the select inputs to the address multiplexers low, allowing the

column address bits onto the RAM address bus. The pulse is then inverted and enables the Data In latch (see 2.4.3 below). Inverted once again, it enables the 2-to-4-line decoder, U12a. This chip then decodes address bits 14 and 15 and pulls the CAS\* signal to one of the 16K blocks low. The gate delays in propagating CAS\* allow for a sufficient RAS\* hold time before CAS\* goes active. Also, since there are several gate delays from the time the select lines to the multiplexers change state to the time CAS\* becomes active, the column address bits have time to settle on the RAM address bus before CAS\* goes low.

### 2.4.3 READ, WRITE, AND DATA BUFFER CONTROL

The control line WR\* to the RAM blocks is normally high, making the RAMs read-enabled. During a Memory Read cycle memory access begins when RAS\* goes active low and ends when RAS\* goes high approximately 225 ns later. At this time valid data should be present on the system Data In bus. Because the memory access time is short, the read cycle may be over before a slow CPU has a chance to read the data. Thus although U60, an 8-bit latch/bus driver, latches the data on the internal data lines whenever CAS\* is active, it gates the data onto the Data In bus only when pDBIN is active while BOARD SELECT and PHANTOM\* are high, allowing the CPU to control the data availability through pDBIN.

During a Memory Write cycle, the control line WRITE\* to the RAM blocks will be pulled low by either MWRITE or pWR\* being active when BOARD SELECT is active. The same conditions enable U59, an 8-bit buffer which gates the Data Out bits onto the 2065's internal bi-directional data bus where they are latched by the RAMs' internal latches.

### 2.5 REFRESHING THE MEMORY

Dynamic memories need to be refreshed every 2 milliseconds. The 16K RAMs use what is known as a RAS-only refresh. During a RAS-only refresh, a 7-bit row address is put onto the RAM's address bus from an external counter. RAS\* must then be generated. At that time, all memory locations sharing that row address are refreshed. The refresh address counter is then incremented in preparation for the next refresh cycle. Since each location in a dynamic RAM needs to be refreshed every 2 ms, one row out of the 128 rows of memory



needs to be refreshed every 16 us. Thus the 2065 board must put out every 16 us an internal refresh control signal which multiplexes the refresh address onto the RAM address bus and which generates RAS\*.

During normal operations, refreshes occur on the 2065 during the last two clock cycles of every M1 (Op Code Fetch) cycle. During this time the 8080 and Z-80 are involved in internal operations. Since a Z-80 CPU operating at 2 MHz takes 11.5 us to execute the longest instruction in its set (an 8080 takes 9 us), M1 cycles normally occur frequently enough for the memory to be refreshed adequately by this method. More importantly, a refresh at this time is transparent to the processor, stealing no processing time and causing no signal conflict. However, both prolonged Wait states and DMA operations inhibit the execution of M1 cycles. To ensure the memory is adequately refreshed during Wait states, the 2065 is designed to automatically generate a refresh cycle if a refresh or memory cycle has not occurred within 16 us. Because this refresh is asynchronous to the processor, it is not suited for normal operation. During DMA, the normal DMA operations refresh the memory.

### 2.5.1 THE M1 REFRESH

In the 8080, the falling edge of pDBIN during an M1 cycle marks the beginning of internal operations. The 2065 inverts pDBIN and uses the rising edge of the inverted signal to clock flip-flop U45a. The D input to the flip-flop is the M1 signal. If the flip-flop is clocked when M1 is active high, it outputs the active control signals RFSH and RFSH\*. RFSH pulls the address multiplexers' output control line high, disabling the multiplexers' output. At the same time it enables U42, an 8-bit buffer which gates the outputs of the Refresh Address Counter, U43, onto the RAM address bus. RFSH\* pulls NAND gate U15b high, resulting in the active RAS\*. All memory locations sharing the row address on the RAM address bus are refreshed while RAS\* is low. The high from U15b also triggers monostable multivibrator U14b as described in section 2.4.2 above. When the pulse from U14b is NANDed with the active RFSH\*, however, it is disqualified, keeping CAS\* from being generated. The falling edge of this pulse triggers U14a, and the resulting low pulse clears flip-flop U45a, resetting RFSH and RFSH\*. The high RFSH\* terminates RAS\*, while the low RFSH places the outputs of buffer U42 in the high impedance state at the same that it causes the Refresh counter, U43, to increment.

In the Z-80, M1 goes inactive about the same time as pDBIN, making it impossible for a flip-flop clocked by pDBIN to catch the M1 signal before it goes inactive. Thus the signals used to generate an M1 refresh for an 8080 cannot be used for a Z-80. Happily, however, the Z-80 designers took advantage of the fact that the last two T cycles of an M1 cycle are available for refresh and designed the Z-80 to generate a control signal, REFRESH\*, during this time. The 2065 board uses this signal to generate a refresh cycle every time REFRESH\* goes active. REFRESH\* is tied to the Clock 1 input of U62, a counter, which in this case is being used essentially as a negative-edge triggered latch, allowing the refresh cycle, once triggered by REFRESH\*, to continue independent of the state of the signal. When REFRESH\* goes active, it triggers the counter, pulling the A output of the counter high. The high signal is inverted, pulling the Preset line to flip-flop U45a low. This results in the active RFSH and RFSH\* signals, which initiate a refresh cycle as described above. The counter is cleared by a low-going pulse from U14a, generated at the same time as the high-going pulse.

### 2.5.2. MEMORY REFRESH DURING WAIT STATES

Because prolonged Wait states may inhibit the CPU's execution of M1 cycles, the asynchronous refresh circuitry on the 2065 is set to generate a refresh if one has not occurred within 16 us. The Clock 2 input of counter U62 is tied to the 2 MHz signal from the system bus. U62 divides this signal by 4, outputting a signal with a 2 us cycle time. On the rising edge of this signal, U46, an 8-bit parallel-out shift register, is clocked. This shift register's outputs go high successively as it is clocked. When it has been clocked seven times, its G output goes high. This signal is ANDed with the inverted clock input to the shift register. When the clock input goes low again, the AND gate is forced high. This high, input to NOR gate U13, pulls the NOR gate's output, pREADY, low. This allows the asynchronous refresh to be completed without interference from a memory cycle or another refresh cycle. On the eighth clock of the shift register, or approximately 14 us after the shift register was first clocked, the H output will go high. Inverted, it pulls flip-flop U45a's Preset input low, resulting in the active RFSH and RFSH\*. The high H output also pulls NOR gate U13 low, to keep pREADY low, since the G output goes low as H goes high. To ensure pREADY stays low for a complete Refresh cycle, the rising-edge of the G output also clocks flip-flop U45b. The resulting high from U45b pulls pREADY low. The counter and shift register are cleared by the low-going pulse

from U14b, while flip-flops U45a and U45b are reset by the low-going pulse from U14a. Since the low-going pulse from U14b is generated during any refresh or memory cycle, the counter and shift register are usually cleared before they have a chance to generate a refresh.

Occasionally, the 2065 board may be shipped with dynamic RAMS which require refreshing every 1 ms instead of every 2 ms. In this case, the factory will have set the asynchronous refresh circuitry to generate refreshes every 8 us instead of 16 by jumpering the divide-by-8 output of counter U62 to the shift register's clock.

### 2.5.3 MEMORY REFRESH DURING DMA

During DMA operations, M1 cycles are inhibited. However, RAS\* is generated as described in section 2.4.1 above whenever either pWR\* or pDBIN (or sMEMR) is active during a DMA operation. All the memory locations sharing the row address on the RAM address bus at that time are then refreshed, whether or not the board is selected; CAS\* alone is disqualified when BOARD SELECT is low. Because of the frequency with which memory cycles occur during DMA, the memory is refreshed adequately by this method.

# APPENDIX

## TECHNICAL INFORMATION

### A.1 2065 SPECIFICATIONS

#### MEMORY

Capacity	64 Kilobytes
Type	4116-type Dynamic RAM, 16K x 1-bit

BUS COMPATIBILITY	S-100
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#### POWER REQUIREMENTS

Supply	Unregulated +8, +16, and -16 volts
Maximum Draw	400 mA at +8 volts 175 mA at +16 volts 5 mA at -16 volts

#### DISSIPATION

Watts	8
BTU/min	.6

#### PHYSICAL MEASUREMENTS

Dimensions	10" l x 5" w (25.4 cm x 12.7 cm)
Weight	10 oz (.28 kg)

#### ENVIRONMENTAL REQUIREMENTS

Temperature	32° to 160° F (0° to 70° C)
Humidity	0 to 90% noncondensing

## A.2 THE 2065 SYSTEM BUS

### A.2.1 CONFORMANCE TO THE IEEE S-100 BUS STANDARDS

The S-100 bus came into being with the Altair line of microcomputers using the 8080 microprocessor. Known then as the Altair bus, it was adopted by many other microcomputer manufacturers and became an unofficial industry standard, resulting in the name "Standard-100" bus. Recently the IEEE has undertaken the development of an official standard for the S-100 bus. With the exception of pin 66, the 2065 system bus conforms to the IEEE S-100 standard. Pin 66 is left undefined for manufacturer's use in the proposed standards; we have used it, as have many other manufacturers, for the REFRESH\* signal from a Z-80 CPU. Since the 2065 requires this signal when used with a Z-80 CPU, the 2065 may not be compatible with a Z-80 system which conforms to the IEEE standard.

### A.2.2 SIGNAL DEFINITIONS AND PIN ASSIGNMENTS

The following are definitions of the signals used by the 2065 board. We have followed the IEEE convention of indicating active low signals with an asterisk (\*) following the signal mnemonics.

#### THE DATA AND ADDRESS LINES

A0-A15        The 16-bit parallel address lines.  
 DI0-DI7      The 8-bit parallel data input lines to the CPU.  
 DO0-DO7      The 8-bit parallel data output lines from the CPU.

#### THE STATUS SIGNALS

sOUT         The Output signal indicates the CPU is executing an output instruction.  
 sM1         The M1 cycle signal indicates the CPU is in the Op Code fetch portion of an instruction cycle.  
 sINP         The Input signal indicates the CPU is executing an input instruction.

sMEMR            The Memory Read signal indicates the CPU is reading from memory.

#### THE CLOCK AND CONTROL SIGNALS

pDBIN            The Data Bus In signal indicates the CPU or temporary bus master is conditioned to read data on the Data In bus.

pWR\*            The Write signal indicates valid data is on the Data Out bus.

pREADY          The Ready signal, when pulled low, requests a Wait state.

EXT CLR\*        When active, the External Clear signal resets all bus slaves.

MWRT            The Memory Write signal indicates that the current data on the Data Out bus is to be written into the memory location specified by the address bus. Often generated by front panel devices, it usually is used for front panel memory deposit.

PHANTOM\*        The Phantom signal is used to control memory overlay. On the 2065 board it is an input which, when active, places the Data In bus (DI0-DI7) driver in its high impedance state.

REFRESH\*        The Refresh signal is generated by a Z-80 CPU during the last two T cycles of every M1 cycle. Memory refresh at this time is transparent to the processor.

CLOCK            Clock is a 2 Mhz signal for timing reference.

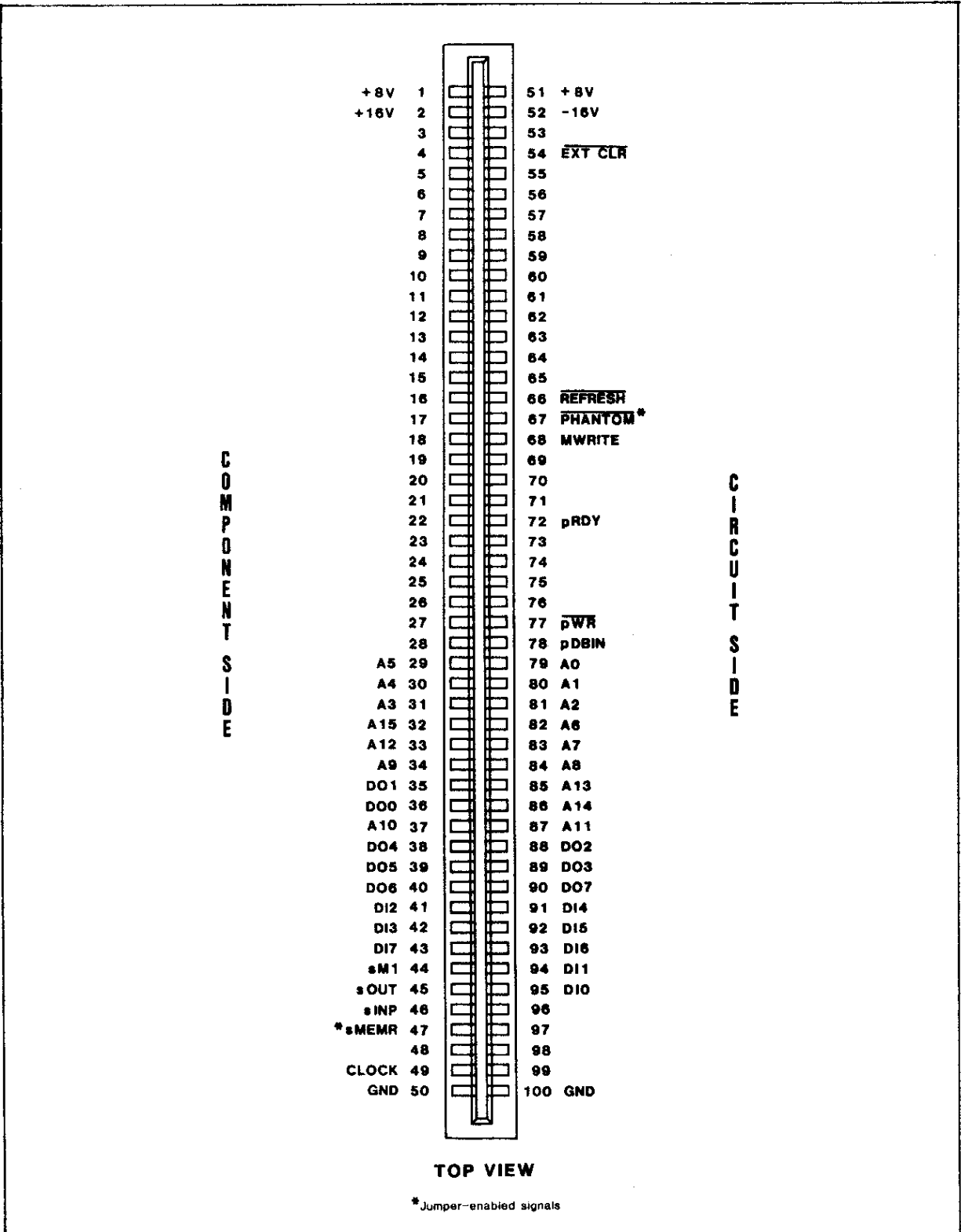
#### THE POWER LINES

+8 VOLTS        This is the unregulated +8 volts power line.

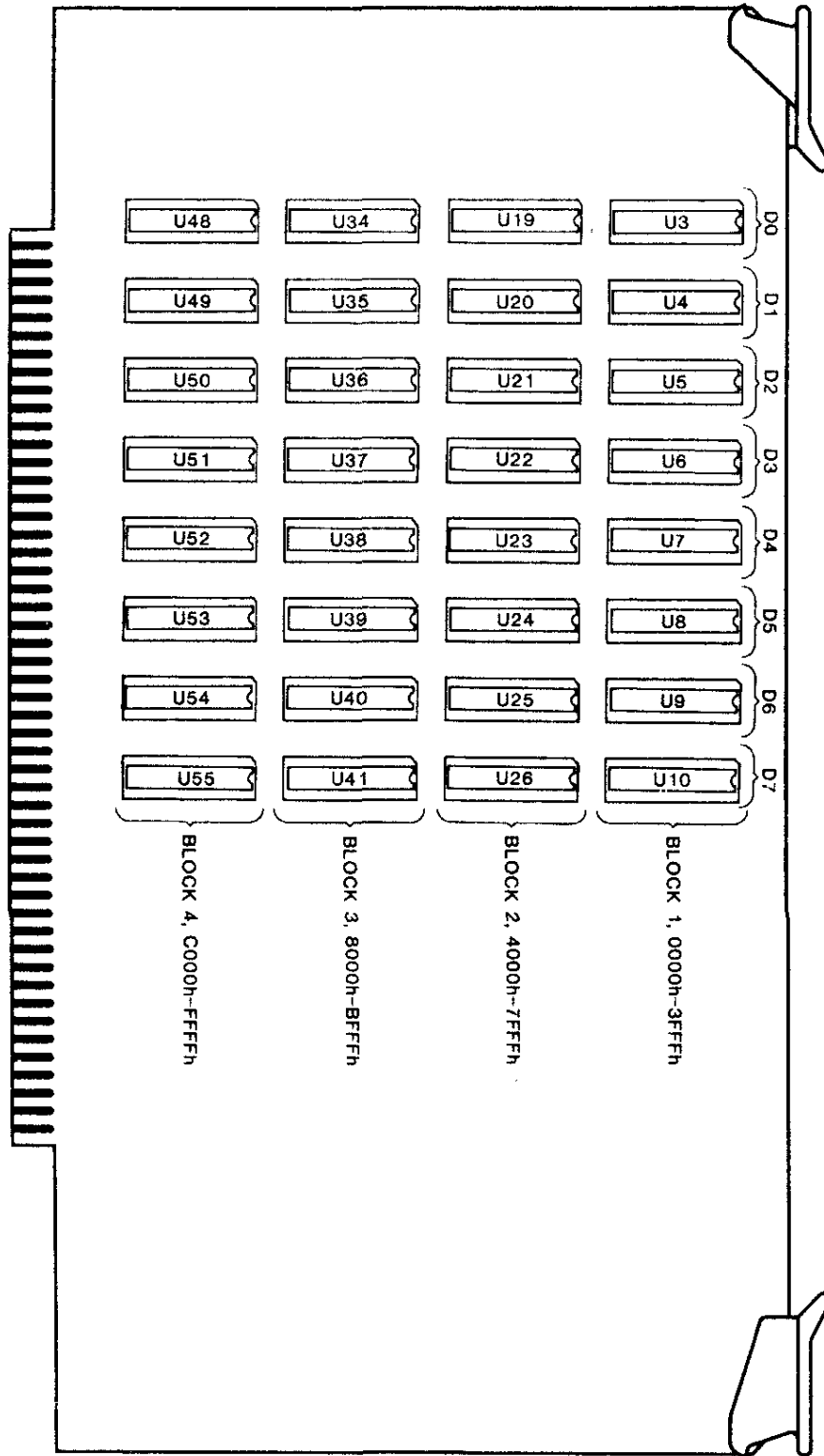
+16 VOLTS       This is the unregulated +16 volts power line.

-16 VOLTS       This is the unregulated -16 volts power line.

FIGURE A-1 2065 BUS CONNECTOR PINOUT



A.3 ADDRESS/DATA CONFIGURATION OF MEMORY ARRAY





## A.4 PARTS LIST

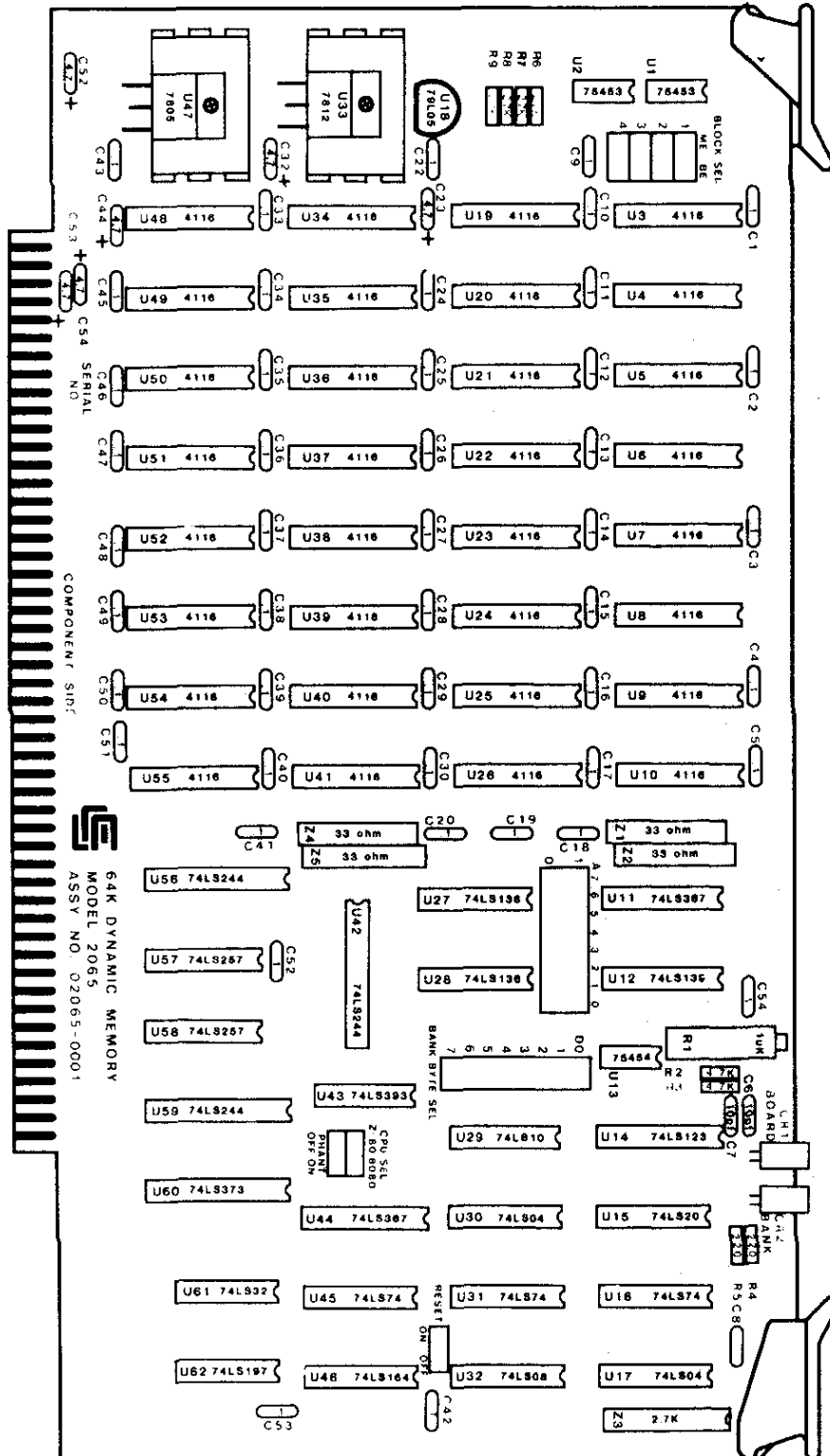
QTY	REF NO.	DESCRIPTION	CCS PART NO.
---	-----	-----	-----
CAPACITORS			
47	C1-5,8-22, 24-31,33-43, 45-51,55	.1uf 50v 20% Monolythic	42034-21046
2	C6,7	10pf 500v 10% Mica	42215-51005
6	C23,33,44,52, 54	4.7uf 35v 20% Tantalum	42804-54756
INTEGRATED CIRCUITS			
2	U1,2	75453	30300-00453
32	U3-10,19-26, 34-41,48-55	4116 (or equiv) 16K x 1 dynamic RAM	31900-04116
2	U11,44	74LS367	30000-00367
1	U12	74LS139	30000-00139
1	U13	75454	30300-00454
1	U14	74LS123	30000-00123
1	U15	74LS20	30000-00020
3	U16,31,45	74LS74	30000-00074
2	U17,30	74LS04	30000-00004
1	U18	79L05, -5v Regulator	32000-17905
1	U27,28	74LS136	30000-00136
1	U29	74LS10	30000-00010
1	U32	74LS08	30000-00008
1	U33	7812, +12v Regulator	32000-07812
3	U42,56,59	74LS244	30000-00244
1	U43	74393	30200-00393
1	U46	74LS164	30000-00164
1	U47	7805, +5v Regulator	32000-07805
2	U57,58	74LS257	30000-00257
1	U60	74L373	30000-00373
1	U61	74LS32	30000-00032
1	U62	74LS197	30000-00197
RESISTORS			
1	R1	10K 1/2W 10% 10-turn vari.	40601-01035
2	R2,3	4.7K 1/4W 5%	40002-04725
2	R4,5	220 1/4W 5%	40002-02215
4	R6,9	2.7K 1/4W 5%	40002-02725
4	Z1,2,4,5	33 x 4 10% Network	40931-43305
1	Z3	2.7K x 7 20% Network	40930-72726
1		330 1/4W 5%	40002-03315

\*Use CCS part number when ordering spare or replacement parts.

## PARTS LIST CONTINUED

QTY	REF NO.	DESCRIPTION	CCS PART NO.
---	-----	-----	-----
SOCKETS			
3	U1,2,13	8-pin IC	58102-00080
38	U3-12,14,19- 26,34-41,44, 48-55,57,58	16-pin IC	58102-00160
14	U15-17,27-32, 43,45,46,61,62	14-pin IC	58102-00140
4	U42,56,59,60	20-pin IC	58102-00200
MISCELLANEOUS			
2	CR1,2	LED, rectangular red	37400-00001
15	W1-12,21-23	Header strips, 1 x 3	56004-01003
8	W13-20	Header strips, 1 x 2	56004-01002
16	--	Berg jumper plugs	56200-00001
2	--	Heatsinks, 220-type, .5"	60022-00001
2	--	Screws, 6-32 x 3/8"	71006-32061
2	--	Nuts, 6-32 Pem	72606-32250
2	--	PCB extractor, non-locking	60010-00001
2	--	Roll pin extractor mounting	60010-00000
1	--	PCB board, rev. B	02065-00002
1	--	Manual	89000-02065

A.5 COMPONENT ASSEMBLY DIAGRAM



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California Computer Systems  
250 Caribbean Drive  
Sunnyvale, California  
94086

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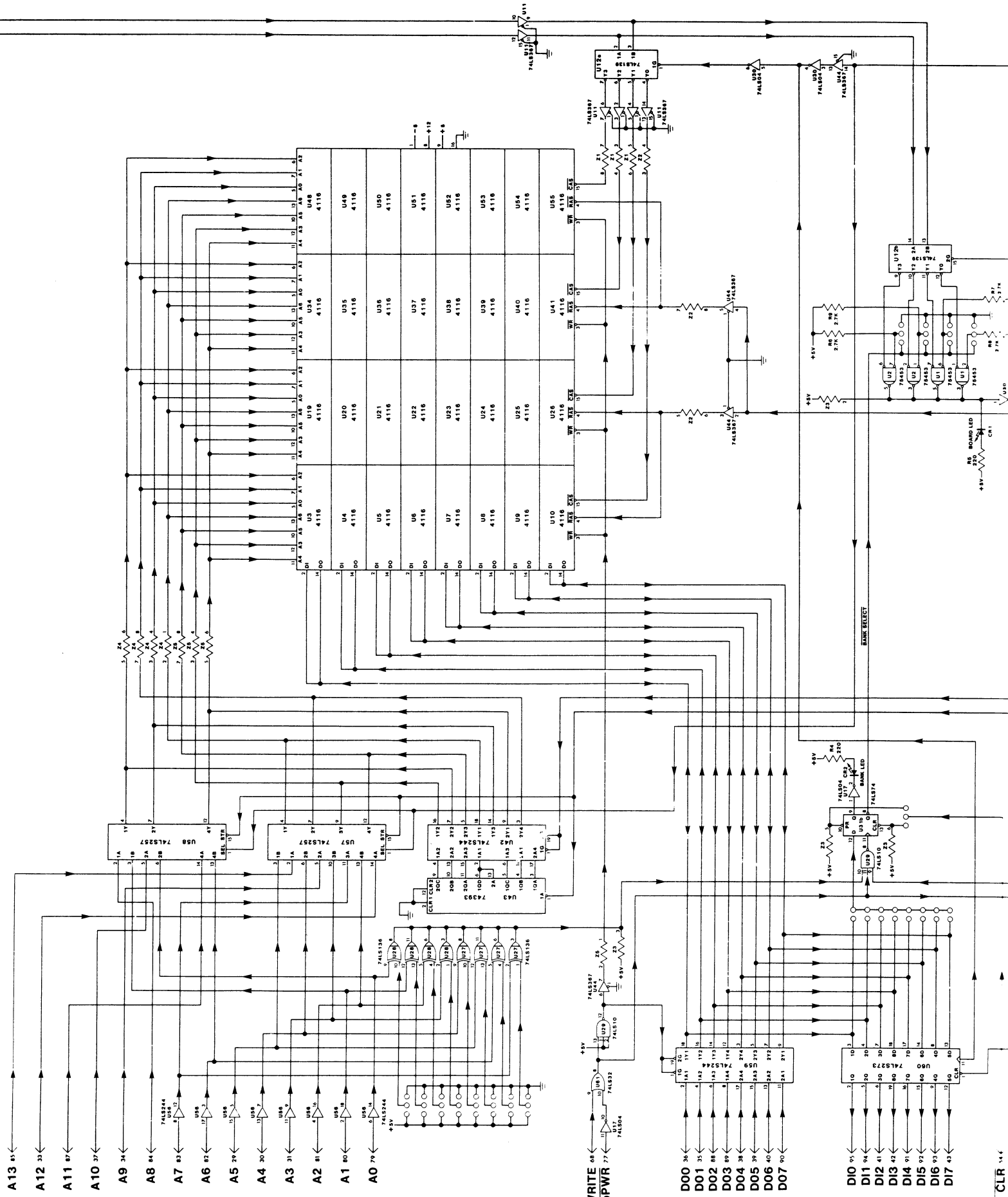
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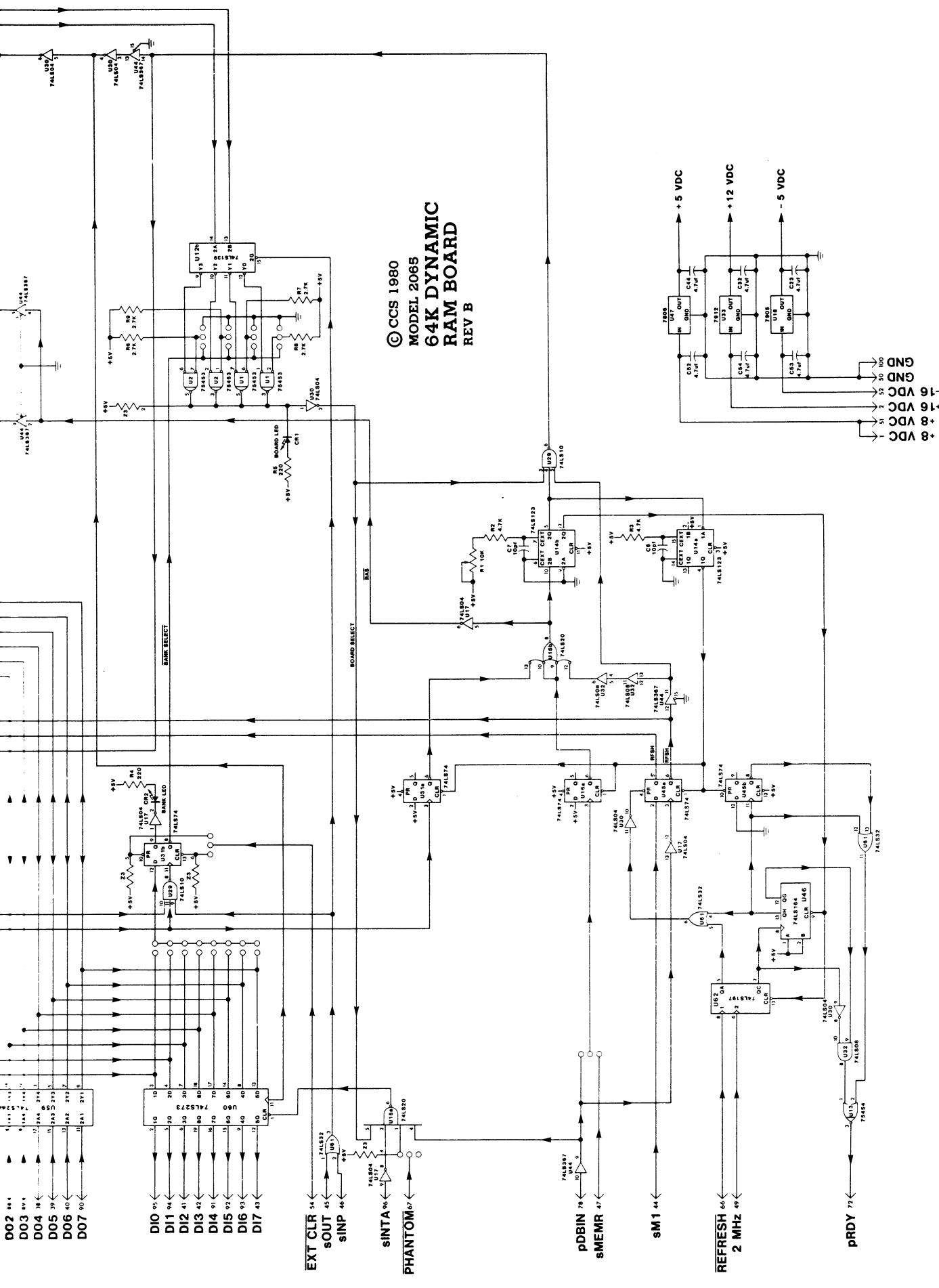
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A15 119  
A14 807  
A13 851  
A12 331  
A11 871  
A10 371  
A9 341  
A8 841  
A7 831  
A6 821  
A5 351  
A4 301  
A3 311  
A2 811  
A1 801  
A0 791



MWRITE 08  
pPWR 77  
D00 36  
D01 35  
D02 88  
D03 89  
D04 38  
D05 39  
D06 40  
D07 90  
D10 95  
D11 94  
D12 41  
D13 42  
D14 91  
D15 92  
D16 93  
D17 43  
EXT CLR 144



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A.6 SCHEMATIC