CGRS MICROTECH

P.O. BOX 368 SOUTHAMPTON, PA. 18966 (215) 757-0284

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SPECIFICATIONS ---Level II MPU Board , Revision 4
August 5, 1977

MPU: MCS6502 , MOS TECHNOLOGY, INC.

BOARD SIZE: 5.1 inch X 10 inches Basic board size
with .3 inch Card Edge Connector

POWER REQUIREMENTS: +8 volts @ 1.2 amps
(2.5 amps with front panel)
+16 volts @ 200 ma. max.
-16 volts @ 180 ma. max.
Note: all supplies may be unregulated

MEMORY COMPLIMENT(ROM):
4096 bytes of EPR0M(2708)
Locatable on any of the following 4K
blocks: 0,1,3,4,5,E,F

MEMORY COMPLIMENT(RAM):
2048 bytes of RAM (2111)
Locatable on the bottom half X000-X7FF,
of any of the following 4K blocks:0,1,3,4,5,E,F

CLOCK SPEED: 1.0 Mhz. standard. Others optional

BUFFERING: Address lines drive: 10 TTL loads
Data Out lines drive: 10 TTL loads

CARD EDGE CONNECTOR: 50 Pin dual readout (100) contacts with
.125 inch spacing. Standard S100 configuration.

DESCRIPTION_____LEVEL II MPU BOARD, REVISION 4
AUGUST 5, 1977

THE CGRS LEVEL II MPU BOARD IS A MICROCOMPUTER BOARD THAT CONTAINS THE MCS6502 MICROPROCESSOR, READ/WRITE MEMORY (RAM), READ-ONLY MEMORY, TTL SUPPORT LOGIC AND ON-BOARD VOLTAGE REGULATORS.

THE COMPONENTS ARE MOUNTED ON A 5 1/4 INCH X 10 INCH P.C. BOARD THAT CONFORMS TO STANDARD S100 P.C. CARD DIMENSIONS AND CONNECTOR PINOUTS. THE LEVEL II MPU BOARD IS COMPATIBLE WITH S100 PERIPHERAL BOARDS, ALLOWING CONSIDERABLE AND INEXPENSIVE COMPUTER EXPANSION.

THE CGRS LEVEL II MPU BOARD, WITH ITS ON-BOARD RAM AND ON-BOARD ROM, PROVIDES THE BASE BOARD FOR ANY MICROCOMPUTER SYSTEM. THE LEVEL II MPU BOARD CAN BE USED WITH THE CGRS FRONT PANELS OR A SOFTWARE MONITOR SUCH AS T.I.M. II I/O BOARD, WITH THE T.I.M. MONITOR, FOR MICROCOMPUTER/MICROCONTROLLER.

THE CGRS LEVEL II MPU BOARD CONTAINS, IN ADDITION TO ITS MEMORY, TTL SUPPORT LOGIC REQUIRED TO IMPLEMENT 1. BUFFERED CRYSTAL CLOCK, 2. SLOW MEMORY INTERFACE, 3. DMA CONTROL LOGIC THAT CAUSES ADDRESS LINE DRIVERS TO GO TO A HIGH-IMPEDANCE MODE., 4. S100 INTERFACE LOGIC THAT PROVIDES LEVELS FOR PERIPHERAL COMPUTER BOARDS., 5. POWER-UP RESET GENERATOR THAT PROVIDES AUTOMATIC RESTART ACTION ON POWER TURN ON., AND 6. ADDRESS DECODE LOGIC FOR SIMPLIFIED I/O PERIPHERAL BOARDS.

MEMORY - MAPPED I/O DECODER

THE S100 BUS STRUCTURE PROVIDES TWO CONTROL LINES USED TO ENABLE INPUT AND OUTPUT DEVICES. THESE TWO LINES, SINP AND SOUT, ENABLE I/O BOARDS WHEN THEY SWITCH TO LOGIC 1. THE 6502 MICRO-PROCESSOR ADDRESSES "MEMORY-MAPPED" I/O, THAT IS, ALL INPUT OR OUTPUT DEVICES ARE ADDRESSED EXACTLY LIKE MEMORY. THE CGRS LEVEL II MPU PROVIDES CIRCUITRY TO GENERATE SINP AND SOUT WHEN THE SELECTED PACE OF MEMORY IS DECODED. THIS INSURES COMPATIBILITY OF "PORT" TYPE I/O BOARDS ORGINALLY DESIGNED FOR THE 8080 AND SIMPLIFIES ADDRESS DECODE LOGIC OF MEMORY-MAPPED I/O CARDS.

STATUS INPUT (SINP) GOES TO LOGIC 1 WHEN THE SELECTED MEMORY PAGE IS DECODED AND THE MPU READ/WRITE LINE IS IN THE READ STATE. THIS ENABLES INPUT DEVICES. THE STATUS OUTPUT (SOUT) LINE GOES TO LOGIC 1 WHEN THE SELECTED MEMORY PAGE IS DECODED AND THE MPU READ/WRITE LINE IS IN THE WRITE STATE, LOGIC 0. THIS ENABLES OUTPUT DEVICES.

MEMORY AND I/O DECODING

THE ON-BOARD MEMORY AND THE MEMORY-MAPPED I/O DECODER CAN BE OPTIONALLY DECODED INTO ONE OF SEVERAL DIFFERENT LOCATIONS. THE 2048 (2K) BYTES OF RAM OCCUPY THE LOWER HALF OF A SELECTED 4096 (4K) MEMORY BLOCK. THE 4096 BYTES OF ROM OCCUPY ONE ENTIRE SELECTED 4K BLOCK AND THE I/O DECODE LOGIC RESPONDS TO PAGE 0 OF A SELECTED 4K BLOCK. THE ROM/RAM/I/O CAN BE SELECTED TO ANY OF THE FOLLOWING 4K BLOCKS: 0,1,3,4,5,E,F.

ADDRESS* DECODING CHART

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	HEX ADDRESS
ROM	X	X	X	X	*	*	*	*	*	*	*	*	*	*	*	*	X000-XFFF
RAM	X	X	X	X	0	*	*	*	*	*	*	*	*	*	*	*	X000-X7FF
I/O	X	X	X	X	0	0	0	0	*	*	*	*	*	*	*	*	X000-X0FF

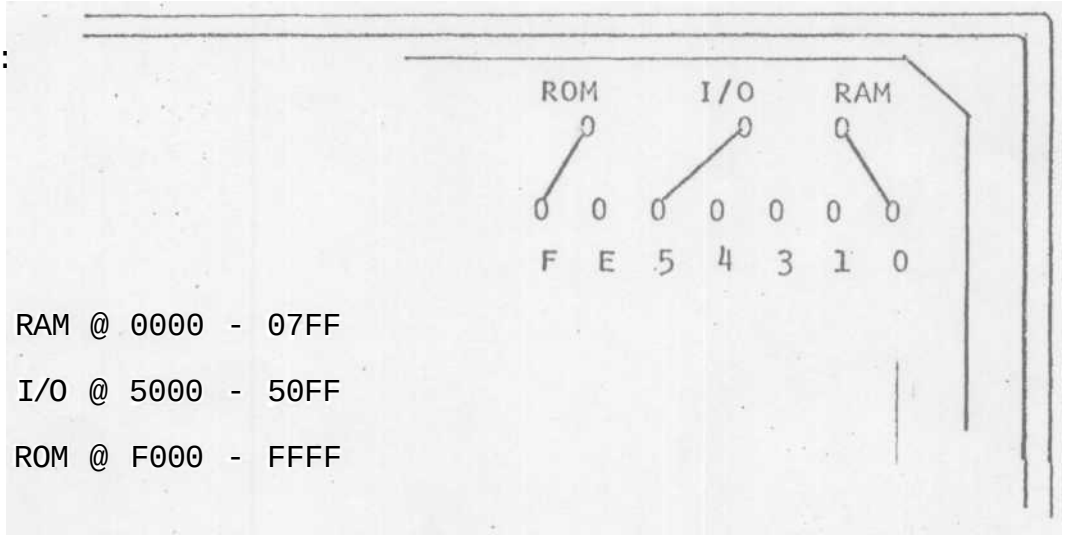
* = VARIABLE ADDRESS BIT
X = SELECTABLE ADDRESS BIT

OPTIONAL SELECTIONS:

0	0	0	0	= $Ø
0	0	0	0	= $1
0	0	1	1	= $3
0	1	0	0	= $4
0	1	0	1	= $5
1	1	1	0	= $E
1	1	1	1	= $F

ADDRESS SELECTIONS CAN BE MADE BY JUMPER WIRE PLACEMENT. THE ADDRESS SELECTION JUMPERS ARE LOCATED IN THE UPPER RIGHT CORNER OF THE LEVEL II MPU BOARD.

EXAMPLE:



RAM @ 0000 - 07FF

I/O @ 5000 - 50FF

ROM @ F000 - FFFF

OPTIONAL NMI INPUT

THE NON-MASKABLE INTERRUPT INPUT TO THE 6502 MICROPROCESSOR CAN BE JUMPER CONNECTED TO BUS PINS 3,4,5,6,7 OR 8. THESE ARE THE VECTOR INTERRUPT INPUTS OF THE S100 BUS. THE JUMPER IS LOCATED IN THE LOWER LEFT CORNER OF THE LEVEL II MPU BOARD.

PARTS LIST-----LEVEL II MPU BOARD, REVISION 4
OCTOBER 1, 1977

DESIGNATOR	DESCRIPTION	QUANTITY
Ul	MCS6502 MICROPROCESSOR	1
U2, U31	8098 HEX TRI-STATE INVERTER	2
U3	7408 QUAD 2IN AND GATE	1
U4	7474 DUAL D FLIP FLOP	1
U5	7404 HEX INVERTER	1
U6	7410 TRIPLE 3IN NAND GATE	1
U7, U8, U9	8097 HEX TRI-STATE BUFFER	3
U10 THRU U25	2111A-4 OR 2111AL-4 256 X 4 RAM	8(LEVEL II-1K) 8 ADDITIONAL, NOT SUPPLIED
U26, U27	8833 QUAD DATA TRANSCEIVER	2
U28	7400 QUAD 2IN NAND GATE	1
U29	7432 QUAD 2 IN OR GATE	1
U30, U37	7442 BCD TO DECIMAL DECODER	2
U32	74LS139 DUAL 2 TO 4 DECODER	1
U33 - U36	2708 1K X 8 EPROM	4 (NOT SUPPLIED)
UR1, UR2	7805 5 VOLT REGULATOR	2 (1 WHEN SUPPLIED WITH TIM BOARD)
UR3	LM320 T-5 -5 VOLT REGULATOR	1
UR4	LM340 T-12 +12 VOLT REGULATOR	1
Rl	39K OHM RESISTOR	1
R2	470 OHM RESISTOR	1
R3, R5-R8, R9 R15,R16, R18	6.8K OHM RESISTOR	9
R4, R17,R13, R10 R14,	1K OHM RESISTOR	5
Rll	47K OHM RESISTOR	1
R12	270K OHM RESISTOR	1
CR1, CR2	1N914 OR EQUAL DIODE	2
Ql, Q2, Q4	2N4265 OR EQUAL NPN TRANSISTOR	3
Q3	2N4402 OR EQUAL PNP TRANSISTOR	1
S1	2 POSITION DIP SWITCH	1
X1	1 MHZ CRYSTAL - HC 33U	1
PL1	50 POSITION CONNECTOR	1 (NOT SUPPLIED IN LEVEL III SYSTEM)
Cl	10 PF CERAMIC CAPACITOR	1
C3	200 PF CERAMIC CAPACITOR	1
C2, C4, C5 C7-C10, C12, C13 C16-C29	BYPASS CAPACITOR	16
C14, C15, Cll	1 UF CAPACITOR - TANTALUM	3

PARTS LIST CONTINUED LEVEL II MPU BOARD, REVISION 4

MISC.	40 PIN I.C. SOCKET	1
	24 PIN I.C. SOCKET	4
	18 PIN I.C. SOCKET	8
	16 PIN I.C. SOCKET	7
	HEAT SINK - CGRS	1

C8
U34
C12
U33
C14
C15
UR2
UR1
U36
C13
U35
C9
UR4
C16
C23
U32
U11
U10
C10
UR3
C17
C24
U31
U13
U12
C11
C18
C25
U30
U15
U14
S1
C19
C26
U17
U16
C20
C27
U19
U18
C21
C28
U29
U21
U20
C22
C29
U23
U22
U28
U25
U24
U8
U26
U27
U7
U1
U9
Q4
Q2
R9
R14
R13
C1
X1
U5
U3
R4
R1
Q3
R12
R5
Q1
U2
U37
U6
U4
R3
CR2
R8
C5
C4
C3
R2
C2
ROM
I-O
RAM
CGRS MICROTECH
P.O. BOX 368
SOUTHAMPTON, PA. 18966

ASSEMBLY INSTRUCTIONS

1. CHECK ALL PARTS RECEIVED AGAINST THE PARTS LIST. MAKE SURE YOU UNDERSTAND WHAT EACH PART IS AND WHERE IT BELONGS.

2. CAREFULLY EXAMINE THE P.C. BOARD FOR SHORT CIRCUITS OR BROKEN CONDUCTORS. TRACE ALONG THE PATH OF ANY CONDUCTORS WITH SUSPECTED SHORTS.

3. INSERT AND SOLDER I.C. SOCKETS AND VOLTAGE REGULATORS. INSTALL UR1 AND UR2 WITH THEIR HEAT SINK. USE HEAT SINK GREASE BETWEEN THE VOLTAGE REGULATOR AND THE HEAT SINK.

4. INSTALL ALL BYPASS CAPACITORS.

5. INSTALL REMAINING COMPONENTS.

6. CHECK BOARD OVER FOR SOLDER SHORTS.

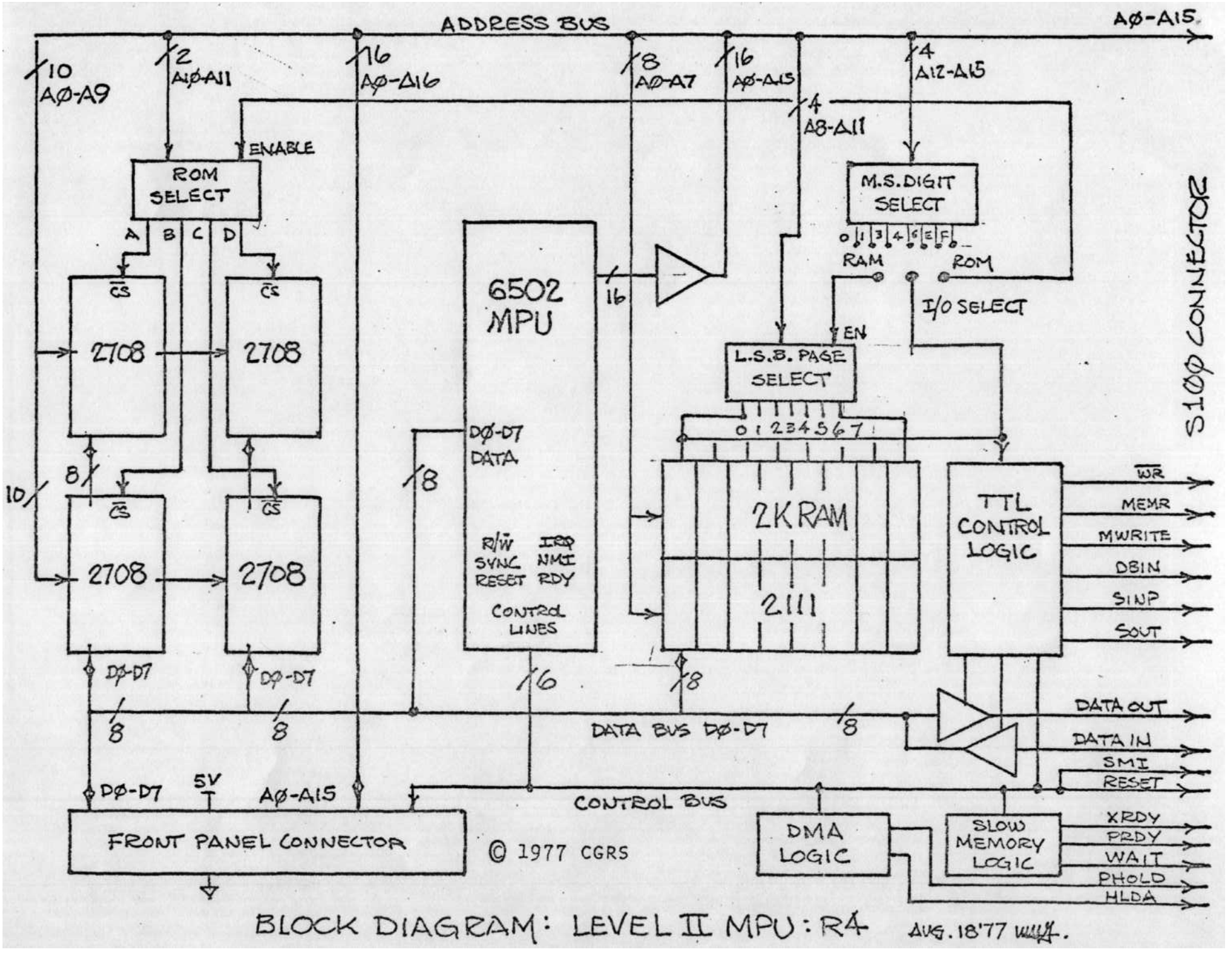
CHECK OUT

1. BEFORE INSERTING THE I.C.'S INTO THEIR SOCKETS, APPLY POWER (+8 VOLTS) TO THE BOARD. CHECK THE OUTPUT OF THE VOLTAGE REGULATORS. THE OUTPUT OF URl AND UR2 SHOULD BE 5 VOLTS +/-5%. THE OUTPUT OF UR3 SHOULD BE -5 VOLTS +5% AND THE OUTPUT OF UR4 SHOULD BE 12 VOLTS +/-5%. IF VOLTAGES ARE NOT CORRECT, FIND THE PROBLEM BEFORE PROCEEDING.

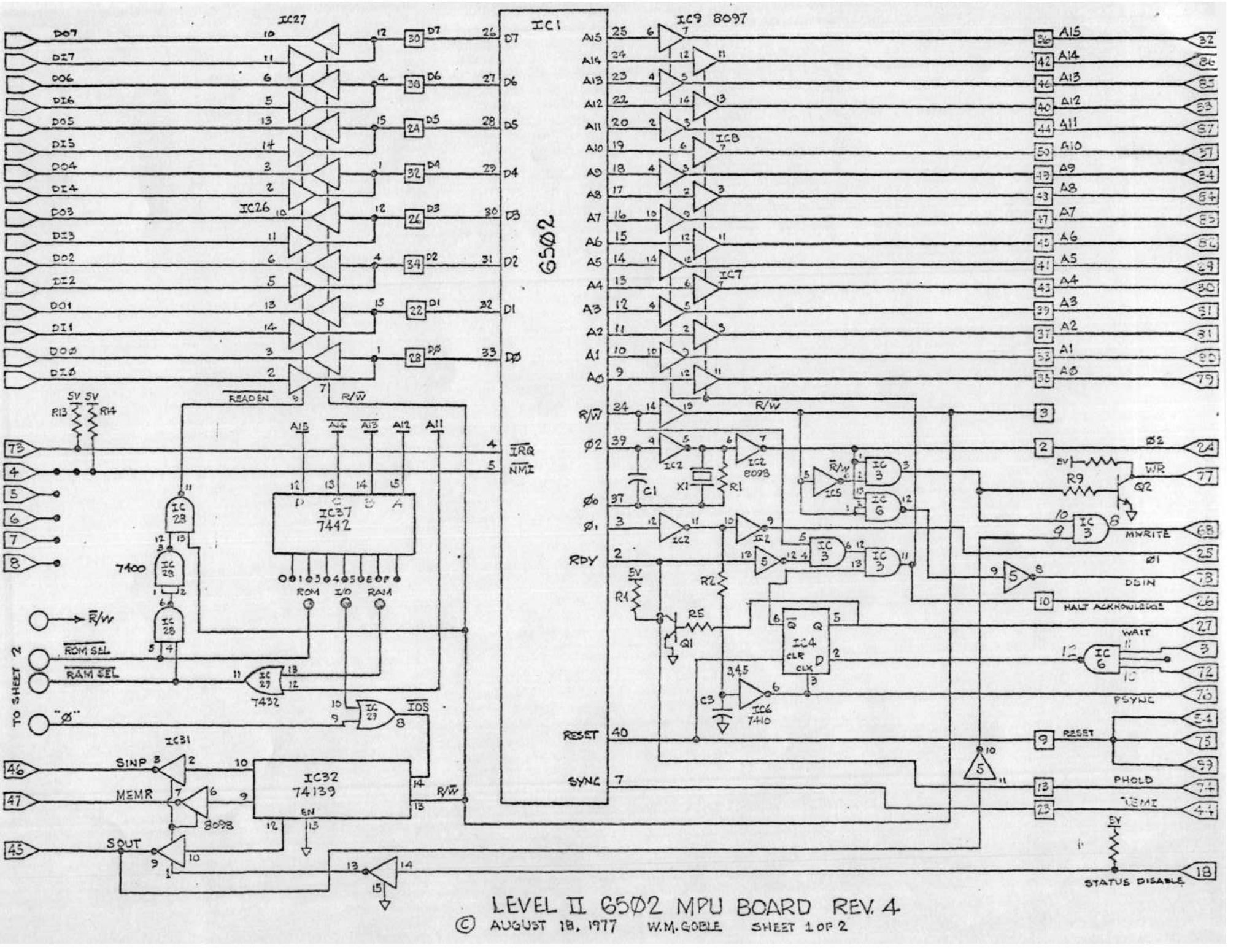
2. INSERT I.C.'S INTO THEIR SOCKETS AND AGAIN APPLY POWER. CHECK OUTPUT OF THE VOLTAGE REGULATORS. CHECK I.C.'S FOR ABNORMAL HIGH TEMPERATURE.

3. IF A CGRS CONTROL PANEL WAS PURCHASED WITH THE MPU BOARD, TURN OFF POWER AND CONNECT THE FRONT PANEL. CONTINUE WITH FRONT PANEL CHECKOUT.

4. IF NO FRONT PANEL IS AVAILABLE, SEVERAL ADDITIONAL CHECKS CAN BE MADE:
   A. VERIFY MPU CLOCK CIRCUIT OSCILLATION.
   B. VERIFY POWER UP RESET CIRCUIT OPERATION.
   C. VERIFY PROPER INPUTS TO THE MICROPROCESSOR, RESET, IRQ AND NMI.

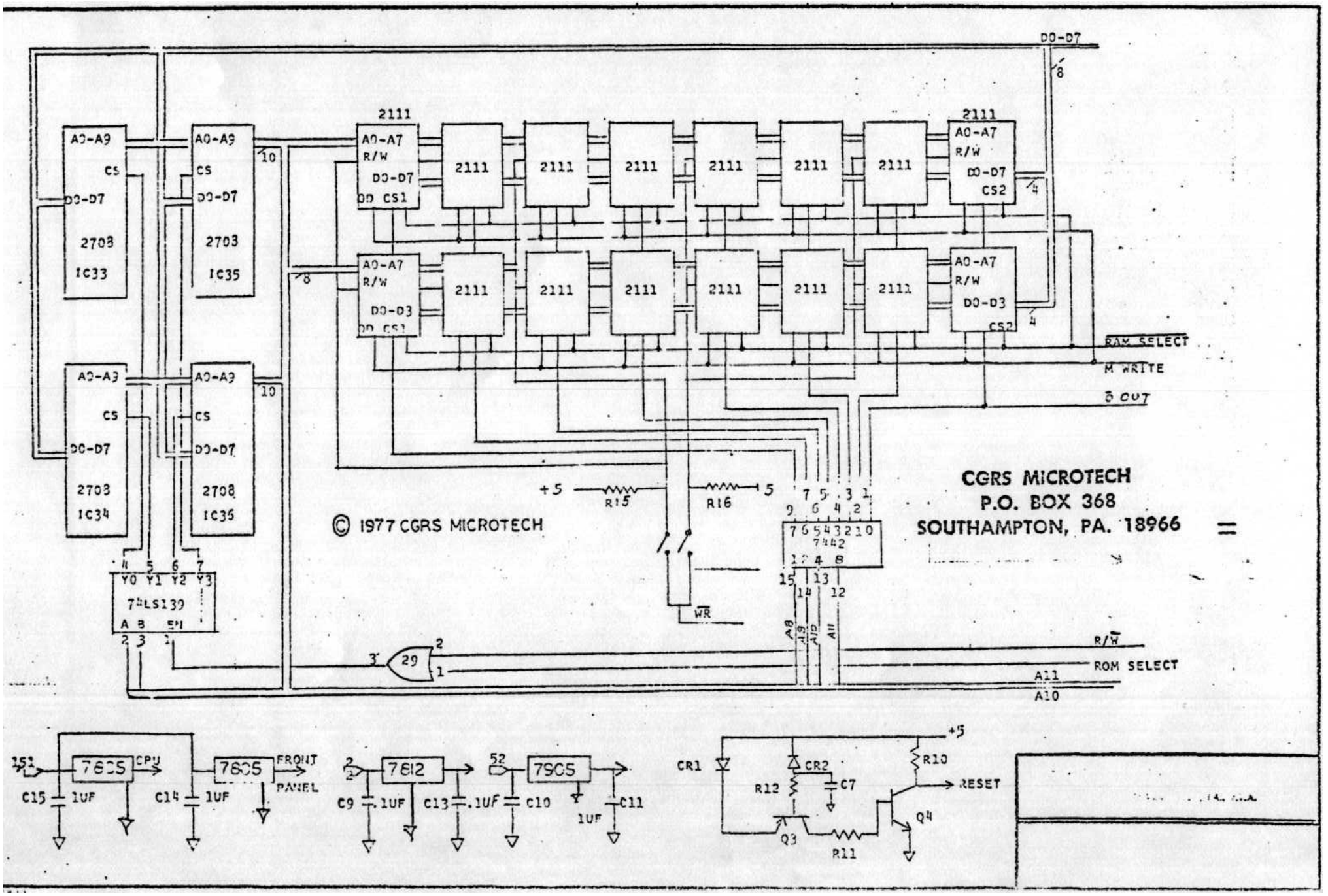


BLOCK DIAGRAM: LEVEL II MPU: R4 AUG. 18'77



LEVEL II 6502 MPU BOARD REV. 4

 SHEET 1 OF 2


D0-D7
2111
A0-A7
R/W
D0-D7
CS1
CS2
2708
IC33
IC35
IC34
IC36
A0-A9
CS
D0-D7
RAM SELECT
M WRITE
5 OUT
+5
R15
R16
WR
7442
74LS139
Y0 Y1 Y2 Y3
A B EN
29
R/W
ROM SELECT
A11
A10
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SOUTHAMPTON, PA. 18966
7805
CPU
FRONT PANEL
C15 1UF
C14 1UF
7812
7905
C9 .1UF
C13 .1UF
C10
C11
1UF
CR1
CR2
R10
R12
C7
RESET
Q3
Q4
R11

THEORY OF OPERATION

DESCRIPTION OF BLOCK DIAGRAM

THE LEVEL II MPU BOARD CONSISTS OF A 6502 MICROPROCESSOR, 2K BYTES OF 2111 TYPE RAM, 4K BYTES OF 2708 TYPE EPROM, TTL INTERFACE LOGIC, AND TTL SUPPORT LOGIC FOR THE 6502 MICROPROCESSOR. THIS SUPPORT LOGIC INCLUDES ADDRESS LINE AND DATA LINE BUFFERS, TWO-PHASE CLOCK BUFFERS, SLOW MEMORY INTERFACE LOGIC AND DMA (DIRECT MEMORY ACCESS) CONTROL LOGIC.

THE 6502 MICROPROCESSOR OPERATES FROM A TWO-PHASE CLOCK WITH THE CLOCK GENERATOR CIRCUITRY ON THE CHIP. IC2(8098) PROVIDES EXTRA AMPLIFICATION FOR THE ON-CHIP CLOCK CIRCUIT AS WELL AS BUFFERS TO FEED THE S100 CARD EDGE CONNECTOR.

ADDRESS LINE BUFFERING FROM THE MICROPROCESSOR IS DONE BY IC'S 7, 8, AND 9. THESE LINES PROVIDE A HIGH POWER DRIVE SIGNAL TO THE S100 CARD EDGE CONNECTOR AS WELL AS THE ON-BOARD MEMORY DECODERS. BUFFERED ADDRESS LINES A12 THROUGH A15 ARE FED TO THE MOST SIGNIFICANT DIGIT SELECT CIRCUIT COMPRISED OF IC 37 AND TWO INVERTOR GATES FROM IC2. THREE JUMPERS CAN BE PLACED IN ONE OF SEVERAL POSITIONS IN ORDER TO DETERMINE WHAT ADDRESS LINE COMBINATION WILL ACTIVATE THE ON-BOARD RAM, ROM AND I/O DECODERS.

INDIVIDUAL RAM CHIP SETS ARE SELECTED BY IC 30 WHICH DECODES ADDRESS LINES A8-A11. ROM CHIPS ARE SELECTED BY IC 32 WHICH DECODES ADDRESS LINES A10-A11.

MICROPROCESSOR DATA LINES ARE BUFFERED BY IC 26 AND IC 27, QUAD DATA TRANSCEIVERS. DATA DIRECTION CONTROL IS ACCOMPLISHED WITH IC 28. THIS TTL LOGIC DECODES THE "MEMORY SELECT" SIGNAL, IC28 PIN 3, THAT SWITCHES TO LOGIC 0 IF ANY OF THE ON-BOARD MEMORY IS SELECTED. ANOTHER NAND GATE FROM IC 28 DECODES THIS LINE ALONG WITH THE MPU BOARD READ/WRITE LINE TO ENABLE THE DATA INPUT BUFFERS. THESE DATA INPUT BUFFERS ARE ENABLED ONLY WHEN THE READ/WRITE LINE EQUALS LOGIC 1 AND THE "MEMORY SELECT" LINE EQUALS LOGIC 1, INDICATING ON-BOARD MEMORY IS NOT SELECTED. THE DATA OUTPUT BUFFERS TRANSFER INFORMATION TO THE S100 BUS WHENEVER THE MPU READ/WRITE LINE EQUALS LOGIC 0, A WRITE CYCLE.

S100 CONTROL LINES

S100 CONTROL LINES ARE GENERATED BY TTL LOGIC ON THE LEVEL II MPU BOARD. TIMING RELATIONSHIPS FOR MICROPROCESSOR READ AND WRITE CYCLES ARE SHOWN ON PAGE 14.

THEORY OF OPERATION

THE 6502 MICROPROCESSOR ADDRESSES INPUT/OUTPUT (I/O) EXACTLY AS IF IT WERE MEMORY. THIS ALLOWS USE OF THE COMPLETE MICROPROCESSOR INSTRUCTION SET ON I/O AS WELL AS MEMORY. MANY I/O CARDS DESIGNED FOR THE S100 BUS ARE ACTIVATED BY BUS LINE 46, STATUS INPUT, OR BUS LINE 45, STATUS OUTPUT. THE LEVEL II MPU BOARD DECODES A PAGE OF MEMORY AND ACTIVATES EITHER SINP OR SOUT DEPENDING ON THE STATUS OF THE READ/WRITE LINE.

SLOW MEMORY INTERFACE

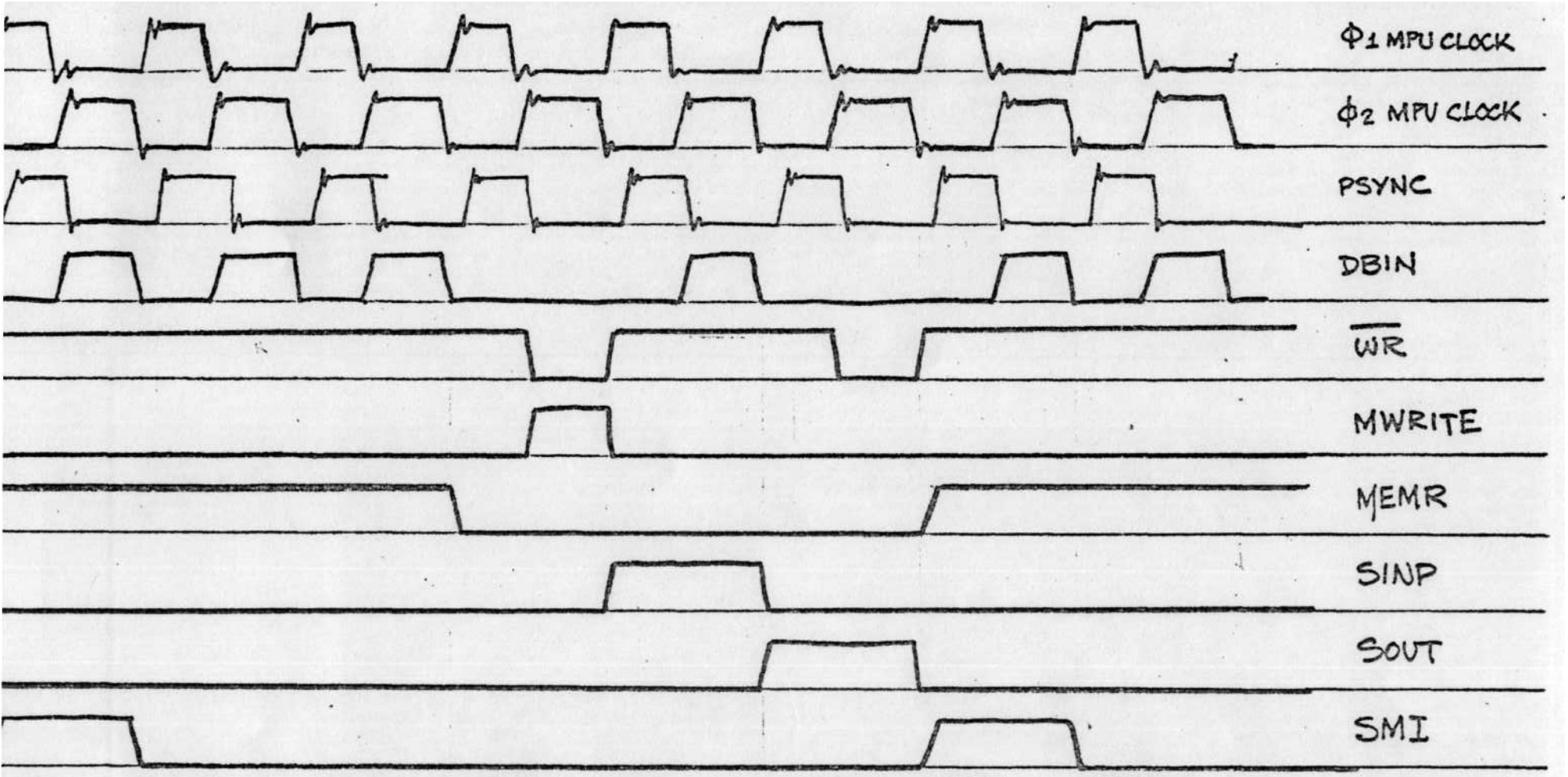
THE 6502 CAN BE HALTED INDEFINATELY BY PULLING ITS RDY LINE, PIN 2, TO LOGIC 0. SLOW S100 MEMORY BOARDS CAN BE ACCOMADATED BY THE LEVEL II MPU BOARD BY PULLING ONE OF THE S100 "READY" LINES, BUS LINE 3 OR 72, TO LOGIC 0. IF EITHER OF THESE LINES ARE PULLED TO LOGIC 0, A NAND GATE OF IC6 SWITCHES TO LOGIC 1. THIS SIGNAL IS FED TO IC4, A "D" TYPE FLIP-FLOP. THE FLIP-FLOP SYNCHRONIZES EXTERNAL INPUTS WITH THE 6502 MICROPROCESSOR. THE TIMING STRUCTURE OF THE 6502 IS CONSIDERABLY SIMPLER THAN THE 8080 AND IN SOME S100 BOARDS, ACTUAL WAIT STATES GENERATED MAY DIFFER FROM THOSE GENERATED BY AN 8080 SYSTEM. IN SOME OLDER MEMORY DESIGNS, ONE LESS WAIT STATE WAS GENERATED.

DIRECT MEMORY ACCESS

THE LEVEL II MPU BOARD CAN BE USED IN A DIRECT MEMORY ACCESS (DMA) MODE. DIRECT ACCESS TO THE S100 BUS CAN BE HAD BY PULLING BUS LINE 74, PHOLD, TO LOGIC 0. THE BOARD RESPONDS WITH LOGIC 1 TO BUS LINE 26, HALT ACKNOWLEDGE, INDICATING THE 6502 HAS STOPPED OPERATION. THE LEVEL II MPU BOARD THEN AUTOMATICALLY SIGNALS THE ADDRESS OUTPUT BUFFERS AND THE DATA OUTPUT BUFFERS TO SWITCH TO THEIR "TRI-STATE" OR HIGH-IMPEDANCE MODE. CONTROL LIMES FROM THE LEVEL II MPU BOARD WILL GO "TRI-STATE" WHEN BUS LINE 18, STATUS DISABLE, IS PULLED TO LOGIC 0.

THE LEVEL II MPU BOARD OPERATES DIFFERENTLY THAN OLDER 8080 CPU CARDS WITH REGARD TO DIRECT MEMORY ACCESS. OLDER STYLE CARDS DID NOT AUTOMATICALLY GO "TRI-STATE" WHEN THE MPU IS STOPPED. IN ADDITION, ALL LINES FROM THE LEVEL II MPU CARD DO NOT GO "TRI-STATE" WHEN BUS LINE 18 IS PULLED TO LOGIC 0. THEREFORE, WHEN USING DMA CARDS WITH THE LEVEL II MPU THE FOLLOWING LINES SHOULD BE DISCONNECTED ON THE DMA CARD; PWAIT LINE 27, SMI - LINE 44, AND DBIN - LINE 78.

-CONTINUED



6502/S100 INTERFACE TIMING RELATIONSHIPS

W.M.GOBLE
SEPT 6, 1977

THE CGRS BUS STRUCTURE

THE BUS STRUCTURE OF THE CGRS 6502 MPU BOARD CONFORMS TO THE PINOUT OF THE S100 (STANDARD - ONE HUNDRED) BUS STRUCTURE USED BY. OVER FIFTY MANUFACTURERS OF MICROCOMPUTER EQUIPMENT. THERE ARE DIFFERENCES IN THE EXACT FUNCTION OF CERTAIN PINS BETWEEN THE CGRS MPU BOARD AND THE ORIGINAL 8080 MPU BOARDS.

THE PINS USED ON THE CGRS BUS ARE:

PIN 1.	+ 8 VOLTS UNREGULATED	PIN 51.	+ 8 VOLTS UNREGULATED
PIN 2.	+18 VOLTS UNREGULATED	PIN 52.	-18 VOLTS UNREGULATED
PIN 3.	XRDY - EXTRA READY	PIN 53.	NC
PIN 4.	VI0- VECTOR INTERRUPT 0	PIN 54.	EXT CLR (RESET)
PIN 5.	VI1	PIN 55.	NC
PIN 6.	VI2	PIN 56.	NC
PIN 7.	VI3	PIN 57.	NC
PIN 8.	VI4	PIN 58.	NC
PIN 9.	VI5	PIN 59.	NC
PIN 10.	VI6	PIN 60.	NC
PIN 11.	VI7	PIN 61.	NC
PIN 12.	N.C.	PIN 62.	NC
PIN 13.	N.C.	PIN 63.	NC
PIN 14.	N.C.	PIN 64.	NC
PIN 15.	N.C.	PIN 65.	NC
PIN 16.	N.C.	PIN 66.	NC
PIN 17.	N.C.	PIN 67.	NC
PIN 18.	STATUS DSBL	PIN 68.	MWRITE
PIN 19.	N.C.	PIN 69.	PROTECT STATUS
PIN 20.	UNPROTECT	PIN 70.	PROTECT
PIN 21.	N.C.	PIN 71.	NC
PIN 22.	N.C.	PIN 72.	PRDY
PIN 23.	N.C.	PIN 73.	PINT (INTERRUPT REQ.)
PIN 24.	02 CLOCK	PIN 74.	PHOLD
PIN 25.	01 CLOCK	PIN 75.	PRESET (RESET)
PIN 26.	PHLDA	PIN 76.	PSYNC
PIN 27.	PWAIT	PIN 77.	PMR (WRITE)
PIN 28.	N.C.	PIN 78.	DBIN
PIN 29.	A5	PIN 79.	A0
PIN 30.	A4	PIN 80.	Al
PIN 31.	A3	PIN 81.	A2
PIN 32.	A15	PIN 82.	A6
PIN 33.	A12	PIN 83.	A7
PIN 34.	A9	PIN 84.	A8
PIN 35.	DO1	PIN 85.	A13
PIN 36.	DO0	PIN 86.	A14
PIN 37.	A10	PIN 87.	All
PIN 38.	DO4	PIN 88.	DO2
PIN 39.	DO5	PIN 89.	DO3
PIN 40.	DO6	PIN 90.	DO7

PIN 41. DI2	PIN 91. DI4
PIN 42. DI3	PIN 92. DI5
PIN 43. DI7	PIN 93. DI6
PIN 44. SMI (SYNC)	PIN 94. DI1
PIN 45. SOUT	PIN 95. DI0
PIN 46. SINP	PIN 96. NC
PIN 47. MEMR	PIN 97. NC
PIN 48. N.C.	PIN 98. NC
PIN 49. N.C.	PIN 99. POC (RESET)
PIN 50. GND	PIN 100 GND

THE MAIN DIFFERENCE BETWEEN THE BUS PINOUT OF THE CGRS 6502 MPU BOARD AND ORIGINAL 8080 BOARDS IS THAT THE 6502 BOARD DOES NOT GENERATE THE EXTRA 8080 STATUS LINES FOUND ON 8080 MPU'S. SINCE THESE LINES ARE NOT USED BY PERIPHERALS, NO PROBLEMS ARE EXPECTED.

OTHER DIFFERENCES ARE IN THE FUNCTION OF VARIOUS PINS OF THE 6502 MPU. 8080 MPU CARDS CAN ADDRESS UP TO 256 I/O "PORTS" BY ACTIVATING EITHER THE SINP (INPUT) OR SOUT (OUTPUT) LINE AND TRANSMITTING AN EIGHT BIT ADDRESS. THE 8080 MPU CARDS DUPLICATE THE I/O ADDRESS ON BOTH THE HIGH ORDER ADDRESS (A8-A15) AND THE LOW ORDER ADDRESS LINES (A0-A7). THE 6502 MICROPROCESSOR EXCLUSIVELY ADDRESSES "MEMORY-MAPPED" I/O. THE S100 INTERFACE IS ACCOMPLISHED BY DECODING A SINGLE PAGE OF MEMORY AND ACTIVATING SINP OR SOUT WHEN THIS OCCURS. THE I/O ADDRESS IS THEN TRANSMITTED OVER THE LOW ORDER ADDRESS LINES (A0-A7). THE 6502 MPU DOES NOT DUPLICATE THE I/O ADDRESS ON THE HIGH ORDER ADDRESS LINES. VERY FEW OF THE S100 I/O BOARDS DECODE THE HIGH ORDER ADDRESS LINES, HOWEVER THOSE THAT DO WILL NEED TO BE MODIFIED. A LIST OF I/O BOARDS IS INCLUDED IN THE COMPATIBILITY SECTION.

THE TIMING OF THE 6502 IS ONE COMPLETE LEVEL SIMPLER THAN THE 8080. THIS ALLOWS THE 6502 TO ACTUALLY OPERATE OVER TWICE AS FAST AT THE SAME BASE CLOCK SPEED. THESE TIMING DIFFERENCES ARE REFLECTED IN THE CONTROL LINES OF THE 6502 MPU BOARD BUT THIS MAKES LITTLE DIFFERENCE IN THE OPERATION OF S100 MEMORY AND I/O BOARDS. ON SOME S100 MEMORY CARDS, THE ACTUAL NUMBER OF "WAIT" STATES WILL BE LESS THAN THE DESIGNATED NUMBER. HOWEVER, WAIT STATES ARE RARELY REQUIRED WITH THE 6502 OPERATING AT 1 MHZ BECAUSE OF ITS SIMPLE TIMING STRUCTURE.

FOLLOWING IS A LIST OF S100 BOARDS AND THEIR STATUS WITH REGARD TO THE 6502 MPU BOARD.

S100 BOARD LISTING

OCT., 1977

THE FOLLOWING BOARDS HAVE BEEN TESTED AND FOUND COMPATIBLE WITH THE 6502 MPU BOARD.

1. SOLID STATE MUSIC MB6: 8K RAM
2. ITHACA AUDIO: 8K RAM
3. IMSAI RAM4: 4K RAM
4. IMSAI RAM4A: 4K RAM*
5. TECHNICAL DESIGN LABS Z-16: 16K RAM
6. VANDENBURG DATA SYSTEMS: 16K RAM* (DOES NOT WORK IN SINGLE CYCLE MODE WITH FRONT PANEL)
7. SOLID STATE MUSIC MB7: 16K ROM
8. SOLID STATE MUSIC VBl: VIDEO OUTPUT BOARD
9. POLYMORPHICS VIDEO TERMINAL INTERFACE (KEYBOARD INPUT LATCH MUST BE REMOVED)
10. IMSAI 3P&S I/O BOARD
11. MERLIN - MULTI-PURPOSE VIDEO BOARD.

THE FOLLOWING BOARDS HAVE BEEN SCHEMATICALLY REVIEWED AND APPEAR PERFECTLY COMPATIBLE.

1. S.D. SALES 4K RAM
2. DUTRONIC 8K RAM
3. FRANKLIN ELECTRIC 8K RAM
4. SPEECHLOB - SPEED SYNTHESIZER
5. PERIPHERAL VISION - FLOPPY DISK CONTROLLER
6. TARBELL CASSETTE INTERFACE
7. CROMENCO T.V. DAZZLER (SIMPLE MODIFICATION REQ'D)
8. CROMENCO FLOPPY DISK CONTROLLER
9. PROCESSOR TECHNOLOGY - 4KRA: 4K RAM
10. MITS 882SIO: 2 PORT SERIAL INTERFACE
11. MITS 88-4 PIO: 4 PORT PARALLEL INTERFACE
12. POLYMORPHIC
13. NATIONAL MULTIPLEX

THE FOLLOWING BOARDS HAVE BEEN REVIEWED AND FOUND TO BE INCOMPATIBLE.

1. ICOM: FLOPPY DISK CONTROLLER (THIS BOARD DECODES HIGH ORDER ADDRESS LINES FOR I/O. MODIFICATION REQUIRED.)
2. PROCESSOR TECHNOLOGY VDM-1: VIDEO BOARD (THIS BOARD ALSO DECODES HIGH ORDER ADDRESS LINES FOR I/O. OTHER THAN MODE LATCH, THIS BOARD WORKS PERFECTLY.)

CGRS MICROTECH

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