ME32K RAM/ROM/Bootstrap Module

1 February 2025

PREFACE

This manual provides the information needed to install, operate, maintain, and troubleshoot the ME32K Rev D RAM/ROM/Bootstrap Module by Martin Eberhard

The reader is assumed to have a basic knowledge of digital computer theory and an understanding of the PDP11/20 computer in which the ME32K is used.

TABLE OF CONTENTS

1 GENERAL INFORMATION

1.1 Introduction

This manual provides the information needed to install, operate, maintain and troubleshoot the ME32K Rev C memory, designed by Martin Eberhard

The material is arranged into five sections as follows:

Section 1 - GENERAL INFORMATION contains a brief functional description and specifications of the ME32K.

Section 2 - INSTALLATION explains the requirements and procedures for equipment installation. Address selection and other options are described.

Section 3 - THEORY OF OPERATION. contains a detailed functional description of the ME32K

APPENDIX - The appendix contains the parts list, logic diagrams, and assembly drawing required for a complete understanding of the unit.

1.2 General Description

The ME32K provides Random-Access Memory (RAM), Read-Only Memory (ROM), and Bootstrap capability for Digital Equipment Corporation (DEC) PDP11 computers that have Unibus interfaces - especially the PDP11/20. It is designed to plug into any Small Peripheral Option slot on the Unibus, such as those on a DD-11A System Unit or in slots 13 and 14 of the PDP11/20 (which are also for small peripheral options).

1.2.1 RAM Capacity and Address

RAM on the ME32K is fully-static memory, comprising 32,768 words, 16 bits each. (This is the maximum memory in a basic PDP11/20.) Switches on the ME32K allow you to select one of four address ranges for the ME32K, for systems that can address 128K words of memory.

Memory on the ME32K between 760000_8 and 777777_8 is disabled because this region is reserved by PDP11/20 convention for device registers, I/O devices and ROMs. Note that in its standard configuration (without a KT11-B Paging Option), the PDP11/20 CPU will map addresses between 160000_8 and 177777_8 into this I/O region between 760000_8 and 777777_8.

The ME32K RAM can be battery-backed so that it retains its data when the PDP11's power is off, similar to core memory.

The ME32K RAM can be disabled with a DIP switch setting.

1.2.2 ROM Capacity and Addresses

The ME32K supports ROM in two regions. Low ROM is between 765000_8 and 765777_8. High ROM is between 773000_8 and 773777_8. Each ROM bank can be disabled with a DIP switch setting, (The PDP11 normally has its "console emulator" and diagnostics firmware in Low ROM, and a selection of boot loader programs in High ROM.)

The ME32K supports up to 8 separate pairs of Low ROM and High ROM data, selectable with a DIP switch setting.

1.2.3 Bootstrap Vector

The ME32K supports a bootstrap vector similar to that on the DEC M9312 Bootstrap-Terminator board.

Immediately following power-on, the bootstrap vector hardware forces the PDP11's program counter (PC) and status register to be read from addresses 773024_8 and 773026_8, instead of the PDP11/20's normal addresses, 000024_8 and 000026_8. This feature can be disabled with a DIP switch.

773024_8 is the address of the Bootstrap Vector Switch Bank, which is only available if high ROM is also enabled. This 16-bit switch bank specifies the initial PC value. (Though bit 0 should always 0.) The Bootstrap Vector Switch Bank can be disabled with a DIP switch. When disabled, reading from address 773024_8 will read from high ROM instead, assuming high ROM is enabled.

1.2.4 Access and Cycle times

Access time is the time from when MSYN initiates a bus cycle to when the ME32K ends the cycle with SSYN. Unlike core memory, reading is nondestructive and writes do not require memory to be cleared first. This means that cycle time for the ME32K is the same as its access time.

Item	Nominal	Maximum
RAM Read Access Time	200 ns	350 nS
RAM Write Access Time	200 nS	350 nS
RAM Read Access Time, Battery Backup Deleted	140 nS	160 nS
RAM Write Access Time, Battery Backup Deleted	140 nS	160 nS
ROM Read Access Time	140 nS	160 nS

1.3 Unibus Interface

1.3.1 Access Modes

The ME32K operates in several different modes, as determined by the state of address Bit A00 and control lines C0 and Cl. The modes of operation are as follows. (0 means "inactive," 1 means "active", and X means "any state." These signals on the Unibus are negative signals, meaning that active signals are below 0.8V and inactive signals are above 2.4V.)

C0	C1	A00	Mode	Description
0	x	X	Read	16-bit read operation
1	0	X	Word Write	16-bit write operation
1	1	0	Low-Byte Write	8-bit write to D<7:0>
1	1	1	High-Byte Write	8-bit write to D<15:8>

1.3.2 Writing to ROM Addresses

Attempts to write to ROM are ignored by the ME32K, which will cause a Unibus timeout, invoking a TRAP operation by the PDP11. You can modify the ME32K to respond (with the SSYN signal) to writes in the ROM address spaces, though no actual writes will occur.

Operation	Side	Location
Cut	Solder	Trace between E14 pin 6 and E15 pin 10
Cut	Solder	Trace between E19 pin 20 and via to GND, near E19 pin 14
Jumper	Solder	From E14 pin 6 and E14 pin 16
Jumper	Solder	From E19 pin 20 and E1 pin 1

1.3.3 Interface Signals

The following signals of the Unibus Small Peripheral Interface are used by the ME32K:

Name	Dir	Pin	Function	Name	Dir	Pin	Function	Name	Dir	Pin	Function
A00	IN	EH2	Byte Select	A13	IN	EK2	Address 13	D05	I/O	CP2	Data 5
A01	IN	EH1	Address 1	A14	IN	EK1	Address 14	D06	I/O	CV2	Data 6
A02	IN	EF1	Address 2	A15	IN	ED2	Address 15	D07	I/O	CM2	Data 7
A03	IN	EV2	Address 3	A16	IN	EE2	Address 16	D08	I/O	CL2	Data 8
A04	IN	EU2	Address 4	A17	IN	ED1	Address 17	D09	I/O	CK2	Data 9
A05	IN	EV1	Address 5	MSYN	IN	EE1	Master Sync	D10	I/O	CJ2	Data 10
A06	IN	EU1	Address 6	C0	IN	EJ2	Mode 0	D11	I/O	CH1	Data 11
A07	IN	EP2	Address 7	C1	IN	EF2	Mode 1	D12	I/O	CH2	Data 12
A08	IN	EN2	Address 8	D00	I/O	CS2	Data 0	D13	I/O	CF2	Data 13
A09	IN	ER1	Address 9	D01	I/O	CR2	Data 1	D14	I/O	CE2	Data 14
A10	IN	EP1	Address 10	D02	I/O	CU2	Data 2	D15	I/O	CD2	Data 15
A11	IN	EL1	Address 11	D03	I/O	CT2	Data 3	SSYN	OUT	EJ1	Slave Sync
A12	IN	EC1	Address 12	D04	I/O	CN2	Data 4	DC LO	IN	CN1	Power fail

1.3.4 Power Supply

Power is supplied to the ME32K with the following Unibus Small Peripheral Interface pins:

Supply	Pins	Function
GND	CC2, CT1	Ground, used for data bus transceivers
GND	DC2, DT1	Ground, used for onboard logic and memory components
GND	EC2, ET1	Ground, used for address and control bus receivers
+5V	CA2	+5 Volts, used for data bus transceivers
+5V	DA2	+5V, used for onboard logic and memory components
+5V	EA2	+5V, used for address and control bus receivers

1.4 Physical Specifications

The ME32K consists of a single 3-high circuit board that occupies connectors C,D, and E of one Small Peripheral Option interface slot on the Unibus. Note that the AAA batteries are positions so as not to interfere with an adjacent board, despite their height.

Characteristic		Specification
Interface Signal Levels:	High (inactive)	2.4V
	Low (active)	0.8V
Mechanical Dimensions:	Width	7.7 inches
	Height	8.5 inches, not including handles
Max Component Height	Without AAA batteries	0.33 inches, not including handles
	With AAA batteries	0.50 inches

1.4.1 Power Requirements

Voltage	Standby Current	Operating Current	
		Typical	Worst Case
+5V		350 mA	650 mA

2 CONFIGURATION AND INSTALLATION

2.1 Assembly Options

The ME16K can be assembled a few different ways, trading off speed, cost, and functionality.

2.1.1 EPROMs

The ME2732 supports the following EPROM types: 2732, 2764, 27128, 27256, and 27512. If EPROMs are used, then both EPROMs must be installed. The EPROM at E18 contains the even bytes, and the EPROM at E17 contains the odd bytes of every word.

Note that data in the EPROMs must be inverted when the EPROMs are programmed.

Only 4K-bytes from each EPROM are used, with the EPROM at E18 contains the even bytes, and the EPROM at E17 contains the odd bytes of every word in the 4K-word EPROM space.

For EPROMs larger than 2732's, address pin A12 is tied low, and all higher address lines are tied high. (This is represented by the "(E)" in the table below.)

The 4K-word EPROM space is subdivided into eight 512-word banks, which are selectable by DIP switch SW1. (See below.)

Each 512-word bank is further subdivided into a 256-word Low-ROM region and a 256-word high-ROM region The EPROM data is mapped into the PDP11 address space as follows. (This table shows the EPROM address for both the low-byte EPROM and the high-byte EPROM.)

EPROM Address Range (Hex)	ROM Bank	ROM Region	PDP11 Address Range (Octal)
(E)000-(E)0FF	0	Low ROM	765000-765777
(E)100-(E)1FF	0	High ROM	773000-773777
(E)200-(E)2FF	1	Low ROM	765000-765777
(E)300-(E)3FF	1	High ROM	773000-773777
(E)400-(E)4FF	2	Low ROM	765000-765777
(E)500-(E)5FF	2	High ROM	773000-773777
(E)600-(E)6FF	3	Low ROM	765000-765777
(E)700-(E)7FF	3	High ROM	773000-773777
(E)800-(E)8FF	4	Low ROM	765000-765777
(E)900-(E)9FF	4	High ROM	773000-773777
(E)A00-(E)AFF	5	Low ROM	765000-765777
(E)B00-(E)BFF	5	High ROM	773000-773777
(E)C00-(E)CFF	6	Low ROM	765000-765777
(E)D00-(E)DFF	6	High ROM	773000-773777
(E)E00-(E)EFF	7	Low ROM	765000-765777
(E)F00-(E)FFF	7	High ROM	773000-773777

A typical EPROM configuration would put DEC's Console/Diagnostic PROM data in the low ROM region and four different boot ROMs' data in the high ROM region. The ROM bank select switches allow you to have up to eight different configurations, supporting alternative Console/Diagnostic programs and alternative boot ROM data.

2.1.2 Delete Battery Backup

Battery backup for the static RAM's can be deleted, which has the effect of speeding up SRAM accesses by as much as 200 nS per cycle. To delete battery backup:

1. Do not install either battery holder (B1 or B2)
2. Do not install an IC in location E21 (the MAX693)
3. Install a jumper from pin 2 to 3 at IC location E21
4. Install a jumper from pin 12 to pin 13 at IC location E22
5. Optionally, delete transistor Q1. (Leaving it in is harmless but also useless.)
6. Optionally, delete diode D1 and replace it with a jumper wire. You can then delete resistor R6.

2.1.3 Battery Type for Backup

The ME32K can be assembled to use either a 20 mm (CR2032) lithium "coin-cell" or two AAA batteries, to power the static RAM chips when the PDP11 power is off. The coin cells are (obviously) much smaller and less prone to chemical leakage. The AAA batteries have much higher capacity.

For a coin cell, the battery holder is part number 122-2620-GR, manufactured by Eagle Plastic Devices. For AAA batteries, the battery holder is part number 12BH425P-GR, manufactured by Eagle Plastic Devices.

It is strongly recommended that lithium-type batteries be used for the AAA battery option (as opposed to alkaline or "standard" AAA batteries), to reduce the chance of chemical leakage as the batteries age.

2.1.4 Grounding Options

Per the recommendations on page 4-6 of *PDP-11 Unibus(tm) Design Description* published by Digital Equipment Corporation, the backplane power and ground pins used for the ME32K's onboard logic are completely separate from those used to power the bus transceiver ICs.

Should you wish to connect the separate ground signals on the ME32K, install jumpers at J1 and J2. (Normally, these should not be jumpered.)

2.1.5 NPG

The ME32K does not do Active Data Transmission (DMA), and therefore does to use the Unibus NPG signal. You can pass this signal on through the ME32K by installing a jumper wire at J3.

2.2 Switch-Selectable Options

There are four DIP switches on the ME32K, which allow you to control various options.

2.2.1 DIP Switch SW1

Switch 1 of SW1 disables Power-On Boot when closed.

The two EPROMs contains 8 separate 512-word EPROM banks, Only one bank is available to the PDP11 at any time, selectable with SW1 switches 2 through 4:

SW1 Switch			EPROM Bank
4	3	2	
on	on	on	Bank 0
on	on	off	Bank 1
on	off	on	Bank 2
on	off	off	Bank 3
off	on	on	Bank 4
off	on	off	Bank 5
off	off	on	Bank 6
off	off	off	Bank 7

2.2.2 Bootstrap Vector Switch Bank (DIP Switches SW2 and SW3)

SW2 switch 6 disables the Bootstrap Vector when closed. When this switch is open, reading from address 173024_8 will always read from the Bootstrap Vector Switch Bank (BVSB).

SW2 and SW3 together specify the 16-bit Bootstrap Vector. For these switches, closed represents a logical 1 and open represents a logical 0. SW3 switch 8 is the most-significant bit (bit 15), and SW2 switch 1 is the least-significant bit (bit 0). Bit 0 should always be set to 0.

2.2.3 DIP Switch SW4

The 6-positionDIP Switch at location SW4 provides the following options:

SW2 Switch	Off	On
1	RAM is disabled	RAM is enabled
2	Unibus A16 must be low to address RAM	Unibus A16 must be high to address RAM
3	Unibus A17 must be low to address RAM	Unibus A17 must be high to address RAM
4	High ROM is disabled	High ROM is enabled
5	Low ROM is disabled	Low ROM is enabled
6	BVSB is disabled	BVSB is enabled

For a basic PDP11/20 (without a KT11-B Paging Option) set both switches 2 and 3 to the Off position.

RAM between 760000_8 and 777777_8 is disabled on the ME32K because this region is for I/O devices and ROMs. Note that in its standard configuration, the PDP11/20 will map addresses between 160000_8 and 177777_8 into this I/O region between 760000_8 and 777777_8.

2.3 Installation

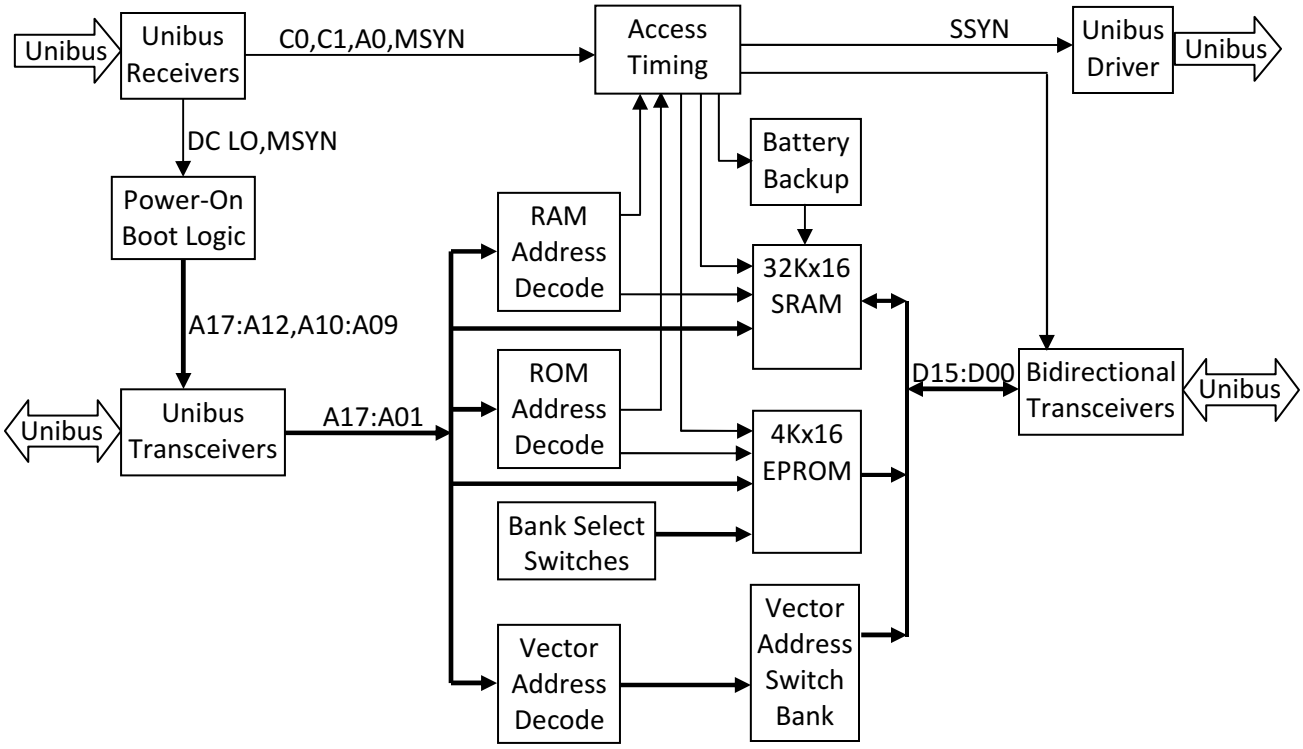
Once the ME32K is configured correctly, it can be installed in any PDP-11 Unibus Small Peripheral Option slot, such as those on a DD-11A System Unit or in slots 13 and 14 of the PDP11/20's CPU system unit (which are also for small peripheral options).

The ME32K occupies one Small Peripheral Option interface slot on the Unibus. It plugs into connectors C, D, and E, leaving connectors A, B (on the right) and slot F (on the left) unused.

A wire may be needed to connect the Unibus DC LO L signal to pin CxN1, where x is the slot number for the ME32K.

3 THEORY OF OPERATION

3.1 Block Diagram



3.2 Circuit Descriptions

3.2.1 Unibus Receivers, Drivers, and Transceivers

The single-direction Unibus receivers are the DS8640, which is equivalent to the DEC8640, as specified on page 4-1 of *PDP-11 Unibus(tm) Design Description* published by Digital Equipment Corporation.

The single-direction Unibus driver is the DEC8881, also as specified by DEC.

The eight address lines (A09, A10, and A12 through A17) that are driven by the ME32K during power-on boot are buffered using the bidirectional DS8641 transceiver, equivalent to the DEC 8641 as specified by DEC.

DEC did not specify a bus transceiver with a bidirectional bus on the both sides. The ME32K uses a 74LS639 for this purpose. The two 74LS639s are enabled whenever either RAMSEL or ROMSEL is true. Its direction is controlled by C0, which is low for read transactions and high for write transactions.

Data sheets for these ICs may be found in the Appendix.

3.2.2 RAM Address Decode

RAM address decode is shown in the upper-left corner of the schematic, comprising ICs E16, half of E23, and related gates, and 2 switches in SW4.

The two exclusive -OR gates in E23 (E23a and E23b) compare the DIP switch setting to Unibus address bits A16 and A17. If the Unibus address matches the DIP switch setting, then the outputs of both exclusive-OR gates will be high (true).

E16b and related gates detect addresses in the range that is reserved for PDP-11 I/O and ROM accesses. If the Unibus address is in this range then the output of E16b will be low (false), which will block RAM accesses.

E16a's output will be low (true) if the Unibus address matches the DIP switch selections, and the address does not match the I/O/ROM address range, and the Unibus MSYN signal is true. This output is SRAMSEL L, where low (true) means the cycle on the bus is accessing the ME32K's RAM.

3.2.3 ROM Address Decode

ROM address decode is directly below the RAM address decode on the schematic, comprising E14, E16b, three gates from E24, and two switches in SW4.

E14, E16b, and related gates decode ROM accesses for both the Low ROM address region and the High ROM address region. SW4 switches 4 and 5 independently enable/disable either ROM region.

E24a logically OR's the two region selects to produce the ROMSEL signal, which enables the EPROM outputs. The active-low Low ROM select signal drives EPROM address bit 8, so that the low half of every 512-word bank is Low ROM, and the high half is High ROM.

EPROM address signals A<11:A9> are connected to SW1 switches 2 through 4, selecting one of the eight possible ROM banks.

If the Vector Vector Address Switch Bank is enabled (via SW4 switch 6), then the EPROMs are disabled for the single 16-bit word at address 173024_8.

3.2.4 Bootstrap Vector Address

The ME32K can provide a bootstrap vector address via the Vector Address Bank. The Vector Address Switch Bank is available only if High ROM is also enabled (by closing SW3 switch 4). When enabled (by closing SW4 switch 6), reading from address 173024_8 will read from the Vector Address Switch Bank (SW2 and SW3. This address is decoded by E17, E18, and related gates.

3.2.5 Power-On Boot

When enabled (by opening SW1 switch 1), the ME32K will force address bits 9-10 and 12-17 high during the first two Unibus transactions after the Unibus DC LO signal goes false. During these Unibus transactions, the PDP11/20's CPU will attempt to read from address 000024_8 for its initial Program Counter value, and from 000026_8 for its initial Status Register value. The Power-On Boot logic changes these addresses to 173024_8 and 173026_8.

When Power-On Boot is enabled, E12 holds the VECTOR signal true until the end of the second MSYNC pulse. While VECTOR is true, E4 and E8 drive the required address line to their "1" state. (Note that signals on the Unibus are active-low.)

3.2.6 Access Timing

Unibus

Unibus timing is completely asynchronous. When the current bus master wants to access memory, it puts the desired address on the Unibus address signals, sets the two Unibus control signals, C0 and C1, appropriately for the type of transaction it needs, for a write cycle, puts the write data on the Unibus data signals, and then waits 150 nS to account for propagation delays, skew, and setup times. At this

point, the bus master sets MSYNC true to indicate the start of the transaction. The bus master will then wait until it gets a response from the bus slave (in this case the ME32K).

For a write cycle, the slave sets SSYN true once it has latched the data from the Unibus. For a read cycle, the slave sets SSYN true when the requested data is on the Unibus data signals.

When the bus master sees SSYN true, it waits 150 nS, then (in the case of a read cycle) latches the data from the Unibus. It then sets MSYN low, indicating the end of the cycle.

SRAM Accesses

When the slave sees MSYN become false, it sets SSYN false, indicating that it is ready for another cycle.

The SRAM on the ME32K has 100 nS access time, meaning that data is stable on its data pins 100 nS from when Chip Select goes low (true).

The Chip Select signal is SRAMSEL L, after it passes through the MAX693 (discussed later). The propagation through the MAX693 is specified as 50 nS nominal, 200 nS maximum. Because of this long and loosely-specified propagation delay, the ME32K starts its SRAM cycle based on the the output of the MAX693.

The low-going leading edge of the SRAM Chip Select signal triggers one-shot E26, whose output is configured to generate a negative pulse starting at the trigger and ending 125 nS later. The trailing edge of this pulse clocks a 1 into flip-flop E25b, which set the SSYN signal true on the Unibus SSYN remains true until the end of the MSYN pulse, as controlled by the bus master.

If C0 indicates a write cycle, then flip-flop E25a's output goes high (true) when the output of E25b is true. E25a's output, combined with Unibus signals A0 and C1, generate the active-low write enable signals to the two SRAM chips. (See the table in section 1.3.) The Write Enable signals end when SSYN ends.

Gate E15A delays the start of the SSYN pulse until the SRAM write Enable signal is low (true), to guarantee stable data when the SRAM chips latch data at the leading edge of the Write Enable signal.

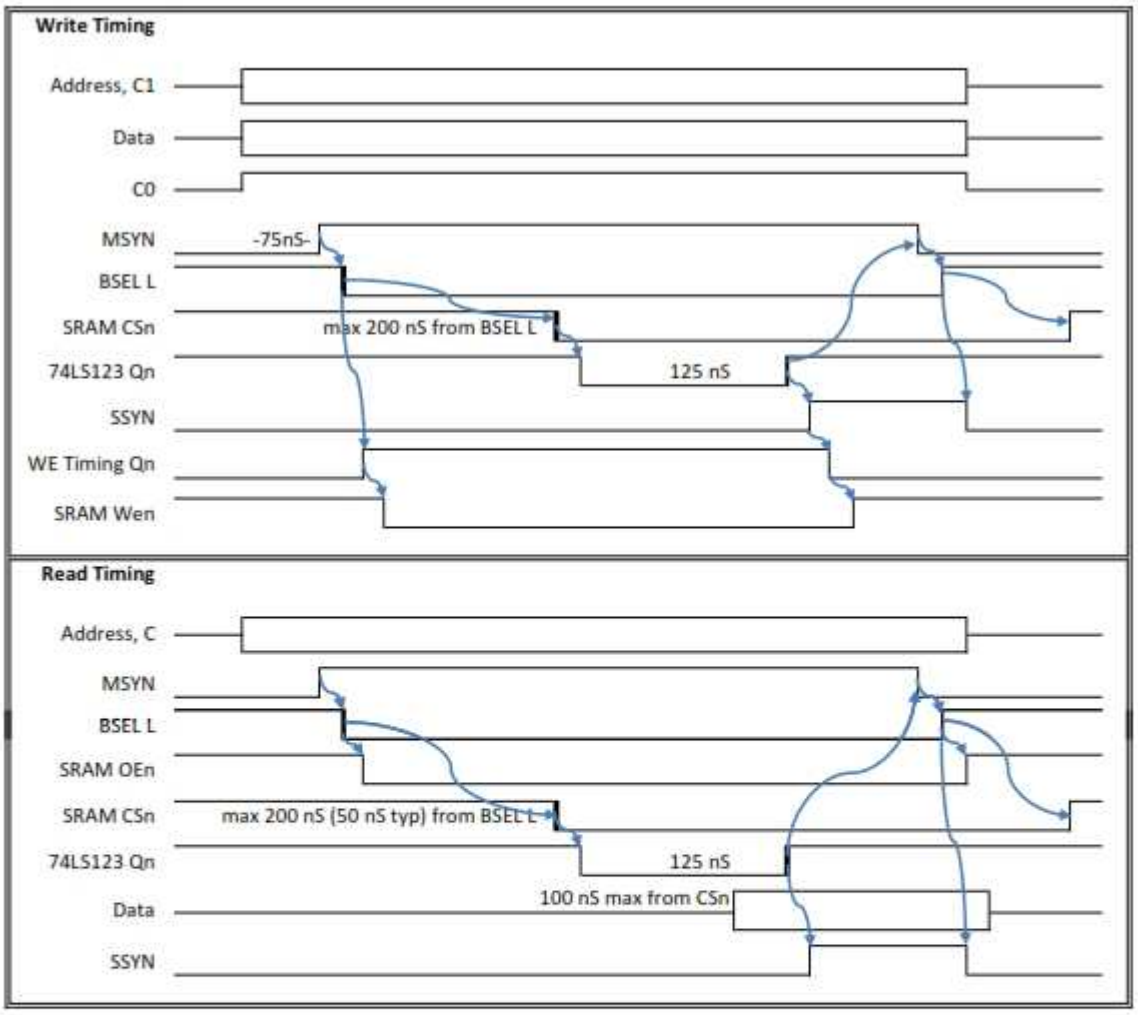
ROM Accesses

The ME32K ROMs are specified to be 150 nS EPROMs, such as the Fairchild NMC27C32B. This means that their data signals will be stable no more that 150 nS after their address pins are stable and their Chip Enables pins are low (true).

Because the Chip Enable signals of the EPROMs are tied low (true), they will begin decoding their address as soon as it is stable, which will be long before ROMSEL is true. When ROMSEL becomes true (after MSYN becomes true), then the EPROM's outputs are enabled via their Output Enable signals. The access time for these EPROMs from Output Enable to stable data is specified as 60 nS maximum. This means that the 125 nS delay of the one-shot at E24 is adequate time for EPROM accesses.

During a ROM read cycle, the SSYN signal is started 125 nS after ROMSEL is high (true). This implies that the Unibus address signals must be stable 25 nS before MSYN becomes active.

RAM and ROM Timing Diagrams



3.2.5 256x16 ROM

The ME32K's ROM comprises two 150 nS (or faster) 2732-type 4Kx8 EPROMs.. See the Fairchild NM27C32B data sheet in the Appendix for details.

Note that the data in the EPROMs are inverted if the two data buffer chips are 74LS639's. (74LS638s would allow for non-inverted EPROM data, but these seem to be unavailable.)

3.2.6 32Kx16 RAM

The ME32K's RAM comprises two 100 nS (or faster) 32Kx8 fully-static RAM chips, such as the Hitachi HM62256APL-100. See the Hitachi data sheet in the Appendix for details.

3.2.7 Battery Backup

The SRAM chips are backed up with a nominally 3-volt battery. Backup is managed by a MAX693 Microprocessor Supervisory Circuit at location E21.

The MAX693 maintains the integrity of the data in SRAM. The ME32K's 5-volt supply drops below 4.4 volts, the MAX693 de-asserts the SRAM Chip Select signal (to prevent unintended writes), and switches over to the battery to power the SRAM chips. (Transistor Q1 boosts the current capability of the MAX693, so that most SRAM chips can be powered by this circuit.)

As discussed above, the propagation of the Chip Select signal through the MAX693 is surprisingly slow, with a maximum propagation delay of 200 nS. For this reason, the ME32K does not start timing SRAM accesses until the Chip Enable signal has made it through the MAX693.

Since the Chip Enable output of the MAX693 is driving a chip (E23c) that is not battery-backed, this signal is buffered by Schottkey diode D1, with resistor R6 acting as a pullup. This prevents the MAX693 from supplying any current to an unpowered IC at E23.

With the "L" version of the Hitachi SRAM chip, power consumption during standby is typically 0.3 uA, but could be as high as 100 uA for each of the two SRAM chips.

A CR2032 lithium coin cell battery has a capacity of 225 mAh. We can calculate how long this battery will last when powering the ME32K's SRAMs:

225,000 / (2* 0.3) =375,000 hours, or 42 years, typical case.

225,000 / (2* 100) = 1125 hours, or 46 days, worst case.

An Energizer L92 lithium AAA battery has a capacity of 1250 mAh, We can calculate how long a pair of these batteries will last when powering the ME32K's SRAMs:

1,250,000 / (2* 0.3) =about 2,000,000 hours, or238 years, typical case.

1,250,000 / (2* 100) = 6250 hours, or 260 days, worst case.

Without data, we can assume that the SRAM chips will tend to behave more like the typical case cited in the datasheet.

APPENDIX

A.1 Bill of Materials

Part No.	Device	Qty	Locations	Comment
74LS00	Quad 2-Input NAND	2	E13, E24	
74LS04	Hex Inverter	2	E15,E22	
74LS20	Dual 4-Input NAND	1	E16	
74LS27	Triple 3Input NOR	1	E17	
74LS30	8-Input NAND	1	E18	
74LS74	Dual D-Type Flip-flop	2	E12,E25	
74LS86	Quad XOR	1	E23	
74LS123	Dual One-Shot	1	E26	
74LS138	3:8 Decoder	1	E14	
74LS245	8-bit Bidirectional Buffer	2	E28,E29	
74LS639	8-bit Bidirectional Buffer	2	E1, E2	
DS8640	Quad Unibus Receiver	4	E3,E4,E7,E9	Equivalent: DEC8640
DS8641	Quad Unibus Transceiver	2	E5,E8	Equivalent: DEC8641
8881	Quad Unibus Driver	1	E6	
NM27C32B	4K-byte EPROM	2	E18,E19	Programmed
HM62256ALP-10	100 nS 128K-byte SRAM	2	E10,E11	-10SL version is better
MAX693	Microprocessor Supervisory Ckt	1	E20	Battery backup control
IC Socket28	24-pin, 0.6” wide IC socket	2	E18,E19	
DIPSW, 4 Pos	4-position DIP Switch	1	SW1	
DIPSW, 6 Pos	6-position DIP Switch	1	SW4	
DIPSW, 8 Pos	8-position DIP Switch	2	SW2,SW3	
BAT46	Schottkey Diode	1	D1	
Cap, 0.1 uF	0.1 uF Ceramic Capacitor	29	C1-C29	
Cap, 100 pF, 5%	100 pF±5% Ceramic Capacitor	1	C30	
Cap, 10uF 10V	10 uF 10V Electrolytic Capacitor	3	C31-C33	
Res, 1K	1KΩ±5% Resistor	2	R4,R5	
Res, 4.7K	4.7KΩ±5% Resistor	10	R1-R3, R6-R12	
Res, 1.74K, 1%	1.74KΩ±1% Resistor	1	R13	
2N6520	NPN Transistor	1	Q1	
122-2620-GR	20mm Coin Cell Battery Holder	1	B1	Option: either B1 or B2
12BH425P-GR	Double AAA battery holder	0	B2	Option: either B1 or B2

A.2 Component Specifications

Following are data sheets for some of the less-common components used on the ME32K

A.2.1 HM62246ALP-100 SRAM

HM62256A Series — Maintenance only

32,768-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM62256A is a CMOS static RAM organized 32-kword × 8-bit. It realizes higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology. The device, packaged in a 8 × 14 mm TSOP with thickness of 1.2 mm, 450-mil SOP (foot print pitch width), 600-mil plastic DIP, or 300-mil plastic DIP, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided. It offers low power standby power dissipation; therefore, it is suitable for battery back up system.

Features

- High speed: Fast Access time 85/100/120/150 ns (max)
- Low Power
  Standby: 5 µW (typ) (L/L-SL version)
  Operation: 40 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation

Ordering Information

Type No.	Access time	Package
HM62256AP-8	85 ns	600-mil 28-pin plastic DIP (DP-28)
HM62256AP-10	100 ns	
HM62256AP-12	120 ns	
HM62256AP-15	150 ns	
HM62256ALP-8	85 ns	
HM62256ALP-10	100 ns	
HM62256ALP-12	120 ns	
HM62256ALP-15	150 ns	
HM62256ALP-8SL	85 ns	
HM62256ALP-10SL	100 ns	
HM62256ALP-12SL	120 ns	
HM62256ALP-15SL	150 ns	
HM62256ASP-8	85 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62256ASP-10	100 ns	
HM62256ASP-12	120 ns	
HM62256ASP-15	150 ns	
HM62256ALSP-8	85 ns	
HM62256ALSP-10	100 ns	
HM62256ALSP-12	120 ns	
HM62256ALSP-15	150 ns	
HM62256ALSP-8SL	85 ns	
HM62256ALSP-10SL	100 ns	
HM62256ALSP-12SL	120 ns	
HM62256ALSP-15SL	150 ns	
HM62256AFP-8T	85 ns	450-mil 28-pin plastic SOP (FP-28DA)
HM62256AFP-10T	100 ns	
HM62256AFP-12T	120 ns	
HM62256AFP-15T	150 ns	
HM62256ALFP-8T	85 ns	
HM62256ALFP-10T	100 ns	
HM62256ALFP-12T	120 ns	
HM62256ALFP-15T	150 ns	
HM62256ALFP-8SLT	85 ns	
HM62256ALFP-10SLT	100 ns	
HM62256ALFP-12SLT	120 ns	
HM62256ALFP-15SLT	150 ns	

Note: This device is not available for new application.

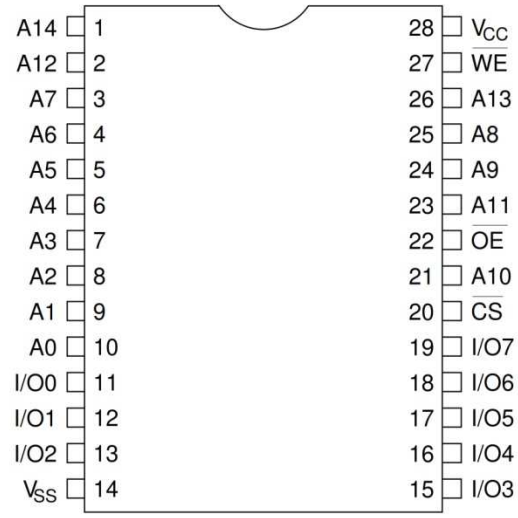
TSOP Series

Type No.	Access time	Package
HM62256ALT-8	85 ns	8 mm × 14 mm
HM62256ALT-10	100 ns	32-pin TSOP
HM62256ALT-12	120 ns	(normal type)
HM62256ALT-15	150 ns	(TFP-32DA)
HM62256ALT-8SL	85 ns	
HM62256ALT-10SL	100 ns	
HM62256ALT-12SL	120 ns	
HM62256ALT-15SL	150 ns	

Type No.	Access time	Package
HM62256ALR-8	85 ns	8 mm × 14 mm
HM62256ALR-10	100 ns	32-pin TSOP
HM62256ALR-12	120 ns	(reverse type)
HM62256ALR-15	150 ns	(TFP-32DAR)
HM62256ALR-8SL	85 ns	
HM62256ALR-10SL	100 ns	
HM62256ALR-12SL	120 ns	
HM62256ALR-15SL	150 ns	

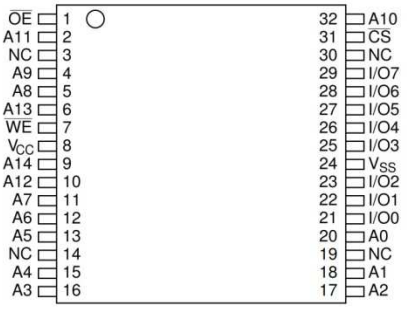
Pin Arrangement

HM62256AP/AFP/ASP Series



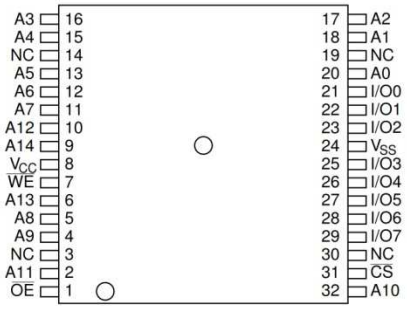
(Top view)

HM62256AT Series



(Top view)

HM62256AR Series

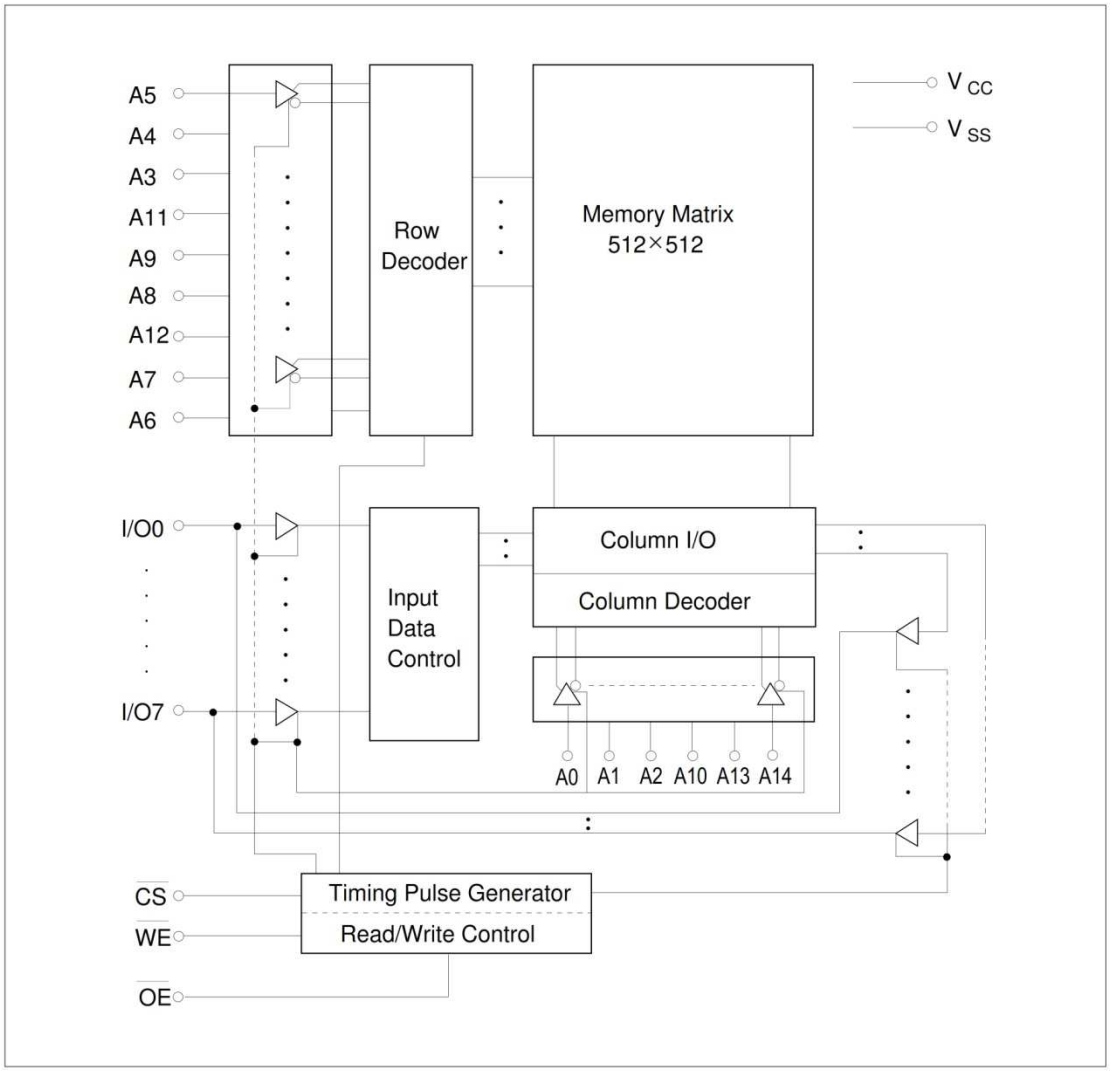


(Top view)

Pin Description

Symbol	Function	Symbol	Function
A0 – A14	Address	$\overline{OE}$	Output enable
I/O0 – I/O7	Input/output	NC	No connection
$\overline{CS}$	Chip select	V_{CC}	Power supply
$\overline{WE}$	Write enable	V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5[*1] to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. V_T min = –3.0 V for pulse half-width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5[*1]	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC}	—	6	15	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} Iout = 0 mA
HM62256A-8	I_{CC1}	—	33	50	mA	min cycle, duty = 100%, $I_{I/O}$ = 0 mA
HM62256A-10		—	30	50		$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}
HM62256A-12		—	27	45		
HM62256A-15		—	24	40		
	I_{CC2}	—	5	15	mA	Cycle time = 1µs, $I_{I/O}$ = 0 mA $\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0
Standby V_{CC} current	I_{SB}	—	0.3	2	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	0.01	1	mA	Vin ≥ 0 V $\overline{CS}$ ≥ V_{CC} – 0.2 V
		—	0.3*2	100*2	µA	
		—	0.3*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$= 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

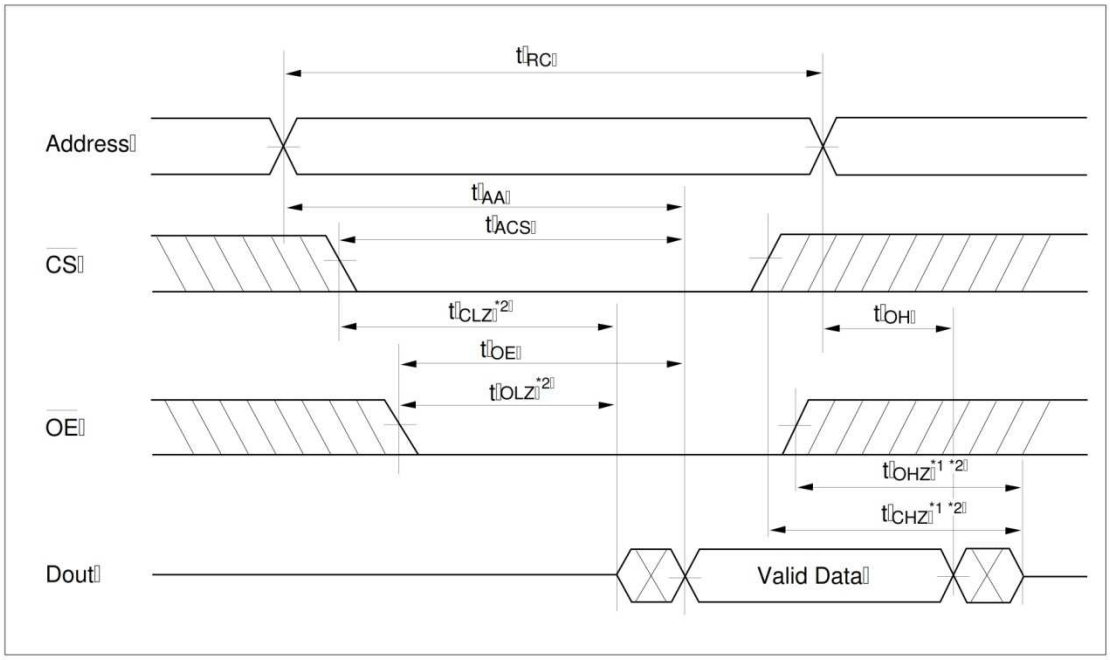
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing refernce levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

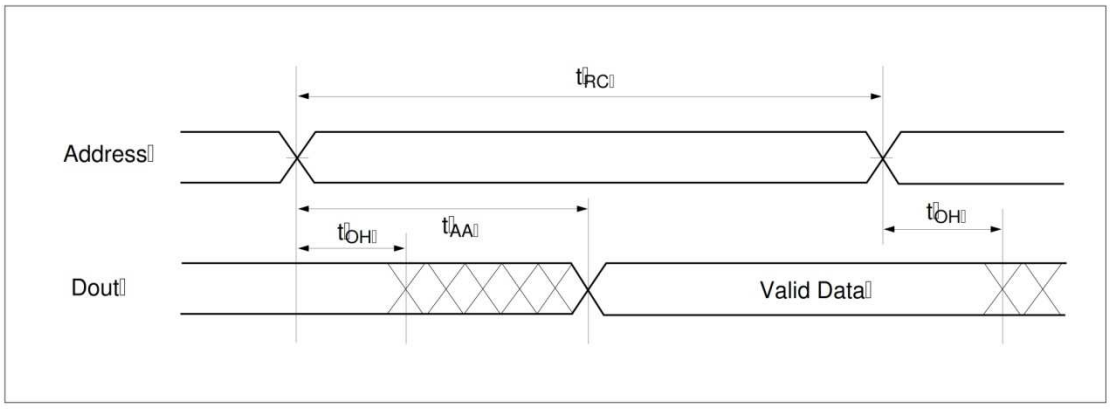
Read Cycle

		HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	85	—	100	—	120	—	150	—	ns	
Address access time	t_{AA}	—	85	—	100	—	120	—	150	ns	
Chip select access time	t_{ACS}	—	85	—	100	—	120	—	150	ns	
Output enable to output valid	t_{OE}	—	45	—	50	—	60	—	70	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns	

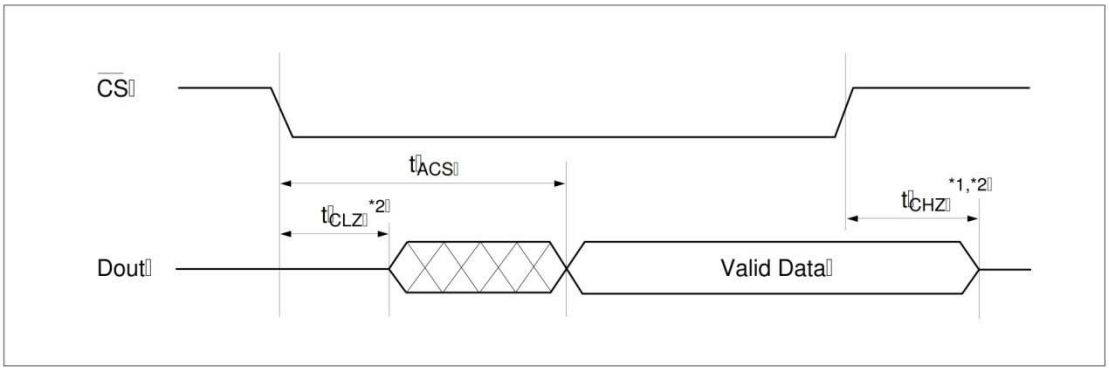
Read Timing Waveform (1) *3



Read Timing Waveform (2) *3 *4 *6



Read Timing Waveform (3) *3 *5 *6

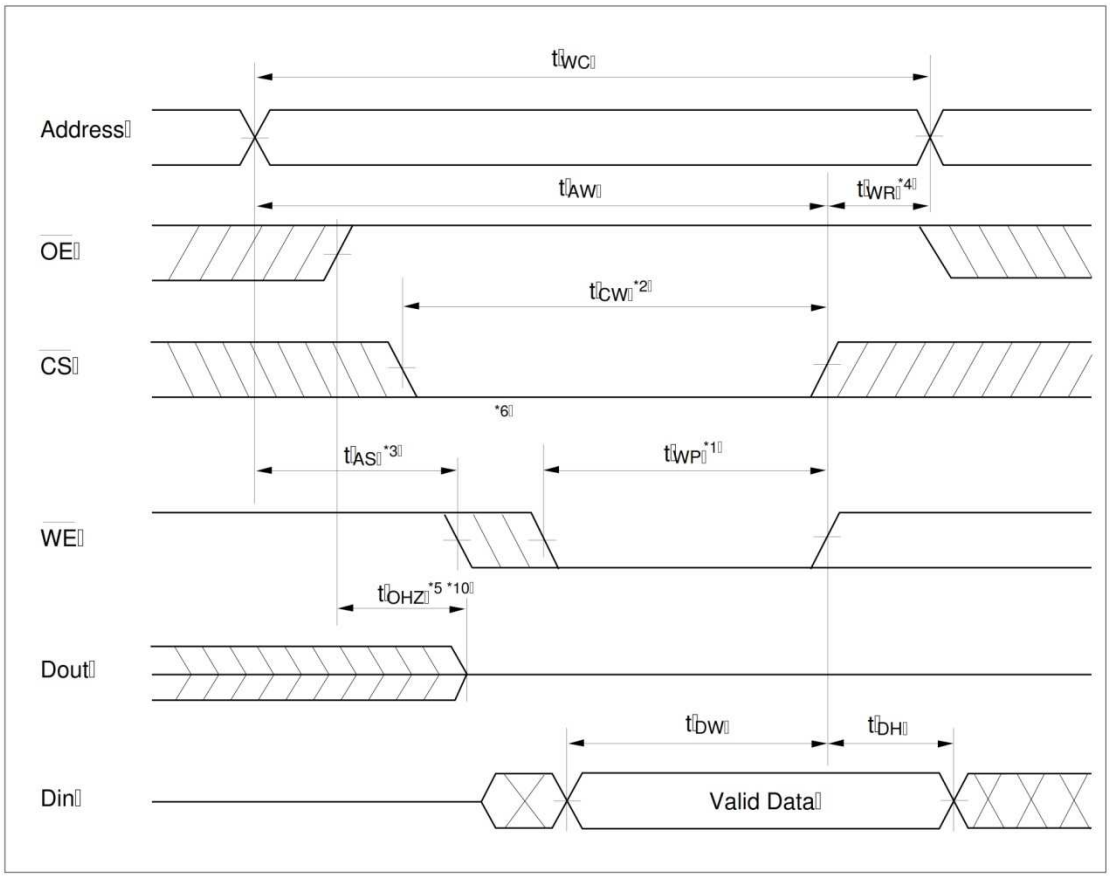


Notes:
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
6. $\overline{OE} = V_{IL}$.

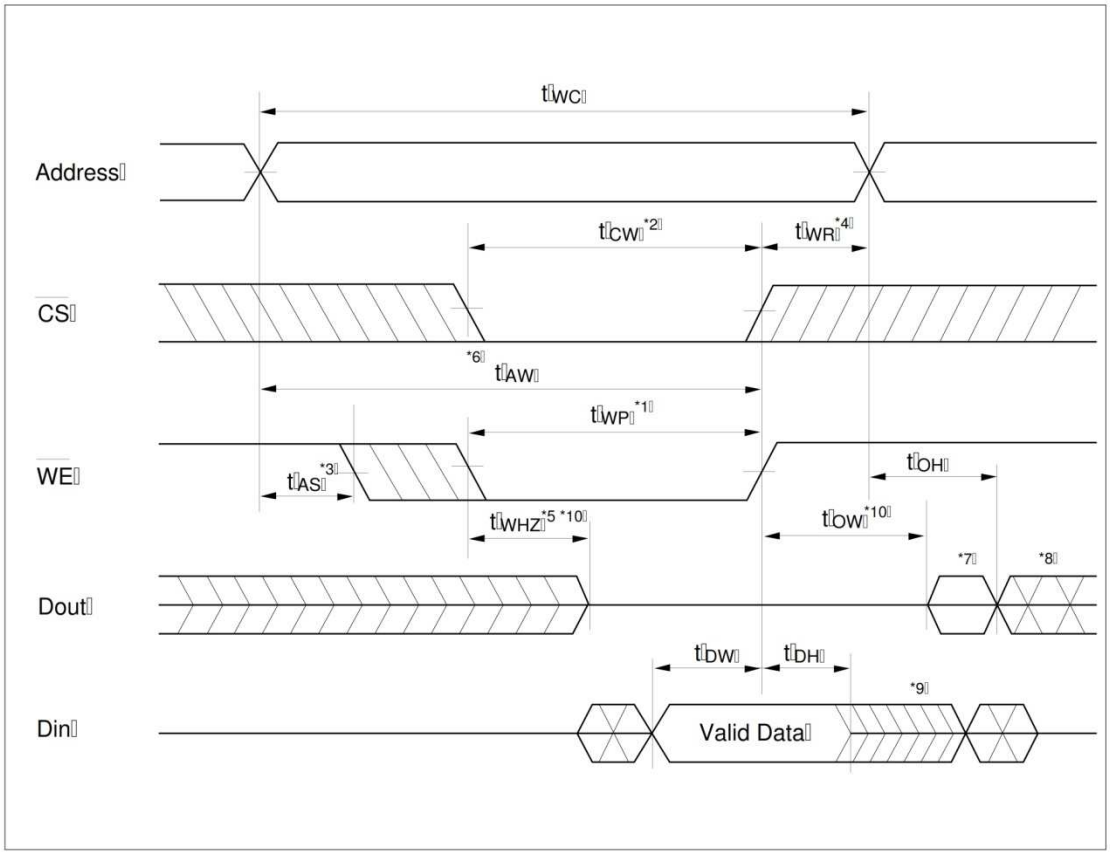
Write Cycle

		HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns	2
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns	
Write pulse width	t_{WP}	55	—	60	—	70	—	90	—	ns	1
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns	4
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	10, 11

Write Timing Waveform (1) (OE Clock)



Write Timing Waveform (2) (OE Low Fixed)



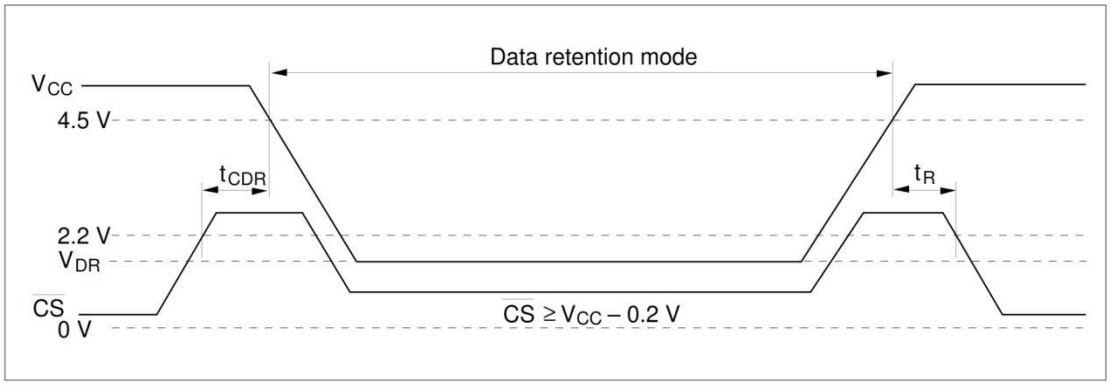
Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. Dout is the same phase of the write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	0.2	30*2	µA	V_{CC} = 3.0 V, Vin ≥ 0 V
		—	0.2	10*3	µA	$\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*4	—	—	ns	

Low V_{CC} Data Retention Timing Waveform



Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. 20 µA max at Ta = 0 to +40°C. (only for L-version)
3. 3 µA max at Ta = 0 to +40°C. (only for L-SL version)
4. t_{RC} = read cycle time.
5. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

A.2.2 NM26C32B EPROM

FAIRCHILD SEMICONDUCTOR™

January 1999

NMC27C32B
32,768-Bit (4096 x 8) CMOS EPROM

General Description

The NMC27C32B is a 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance.

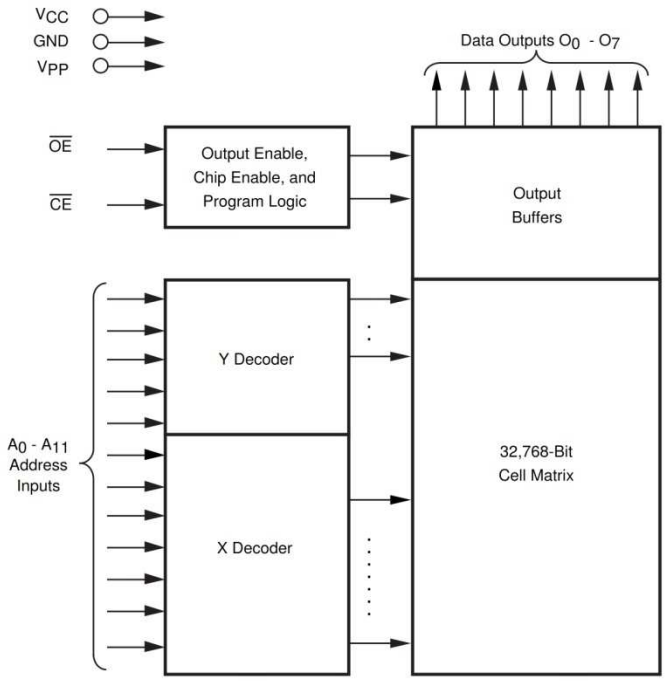
The NMC27C32B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  - — Active Power: 55 mW Max
  - — Standby Power: 0.55 mW Max
- Industrial temperature range, -40°C to +85°C
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE ® output
- Manufacturer's identification code for automatic programming
- High current CMOS level output drivers
- Compatible with NMOS 2732

Block Diagram

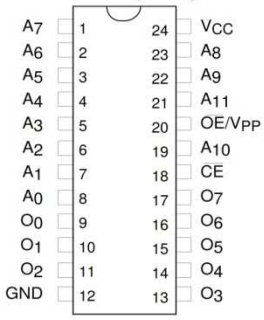


DS008827-1

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32B
Dual-in-line-package



27C16 2716	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	PGM	PGM	A_{14}
V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
OE	OE	OE	OE
A_{10}	A_{10}	A_{10}	A_{10}
CE	CE	CE	CE
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pin.

DS008827-2

Order Number NMC27C32BQ See Package Number J24AQ

Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O0 –O7	Outputs
V_{CC}	Power Supply
GND	Ground

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ150	150
NMC27C32BQ200	200

Industrial Temp Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} +1.0V to GND-0.6V
$\overline{OE}/V_{PP}$ Supply and A9 Voltage with Respect to Ground	+14.0V to -0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	
NMC27C32BQ150, 200	0°C to +70°C
NMC27C32BQE 200	-40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	µA
I_{PP}	$\overline{OE}/V_{PP}$ Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	µA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f=5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = -10 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B				Units
			Q150		Q200, QE200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE}$ = V	0		0		ns

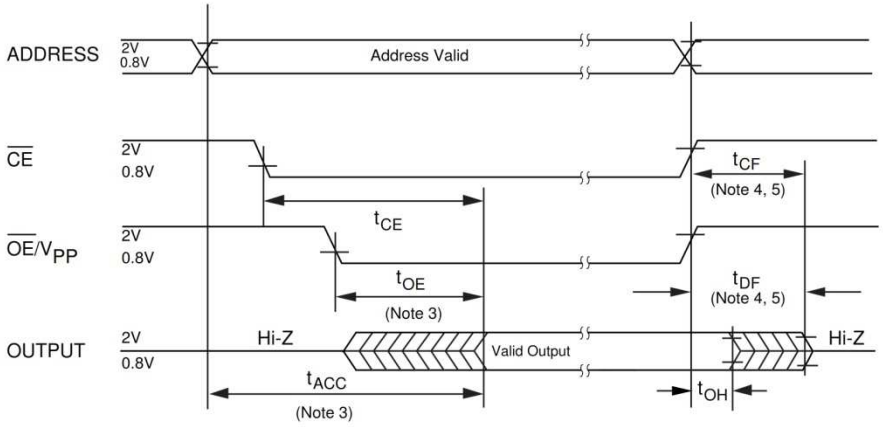
Capacitance (Note 2) T_A = +25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	V_{IN} = 0V	6	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	16	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7)



DS008827-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to -2.0V for 20 ns Max, except for $\overline{OE}/V_{PP}$ which cannot exceed -0.2V.

Note 10: Typical values are for T_A = 25°C and nominal supply voltages.

A.2.3 DS8640 Unibus Receiver

National Semiconductor

February 1996

DS7640/DS8640 Quad NOR Unified Bus Receiver

General Description

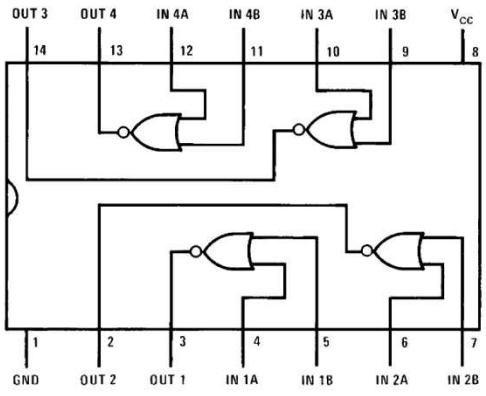
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (30 μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

Connection Diagram

Dual-In-Line Package



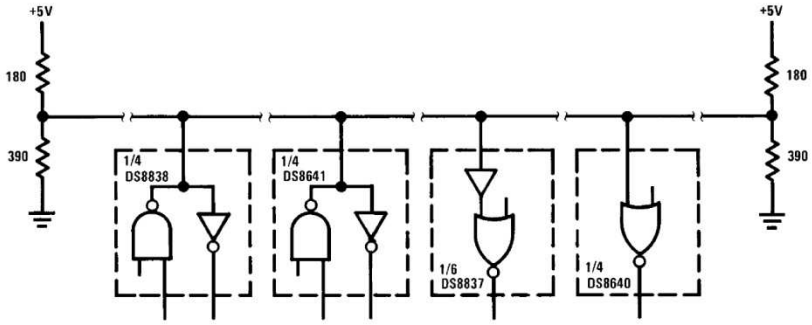
TL/F/5805–1

Top View

Order Number DS7640J or DS8640N
See NS Package Number J14A or N14A

Typical Application

120Ω Unified Data Bus



TL/F/5805–2

 TL/F/5805 RRD-B30M36/Printed in U. S. A. http://www.national.com

DS7640/DS8640 Quad NOR Unified Bus Receiver

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	μA
			$V_{CC} = 0V$		1.0	50	μA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	μA
V_{OH}	Output Voltage	$I_{OH} = -400\ \mu A$, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply to $V_{CC} = 5V$, $T_A = 25°C$.

A.2.4 DS8641 Unibus Transceiver

National Semiconductor

January 1996

DS8641
Quad Unified Bus Transceiver

General Description

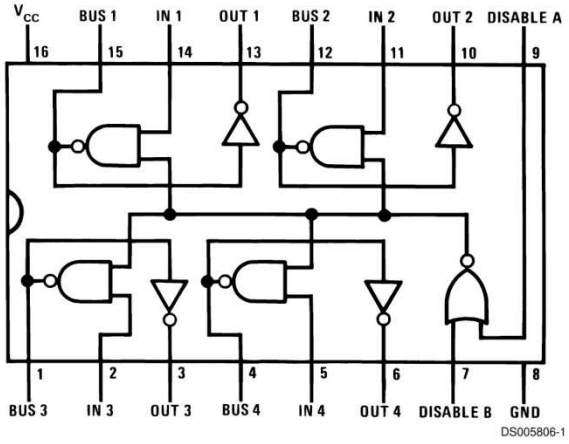
The DS8641 is a quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30 µA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

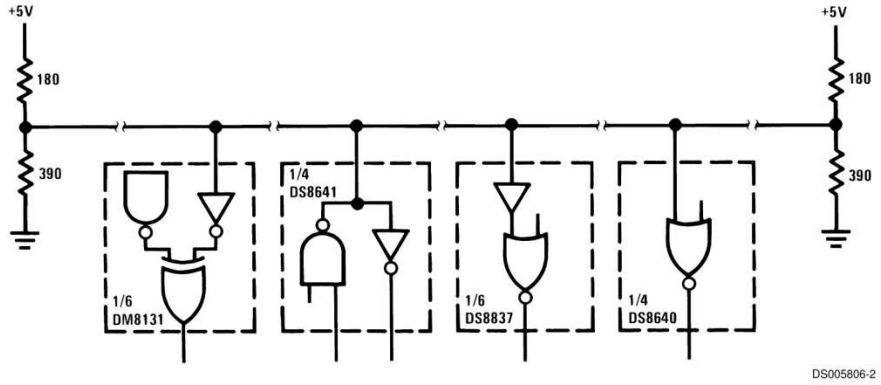
Connection Diagram

Dual-In-Line Package



Top View
Order Number DS8641N
See NS Package Number N16A

Typical Application



Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65˚C to +150˚C
Maximum Power Dissipation (Note 1) at 25˚C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260˚C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS8641	0	+70	˚C

Note 1: Derate molded package 10.9 mW/˚C above 25˚C.

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Note 3) and (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS						
V_{IH}	Logical “1” Input Voltage		2.0			V
V_{IL}	Logical “0” Input Voltage				0.8	V
I_I	Logical “1” Input Current	V_{IN} = 5.5V			1	mA
I_{IH}	Logical “1” Input Current	V_{IN} = 2.4V			40	µA
I_{IL}	Logical “0” Input Current	V_{IN} = 0.4V			−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25˚C		−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT						
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA		0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}		30	100	µA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V		2	100	µA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16 mA	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400 µA		1.50	1.30	V
RECEIVER OUTPUT						
V_{OH}	Logical “1” Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400 µA	2.4			V
V_{OL}	Logical “0” Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA		0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 5)	−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (per Package)		50	70	mA

Switching Characteristics

T_A = 25˚C, V_{CC} = 5V, unless otherwise indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD}	Propagation Delays (Note 8)	(Note 6)				
	Disable to Bus "1"			19	30	ns
	Disable to Bus "0"			15	30	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			17	25	ns
	Bus to Logical "1" Receiver Output	(Note 7)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0˚C to +70˚C range for the DS8641. All typical values are for T_A = 25˚C and V_{CC} = 5V.

Note 4: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 5: Only one output at a time should be shorted.

Note 6: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

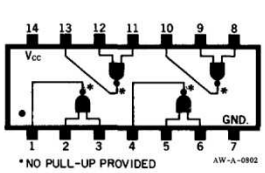
Note 8: The following apply for V_{CC} = 5V, T_A = 25˚C unless otherwise specified.

A.2.5 8881 Unibus Driver

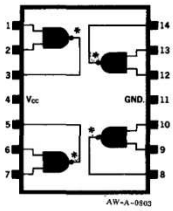
SIGNETICS DCL INTEGRATED CIRCUITS

8881 QUAD 2-INPUT NAND GATE

A F PACKAGE



J PACKAGE

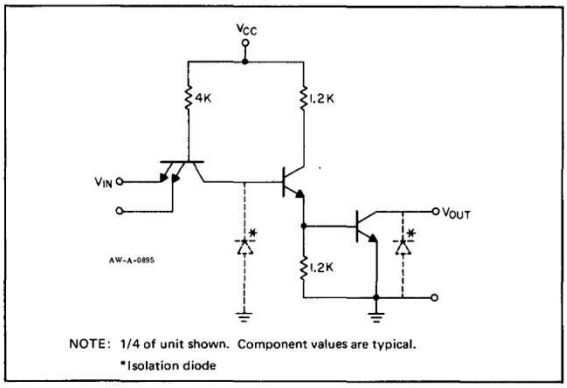


The 8881 is a Quad 2-Input NAND Gate with bare output collectors. Absence of an output pull-up structure allows the user complete freedom in the use of the 8881 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 50 outputs to be tied together.

Collector-logic, using the 8881, can provide increased system flexibility and lower system cost due to reduced can count.

Section 4 of this handbook provides detailed usage rules and collector-logic information for this element.

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8881	TEMP. N8881	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	µA	+125°C	+75°C	5.0V	0.6V			8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	2.0V	17mA	9
A-3				0.4	V	+25°C	+25°C	5.0V	2.0V	2.0V	17mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	2.0V	17mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.4V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.4V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.4V	5.25V		
A-4	"1" INPUT CURRENT			25	µA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY			20	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10,14
A-6	TURN-OFF DELAY			30	ns	+25°C	+25°C	5.0V			D.C.F.O. = 20	10,14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C.F.O. = 6	11,14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			31	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			8.9	mW	+25°C	+25°C	5.25V	0V			
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	10mA	0V		12

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Connect an external 1K ±1% resistor from V_{cc} to the output terminal for this test.
9. Output sink current is supplied through a resistor V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

A.2.6 74LS639 Bus Transceiver

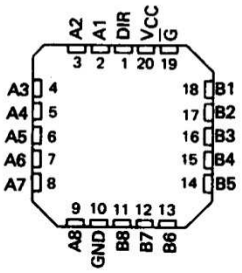
SN54LS638, SN54LS639, SN74LS638, SN74LS639
OCTAL BUS TRANSCEIVERS

D2636, JANUARY 1981—REVISED MARCH 1988

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **A Bus Outputs are Open-Collector, B Bus Outputs are 3-State**

SN54LS638, SN54LS639 . . . J PACKAGE
SN74LS638, SN74LS639 . . . DW OR N PACKAGE
(TOP VIEW)

SN54LS638, SN54LS639 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

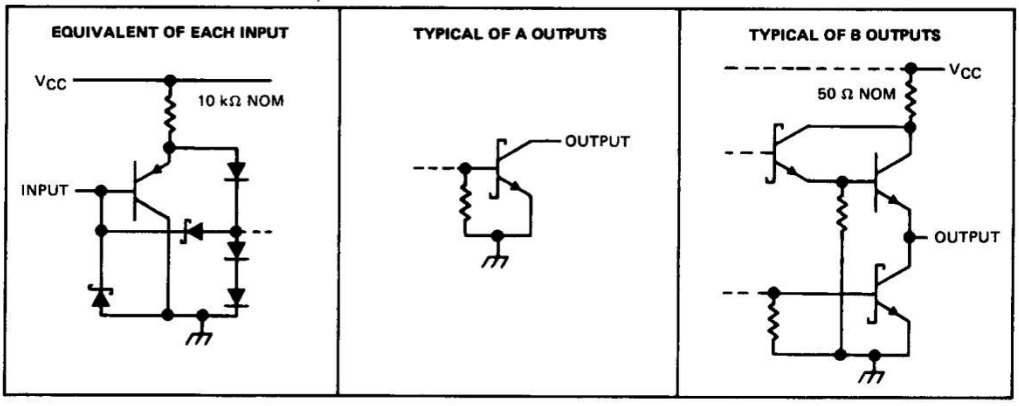
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'LS638	'LS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS638	Open-Collector	3-State	Inverting
'LS639	Open-Collector	3-State	True

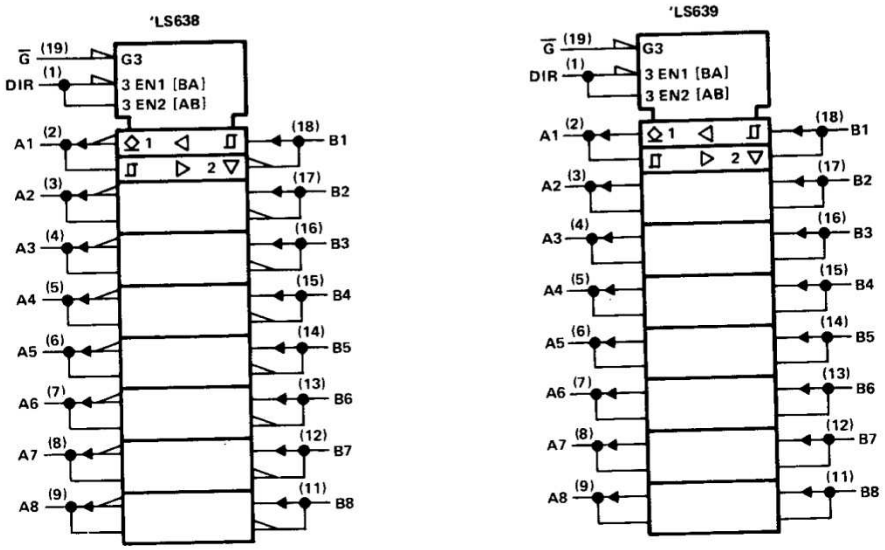
schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

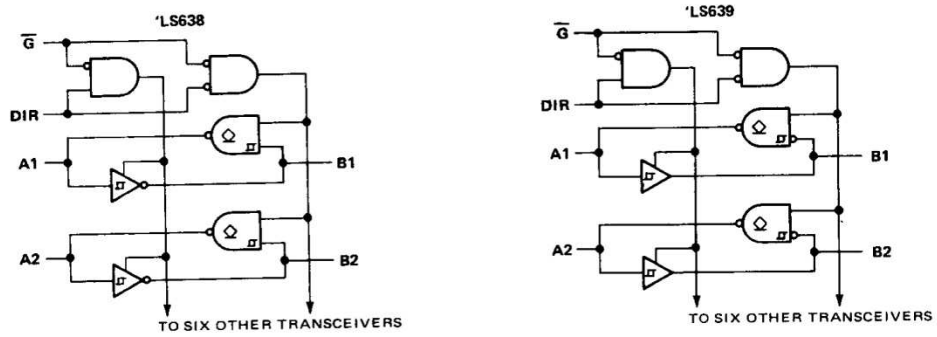
2-1063

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (DIR or $\overline{G}$)		7 V
Off-state output voltage (A or B)		5.5 V
Operating free-air temperature range:	SN54LS638, SN54LS639	−55°C to 125°C
	SN74LS638, SN74LS639	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

TEXAS INSTRUMENTS
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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH} (A bus)			5.5			5.5	V
High-level output current, I_{OH} (B bus)			−12			−15	mA
Low-level output current, I_{OL} (A or B bus)			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
	Hysteresis ($V_{T+}-V_{T-}$)		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	A	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OH}	High-level output voltage	B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −3 mA	2.4			2.4			V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	A or B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	B	V_{CC} = MAX, $\overline{G}$ at 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current low-level voltage applied	A or B	V_{CC} = MAX, $\overline{G}$ at 2 V,	V_O = 0.4 V			−0.4			−0.4	mA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	B	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, Outputs open			48	70		48	70	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, Outputs open			62	90		62	90	mA
I_{CCZ}	Supply current, outputs off		V_{CC} = MAX, Outputs open			64	95		64	95	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS638			'LS639			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B	C_L = 45 pF, R_L = 667 Ω		6	10		8	15	ns
	B	A			17	25		19	25	
t_{PHL}	A	B			8	15		11	15	ns
	B	A			14	25		16	25	
t_{PLH}	$\overline{G}$	A			26	40		23	40	ns
t_{PHL}	$\overline{G}$	A			43	60		34	50	ns
t_{PZH}	$\overline{G}$	B			23	40		26	40	ns
t_{PZL}	$\overline{G}$	B			31	40		31	40	ns
t_{PHZ}	$\overline{G}$	B	C_L = 5 pF, R_L = 667 Ω		15	25		15	25	ns
t_{PLZ}	$\overline{G}$	B			15	25		15	25	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

A.2.7 MAX693 Microprocessor Supervisory Circuit

General Description

The MAX690 family of supervisory circuits reduces the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include µP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX690 family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

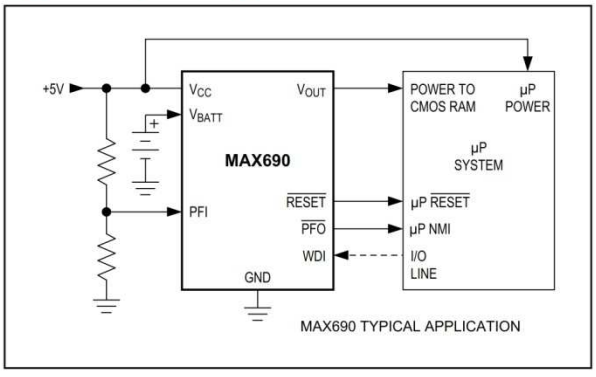
The MAX690, MAX692, and MAX694 are supplied in 8-pin packages and provide four functions:

- A reset output during power-up, power-down, and brownout conditions.
- Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
- A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
- A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MAX691, MAX693, and MAX695 are supplied in 16-pin packages and perform all MAX690, MAX692, MAX694 functions, plus:

- Write protection of CMOS RAM or EEPROM.
- Adjustable reset and watchdog timeout periods.
- Separate outputs for indicating a watchdog timeout, backup-battery switchover, and low V_{CC}.

Typical Operating Circuit



MAX690 TYPICAL APPLICATION

Benefits and Features

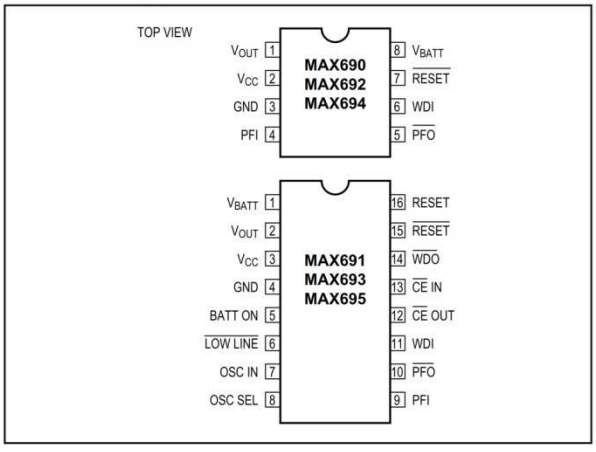
- Supervisory Function Integration Saves Board Space while Fully Protecting Microprocessor-Based Systems
  - Precision Voltage Monitor
    - 4.65V (MAX690, MAX691, MAX694, MAX695)
    - 4.40V (MAX692, MAX693)
  - Power OK/Reset Time Delay
    - 50ms, 200ms, or Adjustable
  - Watchdog Timer
    - 100ms, 1.6s, or Adjustable
  - Battery Backup Power Switching
  - Voltage Monitor for Power Fail or Low Battery Warning
  - Minimum External Component Count
- Low Power Consumption in Battery Backup Mode Extends Battery Life
  - 1µA Standby Current
- Onboard Gating of Chip Enable Signals Protects Against Erroneous Data Written to RAM During Low V_{CC} Events

Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

Ordering information appears at end of data sheet.

Pin Configurations



19-0218; Rev 5; 4/15

maxim integrated™

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6.0V
- V_{BATT} ..... -0.3V to +6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{OUT} + 0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/µs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... -40°C to +85°C
- M suffix ..... -55°C to +125°C

Power Dissipation
- 8-Pin Plastic DIP (derate 5mW/°C above +70°C) 400mV
- 8-Pin CERDIP (derate 8mW/°C above +85°C) 500mV
- 16-Pin Plastic DIP (derate 7mW/°C above +70°C) 600mV
- 16-Pin Small Outline (derate 7mW/°C above +70°C) 600mV
- 16-Pin CERDIP (derate 10mW/°C above +85°C) 600mV

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (Soldering, 10s) ..... 300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATTERY BACKUP SWITCHING						
Operating Voltage Range (V_{CC})			4.75		5.5	V
Operating Voltage Range (V_{BATT})			2.0		4.25	V
Operating Voltage Range (V_{CC})			4.5		5.5	V
Operating Voltage Range (V_{BATT})			2.0		4.0	V
V_{OUT} Output Voltage	I_{OUT} = 1mA		V_{CC} - 0.3	V_{CC} - 0.1		V
	I_{OUT} = 50mA		V_{CC} - 0.5	V_{CC} - 0.25		V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Supply Current (Excluded I_{OUT})	I_{OUT} = 1mA			2	5	mA
	I_{OUT} = 50mA			3.5	10	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V			0.6	1	µA
Battery Standby Current (+ = Discharge, - = Charge)	5.5V > V_{CC} > V_{BATT} + 1V	T_A = +25°C	-0.1		+0.02	µA
		T_A = full operating range	-1.0		+0.02	µA
Battery Switchover Threshold (V_{CC} - V_{BATT})	Power-up			70		mV
	Power-down			50		mV

Electrical Characteristics (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short-Circuit Current	BATT ON = V_{OUT} = 4.5V sink current			25		mA
	BATT ON = 0V source current		0.5	1	25	µA
RESET AND WATCHDOG TIMER						
Reset Voltage Threshold	T_A = full operating range	MAX690, MAX691, MAX694, MAX695	4.5	4.65	4.75	V
		MAX692, MAX693	4.25	4.4	4.5	
Reset Threshold Hysteresis				40		mV
Reset Timeout Delay (MAX690/MAX691/ MAX692/MAX693)	Figure 6, OSC SEL HIGH, V_{CC} = 5V		35	50	70	ms
Reset Timeout Delay (MAX694/MAX695)	Figure 6, OSC SEL HIGH, V_{CC} = 5V		140	200	280	ms
Watchdog Timeout Period, Internal Oscillator	Long period, V_{CC} = 5V		1.0	1.6	2.25	s
	Short period, V_{CC} = 5V		70	100	140	ms
Watchdog Timeout Period, External Clock	Long period		3840		4097	Clock Cycles
	Short period		768		1025	
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 0.8V_{CC}		200			ns
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage	I_{SINK} = 1.6mA, V_{CC} = 4.25V				0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V		3.5			
RESET and $\overline{WDO}$ Output Voltage	I_{SINK} = 1.6mA				0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V		3.5			
Output Short-Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$		1	3	25	µA
WDI Input Threshold Logic-Low	V_{CC} = 5V (Note 2)				0.8	V
WDI Input Threshold Logic-High	V_{CC} = 5V (Note 2)		3.5			
WDI Input Current	WDI = V_{OUT}			20	50	µA
	WDI = 0V		-50	-15		
POWER-FAIL DETECTOR						
PFI Threshold	V_{CC} = 5V, T_A = full		1.2	1.3	1.4	V
PFI Current				±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA				0.4	V
	I_{SOURCE} = 1µA		3.5			V
$\overline{PFO}$ Short Circuit Source Current	PFI = V_{IH}, $\overline{PFO}$ = 0V		1	3	25	µA

Electrical Characteristics (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP ENABLE GATING					
$\overline{CE}$ IN Thresholds	V_{IL}			0.8	V
	V_{IH}	3.0			
$\overline{CE}$ IN Pullup Current			3		µA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 3.0mA	V_{OUT} - 1.5			
	I_{SOURCE} = 1µA, V_{CC} = 0V	V_{OUT} - 0.05			
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		50	200	ns
OSCILLATOR					
OSC IN Input Current			±2		µA
OSC SEL Input Pullup Current			5		µA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125kΩ.

Pin Description

PIN		NAME	FUNCTION
MAX690/ MAX692/ MAX694	MAX691/ MAX693/ MAX695		
2	3	V_{CC}	The +5V Input
8	1	V_{BATT}	Backup Battery Input. Connect to Ground if a backup battery is not used.
1	2	V_{OUT}	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used. Connect a 0.1µF or larger bypass capacitor to V_{OUT}.
3	4	GND	0V Ground Reference for All Signals
7	15	$\overline{RESET}$	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MAX690/691/694/695, and 4.4V for the MAX692 and MAX693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V, (except 200ms in MAX694/695). $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
6	11	WDI	Watchdog Input (WDI). WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer input.
4	9	PFI	Noninverting Input to the Power-Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX690/ MAX692/ MAX694	MAX691/ MAX693/ MAX695		
5	10	$\overline{PFO}$	Output of the Power-Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
—	13	$\overline{CE}$ IN	$\overline{CE}$ Gating Circuit Input. Connect to GND or V_{OUT} if not used.
—	12	$\overline{CE}$ OUT	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MAX691 and MAX695, 4.4V for MAX693). See Figure 6.
—	5	BATT ON	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 25mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
—	6	$\overline{LOW\ LINE}$	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
—	16	RESET	Active-High Output. It is the inverse of $\overline{RESET}$.
—	8	OSC SEL	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3µA internal pullup. See Table 1.
—	7	OSC IN	When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting and external oscillator to this pin. See Figure 8. When OSC SEL is high or floating, OSC IN selects between fast and slow Watchdog timeout periods.
—	14	$\overline{WDO}$	The Watchdog Output ($\overline{WDO}$). $\overline{WDO}$ goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

Typical Applications

MAX691, MAX693, and MAX695

A typical connection for the MAX691/693/695 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 25mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1µA maximum when V_{CC} is between 0V and V_{BATT}–700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's Reset line low when V_{CC} is below 4.65V (4.4V for MAX693). An internal monostable holds $\overline{RESET}$ low for 50ms* after V_{CC} rises above 4.65V (4.4V for MAX693). This prevents repeated toggling of $\overline{RESET}$ even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{RESET}$ must be held low until the microprocessor clock oscillator has started. The MAX690 family power-up $\overline{RESET}$ pulse lasts 50ms* to allow for this oscillator start-up time. The manual reset switch and the 0.1µF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

*200ms for MAX695

Power-Fail Detector

The MAX691/93/95 issues a nonmaskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the power-fail input (PFI). When the voltage at PFI falls below 1.3V, the power-fail output ($\overline{PFO}$) drives the processor's NMI input low. If a power-fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} fails from 4.8V to 4.65V to save data into RAM. An earlier power-fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MAX691/MAX693/MAX695 $\overline{CE}$ OUT line drives the Chip Select inputs of the CMOS RAM. $\overline{CE}$ OUT follows $\overline{CE}$ IN as long as V_{CC} is above the 4.65V (4.4V for MAX693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{CE}$ OUT goes high, independent of the logic level at $\overline{CE}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The $\overline{LOW\ LINE}$ output goes low when V_{CC} falls below 4.65V (4.4V for MAX693).

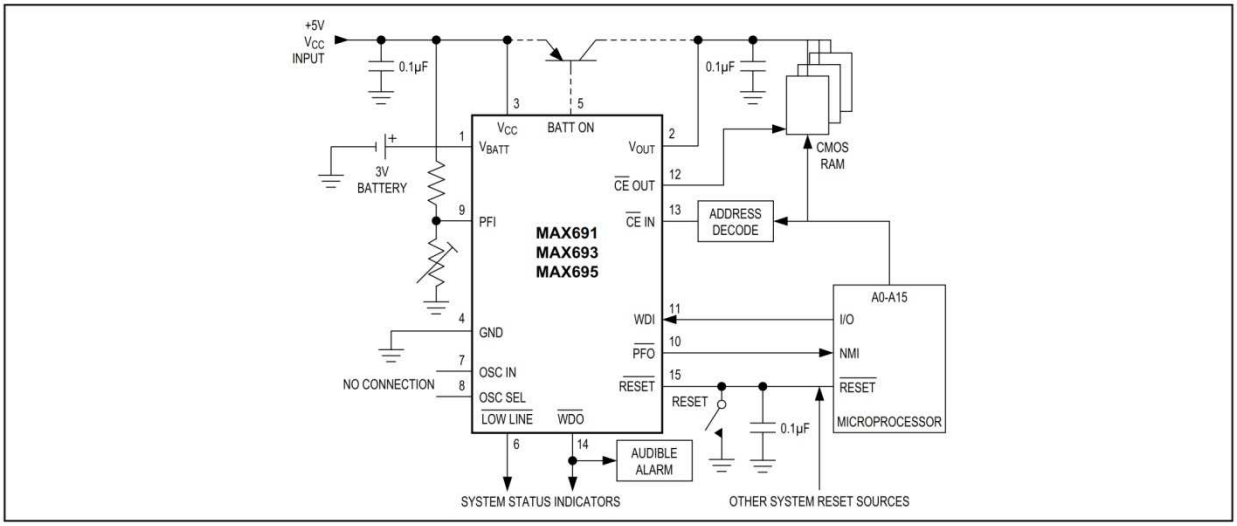


Figure 1. MAX691/693/695 Typical Application

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6s to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled the MAX691/MAX693 will issue a 50ms* $\overline{\text{RESET}}$ pulse after 1.6s. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6s until the WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MAX690, MAX692, and MAX694

The 8 pin MAX690, MAX692, and MAX694 have most of the features of the MAX691, MAX693, and MAX695. Figure 2 shows the MAX690/MAX692/MAX694 in a typical application. Operation is much the same as with the MAX691/MAX693/MAX695 (Figure 1), but in this case, the power- fail input (PFI) monitors the unregulated input to the 7805 regulator. The MAX690/MAX694 $\overline{\text{RESET}}$ output goes low when V_{CC} falls below 4.65V. The $\overline{\text{RESET}}$ output of the MAX692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 50mA. The MAX690/MAX692/MAX694 does not have a BATT ON output to drive an external transistor. The MAX690/MAX692/MAX694 also does not include chip enable gating circuitry that is available on the MAX690/MAX692/MAX694. In many systems though, $\overline{\text{CE}}$ gating is not needed since a low input to the microprocessor $\overline{\text{RESET}}$ line prevents the processor from writing to RAM during power-up and power-down transients.

The MAX690/MAX692/MAX694 watchdog timer has a fixed 1.6s timeout period. If WDI remains either low or high for more than 1.6s, a $\overline{\text{RESET}}$ pulse is sent to the microprocessor. The watchdog timer is disabled if WDI is left unconnected.

**200ms for MAX695*

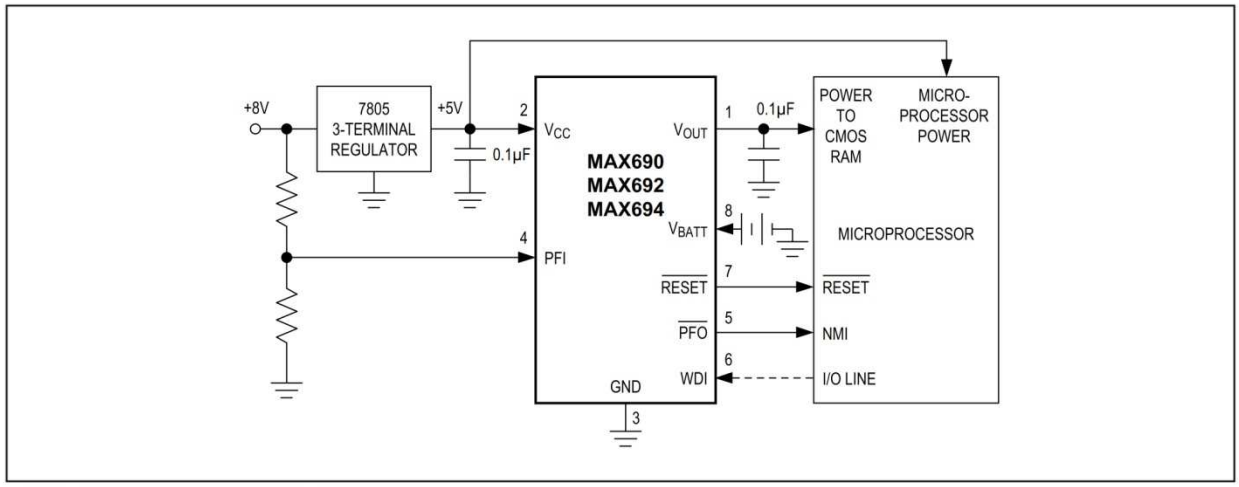


Figure 2. MAX690/692/694 Typical Application

Detailed Description

Battery-Switchover and V_{OUT}

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MAX691/MAX693/MAX695 only) can directly drive the base of the external transistor.

It should be noted that the MAX690–MAX695 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} - 700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX690/MAX691/MAX694/MAX695 operate with battery voltages from 2.0V to 4.25V while MAX692/MAX693 operate with battery voltages from 2.0V to 4.0V. High value capacitors can also be used for short-term memory backup. External circuitry is required to ensure that the capacitor voltage does not rise above the reset threshold, and that the charging resistor does not discharge the capacitor when in backup mode. The MAX691A and the MAX791 provide solutions requiring fewer external components.

A small charging current of typically 10nA (0.1µA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

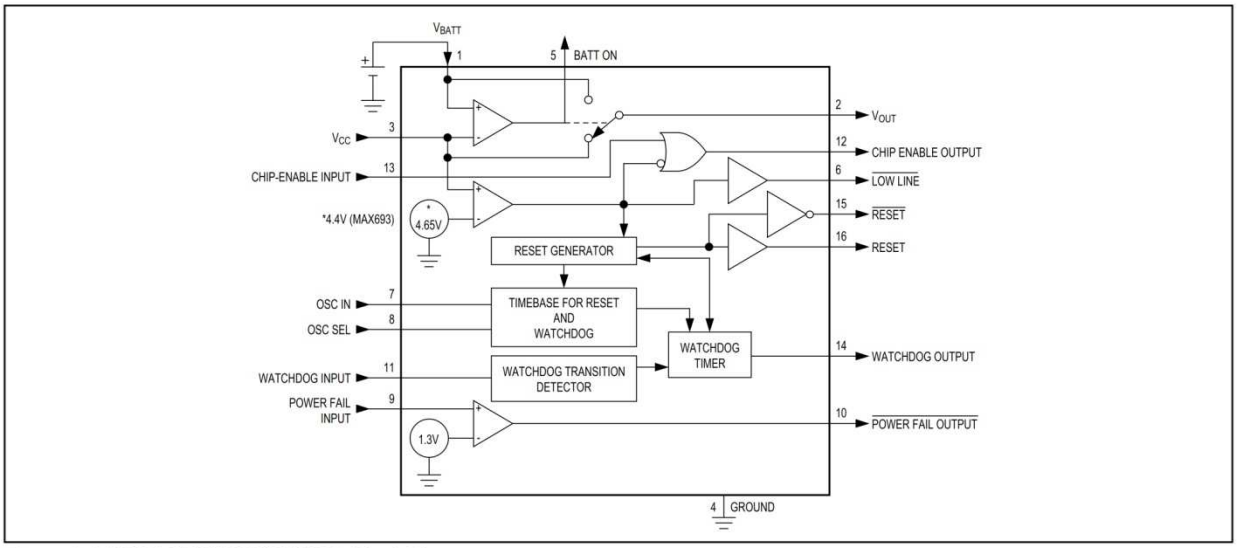


Figure 3. MAX691/MAX693/MAX695 Block Diagram

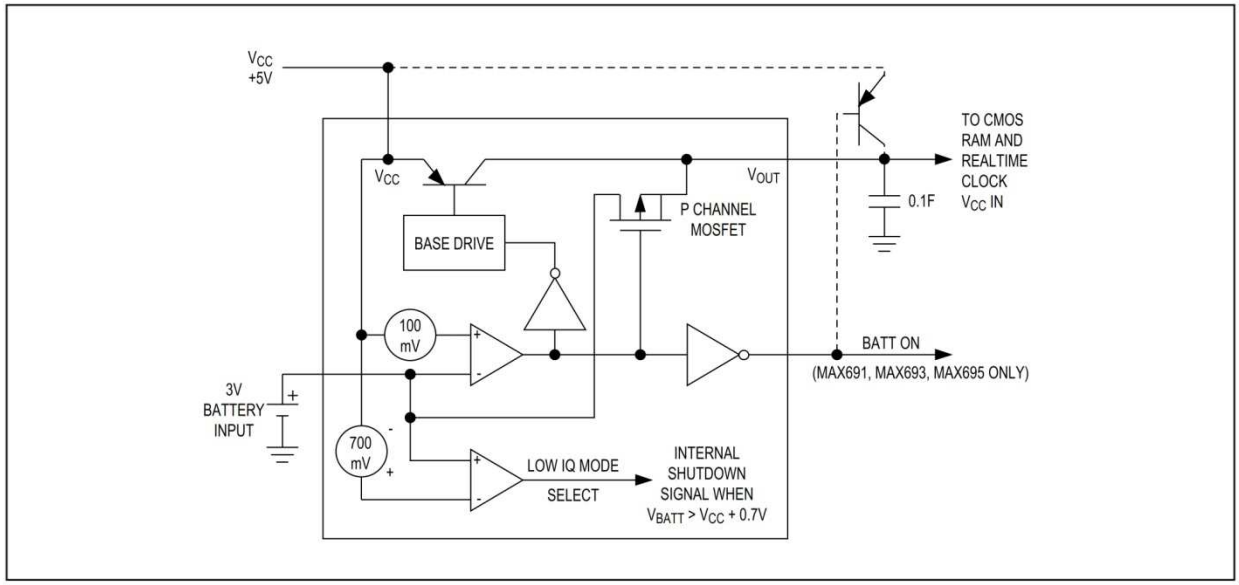


Figure 4. Battery-Switchover Block Diagram

Reset Output

$\overline{\text{RESET}}$ is an active-low output which goes low whenever V_{CC} falls below 4.5V (MAX690/MAX691/MAX694/MAX695) or 4.25V (MAX692/MAX693). It will remain low until V_{CC} rises above 4.75V (MAX690/691/694/695) or 4.5V (MAX692/MAX693) for milliseconds*. See Figures 5 and 6.

The guaranteed minimum and maximum thresholds of MAX690/MAX691/MAX694/MAX695 are 4.5V and 4.75V, while the guaranteed thresholds of the MAX692/MAX693 are 4.25V and 4.5V. The MAX690/MAX691/MAX694/MAX695 is compatible with 5V supplies with a +10%, -5% tolerance while the MAX692/MAX693 is compatible with 5V ±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MAX690/MAX691/MAX694/MAX695, and 4.4V in the MAX692/MAX693.

The response time of the reset voltage comparator is about 100µs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{\text{RESET}}$ output.

$\overline{\text{RESET}}$ also goes low if the watchdog timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{RESET}}$ has an internal 3µA pullup, and can either connect to and open collector Reset bus or directly drive a CMOS gate without and external pullup resistor.

**200ms for MAX694 and MAX695*

$\overline{\text{CE}}$ Gating and RAM Write Protection

The MAX691/MAX693/MAX695 use two pins to control the $\overline{\text{Chip Enable}}$ or $\overline{\text{Write}}$ inputs of CMOS RAMs. When V_{CC} is +5V, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces $\overline{\text{CE}}$ OUT high, independent of $\overline{\text{CE}}$ IN. The MAX693 $\overline{\text{CE}}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{\text{CE}}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{\text{CE}}$ OUT typically drives the $\overline{\text{CE}}$, $\overline{\text{CS}}$, or $\overline{\text{Write}}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at and invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{\text{CE}}$ OUT to drive the $\overline{\text{Store}}$ or $\overline{\text{Write}}$ inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{\text{CE}}$ OUT is too long, connect $\overline{\text{CE}}$ IN to GND and use the resulting $\overline{\text{CE}}$ OUT to control a high speed external logic gate. A second alternative is to AND the $\overline{\text{LOW LINE}}$ output with the $\overline{\text{CE}}$ or $\overline{\text{WR}}$ signal. An external logic gate and the $\overline{\text{RESET}}$ output of the MAX690/MAX692/MAX694 can also be used for CMOS RAM write protection.

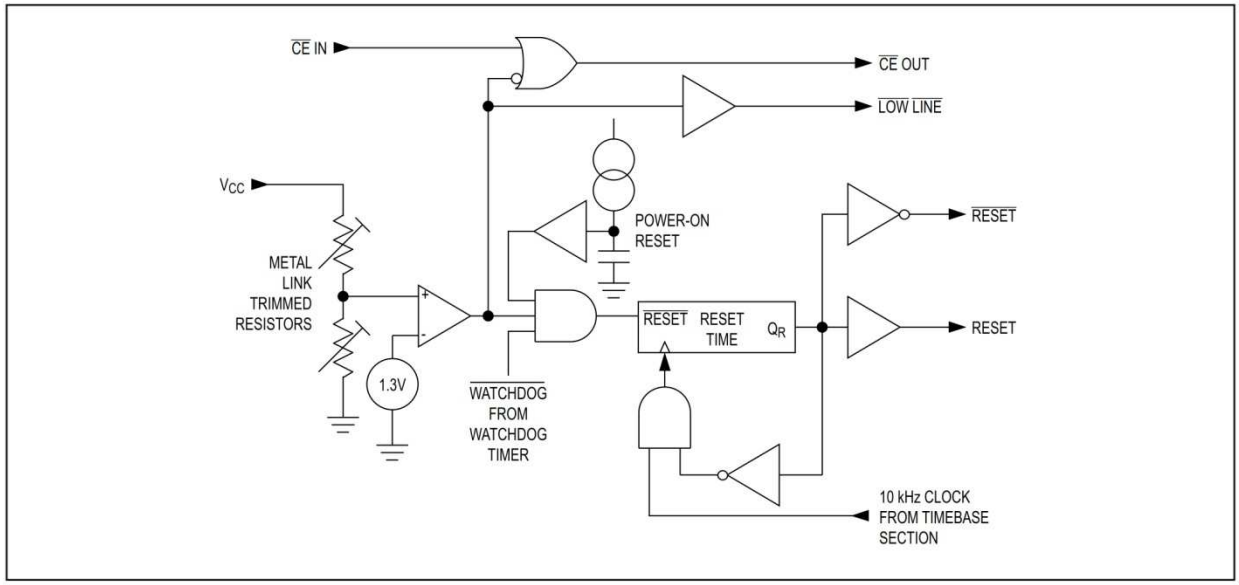


Figure 5. Reset Block Diagram

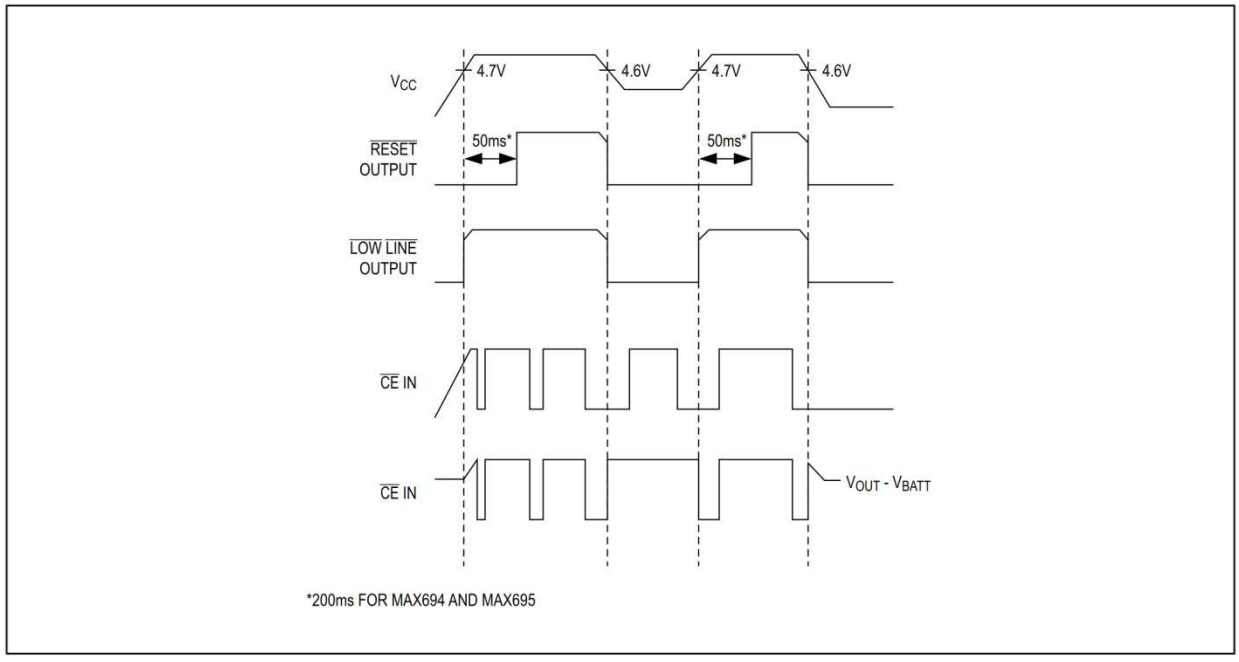


Figure 6. Reset Timing

1.3V Comparator and Power-Fail Warning

The power-fail input (PFI) is compared to an internal 1.3V reference. The power-fail output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3V. Typically, PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the +5V supply falls below 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the $\overline{RESET}$ output goes low (4.5V for MAX692/MAX693).

The power-fail detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced when V_{CC} is lower than V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50ms* $\overline{RESET}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX691/MAX693/MAX695 has a longer timeout period after reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{RESET}$ has gone high. The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6s. The watchdog monitor can be deactivated by floating the watchdog input (WDI).

The watchdog output ($\overline{WDO}$, MAX691/MAX693/MAX695 only) goes low if the watchdog timer times out and remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6s and the reset pulse width is fixed at 50ms* on the 8-pin MAX690/MAX692/MAX694. The MAX691/MAX693/MAX695 allow these times to be adjusted per Table 1. Figures 8 shows various oscillator configurations.

The internal oscillator is enabled when OSC SEL is floating. In this mode, OSC IN selects between the 1.6s and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period 1.6s. This gives the microprocessors time to reintialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

**200ms for MAX694*

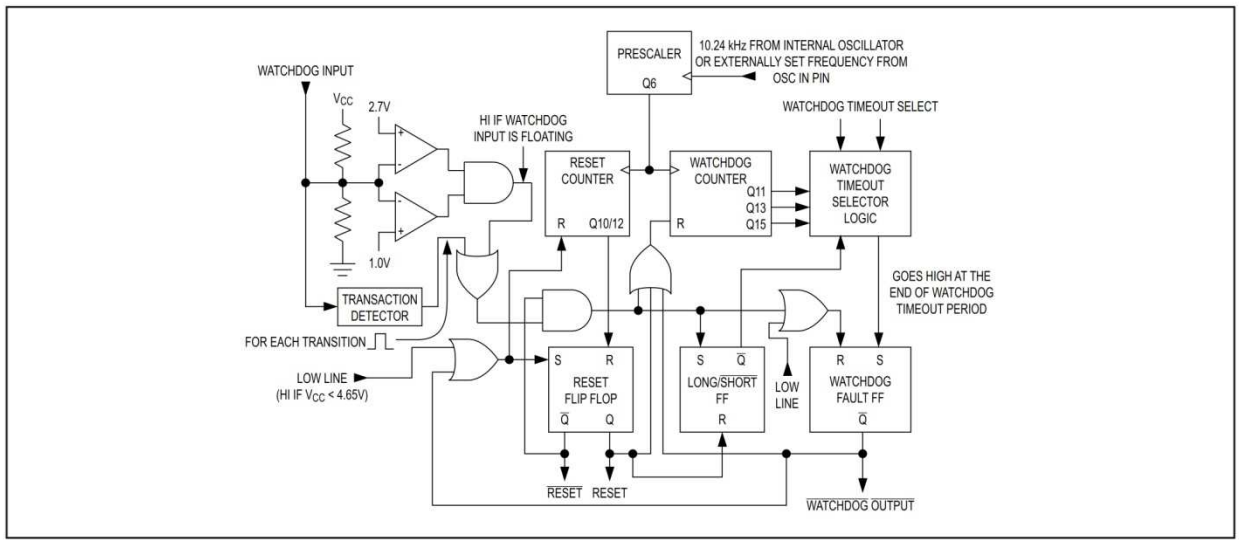


Figure 7. Watchdog Timer Block Diagram

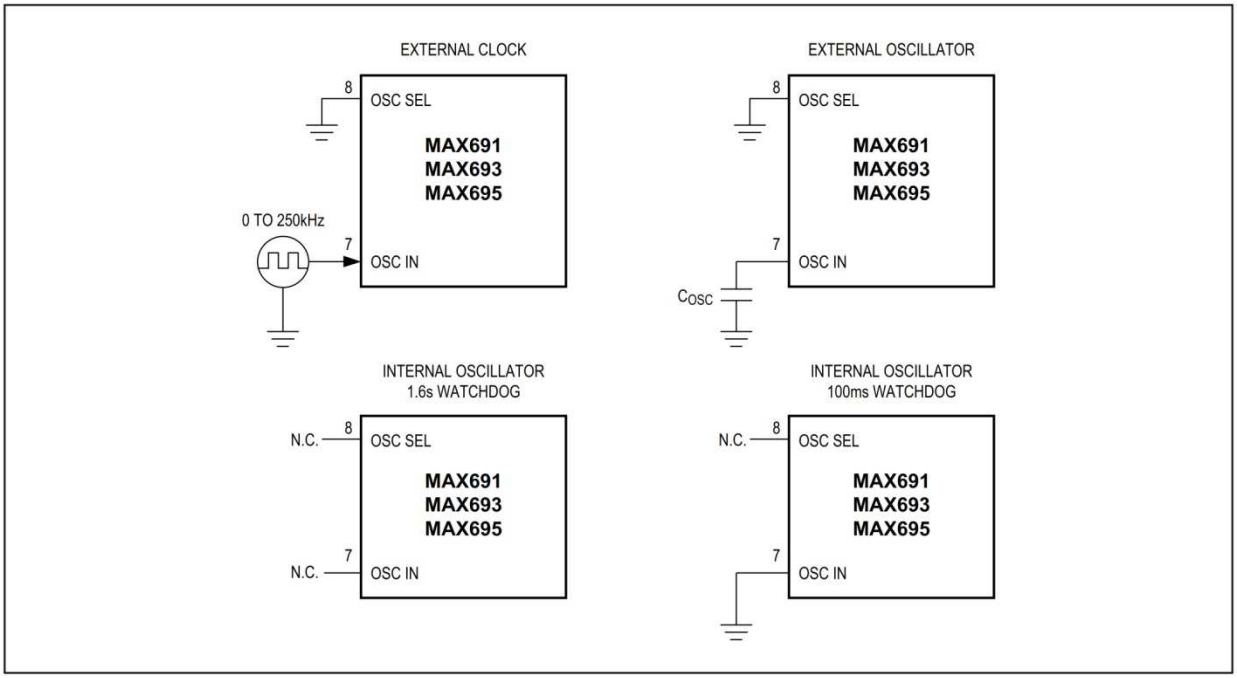


Figure 8. Oscillator Circuits

Table 1. MAX691/MAX693/MAX695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	WATCHDOG TIMEOUT PERIOD		RESET TIMEOUT PERIOD	
		NORMAL	IMMEDIATELY AFTER REST	MAX691/MAX693	MAX695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor	400ms/47pF x C	1.6s/47pF x C	200ms/47pF x C	800ms/47pF x C
Floating	Low	100ms	1.6s	50ms	200ms
Floating	Floating	1.6s	1.6s	50ms	200ms

Note 1: The MAX690/MAX692/MAX694 watchdog timeout period is fixed at 1.6s nominal, the MAX690/692 reset pulse width is fixed at 50ms nominal and the MAX694 is 200ms nominal.

Note 2: When the MAX691 OSC SEL pin is low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 6.55kHz. The nominal oscillator frequency with capacitor is:

$$f_{OSC}(Hz) = \frac{120{,}000}{C(pF)}$$

Note 3: See *Electrical Characteristics* table for minimum and maximum timing values.

Application Hints

Other Uses of the Power-Fail Detector

In Figure 9, the power-fail detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the power-fail detector is not as accurate as the onboard reset-voltage detector, a trimpot must be used to adjust the voltage detection threshold. Both the $\overline{PFO}$ and $\overline{RESET}$ outputs have high sink current capability and only 10µA of source current drive. This allows the two outputs to be connected directly to each other in a wired OR fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is noninverting, hysteresis can be added by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 12. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a three-state buffer (Figure 13). The drawback to this circuit is that a software fault may be erroneously three-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01µF capacitor sets a watchdog timeout delay of 100s. When the control input is low the OSC SEL pin is high, selecting the internal oscillator. The 100ms or the 1.6s period is chosen, depending on which diode in Figure 14 is used.

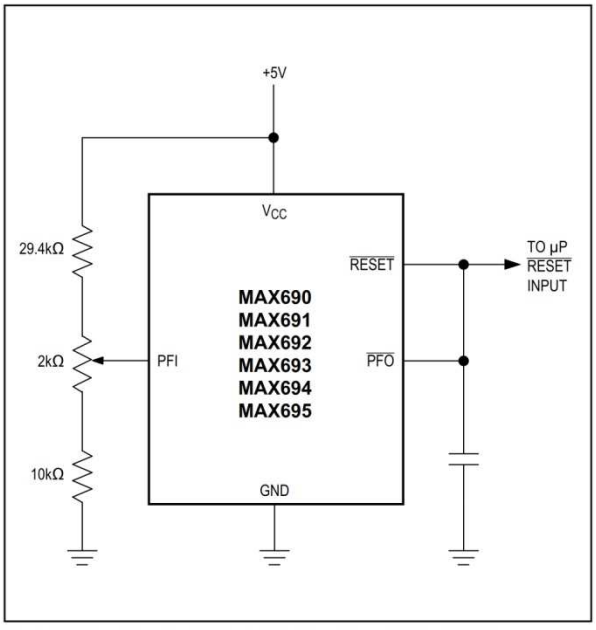


Figure 9. Externally Adjustable V_{CC} Reset Threshold

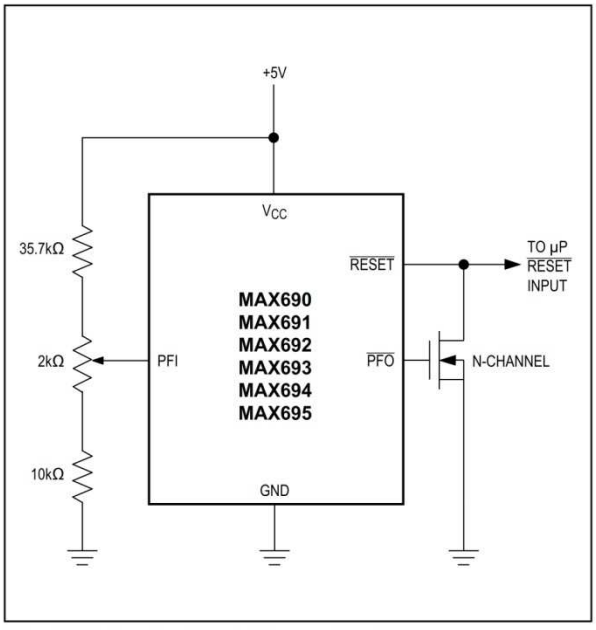


Figure 10. Reset on Overvoltage or Undervoltage

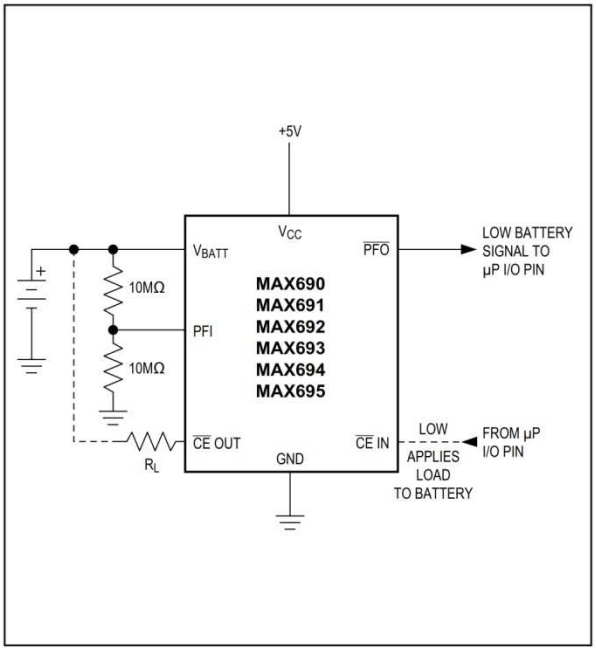


Figure 11. Backup VBattery Monitor with Optional Test Load

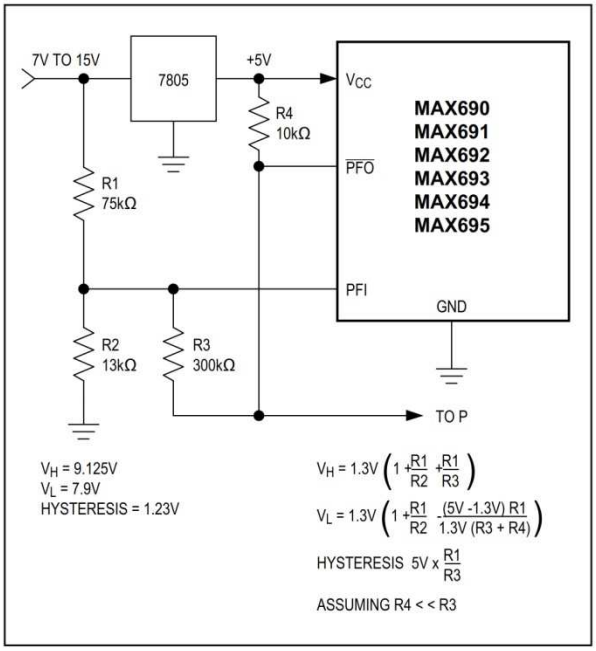


Figure 12. Adding Hysteresis to the Power-Fail Voltage Comparator

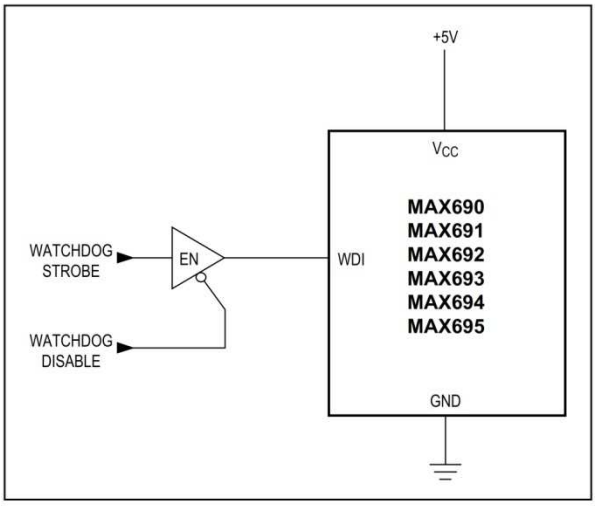


Figure 13. Disabling the Watchdog Under Program Control

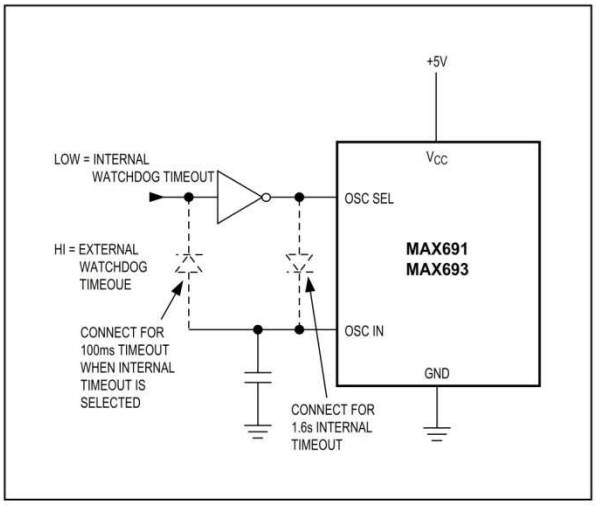


Figure 14. Selecting Internal or External Watchdog Timeout

Table 2. Input and Output Status In Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic-low
RESET	Logic-high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic-low
BATT ON	Logic-high
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect the source current.
$\overline{WDO}$	Logic-high
PFI	The power-fail comparator is turned off and the power-fail input voltage has no effect on the power-fail output.
$\overline{PFO}$	Logic-low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect the source current.
$\overline{CE}$ OUT	Logic-high
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12µA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} +100mV and V_{BATT} - 700mV. The supply current is 1µA maximum when V_{CC} is less than V_{BATT} - 700mV.

A.2.8 74LS123 Retriggerable Monostable Multivibrator

SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS043 – DECEMBER 1983 – REVISED MARCH 1988

- **D-C Triggered from Active-High or Active-Low Gated Logic Inputs**
- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **'122 and 'LS122 Have Internal Timing Resistors**

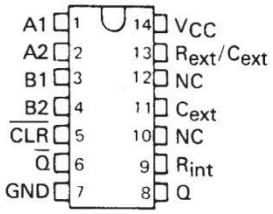
description

These d-c triggered multivibrators feature output pulse-duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122 and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

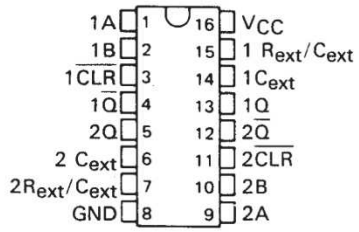
The R_{int} in nominall 10 kΩ for '122 and 'LS122.

SN54122, SN54LS122 . . . J OR W PACKAGE
SN74122 . . . N PACKAGE
SN74LS122 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

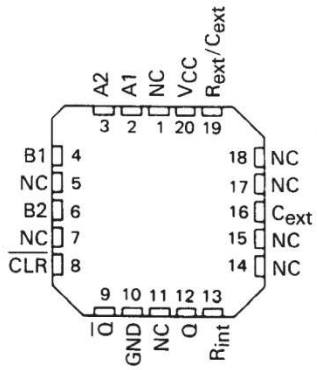


NOTES: 1. An external timing capacitor may be connected between C_{ext} and Re_{xt}/C_{ext} (positive).
2. To use the internal timing resistor of '122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse duration accuracy and repeatability, connect an external resistor between R_{ext}/Ce_{xt} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse durations, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

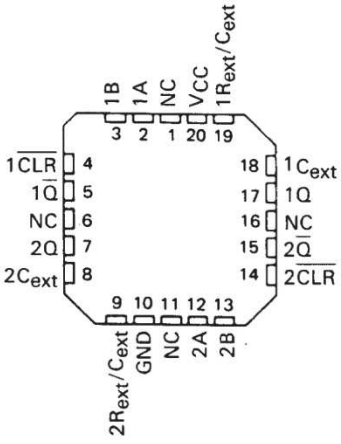
SN54123, SN54130, SN54LS123 . . . J OR W PACKAGE
SN74123, SN74130 . . . N PACKAGE
SN74LS123 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS122 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

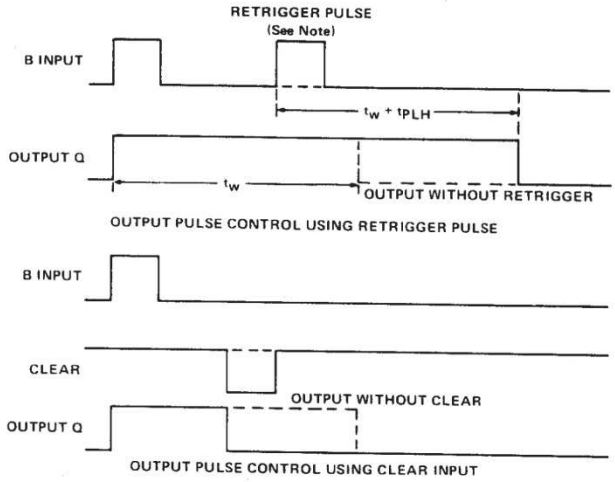


SN54LS123 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



NC - No internal connection

description (continued)



NOTE: Retrigger pulses starting before 0.22 C_{ext} (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output duration will remain unchanged.

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

'122, 'LS122
FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

'123, '130, 'LS123
FUNCTION TABLE

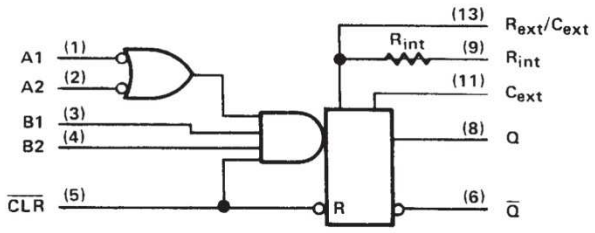
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

See explanation of function tables on page

† These lines of the functional tables assume that the indicated steady-state conditons at the A and B inputs have been set up long enough to complete any pulse started before the set up.

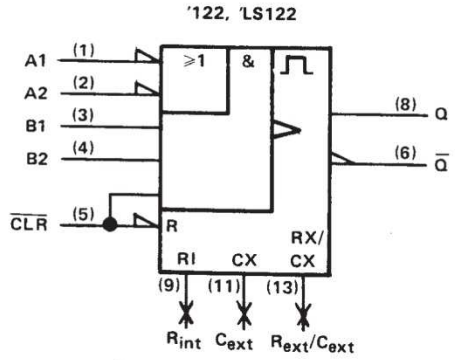
logic diagram (positive logic)

'122, 'LS122



logic symbol†

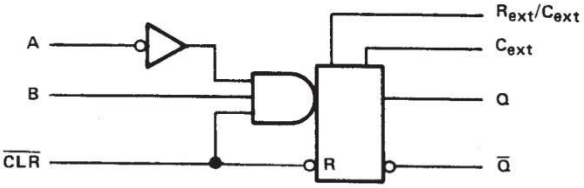
'122, 'LS122



R_{int} is nominally 10 kΩ for '122 and 'LS122

logic diagram (positive logic) (each multivibrator)

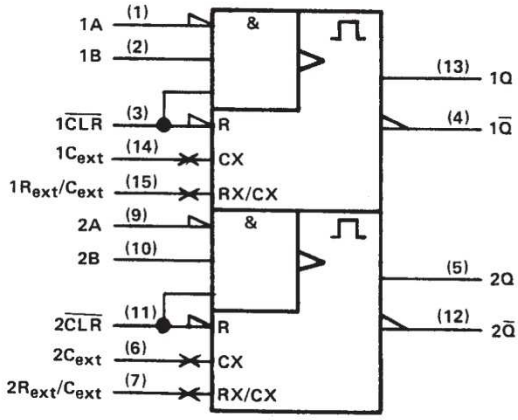
'123, '130, 'LS123



Pin numbers shown are for D, J, N, and W packages.

logic symbol†

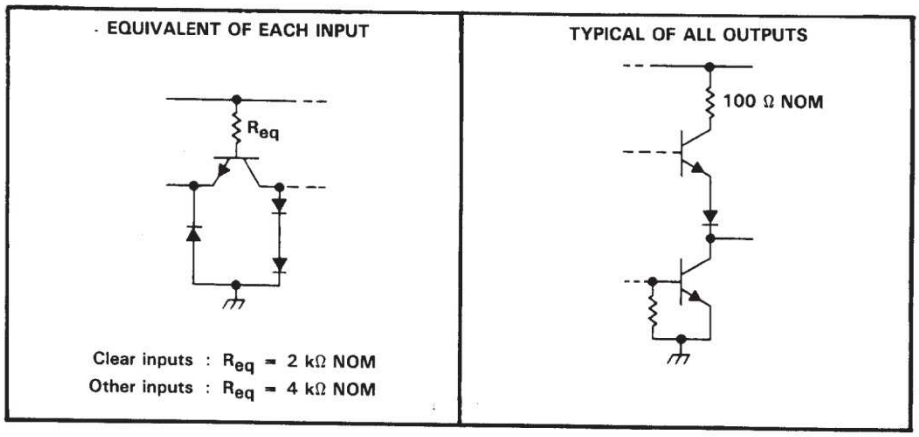
'123, '130, 'LS123



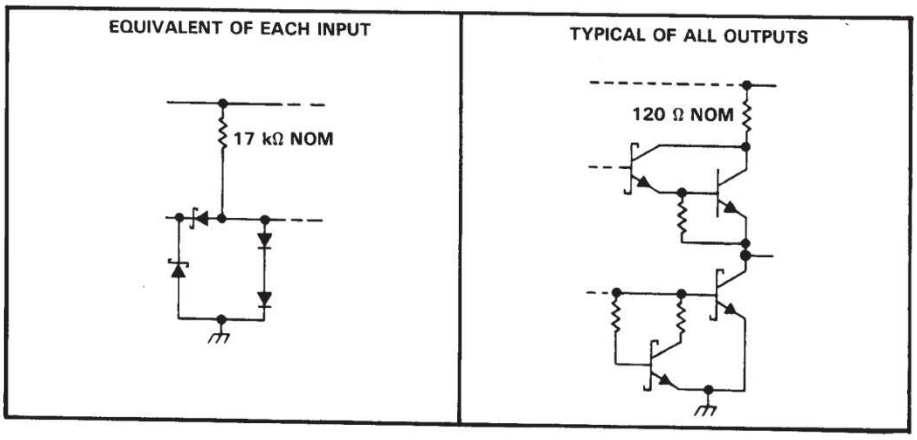
†These symbols are in accordance with ANSI/IEEE Std 91-198
and IEC Publication 617-12.

schematics of inputs and outputs

'122, '123, '130 CIRCUITS



'LS122, 'LS123 CIRCUITS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '122, '123, '130 . . . . . 5.5 V
'LS122, 'LS123 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse durations when $C_{ext} \leq 1000$ pF, see Figure 4.

The output pulse duration is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse duration (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

where

K is 0.32 for '122, 0.28 for '123 and '130

R_T is in kΩ (internal or external timing resistance.)

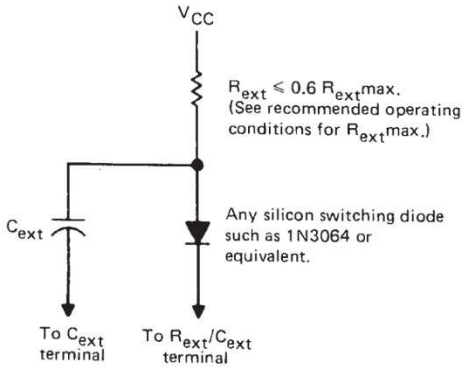
C_{ext} is in pF

t_w is in ns

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse duration is:

$$t_w = K_D \cdot R_T \cdot C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

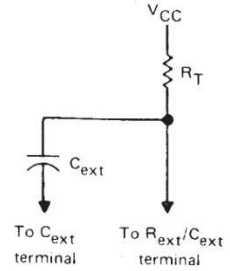
K_D is 0.28 for '122, 0.25 for '123 and '130



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} > 1000$ pF AND CLEAR IS USED

FIGURE 2

Applications requiring more precise pulse durations (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.



TIMING COMPONENT CONNECTIONS

FIGURE 3

TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE

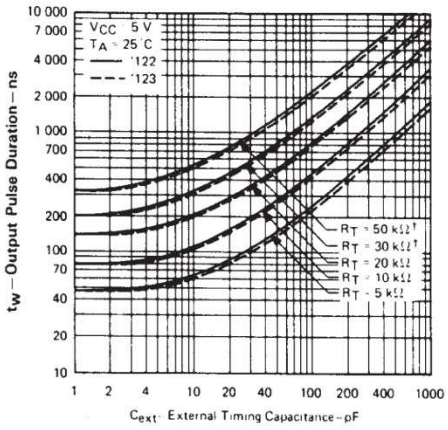


FIGURE 4

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' circuits.

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when $C_{ext} \leq 1000$ pF, use Figure 6, or use Figure 7 where the pulse duration may be defined as:

$$t_w = K \cdot R_T \cdot C_{ext}$$

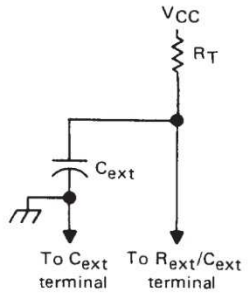
When $C_{ext} \geq 1\ \mu F$, the output pulse width is defined as:

$$t_w = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

K is multiplier factor, see Figure 7
R_T is in kΩ (internal or external timing resistance)
C_{ext} is in pF
t_w is in ns

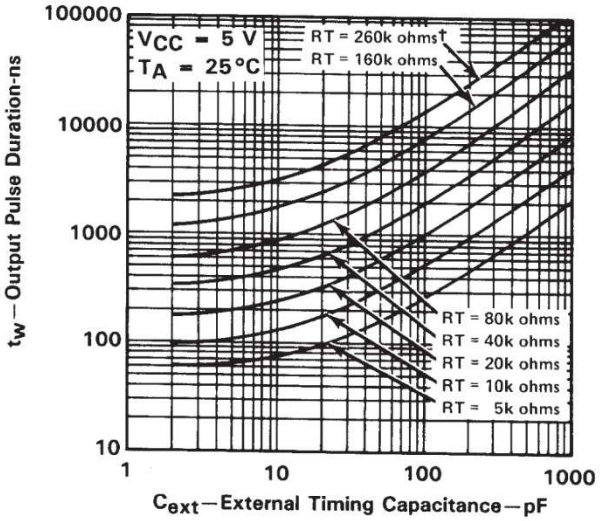
For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electolytic capacitors.



TIMING COMPONENT CONNECTIONS

FIGURE 5

'LS122, 'LS123
TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE



†This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 6

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123†

MULTIPLIER FACTOR
vs
EXTERNAL CAPACITOR

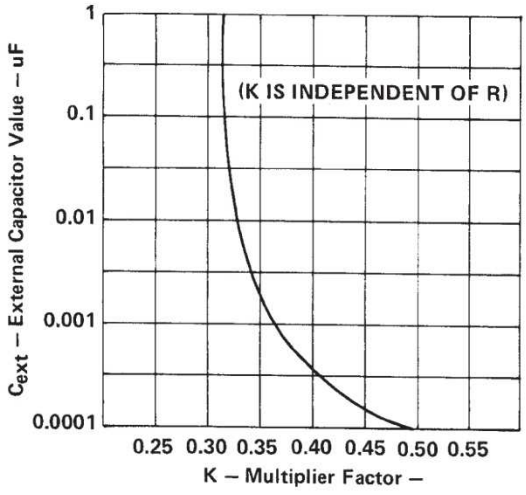


FIGURE 7

DISTRIBUTION OF UNITS
vs
OUTPUT PULSE DURATION

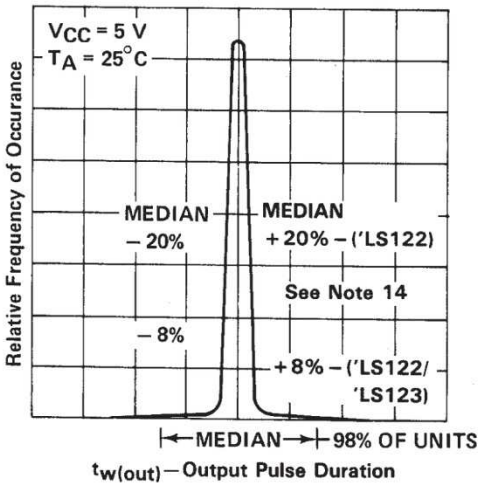


FIGURE 8

VARIATION IN OUTPUT PULSE DURATION
vs
SUPPLY VOLTAGE

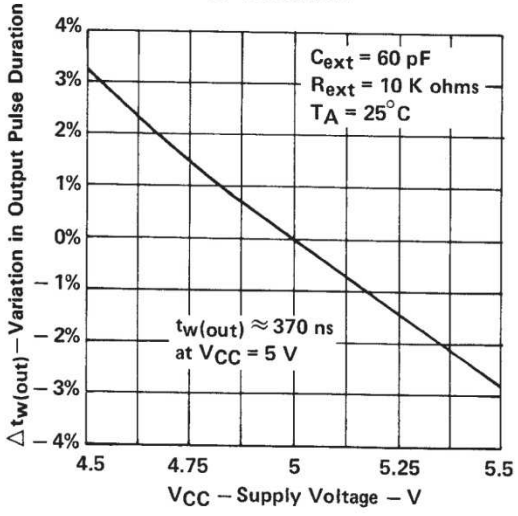


FIGURE 9

VARIATION IN OUTPUT PULSE DURATION
vs
FREE-AIR TEMPERATURE

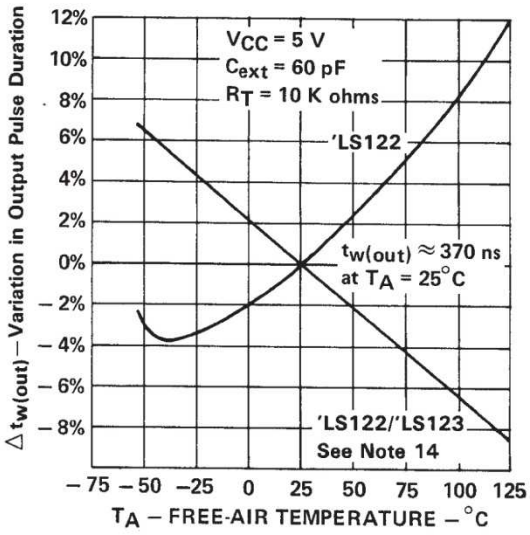


FIGURE 10

NOTE 14: For the 'LS122, the internal timing resistor, R_{int} was used. For the 'LS122/123, an external timing resistor was used for R_T.

†Data for temperatures below 0°C and above 70°C and for suply voltages below 4.75 V and above 5.25 V are applicable for SN54LS122 and SN54LS123 only.