CP/M 2.2b for Tarbell SD Controller (Track Buffered CP/M 2.2)

This version of CP/M 2.2 is for the Tarbell single density floppy controller with an Altair 88-2SIO for serial I/O. The console, punch, and reader use the first port on the 2SIO and the list device routes through the second port on the 2SIO. IOBYTE support can be enabled after cold boot to allow flexible use of a variety of typical Altair I/O devices. See "IOBYTE Implementation" below.

The BIOS uses full track buffering on both reads and writes to improve performance. Performance is 20%-70% faster than the non-buffered BIOS for typical disk based operations. Disks are fully interchangeable with the non-buffered versions of CP/M 1.4 and 2.2.

The disk image file, CPM22b15-48K-SSSD.DSK, is sized for 48K of RAM and includes the source files and utilities required to transfer files to/from a PC, backup/restore disk images, and size CP/M for a different amount of RAM with MOVCPM. The MOVCPM on this disk is custom for this version of CP/M and *does not* require the boot loader or BIOS to be patched into the CP/M image.

In order to fit in the boot tracks of a standard SSSD IBM format soft sectored 8" disk, the code/initialized data portion of this BIOS can only be 380h bytes long. This restriction substantially reduces the features that can be provided by this BIOS and required a few tricks in the code to save space. The source file has a conditional assembly statement to detect when this size limit is exceeded. Look for "BIOS IS TO BIG ****" as an error statement when assembling.

IOBYTE Implementation

Due to size constraints, IOBYTE support is not implemented in the BIOS as it exists on the boot tracks. Instead, full I/O support can be loaded into the BIOS in RAM after cold boot by running the IOBYTE.COM program. The IOBYTE program also allows configuring CP/M to automatically run IOBYTE upon cold boot and to save the default IOBYTE value. Run the IOBYTE program with no parameters to see program help.

Once IOBYTE support is loaded, the following port assignments are available:

CON device (bits 1,0): 00 - TTY on 88-SIO at 0/1 01 - CRT on 88-2SIO at 10h/11h* 10 - BAT (indirect through RDR and LST devices) 11 - UC1 on 88-2SIO at 12h/13h	**PUN** device (bits 5,4): 00 - TTY on 88-SIO at 0/1 01 - PTP on 88-2SIO at 10h/11h* 10 - UP1 on cassette port (SIO 6/7) 11 - UP2 on 88-2SIO at 12h/13h
RDR device (bits 3,2): 00 - TTY on 88-SIO at 0/1 01 - PTR on 88-2SIO at 10h/11h* 10 - UR1 on cassette port (SIO 6/7) 11 - UR2 on 88-2SIO at 12h/13h	**LST** device (bits 7,6): 00 - TTY on 88-SIO at 0/1 01 - CRT on 88-2SIO at 10h/11h 10 - LPT on 88-2SIO at 12h/13h* 11 - UL1 on 88-LPC at 2/3

* = Default IOBYTE

Patching the IOBYTE and MODE Byte

The STAT utility in CP/M is typically used to make IOBYTE device assignments as required. These assignments are temporary and the default IOBYTE value is restored upon cold boot. To permanently modify the IOBYTE, the default IOBYTE in the CP/M boot image must be patched.

The IOBYTE.COM program can be used to patch the IOBYTE value loaded upon cold boot. When IOBYTE is run with the “A” or “D” options, the current value of the IOBYTE is written into the boot tracks to be the default IOBYTE for subsequent cold boots. Run the IOBYTE program with no parameters to see additional information.