

FD3812 DOUBLE DENSITY  
FLEXIBLE DISK SYSTEM  
AND  
FF38-XX "FRUGAL FLOPPY" SERIES  
USER'S GUIDE



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CHANGE RECORD

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## SCOPE OF MANUAL

This documentation provides a description of the FD3812 Flexible Disk system and the FF38-XX Frugal Floppy systems, and the associated Double Density Controller. These systems, unless otherwise specified, are referred to in this documentation as the Double Density Disk system.

The manual contains an operator's guide, an interfacing guide and a theory of operation. Also included are some general troubleshooting aids, designed for use with the theory of operation to help isolate minor system malfunctions.

The manual contains five sections as follows:

SECTION	DESCRIPTION
1	The Introduction to this manual contains a description of the system. Also included are controller, drive and media specifications.
2	Provided in the Interfacing Requirements is information needed for interfacing the Double Density Controller to a microcomputer. Also contained are cable installation instructions and pin assignments.
3	The Operator's Guide provides an explanation of command and status instructions, as well as, diskette care and loading information. The switches and indicators are also defined in this section.
4	A general description of the Double Density Controller schematics is provided in the Theory of Operation section.
5	A Troubleshooting section provides general procedures for locating problems that may be encountered when using the Double Density Disk system.

SECTION 1  
INTRODUCTION

# 1 INTRODUCTION

## 1-1 SYSTEM DESCRIPTION

The FD3812 Flexible Disk system consists of a Double Density Controller, two disk drives, a power supply and a cabinet. "Frugal Floppy" FF38-XX systems do not have the cabinet and power supply, and may consist of one, two, three or four disk drives.

Disk formats used with the Double Density Disk systems are IBM Diskette 1 single-density, or IBM Diskette 2D double density. Both formats are for single sided operation only.

The Double Density Controller is designed for easy integration into commercial, industrial and developmental applications, providing the necessary features for successful and convenient operation of a powerful disk system. The Double Density Controller is capable of driving up to four floppy disk drives.

The Double Density Controller consists of one printed circuit board with all connectors along one edge of the board. This eliminates the need for card cages or back plane wiring.

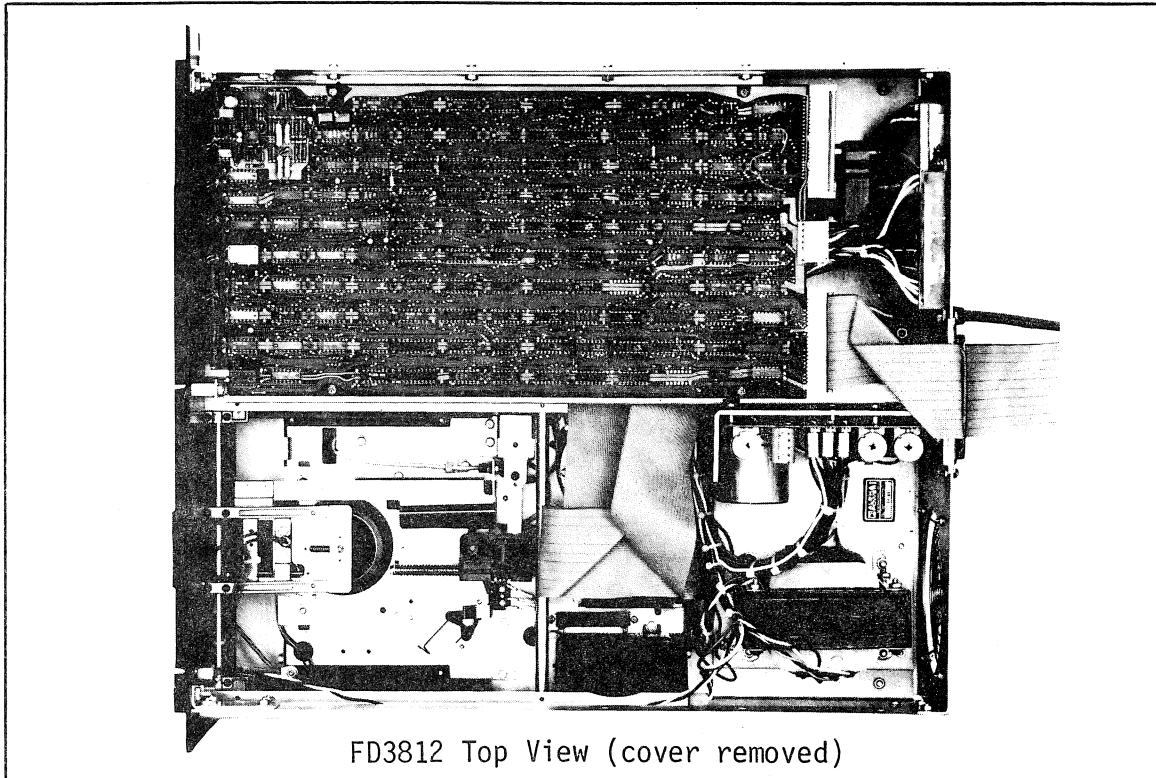
The physical specifications of the FD3812 system follow:

Height:	7.75 in. (196.8 mm)
Width:	19.16 in. (486.6 mm)
Depth:	20.50 in. (520.0 mm)
Weight:	70 lb. (32 Kg)

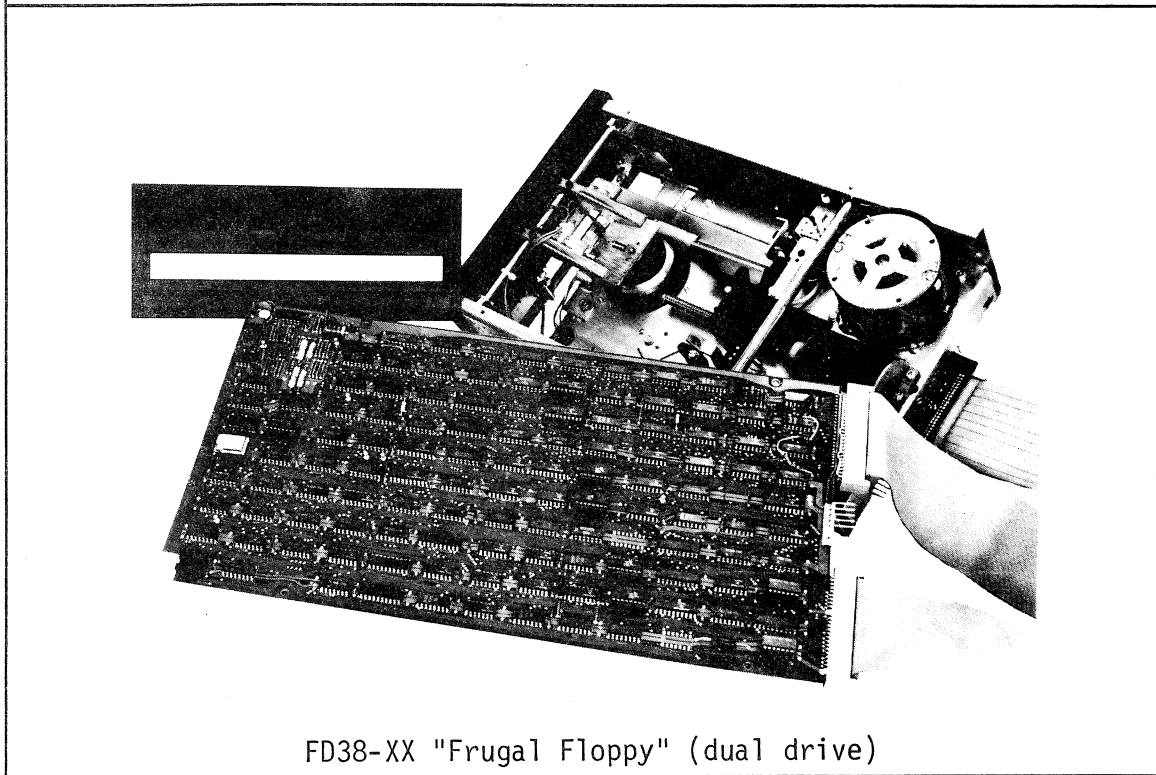
Double Density Disk systems use less than 300 watts (nominal) of AC power. A third wire AC line cord ground return, and an AC power fuse (at rear of cabinet) is provided for safety.

Interfacing for the Double Density Disk systems may be performed by utilizing the S-100 interface board when the system is being used with a MITS 8800 series computer. Interfacing for Multibus<sup>TM</sup> systems may be obtained using the Multibus<sup>TM</sup> interface board.

Multibus<sup>TM</sup> is a trademark of Intel Corporation.



FD3812 Top View (cover removed)



FD38-XX "Frugal Floppy" (dual drive)

# 1 INTRODUCTION

## 1-2 DRIVE SPECIFICATIONS

The Double Density Disk system employs a modified Pertec model FD514 disk drive, part number 250254. The performance characteristics and power requirements are stated below.

### ROTATION AND START UP CHARACTERISTICS

- Rotational Speed - 360 rpm
- Speed Variation -  $\pm 1.5\%$  ( $\pm 1.6\%$  per Hz variation at 60 Hz or  $\pm 2\%$  per Hz variation at 50 Hz).
- Rotational Direction - CCW (Counterclockwise) as viewed from the recording side.
- Average Latency - 83.3 milliseconds
- Start-up time - 2 seconds (max)
- Stop time - 2 seconds (max)

### ACCESS TIME

- Track to Track - 10 milliseconds (min) seek time
- Head Settling Time - 20 milliseconds (at last track addressed)
- Head Loading Time - 40 milliseconds (max)

### ERROR RATE

- The error rate (exclusive of external sources, i.e., user's electronics, diskette defects or other contamination) will be a maximum of:

1 recoverable error per  $10^9$  bits  
1 non-recoverable error per  $10^{12}$  bits

A non-recoverable error is defined as an error that persists after the error recovery procedure is performed.

The read error recovery procedure is as follows:

- Reread the track 5 times.
- If data is not recovered, move the head away (not less than 5 tracks) from the track in question in either direction; return to the desired track and reread the track 5 times.
- If data is still not recovered, unload and reload the head, then reread the track 5 times.

The seek error recovery procedure is as follows:

Recalibrate the track location by issuing repetitive Step Out commands until the Track 0 signal is recovered, then reseek the desired track and reread.

#### DC POWER REQUIREMENTS

- + 24 volts DC  $\pm$  1.0 volts, 1.4 amperes maximum (in operation the current load on the 24 volt line is pulsating and depends on the operating conditions).
- + 5 volts DC  $\pm$  0.25 volts, 1.4 amperes maximum; 1.25 amperes typical (100 millivolts peak-to-peak ripple).
- -12 volts DC  $\pm$  0.50 volts, 0.3 amperes maximum (200 millivolts peak-to-peak ripple).

#### DC POWER REQUIREMENTS (STANDBY CONDITION)

- Standard configuration, 24 volts line: 0.6 amperes maximum

#### DC POWER REQUIREMENTS (OPERATING CONDITION)

- Peak current, 24 volt line: 1.4 amperes maximum
- Average current, worst case seek: 1.0 amperes maximum

#### DC POWER SEQUENCING

- None required. 100 milliseconds maximum required from time of power application to time when unit can receive commands.

#### AC POWER REQUIREMENTS

- Standard, 90-130 volts AC at 60 Hz  
Run Current: 0.43 amperes nominal; 0.48 amperes maximum  
Power: 33 watts nominal; 42 watts maximum
- Option 1, 190-250 volts AC at 50 Hz  
Run Current: 0.25 amperes nominal; 0.30 amperes maximum  
Start Current: 0.11 amperes nominal; 0.13 amperes maximum  
Power: 39 watts nominal; 46 watts maximum

## 1 INTRODUCTION

### 1-3 FUNCTIONAL DESCRIPTION

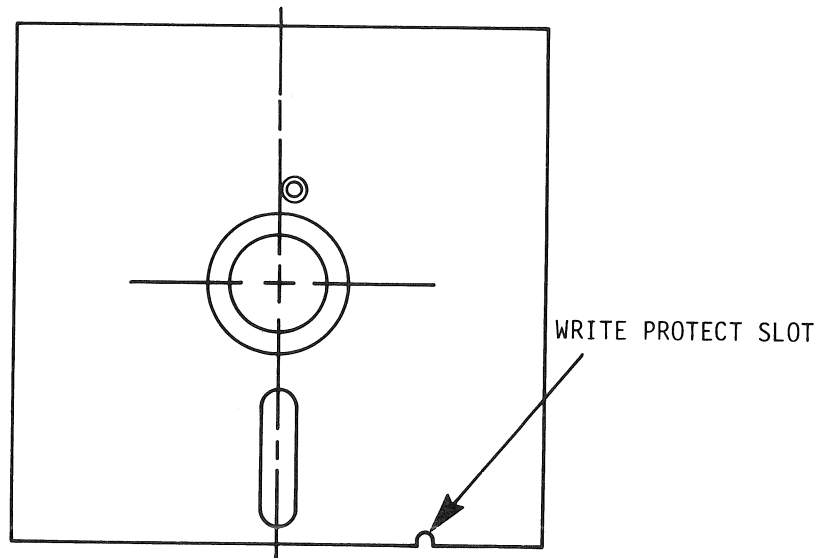
General functions of the Double Density Controller are described in this section.

The Double Density Controller responds to eight-bit command words to transfer data to the write buffer from the read buffer, or to and from the diskette. Commands are also used to seek to data tracks, and to format the diskette.

Seek commands are used to position the READ/WRITE head at the desired track. All seek timing is controlled by the Double Density Controller. Positioning is verified by reading the track address from the disk.

The READ/WRITE head will remain loaded for approximately 700 milliseconds following a disk operation, as long as the drive remains selected. If no other read, write or seek commands are issued, the head will be unloaded after this time period. The head will be unloaded immediately if the disk drive is deselected.

The disk drive units sense write protected diskettes and present this status to the interface. Light from an LED, passing through the slot in the diskette (see the following diagram), activates a photo transistor sensor which disables the disk drive write electronics.





The controller may be used to format blank diskettes in either single or double density, and data is recorded on the disk in either IBM-3740 single-density format or IBM double density format (format described in section 3-4). These are both soft sectored formats (hard sectored formats are not allowed). Format specifications are summarized in the following table:

	SINGLE DENSITY	DOUBLE DENSITY
Data bytes per sector - Track 0	128	128 (single density)
- All other tracks	128	256
Sectors per track	26	26
Tracks per diskette	77	77
Data bytes per diskette	256,256	509,184
Transfer rate to/from disk (Bytes/sec.)	31,250	62,500

Up to four drives may be operated by the Double Density Controller in a master-slave configuration (only one drive is accessed by the controller at any one time).

1 INTRODUCTION

1-4 MEDIA REQUIREMENTS

This section specifies the type of diskette that can be used with the systems for single or double density recording.

SINGLE DENSITY	Any 3740 - type diskette as defined by IBM Original Equipment Manufacturers (OEM) information GA 21-9190-1 (with subsequent revisions) may be used.
DOUBLE DENSITY	Any unformatted diskette that has been qualified specifically for double density recording may be used. Such diskettes formatted or written by other systems must be reformatted by the Double Density Controller system. Hard Sektored diskettes are not allowed. Diskettes must have a single index hole and must be single sided (these Double Density Disk systems do not have double sided recording capabilities).

1 INTRODUCTION

1-5 ENVIRONMENTAL CONDITIONS

There are specific operating and non-operating conditions which should be observed for the disk drive and controller, as well as the media (diskette) used in the disk drive.

MEDIA

The environmental specification for the media used in the disk drive determines the allowable temperature and humidity at the site where the system is installed. Ambient temperature of the system should not exceed a value of 10°C below the maximum operating temperature of the media being used.

DRIVE/CONTROLLER (NON-OPERATING)

Non-operating conditions are a temperature range of -40°C to 70°C (-40°F to 156°F), and a relative humidity range of 5% to 95% (without condensation).

DRIVE/CONTROLLER (OPERATING)

During operation, vibration limits are 6-600 Hz at .05G. The shock limit is 1.5G for 11 milliseconds.

A temperature range of 10°C to 42°C (50°F to 110°F) and a relative humidity of 20% to 80% should be observed.

1 INTRODUCTION

1-6 CONTROLLER OPTIONS

The following options are available for the Double Density Controller.

A version of the controller is available without the Read Data Buffer and Write Data Buffer. This version allows use of the Direct Memory Access (DMA) method of data transfer to and from the disk.

A controller and drive configuration is available to meet either of the following input power requirements:

115 VAC, 60 Hz  
or  
230 VAC, 50 Hz

The FD3812 system is available with a special cabinet for mounting in a 19-inch EIA (Electronic Industry Association) approved rack enclosure.

An FD3812 system is available without the Double Density Controller board, so that it can be used as a "SLAVE" unit in a three or four drive "MASTER" and "SLAVE" configuration.

SECTION 2  
INTERFACING REQUIREMENTS

## 2 INTERFACING REQUIREMENTS

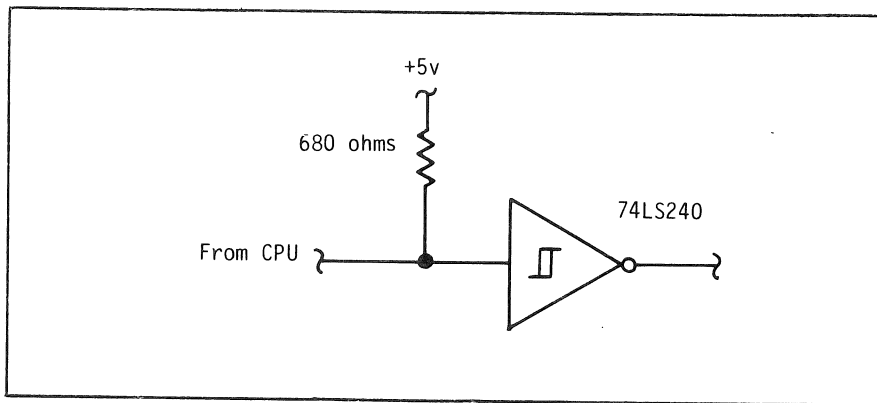
### 2-1 SIGNAL LEVELS

Input and output logic signals, input receivers and output drivers used by the Double Density Controller are described in this section.

Input logic signals for the system are as follows:

Logic "0": +2.0V min to +5V max (False)  
Logic "1": +0.0V min to +0.8V max (True)

The standard input load (shown below) is a TTL gate (74LS240 plus 680 ohms to +5V).



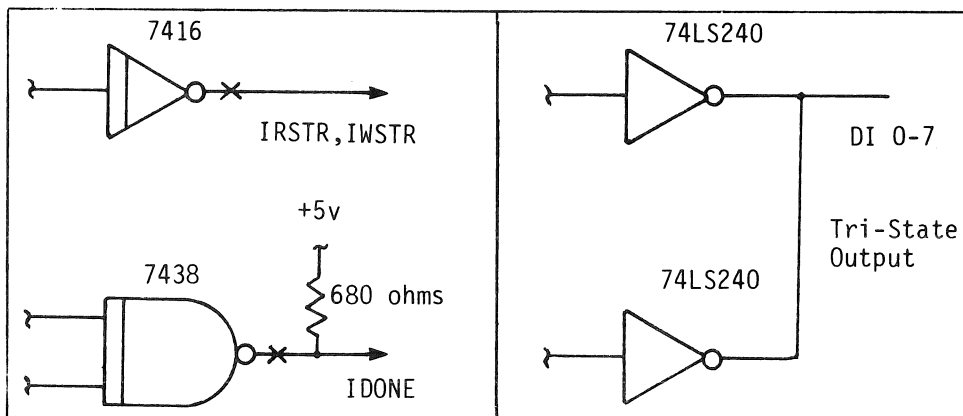
Output drivers are also 74LS240 TTL gates.

Output logic signals for the system are as follows:

Logic "0": +2.4V min to +5V max (False)  
Logic "1": +0.0V min to +0.4V max (True)

Sink current at logic "1" is 24 milliamps

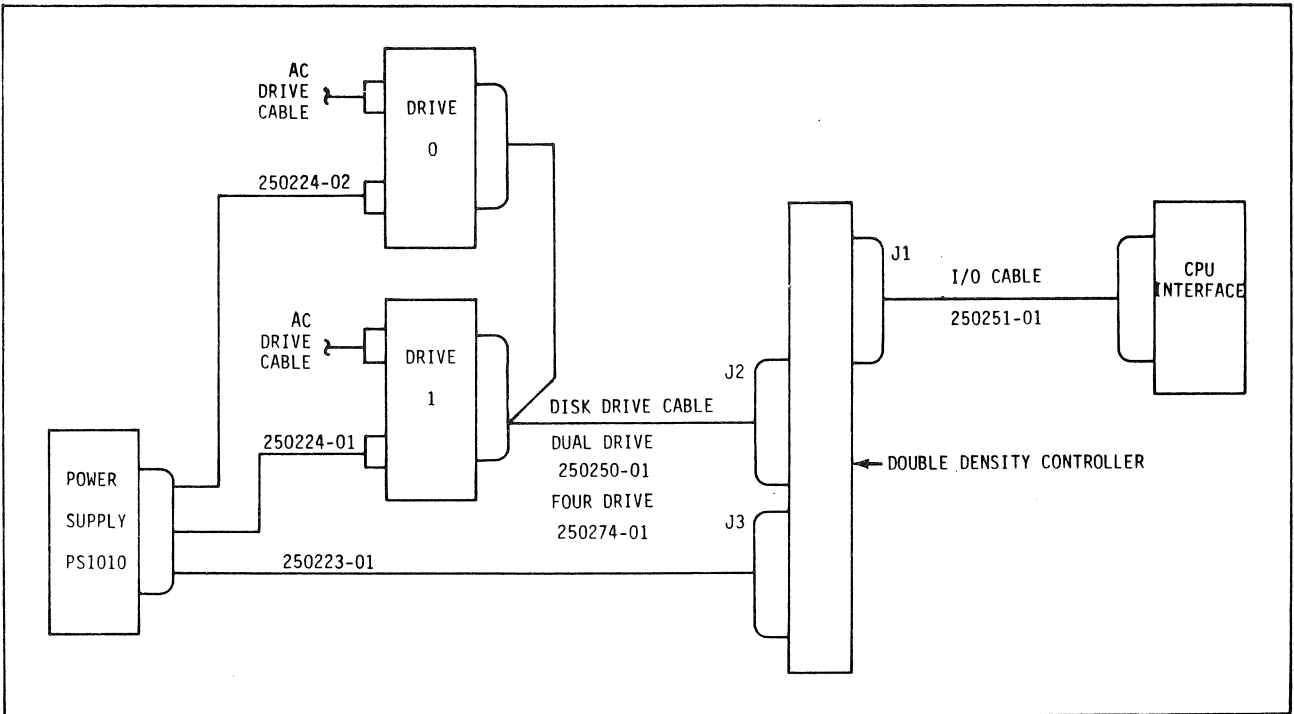
Output drivers used on the Double Density Controller are as follows.



## 2 INTERFACING REQUIREMENTS

### 2-2 SYSTEM INTERCONNECTION DIAGRAM

A typical FD3812 system interconnection diagram is provided below. Note the fact that drive 0 is at the terminus of the disk drive cable. Drive 0 contains the line terminator.



## 2 INTERFACING REQUIREMENTS

### 2-3 CABLE/CONNECTOR INSTALLATION

There are three flat cables that interconnect the Frugal Floppy FF38-XX system. The cables for the FD3812 system are pre-connected, however, these same instructions would apply.

#### CABLES

The Input/Output (I/O) cable and the disk drive cable are 50 conductor ribbon cables. The I/O cable extends out the back of the FD3812 system cabinet, and is used to connect the controller to the interface or mainframe (CPU). The disk drive cable connects the Disk Drives to the controller.

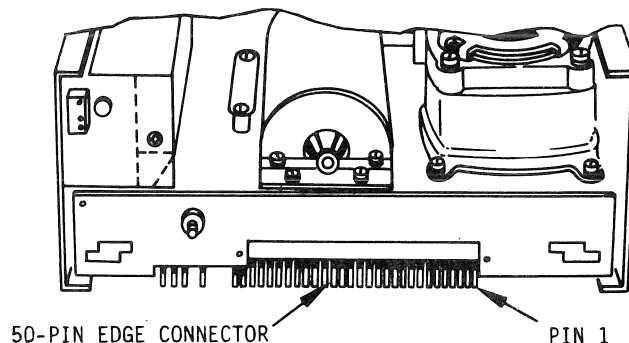
#### I/O CABLE CONNECTION

On each end of the I/O cable is a 50-pin connector. These cable connectors (as well as the disk drive cable connectors) are Pertec part number 503-0147. The connector on one end of the I/O cable connects to the interface board and the other connector plugs into the controller edge connector "J1" (indicated in the photograph on the opposite page). The connector pin numbers are marked on the face of the connector, and the arrows indicating connectors J1 through J4 in the photograph are also pointing to the edge connector pin 1 location. Pin 1 is also indicated on the controller silkscreen diagram in Appendix B. Align pin 1 of the cable connector on one end of the cable with pin 1 of the edge connector, and attach the cable connector to the controller. Then, attach the remaining connector to the interface.

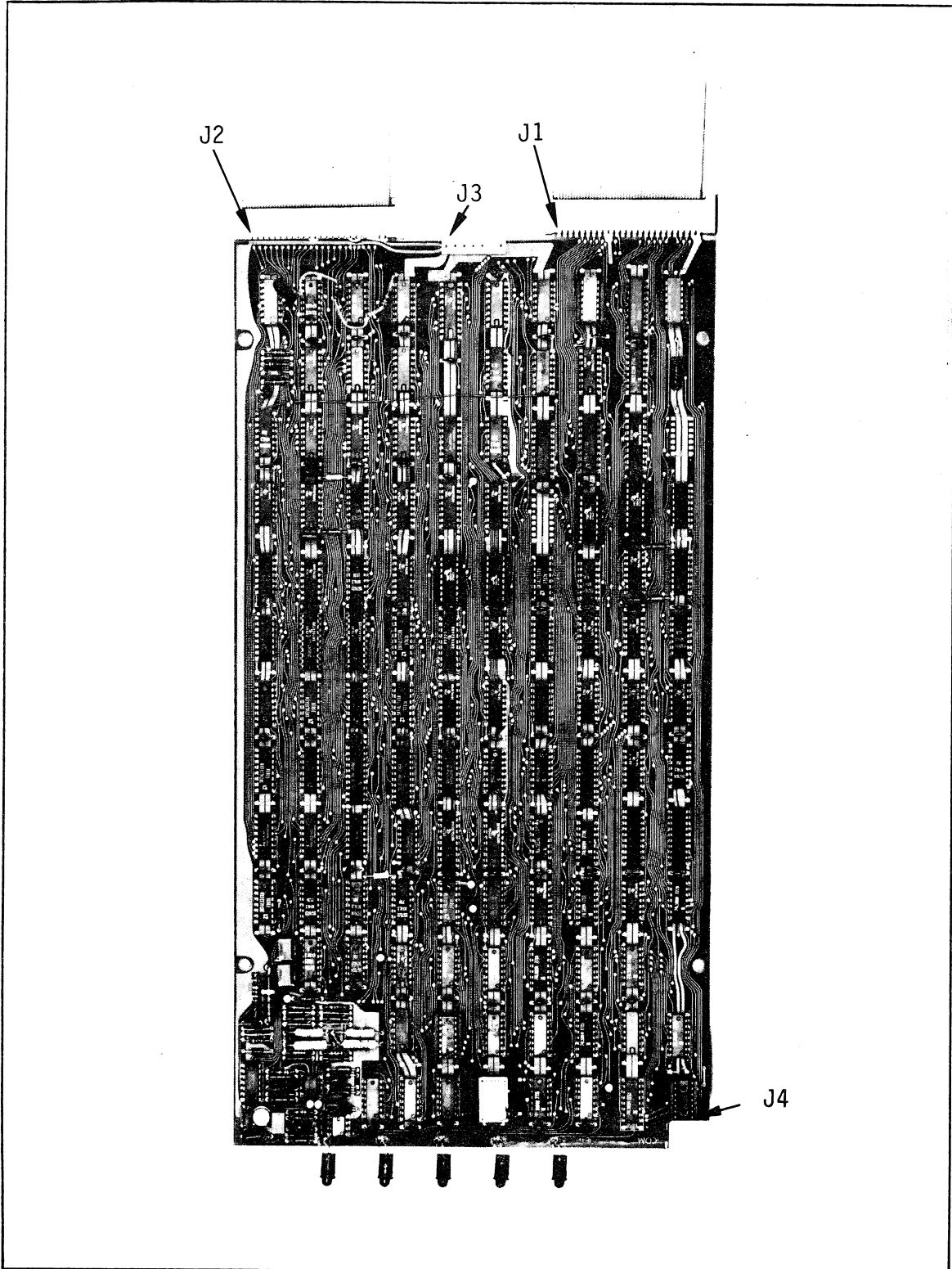
#### DRIVE/CONTROLLER CABLE INSTALLATION

The pre-connected Disk Drive Cable for a FD3812 system has one connector on each end, and an additional connector attached along the cable, allowing two drives to be connected to the controller in daisy chain fashion. For three or four drive systems, the cable is extended in length and additional connectors are added. Thus, up to four drives may be connected to the controller in serial fashion.

The cable for a "Frugal Floppy" may contain a connector at each end for single drive systems, or up to five connectors for multiple drive systems. Attach the connector at one end of the cable to the 50-pin edge connector on the controller card, as indicated by "J2" in the photograph on the opposite page. The arrow indicating J2 in the photograph also identifies the controller edge connector pin 1 location. Attach the remaining cable connectors to the 50-pin edge connector on the back panel of each drive (pin 1 to pin 1). The drive pin 1 location is shown in the following diagram.







Double Density Controller Cable Connector Locations

## 2 INTERFACING REQUIREMENTS

### 2-4 STATUS INDICATOR CONNECTOR

A fourth cable may be added to FF38-XX systems if LED status indicators are required.

J4 is a 14-pin DIP socket that allows the addition of external status indicators (LEDs) to Frugal Floppy™ systems. The socket includes a pin position for +5 volts, and all status signals are open collector low True. A series resistor must be included with the external LEDs. The LED current should be limited to 40 milliamps.

#### PIN CONFIGURATION - STATUS INDICATOR

PIN NUMBER	SIGNAL NAME
1	Controller Busy
2	Drive Ready
3	Ground ("POWER" light)
4	Write Protect
5	Double Density
6	+5 volts (for power to all LEDs)
7 through 14	Not Used

## 2 INTERFACING REQUIREMENTS

### 2-5 CONTROLLER POWER REQUIREMENTS

The table below shows the controller power connector pin assignments. This connector is designated J3, and connects the power supply voltages to the Double Density Controller board. Current requirements at each pin are also provided.

CONNECTOR J3

PIN NUMBER	DESCRIPTION	CURRENT REQUIREMENT
1	Ground	N/A
2	+5 volts ( $\pm 0.25$ volt)	2.6 amperes
3	-12 volts ( $\pm 0.5$ volts)	60 milliamperes
4	+24 volts ( $\pm 1.4$ volts)	85 milliamperes
5	UNO (selected unit status)	N/A
6	Key	N/A
7	UNI (selected unit status)	N/A

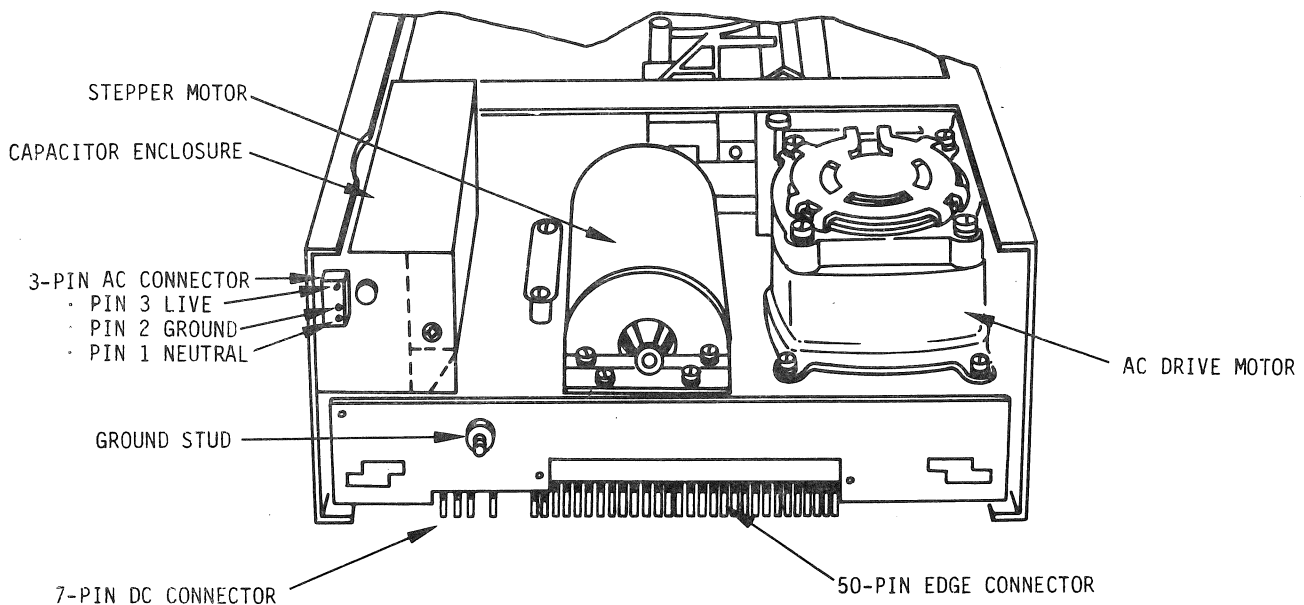
N/A = Not Applicable

## 2 INTERFACING REQUIREMENTS

### 2-6 DRIVE AC AND DC POWER CONFIGURATION

The physical power pin locations and the power pin assignment for the FD514 drive are described in this section.

Power is applied to the FD514 drive through a 7-pin connector (designated in the following diagram) soldered to the printed circuit board (Pertec part number 600057-01). The following diagram also shows the pin configuration for the 3-pin AC input power connector and the basic drive configuration.



The chassis must be connected to earth ground using the ground stud on the drive back panel to ensure proper operation.

The following table provides part numbers for AC supply voltage connector components.

DESCRIPTION	PERTEC PART NUMBER
Pin Housing (Used on Drive)	503-0087
Pins 1 and 3	503-0088
Pin 2 (Ground)	503-0089
Socket Housing (Attached to Power Cord)	503-0095
Sockets	503-0094

The pin assignments for the DC supply voltages are provided in the following table.

PIN NUMBER	SUPPLY VOLTAGE
1	-5 volts DC (-12 volts/ - 16 volts)
2	Return (-5 volts, -12 volts/ - 16 volts)
3	+5 volts DC
4	Return (+5 volts)
5	Key
6	Return (+24 volts)
7	+ 24 volts DC

2 INTERFACING REQUIREMENTS

2-7 USER INTERFACE

The following table shows the pin connections for the I/O Cable (J1).

PIN CONFIGURATION - USER INTERFACE

PIN NO.	SIGNAL NAME	SOURCE	DESCRIPTION
1-7	-----	-----	Not Used
8	IDONE	FD3812 or FF38-XX	Optional Usage
9	DI 0	"	DATA IN 0 (LSB)/BUSY
10	DI 1	"	DATA IN 1/UN 0 (Unit Select)
11	DI 2	"	DATA IN 2/UN 2 (Unit Select)
12	DI 3	"	DATA IN 3/CRC ERROR
13	DI 4	"	DATA IN 4/WRITE PROTECTED
14	DI 5	"	DATA IN 5/DRIVE FAIL
15	DI 6	"	DATA IN 6/MEDIA STATUS
16	DI 7	"	DATA IN 7/DELETED DATA MARK
17-20	GND		GROUND
23-28	N.U.		NOT USED
29	N.U.		NOT USED
30	CPU 0	USER	COMMAND WORD STROBE (Bit 4)
31	CPU 1	"	COMMAND WORD (Bit 1)
32	CPU 2	"	COMMAND WORD (Bit 2)
33	CPU 3	"	COMMAND WORD (Bit 3)
34	CPU 4	"	COMMAND WORD (Bit 4)
35	CPU 5	"	COMMAND WORD (Bit 5)
36	CPU 6	"	COMMAND WORD (Bit 6)

PIN NO.	SIGNAL NAME	SOURCE	DESCRIPTION
37	CPU 7	USER	COMMAND WORD (Bit 7)
38	N.U.		NOT USED
39	CDO 0	USER	DATA OUT BIT 0
40	CDO 1	"	DATA OUT BIT 1
41	CDO 2	"	DATA OUT BIT 2
42	CDO 3	"	DATA OUT BIT 3
43	CDO 4	"	DATA OUT BIT 4
44	CDO 5	"	DATA OUT BIT 5
45	CDO 6	"	DATA OUT BIT 6
46	CDO 7	"	DATA OUT BIT 7
47-50	GND		GROUND
21	IRSTR	FD3812 or FD38-XX	READ STROBE (DMA Only)
22	IWSTR	"	WRITE STROBE (DMA Only)

## 2 INTERFACING REQUIREMENTS

### 2-8 USER INTERFACE SIGNAL DESCRIPTION

The interface signal appearing at the respective I/O cable connector pairs is explained in this section.

SIGNAL DESCRIPTION TABLE

PIN/SIGNAL	DESCRIPTION
Pin 8 - DONE	<p>This signal is a 100 nanosecond pulse that occurs when the controller has completed a read, write or seek operation. Any such operation is completed if one of the following conditions occur:</p> <ul style="list-style-type: none"> <li>• The data transfer to or from the disk is complete and the controller is ready to accept the next command.</li> <li>• An error has occurred during the data transfer process.</li> <li>• A clear command is issued to the controller, while the controller is busy.</li> <li>• A power failure occurs in the controller, while the controller is busy.</li> </ul>
Pin Numbers 9-16 DATA IN and STATUS	<p>When CPU bit 6 is set True (LOW) on the interface, these lines provide the read buffer data. When CPU bit 6 is set False (HIGH), these 8 lines provide status information. The 8 status signals are described in detail in Section 3-6.</p>
Pin Number 21 READ STROBE	<p>This signal is generated by the Double Density Controller and is used with <u>non-buffered</u> versions of the controller only. The data from the disk is transferred to the user by this strobe signal. During read operations, the CPU bit 6 command line is set True, and the data is valid on the Data Out lines between 30 and 800 nanoseconds after the trailing edge of the RSTR signal.</p>
Pin Number 22 WRITE STROBE	<p>This signal is generated by the Double Density Controller and is used with <u>non-buffered</u> versions of the controller only. The first data byte to be written on the disk is placed on the Data Out lines 0.8 milliseconds following the "WRITE" command. The controller will then pulse the "INSTR" interface signal after this first byte has been written on the disk. The data to be written at the next byte location, should be set up on the Data Out lines within one half of a byte time from the trailing edge of the "INSTR" pulse.</p>



PIN/SIGNAL	DESCRIPTION
Pin Numbers 30-37 COMMAND WORD	These lines carry the 8-bit command word to the controller. Commands should remain stable on these lines for the duration of the command. Each command (except "EXAMINE STATUS" and "EXAMINE READ BUFFER") must be preceded by a return of the CPU bit 0 to the "ZERO" state. This may be done by issuing either a "READ STATUS" or "READ DATA BUFFER" command. Each command is described in detail in Sections 3-7 through 3-9.
Pin Numbers 39-46 DATA OUT BITS 0-7	The data on these lines is sent to the controller with each appropriate command. The data on these lines should be stable prior to the leading edge of the CPU bit 0 command signal, and should remain True for at least 2.0 microseconds after the leading edge of the CPU bit 0 command signal.

## 2 INTERFACING REQUIREMENTS

### 2-9 CONTROLLER/DRIVE INTERFACE PIN DESCRIPTION

The Controller/Drive interface pin description (connector J2) is described in the tables below.

#### Controller to Disk Drive (Connector J2 of controller PCBA)

SIGNAL	GROUND	DESCRIPTION
2	1	Head Current Switch (IHCS)
4	3	IDENO
6	5	IDEN1
8	7	IDEN2
12	11	IDEN3
14	13	Head Select (IHSLT)
16	15	Busy (IBSY)
18	17	Head Load (IHLD)
26	25	Drive Select 1 (ISLT0)
28	27	Drive Select 2 (ISLT1)
30	29	Drive Select 3 (ISLT2)
32	31	Drive Select 4 (ISLT3)
34	33	Direction Select (IDIR)
36	35	Step (ISTP)
38	37	Write Data (IWDA)
40	39	Write Enable (IWEN)

#### Disk Drive to Controller (Connector J2 of controller PCBA)

SIGNAL	GROUND	DESCRIPTION
10	9	Media Status
20	19	Index (INXP)
22	21	Ready (ISRDY)
24	23	Drive Status (IDRVS)
42	41	Track 00 (ITRK)
44	43	Write Protect (IWPT)
46	45	Read Data (IRDA)

#### NOTE

All Controller/Drive interface signals are LOW True.

SECTION 3  
OPERATOR'S GUIDE



### 3 OPERATOR'S GUIDE

#### 3-1 HANDLING AND CARE OF DISKETTES

Special handling and care is required for proper functioning of the flexible diskettes.

To protect the diskettes, the following guidelines should be observed:

- To load a diskette, remove it from its protective envelope, and follow the step by step procedure for loading and unloading a diskette provided in the next section.
- Always place the diskette back into its protective envelope after use. Dirt, dust, or stains on the diskette could cause the loss of data. NEVER place fingers on the magnetic surface of the diskette through the window slot.
- Never leave the diskette lying on the video unit or near an electric motor. Magnetic fields produced by such devices may cause the loss or scrambling of data.
- Use a felt-tip pen to make any notes on the diskette envelope. Using a ballpoint pen or a pencil could damage the diskette inside the envelope.
- Never load a diskette with the disk drive power off.
- Never remove a diskette from the disk drive compartment when the "BUSY" light is on.
- Observe the operating and non-operating temperature specifications for the diskette.

### 3 OPERATOR'S GUIDE

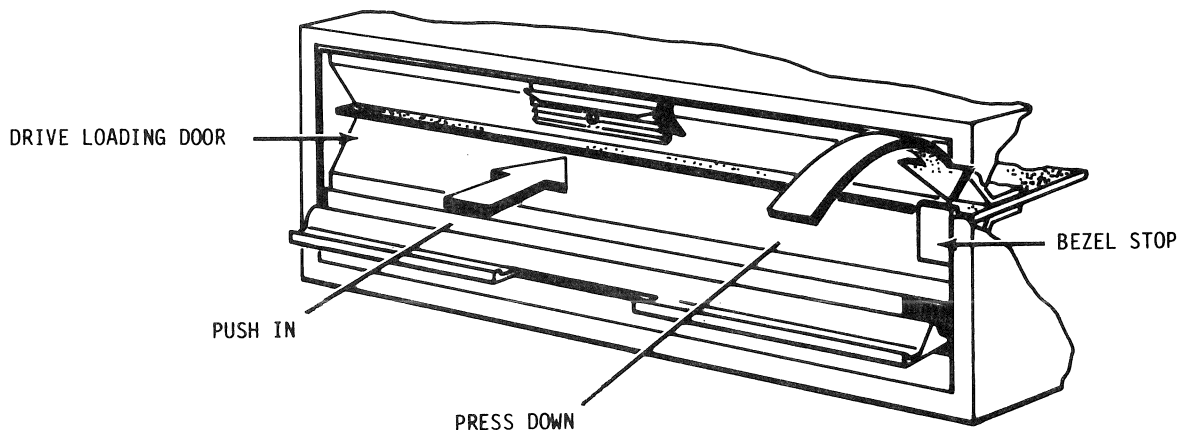
#### 3-2 LOADING AND UNLOADING DISKETTES

The following procedures and precautions must be observed in loading and unloading diskettes.

##### LOADING THE DISKETTE

The following guidelines should be observed when loading a diskette. Refer to the illustration at the bottom of the page.

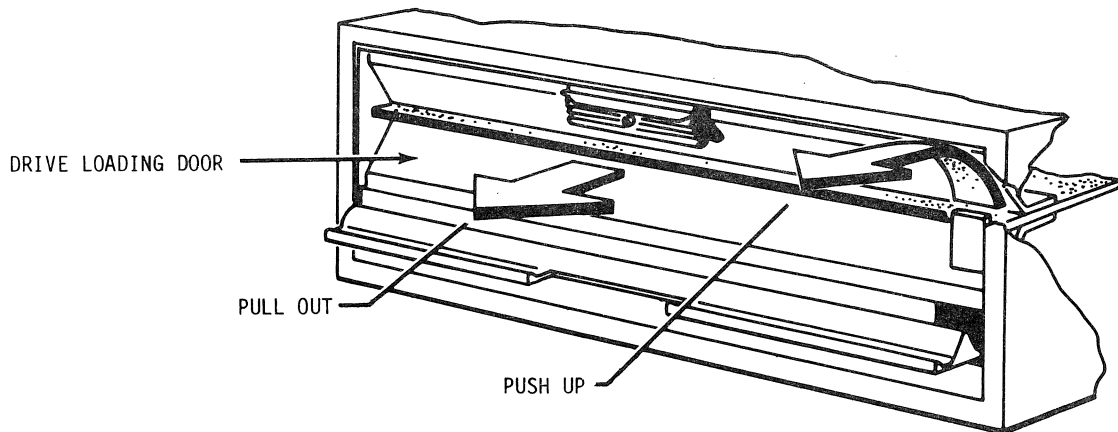
STEP	PROCEDURE
1	Turn the disk drive power on.
2	Open the drive loading door and insert the diskette with the label side up; the oval slot in the jacket inserted first (a light force is required on the right portion of the diskette to overcome a spring load ejector mechanism in the drive).
3	When the diskette is fully inserted, apply a light downward pressure at the right side of the diskette. This will allow it to seat behind the bezel stop. If the diskette did not latch behind the bezel stop, a spring load slide will eject it at least 1 inch from the proper operating position, providing a clear indication that the diskette is not properly inserted. Damage to the diskette hub hole (in center of the diskette) may result if the door is closed and the diskette is not properly inserted.
4	When the diskette is properly inserted and seated behind the bezel stop, close the loading door. This engages the cone/clamping assembly within the drive.



## UNLOADING THE DISKETTE

To remove the diskette make sure the head is not loaded (in contact with the diskette). The BUSY and Drive Door indicators will be ON. Then, referring to the figure on the opposite page, proceed as follows:

STEP	PROCEDURE
1	Open the loading door, making sure the door is fully open to insure the cone clamping assembly within the drive is disengaged. Partial engagement of the cone could cause damage to the diskette.
2	Exert a slight upward pressure on the diskette near the right front corner. The diskette will be partially ejected by the spring load ejector.
3	Fully withdraw the diskette and place it in a protective jacket.
4	Close the loading door.



### 3 OPERATOR'S GUIDE

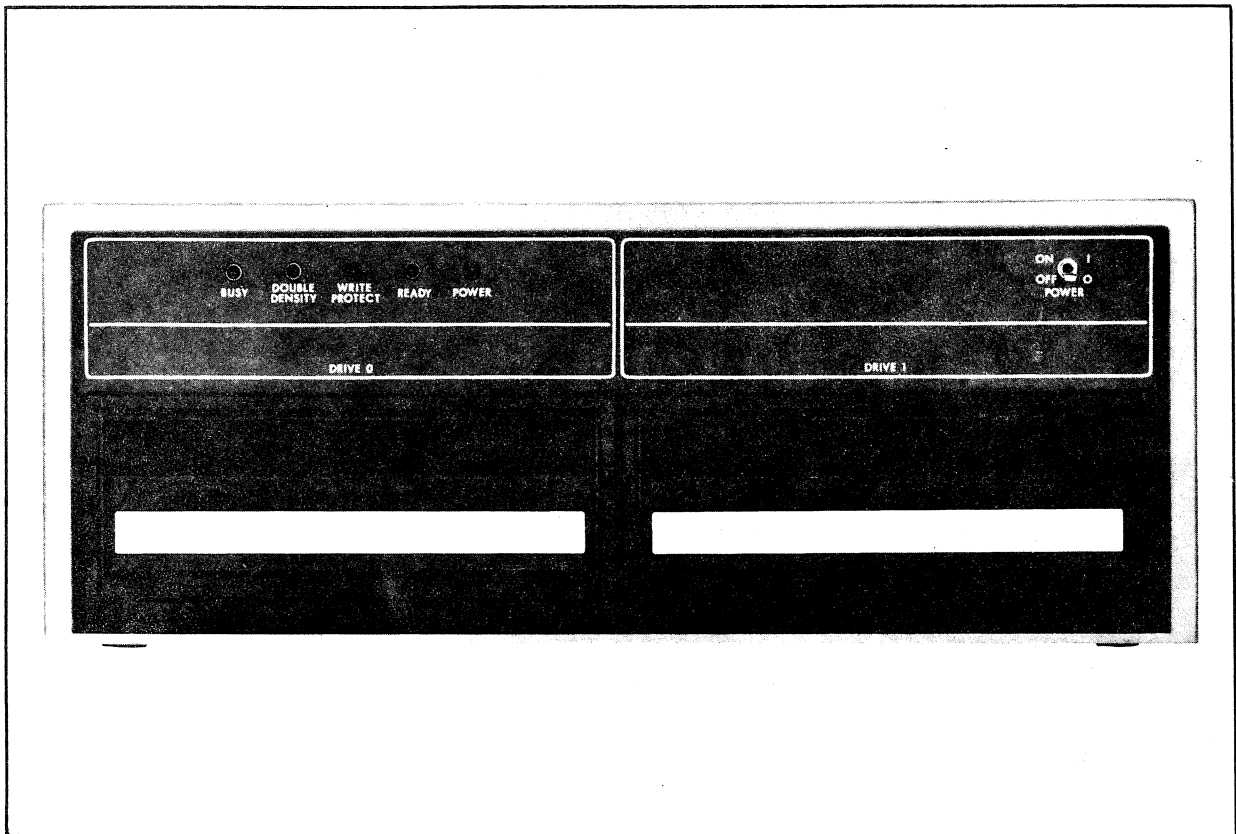
#### 3-3 CONTROLS AND INDICATORS

This section describes the controls and indicators for the Double Density Disk system.

The controls and indicators of the FD3812 disk system (as shown on the facing page) are described in the following table:

SWITCH/INDICATOR	FUNCTION
Power ON/OFF Switch	Turns power on or off.
POWER Indicator	Indicates that the +5 volt power is present on the controller.
READY Indicator	Indicates that the selected drive is turning at the proper speed after the diskette is inserted and the drive door is closed.
BUSY Indicator	Indicates that the controller is executing a command.
WRITE PROTECT Indicator	Indicates that the "Write Protect Slot" on the diskette jacket is <u>uncovered</u> in the selected drive. Data can be read from the diskette, but data cannot be written or changed.
Drive Door Indicator	Indicates that the disk drive is selected and the head is loaded (in contact with the diskette) to perform a command.
DOUBLE DENSITY Indicator	Indicates that the double density mode of reading or writing data is selected.





FD3812 Front Panel

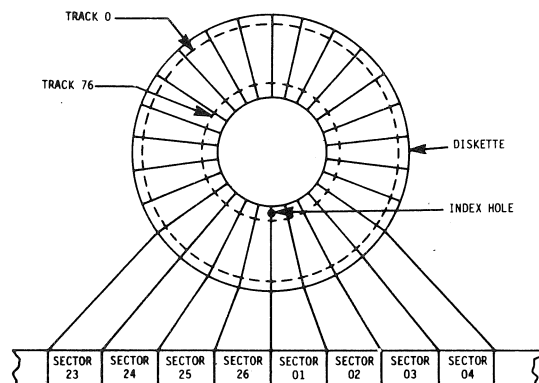
### 3 OPERATOR'S GUIDE

#### 3-4 TRACK FORMAT

Each diskette used with the Double Density Disk system must be initialized using the IBM soft sectoring technique before it can be used for data storage. The initialization process consists of pre-recording sector information on the diskette.

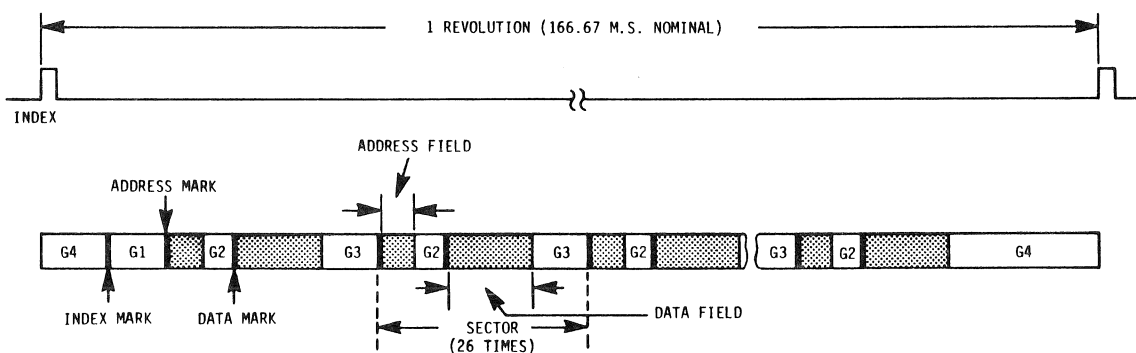
A diskette is divided into 77 tracks; the outermost track is designated Track 0 and the innermost, Track 76. The initialization process writes each track in one continuous operation, dividing each track into 26 sectors. The sectors are referenced by an index hole between sector 1 and 26.

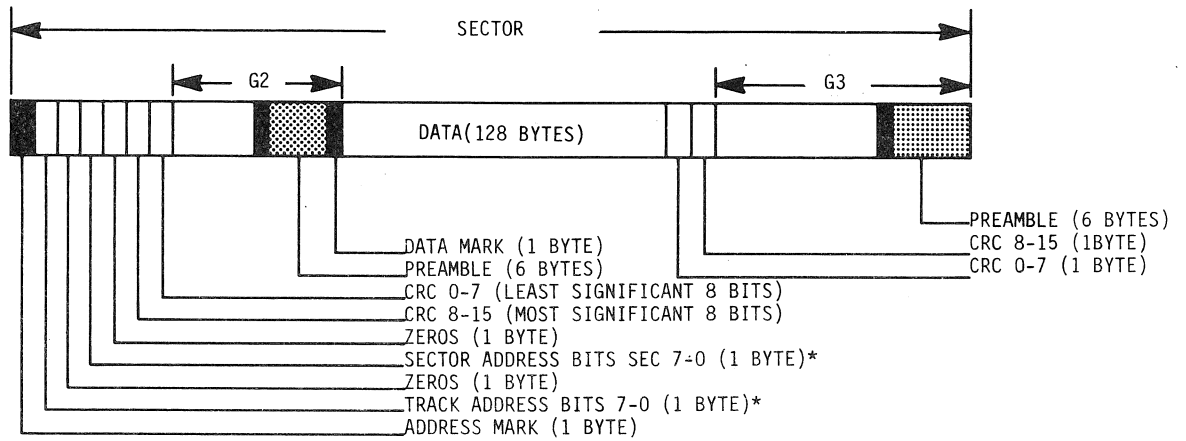
The following diagram illustrates the diskette configuration:



The components of the sector format for both single and double density operation are shown in the figures on the following page. These components are: Mark Bytes (i.e., Index Mark, Address Mark, Data Mark), Address Field, Data Field, and Gap Fields (G1, G2, G3, and G4). Mark bytes are unique combinations of data bits and clock bit patterns which are not allowed in address fields, data fields, or gaps. A gap provides for a preamble and sufficient buffer space. This offsets the effects of deviations from the nominal data density on the track due to tolerances of disk speed and with frequency.

The following figure shows an initialized track from index to index:





GAP FIELDS

G1= 26 BYTES HEX FF  
 6 BYTES HEX 00

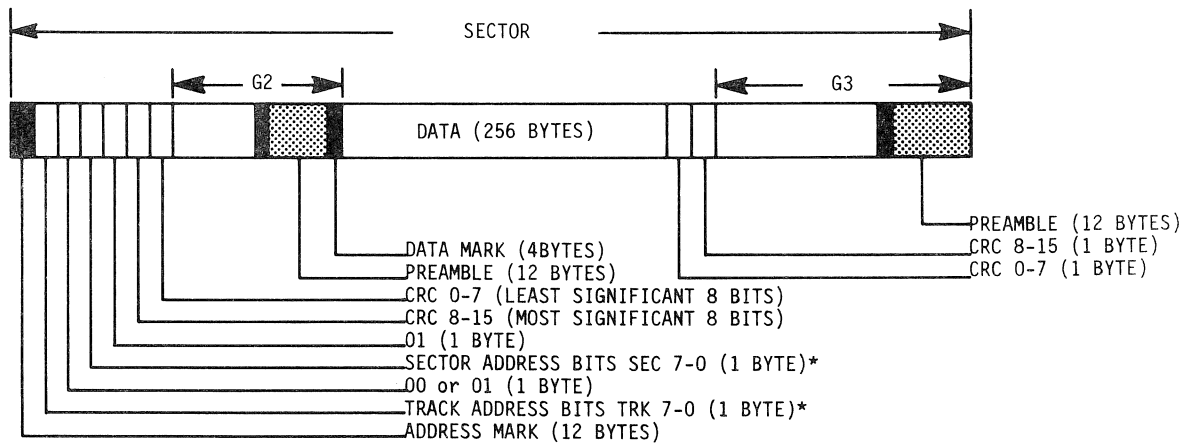
G2= 16 BYTES HEX FF  
 6 BYTES HEX 00

G3= 27 BYTES HEX FF  
 6 BYTES HEX 00

G4=314 BYTES HEX FF  
 6 BYTES HEX 00

\*BIT 7 IS THE MOST SIGNIFICANT BIT

### Single Density



GAP FIELDS

G1= 52 BYTES HEX 4E  
 12 BYTES HEX 00

G2= 22 BYTES HEX 4E  
 12 BYTES HEX 00

G3= 54 BYTES HEX 4E  
 12 BYTES HEX 00

G4=628 BYTES HEX 4E  
 12 BYTES HEX 00

\*BIT 7 IS THE MOST SIGNIFICANT BIT

### Double Density

### 3 OPERATOR'S GUIDE

#### 3-5 DISKETTE INITIALIZATION

The single and double density formats for diskette initialization are presented in this section.

Data is represented by 8-bit bytes. Clock and data bits have a value of either one or zero. The presence of magnetic flux transition represents a binary one and the absence of a transition represents a binary zero. Clock bits are binary one unless otherwise noted. The single density initialization format (provided in the table below) uses a frequency modulation encoding scheme whereby each data bit is preceded by a clock bit. The double density format (provided in the table on the opposite page) uses a modified frequency encoding scheme, whereby a clock bit is only provided at the beginning of bit cell time for a binary zero preceded by a binary zero.

The following initialization data is used to initialize all tracks on single density diskettes, and Track 0 on double density diskettes. Starting immediately after index, write the bytes in frequency modulation coding.

WHEN WRITTEN	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN	REMARKS
Write this field once at start of the track.	40	FF	Index Mark -- This byte has a clock bit pattern of HEX D7; Data bit pattern of HEX FC
	6 1	00 FC	
Write this field once for each sector on the track (26 times).	26	FF	Read Preamble Address Mark -- This byte has a data bit pattern of HEX FE; clock bit pattern of HEX C7 Track Address  Sector Address -- This byte is 01 the first time written, 02 the second time, etc., and 1A the last time.  Computed CRC bits 15-0 for address field being written -- See note 1 below.  Read Preamble Data Mark -- This byte has a data bit pattern of HEX FB; clock bit pattern of HEX C7 Data Bytes CRC bytes -- See note 2 below.
	6	00	
	1	FE	
	1	XX	
	1	00	
	1	XX	
	1	00	
	2	XX	
	11	FF	
	6	00	
	1	FB	
Write once at end of track.	128	00	The length of this field can vary due to timing tolerances.
	2	XX	
	27	FF	
NOTE 1: Determine the value of these 2 bytes by computing the cyclic redundancy check characters for the preceding 5 bytes, using the following checking polynomial: $x = 1 + x^5 + x^{12} + x^{16}$ Prior to computing the CRC bytes, initialize the accumulating register to all ones.			
NOTE 2: Same as NOTE 1 except change 5 bytes to 129 bytes.			

The following double density format is used to initialize tracks 1 through 76 for double density diskettes (the single density format provided in the preceding Table is always used on Track 0). To initialize all sectors of tracks 1 through 76, start immediately after index and write the following bytes in modified frequency modulation coding. The procedure is repeated for each track on the diskette.

WHEN WRITTEN	NUMBER OF BYTES	HEX VALUE OF BYTES WRITTEN	REMARKS
Write this field once at the start of the track.	80	4E	Read Preamble  These 3 bytes are missing clock transitions between bits 3 and 4. These 4 bytes are the Index Mark.
	12	00	
	3	C2	
	1	FC	
	50	4E	
Write this field once for each sector on the track (26 times)	12	00	Read Preamble
	3	A1	These bytes are missing clock transitions between bits 4 and 5.
	1	FE	These 4 bytes are the Address Mark.
	1	XX	Track Address -- XX = Cylinder number
	1	00	Sector Address -- XX =01 the first time written, 02 the second time, etc., and 1A the last time.
	1	XX	
	1	01	CRC bytes -- see note 1 below
	2	XX	
	22	4E	
	12	00	
	3	A1	These bytes missing data transitions between bits 4 and 5. These 4 bytes
	1	FB	These 4 bytes are the Data Mark.
	256	00	Data bytes
	2	XX	CRC bytes -- see note 2 below
54	4E		
Write this field once at the end of each track.	598	4E	The length of the field can vary due to timing tolerances.
<p>NOTE 1: Determine the value of these 2 bytes by computing the cyclic redundancy check characters for the preceding 8 bytes using the following checking polynomial;</p> $X = 1 + X^5 + X^{12} + X^{16}$ <p>Prior to computing the CRC bytes, initialize the accumulating register to all ones.</p> <p>NOTE 2: Same as NOTE 1 except change 8 bytes to 260 bytes.</p>			

### 3 OPERATOR'S GUIDE

#### 3-6 DISK STATUS SIGNAL DESCRIPTION

When CPU bit 6 is set HIGH (False) the Double Density Controller presents disk status on the DIO through D17 data lines (connector J1, pins 9 through 16).

A description of the status signals follows:

STATUS SIGNAL	DESCRIPTION
DELETED DATA MARK (Bit 7)	This bit is tested after each read command. A "ONE" at this bit indicates that a Deleted Data Mark has been found at the beginning of the data field of the sector being read. This status, as well as CRC Error Status, must be tested following read operations, but prior to any "CLEAR" or "CLEAR ERROR FLAG" commands. The "CLEAR" or "CLEAR ERROR FLAG" command may then be used to reset this bit and the CRC Error bit.
MEDIA STATUS (Bit 6)	This bit is always a "ONE" for the Double Density Disk system.
DRIVE FAIL (Bit 5)	This bit is a "ZERO" if all the following conditions exist: <ul style="list-style-type: none"><li>• The selected drive is up to speed.</li><li>• The diskette is seated properly.</li><li>• The door is closed.</li></ul> The system should not attempt a data transfer to a drive that is not ready.
WRITE PROTECT (Bit 4)	This bit is set to a "ONE" if the selected drive contains a write protected diskette. This condition should not be tested if the selected drive has a "DRIVE FAIL" status.
CRC ERROR (Bit 3)	This bit is a "ONE" when an error has occurred during the previous command. This bit must be tested after all read, write, or seek operations. If this bit is True, it must be reset after both the "DELETED DATA MARK" and "CRC ERROR" status bits have been checked. Further commands will not be performed unless the "CRC ERROR" status is reset by either a "CLEAR" or "CLEAR ERROR FLAG" command

STATUS SIGNAL	DESCRIPTION
UNIT SELECT (Bits 2 and 1)	These two bits contain the address of the drive currently being selected by the controller.
BUSY (Bit 0)	This bit is set to "ONE" when a read, write, or seek command is sent to the controller. No commands other than "EXAMINE STATUS" commands may be sent to the controller while the controller is busy (with the exception of the "CLEAR" command).

3 OPERATOR'S GUIDE

3-7 COMMAND SET

The Double Density controller receives commands on the CPU 0 through CPU 7 data lines of connector J1 (pins 30 through 37). The table on the following page describes each of these commands, showing CPU bit settings, hexadecimal (HEX) codes, and whether or not the controller is "BUSY" (head in contact with diskette) when a specific command is issued.



COMMAND SET

COMMAND	CPU BIT (ZERO TRUE) SET								BUSY	HEX CODE
	7	6	5	4	3	2	1	0		
EXAMINE STATUS	0	0	0	0	0	0	0	0	No	00
READ	0	0	0	0	0	0	1	1	Yes	0B
WRITE	0	0	0	0	0	1	0	1	Yes	06
READ CRC	0	0	0	0	0	1	1	1	Yes	07
SEEK	0	0	0	0	1	0	0	1	Yes	09
CLEAR ERROR FLAGS	0	0	0	0	1	0	1	1	No	0B
SEEK TRACK ZERO	0	0	0	0	1	1	0	1	Yes	0D
WRITE DELETED DATA MARK	0	0	0	0	1	1	1	1	Yes	0F
LOAD TRACK ADDRESS	0	0	0	1	0	0	0	1	No	11
LOAD UNIT/SECTOR	0	0	1	0	0	0	0	1	No	21
LOAD WRITE BUFFER	0	0	1	1	0	0	0	1	No	31
EXAMINE READ BUFFER	0	1	0	0	0	0	0	0	No	40
SHIFT READ BUFFER	0	1	0	0	0	0	0	1	No	41
CLEAR CONTROLLER	1	0	0	0	0	0	0	1	No	81
LOAD CONFIGURATION	0	0	0	1	0	1	0	1	No	15

3 OPERATOR'S GUIDE

3-8 NON-OPERATIONAL COMMANDS DESCRIPTION

In this section are the commands for loading Track, Unit, and Sector information into their respective registers, and the commands used to place status information on the Data In lines. Also discussed are three commands used to transfer data to the controller write or read buffer. When using these three commands, transfers should be continuous, i.e., no other commands should be issued to the controller until either 128 (single density) or 256 (double density) bytes of data have been transferred. The command codes within the parenthesis are in HEX notation.

COMMAND	DESCRIPTION																								
EXAMINE STATUS (00)	<p>This command causes status information to be placed on the Data In lines. The controller does not go busy. The Input Word is available within 200 nano-seconds after the CPU bit 6 interface command signal is set to the "ZERO" (HIGH) state.</p> <table border="1"> <tr> <td>DELETED DATA MARK</td> <td>1</td> <td>DRIVE FAIL</td> <td>WRITE PROTECT</td> <td>CRC ERROR</td> <td>UNIT CODE BIT 1</td> <td>UNIT CODE BIT 0</td> <td>BUSY</td> </tr> <tr> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td colspan="8" style="text-align: center;">DI LINES</td> </tr> </table>	DELETED DATA MARK	1	DRIVE FAIL	WRITE PROTECT	CRC ERROR	UNIT CODE BIT 1	UNIT CODE BIT 0	BUSY	7	6	5	4	3	2	1	0	DI LINES							
DELETED DATA MARK	1	DRIVE FAIL	WRITE PROTECT	CRC ERROR	UNIT CODE BIT 1	UNIT CODE BIT 0	BUSY																		
7	6	5	4	3	2	1	0																		
DI LINES																									
LOAD TRACK ADDRESS (11)	<p>Track Address on the CDU 0 through CDU 7 lines is loaded into the "Seek Track" register in the controller.</p> <table border="1"> <tr> <td>TRK 7 MSB</td> <td>TRK 6 MSB</td> <td>TRK 5</td> <td>TRK 4</td> <td>TRK 3</td> <td>TRK 2</td> <td>TRK 1</td> <td>TRK 0 LSB</td> </tr> <tr> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td colspan="8" style="text-align: center;">CDO LINES</td> </tr> </table>	TRK 7 MSB	TRK 6 MSB	TRK 5	TRK 4	TRK 3	TRK 2	TRK 1	TRK 0 LSB	7	6	5	4	3	2	1	0	CDO LINES							
TRK 7 MSB	TRK 6 MSB	TRK 5	TRK 4	TRK 3	TRK 2	TRK 1	TRK 0 LSB																		
7	6	5	4	3	2	1	0																		
CDO LINES																									
LOAD UNIT/SECTOR (21)	<p>The unit and sector information is loaded into their respective registers from the CDU 0 through CDU 7 lines.</p> <table border="1"> <tr> <td>UNIT CODE BIT 1</td> <td>UNIT CODE BIT 2</td> <td>"0"</td> <td>SEC 4 MSB</td> <td>SEC 3</td> <td>SEC 2</td> <td>SEC 1</td> <td>SEC 0 LSB</td> </tr> <tr> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td colspan="8" style="text-align: center;">CDO LINES</td> </tr> </table>	UNIT CODE BIT 1	UNIT CODE BIT 2	"0"	SEC 4 MSB	SEC 3	SEC 2	SEC 1	SEC 0 LSB	7	6	5	4	3	2	1	0	CDO LINES							
UNIT CODE BIT 1	UNIT CODE BIT 2	"0"	SEC 4 MSB	SEC 3	SEC 2	SEC 1	SEC 0 LSB																		
7	6	5	4	3	2	1	0																		
CDO LINES																									

NOTE

DI 6 (EXAMINE STATUS) and CDO 5 (LOAD UNIT SECTOR) are reserved for use in two sided disk systems.

COMMAND	DESCRIPTION																								
LOAD WRITE BUFFER (31)	<p>Write data is loaded into the Write Data Buffer register*</p> <table border="1"> <tr> <td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td> </tr> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> </table> <p>CDO LINES</p>	DO	DO	DO	DO	DO	DO	DO	DO	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
DO	DO	DO	DO	DO	DO	DO	DO																		
7	6	5	4	3	2	1	0																		
7	6	5	4	3	2	1	0																		
EXAMINE READ BUFFER (40)	<p>Read Data is placed on the Data In lines.*</p> <table border="1"> <tr> <td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td><td>DO</td> </tr> <tr> <td></td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> </table> <p>DI LINES</p>	DO	DO	DO	DO	DO	DO	DO	DO		6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
DO	DO	DO	DO	DO	DO	DO	DO																		
	6	5	4	3	2	1	0																		
7	6	5	4	3	2	1	0																		
SHIFT READ BUFFER (41)	<p>The Read Buffer is shifted, to place the next Read Data character on the Data In lines.*</p>																								
LOAD CONFIGURATION REGISTER (15)	<table border="1"> <tr> <td>0</td><td>0</td><td>FORMAT MODE</td><td>DOUBLE DENSITY</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> </table> <p>CDO LINES</p> <p>This command conditions the controller in the following manner (note that this command does not set the "Busy" signal True):</p> <p>BITS 0, 1, 2, 3, 6 and 7 must be set to zero. These bits are reserved for use in double sided disk systems.</p> <p>BIT 4 is False to indicate single density and True to indicate double density. This bit must be set properly prior to a seek, write, or read operation. It is not necessary to change this bit if the next operation is the same density. This bit must be set True when doing a seek from track zero in double density. Note that in double density recording formats, track zero is recorded in single density. It is therefore necessary to reset this bit to single density when reading or writing on track zero of double density formatted diskettes.</p> <p>BIT 5 is False to indicate normal operation and True to indicate "Format" mode. In the "Format" mode, a "WRITE" command is interpreted by the controller as a "Format Single Track" command. With the controller in the "Format" mode, a "SEEK" command is performed (when issued) without reading the track header information on the diskette. It is therefore possible to perform a series of "WRITE" and "SEEK" commands to the controller with the controller in the "Format" mode. This sequence may be used to format the entire diskette. Remember that BIT 4 must be "ZERO" when formatting Track Zero.</p>	0	0	FORMAT MODE	DOUBLE DENSITY	0	0	0	0	7	6	5	4	3	2	1	0								
0	0	FORMAT MODE	DOUBLE DENSITY	0	0	0	0																		
7	6	5	4	3	2	1	0																		

\* These three commands are modified when using a Pertec-supplied interface board. Refer to the appropriate interface board specifications for details.

### 3 OPERATOR'S GUIDE

#### 3-9 OPERATIONAL COMMANDS DESCRIPTION

The following description explains the functional characteristics of the controller command operational sequence. It may be used as a guide in developing disk system application software. The command code (in parentheses following the command) is in HEX notation.

##### SEEK OPERATION

The Seek command (09) is used to change tracks on a disk. The Double Density Disk system reads the present track location of the disk drive being read, and compares the actual and desired track address. The disk drive head is stepped in the appropriate direction until it aligns with the desired track. Then, the track is read to verify its location. If the head is at its correct location, this Seek operation is completed.

Seek operations are necessary only to change tracks. To change sectors, the Load Unit/Sector command (21) is used.

##### SEEK TRACK ZERO

A Seek Track Zero command (0D) should always be used to position the head on Track 0. A Seek Track Zero command is used to seek to track zero regardless of the present track. A transfer of the track address is not required.

##### READ OPERATION

When the head is positioned on the desired track using the Seek command, a Unit/Sector command is executed to select the sector to be read.

On the standard IBM format diskette, sector one is positioned just following the index hole and sector 26 just before the index hole.

The Double Density Controller systems Cyclic Redundancy Check (CRC) computes information automatically during read operations, and if an error is detected, the CRC status bit is set at the end of a read operation.

Data is shifted into the read buffer at 500 bits per second rate (double density) from the sector. Upon completion of a Read command, the first character of the sector is at the front of the read buffer. An Examine Read Buffer command (40) places the buffer output on the Data In lines (DI 7-0).

When the Shift and Read Buffer commands are executed, the read buffer is shifted and the next read data byte is placed on the Data In lines.

The Read CRC command (07) tests CRC on the data field. This command is used following a Write operation to ensure data integrity. After all read operations the CRC Error bit and the Deleted Data Mark bit should be tested. If either bit is set True, the Clear command should be issued.

## WRITE OPERATION

Write command operations write the contents of the write buffer to the desired track and sector of the selected unit.

After the write buffer is loaded using the Load Write Buffer command (31), the Seek command will move the head to the desired track. Then, the system will begin searching for the correct sector.

A field of six bytes consisting of all logical zeros, is now written ahead of the intended location of the data sector.

The data that was written should then be read by issuing a Read CRC command to ensure validity of the Write operation.

## WRITE DELETED DATA MARK

If an error persists after rereading the data as specified in Section 1-2, the Deleted Data Mark command (0F) should be issued and the write data will be preceded by a Deleted Data Mark. When reading, this mark indicates that this sector should be ignored.

## CLEAR

The Clear command (81) resets the controller electronics. If the controller is busy, the BUSY status will be reset, the head will be unloaded (removed from contact with the diskette) and the DONE signal will be pulsed.

## CLEAR ERROR FLAGS

A Clear Error Flags command (0B) clears the Deleted Data Mark status bit and the CRC Error status bit.



SECTION 4  
THEORY OF OPERATION

## 4 THEORY OF OPERATION

### 4-1 INTERFACE

The controller interface circuitry is discussed in this section. Refer to sheet 2 of the Double Density Controller schematic diagrams in Appendix B.

A description of the interface circuitry begins with the 8 CPU lines, CPU 0 through CPU 7. The CPU lines carry the commands from the CPU to the controller. They are then buffered through an 8-bit inverting buffer, U129 and brought to the Programmable Read Only Memory (PROM) in U119. Different addresses at the input to this PROM produce outputs which perform various commands within the controller. The command Load Unit/Sector (NLDSEC) is decoded at U119 pin 2 and brought through gate U114. This generates the clock to load the Unit/Sector Register. U119 pins 3 and 4 are decoded in similar fashion to supply clock signals NLDCONFIG (Load Configuration) and NLDTRK (Load Track). NLDCONFIG clocks the Load Configuration register, U125 (sheet 12) and NLDTRK clocks the Seek Track Register, U58 (sheet 4).

There are three outputs of the PROM which result in the command signals CMD 0, CMD 1, and CMD 2 at the output of 6-bit register, U118. The outputs at pins 5 through 8 of U119 are essentially condensed into these three command status signals which provide to the main control logic the command the controller is to perform.

At the beginning of a new command, flip-flops U92 generate a strobe pulse to U118. Flip-flop U93 is set at the beginning of a command and reset at the end of a command, producing the BUSY signal. The BUSY signal is sent out to the status register and monitored by the system while a command is in process.



## 4 THEORY OF OPERATION

### 4-2 MAIN CONTROL

The main control circuitry is discussed in this section. Refer to sheet 3 of the Double Density Controller schematic diagrams in Appendix B.

Three ICs, U63, U64 and U71 make up the Program Counter. At the various counts of the Program Counter, different operations are performed; that is, either a jump operation to a different program count, or a particular Input/Output (I/O) command. The output of the program counters are then brought to the PROM in U72 and U73. The outputs from the PROM are gated through U79, U81, U82 and U102, and latched at U53 and U54. Each output line from this pair of latches performs a specific function within the controller.

The controller will increment through the program count unless a specific jump operation is encountered. A jump operation is conditional; that is, a selected flag must be either True or False, as required by the program, to cause a jump to occur. Flags are selected by three Flag Multiplexers, U42, U43 and U44. These Flag Multiplexers have as inputs the various status conditions throughout the controller (such as, INDEX, BUSY, etc.,) allowing different jump operations to occur when these conditions are encountered.

A Timer, made up of U51, U52, U61 and U62, is also loaded by the output of PROMS U72 and U73. The Timer allows different timing loops to be done by the controller. For instance, the Timer will time out 128-bytes when a Read or Write operation is being performed.

## 4 THEORY OF OPERATION

### 4-3 CODE GENERATOR AND TRACK COMPARATOR

The code generator and track comparator circuitry is discussed in this section. Refer to sheet 4 of the Double Density Controller schematic diagrams in Appendix B.

The output signals CODESEL 0 through CODESEL 4 (Code Select 0 through 4) from the main control circuit (sheet 3) are used to address the PROM, U56. The output of U56 selects either another PROM, or one of two buffers to allow different items of information to be placed on the Data Code Bus (DCODE 0 through DCODE 7). The code select lines are also connected to the PROM in U57.

The Data Code Bus contains the information to be serialized and written onto the diskette. The Data Code Bus consists of any information that goes within the header; such as, Track Address, Sector Number and the Sector Length Code.

Boundary Codes (BCODE 0 through BCODE 7) are required between Data Codes. The Boundary Codes are presented by PROM, U57 to the Boundary Code Bus for serialization.

Read Data from the Read Data Comparator circuit (sheet 10) is presented to the Current Track Register, U36 and U37. The Current Track Register contains the address of the track that the Drive Head is currently positioned on. The output of U36 and U37 is input to Comparators, U38 and U48. These Comparators determine the direction the head positioning stepper motor should move the Drive Head during a Seek operation. The Comparators then input the Seek Track Register, U58 providing the track/cylinder address to which the head will be moved during the next seek operation.

## 4 THEORY OF OPERATION

### 4-4 WRITE ENCODER

The Write Encoder circuitry is explained in this section. Refer to sheet 6 of the Double Density Controller schematic diagrams in Appendix B.

The BCODE 0 through BCODE 7 (Boundary Code Bus) signals (from sheet 4) are brought into shift register U95, and the DCODE 0 through DCODE 7 (Data Code Bus) signals (also from sheet 4) are brought into shift register, U96 in like manner. The Boundary and Data Codes appear in serial form (SERCODES) at U96 pin 13 and are applied to Data Selector, U83 pins 2 and 3. At the proper time (determined by the Main Control logic on sheet 3) the Data Selector selects either the SERCODES, the incoming Write Data from U84, or the CRCOUT (Cyclic Redundancy Check Output) data to be written on the diskette.

The schematic diagram for the CRC Register is supplied on sheet 8 of Appendix B. The CRC Register simply looks at the Write Data lines during a Write operation, and introduces this data through some Exclusive OR gates (U40) to the CRC Registers, U49 and U50 (sheet 8 of the Double Density Controller schematics). The CRC Output (CRCOUT) is then brought to Data Multiplexer, U83 (schematic sheet 6) to be serialized and added to the end of the data field.

The circuit comprised of U94 and U105 (sheet 6) generates the correct encoded data schemes for either the MFM (Modified Frequency Modulation) coding technique used in double density or the Double Frequency coding technique used in single density operations.

## 4 THEORY OF OPERATION

### 4-5 WRITE BUFFER AND SYSTEM CLOCK

The Write Buffer and System Clock circuitry is discussed in this section. Refer to sheet 5 of the Double Density Controller schematic diagrams in Appendix B.

The Write Data (WDO through WD7) signals originate from the CDO 0 through CDO 7 signals being transmitted from the interface card to the controller. Data coming into the controller on the CDO 0 through CDO 7 data lines is written into Buffer Memories, U85 and U86. Two counters U77 and U87 increment the address of U85 and U86 each time data is transmitted to the controller. Then, when it is time to write the data to the disk, the Write Data is transmitted to the WDO through WD7 Write Data lines.

The system clock is actually two clocks. The NSYSCLK 2 clock is the System Write Clock, generated by Counter U35 and Crystal Oscillator, U6. The crystal generated clock is used during write and step timing operations. The NSYSCLK 1 clock is generated by the Read Clock (RCLK) which is a signal derived from the Phase Lock Loop circuit when reading data back from the diskette. The phase lock loop is explained in section 4-7.

## 4 THEORY OF OPERATION

### 4-6 WRITE COMPENSATION

The write compensation circuitry is explained in this section. Refer to sheet 7 of the Double Density Controller schematic diagrams in Appendix B.

The output signal, WTRANS (from sheet 6) represents serialized data to be written on the disk in either single density or double density format. For single density format, the WTRANS signal is gated with the system clock (SYSCLK 1) and DDS (Double Density Status False) at U14. It then strobes the IWDA (Interface Write Data) signal to the drive.

For double density operation, the WTRANS signal is input to shift register, U25. The shift register is shifted by the system clock (NSYSCCK 2) at U25 pin 8. The shift register, in conjunction with the PROM in U15, modifies the exact position of the right data pulses to compensate for peak shift characteristics on the diskette. The function of the shift register and the PROM is to shift the write data pulses farther apart to compensate for the peak shifting effect.

## 4 THEORY OF OPERATION

### 4-7 DATA SEPERATOR PHASE LOCK LOOP CONTROL

The Phase Lock Loop which begins the discussion of the read circuitry is described in this section. Refer to sheet 9 of the Double Density Controller schematic diagrams supplied in Appendix B.

One component of the Phase Lock Loop is a variable frequency oscillator. The phase and frequency of the oscillator is controlled by an incoming data stream from the diskette. The Oscillator signal generated has a phase relationship that is constant with respect to the data coming off the diskette. This allows data decoding of pulses off the diskette having various pulse spacings.

The variable control oscillator is made up of transistor Q2, serving as a constant current source to charge capacitors C6 and C7. This results in a ramp voltage which is compared, at comparator U1, to a reference voltage set up by R4 and R3. When this reference voltage is exceeded by the ramp voltage charging from 0 to 3 volts, the output of the comparator turns off the ramp voltage by enabling U2. When U2 is enabled, the charge is pulled off C6 and C7, bringing the ramp voltage back to zero, thus, providing an oscillator circuit.

The resultant output of the oscillator is used as the PLO (Phase Loop Oscillator) signal. This is the basis of the Phase Loop clock.

The charging rate of capacitors C6 and C7 is controlled by the bias voltage set up at test point 1 (TP1). This voltage is in turn set up by control signals at U11 pins 3 and 6. These are called phase correction signals.

There are three signals, Phase A ( $\emptyset A$ ), Phase B ( $\emptyset B$ ) and Read Pulse Wide (RPW). RPW is a one-shot pulse that is fired with every data transition brought from the disk into the controller. The Read Data signal (IRDA) is input at connector J2 pin 46, shown in the upper right hand corner of the schematic. The  $\emptyset A$  and  $\emptyset B$  signals are generated by flip-flop U33. Flip-flop U33 is clocked by the output of counter U31 which is in turn clocked by the Phase Loop Oscillator clock (NPL0). U33 is comparing that Phase Loop Oscillator clock with the one-shot pulse generated from the Read Data (IRDA) at U22. Thus, the  $\emptyset A$  and  $\emptyset B$  signals represent the results of that comparison.  $\emptyset A$  and  $\emptyset B$  signals, in conjunction with the RPW signal, are used to generate the correction signals at U11 (in the lower left corner of the schematic).

The Phase Loop Oscillator clock (NPL0) is used to decode the data coming from the diskette. Since the NPL0 clock is in phase with, synchronous to, and at the same frequency as the read data, it can be used to determine if the pulses coming from the diskette are either 2, 3, or 4 microseconds wide. With every read data pulse from the diskette, one-shot U22 is triggered for 500 nanoseconds. This 500 nanosecond signal (designated RPN) is brought into flip-flop U23 which is changing states with every transition (toggling). Every state change is clocked into two flip-flops in series (U69) by the system clock NSYSCLK 1. The system clock is derived from the Phase Lock

Loop. In response to the signal at U69 pin 2, the output of U69 has a transition only on the edge of the clock pulse at pin 3. Thus, at this point the data is synchronized with the Phase Lock Loop.

The actual data decoding is done using the two flip-flops, U69 and the Exclusive OR gate, U40 to generate the TDATA (Transition Data) signal. The transition data is a HIGH level when a transition has occurred and a LOW level when a transition has not occurred. Now the signal TDATA and the signal RCLK (Read Clock, derived from the Phase Lock Loop clock) are used to represent a separated clock and data to further decode specific data from the disk.

## 4 THEORY OF OPERATION

### 4-8 READ DATA COMPARATOR

This section contains an explanation of the read data comparator circuit. Refer to sheet 10 of the Double Density Controller schematic diagrams in Appendix B.

The TDATA (Transition Data from sheet 9) signal is introduced to the Read Data Comparator circuitry at shift register U29. U29 and U19 are tied together to form a 16-bit shift register which provides a 16-bit parallel word that is monitored by a series of comparators. These comparators are made up of U26, U27, U20, U9, U16, U17, U18 and U28.

In addition to looking for data marks and header information, the 16-bits of serial data must be decoded. Since there is always a data bit and a boundary bit relationship for the data coming from the diskette, every other line is picked up as an output. These output signals are designated RDO through RD7.

Input into the other side of the comparators are the BCODE (Boundary Code) and DCODE (Data Code) lines which are derived from control signals set up by the main control logic (these codes were first discussed in sections 4-3 and 4-4). These comparators tests for specific data patterns, track address or sector address from the main control appearing on these data lines. Two output signals from the comparators, COMPARE and DECOMP, are brought back to the main control logic. The third output is the DDMF (Deleted Data Mark) signal which checks for the deleted data marks.



## 4 THEORY OF OPERATION

### 4-9 READ BUFFER

The read buffer circuitry is discussed below. Refer to sheet 11 of the Double Density Controller schematic diagrams in Appendix B.

The read data signals (RD0 through RD7) are introduced to a buffer, U109. The signals from this buffer are output to two memory chips U98 and U99. The read buffer addresses are controlled by 4-bit counters, U90 and U100. These counters are used to set up a specific address, allowing a maximum 256 bytes per sector to be stored in the buffers. When data is to be transferred out of the interface during a Read Buffer operation, the data is sent from the memory chips to the 8-bit buffer, U108.

Status signals FDDAM (Deleted Data Mark Found) and CRCER (CRC Error) are latched at U106 pins 15 and 11, respectively. These two status signals, as well as all other status signals, are then brought to the Status Buffer, U107. Both Buffers, U107 and U108, output to Data In lines (DIO through DI7). Thus, DIO through DI7 may provide either read data or status information to the system.

## 4 THEORY OF OPERATION

### 4-10 DRIVE INTERFACE

The Drive Interface circuitry is described below. Refer to sheet 12 of the Double Density Controller schematics in Appendix B.

An 8-bit register U125 is used to latch specific configuration information for the controller. There is one unique command which configures the controller for such functions as formatting status, double density status, or controlling the BUSY light or the drive motor enable (in the case of DC motors).

The power supply enable (PSEN) generator circuit is made up of Q2 and the associated components towards the center of the schematic, and is utilized as a "POWER ON" clear.

The Index Counter, U126 counts the Index pulses (INDX). If any operation should cause the controller to stay busy for more than 16 Index pulses, it will generate a CRC Error condition (NSCRC) and reset the controller. This prevents the controller from hanging up indefinitely.

SECTION 5  
TROUBLESHOOTING

5 TROUBLESHOOTING

5-1 GENERAL PROBLEMS

Some general problems that may be encountered when using the Double Density Disk system are defined below. This section is designed to help determine if the controller, drive, cables, etc., are causing the malfunction.

PROBLEM	POSSIBLE CAUSES
Power not reaching unit (Power light not on in FD3812 system).	<ul style="list-style-type: none"> <li>● No AC Power (not plugged in).</li> <li>● Blown Line Fuse (rear of unit).</li> <li>● Incorrect AC voltage (220V and should be 110V, etc.).</li> <li>● Problem is within the unit.</li> </ul>
Power is reaching unit but the system does not respond to commands (Power light ON on FD3812 system).	<ul style="list-style-type: none"> <li>● Incorrect I/O cable connection.</li> <li>● Open power supply cable.</li> <li>● Drive to controller cable is open.</li> <li>● Wrong interface board being used.</li> </ul>
One drive functions but another drive does not.	<ul style="list-style-type: none"> <li>● Defective drive.</li> <li>● Open power supply cable.</li> <li>● Open drive to controller cable.</li> </ul>
Both drives appear to function but will not read a particular diskette.	<ul style="list-style-type: none"> <li>● Defective diskette.</li> <li>● Check density of diskette.</li> <li>● Diskette not loaded properly.</li> <li>● Defective drive to controller cable.</li> <li>● Defective controller.</li> <li>● Controller has been issued an invalid sector or cylinder word.</li> <li>● Controller bus has issued incorrect density status.</li> </ul>

PROBLEM	POSSIBLE CAUSES
Diskette is read on one drive but not the other.	<ul style="list-style-type: none"> <li>● Defective drive.</li> <li>● Defective drive to controller cable.</li> </ul>
Controller does not respond properly with known good diskette in drive.	<ul style="list-style-type: none"> <li>● Controller has been issued an invalid sector or cylinder word.</li> <li>● Controller has been issued incorrect density status.</li> <li>● Defective controller.</li> <li>● Program Error</li> </ul>



APPENDIX A  
DOUBLE DENSITY CONTROLLER  
PARTS LIST

QUANTITY FD3812 FF38-XX		PART NUMBER	DESCRIPTION	REFERENCE
1	1	250142-01	Integrated Circuit PROM, 512 x 8	U73
1	1	250142-02	Integrated Circuit PROM, 512 x 8	U72
1	1	250140-01	Integrated Circuit PROM, 256 x 4	U15
1	1	250141-01	Integrated Circuit PROM, 32 x 8	U47
1	1	250141-02	Integrated Circuit PROM, 32 x 8	U57
1	1	250141-03	Integrated Circuit PROM, 32 x 8	U56
1	1	250141-04	Integrated Circuit PROM, 32 x 8	U119
1	1	400-0306	Integrated Circuit	U1
1	1	400-0318	Integrated Circuit, OP-AMP	U12
1	1	700-4123	Integrated Circuit	U22
1	1	700-5452	Integrated Circuit	U2
1	1	700-7400	Integrated Circuit	U11
4	4	700-7416	Integrated Circuit	U8, 123, 124,127
1	1	700-7438	Integrated Circuit	U122
1	1	700-7404	Integrated Circuit	U7
4	4	702-2112	Integrated Circuit, 256 X 4 MOS Memory	U85, 86, 98, 99
1	1	710-4145	Integrated Circuit	U66
2	2	710-4153	Integrated Circuit	U32, 83
14	14	710-4161	Integrated Circuit	U31, 35, 52, 61, 62, 63, 64, 71, 74, 77, 87, 90, 100



QUANTITY FD3812 FF38-XX		PART NUMBER	DESCRIPTION	REFERENCE
3	3	710-4164	Integrated Circuit	U19, 25, 29
3	3	710-4166	Integrated Circuit	U84, 95, 96
2	2	710-4174	Integrated Circuit	U94, 118
5	5	710-4191	Integrated Circuit	U36, 37, 55, 65, 126
2	2	710-4221	Integrated Circuit	U89, 92
5	5	710-4251	Integrated Circuit	U41, 42, 43, 44, 105
6	6	710-4273	Integrated Circuit	U49, 50, 53, 54, 58, 125
7	7	710-7400	Integrated Circuit	U39, 68, 79, 82, 103, 112, 114
7	7	710-7402	Integrated Circuit	U3, 59, 80, 88, 104, 113, 116
3	3	710-7404	Integrated Circuit	U24, 78, 102
3	3	710-7410	Integrated Circuit	U14, 67, 81
1	1	710-7451	Integrated Circuit	U5
4	4	710-7474	Integrated Circuit	U69, 70, 91, 76
8	8	710-7476	Integrated Circuit	U4, 23, 33, 34, 60, 93, 101, 106

QUANTITY FD3812 FF38-XX		PART NUMBER	DESCRIPTION	REFERENCE
11	11	710-7485	Integrated Circuit	U9, 16, 17, 18, 20, 26, 27, 28, 38, 48, 117
1	1	710-7486	Integrated Circuit	U40
4	4	710-4240	Integrated Circuit	U75, 107, 108, 129
3	3	710-4244	Integrated Circuit	U45, 46, 109
1	1	100-2205	Resistor, 22 OHMS, 5%, $\frac{1}{4}$ W	R38
2	2	100-1015	Resistor, 100 OHMS, 5%, $\frac{1}{4}$ W	R6, R44
1	1	100-1025	Resistor, 1K OHMS, 5%, $\frac{1}{4}$ W	R32
2	2	100-1515	Resistor, 150 OHMS, 5%, $\frac{1}{4}$ W	R11, R37
2	2	100-1815	Resistor, 180 OHMS, 5%, $\frac{1}{4}$ W	R1, R39
2	2	100-2215	Resistor, 220 OHMS, 5%, $\frac{1}{4}$ W	R15, R25
1	1	100-2225	Resistor, 2.2K OHMS, 5%, $\frac{1}{4}$ W	R16
1	1	100-3305	Resistor, 33 OHMS, 5%, $\frac{1}{4}$ W	R7
2	2	100-3315	Resistor, 330 OHMS, 5%, $\frac{1}{4}$ W	R13, R23
2	2	100-4725	Resistor, 4.7K OHMS, 5%, $\frac{1}{4}$ W	R10
1	1	100-6805	Resistor, 68 OHMS, 5%, $\frac{1}{4}$ W	R10
1	1	200-4715	Resistor, 470 OHMS, 5%, $\frac{1}{4}$ W	R45

QUANTITY FD3812 FF38-XX		PART NUMBER	DESCRIPTION	REFERENCE
1	1	101-1815	Resistor 180 OHMS, 5%, 1/2W	R26
1	1	103-2215	Resistor, 220 OHMS, 5%, 2W	R27
2	2	107-1000	Resistor, 100 OHMS 1%, 1/8W	R5, R44
2	2	107-1212	Resistor, 12.1K OHMS 1%, 1/8W	R12, 22
1	1	107-1213	Resistor, 121K OHMS, 1%, 1/8W	R18
1	1	107-1330	Resistor, 330 OHMS, 1%, 1/8W	R8
1	1	107-1961	Resistor, 1.96K OHMS, 1%, 1/8W	R36
1	1	107-2150	Resistor, 215 OHMS, 1%, 1/8W	R21
4	4	107-2151	Resistor, 2.15K OHMS, 1%, 1/8W	R14, 24, 34, 35
1	1	107-2152	Resistor, 21.5K OHMS, 1% 1/8W	R17
1	1	107-2612	Resistor, 261K OHMS, 1%, 1/8W	R19
1	1	107-5110	Resistor, 511 OHMS, 1%, 1/8W	R4
2	2	107-6810	Resistor, 681 OHMS, 1% 1/8W	R3, 9
1	1	107-7500	Resistor, 750 OHMS, 1%. 1/8W	R20
1	1	107-3161	Resistor, 3.16K OHMS, 1%, 1/8W	R33
1	1	100-0005	Resistor, Jumper Wire	W3
1	1	120-0001	Resistor Pack, 220/330 DIP	U121

QUANTITY FD3812 FF38-XX		PART NUMBER	DESCRIPTION	REFERENCE
2	2	120-0009	Resistor Pack, 13 x 680, DIP	U128, 130
1	1	124-5010	Potentionmeter, 500 OHMS, 10%, $\frac{1}{2}W$	R2
2	2	124-5020	Potentiometer, 5K OHMS, 10%, $\frac{1}{2}W$	R28, 29
2	2	130-1015	Capacitor, 100 Picofarad, 5% 500V, MICA	C10, 12
2	2	130-1515	Capacitor, 150 Picofarad, 5%, 500V, MICA	C7, C16
1	1	130-2215	Capacitor, 220 Picofarad, 5%, 500V, MICA	C20
1	1	130-4705	Capacitor, 47 Picofarad, 5%, 500V MICA	C1
1	1	130-4715	Capacitor, 470 Picofarad, 5%, 500V MICA	C6
1	1	130-6805	Capacitor, 68 Picofarad, 5%, 500V MICA	C18
3	3	130-7515	Capacitor, 750 Picofarad, 5%, 500V MICA	C17, 19 23
1	1	130-3315	Capacitor, 330 Picofarad, 5%, 500V MICA	C15
2	2	131-2230	Capacitor, .022 Microfarad, 10%, 100V, FILM	C9, 13
2	2	131-4730	Capacitor, .047 Microfarad, 10%, 100V, FILM	C8, 14
5	5	135-0003	Capacitor, .01 Microfarad, Ceramic	C2, 3, 4, 5, 11
69	69	135-1004	Capacitor, .1 Microfarad, 20%, 50V, Ceramic	As shown on Silk- screen
1	1	135-4742	Capacitor, .47 Microfarad, 20%, 50V Ceramic	C21

QUANTITY		PART NUMBER	DESCRIPTION	REFERENCE
FD3812	FF38-XX			
1	1	139-2262	Capacitor, 22 Microfarad, 20%, 15V	C22
2	2	200-4125	Transistor, PNP, 2N4125	Q1, 2
5	5	300-4446	Diode, Switching	CR1, 2, 3, 4, 5
5	5	301-0559	Light Emitting Diode	CR6, 7, 8, 9, 10
1	1	330-0395	Diode, Zener, 3.9V, IN4730	VR4
1	1	330-0475	Diode, Zener, 4.7V, IN4732	VR3
1	1	330-0515	Diode, Zener, 5.1V, IN4733	VR1
1	1	330-1005	Diode, Zener, 10V, IN4740	VR2
1	1	402-1003	Oscillator, 10MHz	V6
1	1	503-0107	Connector, 7 Pin P.C. Mount	J3
0	1	503-7545	Connector, 14 Pin Dip	J4
1	1	250107	Process Board	
Ref	Ref	250105	Schematic	



APPENDIX B  
DOUBLE DENSITY CONTROLLER  
SCHEMATIC DIAGRAMS







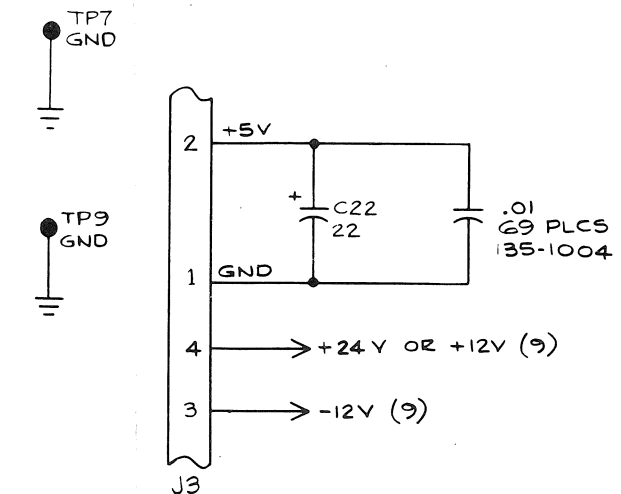


DESCRIPTION				PCBA DASH NO	C17, C19, W3, R23, 35, U77, 85, 86, 87, 89, 90, 98, 99, 100	W1	U71	U72	R27	W4, W2	J4	U75, 107, 108	CR6-10
+24V	LOW TRUE	INDICATORS	BUFFERED	-01	USE	OMIT	250142-01	250142-02	220, 2W	OMIT	OMIT	74LS240	USE
+12V	HIGH TRUE	NO INDICATORS	NON-BUFFERED	-02	OMIT	OMIT	250142-01	250142-02	27, 1/4W	USE	USE	74LS244	OMIT
-24V	LOW TRUE	NO INDICATORS	BUFFERED	-03	USE	OMIT	250142-01	250142-02	220, 2W	OMIT	OMIT	74LS240	OMIT
+24V	LOW TRUE	INDICATORS	NON-BUFFERED	-04	OMIT	OMIT	250142-01	250142-02	220, 2W	USE	USE	74LS240	USE

TABLE I

SPARES TABLE		
REF. DES.	TYPE	SPARES
U3	LS02	A, B
U7	7404	A
U8	7416	D, E
U23	LS76	A
U24	LS04	E
U33	LS76	A
U59	LS02	D
U68	LS00	B
U78	LS04	A, B, C
U79	LS00	B
U80	LS02	A
U88	LS02	C
U93	LS76	B
U101	LS76	A
U116	LS02	B
U122	7438	D
U123	7416	C
U124	7416	D
U127	7416	C

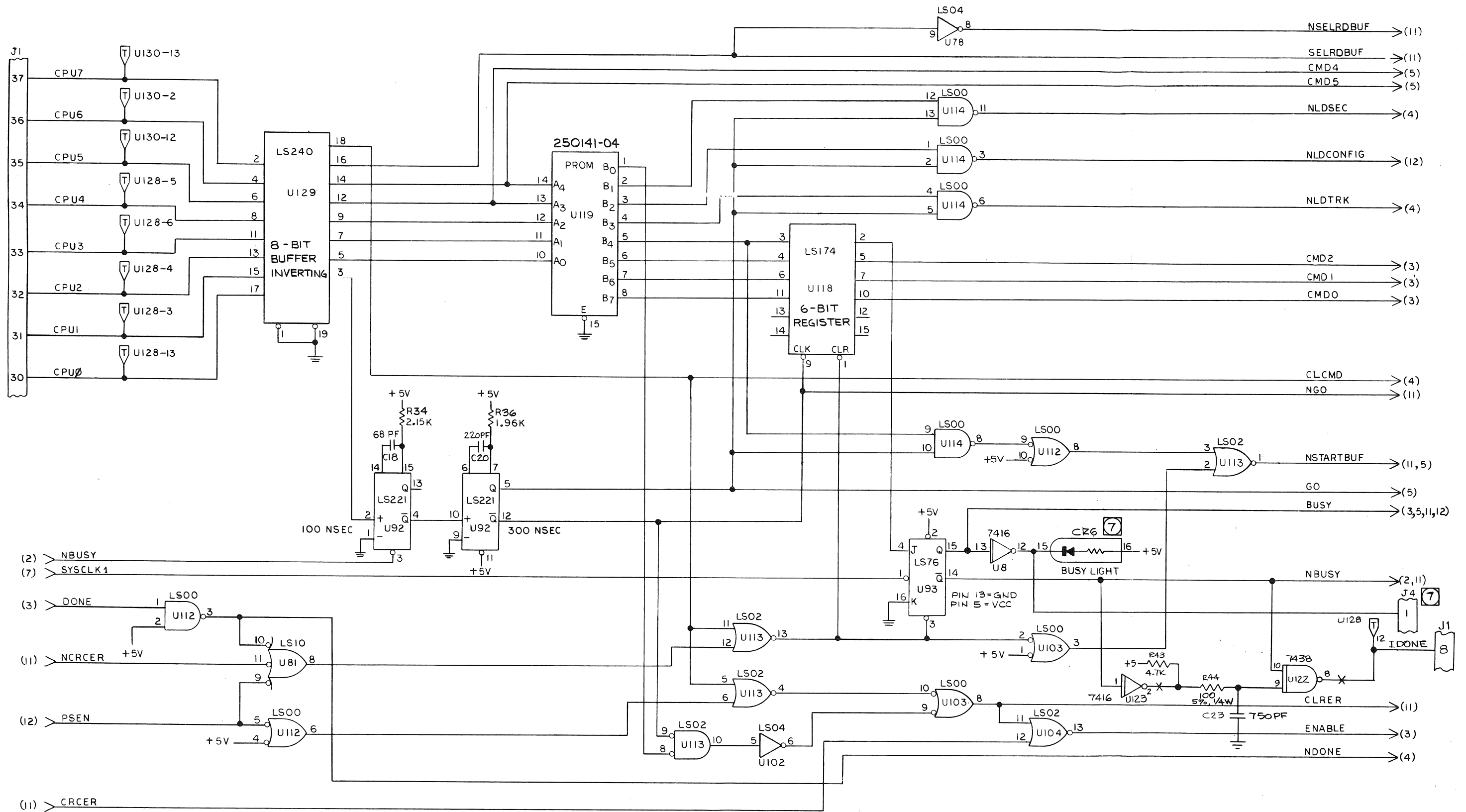
LAST USED	NOT USED	DELETED
U130	U13, U21, U30, U97,	
	U110, U111, U115, U120	
R45	R31, R40, R41, R42	



NOTES: UNLESS OTHERWISE SPECIFIED.

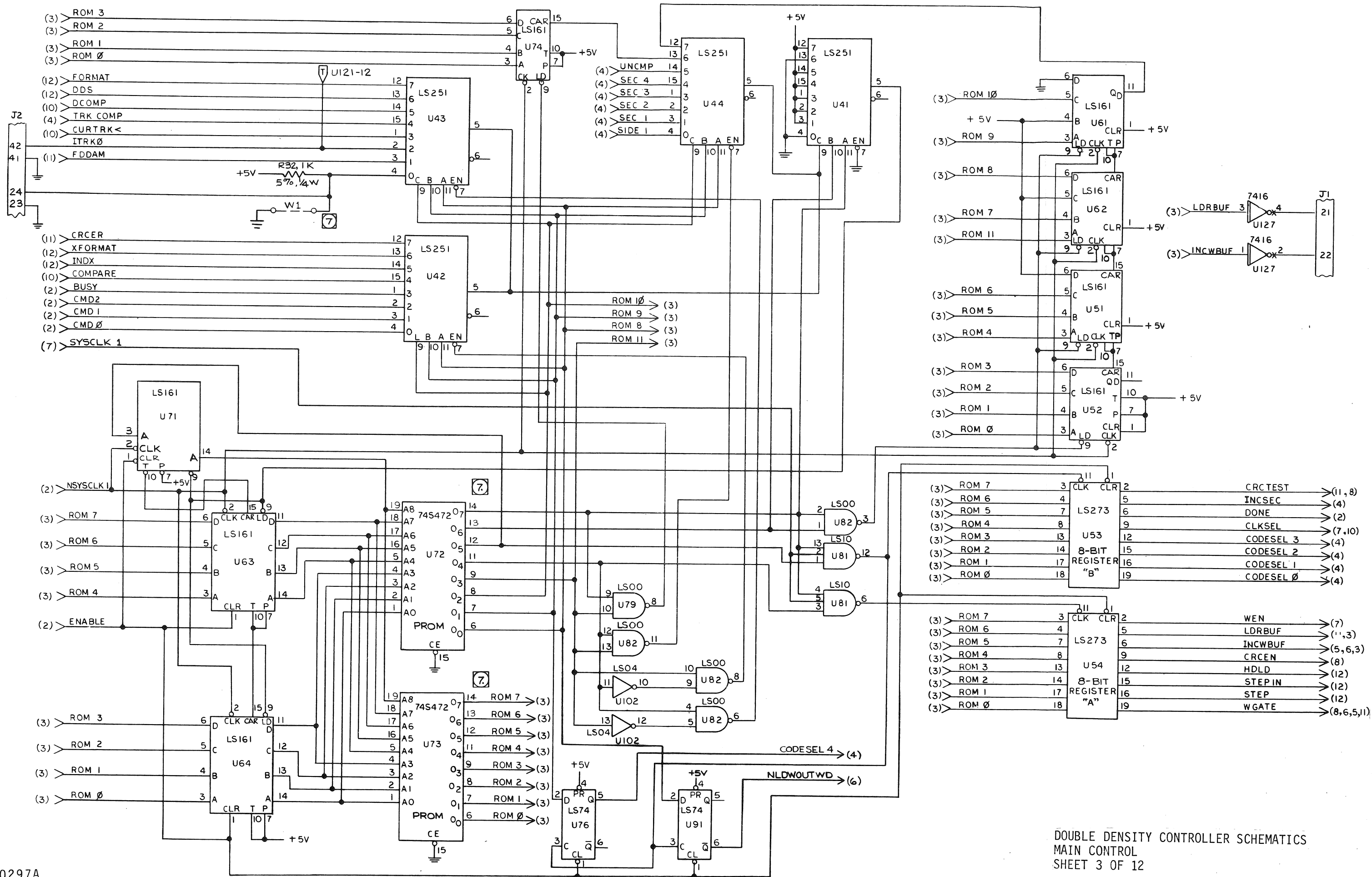
1. FOR SPARE LOGIC ELEMENTS SEE TABLE I.
2. RESISTOR VALUES ARE IN OHMS, 1%, 1/8W.
3. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 35V.
4. SIGNALS ARE CROSS-REFERENCED BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC.
5. 14 PIN I.C.'S - PIN 7 IS GROUND & PIN 14 IS +5V.  
16 PIN I.C.'S - PIN 8 IS GROUND & PIN 16 IS +5V.  
20 PIN I.C.'S - PIN 10 IS GROUND & PIN 20 IS +5V.
6. DRAWING NUMBER INCOMPLETE WITHOUT DASH NUMBER. SEE TABLE II FOR PROPER DASH NUMBER.
7. FOR VALUE, P/N AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER SEE TABLE II.
8. FOR VALUE AND P/N OF COMPONENTS NOT AFFECTED BY VERSION NUMBER REFER TO PARTS LIST PL250106.





DOUBLE DENSITY CONTROLLER SCHEMATICS  
 CONTROLLER INTERFACE  
 SHEET 2 OF 12

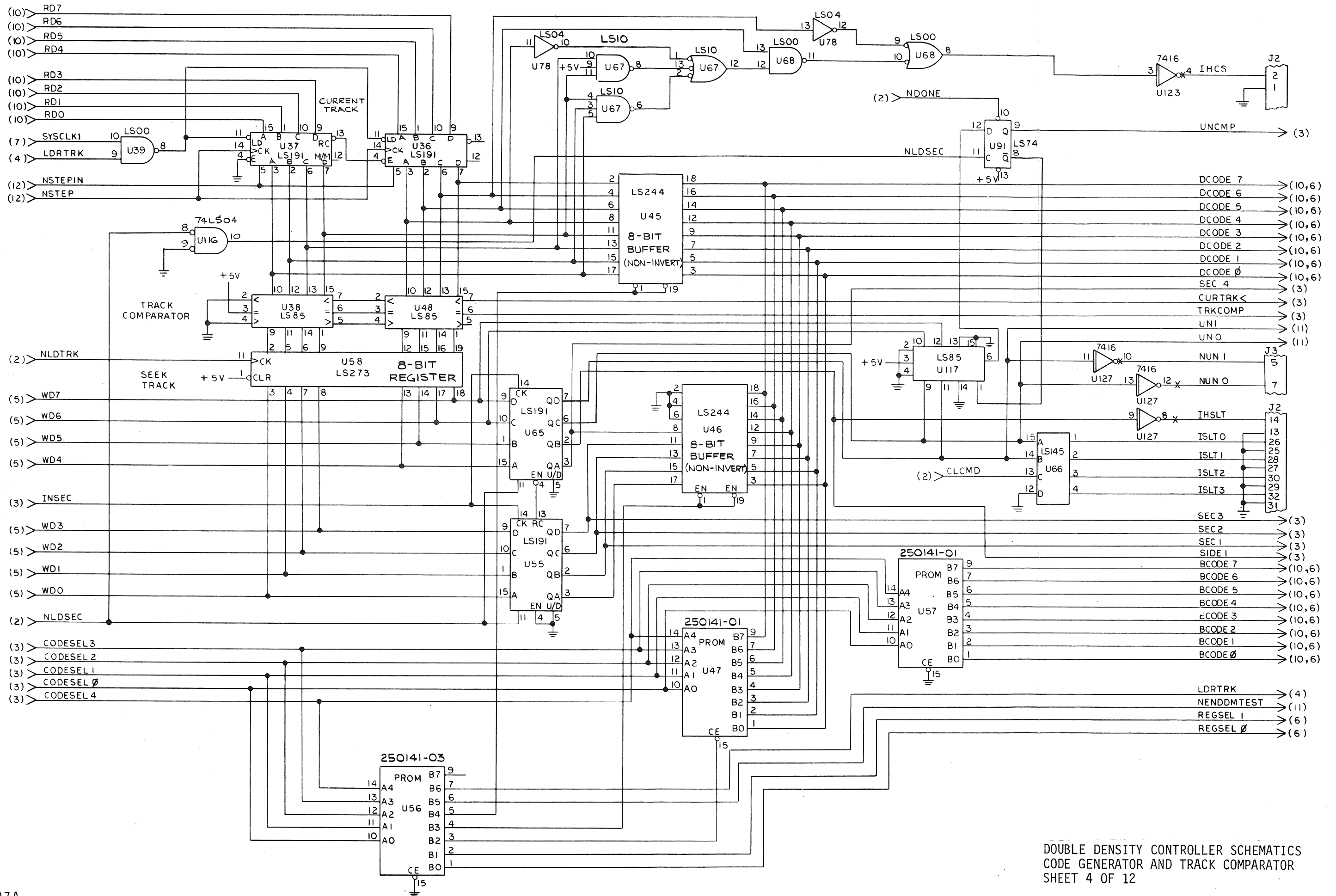




DOUBLE DENSITY CONTROLLER SCHEMATICS  
 MAIN CONTROL  
 SHEET 3 OF 12

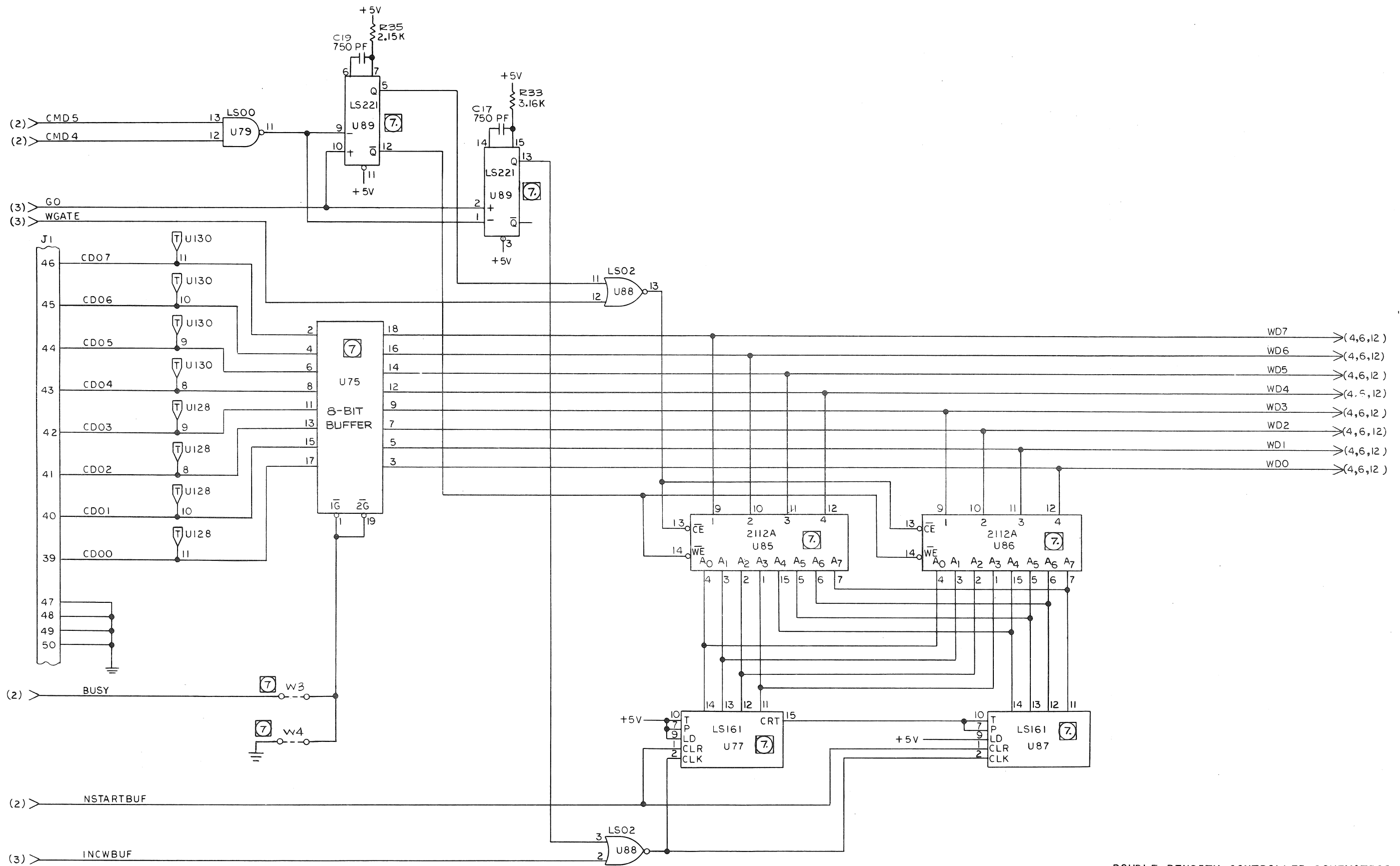






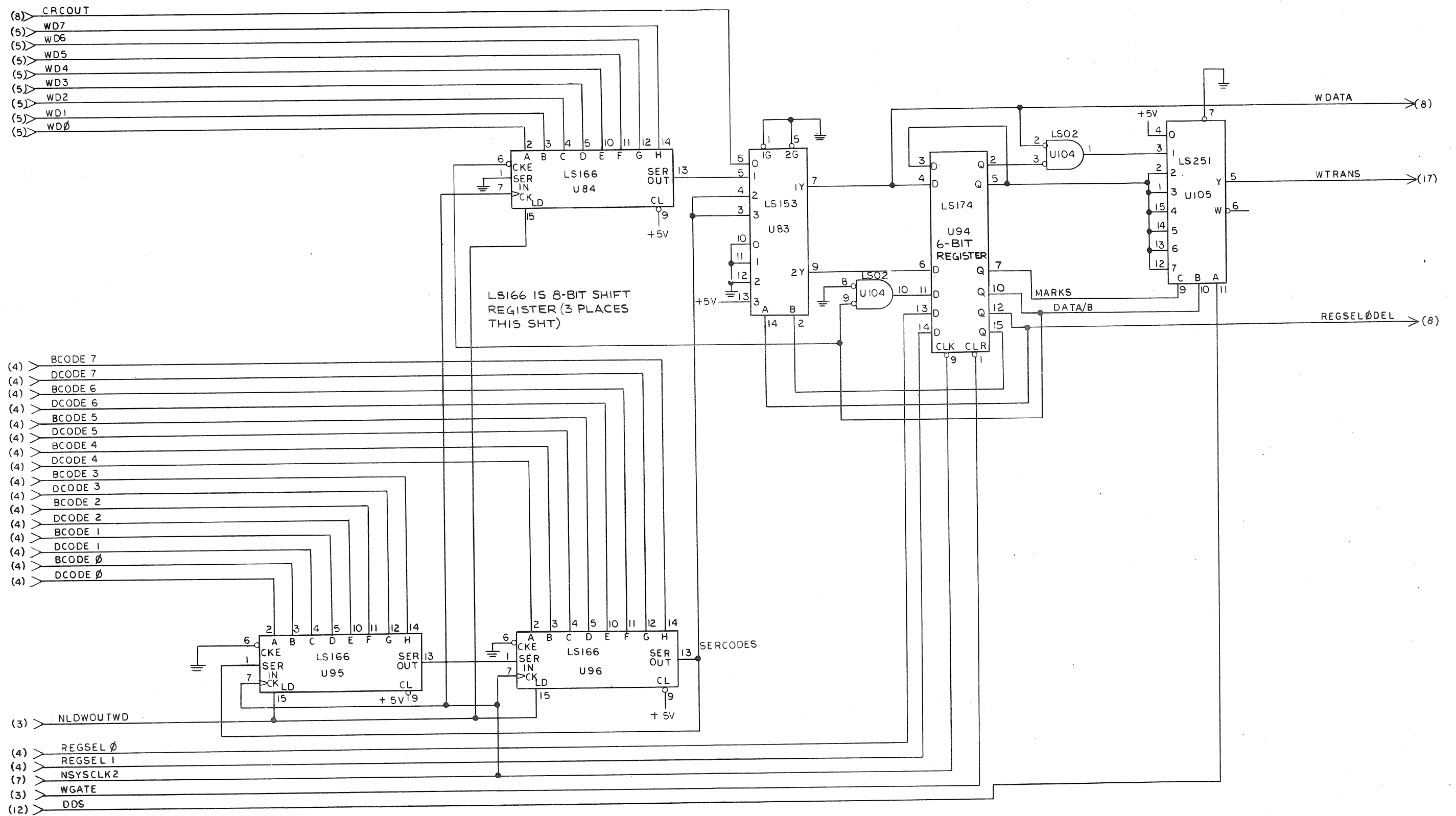
DOUBLE DENSITY CONTROLLER SCHEMATICS  
 CODE GENERATOR AND TRACK COMPARATOR  
 SHEET 4 OF 12





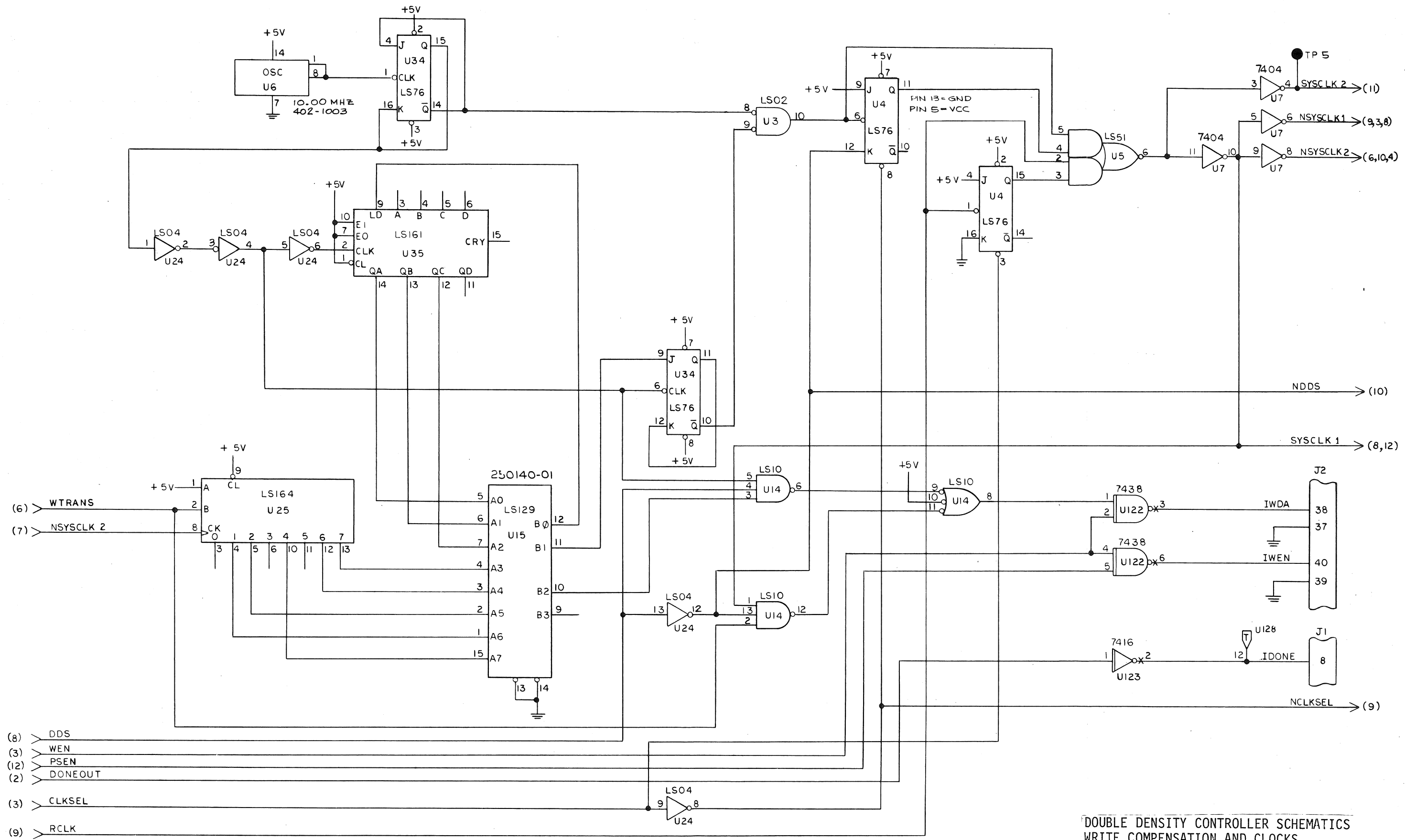
DOUBLE DENSITY CONTROLLER SCHEMATICS  
 WRITE BUFFER  
 SHEET 5 OF 12





DOUBLE DENSITY CONTROLLER SCHEMATICS  
 WRITE ENCODER  
 SHEET 6 OF 12

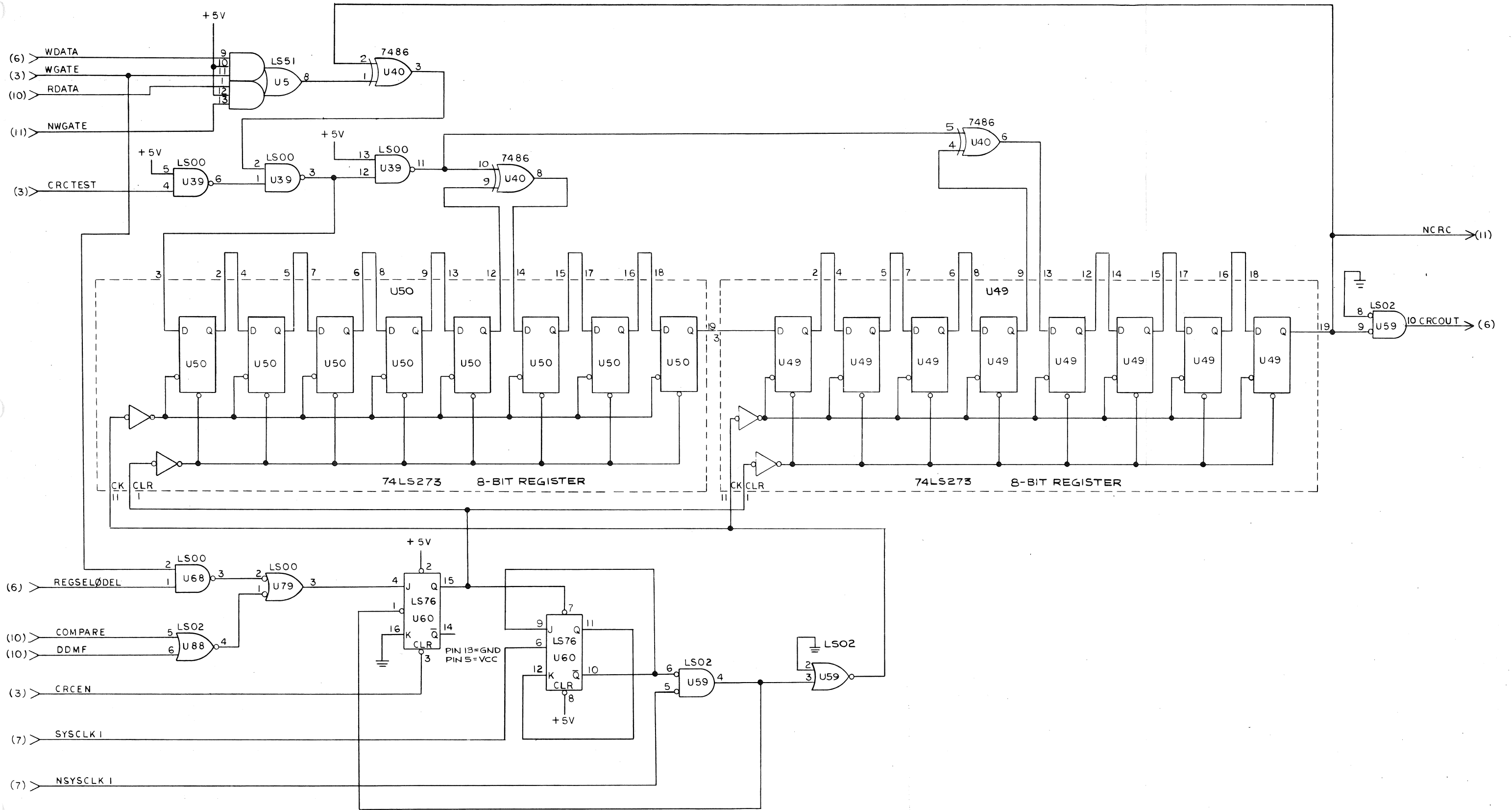




DOUBLE DENSITY CONTROLLER SCHEMATICS  
 WRITE COMPENSATION AND CLOCKS  
 SHEET 7 OF 12

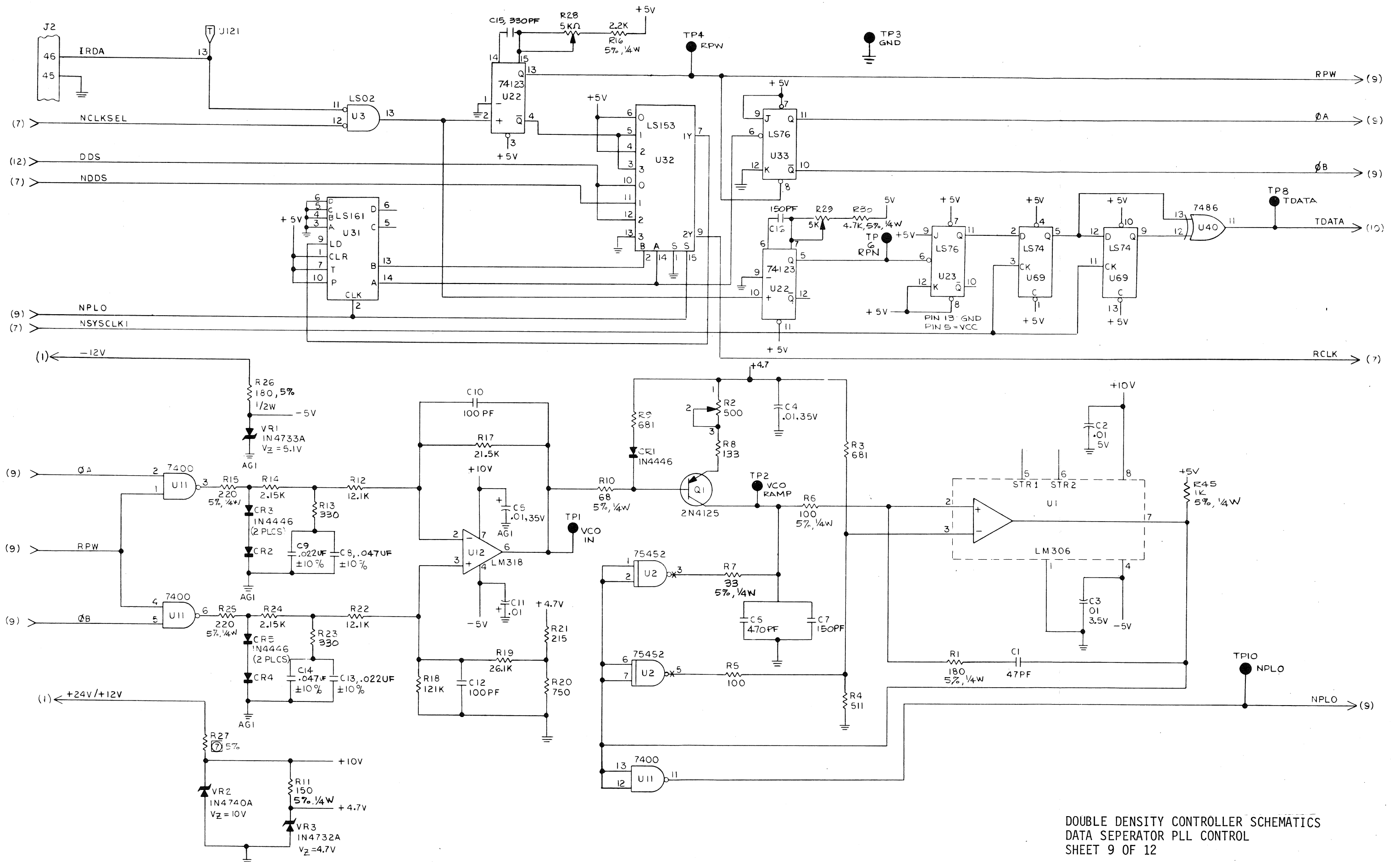






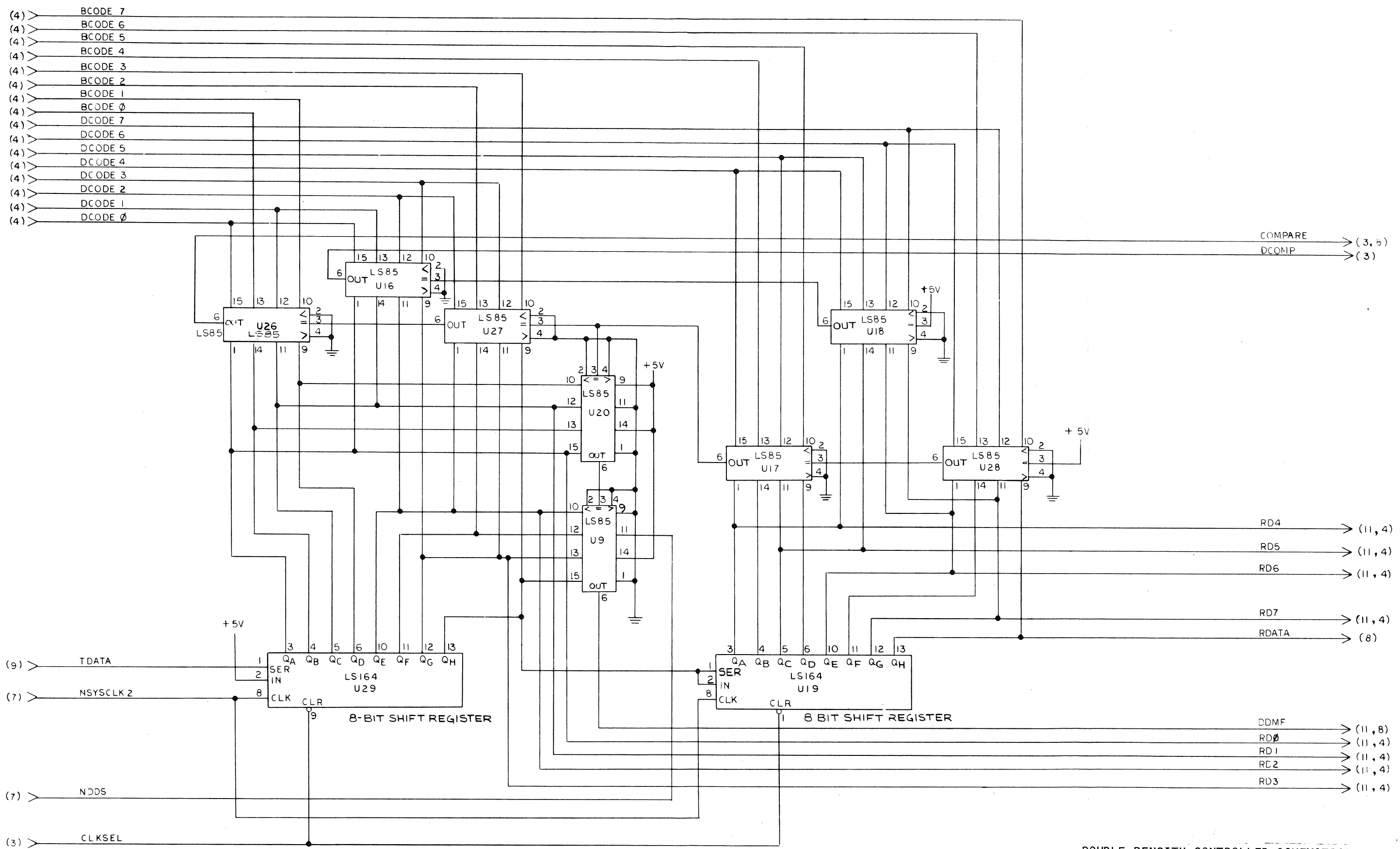
DOUBLE DENSITY CONTROLLER SCHEMATICS  
CRC REGISTER  
SHEET 8 OF 12





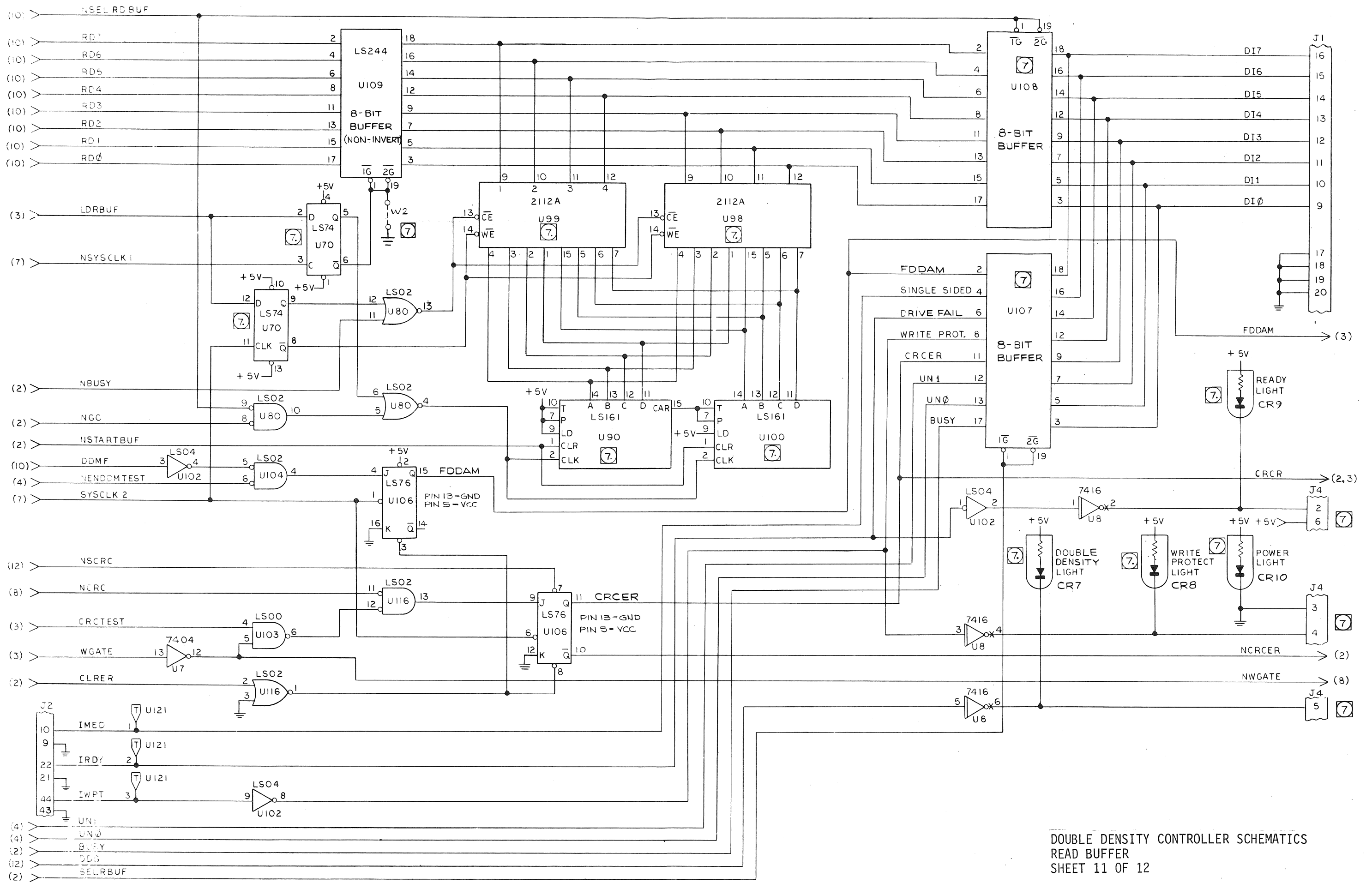
DOUBLE DENSITY CONTROLLER SCHEMATICS  
 DATA SEPERATOR PLL CONTROL  
 SHEET 9 OF 12





DOUBLE DENSITY CONTROLLER SCHEMATICS  
 READ DATA COMPARATOR  
 SHEET 10 OF 12





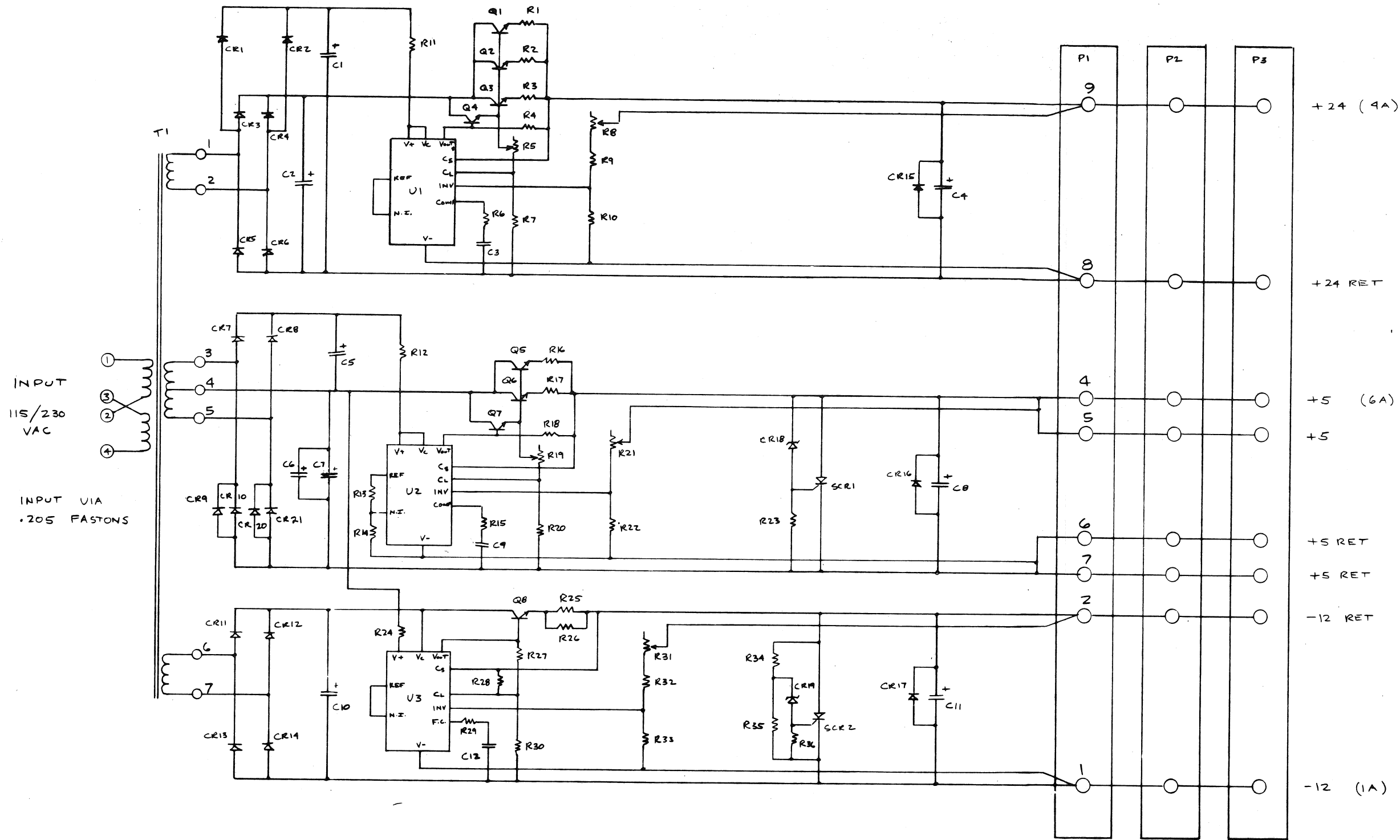
DOUBLE DENSITY CONTROLLER SCHEMATICS  
 READ BUFFER  
 SHEET 11 OF 12





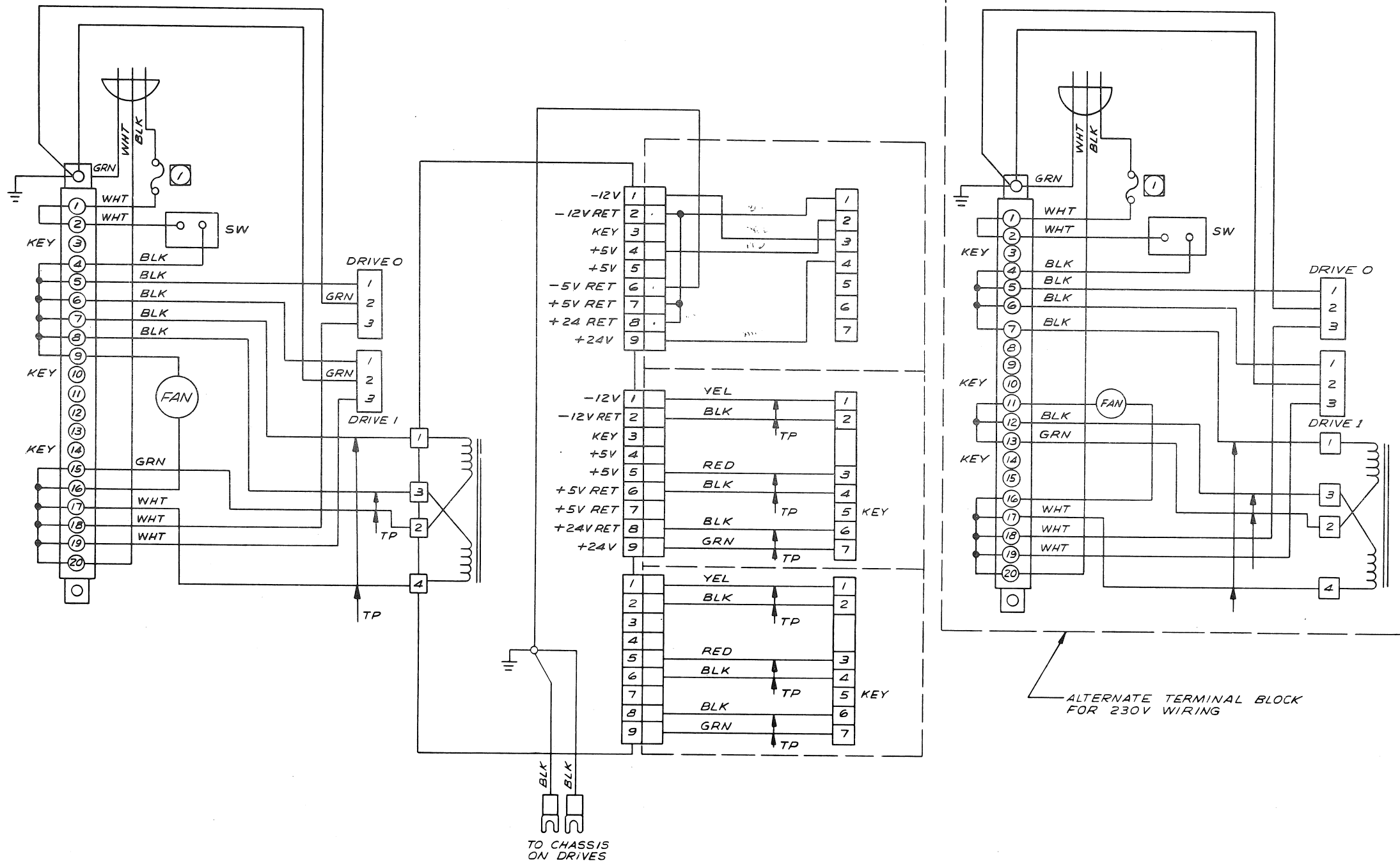






DOUBLE DENSITY CONTROLLER POWER SUPPLY  
SHEET 1 OF 1





NOTES: UNLESS OTHERWISE SPECIFIED  
 1. FOR 120 AC USE 3.0A SB FUSE. FOR 230V AC. USE 1.5A SB FUSE.  
 2. TP INDICATES TWISTED PAIR WIRES

ALTERNATE TERMINAL BLOCK FOR 230V WIRING



## APPENDIX C

### DISK DRIVE

#### SCHEMATIC DIAGRAMS

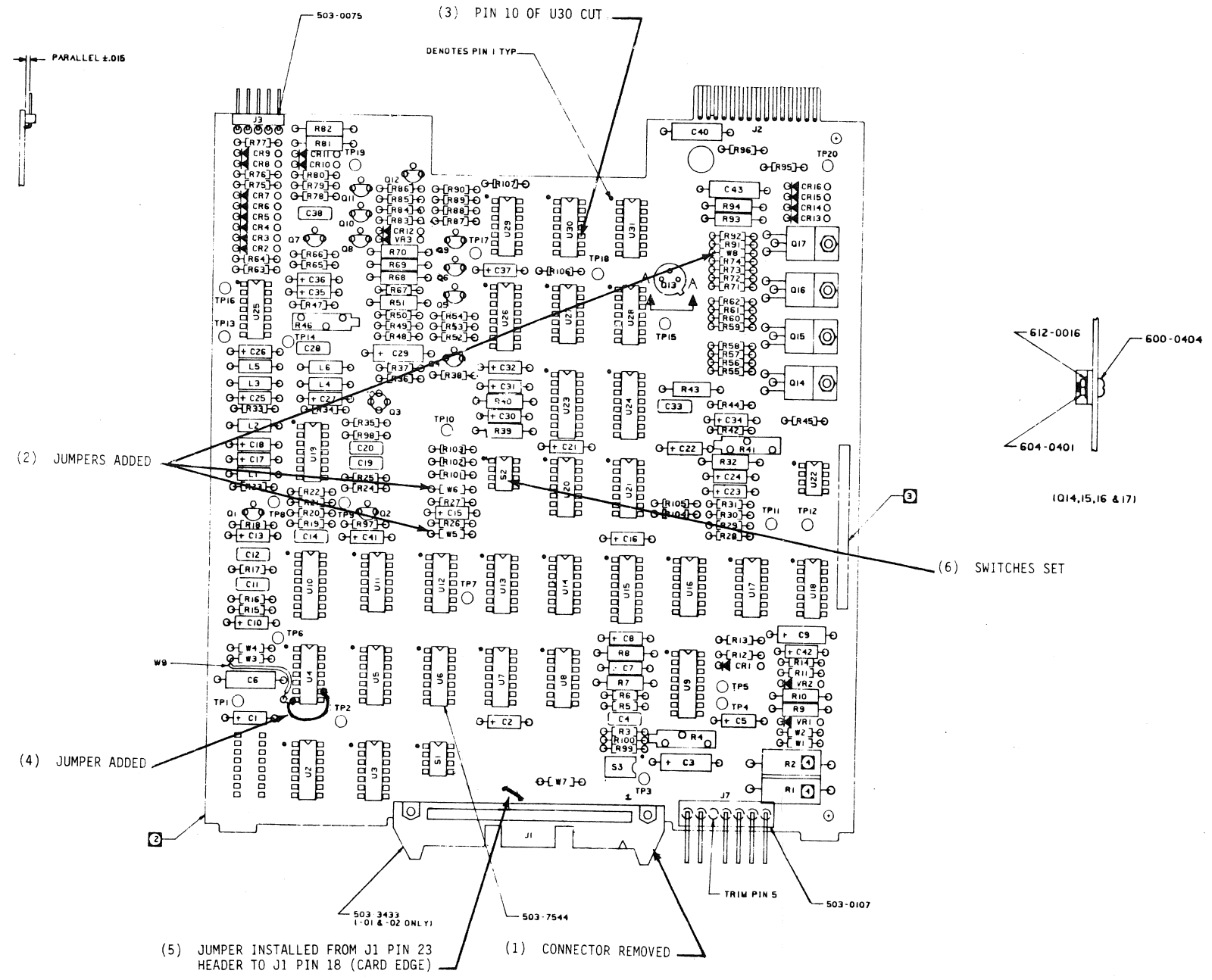
#### NOTE

The following modifications were made to the Pertec FD511A drive to create the drive used in the Double Density Disk system. These changes are identified on the following drive component layout diagram and schematics.

- (1) Remove J1
- (2) Install W5, W6 and W8
- (3) Cut Pin 10 of U30
- (4) Add a jumper from U4 pin 9 to U4 pin 7
- (5) Add a jumper from J1 (header) - Pin 23 to J1 (card edge) - Pin 18
- (6) Set S2 to positions as follows:
  - J1 - Closed
  - J2 - Open
  - J3 - Open
  - J4 - Open
- (7) The part number for these changes (250254) is stamped on the inside of the drive next to the identification label.







SECTION A-A



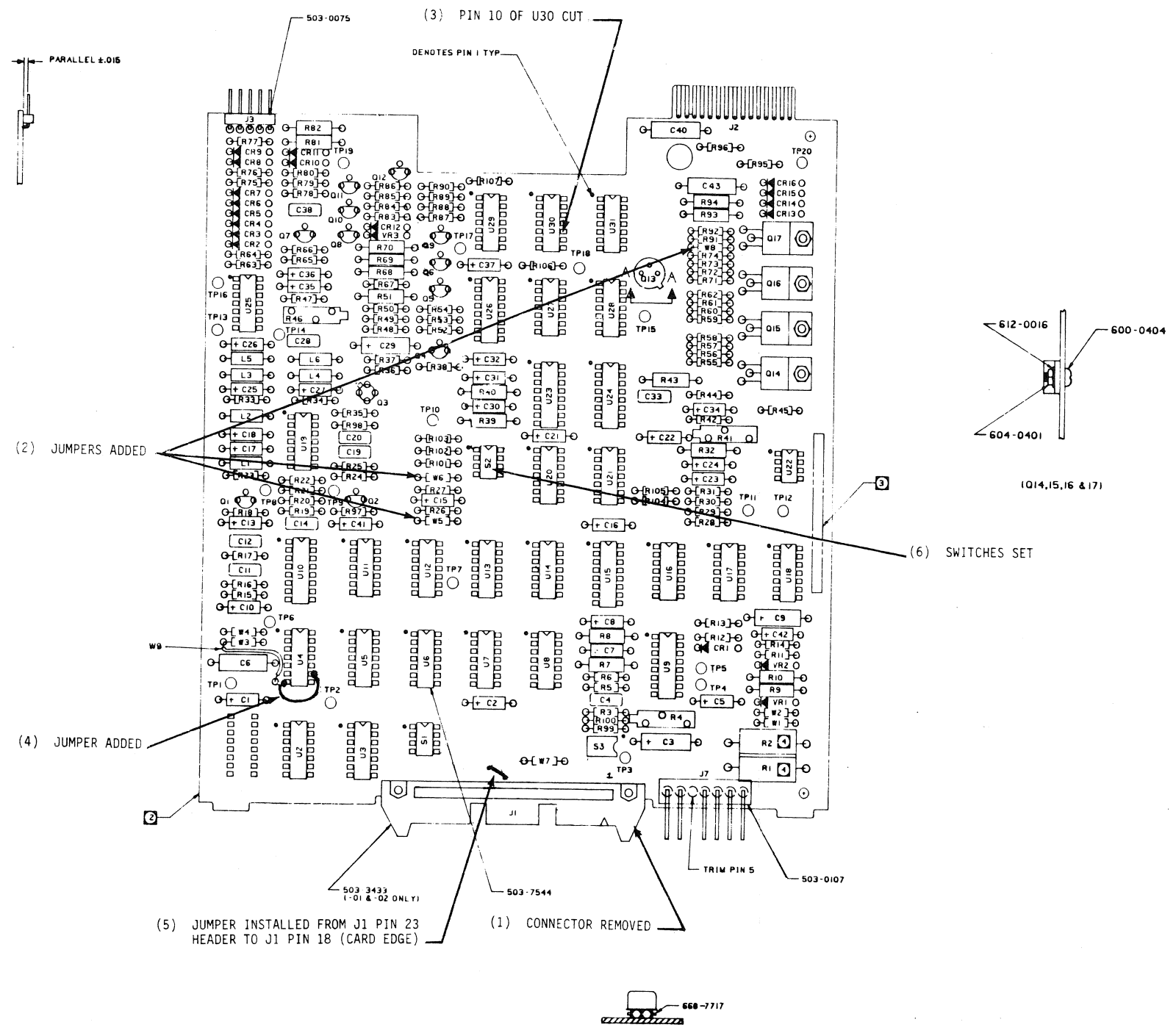




TABLE I ①

PART NO.	REFERENCE DESIGNATION
100-1015	R20,21,90
100-1025	R13,17,48,66,89,100
100-1035	R31,54,75,76
100-1045	R79,80
100-1055	R96
100-1515	R61,62
100-1525	R26,27,28,29,42,57,101,102,103,106,107,95
100-1535	R3
100-2215	R19,22,33,34,74,95
100-2225	R38,52,83,86,87
100-2235	R12,63,64,78
100-2725	R15
100-2735	R44,77
100-1225	R11
100-4705	R47
100-4715	R5,6,18,23,24,56,60,73,88,92,97
100-4725	R16,105
100-4735	R30
100-6805	R55,59,71,72,91
100-6815	R84,85
100-6825	R53,65
100-6835	R104
100-8225	R45
100-5525	R58
100-5615	R14
101-1015	R82
101-1215	R81,93,94
101-1525	R68
101-1825	R69,70
103-1015	R1,2
104-1621	R51
104-1961	R10
104-2152	R32,43
104-2871	R39
104-4640	R9
104-5621	R8
104-6191	R7
104-6811	R40
120-0001	U6
121-1030	R4
121-2020	R46
121-2030	R41
130-1015	C11,14
130-3315	C20
130-4705	C12
130-4715	C38
130-5615	C4
130-7515	C28,33

TABLE I ①

PART NO.	REFERENCE DESIGNATION
131-1030	C40
131-1520	C6
139-1020	C30,31
139-1045	C7
139-1055	C8,13,23,24,41
139-2244	C1,2,5,10,15,16,17,18,21,22,26,32,34,36,37,42
139-4751	C9,29,43
139-4755	C25,27,35
139-4762	C3
200-1100	Q16,17
200-1120	Q14,15
200-4123	Q1,2,4,9
200-4125	Q5,7,8,10,11,12
200-5321	Q13
300-4002	CR13,14,15,16
300-4446	CR1 THRU 12
330-0515	VR1
330-0685	VR3
331-1605	VR2
400-0339	U16
400-0555	U22
400-0592	U19,25
514-0008	S1
515-1015	L1,2,5,6
515-2405	L3,4
700-4107	U13,28
700-4123	U9
700-4221	U15,23,24
700-7400	U7,27
700-7402	U5,12,21
700-7404	U4,18
700-7406	U30
700-7407	U29
700-7410	U14
700-7414	U17
700-7438	U2,3,11
700-7450	U31
700-7474	U8,20
700-7476	U26
700-8020	U10

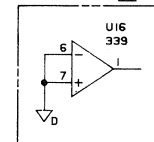
TABLE II ②

ASSEMBLY 600261 VERSION NO.	VERSION CHARACTERISTICS	W1	W2	W3	W4	W5	W6	W7	W8	W9	C19	W10	W11	R25	R35	R36	R37	R49		
		100-0005										691-6030	130-5615	691-6030	691-6030	100-4745	100-2225	100-2745	100-4725	100-6825
-01	-5V, SINGLE/DOUBLE	USE	OMIT	OMIT	USE	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USE	OMIT	OMIT	USE	USE	USE	USE	USE	
-02	-12V, SINGLE/DOUBLE	OMIT	USE	OMIT	USE	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USE	OMIT	OMIT	USE	USE	USE	USE	USE	
-03	MODEL "S"	USE	OMIT	OMIT	USE	USE	USE	USE	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	
-04	MODEL "S"	OMIT	USE	OMIT	USE	USE	USE	USE	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	
-05	-5V, SINGLE/DOUBLE	USE	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USE	USE	USE	OMIT	OMIT	USE	USE	USE	USE	USE	USE	
-06	MODEL "S" -12V	OMIT	USE	USE	OMIT	USE	USE	OMIT	OMIT	OMIT	USE	USE	USE	USE	USE	USE	USE	USE	USE	

TABLE II ②

ASSEMBLY 600261 VERSION NO.	R50	R67	R98	W12	S2	S3	Q3	Q6	
	100-1025	100-6825	VALUE	PART NO.	691-6030	514-0008	514-0008	204-3993	200-4125
-01	USE	USE	2.2K	100-2225	OMIT	USE	OMIT	USE	USE
-02	USE	USE	2.2K	100-2225	OMIT	USE	OMIT	USE	USE
-03	OMIT	OMIT	1K	100-1025	OMIT	USE	OMIT	OMIT	OMIT
-04	OMIT	OMIT	1K	100-1025	OMIT	USE	OMIT	OMIT	OMIT
-05	USE	USE	2.2K	100-2225	OMIT	USE	USE	USE	USE
-06	USE	USE	2.2K	100-2225	USE	OMIT	OMIT	USE	USE

TABLE III ①

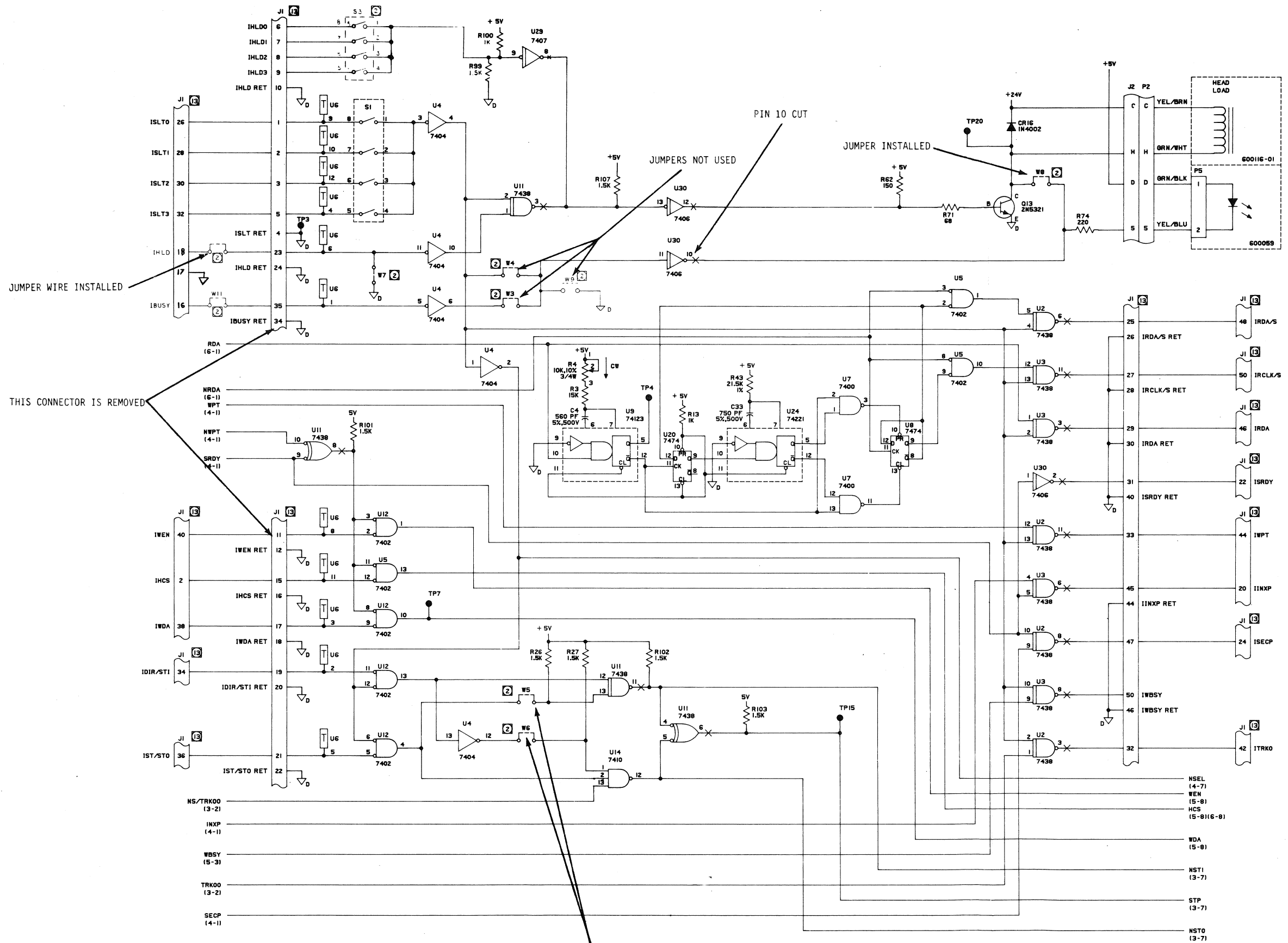


REFERENCE DESIGNATIONS

LAST USED	NOT USED	DELETED
C43		C38
CR16		
LE		
Q17		
R107		
S3		
TP20		
U31	U1	
VR3		
W12		

- ④ TERMINATING RESISTOR PACK IS SPECIFIED AT TOP ASSY.
  - ③ CONNECTOR J1 SHOWN SCHEMATICALLY FOR BOTH THE STANDARD FDSX3 AND FDSX4 CONFIGURATIONS.
  - 12. LOGIC GROUND IS DENOTED BY A  $\nabla$  SYMBOL.  
ANALOG GROUND IS DENOTED BY A  $\nabla_A$  SYMBOL.
  - 11. SIGNALS ARE CROSS-REFERENCED BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.
  - ⑩ FOR SPARE LOGIC ELEMENTS SEE TABLE III.
  - 9. PIN 7 OF 14 PIN I.C.'S IS LOGIC GND.  
PIN 14 OF 14 PIN I.C.'S IS +5V.  
PIN 13 OF 7476 IS LOGIC GND.  
PIN 5 OF 7476 IS +5V.  
PIN 8 OF 16 PIN I.C.'S IS LOGIC GND.  
PIN 16 OF 16 PIN I.C.'S IS +5V.  
PIN 12 OF 339 IS LOGIC GND.  
PIN 13 OF 339 IS +24V.
  - 8. DIODES ARE IN4446.
  - 7. PNP TRANSISTORS ARE 2N4125.
  - 6. NPN TRANSISTORS ARE 2N4123.
  - 5. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.
  - 4. RESISTOR VALUES ARE IN OHMS 5%, 1/4W.
  - 3. (RESERVED)
  - ② FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER SEE TABLE II.
  - ① FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER SEE TABLE I.
- NOTES: UNLESS OTHERWISE SPECIFIED





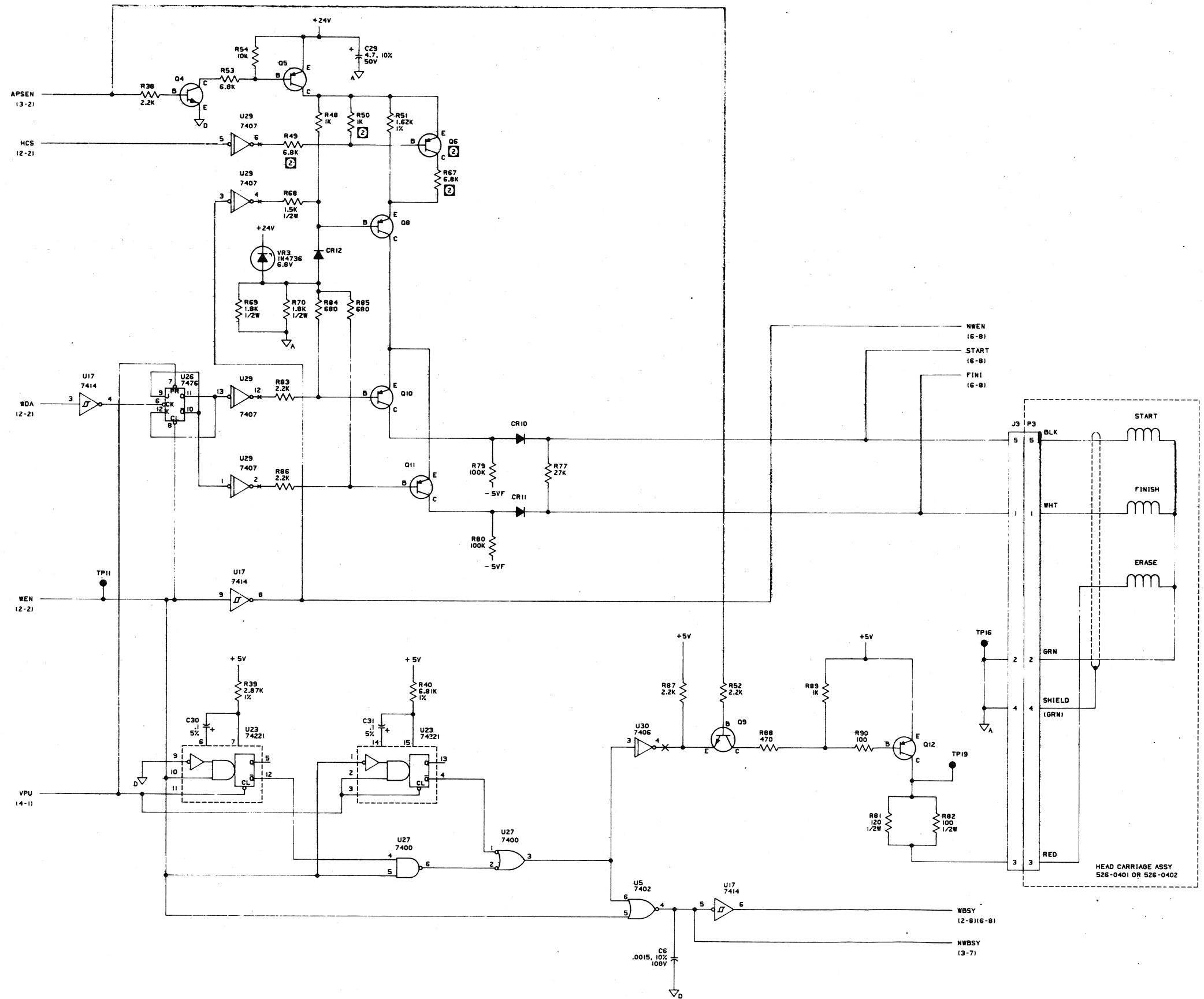
DISK DRIVE SCHEMATICS  
INTERFACE/CONTROL  
SHEET 2 OF 6





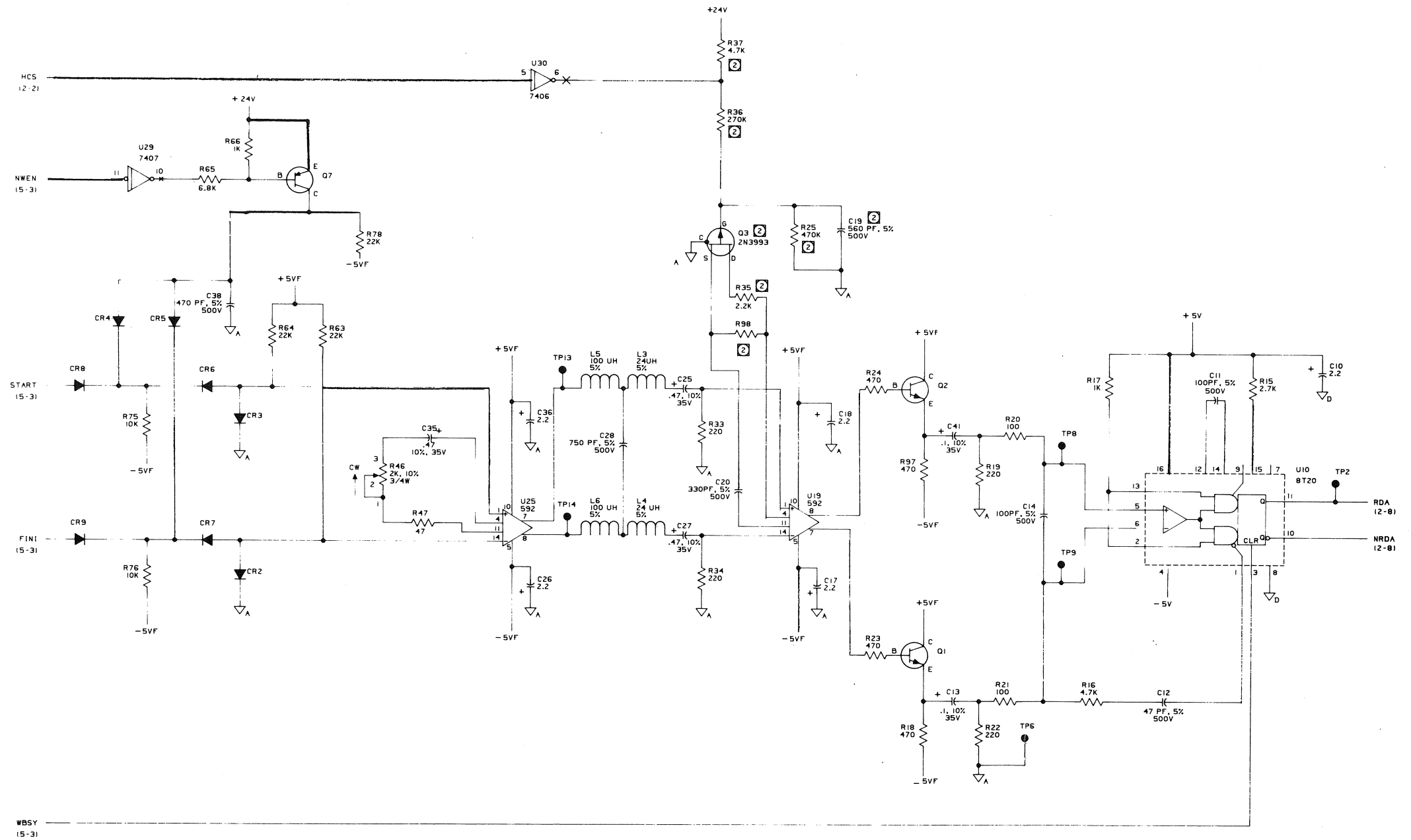






DISK DRIVE SCHEMATICS  
WRITE LOGIC  
SHEET 5 OF 6





DISK DRIVE SCHEMATICS  
 READ AMPLIFIER  
 SHEET 6 OF 6





