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A Division of Pertec Computer Corporation
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# MAINTENANCE GUIDE

## MODEL FD2400 SERIES

## FLOPPY DISK SYSTEM

Revision A
April, 1977

## FORWARD

This manual provides the operating and maintenance information for the Microfloppy™ FD2400 series floppy disk drive manufactured by iCOM® Division of Pertec Computer Corporation.

The major divisions of this manual are:

OPERATORS GUIDE

MAINTENANCE GUIDE

SCHEMATIC DIAGRAMS

INTERFACING GUIDE

NOTES - MISC.

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## SCHEMATIC DIAGRAMS



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## NOTES-MISC

BASIC-M

TEXT EDITOR

MACRO ASSEMBLER

SMALL DIAGNOSTIC

RESIDENT FDOS

# MAINTENANCE GUIDE

## 1. INTRODUCTION

This maintenance guide is intended as a trouble-shooting aid for fault isolation down to the replaceable subassembly level. Schematics are supplied in the following section as supplementary information in signal tracing.

No attempt is made to explain the operation of the equipment down to the component level. This is possible, however, if given the necessary experience and test equipment.

## 2. SECTION CONTENTS

This section is comprised of:

Signal Glossary

Possible Failure Causes

Microfloppy Controller/Interface Parts List

## 3. SIGNAL GLOSSARY

| Signal | Description |
|---|---|
| AØØ thru AØ15 | Address Bits Ø thru 15 |
| BMS | Board Memory Select |
| BSINP | Buffered Status Input |
| CCS | Control Chip Select |
| DI1 thru DI7 | Data Input Bits 1 thru 7 |
| DO1 thru DO7 | Data Outputs Bits 1 thru 7 |
| DIRC | R/W Head Direction Control |
| DRQ | Data Request |
| DSE | Drive-select-port Select Enable |
| FDCLOCK | Separated Read Clock |
| DRIVE SELECT 1 thru 3 | Disk Drive Select Ø thru 2 |
| FDDATA | Separated Read Data |
| GDO | Gate Data Output |
| GIDI | Gate Input Data In |
| GMDI | Gate Memory Data In |

3. SIGNAL GLOSSARY (cont.)

| Signal | Description |
|---|---|
| HLD | Head Load |
| HLDB | Head Load Buffered |
| HLT | Head Load Timing |
| IB | Internal Bus |
| INDEX/SECTOR | Index/Sector Sense |
| INTRQ | Interrupt Request |
| IOW | Input/Output Write |
| IP | Index Pulse |
| MWRITE | Memory Write |
| PDBIN | Processor Data Bus In |
| POC | Processor Output |
| PRDY | Processor Ready |
| PROGC | Programmed Clear |
| PSINP | Processor Status Input |
| PWR | Power |
| ROMCS | Read-Only-Memory |
| SINP | Status Input |
| SMEMR | Status Memory Read |
| SOUT | Status Output |
| STEP | R/W Head Control |
| WD | Write Data |
| WG | Write Gate |

4. POSSIBLE FAILURE CAUSES

| Symptom | Possible Causes |
|---|---|
| Drive Fail Status, Drive Motor does not run | Drive not up to speed yet. Software should allow 6-7 seconds after closing door. |
| | Diskette jammed. Open door. Reinsert diskette. Try again. Diskette may be out of tolerance. Try another diskette. |
| | Check cable connection. Ribbon connector. Power connector. Drive connector. |
| | Is a valid unit selected? Check drive select. Should be logic "1" (low) for selected drive. All others should be logic "0" (high). |

4. POSSIBLE FAILURE CAUSES (cont.)

| Symptom | Possible Causes |
|---|---|
| Head Loads, but does not seek | Head may be past track 34, issue Seek 0 Command and retry. |
| | Diskette may be bad. Try another. |
| | Check STEP signal. When seeking, STEP should be alternate low and highs. |
| | In a multidrive system, if one unit seeks OK and the other doesn't, swap controllers in the disk drives. If problem now is in the other drive, replace the defective controller. If the same drive is bad, replace drive. |
| CRC Errors | Excessive wear on diskette. Replace diskette. |
| | Diskette not seated. Reinsert and retry, put system in a read loop. |
| Seeks to wrong track | Bad controller. Replace. |
| One bit of data is bad on read | Bad controller or interface. Write a pattern of all one's and examine input and output of read buffer. |
| One bit of data is bad on write | Verify that data written previously can be read correctly. |
| | Write all one's pattern continuously to one sector. Check inputs to write buffer DØØ-D07 and outputs of write buffer. |

5. MICROFLOPPY CONTROLLER/INTERFACE PARTS LIST

| Description | Reference Designator | Part Number |
|---|---|---|
| Printed Circuit Board | | 200062-800 |
| Digital IC's | | |
| Quad 2-Input Positive NAND | U19,U32 | 74LS00 |
| 8-Input Positive NAND | U23,U24 | 74LS30 |

5. MICROFLOPPY CONTROLLER/INTERFACE PARTS LIST (cont.)

| Description | Reference Designator | Part Number |
|---|---|---|
| Quad 2-Input Positive-OR | U25 | 74LS32 |
| Quad 2-Input Exclusive OR | U36 | 74LS86 |
| Quad 2-Input Positive NOR | U26 | 74LS02 |
| Hex Inverter | U13,U14 | 74LS04 |
| Hex Schmitt Trigger Inverters | U30,U35 | 74LS |
| Dual Monstable Multivibrators with Schmitt Trigger Input | U33 | 74LS221 |
| Non-Inverting Buffer (Tristate) | U5,U7,U15 | 74LS367 |
| Inverting Buffer (Tristate) | U6,U16,U17,U34 | 74LS368 |
| Hex Inverter Buffer/Driver (Open Collector) | U29 | 7416 |
| Quad 2-Input NAND Buffer (Open Collector) | U28 | 7438 |
| 1K X 8 EPROM | U4 | 2708 |
| 128 X 8 RAM | U1,U2,U3 | MCM6810AP |
| Floppy Controller | U8 | FD7711B-1 |
| Linear IC's | | |
| Dual Voltage Controlled Oscillator | U31 | MC4024P |
| Phase Comparator | U20 | MC4044P |
| Crystal Oscillator, 4MHZ | U18 | K1116A-4MHZ |
| Voltage Regulator,+5V | Q1 | LM340-5 or 7805 |

5. MICROFLOPPY CONTROLLER/INTERFACE PARTS LIST (cont.)

| Description | Reference Designator | Part Number |
|---|---|---|
| Voltage Regulator,+12V | Q2 | LM340-12 or 7812 |
| Voltage Regulator,-5V | Q3 | LM320-5 or 7905 |
| Transistor, NPN, Small Signal | Q4 | MPS6571 |
| Resistors, Carbon Composition | | |
| 20 ohms | R7,R9,R15,R19 | 100-2215 |
| 330 ohms | R8,R10,R12,R16, R23 | 100-3315 |
| 820 ohms | R20 | 100-8215 |
| 1K ohms | R1,R6,R13,R14,R18 | 100-1025 |
| 2.2k ohms | R2,R21,R22 | 100-2225 |
| 3.6k ohms | R17 | 100-3625 |
| 5.1k ohms | R3,R4 | 100-5125 |
| 24k ohms | R5 | 100-2435 |
| Capacitors, Ceramic | | |
| 15-60pf, Trimmer | C1 | 135-0001 |
| 0.05mf, +20% 50V | C6 | 135-0002 |
| Capacitors, Mica | | |
| 36pf, ±5%, 500V | C5 | 135-3605 |
| 100pf, ±5%, 500V | C4 | 135-1015 |
| 430pf, ±5%, 500V | C2 | 135-4315 |
| Capacitors, Tantalum | | |
| 3.9mf, 10%, 35V | C7,C28,C29 | 135-0001 |
| 4.7mf, 10%, 35V | C3 | 135-4751 |
| Heatsink | HS1 | |
| IC Sockets | | |
| 14 Pin | (16 reqd.) | 503-7544 |
| 16 Pin | (15 reqd.) | 503-7541 |

5. MICROFLOPPY CONTROLLER/INTERFACE PARTS LIST (cont.)

| Description | Reference Designator | Part Number |
|---|---|---|
| 24 Pin | (4 reqd.) | 503-7542 |
| 40 Pin | (1 reqd.) | 503-7540 |
| Panhead Phillips Screw, 6-32 X 3/8 | (3 reqd.) | 600-0606 |
| Lock Washer, No. 6 | (3 reqd.) | 605-0600 |
| Hex Nut, 6-32 | (3 reqd.) | 604-0600 |

# SCHEMATIC DIAGRAMS
# FOR
# FD2400 SERIES
# FLOPPY DISK SYSTEM

PERTEC COMPUTER CORPORATION
MICROSYSTEMS DIVISION

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NOTICE



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# SCHEMATIC DIAGRAMS

## 1. INTRODUCTION

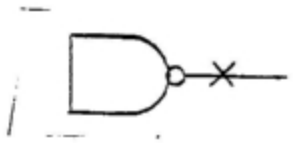
This section consists of the following schematics:

Figure 1. Controller/Interface Board
Figure 2. Disk Drive Interface
Figure 3. Disk Drive Motor and Speed Control
Figure 4. Power Supply
Figure 5. AC Power

## 1.2 SPECIAL SYMBOLS

The schematic diagrams contained in this section conform to standard symbology. The special symbols are:

Open Collector Output



High Current Buffer

Schmitt Trigger Operation

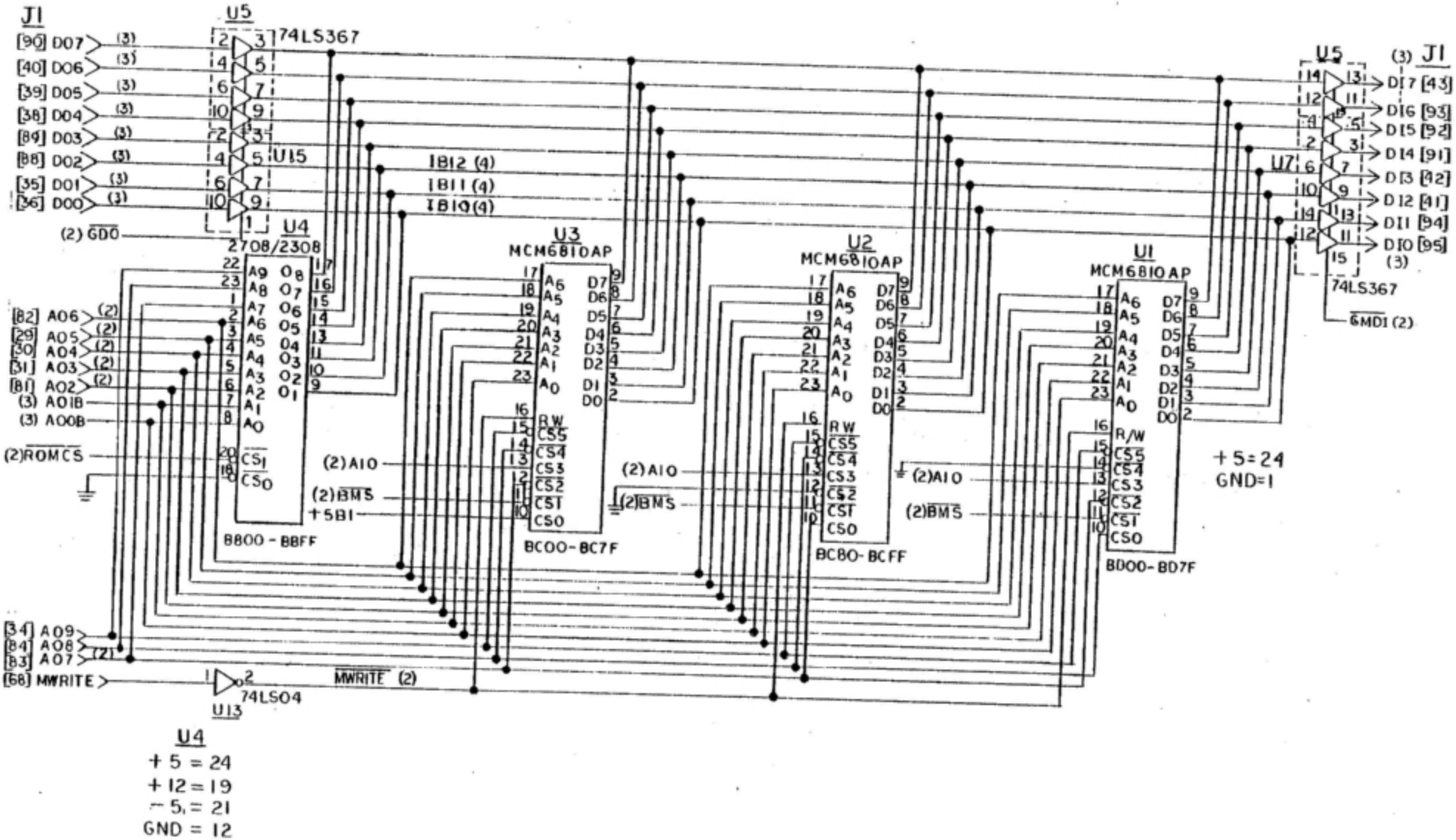



Figure 1. Controller/Interface Schematic (Sheet 1 of 6)

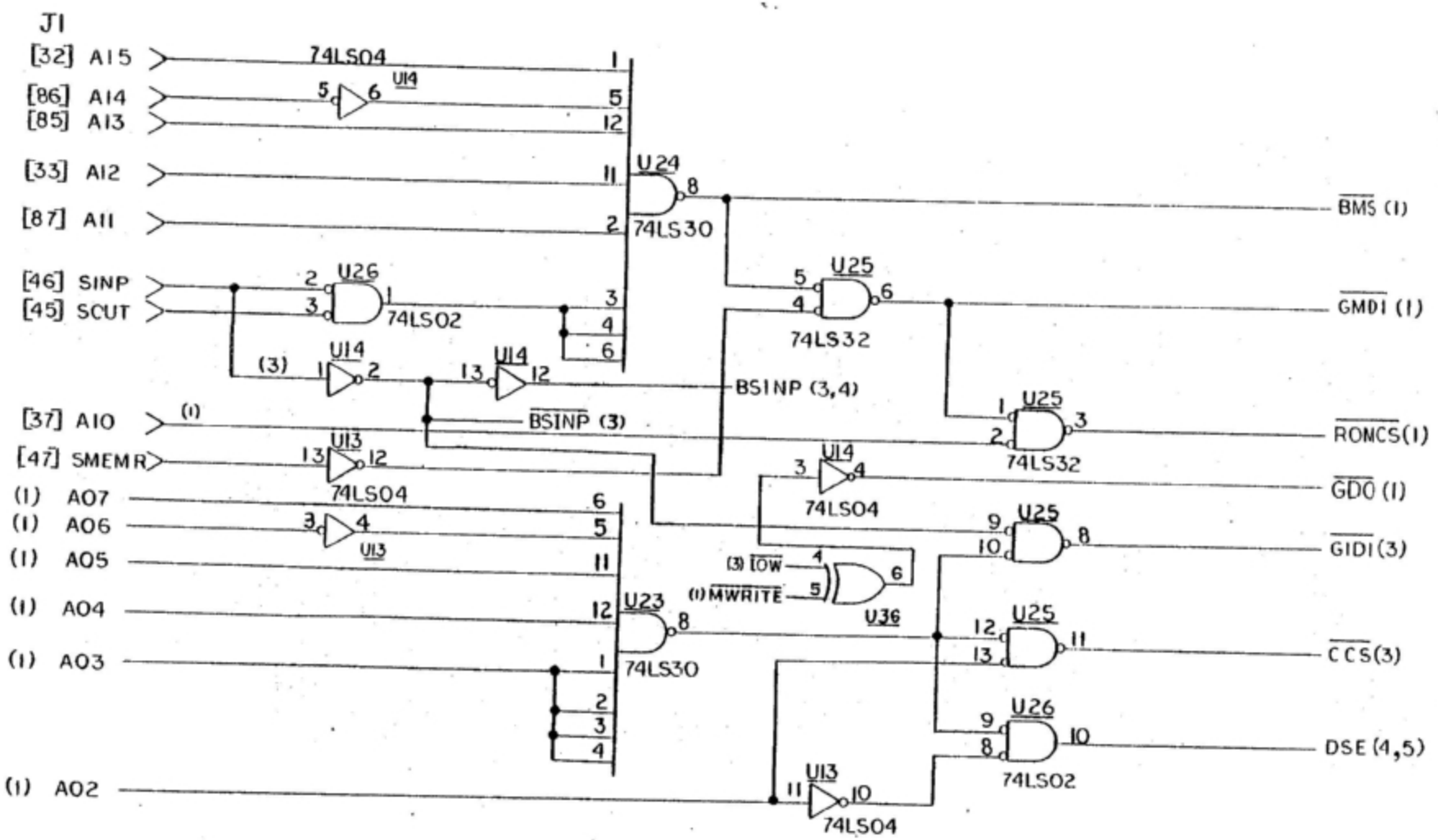



Figure 1. Controller/Interface Schematic (Sheet 2 of 6)

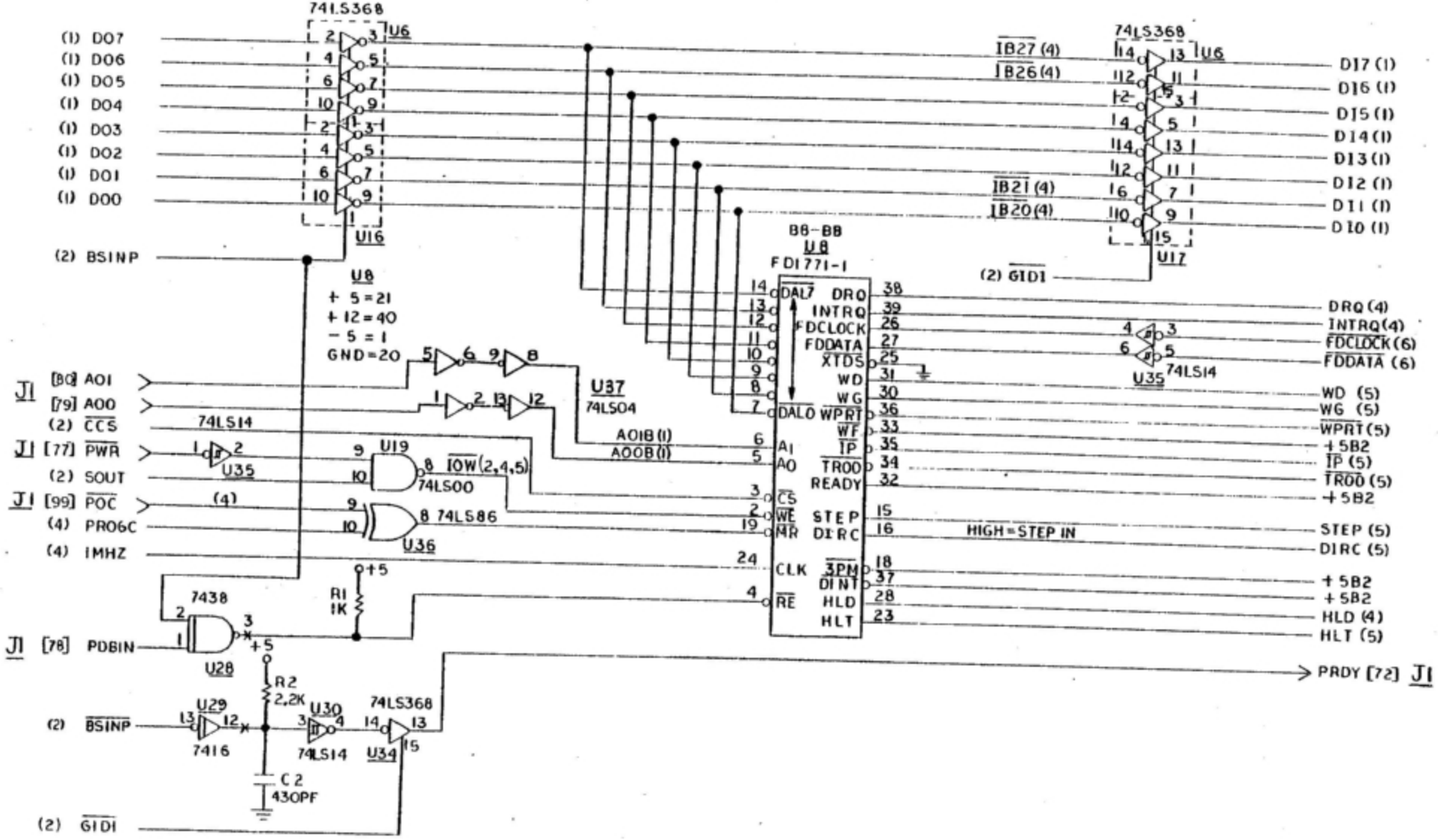



Figure 1. Controller/Interface Schematic (Sheet 3 of 6

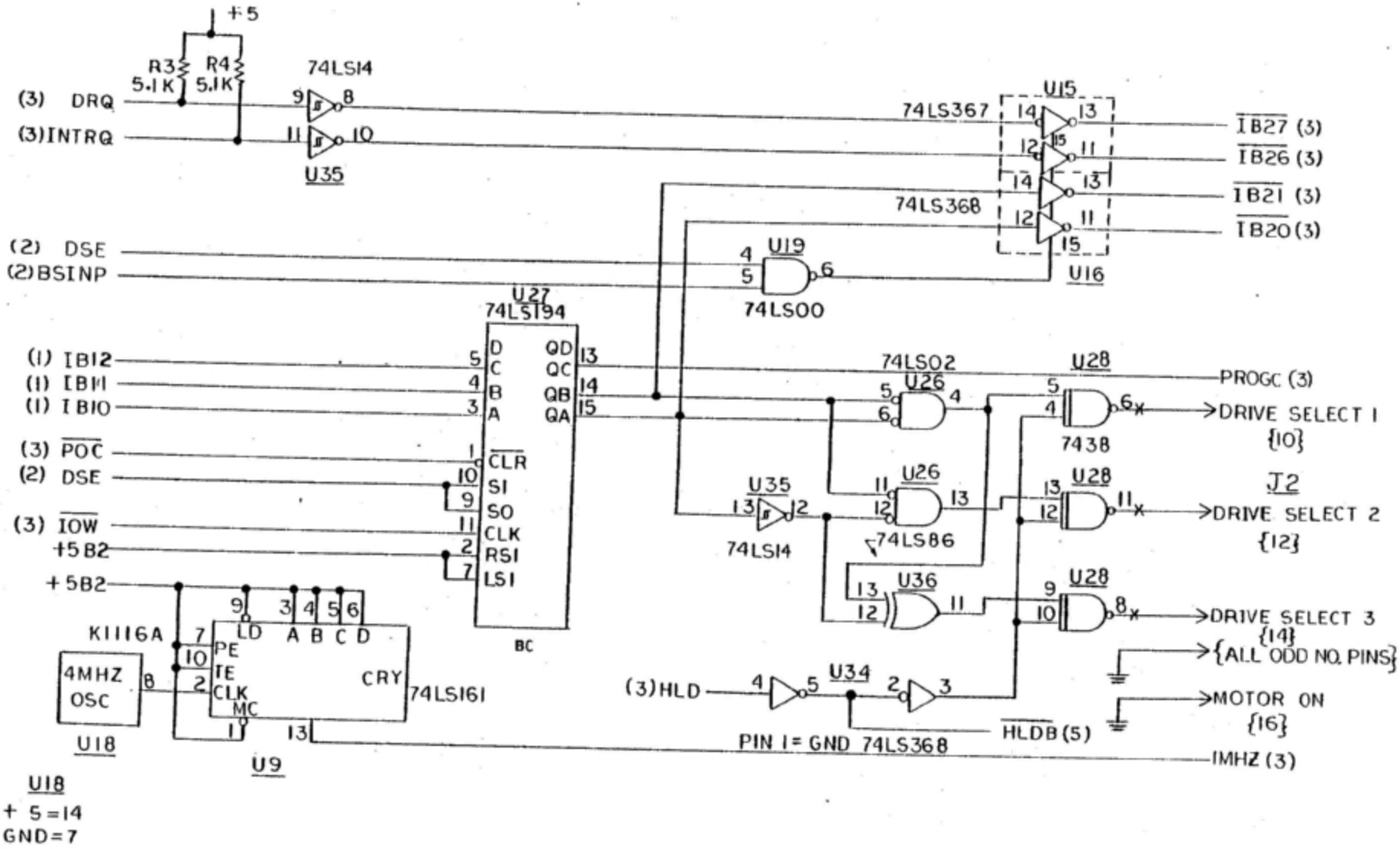



Figure 1. Controller/Interface Schematic (Sheet 4 of 6)

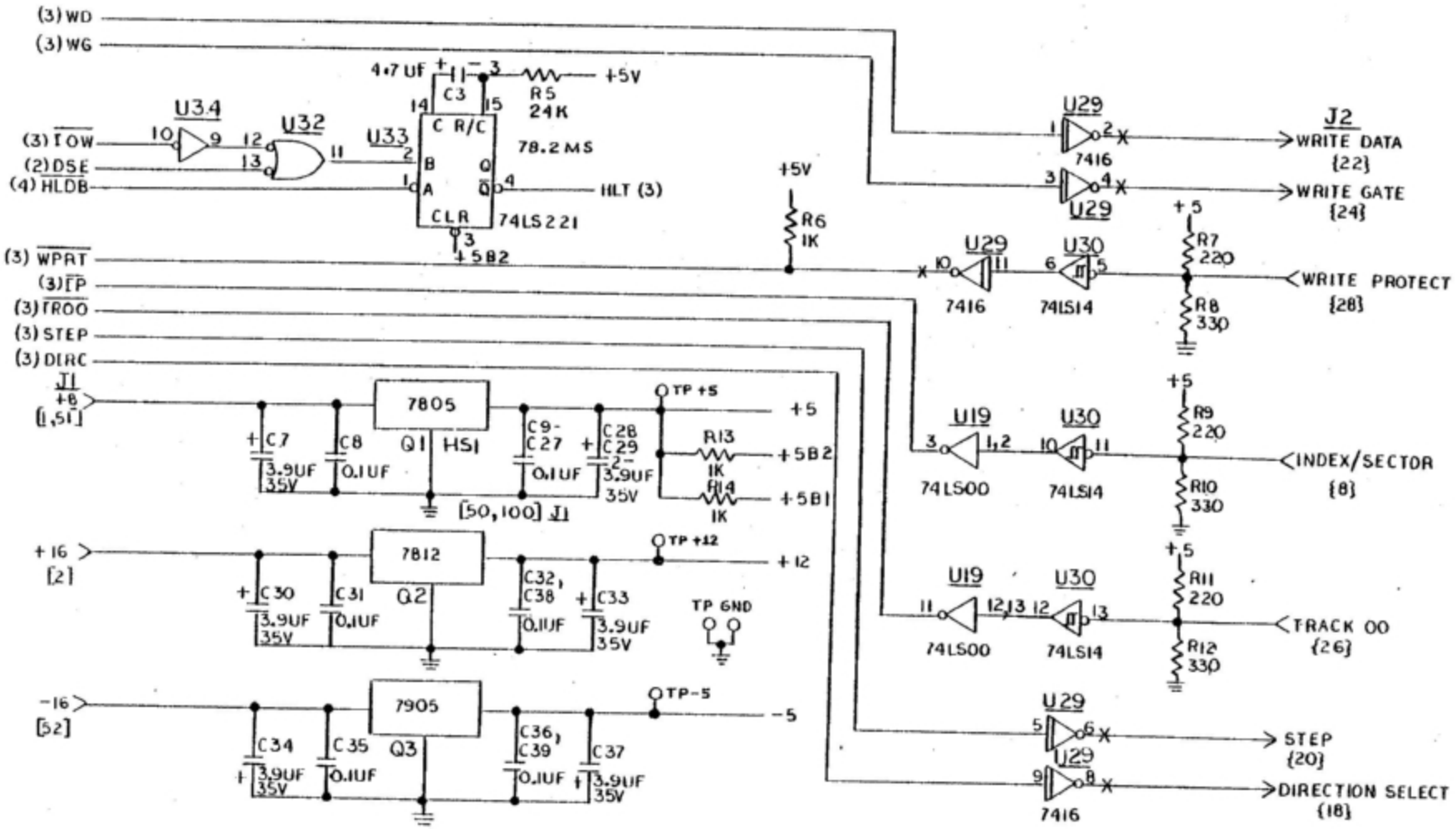



Figure 1. Controller/Interface Schematic (Sheet 5 of 6)

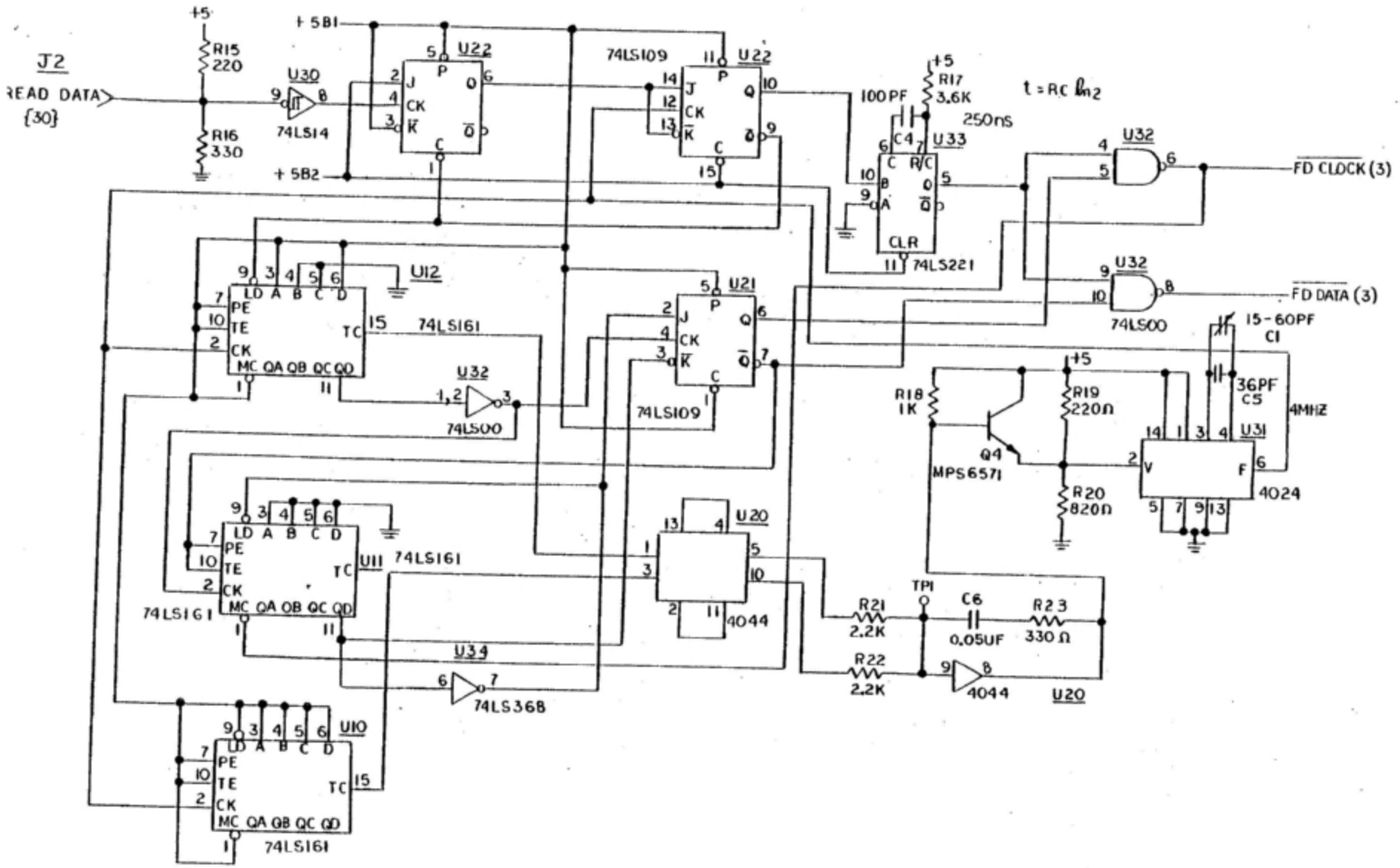
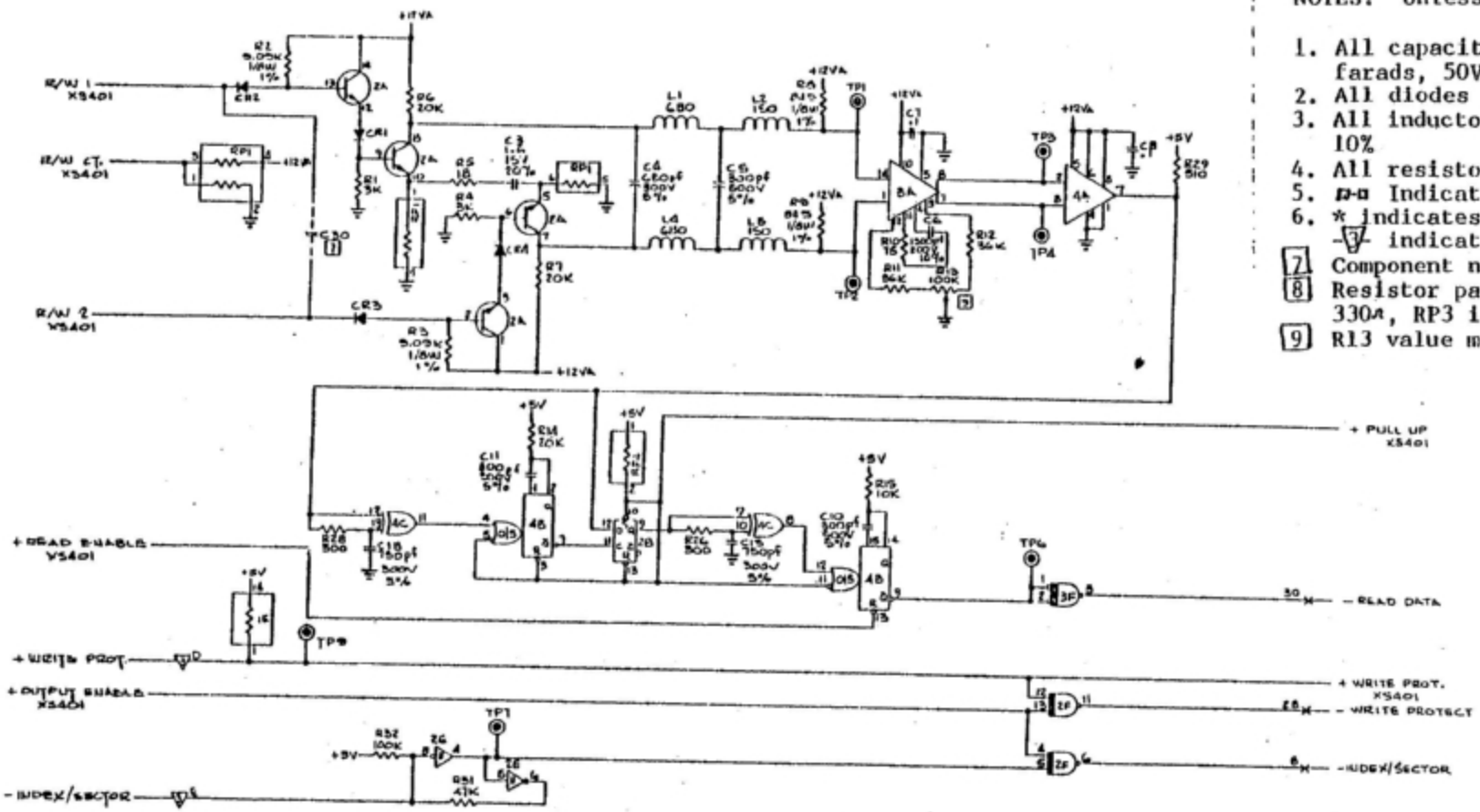
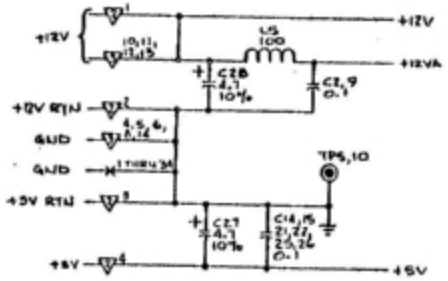



Figure 1. Controller/Interface Schematic (Sheet 6 of 6)




NOTES: Unless otherwise Specified

1. All capacitors are in microfarads, 50V,+80 - 20%
2. All diodes are IN4148
3. All inductors are in microhenries 10%
4. All resistors are in ohms ¼w 5%
5. ▫-▫ Indicates cut trace option.
6. * indicates 01, -▽- indicates J2 -▽- indicates 03, -▽- indicates J4
7. Component not installed
8. Resistor pack RP1 is 680Ω, RP2 is 330Ω, RP3 is 330Ω, and RP4 is 1K
9. R13 value may be 50K

| TYPE | POS. | UNUSED | | | | TYPE | POS. | UNUSED | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 7400 | 3E | | 14 | 7 | — | 75453B | 5F | | 8 | 4 | — |
| 7402 | 5D | | 14 | 7 | — | LM311 | 4A | | — | 1 | 8 |
| 74LS14 | 2E | | 14 | 7 | — | MC4741A | 5A | | — | 5 | 10 |
| 7407 | 2C | 2C4 | 14 | 7 | — | 7486 | 4C | 4C, 3 | 14 | 7 | — |
| 7433 | 2D | | 14 | 7 | — | 9602 | 4B,3C | | 16 | 8 | — |
| 7455 | 2F | | 14 | 7 | — | ZQTZ22 | 2A | | — | — | — |
| 7414 | 2B | | 14 | 7 | — | ZQTZ20B | 1C | | — | — | — |
| 74LS5 | 5D | | 16 | 8 | — | 150Ω | 1B | | — | — | — |
| 75452P | 1D,4E | | 8 | 4 | — | | | | | | |

| REF DESIGNATION NOT USED | REF DESIGNATION NOT USED |
|---|---|
| C30 | C19,20,23,24,29,30(RESERVED) |
| CR18 | |
| L5 | |
| Q7 | |
| R36 | |
| RP4 [8] | |
| TP12 | |

Figure 2. Disk Drive Interface Schematic (Sheet 1 of 2)

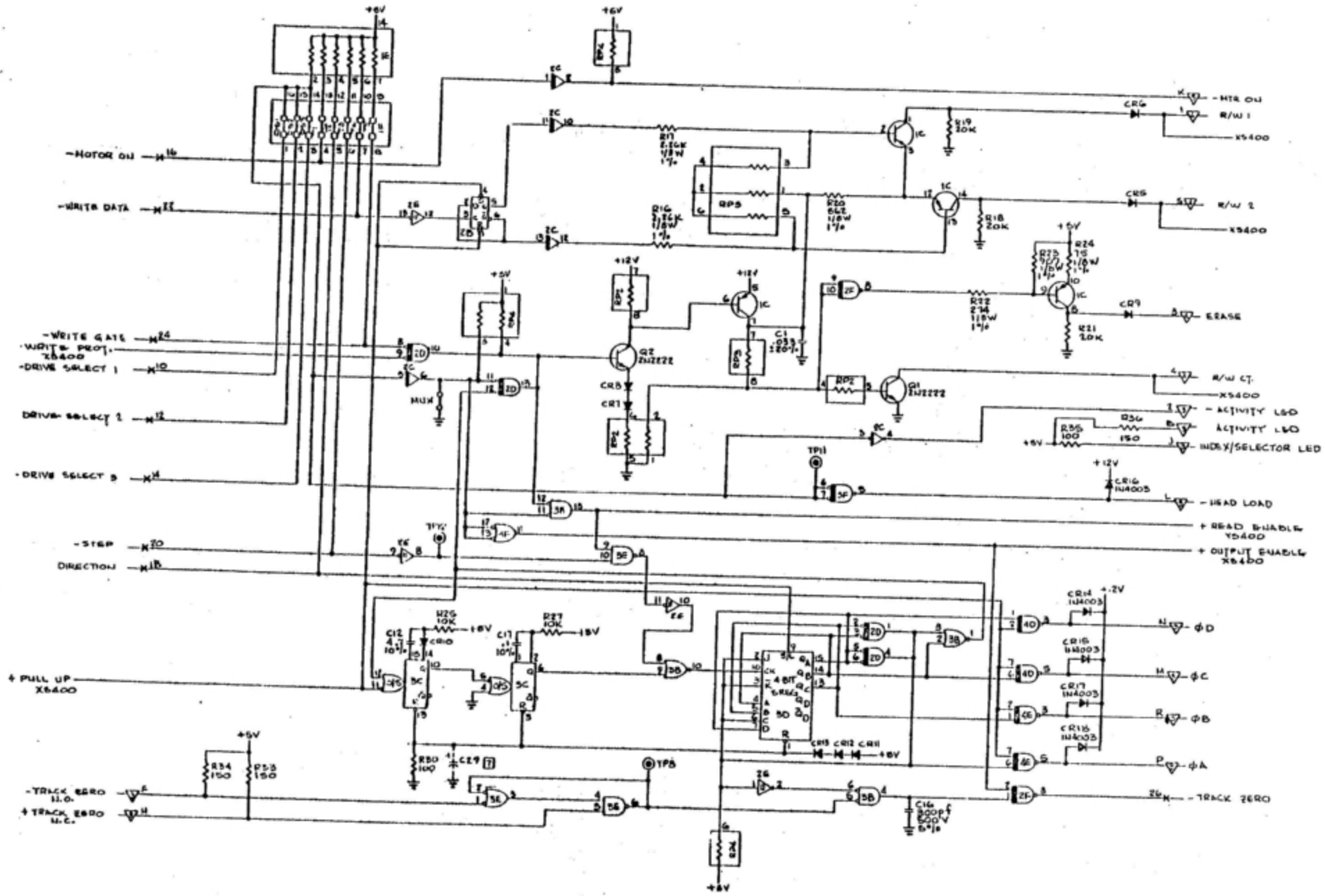



Figure 2. Disk Drive Interface Schematic (Sheet 2 of 2)

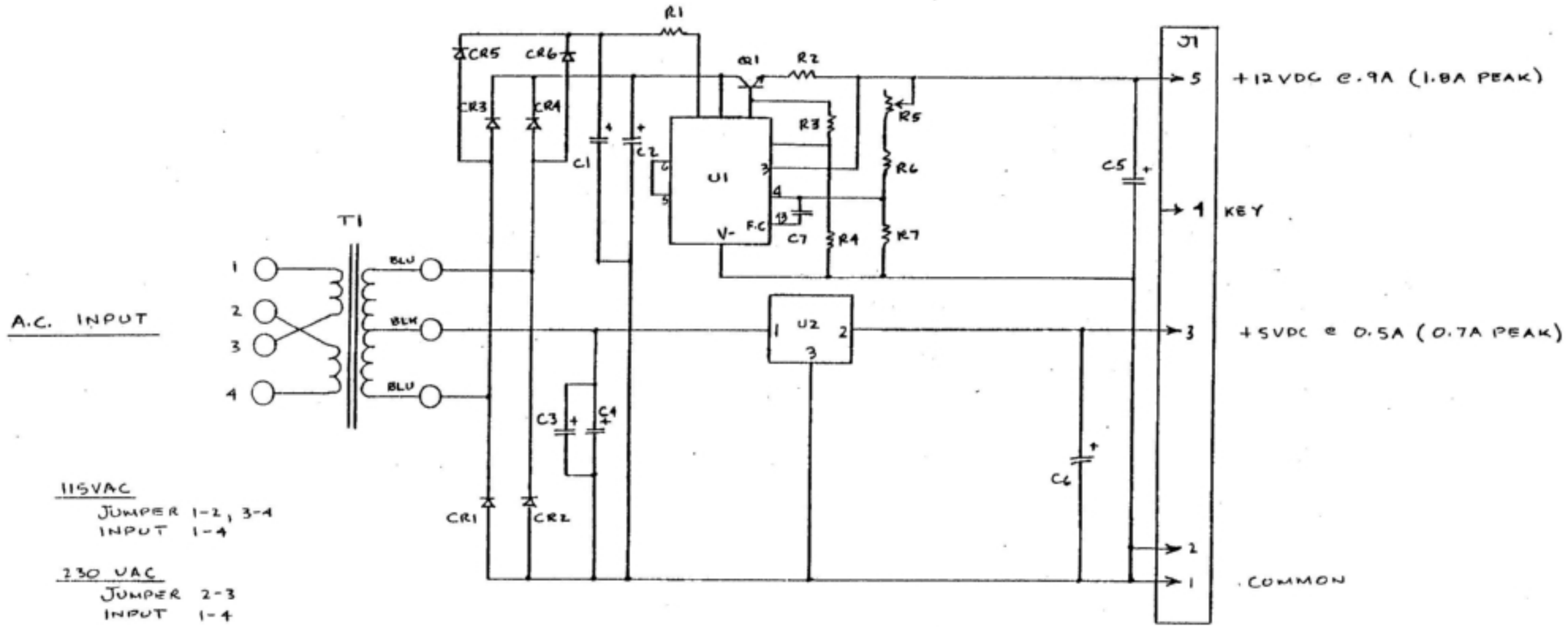
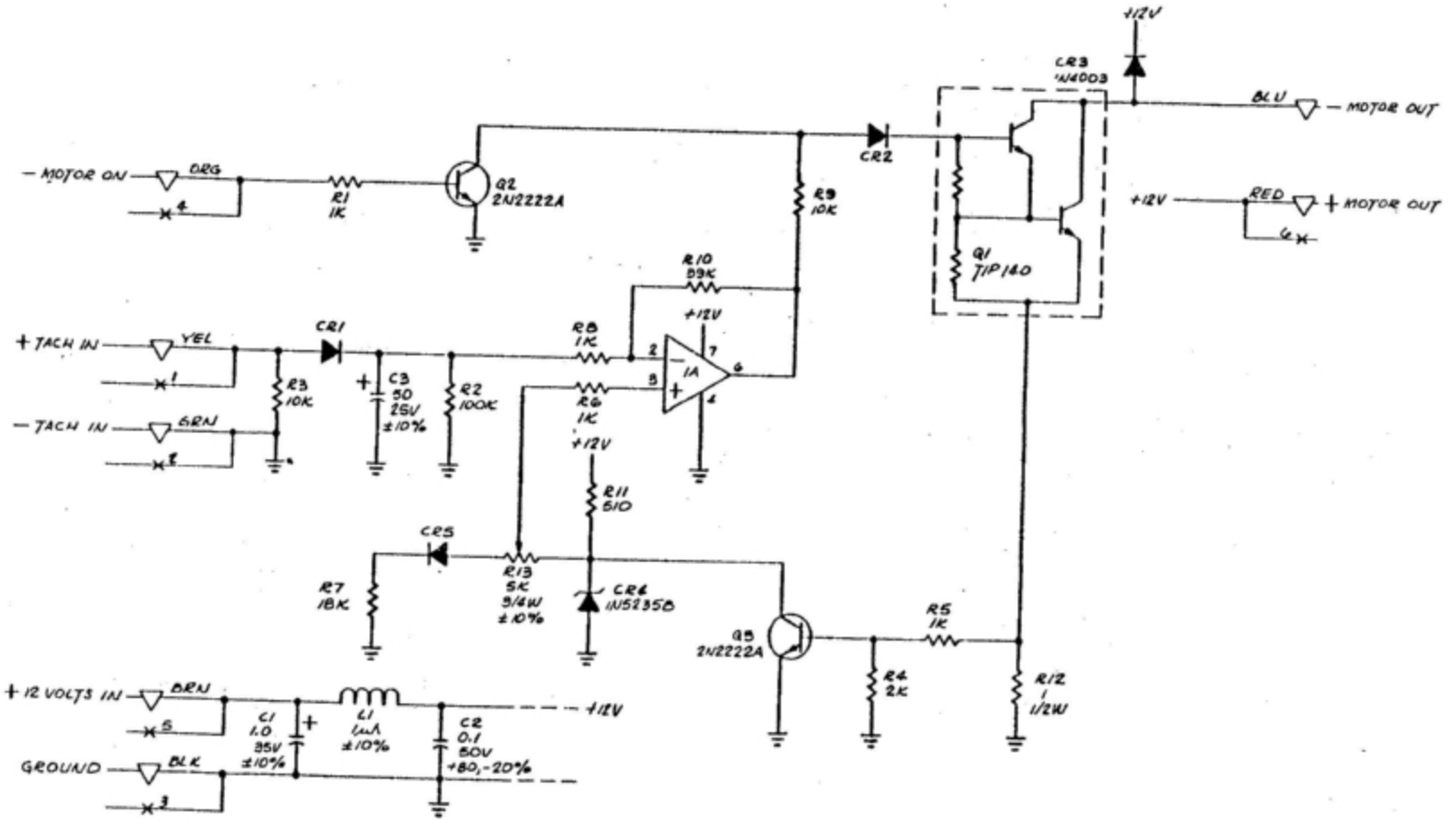



Figure 4. Power Supply Schematic

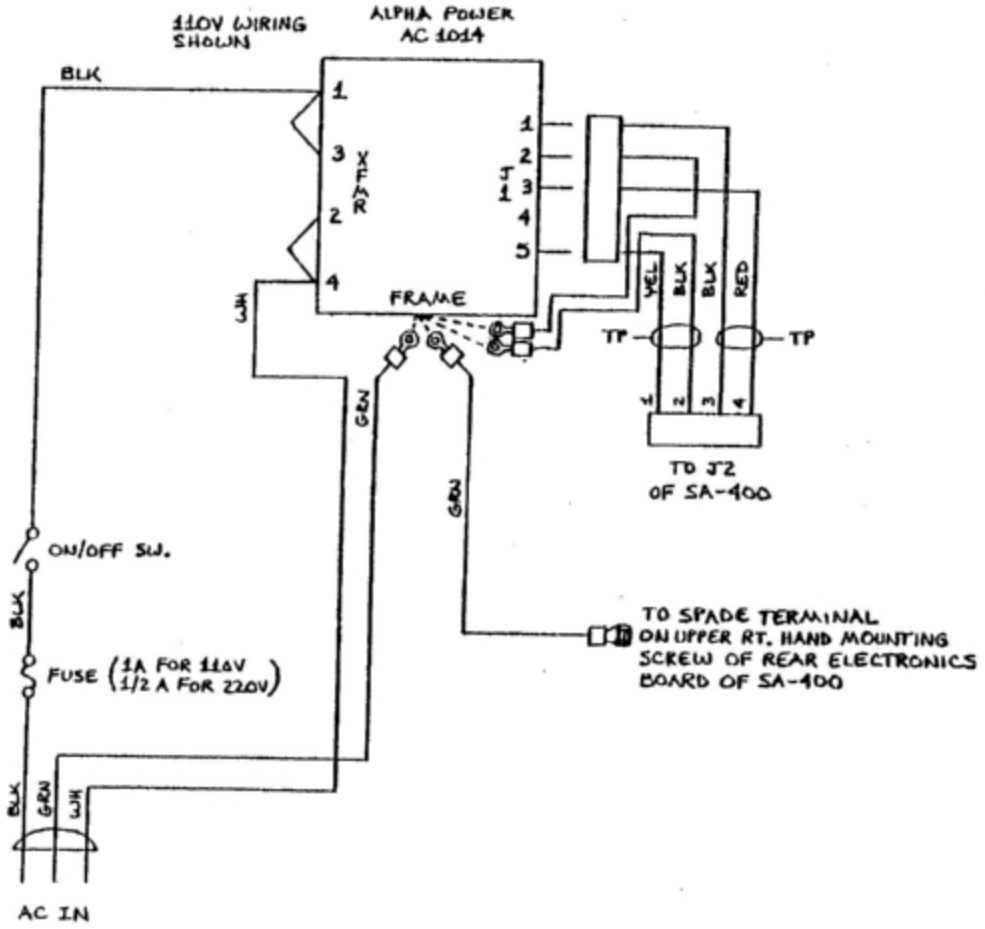


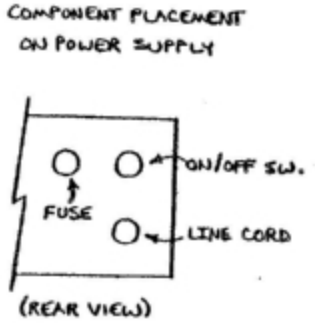

NOTES; UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL DIODES ARE IN4148.
3. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
4. ▽ INDICATES SOLDERED WIRE CONNECTION.

| REF DESIGNATION LAST USED | REF DESIGNATION NOT USED |
|---|---|
| C3 | |
| CR5 | |
| L1 | |
| Q3 | |
| R13 | |

Figure 3. Disk Drive Motor and Speed Control Schematic



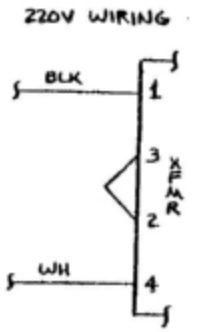




Figure 5. AC Power Schematic

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# INTERFACING GUIDE

## MODEL FD2400 SERIES

## FLOPPY DISK SYSTEM

Revision A
April, 1977

NOTICE

# INTERFACING GUIDE

## 1. INTRODUCTION

This section deals with the Microfloppy Controller/Interface iCom Part Number 200062-100. The Controller/Interface is primarily designed for the computer hobbyist, and it can accomodate up to three disk drivers and is compatible with micro computers having an Altair bus structure.

## 2. PHYSICAL DESCRIPTION

The Controller/Interface is a 5.4 x 10.0 inch (13.72 x 15.4 cm) printed circuit board containing 39 IC's.

The Controller/Interface board simply is placed into one of the available circuit board connectors.

The Interface/Controller is connected to the Microfloppy disk drive by a 34 pin ribbon cable.

The ribbon cable connector mates with J2 of the Controller/Interface. Connector J2 is located on the upper right hand corner as viewed from the components side of the Controller/Interface printed circuit board assembly.

## 3. INTERFACE SIGNALS

Signals that are routed between the Controller/Interface and the Microfloppy disk drive are TTL negative logic tristate levels.

I/O signal levels:

Logic "0": +2.4v to +5.25v
Logic "1": +0.0v to +0.40v

### 3.1 Input Signals (from Microfloppy disk drive)

Index/Sector

This signal is provided by the Microfloppy once each revolution to indicate the beginning of a track. Normally this signal is true (low) and goes false (high) with each revolution of the diskette.

Read Data

This line furnishes the clock and data bits as detected by the Microfloppy.

At its normal state this signal is a true (low) and goes false (high) when the active state is initiated.

Track ØØ

This signal indicates a true (low) when the R/W head is positioned at track zero, the outermost data track. This signal indicates a false (high) when the R/W head of the selected track is not at track zero.

Write Protect

This signal provides an indication when the write protect feature is enabled on the Diskette. This signal line goes true (low) when the diskette is write protected. The electronics in the drive are internally disabled when the diskette is write protected. To utilize this feature, cover the write-protect notch on the diskette with an adhesive tab or a piece of tape.

## 3.2 Output Signals (to Microfloppy Disk Drive)

Direction Select

The R/W head direction is determined by this signal in conjunction with STEP. If DIRECTION SELECT is true (low) and STEP is pulsed, then the R/W head will move in. An outward movement of the head is done when DIRECTION SELECT is false (high) and when STEP is present.

Drive Select 1 thru 3

These lines select the drive unit desired. In this type of operation only the drive which has an active input line will respond to the input and output lines.

Motor On

This line, when true (low), will turn on the drive motor of the Microfloppy, which allows the drive to read or write. Before reading or writing a 1 second delay must occur.

Step

This is a control signal that causes the R/W head to move in the direction as determined by DIRECTION SELECT signal.

Write Data

This signal provides data to be written on the diskette. Causes reversal of current through the R/W head if WRITE GATE is active.

Write Gate

When WRITE GATE is true (low), WRITE DATA is written on the diskette. The false (high) state of this signal allows data to be transferred from the drive and enables STEP to advance the R/W head.

## 4. CONTROLLER/INTERFACE SIGNAL LIST

The I/O signals on J1 and J2 of the Controller/Interface are given as an additional aid for the user.

### 4.1 Controller/Interface J1 Signal List

| Pin | Signal | I/O |
|---|---|---|
| 1 | +8v | I |
| 2 | +16v | I |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | | |
| 12 | | |
| 13 | | |
| 14 | | |
| 15 | | |
| 16 | | |
| 17 | | |
| 18 | | |
| 19 | | |
| 20 | | |
| 21 | | |
| 22 | | |
| 23 | | |
| 24 | | |
| 25 | | |
| 26 | | |
| 27 | | |
| 28 | | |
| 29 | A05 | I |
| 30 | A04 | I |
| 31 | A03 | I |
| 32 | A15 | I |
| 33 | A12 | I |
| 34 | A09 | I |
| 35 | D01 | O |
| 36 | DOØ | O |
| 37 | A1Ø | I |
| 38 | DO4 | O |
| 39 | DO5 | O |
| 40 | DO6 | O |
| 41 | DI2 | O |
| 42 | DI3 | O |
| 43 | DI7 | O |
| 44 | | |
| 45 | SOUT | I |

| Pin | Signal | I/O |
|---|---|---|
| 46 | SINP | I |
| 47 | SMEMR | I |
| 48 | | |
| 49 | | |
| 50 | | |
| 51 | +8v | I |
| 52 | -16v | I |
| 53 | | |
| 54 | | |
| 55 | | |
| 56 | | |
| 57 | | |
| 58 | | |
| 59 | | |
| 60 | | |
| 61 | | |
| 62 | | |
| 63 | | |
| 64 | | |
| 65 | | |
| 66 | | |
| 67 | | |
| 68 | MWRITE | I |
| 69 | | |
| 70 | | |
| 71 | | |
| 72 | PRDY | O |
| 73 | | |
| 74 | | |
| 75 | | |
| 76 | | |
| 77 | $\overline{\text{PWR}}$ | I |
| 78 | PDBIN | I |
| 79 | A0Ø | I |
| 80 | A01 | I |
| 81 | A02 | I |
| 82 | A06 | I |
| 83 | A07 | I |
| 84 | A08 | I |
| 85 | A13 | I |
| 86 | A14 | I |
| 87 | A11 | I |
| 88 | D02 | O |
| 89 | D03 | O |
| 90 | D07 | O |
| 91 | DI4 | O |
| 92 | DI5 | O |
| 93 | DI6 | O |
| 94 | DI1 | O |
| 95 | DIØ | O |
| 96 | | |
| 97 | | |
| 98 | | |
| 99 | $\overline{\text{POC}}$ | I |
| 100 | GROUND | - |

## 4.2 Controller/Interface J2 Signal List

| Pin | Signal | I/O |
|---|---|---|
| 2 | SPARE | |
| 4 | SPARE | |
| 6 | SPARE | |
| 8 | INDEX/SECTOR | I |
| 10 | DRIVE SELECT 1 | O |
| 12 | DRIVE SELECT 2 | O |
| 14 | DRIVE SELECT 3 | O |
| 16 | MOTOR ON | O |
| 18 | DIRECTION SELECT | O |
| 20 | STEP | O |
| 22 | WRITE DATA | O |
| 24 | WRITE GATE | O |
| 26 | TRACK ØØ | I |
| 28 | WRITE PROTECT | I |
| 30 | READ DATA | I |
| 32 | SPARE | |
| 34 | SPARE | |

NOTE:
All odd-numbered pins
are ground returns.