ALTAIR HARD DISK (88-HDSK)
PRELIMINARY DOCUMENTATION

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INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

This Altair Hard Disk (88-HDSK) Documentation provides a general description of the Hard Disk System and Datakeeper Controller Cards, and a detailed theory of Controller operation. System installation, operating information and troubleshooting procedures are also included.

The manual contains five sections as follows:

1. Section I includes a general description of the Hard Disk System.
2. Section II contains Hard Disk system installation and unpacking instructions.
3. Section III contains a user's or operators guide, including Hard Disk Datakeeper BASIC operation.
4. A detailed theory explanation of the Hard Disk Datakeeper Controller is found in Section IV.
5. Included in Section V is troubleshooting procedures.

1-2. SYSTEM DESCRIPTION

The Altair 88-HDSK (Hard Disk) System is designed to operate with the Altair 8800 series computer, providing a minimum of 9.9 Megabytes (Mbytes) mass storage with a maximum access time of 92 milliseconds.

The 88-HDSK Datakeeper Controller acts as the interface between the Pertec D3000 Drive and the Altair 8800 series computer. The Controller contains a bipolar microprocessor, 1K of buffer memory and communicates with the Altair 8800 series computer through two Parallel I/O Ports.

The Pertec Drive used is a D3000 type with one fixed platter (approximately 5 Mbytes) and one top loading 5440 type cartridge (approximately 5 Mbytes). The platters rotate at 2400 RPM (40 revolutions/sec) with a bit density of 2200 bits per inch, yielding a data transfer rate of 2.5 Mbits/second between the Drive and Controller. Up to 4 Drives may be "daisy chain" connected to one 88-HDSK Datakeeper Controller.

The software used with the 88-HDSK System is a special version of Altair Extended BASIC, with a file system designed to take advantage of the speed and capacity of the Pertec D3000 Drive. The software is provided on a 5440 type cartridge, and Bootstrap Loader PROMs are included for fast system initialization.

1-3. SPECIFICATIONS

A. System Components - The Altair 88-HDSK (Hard Disk) System consists of the following:

1. 88-HDSK Datakeeper Controller
2. One pair of interconnect cables for Controller to Altair 8800 connection
3. One cable assy. for Controller to Pertec Hard Disk Drive Connection
4. One Pertec D3000 type Drive (approximately 10 Mbytes) including Drive Manual
5. One 5440 disk cartridge with Altair Datakeeper BASIC
6. One set of bootstrap loader PROMs for system initialization (address 176000)
7. One set of documentation including Altair Datakeeper BASIC and 88-HDSK System Manual

B. Altair 8800 Computer Requirements - The minimum configuration for the Altair 8800 computer to be used with the 88-HDSK system is:

1. Altair 8800b Computer
2. 48K of memory (3 ea. 88-16MCS or 88-16MCD)
3. 2 parallel ports (1 ea. 88-4PIO, 1 ea. 88-PP) addressed at 160 (decimal) 240 (octal)
4. 88-PMC PROM Memory Card addressed at highest location
5. I/O Card for terminal (1 ea. 88-2SIO) addressed at 020 (octal) 16 (decimal) (specify baud rate and interface level - RS232, TTY)
6. Terminal - CRT, Teletype, etc., to match I/O Card interface

NOTE

If using the Altair 8800b Turnkey computer, the 88-PMC and 88-2SIO are not required.

C. Controller Specifications

1. Controller Configuration

The 88-HDSK Datakeeper Controller is bus oriented with a 5 slot motherboard. The power supply consists of a single 5 volt regulator with overcurrent protection that will power up to 5 plug-in boards. The circuitry is entirely TTL logic and 100% synchronous. The Controller comes with 3 plug-in boards that perform the following functions:

a. Processor Board.--Has 8X300 bipolar processor, TTL ROM, 1K of buffer RAM for data transfers, and 2 bidirectional I/O ports for communicating with the Altair 8800.

b. Disk Data Board.--Has serial/parallel-parallel/serial data converters, FIFO (First In, First Out) Registers, CRC (Cyclical Redundancy Check) generator and checker and bit counters.

c. Disk Interface Board.--Has the write data rate clock, I/O ports and line drivers for communicating with the Hard Disk Drive--24 lines in, 24 lines out. Interfaces with up to four Drives.

2. Power Requirements

70 watts typical, 120 watts maximum
Wired for 105-120V, 50/60 Hz
210-260 V, 50/60 Hz available on request.

3. Physical Specifications

Size: Height 5.3 in. (13.5 cm) Width 16.85 in. (40.5 cm)
Depth 17.3 in (41.5 cm)

Weight: 20 lbs (9.2 Kg)

Cabinet styling matches the Altair 8800b and 8800b Turnkey. A keyswitch on the front panel controls the power switch and CPU Reset and Run mode.

D. Drive Specifications

1. Drive Type: Pertec D3422-E024-NWU
2. Data Storage Capacity:

1 each fixed platter
4,988,928 Data Bytes
1 each 5440 type removable cartridge
4,988,928 Data Bytes
TOTAL 9,977,856 Data Bytes

3. Physical Format:

Tracks per inch-	200
Cylinders-	406
Disk surfaces-	4
Tracks-	1624
Sectors-	24
Data Bytes/Sector-	256

4. Serial data transfer rate - 2.5 Mbits/second, determined by:

Spindle speed: 2400 RPM
Density: 2200 BPI

5. Access Time

a. Latency - Maximum 25.0 ms ± 1%
- Typical 12.5 ms ± 1%

b. Seek Time - Minimum (Adjacent Track) 10 ms, Max.
Average (1/3 Full Stroke) 40 ms, Max.
Maximum (Full Stroke) 65 ms, Max.

c. Total maximum access time to read a Sector: 92 ms
25 ms latency
65 ms seek
2 ms read time

6. Power Requirements

   1100 watts Peak (start/stop cycle only)

   400 watts typical

   95 to 125 V or } Must specify nominal voltage
   190 to 250 V }

   48 to 52 Hz or } Must specify if normal line frequency is 50 Hz
   58 to 62 Hz }

7. Physical Specifications

Height	8-3/4 inches	(22.2 cm)
Width	19 inches	(48.3 cm)
Depth	29-1/4 inches	(74.3 cm)
Weight	130 lbs.	(59 Kg)

8. Reliability

   Meantime between failure - MTBF - 4000 hrs.

   Service life 5 years or 24,000 hrs.

   Meantime to repair - 1 hr.

9. Preventive Maintenance

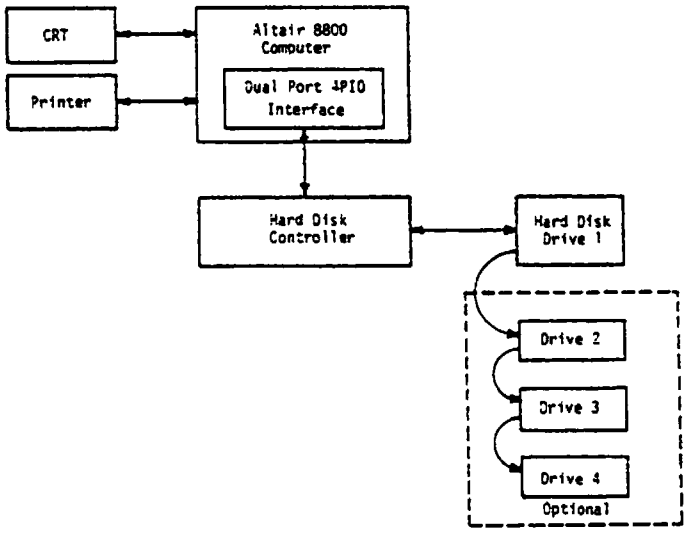
   -Alignment check is recommended after moving or every 3 months/ 1000 hrs.

   -1000 hr/3 months inspection and cleaning recommended

   -2000 hr/6 months replace air filter, inspect for wear

E. Altair Hard Disk System

1. Block Diagram of a Typical System



2. System Characteristics
   a. Drive used is a Pertec D3422
   b. 24 Sectored Format, 256 Data Bytes/Sector
   c. Disk Controller can interface up to Four Disk Drives
   d. Removable Top Loading Cartridge
   e. Storage Capacity--approximately 5 Mbytes using Fixed Cartridge, increasing to nearly 10 Mbytes using Removable Cartridge
   f. Maximum Access Time to Read Sector--approximately 92 msec (65 Seek, 25 Latency, 2 Read)
   g. Minimum Access Time for Non-Buffered Read-approximately 2 msec
   h. Average Access Time of 54.5 msec (40 Seek, 12.5 Latency, 2 Read)
   i. Maximum Single Track Seek Time of 10 msec
   j. Seeks may be overlapped with Buffer Transfers and Seeks of other Drives
   k. Data Rate from Controller to Altair 8800a or b is asynchronous with Handshaking and may vary from 0 to 2.5 Mbytes/sec
   l. 1K of Buffer Storage is provided in the Controller

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PRELIMINARY DOCUMENTATION
SECTION II
SYSTEM INSTALLATION

SYSTEM INSTALLATION

2-1. UNPACKING AND INSTALLATION OF DRIVE

The Pertec D3000 Disk Drive is shipped in a heavy duty container consisting of an inner and outer carton. Use of the dual carton minimizes the possibility of damage during shipment. Inspect the carton for obvious damage and notify the carrier if damage is noted. To uncrate the Disk Drive:

A. Place the shipping carton in the position indicated by the arrows on the outer carton.

B. Open the outer carton and remove the packing material.

C. Lift the Drive and its shipping frame and set it on a clean work surface. Ensure access to the top of the unit.

CAUTION

THE D3000 DISK DRIVE WEIGHS 130 POUNDS IN ITS SHIPPING CONFIGURATION. DO NOT ATTEMPT TO LIFT THE DRIVE WITHOUT SUFFICIENT PERSONNEL.

D. Check the contents of the shipping container against the packing slip and investigate for possible damage. Notify the carrier if damage is noted.

CAUTION

TO AVOID DAMAGE TO EQUIPMENT, DO NOT ATTEMPT TO APPLY POWER TO THE DISK DRIVE UNTIL ALL POSITIONER AND MECHANISM SHIPPING RESTRAINTS HAVE BEEN REMOVED.

After the Drive is removed from the shipping carton make sure you have the accessories that are included with the Drive. The Pertec manual, which is shipped with the Drive, is taped underneath the Drive or somewhere in the inner carton. If the manual is not with the unit, notify MITS immediately because it is an important part of the Drive check out and operation. Another important accessory is the chassis slide set for mounting the Pertec D3000 Drive in a rack. If it is not in the carton, contact MITS for immediate replacement.

Disassemble the cover of the Drive and inspect the circuit boards and the wiring for loose wiring and connectors. Refer to sections 5 through 10 on pages 2-1 and 2-2 of the Pertec Drive manual, concerning top loading Drives.

Read pages 2-3 through 2-8 of the Pertec D3000 manual covering compo-

nent identification pictures and the initial check out procedure. The Drive should be left in the shipping rack or shipping frame until a complete checkout of the unit is completed. This not only includes the preliminary or initial checkout procedure, but complete testing of the Drive with the Datakeeper Controller before it is mounted in its final unit. During the checkout procedure it is required that the user install the top-loading cartridge. The procedure is explained in paragraph 3.4.3 which is on page 3-5 of the Pertec D3000 Manual. Essentially it consists of removing the bottom cover from the top-loading cartridge, inserting the cartridge in the position in the top of the Drive and replacing the original bottom cartridge cover on top of the cartridge.

The Drive interconnect cable supplied with the Altair Datakeeper Controller consists of two 50 conductor cables which are wired to a PC board with a 100-pin PC board connector; 50-pins on each side. This PC board plugs into socket J101 which is adjacent to a terminator board. If this is a single Drive system, the terminator board remains in the socket J102. If the Drive is an intermediate Drive in a daisy chain system, the terminator board in socket J102 should be removed. If the Drive is the end Drive or the last Drive in a daisy chain configuration, the terminator board remains in J102. When the system is completely checked out, refer to page 2-11 of the Pertec D3000 Drive Manual for information on rack mounting the Disk Drive. Due to the sensitivity of the Drive to dust and dirt, it is recommended the Drive not be mounted lower than 2 feet above the floor.

2-2 UNPACKING AND INSTALLATION OF CONTROLLER

Inspect the carton for obvious damage and notify the carrier of any damage. The following items should be included with the Controller package: Two 26 conductor cable assemblies consisting of a six foot cable, a 26-pin bulk head connector and an 18 inch cable with a 25-pin D type connector. Also included is a Drive interconnect cable assembly consisting of two 50 conductor cables connected to a Drive connector board, a top-loading cartridge containing the system operating software and a Bootstrap Loading PROM for use in the Altair 8800b computer. Check these items against the packing list; and if any of these items are missing, please notify MITS immediately.

After identifying the contents of the package, perform an inspection of the P.C. cards in the Controller. To inspect the Datakeeper Controller, remove the case top which is held by two number 6-32 screws and remove the cable cover on the back panel.

Be sure all the components and ICs are in place and there is no internal damage in the Controller itself. The Controller has three plug-in PC cards approximately 8" x 10". The Processor Card is identified by the large 50-pin IC near the center of the board. There are 16 IC sockets near the edge connector of the PC board and there should be two IC chips installed; one in position E and one in position N. This is the Read Only Memory (ROM) array, and these two chips supply all the required Read Only Memory for the system. The other 14 ROM sockets should be empty. The remaining ICs should be in place in the board. There are two 26-pin connectors on one end of the board labelled P1 and P2. P1 is color coded with a brown dot and a blue dot. P2 is color coded with a red dot and a blue dot. These color dots indicate orientation of the connector cables that go to the 4PIO PC Card in the computer (interconnection is described in paragraph 2-4). The Disk Data Card has several large ICs on it, and all sockets have ICs in them. There are no interface connectors on this card. The Disk Interface Card has two 50-pin connectors on one end. Connector 1 is identified by a brown dot and a green dot, and connector 2 is identified by a red dot and a green dot. These colored dots indicate proper cable orientation for the Disk Drive connector cable. All sockets on the Disk Interface Card should have ICs. Check the three cards to insure that all the ICs are properly seated in their sockets and there is no damage to the components.

The controller motherboard is bus oriented, meaning that these three cards may be installed in any order and position. The controller Power Supply should be checked with the cards installed. This is done by plugging the AC cord in and turning the key switch to reset. Both AC power and DC power LED's should turn on. Turn off the power and connect the connector cables to the Processor Card, noting the correct orientation as indicated by the color coded dots. These two cables will be connected to the 4PIO Interface Card in the Altair 8800 in the next section. Also connect the two 50 conductor cables to the Disk Interface Card again noting proper orientation as indicated by the color coded dots. At this point install the three cards in the Controller. Turn the power switch to ON and the lights should stay on. The power supply in the Controller has an over current protection circuit which shuts the DC power off under abnormal load conditions. If the circuit is triggered, the DC power light will go out and must be reset by turning the power switch to OFF and back to ON. For the system checkout leave the case top and cable cover off the unit.

2-3. ALTAIR 8800b SET-UP

The minimum configuration for the Altair computer to be used with the Hard Disk System is 48K of memory, 2 parallel ports and 88-4PIO addressed at 240 octal (160 decimal). Also required is one 88-PMC PROM memory card addressed at the highest location and an I/O card wired to match the user's terminal for I/O data rate and standard. The I/O card is normally a 2SIO wired for addresses 20 and 21 octal. Install the PROM Bootstrap Loader IC in PROM socket E of the 88-PMC PROM Memory Card. This is verified by plugging in the card, turning the computer on, and examining addresses starting at 176000 (374000). If the board is incorrectly addressed, the data lights indicate all logic 1's (all HIGH). Consult the 88-PMC Manual for correct installation if difficulties are encountered. If using the Altair Turnkey B computer, use the Turnkey Module Board for the I/O port and the PROM connection. Consult the Turnkey Module instructions for addressing the 1K RAM and the I/O port. Use PROM socket L1 and address PROM switch to 374000.

2-4. INTERCONNECTION OF THE SYSTEM

Good grounding of all the chassis units is required. It is essential that the AC power supplied to the units is noise free and has a good ground connection. If in doubt, connect all chassis to a cold water pipe. First, connect the two ports of the 4PIO Card to the cable coming from the Processor Card of the Datakeeper Controller. Port 1 connects to the brown and blue dotted connector. If the Drive connector is not already connected to the Drive, plug it in with the nomenclature on the PC board facing the outside. The PC board is attached to the chassis with two number 8-32 screws, each screw having a number 8 lockwasher underneath it. The Drive address must be set on the front of the Drive by a thumbwheel switch. For a single Drive system, the switch is set at 1. For a multiple Drive system: use 1 and 2 for a two Drive system; 1, 2 and 3 for a three Drive system; or 1, 2, 3 and 4 for a four Drive system. The Drives may be connected in any order but each Drive address must be unique.

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SECTION III
USING THE SYSTEM

3-1. GENERAL OPERATING INFORMATION

By far the most important thing to keep in mind when using the Datakeeper Controller with the Hard Disk Drive is to keep the operating area clean. This includes no smoking. The Hard Disk Drive is extremely sensitive to dirt, dust and smoke. Although the Hard Disk Drive has an excellent filtering system, it is possible for a small dust or smoke particle to cause a head crash, which requires a very expensive and time consuming repair procedure. The heads on the Hard Disk Drive do not touch the recording surface of the Disk Platters. They float approximately 100 microinches (2.54 micrometers) above the surface of the platter. Figure 3-1 shows the relative size of dirt particles to the height of the Read/Write head.

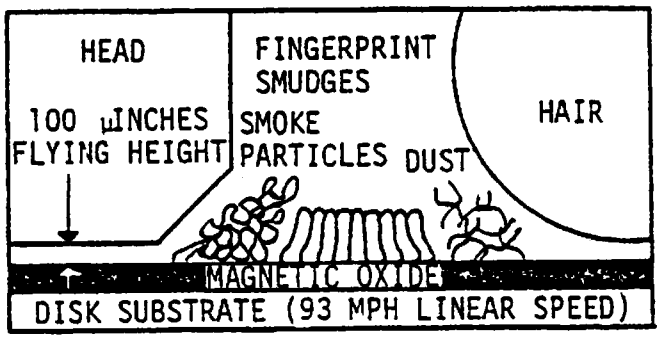

Figure 3-1. Head Sensitivity

Periodic preventive maintenance is required to insure maximum data integrity and minimum down time. It is recommended that the removable Disk Cartridges be cleaned periodically. There are several companies marketing Disk Cartridge cleaning equipment. Typically it can cost as much as 10 to 12 dollars if the Disk Cartridges are cleaned by an outside service. There are several ways to clean your own Cartridge. The Tex Wipe company manufactures relatively inexpensive cleaning equipment and instruments; and another company, Innovative Computer Products, manufactures a line of automatic Disk Cartridge cleaning equipment.

When turning the system on and off, the Datakeeper Controller is always turned on before the Disk Drive is turned on, and the Disk Drive is always turned off before the Datakeeper Controller is turned off. This will prevent the emergency unload condition and insure an orderly shut down of the system. The sequence for turning on the system is:

A. Turn on the Altair Computer
B. Turn the Datakeeper Controller switch to RESET
C. Turn the Disk Drive Power Switch to ON (wait for the safe light to come on)
D. Depress the RUN/STOP switch (the Drive motor can be heard starting)

After approximately one minute, the RUN/STOP switch should light up along with the READY light indicating the Disk Drive is properly enabled and powered for data transfers. Before enabling the Bootstrap Loader in the Altair, actuate the Datakeeper Reset switch to RUN. If you are using the system with an 8800 Turnkey B, the Disk Drive should be enabled and the Datakeeper set to RUN before turning on the Turnkey B since the first action of the Turnkey B is to activate the Bootstrap Loader after power is turned on.

To minimize errors due to static electricity, anti-static spray is recommended for carpets in the operating area.

3-2. INITIALIZATION OF SYSTEM

The following is a step by step procedure for initializing the 88-HDSK system for use with the 8800b computer:

A. Install the Datakeeper BASIC cartridge in the Drive following the recommended procedure in section 3.4.3 of the D3000 manual.

B. With the Altair computer power off, install the Boot Loader PROM (identified by the label HD-LDR, 103292) in the lowest section of the 88-PMC (IC E), with the 88-PMC wired for the highest address. The Boot Loader PROM address is 176000 octal (374000).

C. Connect the system as described in section 2-4.

D. Power the system up as described in the previous section, 3-1.

E. Examine location 176000, set sense switches as required, and RUN.

To initialize the 88-HDSK System when using the Turnkey B Computer, follow these instructions:

A. Install the Datakeeper BASIC cartridge in the Drive following the recommended procedure in section 3.4.3 of the D3000 manual.

B. With the Turnkey B Computer power off, install the Boot Loader PROM (identified by the label HD-LDR, 103292) in the Turnkey Module (I.C. L1) and set the auto start address to 374000. Set the 1K memory address to an unused area of memory (i.e., 48-49K).

C. Connect the system as described in Section 2-4.

D. Power the system up as described in Section 3-1, and it will automatically start at location 176000 (374000).

3-3. 88-HDSK TERMINOLOGY

The unit is the physical Disk Drive. There are up to four physical Disk Drives attached to the Hard Disk System. The unit address is from zero to three and corresponds to the switch settings 1 through 4 on the front of the physical Drive. Unit zero is physical Drive 1, unit one is physical Drive 2, unit two is physical Drive 3 and unit three is physical Drive 4. No two units within a Hard Disk System may have the same address.

Each unit contains from one to four physical platters. A platter, in this case, is a flat, circular oxide coated sheet of aluminum upon which

magnetic data is recorded. In some units the platters are fixed within the unit and may not be removed. These are called fixed platters or fixed cartridges. In other units one platter may be removed. This one is called the removable platter or removable cartridge.

The Pertec D3422 Drive supplied with the system contains one fixed platter or one removable platter. Pertec Drives that may be used in addition to the D3422 Drive are the D3412 Drive (one removable platter) and the D3462 Drive (3 fixed and 1 removable platter).

Each platter within the Hard Disk System is called a logical Drive and has two head surfaces. Referring to Figure 3-2 a unit containing the D3422 Drive may contain up to two platters, one removable platter and one fixed platter. The individual head surfaces of a platter are divided into 24 sectors (0 through 23), each containing 406 cylinders. A sector is defined by the rotational position of the head assembly and a cylinder by the radial position of the head assembly. The sectors in each logical Drive are called pages; each page containing 256 bytes of data. There are 19,488 pages (numbered 0 through 19,487) per logical Drive and 38,976 pages for each sector. Thus, a Drive unit contains a little less than 10 million bytes of usable data (see example in Table 3-A).

In allocating space on a Drive, pages are allocated in groups of eight, so the term group corresponds to a set of eight pages.

Table 3-A. Total Usable Bytes for D3422 Drive

4(surfaces) x 24(sectors) x 406(Cylinders) = 38,976(pages per sector)
38,976(pages per sector) x 256(data bytes per page) = 9,977,856(Total Usable Bytes)

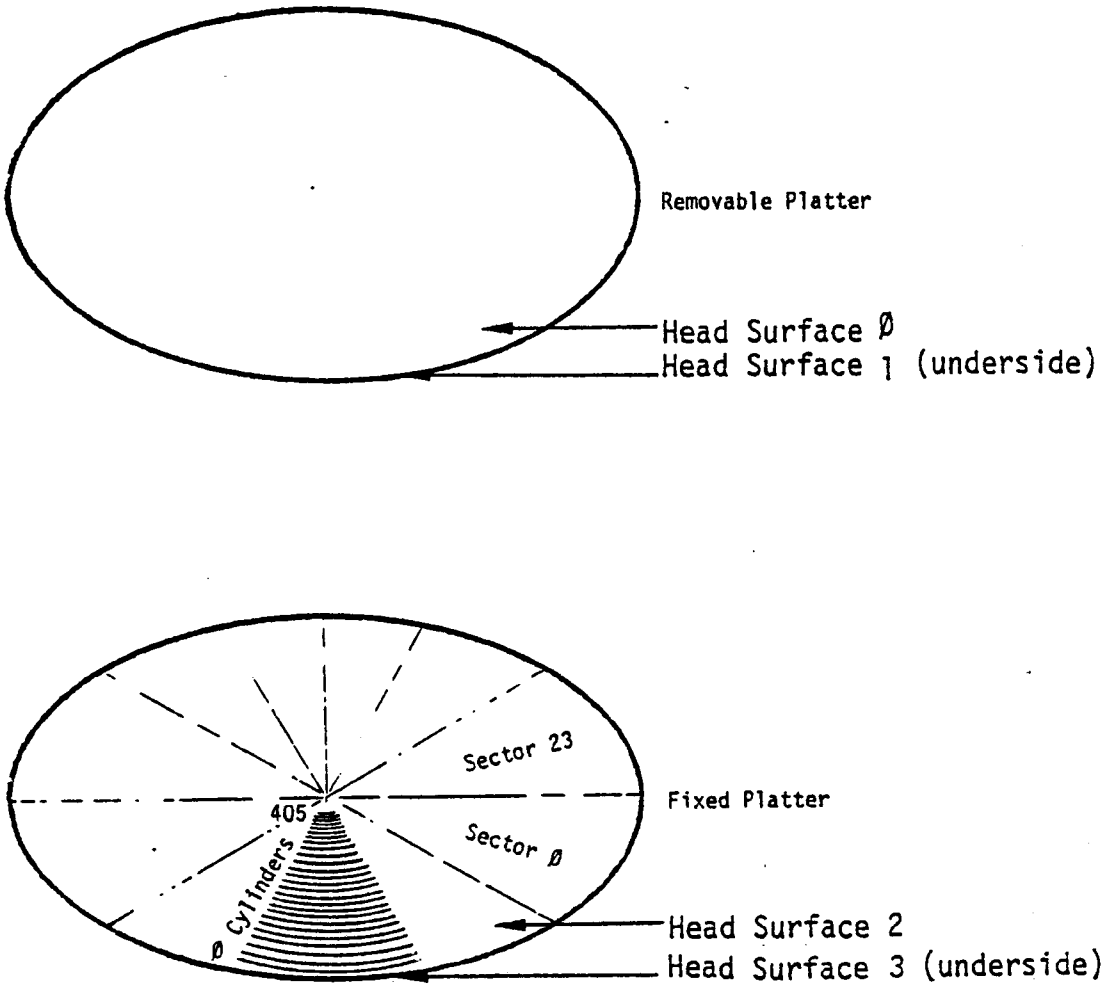

Figure 3-2. Platters For D3422 Drive

3-4. ASSEMBLY LANGUAGE OPERATION

There are seven currently defined commands which may be issued to the Datakeeper Controller. There is the command to Seek To A Cylinder whose parameters are unit address 0 through 3, and the cylinder address which is between 0 and 405 (the command addresses are described in Table 3-B). Cylinder is the term corresponding to the radial position of the head assembly.

The second command is Read Sector whose parameters are unit address 0 through 3, head address 0 through 7, sector address 0 through 23 and buffer address 0 through 3. The head address (0 through 7) corresponds to the selected surface of the respective platter for Read or Write operations. The buffer address (0 through 3) determines which of the four data buffers is to be used during a transfer (buffer size 256 bytes). The sector address ranges from 0 through 23 and corresponds to the 24 addressable sectors per cylinder.

The Write Sector command is the third command. The parameters are unit number 0 through 3, head number 0 through 7, sector 0 through 23 and buffer number 0 through 3.

For these three commands the range on the head number may be restricted when accessing units with less than four platters. Thus, the head range of a Drive containing only one platter is 0 through 1, two platters is 0 through 3 and four platters is 0 through 7.

The fourth command is the Read Buffer command. The parameters are buffer number 0 through 3 and the transfer length 0 through 255 (transfer length = n-1; n=# of databytes).

Write Buffer is the fifth command. The parameters are buffer number 0 through 3 and transfer length 0 through 255. Note that a value of 0 in the transfer length implies a transfer of 256 bytes.

The next command is a Status Check whose parameters are Unit number 0 through 3 and status word address 0 through 255. Note that the Status Word address should correspond to the address of one of the IV Bytes within the Datakeeper Controller system (see IV Byte Functions, Table 3-D).

The last command, Set Byte, outputs data to (IV byte) I/O Port for control of IV bytes outputs. The parameter is the IV byte address (see IV Byte Functions, Table 3-D).

Table 3-B. Command Addresses

Drive Unit Address	=	0-3 (corresponds to 1-4 on Drive)
*Head Address	=	0-7 (Fixed is 2,3; Removable is 0,1)
Buffer Address (1K memory on Processor Card)	=	0-3 (each is 256 bytes)
Sector Address (Rotational position)	=	0-23 (each is 256 bytes)
Cylinder Address (Radial Position)	=	$0\text{-}405_{10}$
**IV Byte Address	=	0-255 addr used 1-7, 17-22, 34-37

*See Table 3-E, page 42, for further definition of head address.

**See Table 3-D, page 24, for further definitions of IV Byte functions.

Each of these commands is transferred on the 16 bit command and data path from the computer to the Controller. The least significant 8 bits of the command are transferred on 4PIO channel 167 and the most significant 8 bits are transferred on 4PIO channel 163. The order of transfer must be the least significant 8 bits first followed by the most significant 8 bits when the Controller is ready to accept the command.

Bits 0 through 8 of the Seek Command indicate the cylinder address, 0 through 405. Bit 9 is not used. Bits 10 and 11 indicate the unit number 0 through 3. Bits 12, 13, 14 and 15 must be 0, indicating the Seek command type.

The Read Sector command bits, 0 through 4, indicate the sector number with a value of 0 through 23. Bit 5, 6 and 7 indicate the head number, 0 through 7 and bits 8 through 9 indicate the buffer number, 0 through 3. Bits 10 and 11 indicate the unit number 0 through 3. Bits 12 and 13 must be ones and bits 14 and 15 must be zeros, indicating the Read Sector command type. The command for Write Sector is the same as the command for Read Sector, except that bit 13 must be zero rather than one.

The Read Buffer command format has bits 0 through 7 indicating the transfer length 0 (MSB) through 255 (LSB), bits 8 and 9 indicating the buffer number 0 through 3, bits 10 and 11 not used, bit 12 HIGH, bit 13 LOW, bit 14 HIGH and bit 15 LOW.

The Write Buffer command has the same format as the Read Buffer command except that bit 12 must be zero for the Write Buffer command type. Note that the transfer length again has a value of 0 to imply a 256 byte transfer.

The next command is a Read Status command, where bits 0 through 7 indicate the status word address, bits 8 and 9 are not used and bits 10 and 11 indicate the unit number 0 through 3. Bit 12 is zero, bit 13 is one, bit 14 is one and bit 15 is zero, indicating the Read Status command type.

The last command is Set Byte. Bits 0-7 indicate the IV Byte address to be written, bits 8-11 not used, bits 12-14 are 0s and bit 15 is equal 1.

The diagrams in Paragraph 3-5, Section B illustrates the bit settings more fully.

The 4PIO must be properly initialized for communication with the controller. See Table 3-C for initialization procedure.

Table 3-C. 4PIO Initialization

	Clear Registers	Set Direction	Set Registers
Port 1A	OUT 160,Ø	OUT 161,Ø	OUT 16Ø,44
Port 1B	OUT 162,Ø	OUT 163,255	OUT 162,36*
Port 2A	OUT 164,Ø	OUT 165,Ø	OUT 164,44
Port 2B	OUT 166,Ø	OUT 167,255	OUT 166,44

*CB2 will hold LOW until CB1 is strobed.

Table 3-D. 8T32 BYTE FUNCTIONS

Processor Card

IV Byte X (Address 1) - Output Mode

IV Bit-Pin	User Data Bit-Pin	Line Designation	General
0 16	0 8	RAM Address Bit 9	Selects 1 of 4,256 byte data buffers
1 17	1 7	RAM Address Bit 8	
2 18	2 6	IV Byte A11 Direction Control	
3 19	3 5	IV Byte A10 Direction Control	
4 20	4 4	IV Byte A13 Direction Control	
5 21	5 3	IV Byte A12 Direction Control	
6 22	6 2	IV Byte A9 Direction Control	
7 23	7 1	IV Byte A8 Direction Control	

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IV Byte A8 (Address 2) is used for communicating error conditions to the computer, as part of 88-HDSK communications. (The General comment for this IV Byte is incorrect.)

IV Byte A8 (Address 2) - Output Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General [IN 161]
0	16	0	8	P1 - PA7	
1	17	1	7	P1 - PA6	
2	18	2	6	P1 - PA5	
3	19	3	5	P1 - PA4	These data lines are
4	20	4	4	P1 - PA3	not used in 88-HDSK
5	21	5	3	P1 - PA2	communication
6	22	6	2	P1 - PA1	
7	23	7	1	P1 - PAØ	

IV Byte A9 (Address 3) - Input Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General [OUT 163]
0	16	0	8	P1 - PB7	
1	17	1	7	P1 - PB6	
2	18	2	6	P1 - PB5	
3	19	3	5	P1 - PB4	Signals from Altair
4	20	4	4	P1 - PB3	to controller upper
5	21	5	3	P1 - PB2	8 bits of command
6	22	6	2	P1 - PB1	instruction
7	23	7	1	P1 - PBØ	

IV Byte A12 (Address 6) - Output Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General [IN 165]
0	16	0	8	P2 - PA7	
1	17	1	7	P2 - PA6	
2	18	2	6	P2 - PA5	
3	19	3	5	P2 - PA4	Signals from controller
4	20	4	4	P2 - PA3	to computer Read Data
5	21	5	3	P2 - PA2	or Controller Status
6	22	6	2	P2 - PA1	
7	23	7	1	P2 - PAØ	

IV Byte A13 (Address 7) - Input Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General [OUT 167]
0	16	0	8	P2 - PB7	
1	17	1	7	P2 - PB6	
2	18	2	6	P2 - PB5	
3	19	3	5	P2 - PB4	Signals from controller
4	20	4	4	P2 - PB3	to computer Write Data,
5	21	5	3	P2 - PB2	Setbyte Data, or lower
6	22	6	2	P2 - PB1	8 bits of command
7	23	7	1	P2 - PBØ	instruction

IV Byte A10 (Address 4) - Output Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	P2 - CB1	Strobed LOW by controller when ready for write data or LOW command byte Xfer (sets bit 7 HIGH, Port 166).
1	17	1	7	P2 - CA1	Strobed LOW by controller when ready for read data byte or status byte Xfer (sets bit 7 HIGH, Port 164).
2	18	2	6	X	
3	19	3	5	X	
4	20	4	4	X	
5	21	5	3	X	
6	22	6	2	P1 - CB1	Strobed LOW by Controller to acknowledge command (sets Bit 7 HIGH, Port 162).
7	23	7	1	P1 - CA1	Strobed LOW by Controller when ready for new command (sets Bit 7 HIGH, Port 160).

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IV Byte A13 (Address 7) provides signals from the computer to the controller, either Write Data, Set Byte data, or the lower 8 bits of a command instruction. (The General comment for this IV Byte has the data direction incorrect.)

IV Byte A11 (Address 5) - Input Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	P2 - CB2	Strobed LOW by computer when writing to 167.
1	17	1	7	P2 - CA2	Strobed LOW by computer when reading Port 165.
2	18	2	6	X	
3	19	3	5	X	
4	20	4	4	X	
5	21	5	3	X	
6	22	6	2	P1 - CB2	Latched LOW by computer when write to 163-reset HIGH when CB1 strobed (Port 1) by Controller
7	23	7	1	P1 - CA2	Strobed by computer when read 161-not used

NOTE: X = NOT USED

Disk Data Card

IV Byte B (Address 34) - Output Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation		General
0	16	0	8	DØ	HIGH 4 bits (IC F)	Write Data to FIFO registers
1	17	1	7	D1		
2	18	2	6	D2		
3	19	3	5	Q3		
4	20	4	4	DØ	LOW 4 BITS (IC M)	
5	21	5	3	D1		
6	22	6	2	D2		
7	23	7	1	D3		

IV Byte A (Address 33) - Input Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation		General
0	16	0	8	QØ	HIGH 4 BITS (IC F)	Read Data to FIFO Registers
1	17	1	7	Q1		
2	18	2	6	Q2		
3	19	3	5	Q3		
4	20	4	4	QØ	LOW 4 BITS (IC M)	
5	21	5	3	Q1		
6	22	6	2	Q2		
7	23	7	1	Q3		

IV Byte C (Address 35) - Input Mode

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Load pulses (enabled one at a time)	Used to Set Bit Counters for # of bits to be transferred during a Read or Write
1	17	1	7		
2	18	2	6		
3	19	3	5		
4	20	4	4	Data to be loaded into bit counter	
5	21	5	3		
6	22	6	2		
7	23	7	1		

IV Byte D (Address 36) - Input Mode (used for status)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	X	
1	17	1	7	X	
2	18	2	6	X	
3	19	3	5	DRDST	Check after read sector HIGH = CRC error
4	20	4	4	X	
5	21	5	3	DRDST	
6	22	6	2	DTRCMP	Data transfer complete when HIGH, indicates end of sector data
7	23	7	1	TRR	Transfer request-when HIGH, requests data byte transfer

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1. IV Byte C (Address 35) is Output Mode (not Input Mode, as written.)
2. IV Byte D (Address 36): the DRDST bit (the CRC test result for reads) is only on IV Bit 5 (pin 3). (It is not available on IV bit 3 as the documentation claims.)

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1. The first line of Page 29 is wrong. The Output Control Signals at IV address 37 are IV Byte E (not IV Byte B).
2. The $\overline{\text{CLR}}$ bit in IV Byte E is Bit 4 (pin 4), not Bit 5 (pin 3). (See Figure 4-10, the Schematic for the 88-HDSK Data Card.)

IV Byte B (Address 37) - Output Mode (used for control signals)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	CRCAPE 1 = CRC append enable	
1	17	1	7	DISTRAN STRT 1 = Disk transfer start-starts read or write of data	
2	18	2	6	DISRMD,1 = Read mode, Ø = write mode	
3	19	3	5	X	
4	20	4	4	X	
5	21	5	3	$\overline{\text{CLR}}$ - Clears registers + latches at beginning of sector Read or Write	
6	22	6	2	TRAS - Transfer acknowledge strobe-strobed after data byte Xfer to/from FIFO	
7	23	7	1	$\overline{\text{SDSEL}}$ - Source data select - when=0, selects processor data (normal); when=1 selects cache memory data (optional, not available at this time)	

X = NOT USED

Disk Interface Card - Disk Function Control

IV Byte H (Address 17) - Output (to Disk Drives)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Start/Stop	Start/Stop all Drives
1	17	1	7	[1] Extension Select	Read/Write Head Selection
2	18	2	6	[2] Platter Select	
3	19	3	5	[3] Head Select	
4	20	4	4	Select 4	Physical Disk Drive (Unit) Selection
5	21	5	3	Select 3	
6	22	6	2	Select 2	
7	23	7	1	Select 1	

Notes: 1 - LOW = Bottom two (Extended) Platters; HIGH = Upper two Platters

2 - LOW = Top (Removable) Platter; HIGH = Bottom (Fixed) Platter

3 - LOW = Top surface of selected platter; HIGH = Bottom surface . . .

IV Byte I (Address 18) - Output (to Disk Drives)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Emergency Unload	Unload All
1	17	1	7	Offset plus	
2	18	2	6	Offset minus	
3	19	3	5	Enable Write	
4	20	4	4	Cylinder Restore	LOW(and Cyl. strobe)= Slow Seek to Ø
5	21	5	3	Cylinder Strobe	Goes LOW then HIGH; Active going HIGH
6	22	6	2		
7	23	7	1	Cylinder Address 8	

IV Byte J (Address 19) - Output (to Disk Drives)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Cylinder Address 7	8 of 9 Cylinder Address Lines
1	17	1	7	Cylinder Address 6	
2	18	2	6	Cylinder Address 5	
3	19	3	5	Cylinder Address 4	
4	20	4	4	Cylinder Address 3	
5	21	5	3	Cylinder Address 2	
6	22	6	2	Cylinder Address 1	
7	23	7	1	Cylinder Address Ø	

IV Byte K (Address 20) - Input (from Disk Drives)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Malfunction	
1	17	1	7	X	
2	18	2	6	X	
3	19	3	5	Extension Status	
4	20	4	4	X	
5	21	5	3	Dual Platter	
6	22	6	2	X	
7	23	7	1	Double Track	

IV Byte L (Address 21) - Input (from Disk Drives)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Ready	
1	17	1	7	Index Pulse	
2	18	2	6	File Protected	
3	19	3	5	Illegal Address	
4	20	4	4	Busy Seeking 4	Unit # busy seeking
5	21	5	3	Busy Seeking 3	
6	22	6	2	Busy Seeking 2	
7	23	7	1	Busy Seeking 1	

NOTE: X = NOT USED

IV Byte M (Address 22) - Input (from Disk Drives)

IV Bit-Pin		User Data Bit-Pin		Line Designation	General
0	16	0	8	Sector Pulse	
1	17	1	7	Sector Count 6	
2	18	2	6	Sector Count 5	
3	19	3	5	Sector Count 4	
4	20	4	4	Sector Count 3	
5	21	5	3	Sector Count 2	
6	22	6	2	Sector Count 1	
7	23	7	1	Sector Count Ø	

IV BYTE DESIGNATION

Controller - Altair Interface
Command & Data Communication

IV Byte		4PIO	Connection	Usage
A8	◄——►	Port 1	Section A	Command Response-IN 161-(Not Used)
A9	◄——	Port 1	Section B	Command Transfer - OUT 163
A12	◄——►	Port 2	Section A	Read Buffer Data, Status Data-IN 165
A12	◄——	Port 2	Section B	Command Parameters, Write Buffer Data, set byte data OUT 167

Controller - Altair Interface
Status Flags

IV Byte A10		4PIO	Connection	Usage
(Input lines to Altair)				
Bit 7	——►	Port 1	CA1	Controller Ready
6	——►	Port 1	CB1	Controller command acknowledge (command received)
1	——►	Port 2	CA1	Ready For Read Buffer (Read Data Byte Ready)
Ø	——►	Port 2	CB1	Ready for Write Buffer (OK to write Data Byte to Controller)

IV Byte A11		4PIO	Connection	Usage
(Output lines from Altair)				
Bit 7	◄——	Port 1	CA2	Not used
6	◄——	Port 1	CB2	Altair Command Ready (command sent)
1	◄——	Port 2	CA2	Read Buffer Strobe (Data Byte Read by computer)
Ø	◄——	Port 2	CB2	Write Buffer Strobe (Data Byte written by computer)

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Port 1, Section A, Command Response (IN 161) provides Error Flags, as described in the Addendum Page 7, and reproduced (with 1 erratum) here:

Bit	**1 Means:**[1]	**Error may occur in:**
0	Drive not ready	Any command except INITIALIZE and SET IV BYTE
1	Illegal sector	SEEK, READ SECTOR, WRITE SECTOR, FORMAT, & READ UNFORMATTED commands
2	CRC error in sector read	READ SECTOR, READ UNFORMATTED[2] commands
3	CRC error in header read	SEEK, READ SECTOR, WRITE SECTOR & FORMAT commands
4	Header has wrong sector	Same as in bit 3
5	Header has wrong cylinder	Same as in bit 3[3]
6	Header has wrong head	Same as in bit 3
7	Write protect	Same as in bit 1[4]

NOTES

1. All bits of port 161 are ones on the first read after the controller is turned on.

2. Always occurs on an unformatted read of a formatted sector.

3. Occurs spuriously when one of these commands is issued for a drive different from the one specified in the last seek. This spurious error is ignored by the write logic.

4. Only relevant during a Write Sector command. If a sector is write-protected, data may not be written to it. The Write Sector command is ignored and the error flag is set.

(**Erratum:** The Write Protect bit is also relevant during a FORMAT command. If the drive is write-protected, then the FORMAT command will fail.)

3-5. COMPUTER-CONTROLLER COMMUNICATIONS

A. 4PIO Status Signal Uses

Port 1A - CA1 Strobed by Controller when Ready - sets bit 7, Port 160 HIGH

```
L1   INP   160
     ANI   128     Wait for Command Ready
      JZ    L1
```

NOTE: Input on 161 to reset bit 7, Port 160 LOW

Port 1A - CA2 Strobed by Altair computer when Read 161

Port 1B - CB1 Strobed by Controller to acknowledge a command, sets bit 7, Port 162 HIGH

```
L2   INP   162
     ANI   128
      JZ    L2
```

NOTE: Input on 163 to reset bit 7, Port 162 LOW

Port 1B - CB2 Latched LOW by computer when Write to 163

NOTE: Reset HIGH when CB1 is strobed

Port 2A - CA1 Strobed by Controller when Ready for Read Data or Status transmission, sets bit 7, Port 164 HIGH

```
L3   INP   164
     ANI   128
      JZ    L3
```

NOTE: Input on 165 to Reset bit 7, Port 164 LOW

Port 2A - CA2 Strobed by Altair computer when Read 165

Port 2B - CB1 Strobed by Controller when Ready for Altair computer Write Data transmission, or Set byte data bit 7, Port 166 HIGH

```
L4   INP   166
     ANI   128
      JZ    L4
```

NOTE: Input on 167 to reset bit 7, Port 167 LOW

Port 2B - CB2 Strobed by computer when Write to 167

4PIO Channel Address	Function
161	Not Used
165	Primary Data In
	-Read Buffer Data
	-Read Status Data
163	Command Out
	-High order Byte of a Command
167	Data Out
	-LOW order Byte of a Command
	-Write Buffer Data
	-Set Byte Data

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Page 35-36

1. For all IV Bytes shown in Table 3-D (8T32 Byte Functions), the User Data Bits are reversed from the way they appear to the Altair via the Set Byte and Read Status commands, as follows:

User Data Bit	-Pin	Altair Bit
0	8	7
1	7	6
2	6	5
3	5	4
4	4	3
5	3	2
6	2	1
7	1	0

2. IV Bytes H, I, and J (addressed 17, 18, and 19) all invert the data. This means the data must be inverted when written to these IV Bytes. For example, to select Cylinder Address 0 in IV Byte J, you would write 255 (decimal) to IV byte J.

3. Note that the Read Status command rewrites 7 bits in IV Byte H (Address 17). User Bits 4-7 get set according to the Unit bits in the command byte (bits 3:2). User Bits 1:3 always get set to 011b (Extension Select low, Platter and Head select high). User Bit 0 (Start/Stop all drives) is unchanged by the Read Status command.

4. The Read Status command will not complete if the selected Unit is not Ready. This means that the Ready line on P2 of the 88-HDSK Interface Card must be pulled low for testing IV Bytes, when no disk drive is connected.

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Corrected sample routine for Set Byte command

The sample on page 35 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of some commands to be checked when that command completes. (See line 140.)

The controller sets the Altair Data Port Available bit 4.5 uSec after receiving this command. This is only 1 or 2 8080 instruction times, so there is no need to spin waiting for this bit at line 135. Similarly, the controller sets the Controller Ready bit 1 uS after receiving the data, so there is no need to spin waiting for this bit at line 140.

This program inverts the data written to IV Byte 17 because IV Byte 17 is inverting. (See lines 25 and 35.)

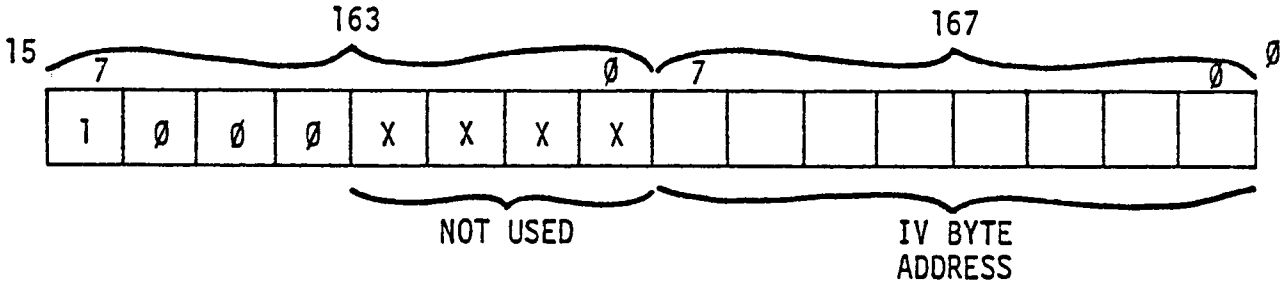
```
10 REM EXAMPLE- START/STOP DRIVE D (1<=D<=4)
15 E=(D-1)*4      :REM PUT UNIT BITS IN PLACE
20 I=17           :REM SELECT DISK FUNCTION CONTROL IV BYTE
25 J=NOT(E+128)   :REM SELECT DRIVE, SET START/STOP BIT
30 GOSUB 100
35 J=NOT E        :REM CLEAR START/STOP BIT
40 GOSUB 100
45 END

100 REM GENERAL SUBROUTINE TO WRITE J TO IV-PORT I
105 OUT167,I       :REM IV ADDRESS
110 A=INP(167)     :REM RESET ALTAIR DATA PORT HANDSHAKE
115 A=INP(161)     :REM RESET CONTROLLER READY
120 OUT163,128     :REM 'SET BYTE' INITIATES THE COMMAND
125 IF 128 AND INP(166)=0 THEN E$="PORT NOT READY":GOTO 200
135 OUT167,J       :REM WRITE J TO IV-PORT I
140 IF 128 AND INP(160)=0 THEN E$="CTLR NOT READY":GOTO 200
150 RETURN
200 PRINT "ERROR: ";E$:STOP
```

Assembly Language Example:

```
CREADY   equ   160
CSTAT    equ   161
ACMD     equ   163
ADSTA    equ   166
ADATA    equ   167

CSETIV   equ   80h

;===Subroutine========================================================
;Send IV byte
; On entry:
;   c = IV byte address
;   e = IV byte data
; On Exit:
; carry bit set for controller timeout
; a,d trashed, all other registers preserved
;=====================================================================
SENDIV:  in    ACMD          ;reset CMDACK in ACSTA

         mov   a,c           ;IV Byte address
         out   ADATA         ;low byte of command
         in    ADATA         ;clear ADPA bit in ADSTA

         mvi   a,CSETIV      ;Set IV Byte command
         out   ACMD          ;initiate command now

         mvi   d,0           ;256x37/2 uS=4.7 mS timeout

SIVLP1:  dcr   d             ;(4)timeout?
         stc                 ;(4) set carry for error return
         rz                  ;(5) error return with carry set
         in    ADSTA         ;(10)wait for ADPA
         rlc                 ;(4)test ADPA
         jnc   SIVLP1        ;(10)(37 cycles through loop)

         mov   a,e           ;send IV Byte data
         out   ADATA

         mvi   d,0           ;256x37/2 uS=4.7 mS timeout

SIVLP2:  dcr   d             ;(4)timeout?
         stc                 ;(4) set carry for error return
         rz                  ;(5) error return with carry set
         in    CREADY        ;(10)Is the controller done?
         rlc                 ;(4)look at msb=CRDY
         jnc   SIVLP2        ; (10)(37 cycles through loop)

         in    CSTAT         ;reset CRDY flag
         ora   a             ;and get A=error code
         jnz   UNXERR        ;Go deal with unexplained error
         ret
```

B. Command Format

1. Set byte



NOTE: Data to IV byte written to Channel 167 after command issued

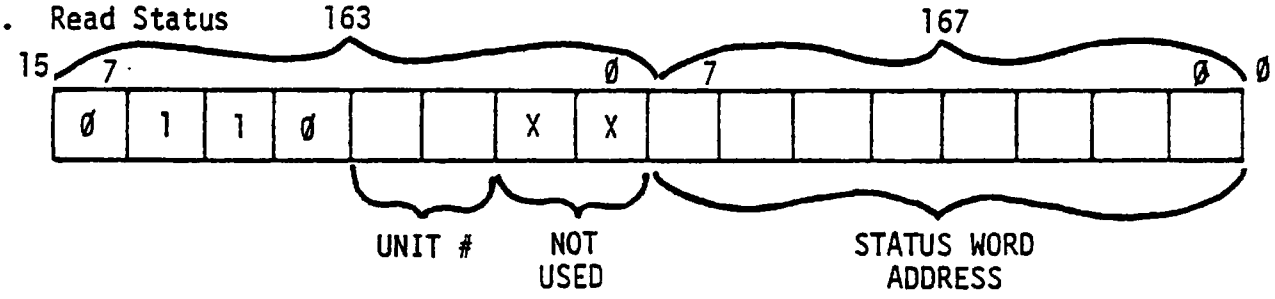
Sample BASIC Program:

-Use this program to control automatic start/stop of the D3000 Drive.

-IV byte address 17, bit 7 is strobed LOW, then HIGH (bit Ø-unit 1 select-is kept LOW)

```
1Ø WAIT16Ø, 128:  OUT167, 17
15 REM.....CHECK CONTROLLER RDY, OUTPUT IV BYTE ADDR
2Ø A=INP(161):    A=INP(163):  A=INP(167)
25 REM.....RESET ALL I/O HNDSHK LINES USED FOR SETBYTE COMMAND
3Ø OUT163, 128:   WAIT166, 128:  OUT167, 126
35 REM.....OUTPUT SETBYTE COMMAND, CHECK WRITE CHANNEL, OUTPUT BITS
                  Ø & 7 LOW
4Ø WAIT16Ø, 128:  OUT167, 17
45 REM.....CHECK CONTROLLER READY, OUTPUT IV BYTE ADDR
5Ø A=INP(161):    A=INP(163): A=INP(167)
55 REM.....RESET ALL I/O HNDSHK LINES USED FOR SETBYTE COMMAND
6Ø OUT163, 128:   WAIT166, 128: OUT167, 254
65 REM.....OUTPUT SETBYTE COMMAND, CHECK WRITE CHANNEL, OUTPUT BIT Ø
                  LOW, BIT 7 HIGH
```

2. Read Status



NOTE: IV byte status data is read from chan 165 after Status Command given

Sample BASIC Program:

-Use this program to check status bits on IV byte 36

```
1Ø WAIT16Ø, 128:  OUT167, 36
15 REM.....CHECK CONTROLLER RDY, OUTPUT IV BYTE ADDR
20 A=INP(161):    A=INP(163):  A=INP(165)
25 REM.....RESET ALL I/O HNDSHK LINES USED FOR STATUS COMMAND
30 OUT163, 96:    WAIT164, 128:  PRINT INP(165)
35 REM.....OUTPUT STATUS COMMAND, CHECK READ CHANNEL, INPUT READ
               CHANNEL AND PRINT DATA
```

-The status of both Input and Output IV bytes may be read.

-When reading status, the data in the IV byte is being read (Output data latched, Input data unlatched).

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Page 36

Corrected sample routine for Read Status command

The sample on page 36 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of some commands to be checked when that command completes. (See line 135.)

The controller will wait for the specified drive to be Ready before it reads any IV byte and send it to the computer. Therefore, the computer should wait for the controller to be Ready before reading the Status Byte data. (See line 125. Note that the WAIT command is an infinite loop. Better would be a loop with a timeout.)

The controller sets the Controller Ready bit 1 uS after writing the status the data to the Controller Data Port, so there is no need to spin waiting for this bit at line 130.

```
100 REM GENERAL SUBROUTINE TO READ A FROM IV-PORT I, UNIT D
105 OUT167,I            :REM IV ADDRESS
110 A=INP(165)          :REM RESET DATA PORT HANDSHAKE
115 A=INP(161)          :REM RESET CONTROLLER READY
120 OUT163, (D-1)*4+96:REM INITIATE THE COMMAND
125 WAIT164,128         :REM WAIT FOR CONTROLLER DATA
130 A=INP(165)          :REM A=IV-PORT I DATA
135 IF 128 AND INP(160)=128 THEN RETURN
140 PRINT "ERROR: COMMAND DID NOT COMPLETE":STOP
```

Assembly Language Example:

```
CREADY    equ    160
CSTAT     equ    161
ACMD      equ    163
CDSTA     equ    164
CDADA     equ    165
ADATA     equ    167

CRSTAT    equ    60h

;===Subroutine=========================================================
;Read IV byte
; On entry:
;   c = IV byte address
; On Exit:
;   carry set means no IV data because the drive was not ready
;   a = IV Byte Status
;   b trashed, all other registers preserved
;=======================================================================
READIV:  in      CDATA          ;clear CDA
         in      ACMD           ;reset CMDACK in ACSTA

         mov     a,c            ;low byte of command 1st
         out     ADATA
         mvi     a, CRSTAT      ;read status command
         out     ACMD           ;and issue command

         mvi     b,0            ;256x37/2 uS=4.7 mS timeout

RIVLP1:  dcr     b              ;(4) timeout?
         stc     c              ;(4)set carry for error return
         rz                     ;(5)timeout: carry set
         in      CREADY         ;(10)Is the controller done?
         rlc                    ;(4)look at msb=CRDY
         jnc     RIVLP1         ;(10)(37 cycles through loop)

         in      CSTAT          ;reset CRDY flag
         jnz     UNXERR         ;Go deal with unexplained error

         in      CDSTA          ;CDA should already be set
         rlc                    ;test CDA
         cmc                    ;so c means error
         rc                     ;not there? error return

         in      CDATA          ;Read & report IV Byte
         ret                    ;carry clear for normal return
```

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Page 37

Corrected sample routine for Write Buffer command

The sample on page 37 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of some commands to be checked when that command completes. (See line 165.)

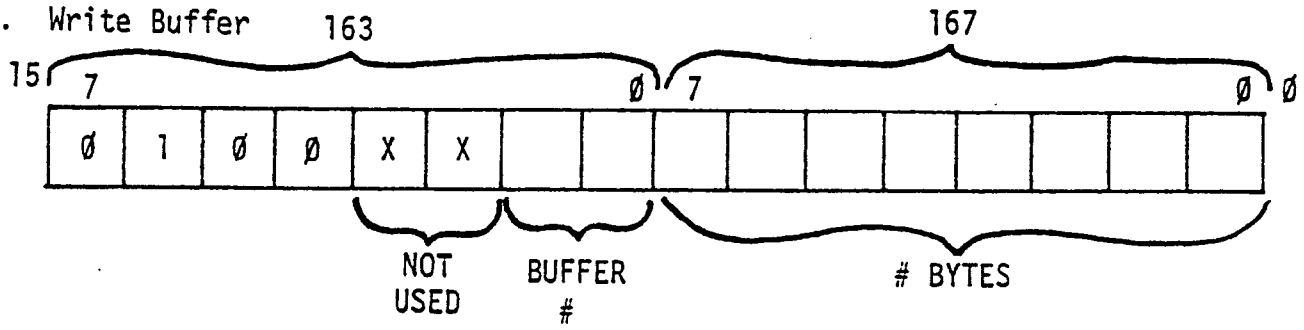
The controller sets the Altair Data Port Available bit 7 uSec after receiving this command. This is only 3 or 4 8080 instruction times, so there is no need to spin waiting for this bit at line 140. Similarly, the controller sets the Controller Ready bit 1 uS after receiving the last data byte, so there is no need to spin waiting for this bit at line 165.

```
100 REM GENERAL SUBROUTINE TO WRITE A$ TO BUFFER B
105 L=LEN(A$)
110 IF L>256 OR L=0 THEN E$="ILLEGAL STRING":GOTO 200
115 IF B>3 THEN E$="ILLEGAL BUFFER":GOTO 200
120 OUT167,L MOD 256     :REM COMMAND LOW BYTE IS BYTE COUNT
125 A=INP(167)           :REM RESET ALTAIR DATA PORT HANDSHAKE
130 A=INP(161)           :REM RESET CONTROLLER READY
135 OUT163,64+B          :REM 'WRITE BUFFER' INITIATES CMD
140 IF 128 AND INP(166)=0 THEN E$="PORT NOT READY":GOTO 200
150 FOR I=1 TO L         :REM WRITE L BYTES TO THE CONTROLLER
155 OUT 167,MID$(A$,1)
160 NEXT I
165 IF 128 AND INP(160)=0 THEN E$="CTLR TIMEOUT":GOTO 200
175 RETURN
200 PRINT "ERROR: ";E$:STOP
```

Assembly Language Example:

```
CREADY    equ    160
CSTAT     equ    161
ACMD      equ    163
ADSTA     equ    166
ADATA     equ    167

CWRBUF    equ    40h

;===Subroutine=======================================
; Write to controller buffer
; On Entry:
;   b = number of bytes to write (0 means 256)
;   c = controller buffer number
;  hl = address of write data
; On Exit:
;   carry set if timeout error on controller
;   a,bc,hl trashed, de preserved
;=====================================================
WRBUF:    in      ADATA        ;reset ADPA in ADSTA
          in      ACMD         ;reset CMDACK in ACSTA

          mov     a,b          ;transfer byte count
          out     ADATA        ;low byte of command 1st

          mov     a,c          ;Controller buffer number
          ori     CWRBUF       ;combine with write buffer command
          out     ACMD         ;and issue command

          mvi     c,0          ; 256x37/2 uS=4.7 mS timeout

WRBLP1:   dcr     c            ;(4)timeout?
          stc                  ;(4)carry set for error
          rz                   ;(5)exit with carry set for timeout

          in      ADSTA        ;(10)Wait for data port to be ready
          rlc                  ;(4)msb=ADPA
          jnc     WRBLP1       ;(10) (37 cycles through loop)

; loop to write b bytes from (hl) to controller

WRBLP2:   mov     a,m          ;get RAM buffer data
          out     ADATA        ;send to controller
          inx     h            ;next
          dcr     b
          jnz     WRBLP2

          in      CREADY       ;CRDY should already be set
          rlc                  ;test CRDY
          cmc                  ;so carry means error
          ret                  ;success/fail in carry
```

3. Write Buffer



NOTE: Write Data is sent to the Controller on channel 167 after the Write Buffer Command is given.

Sample BASIC Program:

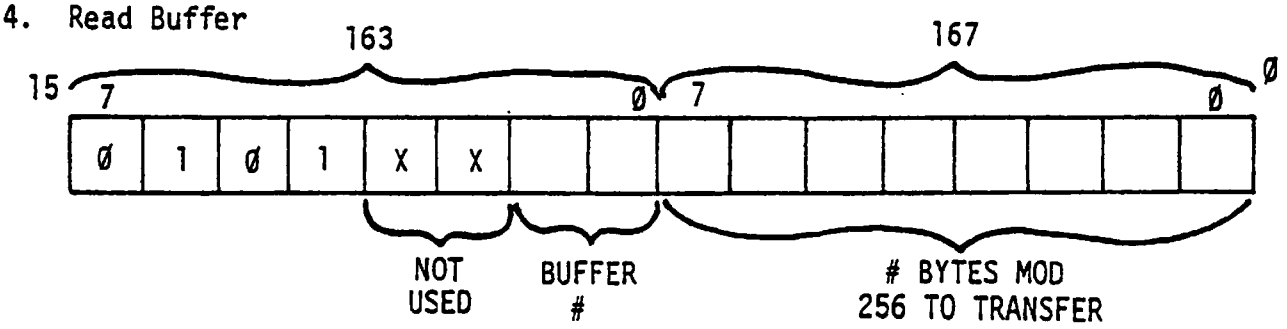
-Use this program to write data into a buffer in the Controller. The program asks for the buffer # and the ASCII message. It then transfers the proper command to the Controller, and outputs the ASCII message to be stored in one of the 4 buffers in the Controller.

```
16Ø INPUT "ENTER BUFFER NUMBER (Ø-3)";BF
17Ø INPUT "ENTER MESSAGE TO WRITE";S$
18Ø WAIT 16Ø, 128
19Ø OUT 167,(LEN(S$)+1) AND 255:A=INP(161): A=INP(163):A=INP(167)
2ØØ OUT 163,64+BF
21Ø WAIT 166,128:  OUT 167,LEN(S$)
22Ø FOR II=1TO LEN(S$): OUT 167, ASC(MID$(S$,II,1)):  NEXT
```

-Use this program with the "Read Buffer" program.

-The first byte placed in the buffer indicates the # of bytes in the string. Up to 255 bytes may be written.

4. Read Buffer



NOTE: Read Data is received from the Controller on channel 165 after the Read Buffer command is given.

Sample BASIC Program:

-This program inputs the buffer # to be read and issues a Read Buffer command to input the first byte in the buffer, indicating length of data.

-It then issues another Read Buffer command to read and print the data.

```
240 INPUT "ENTER BUFFER NUMBER (Ø-3)";BF
250 WAIT 160,128: OUT 167,1
260 A=INP(161): A=INP(163): A=INP(165)
270 OUT 163,64+16+BF: WAIT 164,128: L=INP(165)
280 PRINT "LENGTH OF STRING IS";L
290 WAIT160,128: OUT 167,(L+1)AND255
300 A=INP(161): A=INP(163): A=INP(165)
310 OUT 163,64+16+BF: WAIT 164,128: L=INP(165)
320 FOR II=1 TO L: PRINT CHR$(INP(165));: NEXT
```

-Use this program with the "Write Buffer" command.

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Page 38

Corrected sample routine for Read Buffer command

The sample on page 38 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of some commands to be checked when that command completes. (See line 165.)

The controller sets the Altair Data Port Available bit 7 uSec after receiving this command. This is only 3 or 4 8080 instruction times, so there is no need to spin waiting for this bit at line 135. Similarly, the controller sets the Controller Ready bit 1 uS after receiving the last data byte, so there is no need to spin waiting for this bit at line 165.

```
100 REM GENERAL SUBR TO READ L BYTES FROM BUFFER B INTO A$
105 IF L>256 OR L=0 THEN E$="ILLEGAL LENGTH":GOTO 200
110 IF B>3 THEN E$="ILLEGAL BUFFER":GOTO 200
115 OUT167,L MOD 256 :REM COMMAND LOW BYTE IS BYTE COUNT
120 A=INP(165)       :REM RESET CONTROLLER DATA PORT HANDSHAKE
125 A=INP(161)       :REM RESET CONTROLLER READY
130 OUT163,80+B      :REM 'READ BUFFER'INITIATES CMD
135 IF 128 AND INP(164)=0 THEN E$="PORT NOT READY":GOTO 200
145 A$=''
150 FOR I=1 TO L     :REM READ L BYTES FROM THE CONTROLLER
155 A$=''=A$+INP(165)
160 NEXT I
165 IF 128 AND INP(160)=0 THEN E$="CTLR TIMEOUT":GOTO 200
175 RETURN
200 PRINT "ERROR: ";E$:STOP
```

Assembly Language Example:

```
CREADY   equ   160
CSTAT    equ   161
ACMD     equ   163
CDSTA    equ   164
CDADA    equ   165
ADATA    equ   167

CRDBUF   equ   50h

;===Subroutine=====================================
; Read controller buffer
; On Entry:
;   b = number of bytes to write (0 means 256)
;   c = controller buffer number
;  hl = address for data
; On Exit:
;   a,bc,hl trashed, de preserved
;==================================================
RDBUF:  in      CDATA       ;reset CDA in CDSTA
        in      ACMD        ;reset CMDACK in ACSTA

        mov     a,b         ;transfer byte count
        out     ADATA       ;low byte of command 1st

        mov     a,c         ;buffer number
        ori     CRDBUF      ;combine with read buffer command
        out     ACMD        ;and issue command

        mvi     c,0         ; 256x37/2 uS=4.7 mS timeout

RDBLP1: dcr     c           ;(4)timeout?
        stc                 ;(4)carry set for error
        rz                  ;(5)exit with carry set for timeout

        in      CDSTA       ;(10)Wait for data port to be ready
        rlc                 ;(4)msb=CDA
        jnc     RDBLP1      ;(10) (37 cycles through loop)

; Loop to read b bytes from controller into memory at hl

RDBLP2: in      CDATA       ;get a data byte
        mov     m,a         ;stash in buffer
        inx     h           ;next
        dcr     b
        jnz     RDBLP2

        in      CREADY      ;CRDY should already be set
        rlc                 ;test CRDY
        cmc                 ;so carry means error
        ret                 ;success/fail in carry
```

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Preliminary Documentation, October 1977

Page 39

Corrected sample routine for Write Sector command

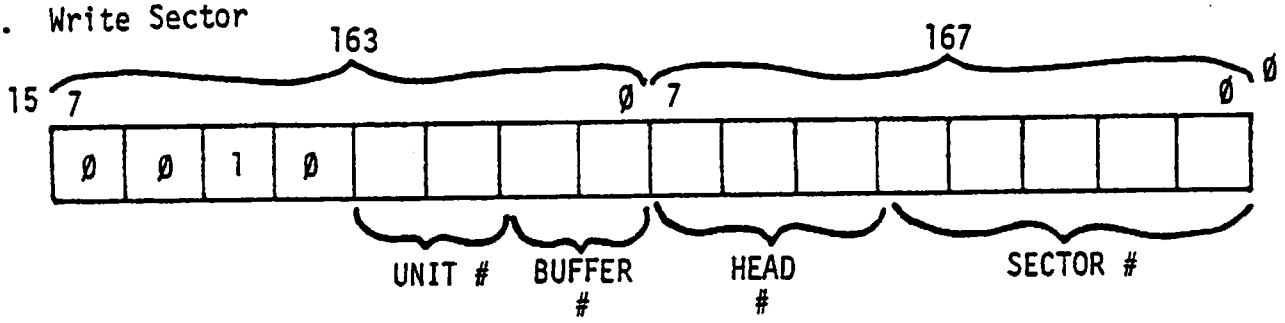
The sample on page 39 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of this command to be checked when the command completes. (See lines 125-135.)

```
100 REM SUBR TO WRITE BUFFER B TO HEAD H, SECTOR A ON UNIT D
105 IF B>3 THEN E$="ILLEGAL BUFFER":GOTO 200
110 IF S>23 THEN E$="ILLEGAL SECTOR":GOTO 200
115 OUT167,H*64+A        :REM HEAD AND SECTOR
120 OUT163,(D-1)*4+B+32 :REM UNIT, BUFF, WRITE SECTOR COMMAND
125 WAIT INP(160),128    :REM WAIT FOR SECTOR-WRITE TO COMPLETE
130 C=INP(161)           :REM RESET CTLR READY, READ STATUS
135 IF C=0 THEN RETURN
140 REM.....DECODE ERROR FLAGS
145 IF C AND 1=1 THEN PRINT "DRIVE NOT READY"
150 IF C AND 2=2 THEN PRINT "ILLEGAL SECTOR"
155 IF C AND 8=8 THEN PRINT "CRC ERROR IN SECTOR HEADER"
160 IF C AND 16=16 THEN PRINT "HEADER HAS WRONG SECTOR"
165 IF C AND 32=32 THEN PRINT "HEADER HAS WRONG CYLINDER"
170 IF C AND 64=64 THEN PRINT "HEADER HAS WRONG HEAD"
175 IF C AND 128=128 THE PRINT "WRITE PROTECTED"
200 PRINT "ERROR: ";E$:STOP
```

Assembly Language Example:

```
CREADY    equ   160
CSTAT     equ   161
ACMD      equ   163
ADATA     equ   167

CWRSEC    equ   20h

;===SUBROUTINE=======================================================
; write Sector
; (Note: This could easily be combined with Read Sector.)
; On Entry:
; b = sector number
; c = controller buffer number
; h = head number
; On Exit:
;  requested controller buffer has been written to disk sector
;  carry set if timeout for controller
;  Z set if no errors
;  a = error flags
;  bc trashed, others preserved
;=============================================================
WRSEC:    in    ACMD          ;(10)reset CMDACK in ACSTA

          mov   a,h           ;head number
          rrc
          rrc
          rrc                 ;...to bits 7:5
          ora   b             ;combine with sector
          out   ADATA

          mov   a,c           ;buffer number
          ora   CWRSEC        ;create write sector command
          out   ACMD          ;issue command

          lxi   b,5102        ;5102*49/2=125 mS (5 rotations)

WRSLP1:   dcx   b             ;(7)timeout?
          mov   a,b           ;(5)
          ora   c             ;(4)16-bit test
          stc                 ;(4)
          rz                  ;(5)carry set for error return
          in    CREADY        ;(10)Is the controller done?
          rlc                 ;(4)look at msb=CRDY
          jnc   WRSLP1        ;(10)(49 cycles through loop)

          in    CSTAT         ;reset CRDY flag, read error flags
          ora   a             ;test for errors
          ret                 ;Z set if okay
```

5. Write Sector



NOTE: See Table 3-E for head # selection

Sample BASIC Program:

-This program inputs the desired parameters and then issues a command to the Controller. The Controller will then write data from the selected buffer to the requested area.

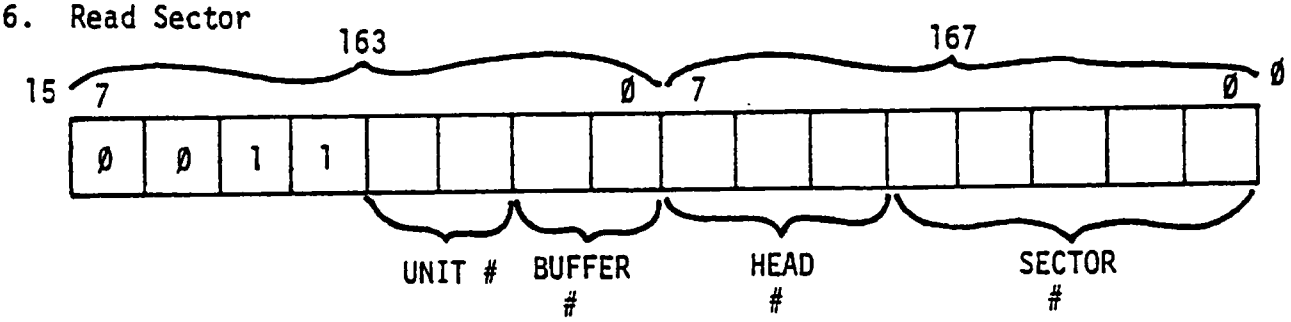
```
35Ø PRINT "WRITE SECTOR":INPUT "ENTER DRIVE (Ø-3), TRACK (Ø-7), SECTOR (Ø-23)";DR,TK,SC
36Ø INPUT "ENTER BUFFER NUMBER (Ø-3)";BF
37Ø WAIT 16Ø,128: OUT 167,SC+TK*32
38Ø A=INP(161): A=INP(163): OUT 163,32+DR*4+BF
```

-"Track" refers to HEAD #

-This program may be used after the "Write Buffer" command to write messages on the cartridge.

NOTE: Be sure good data is not overwritten when using this program. The program writes data to the cylinder that the head is currently positioned on.

6. Read Sector



NOTE: See Table 3-C for head # selection

Sample BASIC Program:

-This program will input the desired parameters and then issue a command to the Controller. Data will be read from the desired area and stored in the requested buffer.

```
4ØØ PRINT "READ SECTOR"
41Ø INPUT "ENTER DRIVE 0-3, TRACK 0-7, SECTOR 0-23":DR,TK,SC
42Ø INPUT "ENTER BUFFER NUMBER (Ø-3)";BF
43Ø WAIT 16Ø,128: OUT 167,SC+TK*32
44Ø A=INP(161): A=INP(163): OUT 163,32+16+DR*4+BF
```

-The program reads from the cylinder that the head is currently positioned on. "Track" refers to the HEAD #.

-This program may be used after the "Write Sector" program to read data back into a buffer. Use the read buffer program to print the data out.

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Altair Hard Disk (88-HDSK)
Preliminary Documentation, October 1977

Page 40

Corrected sample routine for Read Sector command

The sample on page 40 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of this command to be checked when the command completes. (See lines 130-140.)

```
100 REM SUBR TO READ HEAD H, SECTOR A ON UNIT D INTO BUFFER B
105 IF B>3 THEN E$="ILLEGAL BUFFER":GOTO 200
110 IF S>23 THEN E$="ILLEGAL SECTOR":GOTO 200
120 OUT167,H*64+A:REM.........HEAD AND SECTOR
125 OUT163,(D-1)*4+B+48 :REM UNIT, BUFF, WRITE SECTOR COMMAND
130 WAIT INP(160),128   :REM WAIT FOR SECTOR-WRITE TO COMPLETE
135 C=INP(161)          :REM RESET CTLR READY, READ STATUS
140 IF C=0 THEN RETURN
145 REM.....................DECODE ERROR FLAGS
150 IF C AND 1=1 THEN PRINT "DRIVE NOT READY"
155 IF C AND 2=2 THEN PRINT "ILLEGAL SECTOR"
160 IF C AND 4=4 THEN PRINT "CRC ERROR IN SECTOR DATA"
165 IF C AND 8=8 THEN PRINT "CRC ERROR IN SECTOR HEADER"
170 IF C AND 16=16 THEN PRINT "HEADER HAS WRONG SECTOR"
175 IF C AND 32=32 THEN PRINT "HEADER HAS WRONG CYLINDER"
180 IF C AND 64=64 THEN PRINT "HEADER HAS WRONG HEAD"
185 IF C AND 128=128 THE PRINT "WRITE PROTECTED"
190 STOP
200 PRINT "ERROR: ";E$:STOP
```

Assembly Language Example:

```
CREADY    equ    160
CSTAT     equ    161
ACMD      equ    163
ADATA     equ    167

CRDSEC    equ    30h

;===SUBROUTINE=======================================================
; Read Sector
; (Note: This could easily be combined with Write Sector.)
; On Entry:
; b = sector number
; c = controller buffer number
; h = head number
; On Exit:
;  disk sector data is in requested controller buffer
;  carry set if timeout for controller
;  Z set if no errors
;  a = error flags
;  bc trashed, others preserved
;=====================================================================
RDSEC:    in     ACMD          ;(10)reset CMDACK in ACSTA

          mov    a,h           ;head number
          rrc
          rrc
          rrc                  ;...to bits 7:5
          ora    b             ;combine with sector
          out    ADATA

          mov    a,c           ;buffer number
          ora    CRDSEC        ;create read sector command
          out    ACMD          ;issue command

          lxi    b,5102        ;5102*49/2=125 mS (5 rotation times)

RDSLP1:   dcx    b             ;(7)timeout?
          mov    a,b           ;(5)
          ora    c             ;(4)16-bit test
          stc                  ;(4)
          rz                   ;(5)carry set for error return
          in     CREADY        ;(10)Is the controller done?
          rlc                  ;(4)look at msb=CRDY
          jnc    RDSLP1        ;(10)(49 cycles through loop)

          in     CSTAT         ;reset CRDY flag, read error flags
          ori    7Fh           ;test for errors (Write protect is not an error)
          ret                  ;Z set if okay
```

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Altair Hard Disk (88-HDSK)
Preliminary Documentation, October 1977

Page 41

Corrected sample routine for Seek command

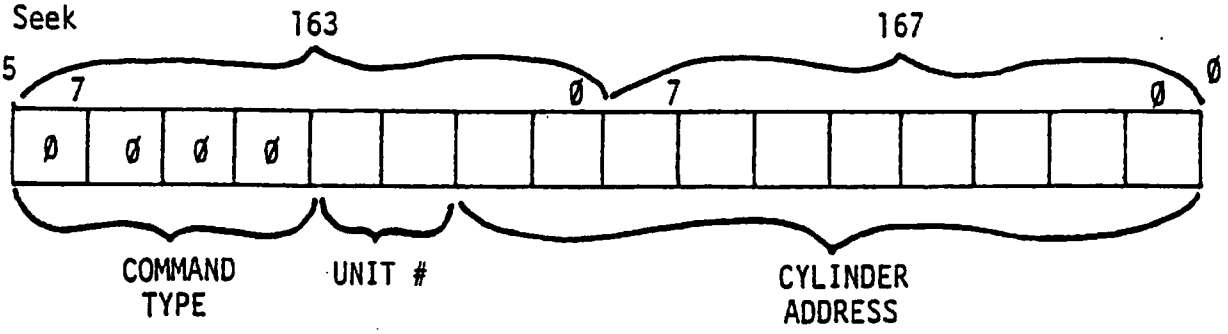
The sample on page 41 is nonfunctional because the Controller Ready signal is never cleared. Additionally, it is generally better to wait for commands to complete (by waiting for the controller to become Ready) at the end of each command, rather than to check to see of the controller is ready at the beginning of each command. This allows the error bits that are returned at the end of this command to be checked when the command completes. (See lines 135-145.)

```
100 REM SUBROUTINE TO SEEK CYLINDER C ON UNIT D
105 IF C>405 THEN E$="ILLEGAL CYLINDER":GOTO 200
115 A=0:IF C>255 THEN C=C-256:A=1
125 OUT167,C              :REM LOW 7 BITS OF CYLINDER
130 OUT 163,(D-1)*4+A+0 :REM UNIT, HIGH BIT OF CYL, SEEK CMD
135 WAIT INP(160),128    :REM WAIT FOR SECTOR-READ TO COMPLETE
140 C=INP(161)            :REM RESET CTLR READY, READ STATUS
145 IF C=0 THEN RETURN
150 REM.....DECODE ERROR FLAGS
155 IF C AND 1=1 THEN PRINT "DRIVE NOT READY"
160 IF C AND 4=4 THEN PRINT "CRC ERROR IN SECTOR DATA"
165 IF C AND 8=8 THEN PRINT "CRC ERROR IN SECTOR HEADER"
170 IF C AND 16=16 THEN PRINT "HEADER HAS WRONG SECTOR"
175 IF C AND 32=32 THEN PRINT "HEADER HAS WRONG CYLINDER"
180 IF C AND 64=64 THEN PRINT "HEADER HAS WRONG HEAD"
185 IF C AND 128=128 THE PRINT "WRITE PROTECTED"
190 STOP
200 PRINT "ERROR: ";E$:STOP
```

Assembly Language Example:

```
CREADY    equ   160
CSTAT     equ   161
ACMD      equ   163
ADATA     equ   167

CSEEK     equ   00h

;===SUBROUTINE=======================================================
; Seek
; (Note: This could easily be combined with Read & Write Sector.)
; On Entry:
; hl = cylinder number
; On Exit:
;  disk sector data is in requested controller buffer
;  carry set if timeout for controller
;  Z set if no errors
;  a = error flags
;  bc trashed, others preserved
;=====================================================================
RDSEC:    in    ACMD          ;(10)reset CMDACK in ACSTA

          mov   a,l           ;cylinder number bits 7:0
          out   ADATA

          mov   a,h           ;cylinder number bit 8
;         ora   CSEEK         ;create read sector command (CSEEK=0)
          out   ACMD          ;issue command

          lxi   b,5102        ;5106*49/2=130 mS (2* max seek time)

RDSLP1:   dcx   b             ;(7)timeout?
          mov   a,b           ;(5)
          ora   c             ;(4)16-bit test
          stc                 ;(4)
          rz                  ;(5)carry set for error return
          in    CREADY        ;(10)Is the controller done?
          rlc                 ;(4)look at msb=CRDY
          jnc   RDSLP1        ;(10)(49 cycles through loop)

          in    CSTAT         ;reset CRDY flag, read error flags
          ori   7Fh           ;test for errors (Write protect is not an error)
          ret                 ;Z set if okay
```

7. Seek



NOTE: Check for correct seek by checking status of port 21, bit 4 - Illegal Address status from Drive.

Sample BASIC Program:

-This program asks for track #, drive #, then transfers the command to the Controller. After the Controller executes the seek, the status of illegal address from the Drive is checked.

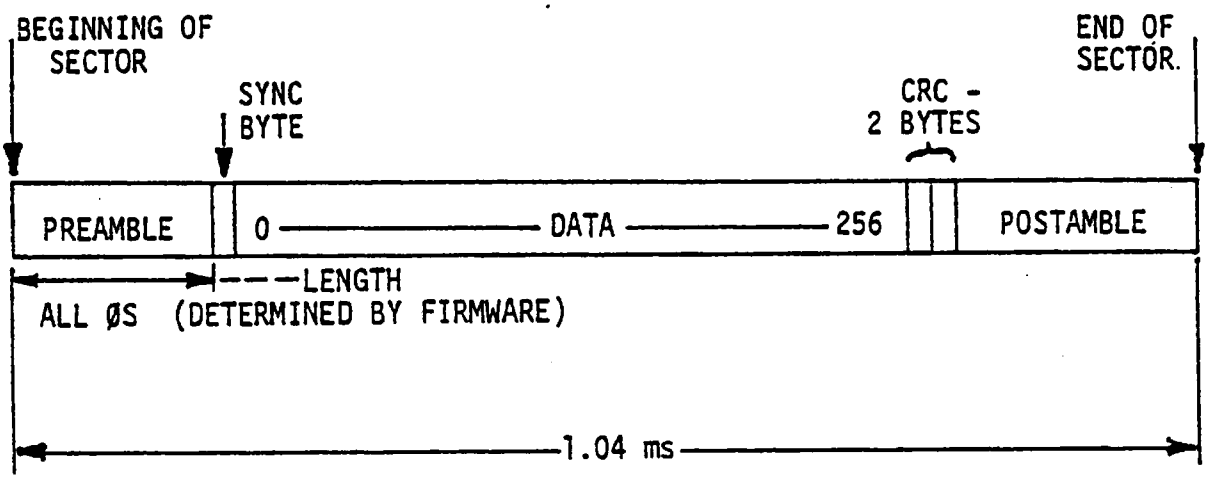
```
46Ø INPUT "ENTER TRACK NUMBER Ø-4Ø5";TK
47Ø INPUT "ENTER DRIVE NUMBER";DR
48Ø OUT 167,TK AND 255: WAIT 160,128
49Ø A=INP(161):A = INP(163): OUT 163, (TK-256)+DR*4
5ØØ WAIT 16Ø,128: A=INP(161): A=INP(163): A=INP(165)
51Ø OUT 167,21: OUT 163,96+DR*4  STATUS READ
52Ø WAIT 164,128: IF (INP(165)AND16)=Ø THEN PRINT "SEEK OK" ELSE PRINT "SEEK ERROR"
```

Table 3-E. Head # Selection Chart

Used on Write Sector and Read Sector Commands

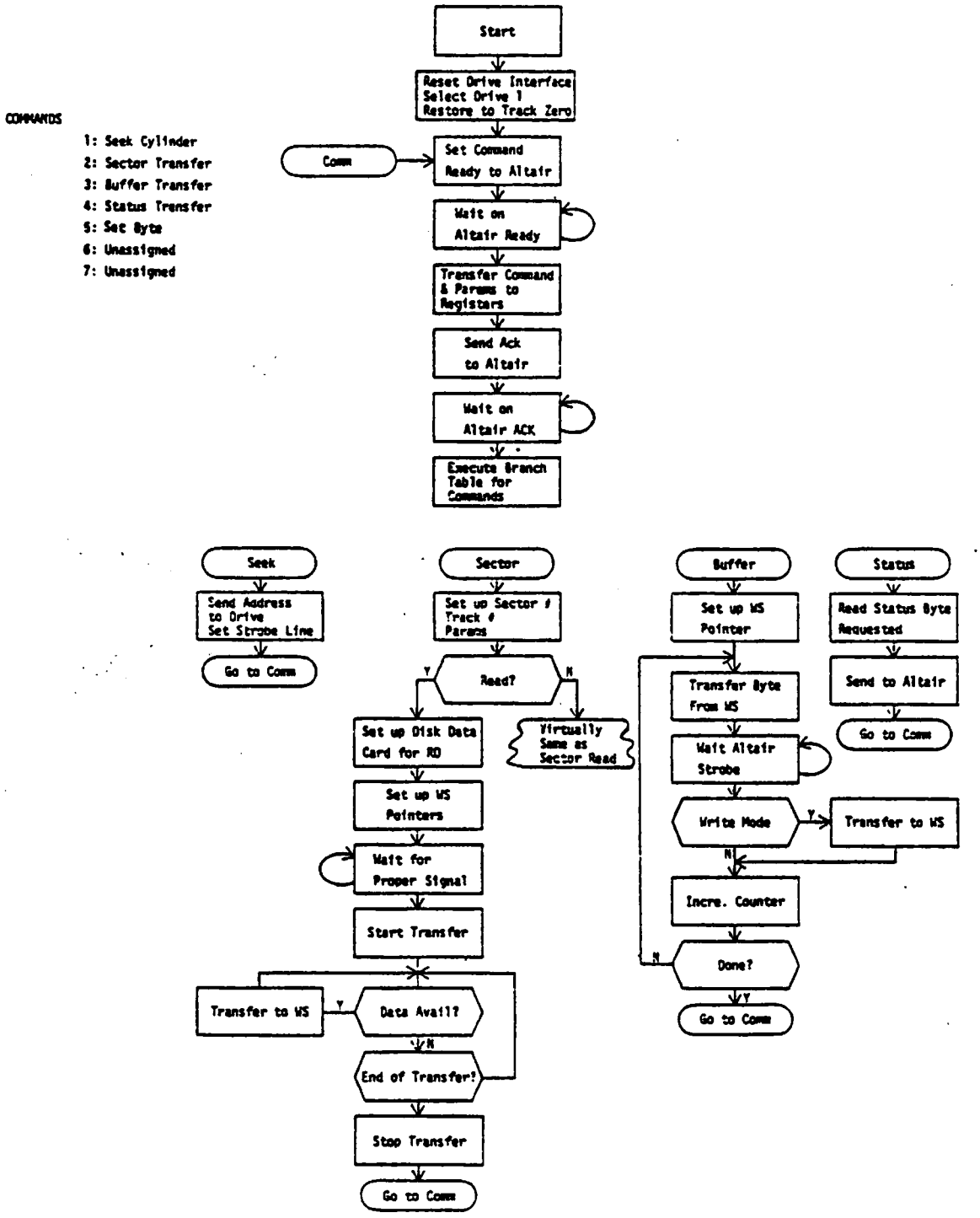
Address	Channel 167 Bit 7	6	5	Surface/Cartridge Selected	
0	0	0	0	Top	Removable
1	0	0	1	Bottom	Cartridge
2	0	1	0	Top	Fixed
3	0	1	1	Bottom	Platter
4	1	0	0	Top	Extended
5	1	0	1	Bottom	Fixed Platter 1
6	1	1	0	Top	Extended
7	1	1	1	Bottom	Fixed Platter 2

C. Data Format On Sector



D. Firmware Flowchart

The following flowchart is for the ROM program on the 88-HDSK Processor Card in the Datakeeper Controller.



3-6. Datakeeper Disk BASIC

MITS BASIC for the Datakeeper disk is virtually identical to that for floppy disks. The differences are as follows:

A. Loading. The HD-LDR PROM starts at address 176000 octal. To load BASIC from the Datakeeper disk, first make sure the disk drive is on-line and ready and that the controller is reset. (Do not reset controller if ready light is not on.)

For the 8800b Computer

1. Raise the STOP and RESET switches, in that order, and release them.
2. Set the address switches to 176000 octal (switches A10 - A15 up, the rest down). Raise and then release the EXAMINE switch.
3. Set the terminal sense switches according to the table on p. 101 of the BASIC Reference Manual, version 4.1.
4. Push the RUN switch.

For the 8800b Turnkey Computer

1. With the HD-LDR PROM at the AUTO-START address, simply set the RUN/STOP switch to RUN and actuate the START switch.
2. With the Turnkey Monitor PROM at the AUTO-START address, set RUN/STOP to RUN, actuate START and, when the Monitor's prompt period appears on the terminal, type J 176000.

B. Disk Organization. Each platter in the Datakeeper system is treated as one disk in the floppy disk system. For example, if unit 0 is a 10 Mbyte Datakeeper drive, the fixed platter is referred to as disk Ø and the removable platter as disk 1. These numbers are used in any BASIC instruction requiring disk numbers.

C. Maximum File Size. A file may not span more than one platter (or disk), so the maximum file size is approximately 5 Mbytes or 37,500 random file records (128 bytes per record).

D. Maximum Number of Files. The directory is a fixed size file, allowing approximately 500 separate files per platter, compared with 255 files per floppy diskette.

E. The DSKI$ and DSKO$ disk primitives are not included in Datakeeper BASIC.

F. Datakeeper BASIC allows the use of the Backspace function to delete characters on the terminal input line without echoing the backslash and the characters being deleted. It moves the cursor to the left one space on the CRT and in the input buffer. The Backspace is executed by typing Control/H (ASCII Code ØlØ octal), or by typing the backspace key on some terminals.

G. The PIP utility program is <u>not</u> provided with the Datakeeper BASIC. Instead, several individual utility programs are provided on the system platter. Use of these utilities is described in the HELP file which may be read by typing the following command: RUN "HELP". Before using any of these utilities, MEMORY SIZE must be limited to 44,000 during the BASIC initialization dialog.

The system utility programs include:

COPYFLOP - a system program to copy all named files on tracks 6 - 76 from floppy disk Ø and save them on Hard Disk Ø.

COPYHARD - a system program to copy one hard disk platter to another. It performs the necessary initialization of the cartridge for use by BASIC. If the program is to be used for initialization only, unnecessary files may be deleted from the newly copied platter by using the KILL command.

DIRLIST - provides an alphabetically sorted list of the Directory with optional hard copy output.

HELP - provides the specific details on how to use the utility programs. To read the HELP file, type

```
RUN "HELP", Ø
```

STARTREK - the game of STARTREK based upon the TV show of the same name.

The following programs appear in the disk directory when a FILES command is issued. They cannot, however, be LOADed or RUN because they are data files pertaining to these utility programs. For more information, RUN "HELP".

```
COPFTH
HDCPYBS
HELP.TXT
```

With these exceptions, Datakeeper BASIC is the same as that described in the <u>MITS BASIC Reference Manual, Version 4.1</u>.

3-7. File Manager Error Messages

When BASIC encounters difficulty with disk data or program files, the hard disk file manager prints one or more of the following error messages. BASIC prints the error code in hexadecimal. The codes and their meanings are as follows.

Hex	Decimal	Error Description
01	1	UNDEFINED SYSTEM ERROR
05	5	INVALID MODE PARAMETER
07	7	UNABLE TO FIND BUFFER TO ALLOCATE, SYSTEM ERROR
09	9	INVALID DRIVE NUMBER PARAMETER
0A	10	ATTEMPT TO WRITE TO VOLUME MOUNTED READ ONLY
13	19	VOLUME IS ALREADY MOUNTED
15	21	INVALID DRIVE NUMBER PARAMETER IN MOUNT
17	23	DRIVE IS NOT MOUNTED
1F	31	FILE NAME NOT FOUND
21	33	ATTEMPT TO OPEN TOO MANY FILES - OUT OF OPEN ENTRY BLOCKS
23	35	INTERNAL INCONSISTENCY, OUT OF INDEX ENTRY BLOCKS
27	39	INVALID FILE NUMBER PARAMETER
29	41	FILE NUMBER HAS NOT BEEN OPENED
2D	45	CRC ERROR ON READ OF SECTOR FROM DISC
2F	47	ATTEMPT TO OPEN READ ONLY FILE IN WRITE MODE
31	49	NOT ENOUGH SPACE ON VOLUME TO SATISFY REQUEST
33	51	FILE NAME ALREADY ON VOLUME
35	53	NOT ENOUGH SPACE IN DIRECTORY FOR NEW FILE
39	57	CONTROLLER DID NOT RESPOND TO SEEK COMMAND, RESET CONTROLLER
3B	59	CONTROLLER DID NOT RESPOND TO READ SECTOR COMMAND, RESET CONTROLLER
3D	61	CONTROLLER DID NOT RESPOND TO READ BUFFER COMMAND, RESET CONTROLLER NOTE - ABOVE COULD ALSO RETURN ERR=1
3F	63	CONTROLLER DID NOT RESPOND TO WRITE SECTOR COMMAND, RESET CONTROLLER
40	64	DRIVE IS NOT ON LINE

Hex	Decimal	Error Description
43	67	CONTROLLER DID NOT RESPOND TO STATUS COMMAND, RESET CONTROLLER
44	68	CONTROLLER DID NOT RESPOND TO WRITE BUFFER COMMAND, RESET CONTROLLER
47	71	NOT ENOUGH SPACE FOR INTERNAL TABLES IN SET-UP
49	73	INVALID NUMBER OF BUFFERS IN SET-UP
4B	75	INVALID NUMBER OF DRIVES OR FILES PARAMETERS IN SET-UP
4D	77	ATTEMPT TO WRITE TO DISC THAT HAS WRITE PROTECT SWITCH SET
4F	79	UNABLE TO UPDATE DIRECTORY, CHECK WRITE PROTECT OR DRIVE ON LINE
55	85	ATTEMPT TO READ PAST END OF FILE
57	87	INTERNAL INCONSISTENCY, ATTEMPT TO ALLOCATE TO ALLOCATED GROUP
59	89	ATTEMPT TO ACCESS INVALID LOGICAL PAGE
5B	91	INTERNAL INCONSISTENCY, NO FREE BIT FOUND DURING ALLOCATION
5D	93	ATTEMPT TO WRITE TO FILE OPENED READ ONLY OR TO KILL READ ONLY FILE
5F	95	UNABLE TO UPDATE DIRECTORY ENTRY, CHECK WRITE PROTECT
61	97	UNABLE TO UPDATE VOLUME DESCRIPTOR, CHECK WRITE PROTECT
63	99	INTERNAL INCONSISTENCY, DRIVE NUMBER FOR OPEN FILE IS INVALID
67	103	INTERNAL INCONSISTENCY, INDEX POINTER FOR OPEN FILE IS INVALID
69	105	INVALID SEEK MODE PARAMETER
6B	107	CONTROLLER DID NOT RESPOND TO READ BUFFER IN COMPARE
6D	109	DATA WRITTEN TO DISC DID NOT COMPARE PROPERLY ON READ BACK
6F	111	ERROR IN CLOSING FILE DURING DISMOUNT, VOLUME STILL MOUNTED

Hex	Decimal	Error Description
71	113	FILE IS OPEN, CANNOT KILL IT UNTIL CLOSED
73	115	ERROR IN WRITING PAGE TO DISC FROM BUFFER POOL, CHECK WRITE PROTECT
FF	255	INVALID FUNCTION PARAMETER TO DRIVER

88-HDSK
PRELIMINARY DOCUMENTATION
SECTION IV
THEORY OF OPERATION

4-1. GENERAL

This section contains information needed to understand the operation of the 88-HDSK (Hard Disk) System. Provided in this section is a fundamental description of the logic circuits used on the 88-HDSK Datakeeper Controller schematics, block diagrams of the various Datakeeper Controller Cards, and detailed theory of operation.

4-2. SCHEMATIC REFERENCING

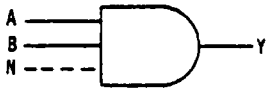
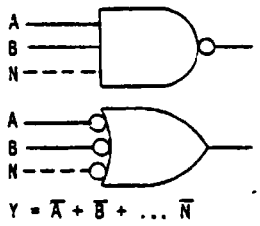
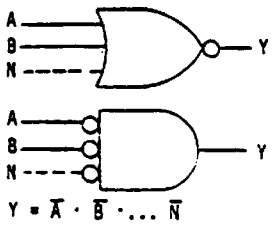
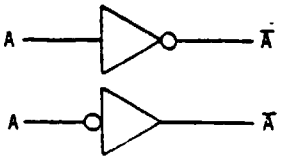
The detailed schematics are provided to aid in determining signal direction and tracing. A solid arrow (→) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as number-letter number (e.g. 2-A3), indicating sheet 2 and schematic zone A3.

A bar over the signal description on the schematic indicates an active LOW. The absence of a bar over the signal description indicates an active HIGH.

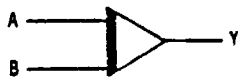
4-3. LOGIC CIRCUITS

The logic circuits used in the schematics are presented as a tabular listing in Table 3-A followed by a detailed explanation of the 8X300 Interpreter, the 8T32 Bidirectional I/O Ports, the 9401 CRC Generator and Checker, and the 9403 FIFO (first in-first out) Buffer Memory. The table is constructed to present the functional name, symbolic representation and a brief description of each logic circuit. Truth tables are provided to aid in understanding circuit operation where applicable. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle on the input or output indicates an active HIGH.

Table 4-A. Symbol Definitions

Name/Logic Symbol	Description
AND gate 	All the inputs have to be enabled HIGH to produce the desired HIGH output. The output is LOW of any of the inputs are LOW.
NAND gate 	All of the inputs have to be enabled HIGH to produce the desired LOW output. The output is HIGH if any of the inputs are LOW.
NOR gate 	Any of the inputs need to be enabled HIGH to produce the desired LOW output. The output is HIGH if all of the inputs are LOW.
Inverter 	The inverter is a device whose output is the opposite state of the input.

Dual Peripheral Positive-AND Driver (75451)



Any LOW on the input (A or B) enables the driver. A HIGH on both inputs, turns the driver off.

Truth Table

A	B	Y
L	H	L(on state)
L	H	L(on state)
H	L	L(on state)
H	H	L(off state)

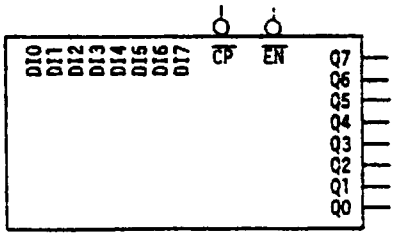
Dual Peripheral Positive-NAND Driver (75452)

Both inputs (A and B) must be HIGH to enable the driver.

Truth Table

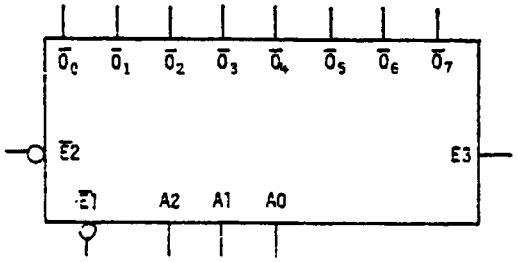
A	B	Y
L	L	H(off state)
L	H	H(off state)
H	L	H(off state)
H	H	L(on state)

Quad D-Type Flip-flop with Enable (74LS377)

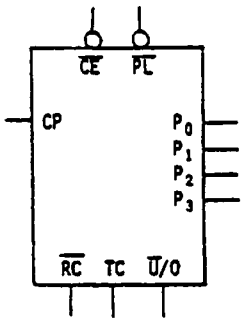
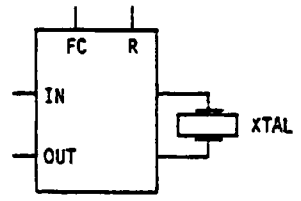
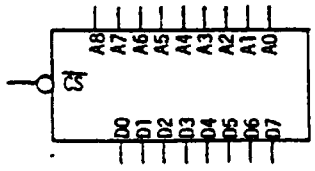


Information at the DI inputs is transferred to the outputs on the positive going edge of the clock pulse ($\overline{CP}$) if the enable input ($\overline{EN}$) is LOW.

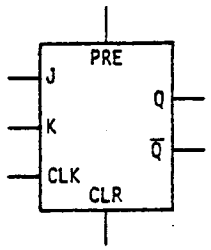
Three to Eight Line Decoder (74S138)



When $\overline{E1}$ and $\overline{E2}$ are LOW and E3 is HIGH, one of the eight output lines ($\overline{O}_0$ - $\overline{O}_7$) is enabled depending on the conditions at the three binary select inputs (A0-A2).

Synchronous Up/Down Counter (74LS191)  	The outputs of the four internal master-slave flip-flops are triggered on a LOW-to-HIGH transition of the clock (CP) if the enable input ($\overline{CE}$) is LOW. The counter is an Up Counter when the up/down ($\overline{U}$/D) input is LOW, and a Down Counter when $\overline{U}$/D is HIGH. The outputs may be preset to either level by placing a LOW on the load ($\overline{PL}$) input and entering the desired data at the data inputs (P0 - P3). Terminal Count (TC) produces a HIGH level output pulse with a duration approximately equal to one complete clock cycle when the counter over-flows or underflows. Ripple clock ($\overline{RC}$) produces a LOW-level output pulse to the LOW-level portion of the clock input when an overflow or underflow condition exists.
Dual Voltage-Controlled Oscillator (74S124)  	The enable input (IN) starts or stops the output pulses when it is LOW or HIGH, respectively. The internal oscillator is started and stopped by the enable input.
4096-Bit Programmable Read Only Memory (74S472)  	A LOW level at the Chip-Select ($\overline{CS}$) inputs enables all of the outputs (D). A HIGH level at $\overline{CS}$ inputs causes all the outputs to be off. Data is programmed at factory by burning fuse links.

J-K Master Slave Flip-flop
(74LS107)

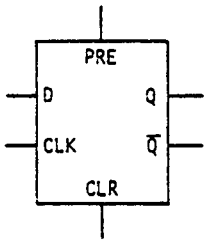


When the inputs are conditioned with J and K both HIGH, the Q output changes to the opposite state at each HIGH to LOW transition at the Clock (CLK) input. When J is HIGH and K is LOW, the Q output goes HIGH on the positive transition of the clock pulse.

Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	X	H
H	⎍	L	L	L	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

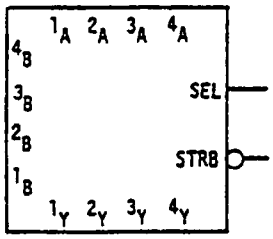
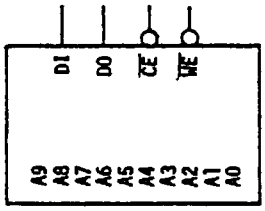
Edge Triggered Flip-flop
(74LS74)



Applying a LOW signal to the clear (CLR) input resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. When PRE (Preset) and CLR (Clear) are both HIGH, the Q output is directly affected on the positive transition of the clock pulse at CLK.

Truth Table

Inputs				Outputs	
PRE	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	H	Q_0	Q_0

Data Selector/Multiplexer (74LS157)  	When the strobe (STRB) input is LOW, a LOW level at the select (SEL) inputs enables the A inputs; a HIGH level at SEL selects the B inputs. If the selected A or B inputs are HIGH, the Y outputs are HIGH. When the selected A or B input is LOW, the output (Y) is LOW.
1024 X 1 Bit Fully Decoded Ramdom Access Memory (93425)  	When Write enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) are held LOW, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ is held LOW. Data in the specified location is presented to D_{out} and is non-inverted. D_{out} is held in a HIGH impedance state when writing.

8X300 INTERPRETER DATA SPECIFICATIONS

The 8X300 is a microcomputer designed for control. It features:

Execution Speed

- 250ns instruction execution time
- Direct address capability—up to 8192 16-bit words of program memory
- Eight 8-bit general purpose registers
- Simultaneous data transfer and data edit in a single instruction cycle time
- n-way branch or n-entry table lookup in 2 instruction cycle times
- 8X300 instructions operate with equal speed on 1-bit, 2-bit, 3-bit, 4-bit, 5-bit, 6-bit, 7-bit, or 8-bit data formats

The 8X300 instruction set features control-oriented instructions which directly access variable length input/output and internal data fields. These instructions provide very high performance for moving and interpreting data. This makes the 8X300 ideal in switching, controlling, and editing applications.

Direct Processing of External Data

The 8X300 I/O system is treated as a set of internal registers. Therefore data from external devices may be processed (tested, shifted, added to, etc.) without first moving them to internal storage. In fact, the entire concept is to treat data at the I/O interface no differently than internal data. This concept extends to the software which allows variables at the input/output system to be named and treated in the same way as data in storage.

Separate Program Storage and Data Storage

The storage concept of the 8X300 is to separate program storage from data storage. Program storage is implemented in read-only memory in recognition of the fact that programs for control applications are fixed and dedicated. The benefits of using read-only memory are that great speeds may be obtained at lower cost than if read/write memory were used, and that program instructions reside in a non-volatile medium and cannot be altered by system power failures.

8X300 Architecture

Figure 2 of the 8X300 data sheet illustrates the 8X300 architecture. The 8X300 contains an Arithmetic Logic Unit (ALU), Program Counter, and an Address Register. Eight 8-bit general purpose registers are also provided, including 7 working registers and an auxiliary register which performs as a working register and also provides an implied operand for many instructions. The 8X300 registers are shown in Figure 2 of the 8X300 data sheet and are summarized below:

Control Registers include:

- Instruction—A 16-bit register containing the current instruction
- Program Storage Address Register (AR)—A 13-bit register containing the address of the current instruction being accessed from Program Storage
- Program Counter (PC)—A 13-bit register containing the address of the next instruction to be read from Program Storage

Data Registers include:

- Working Registers (WR)—Seven 8-bit registers for data storage
- Overflow (OVF)—A 1-bit register that retains the most significant bit position carry from ALU addition operation. Arithmetically treated as 2^8
- Auxiliary (AUX)—An 8-bit register. Source of implied operand for arithmetic and logical instructions. May be used as a working register.

A crystal external to the CPU may be used to generate the CPU system clock. The CPU executes 8 instruction types.

DESCRIPTION

The Signetics 8X300 Interpreter is a monolithic, high-speed microprocessor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 250ns. A 250ns instruction cycle requires maximum memory access of 65ns, and maximum I/O device access of 35ns.

Interpreter instructions operate on 8-bit, parallel data. Logic is distributed along the data path within the Interpreter. Input data can be rotated and masked before being subject to an arithmetic or logical operation; and output data can be shifted and merged with the input data, before being output to external logic. This allows 1- to 8-bit I/O and data memory fields to be accessed and processed in a single instruction cycle.

PROGRAM STORAGE INTERFACE

Program Storage is typically connected to the A0-A12 (A12 is least significant bit) and I0-I15 signal lines. An address output on A0-A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0-I15 and defines the interpreter operations which are to follow.

The Signetics 82S115 PROM, or any TTL compatible memory, may be used for program storage.

I/O DEVICES INTERFACE

An 8-bit I/O bus, called the Interface Vector (IV) data bus, is used by the Interpreter to communicate with 2 fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is selected.

Both I/O data and I/O address information can be output on the IV bus. The SC and WC signals are typically used to distinguish between I/O data and I/O address information as follows:

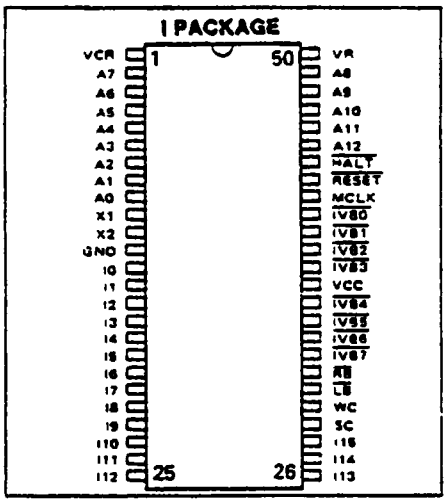
SC	WC	
1	0	I/O address is being output on IV bus
0	1	I/O data is being output on IV bus
0	0	I/O data is expected on the IV, bus, as input to the Interpreter
1	1	Not generated by the Interpreter

The Signetics 82SXXX series RAM, and the 8T32/33 may be attached to the IV bus.

FEATURES

- 185ns instruction decode and execute delay (with Signetics 8T32/33 I/O port)
- Eight 8-bit working registers
- Single instruction access to 1-bit, 2-bit, 3-bit . . . or 8-bit field on I/O bus
- Separate instruction address, instruction, and I/O data busses
- On-chip oscillator
- Bipolar Schottky technology
- TTL inputs and outputs
- Tri-state output on I/O data bus
- +5 volt operation from 0° to 70° C

PIN CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
2-9, 45-49	A0-A12:	Instruction address lines. A high level equals "1." These outputs directly address up to 8192 words of program storage. A12 is least significant bit.	Active high
13-28	I0-I15:	Instruction lines. A high level equals "1." Receives instructions from Program Storage. I_{15} is least significant bit.	Active high
33-36, 38-41	$\overline{IV80}$-$\overline{IV87}$	Interface Vector (IV) Bus. A low level equals "1." Bidirectional tri-state lines to communicate with I/O devices. $\overline{IV87}$ is least significant bit.	Three-state Active low
42	$\overline{MCLK}$:	Master Clock. Output to clock I/O devices, and/or provide synchronization for external logic	
30	WC:	Write Command. High level output indicates data is being output on the IV Bus.	Active high
29	SC:	Select Command. High level output indicates that an address is being output on the IV Bus.	Active high
31	$\overline{LB}$:	Left Bank. Low level output to enable one of two sets of I/O devices ($\overline{LB}$ is the complement of RB).	Active low
32	$\overline{RB}$:	Right Bank. Low level output to enable one of two sets of I/O devices ($\overline{RB}$ is the complement of $\overline{LB}$).	Active low
44	$\overline{HALT}$:	Low level is input to stop the Interpreter.	Active low
43	$\overline{RESET}$:	Low level is input to initialize the Interpreter.	Active low
10-11	X1, X2:	Inputs for an external frequency determining crystal. May also be interfaced to logic or test equipment.	
50	VR	Reference voltage to Pass Transistor.	
1	VCR	Regulated output voltage from Pass Transistor.	
37	VCC:	5V power connection.	
12	GND:	Ground.	

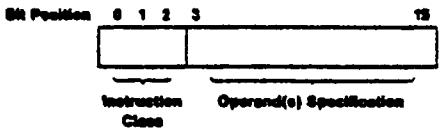
INSTRUCTION CYCLE

Each interpreter operation is executed in 1 instruction cycle, which may be as short as 250ns. The Interpreter generates MCLK to synchronize external logic to the instruction cycle. Instruction cycles are subdivided into quarter cycles. MCLK is an output during the last quarter cycle.

During the third quarter cycle of an instruction, an address is output on A0-A12, identifying the location in program storage of the next instruction word. This instruction word defines the next instruction, which must be input on I0-I15 during the first quarter cycle of the next instruction cycle (see Table 1).

Instruction Set Summary

The 16-bit instruction word input on I0-I15 is decoded by the instruction decode logic to implement events that are to occur during the remainder of the instruction cycle. Generally the 16-bit instruction word is decoded as follows:



A detailed usage of the 13 "operand(s) specification" bits is given in following sections.

Three operation code bits allow for 8 instruction classes. The 8 instruction classes are summarized in Table 2. Each entry is referred to as an "Instruction class" because the unique architecture of the Interpreter allows a number of powerful variations to be specified by the 13 operand(s) specification bits. A complete description of instruction formats and some instruction examples are provided in the Application Notes.

Data Processing

The Interpreter architecture includes eight 8-bit working registers, an arithmetic logic unit (ALU), an overflow register, and the 8-bit IV Bus. Internal 8-bit data paths connect the registers and IV Bus to the ALU inputs, and the ALU output to the registers and IV Bus. Data processing logic is distributed along these internal 8-bit data paths. Rotate and mask logic precedes the ALU on the data entry path. Shift and merge logic precedes the ALU on the data entry path. Shift and merge logic follows the ALU on the data output path. All 4 sets of logic can operate on 8 data bits in a single instruction cycle. (See Figure 2)

When less than 8 bits of data are specified for output to the IV bus by the ALU, the data field (shifted if necessary) is inserted into the prior contents of the IV bus latches. The

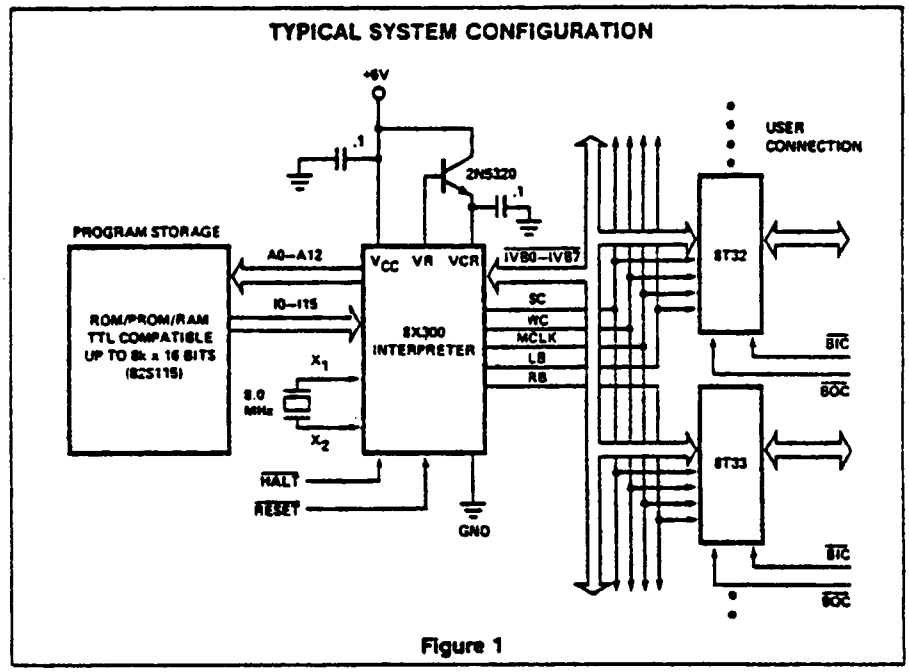


Figure 1

INST. AND IV BUS DATA INPUT	DATA PROCESSING	ADDR. AND IV BUS CHANGING	ADDR. AND IV BUS DATA VALID MCLK-HIGH
← ¼ cycle →	← ¼ cycle →	← ¼ cycle →	← ¼ cycle →

Table 1 INSTRUCTION CYCLE

IV bus latches contain data input at the start of an instruction. This data in the IV bus latches will be specified in the instruction as a) IV bus source data or b) data from an automatic read when the IV bus is specified as a destination. Therefore, IV bus bit positions outside an inserted bit field are unmodified.

Data Addressing

Sources and destinations of data are specified using a 5-bit octal number, as shown in Table 2. The source and/or destination of data to be operated upon is specified in a single instruction word.

Referring to Table 3, the Auxiliary register (address 00) is the implied source of the second argument for ADD, AND or XOR operations.

IVL and IVR are write-only registers used only as a destination. They have addresses and are treated as registers, but in reality they do not exist. When IVL is specified as a destination or the D field = $20\text{-}27_8$, then LB = 'low', RB = 'high' are generated; when IVR is specified as a destination or the D field = $30\text{-}37_8$, then RB = low, LB = 'high' are generated.

When IVL or IVR is specified as the destination in an instruction, SC is also activated and data is placed on the IV bus. If IVL or IVR is specified as a source of data, the source data is all zeroes.

INSTRUCTION SEQUENCE CONTROL

The Address Register and Program Counter are used to generate addresses for accessing an instruction. The Address Register is used to form the instruction address, and in all but 3 instructions (XEC, NZT, and JMP) the address is copied into the Program Counter. The instruction address is formed in 1 of 3 ways:

1. For all instructions but the JMP, XEC, and a satisfied NZT, the Program Counter is incremented by 1 and placed in the Address Register.
2. For the JMP instruction, the full 13-bit address field from the JMP instruction is placed into the Address Register and copied into the Program Counter.
3. For the XEC and NZT instructions, the high order 5- or 8-bits of the Program Counter are combined with 8- or 5-lower-order bits of ALU output (XEC or NZT) and placed in the Address Register. For the NZT instruction, it is also copied into the Program Counter.

INTERPRETER ARCHITECTURE

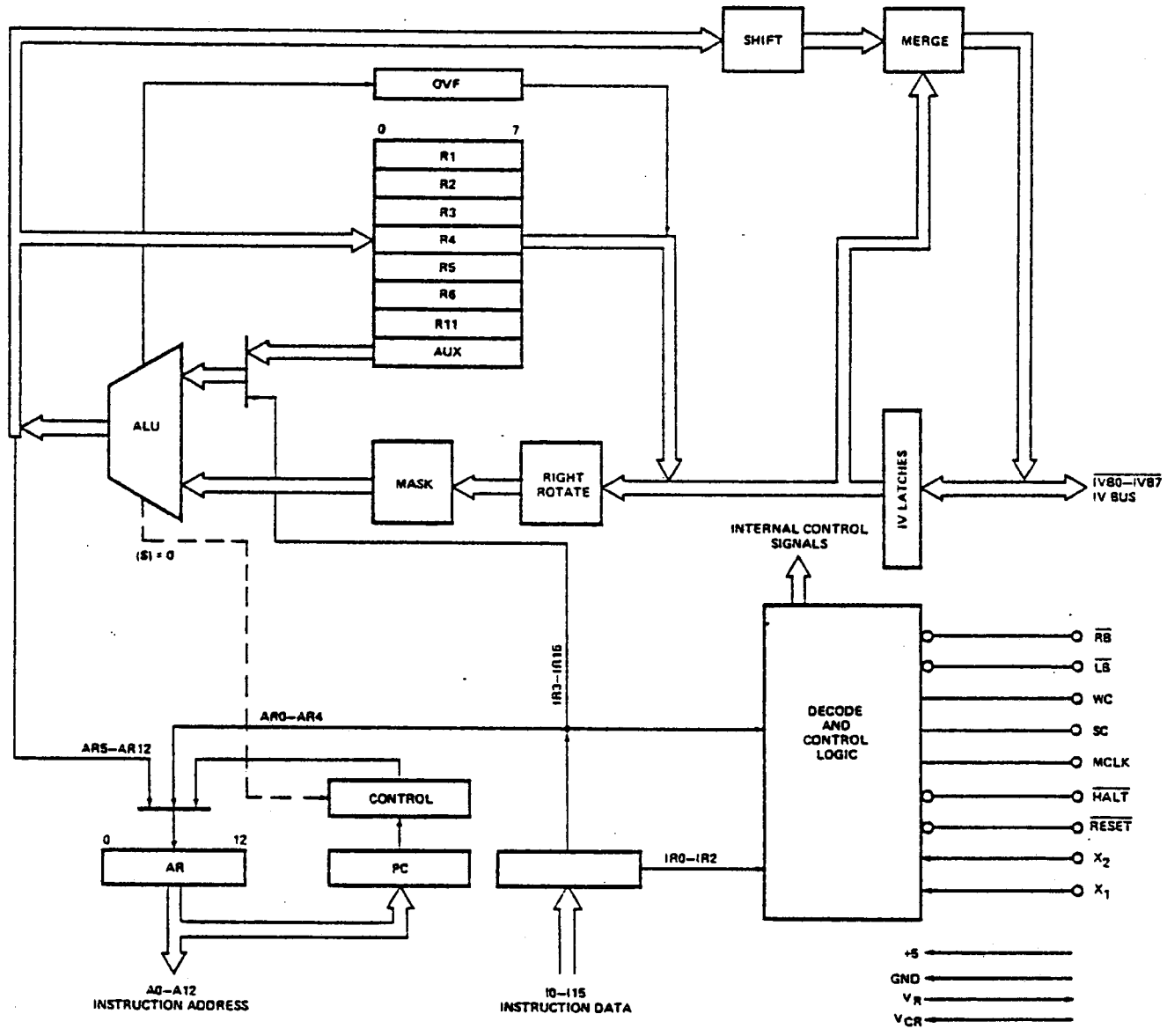


Figure 2

INSTRUCTION MNEMONIC	OP CODE	FORMATS	DESCRIPTION	I/O CONTROL SIGNALS	– INSTRUCTION CYCLE – Instruction Input and Data Processing	– INSTRUCTION CYCLE – Address/IV Bus Output
MOVE	0	Register to Register 0 2 3 7 8 10 11 15 0 | S | R | D S≠07,17,20-37$_8$ D≠10,20-37$_8$	(S) – D Move contents of register specified by S to register specified by D. Right rotate contents of register S by R places before operation.	SC = WC = $\overline{CB}$/RB = $\overline{CB}$/RB =	0 0 X X	1 if D = 07,17 0 1 if D = 17 0 if D = 07
		IV Bus to Register: 0 2 3 7 8 10 11 15 0 | S | L | D S=20-37$_8$ D≠10,20-37$_8$	Move right rotated IV bus (source) data specified by S to register specified by D. L specifies the length of source data with most significant bits set to zero.	SC = WC = $\overline{CB}$/RB = $\overline{CB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	1 if D = 07,17 0 1 if D = 17 0 if D = 07
		Register to IV Bus: 0 2 3 7 8 10 11 15 0 | S | L | D S≠07,17,20-37$_8$ D=20-37$_8$	Move contents of register specified by S to the IV bus. Before placement on IV bus, data is shifted as specified by D, and L bits merged with destination IV bus data.	SC = WC = $\overline{CB}$/RB = $\overline{CB}$/RB =	0 0 0 if D = 20-27 1 if D = 30-37	0 1 0 if D = 20-27 1 if D = 30-37
		IV Bus to IV Bus: 0 2 3 7 8 10 11 15 0 | S | L | D S=20-37$_8$ D=20-37$_8$	Move right rotated IV bus data (sources) specified by S to the IV bus. Before placement on IV bus, data is shifted or specified by D and merged with original source data. L specifies the length of source data to be operated on.	SC = WC = $\overline{CB}$/RB = $\overline{CB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	0 1 0 if D = 20-27 1 if D = 30-37
ADD	1	SAME AS MOVE	(S) plus (AUX) – D Same as MOVE but contents of AUX added to the source data. If carry from most significant bit then OVF = 1, otherwise OVF = 0		SAME AS MOVE	
AND	2	SAME AS MOVE	(S)∧(AUX) – D Same as MOVE but contents of AUX ANDed with source data.		SAME AS MOVE	
XOR	3	SAME AS MOVE	(S) ⊕ (AUX) – D Same as MOVE but contents of AUX exclusive ORed with source data.		SAME AS MOVE	
XEC	4	Register Immediate: 0 2 3 7 8 15 4 | S | I S≠07,17,20-37$_8$ I=000-377$_8$	Execute instruction at current page address offset by I + (S).	SC = WC = $\overline{CB}$/RB	0 0 x	0 0 x
		IV Bus Immediate: 0 2 3 7 8 10 11 15 4 | S | L | I S=20-37$_8$ I=00-37$_8$	Execute the instruction at the address determined by concatenating 5 high order bits of PC with the 8 bit sum of I and register specified by S. PC is not incremented. Execute the instruction at the address determined by concatenating 8 high order bits of PC with the 5 bit sum of I and rotated IV bus data (source) specified by S. R/L specifies length of source data with most significant bits set to zero. PC is not incremented.	SC = WC = $\overline{CB}$/RB = $\overline{CB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	0 0 x x

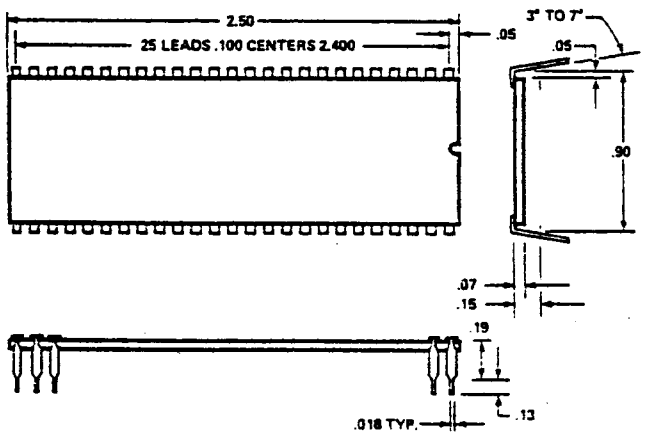
Table 2 INSTRUCTION SET SUMMARY

INSTRUCTION MNEMONIC	OP CODE	FORMATS	DESCRIPTION	I/O CONTROL SIGNALS	– INSTRUCTION CYCLE – Instruction Input and Data Processing	– INSTRUCTION CYCLE – Address/IV Bus Output
NZT	5	Register Immediate: 0 2 3 7 8 15 5 | S | I S≠07,17,20-37$_8$ I=000-377$_8$	If (S) = 0, jump to current page address offset by I; if S = 0, PC + 1 → PC If contents of register specified by S is non zero then transfer to address determined by concatenating 5 high order bits of PC with I; if contents of register specified by S is zero, increment PC.	SC = WC = $\overline{LB}$/RB	0 0 x	0 0 x
		IV Bus Immediate: 0 2 3 7 8 10 11 15 5 | S | L | I S=20-37$_8$ I=00-37$_8$	If right rotated IV bus data (source) is Non Zero then Transfer to address determined by concatenating 8 high order bits of PC with I; if contents of register specified by S is zero, increment PC.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if S = 20-27 1 if S = 30-37	0 0 x x
XMIT	6	Register Immediate: 0 2 3 7 8 15 6 | D | I D≠10, 20-37$_8$ I=000-377$_8$	Transmit I → D Transmit and store 8 bit binary pattern I to register specified by D.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RD =	0 0 x x	1 if D = 07,17 0 1 if D = 17 0 if D = 07
		IV BUS IMMEDIATE 0 2 3 7 8 10 11 15 6 | D | L | I D=20-37$_8$ I=00-37$_8$	Transmit binary pattern I to IV bus. Before placement on IV bus, literal I is shifted as specified by D and L bits merged with existing IV bus data.	SC = WC = $\overline{LB}$/RB = $\overline{LB}$/RB =	0 0 0 if D = 20-27 1 if D = 30-37	0 1 0 if D = 20-27 1 if D = 30-37
JMP	7	Address Immediate: 0 2 3 15 7 | A A=00000-17777$_8$	Jump to Program Address A Jump to program storage address A. A is stored in the address register (AR).	SC = WC = $\overline{LB}$/RB =	0 0 x	0 0 x

NOTE
1. RB is complement of LB.
2. "0" = Low voltage
   "1" = High voltage
   x = Don't care

Table 2 INSTRUCTION SET SUMMARY (Cont'd)

INTERPRETER PACKAGE DIMENSIONS



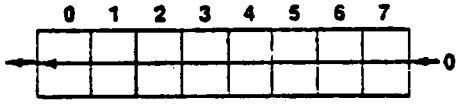
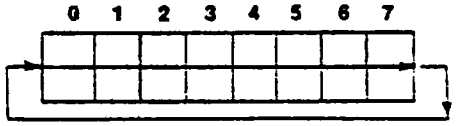
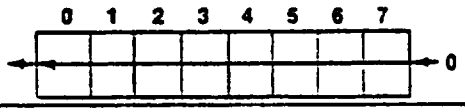
S AND/OR D FIELD SPECIFICATION (OCTAL)	SOURCE/DESTINATION
00 01 to 06 07 10 11 17	Auxiliary Register (AUX) Work registers (R1 to R6) respectively IVL write-only "register" (destination only) Overflow status (OVF)—source only Working register (R11) IVR write-only "register" (destination only)
2N (N = 0,1,2, 3,4,5,6,7)	a. If a source, IV bus data right rotated (7—N) bits and masked (specified by R/L). $\overline{LB}$ = 'low' and $\overline{RB}$ = 'high' generated. **IV Bus Source Data** 0 1 2 3 4 5 6 7  b. If a destination, IV bus data left shifted (7—N) bits and merged (specified by $\overline{R/L}$). LB = 'low' and $\overline{RB}$ = 'high' generated. **IV Bus Destination Data** 0 1 2 3 4 5 6 7  0
3N (N = 0,1,2, 3,4,5,6,7)	a. If a source, IV bus data right rotated (7—N) bits and masked (specified by R/L). $\overline{LB}$ = 'high' and $\overline{RB}$ = 'low' generated. **IV Bus Source Data** 0 1 2 3 4 5 6 7  b. If a destination, IV bus data left shifted (7—N) bits and merged (specified by R/L). $\overline{LB}$ = 'high' and $\overline{RB}$ = 'low' generated. **IV Bus Destination Data** 0 1 2 3 4 5 6 7  0

Table 3 DATA SOURCE DESTINATION ADDRESS

INTERPRETER INTERNAL REGISTERS

Programmable Registers (all 8 bits):

AUX — General working register. Contains second term for arithmetic or logical operations.

R1 — General working register

R2 — General working register

R3 — General working register

R4 — General working register

R5 — General working register

R6 — General working register

R11 — General working register

Other Registers:

Address Register (AR)
— A 13-bit register containing the address of the current instruction.

OVF — The least-significant bit of this register is used to reflect overflow status resulting from the most recent ADD operation (see Instruction Set Summary).

Program Counter (PC)
— Normally contains the address of the current instruction and is incremented to obtain the next instruction address.

Instruction Register (IR)
— Holds the 16-bit instruction word currently being executed.

Table 4

SYSTEM DESIGN USING THE INTERPRETER

Designing hardware around the 8X300 Interpreter reduces to selecting a program storage devicer (ROM, PROM, etc.), selecting I/O devices (IV byte, multiplexers, RAM, etc.), selecting clock mode (system driven or crystal controlled) and interfacing the Interpreter to these components, as shown in Figure 3.

System Clock

The Interpreter has an integrated oscillator which generates all necessary clock signals. The oscillator is designed to connect directly to a series resonant quartz crystal via pins X1 and X2. The crystal resonant frequency, f, is related to the desired cycle time, T, by the relationship f = 2/T. For a 250ns system, f = 8.00MHz.

In lower speed applications where the cycle time need not be precisely controlled, a capacitor may be connected between X1 and X2 to drive the oscillator. Approximate capacitor values are given in Table 6. If cycle time is to be varied, X1 and X2 should be driven from complementary outputs of a pulse generator. Figure 4 shows a typical configuration. For systems where the Interpreter is to be driven from a master clock, the X1 and X2 lines may be interfaced to TTL logic as shown in Figure 5.

Type:	Fundamental mode, series resonant
Impedance at Fundamental:	35 ohms maximum
Impedance at harmonics and spurs:	50 ohms minimum

Table 5 CRYSTAL CHARACTERISTICS

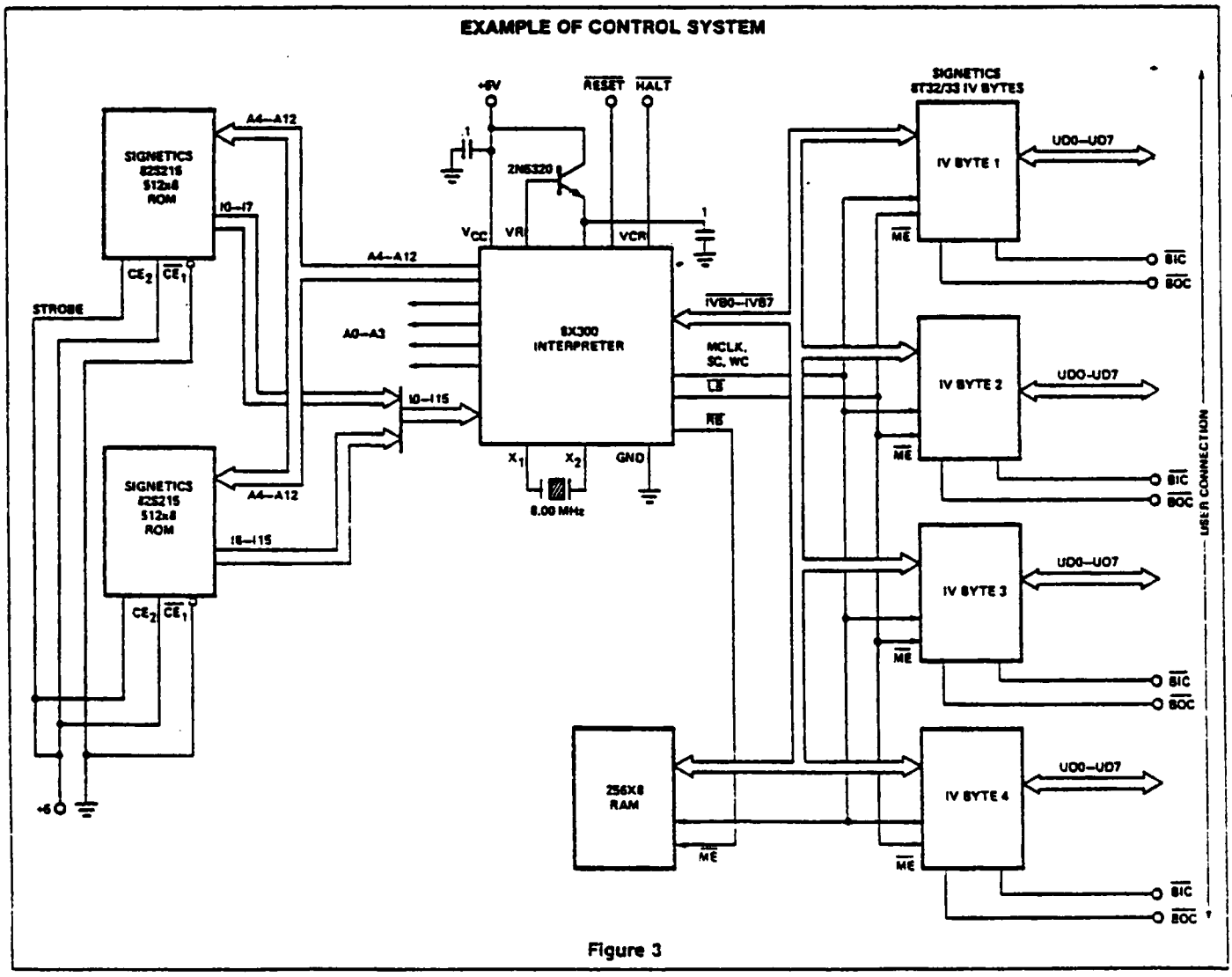


Figure 3

Cx,pF	CYCLE TIME
100	300ns
200	500ns
500	1.1μs
1000	2.0μs

Table 6 CLOCK CAPACITOR VALVES

Halt, Reset Signals

HALT:

A low level at the $\overline{HALT}$ input stops internal operation of the Interpreter at the start of the next instruction after $\overline{HALT}$ is applied (quarter cycle after MCLK). Since $\overline{HALT}$ is sampled at the start of each instruction cycle it is possible to prevent a cycle by applying $\overline{HALT}$ early in that cycle. $\overline{HALT}$ does not inhibit MCLK or affect any internal registers. Normal operation begins with the next complete cycle after the $\overline{HALT}$ input goes high.

RESET:

A low level at the $\overline{RESET}$ input sets the program counter and address register to zero. While $\overline{RESET}$ is low MCLK is inhibited. If $\overline{RESET}$ is applied during the last 2 quarter cycles, the MCLK during that cycle may be shortened. $\overline{RESET}$ should be applied for 1 full instruction cycle time to assure proper operation. When $\overline{RESET}$ input goes high an MCLK occurs prior to the resumption of normal processing. $\overline{RESET}$ does not affect the other internal registers.

EXAMPLE:

A specific example of a control system, using the 8X300 Interpreter—four 8T32/33 IV Bytes, and two 82S215 ROMs is shown in Figure 3. Only 8 components are required to build this system which contains 512 words of program storage, 32 TTL I/O connection points, and operates at a 250ns instruction cycle time.

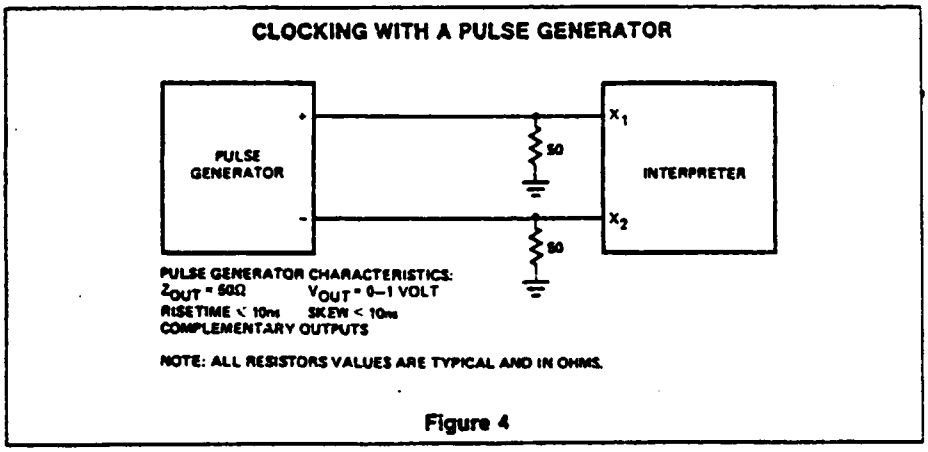


Figure 4

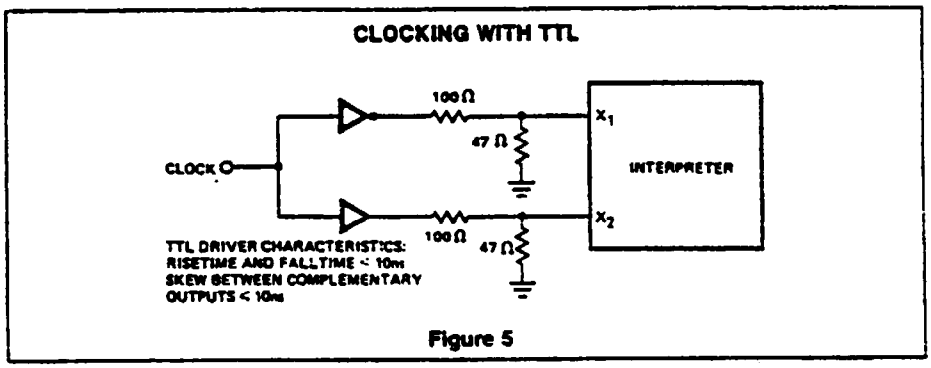


Figure 5

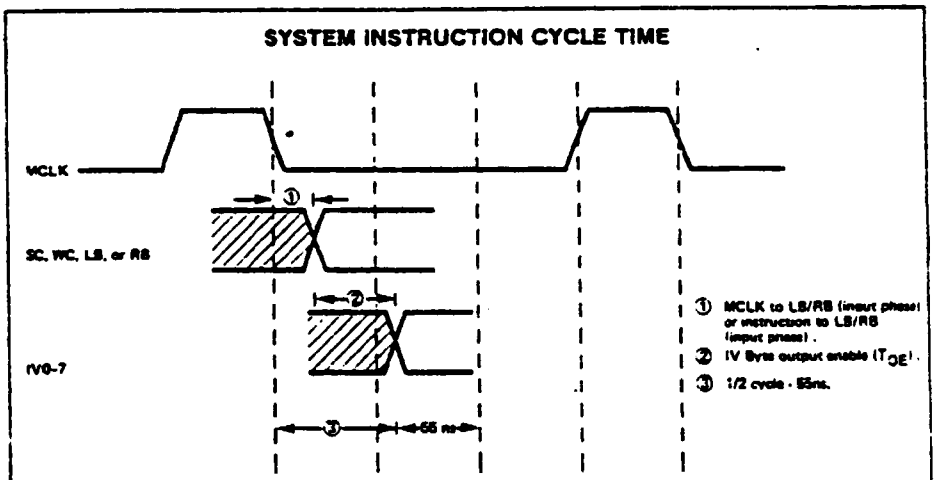


Figure 6

SYSTEM TIMING

In systems with fast instruction cycle times, most Interpreter delays are strictly determined by internal gate propagation delays. Since some events are constrained to occur in certain quarter cycles, as system cycle times become slower, the delays will appear to increase due to gating with internal clocks. In the table of AC Electrical Characteristics, 2 columns are used: 1 to denote times which occur due to internal clock intervention and 1 to denote minimum delays for fast cycle times.

When using Signetics 8T32/33/35/36 IV Bytes, selection of instruction cycle time involves calculating the maximum program storage access time. Assuming the instruction is available when MCLK falls, the I/O control lines are stable 35ns later. Signetics IV Bytes require another 35ns to disable a previously selected byte and enable the desired byte (assumes a change in bank signals). A 10ns margin has been added to the IV Byte enable for this evaluation to reflect the fact that most systems will have more capacitive loading than the 50pF test condition in the IV Byte specification and to allow for line delays.

The system instruction cycle time for normal systems such as shown in Figure 7 is determined by Interpreter propagation delays, program storage access time, and IV Byte output enable times. Instruction cycle time is normally constrained by one or more of the following conditions:

1. Instruction to LB/RB (input phase) and IV Byte output enable:
   $T_{OE} \leq$ ½ cycle - 55ns (Figure 6).

2. Program storage access time and instruction to LB/RB (input phase) and IV Byte output enable and IV data (input phase) to address ≤ instruction cycle time (Figure 7).
3. Program storage access time and instruction to address ≤ instruction cycle time (Figure 8).

The first constraint can be used to determine the minimum cycle time. Using the inequality 35ns + 35ns ≤ ½ cycle - 55ns implies ½ cycle ≥ 125ns or an instruction time of 250ns.

Program storage access time for a 250ns instruction cycle can be calculated from the second constraint. Noting that the specification for IV data (input phase) to address is 115ns: Program storage access time + 35ns + 35ns + 115ns ≤ 250ns implies program storage access time ≤ 65ns.

The third constraint can be used to verify the maximum program storage access time. Noting that the specification for instruction to address is 185ns: Program storage access time + 185ns ≤ 250ns confirms that program storage access time 65ns is satisfactory.

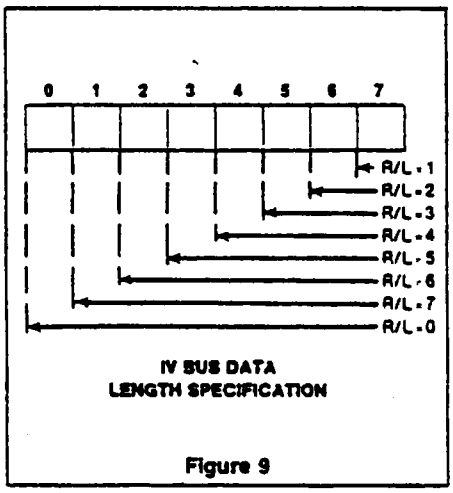


Figure 9

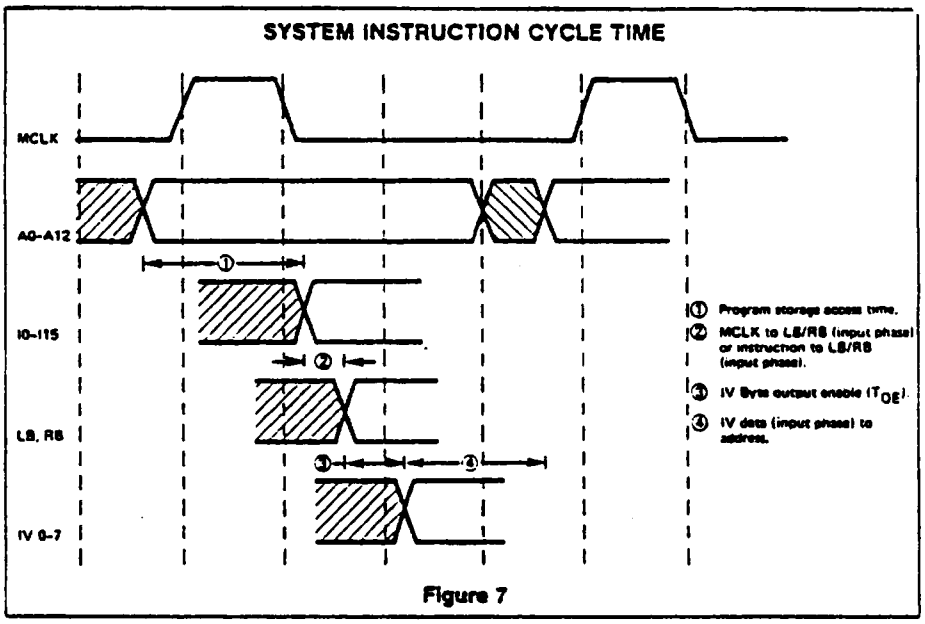


Figure 7

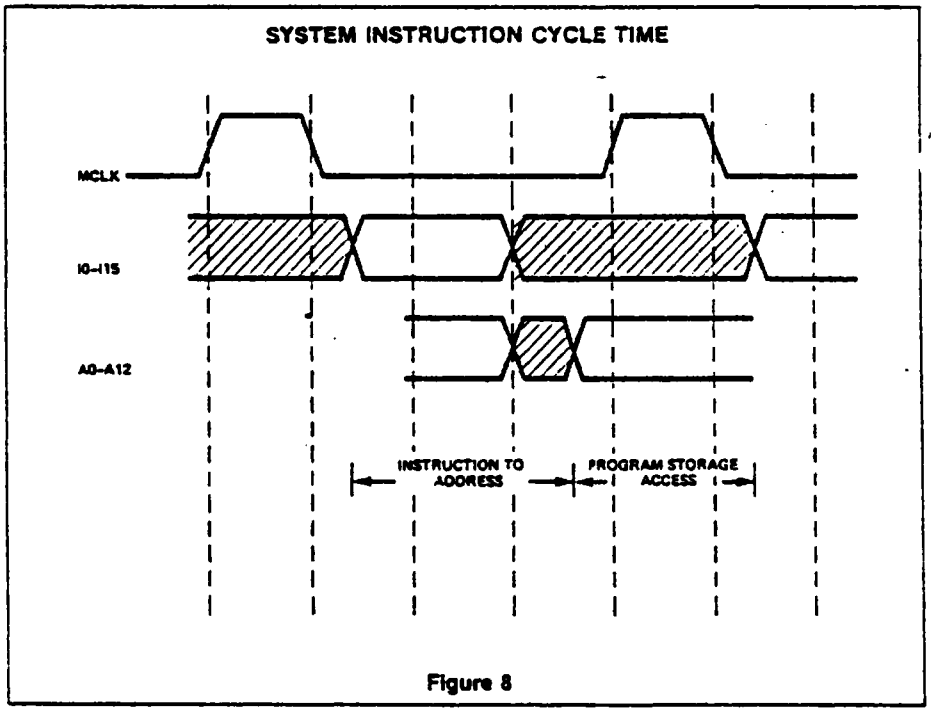


Figure 8

TYPICAL INSTRUCTION CYCLE TIMING

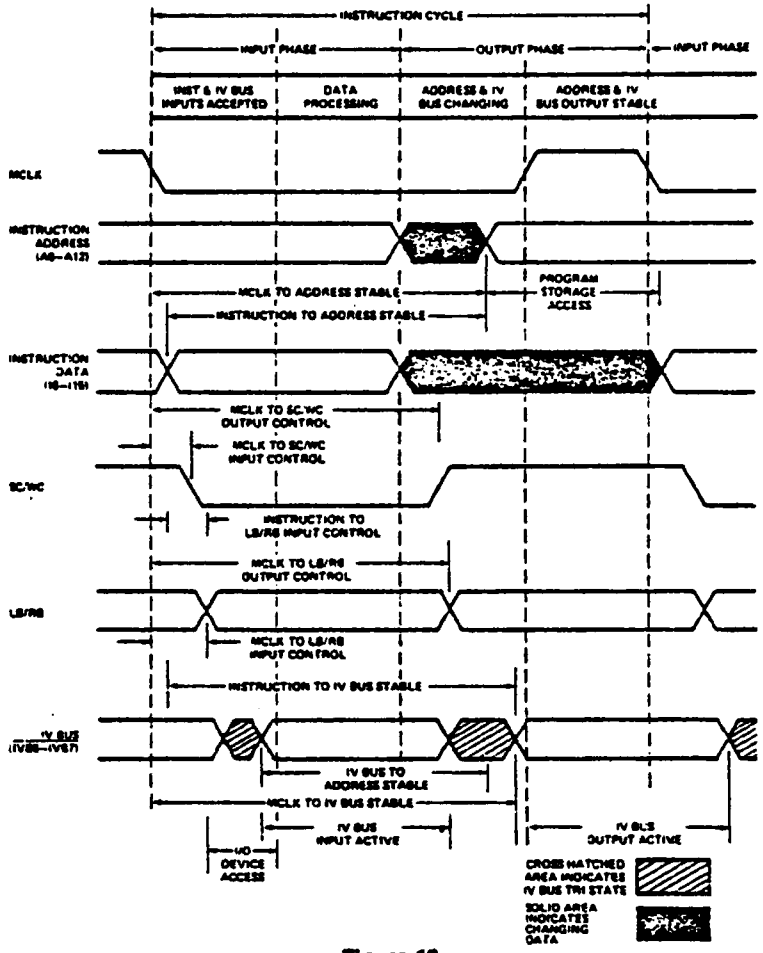


Figure 10

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 7V
Logic Input Voltage 5.5V
Crystal Input Voltage 2V

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5% and 0°C ≤ T_A < 70°C

DELAY DESCRIPTION	PROPAGATION DELAY TIME	CYCLE TIME LIMIT
X1 falling edge to MCLK (driven from external pulse generator)	75ns	
MCLK to SC/WC falling edge (input phase)	25ns	
MCLK to SC/WC rising edge (output phase)		½ cycle + 25ns
MCLK to LB/RB (input phase)	35ns	
Instruction to LB/RB output (input phase)	35ns	
MCLK to LB/RB (output phase)		¼ cycle + 35ns
MCLK to IV data (output phase)	185ns	½ cycle + 60ns
IV data (input phase) to IV data (output phase)	115ns	
Instruction to Address	185ns	½ cycle + 40ns
MCLK to Address	185ns	½ cycle + 40ns
IV data (input phase) to Address	115ns	
MCLK to IV data (input phase)		½ cycle – 55ns
MCLK to Halt falling edge to prevent current cycle		¼ cycle – 40ns
Reset rising edge to first MCLK		0 to 1 cycle

NOTE
1. Reference to MCLK is to the falling edge when loaded with 300pF
2. Loading on Address lines is 150pF

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	High level input voltage					
	X1,X2		.6			V
	All others		2			V
V_{IL}	Low level input voltage					
	X1,X2				.4	V
	All others				.8	V
V_{CL}	Input clamp voltage (Note 1)	V_{CC} = 4.75V I_I = -10mA			-1.5	V
I_{IH}	High level input current					
	X1,X2	V_{CC} = 5.25V V_{IH} = .6V		2700		μA
	All others	V_{CC} = 5.25V V_{IH} = 4.5V		<1	50	μA
I_{IL}	Low level input current					
	X1,X2	V_{CC} = 5.25V		-2500		μA
	$\overline{IVBO}$-7	V_{IL} = .4V		-140	-200	μA
	IO-I15	V_{CC} = 5.25V V_{IL} = .4V		-880	-1600	μA
	$\overline{HALT}$, $\overline{RESET}$	V_{CC} = 5.25V V_{IL} = .4V		-230	-400	μA
V_{OL}	Low level output voltage					
	A0-A12	V_{CC} = 4.75V I_{OL} = 4.25mA		.35	.55	V
	All others	V_{CC} = 4.75V I_{OL} = 16mA		.35	.55	V
V_{OH}	High level output voltage	V_{CC} = 4.75V I_{OH} = 3mA	2.4			V
I_{OS}	Short circuit output current (Note 2)	V_{CC} = 5.25V	-30		-140	mA
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current	V_{CC} = 5.25V		300	450	mA
I_{REG}	Regulator control	V_{CC} = 5.0V	-14		-21	mA
I_{CR}	Regulator current (Note 3)	V_{CR} = 0			290	mA
V_{CR}	Regulator voltage (Note 3)	V_{REG} = 0V	2.2		3.2	V

NOTES

1. Crystal inputs X1 and X2 do not have clamp diodes.
2. Only one output may be grounded at a time.
3. (Limits apply for V_{CC} = 5V ± 5% and 0°C < T_A < 70°C unless specified otherwise.)

8T32 8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT

TYPES

8T32 Tri-State, Synchronous User Port
8T33 Open Collector, Synchronous User Port
8T35 Open Collector, Asynchronous User Port
8T36 Tri-State, Asynchronous User Port

DESCRIPTION

The Interface Vector (IV) Byte is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 data latches accessible from either a microprocessor (IV) port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the IV Byte. In this case, the user port has priority.

A unique feature of the 8T32/33/35/36 IV Byte is the way in which it is addressed. Each IV Byte has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the IV Byte's internally programmed address, the microprocessor port is enabled, allowing data transfer through it.

The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input ($\overline{ME}$) can serve as a ninth address bit, allowing 512 IV Bytes to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

A unique feature of this family is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the IV port will be all logic 0 levels.

ORDERING

The 8T32/33/35/36 may be ordered in preaddressed form. To order a preaddressed IV Byte, use the following part number format:

N8TYY-XXX P

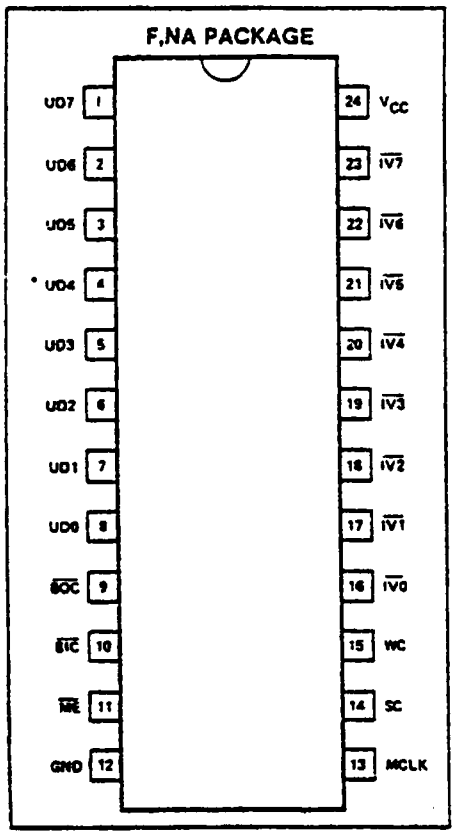
- -P = F Ceramic package, NA Plastic package
- XXX = Any address from 000 through 255 (decimal) - 256 available addresses
- YY = IV Byte version (32, 33, 35, 36)

A stock of 8T32s and 8T36s with addresses 1 through 10 will be maintained. A small quantity of addresses 11 through 50 will also be available with a longer lead time.

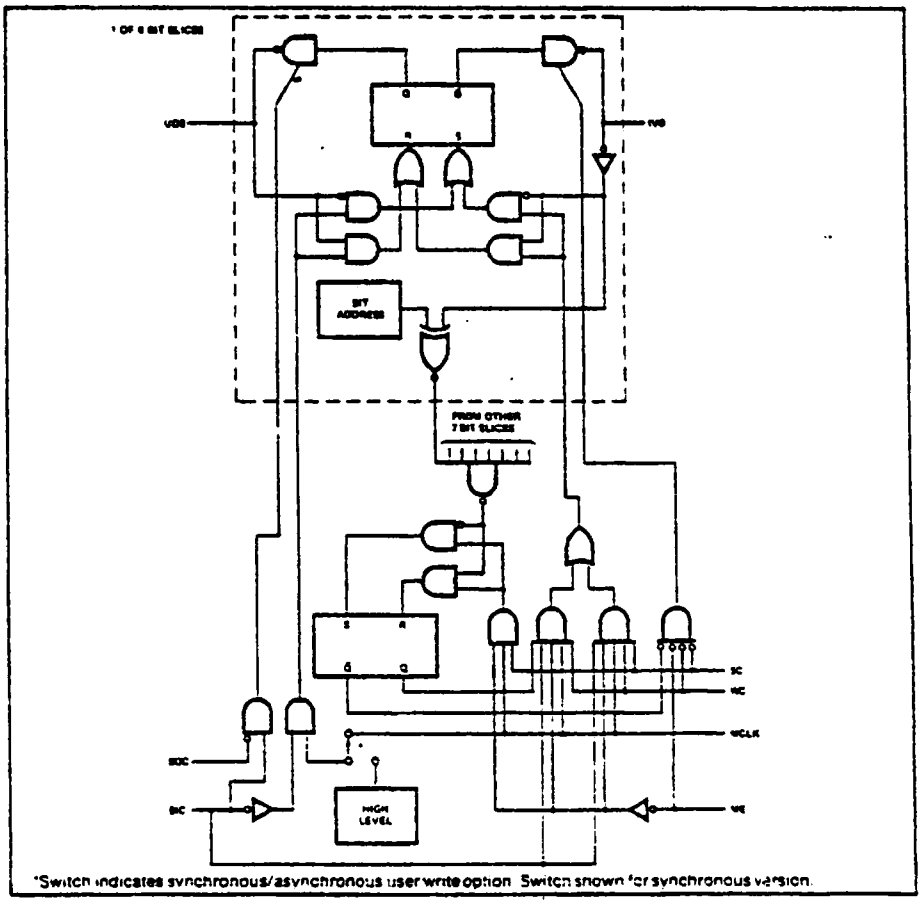
FEATURES

- A field-programmable address allows 1 of 512 IV Bytes on a bus to be selected, without decoders.
- Each byte has 2 ports, one to the user, the other to a microprocessor. IV Bytes are completely bidirectional.
- Ports are independent, with the user port having priority for data entry.
- A selected IV Byte de-selects itself when another IV Byte address is sensed.
- User data input available as synchronous (8T32, 8T33) or as asynchronous (8T35, 8T36) function.
- The User Data Bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs.
- At power up, the IV Byte is not selected and the user port outputs are high.
- Tri-state TTL outputs for high drive capability.
- Directly compatible with the 8X300 Interpreter.
- Operates from a single 5V power supply over a temperature range of 0° C to 70° C.

PIN CONFIGURATION



BLOCK DIAGRAM



*Switch indicates synchronous/asynchronous user write option. Switch shown for synchronous version.

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	$\overline{UD0}$-$\overline{UD7}$:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment. Either tri-state or open collector outputs are available.	Active high
16-23	$\overline{IV0}$-$\overline{IV7}$:	Interface Vector (IV) Bus. Bidirectional data lines to communicate with controlling digital system (microprocessor).	Active low three-state
10	$\overline{BIC}$:	Byte Input Control. User input to control writing into the IV Byte from the User Data Lines.	Active low
9	$\overline{BOC}$:	Byte Output Control. User input to control reading from the IV Byte onto the User Data Lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high and SC is low, IV Byte, if selected, stores contents of IV0-IV7 as data.	Active high
14	SC:	Select Command. When SC is high and WC is low, data on IV0-IV7 is interpreted as an address. IV Byte selects itself if its address is identical to IV bus data; it de-selects itself otherwise.	Active high
13	MCLK:	Master Clock. Input to strobe data into the latches. See function tables for details.	Active high
24	VCC:	5V power connection.	
12	GND:	Ground.	

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION	
			8T32, 8T33	8T35, 8T36
H	L	X	Output Data	Output Data
L	X	H	Input Data	Input Data
L	X	L	Inactive	Input Data
H	H	X	Inactive	Inactive

H = High Level L = Low Level X = Don't care

Table 1 USER PORT CONTROL FUNCTION

$\overline{ME}$	SC	WC	MCLK	$\overline{BIC}$	STATUS LATCH	IV BUS FUNCTION
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

Table 2 MICROPROCESSOR PORT CONTROL FUNCTION

USER DATA BUS CONTROL

The activity of the User Data Bus is controlled by the BIC and BOC inputs as shown in Table 1.

For the 8T32 and 8T33, User Data Input is a synchronous function with MCLK. A low level on the BIC input allows data on the User Data Bus to be written into the Data Latches only if MCLK is at a high level. For the 8T35 and 8T36, User Data Input is an asynchronous function. A low level on the BIC input allows data on the User Data Bus to be latched regardless of the level of the MCLK input. Note that when 8T35 or 8T36 IV Bytes are used with the 8X300 Interpreter care must be taken to insure that the IV Bus is stable when it is being read by the 8X300 Interpreter.

To avoid conflicts at the Data Latches, input from the Microprocessor Port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

INTERFACE VECTOR BUS CONTROL

As is shown in Table 2, the activity of t microprocessor port (IV Bus) is controll by the ME, SC, WC and BIC inputs, as well as the state of an internal status latch. BIC is included to show user port priority over the microprocessor port for data input.

Each IV Byte's status latch stores the result of the most recent IV Byte select: it is set when the IV Byte's internal address matches the IV Bus. It is cleared when an address that differs from the internal address is presented on the IV Bus.

In normal operation, the state of the status latch acts like a master enable: the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the IV Bus is accepted as data, whether or not the IV Byte was selected. The data is also interpreted as an address. The IV Byte sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the IV Byte from one port will appear inverted when read from the other port. Data written into the IV Byte from one port will not be inverted when read fr the same port.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	INPUT	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
t_{PD} User data delay (Note 1)	UDX	C_L = 50pF		25	38	ns
	MCLK*			45	61	
	BIC†			40	55	
t_{OE} User output enable	BOC	C_L = 50pF	18	26	47	ns
t_{OD} User output disable	BIC	C_L = 50pF	18	28	35	ns
	BOC		16	23	33	
t_{PD} IV data delay (Note 1)	IVBX	C_L = 50pF		38	53	ns
	MCLK			48	61	
t_{OE} IV output enable	ME	C_L = 50pF	14	19	25	ns
	SC					
	WC					
t_{OD} IV output disable	ME	C_L = 50pF	13	17	32	ns
	SC					
	WC					
t_W Minimum pulse width	MCLK		40			ns
	BIC†		35			
t_{SETUP} Minimum setup time	UD□	(Note 2)	15			ns
	BIC*		25			
	IVX		55			
	ME		30			
	SC		30			
	WC		30			
t_{HOLD} Minimum hold time	UDX□	(Note 2)	25			ns
	BIC*		10			
	IVX		10			
	ME		5			
	SC		5			
	SC		5			

* Applies for 8T32 and 8T33 only.
† Applies for 8T35 and 8T36 only.
□ Times are referenced to MCLK for 8T32 and 8T33, and are referenced to BIC for 8T35 and 8T36.

NOTES.

1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. BIC setup and hold times are for a user write operation. SC setup and hold times are for an IV Byte select operation. WC setup and hold times are for an IV Bus write operation. ME setup and hold times are for both IV write and select operations.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				.8	
V_{IC}	Clamp	I_I = -5mA			-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OH}	High		2.4			
V_{OL}	Low				.55	
	Input current[3]	V_{CC} = 5.25V				μA
I_{IH}	High	V_{IH} = 5.25V		<10	100	
I_{IL}	Low	V_{IL} = .5V		-350	-550	
	Output current[4]					mA
I_{OS}	Short circuit	V_{CC} = 4.75V				
	UD bus		10			
	IV bus		20			
I_{CC}	V_{CC} supply current	V_{CC} = 5.25V		100	150	mA

PROGRAMMING SPECIFICATIONS[5]

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{CCP}	Programming supply voltage					
	Address		7.5		8.0	V
	Protect			0		V
I_{CCP}	Programming supply current	V_{CCP} = 8.0V			250	mA
	Max time V_{CCP} > 5.25V				1.0	s
	Programming voltage					
	Address		17.5		18.0	V
	Protect		13.5		14.0	V
	Programming current					
	Address				75	mA
	Protect				150	mA
	Programming pulse rise time					
	Address		.1		1	μs
	Protect		100			μs
	Programming pulse width		.5		1	ms

NOTES

3. The input current includes the tri-state/open collector leakage current of the output driver on the data lines.
4. Only one output may be shorted at a time.
5. If all programming can be done in less than 1 second, VCC may remain at 7.75V for the entire programming cycle.

ADDRESS PROGRAMMING

The IV Byte is manufactured such that an address of all high levels (> 2V) on the IV Data Bus inputs matches the Byte's internal address. To program a bit so a low-level input (< 0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state (BIC = BOC = ME = V_{CC}, SC = WC = MCLK = GND). Leave all IV Data Bus I/O pins open.
2. Raise V_{CC} to 7.75V ± .25V.
3. After V_{CC} has stabilized, apply a single programming pulse to the User Data Bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited to 75mA. Apply the pulse as shown in Figure 1.
4. Return V_{CC} to 0V. (Note 6).
5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Byte's status latch (IV0-IV7 = desired address, ME = WC = L, SC = MCLK = H). If the proper address has been programmed, data presented at the IV Bus will appear inverted on the User Bus outputs. (Use normal V_{CC} and input voltage for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = BIC = BOC = ME = SC = WC = MCLK = 0V). Leave all IV Data Bus I/O pins open.
2. Apply a protect programming pulse to every User Data Bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Figure 2.
3. Verify that the address circuitry is isolated by applying 7V to each User Data Bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	-0.5 to +7	Vdc
V_{IN}	Input voltage	-0.5 to +5.5	Vdc
V_O	Off-state output voltage	-0.5 to +5.5	Vdc
T_A	Operating temperature range	-55 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

ADDRESS PROGRAMMING PULSE

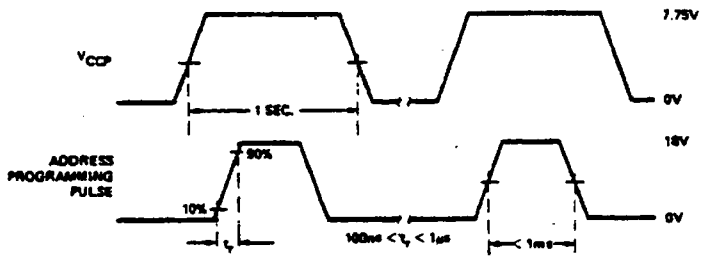


Figure 1

PROTECT PROGRAMMING PULSE

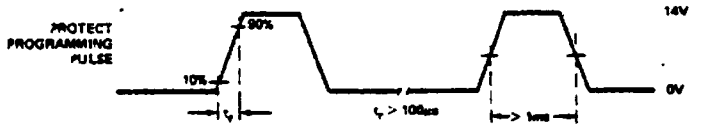
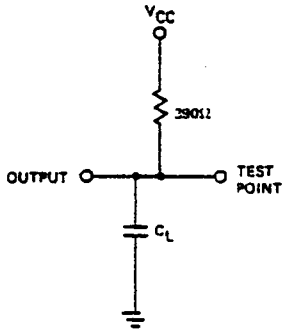


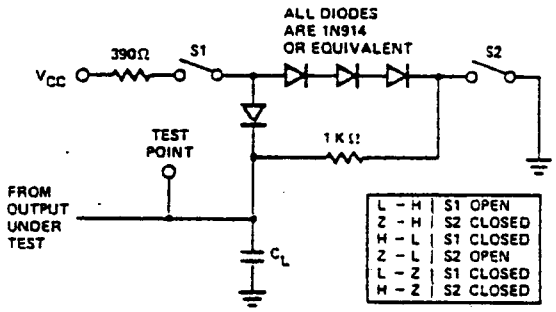
Figure 2

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR OPEN COLLECTOR OUTPUTS

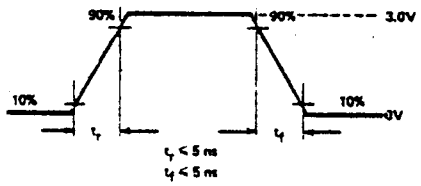


LOAD CIRCUIT FOR TRI-STATE OUTPUTS

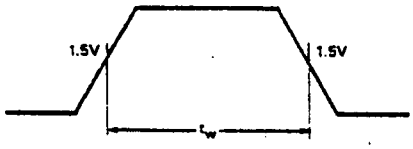


NOTE: C_L includes fixture capacitance.

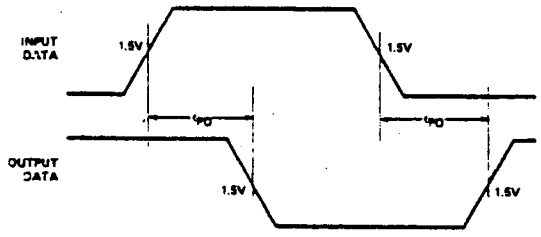
INPUT WAVEFORM



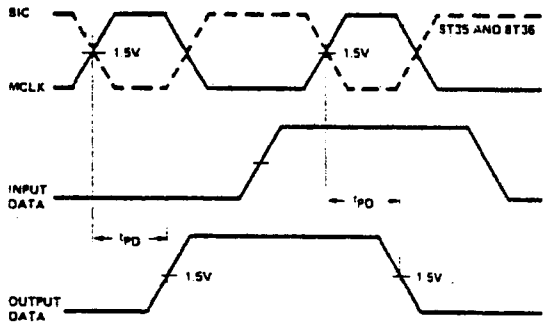
CLOCK PULSE WIDTH



DATA DELAY TIMES
Input Data Reference

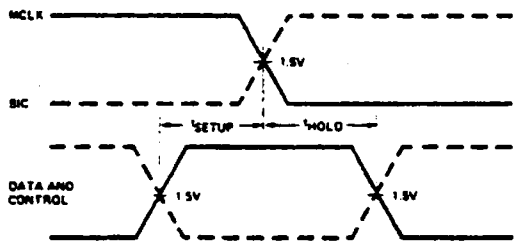


DATA DELAY TIMES
Clock Referenced

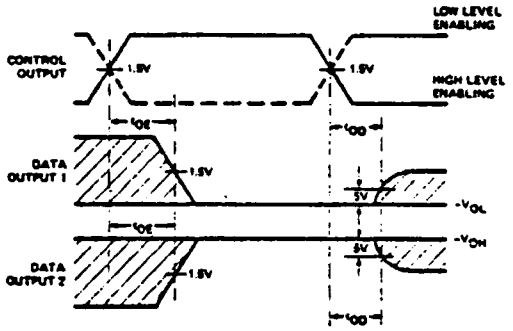


PARAMETER MEASUREMENT INFORMATION (Cont'd)

SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Tri-State Outputs)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE TRI-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.

APPLICATIONS

Figure 3 shows some of the various ways to use the IV Byte in a system. By controlling the BIC and BOC lines, the Bytes may be used for the input and output of data, control, and status signals. IV Byte 1 functions bidirectionally for data transfer and IV Byte 2 provides a similar function for discrete status and control lines. IV Bytes 3 and 4 serve as dedicated output and input ports, respectively.

IV BYTE APPLICATIONS

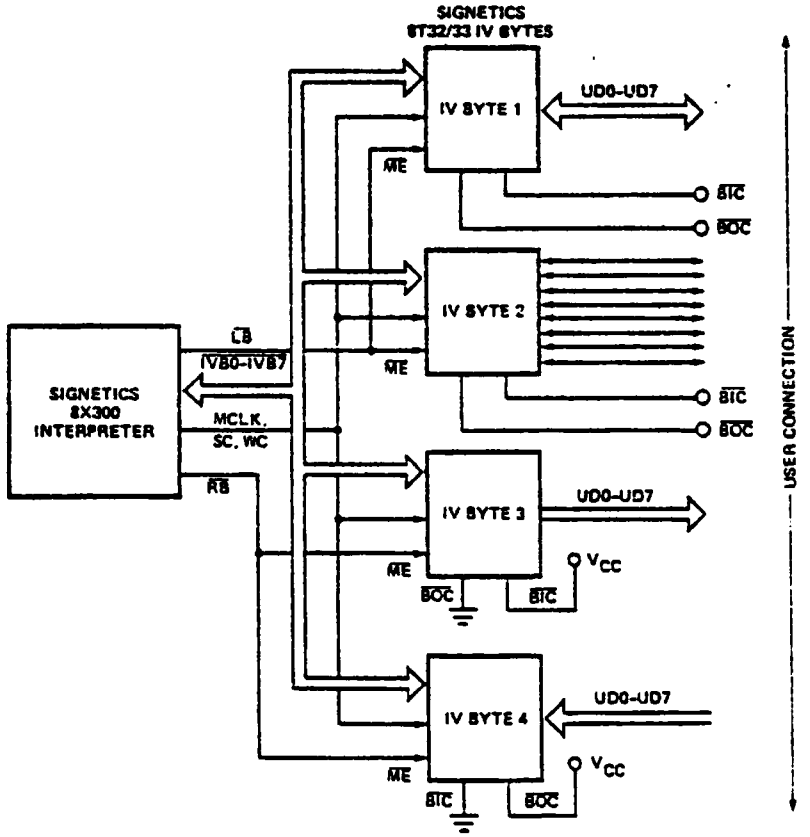


Figure 3

CRC GENERATOR/CHECKER (9401)

DESCRIPTION — The 9401 Cyclic Redundancy Check (CRC) Generator/Checker provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Individual clear and preset inputs are provided for floppy disc and other applications. The Error Output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 9401 is a member of Fairchild's MACROLOGIC family and is fully compatible with all TTL families.

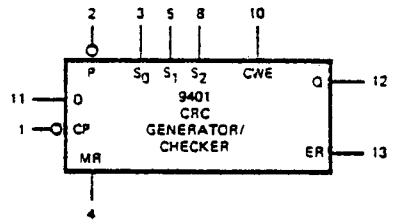
- GUARANTEED 12 MHz DATA RATE
- EIGHT SELECTABLE POLYNOMIALS
- ERROR INDICATOR
- SEPARATE PRESET AND CLEAR CONTROLS
- AUTOMATIC RIGHT JUSTIFICATION
- FULLY COMPATIBLE WITH ALL TTL LOGIC FAMILIES
- 14-PIN PACKAGE
- TYPICAL APPLICATIONS:
  - FLOPPY AND OTHER DISC STORAGE SYSTEMS
  - DIGITAL CASSETTE AND CARTRIDGE SYSTEMS
  - DATA COMMUNICATION SYSTEMS

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Polynomial Select Inputs	0.5 U.L.	0.23 U.L.
$\overline{D}$	Data Input	0.5 U.L.	0.23 U.L.
$\overline{CP}$	Clock (Operates on HIGH to LOW Transition) Input	0.5 U.L.	0.23 U.L.
CWE	Check Word Enable Input	0.5 U.L.	0.23 U.L.
$\overline{P}$	Preset (Active LOW) Input	0.5 U.L.	0.23 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.23 U.L.
Q	Data Output (Note b)	10 U.L.	5 U.L.
ER	Error Output (Note b)	10 U.L.	5 U.L.

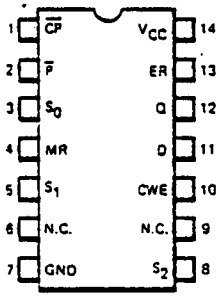
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

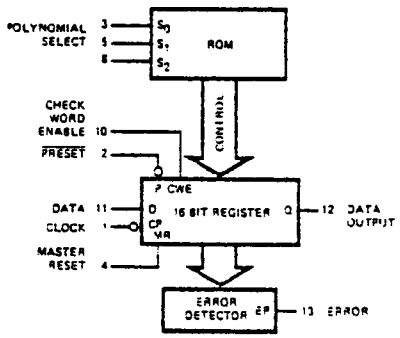
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



V_{CC} = 14
GND = 7

FUNCTIONAL DESCRIPTION – The 9401 Cyclic Redundancy Check (CRC) Generator/Checker is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 9401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the HIGH to LOW transition of the Clock Input ($\overline{CP}$). This data is gated with the most significant Output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWE Input held HIGH. The 9401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 9401 by a HIGH to LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH. ER remains valid until the next HIGH to LOW transition of $\overline{CP}$ or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the register. A LOW on the Preset Input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE 1

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$x^{16}+x^{15}+x^2+1$	CRC-16
L	L	H	$x^{16}+x^{14}+x+1$	CRC-16 REVERSE
L	H	L	$x^{16}+x^{15}+x^{13}+x^7+x^4+x^2+x^1+1$	
L	H	H	$x^{12}+x^{11}+x^3+x^2+x+1$	CRC-12
H	L	L	$x^8+x^7+x^5+x^4+x+1$	
H	L	H	x^8+1	LRC-8
H	H	L	$x^{16}+x^{12}+x^5+1$	CRC-CCITT
H	H	H	$x^{16}+x^{11}+x^4+1$	CRC-CCITT REVERSE

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage	XM & XC		0.35	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.45	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			70	110	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 2)	MAX			
f_{max}	Maximum Clock Frequency	12	20		MHz	Fig. 3, 4, 5	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR to Data Output		30	55	ns		
t_{PHL} t_{PLH}	Propagation Delay, Preset to Data Output		40	60	ns		
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR or Preset to Error Output		40	60	ns		

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP	MAX			
$t_w\overline{CP}$ (L)	Clock Pulse Width (LOW)	35			ns	Fig. 2	C_L = 15 pF
t_sD	Set-up Time, Data to Clock		35	55	ns	Fig. 6	
t_sCWE	Set-up Time, CWE to Clock		35	55	ns		
t_h	Hold Time, Data and CWE to Clock		0		ns		
t_wP (L)	Preset Pulse Width (LOW)	35	25		ns	Fig. 4	
t_wMR (H)	Master Reset Pulse Width (HIGH)	35	25		ns	Fig. 6	
t_{rec}	Recovery Time, MR and Preset to Clock		25	35	ns	Fig. 4, 5	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$

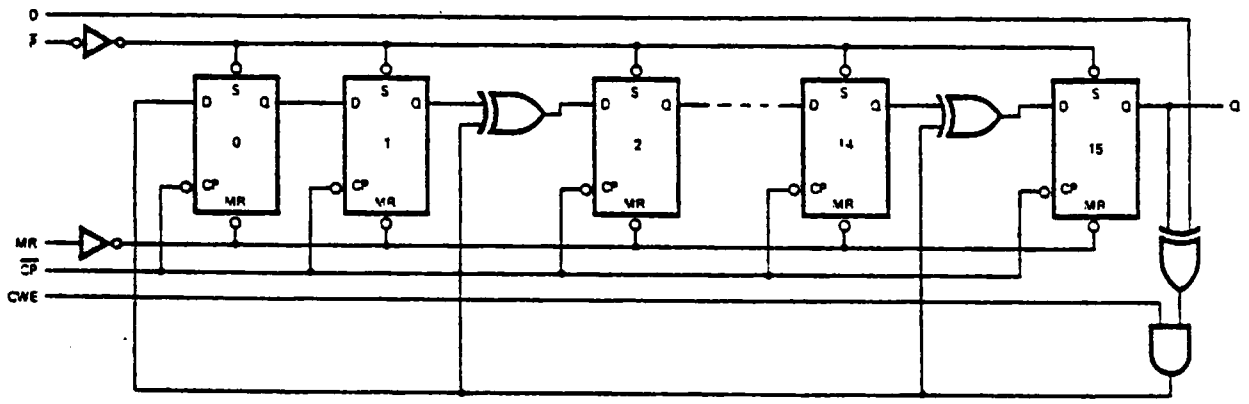
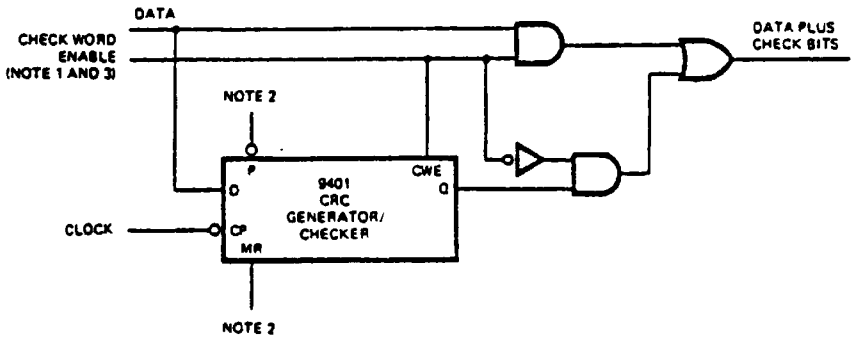


Fig. 1



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Fig. 2
CHECK WORD GENERATION

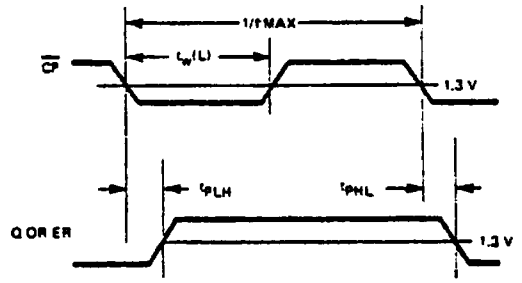


Fig. 3
PROPAGATION DELAYS, $\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

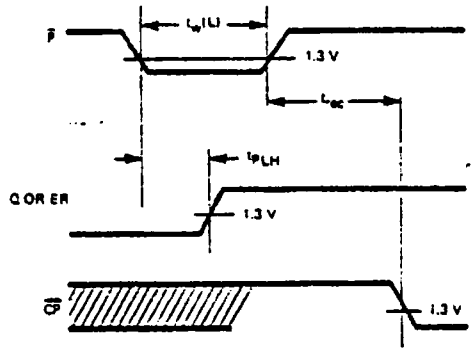


Fig. 4
PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER PLUS RECOVERY TIME P TO $\overline{CP}$

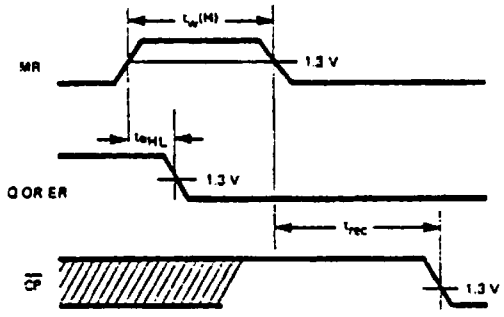


Fig. 5
PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO $\overline{CP}$

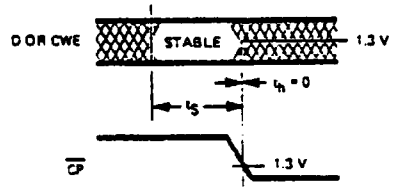


Fig. 6
SET-UP AND HOLD TIMES, D TO $\overline{CP}$ AND CWE TO $\overline{CP}$

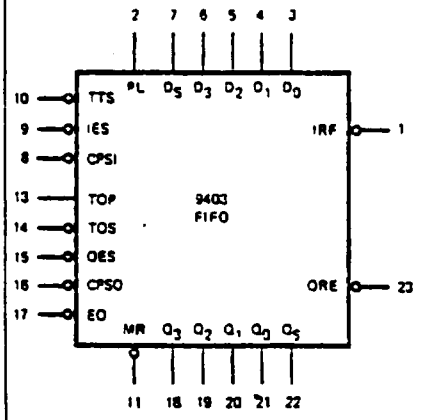
FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY (9403)

DESCRIPTION – The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of 4). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility. It is a member of Fairchild's TTL MACROLOGIC family and is fully compatible with all TTL families.

- **14 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **24-PIN PACKAGE**

LOGIC SYMBOL



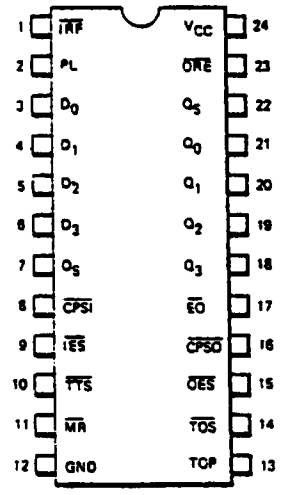
V_{CC} = Pin 24
GND = Pin 12

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Parallel Data Inputs	0.5 U.L.	0.23 U.L.
D_S	Serial Data Input.	0.5 U.L.	0.23 U.L.
PL	Parallel Load Input	0.5 U.L.	0.23 U.L.
$\overline{CPSI}$	Serial Input Clock (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$\overline{IES}$	Serial Input Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{TTS}$	Transfer to Stack Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{OES}$	Serial Output Enable Input (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)	0.5 U.L.	0.23 U.L.
TOP	Transfer Out Parallel Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CPSO}$	Serial Output Clock Input (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$Q_0 - Q_3$	Parallel Data Outputs (Note b)	130 U.L.	10 U.L.
Q_S	Serial Data Output (Note b)	10 U.L.	10 U.L.
$\overline{IRF}$	Input Register Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{ORE}$	Output Register Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

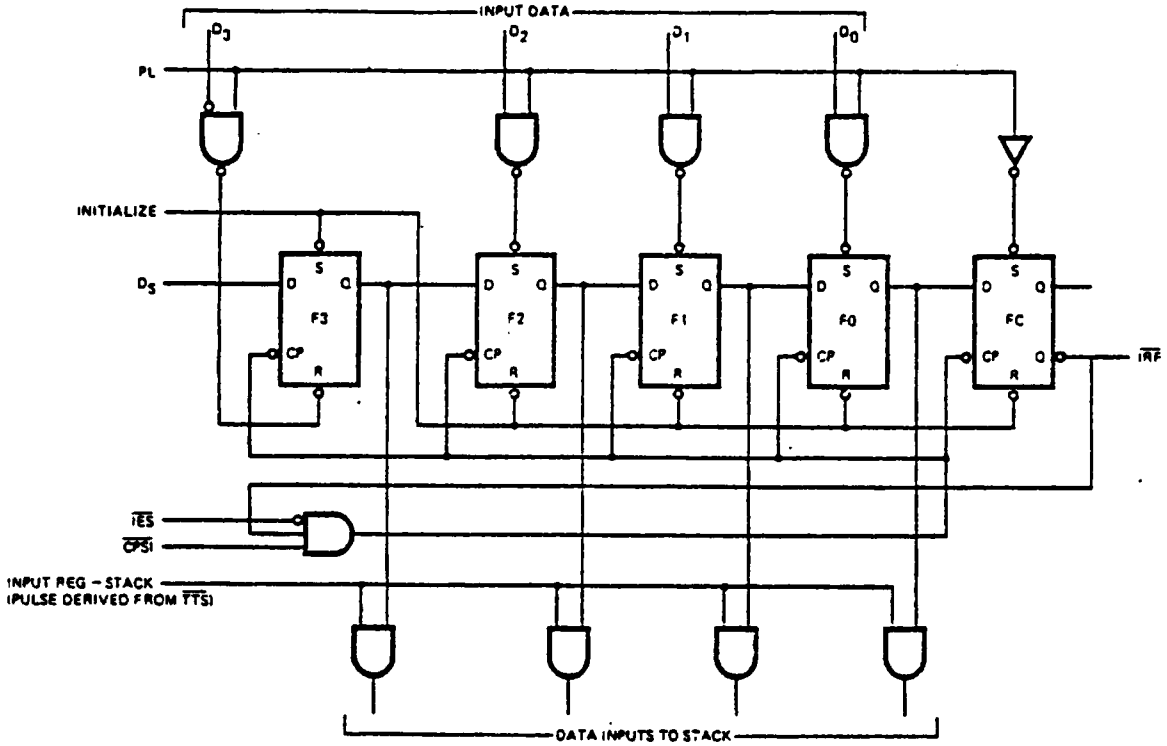


Fig. 1
CONCEPTUAL INPUT SECTION

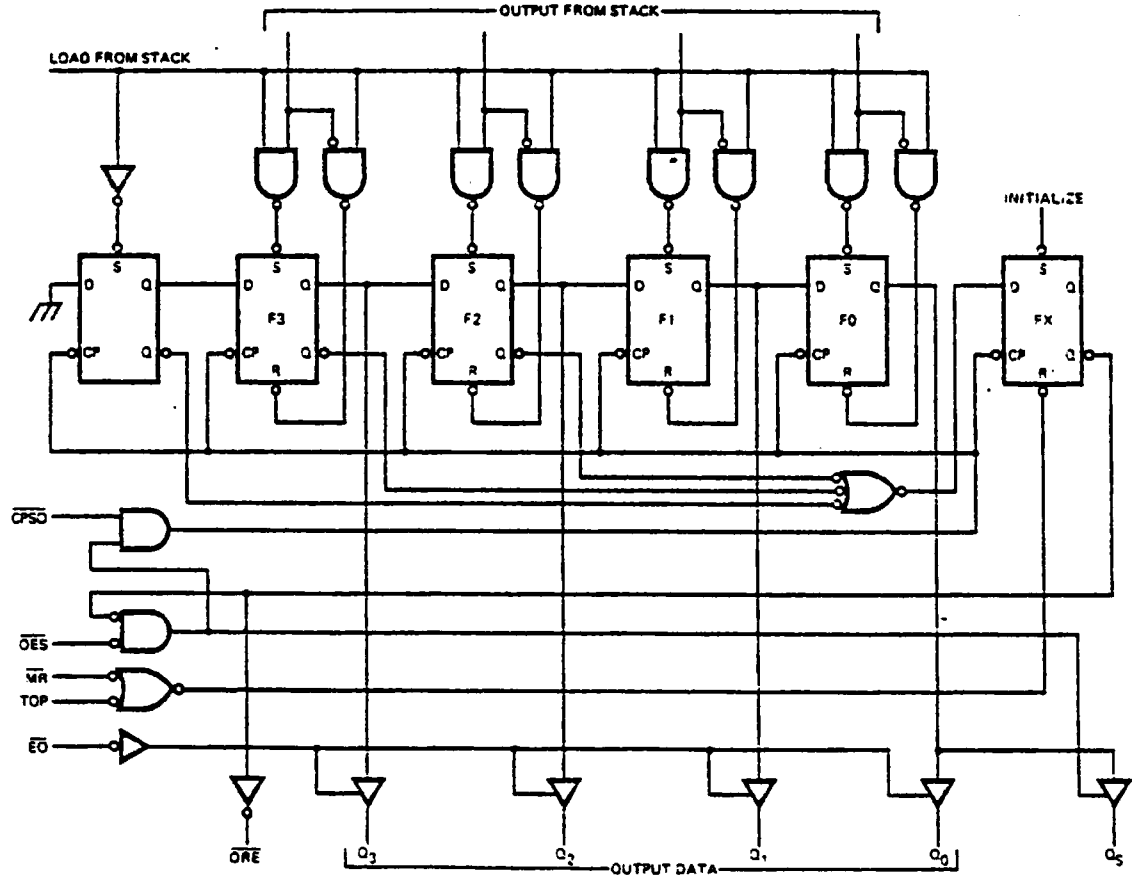
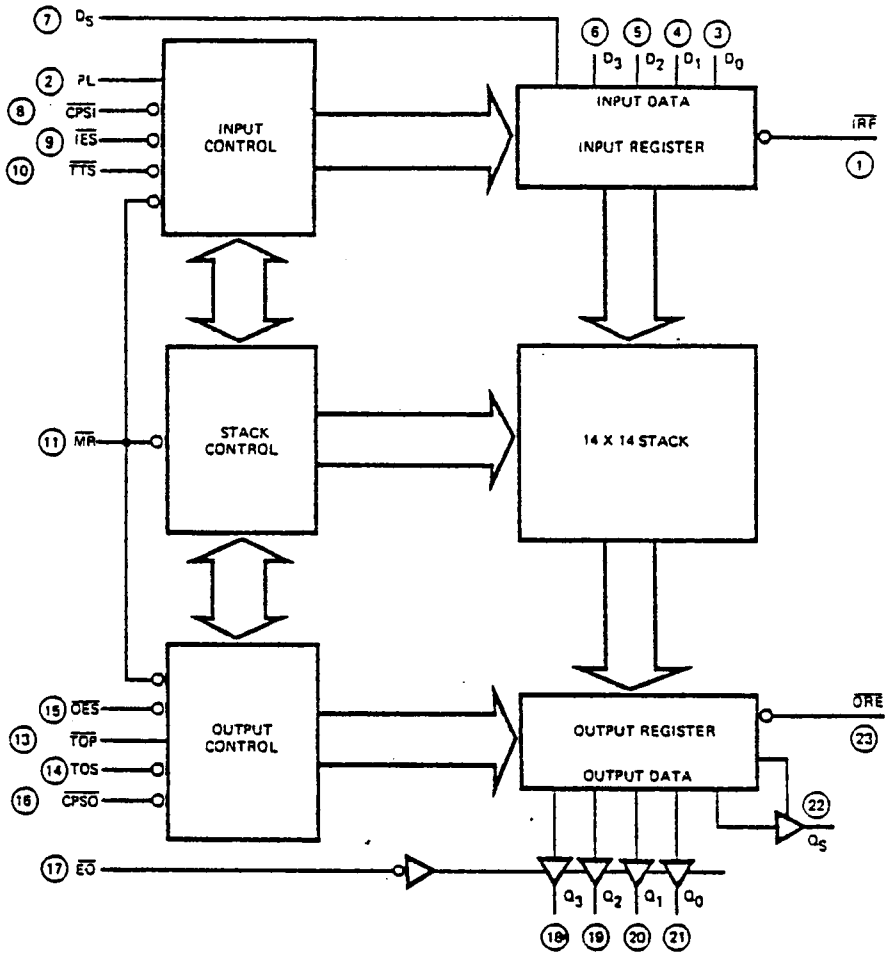


Fig. 2
CONCEPTUAL OUTPUT SECTION

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION — As shown in the Block Diagram the 9403 consists of three parts:

1. An Input Register with Parallel and Serial Data Inputs as well as control inputs and outputs for input handshaking and expansion.

2. A 4-bit wide, 14-word deep Fall-Through Stack with self-contained control logic.

3. An Output Register with Parallel and Serial Data Outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

INPUT REGISTER (DATA ENTRY):

The Input Register can receive data in either bit-serial or in 4-bit parallel form, store it until it is sent to the Fall-Through Stack and generate and accept the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 Flip-Flop and resetting the other flip-flops. The $\overline{Q}$ Output of the last Flip-Flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

PARALLEL ENTRY:
A HIGH level on the PL Input loads the $D_0 - D_3$ Data Inputs into the F0 – F3 Flip-Flops and sets the FC Flip-Flop, which forces $\overline{IRF}$ LOW, indicating "Input Register Full". The D Inputs must be stable while PL is HIGH. During parallel entry, the $\overline{IES}$ Input should be LOW; the $\overline{CPSI}$ Input may be either HIGH or LOW.

SERIAL ENTRY:
Data on the DS Input is serially entered into the F3, F2, F1, F0, FC Shift Register on each HIGH-to-LOW transition of the $\overline{CPSI}$ Clock Input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition the four serial data bits are aligned in the four data flip-flops and the FC Flip-Flop is set, forcing $\overline{IRF}$ LOW (Input Register full) and internally inhibiting further $\overline{CPSI}$ clock pulses. Figure 3 illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B0 is the first bit, B63 the last bit.

TRANSFER TO THE FALL-THROUGH STACK:
The outputs of Flip-Flops F0 – F3 feed the Stack. A LOW level on the $\overline{TTS}$ Input attempts to initiate a "fall-through" action. If the top location of the Stack is empty, data is loaded into the Stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

Data falls through the Stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the Stack control section and does not clear the data.

OUTPUT REGISTER (DATA EXTRACTION):
The Output Register receives 4-bit data words from the bottom Stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 2 is a conceptual logic diagram of the output section.

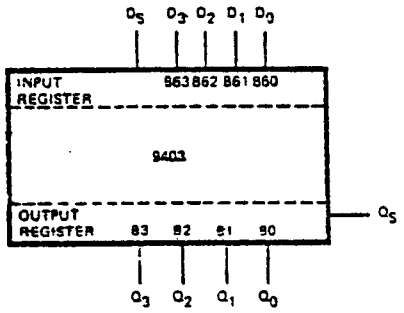


Fig. 3
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

PARALLEL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) Output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output register, provided the "Transfer Out Parallel" (TOP) Input is HIGH, and the $\overline{OES}$ Input is LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next LOW-to-HIGH transition of TOP transfers the next word (if available) into the output register as explained above. During parallel data extraction, $\overline{TOS}$, $\overline{CPSO}$, and $\overline{OES}$ should be LOW.

SERIAL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output shift register provided the "Transfer Out Serial" ($\overline{TOS}$) is LOW. TOP must be HIGH, and $\overline{OES}$ and $\overline{CPSO}$ must be LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the shift register. The 3-state serial Data Output Q_S is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW and disables the serial output Q_S. For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the Stack as soon as the previous one has been shifted out.

EXPANSION:

Vertical Expansion – The 9403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of 15n + 1 words by four bits can be constructed. Note that expansion does ot sacrifice any of the FIFO's flexibility tor serial/parallel input and output.

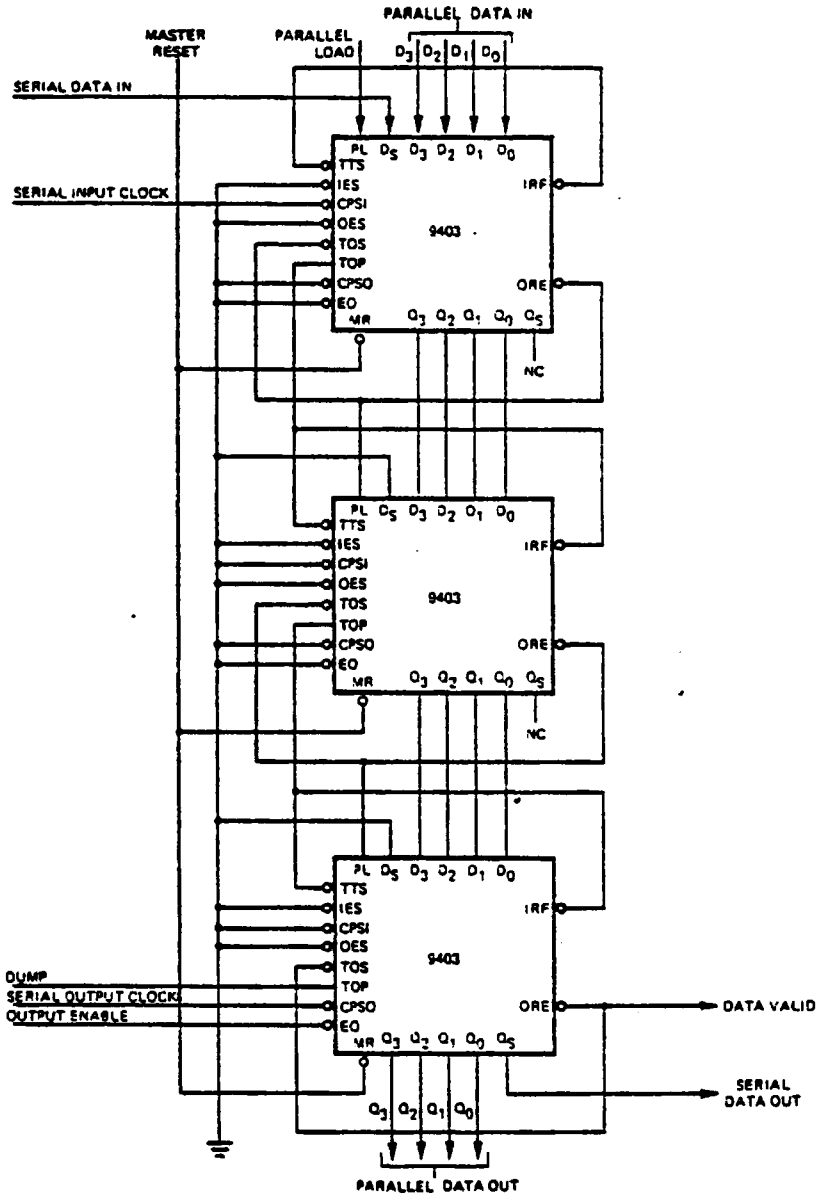


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 9403 may also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 16 words by 4 X n bits can be constructed. When expanding in the horizontal direction, it is usual to connect the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs respectively of all devices to the left (less significant devices) to guarantee that no operation is initiated before all devices are ready.

As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the FIFO's flexibility for serial/parallel input and output.

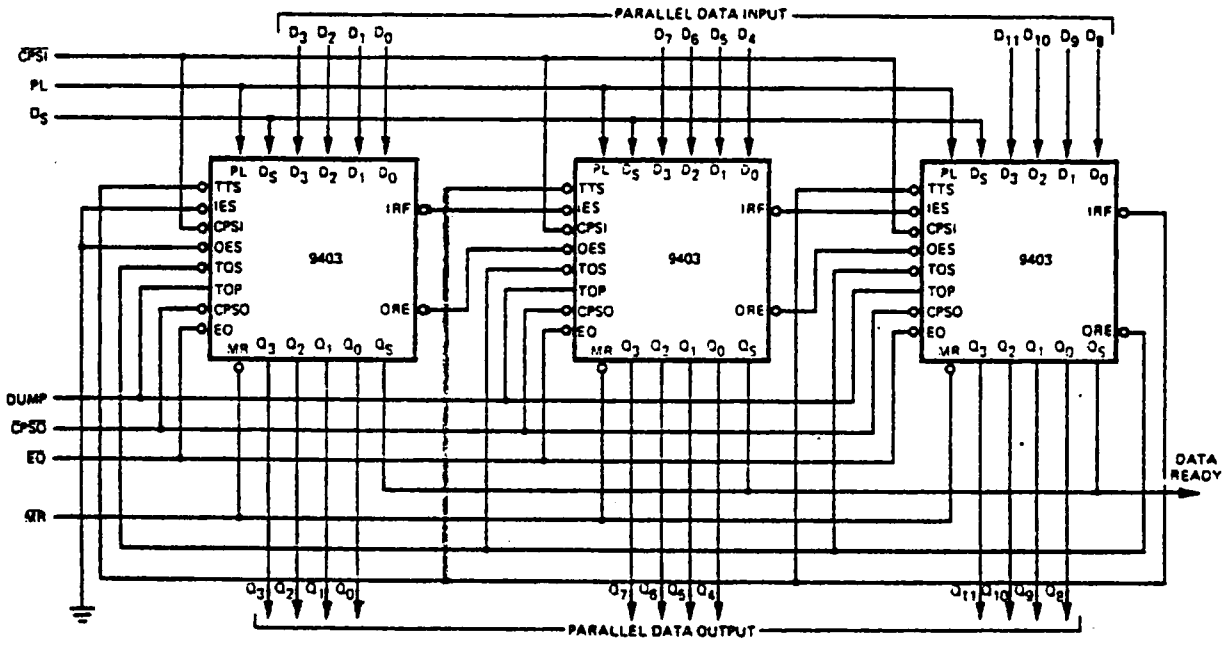


Fig. 5
A HORIZONTAL EXPANSION SCHEME

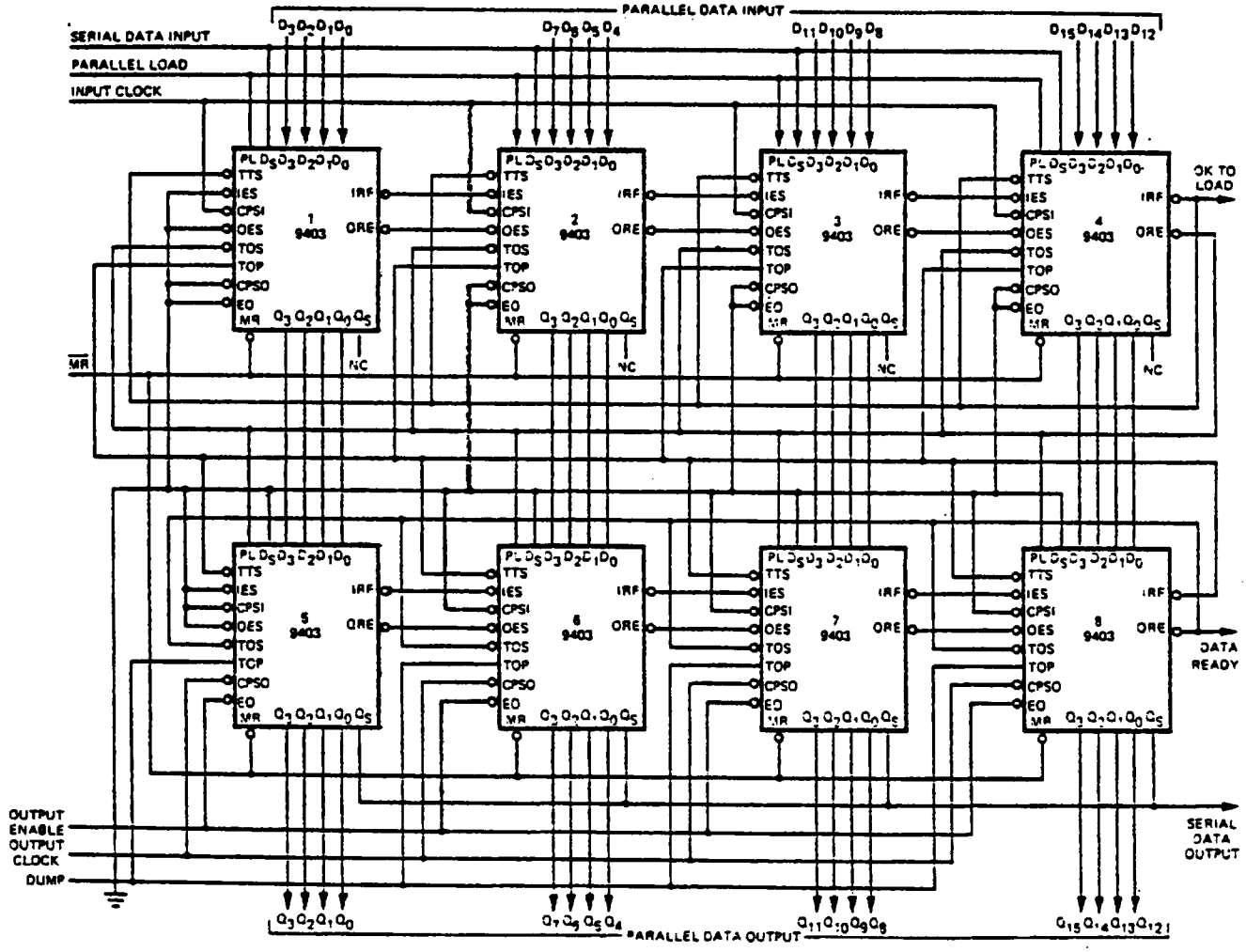


Fig. 6
A 31 X 16 FIFO ARRAY

Horizontal and Vertical Expansion – The 9403 can be expanded in both the horizontal and vertical direction without any external parts and without sacrificing any of the FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of $15n_1 + 1$ words by $4 \times n_2$ bits can be constructed.

Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

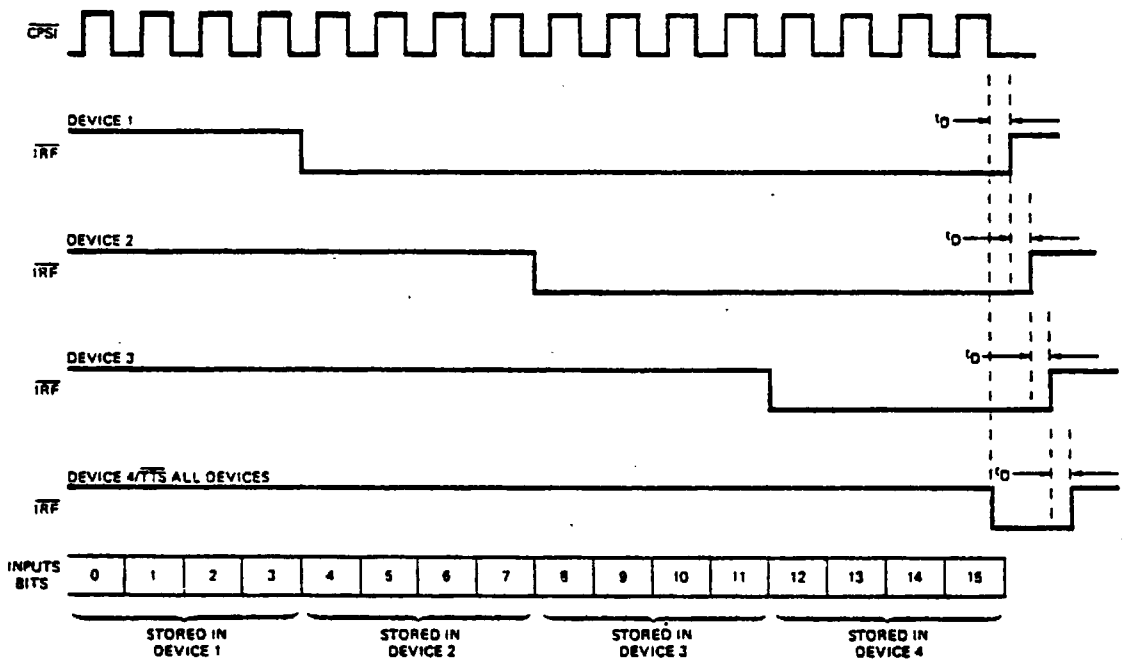


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

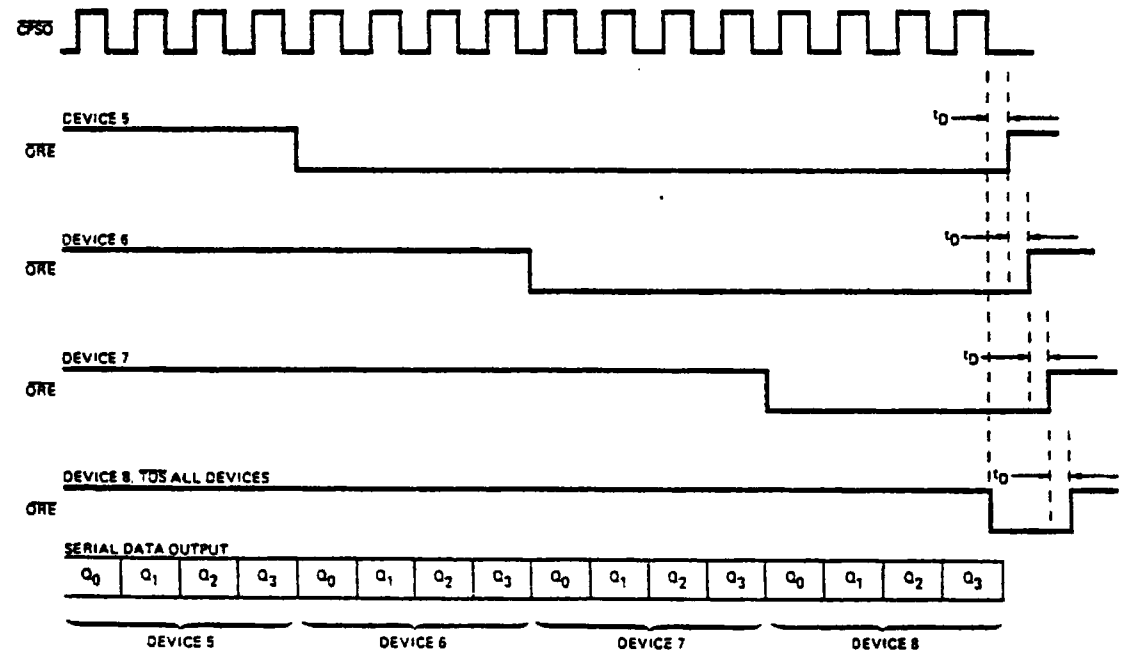


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

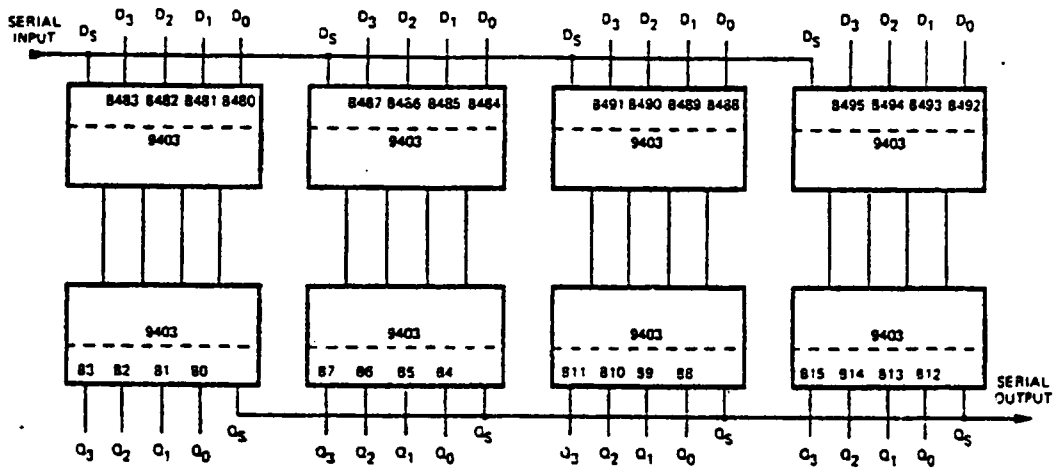


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

INTERLOCKING CIRCUITRY:

Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of Figure 6 devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ input has gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. Figure 10 is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the master latch is set. Whenever $\overline{TTS}$ goes LOW the request initialization flip-flop will be set. If the master latch is HIGH, the input register will be immediately initialized and the request initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ request flip-flop. If the master latch is set, the last Output Register flip-flop is set and $\overline{ORE}$ goes HIGH. If the master latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

TABLE 1

OUTPUT CONDITION	INTERNAL STATE	
	Master Operation – IES LOW when Initialized	Slave Operation – IES HIGH when Initialized
IRF LOW	Input Register Full	Input Register Full and IES LOW
ORE LOW	Output Register not Full	Output Register not Full and OES LOW

Table 1 summarizes master/slave status outputs.

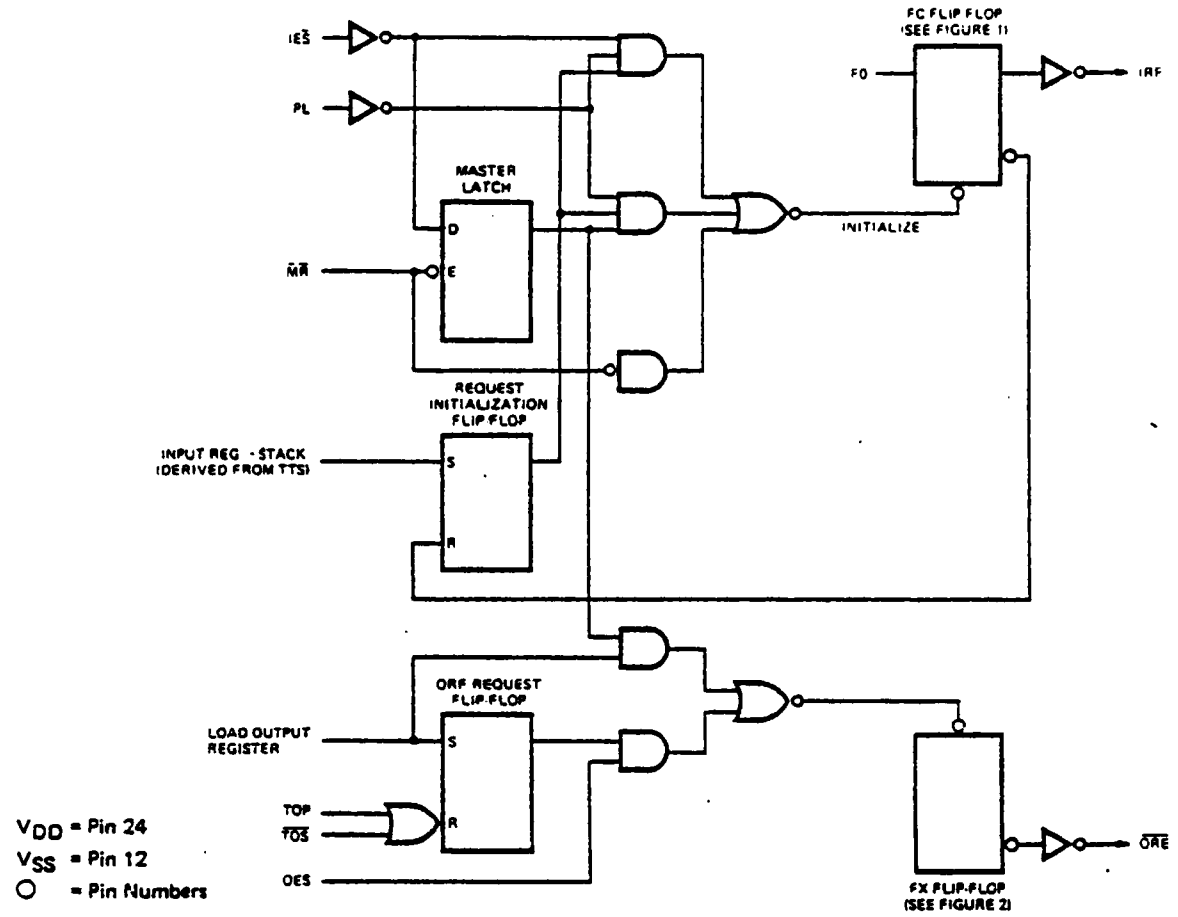


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage Q_S, QRE, OES	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA	
		XC	2.4	3.4				
V_{OH}	Output HIGH Voltage, Q_0–Q_3	XM	2.4	3.4		V	I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA	
V_{OL}	Output LOW Voltage, Q_0–Q_3, Q_S			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA	
				0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{OL}	Output LOW Voltage, ORE, OES			0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN
				0.35	0.5		I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH, Q_0–Q_3, Q_S				100	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V	
I_{OZL}	Output Off Current LOW, Q_0–Q_3, Q_S				−100	µA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V	
I_{IH}	Input HIGH Current			1.0	40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current, all except OES				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	OES				−0.86			
IOS	Output Short Circuit Current, ORE, OES		−10		−42	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{OS}	Output Short Circuit Current, Q_0–Q_3, Q_S		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0, (Note 3)	
I_{CC}	Supply Current			105	160	mA	V_{CC} = MAX, Inputs Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PWH}	$\overline{CPSI}$ Pulse Width (HIGH)		25		ns	Stack not full, PL LOW, Figures 11 & 12
t_{PWL}	$\overline{CPSI}$ Pulse Width (LOW)		12		ns	
t_{PWH}	PL Pulse Width (HIGH)		15		ns	Stack not full, Figures 17 & 18
t_{PWL}	$\overline{TTS}$ Pulse Width (LOW) Serial or Parallel Mode		6.0		ns	Stack not full, Figures 11, 12, 17, 18
t_{PWL}	$\overline{MR}$ Pulse Width (LOW)		15		ns	Figure 16
t_{PWH}	TOP Pulse Width (HIGH)		17		ns	$\overline{CPSO}$ LOW, Data available in stack,
t_{PWL}	TOP Pulse Width (LOW)		25		ns	Figure 15
t_{PWH}	$\overline{CPSO}$ Pulse Width (HIGH)		16		ns	TOP HIGH, Data in stack, Figures 13 & 14
t_{PWL}	$\overline{CPSO}$ Pulse Width (LOW)		20		ns	
t_s	Set-Up Time D_S to Negative $\overline{CPSI}$		20		ns	PL LOW, Figures 11 & 12
t_s	Set-Up Time, $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode		0		ns	Figures 11, 12, 17, 18
t_s	Set-Up Time Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$		0		ns	TOP HIGH, Figures 13 & 14
t_{rec}	Recovery Time $\overline{MR}$ to any Input		5.0		ns	Figure 16

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output		18		ns	Stack not full, PL LOW, Figures 11 & 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$		50		ns	
t_{PLH}	Propagation Delay, Negative-Going $\overline{CPSO}$		30		ns	Serial Output $\overline{OES}$ LOW, TOP HIGH,
t_{PHL}	to Q_S Output		20			Figures 13 & 14
t_{PLH}	Propagation Delay, Positive-Going TOP		42		ns	$\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PHL}	to Outputs $Q_0 - Q_3$		32			
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$		35		ns	Serial Output $\overline{OES}$ LOW, TOP HIGH,
t_{PLH}	Propagation Delay, Positive-Going $\overline{TOS}$ to $\overline{ORE}$					Figures 13 & 14
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$				ns	Parallel Output, $\overline{EO}$, $\overline{CPSO}$ LOW,
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$		45			Figure 15
t_{ft}	Fall Through Time		450		ns	$\overline{TTS}$ connected to $\overline{IRF}$ TOS connected to $\overline{ORE}$ $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH, Figure 16
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$		48		ns	Data in stack, TOP HIGH, Figures 13 & 14
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going IRF		35		ns	Stack not full, Figures 17 & 18

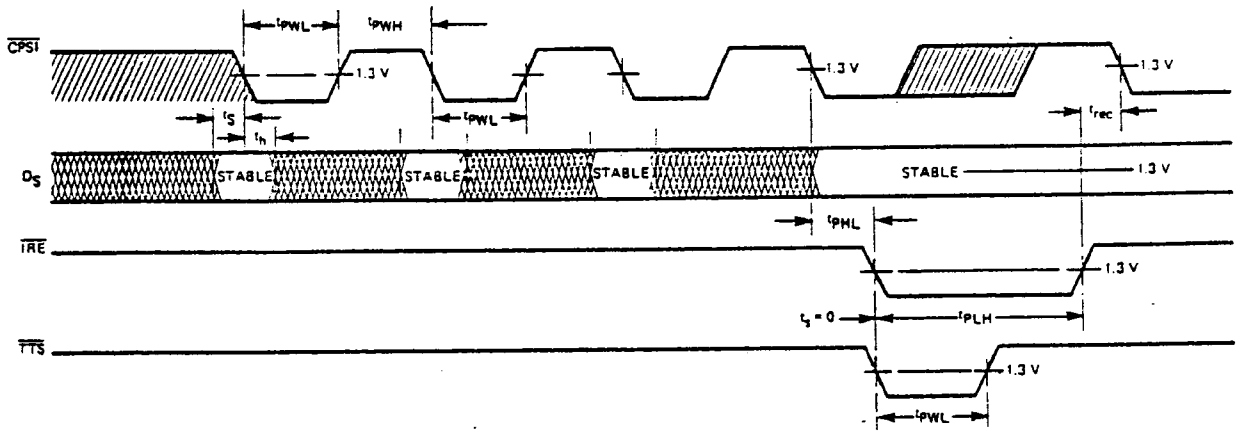


Fig. 11
SERIAL INPUT, UNEXPANDED OR MASTER OPERATION
Conditions: Stack not full, $\overline{IES}$, PL LOW

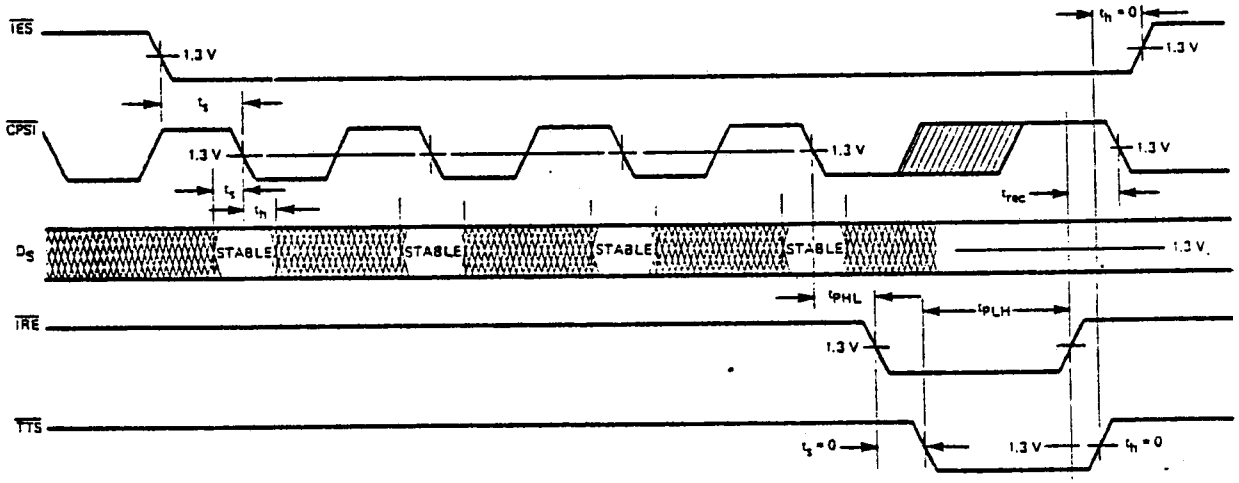


Fig. 12
SERIAL INPUT, EXPANDED SLAVE OPERATION
Conditions: Stack not full, $\overline{IES}$ HIGH when initialized, PL LOW

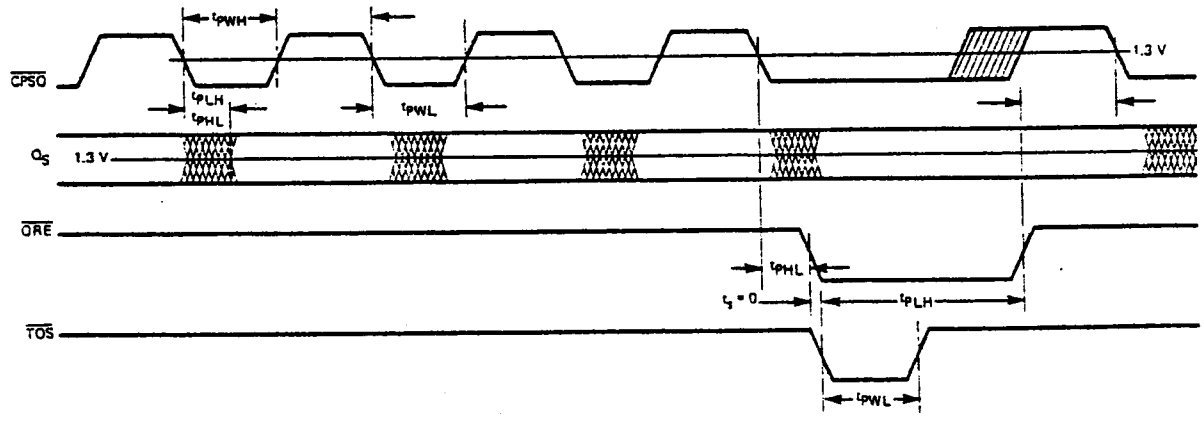


Fig. 13
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION
Conditions: Data in stack, TOP HIGH, $\overline{IES}$ LOW when initialized, $\overline{OES}$ LOW

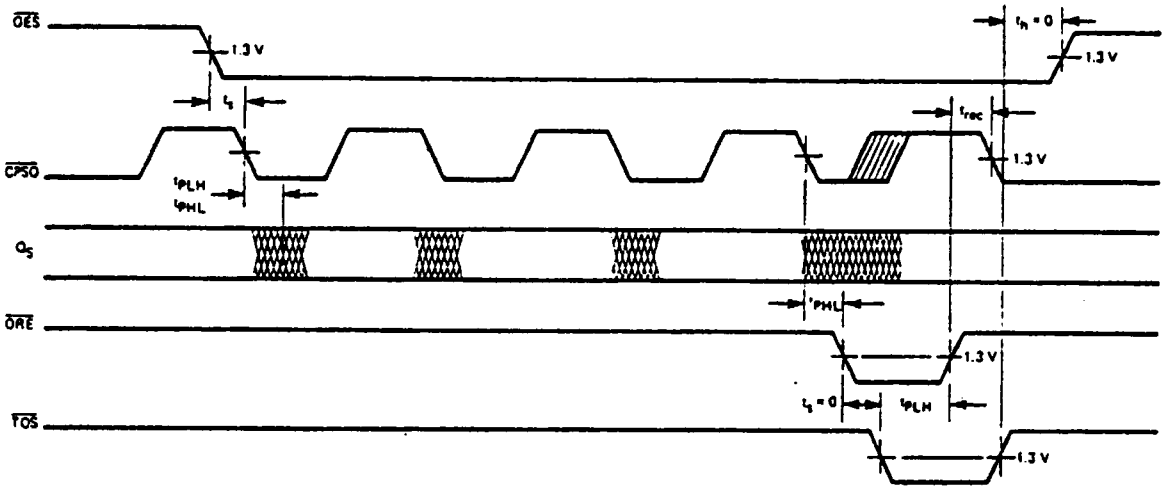


Fig. 14
SERIAL OUTPUT, SLAVE OPERATION
Conditions: Data in stack, TOP HIGH, $\overline{IES}$ HIGH when initialized

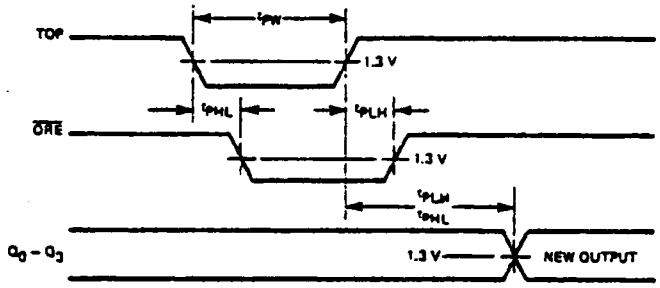


Fig. 15
PARALLEL OUTPUT, 4-BIT WORD OR MASTER IN PARALLEL EXPANSION
Conditions: $\overline{IES}$ LOW when initialized, $\overline{EO}$, $\overline{CPSO}$ LOW. Data available in stack

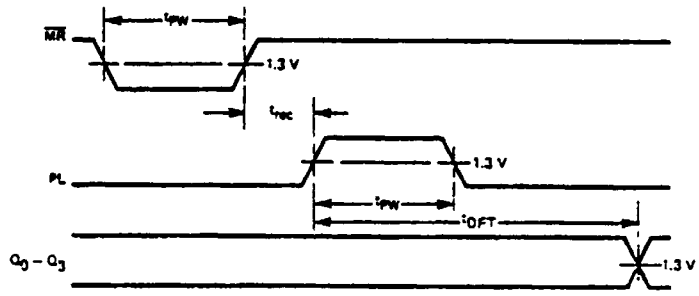
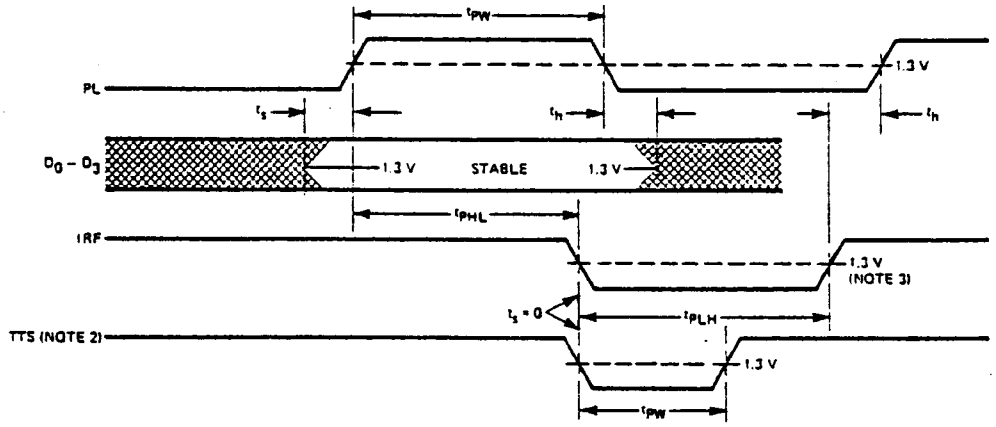


Fig. 16
FALL THROUGH TIME
Conditions: $\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH



NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, IRE will stay LOW.

Fig. 17
PARALLEL LOAD MODE, 4-BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION

Conditions: Stack not full, $\overline{IES}$ LOW when initialized

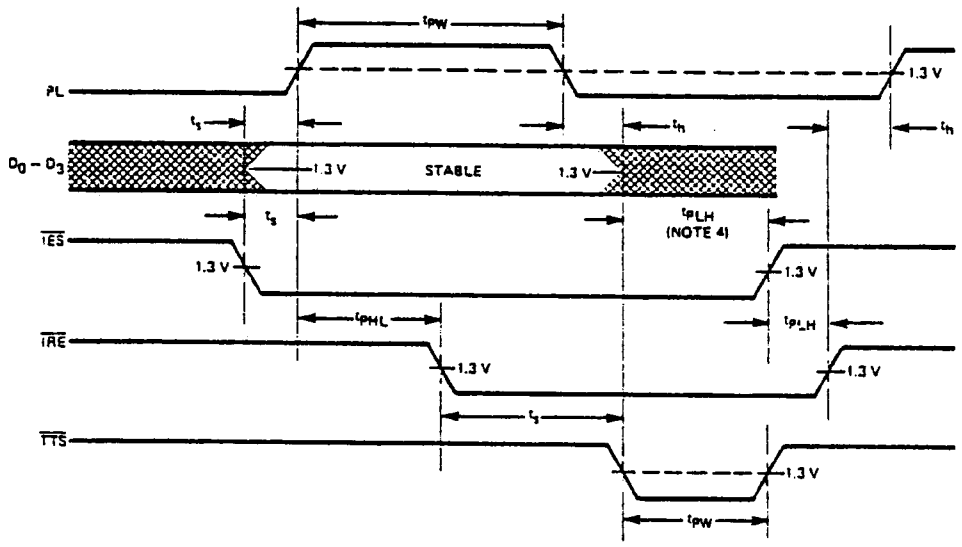


Fig. 18
PARALLEL LOAD, SLAVE MODE

Conditions: Stack not full, device initialized (Note 1) with $\overline{IES}$ HIGH

4-4. 88-HDSK BLOCK DIAGRAM

As shown in Figure 4-1, System Block Diagram, the controller consists of three major circuit functions, each having its own circuit board. Communications between these three boards take place on a common I/O Bus at a 4 MHz rate.

The Processor Card receives commands from the Altair computer and executes them as required by the Read Only Memory (ROM) Program Storage. There are two fundamental types of commands; data transfers, and control of Disk Drive operation.

Data transfers between the Altair computer and the Controller are performed through the 1K RAM Working Storage Memory, while data transfers between the Datakeeper Controller and the Drive go through the Disk Data Card and the 1K RAM Working Storage Memory.

Control of the Disk Drive is handled between the Processor and the Disk Interface Card.

For a detailed system block diagram, refer to Figure 4-2 which describes the function of each card.

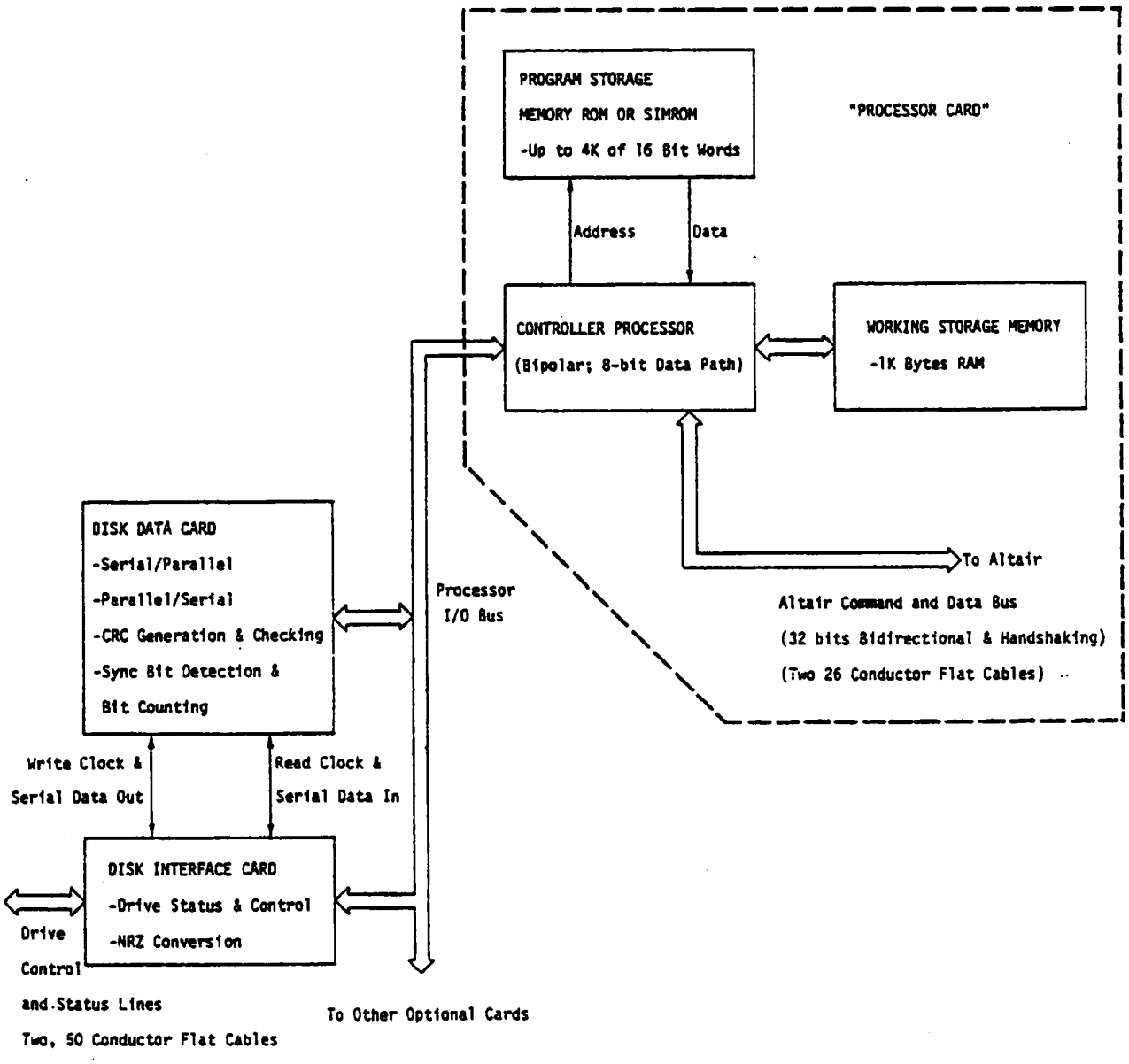


Figure 4-1. System Block Diagram

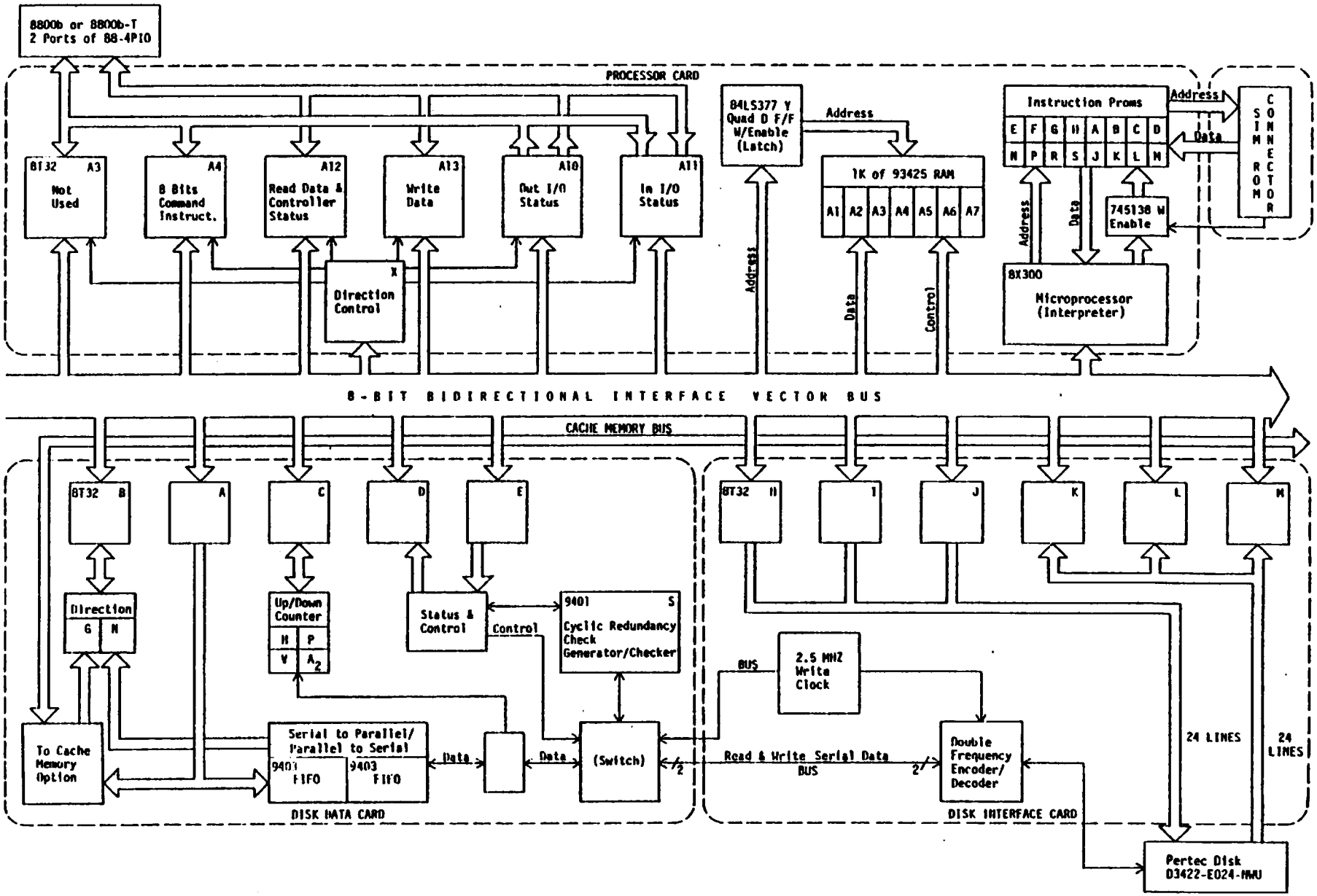


Figure 4-2. 88-HDSK Detailed Block Diagram

4-5. PROCESSOR CARD

A. 8X300 PROCESSOR COMMUNICATION LINES (Figure 4-9)

The Hard Disk Processor Card utilizes the 8X300 processor (refer to Figure 4-3 for Block Diagram). This 8-bit bipolar I/O oriented processor has three buses for communication with the real world. The first of these is the ROM Memory Address bus. This is a 13-bit address path; output from the processor only. Second, is the 16-bit instruction data bus used as input to the processor. All program instructions are transferred from the PROM to the processor on this bus. Third, is the Interface Vector (IV) bus and its associated control lines. This bus system is present on the Motherboard in the Controller and is used for communication with all of the other Cards. The IV bus contains 8-bits of bi-directional multiplexed data which address the I/O interface ICs and transfers data to and from the I/O interface ICs. The five control lines are Write Control (WC), Select Control (SC), Master Clock (MCLK) and Left and Right Bank Select ($\overline{LB}$ and $\overline{RB}$). When HIGH, the SC and WC signals are used to distinguish between I/O data and I/O address information. MCLK provides synchronization for external logic and/or clocking for I/O devices, and $\overline{LB}$ and $\overline{RB}$ enable one of two sets of I/O devices when LOW. In all discussions of the processor data paths, bit Ø is always the most significant bit.

Referring to Figure 4-9, Sheet 1, Zone B4 note that the least significant 9 instruction address bits are brought out directly to each of the 16 ROM locations on the Processor Card. The upper four bits of the 13 bit instruction address path (A0-A3) are decoded by a three to eight decoder, IC W (Zone B3) to select one of the eight 512 x 16 bit ROM memory banks. The instruction address bus allows for a total of 8K words of instructions; however, this Processor Card provides for 4K words.

An additional connector is provided for on the Processor Card for connecting to external banks of RAM or ROM. Each of the lines on the instruction address bus and the instruction data bus are tied to this connector. The ROM ENABLE line (Zone B1) disables all ROM on the Processor Card when connected to logic Ø. This feature is used by the simulated ROM memory in order to provide an easily modifiable substitute for system PROM when developing firmware for the Controller.

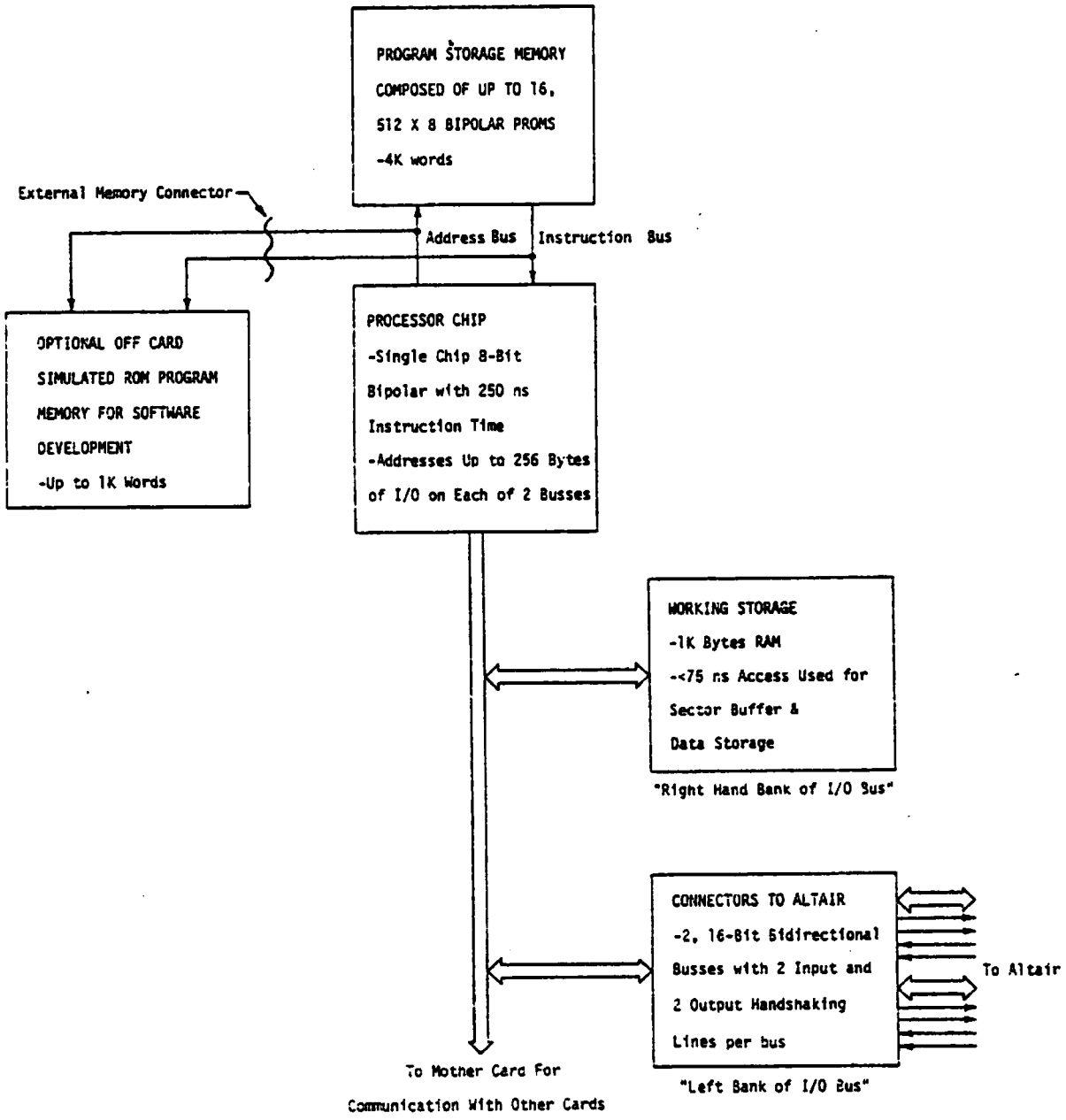


Figure 4-3. Processor Card Block Diagram

B. COMPUTER INTERFACE (Figure 4-9)

The I/O Interface to the Altair computer consists of two 16 bit data paths (PA0-PA7 through PB0-PB7) with their associated controls (Sheet 2, Zone D1 through D8). I/O chips A8 through A13 used in this interface are 8T32 Interface Vector bytes or IV bytes (Zone D1 through D8). Each of these chips is an 8 bit bi-directional latching data path which can be read and written both by the processor and the Altair computer. The I/O (Input or Output) direction of these six IV bytes used to interface to the computer is controlled by the Datakeeper Controller Processor using a seventh IV byte, IC X (Zone C6). There are two steering lines on each IV byte, $\overline{BOC}$ pin 9 and $\overline{BIC}$ pin 10. If IC A8 pin 10 is LOW and pin 9 is HIGH, then IC A8 is an input to the Controller. If pin 9 is LOW and pin 10 is HIGH, then IC A8 is an output from the Controller. IV bytes A8, A9, A12 and A13 are connected to Ports 161, 163, 165 and 167, respectively, on the Altair 4PIO Interface by connector P1. IV bytes A10 and A11 are used as Status and Control flags for communication between the Controller and the Altair computer.

In normal system use, the processor uses IV byte X to set up IV bytes A8, A10 and A12 as outputs from the Controller to the Altair and IV bytes A9, A11 and A13 as inputs to the Controller from the Altair computer. This corresponds to the normal Altair 4PIO setup of section A as input; section B as output.

To select an IV Byte IC to Input or Output the IV Byte address is placed on the IV Data Bus, and the SC line is clocked. Each IV Byte IC is permanently programmed with a unique address (0-255) specified by its circuit function and determined by the firmware. When the programmed address matches the clocked address, the IV Byte is enabled until a different I/O address is clocked on the Bus.

4-6. DISK DATA CARD (Figure 4-10)

The Disk Data Card is broken into five major sections (Figure 4-4). The first section includes logic for parallel to serial/serial to parallel conversion, FIFO (First In, First Out) buffering and parallel byte data source selection. The second section consists of the main control logic for bit counting, Read/Write mode control, CRC write control and end of transfer control. CRC generation and checking is contained in the third section. The fourth section consists of serial write data source selection and the fifth section contains read/sync bit detection.

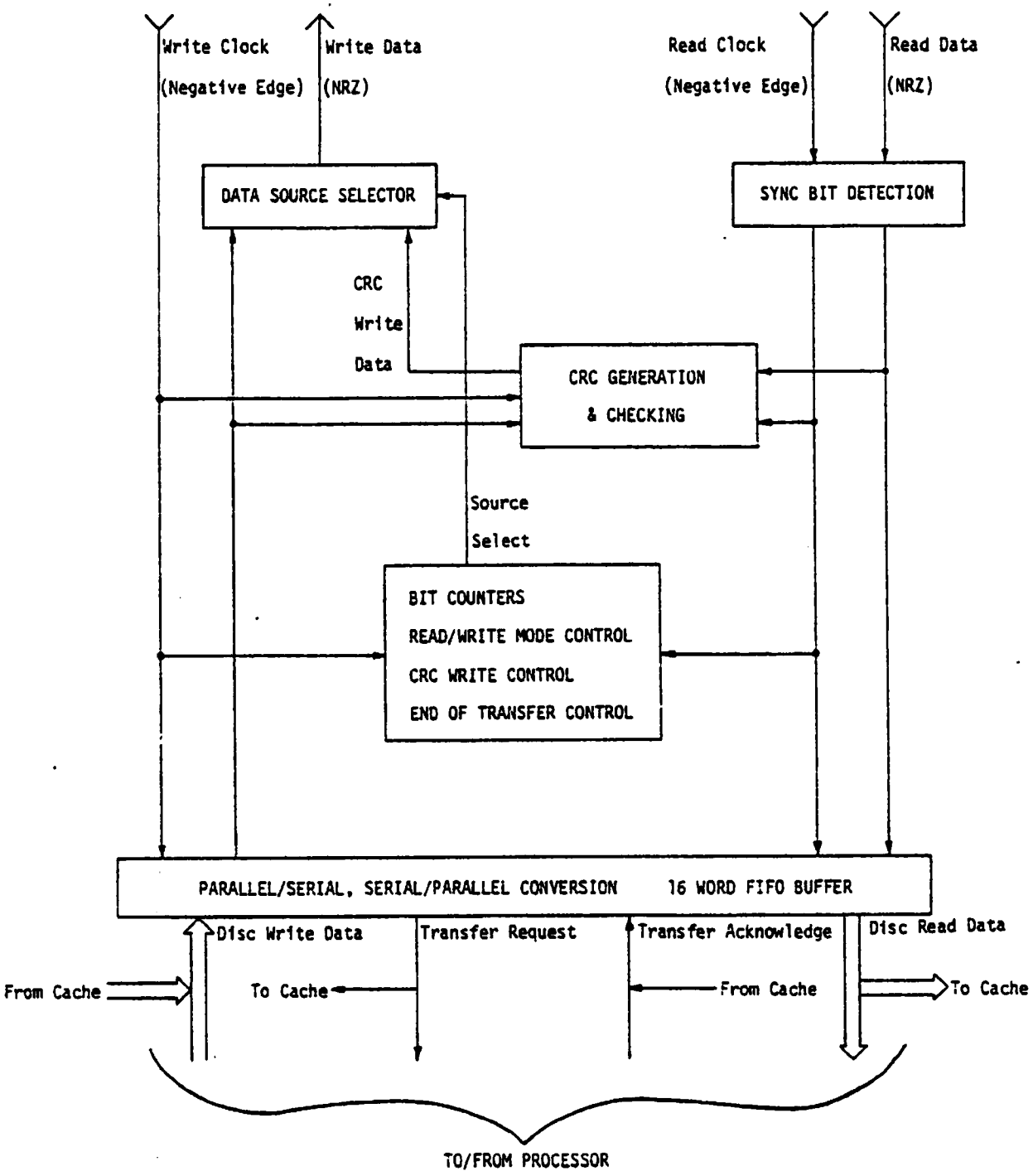


Figure 4-4. Disk Data Card Block Diagram

A. CONTROL AND INTERFACE (Figure 4-10)

Five IV bytes (A through E) are provided for control and interface with the various sections of logic. IV byte A (Figure 4-10, Zone D6) provides a transfer path for the Read Data to the processor when operating in the Disk Read mode. When operating in a Disk Write mode, IV byte B (Zone D7) provides a transfer path for data from the processor to the Disk. IV byte C (Zone D4) loads the 16-bit counter which counts the number of bits that are read or written. IV byte D (Zone D3) transfers status back to the processor, and IV byte E (Zone D2) controls the logic functions on the Disk Data Card. Bit 7 of IV byte E ($\overline{\text{SDSEL}}$) is the source selector for parallel Read and Write Data. Two possible sources to the processor are IV bytes A and B or Cache Memory (optional, not used in this system). Bit 6 (TRAS) is used as an acknowledge strobe to the logic on the card, indicating that a byte of data has been read or is available to be written from the processor. Bit 5 ($\overline{\text{CLR}}$) is the master reset or clear flag for this card. Bit 2 (DISRMD) selects whether the card will operate in the Read mode or Write mode. Bit 1 (DISTRAN STRT) initiates the actual transfer of data to or from the Disk. When operating in the Write mode, bit 0 (CRCAPE) indicates whether or not to append the CRC check word to the data being written. Three status bits are used in IV byte D. Bit 7 (TRR) when HIGH, indicates that the FIFO's in the parallel to serial/serial to parallel conversion section are ready to receive more data or have data ready for transmission. Bit 6 (DTRCMP) is used by the control logic to indicate when the Disk transfer is complete. Bit 5 (DRDST) can be tested after the completion of a read operation to indicate whether or not the CRC checking detected an error.

B. PARALLEL TO SERIAL/SERIAL TO PARALLEL CONVERSION (Figure 4-10)

The serial to parallel/parallel to serial and FIFO buffering logic consists of ICs F, M, G, N, U, portions of IC W, R, A3 and A1, as well as IV bytes A, B and portions of D and E. ICs G, N and U (Zone C7) are four bit data selectors that select the parallel write data source. There are two possible sources for this data. The first is directly from the processor through IV byte B, and the second is from the Cache Memory Card (optional, not used in this system) through pins 41 through 48 on the Motherboard (Zone C8). IC U (Zone C6) selects the source of the transfer acknowledge flag. If the data is being transferred to and from the Cache Memory, the transfer acknowledge flag from the Cache Memory is used; otherwise, the transfer acknowledge flag originating on bit 6 of IV byte E (Zone D2) is used to strobe

data in or out of the First-In, First-Out Buffers (FIFO), ICs F and M (Zones A6 and A7). The sixteen byte First-In, First-Out Buffers also act as Parallel to Serial/Serial to Parallel converters.

Two flags provided from the FIFO section of IC F and M are Not Input Register Full ($\overline{IRF}$) and Not Output Register Empty ($\overline{ORE}$). These flags are gated through portions of ICs A3 and A1 (Zone A5) to provide a transfer request flag when false. This transfer request flag is sent to IV byte D bit 7 ($\overline{TRR}$) and to Cache Memory over bus connector pin 49 (Zone C8) if the card is operating with Cache Memory as the source. When operating in the Write mode, the $\overline{IRF}$ lines go False (HIGH) if the FIFO's require additional data. This signal is gated through ICs A3 and A1 (Zone A5), initiating a strobe onto the transfer request line (Zone D4). When operating in the Disk Read mode and the FIFO has data available for the processor or Cache Memory, the $\overline{ORE}$ flag goes False (HIGH). This is again gated through A3 and A1 (Zone A5), strobing the transfer request line. TRAS (Transfer Acknowledge Strobe) from IV byte E, bit 6 (Zone D2), or Transfer Acknowledge Cache at bus pin 50 (Zone C8) is selected by IC U (Zone C6) and passed through ICs W and R (Zone B6). This provides proper strobing of the byte into or out of the FIFO's, resetting the $\overline{IRF}$ or the $\overline{ORE}$ flags.

When operating in the Disk Write mode, ICs F and M shift the parallel Write Data out serially on the Q_S line (pin 22) upon being strobed by the Write Clock at CPSO. For a Read mode operation, F and M accept data on the DS line (pin 7) when strobed at $\overline{CPSI}$ (Zone A6), accumulating 8-bit bytes and passing them through to the FIFO sections.

C. BIT COUNTERS (Figure 4-10)

Bit counters count the number of bits that will be read or written. The 4-bit binary counters consist of ICs H, P, V and A2 (Zone C5 and B5). These counters, along with the associated logic in ICs J and R for rippling counts through the four bit counters, are used to produce a transfer complete signal at the end of a Read or Write Data Transmission. This is generated by the ripple carry out of the most significant bit in the chain with the counters operating in a count down to zero mode. IV byte C (Zone D4 and D5) is used for loading the initial value into the bit counters. This initial value is the number of bits that are to be read or written into the transmission. Bits 7 through 4 of IV byte C are the four bit data values to be loaded into one of the counters. Bit 3 is used as a load strobe for the next four bits (IC P, Zone C5). Bit 1 is used as a load strobe for the next

four bits (IC V, Zone B5) and bit 0 is used as a load strobe for the most significant four bits at IC A2 (Zone B5).

Portions of ICs T, L, A1, Y and R (Zones A2 and A3) are used in gating the Read and Write Clocks before and after the Read or Write Data transmission.

D. CRC GENERATION AND CHECKING (Figure 4-10)

The Cyclical Redundancy Check (CRC) generation and checking circuits are composed of IC S, K and a portion of A4 and Z. IC S (Zone C2) is a 16-bit CRC generator and checker that produces a 16-bit polynomial when in the Write mode and reads back and checks that 16-bit polynomial in the Read mode. IC K (Zone C1) is a 16-bit counter, and it in conjunction with flip-flop Z and A4 (Zone C3) clocks out the 16-bits of CRC that are appended to the check word.

The Write Data source selector consists of IC A5 (Zone B2) which selects the source of serial Write Data. The two possible sources are the data shifted out by the Parallel to Serial/Serial to Parallel Converters or data generated by the CRC generator.

E. SYNC BIT DETECTION (Figure 4-10)

The last section of the card is the read sync bit detection that consists of a portion of flip-flop A4 (Zone C4). It is used to detect the first valid logic one bit after the start of the transmission. This one bit is used to start and enable all the rest of the circuits of the card for the receipt of Read Data.

F. READ OPERATION (Figure 4-10)

To initiate a Read Data transmission the Datakeeper Controller processor must first set up the proper flags on IV byte E (Zone D2). The Disk Read mode (bit 2) is set for a logic 1, indicating that a read transmission is required. Bit 7, Source Selection, is set to logic 0 if the processor is to receive the Read Data, and logic 1 if Cache Memory is to receive the data. Bit 6, Transfer Acknowledge Strobe, and bit 1, Disk Transmission Start, is set to logic 0. Bit 0, CRC Append, may be set for either a logic 1 or logic 0 as it is not used during the Read transmission.

After setting these bits the processor sets bit 5, Master Clear, LOW and then back HIGH again. The processor then, sets up the data count that is to be loaded into the least significant level of data on IV byte C, bits 7 through 4 (Zone D4). The parallel load input of each of the four bit counters used in the 16-bit counter (ICs H, P, V and A2) is strobed LOW and

returned HIGH by the processor. After waiting until the proper sector has come under the read heads and at least half of the preamble has passed under the heads to insure valid data, the processor sets bit 1 of IV byte E (Disk Transmit Start) to a logic 1. This signal is then gated by IC Z (Zone B1) to assure that it coincides with the proper transision on the Write Clock.

After Disk Transmit Start has occurred in the Read mode, the Read Clock and Data is enabled to IC A4, the Sync Bit Detector. Upon detection of a valid logic 1 bit during the occurrence of a Read Clock, the Sync Bit Detector latches that condition and enables the Read Data and Read Clock to pass through the serial to parallel converters.

DISTRAN STRT enables clocking of the Read Clock signal into the serial to parallel converter and the Bit Counters, ICs H, P, V and A2. Data bits are assembled in the parallel to serial counters of ICs F and M, until a complete byte is assembled. At this time the $\overline{\text{ORE}}$ strobe goes False (HIGH), passes through IC A3 and A1, producing the transfer request flag on IV byte D. The processor, upon seeing transfer request True, reads the byte of data present on IV byte A and stores it into the buffer. It then strobes IV byte E pin 6, Transfer Acknowledge Strobe, TRAS, indicating that the byte of data from the FIFO's has been read. This process continues until all of the data that the processor wishes to transfer has been read. As each bit is clocked into the serial to parallel converter, the counter network is decremented by one and the serial Read Data and Clock are passed through IC X to IC S (Zone C2), the CRC checking logic. When IC X (Zone B3) is in the Read mode, it selects both the Read Clock and the Read Data for transfer to the CRC generating and checking circuit (see Table 4-B for operation of IC X). When the bit counters become zero, the ripple carry out ($\overline{\text{RC}}$, Zone B5) is passed through IC R (Zone B5) and IC X (Zone B3), to bit 6 of IC D (Zone D3). This indicates to the processor that the Disk transfer is complete. At this time the processor sets Disk Transfer Start (DISTRAN STRT), bit 1 of IV byte E to a logic 0 and reads bit 5 on IV byte D. This determines if a read error occurred during the reading of data indicated by a logic 1 at IC S pin 13. An error is indicated by the lack of a match within the CRC checking mechanism.

Table 4-B. IC X Pin 1 Data Selector Select Functions

Read Mode = Logic 1 (B inputs switched to Y outputs) Write Mode = Logic 0 (A inputs switched to Y outputs)	
Section	Function
1Y	Output CRC Clock Select
1A	Input Write Clock
1B	Input Read Clock
2Y	Output CRC Data Select
2A	Input Serial Write Data
2B	Input Serial Read Data
3Y	Output Bit Counter Clock Select
3A	Input Write Clock
3B	Input Read Clock
4Y	Output Disk Transfer Complete
4A	Input Write DTRCMP (Bit CTR = 0)
4B	Input Read DTRCMP (Bit CTR = 0)

G. WRITE DATA OPERATION (Figure 4-10)

The procedure for transmitting Write Data to the Disk is very similar to the Read Data Operation. IV byte E bit 2, Disk Read mode (DISRMD) is set to a logic 0, indicating a Write transmission is to occur, and bit 0, CRCAPE, is set for logic 1 to have the CRC check word appended to the Write Data. Otherwise, CRCAPE is set to a logic 0 and a CRC word is not appended to the Write Data. After setting up the bit counters in exactly the same manner as a Read mode, the processor waits until the proper sector is under the heads and enables the write circuitry in the Drive to write a preamble of 0s. The processor then clears the logic and sets bit 1 of IV byte E, Disk Transmit Start, to a logic 1. This is synchronized by IC Z (Zone B1) in conjunction with the Write Clock to provide a clean transition on the first bit. When Disk Transfer Start goes True, Write Clock is transferred into the parallel to serial converters, as well as through IC X into the CRC generating chip. The Write Data coming from the parallel to serial converters also passes through IC X to IC S in order to provide a basis for generating the CRC. As

data is serially shifted out of the parallel to serial converters, the FIFO portion of ICs F and M at $\overline{IRF}$ provides a transfer request (TRR) to bit 7 of IC D. The processor provides Write Data through IV byte D and produces the Transfer Acknowledge Strobe (TRAS) signal on bit 6 of IV byte E. Note that the first byte of data, the synchronization byte, must be written to the FIFO during the preamble before Disk Transmit Start is signaled. This provides a valid logic one bit of synchronization when reading. As bits are written to the Disk, the counter network is decremented once for each bit until it becomes 0. At this point, the ripple carry from the most significant bit signals the end of that portion of the transmission and the Write Clock and Write Data are disabled from the parallel to serial converter and the bit counter.

If a CRC check word is not to be appended to the data being written, Disk Transfer Complete (DTRCMP, Zone C3) goes True at bit 6 of IV byte D and the processor sets Disk Transmit Start, bit 1 of IV byte E, to a False condition; thus, the completion of the Write to Disk operation. If, however, the CRC check word is to be appended to the Write Data, the Ripple Carry ($\overline{RC}$, Zone B5) goes True at the counter network, and enables the CRC generating portion of IC S, and the 16-bit counter IC Z, K and A4. CRC data is gated through IC A5 to the Write Data line. As soon as all 16 bits of CRC check word are shifted out onto the Write Data line, the Disk Transfer Complete goes True on bit 6 of IC D, indicating the end of the transfer. The processor then sets bit 1 of IC E, Disk Transfer Start, to a logic 0, indicating the completion of the Write transfer.

4-7. INTERFACE CARD (Figure 4-11)

The functions of the Disk Interface Card include Disk Function Control, reporting of Disk Drive Status, transmission of serial Write Data and receipt of serial Read Data (Refer to Figure 4-5 for a Block Diagram of the Interface Card).

A. CONTROL OF DRIVE FUNCTIONS (Figure 4-11)

The three Interface Vector (IV) bytes H, I and J are used for control of Disk Drive functions. Bits 7 through 4 of IV byte H (Zone D7) are used for physical Disk Drive selection. Bits 3 through 1 are used for Read/Write head selection, and bit 0 is used to START/STOP all Drives on the daisy chain. IV byte J (Zone D5) is used to provide the lower eight bits of the cylinder address. Bit 7 of IV byte I (Zone D6) provides the ninth bit of

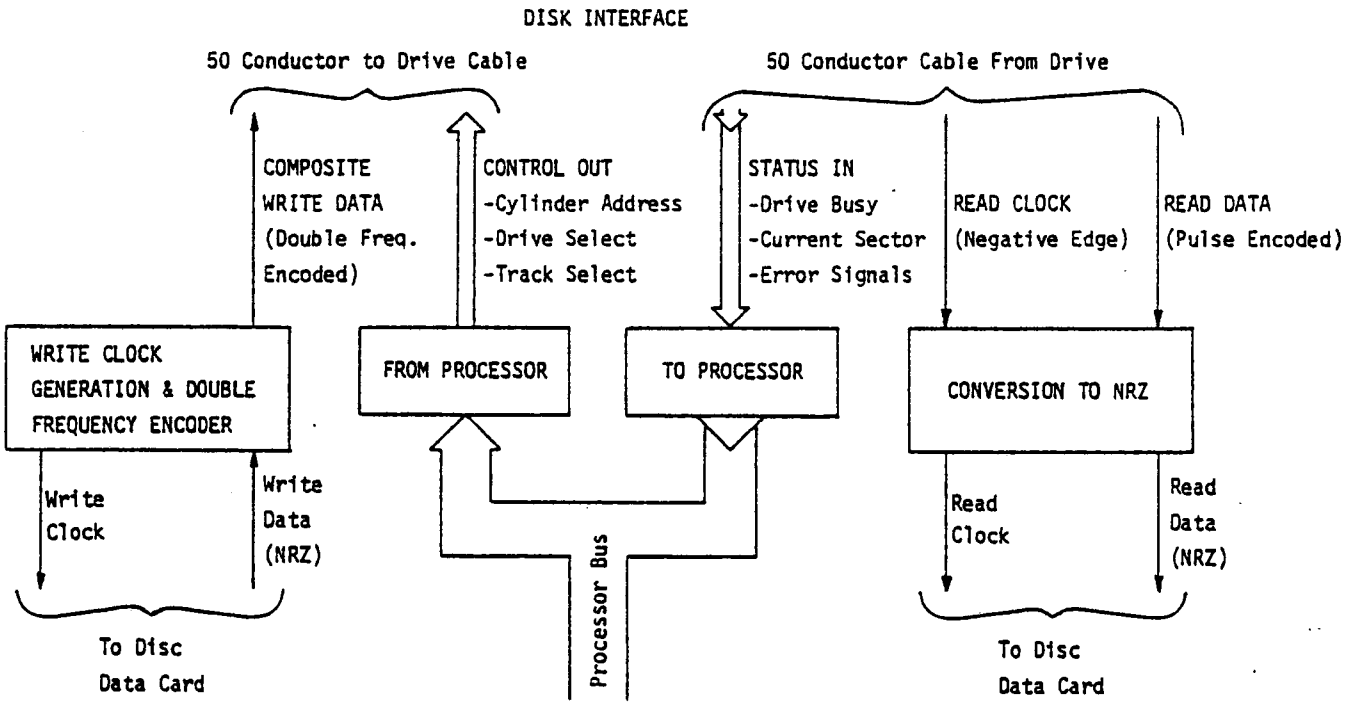


Figure 4-5. Interface Card Block Diagram

the cylinder address. Bit 5 of IV byte I is used as the Cylinder Strobe (CYL STROBE) line. When this line is brought LOW and then HIGH, the selected Disk Drive seeks the specified address. Bit 4 of IV byte I is the Cylinder Restore line (CYL RESTORE). When this line is LOW and the CYL STROBE is issued, the Drive will do a slow speed seek to cylinder Ø. Bit 3 (ENABLE WRITE) enables the Write Circuitry in the selected Disk Drive and bits 2 (OFFSET MINUS) and 1 (OFFSET PLUS) cause a slight offset in the head position from the current cylinder for attempting to recover more than marginally written data. Bit 0 is an emergency unload signal to all Disk Drives.

Each of the output lines from IV bytes H, I and J are buffered by line drivers before going to the termination resistors and then being transmitted to the Disk Drive. All signals to the Drives are active LOW.

B. REPORTING DISK DRIVE STATUS (Figure 4-11)

Disk Drive status is provided by ICs K (Zone D4), L (Zone D3), and M (Zone D1). Note that all output lines on IV byte H, I and J are active LOW, whereas all input lines on ICs K, L and M are active HIGH, and all lines to and from the Drive are active LOW. Bit 7 of IC K (DOUBLE TRACK) reports whether the Drive selected is 100 or 200 tracks per inch. Bit 5 (DUAL PLATTER) indicates whether the Drive has 1 or 2 platters, and bit 3 (EXTENSION STATUS) reports if the selected Drive is an extension Drive having a total of 4 platters. Bit 0 (MALFUNCTION) indicates that one of the Drives in the daisy chain has reported a malfunction. Bits 7 through 4 (BUSY SEEKING 1-4) of IV byte L report the seek status of any Drive. A HIGH on one of those four bits indicates that the corresponding Drive is in the process of seeking from one cylinder to the next. Bit 3 (ILLEGAL ADDR) indicates that the cylinder address given in the last seek to cylinder command is illegal for the currently selected Drive. If IC L bit 2 is HIGH, the head in the selected Drive is protected against writing. Bit 1 (INDEX PULSE) transfers the Index Pulses from the Drive. One pulse is recorded on this line for each revolution of the selected platter. Bit 0 is the READY line, indicating that the selected Drive is READY and no malfunctions have occurred. The Drive may be seeking when this line is True. Bits 7 through 1 of IC M record the sector count that is passing under the head on the Drive selected. The SECTOR PULSE (bit 0) indicates the beginning of a particular sector.

C. READ CLOCK AND READ DATA (Figure 4-11)

The Disk Interface Card transforms the Disk Drive Read Clock and Read Data into a form usable by the Disk Data Card. The Disk Drive data is in a double frequency encoded mode in which the Read Data pulses have been separ-

ated from the Read Clock pulses. There is one 125 nanosecond LOW going pulse on the Read Clock line every 400 nanoseconds. This defines the bit cell time during which data may occur. A logic 1 bit occurs when the Read Clock is HIGH and a LOW going pulse is on the Read Data line.

The two flip-flops of IC B, transform the data into a non-return to zero type format in which the Read Data is always valid on the falling edge of the Read Clock (Consult the timing specifications and waveform diagrams, Figure 4-6, for better understanding of how this transformation occurs).

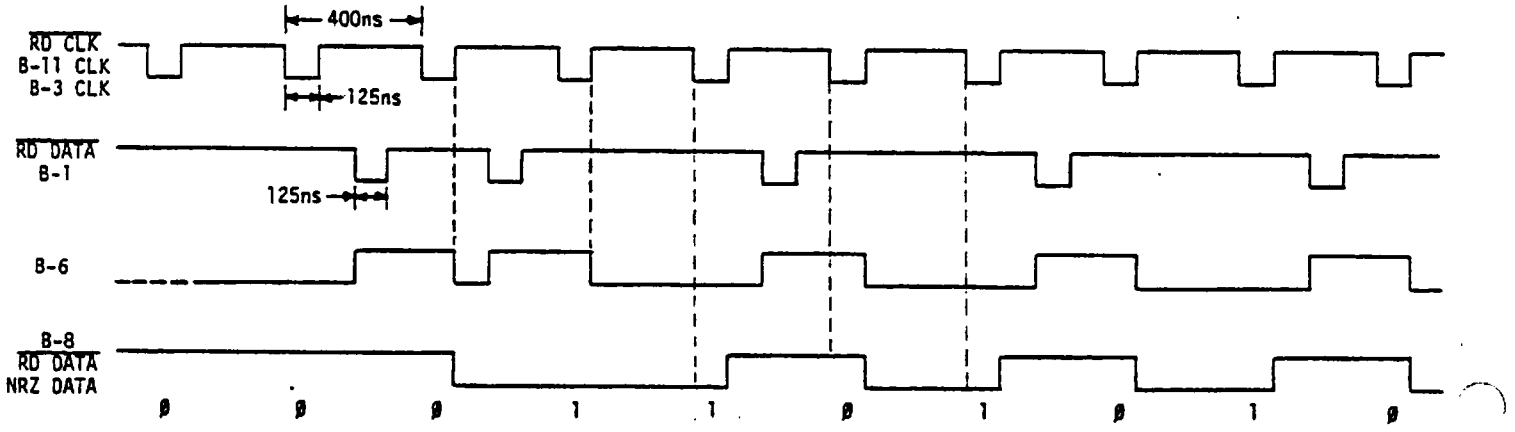


Figure 4-6. Read Data Timing

D. WRITE DATA TO COMPOSITE WRITE DATA (Figure 4-11)

Non-return to Zero Write Data coming from the Disk Data Card is transformed into double frequency encoded Composite Write Data and transferred to the Disk Drive. IC F produces a 10 Megahertz Clock signal which is divided by two stages of IC D to produce a 5 MHz Clock and a 2.5 MHz Clock signal. The 2.5 MHz Clock signal provides the Write Clock ($\overline{WR}$ $\overline{CLK}$) signal to the Disk Data Card. Data transitions from the Disk Data Card occur on the LOW going edge of the Write Clock. Write Data (WR DATA) coming from the Disk Data Card is latched into IC A on the positive going edge of the 2.5 MHz WR CLK at pin 3. Disk Transmit Start (DISTRA STRT), also from the Disk Data Card, holds that latched data in a LOW state until the processor initiates the data transfer. This writes a string of 0's in the beginning of a sector for a preamble. The three gates in IC C are used to encode the latched Write Data and the negative going Write Clock into a double frequency

Composite Write Data (see Figure 4-7). This is applied through line driver G and the termination resistors to the Disk Interface Cable (Consult the detailed timing and waveform diagrams for a better understanding of how this transformation occurs).

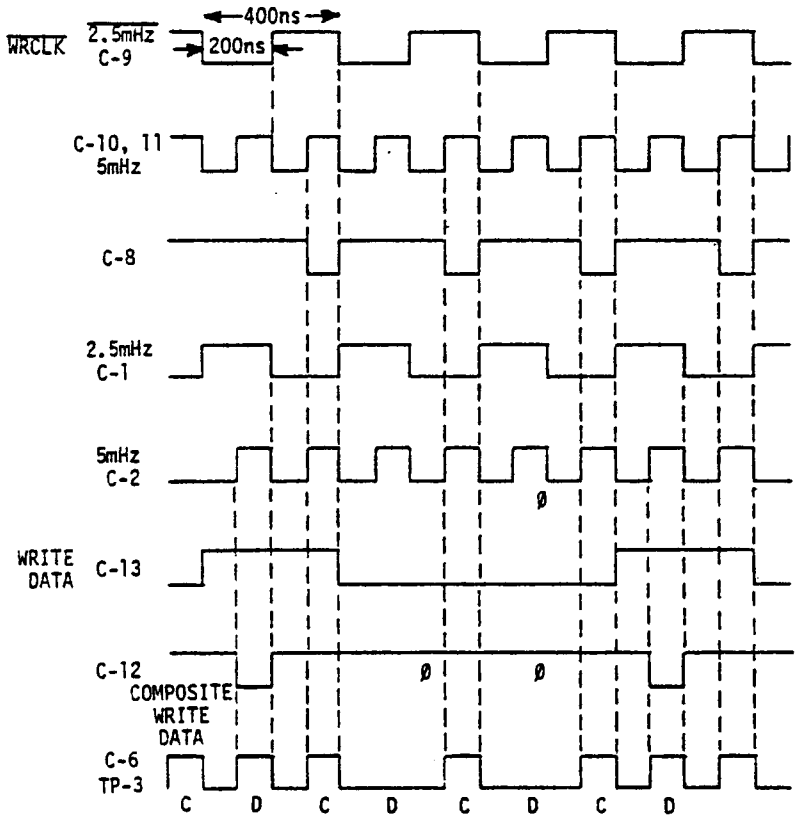


Figure 4-7. Composite Write Data Timing

E. TERMINATOR NETWORKS

Termination Voltage (Vcc EXT) comes from the Disk Drive and is normally 5 volts with the Drives on. A logic 1 on the signal lines (False condition) is approximately 3 volts, and a logic 0 (True) is typically 0.4 volts.

4-8. POWER SUPPLY OPERATION (Figure 4-8)

The 88-HDSK Datakeeper Power Supply input consists of a filtered AC line connected to a step down transformer. This powers the rectifier and a series pass regulator, providing 5 volts at up to 7 amps to the Motherboard. The line filter rejects the line/ground interference and incoming line-to-line noise. The line filter also prevents digital circuit switching noise from being conducted onto the power line. Transformer T1 (Zone C3) provides 10 volts at 8 amps rms through the bridge rectifier, BR1. The DC output of

BR1 is filtered by C4 (Zone B2), a 21,000 µf capacitor. Typical voltages across C4 are 13 volts no load and 10 volts with a 5 amp load. Resistors R8, R9, R10 and R11 (Zone C2) provide the voltage drop for over current sensing. Transistor Q3 is a series pass transistor. The emitter base junction is connected across R4 which provides the voltage drop for forward bias Q3. VR1 (Zone C1), a negative 5 volt regulator, is the reference for the Q3 series pass transistor. Transistor A1 is the shut off device during an over current sense operation. Q2 (Zone B2) is an SCR (Silicon Controlled Rectifier). Current through the .47 resistor network develops a voltage drop which is adjusted by R1 (Zone C2) to turn A2 on at a certain current level. When this predetermined voltage is reached, Q2 turns on, reverse biasing Q1 (Turning it off) which in turn shuts off the 5 volt regulated supply.

The positive side of the power supply is connected directly to the load. The series pass regulation takes place on the negative side of the unregulated voltage and the regulator acts as a variable resistance between the negative side of the unregulated voltage and DC chassis ground. Regulator action starts with VR1 conducting, causing a voltage drop across R4. As current increases through VR1 the voltage drop across R4 increases. With approximately 1 volt across R4, Q3 starts to turn on. As more current is required by the load, Q3 conducts more current since the current that was passing through R4 now passes through the emitter base junction of the darlington transistor Q3. The majority of the current now passes through Q3. VR1 passes only enough current to keep Q3 forward biased and conducting. As the load increases the current through VR1 increases only very slightly. Typically, with a 5 amp load VR1 passes only 100 ma and less than 1 ma flows out of the emitter base junction of Q3. Other typical voltages at a 5 amp load are approximately 2.3 volts between pins 3 and 2 of VR1, approximately .3 volts between the collector and emitter of Q1 and approximately 2 volts across R4. The .47 ohm resistor network has approximately .3 volts across it.

The over current sense potentiometer R1 is normally adjusted by varying the load on the Power Supply until 200 mv, 120 Hz ripples are observed. At this point R1 should be adjusted to turn Q2 on. Typically this is approximately 7 amps. Noise and ripple on the +5 volt line at a 5 amp load is typically less than 100 mv peak to peak. The three card system typically draws 4.25 amps. Once the over current circuit shuts off the 5 volt regulated supply, the only way the supply can be reset is to turn the key switch

to the off position and back on again. This opens switch S3, interrupting the anode-cathode current flow in Q2 causing it to shut off. This turns Q1 on again, allowing regulator action to begin.

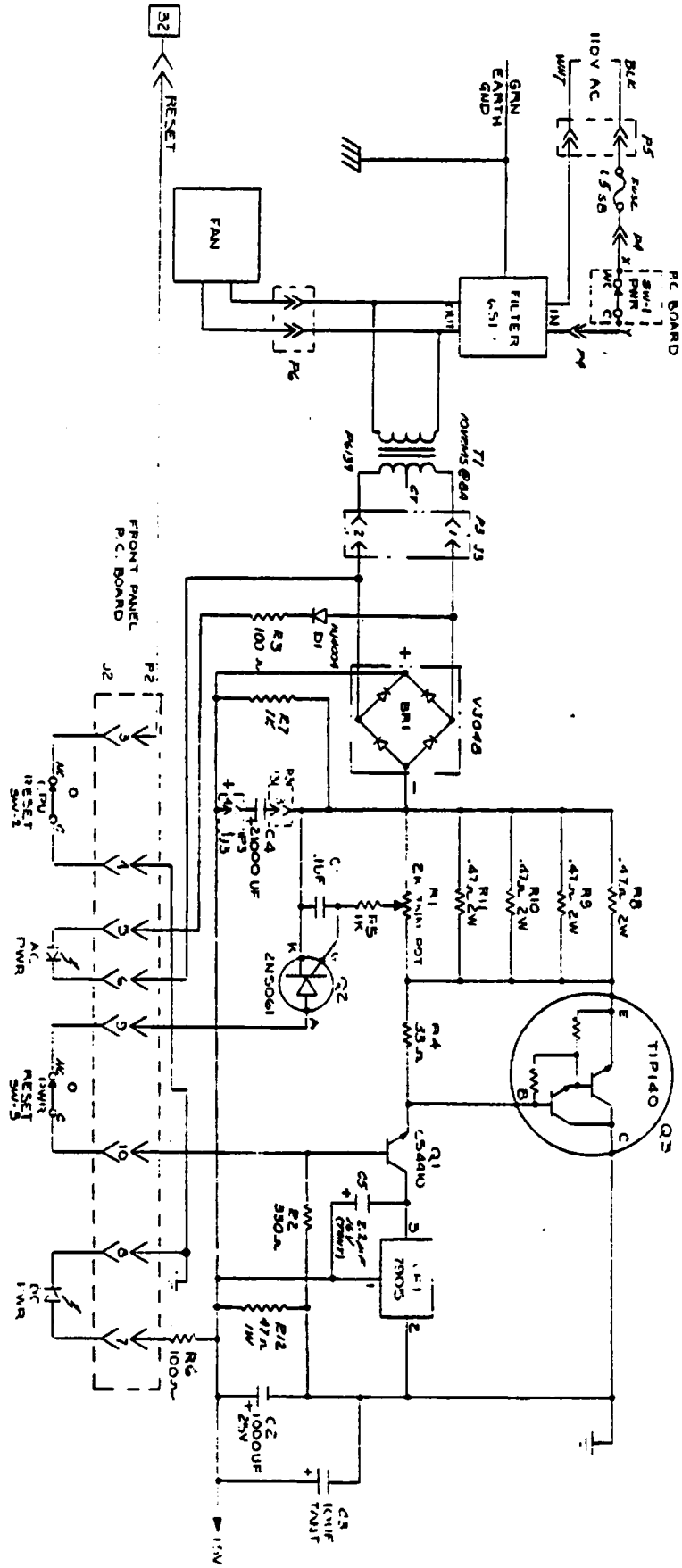


Figure 4-8. 88-HDSK Power Supply

4-9. HDSK BUS WIRING LIST

Bus Pin #	Signal
1	$\overline{IV0}$ (Interface Vector Bus)
2	$\overline{IV1}$ Bidirectional
3	$\overline{IV2}$ Data
4	$\overline{IV3}$ Bus
5	$\overline{IV4}$ To/From 8X300
6	$\overline{IV5}$ Processor & 8T32
7	$\overline{IV6}$ IV Bytes
8	$\overline{IV7}$
9	SC - 8X300 Select Command
10	WC - 8X300 Write Command
11	MCLK - 8X300 Master Clock
12	$\overline{LB}$ - 8X300 Left Bank I/O Select
13	$\overline{RB}$ - 8X300 Right Bank I/O Select
14	Not Used
15	Not Used
16	Not Used
17	RDCLK - Disk-Interface Read Clock
18	RDDATA - Disk Interface Read Data
19	WRCLK - Disk Write Clock
20	WRDATA - Disk Write Data
21	Not Used
22	Not Used
23	Not Used
24	Blank
25	+5V
26	+5V
27	Blank
28	Not Used
29	Not Used
30	Not Used
31	DISTRASTRT
32	Reset * Ext Wire

Bus Pin #	Signal	
33	CWØ	
34	CW1	
35	CW2	
36	CW3	
37	CW4	
38	CW5	
29	CW6	
40	CW7	
41	CRØ	RESERVED FOR OPTIONAL BOARDS
42	CR1	
43	CR2	
44	CR3	
45	CR4	
46	CR5	
47	CR6	
48	CR7	
49	TRRC	
50	TRAC	

51 through 73 GND

74-Blank

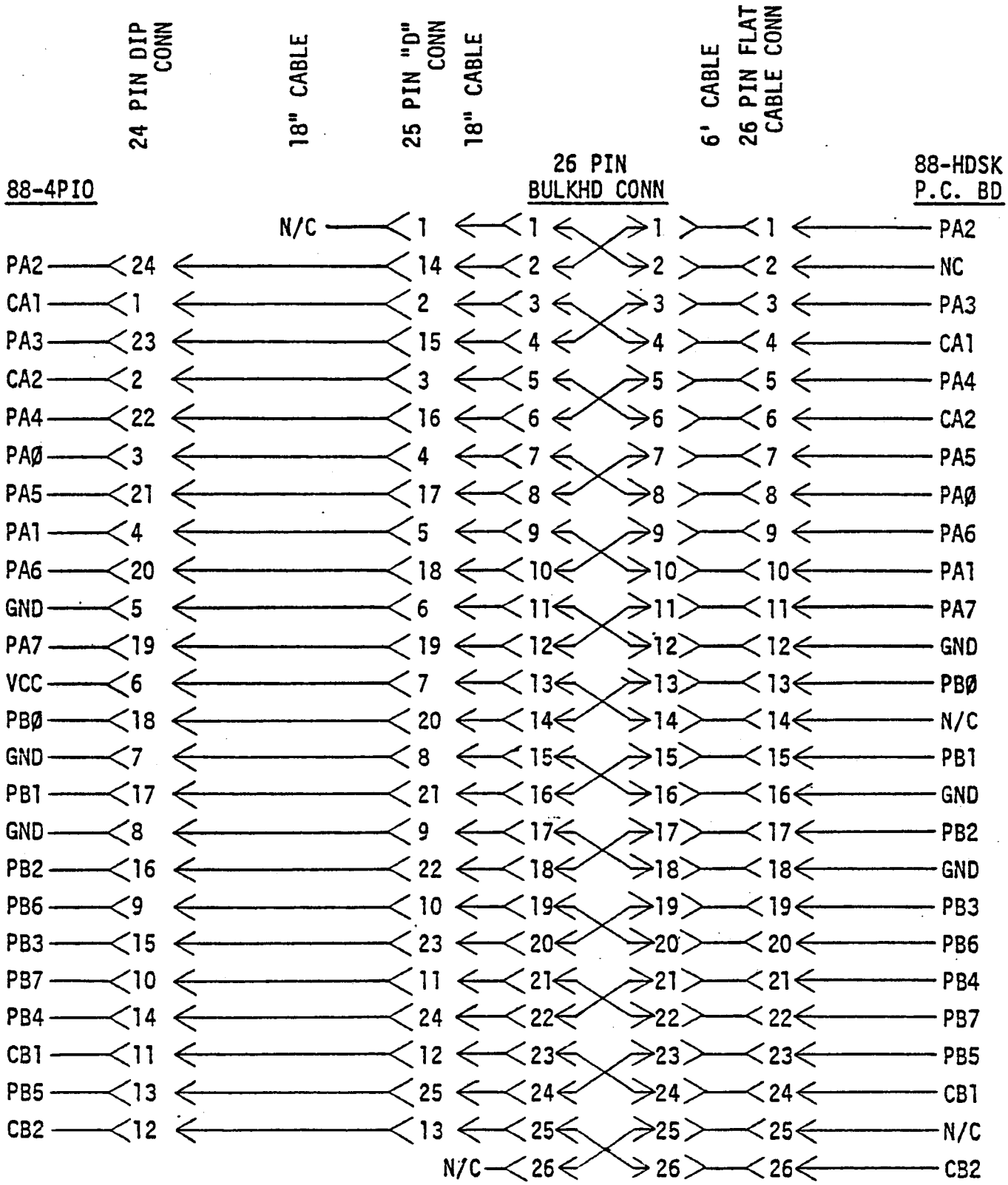
75 + 5V

76 + 5V

77-Blank

78 through 100 GND

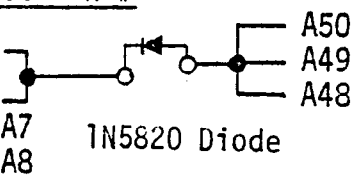
4-10. 88-HDSK-4PIO CABLE A + B WIRING LIST



4-11. 88-HDSK CABLE INTERFACE WIRING LIST

Signal Name	Connector/Pin #	Pertec Pin #
Select 1	1-1	B42
Return	1-2	B41
Select 2	1-3	A42
Return	1-4	A41
Select 3	1-5	B43
Return	1-6	B44
Select 4	1-7	A43
Return	1-8	A44
Head Select	1-9	A27
Return	1-10	A26
Platter Select	1-11	B27
Return	1-12	B26
Ext Sel	1-13	A30
Return	1-14	A23
Start-Stop	1-15	B30
Return	1-16	B29
Cyl Addr 8 (Ext)	1-17	A33
Return	1-18	A32
Cyl Strobe	1-19	B33
Return	1-20	B32
Cyl Restore	1-21	A31
Return	1-22	A32
Enable Write	1-23	B22--Jumper--A22 Enab
Return	1-24	B23--Jumper--A23 Eras
	1-25	Spare Pad
	1-26	B23
Offset Minus	1-27	A25
Return	1-28	A26
Offset Plus	1-29	B25
Return	1-30	B26
Emergency Unload	1-31	B31
Return	1-32	B32
Cyl Addr Ø	1-33	A39
Return	1-34	A38
Cyl Addr 1	1-35	B39
Return	1-36	B38
Cyl Addr 2	1-37	A37
Return	1-38	A38
Cyl Addr 3	1-39	B37
Return	1-40	B38
Cyl Addr 4	1-41	A36
Return	1-42	A35
Cyl Addr 5	1-43	B36
Return	1-44	B35
Cyl Addr 6	1-45	A34
Return	1-46	A35
Cyl Addr 7	1-47	B34
Return	1-48	B35
Write Data	1-49	A28
Return	1-50	A29
Read Enable		B24
Return	Jumper	B23

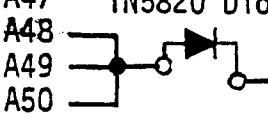
Signal Name	Connector/Pin #	Pertec Pin #
Termination Voltage (+5)	2-1	
Termination Voltage (+5)	2-2	
Double Track	2-3	A7
Return	2-4	A8
Dual Platter	2-5	B7
Return	2-6	B8
Ext Status	2-7	B18
Return	2-8	A2
Malfunction Det	2-9	B6
Return	2-10	B5
Busy Seeking 1	2-11	B19
Return	2-12	B20
Busy Seeking 2	2-13	A19
Return	2-14	A20
Busy Seeking 3	2-15	B21
Return	2-16	B20
Busy Seeking 4	2-17	A21
Return	2-18	A20
Illegal Addr	2-19	B3
Return	2-20	B2
File Protect	2-21	A1
Return	2-22	A2
Index Pulse	2-23	B4
Return	2-24	B5
	2-25	Spare Pad
Return	2-26	B5
Ready	2-27	B1
Return	2-28	B2
Sector Cnt Ø	2-29	A15
Return	2-30	A14
Sector Cnt 1	2-31	B15
Return	2-32	B14
Sector Cnt 2	2-33	A13
Return	2-34	A14
Sector Cnt 3	2-35	B13
Return	2-36	B14
Sector Cnt 4	2-37	A12
Return	2-38	A11
Sector Cnt 5	2-39	B12
Return	2-40	B11
Sector Cnt 6	2-41	A10
Return	2-42	A11
Sector Pulse	2-43	A4
Return	2-44	A5
Read Clock	2-45	B16
Return	2-46	B17
Read Data	2-47	A16
Return	2-48	A17
	2-49	Spare Pad
	2-50	A17



PERTEC DRIVE TO HARD DISK INTERFACE CARD

INTERCONNECTION CROSS REFERENCE

Pertec Pin #	Connector/Pin #	Signal Name
A1	2-21	(File Prot)
A2	2-22	(Return)
A3		
A4	2-43	(Sector Pulse)
A5	2-44	(Return)
A6		
A7	2-3	(Double Track)
A8	2-4	(Return)
A9		
A10	2-41	(Sector Cnt 6)
A11	2-42 + 38	(Return)
A12	2-37	(Sector Cnt 4)
A13	2-33	(Sector Cnt 2)
A14	2-34 + 30	(Return)
A15	2-31	(Sector Cnt Ø)
A16	2-47	(Read Data)
A17	2-48 + 50	(Return)
A18		
A19	2-31	(Busy Sk #2)
A20	2-4 + 18	(Return)
A21	2-17	(Busy Sk #4)
A22		(Erase Enable)--Jumper to B
A23		(Return)
A24		
A25	1-27	(Trk offs Minus)
A26	1-28 + 10	(Return)
A27	1-9	(Head Select)
A28	1-49	(Write Data)
A29	1-50	(Return)
A30	1-13	Exten. Select
A31	1-21	Restore Cyl
A32	1-22 + 18	(Return)
A33	1-17	(Cyl. Addr. 8)
A34	1-45	(Cyl. Addr. 6)
A35	1-46 + 42	(Return)
A36	1-41	(Cyl. Addr. 4)
A37	1-37	(Cyl. Addr. 2)
A38	1-38 + 34	(Return)
A39	1-33	(Cyl. Addr. Ø)
A40		
A41	1-4	(Return)
A42	1-3	(Unit Sel #2)
A43	1-7	(Unit Sel #4)
A44	1-8	(Return)
A45		
A46		
A47		
A48		
+5V A49	2-1	(Term Voltage)
A50	2-2	(Term Voltage)



PERTEC DRIVE TO HARD DISK INTERFACE CARD

INTERCONNECTION CROSS REFERENCE

Pertec Pin #	Connector/Pin #	Signal Name	
B1	2-27	(Ready)	
B2	2-28 + 20	(Return)	
B3	2-19	(Illegal Cyl Addr)	
B4	2-23 + 26	(Index Pulse)	
B5	2-24 + 10	(Return)	
B6	2-9	(Malfunction Det)	
B7	2-5	(Dual Platter)	
B8	2-6 + 8	(Return)	
B9			
B10			
B11	2-40	(Return)	
B12	2-39	(Sector Cnt 5)	
B13	2-35	(Sector Cnt 3)	
B14	2-36 +32	(Return)	
B15	2-31	(Sector Cnt 1)	
B16	2-45	(Read Clock)	
B17	2-46	(Return)	
B18	2-7	Exten. Status	
B19	2-11	(Busy Sk #1)	
B20	2-12 +16	(Return)	
B21	2-15	(Busy Sk #3)	
B22	1-23	(Write Enable)	
B23	1-24 +26	(Return)	
B24		(Read Enable)	Jumper
B25	1-29 + 14	(Trk Offs Plus)	
B26	1-30 + 12	(Return)	
B27	1-11	(Platter Sel)	
B28			
B29	1-16	(Return)	
B30	1-15	(Start/Stop)	
B31	1-31	(Emerg Unload)	
B32	1-32 + 20	(Return)	
B33	1-19	(Cyl Addr Stb)	
B34	1-47	(Cyl Addr 7)	
B35	1-48 + 44	(Return)	
B36	1-43	(Cyl Addr 5)	
B37	1-39	(Cyl Addr 3)	
B38	1-40 + 36	(Return)	
B39	1-35	(Cyl Addr 1)	
B40			
B41	1-2	(Return)	
B42	1-1	(Unit Sel #1)	
B43	1-5	(Unit Sel #3)	
B44	1-6	(Return)	
B45			
B46			
B47			
B48			
B49			
B50			

88-HDSK
PRELIMINARY DOCUMENTATION
SECTION V
TROUBLESHOOTING INFORMATION

TROUBLESHOOTING INFORMATION

5-1. INTRODUCTION

This section is designed to aid in locating a failure that could be encountered on the Datakeeper Controller Cards. It contains a visual inspection check list, troubleshooting procedures to help isolate component failures and a list of general procedures to be followed in troubleshooting TTL logic.

5-2. VISUAL INSPECTION CHECK LIST

Before a board is installed it should be visually inspected for problems due to improper assembly. The following checks should locate most malfunctions:

1. Look for leads that have not been soldered.
2. Check for solder bridges.
3. Check for cold solder connections.
4. Examine PC boards carefully for hairline opens in lands.
5. Check IC chips for proper pin placement and good socket connections.
6. Examine electrolytic capacitors for proper polarity.
7. Examine diodes for proper polarity.
8. Be sure the correct color code has been observed on all resistors.

5-3. GENERAL PROCEDURES FOR TROUBLESHOOTING TTL LOGIC

1. High Level (logic 1) = +2.2 volts to +5 volts
   Low Level (Logic 0) = -.6 volts to +.8 volts
2. Always work backward through the logic from the trouble area.
3. Always remove power when replacing ICs or cutting or resoldering PC lands.
4. When a gate element appears bad (an output is opposite of what it should be with a given input):
   a. Insure the IC package has correct voltage supplies and grounds.
   b. Re-check the output with the pin open (bend the pin up and re-insert the IC in its socket - if not socketed, cut the land that connects the pin to the external circuitry). If the output remains incorrect, replace the IC with a new part. If the output is now correct, look for shorts to nearby PC lands (visually and with an ohmmeter). If none are found, the probable cause

is a defective input at one of the elements that the output feeds. Isolate each input in turn by opening it from the external circuitry.

c. If an input is between .8 volts and 2 volts, check continuity back to the driving output.

5-4. PREVENTIVE MAINTENANCE

The best preventive maintenance you can give your system is a clean environment. The Datakeeper Controller requires no preventive maintenance; however, the 88-HDSK Drive requires extensive maintenance. A clean environment insures reliable operation of the Drive. For information concerning Drive maintenance, consult Section VI of the Pertec Drive Manual.

5-5. EQUIPMENT REQUIRED FOR TROUBLESHOOTING

The most useful device for troubleshooting logic in the Datakeeper Controller is an inexpensive logic probe. The Continental Specialty Corp. LP1 logic probe, which currently sells for $44.00, retail, is recommended. Also useful is a 100 MHz dual trace oscilloscope with delayed sweep. This is required for an indepth study of circuitry problems. The last piece of test equipment required is a low cost Volt/Ohmmeter for checking voltages, continuity and shorts on the circuit boards. For testing the functional operation of the Datakeeper Controller, the Diagnostic Floppy Diskette for the 88-HDSK system is recommended. To utilize this, an Altair 88-HDSK, a Floppy Disk system and 4.1 BASIC is required. The Command Format sample programs provided in Paragraph 3-5, Section B, may be used in the absence of a Diagnostic Floppy Diskette.

5-6. TROUBLESHOOTING THE POWER SUPPLY

Symptom: No +5 Volts

Procedure: Observe the AC Power LED on the Front Panel PC Board. If it is not lighted, the trouble is between the PC board and the Transformer, or the AC line. Typically the trouble is caused by a simple wiring problem. If the AC power LED is lighted, check the unregulated DC voltage across C4. Typically with no load it is 13 volts. If you do have the unregulated DC voltage across C4, check the overcurrent shutoff transistor, Q1. Normally, it should have no more than .3 volts from collector to emitter. Next, check the TIP 140 transistor (Q3) for proper operation. Normally, there should be

no more than 2.2 volts across R4. If the voltage is greater across R4, there is an open circuit in the emitter base junction of Q3. If transistor Q3 is operating properly, check the negative voltage regulator VR1 for at least 7 volts between pins 1 and 3. If all other circuits appear to be functional, VR1 is the suspected defective component. Check for no voltage between pins 1 and 2.

Symptom: Excessive Noise and Ripple on the Power Supply.

Procedure: The most obvious thing to check in this case is the peak-to-peak ripple across C4. With full load (5 amps), peak to peak ripple is 2 volts maximum at 120 Hz. An open leg of the bridge rectifier VJ048 can cause the peak-to-peak ripple to increase and the frequency to decrease to 60 Hz. Excessive noise and ripple can also be caused by a defective regulator VR1 or an excessive voltage drop across Q1.

Symptom: Intermittant Operation or Shutoff

Procedure: Check the heat sinks for Bridge Rectifier BR1 and transistor Q3. If these components are not adequately tightened to their heat sinks, they can become hot enough to melt the solder on the circuit board, causing intermittant operation. Intermittant shut off can occur if the Over Current Protection Adjustment, R1, is defective. Also a defective Q2 can cause intermittant shut down of the system. An easy way to check this is to activate the POWER RESET (switch #3) and keep the anode cathode circuit of Q2 open. In the case of intermittant shut off of the Power Supply due to the over current circuit going into action, consult the adjustment procedure for the correct setting of R1 (see Section IV, Power Supply Operation).

5-7. TROUBLESHOOTING THE PROCESSOR CARD

A preliminary check of the Processor Card may be performed with no other cards in the Controller. After turning the power switch to ON and the key switch to RUN, check pin 13 of IV byte ports 1 through 7. The Master Clock (MCLK) signal whose positive portion is approximately 50ns wide, occurring every 250ns, should be present. If this signal is not present, there is possibly a defective oscillator circuit in the CPU chip. Be sure the Reset line on the processor is HIGH when in the CPU RUN position. Next, check IC X with the CPU in the RUN mode. This sets the direction of the I/O ports going to the Altair. Pin 1 should be HIGH, pin 2 LOW, pin 3 HIGH, pin 4 LOW,

pin 5 HIGH, and pin 6 LOW. Pins 7 and 8 select the buffer number for the 256 byte block of the 1K RAM Buffer Memory. If these signals are not present on IV byte 1, the problem could be a defective IV byte 1, a defective RAM or the processor chip. To isolate the probable cause of the difficulty use known good components to replace the suspect components when possible.

Communication to the computer may now be checked. A statement in BASIC, PRINT INP(160), will test the primary handshake channel. If the result of this statement is 44, there is no communication. If the result is 172, the Primary handshake channel is functioning. A likely cause of improper communication between the Altair and the Controller is a defective IV byte or a defective cable.

A complete test of communications channels requires the use of the Diagnostic Floppy Diskette (DISCTEST). This program allows checking of all communication channels to the Processor Card. After the program is loaded and running, it requests a command be given to the Processor Card of the 88-HDSK Datakeeper Controller. When testing only the Processor Card in the system, the instructions used for checking the Data Channels are RB (Read Buffer) and WB (Write Buffer). When testing the communication channels, be sure to test all four buffer locations by Writing and Reading into each buffer. This also tests the 1K of Memory and all seven of the IV byte I/O ports. This completes the preliminary test of the Processor Card and checks almost all of its functions.

5-8. TESTING THE DISK DATA CARD

The test procedure for the other cards must be done with a fully operational system. If possible, use known good cards when testing a questionable PC Card.

To test the Disk Data Card, first identify the functions of the IV byte I/O ports. Address 33 takes Read Data from shift registers, F and M, and makes it available to the Processor. IV Byte 34 outputs Write Data from the Processor to shift registers F and M. IV Byte address 35 outputs the number of bits to be written on a sector to IC's H, P, V and A2, the Bit Counter Array. IV byte 36 takes the Disk Data Card status and makes it available to the Processor. IV byte 37 takes control signals from the Processor and presents them to the various circuits to be controlled on the Disk Data Card.

Errata 88-HDSK-ME04
Altair Hard Disk (88-HDSK)
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Page 122, first new paragraph

If the 88-HDSK Interface Card is installed, but no disk drive is connected to the 88-HDSK Interface Card, then the four Seeking lines on the 88-HDSK Interface Card must be pulled high (inactive), so that the controller can complete its initialization routine and respond to commands from the computer.

A simple way to do this is to install a temporary jumper from the positive terminal of C3 to the positive terminal of C8. This provides +5V to the termination resistors of the disk interface, and effectively pulls all signals high, including Ready. Be sure to remove this jumper before connecting a disk drive to the 88-HDSK Interface Card!

For further testing, it is convenient to build a simple tester board that plugs into P2 of the 88-HDSK Interface Card, and has 20 DIP switches to ground -- one for each input signal except Read Clock and Read Data.

The first check to make on the Disk Data Card is whether the malfunction is occurring in the Read mode or the Write mode. For a malfunction occurring in the Read mode, check pin 6 of IC E (Zone D2). Pin 6 is the DISRMD (Disk Read Mode) signal and should be HIGH. This selects the direction of IC X (Zone B3) and enables Read Clock and Read Data to be fed into the shift registers, IC F and M (Zone A7). At the beginning of the Read operation all logic must be cleared. When performing a Read operation a pulse should be present at IC E Pin 4 ($\overline{CLR}$). Next, the number of bits to be read is set up in the bit counter IC H, P, V, and A2. There should be a pulse at pin 11 of these chips before the Read mode is initiated. As soon as the Processor locates the required sector, DISTRAN STRT (Disk Transfer Start) will go HIGH for about 1 ms.

Useful test points for checking the Read operation are TP-1 (Read Clock) and TP-2 (Read Data). This will insure that the Read Clock and Read Data are being properly transferred to FIFO registers F and M. Test Point 6 (TP-6) indicates a logic 1 when the correct number of bits have been read in.

Troubleshooting the system is made easier by identifying the two fundamental modes of failure. First, there is the mode of failure where errors in data are made. This is usually caused by defective shift registers, clocks or IV bytes. The second type of failure occurs when the Processor locks up while looking for a status bit. This can be easily isolated by identifying the IV byte that is being enabled and locating the status bit that is not being made available.

To isolate the IV port the processor is holding open, check the IV bus, IV0 through IV7 and note the signal pattern. Then, check the pins of the IV bytes A through E (addresses 33 through 37) on the Hard Disk Data Card or addresses 17 through 22 on the Hard Disk Interface Card and compare the two signals. The status bit that is in error should be isolated. It is usually due to defective circuitry or to defective IV byte ICs.

One other point to test in the Read mode is the sync bit detector, IC A4 pin 2. It should be normally HIGH, going LOW when a sync bit is detected. This enables the bit counters to start counting. After the bit counters have counted to zero and TP-6 goes HIGH, the CRC checker (IC S) starts testing the next 16 bits to match them to the CRC count generated internally. If an error is detected, S pin 13 goes HIGH, or if there is no error, S pin 13 stays LOW. Pin 5 of IC K and A4 count the 16 bits of data for CRC checking.

When troubleshooting in the Write mode, the important signals to observe are Disk Transfer Start, TP-5 (Write Clock), TP-4 (Write Data) and TP-3 which is normally a 400ns clock signal. To make it easier to observe these signals it is best to put the test program, typically the Write Sector Command Program (Paragraph 3.5, Section B), in a loop that continuously issues the Write Sector command. This generates a continuous stream of signals for testing. In the Write mode check IC E pin 6 for DISRMD to go LOW. IC E pin 7, DISTRAN STRT, should go HIGH for approximately 1ms during a Write mode. If a CRC check is to be enabled, IC E pin 8 should be HIGH. This enables the check word enable pin of IC S (pin 10). IC E pin 2 should also be HIGH. This enables the mode select for Shift Registers F and M through the selection of the Disk Read mode status; thus, enabling either parallel to serial operation for writing data or serial to parallel operation for reading data. IC E pin 1, is a mode select line and should normally be LOW. This enables data transfers between the FIFO registers F and M and the IV bus.

5-9. TROUBLESHOOTING THE DISK INTERFACE CARD

The Disk Interface Card provides communication between the 88-HDSK Drive and the Processor. This card is relatively easy to troubleshoot using the Diagnostic Test Program (DISCTEST). It has three IV byte ports 17, 18, and 19 (ICs H, I and J) which output data from the Controller through line drivers to the 88-HDSK Drive. A simple check of the signals will indicate proper or improper communications from the bus to the outputs of the IV byte ports. A check on either side of the line drivers could locate a defective line driver. Checking signals being transferred from the 88-HDSK Drive to the Processor includes IV byte address 20, 21 and 22 (IC's K, L and M). Inverters are used to drive the IV bytes and a simple check on either side of these inverters again indicate whether the signal is getting through the inverter or not. When a Drive is selected, check for the continuous sector count on the inputs to IV byte M, pins 1 through 8 (address 22). IC H determines which one of four Drives may be selected. Head select, Platter select, or Extension select should also match the command given to the unit. These signals going to and from the Drive are active LOW. A HIGH condition is a False condition and a LOW condition is an enable or True condition. When selecting a cylinder address, the command may be verified by checking the cylinder address lines. The Read Circuit and the Write Circuit are contained in IC's A, B, C, D and F. Check IC F pin 7 in the Write Circuit for a 10MHz

square wave. TP-4 (IC D) should be a 2.5MHz square wave which is the $\overline{\text{Write Clock}}$. The Read Circuit,consisting primarily of IC B,converts the pulsing Return To Zero Read Data into Non-Return To Zero Read Data (NRZ) at TP-2. NRZ Read Data is stable during the falling edge of the $\overline{\text{Read Clock}}$. The signals should be checked during Read mode operation.

appendix A
parts list

88-HDSK Processor Card

Quantity	Component Description	MITS Part #
1	2N5320 transistor	102833
1	MP080 crystal, 8MHz	102553
2	26-pin connector, right angle	102548
1	50-pin connector, straight	102554
2	25-pin socket strip	102126
7	24-pin IC socket	102105
17	20-pin IC socket	102127
9	16-pin IC socket	102103
2	14-pin IC socket	102102
2	PC ejectors & pins	102552
1	PC board	100234
2	cable assembly	103916
2	bulkhead connector assembly	100917
2	cable assembly	103906
1	marking dot (brown)	102562
1	marking dot (red)	102535
2	marking dot (blue)	102560
1	8X300 IC bipolar processor	101448
1	74LS04 IC inverter	101042
1	74LS00 IC NAND gate	101069
1	74S138 IC 3 to 8 decoder	101450
1	74LS377 IC octal latch	101451
1	8T32 IC IV byte, I/O port - addr. 1	101436
1	8T32 IC IV byte, I/O port - addr. 2	101437
1	8T32 IC IV byte, I/O port - addr. 3	101438
1	8T32 IC IV byte, I/O port - addr. 4	101439
1	8T32 IC IV byte, I/O port - addr. 5	101440
1	8T32 IC IV byte, I/O port - addr. 6	101441
1	8T32 IC IV byte, I/O port - addr. 7	101442
8	93425 IC 1K memory	101452
4	1K 1/2W 5% resistor	101928
4	10µf, 16v capacitor, tant. dip	100394
37	.1µf, 12v capacitor, ceramic disk	100348

88-HDSK Interface Ca[illegible]

Quantity	Component Description	MITS Part #
1	8T32 IC, IV byte I/O port - addr. 17	101425
1	8T32 IC, IV byte I/O port - addr. 18	101426
1	8T32 IC, IV byte I/O port - addr. 19	101427
1	8T32 IC, IV byte I/O port - addr. 20	101428
1	8T32 IC, IV byte I/O port - addr. 21	101429
1	8T32 IC, IV byte I/O port - addr. 22	101430
12	75451 IC non-inv. line driver	101443
1	75452 IC inv. line driver	101444
5	74LS04 IC inverter	101042
1	74LS10 IC NAND gate	101133
2	74LS74 IC D-FF	101088
1	74107 IC JK-FF	101002
1	74S124 IC, VCO	101445
5	1K, 1/2W 5% resistor	101928
1	22 ohm, 1/2W 5% resistor	102220
6	330 ohm resistor pack	102222
6	220 ohm resistor pack	102221
5	10µf, 16v capacitor, tant. dip	100394
19	.1µf, 12v capacitor, ceramic disk	100348
1	MP100 crystal, 10MHz	102551
8	1030-4 test point terminal	101663
2	50-pin connector	102503
6	24-pin IC socket	102105
1	16-pin IC socket	102103
9	14-pin IC socket	102102
13	8-pin IC socket	102101
2	PC ejector & pins	102552
1	PC board	100232
4	2.2µf, 16v capacitor, tant. dip	100402
1	marking dot (brown)	102562
1	marking dot (red)	102535
2	marking dot (green)	102559

88-HDSK Data Card

Quantity	Component Description	MITS Part #
1	8T32 IC, IV byte I/O port addr. 33	101431
1	8T32 IC, IV byte I/O port addr. 34	101432
1	8T32 IC, IV byte I/O port addr. 35	101433
1	8T32 IC, IV byte I/O port addr. 36	101434
1	8T32 IC, IV byte I/O port addr. 37	101435
2	9403 IC	101447
5	74LS191 IC	101148
4	74LS08 IC AND gate	101186
5	74LS157 IC 2T01 MUX	101196
2	74LS04 IC inverter	101042
1	9401 IC	101446
1	74LS11 IC AND gate	101089
1	74LS74 IC D-FF	101088
1	74LS32 IC OR gate	101191
1	74LS107 IC JK-FF	101195
2	1K 1/2W 5% resistor	101928
8	10µf, 16v capacitor, tant. dip	100394
29	.1µf, 12v capacitor, ceramic dip	100348
4	12-pin strip socket	102125
5	24-pin IC socket	102105
10	16-pin IC socket	102103
11	14-pin IC socket	102102
7	1030-4 test point terminals	101663
2	6297 PC ejectors & pins	102552
1	PC card	100233

88-HDSK Mother Board

Quantity	Component Description	MITS Part #
1	trimpot 2K, 20T	102219
1	330 ohm 1/2W 5% resistor	101926
2	100 ohm 1/2W 5% resistor	101924
1	33 ohm 1/2W 5% resistor	101921
2	1K 1/2W 5% resistor	101928
4	.47 ohm 2W 5% resistor (wirewound)	102004
1	47 ohm 1W 5% resistor	101955
1	.1µf, 12v capacitor, ceramic disk	100348
1	1000µf, 25v capacitor, electrolytic	100365
1	10µf, 16v capacitor, dip tant.	100394
1	2.2µf, 16v capacitor, dip tant.	100402
1	1N4004 diode	100718
1	CS4410 transistor, NPN	102806
1	2N5061 thyristor (SCR)	102832
1	TIP140/141 transistor	102819
1	7905 regulator (-5v)	101146
1	VJ048 10 amp 50v bridge rectifier	100711
1	10-pin male connector	102549
1	4-pin PC mount plug	102550
5	100-pin edge connector	101864
1	PC board	100231

88-HDSK Cable Interface

Quantity	Component Description	MITS Part #
2	cable assembly	103915
2	8-32 x 3/8" screw	100928
2	#8 lockwasher	100945
1	PC board	100236
1	1N5820 diode, 3.0 amp, 20v	100713