altair 680b

UNIVERSAL I/O BOARD DOCUMENTATION

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altair 680h

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Altair 680b Universal I/O Board

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SECTION I
INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

The Altair 680b Universal I/O Board Documentation provides a general description of the printed circuit board and detailed theory of its operation. The manual contains five sections as follows:

1. Section I contains a general description of the Altair 680b Universal I/O Board.
2. An explanation of parallel (PIA) and serial (ACIA) port selection, including the port structure and operation, is presented in Section II.
3. Section III includes a detailed theory explanation of the 680b Universal I/O circuit operation.
4. Section IV contains instructions for installing the Universal I/O Board into the Altair 680b computer.
5. Troubleshooting information for the 680b Universal I/O Board is found in Section V.

1-2. DESCRIPTION

The 680b Universal I/O Board provides two parallel ports and one serial port while occupying only one slot on the 680b expander card. The design of the parallel and serial ports is based upon two peripheral ICs, the 6820 Parallel Interface Adapter (PIA) and the 6850 Asynchronous Communication Interface Adapter (ACIA), respectively.

The PIA contains all Control and Data Registers, thus most options are software selectable. These options include data direction (each data line can act as an input or an output) and interrupt/control structure. The Universal I/O Board can be expanded up to two parallel ports. With only one PIA parallel port, the board can handle two inputs (such as a paper tape reader or keyboard) or two output devices (such as a paper tape punch and printer) or any combination of custom applications. A Universal I/O with two PIA parallel ports has 32 data lines (each group of eight is individually selectable) and all data lines are fully TTL compatable. When utilized as outputs, eight of the 16 data lines are capable of directly driving the base of a transistor switch (1.5v at 1ma). The Universal I/O is also provided with a parallel 8-bit non-latched output at TTL levels.

The ACIA allows data to be taken in from a device in serial and transferred onto the data bus in parallel. Data can also be entered from the data bus into the ACIA in parallel and sent out to a device in serial form. The ACIA contains both Control and Status Registers. Five control lines allow maximum utilization of sophisticated terminals. The five control lines are Transmit Data, Receive Data, Data Carrier Detect, Clear To Send, and Request To Send. The 8-bit Status Register allows for greater control and handshaking ability by indicating received data available, transmitter buffer empty, carrier detect, clear to send, framing error, received data overflow, parity error, and interrupt request.

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SECTION II
THEORY OF OPERATION - PORT SELECTION

2-1. GENERAL

Section II contains a detailed description of the MITS Altair 680b Universal I/O Board parallel (PIA) and serial (ACIA) port selection. Tables are provided to aid in understanding the PIA and ACIA structure and operation.

2-2. PARALLEL PORT (PIA) SELECTION

The Altair 680b reserves 256 address locations for I/O interfacing and each I/O card requires 16 address lines. Hardware sets the upper address lines, A15 through A8, to F0 for all I/O ports. These addresses are F0XX (XX = user selectable). Address lines A7 through A4 and their complements, $\overline{A7}$ through $\overline{A4}$, are also user selectable. With these addresses, there are 16 different address locations for the Universal I/O. Address lines A3 and A2 select between three ports. A3 addresses the parallel ports or the serial port and A2 selects between the parallel ports.

Each PIA contains two sections, A and B, and each section has two channels, Control/Status and Data-Data Direction. Address lines AØ and A1 enable the selection of the port section and the channel. If the two parallel ports are addressed at F008 and F00C, the port, section, and channel addresses would appear as in Table 2-1, assuming the board is strapped at the lowest possible position.

Table 2-1. PIA Address Selection

ADDRESS	IC	SECTION	CHANNEL
F008	C	A	CONTROL/STATUS
F009			DATA - DDR
F00A		B	CONTROL/STATUS
F00B			DATA - DDR
F00C	B	A	CONTROL/STATUS
F00D			DATA - DDR
F00E		B	CONTROL/STATUS
F00F			DATA - DDR

The simplified block diagram (Figure 2-A) illustrates the internal structure of a PIA. Each port section, A and B, contains three registers, eight data lines, two control lines and an interrupt request output. The Control/Status Register (Table 2-2) is a Read/Write register, meaning that it can be written into and read from. Bits 7 and 6 are unaffected during a Write.

Figure 2-A. Internal Structure of a PIA

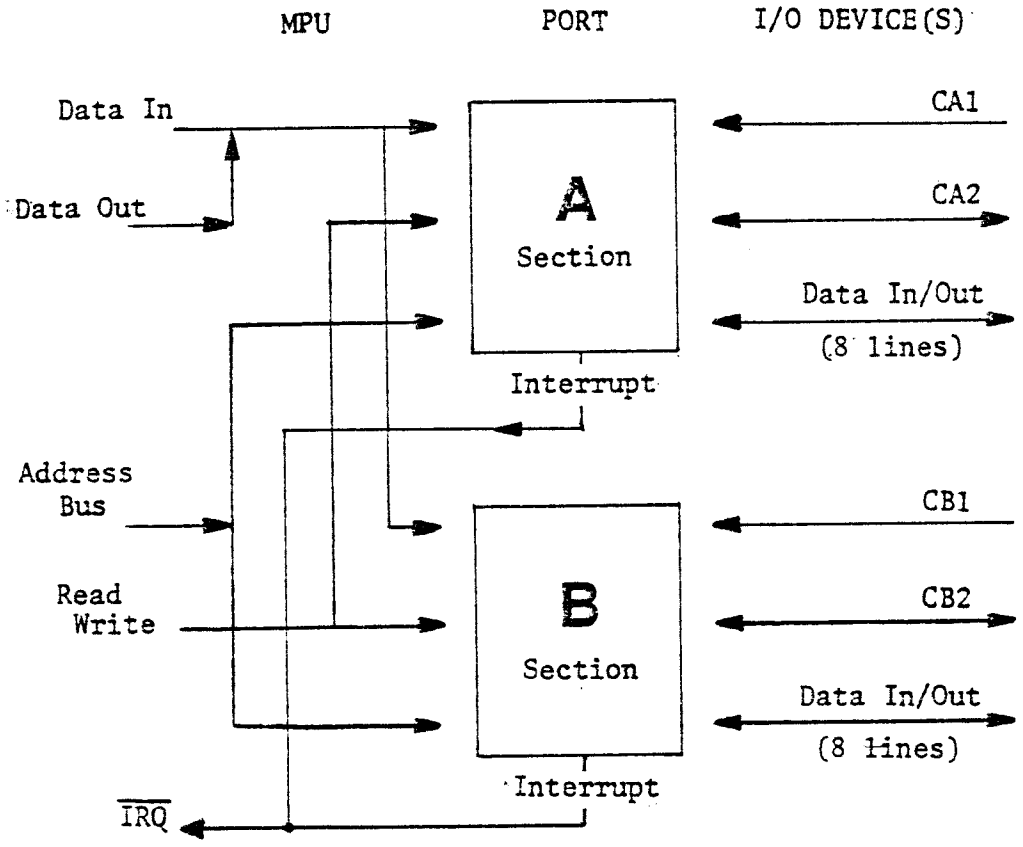

Table 2-2. PIA Control Status Register

Bit #	7	6	5	4	3	2	1	0
Function	Interrupt Request		C2 Control			DDR Control	C1 Control	

Control bits 1 and Ø affect the operation of the external control line, C1. C1 is used as an input control line from the I/O device. Status bit 7 and the interrupt request output to the system bus, $\overline{IRQ}$, are then affected by the activity of C1 as shown in Table 2-3. Bit 7 and $\overline{IRQ}$ are reset (bit 7 goes LOW, $\overline{IRQ}$ goes HIGH) when the Data Register is read by the MPU. Control bit 1 determines whether C1 is active with a LOW going transition (bit 1 = 0) or active with a HIGH going transition (bit 1 = 1). The $\overline{IRQ}$ is dependant on how bit Ø is set in the Control Register. For example, if bit Ø = 1 and C1 is active, the $\overline{IRQ}$ output will be LOW, interrupting the system.

Table 2-3. Control of Interrupt Inputs, C1 (CA1 and CB1)

CONTROL BITS 1	0	C1 INPUT	STATUS BIT 7	$\overline{IRQ}$ OUTPUT
0	0	Active LOW	Set HIGH when C1 is active	Disabled -- remains HIGH
0	1	Active LOW	Set HIGH when C1 is active	Goes LOW when Bit 7 is HIGH
1	0	Active HIGH	Set HIGH when C1 is active	Disabled -- remains HIGH
1	1	Active HIGH	Set HIGH when C1 is active	Goes LOW when Bit 7 is HIGH

The C2 control line can function as either an input or an output for the I/O device. When C2 functions as an input (control bit 5 LOW), its mode of operation is determined by control bits 5, 4, and 3 as shown in Table 2-4. Sections A and B operate identically when C2 functions as an input.

Table 2-4. Control of Interrupt Inputs, C2 (CA2 and CB2)

CONTROL BITS 5	4	3	C2 INPUT	STATUS BIT 6	$\overline{IRQ}$ OUTPUT
0	0	0	Active LOW	Set HIGH when C2 is active	Disabled -- remains HIGH
0	0	1	Active LOW	Set HIGH when C2 is active	Goes LOW when Bit 6 is HIGH
0	1	0	Active HIGH	Set HIGH when C2 is active	Disabled -- remains HIGH
0	1	1	Active HIGH	Set HIGH when C2 is active	Goes LOW when Bit 6 is HIGH

C2 (noted as CA2) functions as an output in section A (control bit 5 HIGH) as shown in Table 2-5. The E pulse is the Ø2 (500KHz) from the 680b system bus which partially enables the port to Read and Write.

Table 2-5. Control of CA2 As An Output

A SECTION CONTROL BITS			CA2	
5	4	3	CLEARED	SET
1	0	0	LOW after E pulse, following read of A data channel	HIGH when CA1 is active
1	0	1	LOW after a read of A data channel	HIGH following next E pulse
1	1	0	Always LOW when Bit 3 is LOW	
1	1	1		Always HIGH when Bit 3 is HIGH

C2 (noted as CB2) functions as an output in section B (control bit 5 HIGH) as shown in Table 2-6. To write into a Control Register, load the accumulator with each bit set according to the tables. Then store the accumulator at the address location of the control channel. All the ports are reset when power is first applied, thereby resetting the data lines and the C2 line for both sections as inputs.

Table 2-6. Control of CB2 As An Output

B SECTION CONTROL BITS			CB2	
5	4	3	CLEARED	SET
1	0	0	LOW on positive going transitions of first E pulse following write on B data channel after Control/ Status bit 7 is cleared by read of B data channel.	HIGH when C/S Bit 7 is set HIGH by CB1 active transition
1	0	1	LOW when E pulse goes HIGH, following a write of B data channel	HIGH when next E pulse goes HIGH
1	1	0	Always LOW when Bit 3 is LOW	
1	1	1		Always HIGH when Bit 3 is HIGH

Data channel address permits access to either the Data Register or the Data Direction Register (DDR). The status bit 2 in the Control Register determines whether the Data Register or the DDR is accessed. If bit 2 is a logic Ø, the DDR is accessed. If bit 2 is logic 1, the Data Register is accessed. Writing a logic 1 into any bit of the DDR will cause the corresponding data line to act as an output. Writing a logic Ø into any bit of the DDR will cause the corresponding data line to act as an input. Thus, there can be any combination of inputs or outputs on the data lines (PAØ through PA7 and PBØ through PB7).

2-3. PIA Initialization

Program 2-I illustrates the initialization procedure for a parallel port. The initialization sets up communication between the MPU and the 680b Universal I/O Board. In this example, PIA-C is utilized and the Universal I/O is addressed at its lowest location, F008 through F00B. If a second parallel port is used, the lowest address location would be F00C through F00F.

The addresses function as follows: F008 = section A Control/Status Register; F009 = section A Data-Direction (when accessed) and Data Channel Register; F00A = section B Control/Status Register; F00B = section B Data-Direction (when accessed) and Data Channel Register.

Section A functions as an input and section B functions as an output.

INPUT

1. If the I/O device has valid data, a strobe signal from the I/O device pulls the input CA1 line LOW. Bit 7 of section A Control/Status Register goes HIGH. CA2 goes LOW following a Read of section A Data Channel, then returns HIGH after the next ENABLE pulse. CA2 is telling the I/O device that data has been read and to send more data.
2. With additional programming, the MPU can be instructed to periodically check the section A Control/Status Register to interpret the status of bit 7. When bit 7 is HIGH, Step 3 will be entered.
3. Data Channel Register is input to the accumulator. This, in turn, resets bit 7 of the Control/Status Register and CA2 becomes active. CA2 returns HIGH after the next E pulse. CA2 tells the I/O device that new data may be entered.

OUTPUT

1. CB1 is pulled LOW by the device when it is ready to receive new data.
2. With additional programming, the MPU can be instructed to periodically input the section B Control/Status Register to interpret the status of bit 7. When bit 7 is HIGH, Step 3 will be entered.
3. Data is output to the I/O device and latched into the port's output. CB2 goes LOW when the next E pulse goes HIGH. CB2 returns to a HIGH position when the E pulse goes HIGH again. CB2 can be used to strobe data into the I/O device.

Using the 680b monitor M and N commands, enter all underlined characters in Program 2-I. The index mode of addressing is used.

Program 2-I. PIA Initialization

```
.M  0000  CE
.N  0001  F0
.N  0002  08
.N  0003  4F          CLRA   A➔00
.N  0004  A7  }
.N  0005  00  }       ACCESS DDR OF SECTION A
.N  0006  A7  }
.N  0007  01  }       SET SECTION A AS INPUTS
.N  0008  A7  }
.N  0009  02  }       ACCESS DDR OF SECTION B
.N  000A  43          COMA   A➔FF
.N  000B  A7  }
.N  000C  03  }       SET SECTION B AS OUTPUTS
.N  000D  86  }       CA1 = ACTIVE LOW; IRQ IS DISABLED
.N  000E  2C  }       CA2 = ACTIVE LOW AFTER READ OF SECTION A
.N  000F  A7  }             DATA CHANNEL REGISTER, THEN GOES
.N  0010  00  }             HIGH FOLLOWING NEXT E (ENABLE) PULSE.
.N  0011  A7  }       CB1 = ACTIVE LOW; IRQ IS DISABLED
.N  0012  02  }       CB2 = ACTIVE LOW WHEN E PULSE GOES HIGH
                            FOLLOWING A WRITE OF SECTION B
                            DATA CHANNEL REGISTER. RETURNS
                            HIGH WHEN THE NEXT E PULSE GOES HIGH.
```

2-4. SERIAL PORT (ACIA) SELECTION

The 680b Universal I/O Board utilizes a 6850 Asynchronous Communications Interface Adapter (ACIA). The ACIA allows serial data to be taken in on its receive line and transfers the data onto the data bus, or data can be entered from the data bus into the ACIA and sent out the transmit data line in serial form.

The ACIA has three chip select inputs, CSØ, CS1, and $\overline{CS2}$, which are used in the selection of the ACIA. It also has a Register Select (RS) input, controlled by address line AØ, that can select between the different internal registers. The ENABLE signal is used for internal interrupt control and the timing of Control/Status changes. Since all data transfers take place during Ø2 of the system clock, it is used as the ENABLE signal. The R/W signal determines the direction of data flow.

2-5. ACIA Control Register

The ACIA has an 8-bit Control Register that allows port configuration under software control. Each bit is defined in Table 2-7.

7	6	5	4	3	2	1	0
In Interrupt	Out Interrupt		Transmission Bits			Clock Divide And Reset	

NOTE: Data Bit LOW = 0
Data Bit HIGH = 1

Table 2-7. ACIA Control Register

The first two data bits, Ø and 1, control the internal clock divide circuit and the Master Reset as shown in Table 2-8.

BIT 1	BIT Ø	FUNCTION
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Table 2-8. Control Bits for Internal Clock Divide and Master Reset

Normal operations output bits Ø and 1 as equal to "1" to reset the ACIA. When initializing the port, the internal clock divide is set to ÷ 16 because the baud rate clock frequency is 16 times higher than the selected baud rate. Refer to Table 2-9 for the desired baud rate.

POSITION				BAUD RATE
1	2	3	4	
0	1	0	0	50
1	1	0	0	75
0	0	1	0	134.5
1	0	1	0	200
0	1	1	0	600
1	1	1	0	2400
0	0	0	1	9600
1	0	0	1	4800
0	1	0	1	1800
1	1	0	1	1200
0	0	1	1	2400
1	0	1	1	300
0	1	1	1	150
1	1	1	1	110

NOTE: This Baud Rate uses the ÷ 16 mode for the ACIA. To select the correct baud rate, position the correct switch of S10 to the 1 or 0 side marked on the silkscreen.

Table 2-9. S10 Baud Rate Selection

In order to choose any one of 5 additional baud rates, select the baud rate from Table 2-10 and set S10, using the ÷ 64 mode (data bits 1 and Ø are equal to 1 and Ø, respectively). Note that the selected baud rate is four times larger than the desired baud rate. Due to the internal structure of the ACIA, it is not possible to use the ÷ 1 clock because some means of external synchronization must be used.

DESIRED BAUD RATE	SELECTED BAUD RATE
27.5	110
37.5	150
75.0	300
450	1800
600	2400

Table 2-10. Additional Baud Rate Selection

The next three bits of the Control Register determine word length, parity, and the number of stop bits. Consult the I/O device manual for the configuration required and set the bits according to Table 2-11.

DATA BIT			FUNCTION		
4	3	2	# of Data Bits	# of Stop Bits	Parity
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	2	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

Table 2-11. Transmission Control Bits

The last three bits of the Control Register control interrupts and I/O device handshake as shown in Table 2-12.

DATA BIT			FUNCTION
7	6	5	
X	0	0	$\overline{RTS}$ = LOW, transmitting interrupt disabled.
X	0	1	$\overline{RTS}$ = LOW, transmitting interrupt enabled.
X	1	0	$\overline{RTS}$ = HIGH, transmitting interrupt disabled.
X	1	1	$\overline{RTS}$ = HIGH, transmits a break level on the transmit data output. Transmit interrupt disabled.
0	X	X	Receive interrupt disabled
1	X	X	Receive interrupt enabled
X = does not matter			

Table 2-12. Interrupt Control Bits

Table 2-13 shows the ACIA initialization for a Teletype with eight data bits, two stop bits, and no parity. This example illustrates the initialization when the Control/Status Registers are located at address F006.

OCTAL CODE	FUNCTION
86	
03	
B7	Reset Port
F0	
06	
86	Set up for 8 data bits,
B1	2 stop bits, no parity,
B7	÷ 16 mode,
F0	$\overline{RTS}$ = LOW, transmit and
00	receive interrupts enabled.

Table 2-13. ACIA Sample Initialization

2-6. ACIA Status Register*

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when Register Select (RS) is LOW and R/W is HIGH. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit Ø - RDRF indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. $\overline{\text{Data Carrier Detect}}$ being HIGH also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The TDRE bit being set HIGH indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The LOW state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

$\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), Bit 2 - The $\overline{\text{DCD}}$ bit will be HIGH when the $\overline{\text{DCD}}$ input from a modem has gone HIGH to indicate that a carrier is not present. This bit going HIGH causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains HIGH after the $\overline{\text{DCD}}$ input is returned LOW until cleared by first reading the Status Register and then the Data Register or until a Master Reset occurs. If the $\overline{\text{DCD}}$ input remains HIGH after Read Status and Read Data or Master Reset have occurred, the $\overline{\text{DCD}}$ status bit remains HIGH and will follow the $\overline{\text{DCD}}$ input.

$\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$), Bit 3 - The $\overline{\text{CTS}}$ bit indicates the state of the $\overline{\text{CTS}}$ input from a modem. A LOW $\overline{\text{CTS}}$ indicates that there is a $\overline{\text{Clear To Send}}$ from the modem. In the HIGH state, the Transmit Data Register Empty bit is inhibited and the $\overline{\text{Clear To Send}}$ status bit will be HIGH. Master Reset does not affect the $\overline{\text{Clear To Send}}$ status bit.

Framing Error (FE), Bit 4 - FE indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The FE flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 - Overrun is an error flag that indicates one or more characters in the data stream were lost. This means that a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a Read of the RDR having occurred. The overrun does not occur in the Status Register until the valid character prior to overrun has been read. The RDRF bit remains set until the overrun is reset. Character synchronization is maintained during the overrun condition. The overrun indication is reset after reading of the data from the RDR. Overrun is also reset by the Master Reset.

Parity Error (PE), Bit 6 - The parity error flag indicates that the number of HIGHs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request (IRQ), Bit 7 - The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is LOW the IRQ bit will be HIGH to indicate the interrupt or service request status.

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SECTION III
THEORY OF OPERATION-CIRCUITRY

3-1. GENERAL

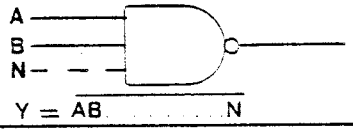
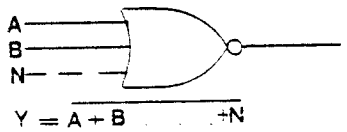
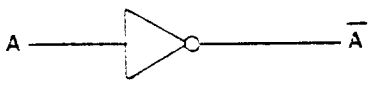
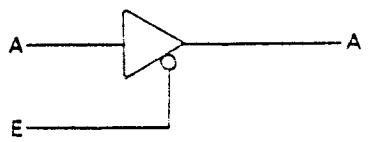
Section III provides a detailed theory explanation of the 680b Universal I/O Board circuitry, including a basic description of the logic symbols used in the Universal I/O schematics.

3-2. LOGIC CIRCUITS

The detailed schematics of the 680b Universal I/O Board (sheets 1 of 3, 2 of 3, and 3 of 3) are drawn to aid in determining signal direction and tracing. A solid arrow (→) on the signal line indicates direction.

The logic circuits used in the Universal I/O schematics are presented in Table 3-1. The table provides the functional name, symbolic representation, and brief description of each logic circuit. Where applicable, a truth table is furnished to aid in understanding circuit operation. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

Table 3-1. Symbol Definitions

NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate		The NAND gate performs one of the common logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output.
NOR gate		The NOR gate performs one of the common logic functions. Any of the inputs needs to be enabled (HIGH) to produce the desired (LOW) output.
Inverter		The inverter is an amplifier whose output is the opposite state of the input.
Non-Inverting Bus Driver		The non-inverting bus driver is an amplifier whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.

3-3. ADDRESS DECODING

All the ports begin with the starting address FOXX (XX = user selectable). With FO on the upper eight address lines (sheet 1 of 3, zone D7), all the inputs to NAND gate W are HIGH (logic 1). Address lines A11 through A8 are inverted HIGH. This enables NAND gate W pin 8 (zone D6) LOW (logic Ø). This signal is inverted HIGH and presented to the input of NAND gate J pin 5 (zone D4). The VMA (Valid Memory Address), which is used to tell I/O peripherals that a valid memory address exists on the address bus, also presents a HIGH signal at pin 4 (zone D4) to enable gate J pin 6 LOW. The LOW at pin 6 of J is inverted at pin 6 of V (zone D3).

The next four address lines, A7 through A4 (zone C7), are user changeable with a possible 16 switch positions that are controlled by switch S9. Refer to Table 3-2 for S9 address selection. Depending on the position of S9, A7 through A4 can be inverted or double inverted to the inputs of NAND gate Z pins 13, 12, 10, and 9 (zone C4). Assuming that S9 is positioned for $\overline{A7}$, $\overline{A6}$, $\overline{A5}$, and $\overline{A4}$, address lines A7 through A4 are LOW and inverted HIGH at the inputs of NAND gate Z. This enables the output of Z pin 8 LOW and this signal is presented to the input of NOR gate T pin 2 (zone C4). A LOW from NAND gate J pin 6 (zone D4) is also present, thus enabling the output of NOR gate T pin 1 (zone C3) HIGH. Therefore, two of the enabling signals required for the chip selects (CS) on the PIAs and ACIA have been decoded.

Table 3-2. S9 Address Selection

PIA - B	PIA - C	ACIA - D	S9 Positions A7	A6	A5	A4
F00C - F00F	F008 - F00B	F006 - F007	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
F01C - F01F	F018 - F01B	F016 - F017	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4
F02C - F02F	F028 - F02B	F026 - F027	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$
F03C - F03F	F038 - F03B	F036 - F037	$\overline{A7}$	$\overline{A6}$	A5	A4
F04C - F04F	F048 - F04B	F046 - F047	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$
F05C - FC5F	F058 - F05B	F056 - F057	$\overline{A7}$	A6	$\overline{A5}$	A4
F06C - F06F	F068 - F06B	F066 - F067	$\overline{A7}$	A6	A5	$\overline{A4}$
F07C - F07F	F078 - F07B	F076 - F077	$\overline{A7}$	A6	A5	A4
F08C - F08F	F088 - F08B	F086 - F087	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
F09C - F09F	F098 - F09B	F096 - F097	A7	$\overline{A6}$	$\overline{A5}$	A4
F0AC - F0AF	F0A8 - F0AB	F0A6 - F0A7	A7	$\overline{A6}$	A5	$\overline{A4}$
F0BC - F0BF	F0B8 - F0BB	F0B6 - F0B7	A7	$\overline{A6}$	A5	A4
F0CC - F0CF	F0C8 - F0CB	F0C6 - F0C7	A7	A6	$\overline{A5}$	$\overline{A4}$
F0DC - F0DF	F0D8 - F0DB	F0D6 - F0D7	A7	A6	$\overline{A5}$	A4
F0EC - F0EF	F0E8 - F0EB	F0E6 - F0E7	A7	A6	A5	$\overline{A4}$
F0FC - F0FF	F0F8 - F0FB	F0F6 - F0F7	A7	A6	A5	A4

The address location for the hardware programmable bits is F003 on the address bus. This location is fixed and cannot be changed by the user. The correct address will enable Tri-State drivers R and S pins 1 (zone C2 and D2) LOW, and this signal allows the switch selectable inputs (logic 1 or Ø) to be passed on to the outputs of R and S. The inputs of NAND gate H pins 1, 2, and 13 (zone C3) are HIGH, enabling the output pin 12 LOW. The HIGH signal at pin 1 comes directly from inverter V (zone D3) and was derived from NAND gate W as described earlier. The HIGH signal at pin 2 is derived from address lines A7 through A4. These address lines are LOW and inverted to the inputs of NAND gate Z pins 1, 2, 4, and 5 (zone D6). The output of Z pin 6 is enabled LOW then inverted, presenting a HIGH at pin 2 of gate H. The HIGH at pin 13 is supplied when the output of NAND gate B1 pin 6 (zone C5) is LOW and inverted at G. To enable B1 LOW, address lines A2 and A3 (zone B7) are LOW then inverted to present the appropriate signals at the inputs of B1 pins 5 and 4 (zone C5). The other two inputs of B1, N and P, are double inverted address lines A1 and AØ (sheet 2 of 3, zone C8 and B8) and must be HIGH for the input pins 1 and 2 of B1 to be HIGH.

The address locations for an 8-bit parallel non-latched interface are set at F010 Control/Status and F011 Data for Drive 1 and F012 Control/Status and F013 Data for Drive 2. These addresses are set and are not user selectable. Address lines A1 and and AØ are both inverted. A1 determines which address location is used. If A1 is LOW, F010/F011 is selected and if A1 is HIGH, F012/F013 is used for Control/Status and Data Channels.

When FO for the upper address lines is selected, a LOW signal is presented to the input of NOR gate T pin 5 (sheet 1 of 3, zone C5). A LOW signal also goes to pin 6 from the output of NAND gate A1 pin 8 (zone B5). For A1 to have a LOW output, all the inputs must be HIGH. Address lines A7, A6, A5, A3, and A2 are LOW and inverted HIGH to the inputs of A1 pins 6, 12, 11, 5, and 4. A4 is double inverted to the input of A1 pin 2 and must be HIGH for the proper condition to exist. VMA is tied to pin 1 of A1. With VMA valid and the other input pins of A1 HIGH, the output pin 8 will be LOW.

The LOW signals at the input pins 5 and 6 (zone C5) enable pin 4 of NOR gate T HIGH. This signal goes to NAND gate H pin 11 (zone B5), enabling the gate for double inverted R/W and Ø clock signals. A LOW going pulse, 1 microsecond wide with a 20 microsecond period, occurs at the output pin 8 when data or status is being read from the device. This LOW going pulse is the READ STROBE and goes to J2 which is a 24-pin socket. A flat cable assembly plugs into this socket. The 25-pin plug on the other side of the assembly is used for the interface. The READ STROBE signal enables pins 1 (zone B5 and A5) of Tri-State drivers M and P, allowing data to be transferred from the device to the data bus.

The HIGH signal from NOR gate T pin 4 is also present at the input of NAND gate F pin 2 (zone C4) and inverted to F pin 4 (zone B3). R/W-P (zone D7) is inverted HIGH to F pin 1, enabling the output of F pin 3 (zone C3) LOW. There is a delay on this line and it is used to insure that Write data is valid when it is written into the device. The WRITE STROBE occurs at the output of E pin 6 (zone C2) and is a LOW going pulse with an approximate width of 1 microsecond and a period of 3 milliseconds. This signal goes directly to socket J2. Write data becomes valid 200 nanoseconds (maximum) after Data Bus Enable (DBE), which is tied directly to Ø2 of the system clock, is active HIGH.

The LOW output signal from gate F pin 3 enables pins 1 (zone B6 and A6) of Tri-State drivers L and N, allowing data to be transferred from the 680b data bus to the device. The resistors on the device data lines are used for noise immunity.

If the interface is being addressed, the input of NAND gate F pin 4 (zone B3) is LOW. This keeps the output of F pin 6 HIGH and does not allow an interrupt from the device. When the interface is not being addressed, pin 4 of F is HIGH and the data lines to the interface are HIGH. If an interrupt is seen from the device and pin 4 of F is HIGH, a LOW signal may appear at one of the three inputs of NAND gate H pins 3, 4, or 5 (zone B2). These inputs are tied to bits Ø, 1, and 7, respectively. If a LOW does appear on one of the inputs of H, the output pin 6 (zone B3) is HIGH, enabling NAND gate F LOW, indicating an interrupt.

3-4. PORT SELECTION

The three ports (ACIA-D, PIA-C, PIA-B) each have three chip select lines. These are CSØ, CS1, and $\overline{CS2}$ (sheet 2 of 3). For each port to be enabled, CSØ and CS1 must be HIGH when $\overline{CS2}$ is LOW. This is accomplished by address decoding. The CSØ lines for each port are tied together by line J (zone A8). The two CS1 lines of PIAs C and B are tied together by line K, and CS1 of ACIA-D is tied to a double inverted A1 line (zone C8).

Assuming the S9 switch is positioned for $\overline{A7}$, $\overline{A6}$, $\overline{A5}$, and $\overline{A4}$, the ACIA-D address will be F006 for Control/Status and F007 for Data. The CSØ line pin 8 (zone D5) is tied to line J and must be HIGH for ACIA-D to be selected. For line J to be HIGH, the correct upper order address for lines A15 through A8 (sheet 1 of 3) must be selected, and lines A7 through A4 must be selected according to the position of switch S9.

The CS1 signal line for ACIA-D pin 10 (sheet 2 of 3, zone C5) is controlled by address line A1. A1 must be HIGH for ACIA-D to be selected since the signal is double inverted to the input pin 10. Line K is tied to CS1 of both parallel ports at pins 24 and must be HIGH at the same time CSØ is HIGH. This signal was derived earlier.

Addresses A3 (zone D8) and A2 (zone C8) are the inputs for a $\overline{CS2}$ decoding circuit. Only one of the outputs of NAND gate J (zone D7 and C7) should be LOW, enabling the particular port being used. The remaining two outputs of J should be HIGH, disabling the other ports. If the output of J pin 3 (zone D7) is LOW (ACIA-D selected), the input pins 1 and 2 are HIGH. Address line 2 is HIGH and this signal is presented to pin 1. Address line 3 is inverted HIGH and goes to pin 2. These two input signals give the desired LOW at the output of NAND gate J. If A3 is LOW, this signal goes directly to the inputs of NAND gates J pins 10 and 13, disabling both gates. If PIA-C (location FOO8) is selected, the output of J pin 8 (zone C7) is LOW. Input pins 10 and 9 must be HIGH for pin 8 to be LOW. This is assuming that S9 is positioned to $\overline{A7}$, $\overline{A6}$, $\overline{A5}$, and $\overline{A4}$. A HIGH signal from A3 goes directly to pin 10. A2 is LOW and inverted to present a HIGH to the input pin 9. The LOW signal from A2 goes directly to the input pins 1 and 12 of J, disabling ACIA-D and PIA-B. If PIA-B is to be enabled (location FOOC), pin 11 (zone C7) should be LOW, and the other two output pins 3 and 8 should be HIGH. A HIGH signal goes directly to input pins 12 and 13 from A2 and A3, respectively, resulting in a LOW output. The HIGH signals from A2 and A3 are inverted to present LOWs at input pins 1 and 2, disabling ACIA-D and PIA-C.

Address line AØ (zone B8) is double inverted to the Register Select (RS) input of ACIA-D pin 11 (zone D5). When AØ is HIGH and ACIA-D is enabled, the Transmit/Receive Data Registers are selected. When AØ is LOW, the Control/Status Registers are selected. The Register Select of the PIAs operate differently from the RS of the ACIA. A1 (zone C8), which is double inverted, goes to pins 35 of PIAs C and B. If A1 is LOW, RS1 is LOW and Sections A of the parallel ports are selected. If A1 is HIGH, RS1 is HIGH and Secitons B of the PIAs are selected.

RSØ determines between Control/Status and Data-Data Direction Channels. Address line AØ is inverted and tied to RSØ, pins 36 of PIAs C and B. If RSØ is HIGH (AØ = LOW), the Control/Status Channel of the section determined by RS1 is selected. If RSØ is LOW (AØ = HIGH), the Data-Data Direction Channels of the section determined by RS1 is selected.

The MPU R/W signal is tied directly to the R/W line of each port, pin 13 of ACIA-D and pins 21 of PIAs C and B. The R/W signal determines the direction of data flow. If R/W is HIGH, each of the ports is in the Read mode. If R/W is LOW, they are in the Write mode.

The Ø2 clock signal goes directly to ENABLE on each of the ports, pin 14 of ACIA-D and pins 25 of PIAs C and B.

The bidirectional data lines, DØ through D7 on each port, are tied directly to the system data bus.

To control the rate of data flow in and out of ACIA-D, a baud rate generator is used. IC-A (zone D7) is a Programmable Bit Rate Generator, implementing a 2.4576 MHz crystal. The output of A pin 10 drives the Receive (RX) and Transmit (TX) clock inputs of ACIA-D pins 3 and 4 (zone D5).

The $\overline{\text{IRQ}}$ output of the ACIA, pin 7 (zone C5), and the PIAs, pins 37 and 38, are tied directly to the $\overline{\text{IRQ}}$ input of the MPU. The $\overline{\text{IRQ}}$ output of each port is an active LOW and is used to interrupt the MPU. This signal remains LOW as long as the cause of the interrupt is present and the appropriate interrupt ENABLE is set within the I/O ports.

The parallel data lines (PAØ through PA7 and PBØ through PB7) and control lines (CA1, CA2 and CB1, CB2) for PIAs C and B go directly to two 24-pin sockets, J3 and J4. Flat cable assemblies plug into these sockets and the 25-pin plug on the other side of the assembly is used for the I/O device.

ACIA-D has a Receive data (RX Data) input pin 2 (zone D5) and a Transmit data (TX Data) output pin 6 (zone C5). It also has Request To Send (RTS) output pin 5 (zone C5), $\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$) input pin 23 (zone C5), and $\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$) input pin 24 (zone C5). These inputs and outputs can be configured for TTY 20 milliamp current loop, RS-232, or TTL. These configurations are determined by the switch settings S1 and S6. Refer to Table 3-3, ACIA-D Interface Selection (page 3-10), for the desired configuration.

Table 3-3. ACIA-D Interface Selection

	TTY			RS-232			TTL		
	SWITCH PACKAGE	SWITCH NUMBER	SETTING A or B	SWITCH PACKAGE	SWITCH NUMBER	SETTING A or B	SWITCH PACKAGE	SWITCH NUMBER	SETTING A or B
TX DATA	S2	4	B	S1	3	B	S2	4	A
PIN 6	S2	1	B				S2	1	A
OUTPUT	S1	3	A				S1	3	A
RX DATA PIN 2 INPUT	S3	1	A	S3	1	B	S3	1	A
	S2	3	B	S1	2	B	S2	3	A
	S2	2	B				S2	2	A
	S1	2	A				S1	2	A
$\overline{\text{RTS}}$	S4	4	B	S4	4	A	S6	3	A
PIN 5	S6	3	B	S5	4	B	S5	4	A
OUTPUT	S5	4	A						
$\overline{\text{DCD}}$ * PIN 23 INPUT	S4	3	A	S4	3	A	S4	3	A
	S6	1	A	S6	1	B	S6	1	A
	S6	2	B	S5	3	B	S6	2	A
	S5	3	A				S5	3	A
$\overline{\text{CTS}}$ * PIN 24 INPUT	S4	2	A	S4	2	A	S4	2	A
	S3	3	A	S3	3	B	S3	3	A
	S3	2	B	S5	1	B	S3	2	A
	S5	1	A				S5	1	A

*NOTE: Whenever $\overline{\text{DCD}}$ input and $\overline{\text{CTS}}$ input are not used, S4-3 and S4-2 must be in the B positions for proper operation of the ACIA-D. Positioning S4-2 and S4-3 in the B position grounds these points (pins 23 and 24) of ACIA-D.

3-5. SERIAL I/O INTERFACE OPERATION

The following two circuit descriptions apply to all TTY interface circuits.

The transmit distributor contacts inside the Teletype input to J1 (10-pin miniature plug) pins 2 and 1 (sheet 3 of 3, zone B5). These contacts are normally closed and allow current flow through R4 and R1 (zone B6). A negative voltage results at the anode of diode D1 (zone B6), and D1 will not conduct. The input pin 11 of E (zone B7) goes LOW via resistor R5. The output of E pin 10 is HIGH, providing an off condition or "marking" state to the port. When the contacts open due to data transmission, the anode of diode D1 is pulled to +16 volts, and D1 conducts. The input of E pin 11 goes to approximately +4 volts via the divider resistors, R1 and R4. Capacitor C1 is used for contact debounce. Thus, the output of E pin 10 is LOW and represents a transmitted data bit to the RX Data line pin 2 of ACIA-D (sheet 2 of 3, zone D5).

The ACIA port output line, TX Data (sheet 2 of 3, zone D5, pin 6), is normally HIGH, causing a LOW at the base of Q2 (sheet 3 of 3, zone C6). The emitter of Q2 is pulled to approximately 1.2 volts through diodes D7 and D8 (zone C6). This forward biases Q2 to cause current flow through resistor R20, Q2, and the device. This is the "marking" state. When a data bit is transmitted, the base of Q2 goes HIGH via resistor R15 (zone C7), turning Q2 off. This provides a very high impedance at the device and represents a valid data bit. The signal connections from the 10-pin miniature plug (J1) to the TTY device are shown in Table 3-4.

	1	2	3	4	5	6	7	8	9	10
TTY	Receive (No Polarity)		* Transmit(+)	Clear To Send (No Polarity)	Blank	Clear To Send (No Polarity)	$\overline{\text{DCD}}$ (No Polarity)		* Request To Send (+)	Ground

* The (+) side of Transmit and Request To Send is the collector of corresponding transistors.

Table 3-4.
Signal Connections
10-Pin Plug (J1) to TTY Device

Figure 3-A illustrates the normal interconnections between the Universal I/O Board and a full duplex, 20 milliamp current-loop Teletype (KSR33 or ASR33).

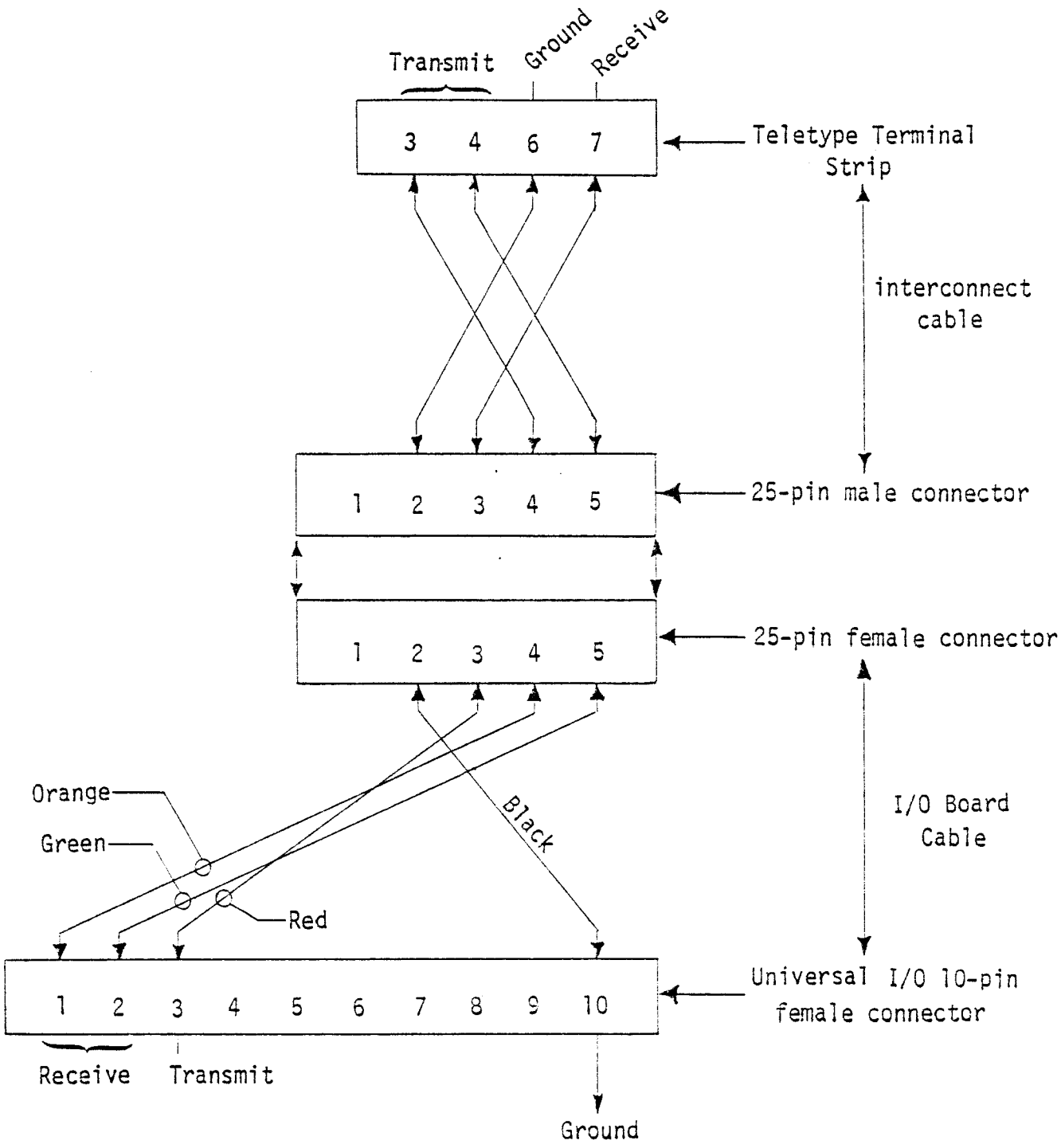


Figure 3-A. Normal Interconnections Between Universal I/O Board and TTY

The following circuit description apply to all RS-232 input and output circuits.

Whenever a logic one (approximately +16 volts) is received from the RS-232 device at the input of the ACIA, RX Data (sheet 2 of 3, zone D5, pin 2), R3 limits the current. D2 (sheet 3 of 3, zone B7) keeps the input of E pin 11 LOW and a TTL HIGH is present at the output of E pin 10 (zone B7). If a logic Ø (approximately +5 volts) is received from the RS-232 device, R3 again limits the current and D2 is reversed biased. The input of E pin 11 is HIGH and the output pin 10 is LOW.

Whenever a logic one is transmitted, transistor Q1 (zone D6) is reversed biased and a -16 volt level appears on the output line. If a logic Ø is transmitted, Q1 will conduct and approximately +5 volts is present on the output. Table 3-5 contains the signal connections for the 10-pin miniature plug (J1) to the RS-232 or TTL device.

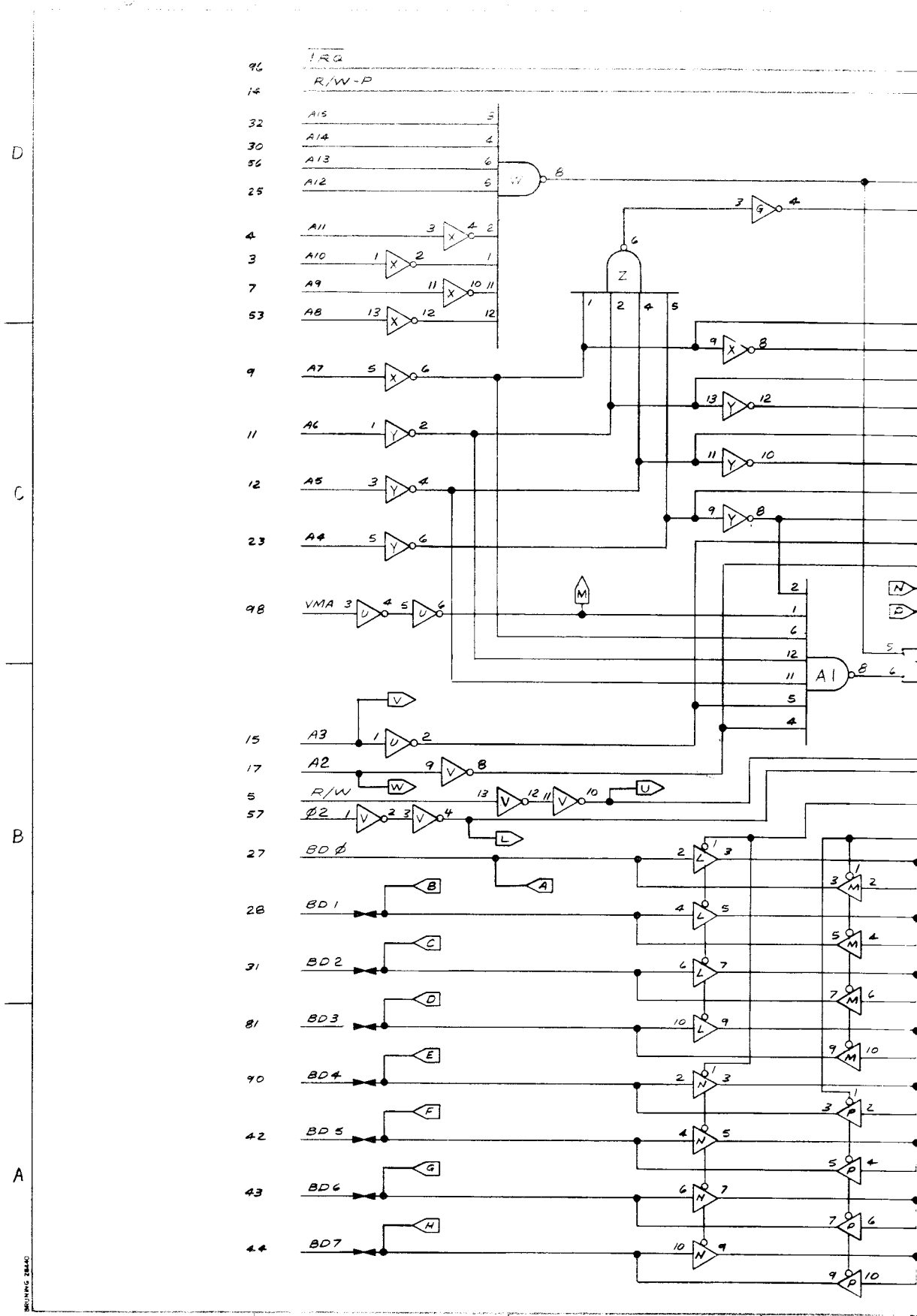
	1	2	3	4	5	6	7	8	9	10
RS-232 and TTL		Receive	Transmit		Blank	Clear To Send		$\overline{DCD}$	Request To Send	Ground
Wire Color		orange	red			green		brown	yellow	black

Table 3-5.
Signal Connections
10-Pin Plug (J1) to RS-232 or TTL Device

The normal interconnections for wiring compatability between the Universal I/O Board and an RS-232 or TTL device are indicated in Table 3-6.

SIGNAL DESCRIPTION	WIRE COLOR	DB-25 PIN NUMBERS
Receive	orange	2
Request To Send	yellow	4
Clear To Send	green	5
Transmit	red	3
$\overline{\text{DCD}}$	brown	8
Signal Ground	black	7

Table 3-6.
Normal Interconnections
Universal I/O Board to RS-232 or TTL


!IRQ
R/W-P
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
VMA
A3
A2
R/W
Ø2
BD Ø
BD 1
BD 2
BD 3
BD 4
BD 5
BD 6
BD 7
96
14
32
30
56
25
4
3
7
53
9
11
12
23
98
15
17
5
57
27
28
31
81
90
42
43
44
D
C
B
A
8
7
5

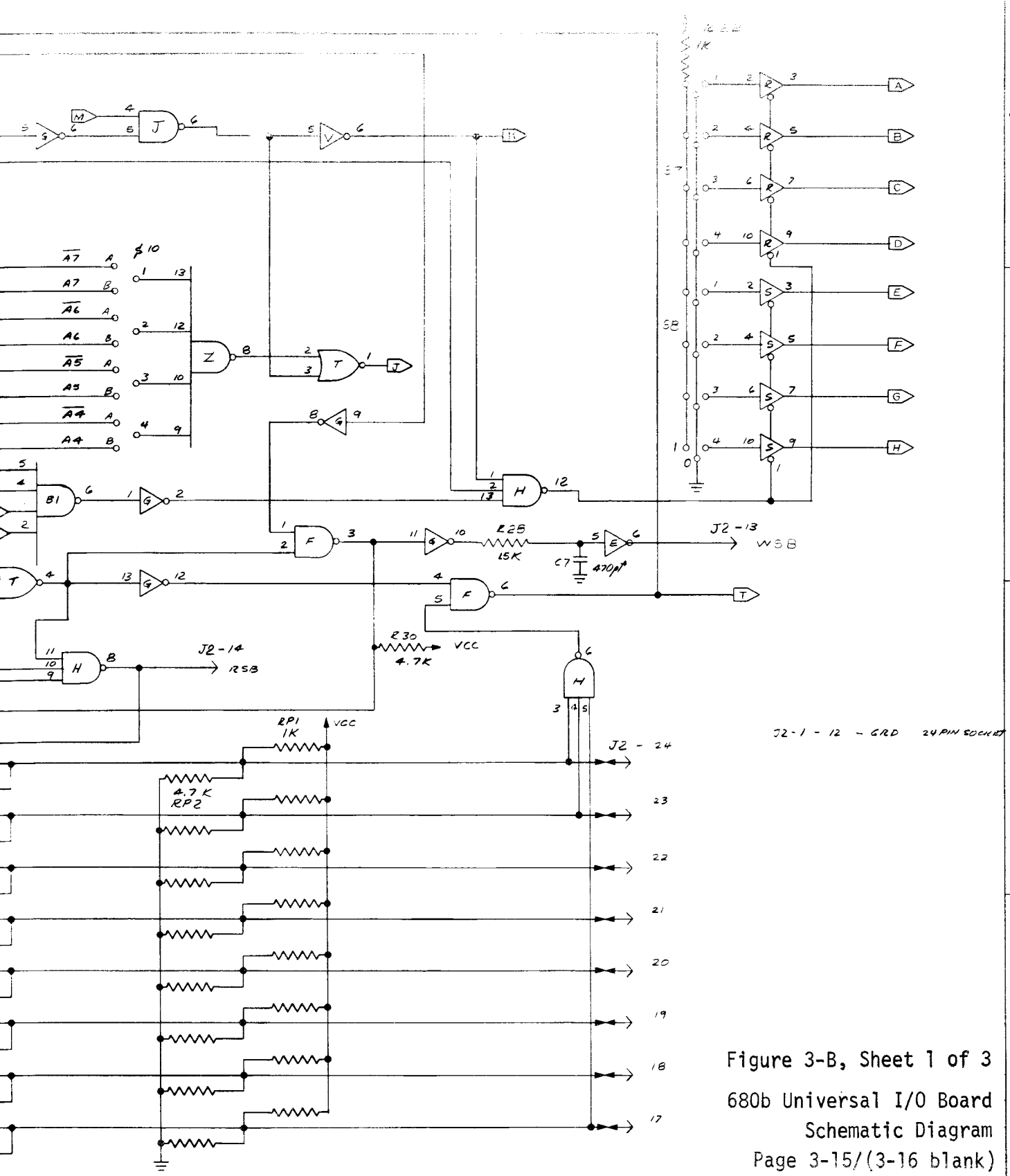
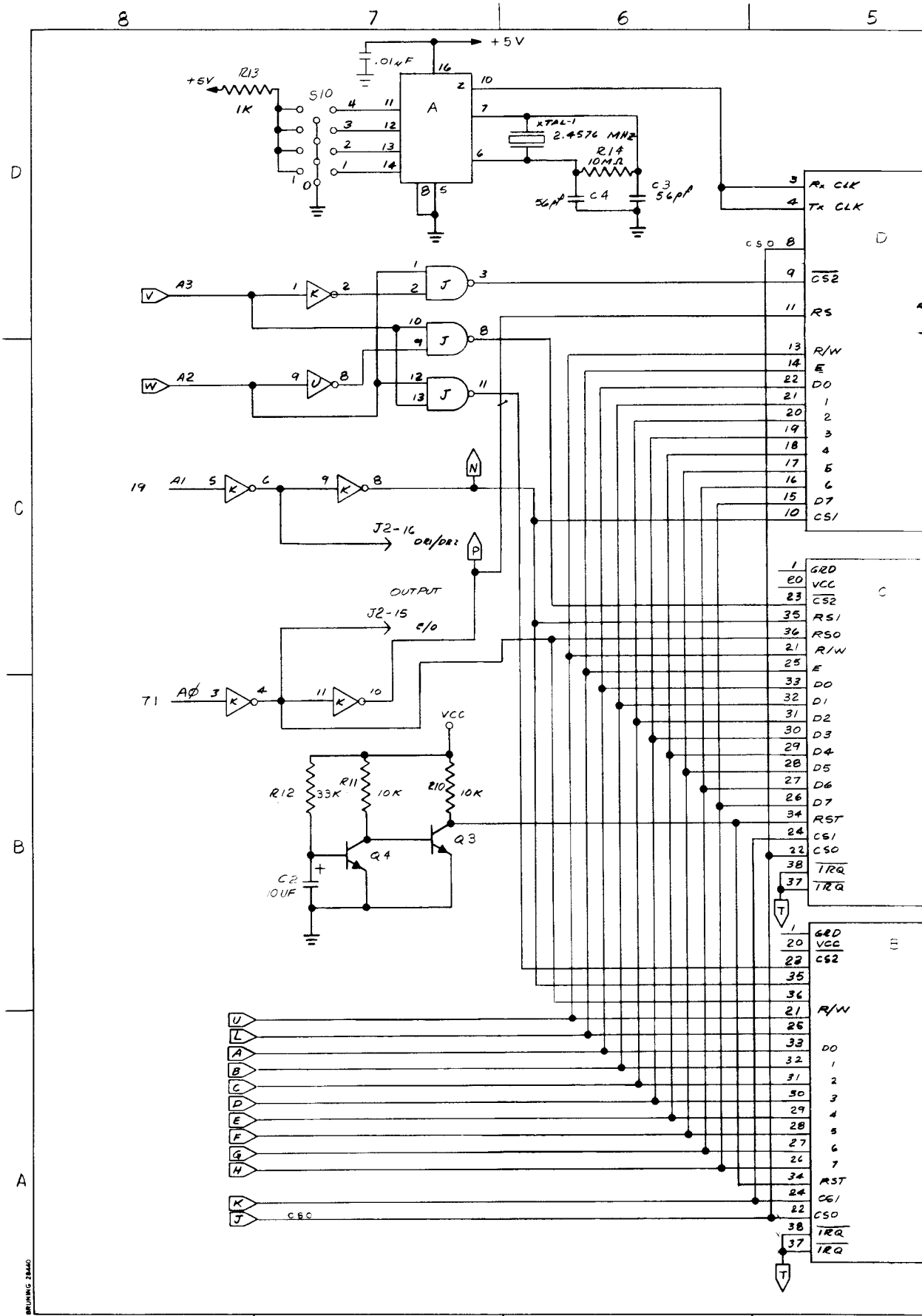


Figure 3-B, Sheet 1 of 3

680b Universal I/O Board
Schematic Diagram
Page 3-15/(3-16 blank)


8
7
6
5
D
C
B
A
+5V
.01μF
+5V
R13
1K
S10
A
XTAL-1
2.4576 MHz
R14
10MΩ
C4
56pF
C3
56pF
Rx CLK
Tx CLK
CSO
CS2
RS
R/W
E
DO
D1
D2
D3
D4
D5
D6
D7
CS1
A3
A2
A1
A0
J2-16
OUTPUT
J2-15
R12
33K
R11
10K
R10
10K
Q3
Q4
C2
10UF
VCC
GRD
RST
IRQ
U
L
A
B
C
D
E
F
G
H
K
J
CBC

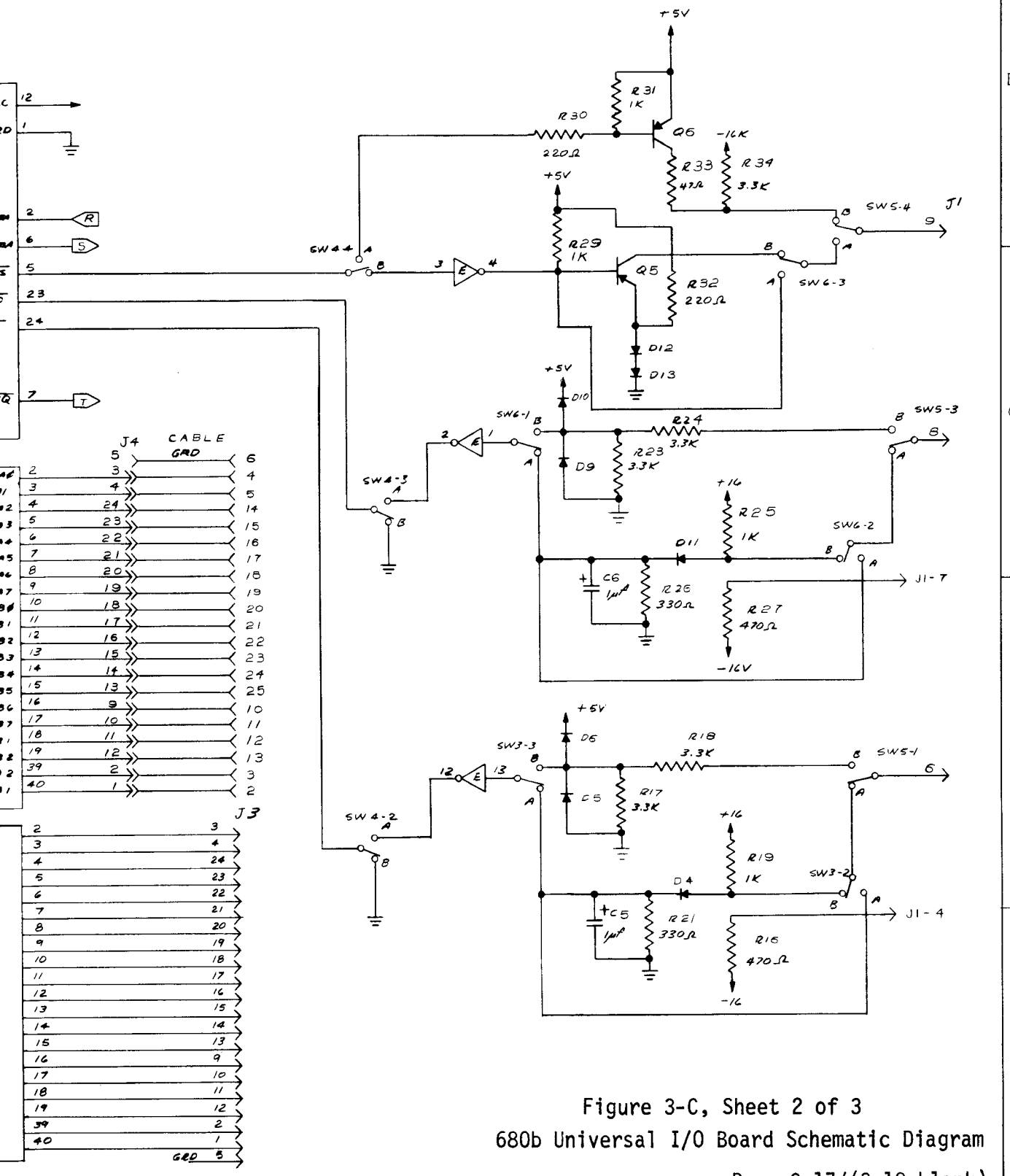
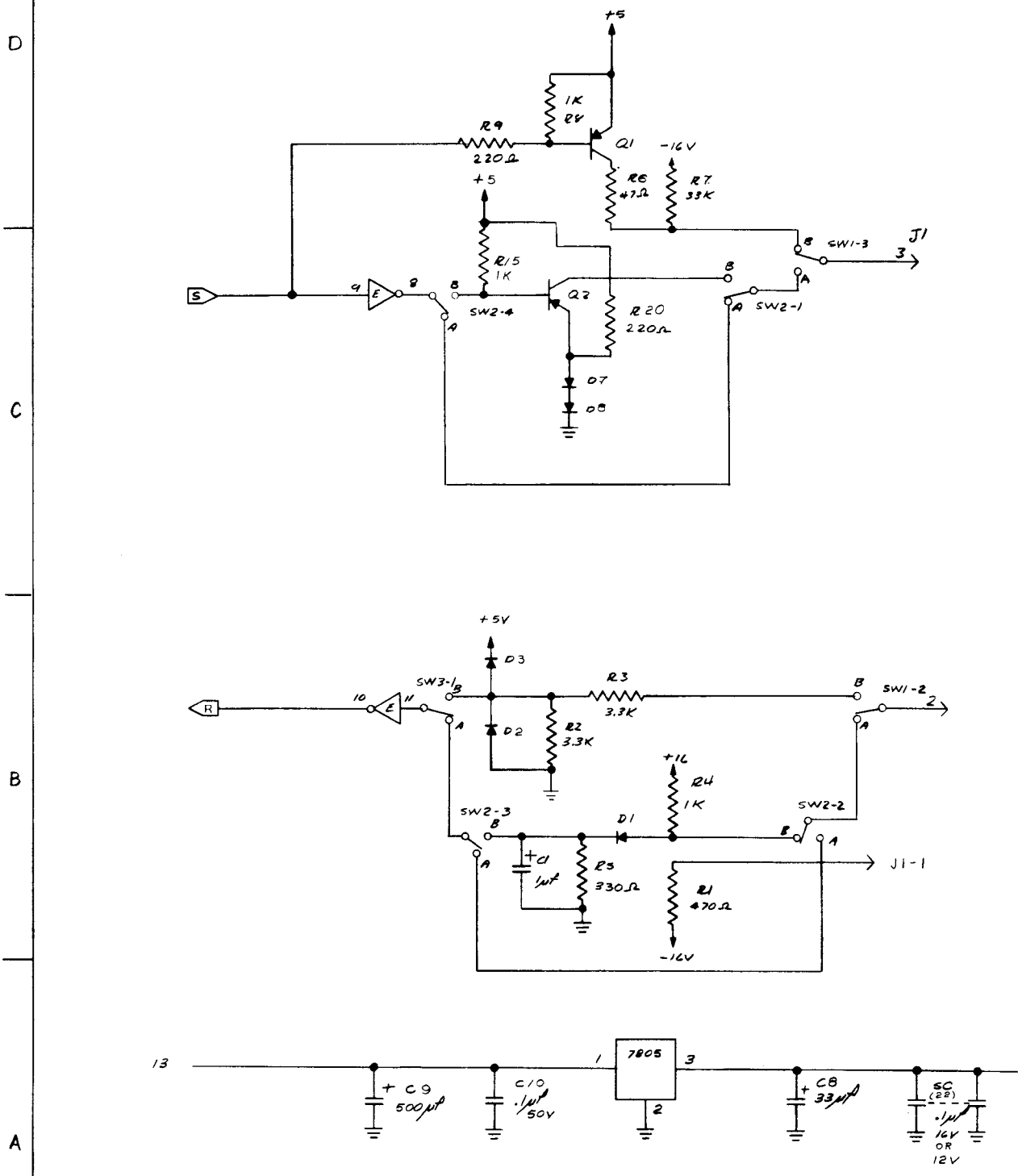


Figure 3-C, Sheet 2 of 3
680b Universal I/O Board Schematic Diagram


8
7
6
5
D
C
B
A
+5
1K
R4
R9
220Ω
Q1
-16V
R6
47Ω
R7
33K
+5
R15
1K
SW1-3
J1
3
S
9
E
8
8
SW2-4
A
Q2
R20
220Ω
B
A
SW2-1
D7
D8
+5V
D3
SW3-1
B
10
R
E
11
A
R3
3.3K
B
SW1-2
2
A
D2
R2
3.3K
+16
R4
1K
SW2-3
B
A
D1
SW2-2
B
A
J1-1
C1
1μF
R5
330Ω
R1
470Ω
-16V
13
+ C9
500μF
C10
.1μF
50V
1
7805
3
2
+ C8
33μF
SC
(22)
.1μF
16V
OR
12V
BRUNING 28440

REF DES.	TYPE	GRD	VCC	VDD	VBB
K, X, G, E, U V, Y	LS7404	7	14		
J	LS7400	7	14		
H	LS7410	7	14		
Z, B1	LS7420	7	14		
W, A1	LS7430	7	14		
T	LS7402	7	14		
F	LS7438	7	14		
P, R, S, L M, N	LS74367	8	16		
D	6850	1	12		
B, C	6820	1	20		
A	34702	8	16		

NOTE :

1. ALL RESISTORS 1/4W UNLESS OTHERWISE SPECIFIED

+5V

Figure 3-D, Sheet 3 of 3

680b Universal I/O Board Schematic Diagram

680b UNIVERSAL I/O

SECTION IV
INSTALLATION

4-1. INTRODUCTION

Before installing the 680b Universal I/O Board, refer to Section V, paragraph 5-2, and perform the visual checks. Make sure the 680-MB Expander Card is correctly installed according to the instructions enclosed with the card. The Universal I/O Board is connected to the expander card by means of a 100-pin edge connector and is installed horizontally above the 680b Main Board with two threaded standoffs. Install the 680b Universal I/O Board according to the following instructions.

4-2. Installation of 100-pin Edge Connector onto Expander Card (Figure 4-A)

1. Remove the expander card from the socket on the 680b Main Board.
2. Orient the 100-pin edge connector over the two rows of holes at the lowest unused position on the expander card.
3. Insert the connector pins into their respective holes. It may be necessary to guide some of the pins with the tip of a small screwdriver. Insure that the 100-pin connector is tight against the board and that all 100 pins are in their respective holes.
4. Secure the connector to the board with two #4-40 x 1/2" screws and two 4-40 nuts.
5. Solder each pin to the foil (bottom) side of the board. Insure that solder bridges are not formed.

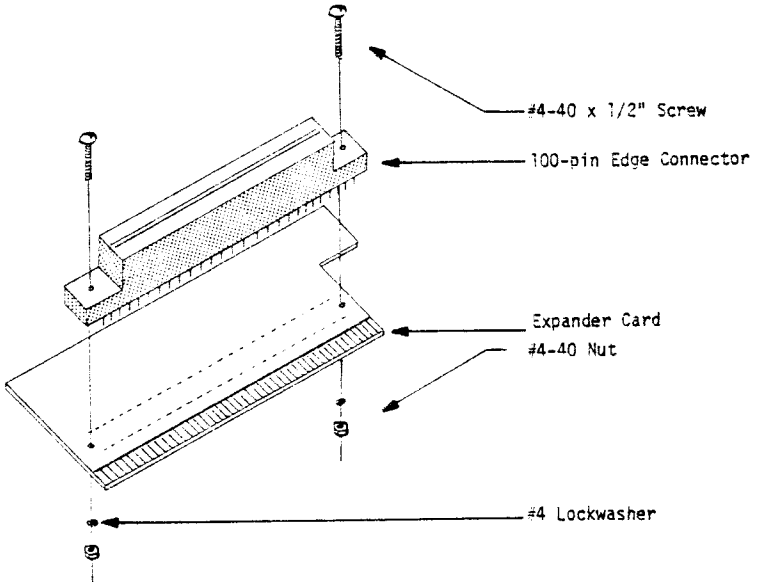


Figure 4-A. Installation of 100-pin Edge Connector onto Expander Card

4-3. Installation of Threaded Standoffs onto 680b Main Board (Figure 4-B)

> NOTE
>
> If this board is not being installed in the lowest position on the expander card, go to Paragraph 4-5.

1. Carefully remove the 680b Main Board from the case.
2. Referring to Figure 4-B, insert a #6-32 x 7/8" threaded standoff with three #6 lockwashers in the mounting hole provided on each side of the main board.
3. Secure each standoff from the foil (bottom) side of the board with a #6 lockwasher and a #6-32 nut.
4. Properly replace the 680b Main Board in the case as shown on pages 69-70 in the 680b Assembly Manual.

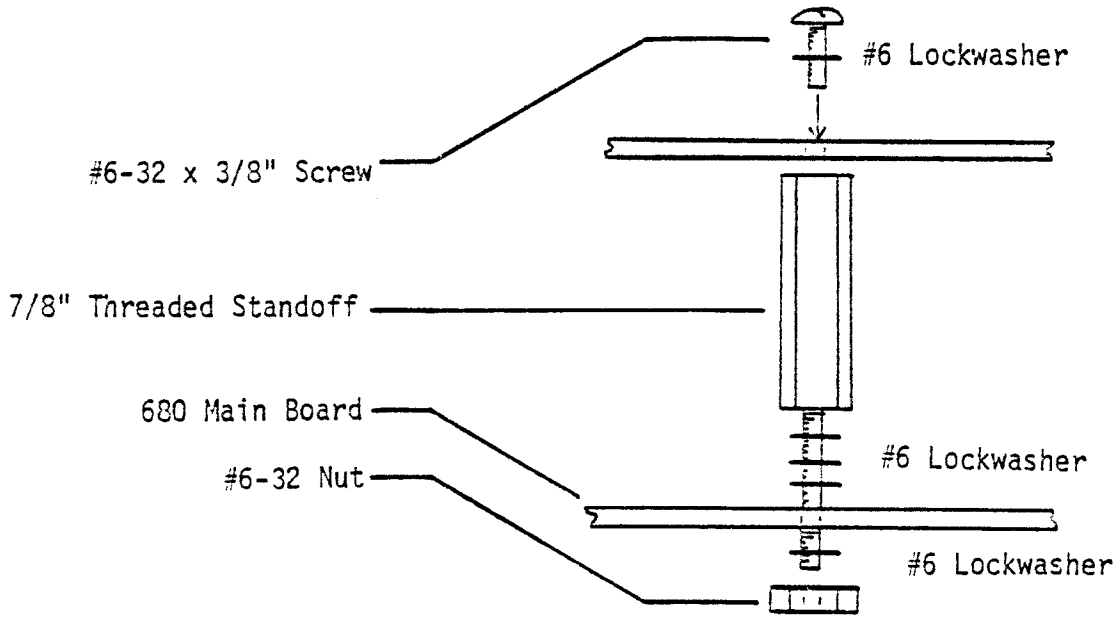


Figure 4-B. Installation of Threaded Standoffs onto 680b Main Board

4-4. Final Installation of the 680b Universal I/O Board

1. Replace the expander card into its socket on the 680b Main Board.
2. Insert the card stab connector of the Universal I/O Board (silk-screen side up) into the 100-pin edge connector on the expander card.
3. Secure the board in place by inserting a #6-32 x 3/8" screw with a #6 lockwasher into the top of each of the threaded standoffs as shown in Figure 4-B.

4-5. Installation of More Than One Board (Figure 4-C)

1. If this board is being installed in the second or third position above the 680b Main Board, follow the same procedure for installation of the 100-pin edge connector onto the expander card (Paragraph 4-2).
2. After installation of the 100-pin connector, reinstall the expander card and the lower board(s) into the 680b Main Board.
3. Replace both #6-32 x 7/8" screws and #6 lockwashers that previously secured the lower board with a #6-32 x 7/8" threaded standoff and a #6 lockwasher.
4. Insert the card stab connector of the Universal I/O Board (silk-screen side up) into the 100-pin edge connector.
5. Secure the Universal I/O Board in place with a #6-32 x 3/8" screw and a #6 lockwasher into the top of each of the threaded standoffs.

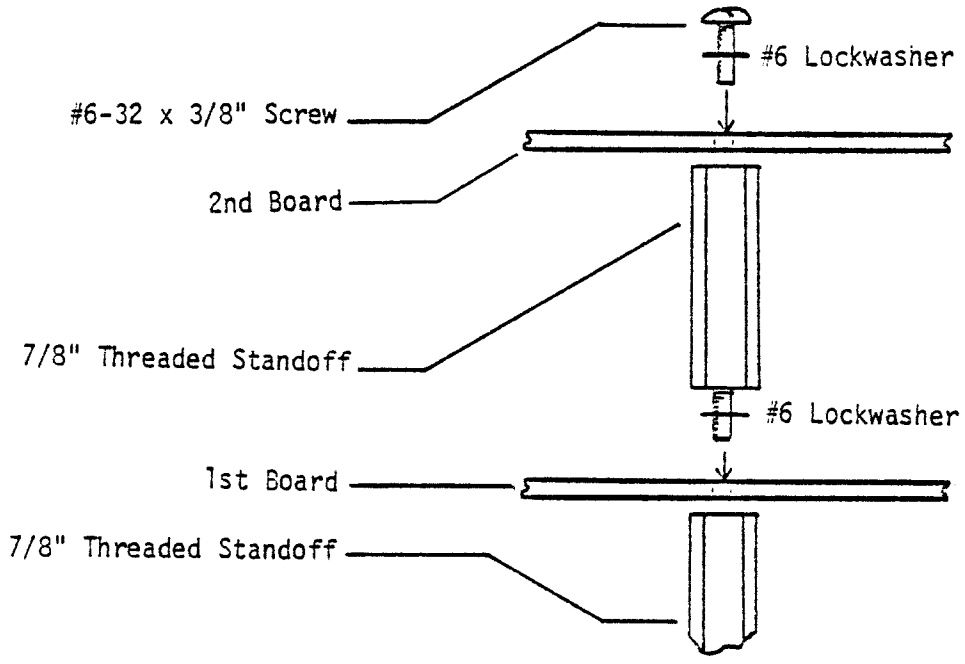


Figure 4-C. Installation of More Than One Board

4-6. Cable Assembly Installation

A 12-conductor round cable assembly is used for the ACIA serial port. Flat cable assemblies are supplied for the PIA parallel ports. Install each cable according to the following procedure.

1. Remove the metal plate with the two #4-40 x 3/8" screws from the 680b back panel slot.
2. Insert the cable(s) through the slot and plug into the appropriate board socket. Up to three flat cables and one round cable will fit through the slot. Refer to Figure 4-D, Cable Assembly Insertion.
   a. For proper orientation, insure that pin 1 of the cable connector is placed over the pin 1 position of the board socket. Refer to Figure 5-A, Silkscreen Diagram (page 5-2), for pin positions of sockets J1, J3, and J4.
   b. The round cable assembly plugs into the 10-pin socket, J1.
   c. The flat cable assembly plugs into the 24-pin socket, J3 or J4. The 25-pin plug on the other side of the assembly is used for the I/O device.

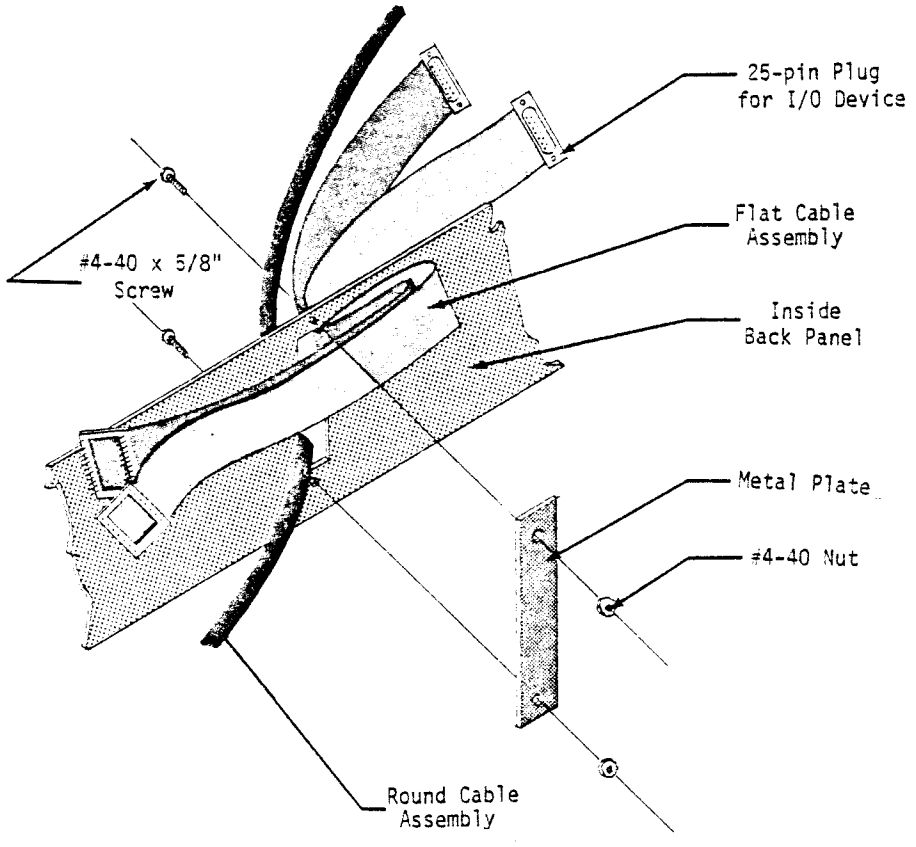


Figure 4-D. Cable Assembly Insertion

3. With the cable sockets properly inserted, fold the excess flat cable once against the back panel slot. Secure the cable(s) with the metal plate supplied with the 680b back panel and the two #4-40 x 5/8" screws supplied with the Universal I/O Board as shown in Figure 4-E.

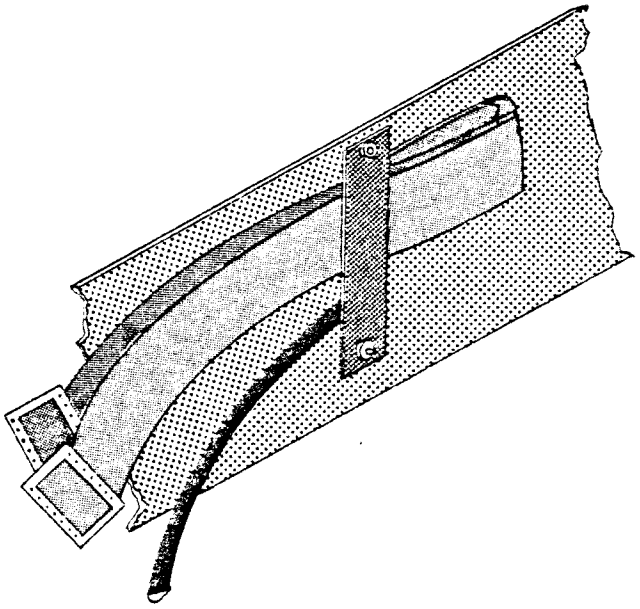


Figure 4-E. Final Cable Assembly Installation

4-7. "Burn-In" Procedure

When assembly and installation of the board have been completed, we recommend that a "burn-in" procedure (at least 48 hours long) be performed. Possible malfunctions due to improper assembly or component failure may occur at this time.

1. Turn the unit on and place the cover on the computer.
2. Leave the computer on for a period of 48 to 100 hours. If problems are encountered, refer to Section V (Troubleshooting) of the manual.

680b UNIVERSAL I/O

SECTION V
TROUBLESHOOTING

5-1. INTRODUCTION

Section V is designed to aid in the location of malfunctions that could be encountered after the Altair 680b Universal I/O Board is installed in the 680b computer. Before installation of the board, it should be visually inspected according to the visual inspection check list. A power supply check, preliminary check, and general procedures for troubleshooting TTL logic are included to insure that the board is functioning properly. Since the board is mainly software controlled, programs for troubleshooting the ACIA, PIAs and sense switches are presented to assist in the location of possible failures.

> WARNING
>
> Always disconnect power when removing the board, cutting or resoldering PC lands, and removing or installing ICs.

5-2. VISUAL INSPECTION CHECK LIST

Before the 680b Universal I/O Board is installed, it is important to check the component assembly, etching of lands, and switch settings. Although the board should be assembled correctly, an extensive inspection may eliminate possible malfunctions.

1. General

   Carefully examine the board for the following:

   a. leads that have not been soldered
   b. solder bridges
   c. cold solder connections
   d. errors such as hairline opens in lands

2. Component Check

   Using the silkscreen diagram (Figure 5-A, page 5-2) as a guide, check the following:

   a. proper polarity of capacitors
   b. proper polarity of diodes
   c. correct color codes on all resistors
   d. proper pin placement and good solder connections
   e. proper placement of all components

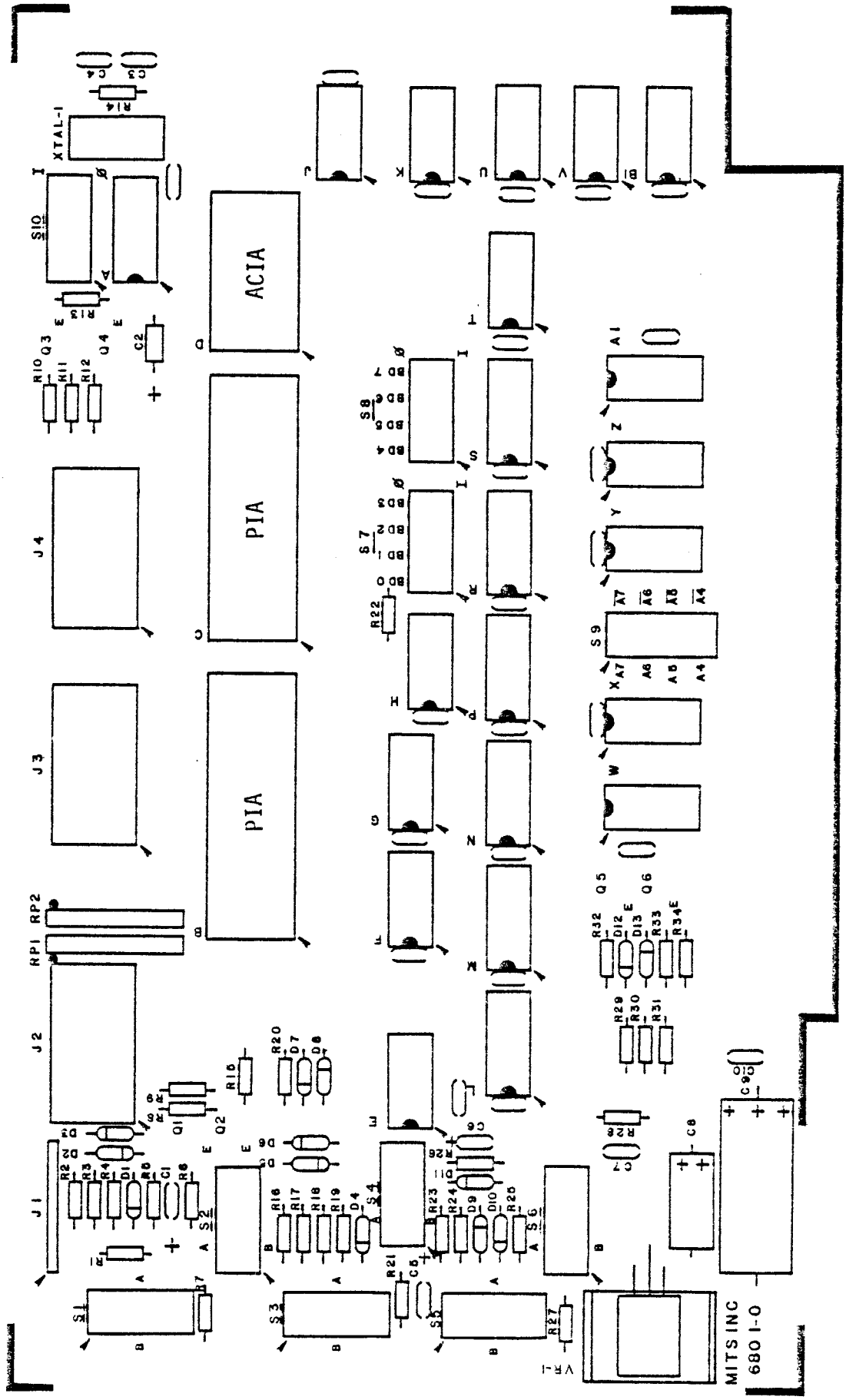


Figure 5-A. 680b Universal I/O Board Silkscreen Diagram

3. Address Switch Settings

   Check to see that all the switch settings are set according to needs.

   a. Refer to Table 3-2, S9 Address Selection (page 3-3), to insure that the board is strapped to the proper locations for the ACIA and the PIAs.
   b. Make sure that your program uses the correct addresses.
   c. If the ACIA serial interface is used, insure that the proper interface is selected on S1 through S6. Refer to Table 3-3, ACIA-D Interface Selection (page 3-10).

5-3. POWER SUPPLY CHECK

After installation of the Universal I/O Board, a power supply check is necessary to insure that the proper voltage levels are being supplied to the various ICs. Follow the instructions in Table 5-1 (page 5-9), Power Supply Check.

5-4. PRELIMINARY CHECK

Upon completion of the power supply check, leave the machine on and place it in the Halt mode to check the address and data lines for shorts and opens.

1. The 16 address switches on the 680b front panel should be in the down position initially. Place all the switches in the up position and observe that all the address LEDs are on. Return all the switches to the down position and observe that all the LEDs go off.
2. Next, place each switch in the up position individually. Observe that the corresponding LED is on. After all the switches are up, return them individually to the down position and each LED should go off.
3. Another way of checking each address line is by toggling each address switch individually and checking the signal toggle while tracing it through the logic.

4. The data lines, DØ through D7, are checked in the same manner. The data switches should be in the down position initially. Position all the data switches up and place the DEPOSIT switch up momentarily. Notice when the DEPOSIT switch is positioned, all data LEDs should be on. Return all the switches to the down position and observe that all LEDs are off.
5. Place each switch up individually while positioning the DEPOSIT switch up each time. Observe that the corresponding LED is on once the DEPOSIT switch is on. Return each switch to the down position and observe that the LED is off.
6. If one LED or several at the same time fail during the address or data line check, there are problems on the Universal I/O Board. Disconnect the power and remove the board. Perform a resistance check on the bus pins corresponding to the address or data lines showing the incorrect indications. If the resistance reading indicates there is a short or open in the circuit, trace the land from the bus until the problem is isolated.

5-5. GENERAL PROCEDURES FOR TROUBLESHOOTING TTL LOGIC

1. High level = logic 1 = 2 to 5 volts
   Low level = logic 0 = .8 to -.5 volts
2. Always work backward through the logic from the trouble area.
3. Always disconnect power when removing or installing ICs and when cutting or resoldering PC lands.
4. When a gate element appears bad (an output is opposite what it should be with a given input) check the following:
   a. Insure the IC package has correct voltage supplies and grounds.
   b. Recheck the output with the pin open (bend the pin up and reinsert the IC in its socket - if not socketed, cut the land that connects the pin to the external circuitry. If the output remains incorrect, replace the IC with a new part. If the output is now correct, look for shorts in nearby PC lands (visually and with an ohmmeter). If none are found,

the probable cause is a defective input at one of the elements that the output feeds. Isolate each input in turn by disconnecting it from the external circuitry.

c. If an input is between .8 volts and 2 volts, check continuity back to the driving output.

5-6. ACIA TROUBLESHOOTING

1. Since the 680b Universal I/O Board is mainly software controlled, possible failures may be due to software bugs. Program 5-I is for ACIA serial port echo.
   a. Be sure the board is strapped at the lowest position.
   b. Program 5-I may be changed for the particular terminal being used (refer to terminal manual). The program also works with TTY.
   c. Using the 680b monitor M and N commands, enter all underlined characters in Program 5-I.

Program 5-I. ACIA Serial Port Echo

.M	ØØØØ	86	.N	ØØØB	FØ	.N	ØØ16	57
.N	ØØØ1	03	.N	ØØØC	Ø6	.N	ØØ17	57
.N	ØØØ2	B7	.N	ØØØD	47	.N	ØØ18	24
.N	ØØØ3	FØ	.N	ØØØE	24	.N	ØØ19	F9
.N	ØØØ4	Ø6	.N	ØØØF	FA	.N	ØØ1A	B7
.N	ØØØ5	86	.N	ØØ1Ø	B6	.N	ØØ1B	FØ
.N	ØØØ6	B1*	.N	ØØ11	FØ	.N	ØØ1C	Ø7
.N	ØØØ7	B7	.N	ØØ12	Ø7	.N	ØØ1D	2Ø
.N	ØØØ8	FØ	.N	ØØ13	F6	.N	ØØ1E	EB
.N	ØØØ9	Ø6	.N	ØØ14	FØ	.J	ØØØØ	
.N	ØØØA	B6	.N	ØØ15	Ø6			

*NOTE: B1 sets up 8 data bits, 2 stop bits, Receive-Transmit interrupts enabled, and ÷ 16 mode.

d. If Program 5-I is not working, make sure the instructions were entered correctly. Also, inspect the switch settings. If the instructions and settings are correct, and the program is still not working, Halt the machine and check the address decoding logic.

2. To check the address decoding logic, tie VMA (IC-U, pin 3) to +5 volts with a clip and follow the instructions in Table 5-2 (page 5-10).

3. If a problem still exists after following Table 5-2, remove the VMA jumper and run the program while checking the RX and TX data line interfaces and associated interface components on the ACIA.
   a. With Program 5-I still entered, check the RX Data line (ACIA-D, pin 2). Observe that information is being received from the I/O device while entering characters on the device keyboard. If information is not coming from the I/O device, check through the RX Data interface circuitry to the back panel connector. Replace defective parts if necessary.
   b. Check the TX Data line (ACIA-D, pin 6) and associated interface components back to the I/O device.

5-7. PIA TROUBLESHOOTING

1. An echo program is also utilized to check the PIAs. Program 5-II is for PIA parallel port echo.
   a. Before Program 5-II is entered, the data and control lines must be shorted by making the following connections with a DB-25 pin male plug.

pin 2 - 13
pin 3 - 12
pin 4 - 20
pin 5 - 21
pin 10 - 18
pin 11 - 19
pin 14 - 22
pin 15 - 23
pin 16 - 24
pin 17 - 25

b. With these connections made, th PA data lines are shorted to the PB data lines. CA1 is tied to CB2 and CA2 is tied to CB1. The connections allow the parallel port echo program (Program 5-II) to be run by outputting data on the PB data lines and inputting data on the PA data lines.

c. Using the 680b monitor M and N commands, enter all underlined characters in Program 5-II.

Program 5-II. PIA Parallel Port Echo

.M	ØØØØ	4F	.N	ØØØD	0B or 0F	.N	ØØ1A	F0
.N	ØØØ1	B7	.N	ØØØE	86	.N	ØØ1B	0B or 0F
.N	ØØØ2	F0	.N	ØØØF	04	.N	ØØ1C	F1
.N	ØØØ3	08 or 0C	.N	ØØ1Ø	B7	.N	ØØ1D	F0
.N	ØØØ4	B7	.N	ØØ11	F0	.N	ØØ1E	09 or 0D
.N	ØØØ5	F0	.N	ØØ12	08 or 0C	.N	ØØ1F	27
.N	ØØØ6	09 or 0D	.N	ØØ13	B7	.N	ØØ2Ø	F5
.N	ØØØ7	B7	.N	ØØ14	F0	.N	ØØ21	7E
.N	ØØØ8	F0	.N	ØØ15	0A or 0E	.N	ØØ22	FF
.N	ØØØ9	0A or 0E	.N	ØØ16	BD	.N	ØØ23	AB
.N	ØØØA	43	.N	ØØ17	FF	.J	ØØØØ	
.N	ØØØB	B7	.N	ØØ18	00			
.N	ØØØC	F0	.N	ØØ19	F7			

d. The program should echo any character entered through the 680b Main Board ACIA. If there is an error whenever a character is entered, the program will jump back to the system monitor and print out a dot.

e. Halt the machine and follow the instructions in Table 5-3 (page 5-12). The table assumes the board is strapped at the lowest location. The VMA must be jumpered HIGH at pin 3 of IC-U.

5-8. SENSE SWITCHES

The sense switches (S7 and S8) are used to set a certain bit pattern and may be used several times during a program. Program 5-III is used to check the sense switches.

1. First, set a bit pattern on the sense switches.
2. Enter all underlined characters in Program 5-III. The program uses all ones to start.

Program 5-III. Sense Switch Check

```
.M  0000  B6
.N  0001  F0
.N  0002  03
.N  0003  B7
.N  0004  00*          *or any location
.N  0005  10*
.N  0006  7E
.N  0007  FF
.N  0008  AB
.J  0000
.M  0010  XX**         **should equal pattern
                         set on sense switches
```

3. When the program has run, the computer will return to the system monitor and print out a dot.
4. Examine location 0010 and observe the bit pattern. If the bit pattern does not match the pattern on the sense switches, refer to Table 5-4 (page 5-14).

Table 5-1. POWER SUPPLY CHECK

Step	Settings and Instructions	Correct Readings	If Incorrect
1	Check +9v UNREG at bus pin 13, +16v at bus pin 76, -16v UNREG at bus pin 72	Should be about +9v; +16v and -16v, respectively	Problem probably with input tramsformer (refer to 680b manual or 680b-MB)
2	Check +5v REG at output side of VR1 or check VCC on various ICs (pin 14 for 14-pin ICs and pin 16 for 16-pin ICs)	Should be a constant +5v with a ±5% tolerance	Check VR1 or check for possible shorts

Table 5-2. ACIA TROUBLESHOOTING

Step	Settings and Instructions	Correct Readings	If Incorrect
1	Address location set at F006 on address switches	CSØ = Logic 1 CS1 = Logic 1 $\overline{CS2}$ = Logic Ø	If CSØ = Logic Ø, go to Step 2 If CS1 = Logic Ø, go to Step 3 If $\overline{CS2}$ = Logic 1, go to Step 4
2	"	CSØ should equal a HIGH	Monitor pins 2 and 3 of IC-T (sheet 1 of 3, zone C4). Both pins should be LOW. If both pins are LOW, IC-T is probably defective. If pin 3 is HIGH, check input pins 4 and 5 of J (zone D4) for HIGHs. Pin 4 of J is HIGH when VMA was jumpered HIGH. If both pins are HIGH, J is probably defective. If pin 5 is LOW, check output pin 8 of W (zone D6). Pin 8 should be LOW and if it is LOW, replace IC-G (zone D5). If pin 8 of W is HIGH, check each input to W (zone D7). All inputs should be HIGH and if they are HIGH, IC-W is probably defective. If one of the input pins 1, 2, 11, and 12 are LOW, inverter X is probably at fault. If one of the input pins 3, 4, 5, and 6 are LOW, the problem lies between the address lines A15 through A12 on the MPU to the I/O Board. The problem could be on the 680b-MB.
3	"	CS1 should equal a HIGH	If CS1 is LOW and A1 is HIGH at the bus, check outputs to inverters K, pin 8 and pin 6 (sheet 2 of 3, zone C7).
4	"	$\overline{CS2}$ should equal a LOW	If $\overline{CS2}$ is HIGH, and input pins 1 and 2 of J (zone D7) are HIGH, then J is probably defective. If pin 2 is LOW, inverter K is probably defective. If pin 1 is LOW, the problem probably lies between A2 on the MPU and the I/O Board.

5	Toggle address switch AØ	RS (pin 11 of ACIA-D) should toggle along with AØ. AØ = RS	If RS (zone D5) does not toggle or toggles but is inverted from AØ, then IC-K (zone B7) is probably defective.
6	"	ENABLE pin 14 should be Ø2 clock (500 KHz). If it is correct, proceed to Step 7.	If Ø2 is missing, IC-V (sheet 1 of 3, zone B7) is probably defective.
7	"	R/W pin 13 (sheet 2 of 3, zone C5) is normally HIGH until deposit switch is actuated. Then it drops LOW for approximately 2.5 msecs. If correct, proceed to Step 8.	If signal is missing or inverted, IC-V (sheet 1 of 3, zone B6) is probably defective.
8	Deposit various bit patterns in memory	Data lines on ACIA-D (pins 22 through 15) should have the same pattern on them as the Data LEDs. If correct, proceed to Step 9.	If pattern differs, check the lines for shorts or opens.
9	Check pin 10 of IC-A	Baud Rate Clock frequency will be 16 times higher than the selected baud rate.	If clock is missing, IC-A (sheet 2 of 3, zone D7) or associated components are probably defective. If baud rate is incorrect, double check baud rate selected.

Table 5-3. PIA TROUBLESHOOTING

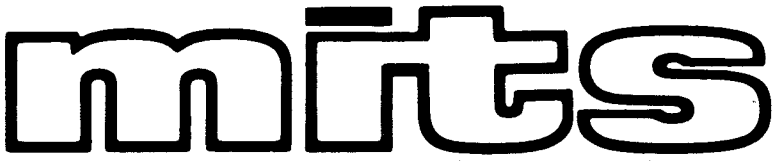
Step	Settings and Instructions	Correct Readings	If Incorrect
1	Set address location F008 for IC-C or F00C for IC-B.	CSØ = Logic 1 (F00C, IC-B) (F008, IC-C)	Monitor pins 2 and 3 of IC-T (sheet 1 of 3, zone C4). Both pins should be LOW. If both pins are LOW, IC-T is probably defective. If pin 3 is HIGH, check input pins 4 and 5 of J (zone D4) for HIGHs. Pin 4 of J is HIGH when VMA was jumpered HIGH. If both pins are HIGH, J is probably defective. If pin 5 is LOW, check output pin 8 of W (zone D6). Pin 8 should be LOW and if it is LOW, replace IC-G (zone D5). If pin 8 of W is HIGH, check each input to W (zone D7). All inputs should be HIGH and if they are HIGH, IC-W is probably defective. If one of the input pins 1, 2, 11, and 12 are LOW, inverter X is probably at fault. If one of the input pins 3, 4, 5, and 6 are LOW, the problem lies between the address lines A15 through A12 on the MPU to the I/O Board. The problem could be on the 680b-MB.
		CS1 = Logic 1 (F00C, IC-B) (F008, IC-C)	Trace the logic back to address lines A15 through A8 (sheet 1 of 3, zone D7) until malfunction is found.
		$\overline{CS2}$ = Logic Ø (F00B, IC-C) (F00C, IC-B)	Trace the logic back to input pins 12 and 13 of IC-J (sheet 2 of 3, zone C7) for HIGHs. If one is LOW, check corresponding address line A3 or A2. If pins 12 and 13 are HIGH, replace IC-J.
2	Same as Step 1 for F008 and F00C	RS1 = Logic Ø	If RS1 = Logic 1, IC-K pins 9 and 8 or 5 and 6 (sheet 2 of 3, zone C7) are defective or address line A1 is HIGH. If A1 switch is toggled, RS1 will change HIGH to LOW along with A1.

		RSØ = Logic 1	If RSØ = Logic Ø, IC-K pins 3 and 4 (sheet 2 of 3, zone C7) are probably defective or address line AØ is HIGH. If AØ switch is toggled, RSØ will be LOW when AØ is HIGH and HIGH when AØ is LOW.
3	Check ENABLE pins 25 of IC-B and IC-C	Ø2 clock (500KHz)	If missing, IC-V pins 1 and 2 and 3 and 4 (sheet 1 of 3, zone B7) are probably defective.
4	Check R/W line pins 21 of IC-B and IC-C	Normally HIGH until deposit switch is actuated and then it drops LOW. (See 680b manual for R/W timing)	If always LOW or always HIGH, IC-V pins 11, 10, and 13, 12 (sheet 1 of 3, zone B6) are probably defective.
5	Check Reset pins 34 of IC-B and IC-C	Should be +5 volts	If LOW, Q3 or Q4 (sheet 2 of 3, zone B7) are probably defective.
6	Deposit various bit patterns in memory	Data lines DØ through D7 (pins 33 through 26) should have the same bit pattern as shown on the Data LEDs	If pattern differs, check the lines for shorts or opens.

Table 5-4. SENSE SWITCHES

Step	Settings and Instructions	Correct Readings	If Incorrect
1	If Program 5-III was executed	Location ØØ1Ø would have FF stored there	If all or most bits are different, proceed to Step 2.
2	With VMA tied HIGH, set address location F003 on the address switches	Pin 1 of ICs R and S are LOW	If pins 1 of R and S (sheet 1 of 3, zones C2 and D2) are HIGH, check input pins 1, 2, and 13 of IC-H (zone C3). These pins should be HIGH and if they are HIGH, replace IC-H. If pin 1 is LOW, proceed to Step 3. If pin 2 is LIW, proceed to Step 4. If pin 3 is LOW, proceed to Step 5.
3	"	Pin 1 of H should be HIGH	If pin 1 is LOW, monitor inverter V pins 5 and 6 (sheet 1 of 3, zone D4). If pin 5 is LOW, replace V. If pin 5 is HIGH, check pins 5 and 4 of J (zone D4). Pin 4 should be HIGH when the VMA line was jumpered HIGH. If pin 5 is HIGH, replace J. If pin 5 is LOW, check pin 8 of W (zone D6). If pin 8 is LOW, replace IC-G (zone D5). If pin 8 is HIGH, check for a LOW input. All inputs should be HIGH. If all inputs of W are HIGH, replace IC-W. If one input is LOW, that line is at fault.
4	"	Pin 2 of H should be HIGH	If pin 2 of H (zone C3) is LOW, check output pin 6 of Z (zone D6). Pin 6 should be LOW. If it is LOW, replace IC-G. If it is HIGH, check for a LOW on one of the input pins 1, 2, 4, or 5. The LOW pin is at fault, thus the corresponding inverter is probably defective.

5	"	Pin 13 of H should be HIGH	If pin 13 is LOW, monitor output pin 6 of B1 (sheet 1 of 3, zone C5). If pin 6 is LOW, replace IC-G (zone C4). If pin 6 is HIGH, check input pins 5, 4, 2, and 1 of B1 (zone C5). All input pins of B1 should be HIGH. If one pin is LOW, the inverter on the pin is probably defective or the address lines are open or shorted.



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