altair™ 680b KCACR

DOCUMENTATION

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INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

This Altair 680b-KCACR (Kansas City Audio Cassette Recording) Documentation provides a general description of the 680b-KCACR printed circuit card and a detailed theory of operation. Troubleshooting information, assembly procedures and an operator's guide are also included in the documentation.

The manual contains five sections as follows:

1. Section I includes a general description of the 680b-KCACR operation, 680b-KCACR specifications, and KCACR accessories and options.
2. Section II contains 680b-KCACR general operating procedures, Machine Language operation and Altair CSAVE BASIC operation. User information is also provided for motor control and interrupt circuitry.
3. A detailed theory explanation of 680b-KCACR circuit operation is found in Section III.
4. Included in Section IV is troubleshooting information for the 680b-KCACR board.
5. Detailed assembly instructions for the 680b-KCACR are provided in Section V.

1-2. DESCRIPTION

The 680b-KCACR is designed to interface between the 680b bus and an audio cassette tape recorder for mass storage of data. Occupying one slot in the 680b bus, the KCACR circuitry uses the Kansas City Standard frequencies and format, making data transfers highly reliable under widely varying conditions. Other design features are no potentiometers or adjustments to circuitry, a digital demodulator, CMOS Logic providing low power consumption, a motor control circuit for starting and stopping tape motion, and the use of test points at key circuit areas. The 680b-KCACR operates at 300 baud with a +20, -20% playback speed tolerance with no adjustments. The software used with the KCACR is Altair 680 CSAVE BASIC, available on audio cassette tape.

1-3. ACCESSORIES AND OPTIONS

Altair 680 CSAVE BASIC is available on audio cassette tape. It includes the standard features of 680 BASIC, plus the capability of storing and loading data and programs through the 680b-KCACR. 680 CSAVE BASIC resides in the lower 8K of memory, making the system ideal for use of the 680b-BSM 16K Static Memory Card. A typical system implementing the 680b-KCACR includes a 680b Mainframe, 680b-BSM Memory Card, and perhaps a 680b-PCI for controlling external devices such as security systems, model railroads, etc. A useful option is the bootstrap loader PROM which allows quick initialization of BASIC without entering the loader program. The bootstrap loader fits into the 680b Main Board PROM socket.

1-4. 680b-KCACR SPECIFICATIONS

Frequencies used (self-clocking)

LOGIC 1 = 2400 Hz

LOGIC Ø = 1200 Hz

Data Rate: 300 baud (27 bytes/second)
36.67 ms. per byte (3.3 ms. per bit)

Data Format: One start bit--logic Ø
Eight data bits
Two stop bits--logic 1
(11 bits per byte)

Demodulator Playback Speed Tolerance: +20, -20% from recorded speed

Demodulator Input Levels (Playback): 300mv peak to peak minimum
(100mv RMS)
10v peak to peak maximum
(3.5v RMS)

Demodulator Input Impedance: 10K ohms

Modulator Output Level: 30mv P-P (suitable for microphone input)

Modulator Output Impedance: 1K ohms

Error Rate: Relative to quality of recorder and tape, typically less than 1 error in 10^6 bits READ with low noise audio tape.

Power Requirements: +8 volts unregulated - 220mA typical
-16 volts unregulated - 50mA typical (less than 3 watts total power)

Requires 1 slot in 680 bus.

Audio Cable Connectors: Mini phone jacks, 3.5mm diameter mounted on back panel.

Address: FØ1Ø = Status; Control
FØ11 = Read data; Write data

KCACR

SECTION II
Operator's Guide

2-1. INTRODUCTION

The following information explains how to set up and use the 680b-KCACR with the 680b computer. Contained in this section are general operating procedures, machine language instructions, Altair CSAVE BASIC operation and motor control circuit operating instructions.

2-2. GENERAL OPERATING PROCEDURES

The 680b-KCACR Audio Recording Interface is designed to be used with any medium quality cassette tape recorder. Music quality recorders generally give better performance than smaller portable recorders. If a stereo recorder is used and tape interchange is desired, it is recommended that only the left channel be used to minimize phase shift due to differences in head alignment. Use only name brand low noise cassette tapes. Off brand and bargain pack tapes may have dropout or mechanical defects that could reduce reliability of data or damage your recorder.

It is recommended that when a recording is being made or a tape played back that only one cable be connected to the recorder at a time. If both PLAY IN and RECORD OUT cables are connected simultaneously between the recorder and the 680b KCACR, Read errors may be generated due to coupling of the signals inside the recorder.

If saving important programs or data on tape, make two recordings on the tape and be sure to remove the record interlock tabs on the back edge of the cassette after recording to prevent accidental erasure of the tape.

Keep recorders and tapes away from power transformers, fluorescent lamps, and other sources of electrical fields and noise, especially when recording or playing tapes.

IMPORTANT
If using the 680b-KCACR board with the 680b-UI/O board, remove IC A1 on the 680b-UI/O to prevent interference with the 680b-KCACR.

2-3. Recording Data on Tape

The proper connection for recording data on tape is from the "RECORD OUT" jack on the 680 to the "MIC" jack on your tape recorder. Most cassette tape recorders use a 3.5 mm or 1/8 inch diameter miniature phone jack similar to the type used on the KCACR, so a shielded audio cable with miniature phone plugs on each end is all that is required. A suitable cable is Radio Shack #42-2420.

Before data can be recorded on tape, an output program must be entered into the computer. Examples of output programs are the Write Test programs (Section IV, pages 79 and 82), the CSAVE function of Altair 680b CSAVE BASIC (page 26), or the Data Output program (page 13). Output programs can be stored on Read Only Memories (ROMs) to eliminate the process of entering them manually each time they are needed.

Once the computer has been set up to output data to the KCACR, start the recorder in the RECORD mode. Let the tape run at least 30 seconds if starting from the beginning of the tape, otherwise, 5 seconds minimum. After the tape recorder mechanism and electronics have stabilized, activate the computer to output data.

If your recorder has a turns counter, set it to zero at the beginning of the tape and note the readings at the start and end of the recording. This will make it much easier to locate the desired program on the tape.

It may be helpful to monitor the recording by listening with an earphone. While recording, plug an earphone into the "EXT SPKR" on "MONITOR" jack. Note that while data is being recorded, the tone is buzzing, indicating that data is modulating the tone. A steady tone indicates that no data is being recorded.

Most cassette tape recorders use automatic record level circuitry which simplifies recording since neither the volume or tone controls have any effect upon the signal. The KCACR is designed to operate with this type of recorder or may be used with manually adjusted record level circuits. If using a unit with a manually adjusted record level, set the control for maximum undistorted record level.

2-4. Playing in Data From Tape

The proper connection for playing in data from tape into the KCACR is from the "SPKR," "MONITOR" or "LINE OUT" jack of your tape recorder to the "PLAY IN" jack on the 680b. Use the Radio Shack cable or equivalent as described in Paragraph 2-3.

Before data can be loaded into the computer, an input or load program must be entered into the computer. Examples of input programs are the Read Test programs (Section IV, pages 80 and 83), the CLOAD function of Altair 680b CSAVE BASIC (page 27), the Loader program (page 19) or the BASIC Bootstrap Loader (page 25). These programs may be put on Read Only Memories (ROMs) to eliminate the process of entering them manually each time they are needed.

Once the computer has been set up to load data from the tape, cue the tape to a point about 5 to 10 seconds before the desired data begins. Start the tape recorder in the run (PLAY) mode and activate the input program.

The volume control should be at least 1/3 volume, with maximum volume preferable. The tone control should also be set at maximum.

2-5. MACHINE LANGUAGE OPERATION

Paragraphs 2-6 and 2-7 include the requirements for operating the 680b-KCACR at a machine language level. Paragraph 2-8 contains sample I/O programs for storing and retrieving data.

2-6. KCACR I/O Address Chart

	ADDRESS		
	HEX	DECIMAL	OCTAL
Status (Load) Control (Store)	FØ1Ø	61456	36Ø,Ø2Ø
Read Data (Load) Write Data (Store)	FØ11	61457	36Ø,Ø21

2-7. Status + Control Bit Designations

STATUS BITS (Load from even address - FØ1Ø)

Note: True = Logic Ø, False = Logic 1

BIT	FUNCTION
DØ	Read Data Available
D1-D6	Not Used
D7	Transmit Buffer Empty

CONTROL BITS (Store to even address - FØ1Ø)

Note: True = Logic Ø, False = Logic 1

BIT	FUNCTION
DØ	Read Interrupt Enable
D1	Write Interrupt Enable
D2-D5	Not Used
D6	Remote Motor Off
D7	Remote Motor On

2-8. Machine Language I/O Programs

Output (Punch) Program

Program 2-I is used to output data to the KCACR from memory locations as specified by the user.

Since this program uses the monitor to take care of housekeeping, do not use any area of memory under Ø1ØØ HEX for your programs.

Execution of this program starts at 3ØØC. After the user enters the starting and stopping address of data to be saved, the data is output to the KCACR. See the operating instructions for the procedures to record data on tape (Paragraph 2-3).

Program 2-I. Output (Punch)

Octal Address	Octal Instruction	Hexadecimal Address	Hexadecimal Instruction				
0000	015	3ØØØ	ØD	FORM:	FCB	^O15,	
0001	012	1	ØA		FCB	^O12,	
0002	000	2	ØØ		FCB	Ø,	
0003	000	3	ØØ		FCB	Ø,	
0004	123	4	A3		FCC	/S/	
0005	061	5	31		FCC	/1/	
0006	377	6	FF		FCB	^O377,	
0007		7-8		BEGADR:	RMB	2,	;FIRST ADDR TO PUNCH
0011		9-A		LASADR:	RMB	2,	;LAST ADDR TO PUNCH
0013		B		NUMBYT:	RMB	1,	
0014	215	C	8D		BSR	GETADR,	;GET FIRST ADDR
0015	154	D	6C				
0016	377	E	FF		STX	BEGADR,	;STORE IT
0017	060	F	3Ø				
0020	007	3Ø1Ø	Ø7				
0021	215	1	8D		BSR	GETADR,	;GET LAST ADDR
0022	147	2	6E				
0023	377	3	FF		STX	LASADR,	;STORE IT
0024	060	4	3Ø				
0025	011	5	Ø9				
0026	215	6	8D		BSR	LEDTRL,	;PUNCH LEADER
0027	117	7	4F				
0030	316	8	CE	PPUN:	LDXI	FORM-1,	;POINT TO PUNCH FORMAT
0031	057	9	2F				
0032	377	A	FF				
0033	010	B	Ø4	PUNØ:	INX		
0034	346	C	E6		LDA	B,X,	
0035	000	D	ØØ				
0036	053	E	2B		BMI	PUN1,	;HIGH ORDER BIT SET - DONE
0037	004	F	Ø4				
0040	215	3Ø2Ø	8D		BSR	OUTDC,	;PUNCH CHARACTER
0041	166	1	76				
0042	040	2	2Ø		BRA	PUNØ,	
0043	367	3	F7				
0044	266	4	B6	PUN1:	LDA	A,LASADR+1,	;SUB LOW ORDER BYTES
0045	060	5	3Ø				
0046	012	6	ØA				

Octal		Hexadecimal	
Address	Instruction	Address	Instruction
0047	260	7	B0
0050	060	8	30
0051	010	9	08
0052	366	A	F6
0053	060	B	30
0054	011	C	09
0055	362	D	F2
0056	060	E	30
0057	007	F	07
0060	046	3030	26
0061	004	1	04
0062	201	2	81
0063	016	3	0E
0064	045	4	25
0065	002	5	02
0066	206	6	86
0067	015	7	0D
0070	267	8	B7
0071	060	9	30
0072	013	A	0B
0073	213	B	8B
0074	004	C	04
0075	215	D	8D
0076	107	E	47
0077	010	F	08
0100	215	3040	8D
0101	056	1	2E
0102	215	2	8D
0103	054	3	2C
0104	376	4	FE
0105	060	5	30
0106	007	6	07
0107	215	7	8D
0110	047	8	27
0111	172	9	7A
0112	060	A	30
0113	013	B	0B
0114	052	C	2A
0115	371	D	FA

```
        SUB     A,BEGADR+1,
        LDA     B,LASADR,       ;SUB HIGH ORDER BYTES
        SBC     B,BEGADR,
        BNE     PUN2,           ;LOTS MORE TO PUNCH
        CMPI    A,16,           ;LESS THAN 16 TO PUNCH?
        BCS     PUN3,
PUN2:   LDAI    A,15,           ;NO, SO PUNCH 16
PUN3:   STA     A,NUMBYT,       ;STORE #OF BYTES TO PUNCH-1
        ADDI    A,4,
        BSR     OUT2DC,         ;PUNCH BYTE COUNT
        INX                     ;POINT TO BEGADR
        BSR     PNCH2,          ;PUNCH ADDRESS
        BSR     PNCH2,
        LDX     BEGADR,         ;POINT TO DATA
PUN4:   BSR     PNCH2,          ;PUNCH DATA
        DEC     NUMBYT,         ;MORE TO PUNCH THIS RECORD?
        BPL     PUN4,
```

Octal		Hexadecimal	
Address	Instruction	Address	Instruction
0116	377	E	FF
0117	060	F	30
0120	007	3050	07
0121	103	1	43
0122	215	2	8D
0123	062	3	72
0124	011	4	0A
0125	274	5	BC
0126	060	6	30
0127	011	7	0A
0130	046	8	26
0131	276	9	BE
0132	306	A	C6
0133	123	B	53
0134	215	C	8D
0135	072	D	3A
0136	306	E	C6
0137	071	F	39
0140	215	3060	8D
0141	066	1	36
0142	215	2	8D
0143	003	3	03
0144	176	4	7E
0145	377	5	FF
0146	253	6	AB
0147	206	7	87
0150	050	8	28
0151	137	9	5F
0152	215	A	8D
0153	054	B	2C
0154	112	C	4A
0155	046	D	26
0156	373	E	FB
0157	071	F	39

```
                STX     BEGADR,         ;STORE NEW START ADDRESS

                COM     A,              ;FORM 1'S COMP OF CHECKSUM
                BSR     OUT2DC,         ;PUNCH CHECKSUM

                DEX                     ;ADJUST POINTER
                CPX     LASADR,         ;ARE WE DONE?

                BNE     PPUN,           ;NO, KEEP ON PUNCHING

                LDAI    B,"S",          ;YES, PUNCH EOF

                BSR     OUTDC,

                LDAI    B,"9",

                BSR     OUTDC,

                BSR     LEDTRL,         ;PUNCH TRAILER

                JMP     CRLF,           ;RETURN TO PROM MONITOR

;*
; SUBROUTINE TO PUNCH 50 NULLS
;*
LEDTRL: LDAI    A,50,

                CLR     B,
LED1:           BSR     OUTDC,          ;PUNCH A NULL

                DEC     A,
                BNE     LED1,           ;KEEP PUNCHING

                RTS                     ;RETURN TO CALLER
```

Octal Address	Octal Instruction	Hexadecimal Address	Hexadecimal Instruction
0160	346	3070	76
0161	000	1	00
0162	033	2	1B
0163	066	3	36
0164	027	4	17
0165	215	5	8D
0166	017	6	0F
0167	062	7	32
0170	010	8	08
0171	071	9	39
0172	275	A	BD
0173	377	B	FF
0174	202	C	82
0175	306	D	C6
0176	077	E	3F
0177	275	F	BD
0200	377	3080	FF
0201	201	1	81
0202	275	2	BD
0203	377	3	FF
0204	142	4	62
0205	071	5	39
0206	026	6	16
0207	124	7	54
0210	124	8	54
0211	124	9	54
0212	124	A	54
0213	215	B	8D
0214	001	C	01
0215	026	D	16
0216	304	E	C4
0217	017	F	0F
0220	313	3090	CB

```
;*
; PUNCH 2 HEX DIGITS POINTED
; TO BY X REG AND UPDATE CHECKSUM
;*
PNCH2:  LDA     B,X,            ;GET BYTE TO PUNCH

        ABA                     ;UPDATE CHECKSUM
        PSH     A,              ;SAVE CHECKSUM
        TBA                     ;COPY BYTE TO A
        BSR     OUT2DC,         ;PUNCH BYTE

        PUL     A,              ;RESTORE CHECKSUM
        INX                     ;BUMP BYTE POINTER
        RTS                     ;RETURN TO CALLER
;*
; READ ADDRESS FORM TTY INTO X REG
;*
GETADR: JSR     OUTS,           ;SEND SPACE

        LDAI    B,"?",          ;SEND QUESTION MARK

        JSR     OUTCH,

        JSR     BADDR,          ;GET ADDRESS

        RTS                     ;RETURN
OUT2DC: TAB
        LSR     B,
        LSR     B,
        LSR     B,
        LSR     B,
        BSR     OUTHR,

        TAB
OUTHR:  ANDI    B,^O17,

        ADDI    B,^O60,
```

Octal		Hexadecimal				
Address	Instruction	Address	Instruction			
0221	060	1	30			
0222	301	2	C1		CMPI	B,^071,
0223	071	3	39			
0224	043	4	23		BLS	OUTDC,
0225	002	5	02			
0226	313	6	CB		ADDI	B,7,
0227	007	7	07			
0230	067	8	37	OUTDC:	PSH	B,
0231	366	9	F6	OUTC1:	LDA	B,DCCS,
0232	360	A	F0			
0233	020	B	10			
0234	053	C	2B		BMI	OUTC1,
0235	373	D	FB			
0236	063	E	33		PUL	B,
0237	367	F	F7		STA	B,DCDA,
0240	360	30A0	F0			
0241	021	1	11			
0242	071	2	39		RTS	
0243				LASTWR::		
					END	

Input (Loader) Program

Program 2-II is used to load data into the 680b memory from the KCACR. The data must be in the same format as the Output program.

Execution of the Input program begins at location 3000. After data is properly loaded, the program returns control to the Monitor. If there is a problem with the data on tape, manually stop the Input program and reset the 680b in order to return program control to the Monitor.

The starting and stopping addresses of data stored in memory are determined when the program is output. When inputting data, the user has no control over the location where data is placed.

Program 2-II. Input (Loader)

Octal		Hexadecimal	
Address	Instruction	Address	Instruction
0000	215	3000	8D
0001	155	3001	6D
0002	300	2	C0
0003	123	3	53
0004	046	4	26
0005	372	5	FA
0006	215	6	8D
0007	147	7	67
0010	301	8	C1
0011	071	9	31
0012	047	A	27
0013	057	B	2F
0014	301	C	C1
0015	061	D	31
0016	046	E	26
0017	360	F	F0
0020	117	3010	4F
0021	215	1	8D
0022	102	2	42
0023	300	3	C0
0024	002	4	02
0025	327	5	D7
0026	371	6	F9
0027	215	7	8D
0030	113	8	4B
0031	215	9	8D
0032	072	A	3A
0033	172	B	7A
0034	000	C	00
0035	371	D	F9
0036	047	E	27
0037	011	F	09
0040	347	3020	E7
0041	000	1	00
0042	341	2	E1
0043	000	3	00
0044	046	4	26

```
$START::
LOAD:   BSR     INCH,           ;READ FRAME
        SUBI    B,"S",
        BNE     LOAD,           ;FIRST CHAR NOT (S)
        BSR     INCH,           ;READ FRAME
        CMPI    B,"9",
        BEQ     C1,             ;S9 END OF FILE
        CMPI    B,"1",
        BNE     LOAD,           ;SECOND CHAR NOT (1)
        CLR     A,              ;ZERO THE CHECKSUM
        BSR     BYTE,           ;READ BYTE
        SUBI    B,2,
        STA     B,BYTECT,       ;BYTE COUNT
        BSR     BADDR,          ;GET ADDRESS OF BLOCK
LOAD11: BSR     BYTE,           ;GET DATA BYTE
        DEC     BYTECT,         ;DECREMENT BYTE COUNT
        BEQ     LOAD15,         ;DONE WITH THIS BLOCK
        STA     B,X,            ;STORE DATA
        CMP     B,X,
        BNE     BADMEM,
```

Octal		Hexadecimal				
Address	Instruction	Address	Instruction			
0045	011	5	09	INX		;BUMP POINTER
0046	010	6	08	BRA	LOAD11,	;GO BACK FOR MORE
0047	040	7	20			
0050	360	8	F0	LOAD15:	INC A,	;INCREMENT CHECKSUM
0051	114	9	4C	LLOAD:	BEQ LOAD,	;ALL OK - IT'S ZERO
0052	047	A	27			
0053	324	B	D4		LDAI B,"C",	
0054	306	C	C6			
0055	103	D	43		SKIP2	
0056	214	E	8C	BADMEM:	LDAI B,"M",	
0057	306	F	C6			
0060	115	3030	4D		SKIP2	
0061	214	1	8C	NOTH:	LDAI B,"H",	
0062	306	2	C6			
0063	110	3	48		LDAI A,3,	
0064	206	4	C6			
0065	003	5	03	SEND:	JSR OUTCH,	
0066	275	6	BD			
0067	377	7	FF			
0070	201	8	81		BRA SEND,	
0071	040	9	20			
0072	373	A	FB	C1:	LDAI A,3,	
0073	206	B	86			
0074	003	C	03		JMP CRLF,	
0075	176	D	7E			
0076	377	E	FF			
0077	253	F	AB	INHEX:	BSR INCH,	;GET A CHARACTER
0100	215	3040	8D			
0101	055	1	2D		SUBI B,"0",	
0102	300	2	C0			
0103	060	3	30		BMI NOTH,	;NOT HEX
0104	053	4	2B			
0105	354	5	EC		CMPI B,11,	
0106	301	6	C1			
0107	011	7	09		BLE IN1HG,	;HEX
0110	057	8	2F			
0111	012	9	0A		CMPI B,21,	
0112	301	A	C1			
0113	021	B	11			

Octal Address	Octal Instruction	Hexadecimal Address	Hexadecimal Instruction				
0114	053	C	2B		BMI	NOTH,	;NOT HEX
0115	344	D	E4				
0116	301	E	C1		CMPI	B,26,	
0117	026	F	16				
0120	056	3050	2E		BGT	NOTH,	;NOT HEX
0121	340	1	E0				
0122	300	2	C0		SUBI	B,7,	;IT'S A LETTER-GET BCD
0123	007	3	07				
0124	071	4	39	INlHG:	RTS		;RETURN
				;*			
				; READ BYTE (2 HEX DIGITS)			
				; INTO B REG			
				; A IS USED FOR PAPER TAPE CHECKSUM			
				;*			
0125	215	5	8D	BYTE:	BSR	INHEX,	;GET FIRST HEX DIG
0126	351	6	E9				
0127	130	7	58		ASL	B,	;SHIFT TO HIGH ORDER 4 BITS
0130	130	8	58		ASL	B,	
0131	130	9	58		ASL	B,	
0132	130	A	58		ASL	B,	
0133	033	B	1B		ABA		;ADD TO CHEKSUM
0134	327	C	D7		STA	B,TEMP,	;STORE DIGIT
0135	370	D	F8				
0136	215	E	8D		BSR	INHEX,	;GET 2ND HEX DIG
0137	340	F	E0				
0140	033	3060	2B		ABA		;ADD TO CHECKSUM
0141	333	1	DB		ADD	B,TEMP,	;COMBINE DIGITS TO GET BYTE
0142	370	2	F8				
0143	071	3	39		RTS		;RETURN
				;*			
				; READ 16 BIT ADDRESS INTO X			
				; STORE SAME ADDRESS IN XHI & XLO			
				; CLOBBERS B REG			
				;*			
0144	215	4	8D	BADDR:	BSR	BYTE,	;GET HIGH ORDER ADDRESS
0145	357	5	EF				
0146	327	6	D7	STA	B,XHI,	;STORE IT	

Octal		Hexadecimal					
Address	Instruction	Address	Instruction				
0147	372	7	FA		BSR	BYTE,	;GET LOW ORDER ADDRESS
0150	215	8	8D				
0151	353	9	EB		STA	B,XLOW,	;STORE IT
0152	327	A	E7				
0153	373	B	FB		LDX	XHI,	;LOAD X WITH ADDRESS BUILT
0154	336	C	DE				
0155	372	D	FA		RTS		;RETURN
0156	071	E	39	INCH:	LDA	B,DCCS,	
0157	366	F	F6				
0160	360	3070	F0				
0161	020	1	10		ROR	B,	
0162	126	2	56		BCS	INCH,	
0163	045	3	25				
0164	372	4	FA		LDA	B,DCDA,	
0165	366	5	F6				
0166	360	6	F0				
0167	021	7	11		ANDI	B,177,	
0170	304	8	C4				
0171	177	9	EF		RTS		
0172	071	A	39	LASTWR::			
0173		B			END		

Below is listed the printout from the Hex Format KCACR Output Program paper tape. It is to be loaded through a paper tape reader by using the 680 monitor "L" command. If you make a paper tape from this listing, be sure to add a carriage return and line feed at the end of each line.

```
S10400F3FF09
S11330000D0A00005331FF00000000008D6CFF30FA
S1133010078D67FF30098D4FCE2FFF08E6002B0484
S11330208D7620F7B6300AB03008F63009F2300752
S1133030260481 0E2502860DB7300B8B048D4708BC
S11330408D2E8D2CFE30078D277A300B2AF9FF3018
S1133050074 38D3209BC300926BEC6538D3AC639A2
S11330608D368D037EFFAB86285F8D2C4A26FB3977
S1133070E6001B36178D0F320839BDFF82C63FBDEF
S1133080FF81BDFF623916545454548D0116C40F88
S1133090CB30C1392302CB0737F6F0102BFB33F7C3
S10730A0F0113900EE
S10400F30008
S9
```

Below is listed the printout from the Hex Format KCACR Loader Program paper tape. It is to be loaded through a paper tape reader by using the 680 monitor "L" command. If you make a paper tape from this listing, be sure to add a carriage return and line feed at the end of each line.

```
S10400F3FF09
S11330008D6DC05326FA8D67C139272FC13126F043
S11330104F8D42C002D7F98D4B8D3A7A00F92709BA
S1133020E700E10026090820F04C27D4C6438CC6EB
S11330304D8CC6488603BDFF8120FB86037EFFAB13
S11330408D2DC0302BECC1092F0AC1112BE4C11600
S11330502EE0C007398DE9585858581BD7F88DE031
S1133060 1BDBF8398DEFD7FA8DEBD7FBDEFA39F697
S10F3070F0105625FAF6F011C47F390068
S10400F30008
S9
```

2-9. Operation With Altair 680 CSAVE BASIC

Paragraphs 2-10 and 2-11 include the loading and operating requirements for using the 680b-KCACR with Altair 680 CSAVE BASIC.

2-10. Loading Altair 680 CSAVE BASIC

Using the 680 KCACR PROM

The procedure for loading 680 CSAVE BASIC using the 680 KCACR PROM is as follows:

a) Connect the computer and recorder and turn on the power (consult page 10 for correct connections and control settings).

b) Place the 680 BASIC cassette tape in the recorder and make sure it is completely rewound.

c) Type .J FDØØ (The underlined period is the Monitor's prompt.)

d) Start the tape recorder in the "PLAY" mode.

e) After approximately 9 minutes, control returns to the Monitor and a . (period) is printed, indicating BASIC is loaded. The tape recorder should be stopped.

f) Type .J ØØØØ to start BASIC. The initialization dialogue will now begin (consult BASIC manual).

NOTE
See error explanation at end of next section if difficulties are encountered.

Using the Bootstrap Loader Program

In the absence of the Loader PROM, BASIC may be loaded by entering a Bootstrap Loader Program with the Monitor's M and N commands and using it to load a checksum loader from the beginning of the BASIC tape. In this case, the following procedure is used:

a) Connect the computer and recorder and turn on the power (consult page 10 for correct connections and control settings).

b) Insert the 680 CSAVE BASIC cassette tape in the recorder and position it about 5 seconds before the leader pattern begins. The start of the leader pattern may be identified by listening to the tape and noting where the steady tone stops and the warbling tone begins.

c) Enter Program 2-III, starting at address 0000:

Program 2-III. Bootstrap Loader Program

Location	Data
0	C6
1	7F
2	8E
3	1F
4	FE
5	B6
6	F0
7	10
8	46
9	25
A	FA
B	B6
C	F0
D	11
E	11
F	27
10	F4
11	36
12	5A
13	26
14	F0
15	39

d) Start the tape recorder in the PLAY mode.

e) After approximately 10 seconds, type in .J ØØØØ to start the execution of the Bootstrap Loader.

The checksum loader on the BASIC tape is loaded into memory so that the last byte of the loader is just below 8K. Then control is transferred to the checksum loader to load BASIC.

If the loading is successful, the loader returns to the Monitor after approximately 9 minutes and the tape recorder may be stopped. To start BASIC, type:

.J ØØØØ

If an error is encountered in loading Motorola format tapes, the checksum loader in PROM or the one loaded with the bootstrap, prints the appropriate error character on the terminal. The error characters are as follows:

C	Checksum error
M	Memory error. An attempt was made to load into a non-existant or non-functioning memory location.
H	Hexadecimal character error. A character was encountered which was not a valid hexadecimal constant.

NOTE

The loader PROM does not print H when a nonvalid hexadecimal character is encountered, but treats it as an immediate checksum error, typing a C.

2-11. Using the 680b-KCACR With CSAVE and CLOAD

CSAVE

The CSAVE command saves a BASIC program on cassette tape. The format of CSAVE is as follows:

CSAVE <string expression> (For example, CSAVE "E")

The program currently in memory is saved on cassette tape under the name specified by the first character of the string expression. CSAVE can be given in direct or indirect mode. Before issuing the CSAVE command, position the tape in an appropriate spot and switch on the recorder to RECORD. String Expression is explained in Section 4 of the BASIC manual.

CSAVE outputs data to address FØ11 and expects the device status from address FØ1Ø. Modifications to the code of BASIC can be made to change these channel numbers.

When CSAVE is finished, execution continues with the next statement. BASIC's internal representation of the program in memory is written onto the tape. The amount of data written onto the tape is equal to the size of the program in memory plus seven bytes.

Variable values are not saved on the tape, nor are they affected by the CSAVE command. The number of nulls printed on the terminal at the start of each line has no effect on the CSAVE or CLOAD commands.

CLOAD

CLOAD reads a program from cassette tape and loads it. The format of CLOAD is as follows:

CLOAD <string expression>

The program on cassette tape designated by the first character of the string expression is loaded into memory. For example,

CLOAD"E"

BASIC inputs a byte from address FØ11 when the character ready flag comes up on FØ1Ø. When BASIC finds the program on the tape, it reads all characters received from the tape into memory until it finds three consecutive zeros which mark the end of the program. Then BASIC returns to command level and types "OK."

Statements given on the same line as a CLOAD command are ignored. The program on the cassette is not in checksum format, so the program must be checked to make sure it was read properly. The CLOAD? command is provided for this purpose.

(If BASIC does not return to command level and print "OK," it means either that BASIC found no file with the right filename character, or that the file did not end with three consecutive zeros.)

Stopping the computer and resetting it will prevent BASIC from searching forever. After reset, however, it is likely that no program is in memory or there is a partial program that contains errors. Typing NEW will always clear out the program that is in the machine at that time.

CLOAD Command

Once a program has been loaded from cassette into the computer's memory, the CLOAD? command checks it to make sure it has loaded properly. The format is as follows:

CLOAD? string expression

CLOAD? checks the program currently in memory byte for byte against the saved program with the name specified by the string expression. If there are any differences, BASIC will type "NO GOOD" and return to command level. If the two programs are the same, BASIC types "OK" and returns to command level. The CLOAD? command can also be used to see if a program that was just CSAVED was saved correctly. CLOAD? does not change the program in memory.

CSAVE* AND CLOAD*

Numeric arrays may be saved on cassette or loaded from cassette using CSAVE* and CLOAD*. The formats of the statements are as follows:

CSAVE* array name

and

CLOAD* array name

The array is written out in binary with four octal 210 header bytes to indicate the start of data. The number of bytes written is four plus 4 *(number of elements).

When an array is written out or read in, the elements of the array are written out with the leftmost subscript varying most quickly, the next leftmost second, etc. For example:

```
DIM A(10)
CSAVE*(A)
```

writes out A(0), A(1), . . . A(10)

```
DIM A(10,10)
CSAVE*A
```

writes out A(0,0),A(1,0), . . . A(10,10),A(10,1), . . . A(10,10)

Thus, it is possible to write out an array as a two dimensional array and read it back in as a single dimensional array, etc. String arrays cannot be saved or loaded by CSAVE* or CLOAD*. An attempt to do so causes a TM (type mismatch error).

2-12. USING THE MOTOR CONTROL CIRCUIT

Most portable cassette tape recorders are equipped with a "REMOTE" jack which allows the recorder's motor to be started and stopped externally. In order to control tape motion, the "PLAY" button must be depressed, and a subminiature phone plug (3/32 dia.) inserted into the "REMOTE" jack. If there is no connection between the two terminals of the phone plug, the motor stops. As soon as the terminals are connected together, as in a relay contact closure or switch closure, power is applied to the tape recorder's motor and tape motion begins.

2-13. Connection

To connect the 680b-KCACR motor control circuit to the tape recorder "REMOTE" jack, a relay with a 5 volt, 100 ohm minimum coil is required. An SPST, NO (Single Pole Single Throw, Normally Open) contact arrangement is recommended. Connect the relay coil across pin 6 (+5v) and pin 9 (relay coil driver - $\overline{MRD}$) of the 10 pin connector used for the KCACR. The normally open contacts of the relay are connected to the two terminals of the subminiature plug. Suggested parts are listed below:

Relay - ITT #PZSM - D1005
Magnecraft #W171DIP-1
Sigma #191TE1A1-5s

Subminiature Phone Plug -
Radio Shack #274-289

2-14. Machine Language Control

For machine language control, the following HEX programs should be used:

MOTOR ON

Address	Instruction	
N	86	Load Accum A immediate
N+1	7F	Bit D7 LOW (motor on)
N+2	B7	Store Accum A
N+3	F0	
N+4	10	At KCACR control channel address

MOTOR OFF

Address	Instruction	
N	86	Load Accum A immediate
N+1	BF	Bit D6 LOW (motor off)
N+2	B7	Store Accum A
N+3	F0	
N+4	10	At KCACR control channel address

2-15. Basic Control

For Altair 680 CSAVE BASIC, the motor may be activated with the following statement:

```
POKE 61456, 127
```

The motor may be turned off with the following statement:

```
POKE 61456, 191
```

2-16. Time Delays

It is recommended that when starting the tape recorder motor a timer program be used to delay activation of the I/O program to allow the tape recorder mechanism time to stabilize. Consult the general operating instructions for timing information.

2-17. USING INTERRUPTS

The 680b-KCACR has circuitry which allows interrupts to be generated when reading or writing data. Interrupts cause the 6800 MPU to stop what it is doing and service the interrupting device. The interrupts generated by the 680b-KCACR are a function of the Read Data Available status bit (Read Interrupt Enable) or the Transmit Buffer Empty status bit (Write Interrupt Enable).

For an explanation of interrupt utilization, Paragraphs 2-18 through 2-20 describe the sequence of events during a 680b-KCACR interrupt operation.

2-18. Interrupt System Operation

To use the Altair 680b interrupt system, all interrupts must be disabled to prevent improper operation. Next, the 6800 MPU must have its interrupt mask cleared by execution of the CLI instruction (ØE, hex) which enables maskable interrupts on the $\overline{IRQ}$ line.

One of the Interrupt Enable Latches must be set on the 680b-KCACR by outputting the correct bit pattern to address FØ1Ø (refer to Paragraph 2-19). When the corresponding status bit requesting data transfer is TRUE, the 680b $\overline{IRQ}$ line will be pulled LOW.

As soon as the MPU (microprocessing unit) finishes the current instruction, the interrupt request is acknowledged. The data in the MPU registers is then pushed into the stack, saving all current information and the interrupt mask is set HIGH, preventing any further interrupts. At this point, the MPU reads memory locations FFF8 and FFF9 which indicate the address of the interrupt servicing software. For the Altair 680b, the address is set at Ø1ØØ by the monitor PROM.

The interrupt servicing software, starting at address Ø1ØØ, typically consists of checking the 680b-KCACR status to verify that it is the interrupting device. Reading the status or the data channel or issuing a Motor Stop command will reset the Interrupt Enable Latches, turning the interrupt request off. After verification of the status, the data is then transferred and manipulated as required.

To return control to the original program before the interrupt was serviced, the MPU register data that was pushed onto the stack should be recalled back off the stack and into the MPU.

If further interrupts are required, the MPU interrupt mask bit is cleared and the 680b-KCACR interrupts are enabled as required. These two operations should be done before recalling data back from the stack.

2-19. 680b-KCACR Interrupt Control Bits

Table 2-A shows the addresses and bit patterns for controlling the interrupt latches on the 680b-KCACR.

Table 2-A. Address and Bit Patterns

INSTRUCTION	ADDRESS	DATA	FUNCTION
Machine (STA Language (or (STB	FØ1Ø	FE FD BF	Read Interrupt Enable Write Interrupt Enable Motor Off, Reset Interrupts
Altair 680 BASIC (Poke	61456	254 253 191	Read Interrupt Enable Write Interrupt Enable Motor off, Reset Interrupts

2-20. Sample Program

Program 2-IV is a Sample Program used to test the interrupt circuitry on the 680b-KCACR board. Figure 2-1 is the Flow Chart from which the program is generated.

Program 2-IV. KCACR Interrupt Test Program

```
.M 0000 0E      CLEAR INTERRUPT MASK BIT
.N 0001 86      ENABLE
.N 0002 FD      WRITE
.N 0003 E7      INTERRUPT
.N 0004 F0      OF KCACR
.N 0005 10
.N 0006 7E      JUMP TO SELF
.N 0007 00
.N 0008 06
.N 0100 BD      JSR
.N 0101 01      ACIA SUBROUTINE
.N 0102 1E
.N 0103 36      OUTPUT
.N 0104 0D      CARRIAGE
.N 0105 B7      RETURN
.N 0106 F0
.N 0107 01
.N 0108 BD      JSR
.N 0109 01      ACIA SUBROUTINE
.N 010A 1E
.N 010B 86      OUTPUT
.N 010C 0A      LINE
.N 010D B7      FEED
.N 010E F0
.N 010F 01
.N 0110 BD      JSR
.N 0111 01      ACIA SUBROUTINE
.N 0112 1E
.N 0113 86      OUTPUT
.N 0114 49      ASCII "I" TO TERMINAL
.N 0115 B7
.N 0116 F0
.N 0117 01
```

NOTE

0002
- FE ENABLES READ INT.
- BF CLEARS INT REQUEST FROM KCACR

```
.N 0118 B6 )   DISABLE
.N 0119 F0 }   KCACR (READ STATUS CHANNEL)
.N 011A 10 )   WRITE INTERRUPT
.N 011B 7E )
.N 011C FF }   JUMP TO
.N 011D AB )   MONITOR
.N 011E B6 )
.N 011F F0 |
.N 0120 00 |
.N 0121 46 |   ACIA STATUS
.N 0122 46 }   SUBROUTINE
.N 0123 24 |
.N 0124 F9 |
.N 0125 39 )
.
.J 0000
I
.
```

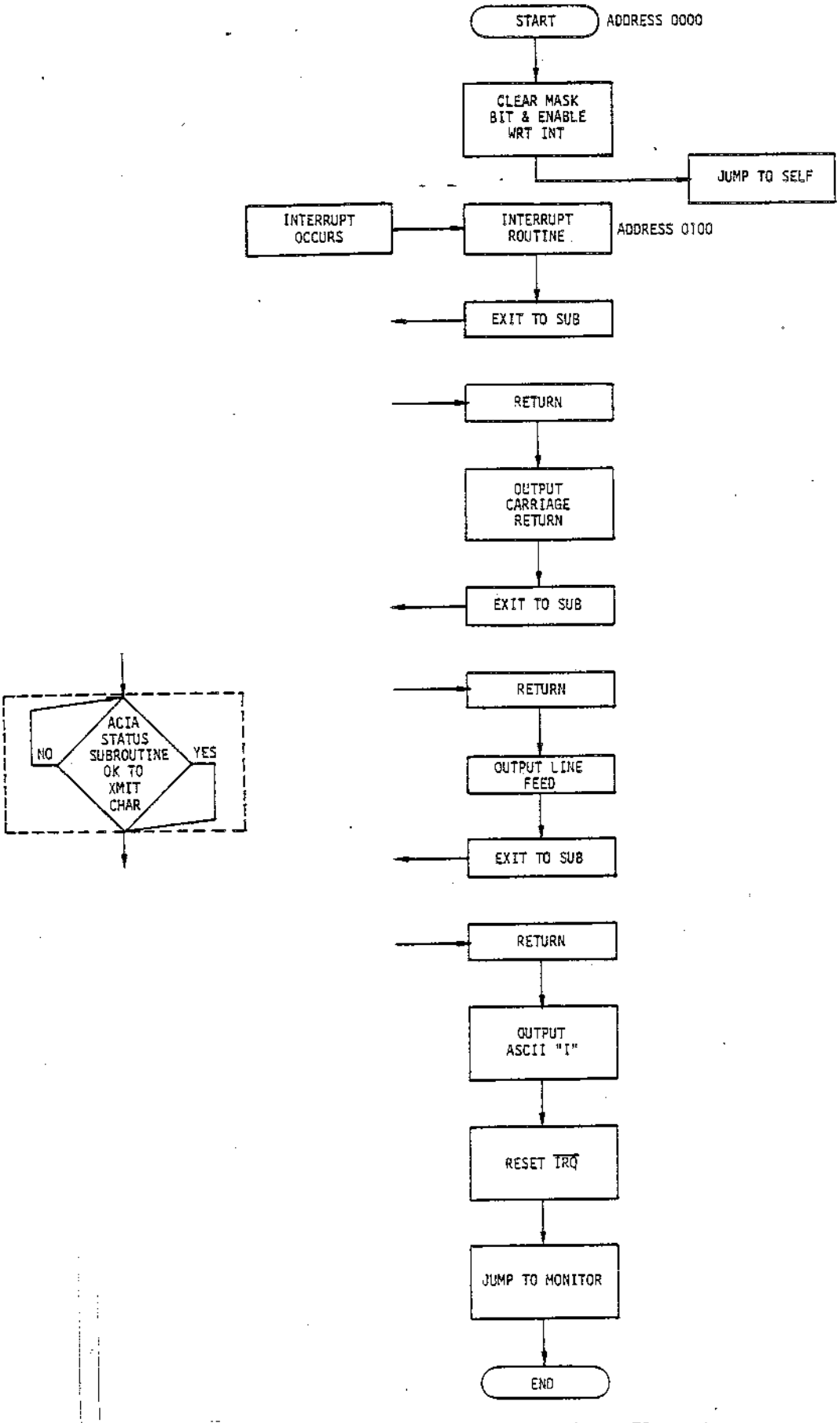


Figure 2-1. KCACR Interrupt Test Flow Chart

2-21. USING KCACR LOADER/PUNCH PROM

The KCACR Loader PROM is a program in read-only memory that loads programs from audio cassette tape through the 680b KCACR interface card. The PROM also contains a punch program that dumps memory between two specified locations onto audio cassette tape through the 680b-KCACR interface card. The KCACR PROM must be installed in socket V on the 680b main board to begin at location FDØØ (refer to page 17 of 680b Assembly Manual).

2-22. Punching (Saving) Data or Programs on Tape

The 680 KCACR PROM is used to record information on cassette tape in the Motorola format. The first and last addresses to be saved are specified by the user. These addresses are saved along with the data and are used to place the data in memory during loading (see Paragraph 2-23).

The procedure for using the KCACR PROM is as follows:

a) Connect the computer and tape recorder and turn the power on.

b) Insert the cassette tape in the recorder and set the tape to the desired recording position.

c) The program to be saved on tape should be in the computer.

d) Start the tape recorder in the RECORD mode.

e) Type .J FD74 (The underlined period is the Monitor's prompt.)

The KCACR PROM then requests the memory address (selected by the user) to start the dump by typing a ? . Type the starting memory address (4 Hex digits). The Monitor then responds with another ? asking for the ending memory address. Type the ending memory address (4 Hex digits). An invalid address causes a return to the Monitor.

After typing the last character of the ending memory address, the data is output to the tape recorder with an additional 50 nulls at the end. At this point, control is returned to the Monitor and the tape recorder should be stopped.

For example, the following command causes the KCACR PROM to dump memory between $Ø4ØØ_{hex}$ and $Ø5ØØ_{hex}$ to a tape recorder in the Motorola format.

.J FD74 ? Ø4ØØ ? Ø5ØØ (The underlined period and question marks are the Monitor's prompt.)

Memory dumps made in this manner are compatible with either the KCACR PROM Loader Program (see Paragraph 2-23) or the Loader Program listed on page 19.

> NOTE
>
> Do not try to punch the section of memory from $00D0_{16}$ to $00FF_{16}$ as this is the Monitor's and KCACR PROM's stack and work area. While punching a tape of this area will not cause any problems, loading the tape back into memory will. The usual result is a checksum error, but generally, the result is indeterminable.

2-23. Loading Tapes in Motorola Format

The program or data on tape that is to be loaded must be in the Motorola format, and end with an S9 record. Suitable format is provided by the PROM Punch Program (Paragraph 2-22) or the Output program listed on page 13. The locations of memory that the information on tape is to be placed is determined at the time of recording and cannot be changed easily. The following procedure should be used when loading with the 680 KCACR PROM:

a) Connect the computer and recorder, and turn the power on. Consult page 10 for the correct connections and control settings.
b) Insert the cassette tape in the recorder and position the tape about 5 to 10 seconds before the start of the desired data.
c) Type .J FDØØ
d) Start the tape recorder in the PLAY mode.
e) When the program is finished loading, control returns to the Monitor and the tape recorder may be stopped.

If an error is encountered in loading Motorola format tapes, the checksum loader in the PROM prints the appropriate error character on the terminal. The error characters are as follows:

C	Checksum or non-hexadecimal character error
M	Memory error. An attempt was made to load into a non-existant or non-functioning memory location.

KCACR

SECTION III
THEORY OF OPERATION

3-1. GENERAL

This section contains information needed to understand the operation of the 680b-KCACR board. Provided in this section is a fundamental description of the logic circuits used on the 680b-KCACR schematics, a paragraph on the Kansas City Standard Principles, and a general overview followed by a detailed theory of operation. Also provided are test point descriptions and waveforms.

3-2. SCHEMATIC REFERENCING

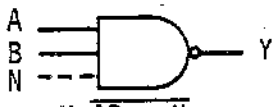
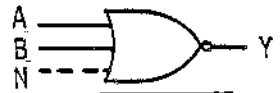
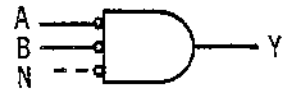
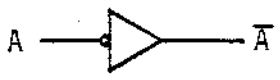
The detailed schematics are provided to aid in determining signal direction and tracing. A solid arrow (➡) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as a number-letter number (e.g. 2-A3), indicating sheet 2 and schematic zone A3.

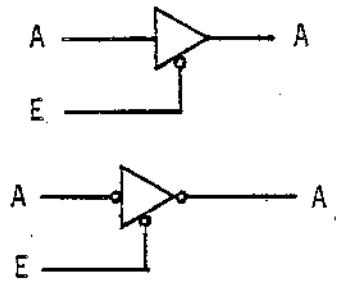
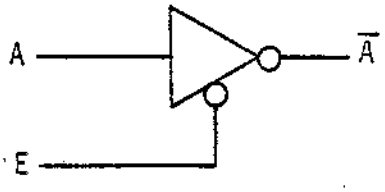
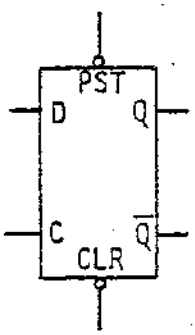
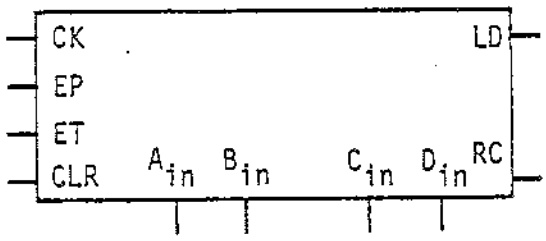
A bar over the signal description on the schematic indicates an active LOW. The absence of a bar over the signal description indicates an active HIGH.

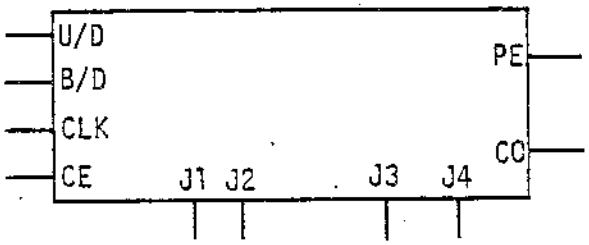
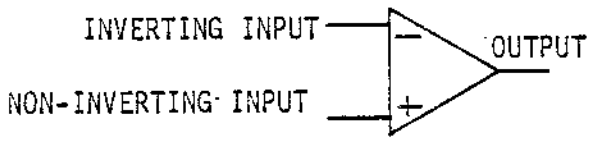
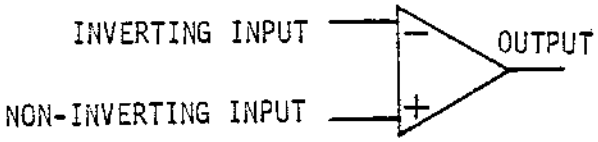
3-3. LOGIC CIRCUITS

The logic circuits used in the schematics are presented as a tabular listing in Table 3-A followed by a detailed explanation of the UART. The table is constructed to present the functional name, symbolic representation and a brief description of each logic circuit. Truth tables are provided to aid in understanding circuit operation where applicable. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle on the input or output indicates an active HIGH.

Table 3-A. Symbol Definitions

Name	Logic Symbol	Description
AND gate		All the inputs have to be enabled HIGH to produce the desired HIGH output. The output is LOW if any of the inputs are LOW.
NAND gate	 $Y=\overline{AB...N}$  $Y=\overline{A}+\overline{B}+...\overline{N}$	All of the inputs have to be enabled HIGH to produce the desired LOW output. The output is HIGH if any of the inputs are LOW.
NOR gate	 $Y=\overline{A+B...+N}$  $Y=\overline{A} \cdot \overline{B} \cdot ...\overline{N}$	Any of the inputs need to be enabled HIGH to produce the desired LOW output. The output is HIGH if all of the inputs are LOW.
Exclusive OR gate		When both inputs are equal, the output is LOW. When the inputs are different, the output is HIGH.
Inverter	 	The inverter is a device whose output is the opposite state of the input.

Name	Logic Symbol	Description
Non-Inverting Bus Driver		When enabled, the non-inverting bus driver is a device whose output is the same state as the input. Data is enabled through the device by applying a LOW signal to the E input. The output "floats" or goes to a high impedance state when the non-inverting bus driver is not enabled.
Inverting Bus Driver		The inverting bus driver is a device whose output is the opposite state of the input when enabled. Data is enabled through the driver by applying a LOW signal to the E input. The output "floats" or goes to a high impedance state when the non-inverting bus driver is not enabled.
Edge Triggered Flip-Flop		Applying a signal to the clear (CLR) input resets the flip-flop with Q LOW and $\overline{Q}$ HIGH.*. If a signal is applied to the D input, the Q and $\overline{Q}$ outputs are directly affected on the positive edge of the clock pulse. *TTL - active LOW PST and CLR CMOS - active HIGH PST and CLR
Synchronous 4-Bit Counter		The synchronous 4-bit counter is used as a divide by 13 presettable counter with internal carry (RC). When all outputs (A_{OUT}, B_{OUT} and C_{OUT}) are clocked HIGH, RC is HIGH. Data is transferred to the outputs when LOAD is LOW and a clock pulse is received. Clocking occurs on the rising edge of the clock pulse.

Name	Logic Symbol	Description
CMOS Octal Counter/Divider		The counter increments on a positive transition at the clock (CLK) input and functions as a divide by 8 counter and output decoder. A carry-out (CO) signal completes one cycle every 8 clock input cycles.
CMOS Presettable Up Counter		This counter functions as a divide by 12 up counter. Binary counting is accomplished when B/D is held HIGH and the counter functions as an up counter when U/D is held HIGH. The counter advances one count at the positive transition of the clock (CLK) when the clock enable (CE) and preset enable (PE) signals are LOW. Advancement is inhibited when PE or CE is HIGH.
Operational Amplifier (LM 358)		
Comparator (LM 393)		

3-4. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART) OPERATION

Generally, UARTs consist of a transmitting section and a receiving section. Paragraph 3-5 provides an explanation of transmitting operation and Paragraph 3-6 explains the operation of the receiver section. Included in Paragraph 3-7 is a brief functional explanation of each pin.

The UART information included in Paragraphs 3-5 through 3-7 is reprinted by permission of SMC MICROSYSTEMS CORPORATION.

3-5. UART Description of Operation - Transmitter (Figures 3-1 and 3-3)

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC and TSO are all at a HIGH level (the line is marking).

When TBMT and TEOC are HIGH, the control bits may be set. After this is accomplished, the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, TDS and CS may occur simultaneously. Once the Data Strobe ($\overline{TDS}$) has been pulsed, the TBMT signal goes LOW, indicating that the Data Bits Buffer Register is full and unavailable to receive new data.

If the Transmitter Shift Register is transmitting data that has been loaded, the TBMT signal remains LOW. If the Transmitter Shift Register is empty, or has transmitted the previous character, the data in the Buffer Register is loaded immediately into the Transmitter Shift Register and data transmission commences. TSO goes LOW (the start bit), TEOC goes LOW and TBMT goes HIGH, indicating that the data in the Data Bits Buffer Register has been loaded into the Transmitter Shift Register. The Data Bits Buffer Register is now available to be loaded with new data.

If new data is loaded into the Data Bits Buffer Register at this time, TBMT goes LOW and remains in this state until the present transmission is completed. An advantage of double buffering is that one full character time is available for loading the next character with no loss in speed of transmission.

Data transmission proceeds in the following order: start bit, data bits, parity bit (if selected) and the stop bit(s). When the last stop bit has been on the line for one bit time, TEOC goes HIGH. If TBMT is LOW, transmission begins immediately. If TBMT is HIGH, the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

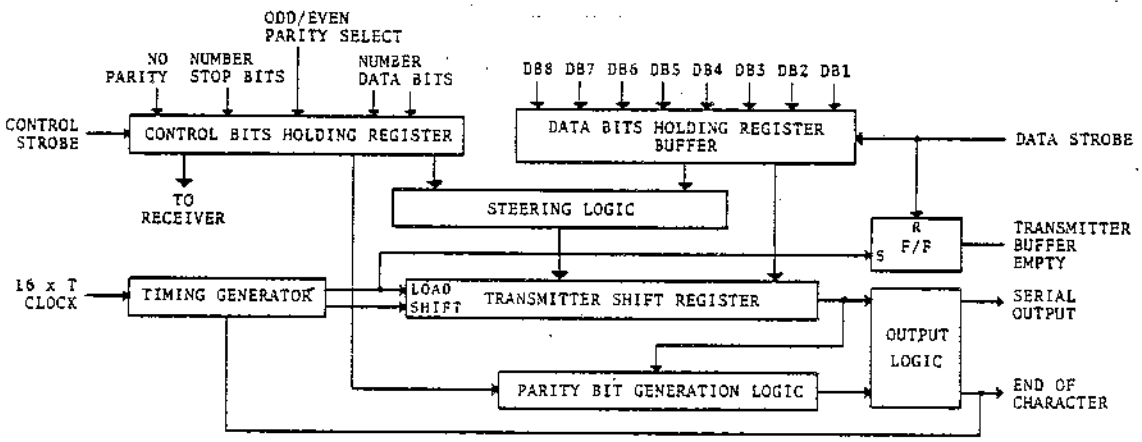


Figure 3-1. Transmitter Block Diagram

3-6. UART Description of Operation - Receiver (Figures 3-2 and 3-3)

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The Data Available (RDA) signal is now LOW. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (HIGH) to space (LOW). If the RSI line remains spacing for 1/2 a bit time, a genuine start bit is verified. Should the line return to a marking condition prior to 1/2 a bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in the following manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the Status Word Buffer Register is set HIGH, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held LOW, inhibiting a parity error indication. If a stop bit is not received, indicating an improperly framed character, the framing error flip-flop is set HIGH, indicating a framing error.

Once a full character has been received, internal logic looks at the Data Available (RDA) signal. If, at this instant, the RDA signal is HIGH, the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set HIGH. The only way the receiver is aware that data has been read out is by having the Data Available reset LOW.

At this time, the RDA output goes HIGH, indicating that all outputs are available to be examined. The Receiver Shift Register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

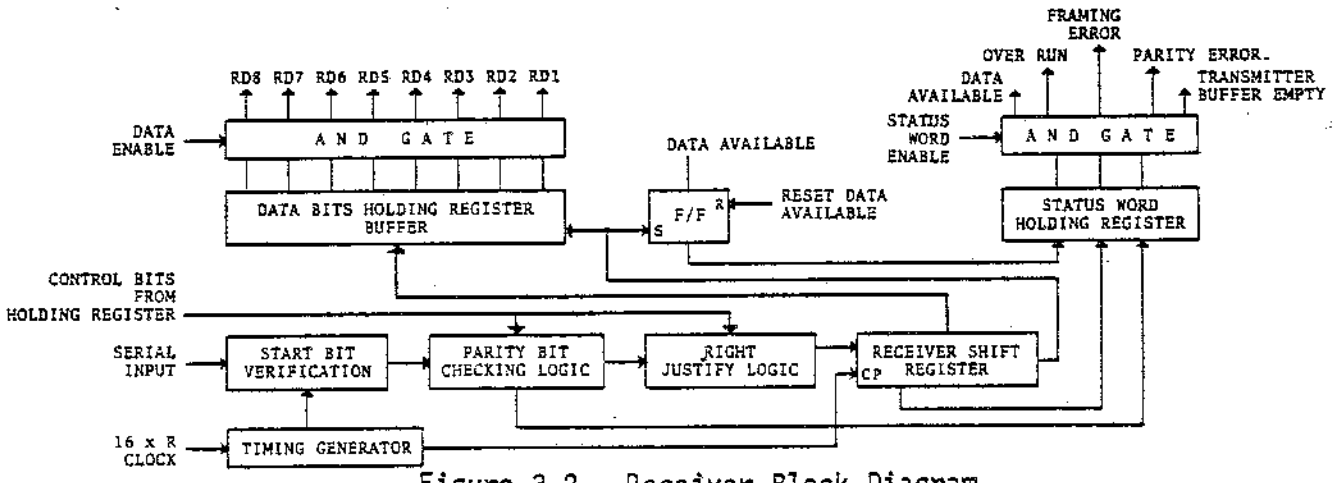
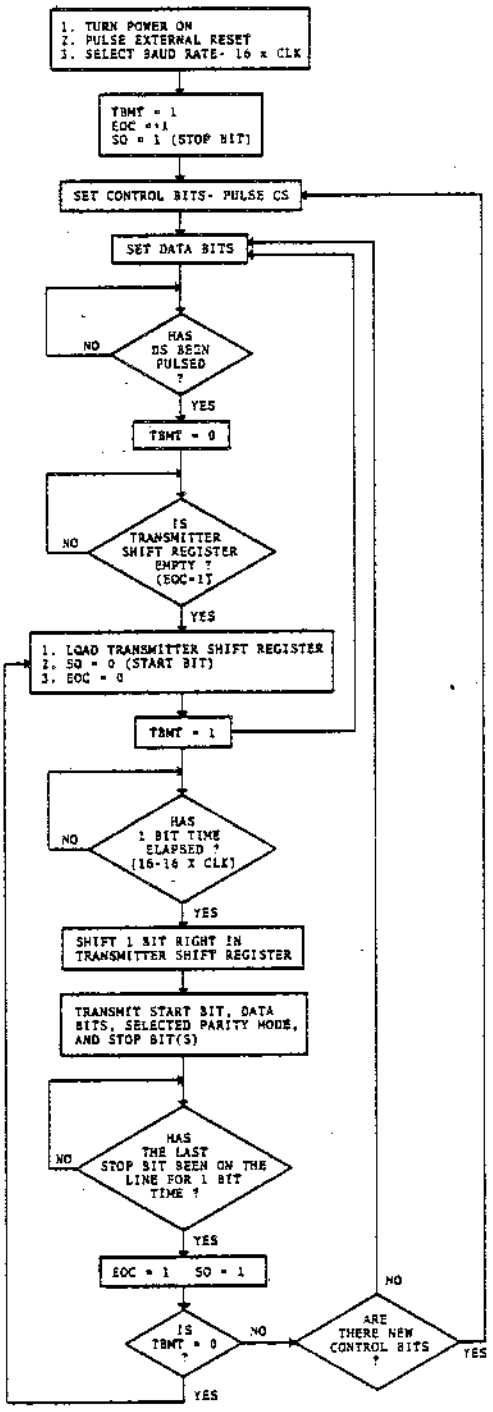


Figure 3-2. Receiver Block Diagram

FLOW CHART - TRANSMITTER



FLOW CHART - RECEIVER

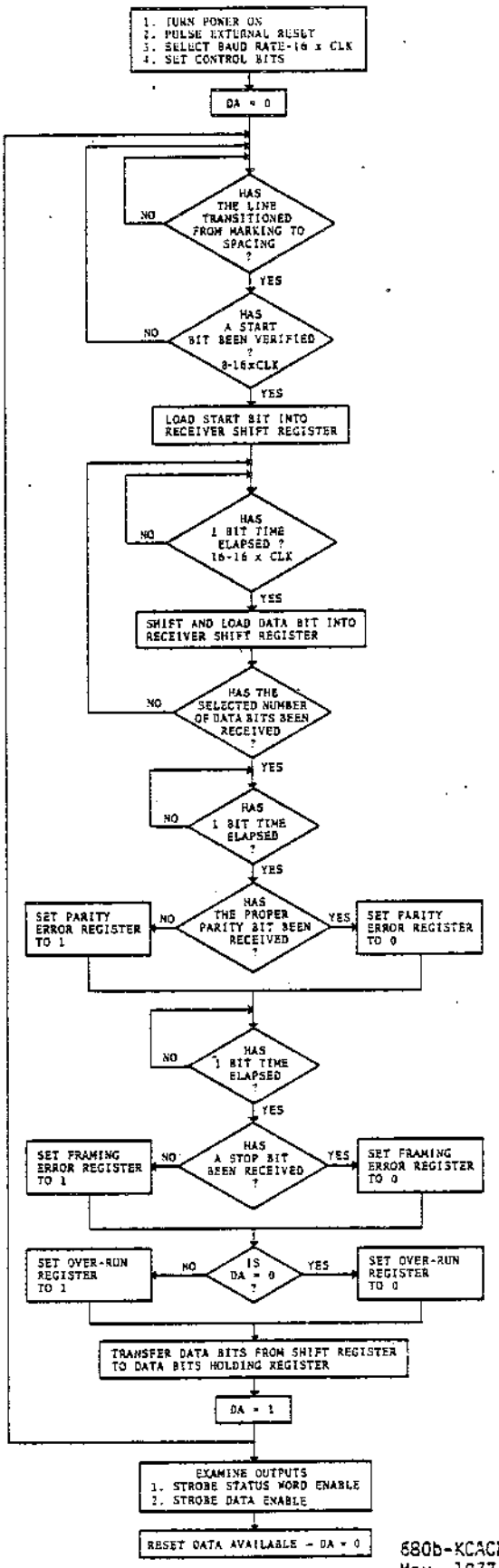


Figure 3-3. UART Transmitter/Receiver Flow Chart

3-7. DESCRIPTION OF PIN FUNCTIONS (Figure 3-4)

Pin #	Symbol	Name	Function
1	V_{CC}	Power Supply	+5 volt supply
2	V_{DD}	Power Supply	-12 volt supply
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A LOW level input enables the outputs (RD8-RD1) of the Receiver Buffer Register.
5-12	RD8-RD1	Receiver Data Outputs	These pins are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a LOW level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a HIGH level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a HIGH level if the received character has no valid stop bit.
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a HIGH level if the previously received character is not read (RDA output not reset) before the present character is transferred into the Receiver Buffer Register.
16	$\overline{SWE}$	Status Word Enable	A LOW level input enables the outputs (RPE, RFE, ROR, RDA and TBMT) of the Status Word Buffer Register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A LOW level input resets the RDA output to a LOW level.

Pin #	Symbol	Name	Function
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is a HIGH level when an entire character has been received and transferred into the Receiver Buffer Register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A HIGH level (mark) to LOW level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a HIGH level after power turn-on. This sets TSO, TEOC and TBMT to a HIGH level and resets RDA, RPE, RFE and ROR to a LOW level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a HIGH level when the Transmitter Buffer Register is loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A LOW level input strobe enters the data bits into the Transmitter Buffer Register.
24	TEOC	Transmitter End of Character	This output appears as a HIGH level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output provides the entire transmitted character in serial form. TSO remains at a HIGH level when no data is being transmitted.

Pin #	Symbol	Name	Function
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines available (strobed by $\overline{TDS}$). Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A HIGH level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the Control Bits Holding Register. This line may be strobed or hardwired to a HIGH level.
35	NPB	No Parity Bit	A HIGH level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a LOW level. See pin 39, POE.
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A LOW level input selects 1 stop bit; a HIGH level input selects 2 stop bits. Selection of two stop bits generates 1.5 stop bits from the COM2017/H when programming a 5 data bit word.
37-38	NDB2, NDB1	Number of Data Bits/Character	These two inputs are internally decoded to select either 5, 6, 7 or 8 data bits/character as shown in the following truth table:

Pin #	Symbol	Name	Function

NDB2	NDB1	data bits/character
L	L	5
L	H	6
H	L	7
H	H	8

39 POE Odd/Even Parity Select

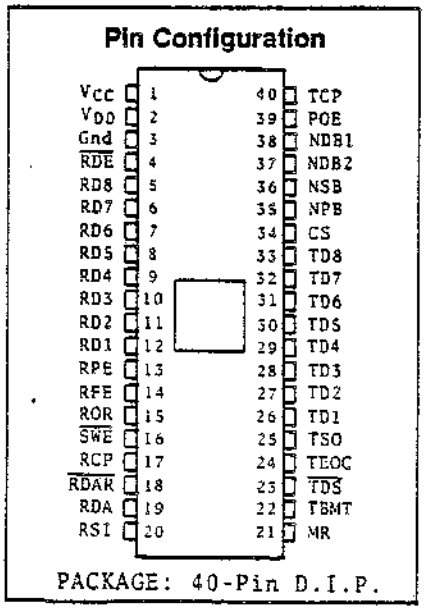
The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as shown in the following truth table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity

X=don't care

40 TCP Transmitter Clock

This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.



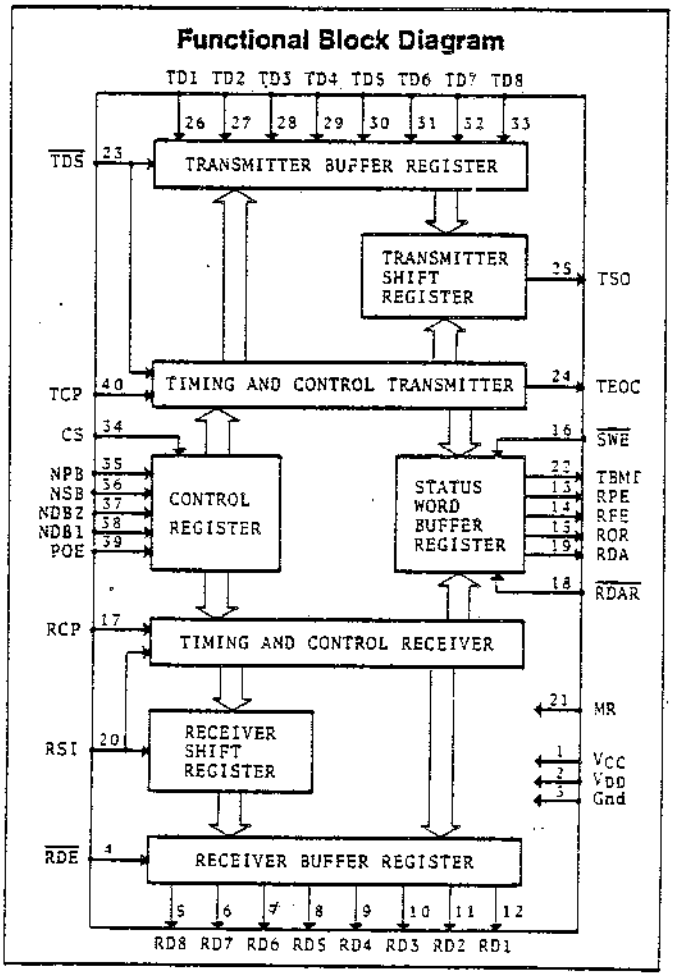


Figure 3-4. UART Block Diagram and Pin Locations

3-8. KANSAS CITY STANDARD PRINCIPLE*

The Kansas City Standard for audio cassette data interchange is based upon the use of a frequency shift modulation method from which serial clock data can be extracted at rates of up to 300 baud. The system is intended to be used with low to medium cost cassette recorders incorporating electrical stop and start capability which may be operated under program control.

The technique provides for long and short term tape speed variation, limitations in bandwidth due to effects such as tape misalignment, and the necessity to retain low cost and low complexity of the hardware. The technique allows for potential operation at higher tape speed than the nominal 1.875 inch/s (4.75 cm/s).

A mark (logical one) bit consists of eight cycles at a frequency of 2400 Hz.

A space (logical zero) bit consists of four cycles at a frequency of 1200 Hz.

A recorded character consists of a space as a start bit, eight data bits, and two or more marks as stop bits.

The interval between characters consists of an unspecified amount of time at the mark frequency. In this respect, the data format is similar to that of asynchronous data communication.

The eight data bits are organized so that the least significant bit is first, most significant bit last followed (optionally) by a parity bit. The total number of significant bits and the parity bit cannot exceed eight.

Where less than eight data bits are used, the unused bits (following the optional parity bit) at the end of the character are mark bits (2400 Hz).

*This article first appeared in the February, 1976, issue of BYTE.

Data will be organized in blocks of arbitrary and optionally variable length preceded by a minimum of five seconds of marks.

To avoid errors due to splicing and wrinkling, the beginning of the first data block will occur no sooner than 30 seconds from the start of clear leader.

The contents of the data block are not specified.

The data block ends after the stop bits of the final character.

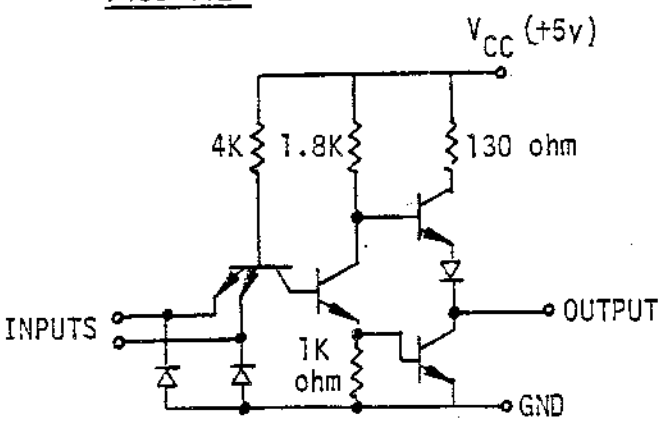
Bit clocking information may be extracted from the recorded waveform, which is always an integer multiple of the bit rate regardless of tape speed. This permits the recovery and retiming of data by means of a UART, which requires a clock of sixteen times the bit rate although other simple circuitry may be used.

A reliable bandwidth of 3000Hz is assumed in choosing mark and space frequencies due to the head misalignment expected between various cassette recorders. The recording technique is a similar form of Manchester or bifrequency code which has a long history of reliability in the computer industry.

3-9. CMOS AND TTL GENERAL OPERATION

The 680b KCACR is mainly comprised of CMOS logic with some TTL. The following information will show the differences between the two types of logic. For example, a 4011 (CMOS) and 7400 (TTL) are both Quad 2 input NAND gates.

7400 TTL



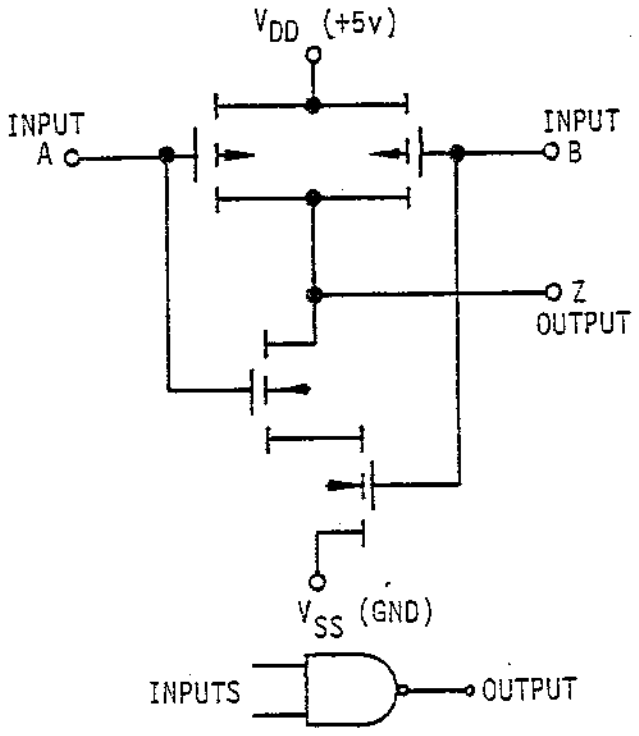
Inputs, if left floating, equal logic 1. When inputs are HIGH, there is typically negligible current flow. When logic Ø is present at the inputs, 1.6 mA current flows into the input or 400µa for low power Schottky TTL.

Output:

Logic 1 = 3.8v Max.

Logic Ø = .1v to .5v

4011 CMOS



Inputs are essentially capacitive. Very high input impedance makes input current very low. Inputs should not be left floating because they are then subject to static damage. Outputs are resistive and act as a 200 ohm to 400 ohm resistor to Ground (logic Ø) or V_{CC} (logic 1).

3-10. GENERAL THEORY AND BLOCK DIAGRAM (Figure 3-5)

Address Decoding

The Address Decoding circuit gates together the necessary signals for activating data transfers to and from the 680b-KCACR. The outputs of the address circuit are as follows:

$\overline{\text{Write Control Strobe}}$	used for control of Read or Write Interrupts and the Motor Control circuit. (Store FØ1Ø)
$\overline{\text{Read Status Strobe}}$	used for enabling the Read and Write Status Bits onto the 680b bus. Also resets the interrupts. (Load FØ1Ø)
$\overline{\text{Write Data Strobe}}$	used for transfer of Write Data into the UART Transmit register from the 680b bus. (Store FØ11)
$\overline{\text{Read Data Strobe}}$	used for transfer of Read Data from the UART to the 680b bus. Also resets the interrupts. (Load FØ11)

UART

The Universal Asynchronous Receiver/Transmitter converts parallel data to serial data when in the $\overline{\text{Write}}$ mode (transmit) and converts serial data to parallel data when in the Read mode (receive). The UART formats the serial data to include a start bit (logic Ø) and a stop bit (one or more logic ones). The rate at which serial data is transferred is the baud rate (or bit rate) and is 16 times the Write Clock or Read Clock.

Write Circuit

As data is transmitted in serial form from the UART, the Write Circuit synchronously converts the changing logic levels into 2400 Hz and 1200 Hz square waves in accordance with the Kansas City Standard. The square waves are then filtered to provide sine wave tones which are more useable to audio tape recorders.

Read Circuit

The Read Circuit inputs the audio signal from the tape recorder during playback and provides serial Read Data and the Read Clock for the UART.

The Read Filter, Zero Crossing Detector, and the Edge Detector function to give a pulse at each half cycle of the sine wave signal being played into the 680b-KCACR.

The Read Data Discriminator counts the time between these pulses to detect the logic 1 or Ø signals for the serial Read Data. Taking advantage of the synchronous nature of the audio tones, the Read Clock Generator uses a shift register to synthesize the Read Clock from the pulses provided by the Edge Detector.

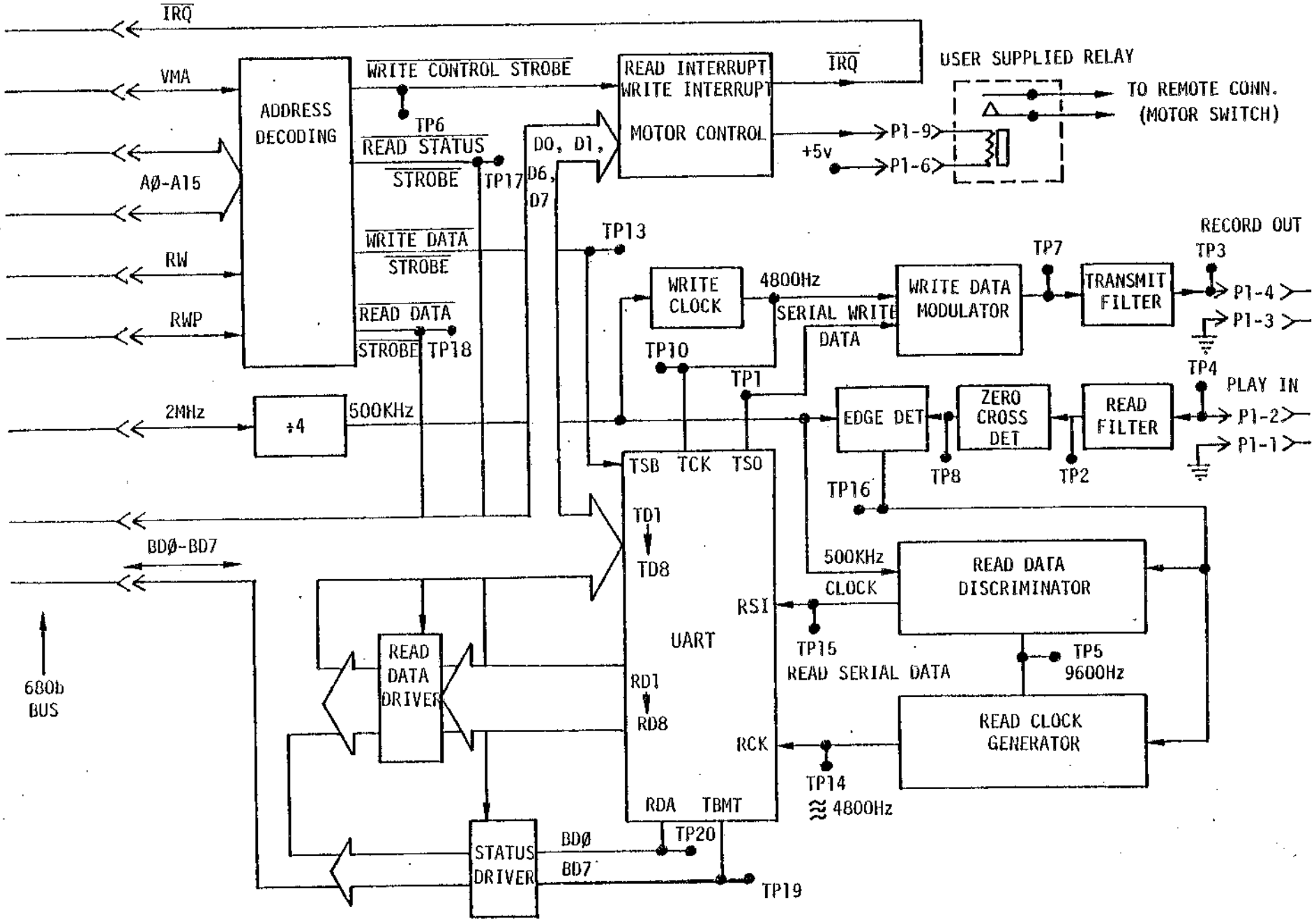


Figure 3-5. 680b-KCACR BLOCK DIAGRAM

3-11. ADDRESS AND CONTROL LOGIC (Figure 3-8)

Each 680b peripheral requires a unique address which distinguishes it from any other peripheral, and on-board circuitry is provided to enable the 680b-KCACR to detect when the processor is addressing it. Referring to Figure 3-8, Paragraphs 3-12 through 3-15 explain how the 680b-KCACR detects its address from any other and the operation of its Interrupt Enable circuitry.

3-12. Board Select (TP-11)

When FØ1Ø or FØ11 is on the address bus and VMA is valid, all the inputs to NAND gates BB (zone C7) and CC (zone D7) are HIGH. The outputs, as a result, are logic Ø (LOW). The LOWs at BB pin 8 and CC pin 8 are applied to NOR gate U pins 2 and 3. U pin 1 is enabled HIGH, providing the Board Select signal to AA pin 13, AA pin 3 (zone D6), S pin 13 and S pin 3 (zone C6).

3-13. $\overline{\text{Read Data Enable}}$ (TP-18)

The Read Data Enable ($\overline{\text{RDE}}$) signal is a function of the data channel, thus an odd address (FØ11) is required on the bus. To achieve an odd address, AØ (zone C8) must be logic 1 (HIGH). This HIGH at AØ is double inverted by DD pin 2 (zone C7) and DD pin 4 (zone C6), and presented to AA pin 2. Since $\overline{\text{RDE}}$ allows data to be read, RW (Read/Write, zone C8) is in the Read (HIGH) state. RW is double inverted by DD pin 10, and DD pin 8 and applied to AA pin 1.

When all inputs are HIGH, AA pin 12 (zone D6) is enabled LOW and the $\overline{\text{RDE}}$ signal is generated. $\overline{\text{RDE}}$ enables the Read Data Drivers GG (zones A7 and B7), and provides the $\overline{\text{RDAR}}$ signal to pin 18 of UART-Y which resets the RDA output. AA pin 12 is also tied to AA pin 11 so that AA pin 8 (zone D5) goes HIGH when AA pin 12 is enabled LOW. The HIGH at AA pin 8 is inverted and tied to the active LOW clear inputs M pin 1 (zone C3) and M pin 13 (zone C2) of the Read and Write Interrupt Enable Flip-flops.

3-14. Read Status Enable (TP-17)

Since Read Status Enable (RSE) is a status channel, an even address (FØ1Ø) must appear on the bus. AØ (zone C8) is LOW at the bus, inverted HIGH at DD pin 2, and present at AA pin 5. $\overline{RSE}$ is a Read signal so the RW line is in the Read (HIGH) state. RW, double inverted by DD pin 10 and DD pin 8, is HIGH at AA pin 4. With all the input pins HIGH, AA pin 6 (zone D6) is enabled LOW, providing the $\overline{RSE}$ signal. $\overline{RSE}$ allows the RDA and TBMT status bits at UART-Y pins 19 and 22 (sheet 2, zone B6) to pass data through T pin 8 and T pin 11 (zone B7). T pin 8 and T pin 11 are NAND gates that act as inverters and drivers by enabling line drivers GG pin 11 and GG pin 13. $\overline{RSE}$ is also tied to AA pin 9 (zone D5). When AA pin 9 goes LOW, AA pin 8 goes HIGH and is enabled LOW at EE pin 12, clearing Read and Write Interrupt Enable Flip-flops, M pin 1 (zone C3) and M pin 13 (zone C2).

3-15. Write Data Strobe (TP-13)

To enable the Write Data Strobe signal, the Board Select line is HIGH at S pin 13. AØ, HIGH at the bus (since an odd address is required), is double inverted by DD pin 2 and DD pin 4 and appears HIGH at S pin 2. The RWP (Read/Write Prime) line (zone C8) is in the Write (LOW) state. Inverted by DD pin 6 (zone C7), RWP is HIGH at S pin 1. When input pins 1, 2 and 13 are all HIGH, S pin 12 (zone C6) is enabled LOW and tied to UART-Y (zone B6) at pin 23 (TSB). When UART-Y pin 23 goes LOW, the data to be transmitted enters the UART's Transmitter Buffer Register.

3-16. Write Control Strobe (TP-6)

When active, the Write Control Strobe ($\overline{WCS}$) signal enables the Read and Write Interrupt control signals and the MOTOR ON and MOTOR OFF control signals. $\overline{WCS}$ is generated when input pins 3, 4 and 5 of S (zone C6) are HIGH. S pin 3 is HIGH when the board is selected. S pin 4 is HIGH when RWP is in the Write (LOW) state and inverted at DD pin 6; S pin 5 is HIGH when AØ is LOW at the bus and inverted by DD pin 2. S pin 6 ($\overline{WCS}$) enables a LOW to NOR gates L pins 2, 5, 9 and 12 (zone C5).

When $\overline{WCS}$ is enabled and a LOW is output on data line BD0 (zone B8), allowing L pin 3 LOW, L pin 1 is enabled HIGH. L pin 1 clocks the Read Interrupt Enable Flip-flop at M pin 3 (zone C3). The Read Interrupt Enable Flip-flop, M pin 5 (zone D3) toggles HIGH on a positive transition at M pin 3. When a character is received by UART-Y (zone B5), RDA (Y pin 19) goes active HIGH. RDA is connected to T pin 2 (zone D3) and M pin 5 is connected to T pin 1. With both inputs HIGH, T pin 3 is enabled LOW, pulling the $\overline{IRQ}$ line (zone D1) LOW, interrupting the system. $\overline{IRQ}$ is reset when data or status is read by the MPU.

L pin 5 (zone C5) is tied to S pin 6 and BD1 (zone B8) is tied to L pin 6. When $\overline{WCS}$ (S pin 6) is active and a logic Ø is output on the BD1 line, L pin 4 is enabled LOW and the Write Interrupt Enable Flip-flop, M, is clocked at pin 11 (zone C2). On the positive transition of L pin 4 (zone C5), M pin 9 toggles HIGH, applying a HIGH to T pin 5 (zone D2). When a character is transmitted, TBMT (zone B6) becomes active HIGH, enabling T pin 4 (zone D2). This pulls the $\overline{IRQ}$ line (zone D1) LOW and the system interrupts as a result. Upon a read of the status or data channels, the Write Interrupt Enable Flip-flop, M, is reset (output pin 9 LOW) and the $\overline{IRQ}$ line is disabled HIGH.

The remote motor control feature, an option of the 680b-KCACR, utilizes an external 5v relay supplied by the user. When $\overline{WCS}$ (zone C6) is active and a LOW is output on the BD7 line (zone A8), L pin 13 (zone C5) is enabled HIGH, supplying the clock pulse to F pin 3 (zone C1). On the positive transition of F pin 3, F pin 6 toggles LOW, enabling the two drivers HH (zone C1). This completes a current path through the relay and the motor is turned on.

To turn the motor off, $\overline{WCS}$ is again active LOW at L pin 9 and a LOW is output to L pin 8 on the BD6 line (zone A8). L pin 10 is enabled HIGH and inverted LOW at DD pin 12. The LOW at DD pin 12 clears flip-flop F at pin 1 (zone C1). This sets F pin 6 HIGH, disabling driver HH and the relay is turned off. The MOTOR OFF signal at DD pin 12 (zone C4) is also tied to AA pin 10 (zone D5). AA pin 8 (zone D5) goes HIGH, is inverted LOW at EE pin 12, sending a LOW to the active LOW clear inputs of the two Interrupt Enable Flip-flops, M. This resets M pin 5 and M pin 9 LOW.

3-17. READ CIRCUIT (Figure 3-8)

The 680b-KCACR utilizes 2400Hz for a logic 1 and 1200Hz for a logic Ø. A frequency discriminator circuit is provided to distinguish between the two frequencies. Referring to Figure 3-6, it is noted that the circuit discriminates between half cycles of the data. If the edges of each half cycle are detected, a pulse occurs every 416 µs. for 1200 Hz (logic Ø). For 2400 Hz (logic 1) a pulse occurs every 208 µs. A counter is set up to output after counting 312 µs. and holds the output by stopping its clock. If a logic 1 pulse is detected, a pulse occurs every 208 µs., starting the frequency counter. Since this counter only outputs after counting 312 µs., the logic 1 half cycle pulse resets the counter to start over again with no output. A logic 1 is detected when the counter does not have an output. However, for a logic Ø, the edge detected pulses are 416 µs. apart, allowing more than enough time for the counter to output and hold.

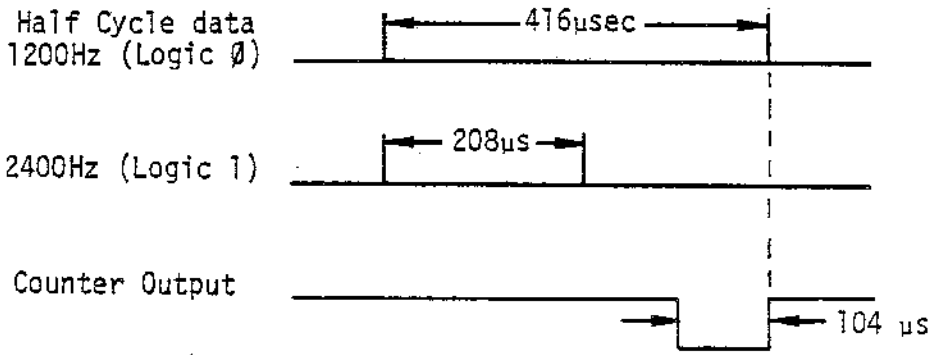


Figure 3-6. Frequency Discriminator Timing Diagram

The synchronous Read Clock is generated by feeding the audio square wave into a shift register. The outputs of the shift register flip-flop are gated together to synthesize the Read Clock. The clock rate for the shift register is two times the Read Clock frequency and appears at TP-5 (sheet 1, zone B5).

3-18. 500KHz Clock

Data from the tape is filtered by operational amplifier, E (sheet 1, zone D6), which has a center frequency of 1.8KHz. The filtered signal is applied to a zero crossing detector, G pin 2 (zone D3). Every time the input signal crosses a zero voltage level there is a change in state at the output. The resulting output at G pin 1 is the audio signal squared. The squared audio is inverted at R pin 2 (zone C7) and applied to the Data (D) input, V pin 5 (zone C7). The input is clocked to the output on the positive transition of the 500KHz clock at V pin 3. The 2MHz clock is divided by 2 at Z pin 2 and divided again by 2 at Z pin 12 (zone B7), resulting in the 500KHz clock.

3-19. Edge Detector

When the positive transition of the first 500KHz clock pulse appears at V pin 3, the squared audio data present at V pin 5 is transferred to the Q output, V pin 1. At this time, X pin 3 (zone C6) goes HIGH. On the next positive transition of the 500KHz clock, which occurs 2 µs. later ($\frac{1}{500}$ = 2 µs.), data present at V pin 9 is clocked to the Q output, V pin 13. As a result, both $\overline{Q}$ outputs, V pin 2 and V pin 12, are in the same logic state, allowing X pin 3 to return LOW until the next data half cycle.

3-20. 38.4KHz Clock

The output pulse at X pin 3 is 2 µs. wide with a period of 416 µs. when a 1200Hz (logic Ø) square wave is present at the data (D) input (V pin 5). When a 2400Hz (logic 1) square wave is present at V pin 5, the pulse period at X pin 3 is 208 µs. (refer to Figure 3-7 for timing diagram). There is a 2 µs. pulse at the Edge Detector, X pin 3, for every half cycle of data.

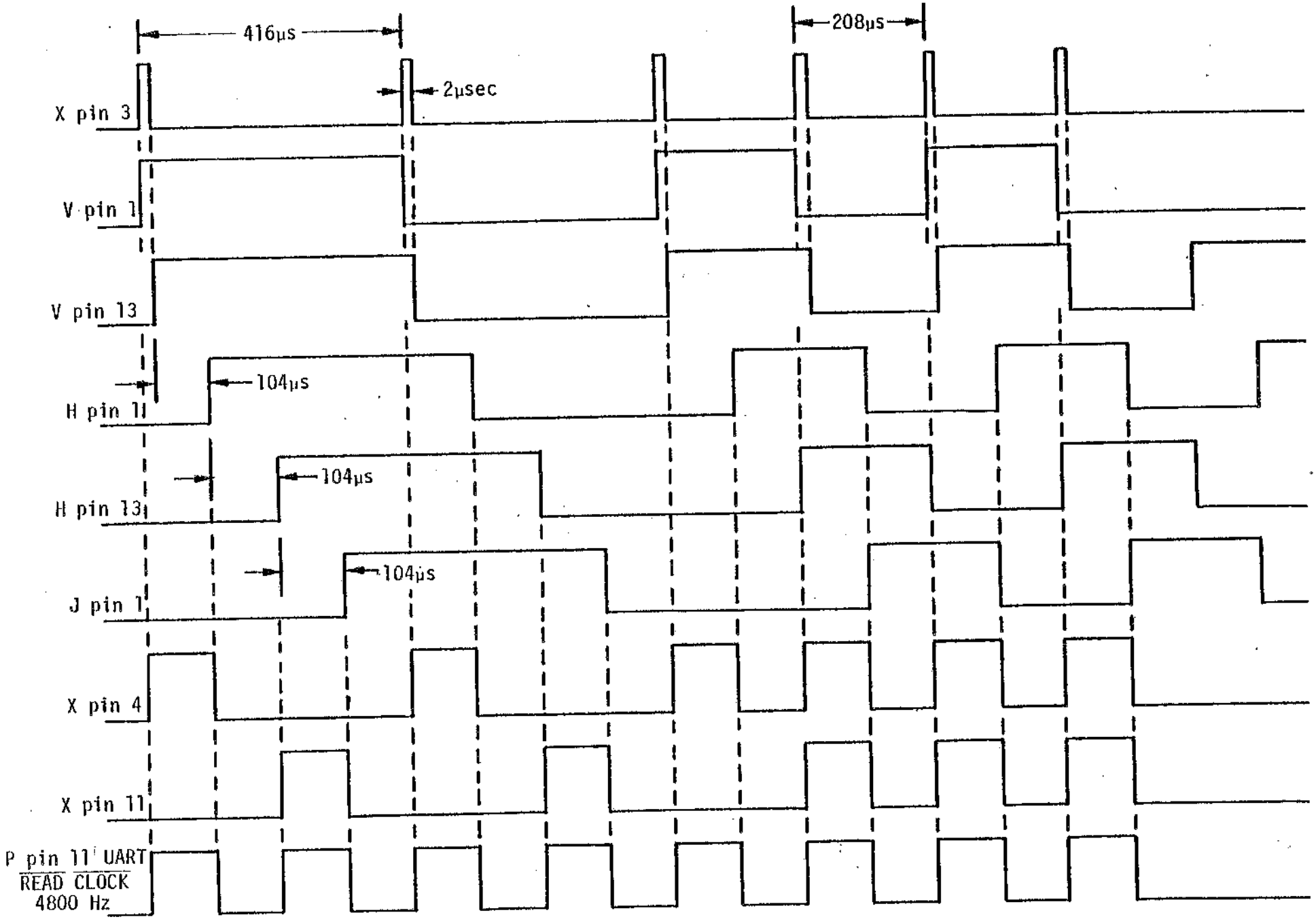


Figure 3-7. Read Circuit Timing

The 500KHz clock is also applied to the clock input (CK) of W pin 2 (zone A7). W, a Presettable Binary Counter, is preset to divide the 500KHz clock by 13 for a 38.4KHz ($\frac{1}{38.4KHz}$ + 26 µs.) signal at the carry output (RC, W pin 15). Each time the Edge Detector (X pin 3) pulses HIGH, P pin 8 (zone A6) is HIGH and P pin 10 goes LOW. The LOW at P pin 10 is connected to the active LOW load (LD) input, W pin 9, to start the counter over again. The 38.4KHz signal is the time base for the Read Data Discriminator and Read Clock Generator.

3-21. Read Data Discriminator

The 38.4KHz clock is inverted at R pin 4 (zone A6) and fed into N pin 15 (zone A6) through NOR gate P (zone A6). N counts the time between Edge Detector Output pulses at X pin 3 (zone B6). If the pulses occur more frequently than 312 µs., the CO output (zone A5) remains HIGH and the Read Data Latch, J pin 12 (zone B5), is clocked to a Logic 1 state on the next pulse from the Edge Detector Output at X pin 3 (zone C6). When J pin 12 is in a logic 1 state, the $\overline{Q}$ output is LOW.

If the pulses from the Edge Detector occur at intervals greater than 312 µs., the CO output of N goes LOW. This LOW at N pin 7 (zone A5) is inverted at R pin 6 (zone B5). The HIGH at R pin 6 clears the Read Data Latch to a logic Ø state (the $\overline{Q}$ output is HIGH) and also inhibits the clock signal at N pin 15 by holding P pin 4 (zone A6) LOW. The CO output of N remains LOW until the next pulse from the Edge Detector Output presets N.

Note that the $\overline{Q}$ output of the Read Data Latch, J pin 12, is used for the $\overline{\text{Read Data}}$ signal. The data is inverted at this point to allow for the TTL level inverting driver, U (sheet 2, zone B6). The signal is inverted at U pin 13 and presented to UART-Y at pin 20 (zone B6), the Read Data Input.

3-22. Read Clock Generator

Referring to the timing diagram in Figure 3-7, the 38.4KHz signal is used to generate the 9.6KHz clock for the Read Clock Generator. The 38.4KHz signal is divided by 2 at the $\overline{Q}$ output, B pin 2. B pin 2 clocks B pin 11 (zone B6) and the signal is divided again by 2 (a total of two divisions), appearing at the $\overline{Q}$ output, B pin 12, as 9.6KHz. The 9.6KHz

signal clocks the Read Clock Generator, consisting of flip-flops V pin 1, V pin 13 (zone C7), H pin 1, H pin 13 (zone C6) and J pin 1 (zone C5) connected as a shift register. When V pin 1 changes state (logic 1 or Ø), approximately 104 µs. later, H pin 1 shows the same change since the period of 9.6KHz is 104 µs. H pin 12 shows the change 104 µs. later, followed by J pin 1, 104 µs. later. Thus, from the time V pin 1 changes state, 312 µs. elapse before J pin 1 shows the same change.

V pin 1 is tied to X pin 6 (zone C6) and X pin 5 is tied to H pin 1. X is an Exclusive OR gate in which the output is HIGH provided one input is HIGH; however, if both inputs are either HIGH or LOW, the output is LOW. When V pin 1 changes state, H pin 1 is the opposite state for 104 µs. due to the shift delay. X pin 4 (zone C5) is a logic 1 for 104 µs. then it returns LOW and stays LOW for the duration of the data half cycle (logic Ø duration = 312 µs.; logic 1 duration = 104 µs.). 208 µs. after V pin 1 (zone C7) changes, H pin 13 (zone C5) changes. H pin 13 is tied to X pin 13 (zone C5). J pin 1, which is in the opposite state for 104 µs. after H pin 13 changes, is tied to X pin 12. Thus, X pin 11 has the same output pulse as X pin 4, except the leading and trailing edges are shifted 208 µs. when a logic Ø is read. When a logic 1 is read, the two outputs appear to occur simultaneously. X pin 4 and X pin 11 are ORed together by the two NOR gates, P pin 3 and P pin 11 (zone C4). A resulting Read Clock frequency of 4800Hz is then inverted at R pin 10 (sheet 2, zone A4) and presented to UART-Y at pin 17 (RCK).

3-23. WRITE CIRCUIT (Figure 3-8)

The Write Circuit provides modulated audio tones for recording data. The data is transferred out in serial form, modulated in the Kansas City Standard format and output onto the cassette tape.

3-24. 4800Hz Clock Circuit

A 500KHz clock is present at the clock (CK) input to the divide by 13 counter C pin 2 (sheet 1, zone B4). Thus, the output frequency at C pin 15 (RC) is 38.4KHz. This 38.4KHz is inverted at R pin 8 (zone B3) and tied to the active LOW load (LD) input to reset the counter. R pin 8 also provides clock pulses to counter D pin 14 (zone B2). D, a divide by 8 counter, divides the 38.4KHz (present at pin 14) down to 4800Hz.

The 4800Hz Write Clock signal is inverted at R pin 10 (zone B1), and is applied to U pin 5 (sheet 2, zone B4). The $\overline{\text{Write Clock}}$ signal is inverted at U pin 4, and provides the Transmit Clock signal to pin 4 of UART-Y.

3-25. Modulator

The 4800Hz clock at D pin 12 is connected to the input of divide by 2 flip-flop, K pin 3 (zone B3). The 2400Hz square wave at the Q and $\overline{Q}$ outputs of K are presented to the inputs of two input AND gates A (zones A3 and B3). If the Write Data is a logic 1, the AND gates are enabled. Since the 2400Hz signals are being applied, the inputs of the AND gates are of opposite phase. At a 2400Hz rate, the AND gates Preset (PST) and Clear (CLR) K pins 8 and 10, resulting in a 2400Hz signal at K pin 12.

If the Write Data is a logic Ø, AND gates A are disabled, leaving K pins 8 and 10 LOW. This enables K to divide the 2400Hz signal at the clock input, K pin 11, resulting in a 1200Hz signal at the $\overline{Q}$ output, K pin 12. Using this arrangement, the 2400Hz/1200Hz modulated Write Data signal, appearing at TP-7 (K pin 12) is synchronous with the Serial Write Data. This results in a completely symmetrical square wave at TP-7, with frequency changes occurring only at the completion of a full cycle of the square wave.

3-26. Filter Circuit

R10, R12 and R9 (zones C4 and C3) act as a filter to integrate the square wave from the modulator and to remove some of its high frequency harmonics. The resulting signal is a sawtooth wave which is then fed to a 2KHz Filter, E pins 5 and 6 (zone C2). E, having a gain of 2 and a Q of 2, removes almost all other harmonics. The output of the filter, approximately 330 mV peak to peak sine wave, is connected to an 11:1 voltage divider (R6 and R7, zone C1), providing a 30 mV peak to peak signal suitable for MIC inputs of tape recorders.

KCACR

SECTION IV
TROUBLESHOOTING

4-1. INTRODUCTION

This section contains Read and Write Test programs to aid the user in testing the operation of the 680b KCACR board. Included is a brief description of all the test points, and troubleshooting charts to aid in locating and correcting any trouble areas.

4-2. VISUAL INSPECTION CHECK LIST

Before a board is installed and a preliminary test performed, the board should be visually inspected for problems due to improper handling. The following visual checks should locate most of these malfunctions.

1. Check for loose or missing components
2. Look for broken leads or leads that have not been soldered
3. Check for solder bridges
4. Check for possible cold solder connections
5. Examine PC board carefully for hairline opens in lands
6. Check IC chips for proper pin placement and good socket connections
7. Examine electrolytic capacitors for proper polarity
8. Examine diodes for proper polarity
9. Be sure the correct color code has been observed on all resistors

4-3. GENERAL PROCEDURES FOR TROUBLESHOOTING TTL AND CMOS LOGIC

1. HIGH level (logic 1) = Vinput, 2v (4v CMOS) min; Voutput, 2.4v (4v CMOS) min.
   LOW level (logic Ø) = Vinput, .8v (1v CMOS) max; Voutput, .4v (1v CMOS) max.
2. Always work backward through the logic from the trouble area.
3. Always disconnect power when removing or replacing ICs, or cutting or resoldering PC lands.
4. When a gate element appears bad (an output is the opposite of what it should be with a given input):
   a. Insure the IC package has correct voltage supplies and grounds.

b. Recheck the output with the pin open (bend the pin up and reinsert the IC in its socket--if not socketed, cut the land that connects the pin to the external circuitry). If the output remains incorrect, replace the IC with a new part. If the output is now correct, look for shorts to nearby PC lands (visually and with an ohmmeter). If none are found, the probable cause is a defective input at one of the elements that the output feeds. Isolate each input in turn by opening it from the external circuitry. This procedure will not work for CMOS logic unless a voltage or ground is applied to the open pin. Be careful when isolating CMOS logic inputs due to high input impedance (static sensitive).

c. If an input is between .8 volts and 2 volts, check continuity back to the driving output. An open input on a CMOS gate is difficult to check. It usually appears as a logic Ø due to the resistance to ground in the scope or meter probe.

4-4. TEST POINT DESCRIPTIONS AND WAVEFORMS

The following is a brief description of each test point. It is helpful to know what signal each test point is representing before beginning troubleshooting. Waveforms generated during a Read and Write test at some of the various test points are also included.

TP-1 -- Write Data from UART -- Approximately 36.7 ms. in duration for 1 data word (bit width = 3.3 ms.). Located in Write Circuit.

TP-2 -- Read Filter Output -- Filtered audio entering the zero crossing detector. Located in the Read Circuit.

TP-3 -- Record Out Audio -- To MIC input of tape recorder. Located in the Write Circuit.

TP-4 -- Play In Audio -- Before entering the Read Data Filter. Located in the Read Circuit.

TP-5 -- Read Clock Generator Shift Clock -- 9600Hz supplied to the Read Clock Generator. Located in the Read Circuit.

TP-6 -- Write Control Strobe -- Active LOW signal supplied to the Read Clock Generator. Located in the Address/Control Circuit.

TP-7 -- Modulated Write Data -- Logic 1 = 2400Hz. Logic Ø = 1200Hz. Located in the Write Circuit.

TP-8 -- Squared Read Audio -- Square wave audio signal after passing through the Zero Crossing Detector. Located in the Read Circuit.

TP-9 -- Read Data Discriminator Counter -- Pulsing indicates logic Ø; steady HIGH indicates logic 1. Located in the Read Circuit.

TP-10 -- 4800Hz UART Transmit Clock -- Located in the UART Circuit.

TP-11 -- Board Select -- Active LOW signal used to enable Control/Status logic. Located in the Address/Control Circuit.

TP-12 -- 38.4KHz output from the divide by 13 Counter -- used to divide the 500KHz clock down to a 38.4KHz clock. Located in the Read Circuit.

TP-13 -- Write Data Strobe -- Active LOW signal used to clock data into the UART. Located in the Address/Control Circuit.

TP-14 -- 4800Hz Read Clock -- Developed by the Read Clock Generator. Located in the Read Circuit.

TP-15 -- Receive Serial In (RSI) to the UART -- Each data word should be approximately 36.7 ms. wide. Located in the UART Circuit.

TP-16 -- Edge Detector Output -- A 2 µs. wide pulse detected at every half cycle of audio input. Duration is approximately 416 µs. for logic Ø and 208 µs. for logic 1. Located in the Read Circuit.

TP-17 -- Read Status Enable -- Active LOW signal used to allow software to check the status bits. Located in Address/Control Circuit.

TP-18 -- Read Data Enable -- Active LOW signal used to enable the Read Data Drivers. Located in the Address/Control Circuit.

TP-19 -- Transmit Buffer Empty -- The Write Status bit. Located in the UART Circuit.

TP-20 -- Receive Data Available -- The Read Status bit. Located in the UART Circuit.

READ CIRCUIT WAVEFORMS

The following waveforms are generated when a read test is in progress:

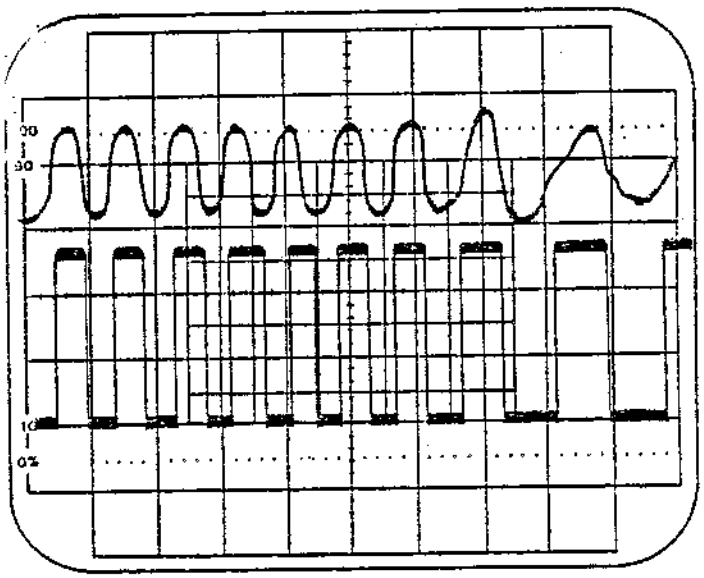
Waveform #1

TP-4 shows data coming off the tape. TP-8 is the Squared Audio signal.

TP-4
Audio Input

2v/CM

TP-8
Squared Audio



.5ms/CM

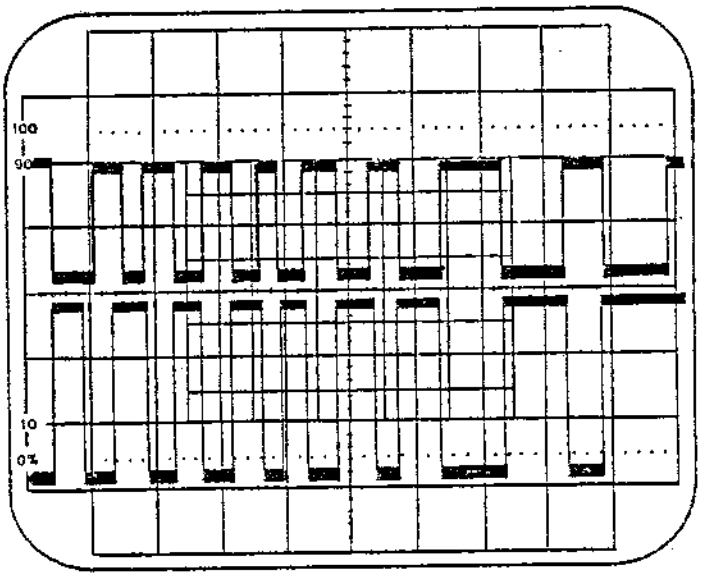
Waveform #2

TP-2 is the audio signal at the Read Filter Output. TP-8 is again the Squared Audio signal.

TP-2 Read
Filter Output

2v/CM

TP-8
Squared Audio



.5ms/CM

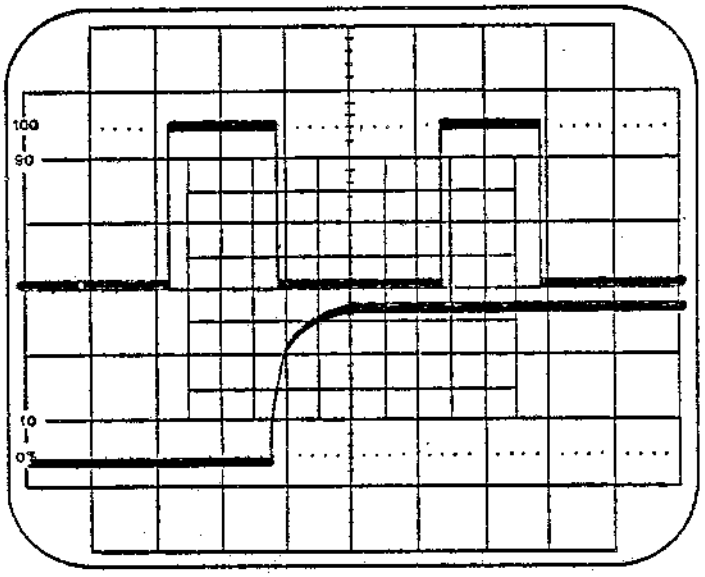
Waveform #3

Trace 1 is the Ø2 clock at the bus. TP-18 is the Read Data Enable pulse which enables the Read data drivers.

Bus Ø2

2v/CM

TP-18
Read Data Enable



.5µs/CM

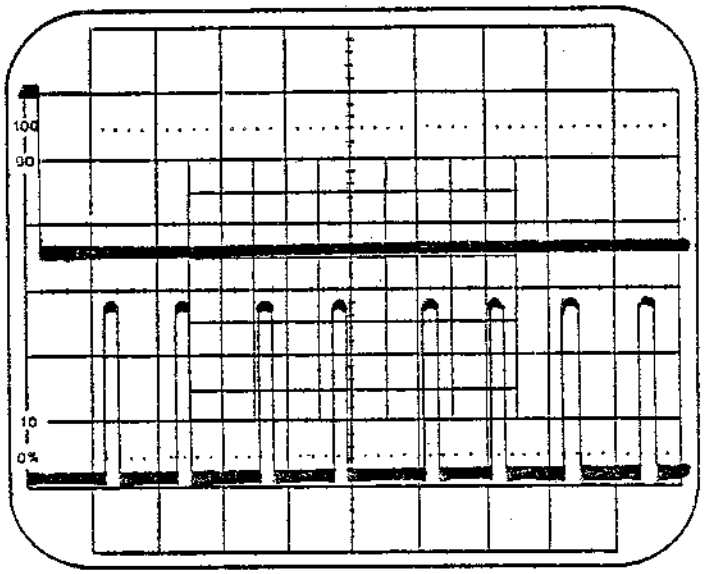
Waveform #4

TP-16 displays the 2 µs. pulse of the Edge Detector Output, compared with the 38.4KHz clock at TP-12. The pulses at TP-12 are 26 µs. apart.

TP-16
Edge Detector
Output

2v/CM

TP-12
38.4KHz Clock



Uncal.

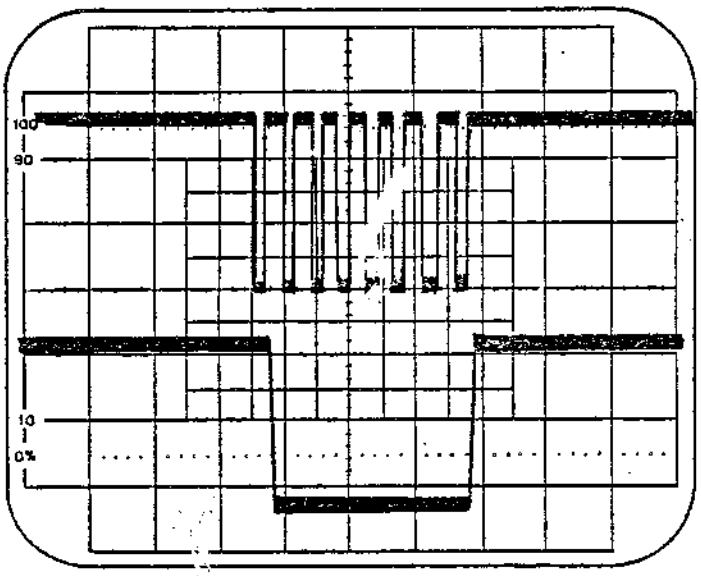
Waveform #5

TP-9 is the Read Data Discriminator Counter. TP-15 is the Read Data. Notice how the Read Data Discriminator Counter has only logic Ø outputs.

TP-9 Read Data Discriminator

2v/CM

TP-15 Serial Read Data



1ms/CM

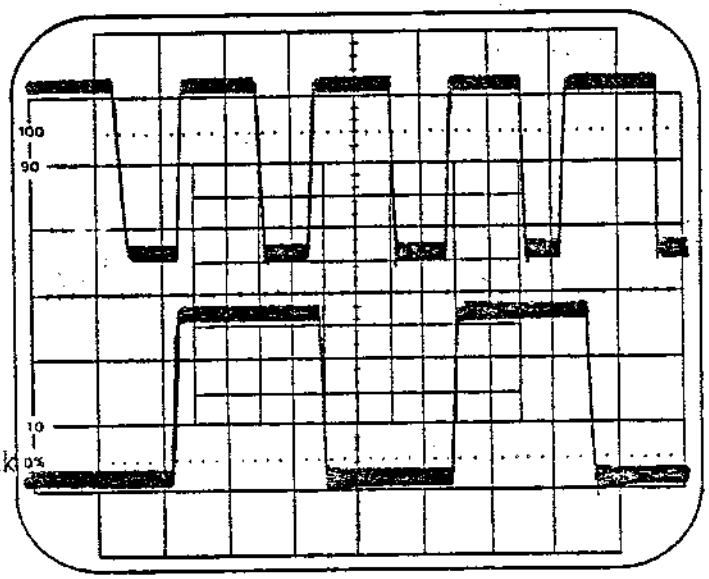
Waveform #6

TP-5 is the 9600Hz Read Clock Generator Shift Register. TP-14 is the 4800Hz Read Clock.

TP-5 Read Clock Generator Shift Register

2v/CM

TP-14 4800Hz Read Clock



50μs/CM

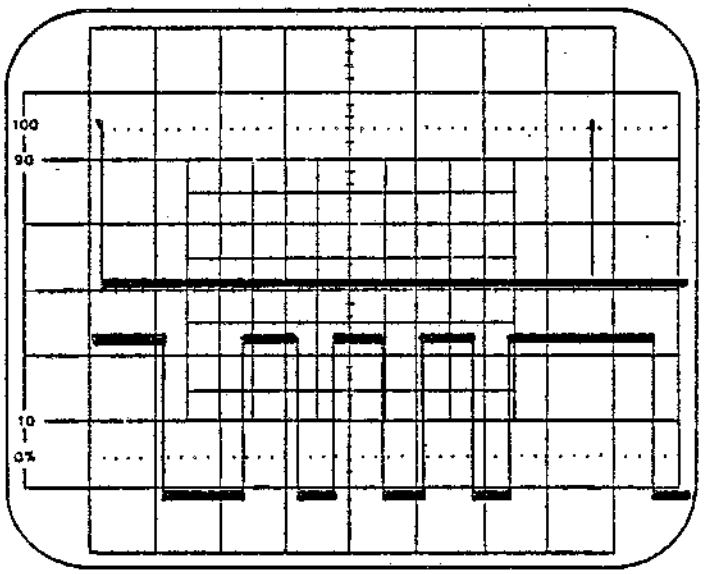
Waveform #7

TP-20 is RDA. On the positive transition, a UART character is ready. When RDA is HIGH, software will recognize it and input the data, resetting RDA LOW. TP-15 is the Read Data.

TP-20 RDA

2v/CM

TP-15 Read Data



5ms/CM

WRITE CIRCUIT WAVEFORMS

The following waveforms are generated when a write test is in progress:

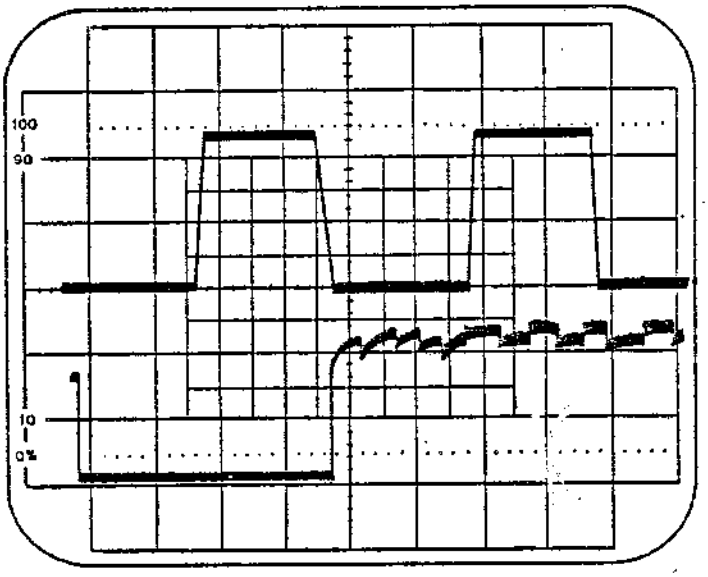
Waveform #1

Displayed with the Ø2 system clock is $\overline{\text{Read Status Enable}}$, TP-17. When $\overline{\text{RSE}}$ is active, the status bit drivers are enabled.

Ø2 System Clock

2v/CM

TP-17 $\overline{\text{RSE}}$



500ns/CM

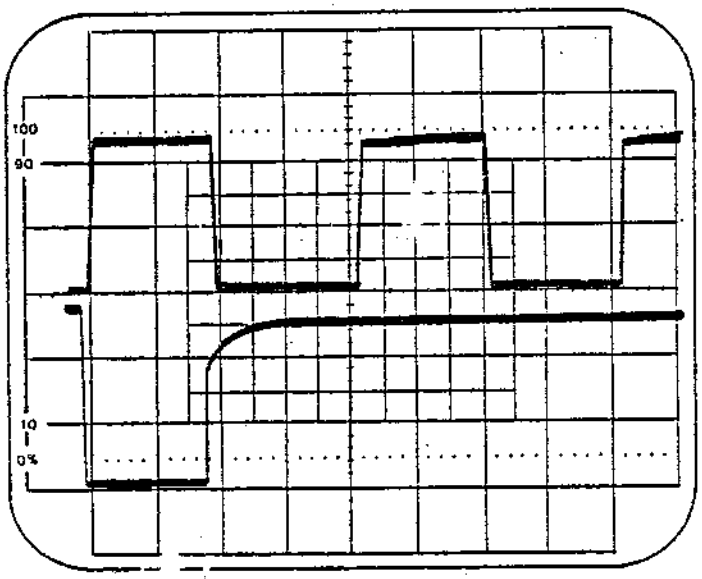
Waveform #2

The Ø2 system clock is shown in respect to $\overline{\text{WRITE DATA STROBE}}$ ($\overline{\text{WDS}}$) at TP-13. When $\overline{\text{WDS}}$ is active, data is loaded into the Transmitter Buffer Register and ready to be output to the tape through the Write Circuit.

Ø2 System Clock

2v/CM

TP-13 $\overline{\text{WDS}}$



500ns/CM

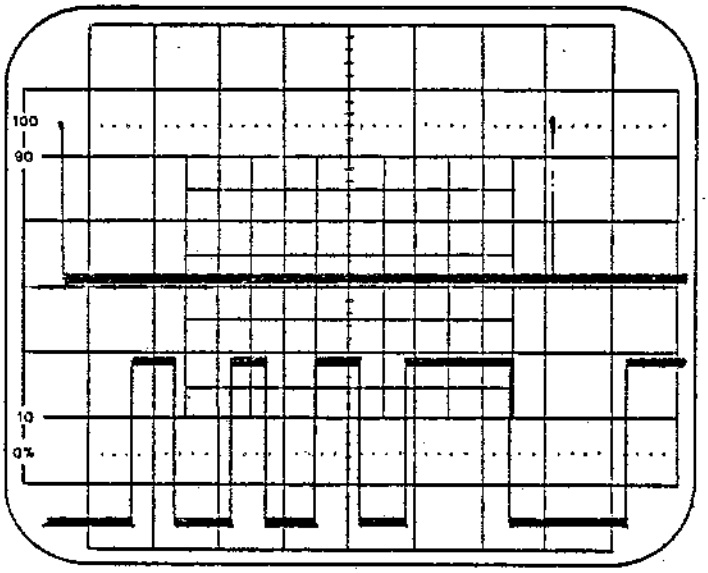
Waveform #3

TP-19 is TBMT. On a positive transition of TBMT the UART is ready for another character. When TBMT is HIGH, software recognizes it and outputs a character to the UART. TP-1 is the Write Data.

TP-19 TBMT

2v/CM

TP-1
WRITE Data



5ms/CM

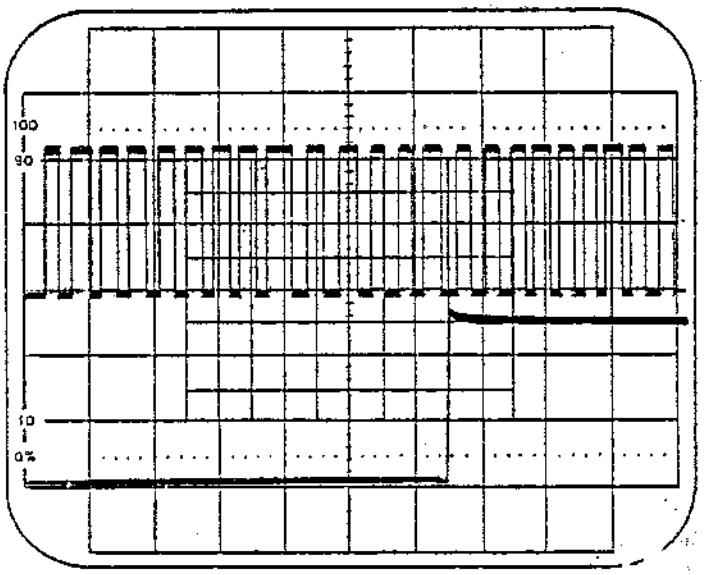
Waveform #4

TP-10 is the 4800Hz Write Data Clock. TP-1 is a logic Ø changing to a logic 1. Due to the 300 baud rate, there are 16, 4800Hz clock pulses for the bit displayed.

TP-10
4800Hz Write
Data Clock

2v/CM

TP-1
Logic Ø to
Logic 1



.5ms/CM

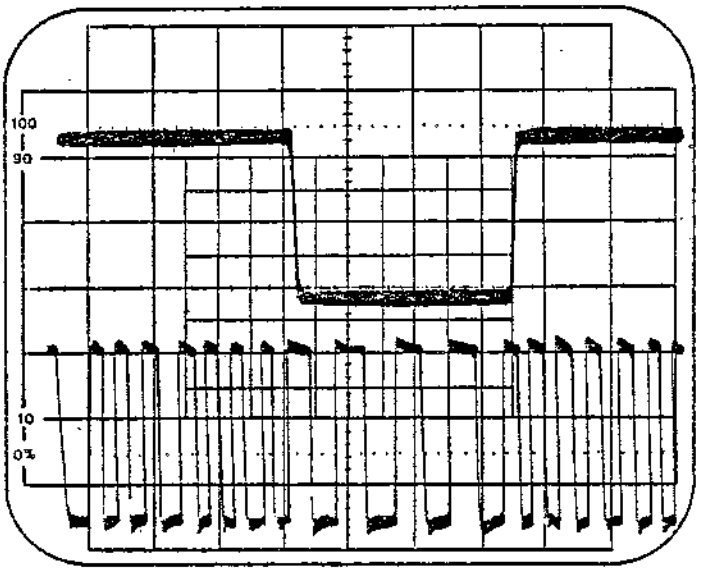
Waveform #5

TP-1 is the Write Data. TP-7 is the modulated Write Data. There are 8 clock cycles of the 2400Hz frequency for a logic 1 and 4 clock cycles of the 1200Hz for a logic Ø. Each data bit at TP-1 is 3.3 ms. wide.

TP-1 Write Data

2v/CM

TP-7 Modulated Write Data



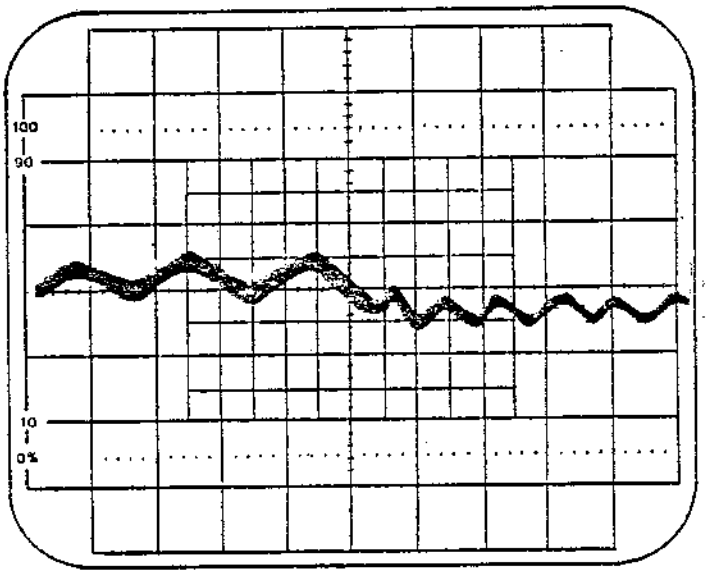
1ms/CM

Waveform #6

TP-3 is the waveform of the write data after the 2KHz filter. The write data is ready to be put on the tape.

50mv/CM

TP-3 Write Data after 2KHz Filter



.5ms/CM

4-5. PRELIMINARY CHECK

After visual inspection has been completed and the 680b-KCACR board is installed, enter and run Program 4-I. This short test program Reads and Writes a fixed bit pattern to check the Read and Write Circuit for proper operation. The bit pattern should be the same for both the Read and Write check. The Write pattern is set by location 0104 and the Read pattern by location 020A. There is no limit to the number of bytes written or read since the test is stopped manually by the operator. An error during the Read operation is indicated by returning control to the monitor. If a malfunction occurs while performing this preliminary check, proceed to Table 4-A to check the Power Supply circuitry.

Program 4-I. Preliminary Test

Write Test

```
.M 0100  CE
.N 0101  F0
.N 0102  00
.N 0103  C6
.N 0104  AA*
.N 0105  A6
.N 0106  10
.N 0107  2B
.N 0108  FB
.N 0109  E7
```

```
.N 010A  11
.N 010B  20
.N 010C  F7

.J 0100  to start
```

*Or any bit pattern

Read Test

.M 0200	F6	.N 0209	C6
.N 0201	F0	.N 020A	AA**
.N 0202	10	.N 020B	11
.N 0203	56	.N 020C	27
.N 0204	25	.N 020D	F2
.N 0205	FA	.N 020E	B7
.N 0206	B6	.N 020F	02
.N 0207	F0	.N 0210	20
.N 0208	11	.N 0211	7E
		.N 0212	FF
		.N 0213	AB
		***.J 0200 To Start	

**Must be same as Loc. 0104

***Allow about 10 sec. of leader tape before starting. All underlined characters are user entries.

4-6. POWER SUPPLY CHECK (Figure 4-1)

The following Power Supply Check (Table 4-A) should always be completed before referring to any of the other tables when a problem is detected. This is to insure that proper voltage levels are being supplied to various ICs.

Table 4-A. Power Supply Check (Figure 4-1.)

STEP	INSTRUCTION	NORMAL INDICATION	IF CORRECT	IF INCORRECT
1	Monitor voltages from power supply a) Check Vcc at positive (+) end of C1 (Figure 4-1, zone C2). b) Check negative (-) end of C5 (zone B3).	a) Vcc = 4.8 - 5.2v (reg). b) Should be 11.5 to 12.5v (reg).	Proceed to Step 3.	Proceed to Step 2.
2	Monitor bus pins 13 (zone C4) and 72 (zone B4).	Bus pin 13 should be 7.5 to 10v (unreg) and pin 72 should be -14 to -18v (unreg).	There is a problem in the power supply circuit. Check for shorts or opens in appropriate line showing incorrect reading. If none are found, check voltage regulator (VR1), zener diode (D1) and associated components.	Possible problem on computer main board (see appropriate manual).
3	Monitor voltage inputs of each IC.	Proper operating voltages should be present.	Power supply is OK. Proceed to Write Circuit Check (be sure to read paragraph 4-7).	Examine connections at ICs and check lands for shorts or opens.

4-7. READ/WRITE TEST PROGRAM

Program 4-II should be used in conjunction with troubleshooting tables 4-B and 4-C. Program 4-II Reads and Writes a 32K test program which is always incrementing from 00 to FF (256 different patterns). However, the program may be set to any desired length. The Write length is set at location 010C (MSB) + 010D (LSB). The Read length is set at location 0213 (MSB) + 0214 (LSB). The Read length should be less than or equal to the Write length.

When the Write test is completed, control is returned to the Monitor. Errors occurring during the Read Test are printed as E, and when the Read test is completed, the number of errors plus one are listed at the terminal. If there are no errors, the print out reads 0001E. Note that the print out will occur until after the last byte of the test is read, and the noise at the end of the test causes the error count to print 0001E. If no noise is detected, there will be no print out.

Program 4-II. Read/Write Test

Write Test

```
.M 0100 C6
.N 0101 13
.N 0102 CE
.N 0103 00
.N 0104 00
.N 0105 09
.N 0106 26
.N 0107 FD
.N 0108 5A
.N 0109 26
.N 010A FA
.N 010B CE
.N 010C 80
.N 010D 00
.N 010E B6
.N 010F F0
.N 0110 10
.N 0111 2B
.N 0112 FB
.N 0113 F7
.N 0114 F0
.N 0115 11
.N 0116 5C
.N 0117 09
.N 0118 26
.N 0119 F4
.N 011A 7E
.N 011B FF
.N 011C AB
.J 0100 to start
```

Read Test

```
.M 0200 F6
.N 0201 F0
.N 0202 10
.N 0203 56
.N 0204 25
.N 0205 FA
.N 0206 F6
.N 0207 F0
.N 0208 11
.N 0209 26
.N 020A F5
.N 020B CE
.N 020C 00
.N 020D 00
.N 020E D[illegible]
.N 020F 00
.N 0210 4F
.N 0211 4C
.N 0212 CE
.N 0213 80
.N 0214 00
.N 0215 F6
.N 0216 F0
.N 0217 10
.N 0218 56
.N 0219 25
.N 021A FA
.N 021B F6
.N 021C F0
.N 021D 11
.N 021E 11
.N 021F 27
.N 0220 0E
.N 0221 DF
.N 0222 02
.N 0223 DE
.N 0224 00
.N 0225 08
.N 0226 DF
.N 0227 00
.N 0228 DE
.N 0229 02
.N 022A C6
.N 022B 45
.N 022C F7
.N 022D F0
.N 022E 01
.N 022F 4C
.N 0230 09
.N 0231 26
.N 0232 E2
.N 0233 C6
.N 0234 0D
.N 0235 BD
.N 0236 FF
.N 0237 81
.N 0238 C6
.N 0239 0A
.N 023A BD
.N 023B FF
.N 023C 81
.N 023D 96
.N 023E 00
.N 023F BD
.N 0240 FF
.N 0241 6D
.N 0242 96
.N 0243 01
.N 0244 BD
.N 0245 FF
.N 0246 6D
.N 0247 7E
.N 0248 FF
.N 0249 AB
.J 0200 to start
```

Table 4-B. Write Circuit Check (Figure 3-8)

STEP	INSTRUCTION	NORMAL INDICATION	IF CORRECT	IF INCORRECT
1	Monitor Write Clock at TP-10 (sheet 2, zone B4).	4800Hz Clock should be present.	Proceed to Step 4.	Proceed to Step 2.
2	Monitor C pin 2. 500KHz input (sheet 1, zone B4).	500KHz clock should be present.	Suspect U pin 5 (sheet 2, zone B4), R pin 10 (sheet 1, zone B1), D (zone B2), C (zone B3) and R pin 8 (zone B3).	Proceed to Step 3.
3	Monitor 500KHz inputs W pin 2 (zone A8) and V pin 3 (zone C7).	500KHz clock should be present.	Signal not reaching C pin 2 (zone B4).	Monitor for 2MHz Clock at bus pin 49. If correct, suspect R pin 12, Z pin 2 and Z pin 12. If incorrect, suspect problem with 680 computer.
4	Monitor Serial Write Data at TP-1 (zone A1).	Write data should be present (resembles waveform #3, page 77).	Proceed to Step 7.	Proceed to Step 5.
5	Monitor Board Select at TP-11 (sheet 2, zone D6).	Should be pulsing LOW.	Proceed to Step 6.	Check U pin 1, CC pin 8, BB pin 8, EE pins 2, 4, 6, and 10 and FF pins 2, 4, 6, 8, 10 and 12.
6	Monitor $\overline{\text{Write Data Strobe}}$ at TP-13 (sheet 2, zone C6).	Should resemble waveform #2, page 76.	Problem probably with UART-Y.	Suspect S pin 12, DD pin 6 or DD pin 2 or DD pin 4.
7	Monitor Modulated Write Data at TP-7 (sheet 1, zone A2).	Modulated Write Data should resemble Waveform #5, page 78.	Suspect E (zone C2) and associated components R10, C12, R9, R8, R5, C9 and C10.	Suspect modulator circuit, consisting of ICs K and A (zone B3).

Table 4-C. Read Circuit Check (Figure 3-8)

STEP	INSTRUCTION	NORMAL INDICATION	IF CORRECT	IF INCORRECT
1	Monitor Play In at TP-4 (sheet 1, zone D8).	Normal indication should resemble waveform #1, page 72,	Proceed to Step 2.	Data was not correctly written on the tape. Check connection. Trouble may be in tape recorder.
2	Monitor Read Filter Output at TP-2 (zone D5).	Should resemble waveform #2, page 72.	Proceed to Step 3.	1.8KHz Read Filter probably defective.
3	Monitor Squared Read Audio at TP-8 (zone C3).	Should resemble waveforms #1 and #2, page 72.	Proceed to Step 4.	Zero Crossing Detector probably faulty.
4	Monitor $\overline{\text{Read Status Strobe}}$ at TP-17 (sheet 2, zone D6).	Should be active LOW pulse.	Proceed to Step 5.	Monitor TP-11 (zone D6). If incorrect, problem with Board Select logic; if correct, suspect DD pin 10, DD pin 8, DD pin 2 or AA pin 6.
5	Monitor $\overline{\text{Read Data Strobe}}$ at TP-18 (sheet 2, zone D6).	Should resemble waveform #3, page 73.	Proceed to Step 6.	Suspect DD pin 4 (zone C6).
6	Monitor Edge Detector Output at TP-16 (sheet 1, zone C5).	Should resemble waveform #4, page 73. Pulse width = 2 µs. period = 416 µs. (logic Ø); Period = 208 µs. (logic 1).	Proceed to Step 8.	Proceed to Step 7.
7	Monitor Edge Detector Flip-flop at V pin 3 and V pin 1 (zone C7).	500KHz clock should be present.	Suspect V pin 12, V pin 2 (zone C7) or X pin 3 (zone C6).	Suspect Z pin 2, Z pin 12 (zone B7) R pin 12 or the absence of the 2MHz Clock at bus pin 49.
8	Monitor 38.4KHz clock at TP-12 (zone A7).	38.4KHz clock should be present (resemble waveform #4, page 73)	Proceed to Step 9.	Suspect W (zone A7) to be defective.
9	Monitor 9.6KHz Read Clock Generator Shift Clock at TP-5 (zone B5).	9600Hz should be present (resembles waveform #6, page 74).	Proceed to Step 10.	Suspect ÷ by 4 Counter B pin 2 or B pin 12 (check for 38.4KHz Clock at B pin 3).

STEP	INSTRUCTION	NORMAL INDICATION	IF CORRECT	IF INCORRECT
10	Monitor Read Data Discriminator Counter at TP-9 (zone A5).	Should resemble waveform #6, page 74.	Proceed to Step 11.	÷ by 12 Counter, N, may be defective. Check inverters R pin 4 and R pin 6 and NOR gate P pin 9.
11	Monitor Read Data at TP-15 (sheet 2, zone B5).	Should resemble waveform #7, page 75.	Proceed to Step 12.	Suspect J pin 12 or NOR gate U pin 13 (sheet 1, zone B4).
12	Monitor Read Clock at TP-14 (sheet 2, zone A5).	Should resemble waveform #6, page 74.	Suspect the UART line drivers GG and HH to be defective.	Check Read Clock Generator H pin 1, H pin 13 and J pin 1. If correct, check X pin 4, X pin 11, P pin 3 and P pin 11.

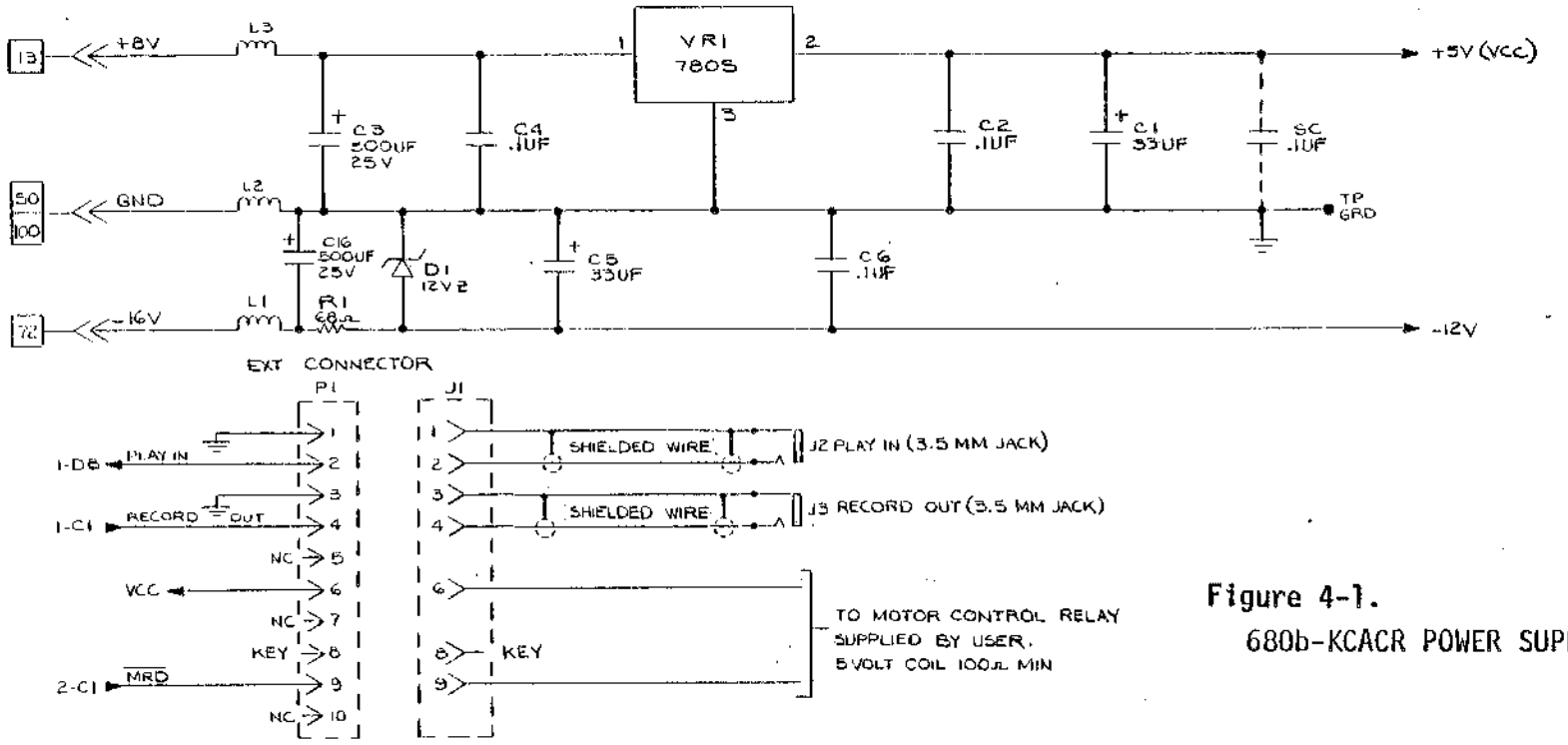


Figure 4-1.
680b-KCACR POWER SUPPLY

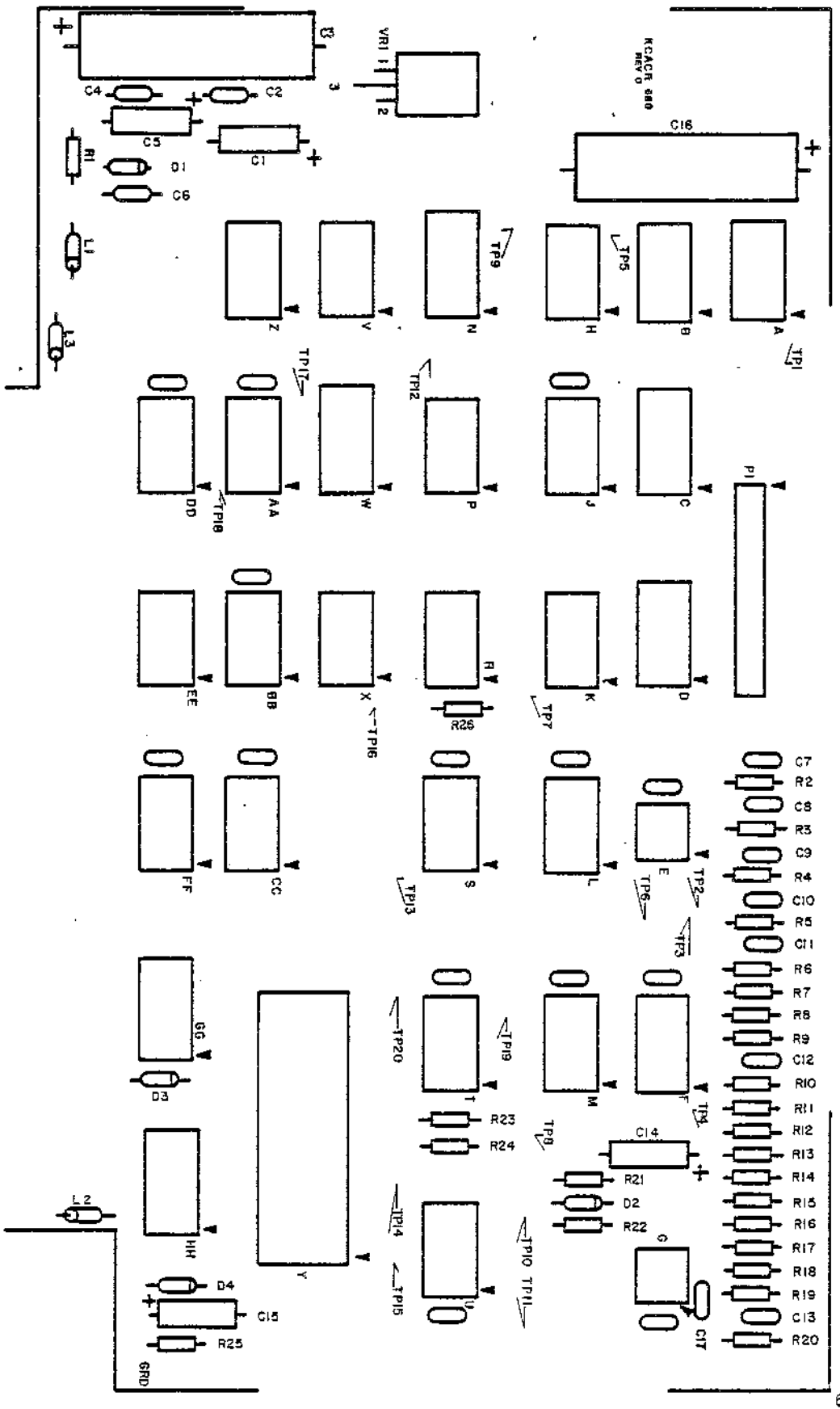


Figure 4-2. 680b-KCACR Component Layout

KCACR

SECTION V
ASSEMBLY

5-1. GENERAL

This section contains all the information needed for circuit construction of the Altair 680b-KCACR board. It consists of some helpful assembly hints and detailed instructions for component installation on the 680b-KCACR board.

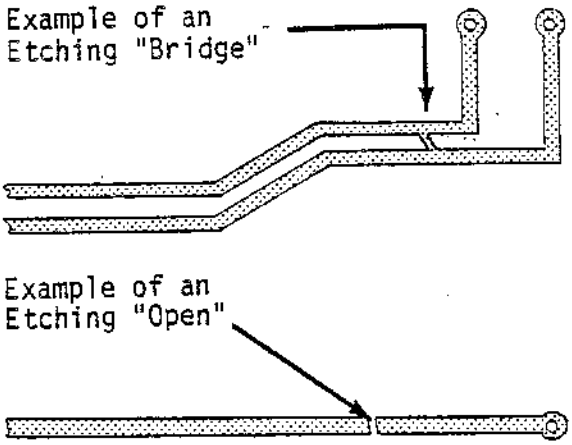
Before beginning the assembly procedure, carefully read the enclosed "MITS Kits Assembly Hints" booklet. It contains helpful suggestions and several important warnings. Failure to heed these warnings could cause you to void your warranty.

Check the contents of your kit against the parts list (Appendix A) to make sure you have the required parts. As you construct the board, read each step carefully and follow the instructions in the order in which they are presented. Always complete each step before going on to the next.

5-2. VISUAL INSPECTION

It is recommended that a visual inspection of the PC board(s) in your kit be made before beginning the assembly procedures.

Look for etching "bridges" or etching "opens" in the printed circuit lands, as shown in the drawings below:



This could also appear as a "hairline" cut.

A thorough visual inspection will eliminate one possibility for errors, should the board not operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

5-3. COMPONENT INSTALLATION INSTRUCTIONS

Pages 94 through 99 describe the proper procedures for installing various types of components in your kit.

Read these instructions very carefully and refer back to them when necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void your warranty.

More specific instructions, or procedures of a less general nature, will be included within the assembly text itself.

Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

Figure 5-1 is a typical silkscreen reproduction provided to assist in locating components being installed, previously installed components, and components yet to be installed.

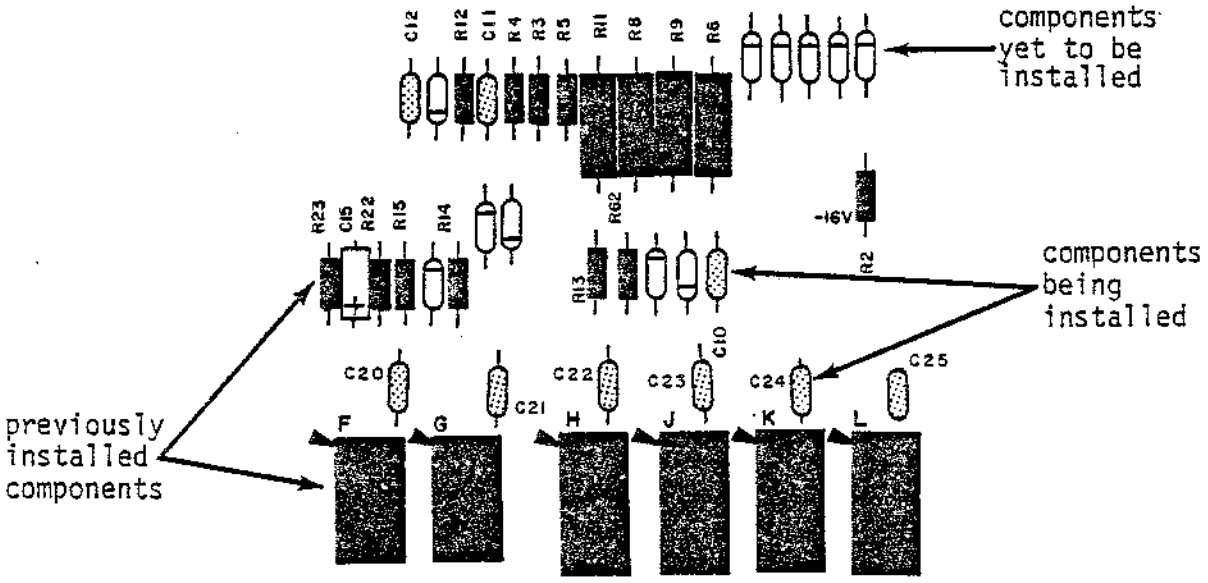
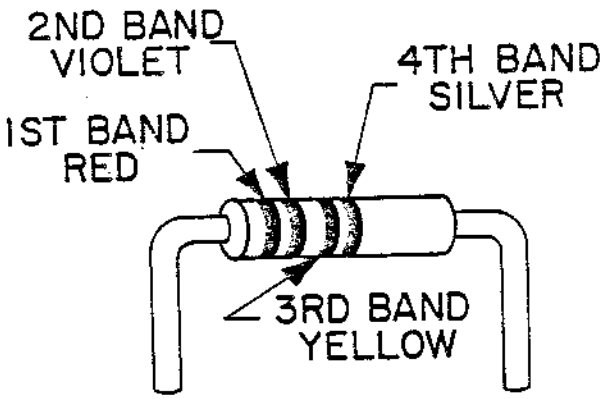


Figure 5-1. Typical Silkscreen

5-4 Resistor Installation

Resistors have four (or possibly five) color-coded bands as represented in the chart below. The fourth band is gold or silver and indicates the tolerance. NOTE: In assembling a MITS kit, you need only be concerned with the three bands of color to the one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example: a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. By looking at the chart below, you see that red is 2 and violet 7. By multiplying 27 by the yellow multiplier band (10,000), you find you have a 270,000 ohm (270K) resistor. The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the manual.



RESISTOR COLOR CODES		
COLOR	BANDS 1&2	3rd BAND (Multiplier)
Black	0	1
Brown	1	10^2
Red	2	10^3
Orange	3	10^4
Yellow	4	10^5
Green	5	10^6
Blue	6	10^7
Violet	7	10^8
Gray	8	10^9
White	9	

Use the following procedure to install the resistors onto the boards. Make sure the colored bands on each resistor match the colors called for in the list of Resistor Values and Color Codes given in the assembly instructions.

1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the PC board.

2. Install the resistor into the correct holes on the silk-screened side of the PC board.

3. Holding the resistor in place with one hand, turn the board over and bend the two leads slightly outward.

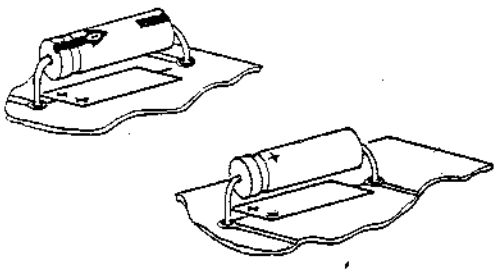
4. Solder the leads to the foil pattern on the back side of the board; the clip off any excess lead lengths.

5-5 Capacitor Installation Instructions

A. Electrolytic Capacitors

Polarity must be noted on electrolytic capacitors before they are installed.

The electrolytic capacitors contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following.



ELECTROLYTIC CAPACITOR

One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there will be a negative (-) sign. The capacitor must be oriented so the arrow points to the negative side.

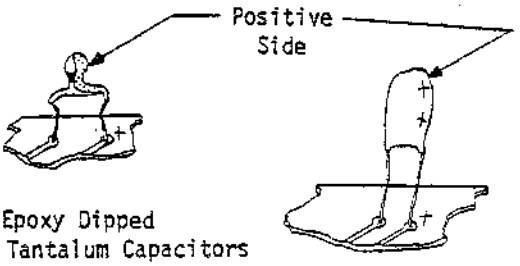
Install the electrolytic capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board, aligning the positive side with the "+" signs printed on the board.
2. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

B. Epoxy Dipped Tantalum, Epoxy Dipped Ceramic, and Ceramic Disk Capacitors

Polarity must be noted on epoxy dipped tantalum capacitors before they are installed.

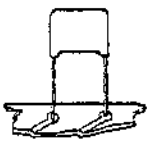
There are two types of epoxy dipped tantalum capacitors contained in you your kit. The first type is blue on the positive side. The second type is marked with "+" signs on the positive side. Both types of epoxy dipped tantalum capacitors are shown in the drawings below.



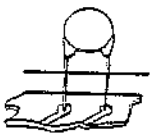
Epoxy Dipped Tantalum Capacitors

The epoxy dipped ceramic capacitors and the ceramic disk capacitors are non-polarized.

These two types of capacitors are shown in the drawings below.



Epoxy Dipped Ceramic Capacitor



Ceramic Disk Capacitor

Install these 4 types of capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two capacitor leads to conform to their respective holes on the board.
2. Insert the capacitor into the correct holes from the silk-screened side of the board. Holding the capacitor in place, turn the board over and bend the two leads slightly outward.
3. Solder the two leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

5-6 Diode Installation

NOTE: Diodes are marked with a band on one end indicating the cathode end. Each diode must be installed so that the end with the band is oriented towards the band printed on the PC board. Failure to orient the diodes correctly may result in permanent damage to your unit.

DIODE

Use the following procedure to install diodes onto the board. Refer to the list of Diode Part Numbers included for each board to make sure you install the correct diode each time.

1. Bend the leads of the diode at right angles to match their respective holes on the board.

2. Insert the diode into the correct holes on the silk screen, making sure the cathode end is properly oriented. Turn the board over and bend the leads slightly outward.

3. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

5-7. IC Installation

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the PC board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Identification Chart to identify Pin 1.

To prepare ICs for installation:
All ICs are damaged easily and should be handled carefully -- especially static-sensitive MOS ICs. Always try to hold the IC by the ends, touching the pins as little as possible. When you remove the IC from its holder, CAREFULLY straighten any bent pins using needle-nose pliers. All pins should be evenly spaced and should be aligned in a straight line, perpendicular to the body of the IC itself.

A. Installing ICs without sockets:

1. Orient the IC so that Pin 1 coincides with the arrowhead on the PC board.

2. Align the pins on one side of the IC so that just the tips are inserted into the proper holes on the board.

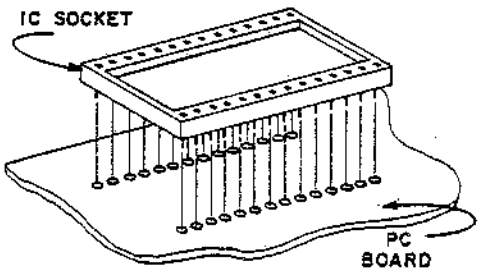
3. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all the pins have been started into their holes, push the IC into the board the rest of the way. Tape the IC to the board with a piece of masking tape.

4. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

WARNING:
Make sure none of the pins have been pushed underneath the IC during insertion.

B. Installing ICs with sockets:

1. Referring to the drawing below, set the IC socket into the designated holes on the board and secure it with a piece of masking tape.



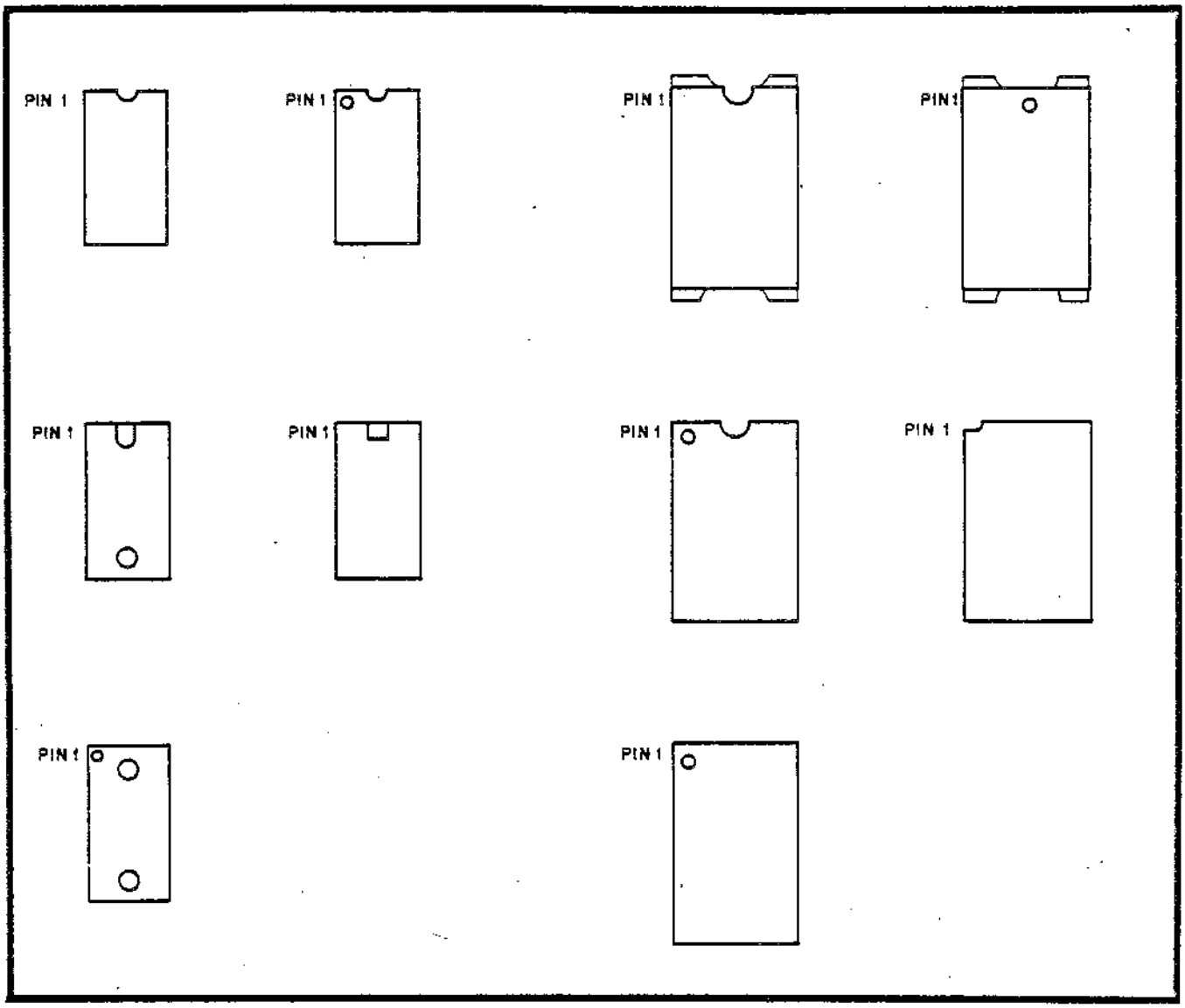
2. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

3. Orient the IC over the socket so that Pin 1 coincides with the arrowhead on the PC board.

4. Align the pins on one side of the socket so that just the tips are inserted into the holes.

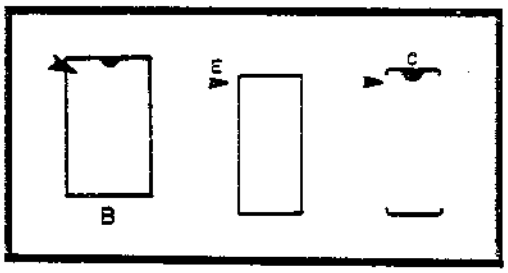
5. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. When the tips of all the pins have been started into their holes, push the IC into the socket the rest of the way.

5-8. IC Identification Chart



INTEGRATED CIRCUITS (IC's) CAN COME WITH ANY ONE OF, OR A COMBINATION OF, SEVERAL DIFFERENT MARKINGS. THESE MARKINGS ARE VERY IMPORTANT IN DETERMINING THE CORRECT ORIENTATION FOR THE IC's WHEN THEY ARE PLACED ON THE PRINTED CIRCUIT BOARDS. REFER TO THE ABOVE DRAWING TO LOCATE PIN 1 OF THE IC's, THEN USE THIS INFORMATION IN CONJUNCTION WITH THE INFORMATION BELOW TO PROPERLY ORIENT EACH IC FOR INSTALLATION.

WARNING: INCORRECTLY ORIENTED IC's MAY CAUSE PERMANENT DAMAGE!



THE DRAWING ON THE LEFT INDICATES VARIOUS METHODS USED TO SHOW THE POSITION OF IC's ON THE PRINTED CIRCUIT BOARDS. THESE ARE SILK-SCREENED DIRECTLY ON THE BOARD. THE ARROWHEAD INDICATES THE POSITION FOR PIN 1 WHEN THE IC IS INSTALLED.

5-9. MOS IC Special Handling Precautions

There are several MOS integrated circuits contained in this kit. These IC's are very sensitive to static electricity and transient voltages. In order to prevent damaging these components, read over the following precautions and adhere to them as closely as possible. FAILURE TO DO SO MAY RESULT IN PERMANENT DAMAGE TO THE IC.

1) All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface and the IC itself along with its container. This can be accomplished by continuous physical contact with the work surface, the components, and everything else involved in the operation.

2) When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself.

3) If the IC has to be moved from one container to another, touch both containers before doing so.

4) Do not wear clothing which will build up static charges. Preferably wear clothing made of cotton rather than wool or synthetic fibers.

5) Always touch the PC board before touching the IC to the board. Try to maintain this contact as much as possible while installing the IC.

6) Handle the IC by the edges. Avoid touching the pins themselves as much as possible.

7) Dry air moving over plastic can build up considerable static charges. Avoid placing the IC near any such area or object.

8) In general, never touch anything to the IC that you have not touched first while touching both it and the IC itself.

5-10. DIODE INSTALLATION (Figure 5-2)

Install diodes D1 through D4 (Bag 4) according to the Diode Installation Instructions on page 96.

Diode	Part Number
( ) D1	1N4742 (12v Zener)
( ) D2, D4	1N914
( ) D3	1N4004

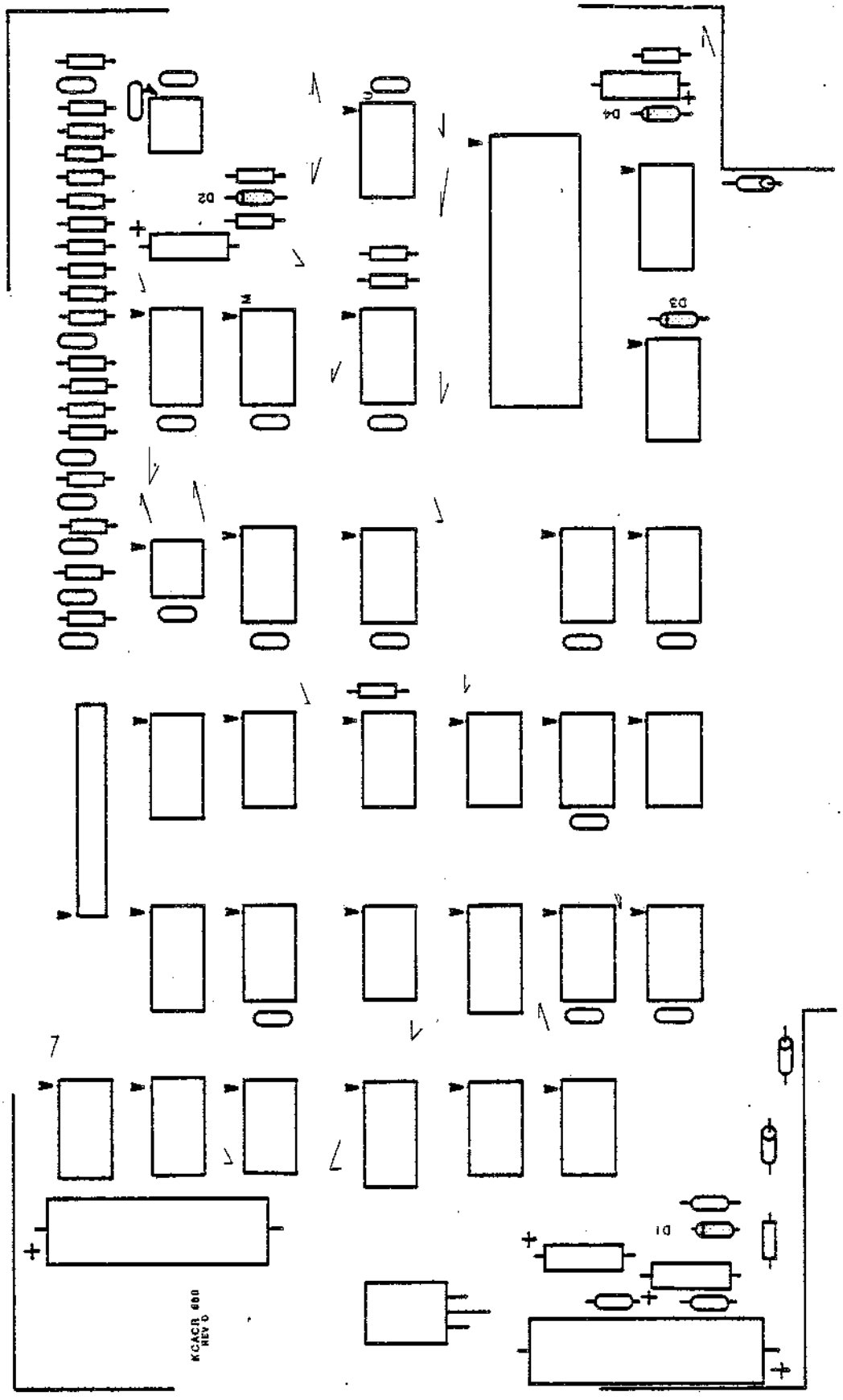


Figure 5-2. Diode Installation

5-11. RESISTOR INSTALLATION (Figure 5-3)

There are 26 resistors (Bag 2) to be installed on the board. Install these resistors according to the Resistor Installation Instructions on page 94.

> NOTE
>
> Save the excess leads for use in Paragraph 5-13.

The following chart shows the silkscreen designation, values and color codes of the supplied resistors.

Silkscreen Designation	Value
( ) R1	68 ohm (blue, gray, black) 1/2W
( ) R2, R8	91K ohm (white, brown, orange) 1/2W
( ) R3, R4	390K ohm (orange, white, yellow) 1/2W
( ) R5, R11	33K ohm (orange, orange, orange) 1/2W
( ) R6, R12, R23, R24	10K ohm (brown, black, orange) 1/2W
( ) R7, R26	1K ohm (brown, black, red) 1/2W
( ) R9	1.5K ohm (brown, green, red) 1/2W
( ) R10	22K ohm (red, red, orange) 1/2W
( ) R13	3K ohm (orange, black, red) 1/2W
( ) R14	4.3K ohm (yellow, orange, red) 1/2W
( ) R15, R19	100K ohm (brown, black, yellow) 1/2W
( ) R16	10M ohm (brown, black, blue) 1/2W
( ) R17	15K ohm (brown, green, orange) 1/2W
( ) R18, R21, R22	4.7K ohm (yellow, violet, red) 1/2W
( ) R20	5.6K ohm (green, blue, red) 1/2W
( ) R25	220 ohm (red, red, brown) 1/2W

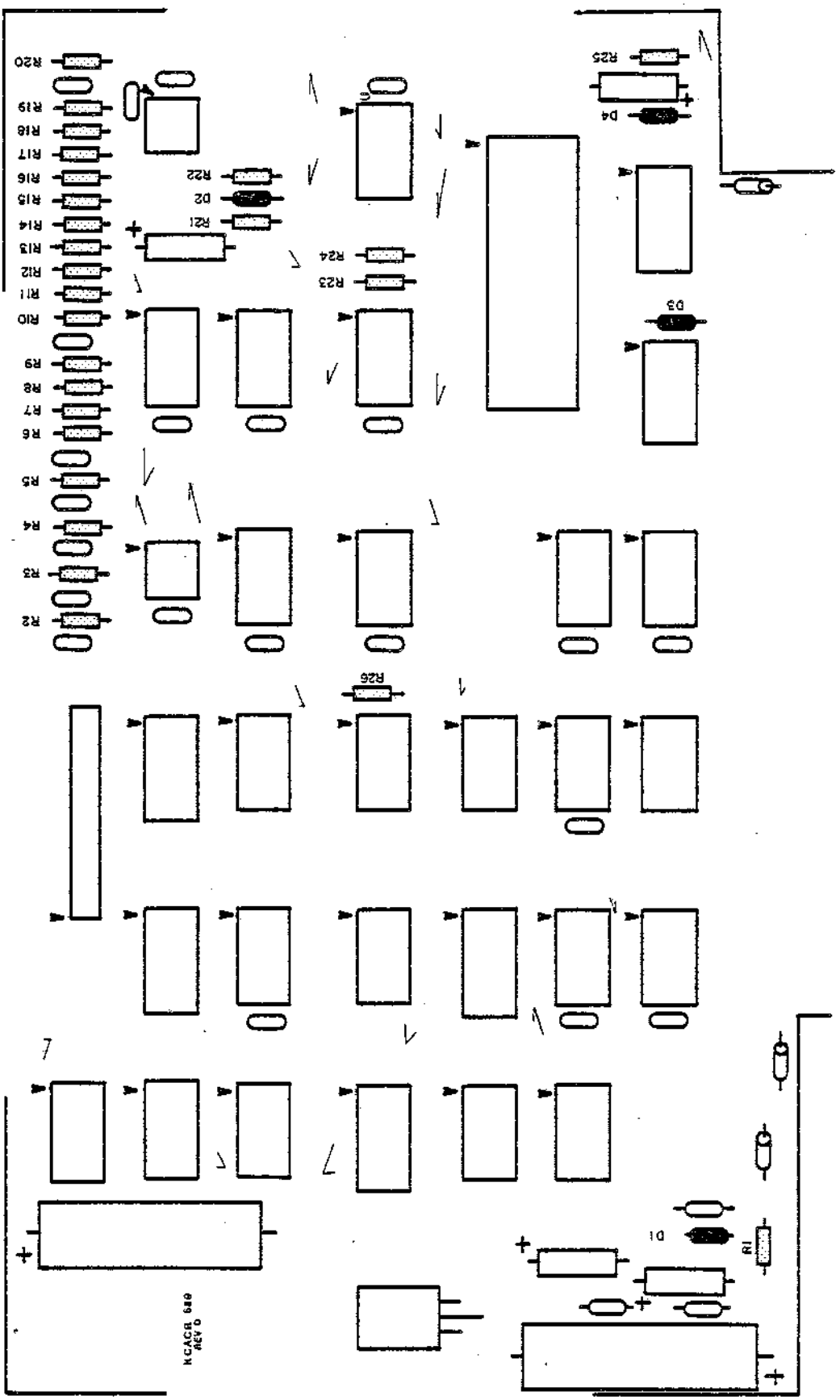


Figure 5-3. Resistor Installation

5-12. IC SOCKET INSTALLATION (Figure 5-4)

Install the 31 IC sockets (Bag 7) according to the Integrated Circuit Installation Instructions on page 97.

> CAUTION
>
> Insure that solder bridges are not formed and do NOT install ICs in sockets at this time.

Socket	Size
( ) E, G	8-pin
( ) C, D, N, W, GG, HH	16-pin
( ) Y	40-pin
( ) All remaining sockets	14-pin

5-13. FERRITE BEAD INSTALLATION (Figure 5-4)

Install the three ferrite beads, L1, L2 and L3 (Bag 5), on the board according to the following instructions.

1. Using a resistor lead saved from paragraph 5-11, cut a one-inch lead length.

2. Insert the lead through the bead and bend the ends to conform to the designated holes on the board.

3. Insert the lead into the silk-screened (top) side of the board and solder to the foil (bottom) side of the board. Be careful not to leave any solder bridges.

4. Clip off any excess lead lengths.

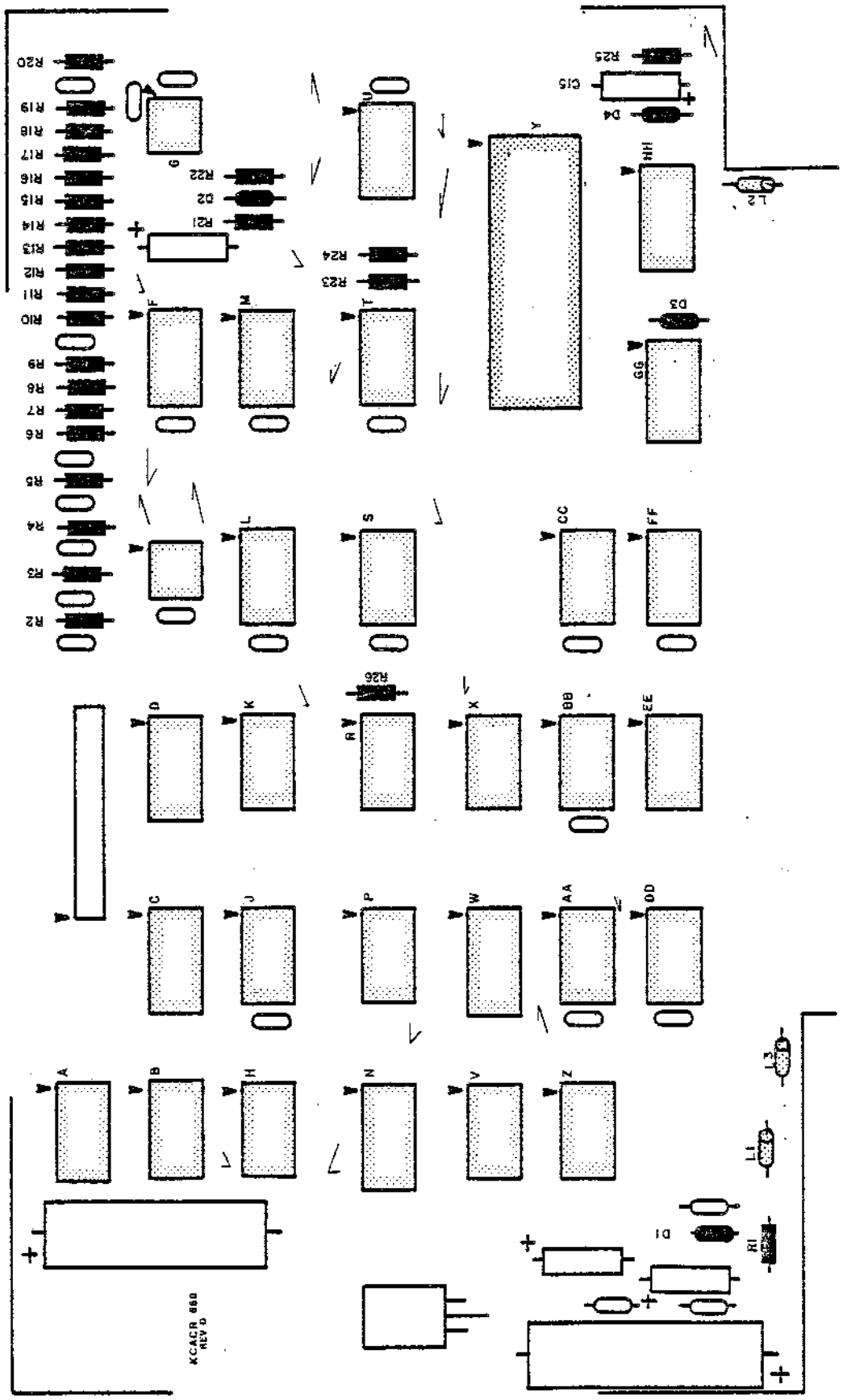


Figure 5-4. IC Socket and Ferrite Bead Installation

5-14. TERMINAL TEST POINT INSTALLATION (Figure 5-5)

Install test points TP-1 through TP-20 (Bag 5) on the board according to the following instructions.

> NOTE
>
> A 21st test point is installed in slot marked GRD.

1. Insert the pin through the silkscreened (top) side of the board and solder it in place on the silkscreened side.

2. Turn the board over and solder the pin on the foil (bottom) side of the board.

3. Return the board to the silkscreened (top) side of the board. Resolder the pin and straighten it if necessary.

> NOTE
>
> Do not clip off the portion of the test point that protrudes from the bottom of the PC board since it can be used during testing and troubleshooting.

5-15. CAPACITOR INSTALLATION (Figure 5-5)

There are three types of capacitors to be installed on the 680b-KCACR board (Bag 3). The electrolytic capacitors should be installed according to the Capacitor Installation Instructions, Section A, on page 95. The ceramic disk and mica capacitors are non-polarized and should be installed according to the Capacitor Installation Instructions, Section B, on page 95.

Silkscreen Designation	Type	Value
( ) C1	electrolytic	33µf, 35v
( ) C2	ceramic disk	.1µf, 50v
( ) C3	electrolytic	470µf or 500µf, 16-25v
( ) C4	ceramic disk	.1µf, 50v
( ) C5	electrolytic	33µf, 35v
( ) C6	ceramic disk	.1µf, 50v
( ) C7	mica	910 pf
( ) C8	mica	910 pf
( ) C9	mica	820 pf
( ) C10	mica	820 pf
( ) C14	electrolytic	33µf, 35v
( ) C15	electrolytic	33µf, 35v
( ) C16	electrolytic	470 or 500µf, 16-25v
( ) C17	ceramic disk	470 pf

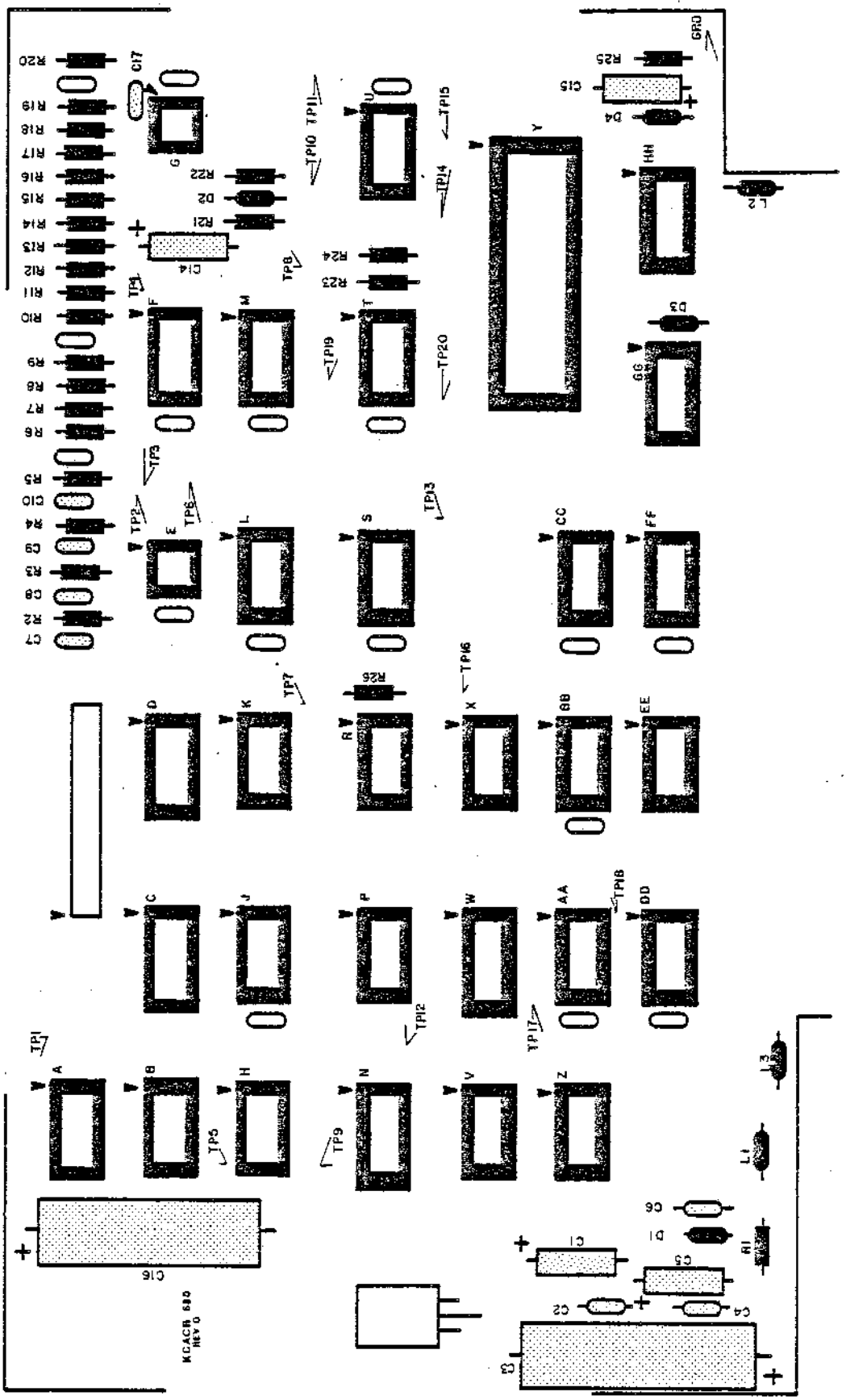


Figure 5-5. Test Point and Capacitor Installation

5-16. SUPPRESSOR CAPACITOR INSTALLATION (Figure 5-6)

There are seventeen capacitors (Bag 8) to be installed, 14 of which are used for noise suppression. They have no individual component designations, but are shown on the silk-screen as small oval shapes. Install the capacitors according to the Ceramic Disk Capacitor Installation Instructions on page 95.

Suppressor Capacitor	Value
( ) 14 Ceramic Disk suppressor capacitors	.1uf, 16v

The remaining 3 capacitors are used in the amplifier circuit.

Suppressor Capacitor	Value
( ) C11, C12, C13	.1uf, 16v

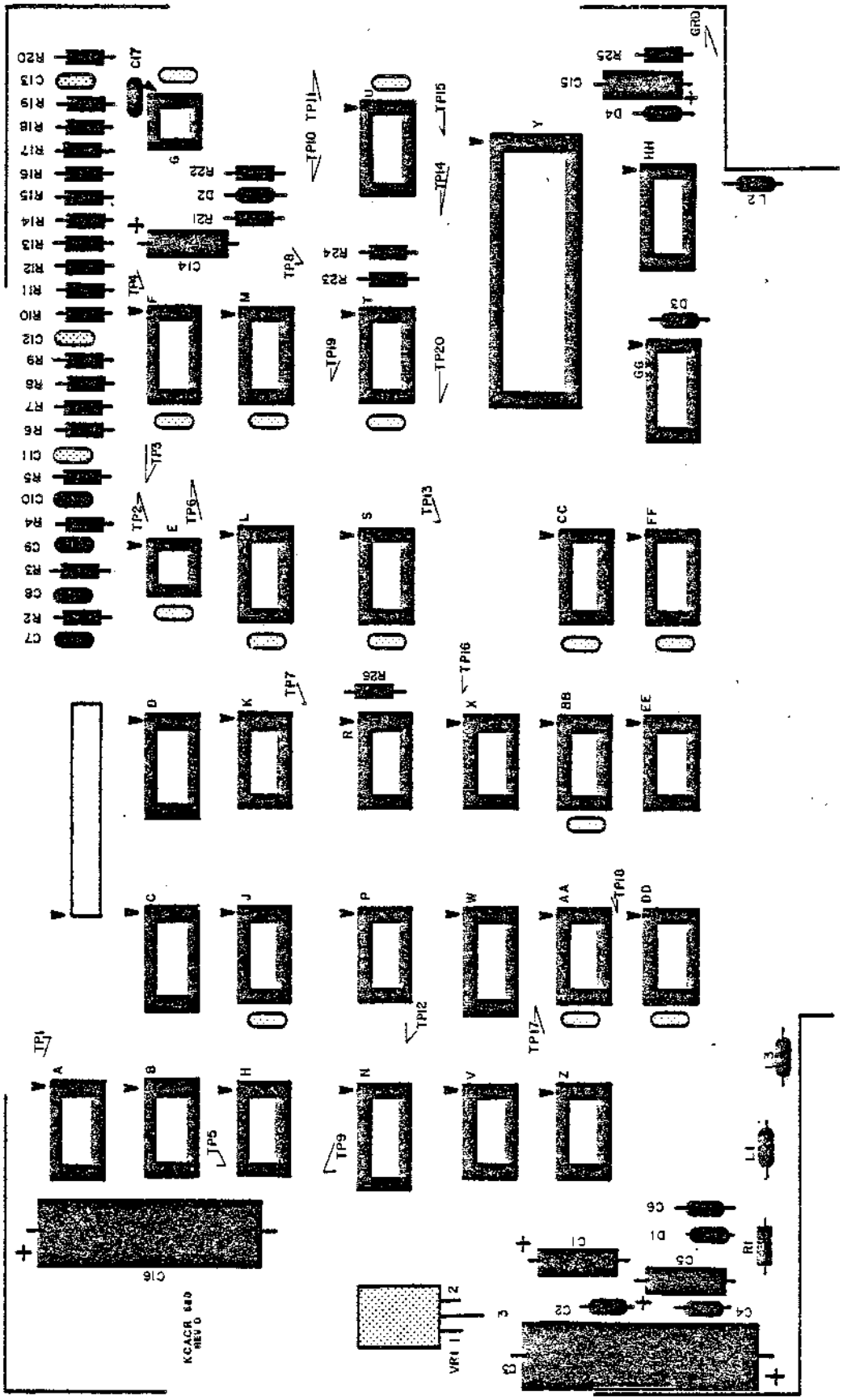


Figure 5-6. Suppressor Capacitor Installation

5-17. VOLTAGE REGULATOR INSTALLATION (Figure 5-7)

Install VR1 with heat sink (Bag 1) according to the following instructions.

1. Set the regulator in place on the silkscreened side of the board, aligning the leads with their designated holes.

2. Use needle-nose pliers to bend the three leads at right angles to conform to their proper holes on the PC board.

> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all metal surfaces which come in contact with each other.

3. Referring to Figures 5-6 and 5-7, set the regulator and heat sink in place on the silkscreened side of the board. Secure them in place with a #6-32 x 3/8" screw, a #6-32 nut and a #6 lockwasher.

4. Solder the three leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges.

5. Clip any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1	7805

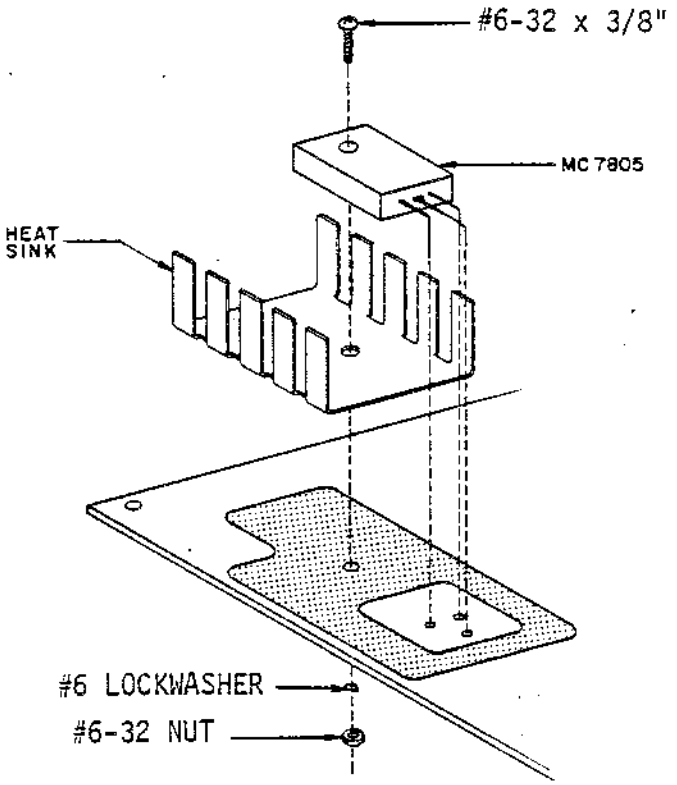


Figure 5-7. Voltage Regulator Orientation

5-18. RIGHT ANGLE PLUG INSTALLATION (Figure 5-8)

The 10-pin male connector, P1 (Bag 5) is installed on the 680b-KCACR board according to the following instructions.

1. Insert the short pins into their designated holes on the silk-screened (top) side of the board with Right Angle pins pointing to the edge of the board (away from components).

2. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges, and clip off any excess lead lengths.

5-19. IC INSTALLATION (Figure 5-8)

Install the following integrated circuits (Bag 1) on the 680b-KCACR board according to the Integrated Circuit Installation Instructions, Section B, on page 97.

IC	Part Number
( ) E	LM358
( ) F, M	74LS74
( ) G	LM393
( ) L, U	74LS02
( ) S, AA	74LS10
( ) T	74LS38
( ) Y	COM2502 or AY-5-1013
( ) BB, CC	74LS30
( ) DD, EE, FF	74LS14
( ) GG, HH	74367 or 8T97

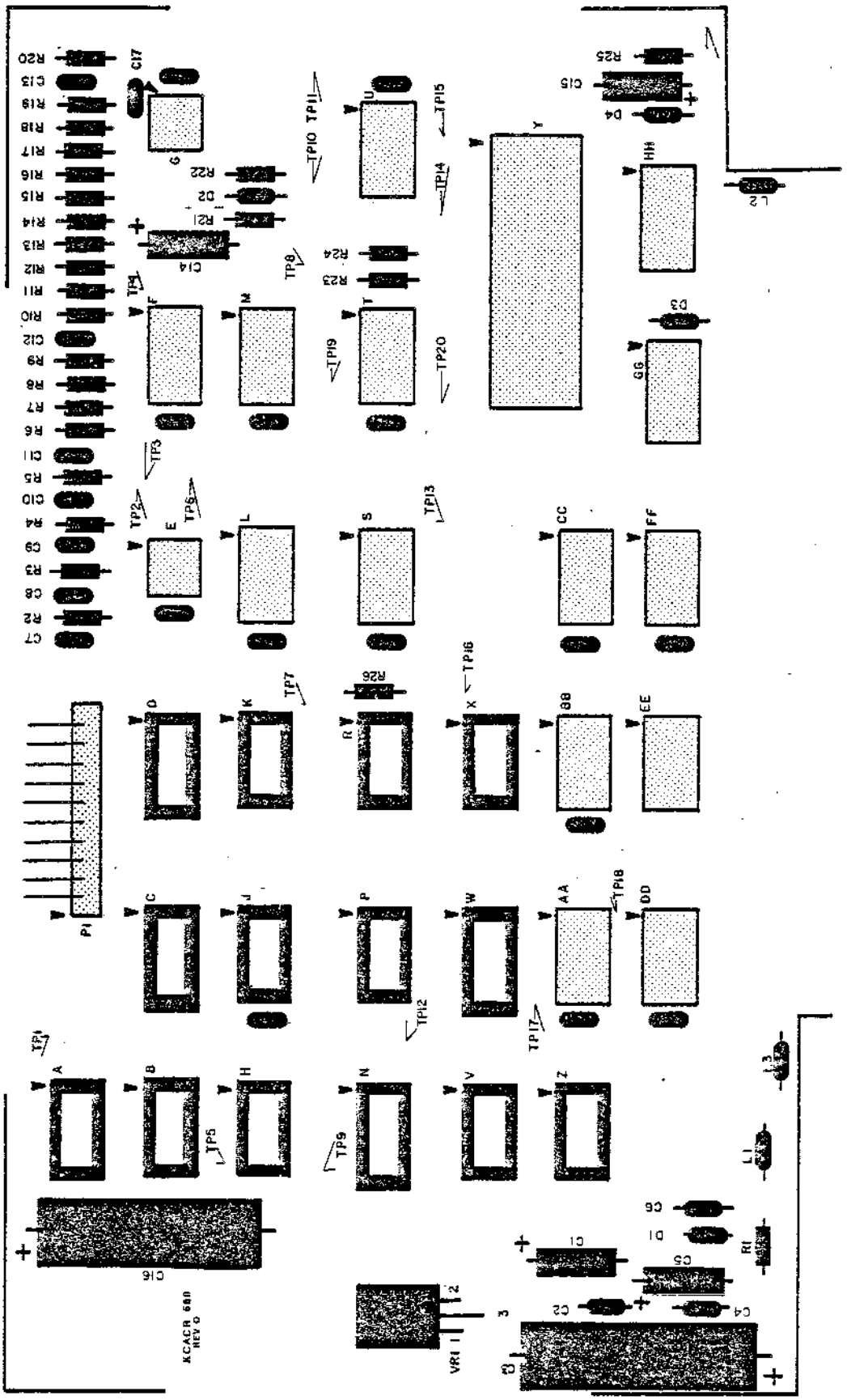


Figure 5-8. Right Angle Plug and IC Installation

5-20. CMOS IC INSTALLATION (Figure 5-9)

Install the following fourteen CMOS ICs (Bag 1) on the 680b-KCACR board according to the Integrated Circuit Installation Instructions, Section B, on page 97. Refer to page 99 for special handling instructions of the CMOS ICs. Failure to carefully follow these instructions may result in permanent damage to the static sensitive ICs.

IC	Part Number
( ) A	4081
( ) B, H, J, K, V, Z	4013
( ) C, W	40161 or 74C161
( ) D	4022
( ) N	4029
( ) P	4001
( ) R	4069 or 74C04
( ) X	4030

NOTE

It is also recommended that a piece of aluminum foil be placed along the card stab connector when installing the ICs so that the pins of the IC are at the same potential. This will reduce the possibility of static damage to the CMOS ICs during assembly.

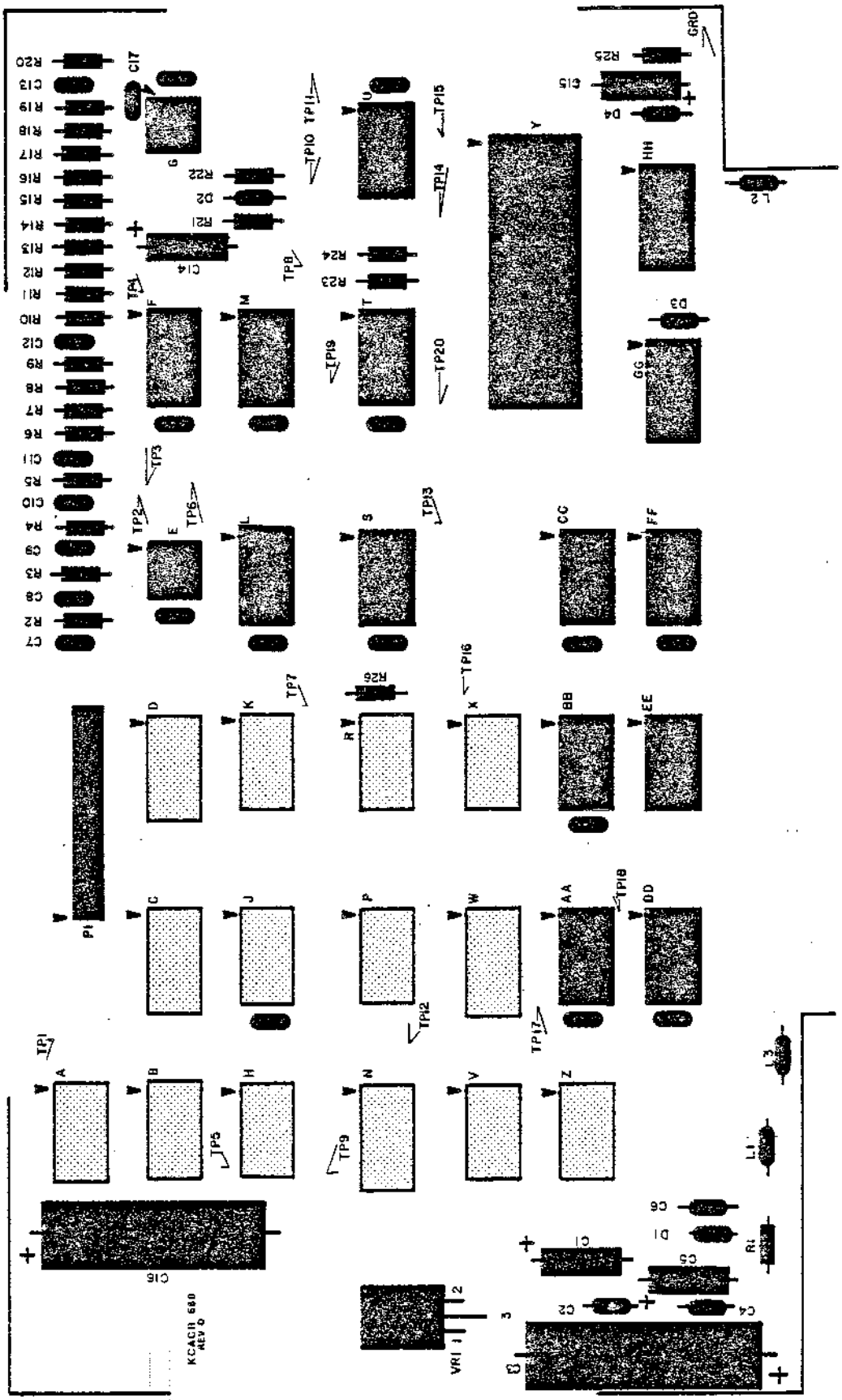


Figure 5-9. CMOS IC Installation

1. I/O INTERFACE CABLE ASSEMBLY

1. There are two 15-inch lengths of shielded cable provided with your kit (Bag 6). Using a small sharp knife, strip 1 inch of the outer insulation from both ends of each of the two cables. Do this by cutting a small circle 1 inch from the end around the cable and pulling the insulation off. Save the pieces you pull off for later use.

2. Separate the shielding from the inner wire, and twist its strands together as tightly as possible on each end.

3. Using a small sharp knife, strip 1/8 inch of insulation from the ends of the inner wires of both cables.

4. Cut 2 pieces of the insulation saved from step 1 and place them over the shielding wire on one end of each cable so that only 1/4 inch of bare wire protrudes.

5. Referring to Figure 5-10, install a connector pin to each of the four wires on one end of each cable by crimping the wire into place and soldering the end to the pin itself.

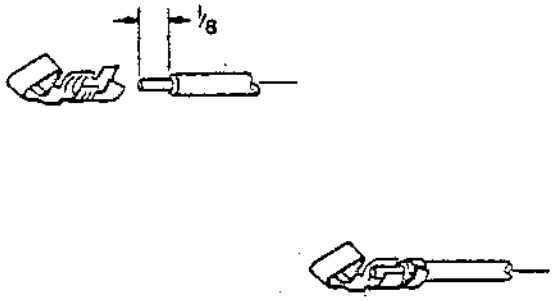


Figure 5-10. Pin Installation

6. Refer to Figure 5-11. Note that the slots in the female socket are numbered from 1 to 10 on the face of the socket. Insert the shield (ground) pin (pin attached to shield wire) of one of the cables into slot 1 and the pin attached to the inner wire into slot 2. This cable should be labelled PLAY IN.

7. Insert the shield (ground) pin (pin attached to shield wire) of the other cable into slot 3 and the remaining (inner wire) pin into slot 4. This cable should be labelled RECORD OUT.

> NOTE
>
> Fill the blank sockets of the 10-pin female connector with the remaining unused pins.

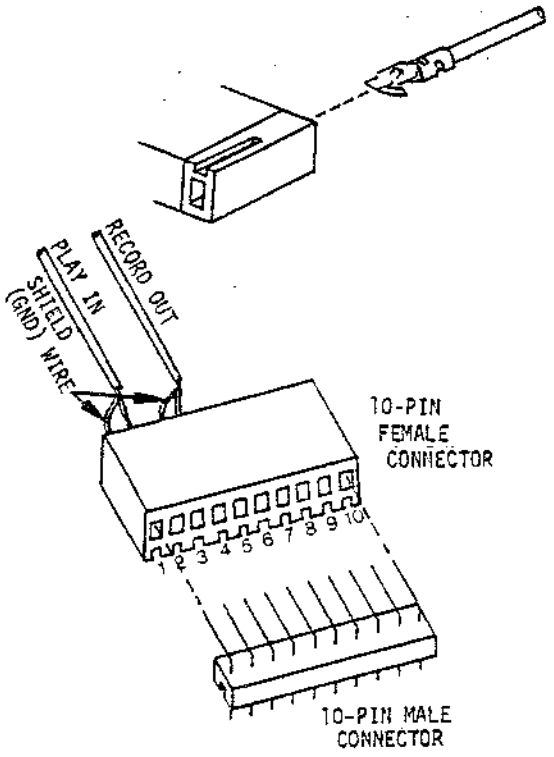


Figure 5-11. Inserting Pins in 10-Pin Female Socket

8. Referring to Figure 5-12, cut two pieces of the insulation saved from step 1 and place them over the shielding on the opposite end of the two cables so that only 1/8 inch of bare shielding protrudes. The two miniature phone jacks included in your kit have three solder terminals on them. One of the solder terminals is connected directly to the center metal portion of the jack which runs through to the mounting threads. Solder the shielding wire from each cable to this solder terminal on each phone jack.

9. Position the jack as shown in Figure 5-12. There are two mechanical contacts on each jack. One is squared (outside position) and the other is curved and on the inside position. The center of the three solder terminals is connected to the curved contact. Solder the inner wires of each cable to the center solder terminal (described above) of each jack.

10. Check the connections on both jacks to be sure there are no shorts and that the connections touch no other portion of the jacks but the solder terminals.

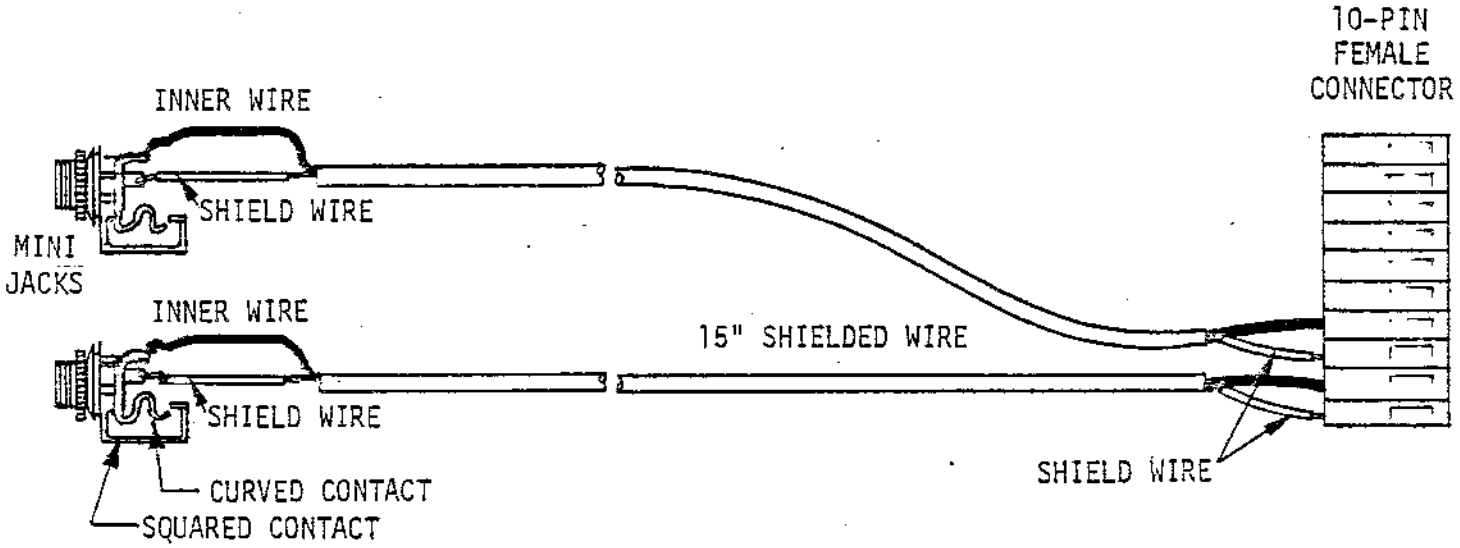


Figure 5-12. Mini Jack and Cable Assembly

5-22. I/O CABLE INSTALLATION

The two phone jacks can now be mounted onto the Altair 680b back panel in the slot marked P2.

1. Remove the mounting hardware from the two phone jacks. Mount the phone jacks on the metal plate containing three holes, leaving the center hole open.

2. Remove the solid plate covering slot P2 on the Altair 680b computer.

3. Using the same 4-40 screws and 4-40 nuts, mount the plate with the jacks installed on it to the 680b back panel from inside the case.

4. Remove the backing from the label "TAPE RECORD OUT" and place the label on the outside of the back panel next to the jack connected to the cable labelled "RECORD OUT".

5. Remove the backing from the other label and place it next to the other jack in the same manner.

6. Remove the tape labels from the two cables.

7. Attach the female connector on the opposite end of the two cables to the 10-pin male connector on the 680b-KCACR board. Pin 1 corresponds to pin 1 of the 10-pin male (right angle) connector (pin 1 is the pin nearest the arrow on the printed circuit board).

5-23. 680b-KCACR BOARD INSTALLATION

Before installing the 680b-KCACR board, refer to Section IV, paragraph 4-2, page 69, and perform the visual checks. When this is completed, make sure the 680b-MB Expander Card is correctly installed according to the instructions enclosed with the card. The 680b-KCACR board is connected to the Expander Card with a 100-pin edge connector, and is installed horizontally above the 680b Main Board with two threaded standoffs. Install the 680b-KCACR according to the following instructions.

5-24. Installation of 100-Pin Edge Connector Onto Expander Card (Figure 5-13)

1. Remove the Expander card from the socket on the 680b Main board.

2. Orient the 100-pin edge connector (Bag 6) over the two rows of holes at the lowest unused position on the Expander Card.

3. Insert the connector pins into their respective holes. It may be necessary to guide the pins with the tip of a small screwdriver. Insure that the 100-pin connector is tight against the board and that all 100 pins are in their respective holes.

4. Secure the connector to the card with two #4-40 x 1/2" screws and two #4-40 nuts (Bag 5).

5. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges.

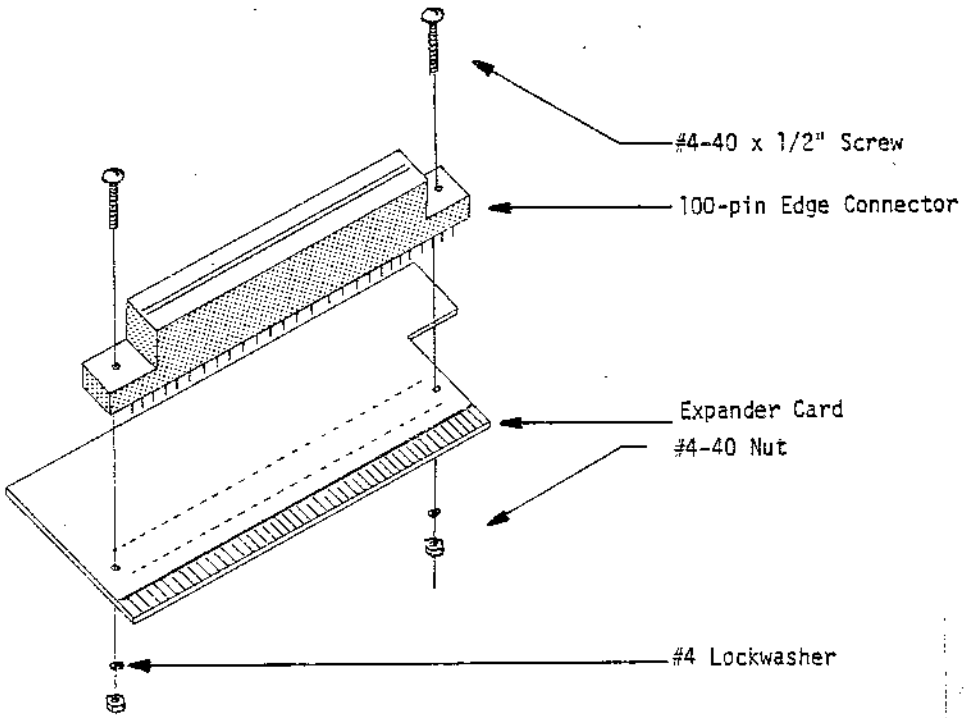


Figure 5-13. Installation of 100-Pin Edge Connector Onto Expander Card

5-25. Installation of Threaded Standoffs Onto 680b Main Board (Figure 5-14)

> NOTE
>
> If this board is not being installed in the lowest position on the Expander card, proceed to Paragraph 5-26.

1. Carefully remove the 680b Main board from the case. Referring to Figure 5-14, insert a #6-32 x 7/8" threaded standoff (Bag 5) with three #6 lockwashers (Bag 5) in the mounting holes provided on each side of the Main board.

2. Secure each standoff by placing a #6 lockwasher and a #6-32 nut on the bottom of the board.

3. Properly replace the 680b Main board in the case as shown on pages 69-70 in the 680b Assembly Manual.

5-26. 680b-KCACR FINAL INSTALLATION

1. Replace the Expander card into its socket on the 680b Main board.

2. Insert the card stab connector of the KCACR board (silkscreened side up) into the 100-pin edge connector on the Expander card.

3. Before securing the KCACR board, refer to Section 4, Paragraph 4-5, and perform an operational check to insure that the board is operating properly.

4. Secure the board in place by inserting a #6-32 x 3/8" screw with a #6 lockwasher into the top of each of the threaded standoffs as shown in Figure 5-14.

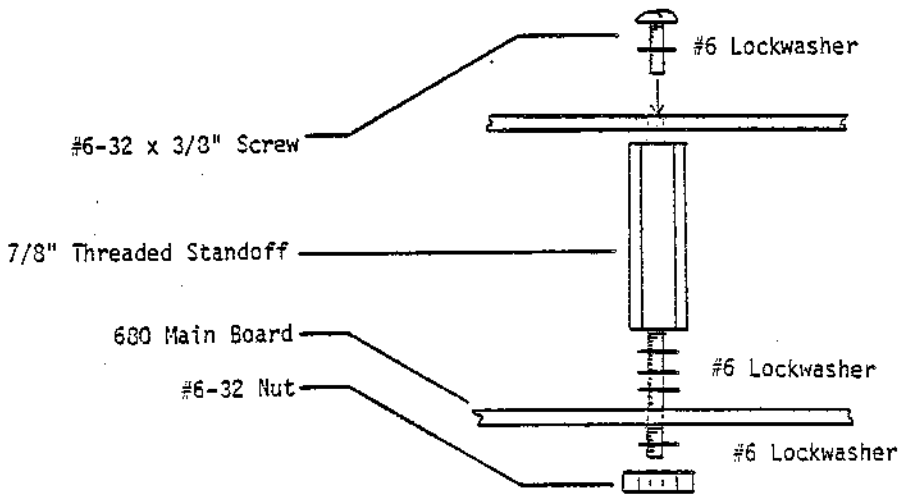


Figure 5-14. Installation of Threaded Standoffs Onto 680b Main Board

5-27. Installation of More Than One Board (Figure 5-15)

1. If this board is being installed in the second or third position above the 680b Main board, follow the same procedure for installation of the 100-pin edge connector onto the Expander card (Paragraph 5-24).

2. After installation of the 100-pin connector has been completed, reinstall the Expander card and the lower board(s) into the 680b Main board.

3. Replace the #6-32 x 3/8" screws and #6 lockwashers that previously secured the lower board with the two #6-32 x 7/8" threaded standoffs and two #6 lockwashers (Bag 5).

4. Insert the card stab connector of the 680b-KCACR board (silk-screened side up) into the 100-pin edge connector.

5. Secure the 680b-KCACR board in place by inserting a #6-32 x 3/8" screw and a #6 lockwasher (Bag 5) into the top of each threaded standoff.

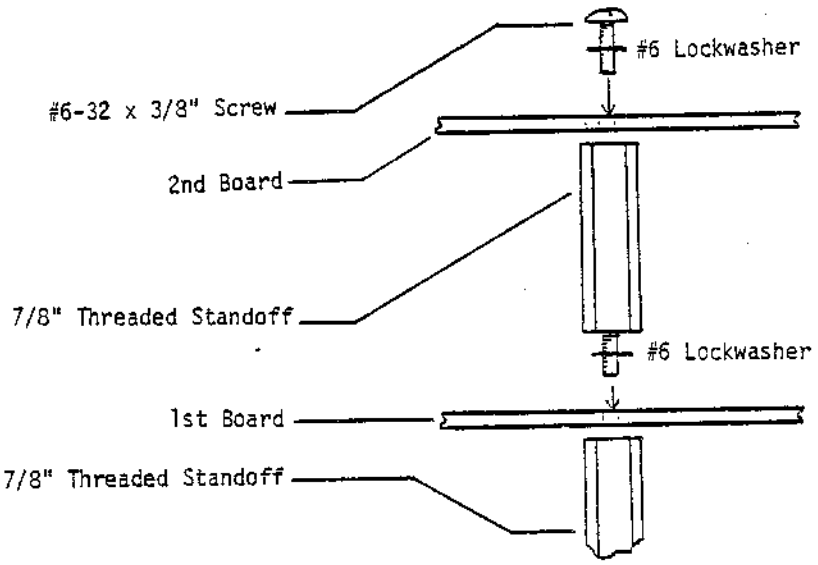


Figure 5-15. Installation of More Than One Board

appendix A
parts list

Bag	Quantity	Component	MITS Part Number
1	1	4001B CMOS Integrated Circuit	101159
	6	4013B CMOS Integrated Circuit	101162
	1	4030B CMOS Integrated Circuit	101407
	1	4029B CMOS Integrated Circuit	101408
	1	4022B CMOS Integrated Circuit	101166
	1	4081B CMOS Integrated Circuit	101409
	1	4069B CMOS Integrated Circuit	101170
	2	74C161/40161B CMOS Integrated Circuit	101410
	1	LM358/NE532 Integrated Circuit	101411
	1	LM393 Integrated Circuit	101412
	2	74367 Integrated Circuit	101040
	1	COM2502/AY-5-1013 Integrated Circuit	101065
	2	74LS30 Integrated Circuit	101135
	3	74LS14 Integrated Circuit	101123
	2	74LS02 Integrated Circuit	101136
	2	74LS10 Integrated Circuit	101133
	2	74LS74 Integrated Circuit	101088
	1	74LS38 Integrated Circuit	101147
	1	7805 Voltage Regulator	101074
2	1	68 ohm, 1/2W Resistor	101923
	1	220 ohm, 1/2W Resistor	101925
	2	1K ohm, 1/2W Resistor	101928
	1	1.5K ohm, 1/2W Resistor	101946
	1	3K ohm, 1/4W Resistor	101981
	1	4.3K ohm, 1/2W Resistor	101995
	3	4.7K ohm, 1/2W Resistor	101930
	1	5.6K ohm, 1/2W Resistor	102091
	4	10K ohm, 1/2W Resistor	101932
	1	15K ohm, 1/2W Resistor	102083
	1	22K ohm, 1/2W Resistor	101933
	2	33K ohm, 1/2W Resistor	102053
	2	91K ohm, 1/2W Resistor	102214
	2	100K ohm, 1/2W Resistor	101936
	2	390K ohm, 1/2W Resistor	102215
	1	10M ohm, 1/2W Resistor	102079
3	4	33uf 35V Elect. Capacitor	100326
	3	.1uf 50V Disc Capacitor	100312
	1	470pf Disc Capacitor	100316
	2	910pf 100V Mica Capacitor	100356
	2	820pf 100V Mica Capacitor	100401
	2	470uf 25V Elect. Capacitor	100310
4	2	IN914 Diode	100705
	1	IN4004 Diode	100718
	1	IN4742 Zener	100722

Bag	Quantity	Component	MITS Part Number
5	3	Ferrite Bead	101876
	1	90° 10-Pin Male Connector	101812
	1	Large Heat Sink	101870
	21	Test Points	101663
	3	6-32 x 3/8" Screw	100925
	3	6-32 Nut	100933
	11	#6 Lockwashers	100942
	2	4-40 x 1/2 Screw	100903
	2	4-40 Nut	100932
	2	#4 Lockwasher	100941
	2	7/8" Threaded Standoff	101666
6	30"	Shielded Audio Wire (ALPHA #2254/1)	103044
	1	10-Pin Female Socket	101768
	10	Pins for Socket	101769
	2	Mini Jacks	101722
	1	ACR Label Set	101834
	1	100-Pin Edge Connector	101864
7	1	40-Pin Socket	102106
	22	14-Pin Socket	102102
	6	16-Pin Socket	102103
	2	8-Pin Socket	102101
8	17	.1uf 16V Disc Capacitor	100327
MISC	1	PC Board	100225
	1	KCACR Connector Plate	101658
	1	680b-KCACR Manual	101566

2450 Alamo SE
Albuquerque, NM 87106

REF DESIG.	TYPE	VGG	VCC	GRD
P	4001		14	7
Z,V,H,J,B,K	4013		14	7
X	4030		14	7
N	4029		16	8
D	4022		16	8
A	4081		14	7
R	4069		14	7
W,C	74C161		16	8
E	LM358/NE532		8	4
G	LM393		8	4
GG,HH	74367		16	8
Y	COM2502	2	1	3
CC,BB	74LS30		14	7
FF,EE,DD	74LS14		14	7
U,L	74LS02		14	7
AA,S	74LS10		14	7
M,F	74LS74		14	7
T	74LS38		14	7

Figure 3-8. 680b-KCACR Read and Write Circuit (Sheet 1 of 2)

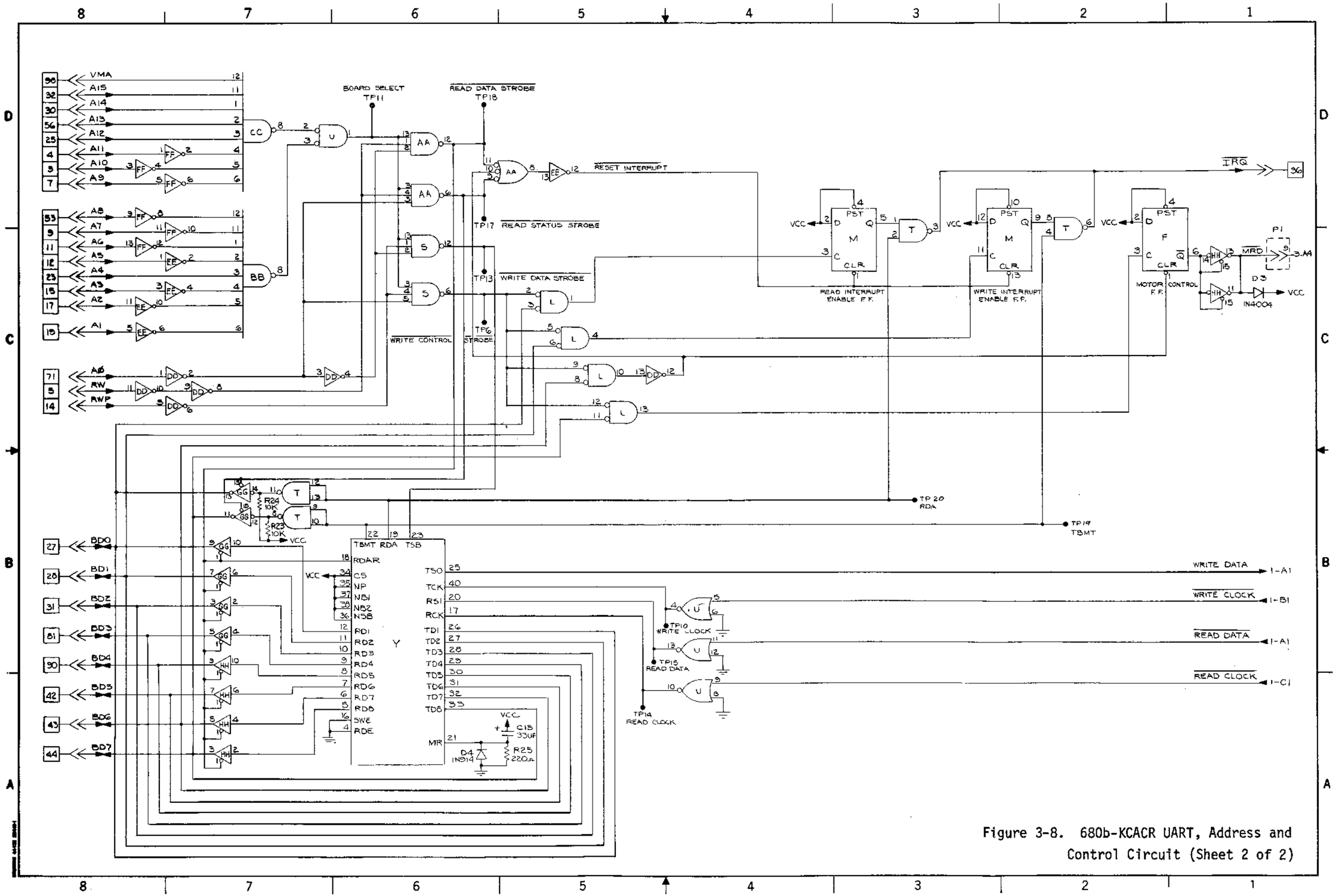


Figure 3-8. 680b-KCACR UART, Address and Control Circuit (Sheet 2 of 2)