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PDP-11/40,-11/35 (21 inch chassis) system manual

digital

EK-11040-TM-002

Tillhör PDP-11/40,-11/35 LPA62 (21 inch chassis) system manual

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FOREWORD

This Manual describes all PDP-11/40s and those PDP-11/35s that are mounted in a 21-inch, (as opposed to a 10-1/2 inch) box.

Text references that specify "PDP-11/40" also apply to the PDP-11/35.


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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual provides a general introduction to the PDP-11/40 System and includes sections on installation, operation, the instruction set, options, peripherals, equipment mounting, power, and maintenance. This overview is supplemented with references to other manuals in the PDP-11/40 series for detailed explanations.

The PDP-11/40 series manuals provide the user with the theory of operation necessary to understand, operate, and maintain the PDP-11/40 System. These manuals and the associated engineering drawings are discussed in Paragraph 1.4. Please note that the associated drawings are separate volumes documented by their Drawing Directory number. The manuals and drawings combine to form a complete documentation package.

The level of discussion in each manual assumes that the reader is familiar with basic digital computer theory. The maintenance philosophy presents information about normal system operation and enables the user to recognize trouble symptoms and take necessary corrective action. Each individual manual contains theory of operation, diagrams, and maintenance techniques. Logic drawings for the specific components covered are contained in separate volumes.

This chapter describes the basic system components (Paragraph 1.2) and provides a functional description of the overall PDP-11/40 System and each of its major components (Paragraph 1.3). The remainder of the chapter covers applicable documents and engineering drawings (Paragraphs 1.4 and 1.5).

1.2 SYSTEM COMPONENTS

The PDP-11/40 System consists of six basic components: processor, programmer's console, core memory, DECwriter with associated control, power system, and mounting box. Possible variations to this basic system are listed in Table 1-1.

Options and peripherals added to the basic PDP-11/40 System are covered in separate manuals delivered with the system. Manuals are included only for those options specifically ordered with an individual system.

1.3 FUNCTIONAL DESCRIPTION

The PDP-11/40 is a 16-bit, general purpose, parallel logic, microprogrammed computer using single and double operand instructions and 2's complement arithmetic. The system contains a multiple word instruction processor, which directly addresses up to 28K words of core memory. All communication among system components (including processor, core memory, and peripherals) is performed on a single high-speed bus, the Unibus. Because of the bus concept, all peripherals are compatible, and device-to-device transfers can be accomplished at the rate of 2.5 million words per second. All system components and peripherals are linked by the Unibus and power connectors, and all peripherals are in the basic system address space. Therefore, all instructions applied to data in memory can also be applied to data in peripheral device registers, enabling peripheral device registers to be manipulated by the processor as flexibly as memory.

Subsequent paragraphs present a brief functional description of basic PDP-11/40 System components (Figure 1-1). A functional description of all processor options is presented in Chapter 4.

Table 1-1
Possible PDP-11/40 Variations

Major Component	Possible Variations
*KD11-A Processor	No variations in basic processor. However, any of the following internal processor options can be included: KE11-E Extended Instruction Set (EIS) KE11-F Floating Instruction Set (FIS) KJ11-A Stack Limit Register KM11-A Maintenance Console KT11-D Memory Management KW11-L Line Time Clock
*KY11-D Programmer's Console	None
Core Memory	MM11-L – 8K word core memory, 900 ns cycle time, 350 ns internal access time *MF11-L – MM11-L memory plus double system unit backplane, (space exists for two additional MM11-Ls) MF11-LP – Same as MF11-L with the addition of two parity bits making it an 18-bit word memory ME11-L – MM11-L memory plus backplane, mounting box, and power supply (complete memory system) MM11-S – MM11-L memory, plus backplane (may be used for expansion of memory above 24K) **NOTE** **Memory systems compatible with the PDP-11/20 may also be used in the PDP-11/40. *However, these memories must be housed in their own mounting boxes and powered by their own power supplies.* The memories are:** **MM11-E 4K by 16 bit** **MM11-F 4K by 16 bit** **MM11-FP 4K by 18 bit, with parity** **MM11-H 1K by 16 bit** **MM11-J 2K by 16 bit** MM11-U – 16K word core memory MF11-U – MM11-U plus double backplane (can accept one additional MM11-U)
DECwriter	MM11-UP, MF11-UP – Same as MM11-U and MF11-U but with addition of parity.
DECwriter	**LA30 – Standard 97-character keyboard. Optional 128-character keyboard available. (LA30-S is a serial DECwriter and is controlled by a DL11 control; LA30-P is a parallel DECwriter and is controlled by an LC11 control.)

Table 1-1 (Cont)
Possible PDP-11/40 Variations

Major Component	Possible Variations
Teletype Unit	**33 ASR 33 KSR 35 ASR 35 KSR — Each unit is available in 120V or 240V models.
Input Terminal Control	DL11-A – Teletype, display, or LA30-S control. DL11-B – EIA terminal control. DL11-C – Teletype, display or LA30-S control. The DL11-C is simply a more flexible version of the DL11-A. The DL11-C features a variable character code plus crystal and switch selectable baud rates. DL11-D – EIA terminal control. The DL11-D is simply a more flexible version of the DL11-B. The DL11-D features a variable character code plus crystal and switch selectable baud rates. DL11-E – Dataset control. KL11-A, KL11-B, KL11-C, KL11-E, KL11-F — ASR or KSR Teletype control. Units differ primarily in baud rates as described in KL11 manual. LC11 – LA30-P DECwriter control.
Power System	*H742 Power Supply (may be jumpered for either 120V or 230V, 50/60 Hz). *H744 +5V regulator, 25A (three supplied with basic system) *H745 - 15V regulator, 10A (one or two) H754 +20, - 5V regulator, used with MF11-U/UP *861 Power Controller – mounted in bottom rear of cabinet. Two versions available: 861B – requires 240 Vac input 861C – requires 120 Vac input
Mounting Box	*BA11-FC Mounting Box

*An asterisk indicates that this is the normal configuration shipped with the basic machine, unless otherwise specified by the customer.

**Either the LA30 DECwriter or the Teletype unit may be used as the basic PDP-11/40 System input/output device.

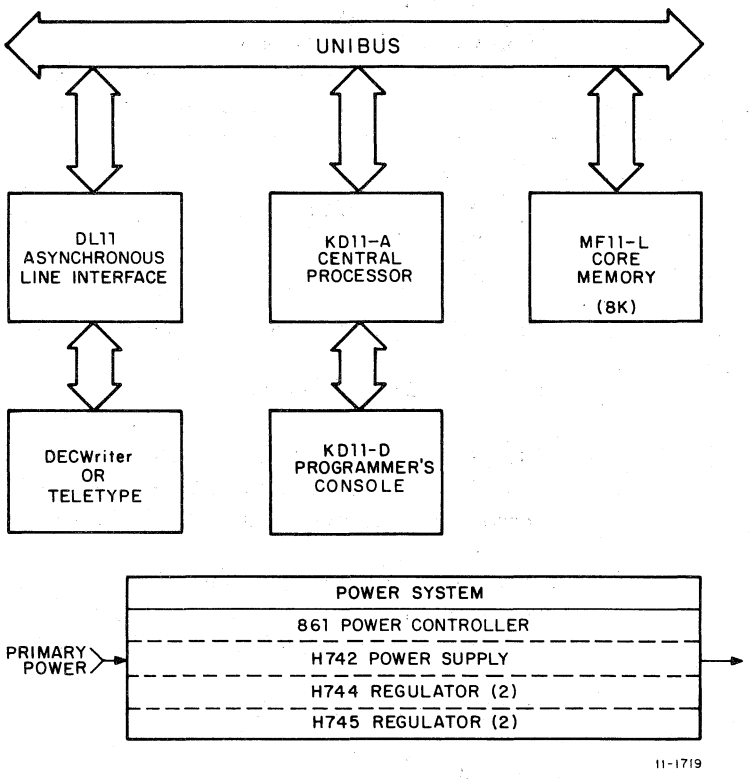


Figure 1-1 PDP-11/40 Basic System Block Diagram

1.3.1 Unibus

The Unibus provides high-speed communication between system components. With bidirectional data, address, and control lines, the Unibus allows data transfers to occur between all units on the bus, with control of the bus an important factor in these transfers. The fixed repertoire of bus operations is flexible enough for speed and design economy, yet provides a fixed specification for interfaces. The asynchronous nature of these operations also eases design and operation. The repertoire of bus operations is:

DATI, DATIP, DATO, DATOB – data operations
INTR, BR, NPR – control operations

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between the master and slave. The DATI, DATIP operations transfer data into the master; DATO, DATOB operations transfer data out of the master. When a device is capable of becoming bus master and requests use of the bus, it is for one of two purposes: to make a Direct Memory Access (DMA) transfer of data directly to or from another device or memory without processor intervention, or to INTeRrupt (INTR) program execution and force the processor to branch to a specific address where an interrupt service routine is located.

Bus control is obtained under a Non-Processor Request (NPR) for the DMA or under a Bus Request (BR) for an INTR. A device can perform a DMA after acquiring bus control via a BR.

Requests for the bus can be made at any time on the BR and NPR lines. Transfer of bus control from one device to another is made by the processor priority arbitration logic which grants control of the bus to the device having the highest priority. NPRs are accorded higher priority than BRs. The NPRs are serviced before and immediately after Unibus data cycles, in addition to specific times during WAIT or TRAP sequences. The BRs are serviced upon completion of the current instruction if the requesting priority exceeds that of the processor.

The PDP-11/40 processor has a special role in bus control operations as it performs the priority arbitration to select the next bus master. The processor assumes bus control when no other device has control.

The Unibus originates in the processor with the Internal Unibus and Terminator module (M981), which carries the Unibus from the processor to the next system unit. All 56 Unibus signals and 17 grounds are carried in this one module. In addition, a 120-conductor Mylar cable may be used to connect system units in different mounting boxes or to connect a peripheral device removed from the mounting box.

A complete description of the Unibus, including specifications, is presented in the *PDP-11 Peripherals Handbook.*

1.3.2 KD11-A Processor

The KD11-A Processor decodes instructions; accepts, modifies, and outputs data; performs arithmetic operations; and controls allocation of the Unibus among external devices. The processor contains sixteen hardware registers, eight of which are programmable. Two of the eight programmable registers are specifically used for processor operation: a program counter (PC) and a stack pointer (SP); the remaining six serve as arithmetic accumulators, index register, and autoincrement and autodecrement registers.

The eight non-programmable registers are used for storage of a variety of functions including: intermediate address, source and destination data, a copy of the instruction register, the last interrupt vector address, console operation data and stack pointer for the KT11-D Memory Management Option.

Because of the flexibility of hardware registers, address modes, instruction set, and DMA, PDP-11/40 programs are written in directly relocatable codes. The processor also includes a full complement of instructions that manipulate byte operands and provisions for byte swapping. Either words or bytes may be displayed on the programmer's console.

Any of the eight programmable internal registers can be used to build last-in, first-out stacks. One register serves as a processor (or system) stack pointer for automatic stacking. This stack-handling capability permits save and restore of the program counter and status word in conjunction with subroutine calls and interrupts. This feature allows true reentrant codes and automatic nesting of subroutines.

The Unibus serves the processor and all peripheral devices; therefore, there must be a priority structure to determine which device becomes bus master. Generally, a device requests use of the bus for one of two reasons: to make a non-processor transfer of data directly to or from memory, or to interrupt program execution and force the processor to branch to an interrupt service routine. An NPR is granted by the processor at the end of bus cycles and allows device-to-device data transfers without processor intervention. A BR is granted by the processor at the end of an instruction and allows the device to interrupt the current processor task.

The processor recognizes four levels of hardware BRs, with each major level containing sublevels. Many devices can be attached on each major level, with the device that is electrically closest to the processor given priority over other devices on the same priority level. The priority level of the processor itself is programmable within the hardware levels; therefore, a running program can select the priority level of permissible interrupts.

Additional speed and power are added to the interrupt structure through the use of the PDP-11/40 fully vectored interrupt scheme. With vectored interrupts, the device identifies itself, and a unique interrupt service routine is automatically selected by the processor. This eliminates device polling and permits nesting of device service routines. The device interrupt priority and service routine priority are independent to allow dynamic adjustment of system behavior in response to real-time conditions.

The Unibus addresses generated by the KD11-A Processor are 18-bit direct byte addresses, even though the PDP-11/40 word length and operational logic is all 16-bit word length. Thus, while the PDP-11/40 word can only contain address references up to 32K words (64K bytes), the KD11-A Processor can reference addresses up to 128K words (256K bytes).

In addition to the word length constraint on basic addressing space, the uppermost 4K words of address space are reserved for peripheral control, status, and data registers. In the basic PDP-11/40 configuration (without memory management), all address references to the uppermost 4K words of 16-bit address space (160000–177777) are converted to full 18-bit references with bits 16 and 17 always set to 1. Thus, a 16-bit reference to address 173224_8 is automatically converted to a full 18-bit I/O device register address of 773224_8. Consequently, the basic PDP-11/40 configuration can address up to 28K words of core memory and 4K words of I/O device registers. If core memory is increased beyond 28K words, the KT11-D Memory Management Option must be installed. A brief description of the KT11-D Memory Management Option is provided in Chapter 4.

A detailed description of the KD11-A Processor is contained in the *KD11-A Processor Maintenance Manual,* EK-KD11A-MM-001.

1.3.3 KY11-D Programmer's Console

The KY11-D Programmer's Console provides the programmer with a direct system interface. The console allows the user to start, stop, load, modify, examine, step, or continue a program. Console displays indicate processor operation and the contents of the address and data registers. The console is mounted as the front panel of the BA11-FC Mounting Box and is connected to the processor by two cables.

The programmer's console interacts with the processor through a microprogram control located in the processor. The console contains only indicators (light emitting diodes), switches, and the contact bounce filtering circuits for the control switches. Console operation does require certain Unibus operations through the processor: DATO for DEP and DATI for EXAM. For single-step operation, the processor responds to a Console Bus Request (CBR) whose priority supersedes all other BR priorities. Note that use of the KM11 Maintenance Console option provides a further display of machine states, and allows single microword stepping.

Console operation, including descriptions of all controls and indicators, is presented in Chapter 3. Detailed descriptions of console logic circuits are contained in the *KD11-A Processor Maintenance Manual,* EK-KD11A-MM-001.

1.3.4 MF11-L Core Memory

The PDP-11/40 contains an MF11-L Core Memory. The MF11-L consists of a three-module, 8K, 16-bit word, MM11-L memory mounted on a double system unit backplane. The backplane has nine slots of mounting space, hence two additional MM11-L memories may be mounted on the backplane as options. With two additional MM11-L memories installed, the memory size is increased to a total of 24K. A detailed description of the memory is contained in the *MM11-S, MF11-L, and MF11-LP Core Memory System,* EK-MM11S-TM-003.

NOTE

PDP-11/40 memory is powered for non-interleaved and non-overlapped situations. Successive and continuous operations to alternate 8K memory segments is considered a prohibited overlapped situation. Interleaving is not allowed within the MF11-L or MM11-S powered by the basic box.

The core memory uses the Unibus for data transfers to and from the processor and other devices. The core memory, however, is never bus master; therefore, DATO or DATOB indicates information transferred out of the master into the memory. Because of the Unibus structure, the memory can be directly addressed by the processor or any other master device. Because of double operand instructions, every location in core can function as a true arithmetic accumulator.

The memory does not enter the priority structure because it is always a slave device. The master device, however, can request use of the Unibus and thus the memory through either a BR or a NPR. Because the memory is completely independent of the processor, any master device can perform direct data transfers with memory without processor intervention.

NOTE

The instruction timing specified for the PDP-11/40 applies only for the memories mounted within the computer mounting box. These memories employ a special MSYN A signal between the processor and the memory.

1.3.5 Optional Memory Systems

Memories with different ranges of speeds and various physical and electrical characteristics can be freely mixed and interchanged in a single PDP-11/40 System. The basic system mounting box can house up to 80K of memory in addition to the processor and processor options. Additional memory units may be added by using separate mounting boxes and power supplies up to a total of 124K. Note that the KT11-D Memory Management Option is required if core memory is increased beyond 28K.

Generally, memory systems compatible with the PDP-11/40 fall into two categories: memories designed for use with the PDP-11/40 and memories designed for use with the PDP-11/20. The PDP-11/40 memories are: MM11-L, MF11-L, MF11-LP, ME11-L, and MM11-S. The PDP-11/20 memories are: MM11-E, MM11-F, MM11-FP, MM11-H, and MM11-J.

1.3.5.1 PDP-11/40 Memories – The following paragraphs provide brief descriptions of the MM11-L, MF11-LP, ME11-L, and MM11-S memories (the MF11-L memory was described in Paragraph 1.3.4). For detailed descriptions of the MM11-L, MF11-LP, and MM11-S memories, refer to the *MM11-S, MF11-L, and MF11-LP Core Memory System,* EK-MM11S-TM-003. For a detailed description of the ME11-L memory, refer to the *ME11-L Core Memory System Manual,* DEC-11-HMELA-B-D.

1.3.5.1.1 MM11-L Core Memory – The MM11-L Core Memory is a read/write, random access, coincident current, magnetic core type memory with a cycle time of 900 ns and Unibus access time of 400 ns. The memory is organized in a 3D, 3-wire planar configuration. It provides 8192 (8K) 16-bit words that are both word and byte addressable.

The memory is organized into 16-bit words, each word containing two 8-bit bytes. The bytes are identified as the low-order byte (bits 07–00) and the high-order byte (bits 15–08). Each byte is addressable and has its own address location. Low bytes are always even numbered and high bytes are odd numbered. Full words are addressed at even-numbered locations only. When a full word is addressed, the high byte is automatically included. For example, the 8K memory has 8,192 words or 16,384 bytes; therefore, 16,384 locations are assigned. Address 000000 is the first low byte, address 000001 is the first high byte, 000002 is the second low byte, 000003 is the second high byte, etc.

The MM11-L consists of three modules: a G110 Hex module containing the memory control logic and data channels; a G231 Hex module containing the memory driver logic; and an H214 Quad module containing the memory core stack.

The memory control logic acknowledges the request of the master device, determines which of the four basic operations (DATI, DATIP, DATO, or DATOB) is to be performed, and sets up appropriate timing and control circuits to perform the desired read or write operation. It also contains the inhibit drivers and sense amplifiers as well as device selector logic to determine if the memory bank has been addressed from the Unibus. The control logic includes a 16-bit flip-flop storage register. During DATI operations, this register stores the contents of the memory location being read (destructive read) so that the data can be written back into memory (restored). The register is also used during DATO and DATOB cycles to store incoming data from the Unibus lines so that it can be written into core memory.

The memory driver logic includes: address selection logic that decodes the incoming address to determine the core specifically addressed; the switches and drivers that direct current flow through the magnetic cores to ensure the proper polarity for the desired function; and the X and Y current generators that provide the necessary current to change the state of the magnetic cores.

The ferrite core memory stack consists of 16 memory mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128 X 64 matrix. Each mat represents a single bit position of a word. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals.

1.3 5.1.2 MF11-LP Core Memory – The MF11-LP is an 8K, 18-bit word memory consisting of four modules mounted on a double system unit backplane. Three modules perform identical functions as those in the MM11-L memory while the fourth module contains parity control circuitry. The two additional bits (bits 16 and 17) provide parity bits for the low and high bytes of the data word respectively. The MF11-LP may be expanded to 24K capacity by installing two additional 8K segments (three modules each) on the double system unit backplane.

Note that while the 8K MF11-LP memory contains four modules, the 24K unit only requires 9 module slots (one double system unit). This is possible because only one parity controller module is needed for 24K. The parity controller module is a dual-height module and is installed in the two normally vacant slot/sections next to the memory stack module.

1.3.5.1.3 ME11-L Core Memory – The ME11-L is a complete memory system consisting of an MM11-L Core Memory and associated backplane housed in its own mounting box which contains an integral power supply. This power supply and mounting box can accommodate up to three MM11-L Core Memories. In effect, the ME11-L can be expanded up to 24K in 8K increments. These memories should not be interleaved due to power supply limitations.

The system mounting box is 5-1/4 in. high, 19 in. wide, and 20 in. deep and is designed for mounting in a standard 19-in. cabinet. Rack-mountable slides are included but the box can be used as a stand-alone unit, if desired. In addition to holding the core memory, backplane, and power supply, the box contains all cables necessary for providing power and for interfacing the units of the ME11-L. It also provides for connection to the Unibus. The rear of the box contains cable clamps, a line cord for input power, a cooling fan for the memory modules and power supply, and a power control circuit breaker.

The memory system power supply converts single-phase 115 or 230 Vac line voltage to the two regulated dc voltages required by the memory system: +5V for the logic and −15V for the core memory. Both outputs are overvoltage and overcurrent protected. The power supply also provides line power to the mounting box cooling fan and the BUS AC LO and BUS DC LO signals which are sent to the Unibus in the event of a power failure.

The power supply consists of a power control, a power chassis assembly, and a dc regulator along with associated ac and dc cables. The power control contains a thermal circuit breaker which protects against input and overload and is reset by depressing a button on the rear of the mounting box. A thermostat in the regulator opens one side of the primary circuit and deenergizes the power supply if the temperature rises above 100° C. It is automatically reset when the temperature reaches 63° C.

1.3.5.1.4 MM11-S Core Memory – The MM11-S Core Memory is an MM11-L memory on a single system unit backplane. The prime physical difference between the MM11-S and the MF11-L is that the MM11-S is an 8K single system unit while the MF11-L is a 24K capacity double system unit. The MM11-S should not be interleaved in the PDP-11/40.

1.3.5.2 PDP-11/20 Memories – Brief descriptions of the PDP-11/20 memories are provided below. These memories may be used with the PDP-11/40 System provided they are powered by H720 Power Supplies and are mounted in a BA11-ES Mounting Box. The MM11-E and MM11-F memories are expandable to 28K with interleaving of 4K segments permitted.

MM11-E – 4K by 16 bit, 1.2 μs access time
MM11-F – 4K by 16 bit, 950 ns access time
MM11-FP – an MM11-F with parity option included
MM11-H – 1K by 16 bit, 950 ns access time
MM11-J – 2K by 16 bit, 950 ns access time

1.3.5.3 MF11-U/UP Core Memory – The MF11-U/UP Memory is a read/write, random access coincident current, magnetic core type with a maximum cycle time of 980 ns and a maximum access time of 425 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 16 bits and the memory consists of 16,384 (16K) words.

The MF11-U provides 16,384 (16K) 16-bit words; the MF11-UP provides the same number of words but includes parity.

The memory can be interleaved in 32K increments for faster operation. Interleaving causes consecutive bus addresses to be located within alternate 16K memory blocks.

The chart below shows the various option descriptions associated with the 16K memory.

MF11-U	M8293 16K Unibus Timing Module G114 Sense Inhibit Module G235 X-Y Driver H217D Stack Module (16 bits) 7009295 Backplane Assembly
MM11-U Module Set	Includes all modules listed in MF11-U but does not include backplane assembly
MF11-UP	M8293 16K Unibus Timing Module G114 Sense Inhibit Module G235 X-Y Driver Module H217C Stack Module (18 bits including parity) 7009295 Backplane Assembly M7259 Parity Control Module
MM11-UP Module Set	Includes all modules listed in MF11-UP except M7259 Parity Control Module and does not include backplane assembly

If a user has a 16K memory system and wishes to add another 16K, he merely specifies the appropriate module set since the existing backplane assembly can hold 32K of memory.

The MF11-U/UP Core Memory is explained in detail in the *MF11-U/UP Core Memory System Maintenance Manual,* DEC-11-HMFMA-C-D.

1.3.6 LA30 DECwriter

The LA30 DECwriter is a dot matrix impact printer and keyboard for use as a hard copy I/O terminal. It is capable of printing a set of 64 ASCII characters at speeds up to 30 characters per second on a sprocket-fed 9-7/8 in. continuous form. Data entry is from a keyboard capable of generating either 97 or 128 characters.

The LA30 is available in two versions: parallel (LA30-P) and serial (LA30-S). The serial version is normally used with the PDP-11/40 System in that it is interfaced to the Unibus via the DL11 Asynchronous Line Interface. The DL11 is basic to the PDP-11/40 System.

The LA30 DECwriter is covered in Chapter 3 and a detailed description is contained in the *LA30 DECwriter Maintenance Manual,* DEC-00-LA30-DD.

1.3.7 DL11 Asynchronous Line Interface

The DL11 Asynchronous Line Interface provides an interface between a communications device, such as a serial LA30 DECwriter or Teletype, and the PDP-11/40 Unibus. Serial information read or written by the device is assembled or disassembled by the control for parallel transfer to or from the Unibus. The control also formats the data from the Unibus so that it is in the format required by the device. The interface provides the flags that initiate these data transfers and cause a priority interrupt to indicate the availability of the device.

The DL11 transfers data via processor DATI and DATOB bus cycles. Although a DATO can be used, normal operation consists of a DATOB transfer because the device and the interface handle byte rather than word data. The interface can acquire bus control through a BR and is normally set at the BR4 priority level. Because the DL11 interface operates through an interrupt, no NPR hardware exists.

Five available DL11 interface options (DL11-A through DL11-E) provide the flexibility needed to handle a variety of terminals. For example, the user can select an option for interfacing a Teletype or display keyboard, for handling EIA data, or for handling dataset devices. In addition, depending on the option used, the user has a choice of line speeds, character size, stop-code length, and parity.

The DL11 consists of a single quad module, which is normally installed in the processor Small Peripheral Controller (SPC) slot. This module contains address selection logic for decoding the incoming bus address, an interrupt control for generating the interrupt, and receiver/transmitter logic that performs the conversion and formatting functions.

A detailed description of the DL11 interface is presented in the *DL11 Asynchronous Line Interface Manual,* EK-DL11-TM-002.

1.3.8 Power System

NOTE

Two different power distribution systems are used in the PDP-11/40; both are described in detail in Chapter 6. This manual refers to these systems as *early* or *older* and *recent* or *newer* models. This note applies to both CPU and expansion boxes and cabinets.

The new power distribution is incorporated in PDP-11/40 systems with serial number 6000 and greater.

The PDP-11/40 power system consists of an 861 Power Controller, an H742 Power Supply, three H744 +5V Regulators, two H745 -15V Regulators, and interconnection and power distribution cabling. One H754 +20, -5 Vdc regulator may replace an H745 if the MF11-U/UP Memory is installed.

The 861 Power Controller controls all ac power input to the system cabinet. The controller is equipped with a circuit breaker for overload protection and a thermostat for excessive heat protection. The power controller provides switched ac outputs (controlled) and unswitched ac outputs (uncontrolled) which provide power for the entire system cabinet and related peripherals.

The H742 Power Supply takes ac input power from the 861 Power Controller, generates and distributes dc power and control signals to the system, and provides ac power to the logic cooling fan and H744 and H745 regulators.

There are three control signals generated: a clock signal, a DC LO logic signal, and an AC LO logic signal. The clock signal drives the processor real-time clock option (KW11-L or KW11-P) if it is installed. The AC LO and DC LO signals warn the processor of imminent power failure, allowing the processor time to perform a power-fail sequence.

The H744 and H745 regulators generate +5V and -15V outputs, respectively, which are distributed to the KD11-A Processor and MF11-L Memory backplanes and the KY11-D console.

Expansion cabinets are similar to the PDP-11/40 cabinet, but can accept two H754 +20, -5V regulators in place of the two H745 -15V regulators, if required by the MF11-U complement.

1.4 APPLICABLE DOCUMENTATION

PDP-11 documents related to the PDP-11/40 System are listed in Table 1-2 in two main categories: general handbooks and PDP-11/40 hardware manuals. Hardware manuals cover equipment specifically related to the PDP-11/40 and have associated engineering drawings. General handbooks cover overall PDP-11 system descriptions, instruction set, addressing modes, basic logic modules, Unibus description, and interfacing information. Also covered is general software documentation for basic programs necessary to develop, load, and run programs. Both the PDP-11/40 hardware manuals and the general PDP-11 handbooks must be used together for a complete understanding of PDP-11/40 Systems.

Table 1-2
Applicable Documents

Title	Associated Drawing Set	Description
PDP-11/40 Processor Handbook DEC, 1972	N/A	A general PDP-11/40 System handbook covering system architecture, addressing modes, the instruction set, programming techniques, memory management, internal processor options, console operation, and system specifications.
PDP-11 Peripherals Handbook	N/A	A general peripheral interface handbook. The first part is devoted to a discussion of the various peripherals used with PDP-11 Systems. The second part provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
Logic Handbook DEC, 1972	N/A	Presents functions and specifications of the M-Series logic modules and accessories used in PDP-11 interfacing (includes other types of logic produced by DEC but not used with the PDP-11).
PDP-11 Paper-Tape Software Programming Handbook, XPTSA-A-D	N/A	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating point and math package.

Table 1-2 (Cont)
Applicable Documents

Title	Associated Drawing Set	Description
PDP-11/40, -11/35 (21 inch Chassis) System Manual EK-11040-TM-002	PDP-11/40 System	A general introduction to the basic PDP-11/40 System including sections on installation, operation, and the instruction set. Also provides detailed information, including maintenance, of the system power supply.
KD11-A Processor Maintenance Manual, EK-KD11A-MM-001	PDP-11/40 System	Block diagram discussion, flow diagram discussion, theory of operation, and maintenance for the KD11-A Processor, KY11-D Programmer's Console, KJ11 Stack Limit Register Option, KW11-L Line Frequency Clock Option, and KM11 Maintenance Module Option.
MM11-S, MF11-L, MF11-LP Core Memory System, EK-MM11S-TM-003	PDP-11/40 System	General description, detailed description, and maintenance of the MF11-L, MF11-LP, and MM11-S memories. (Note that MF11-L is the memory system; MMll-L the basic core memory.) The MF11-L consists of a MM11-L Core Memory on a double system unit backplane.
MF11-U/UP Core Memory System Maintenance Manual, DEC-11-HMFMA-C-D	MF11-U/UP	Contains a detailed description and maintenance information for the MF11-U and -UP Memory Systems. MF11-UP is a parity memory.
KE11-E and KE11-F Instruction Set Option Manual, EK-KE11E-TM-002	KE11-E Extended Instruction Set (EIS) Option and KE11-F Floating Instruction Set (FIS) Option	Algorithms, data programming, theory of operation, and maintenance for the KE11-E Extended Instruction Set (EIS) Option and the KE11-F Floating Instruction Set (FIS) Option.
KT11-D Memory Management Option Manual, EK-KT11D-TM-002	KT11-D Memory Management	Operation, programming, and detailed theory of operation for the KT11-D Memory Management Option.
DL11 Asynchronous Line Interface Manual, EK-DL11-TM-002	PDP-11/40 System	Installation configuration, programming, and theory of operation of the DL11 interface. Covers DL11-A through DL11-E. The DL11-A or C is normally used as a control for the Teletype or the LA30-S DECwriter but the DL11 can be used for a variety of communications devices. The DL11-C is simply a more flexible version of the DL11-A in that the DL11-C features a variable character code plus crystal and switch selectable baud rates.
861-A, B, C Power Controller Maintenance Manual, DEC-00-H861A-A-D	N/A	Installation, theory of operation, and maintenance of the 861-A, B and C Power Controllers.

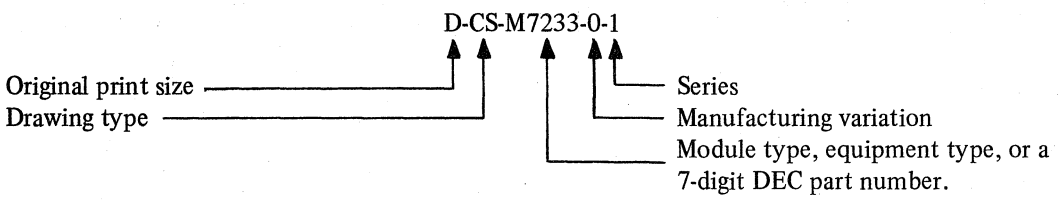
Table 1-2 (Cont)
Applicable Documents

Title	Associated Drawing Set	Description
LA30 DECwriter Manual, DEC-00-LA30-DD	DEC-00-LA30-DA	Presents a detailed discussion of the DECwriter including installation, operation, principles of operation, maintenance, troubleshooting, and engineering drawings.
LC11 DECwriter System Manual, DEC-11-HLCB-D	DEC-11-HLCB-D	Provides general and detailed descriptions, programming, and operation for the LC11 DECwriter interface. The LC11 is used when an LA30-P (parallel) DECwriter is used as a system input/output device.
KL11 Teletype Control Manual, DEC-11-HR4C-D	DEC-11-HR4C-D	Provides general and detailed descriptions, programming, adjustments, and maintenance for the KL11 Teletype Control that may be used instead of the DL11 control.
Automatic Send-Receive Sets, Manual	Bulletin 273B, two volumes, Teletype Corp.	Describes operation and maintenance of the Model 33 ASR Teletype unit that can be used as an input/output device with the PDP-11/40 System. Comparable manuals available for other Teletype models.
Model 33 Page Printer Set, Parts	Bulletin 1184B, Teletype Corp.	Contains an illustrated parts breakdown to serve as a guide for disassembly, reassembly, and parts ordering for the Model 33 ASR Teletype unit. Comparable manuals available for other Teletype models.

1.5 ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each PDP-11/40 System. These print sets are listed in Table 1-2 either under a Drawing Directory reference or as a second volume to the maintenance manual. The engineering drawings support manual discussions and are often directly described therein. The Drawing Director Index (DDI) provides a list of prints included in the set and includes drawing number, title, and revision. An X in the column labeled CUSTOMER PRINT SET indicates each drawing that is provided for the customer. The *1972 DEC Logic Handbook* contains general logic symbols used on DEC drawings. A more detailed discussion of drawing set conventions is contained in the *KD11-A Processor Maintenance Manual,* EK-KD11A-MM-001 with this convention directly applicable to the PDP-11/40 processor and processor options.

All DEC drawings are identified with a drawing identification code shown below:



Drawing Type Designations

CS:	Circuit schematic	AD:	Assembly drawing
BS:	Block schematic	UA:	Unit assembly
BD:	Block diagram	WL:	Wire list
FD:	Flow diagram	PL:	Parts list
DD:	Drawing directory	AL:	Accessory list
MU:	Module utilization		

In addition to the basic drawing identification code, a drawing set/sheet code is also used to identify logic drawings. This code is written in the title block and consists of three characters: two letters identify the equipment drawing set; and a number identifies the sheet in that drawing set. For example, KT-3 indicates sheet 3 of the KT11-D Memory Management Option drawing set.

Because of its multiple module configuration, the processor drawing set/sheet code is a little different. Only one letter, the letter K, is used in the processor code along with two numbers. The first number indicates the module, and the second number indicates the sheet. For example, K2-4 indicates sheet 4 of the processor U WORD Module Drawing set. See Table 1-3 for a complete listing of drawing set/sheet code prefixes.

Table 1-3
Drawing Set/Sheet Code Prefixes

Drawing Set	Module Number	Code Prefixes
KD11-A Processor Modules:		
DATA PATHS	M7231	K1
U WORD	M7232	K2
IR DECODE	M7233	K3
TIMING	M7234	K4
STATUS	M7235	K5
KJ11-A Stack Limit Register	M7237	KJ
KM11-A Maintenance Board	W130, W131	KM
KY11-D Console	—	KYD
DL11 Asynchronous Line Interface	M7800	DL
KT11-D Memory Management	M7236	KT
KE11-E Expanded Instruction Set	M7238	KE
KE11-F Floating Instruction Set	M7239	KF

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides information on PDP-11/40 System site preparation, equipment installation, operation and programming, and customer acceptance. Only installation of the basic PDP-11/40 System and processor options is included in this chapter. A section on installation of peripherals is not provided because of the modular and Unibus concepts of the system. To install a peripheral, for example, it is usually only necessary to insert the interface module(s) into the basic system mounting box and connect appropriate cabling between the interface and the peripheral. Installation and maintenance of the peripheral itself is covered in associated manuals.

2.2 SITE PREPARATION

It is recommended that sufficient time be given to site planning and preparation with particular attention given to the user's specific system configuration especially if a large number of peripherals are part of the system.

Two DEC documents will aid in proper site planning: the PDP-11/10, 40 Configuration Worksheet and the PDP-11 Site Preparation Worksheet.

The Configuration Worksheet permits the user to lay out the system prior to ordering so that he is aware of drawer layout, cabinet layout, and Unibus interconnection. This ensures that the proper number of drawers and cabinets are used and that Unibus length and loading is proper for the system.

The Site Preparation Worksheet permits the user to determine the power requirements, environmental preparations, and physical arrangement of his system. The worksheet provides data on operating environment, power requirements, service and access requirements, and physical specifications for the basic system and available peripherals.

A final layout plan should be approved jointly by the user and DEC prior to delivery of equipment. It is recommended that any modifications to the installation site be effected prior to shipment and installation of the system.

DEC Sales Engineers and Field Service Engineers are available for consultation and planning regarding objectives, course of action, and progress of the installation. It is recommended that a qualified DEC representative either install the system, or at least be present during installation.

Adequate site planning and preparation can greatly simplify the installation process, resulting in a more efficient and reliable installation. Information in the following paragraphs is provided primarily to permit review of the site planning.

2.2.1 Physical Dimensions

The overall dimensions and total weight of the particular PDP-11/40 as well as dimensions, weights, and cable lengths of any optional cabinets and free-standing peripherals should be known prior to shipment of the equipment.

The route the equipment is to travel from the customer receiving area to the installation site should be studied. Measurements of doors, passageways, etc., should be taken and submitted along with floor plans to the DEC Sales Engineers and Field Service to ensure that the equipment is packed to suit the installation site facilities. Any restrictions (such as bends or obstructions in hallways, etc.) should be reported to DEC.

Secondly, elevator limitations should be determined. If an elevator is to be used for transferring the PDP-11/40 and its related equipment to the installation site, DEC should be notified of the size and gross weight limitations so that the equipment can be packed accordingly.

Thirdly, system operational requirements should be considered. Operational requirements determine the specific location of the various options and free-standing peripherals of the system. Dimensions, weights, and cable lengths of free-standing peripheral equipment must be determined prior to installation, preferably during site preparation and planning. Note that peripheral cables must not exceed maximum specified lengths. Operational requirements that should be considered are listed below:

a. Ease of observation of input/output devices by operating personnel.

b. Adequate work area for installing tapes, access to console, etc.

c. Space availability for contemplated future expansion.

d. Proximity of the cabinets to peripherals.

e. Proximity of cabinets and peripherals to any humidity controlling or air conditioning equipment.

Finally, site space requirements should be determined by the specific system configuration to be installed and, when applicable, provision for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout can be helpful. When applicable, space should be provided in the machine room for storage of tape reels, printer forms, card files, etc. The integration of the work area with storage area can be considered in relation to the work flow requirements between areas. In large installations where test equipment is maintained, DEC recommends that the test equipment storage area be within or adjacent to the machine room.

2.2.2 Fire and Safety Precautions

The following fire and safety precautions are presented as an aid to providing an installation that affords adequate operational safeguards for personnel and system components.

a. If an overhead sprinkler system is used, a "dry pipe" system is recommended. This type of system, upon detection of a fire, removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.

b. If the fire detection system is the type that shuts off the power to the installation, a battery-operated emergency light source should be provided.

c. If an automatic carbon dioxide fire protection system is used, an alarm should sound prior to release of the CO_2 to warn personnel within the installation.

d. If power connections are made beneath the floor of a raised-floor installation, waterproof electrical receptacles and connections should be used.

e. An adequate earth ground connection should be provided for the protection of operating personnel.

2.2.3 Environmental Requirements

An ideal computer room environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

2.2.3.1 Humidity and Temperature – The PDP-11/40 electronics are designed to operate in a temperature range of from 50°F (10°C) to 122°F (50°C) at a relative humidity of 20 to 95 percent without condensation. However, typical system configurations that use I/O devices such as magnetic tape units, card readers, etc., require an operational temperature range of from 60°F (15°C) to 80°F (27°C) with 40 to 60 percent relative humidity. Nominal operating conditions for a typical system configuration are a temperature of 70°F (20°C) and a relative humidity of 45 percent.

2.2.3.2 Air Conditioning – When used, computer room air-conditioning equipment should conform to the requirements of the "Standard for the Installation of Air Conditioning and Ventilating Systems (non-residential)", N.F.P.A Number 90A; as well as the requirements of the "Standard for Electronic Computer Systems", N.F.P.A. Number 75.

2.2.3.3 Acoustical Damping – Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise level devices, an acoustically damped ceiling reduces the noise. Operator comfort and efficiency is a major concern here.

2.2.3.4 Lighting – If cathode-ray tube (CRT) peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to increase the visibility of the display.

2.2.3.5 Special Mounting Conditions – If the PDP-11/40 is to be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard a ship), the cabinets should be securely anchored to the installation floor by mounting bolts. Since such installations require modifications to the system cabinets, DEC must be notified upon placement of the order so that necessary modifications can be made.

2.2.3.6 Static Electricity – Static electricity can be an annoyance to personnel and can, in extreme cases, affect the operational characteristics of the PDP-11/40 System and related peripherals. If carpeting is installed on the installation room floor, it should be of a type designed to minimize static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

2.2.4 Electrical Requirements

The PDP-11/40 can be operated from a nominal 115 or 230 Vac, 50/60 Hz power source. Line voltage should be maintained within 10 percent of the nominal value and the 50/60 Hz line frequency should not vary more than 3 Hz. A PDP-11/40 System with 16K of memory and standard peripherals requires approximately 690W of input power (6A @ 115 Vac, 3A @ 230 Vac).

Primary power to the system should be provided on a line separate from lighting, air-conditioning, etc., so that computer operation is not affected by voltage surges or fluctuations.

The PDP-11/40 cabinet grounding point should be connected to the building power transformer ground or to the building ground point. Any questions regarding power requirements and installation wiring should be directed to the DEC Sales Engineer or Field Service Engineer.

Primary power outlets at the installation site must be compatible with the PDP-11/40 primary input connectors. The input connectors provide power directly to the cabinet-mounted 861 Power Controller (one per cabinet) and each model of the power controller uses a specific type of connector. Power controller models 861-B and 861-C are used in the PDP-11/40 System cabinets. Refer to Figure 2-1 in the *861-A, B, C Power Controller Maintenance Manual,* DEC-00-H861-A-A-D for complete connector information.

2.3 INSTALLATION PROCEDURES

The procedures presented in the following paragraphs are provided to assist in unpacking, inspecting and installing the PDP-11/40 System and associated processor options.

CAUTION

Do not attempt to install the system until DEC has been notified and a DEC Field Service Representative is present.

2.3.1 Unpacking

Before unpacking the equipment, check the shipment against the packing list. Ensure that the correct number of packages has been delivered and that each package contains all the items listed on the accompanying packing slip. Also, make certain that all items on the accessories list in the Customer Acceptance Procedures have been included in the shipment. Unpack the cabinets as described in the following procedure.

1. Remove outer shipping container.

NOTE

The container may be either heavy corrugated cardboard or plywood. In either case, remove all metal straps first, then remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from around the cabinet perimeter.

2. Remove the polyethylene cover from the cabinets.
3. Remove the tape or plastic shipping pins, as applicable, from the cabinet(s) rear access door(s).
4. Unbolt cabinet(s) from the shipping skid. The bolts are located on the lower supporting siderails, and are exposed by opening the access door(s). Remove the bolts.
5. Raise the leveling feet above the level of the roll-around casters.
6. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.
7. Roll the system to the proper location for installation.
8. If applicable, repeat steps 1. through 7. for the expansion cabinets.
9. When the cabinets are oriented properly, follow the procedures in Paragraphs 2.3.2 and 2.3.3 to install the cabinet(s).

2.3.2 Inspection

After removing the equipment packing material, inspect the equipment, and report any damage to the local DEC sales office. Inspect as follows:

1. Inspect external surfaces of the cabinets and related equipments for surface, bezel, switch, and light damage, etc.

2. Remove the shipping bolts from the rear door, then open the rear door of the cabinet. Internally inspect the cabinet for console, processor, and interconnecting cable damage; also inspect for loose mounting rails, loose or broken modules, blower or fan damage, any loose nuts, bolts, screws, etc.

3. Inspect the wiring side of the logic panels for bent pins, broken wires, loose external components, and foreign material.

4. Inspect the power supply for proper seating of fuses and power connections.

5. Inspect all peripheral equipment for internal and external damage. This includes inspection of magnetic tape and DECtape transport heads, motors, paper-tape sprockets, etc.

CAUTION

Do not operate any peripheral device which employs motors, tape heads, sprockets, etc., if they appear to have been damaged in shipment.

2.3.3 Cabinet Installation

The PDP-11/40 cabinets are provided with roll-around casters and adjustable leveling feet. It is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation). Cabinet installation procedures follow.

NOTE

In multiple cabinet installation, receiving restrictions may necessitate shipping cabinets individually or in pairs. In such cases, the cabinets are connected at the installation site.

1. With the cabinets positioned in the room, install H952-GA Filler Strips between cabinet groups (filler strips are shipped attached to the end of a cabinet group). Remove 4 bolts each from the front and rear filler strips. Butt the cabinet groups together while holding the filler strips in place and rebolt through both cabinets and the filler strips. Do not tighten the bolts securely at this time.

2. Lower the leveling feet so that the cabinet(s) are not resting on the roll-around casters but are supported on the leveling feet.

3. Use a spirit level to level all cabinets and ensure that all leveling feet are firm against the floor.

4. Tighten the bolts that secure the cabinet groups together and then recheck the cabinet leveling. Again ensure that all leveling feet are planted firmly on the floor.

5. Remove the shipping bracket that secures the extendable BA11-FC Mounting Box in the cabinet.

2.3.4 AC Power Connections

A 3-wire cable is used to connect the site source power to the power controller in the H960-C cabinet. The cable is connected at the factory for either 230V, 50 Hz or 115V, 60 Hz operation. All cabinets in a PDP-11/40 System include a power controller and a single ac power cable; power is distributed within the cabinet from the power controller.

Proper connection of power is basic to system operation and personnel safety. Power cables must be connected to a site power system that provides ac power plus ground. The cabinets should be grounded to an earth ground, with ground straps connecting all the cabinets to each other. In addition, the frame ground wire in each power cable connects the cabinet ground system to the site power system ground.

Before connecting any power cables to the site source power, check all site wiring. Ensure that power receptacles of the appropriate types have been provided for each cabinet, and that the receptacles are positioned close enough to the cabinet positions to allow connecting the cables without stretching or crossing the cables. In particular, check that the proper voltage levels are present and that the phase wires have been connected to the same pins in each receptacle so that all cabinet power controllers receive the same voltage phase.

2.3.5 Intercabinet Connections

When a multi-cabinet system is assembled, three types of electrical connections must be made between cabinets (see Paragraph 2.3.3 for mechanical connections). These connections are:

a. Unibus connections – a BC11-A cable must connect the last system unit in a cabinet to the first system unit in the next cabinet. The shortest possible length should be used to reduce loading.

b. Remote power connections – all cabinet power controllers are interconnected by a 3-wire control bus that provides for system turn-on and turn-off and emergency shut-off.

c. Ground strapping – the frame ground of the system is distributed through the cabinets by direct electrical connections between the cabinet frames.

2.3.5.1 Unibus Connections – To connect the Unibus between the H960-C Cabinet and an H960-D Expansion Cabinet, insert the BC11-A cable in the rear system unit slot of the BA11-FC Mounting Box of the H960-C Cabinet. The cable then runs through a cable clamp in the upper left corner at the rear of the BA11-FC Mounting Box and is passed under the power supply mounting rails into the next cabinet. In the H960-D Cabinet, the cable passes through a similar cable clamp and is inserted in the appropriate slot of the first system unit of the mounting box. The BA11-FC is noted above as an example, other mounting boxes might be the last box.

2.3.5.2 Remote Power Connections – Each cabinet in the system has one 861 Power Controller. All controllers are connected by a 3-wire bus that enables a remote turn-on and turn-off, and an emergency shut-off. There are three Mate-N-Lok connectors on each power controller for the 3-wire bus. A cable is supplied with each cabinet to connect the power control of that cabinet to the next cabinet. Because each 861 Power Controller must be capable of connecting to the 861 Power Controllers in the preceding and following cabinets, two Mate-N-Lok connectors are reserved for the intercabinet cables. The third connector is provided for connection to a remote on/off switch and a thermal switch, or other emergency shut-off devices within the cabinet.

2.3.5.3 Ground Strapping – Electrical safety is provided by connecting all the cabinet frames to the ground level of the site power system. This is done by connecting a wire in each power cable between the frame and the power system ground; this is not a load carrying wire, and is intended only as an emergency ground path. The green wire in each power cable is the frame ground, while the white wire is the neutral, or return wire, that carries the load current.

To improve the level of safety provided by the frame ground connections, all cabinet frames are connected by braided copper straps of 4 AWG solid wire with crimp-on lugs, which are fastened to copper studs that are welded to the frames (this also prevents the generation of ground loops between cabinets that are connected by signal-carrying cables). The studs are welded to the bottom side rails of the cabinet frame, facing inward; the stud on the left side of the cabinet is slightly forward of center while the stud on the right side is slightly to the rear.

The ground strap supplied with each cabinet is fastened to one stud, passed over the side rail of that cabinet and the side rail of the adjacent cabinet, and fastened to the stud in that cabinet. The copper studs are threaded, and nuts are supplied on the studs.

2.3.6 Remote Peripheral Interconnection

Installation instructions for remote peripherals, such as line printers, card readers, and magnetic tape units, are covered in the appropriate peripheral maintenance manual. Normally, the peripheral itself is a free-standing unit and the peripheral controller is mounted in one of the system drawers. The controller and peripheral must be interconnected, and the peripheral must also be connected to an ac power source.

In a basic PDP-11/40 System, there is a small peripheral controller mounting slot that houses the controller for the system input/output device (LA30 DECwriter or Teletype unit). This device is characteristic of remote peripherals installation.

When installing the system, it is necessary to interconnect the system and the input/output device (DECwriter or Teletype) as described in the following steps:

1. Place the free-standing LA30 DECwriter or Teletype in the desired position next to the system cabinet.

2. Run the control cable from the DECwriter or Teletype unit through the back of the system cabinet and through the cable clamp at the rear of the mounting box. Note that because of the size of the control cable connector one side of the cable clamp must first be loosened and moved aside before the connector can be brought into the box.

3. Bring the cable connector into the mounting box and connect it to the receptacle on the input terminal control (DL11, KL11, or LC11) mounted in the small peripheral controller slot of the processor.

4. Place the cable clamp moved in step 2. above over the cable and tighten.

5. Verify that the input terminal control module is plugged securely into the small peripheral controller slot.

6. Connect the power cable from the DECwriter or Teletype unit into one of the 861 Power Controller power receptacles.

2.3.7 Installation Verification

Prior to turning power on, proper installation of all processor internal options and memory should be verified. Although memory and processor options are installed in the system at the factory, installation should be verified at the site.

Installation verification procedures for the available processor options are given in Table 2-1. Verification procedures for core memory, as well as procedures for installing additional memory, are given in Table 2-2. A diagram of the memory system unit is shown in Chapter 6 (Figure 6-4).

Table 2-1
Option Installation Verification

Option	Procedure
KE11-E Extended Instruction Set (EIS) Option	1. Verify that KE11-E module M7238 is installed in slot 02 (sections A–F) of processor backplane. 2. Ensure that jumper W1 on print K3-8 of KD11-A processor module M7233 (located in slot 05, sections A–F) has been removed. 3. Ensure that the three over-the-back cables have been connected to the 40-pin Berg connectors on the M7238 KE11-E module and the M7232 processor module (slot 03, section A-D). These cables provide a required logic interconnecton between the processor and the KE11-E option.
KE11-F Floating Instruction Set (FIS) Option	1. Verify that the KE11-E option has been installed. The KE11-E is a prerequisite for the KE11-F. 2. Verify that KE11-F module M7239 is installed in slot 01 (sections A–D) of processor backplane. 3. Ensure that the three jumpers on the KE11-E M7238 module have been removed. These jumpers must be removed to allow the KE11-F option to execute floating-point instructions. The jumpers are as follows: **Jumper / Print / Module** W1 / KE-2 / M7238 W2 / KE-5 / M7238 W3 / KE-9 / M7238
KT11-D Memory Management Option (requires the KJ11-A installation procedure also)	1. Verify that KT11-D module M7236 is installed in slot 08 (sections A–F) of processor backplane. 2. Verify that processor jumper changes have been made as indicated below (these changes are detailed in the installation section of the KT11-D option manual): Verify that the following jumpers have been removed: **Jumper / Print / Module** W9 / K1-8 / M7231 W6 / K1-8 / M7231 W5 / K1-8 / M7231 W1 / K1-7 / M7231 W2 / K1-7 / M7231 W3 / K1-7 / M7231 W4 / K1-7 / M7231 W7 / K1-9 / M7231 W8 / K1-9 / M7231

Table 2-1 (Cont)
Option Installation Verification

Option	Procedure
	Verify that the following jumpers have been moved in accordance with notes on prints: W10 K1-6 M7231 W2 K4-4 M7234 Verify that the following components have been added: C113 K4-4 M7234 C114 K4-4 M7234
KJ11-A Stack Limit Register	1. Verify that KJ11-A module M7237 is installed in slot E03 of the processor backplane. 2. Verify that the following processor jumpers have been moved in accordance with notes on prints: **Jumper Print Module** W2* K1-7 M7231 W1 K4-4 M7234 W1 K5-4 M7235 *Note that if the KT11-D option is present, jumper W2 of M7231 is removed completely.
KW11-L Line Time Clock	Verify that KW11-L module M787 is installed in slot F03 of the processor backplane. Verify that the backpanel wire between pin F03R2 and F03V2 for BG6 H has been removed.
KM11-A Maintenance Console	This option consists of a double-length module (W130/W131) that is plugged into slot F01 when used to monitor KD11-A operation, and slot E01 when used to monitor KT11-D, KE11-E, or KE11-F operation. Note that this option is not installed in the system during normal use.

Table 2-2
Memory Verification or Installation

Memory	Procedure
MF11-L Core Memory (basic to PDP-11/40)	1. Verify proper address selection on jumpers on G110 Control & Data Loops module. 2. Verify that modules are installed for basic 8K memory as follows: **Module** — **Slot/Sections** H214 Memory Stack — 01/C–F G231 Memory Drivers — 02/A–F G110 Control & Data Loops — 03/A–F 3. Verify Unibus interconnection to the KD11-A processor (M981) and interconnection or termination to rest of system (M920 or M930). 4a. *If older type system:* Verify that system unit power cable (D-IA-7009103-0-0) is connected from the system unit to Mate-N-Lok receptacles of the power distribution panel located on the BA11-FC Mounting Box (see Figure 6-10). Connector P1 goes to 3; connector P2 goes to 4. 4b. *If newer type system:* Verify that system unit power cable (D-IA-7009565) is connected from the system unit to the power distributors: the -15V connector (15 pin, 2 wire: blue and black) and the 6 pin signal connector, to the first power distributor; the +5V connector (15 pin) to the second power distributor.
MM11-L Core Memories (additional memories added to MF11-L memories)	1. Select proper address selection on jumpers on G110 Control & Data Loops module. 2. For 16K memory, insert modules as follows in addition to the 8K configuration described above: **Module** — **Slot/Sections** G231 Memory Drivers — 04/A–F G110 Control & Data Loops — 05/A–F H214 Memory Stack — 06/C–F 3. For 24K memory, insert modules as follows in addition to the 16K configuration described above: **Module** — **Slot/Sections** G231 Memory Drivers — 07/A–F G110 Control & Data Loops — 08/A–F H214 Memory Stack — 09/C–F

Table 2-2 (Cont)
Memory Verification or Installation

Memory	Procedure
MF11-L Core Memory (expansion units added to basic PDP-11/40)	1. Insert the MF11-L system unit into the BA11-FC Mounting Box using thumb screws provided. 2. Rearrange Unibus connections and termination using the M920 and M930, respectively. If memory is last unit in the mounting box, use BC11-A cable for interconnection to a next box. 3. Verify proper address selections on jumpers on G110 Control & Data Loops modules. 4. Insert modules according to locations noted for MF11-L Core Memory (basic) and MM11-L Core Memories (additional). 5a. *If older type unit:* A system unit power cable (D-IA-7009174-0-0) is used to connect the backpanel of the additional MF11-L to the power distributor panel's Mate-N-Lok receptacles. See Paragraph 6.4.7 for power loading restrictions. 5b. *If newer type unit:* Same as 5a, except that the power cable is D-IA-7009560. **NOTE** **If PDP-11/20 Memory Systems are installed, they must be housed in their own mounting boxes and powered by their own power supplies.**
MF11-U/UP	1. Install the MF11-U/UP backplane into the mounting box, using the screws provided. 2. Rearrange or install Unibus connections, as required. 3. Verify that address and interleaving jumpers are correct. Refer to Chapter 2 of the *MF11-U/UP Core Memory System Maintenance Manual,* DEC-11-HMFMA-C-D, for details. 4. Insert modules as shown in Chapter 1 of the *MF11-U/UP Core Memory System Maintenance Manual.* 5a. *If early type unit:* Install as explained in Paragraph 6.4.7 of this manual. 5b. *If later type unit:* Install power harness 7009535 between the MF11-U/UP and the Power Distribution Panel. If this memory is next to the PDP-11/40 CPU, the harness should be plugged into the second power distributor (not the same one as the CPU).

Table 2-2 (Cont)
Memory Verification or Installation

Memory	Procedure
MF11-U/UP (Cont)	6. Make sure that an H754 +20, −5V regulator is installed in the H742 Power Supply. 7. A complete checkout procedure is included in the *MF11-U/UP Core Memory System Maintenance Manual,* Chapter 5.

2.3.8 Initial Power Turn-on

NOTE
Power distribution system differences are described in Chapter 6. Refer to Figures 6-10 and 6-13 for plug locations.

Before turning power on, check the PDP-11/40 System as described in the following steps:

1. Ensure that all installation verification procedures (Paragraph 2.3.7) have been performed.

2. Before plugging in the system ac power cord, disconnect the following Mate-N-Lok connectors in the basic H742 Power Supply wiring harness: P1 through P7 (and P18 if a newer system). Note that connectors P8 through P15 remain connected.

3. Turn off the circuit breaker on the 861 Power Controller. (If more than one cabinet exists, turn off all 861 Power Controllers.) Check all cable connections for proper seating.

CAUTION
Before connecting the 861 Power Controller to local power, be certain that line frequency and voltage are compatible with power controller requirements. Line frequency should be 50–60 Hz (±3) and line voltage should be 180–270V for the 861-B Power Controller and 90–135V for the 861-C Power Controller.

4. Plug in the ac power cord, turn on the circuit breaker and check the dc voltages generated by the regulators. These voltages can be checked at pins of connectors P1 through P6 (and P18 if a newer system). See Figures 6-11 and 6-14 for specific pin numbers. Check fan ac power on connector P7. If any voltages are found to be incorrect, refer to power system maintenance in Chapter 7 and take corrective action before continuing to the next step of this procedure.

5. Turn off the circuit breaker and reconnect all connectors.

6. Turn on circuit breaker and perform voltage regulator checks in accordance with Paragraph 7.4.2.2.

7. Verify correct operation of the 861 Power Controller's REMOTE/OFF/LOCAL switch in accordance with Paragraph 7.4.2.3.

2.4 INITIAL OPERATION AND PROGRAMMING

Once the system has been installed and power applied, preliminary operating and programming procedures should be followed prior to using the system. Console operation, as well as the basic operating procedures noted in Chapter 3, should be performed first. If the user is already familiar with console operation, then the basic operating procedures given in Paragraph 3.6 may be performed immediately. These procedures are necessary to, but independent from, the customer acceptance procedure noted in Paragraph 2.5.

After initial operation, the above procedures use a common set of system, peripheral, and individual instruction diagnostics. These programs, listed in Table 7-3, define initial acceptance and operation. They also provide for a continuing check on proper operation and permit analysis of system failures.

2.5 CUSTOMER ACCEPTANCE

Verify correct system operation by performing the Customer Acceptance Procedures. The Customer Acceptance Procedures document is shipped with the PDP-11/40 System and lists all the tools, programs, and tests required to certify system operation.

CHAPTER 3
SYSTEM OPERATION

3.1 SCOPE

This chapter provides the information necessary to operate and program the PDP-11/40 System and associated input/output terminal, (LA30 DECwriter or ASR 33 Teletype). The description is divided into five major parts: programmer's console, DECwriter, Teletype, basic system operation, and basic system programming.

The description of controls and indicators for the consoles is in tabular form and provides the user with the type and function of each operating switch and indicator. Operating controls for peripheral devices that are not part of the basic machine are contained in the appropriate peripheral manual. Operation of the programmer's console, LA30 DECwriter, and ASR 33 Teletype is covered in Paragraphs 3.2, 3.3, and 3.4, respectively.

Basic step-by-step procedures for both manual and program operation are given in Paragraph 3.5. More specifically, procedures for loading the bootstrap loader, absolute loader, and the maintenance loader are provided in Paragraphs 3.5.3, 3.5.4.1, and 3.5.4.2, respectively. Basic system programming is covered in Paragraph 3.6.

3.2 KY11-D PROGRAMMER'S CONSOLE

The KY11-D Programmer's Console (Figure 3-1) provides the PDP-11/40 System with a necessary and useful programmer's interface. Manual operation of the system is controlled by switches mounted on this console which is the front panel of the basic mounting box. Visual displays indicate processor operation and the contents of the address and data registers.

All register displays and switches, whether marked on the console panel or not, are numbered from right to left. The numbers correspond to the power of two: 2^{15} . . . . . 2^{2}, 2^{1}, 2^{0}. Therefore, the most significant bit (MSB) is at the left of each specific register or display, the least significant bit (LSB) is at the right. Whenever an indicator is on, it denotes the presence of a binary 1 in the particular bit position. The alternate color coding on the console identifies the different functions or segments of the binary word in octal format.

In addition to the alternate segment color coding, the DATA register contains an index mark that divides the low-order byte (bits 7–0) from the high-order byte (bits 15–8). The high-order byte is divided into octal format by two more index marks. No marks are required for the low-order byte because octal coding for this byte is identical to the alternate segment color coding.

Figure 3-1 shows the location of all PDP-11/40 console controls and indicators. Each indicator and associated function is listed in Table 3-1. Each control and related function is listed in Table 3-2.

Figure 3-1a PDP-11/40 Programmer's Console

Figure 3-1b PDP-11/35 Programmer's Console

Table 3-1
PDP-11/40 Console Indicators

Indicator	Type	Function	Remarks
DATA	16-bit display MSB at left Color-coded in 3-bit segments for octal format Byte division noted with additional indexing for octal format in upper byte	Displays the output of a processor data multiplexer which gates information from a variety of sources within the processor. Normal programming use results in the following displays: HALT instruction has R(00) RESET instruction has R(00) WAIT instruction has R(IR) SINGLE STEP and HALT switch has Processor Status (PS) The display of the data multiplexer is especially important when used in the single clock mode. During this mode, the KM11 Maintenance Console is used to step through a program a single microword at a time. In this instance, the information in the DATA display is the result of a single microword and shown on the processor flow diagrams (refer to *KD11-A Processor Manual*).	When console switches are used, information shown on the DATA display is as follows: LOAD ADRS – the transferred Switch register address. DEP – the Switch register data just deposited. Note that data and address are correlated. The address is where this data was stored. EXAM – the information from the address examined. Note address and data correlate. HALT – displays the current Processor Status (PS) word. When a programmed HALT instruction is issued, bus control is transferred to the console and processor register R0 is displayed on the DATA display. This allows program identification of halts. During DMA operations, the processor is not involved in data transfer functions. Therefore, the data displayed in the DATA display is not that of the last bus operation.

Table 3-1 (Cont)
PDP-11/40 Console Indicators

Indicator	Type	Function	Remarks
ADDRESS	18-bit display MSB at left Color-coded in 3-bit segments for octal format	Displays the address in the Bus Address register (BAR) of the processor. This varies with an instruction execution but for a HALT, WAIT, or single step operation, the program counter is displayed between operations. The updated (or incremented) value of the program counter is always displayed. If the KT11-D Memory Management Option is not included in the system, the two most significant bits (A17, A16) are ordered according to the lower 16 bits; they are set only when bits A15, A14, and A13 are all set. Addresses between 160000 and 177777, therefore, are translated to addresses between 760000 and 777777, respectively. If the KT11-D option is installed, the ADDRESS display usually displays a virtual address with the KT11-D providing an offset physical bus address (not displayed). During console operations, however, the console provides and displays a full 18-bit physical address.	When console switches are used, information shown on the ADDRESS display is as follows: LOAD ADRS – the transferred Switch register address. DEP or EXAM – indicates the bus address just deposited into or examined. During a programmed HALT or WAIT instruction, the ADDRESS displays the incremented address of the instruction. The BAR is the instruction location plus 2. In single instruction mode, the next PC is placed into the BAR and displayed in ADDRESS between instructions. During DMA operations, the processor is not involved in the data transfer functions, and the address displayed in the ADDRESS display is not that of the last bus operation. Within instructions, the display indicates various processor bus addresses. These values are apparent only in a maintenance mode, using the KM11 and single clocking.

Table 3-1 (Cont)
PDP-11/40 Console Indicators

Indicator	Type	Function	Remarks
RUN	Single light	When the RUN indicator is on, the processor clock is running and is operating on an instruction or looping in console operation. When the RUN indicator is off, the microprogramming is not processing an instruction. The processor may be in control of the bus and awaiting a response for a data transfer; or the processor may have relinquished bus control for an NPR or BR request.	During normal machine operation, the RUN light flickers on and off (indicated by a faint glow). A programmed RESET command turns off the RUN light. This also occurs between single clocks when the KM11 Maintenance Console is used. For programmed HALT and WAIT instructions, the clock continues to run with the processor looping in the microprogram. This is also true for console operation from the HALT switch.
PROC	Single light	When on, indicates that the processor is controlling the Unibus as the master device.	When the PROC light is on and the RUN light is off, the processor is waiting for data from the bus.
BUS	Single light	When on, indicates that some device has control of the Unibus. If the PROC indicator is lighted, that device is the processor.	This display is useful for determining where bus control is and that it is present.
CONSOLE	Single light	When on, indicates that the processor is in the console mode (manual operation). Control switch activation is sensed and acted upon.	NPRs and BRs are not serviced in the console mode. Bus errors are also serviced differently (see Table 3-2 for details).
USER	Single light	When on, indicates that the processor is in the user mode and certain KT11-D restrictions on instruction operation and processor status (PS) word loading exist. Refer to the KT11-D option discussion in Chapter 4 of this manual and the KT11-D manual.	Does not function unless the KT11-D Memory Management Option has been installed in the system.

Table 3-1 (Cont)
PDP-11/40 Console Indicators

Indicator	Type	Function	Remarks
VIRTUAL	Single light	When on, indicates that a virtual address is displayed in the ADDRESS display. This virtual address is usually modified by the KT11-D option to provide a different physical address for the Unibus. If the KT11-D option is installed, this display is usually active during program operation. During console operation, the console ADDRESS display and Switch register both provide a full 18-bit physical address. The VIRTUAL light is off in this instance. When VIRTUAL light is off, it indicates that the bus address indicated by the ADDRESS display is the physical address.	Does not function unless the KT11-D Memory Management Option has been installed in the system.

Table 3-2
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
OFF/POWER/LOCK	3-position, key operated switch	Provides system power control and lock-out of console controls as follows:	
		OFF position – removes all power from the system.	System not being used.
		POWER position – applies primary power to the system. All console controls are fully operational when switch is in this position.	Normal operation.
		LOCK position – disables all console (panel) controls except the Switch register key switches. This prevents inadvertent control switch operation from disturbing a running program.	System operating; console control disabled.
		The data entered in the Switch register is still available to the processor whenever the program explicitly addresses the Switch register (address 777570).	

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
Switch register	18 key-type switches Bit position of each switch is labeled; MSB is at left. Color-coded in 3-bit segments for octal format. Up position – logical one (or on). Down position – logical zero (or off).	Provides a means of loading an address or data word into the processor. If the word in the Switch register represents an address, it can be loaded into the ADDRESS register by depressing the LOAD ADRS key. If the word contains data, it is loaded into the address specified by the ADDRESS register by lifting the DEP key. If the KT11-D Memory Management Option is used, bits 17 and 16 are directly used as the physical bus address during console operation. If the KT11-D option is not installed, the processor bus address bits 17 and 16 are set if Switch register bits 15, 14, and 13 are all set. Bits 17 and 16 of the Switch register have no effect. The contents of the Switch register may be used by the processor any time the program explicitly addresses the register at address 777570. This address can only be used by the processor.	

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
LOAD ADRS	Momentary key-type switch Depress to activate	The LOAD ADRS switch transfers the contents of the Switch register to the Bus Address register (BAR) through a temporary location R(ADRSC) within the processor. This bus address, displayed in ADDRESS, provides an address for the console functions of EXAM, DEP, and START.	The address is loaded into a temporary location which is not modified during program execution. To restart a program at a previously specified address, it is only necessary to depress the START switch. **NOTE** **Consecutive examine or deposit functions increment the value of the loaded address both in the BAR and in R(ADRSC).** Console operations are word-ordered operations. If an odd bus address (bit 00 enabled) is used, the odd address is stored in the Bus Address register and the temporary location. Examine or deposit operations on this address will be treated as word operations (bit 00 is ignored).

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
EXAM	Momentary key-type switch Depress to activate	The EXAM switch uses the contents of R(ADRSC) as a bus address; the contents of this bus address is displayed in DATA, the bus address is displayed in ADDRESS. A LOAD ADRS operation usually pre-establishes the initial R(ADRSC) address; sequential examines automatically update R(ADRSC). If the EXAM switch is depressed twice in succession, the contents of R(ADRSC) is word incremented and the next sequential bus address is examined. This action is repeated each time EXAM is depressed provided no other switch is used between these steps. When the LOAD ADRS or DEP switch is depressed, it destroys the incrementing sequence. The next time EXAM is used, it displays the current address rather than the next sequential address.	If an odd address is examined, bit 00 is ignored. For example, if address 1001 is examined, the address 1000 is displayed in ADDRESS. Byte data for location 1001 is located in DATA (bits 15–08). An EXAM operation that references a non-existent address causes a time out (with no TRAP) and the Switch register address (777570) is displayed in DATA.

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
CONT	Momentary key-type switch Depress to activate	Causes the processor to continue operation from the point at which it had stopped. If the ENABLE/HALT switch is in the ENABLE mode, CONT returns bus control from the console to the processor and continues program operation. If the ENABLE/HALT switch is set to HALT, depressing the CONT key causes the processor to perform a single instruction. Control is returned to the console after each instruction, permitting a program to be stepped through one instruction at a time. BRs and interrupts are serviced in this mode of operation.	If program stops, depressing CONT provides a restart without power clear. Because the restart occurs through the service portion of machine operation, any outstanding BRs may be serviced before program operation.

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
ENABLE/HALT	2-position, key-type switch	Allows either the program or the console to control processor operation. ENABLE position – permits the system to run in a normal manner. No console control requests are made. HALT position – halts the processor after the next instruction or outstanding TRAP sequences, and before Unibus Bus Requests service, and passes control to the console. The HALT mode is used with the CONT switch to step the machine through programs one instruction at a time. When the START switch is activated in the HALT mode, a system clear is effected without program start. This mode of operation is useful for clearing conditions in the system that might prevent proper operation. When the START switch is activated in the ENABLE mode, it provides a system clear with a program start.	Continuous program control requires the ENABLE mode. The HALT mode is used to interrupt program control, perform single instruction operation, or clear the system.

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
START	Momentary key-type switch Depress to activate initialize, release to have START function occur.	Depressing the START switch provides a system clear (initialize). When the ENABLE/HALT switch is set to HALT, the processor does not start. When ENABLE/HALT is set to ENABLE, releasing START begins processor operation. The starting address is that of the last console operation determined by R(ADRSC). Usually, this temporary location is loaded from the Switch register by a LOAD ADRS operation. If the program stops at any time, it can be restarted at its original location by the START switch; the value of R(ADRSC) remains unchanged. Use of the START switch in the HALT mode provides for a system clear. This mode of operation is useful for clearing conditions that might prevent proper operation.	

Table 3-2 (Cont)
PDP-11/40 Console Controls

Switch	Type	Function	Remarks
DEP	Momentary key-type switch Lift to activate	The DEP switch uses the contents of R(ADRSC) as a bus address. The contents of the Switch register are transferred to this location. After use, the data appears on the DATA display and the address is on the ADDRESS display. A LOAD ADRS operation usually pre-establishes the initial address; sequential DEP operations automatically update R(ADRSC). If the DEP switch is raised twice in succession, the contents of the Switch register is deposited in the next sequential bus address location. This action is repeated each time DEP is raised provided no other switch is used between these steps. Whenever the LOAD ADRS or EXAM switch is depressed, it destroys the incrementing process. The next time DEP is used, it deposits the current address rather than the next sequential address.	If an attempt is made to deposit an odd address, bit 00 is ignored and a word deposit occurs. A deposit operation that references a non-existent address causes a time out (with no TRAP). No error message is visible from the console for a deposit to a non-existent address. An immediate verification by an examine operation, however, would result in the display of the Switch register address in the DATA display.

3.3 DECwriter

The LA30 DECwriter is an input/output device that can be used with the PDP-11/40 System. Data can be entered into the processor via the keyboard or data from the processor can be printed out by the DECwriter under program control. Controls and indicators for the serial version LA30 DECwriter are shown in Figures 3-2 and 3-3 and listed in Table 3-3. The serial version of the LA30, the LA30-S, would normally be used with the PDP-11/40 in that it is compatible with the DL11 input terminal control and the DL11 is part of the PDP-11/40 basic configuration. The LC11 is compatible with the parallel version of the LA30, the LA30-P. Further detailed operating information is contained in the *LA30 DECwriter Manual* (DEC-00-LA30-DD) and in the *LC11 DECwriter System Manual* (DEC-11-HLCB-D).

Table 3-3
LA30 Controls and Indicators

Index	Control/Indicator	Function
1	READY	Lamp – Indicates power up on printer electronics and that the DECwriter is READY for use. Indicates an interrupt is enabled by keyboard electronics, if INT bit is set by software.
2	LOCAL LINE FEED	Switch – When depressed, causes a local line feed to be applied to the printer without a code being sent out to the computer. This control will also disrupt printing, but no characters will be lost.
3	MODE LOCAL LINE	2-Position Switch – Selects either local or on-line operation.
4	BAUD RATE 110, 150, 300	3-Position Switch – Selects the baud rate clock frequencies for 110, 150, and 300 baud.
5	MOTOR POWER	Breaker (CB2) – Applies power to printer stepping motor electronics.
6	AC POWER	Breaker (CB1) – Applies ac power to the unit power supply.

3.4 TELETYPE

The ASR 33 Teletype unit is an input/output device that can be used with the PDP-11/40 System. Data can be entered into the processor via the keyboard or through a paper-tape reader. The Teletype can also be operated off-line to punch paper tapes. Controls for the ASR 33 Teletype are shown in Figure 3-4 and listed in Table 3-4. Further detailed operating information is contained in the Teletype Corporation manuals listed in Table 1-2 of this manual.

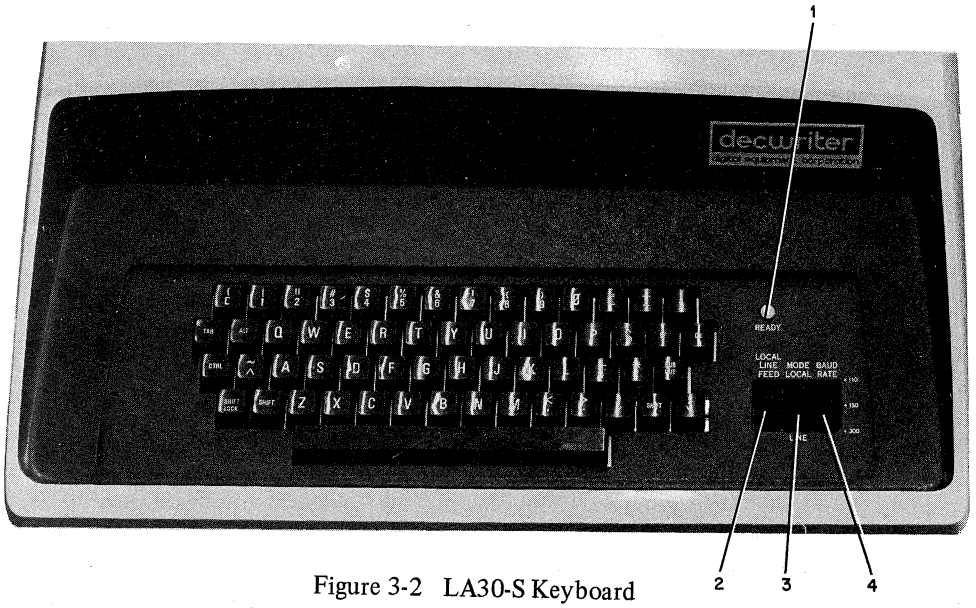


Figure 3-2 LA30-S Keyboard

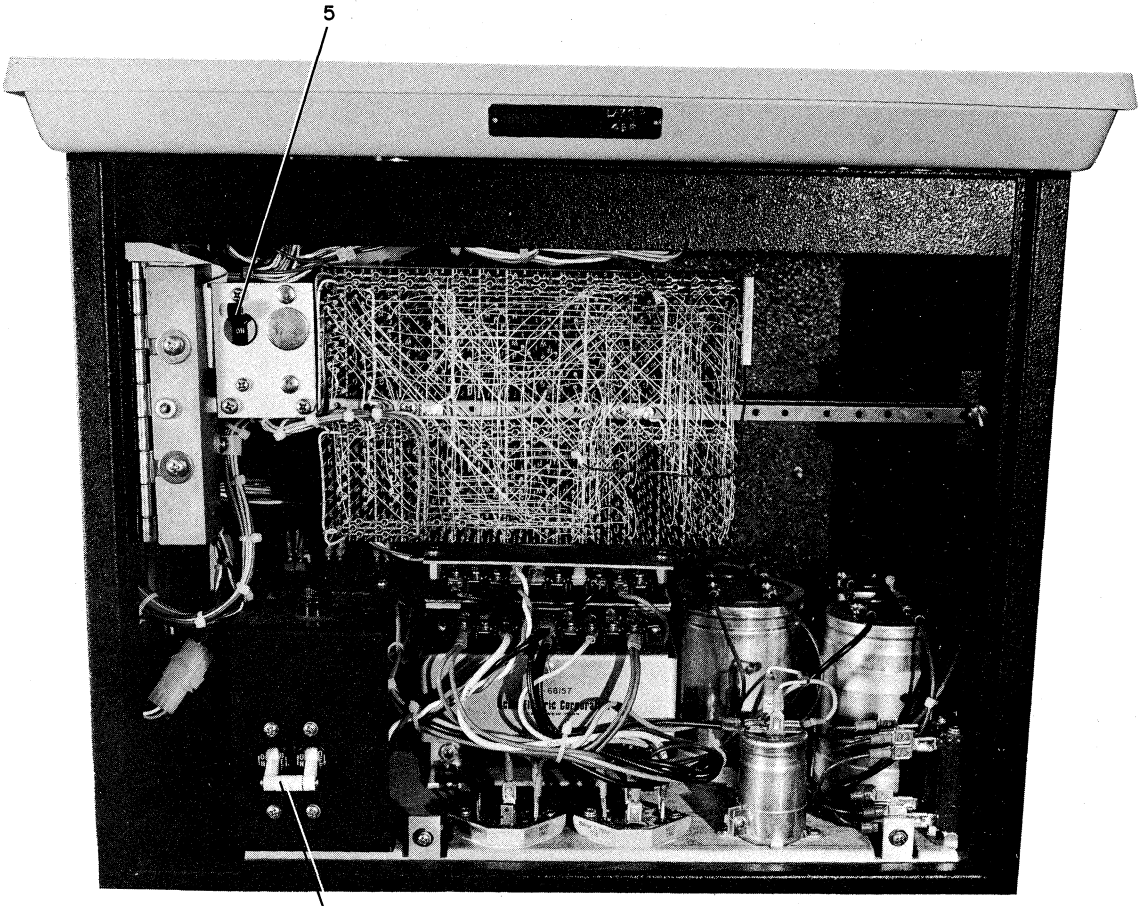


Figure 3-3 LA30 Power Controls

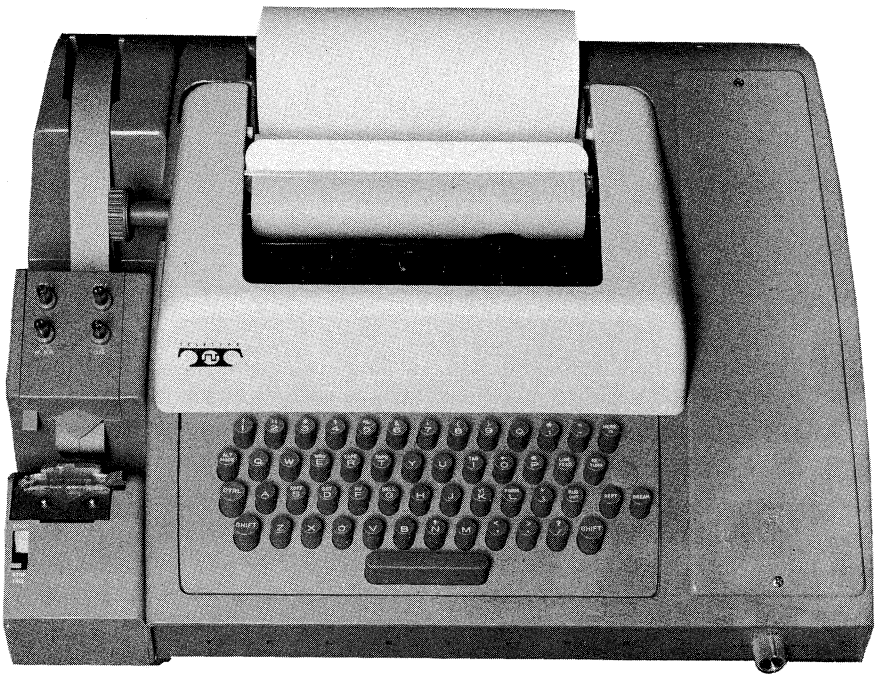


Figure 3-4 Teletype Controls

Table 3-4
Teletype Controls

Control	Type	Function	Remarks
Punch:			
REL. pushbutton	Momentary switch, depress to activate	Disengages the paper tape from the punch to allow loading or removal of tape.	
B. SP. pushbutton	Momentary switch, depress to activate	Backspaces the paper tape by one space each time the pushbutton is depressed to allow manual correction or rubout of character just punched.	
ON pushbutton	2-position switch, connected to OFF pushbutton	When depressed, turns on the paper-tape punch and releases OFF switch.	
OFF pushbutton	2-position switch, connected to ON pushbutton	When depressed, turns off the paper-tape punch and releases ON switch.	

Table 3-4 (Cont)
Teletype Controls

Control	Type	Function	Remarks
Reader:			
START/STOP/ FREE switch	3-position switch	Controls operation of the tape reader. START position – engages tape reader which begins operation under program control. STOP position – engages reader mechanism but does not energize it. In effect, tape is locked in the reader but reading operation does not begin until the switch is moved to START. FREE position – disengages reader to permit loading and unloading of tape.	Used on-line
LINE/OFF/ LOCAL switch	3-position rotary switch	Serves two functions: applies primary power to Teletype and connects computer to Teletype. LINE position – energizes Teletype and connects it to the computer as an input/output device. Signals from either the Teletype reader or keyboard can be used as an input while the computer output can be used to control the keyboard or punch. OFF position – deenergizes the Teletype by removing primary power. LOCAL position – disconnects the Teletype from the computer. The Teletype can be used for punching or reading tapes but all control is localized at the keyboard.	
Keyboard	45 printing characters 6 non-printing characters Typewriter-like layout	Uses a typewriter-like keyboard to print characters on paper, punch tape, or input information into the computer. Off-Line Operation (LOCAL) – When tape reader and punch are off, prints characters on paper.	

Table 3-4 (Cont)
Teletype Controls

Control	Type	Function	Remarks
Keyboard (cont)		When punch is on, simultaneously prints characters on paper and punches equivalent code into paper tape. When reader is on, reads code from punched paper tape and prints equivalent characters on paper. On-Line Operation (LINE) – When tape reader and punch are off, prints characters on paper and sends equivalent signals to the computer. When tape reader is on, reads code from punched paper tape and sends equivalent signals to computer. No characters are printed. When receiving signals from computer, prints equivalent characters on paper and punches tape if punch is on.	
Cover Guard	Latch, push to release	Used to hold paper tape in position when using tape reader.	

3.5 BASIC OPERATION

Many methods exist for storing, modifying, and retrieving information from the PDP-11/40 System. These methods depend on the form of the information, time limitations, and the peripheral equipment connected to the processor. The following procedures are basic to the use of the PDP-11/40 System. Although they may be used less frequently as the programming and use of the system become more sophisticated, they are valuable in preparing the initial programs and in learning the function of system input and output transfers. For an understanding of the various operational controls and indicators, refer to Paragraphs 3.2 through 3.4. Basic programming techniques are given in Paragraph 3.6.

Operating procedures are separated into the following categories:

a. Power on – Paragraph 3.5.1

b. Basic console control – Paragraph 3.5.2

c. Manual program loading – Paragraph 3.5.3

d. Automatic program loading – Paragraph 3.5.4

e. Running programs – Paragraph 3.5.5

3.5.1 Power On

When the programmer's console OFF/POWER/LOCK switch is turned from OFF to POWER, the system is initialized (zeroed). A time delay allows sufficient time for voltages to logic units (especially memory elements) to stabilize.

The power-up initialization logic directly sets the microprogram control to a sequence of controlled events determined by the setting of the ENABLE/HALT switch. If the console ENABLE/HALT switch is set to ENABLE when power is turned on, the processor executes a power-up microprogram sequence with the power-up vector address determined by jumpers on the Status module (M7235) of the KD11-A Processor. A new Processor Status (PS) word and Program Counter (PC) are unstacked from the vector address, and vector address plus two, respectively.

Program operation begins with an entrance to the FETCH portion of the microflow with the new PC used to obtain the first instruction. Note that the processor status module jumpers are initially set at octal location 24. This location can be changed to accommodate system requirements.

If the console ENABLE/HALT switch is set to HALT when power is turned on, the processor microflow is directly set to the console microloop. The machine awaits the activation of a console control switch.

The LOCK position of the programmer's console OFF/POWER/LOCK switch provides for program operation with the console control switches disabled. However, the console Switch register may still be accessed.

3.5.2 Basic Console Control

Two major areas of control exist: control influenced by the ENABLE/HALT switch, which selects either program or console control; and control by the switches and sequences used for loading data manually into the processor.

3.5.2.1 ENABLE/HALT Switch – When the processor has control (ENABLE/HALT in ENABLE), either the START or CONT switch causes the program to run. The START switch initializes the system with a clear signal and begins operation at a specific address determined by the last console operation (usually LOAD ADRS). The CONT switch merely releases console control, and the program continues at the existing Program Counter (PC).

When the ENABLE/HALT switch is set to HALT, the console obtains control. The LOAD ADRS, EXAM, and DEP switches can be used. The CONT switch can now cause the processor to step through the program a single instruction at a time.

3.5.2.2 Loading Data Manually – Whenever data is manually loaded into a computer, it is desirable to have the address increment automatically upon each deposit. Thus, the user can set a starting address and continue to store data in sequential memory locations providing only new data for each location. The programmer's console logic also permits the user to immediately examine the data just deposited without re-addressing, to re-deposit if necessary, and to continue with automatic incrementation. These sequences are associated with the functioning of the DEP and EXAM switches.

The address in the ADDRESS register, and R(ADRSC), does not increment the *first* time EXAM or DEP is used after a HALT or LOAD ADRS. It does not increment if DEP is used immediately after EXAM or if EXAM is used immediately after DEP. It does increment if a DEP is used immediately after a DEP, or if an EXAM is used immediately after an EXAM. This increment is a word increment as the console is word oriented. Thus, the user can look at a location, change it, deposit the changed data, and then reexamine it without having to load an address each time.

Incrementation is on even boundaries for all addresses except the addresses specifically designated for the processor internal registers, which are incremented by 1.

For example, to alter several successive locations, the following steps are performed:

1. LOAD ADRS (starting location)
2. EXAM (no increment – looks at starting location)
3. DEP (no increment – loads starting location)
4. EXAM (no increment – checks previous deposit)
5. EXAM (increment – looks at next location)
6. DEP (no increment – loads second location)
7. EXAM (no increment – checks previous deposit)
8. EXAM (increment – looks at third location)

If the user desires to take advantage of automatic address incrementation for examining or loading data, the following steps can be used to load data into sequential locations:

1. LOAD ADRS (starting location)
2. DEP (no increment – loads starting location)
3. DEP (increment – loads second location)
4. DEP (increment – loads third location
5. DEP (increment – loads fourth location)

   etc.

The same procedure can be used for examining data in sequential memory locations.

3.5.3 Manual Program Loading (Bootstrap Loader)

A primary manual use of the programmer's console is to store the bootstrap loader in the core memory. (Programs and data can be stored or modified by manual use of the programmer's console.) The bootstrap loader (DEC-11-L1PA-LA) is a minimal instruction program that can automatically load programs into core memory from a paper tape punched in a special bootstrap format. One of these programs, after being stored, can in turn load any binary format tape into the computer. (An explanation of the number designations used for DEC programs is given in Table 3-5.)

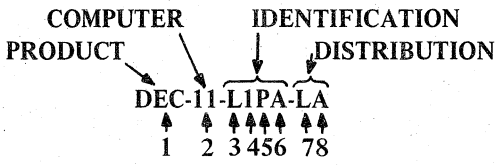
The sequence for loading the computer is shown in Figure 3-5, with programs noted as follows:

a. Bootstrap loader (DEC-11-L1PA-LA) – manually loaded by console switches; provides for automatic loading of programs punched in a special format.

b. Absolute loader – punched in special format; loaded by bootstrap loader; provides for automatic loading of programs punched in binary format.

c. Selected program – punched in binary format; loaded automatically by absolute loader.

Table 3-5
Program Identification Codes



Format:

Notes:

1	Product Code	MAINDEC	= maintenance library products
		DEC	= programming library products
2	Computer Series	11	= PDP-11 Computer Systems
3	Major Category	L	= Loader
4	Minor Category (sequential numbers)	1	= first in a series of programs
		2	= second in series, etc.
5	Option Category (hardware required to use software)	P	= paper tape system
		H	= high-speed reader and/or punch
		K	= Teletype keyboard only
		M	= magtape
6	Revision Category (sequential letters)	A	= basic program
		B	= first revision
		C	= second revision, etc.
7	Distribution Method	L	= listing
		P	= paper tape
8	Distribution Mode	A	= ASCII
		B	= binary (absolute)
		O	= other (bootstrap binary)

Example: DEC-11-L2PB-PO

Indicates a PDP-11 programming library product, second in a series of loaders, requiring a paper tape system to use, the first revision to the program, supplied as a paper tape in bootstrap binary format.

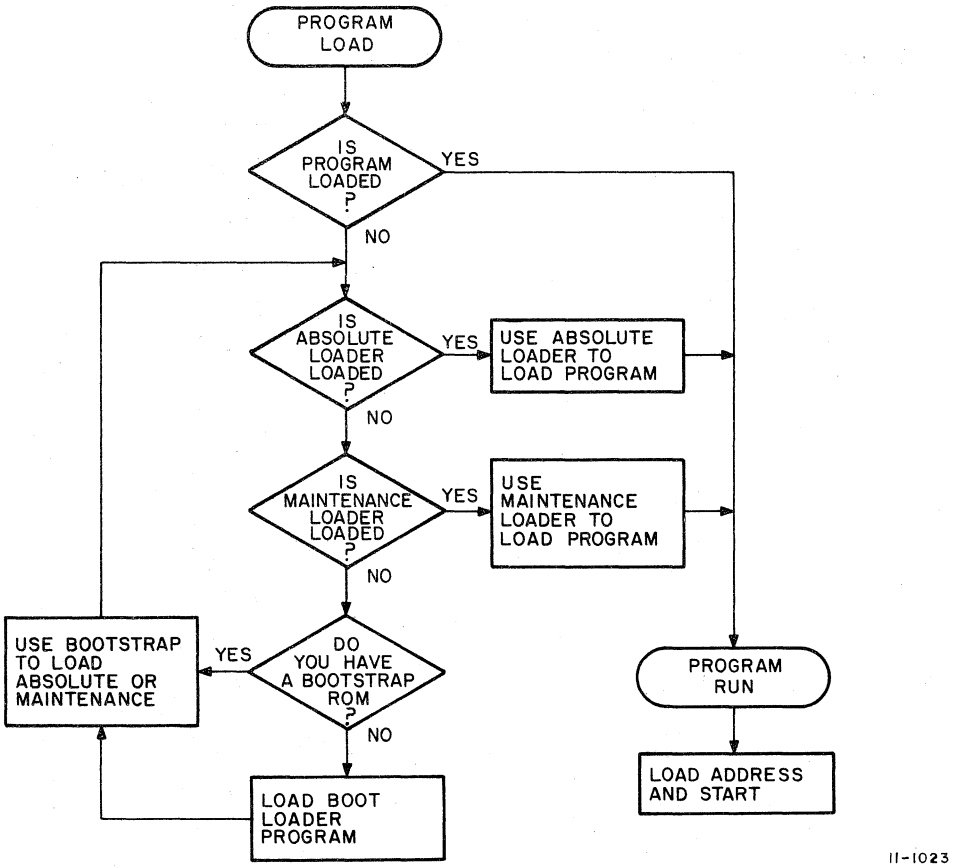


Figure 3-5 Flowchart of Procedure for Loading and Running Programs

To eliminate the necessity of more than one bootstrap loader, the bootstrap loader instructions contain two variables (x and y) to provide compatibility with various memory configurations and reading devices. These variables are listed in Table 3-6. A complete explanation of the bootstrap loader program is given in Chapter 5 of the *PDP-11 Paper Tape Software Programming Handbook* (DEC-11-XPTSA-A-D); further information may be found in the program listing, DEC-11-L1PA-LA.

Table 3-6
Bootstrap Loader
(DEC-11-L1PA-LA)

Bootstrap loader should be toggled into highest core memory bank.

Address	Instruction
xx7744	016701
xx7746	000026
xx7750	012702
xx7752	000352
xx7754	005211
xx7756	105711
xx7760	100376
xx7762	116162
xx7764	000002
xx7766	xx7400
xx7770	005267
xx7772	177756
xx7774	000765
xx7776	yyyyyy

xx represents highest available memory bank. First location of the loader is one of the following, depending on memory size; *xx* in all subsequent locations is the same as the first.

Address	Memory Bank	Memory Size
037744	1	8K
077744	2	16K
137744	3	24K
157744	4	28K

Contents of address xx7776 (yyyyyy) should contain device status register address of paper-tape reader to be used when loading the bootstrap formatted tape. Addresses are:

Teletype Paper-Tape Reader	177560
High-Speed Paper-Tape Reader	177550

The following procedure is used to manually load the BOOT bootstrap loader program (DEC-11-L1PA-LA):

1. Set ENABLE/HALT switch to HALT to give bus control to the console when powering up.

2. Turn OFF/POWER/LOCK switch to POWER position. This energizes the programmer's console.

3. Enter starting address of bootstrap loader (Table 3-6) into Switch register. Make certain that the correct xx value is used (*037*744 for 8K memory, *077*744 for 16K memory, *137*744 for 24K memory, etc.).

4. Depress LOAD ADRS switch. The address set in the Switch register is shown on the ADDRESS display.

5. Enter starting address *contents* (016701) into Switch register.

6. Lift DEP switch. The contents just entered in the Switch register is displayed in the DATA display.

7. Enter *contents* of next address into Switch register.

NOTE

It is not necessary to load addresses after the starting address has been loaded because the address is automatically incremented by two each time DEP is used consecutively.

8. Lift DEP switch.

9. Repeat steps 7 and 8 above for each location of the bootstrap loader. When loading the contents of address xx7766, make certain that the correct x value is used. When loading the contents of the last address, make certain that the correct y value is used.

10. The bootstrap loader program is now loaded in memory locations xx7744 through xx7776 and can be used to automatically load other programs into memory.

11. Correct program entry can be verified by examining the addresses between xx7744 and xx7776. This is accomplished by setting the starting address into the Switch register, depressing the LOAD ADRS switch and depressing the EXAM switch. The contents of the starting address are shown in the DATA display. Each time the EXAM is again depressed, the address is automatically incremented by two and the corresponding contents displayed.

12. Step 11 alone (verification) may be sufficient if the bootstrap loader program has already been loaded into the system. The program is stored in the last portion of available memory so that it tends to survive program operation and is available for reloading programs. If the program is not in tact, load according to the above procedure, beginning with step 1.

3.5.4 Automatic Program Loading

Information can be stored or modified in the computer automatically only if a program capable of performing these functions has previously been stored in the core memory. For example, having the bootstrap loader stored in the computer enables the user to operate any program that has been punched in the special tape format required by the bootstrap loader. Typical programs of this type include the absolute loader, the absolute dump, and the teleprinter dump.

The bootstrap loader is limited because of the special tape format; another loader is used to load any binary format tape into the computer. This is the absolute loader (DEC-11-L2PC-PO), which is loaded into the computer by the bootstrap loader. Once the absolute loader is in memory, any binary tape program (such as PAL III assembler, symbolic editor, input/output service routines, diagnostics, mathematical routines, etc.) may be automatically loaded.

The following paragraphs give procedures for loading the absolute loader, and for using the absolute loader to store other programs. A complete description of the absolute loader program is given in Chapter 5 of the *PDP-11 Paper Tape Software Programming Handbook,* DEC-11-XPTSA-A-D; refer also to the program listing, DEC-11-L2PC-LA.

3.5.4.1 Loading Absolute Loader – The following procedure is used for automatically loading the absolute loader program (DEC-11-L2PC-PO):

1. Set ENABLE/HALT switch to HALT.

2. Make certain that the bootstrap loader has been stored in core memory (Paragraph 3.5.3, step 11).

3. Enter starting address of bootstrap loader into Switch register. The starting address is xx7744 (*037*744 for 8K memory, *077*744 for 16K memory, *137*744 for 24K memory, etc.).

4. Depress LOAD ADRS switch. The address set in the Switch register is displayed in ADDRESS register indicators.

5. Place the input/output device (LA30 DECwriter or Teletype unit) on-line (connected to the computer).

NOTE

If some other reading device (such as the high-speed paper-tape reader) is used, ensure that the y value in bootstrap loader address xx7776 corresponds to the device as described in Table 3-6.

6. Place the absolute loader tape in the reader. Make certain that the special leader (a sequence of 351 punches) is under the reader station. Blank leader does not work.

7. Set ENABLE/HALT to ENABLE.

8. Depress START switch. The tape is now read into the computer which halts when the entire program is loaded.

9. When the tape is completely loaded, the DATA display lights may be in any configuration. The main reason for this is that no checksum capability exists in the bootstrap loader.

Any PDP-11 program punched in binary format may be loaded automatically by using the absolute loader. The absolute loader can be set up to select either an absolute or relocatable code. If a relocatable code is selected, the user may specify that the relocatable code start at a specific address or that the code start loading at the point the previous load stopped. The absolute loader also provides a checksum test to ensure accurate loading. Although the computer normally stops when the binary tape is loaded, instructions on the tape itself may cause the computer to begin execution of the program immediately after loading is finished. This action is beyond the control of the user because it is a part of the program on certain binary tapes.

The following procedure is used for automatic loading of binary tapes into the computer using the absolute loader:

1. Make certain that the absolute loader program is stored in core memory (Paragraph 3.5.4.1).

2. Set ENABLE/HALT switch to HALT.

3. Enter starting address of absolute loader into Switch register. The starting address is xx7500 (*037*500 for 8K memory, *077*500 for 16K memory, *137*500 for 24K memory, etc.).

4. Depress LOAD ADRS switch. The starting address of the absolute loader is now displayed in ADDRESS register indicators.

5. Select the type of load desired by setting the Switch register as specified in Table 3-7.

6. Make certain that input/output device (Teletype unit or LA30 DECwriter) is on-line.

NOTE

The reading device may be changed at any time by the user without reloading the absolute loader. If a reader is to be changed, simply replace the contents of address xx7776 with the appropriate device status address (y value in Table 3-6).

7. Load desired binary tape into reader by placing leader under the reader station.

8. Set ENABLE/HALT switch to ENABLE.

9. Depress START switch. This begins the binary tape load.

10. If the binary tape contains a transfer address instruction, the computer begins execution of the program as soon as loading is complete.

11. The computer stops when either loading is complete or there is a checksum error.

    a. Loading complete – the low-order (right-hand) byte displayed in the DATA indicators is zero. Additional binary tapes may be loaded by repeating steps 5 through 7 above and depressing the CONT switch.

    b. Checksum error – the low-order byte displayed in the DATA indicators is *not* zero, thereby indicating a checksum error has occurred in the previous block of data. In this case, reposition the tape in front of the error-producing block and depress the CONT switch.

Table 3-7
Binary Tape Load Selection
(using Absolute Loader)

Type of Load	Switch Register Settings	
	Bits 15–01	Bit 00
Normal (absolute)	Not applicable	0
Relocatable (continue where left off)	0	1
Relocatable (load at specified address)	Offset from tape origin	1

3.5.4.2 Loading Maintenance Loader – The maintenance loader program, MAINDEC-11-D9EA, provides an alternate method of loading diagnostic programs that can be used if the absolute loader fails to function because of a hardware failure. This loader should only be used to load diagnostic programs if the absolute loader malfunctions.

Use the following procedure to automatically load the maintenance loader:

1. Set ENABLE/HALT switch to HALT and depress START to clear the system.

2. Make certain that the bootstrap loader has been stored in memory, starting at address 037744.

NOTE

The maintenance loader operates in the lowest 8K of memory. If some other memory area must be used, several program locations must be changed as listed in Table 3-8 after the maintenance program is loaded.

3. Set Switch register to 037744 and depress LOAD ADRS.

4. Place the input/output (LA30 DECwriter or Teletype unit) on-line.

5. Place the maintenance loader tape in paper-tape reader.

6. Set ENABLE/HALT switch to ENABLE and depress START. The tape is read into memory and the processor halts when the entire program has been loaded.

NOTE

If the maintenance loader was not loaded into the lowest 8K of memory, make location changes at this time (Table 3-8).

Table 3-8
Relocation of Memory Contents

Move Contents of	To
xx7502	xx7470
xx7510	xx7474
xx7542	xx7475
xx7566	xx7475
xx7624	xx7776
xx7674	xx7474
Where xx equals:	03 for 8K memory 07 for 16K memory 13 for 24K memory

3.5.5 Running Programs

When running any program, the program must first be loaded into the core memory either manually or via the automatic loading programs (bootstrap loader or absolute loader). Once the program is in storage, it can be run at any time by loading the starting address of the program (refer to appropriate program documentation) into the Switch register, depressing the LOAD ADRS switch, and then depressing the START switch. The user also must make certain that the ENABLE/HALT switch is in ENABLE and that the appropriate external devices are on-line (connected to the computer).

The program can be manually stopped at any time by setting the ENABLE/HALT switch to HALT. It can be restarted from that point by returning the ENABLE/HALT switch to ENABLE and depressing the CONT switch. It can be started anew by reloading the starting address and depressing the START switch.

A program can be altered during operation, or new data introduced, through the Switch register. This console register has a bus address that the processor can reference in its instruction sequence. The information transferred may be treated as data or used to alter program flow.

Because of the speed of the computer, console indicators are of limited value while the computer is running. Console indicators are used primarily during manual operation, single instruction operation, or during the maintenance mode. During manual operation, the console indicators reflect the console operations of LOAD ADRS, EXAM, and DEP. During maintenance operations, the console indicators display various data functions of the processor as the maintenance module is used to step through the program a microword at a time. Use of the maintenance module is described in the *KD11-A Processor Maintenance Manual,* EK-KD11A-MM-001.

3.6 BASIC PROGRAMMING

To produce programs that fully utilize the power and flexibility of the PDP-11/40, it is necessary for the user to first become familiar with various programming techniques that are part of the basic design philosophy of the PDP-11/40 System. These techniques (such as use of stacks, subroutine linkage, interrupt nesting, reentrant and recursive programming, etc.) are covered in the *PDP-11/40 Processor Handbook,* which also provides a detailed discussion of the instruction set.

In addition to the general programming information given in the *PDP-11/40 Processor Handbook,* the user should be familiar with console operation (Paragraph 3.2) and with the basic and extended PDP-11/40 instruction sets described in Chapter 4.

For those users already familiar with PDP-11/20 system programming, the primary programming differences between the PDP-11/20 and PDP-11/40 Systems are listed in Table 3-9. With this table, the experienced user can immediately begin to program the PDP-11/40 System.

Basically, the PDP-11/40 offers increased flexibility and speed. The basic system (without options) has five more programming instructions than the PDP-11/20. These instructions are: eXclusive OR (XOR), Subtract One and Branch (SOB), ReTurn from inTerrupt (RTT), Sign eXTend (SXT), and MARK (MARK). System flexibility is increased even more if the KT11-D Memory Management Option and the KE11 Extended Instruction Set (EIS) and Floating Instruction Set (FIS) Options are installed.

Table 3-9
PDP-11 Programming Comparison

PDP-11/20	PDP-11/40
JMP/JSR (R)+ uses (REG)+2 as address	JMP/JSR (R)+ uses (REG) before autoincrement as address. All autoincrements are now post autoincrements.
All REG 6 (SP) autodecrement references can cause overflow. Address modes 4 and 5, JSR and traps are tested.	Address modes 1, 2, 4, and 6, JSR and traps are tested except that nonaltering (DATIs) references to stack data are always allowed.
No red zone on stack overflow.	Red zone trap occurs if stack is 16 words below boundary. This trap saves PC+2 and PS on new stack at locations 2 and 0.
SWAB instruction does not affect V.	SWAB instruction clears V.
Program HALT displays PC of HALT instruction in ADDRESS display.	Program HALT displays PC+2 of HALT instruction in ADDRESS display.
Byte operations to the odd byte of the PS cause odd address traps.	Byte operations to the odd byte of the PS do not trap. Not all bits may exist.
No RTT instruction.	If RTT sets the T bit, the T bit trap occurs after the instruction following RTT.
If RTI sets T bit, T bit trap acknowledged after instruction following RTI.	If RTI sets T bit, T bit trap acknowledged immediately following RTI.
Explicit reference to PS can load T bit. Console can load T bit, initialize can clear it.	Only implicit references (RTI, RTT, traps, and interrupts) can load T bit. Console *cannot* load T bit but initialize can clear it.
The BUS INIT of the RESET instruction occurs when the processor has control of the bus. No bus cycles are interrupted.	The BUS INIT of the RESET instruction occurs asynchronously with other Unibus operations.
CAUTION **Because PDP-11/20 and PDP-11/40 RESET instruction timing precludes the POWER FAIL routine, use of the RESET instruction should be severely limited.**	
Odd address or nonexistent references using the SP cause a HALT. This is a case of double bus error with a second error occurring in the trap service of the first error.	Odd address or nonexistent references using the SP cause a fatal trap. On bus error in trap service, a new stack is created at locations 0 and 2.

Table 3-9 (Cont)
PDP-11 Programming Comparison

PDP-11/20	PDP-11/40
Stack limit boundary fixed at octal 400 with violations serviced by an OVFL trap.	Optional variable stack limit boundary (KJ11-A option). Use of red and yellow zones on either basic (octal 400) or optionally variable boundary.
First instruction in an interrupt service routine is guaranteed to be executed.	The first instruction in an interrupt routine is not executed if another interrupt occurs at a higher priority level than was assumed by the first interrupt.
Power up vector at 24 when power returns.	Power up vector is initially at 24; can alter jumpers to other addresses.
A trap instruction to vector location 14 exists for the IR code 3. No name is given this instruction.	The formerly unnamed instruction for IR code 3 is now called BPT.
Condition codes for a MOV instruction are not altered for present data if a bus error occurs on the last destination address. The error trap occurs on the DATIP of the DATIP, DATO sequence of that address.	Condition codes for a MOV instruction are altered for present data if a bus error occurs on the last destination address. The error trap occurs on the singular DATO sequence to that address.
NOTE **The following is the priority sequence of service for internal processor traps, external interrupts, and HALT and WAIT.**	
BUS ERROR TRAP – odd address, data time out.	BUS ERROR TRAP – odd address, fatal stack overflow (red); if KT11-D option is used, memory management violations; parity error trap response.
HALT instruction for console operation.	Same. (Refer to KT11-D, if installed, for other changes.)
TRAP instructions – illegal or reserved instructions, TRT, IOT, EMT, TRAP.	TRAP instructions – illegal or reserved instructions, BPT, IOT, EMT, TRAP.
TRACE TRAP – T bit of processor status.	Same
OVFL trap – stack overflow.	OVFL – warning (yellow) stack overflow.
PWR FAIL trap – power down.	Same

Table 3-9 (Cont)
PDP-11 Programming Comparison

PDP–11/20	PDP-11/40
CONSOLE BUS REQUEST – console operation after HALT switch.	Same
UNIBUS BUS REQUEST – peripheral request, compared with processor priority, usually an interrupt occurs.	Same
WAIT LOOP – loop on a WAIT instruction in the IR until an interrupt allows exit. A CONSOLE BUS REQUEST returns to this loop after being honored.	Same

CHAPTER 4
PROCESSOR INSTRUCTIONS AND OPTIONS

4.1 SCOPE

This chapter presents a brief introduction of the PDP-11 instruction set and the processor options available for the PDP-11/40 System.

Paragraph 4.2 discusses the basic PDP-11 instruction set and also covers the additional instructions that are available if certain processor options (KE11-E, KE11-F, and KT11-D) are installed in the basic system.

Paragraph 4.3 describes each of the options that can be mounted in the basic KD11-A Processor and references appropriate documents containing detailed information on the specific option. These options are: KE11-E, KE11-F, KJ11-A, KT11-D, KW11-L, KM11-A, and a Small Peripheral Controller. Specifications are contained in Tables 4-12 through 4-16.

4.2 INSTRUCTION SET

This section summarizes the PDP-11/40 address modes and instruction set. Its purpose is to define the operation of the KD11-A Processor and provide quick-reference tabular information. A complete description of PDP-11/40 address modes and instructions, with additional details and examples, is provided in the *PDP-11/40 Processor Handbook.*

The Instruction Set Processor (ISP) notation is used to define the processor operations for each address mode and instruction. Table 4-1 defines the modified ISP symbology used in this chapter. A more detailed description of ISP notation is provided in Appendix A of the *PDP-11/40 Processor Handbook*. Modified ISP notation is used in the *KD11-A Processor Manual* in the block diagram and flow diagram description of instruction implementation. The modifications are as follows:

( )	is used for ⟨ ⟩ or [ ]
•	or ( ) around an expression indicates logical AND
+	indicates logical OR
-	indicates logical negation
plus	indicates addition
minus	indicates subtraction

The following paragraphs cover address modes (Paragraph 4.2.1), the basic instruction set (Paragraph 4.2.2), and the extended instruction set (Paragraph 4.2.3).

Table 4-1
ISP Symbology

Symbol	Definition
⟨ ⟩	Defines the limits of an expression, such as word length ⟨15:0⟩.
[ ]	Defines the limits of a memory declaration; Mw [SP] specifies the address of the stack pointer in memory.
←	The expression to the left of this symbol is replaced by the expression to the right of this symbol, Z ← 1 indicates the Z bit is set, PC ← PC + 2 indicates the program counter register (PC) is incremented by 2.
cat	Indicates concatenation; registers to the left and right of this expression are considered to be one register.
equiv	Designates that expressions to the left and right are equivalent.
&	Logical AND
OR	Logical inclusive-OR
~	Negate
XOR	Logical exclusive-OR
'	Indicates that a reference to the expression with which this symbol is used may cause side effects, e.g., registers may be changed as a result of the operation.
;	Used as a delimiter
;next	A sequential delimiter, the operation to the left must occur before the operation to the right.
m	Designates an address mode; address mode 1 is indicated by m = 1.
rg	General register 7 (program counter)
ai	Auto-increment; by 2 for word instructions, and by 1 for byte instructions.
r	Indicates a result; used many times with limit symbols as an intermediate register (r ⟨15:0⟩).
+	Addition; expression to the left is added to expression to the right.
-	Subtraction; expression to the right is subtracted from expression to the left.
X	Multiply; expression to the left is multiplied by expression to the right.
/	Divide; expression to the left is divided by the expression to the right.
sign-extend	The sign bit of a byte, bit 7, is extended through bits 8 to 15.
Mw	Memory word declaration; the address in brackets points to the memory location.
nw'	Indicates next word, as pointed to by the PC with side effects ('). The word is at the next sequential PC address, or the word pointed to by the next word (deferred addressing).
R [dr]	Indicates that a register (R) address as a memory declaration is that of a device register.
D	Destination
Db	Byte destination
S	Source
Sb	Byte source

4.2.1 Address Modes

The instruction set of the PDP-11/40 System flexibly interacts with the general-purpose registers through the address modes. Table 4-2 lists all of the address modes, including the Program Counter (PC) register address modes. These address modes, along with the general-purpose register designation, determine the instructions' operands (source and/or destination) and form part of the 16-bit instruction format (Figure 4-1).

Table 4-2
Address Modes

Mode	Designation	Symbolic	ISP	Description
			General Purpose Register Addressing	
0	register	R	if (m=0) then Rr ⟨w1:0⟩;	The register (R, Rr) is the operand.
1	register deferred	@R or (R)	if (m=1) then M[Rr];	Defer to operand through register (R, Rr) as address.
2	auto-increment	(R)+	if (m=2) and (rg≠7) then (M[Rr]; next Rr ← Rr + ai);	Defer to operand through register (R, Rr) as address, then increment.
3	auto-increment deferred	@(R)+	if (m=3) and (rg≠7) then (M[Mw[Rr]]; next Rr ← Rr + 2;	Defer to operand through (R), Mw [Rr] as address, then increment register (R, Rr).
4	auto-decrement	-(R)	if (m=4) then (Rr ← Rr - ai); next M[Rr];	Decrement register (R, Rr), then defer to operand through register (R, Rr) as address.
5	auto-decrement deferred	@-(R)	if (m=5) then (Rr ← Rr - ai; next M[Mw[Rr]]);	Defer to operand through (R), Mw Rr after decrement of register (R, Rr).
6	indexed	±X(R)	if (m=6) and (rg≠7) then M[nw' + Rr];	Index via register = (R, Rr) by the amount specified in next PC word (X).
7	indexed deferred	@±X(R) or @(R)	if (m=7) and (rg≠7) then M[Mw[nw' + Rr]];	Defer to operand through index of register (R, Rr) specified in next PC word (X) as address.
			PC Register Addressing	
2	immediate	#n	if (m=2) and (rg=7) then nw' ⟨w1:0⟩	Defer to operand through PC value (next word); next word is immediate operand.
3	absolute	@#A	if (m=3) and (rg=7) then M[nw']	Defer via next word (PC address) as address to operand; absolute addressing.
6	relative	A	if (m=6) and (rg=7) then M[nw' + PC];	Relative to PC; uses next word as deferred address of operand.
7	relative deferred	@A	if (m=7) and (rg=7) then M[Mw[nw' + PC]];	Defer relative to PC; uses next word as address of deferred address of the operand.

NOTE: The following symbols are used in this table:

R = Register
X, n, A = next program counter (PC) word (constant)

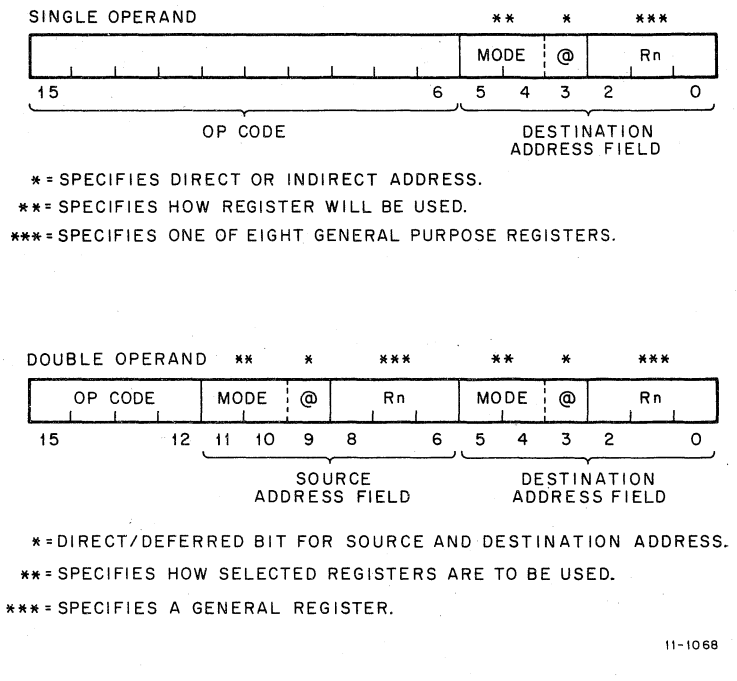


Figure 4-1 Double and Single Operand Addressing

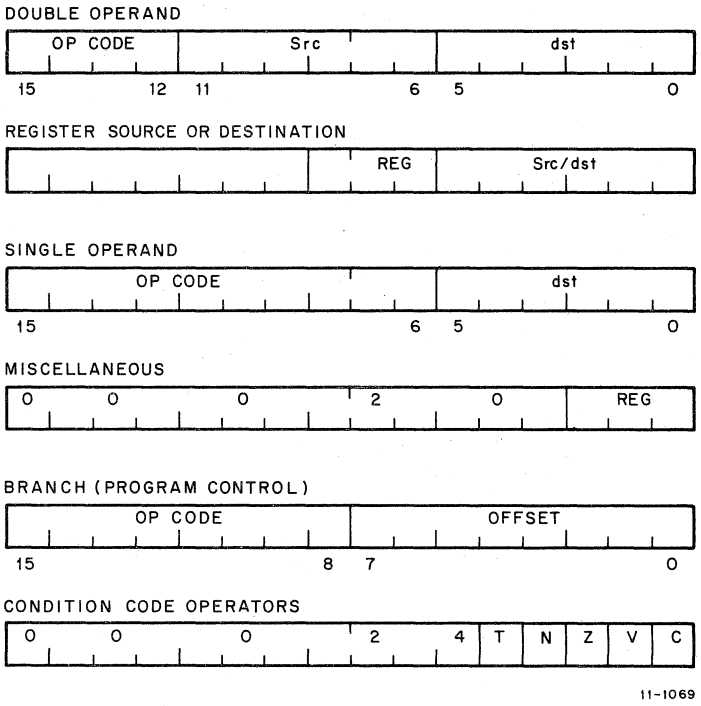


Figure 4-2 Instruction Formats

4.2.2 Basic Instruction Set

The KD11-A basic instruction set is divided into six groups of instructions. The format of each group is shown in Figure 4-2. The six groups of instructions are:

a. Double Operand – Operations which imply two operands (such as ADD, SUBtract, MOVe, and CoMPare) are handled by instructions that specify two addresses. The first operand is called the source operand; the second is called the destination operand. Bit assignments in the source and destination address fields may specify different address modes and different registers.

   Double-operand instructions are listed in Table 4-3.

b. Single Operand – Operations which require only one operand (such as CLeaR, INCrement, TeST) are handled by instructions that specify only a destination address (operand). The operation code, address mode, and destination address are specified by the instruction.

   Single-operand instructions are listed in Table 4-4.

c. Register Source or Destination – Instructions in this group make use of the general processor registers as simple accumulators and the resultant is stored in the selected register. Information can be used as either a source or destination operand. For example, the eXclusive OR of the selected register and the destination operand can be stored in the destination address.

   Register source or destination instructions are listed in Table 4-5.

d. Branch (Program Control) – These instructions permit control of the program by branching to new locations in the program dependent on conditions tested by the program. The instructions cause the program to branch to a location specified by the sum of an offset value (multiplied by 2) and the current contents of the Program Counter (PC), provided the branch is either unconditional or is conditional and the conditions are met after testing the Processor Status (PS) word.

   Branch instructions are listed in Table 4-6.

e. Miscellaneous – These instructions include HALT, WAIT, and RESET as well as interrupt and trap handling instructions such as RTI, RTT, EMT, and TRAP.

   Miscellaneous instructions are listed in Table 4-7.

f. Condition Code Operators – These instructions are used to set or clear individual condition codes in the Processor Status (PS) word. Selected combinations of these bits may be set or cleared together.

   Condition code operators are listed in Table 4-8.

Table 4-3
Double Operand Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
MOV Move (Src to Dst) 01SSDD	r ← S'; next N ← r ⟨15⟩ if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0), V ← 0; D' ← r	Move source to intermediate register, r. Set N if negative. Set Z if 0. Clear V. Transmit result to destination.
MOVB Move Byte (Src to Dst) 11SSDD	r ← Sb'; next N ← r ⟨7⟩; if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; Db' ← r	Move source to intermediate register, r. Set N if negative. Set Z if 0. Clear V. Transmit result to destination.

CMP
Compare
(Src to Dst)
02SSDD
	r ⟨16:0⟩ ← S' - D'; next
	
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (S ⟨15⟩ = ~ D ⟨15⟩) & (S ⟨15⟩ XOR r ⟨15⟩) then
	(V ← 1 else V ← 0);
	C ← r ⟨16⟩
		Source and destination operands are compared, but unaffected.
		Only condition codes are affected, as follows:
		Set N if r is negative.
		Set Z if r is 0.
		Set V if operands have opposite signs and the sign of the source
		is the same as the result, r.
		Clear C if 17th bit is carry.

CMPB
Compare Byte
12SSDD
	r ⟨8:0⟩ ← Sb' - Db'; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (Sb ⟨7⟩ = ~ Db ⟨7⟩ & (Sb ⟨7⟩ XOR r ⟨7⟩) then
	(V ← 1 else V ← 0);
	C ← r ⟨8⟩
		Same as CMP, except operands are bytes.

BIT Bit Test 03SSDD	r ← D' & S'; next N ← r ⟨15⟩; if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0	Logical AND of source and destination operands. Set N if negative. Set Z if 0. No overflow.
BITB Bit Test, Byte 13SSDD	r ← Db' & Sb'; next N ← r ⟨7⟩; if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0	Same as BIT, except byte
BIC Bit Clear 04SSDD	r ← D' & ~ S'; next N ← r ⟨15⟩; if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; D ← r	AND destination operand with complemented source operand. Set N if negative. Set Z if 0. Clear V and put result in destination address.
BICB Bit Clear, Byte 14SSDD	r ← Db' & ~ Sb'; next N ← r ⟨7⟩; if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); V ←0; Db ← r	Same as BIC, except byte.

Table 4-3 (Cont)
Double Operand Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
BIS Bit Set 05SSDD	r ← D' OR S'; next N ← r ⟨15⟩; if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; D ← r	Inclusive OR of source operand and destination operand. Set N if negative. Set Z if 0. Clear V. Put result in destination.
BISB Bit Set, Byte 15SSDD	r ← Db' OR Sb'; next N ← r ⟨7⟩; if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; Db ← r	Same as BIS, except byte.

ADD
Add
06SSDD
	r ⟨16:0⟩ ← S' + D'; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (S ⟨15⟩ equiv D ⟨15⟩) & (S ⟨15⟩ XOR r ⟨15⟩) then (V ← 1 else V ← 0);
	C ← r ⟨16⟩;
	D ← r ⟨15:0⟩
		Add source and destination to provide 17-bit sum.
		Set N if negative result.
		Set Z if 0.
		Set V if both operands were same sign and the result is of opposite sign.
		Set C if carry.
		Put result in destination.

SUB
Subtract
16SSDD
	r ⟨16:0⟩ ← D' - S'; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (D ⟨15⟩ XOR S ⟨15⟩) & (D ⟨15⟩ XOR r ⟨15⟩) then (V ← 1 else V ← 0);
	C ← r ⟨16⟩;
	D ← r ⟨15:0⟩
		Subtract source operand from destination operand.
		Set N if negative results.
		Set Z if 0.
		Set V if operands had different signs and result is opposite sign from destination.
		Clear C if a carry.
		Put result in destination.

Table 4-4
Single Operand Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
CLR Clear dst 0050DD	D' ← 0; N ← 0; Z ← 1; V ← 0; C ← 0	Clear destination, N, V, and C; set Z.
CLRB Clear Byte dst 1050DD	Db' ← 0; N ← 0; Z ← 1; V ← 0; C ← 0	Clear destination byte.
COM Complement dst 0051DD	r ← ~ D'; next N ← r ⟨15⟩; if (r ⟨15:0⟩ = 0) then Z ← 1 else Z ← 0); V ← 0; C ← 1; D ← r	Complement destination. Set N if negative. Set Z if 0. Clear V. Set C. Put result in destination.
COMB Complement Byte dst 1051DD	r ← ~ Db'; next N ← r ⟨7⟩; if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; C ← 1; Db ← r	Same as COM, except byte.

INC
Increment dst
0052DD
	r ← D' + 1; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨15:0⟩ = 100000_8) then (V ← 1 else V ← 0);
	D ← r
		Result is sum of D plus 1.
		Set N if negative.
		Set Z if 0.
		Set V if result equals 100000_8 (dst was 077777_8).
		Put result in destination.

INCB
Increment
Byte dst
1052DD
	r ← Db' + 1; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨7:0⟩ = 200_8) then (V ← 1 else V ← 0);
	Db ← r
		Same as INC, except byte.
		
		Set V if result equals 200_8 (dst byte was 177_8).

DEC
Decrement
dst
0053DD
	r ← D' − 1; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨15:0⟩ = 77777_8) then (V ← 1 else V ← 0);
	D ← r
		Result is destination operand minus 1.
		Set N if negative.
		Set Z if 0.
		Set V if result equals 77777_8 (dst was 100000_8).
		Put result in destination.

DECB
Decrement
Byte dst
1053DD
	r ← Db' − 1; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨7:0⟩ = 177_8) then (V ← 1 else V ← 0);
	Db ← r
		Same as DEC, except byte.
		
		Set V if result is 177_8 (dst byte was 000_8).

Table 4-4 (Cont)
Single Operand Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description

NEG
Negate dst
0054DD
	r ← -D'; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨15:0⟩ = 100000_8) then (V ← 1 else V ← 0);
	if (r ⟨15:0⟩ = 0) then (C ← 0 else C ← 1);
	D ← r
		Negate D by 2's complement.
		Set N if negative result.
		Set Z if 0.
		Set V if result is 100000_8.
		Clear C if result is 0, otherwise set C.
		Put result in destination.

NEGB
Negate Byte
1054DD
	r ← -Db'; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨7:0⟩ = 200_8) then (V ← 1 else V ← 0);
	if (r ⟨7:0⟩ = 0) then (C ← 0 else C ← 1);
	Db ← r
		Same as NEG, except byte.

ADC
Add Carry
0055DD
	r ← D' + C; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨15:0⟩ = 100000_8) & (C = 1) then (V ← 1 else V ← 0); next
	if (r ⟨15:0⟩ = 0) & (C = 1) then (C ← 1 else C ← 0);
	D ← r
		Add the C bit to the destination.
		Set N if negative.
		Set Z if 0.
		Set V if destination was 077777_8 and C was 1.
		Set C if destination was 177777_8 and C was 1.

ADCB
Add Carry Byte
1055DD
	r ← Db' + C; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨7:0⟩ = 200_8) & (C = 1) then (V ← 1 else V ← 0); next
	if (r ⟨7:0⟩ = 0) & (C = 1) then (C ← 1 else C ← 0);
	Db ← r
		Same as ADC, except byte.

SBC
Subtract Carry
0056DD
	r ← D' - C; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨15:0⟩ = 100000_8) then (V ← 1 else V ← 0);
	if (r ⟨15:0⟩ = 0) & (C = 1) then (C ← 0 else C ← 1);
	D ← r
		Subtract C bit from contents of destination.
		Set N if negative.
		Set Z if 0.
		Set V if result is 100000_8.
		Clear C if result is 0 and C = 1.
		Put result in destination.

SBCB
Subtract Carry Byte
1056DD
	r ← Db' - C; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	if (r ⟨7:0⟩ = 200_8) then (V ← 1 else V ← 0);
	if (r ⟨7:0⟩ = 0) & (C = 1) then (C ← 0 else C ← 1);
	Db ← r
		Same as SBC, except byte.

Table 4-4 (Cont)
Single Operand Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
TST Test 0057DD	r ← D' −0; next N ← r ⟨15⟩; if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; C ← 0	Sets N and Z condition codes according to contents of destination address.
TSTB Test Byte 1057DD	r ← Db' −0; next N ← r ⟨7⟩; if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); V ← 0; C ← 0	Same as TST, except byte.

ROR
Rotate Right
0060DD
	r ⟨16:0⟩ ← D' ⟨0⟩ cat C cat D' ⟨15:1⟩; next
	
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	C cat D ⟨15:0⟩ ← r ⟨16:0⟩; next
	if (N XOR C) then (V ← 1 else V ← 0)
		17-bit intermediate result is C and contents of destination rotated right one place.
		Set N if high order bit is set.
		Set Z if result is 0.
		Put 17-bit result into C bit and destination.
		Load V with exclusive-OR of N and C (after rotation is complete).

RORB
Rotate Right
Byte
1060DD
	r ⟨8:0⟩ ← Db' ⟨0⟩ cat C cat Db' ⟨7:1⟩; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	C cat Db ← r ⟨8:0⟩; next
	if (N XOR C) then (V ← 1 else V ← 0)
		Same as ROR, except byte.

ROL
Rotate Left
0061DD
	r ⟨16:0⟩ ← D' ⟨15:0⟩ cat C; next
	
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	C cat D ← r ⟨16:0⟩; next
	
	if (N XOR C) then (V ← 1 else V ← 0)
		17-bit result is C and contents of destination rotated left one bit.
		Set N if result is negative.
		Set Z if result is 0.
		Put result into C and D. Bit 15 into C bit and previous C bit into bit 0.
		Load V with exclusive-OR of N and C after rotation is complete.

ROLB
Rotate Left
Byte
1061DD
	r ⟨8:0⟩ ← Db' ⟨7:0⟩ cat C; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0);
	C cat Db ← r ⟨8:0⟩; next
	if (N XOR C) then (V ← 1 else V ← 0)
		Same as ROL, except byte.

ASR
Arithmetic
Shift Right
0062DD
	r ← D'/2; next
	C ← D ⟨0⟩;
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0 then (Z ← 1 else Z ← 0); next
	if (N XOR C) then (V ← 1 else V ← 0);
	D ← r
		Contents of destination shifted right one place (÷ 2).
		Least-significant bit loaded into C.
		Set N if result negative.
		Set Z if result 0.
		Load V with exclusive-OR of N and C after shift is complete.
		Put result into destination.

Table 4-4 (Cont)
Single Operand Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description

ASRB
Arithmetic
Shift Right
Byte
1062DD
	r ← Db'/2; next
	C ← Db ⟨0⟩;
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); next
	if (N XOR C) then (V ← 1 else V ← 0);
	Db ← r
		Same as ASR except byte.

ASL
Arithmetic
Shift Left
0063DD
	r ← D' ⟨15⟩ cat D' ⟨13:0⟩ cat 0; next
	
	C ← D ⟨14⟩; next
	N ← r ⟨15⟩;
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0); next
	if (N XOR C) then (V ← 1 else V ← 0);
	D ← r
		Shifts contents of destination left one place, but sign bit remains in most significant place.
		Bit 14 loaded into C.
		Set N if result negative.
		Set Z if result 0.
		Load V with exclusive-OR of N and C after shift completed.
		Put result in destination.

ASLB
Arithmetic
Shift Left
Byte
1063DD
	r ← Db' ⟨7⟩ cat Db' ⟨5:0⟩ cat 0; next
	C ← Db ⟨6⟩; next
	N ← r ⟨7⟩;
	if (r ⟨7:0⟩ = 0) then (Z ← 1 else Z ← 0); next
	if (N XOR C) then (V ← 1 else V ← 0);
	Db ← r
		Same as ASL, except byte.

MARK Mark 0064nn	SP ← SP + (2 × df ⟨5:0⟩; next PC ← R[5] ; next R[5] ← Mw [SP] ; SP ← SP + 2	Adjusts stack pointer by the number of words indicated in the low 6 bits of the instruction (2 × nn locations). Puts old PC (R5) into PC. Contents of old R5 popped into R5.

SXT
Sign Extend
destination
0067DD
	if (N = 1) then (r ⟨15:0⟩ ← -1 else r ⟨15:0⟩ ← 0); next
	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);
	D' ← r
		If the N bit is set, then -1 is placed in the destination operand.
		Otherwise, 0 is placed in the destination operand.
		Set Z if result is 0.

JMP Jump 0001DD	PC ← D address	D address is computed in a fashion similar to D.
SWAB Swab Bytes Destination 0003DD	r ← D' ⟨7:0⟩ □ D' ⟨15:8⟩; next N ← r ⟨7⟩; (r ⟨7:0⟩ = 0) → (Z ← 1 else Z = 0); V ← 0; C ← 0; D ← r	Result is byte swapped of D negative? Zero? Clear V, C Transmit result to D.

Table 4-5
Register Source or Destination Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
XOR Exclusive-OR 074RDD	r ← R[sr] XOR D'; next if (r = 0) then (Z ← 1 else Z ← 0); N ← r ⟨15⟩; V ← 0; R[sr] ← r	The exclusive-OR of the register and the destination operand is stored in the destination address. Set Z if result is 0. Set N if result is negative. Clear V; no overflow possible.
SOB Subtract One and Branch 077R offset	r ← R[sr] −1; next R[sr] ← r; if (r ≠ 0) then (PC ← PC − 2 × df ⟨5:0⟩)	Decrement register by 1. If result is not equal to 0, branch. Subtract 2 × 6-bit offset from PC to get new PC.

Table 4-6
Branch Instructons

Mnemonic Instruction and Op Code	ISP Notation	Description
BR Branch Unconditional 0004 loc	PC ← PC + sign-extend (instr ⟨7:0⟩ X 2)	Always branch. PC changed as follows: Eight least-significant bits of instruction are multiplied times 2 and added to PC with sign extended.
BNE Branch Not Equal 0010 loc	if (Z = 0) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if Z is 0.
BEQ Branch on Equal 0014 loc	if (Z = 1) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if Z is 1.
BGE Branch if Greater than or Equal (zero) 0020 loc	if (N equiv V) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if N is equivalent to V.
BLT Branch on Less Than 0024 loc	if (N XOR V) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if exclusive-OR of N and V equal 1.
BGT Branch on Greater Than 0030 loc	if (~Z & (N equiv V)) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if Z equals 0 and N equals V.
BLE Branch on Less Than or Equal (zero) 0034 loc	if (Z OR (N XOR V)) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if Z equals 1 or if exclusive-OR of N and V equals 1.
BPL Branch on Plus 1000 loc	if (N = 0) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if N is 0.
BMI Branch on Minus 1004 loc	if (N = 1) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if N is 1.
BHI Branch on Higher 1010 loc	if ~(C OR Z) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if C and Z are 0.

Table 4-6 (Cont)
Branch Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
BLOS Branch on Lower or Same 1014 loc	if (C OR Z) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if C or Z is 1.
BVC Branch on Overflow Clear	if (V = 0) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if V is 0.
BVS Branch on Overflow Set 1024 loc	if (V = 1) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if V is 1.
BHIS Branch on Higher or Same 1030 loc	if (C = 0) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if C is 0.
BLO Branch on Lower 1034 loc	if (C = 1) then (PC ← PC + sign-extend (instr ⟨7:0⟩ X 2))	Branch if C is 1.
JSR Jump to Subroutine 004RDD	SP ← SP - 2; next Mw [SP] ← R[sr]; R[sr] ← PC PC ← D address	Push contents of R onto stack. Store current PC in R. Load subroutine address into PC.
RTS Return from Subroutine 00020R	PC ← R[dr]; R[dr] ← Mw [SP]; SP ← SP + 2	Load contents of R into PC. Pop stack pointer into R.

Table 4-7
Miscellaneous Instructions

Mnemonic Instruction and Op Code	ISP Notation	Description
HALT Halt 000000	Off ← true	Processor halts with console in control. No activities or instructions can be executed until a console actions restarts the processor.
WAIT Wait 000001	Wait ← true	Processor relinquishes bus and waits for an external interrupt.
IOT I/O Trap 000004	SP ← SP - 2; next Mw [SP] ← PS; SP ← SP - 2; next Mw [SP] ← PC; PC ← Mw [20]; PS ← Mw [22]	Push PS onto Stack. Push PC onto stack. Get new PC from location 20. Get new PS from location 22.
RESET Reset External Bus 000005	Init ← 1; Delay (20 milliseconds); next Init ← 0	Send INIT on Unibus for 20 ms.
BPT Break Point Trap 000003	SP ← SP - 2; next MW [SP] ← PS; SP ← SP - 2; next MW [SP] ← PC; PC ← MW [14_8]; PS ← MW [16_8]	Place PS and PC on stack take new PC and PS from M [14], M [16]
RTI Return from Interrupt 000002	PC ← Mw [SP]; SP ← SP + 2; next PS ← Mw [SP]; SP ← SP + 2	Pop PC off stack. Pop PS off stack. (RTI permits trace trap.)
RTT Return from Interrupt 000006	PC ← Mw [SP]; SP ← SP + 2; next PS ← Mw [SP]; SP ← SP + 2	Pop PC off stack. Pop PS off stack. (RTT inhibits trace trap.)
EMT Emulator Trap 104 Code (104000 – 104377)	SP ← SP - 2; next Mw [SP] ← PS; SP ← SP - 2; next Mw [SP] ← PC; PC ← Mw [30]; PS ← Mw [32]	Push PS onto stack. Push PC onto stack. Get new PC and PS from locations 30 and 32.
TRAP Trap 104 Code (104400 – 104777)	SP ← SP - 2; next Mw [SP] ← PS SP ← SP - 2; next Mw [SP] ← PC; PC ← Mw [34]; PS ← Mw [36]	Push PS onto stack. Push PC onto stack. Get new PC and PS from locations 34 and 36.

Table 4-8
Condition Code Operators

Mnemonic Instruction and Op Code	ISP Notation	Description
CLC Clear C 000241	if (instr ⟨4⟩ = 0 & instr ⟨0⟩ = 1) then C ← 0	When bit 4 of the instruction is 0 bits 3, 2, 1, and 0 clear corresponding bits in PS.
CLV Clear V 000242	if (instr ⟨4⟩ = 0 & instr ⟨1⟩ = 1) then V ← 0	
CLZ Clear Z 000244	if (instr ⟨4⟩ = 0 & instr ⟨2⟩ = 1) then Z ← 0	
CLN Clear N 000250	if (instr ⟨4⟩ = 0 & instr ⟨3⟩ = 1) then N ← 0	
CCC Clear all Condition Codes 000257	if (instr ⟨4⟩ = 0 & instr ⟨3:0⟩ = 17) then (C ← 0; V ← 0; Z ← 0; N ← 0)	
SEC Set C 000261	if (instr ⟨4⟩ = 1 & instr ⟨0⟩ = 1) then C ← 1	When bit 4 of the instruction is 1, bits 3, 2, 1, and 0 set corresponding bits in PS.
SEV Set V 000262	if (instr ⟨4⟩ = 1 & instr ⟨1⟩ = 1) then V ← 1	
SEZ Set Z 000264	if (instr ⟨4⟩ = 1 & instr ⟨2⟩ = 1) then Z ← 1	
SEN Set N 000270	if (instr ⟨4⟩ = 1 & instr ⟨3⟩ = 1) then N ← 1	
SCC Set all Condition Codes 000277	if (instr ⟨4:0⟩ = 37) then (C ← 1; V ← 1; Z ← 1; N ← 1)	

4.2.3 Extended Instruction Set

Additional instructions are available if certain processor options are added to the basic system. These instructions are:

a. KE11-E Extended Instruction Set (EIS) – These instructions have the same format as double-operand instructions and provide an increased arithmetic capability to the basic instruction set. These instructions are: MULtiply (MUL), DIVide (DIV), Arithmetic SHift (ASH), and Arithmetic SHift Combined (ASHC).

   The EIS instructions are listed in Table 4-9.

b. KE11-F Floating Instruction Set (FIS) – These instructions permit arithmetic operations in floating-point notation. The instructions are: FADD, FSUB, FMUL, and FDIV (Floating point ADDition, SUBtraction, MULtiplication, and DIVision).

   The FIS instructions are listed in Table 4-10.

c. KT11-D Memory Management – This option provides expanded address capability for the PDP-11/40. It allows the PDP-11/40 to treat sections of memory differently (user mode and kernel mode). Two instructions are also provided: Move From Previous Instruction (MFPI) and Move To Previous Instruction (MTPI). The MFPI instruction is provided to allow interaddress space communication when the PDP-11/40 is using the memory management option. The MTPI instruction determines the address of the destination operand in the current address space.

   Note that in the table, the move from previous instruction (MFPI) and the move to previous instruction (MTPI) are listed as MFPI/D and MTPI/D. This is because in the PDP-11/40, MFPI and MFPD instructions are executed identically and the same applies to the MTPI and MTPD instructions.

   The KT11-D instructions are listed in Table 4-11.

Table 4-9
Extended Instruction Set (EIS)

Mnemonic Instruction and Op Code	ISP Notation	Description
MUL Multiply 070RSS	r ⟨31:0⟩ ← D' × R[sr] ; next	Multiply contents of source register and destination to form 32-bit product.
	if (r ⟨31:0⟩ = 0) then (Z ← 1 else Z ← 0);	Set Z if product is 0.
	N ← r ⟨31⟩;	Set N if product is negative.
	if (r ⟨31:0⟩ $< -2^{15}$) OR (r ⟨31:0⟩ $\geq 2^{15}$) then (C ← 1 else C ← 0);	Set C if product is more than 16-bit result.
	V ← 0;	No overflow possible; clear V.
	R[sr] ⟨15:0⟩ ← r ⟨31:16⟩; next	Store the high-order result in R.
	R[sr OR 1] ⟨15:0⟩ ← r ⟨15:0⟩;	Store the low-order result in succeeding register if R is even number. Otherwise, store in R.
DIV Divide 071RSS	r1 ⟨31:0⟩ ← R[sr] cat R[sr OR 1] /D'; next	The 32-bit dividend, R, R OR 1, is divided by source operand D. R must be even number.
	r2 ⟨15:0⟩ ← R[sr] cat R[sr OR 1] -(r1 × D);	Determine the remainder.
	next N ← r1 ⟨15⟩;	Set N if quotient is negative.
	if (r1 ⟨31:0⟩ = 0) then (Z ← 1 else Z ← 0);	Set Z if quotient is 0.
	if (D = 0) then (C ← 1 else C ← 0);	Set C if divide by 0 attempted.

	if (r1 ⟨15⟩ = 0) & (r1 ⟨31:16⟩ ≠ 0)
	OR
	if (r1 ⟨15⟩ = 1) & (r1 ⟨31:16⟩ ≠ -1)
	OR
		Set V if divisor is 0, or if the result is too large to be stored as a 16-bit number.

	if (D = 0) then (V ← 1 else V ← 0);	
	R[sr] ← r1 ⟨15:0⟩	Store quotient in R.
	R[sr OR 1] ← r2	Store remainder in R OR 1.
ASH Arithmetic Shift 072RDD	r ⟨79:0⟩ ← sign-extend (R[sr] ⟨15:0⟩ × 2 ↑ (D' ⟨5:0⟩ + 32) mod 64); next	Contents of R are shifted NN places right or left, where NN equals the six low-order bits of DD. NN = -32 to +31.
	R[sr] ⟨15:0⟩ ← r ⟨47:32⟩; next	Store result in R.
	if (R[sr] = 0) then (Z ← 1 else Z ← 0);	Set Z if result is 0.
	if ((R[sr] ⟨15⟩ = 0) & (r ⟨79:48⟩≠ 0) OR (R[sr] ⟨15⟩ = 1) & (r ⟨79:48⟩ ≠ -1)) then (V ← 1 else V ← 0);	Set V if sign of register changed during shift.
	N ← R[sr] ⟨15⟩;	Set N if result is negative.
	if (D ⟨5⟩ = 1) then C ← r ⟨31⟩;	Load C from last bit shifted out of register.
	if (D ⟨5⟩ = 0) & (D ⟨5:0⟩ ≠ 0) then C ← r ⟨48⟩;	
	if (D ⟨5:0⟩ = 0) then C ← 0	

Table 4-9 (Cont)
Extended Instruction Set (EIS)

Mnemonic Instruction and Op Code	ISP Notation	Description

ASHC
Arithmetic
Shift
Combined
073RDD
	r ⟨95:0⟩ ← sign-extend (R[sr] cat R[sr OR 1] × 2 ↑ (D' ⟨5:0⟩ + 32) mod 64); next
	
	R[sr] ← r ⟨63:48⟩; next
	R[sr OR 1] ← r ⟨47:32⟩; next
	if (R[sr] cat R[sr OR 1] = 0) then (Z ← 1 else Z ← 0);
	N ← R[sr] ⟨15⟩;
	if (r ⟨63⟩ = 0) & (r ⟨95:64⟩ ≠ 0) OR
	if (r ⟨63⟩ ≠ 0) & (r ⟨95:64⟩ ≠ −1) then (V ← 1 else V ← 0);
	if (D ⟨5⟩ = 1) then C ← r ⟨31⟩;
	if (D ⟨5⟩ = 0) & (D ⟨5:0⟩ ≠ 0) then C ← r ⟨64⟩;
	if (D ⟨5:0⟩ = 0) then C ← 0
		Contents of R, and R ORed with 1, form a 32-bit word (R = 31:16, ROR 1 = 15:0) that is shifted right or left NN places, specified by six low-order bits of destination operand, DD. Store results in R and R OR 1.
		
		Set Z if result is 0.
		
		Set N if result is negative.
		Set V if sign bit changes during the shift.
		
		Load C with high order if left shift.
		Load C with low order if right shift.
		
		Otherwise, clear C.

XOR Exclusive-OR 074RDD	r ← R[sr] XOR D'; next if (r = 0) then (Z ← 1 else Z ← 0); N ← r ⟨15⟩; V ← 0; R[sr] ← r	The exclusive-OR of the register and the destination operand is stored in the destination address. Set Z if result is 0. Set N if result is negative. Clear V; no overflow possible.
SOB Subtract One and Branch 077R offset	r ← R[sr] −1; next R[sr] ← r; if (r ≠ 0) then (PC ← PC − 2 × df ⟨5:0⟩)	Decrement register by 1. If result is not equal to 0, branch. Subtract 2 × 6-bit offset from PC to get new PC.

Table 4-10
Floating Instruction Set (FIS)

The following abbreviations are used in this table:

FSP = Floating Stack Pointer
FAC = ⟨31:00⟩ = FSP + 4 ⟨15:00⟩ □ FSP + 6 ⟨15:00⟩
FAS' ⟨31:00⟩ = FSP ⟨15:00⟩ □ FSP + 2 ⟨15:00⟩

Mnemonic Instruction and Op Code	ISP Notation	Description
FADD Floating ADD 07500R	FR ← FAC + FPS'; next	Move sum of accumulator and source to temporary register.
	((FR < XUL) V (FR > XLL)) → (FAC ← FR else NO OP); next	Store result if no underflow or overflow, NO OP otherwise.
	((FAC < 0) V (FAC < XLL)) → (N ← 1 else N ← 0);	Negative?, underflow?
	(FAC = 0) = > (Z ← 1 else Z ← 0);	Zero?
	((FAC > XUL) V (FAC > XLL)) → (V ← 1 else V ← 0);	Overflow?, underflow?
	C ← 0	Clear Carry
FSUB Floating Subtract 07501R	FR ← FAC - FPS'; next	Move difference of accumulator and source to temporary register.
	((FR < XUL) V (FR > XLL)) → (FAC ← FR else NO OP); next	Store result if no underflow or overflow, NO OP otherwise.
	(FAC < 0) V (FAC < XLL)) → (N ← 1 else N ← 0);	Negative?, underflow?
	(FAC = 0) → (Z ← 1 else Z ← 0);	Zero?
	(FAC > XUL) V (FAC > XLL)) → (V ← 1 else V ← 0);	Overflow?, underflow?
	C ← 0	Clear Carry

Table 4-10 (Cont)
Floating Instruction Set (FIS)

Mnemonic Instruction and Op Code	ISP Notation	Description
FMUL Floating Multiply 07502R	FR ← FAC * FPS'; next	Move product of accumulator and source to temporary register.
	((FR < XUL) V (FR > XLL)) → (FAC ← FR else NO OP); next	Store result if NO overflow or underflow, NO OP otherwise.
	((FAC < 0V (FAC < XLL)) → (N ← 1 else N ← 0);	Negative?, underflow?
	(FAC = 0) → (Z ← 1 else Z ← 0);	Zero?
	((FAC > XUL) V (FAC > XLL)) → (V ← 1 else V ← 0);	Overflow?, underflow?
	C ← 0	Clear Carry
FDIV Floating Divide 07503R	(FPS = 0) = C ← 1	
	(FPS ≠ 0) → FR ← FAC / FPS'; next	Move result of division to temporary register.
	((FR < XUL) V (FR > XLL)) → (FAC ← FR else NO OP);	Store result if NO overflow or underflow, NO OP otherwise.
	((FAC < 0) V (FAC > XLL)) → (N ← 1 else N ← 0);	Negative?, underflow?
	(FAC = 0) → (Z ← 1 else Z ← 0);	Zero?
	((FAC > XUL) V (FAC > XLL)) → (V ← 1 else V ← 0);	Overflow?, underflow?
	(FPS = 0) → (C ← 1 else C ← 0)	Divide by Zero?

Table 4-11
Memory Management Instruction Set

Mnemonic Instruction and Op Code	ISP Notation	Description
MFPI/D	r ← D'; next	Get destination operand from previous I space.
Move From	SP ← SP - 2;	Push stack.
Previous	N ← r ⟨15⟩;	Set N if negative.
Instruction	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);	Set Z if 0.
Space	V ← 0;	Clear V.
0065DD	Mw [SP] ← r	Put operand into current address space.
MTPI/D	r ← Mw [SP] ;	Get data from current stack.
Move To	SP ← SP + 2; next	Pop stack.
Previous	N ← r ⟨15⟩;	Set N if negative.
Instruction	if (r ⟨15:0⟩ = 0) then (Z ← 1 else Z ← 0);	Set Z if 0.
Space	V ← 0;	Clear V.
0066DD	D' ← r	Move to previous I space destination.

4.3 PROCESSOR OPTIONS

The basic KD11-A Processor contains space for installing six processor options. In addition, there is a Small Peripheral Controller (SPC) slot that is usually used for an input terminal control (such as the DECwriter or Teletype interface) but that also can be used for a variety of options dependent on the user's individual requirements. The specific slot, or slots, allocated for each option is listed in Table 4-12 and shown in Figure 6-3.

The available processor options are:

a. KE11-E Extended Instruction Set (EIS)

b. KE11-F Floating Instruction Set (FIS)

c. KJ11-A Stack Limit Register

d. KT11-D Memory Management

e. KW11-L Line Time Clock

f. KM11-A Maintenance Console

g. Small Peripheral Controller (variable option)

The above options can be used in any combination as they function independently with two exceptions. The KE11-F (FIS) option physically requires the KE11-E (EIS) option, and software for the KT11-D option requires the KJ11-A option. Each option is discussed separately in subsequent paragraphs which include a general description, specifications, and a reference to more detailed documents.

Table 4-12
Location of Processor Options

Option	Section(s)	Slot
KE11-E Extended Instruction Set (EIS)	A–F	02
KE11-F Floating Instruction Set (FIS)	A–D	01
KJ11-A Stack Limit Register	E	03
KT11-D Memory Management	A–F	08
KW11-L Line Time Clock	F	03
KM11-A Maintenance Console		
For maintenance of the basic processor	F	01
For maintenance of the KT11-D and/or EIS and FIS options	E	01
Small Peripheral Controller	C–F	09

4.3.1 KE11-E Extended Instruction Set (EIS) Option

The KE11-E Extended Instruction Set Option is a processor option that expands the basic PDP-11/40 instruction set to include: MULtiply (MUL), DIVide (DIV), Arithmetic SHift (ASH), and Arithmetic SHift Combined (ASHC). The option permits multiplication and division of signed 16-bit numbers and arithmetic shifting of signed 16-bit or 32-bit numbers. Condition codes are set on the result of each instruction.

The KE11-E (EIS) option is a single hex (six section) module (M7238) that plugs directly into slot A02-F02 of the processor backplane. The option functions as an extension of the basic KD11-A data paths, microbranch control, and control ROM. The basic processor timing is not degraded when this option is used. The NPR latency is not affected when the instructions are being executed. Interrupts are serviced at the end of each instruction in the standard manner.

There are no addressable registers in the KE11-E option. All operands are fetched from either core memory or from the general processor registers and the result of each operation is stored in the general registers.

The MUL instruction uses the contents of the effective addresses specified by the destination register and the source register as 2's complement integers which are multiplied. The result is stored in the source register and, if even, the low-order result in the succeeding register. If the source register address is odd, only the low-order product is stored. The MUL instruction multiplies full 16-bit numbers for a 32-bit product.

The DIV instruction permits a 32-bit 2's complement dividend in the destination registers (R and R+1) to be divided by a 16-bit divisor in the source register. A 16-bit quotient is left in R and the 16-bit remainder is left in R+1. The sign of the remainder is always the same as the sign of the dividend unless the remainder is zero. Overflow is indicated if more than 16 bits are required to express the quotient. In this case, the instruction is aborted, the overflow condition code is set, the expansion processor status (EPS) word is loaded into the processor PS register, and the program branches to a service routine. If the source register is zero, indicating divide by 0, an overflow is indicated.

When the ASH instruction is used, the contents of the selected register is shifted right or left the number of places specified by a count. This shift count is a 6-bit, 2's complement number which is the least significant 6 bits of the destination operand. If the count is positive, the number is shifted left; if it is negative, the number is shifted right. This allows for shifts from 31 positions left to 32 positions right (+31 to -32). A count of zero causes no change in the number.

When the ASHC instruction is used, the contents of a register (R) and the contents of another register (R+1) are treated as a single 32-bit word. Register R+1 represents bits 0–15, register R represents bits 16–31. This 32-bit word is shifted right or left the number of places specified by a count. This shift count is the same as that described for the ASH instruction and permits shifts from +31 to -32. If the selected register (R) is an odd number, then R and R+1 are the same. In this case, a shift becomes a rotate and the 16-bit word is rotated the number of counts specified by the shift count (up to 16 shifts).

Specifications for the KE11-E option are listed in Table 4-13. A detailed description of this option is given in the *KE11-E and KE11-F Instruction Set Option Manual,* EK-KE11E-TM-002.

Table 4-13
KE11-E (EIS) Specifications

Function	Description
Instructions	MULtiply (MUL) DIVide (DIV) Arithmetic SHift (ASH) Arithmetic SHift Combined (ASHC)
Operations	Multiplication and division of signed 16-bit numbers. Arithmetic shifting of signed 16-bit or 32-bit numbers.
Registers	None in option. Operands fetched from core or general processor registers.
Timing (approximate)	MUL = 9.5 μs DIV = 10.5 μs ASH = 3.4 μs plus address calculation time plus 300 ns times absolute value of shift count. ASHC = 3.8 μs plus address calculation time plus 300 ns times absolute value of shift count.
Size	Single hex module (M7238)

4.3.2 KE11-F Floating Instruction Set (FIS) Option

The KE11-F Floating Instruction Set Option enables the KD11-A Processor to perform arithmetic operations using floating point arithmetic. The prime advantage of this option is increased speed without the necessity of writing complex floating point software routines. The KE11-F performs single-precision operations. The KE11-F option cannot be used unless the KE11-E (EIS) option has been installed in the system.

The KE11-F (FIS) option is a single quad module (M7239) that plugs directly into slot A01-D01 of the processor backplane. If a BR is issued before the instruction is within approximately 8 μs of completion, the floating point instruction is aborted. In this event, the Program Counter (PC) points to the aborted floating point instruction, making the instruction the next instruction to be performed by the program. The NPR latency is not affected when floating point instructions are being executed. Interrupts are serviced at the end of each instruction in the standard manner.

The FIS option provides four special instructions: Floating point ADDition (FADD), Floating point SUBtraction (FSUB), Floating point MULtiplication (FMUL), and Floating point DIVision (FDIV).

Floating point representation of a binary number consists of three parts: an exponent, a mantissa, and the sign of the mantissa. The mantissa is a fraction in magnitude format with the binary point positioned between the sign bit and the most significant bit. If the mantissa is normalized, all leading 0s are eliminated from the binary representation; the most significant bit is thus a 1. Leading 0s are removed by shifting the mantissa left; however, each left shift to the mantissa must be followed by a decrement of the exponent value to maintain the true value of the number. The exponent value represents the power of 2 by which the mantissa is multiplied to obtain the value to be used.

For FADD or FSUB operations, the exponents must be aligned (or equal). If they are not, the mantissa with the smaller exponent is shifted right until they are. Each right shift is accompanied by incrementation of the exponent value. Once the exponents are aligned (equal), the mantissa is added or subtracted. The exponent value indicates the number of places the binary point is to be moved in order to obtain the actual representation of the number.

For FMUL instructions, the mantissas are multiplied and the exponents are added. For FDIV instructions, the mantissas are divided and the exponents are subtracted.

The KE11-F option stores the exponent in excess 200_8 notation. Therefore, values from -128 to +127 are represented by the binary equivalent of 0 to 255 (octal 0–377). Mantissas are represented in sign magnitude form.

The binary radix point is to the left. The result of the floating-point operations is always rounded away from zero, increasing the absolute value of the number.

If the exponent is equal to 0, the number is assumed to be 0 regardless of the sign bit or fraction value. The hardware generates a clean 0 (32-bit word all zeros) in this instance.

Specifications for the KE11-F option are listed in Table 4-14. A detailed description of this option is given in the *KE11-E and KE11-F Instruction Set Option Manual,* EK-KE11E-TM-002.

4.3.3 KJ11-A Stack Limit Register Option

The KJ11-A option enables variation of the limits of the stack area. In the basic PDP-11/40 System, the first 400_8 memory locations (0 through 377_8) are reserved for storage of trap and interrupt vectors. This area of memory should be accessed only when an interrupt subroutine is to be executed or a trap error occurs such as a power failure. Normally, memory is arranged such that the system stack area is above this vector area. However, to prevent inadvertent entrance of the stack into the vector area, protection is provided. In the basic KD11-A Processor, this protection is provided by a fixed boundary (400_8), detection circuit. The KJ11-A Stack Limit Register Option provides a programmable boundary detection circuit. Note that the processor response for a yellow or red zone boundary violation is unchanged; only the location of the boundary is variable.

Specifications for the KJ11-A option are listed in Table 4-15. A detailed description of this option is presented in the *KD11-A Processor Maintenance Manual,* EK-KD11A-MM-001.

Table 4-14
KE11-F (FIS) Specifications

Function	Description		
Prerequisite	KE11-E Extended Instruction Set Option		
Instructions	Floating point ADDition (FADD) Floating point SUBtraction (FSUB) Floating point MULtiply (FMUL) Floating point DIVide (FDIV)		
Operations	Single precision, floating point addition, subtraction, multiplication, and division of 24-bit numbers.		
Registers	None in option. Operands fetched from core.		
Timing	Time = Basic Time Plus Binary Point Alignment Time Plus Normalization Time		
INSTR	**Basic Time*** (μs)	**Binary Point Alignment Time** (μs)	**Normalization Time Per Shift** (μs)
FADD	18.78	0.30	0.34
FSUB	19.08	0.30	0.34
FMUL	29.00	---	0.34
FDIV	46.27	---	0.34
Size	Single quad module (M7239)		

*Basic instruction times for FADD and FSUB assume exponents are equal or differ by one.

4.3.4 KT11-D Memory Management Option

The KT11-D Memory Management Option provides the capability to expand the 32K word addressing of the KD11-A Processor to 128K words and to enhance the use of multi-user, multi-program systems. A timesharing environment is created by providing two operating modes: kernel and user. These modes can operate with or without relocation and protection. Mode selection is made by using an expanded KD11-A processor status word.

The KT11-D option basically performs four functions:

a. Expands the basic 32K word address capability to 128K words.

b. Provides address space with memory relocation and protection for multi-user timesharing systems.

c. Implements the separate address spaces for the kernel and user modes of operation.

d. Provides memory management information for use of memory in multi-user, multi-program systems.

Specifications for the KT11-D Memory Management Option are listed in Table 4-16. A detailed description of this option is given in the *KT11-D Memory Management Option Manual,* DEC-11-HKTDA-B-D.

Table 4-15
KJ11-A Specifications

Function	Description
Register	8-bit stack limit register (bits 15–08) addressable by console or processor, but not by any bus device.
Register Address	777774 (word addressing) 777775 (byte addressing)
Stack Limit	Programmable; if register is all 0s, then: 000–337 = red zone 340–377 = yellow zone
Yellow Zone Violation	Occurs if the stack operation's address is equal to or less than the stack limit address by 16 words or less. The operation is completed and then a TRAP is executed.
Red Zone Violation	Occurs if the stack operation's address is less than the stack limit address by more than 16 words. The operation is aborted (fatal stack error), a stack vector exists at address 4, and a bus error TRAP occurs. The old PS and PC are pushed into locations 2 and 0; the new PC and PS are taken from locations 4 and 6.
Initialized Stack Limit	The initialized state of the KJ11-A option is 377; this is equivalent to the fixed stack limit of a PDP-11/40 System without the KJ11-A option.
Size	One single-height module.

4.3.5 KW11-L Line Time Clock Option

The KW11-L Line Time Clock option provides a method of referencing real intervals. This option generates a repetitive interrupt request to the processor. The rate of interrupt is derived from the ac line frequency, either 50 Hz or 60 Hz. The accuracy of the clock period, therefore, is dependent on the accuracy of this frequency source.

The KW11-L option can be operated in either an interrupt or noninterrupt mode. When in the interrupt mode, the clock option interrupts the processor each time it receives a pulse from the line frequency source. In the noninterrupt mode, the clock option functions as a program switch that the processor can examine or ignore. Mode selection is made by the program.

Specifications for the KW11-L Line Time Clock Option are listed in Table 4-17. A detailed description of this option is given in the *KW11-L Line Time Clock Manual,* EK-KW11L-TM-002.

Table 4-16
KT11-D Specifications

Function	Description
Memory Expansion	Expands PDP-11/40 memory address capability up to 124K words.
Interface	Address line outputs compatible with PDP-11 Unibus.
Timing	Timing derived from KD11-A Processor.
Delay	Adds 150 ns to every memory reference when installed.
Operating Modes	Kernel and user.
Available Pages	Provides eight 4K word pages for each mode.
Page Length	A page can vary in length from one 32-word block up to 128 32-word blocks. Maximum page length is 4096 words.
Program Capacity	Eight 4096-word pages accommodate 32K word programs.
Size	Single hex module (M7236).

Table 4-17
KW11-L Specifications

Function	Description
Register	2-bit status register bit 06 – interrupt enable bit 07 – interrupt monitor
Register Address	777546
Vector Address	100
Mode Control	bit 06 set – interrupt mode bit 06 clear – non-interrupt mode
Monitor Function	Bit 07 can be used to serve as a partial check on the origin of the interrupt vector.
Interrupt	Same as line frequency; 50 or 60 Hz.
Priority Level	BR6
Size	Single-height module (M787) that mounts in KD11-A Processor slot F03.

4.3.6 KM11-A Maintenance Console Option

The KM11-A Maintenance Console (also referred to as the maintenance module) is a 2-module set containing 28 indicator lights and 4 switches used to monitor and control functions during maintenance tests.

The functions monitored by the option depend on which processor slot the module is installed in. Different overlays are provided to indicate the function being tested. The module is installed in processor backplane slot F01 when testing the KD11-A Processor and is installed in slot E01 when testing the KT11-D or KE11-E, F options.

A detailed description of the maintenance console is provided in the *KD11-A Processor Maintenance Manual,* EK-KD11A-MM-001.

4.3.7 Small Peripheral Controller

Processor backplane slot 09, sections C–F, permit installation of any Small Peripheral Controller option. This slot is normally used to install the controller for the PDP-11/40 System input/output device, but may be used for any Small Peripheral Controller, if desired.

The standard controllers for system I/O devices are:

a. DL11 Asynchronous Line Interface – the standard PDP-11/40 controller used for either the LA30-S DECwriter or for the ASR 33 Teletype unit.

b. LC11 DECwriter Control – a controller used when the LA30-P DECwriter is used as the system I/O device.

c. KL11 Teletype Control – an earlier version of the Teletype control which is used only with the ASR 33 Teletype unit.

A brief description of the DL11 is given in Paragraph 1.3.7. Detailed descriptions of all three controllers are included in related maintenance manuals listed in Table 1-2.

CHAPTER 5
SYSTEM PERIPHERALS AND OPTIONS

5.1 SCOPE

This chapter lists the peripherals and options that may be used with the PDP-11/40. Functional and detailed descriptions of these units are contained in other documents, listed in Paragraph 5.2.

5.2 PERIPHERALS AND OPTIONS

Table 5-1 lists the PDP-11/40 peripherals and options. The *PDP-11 Peripherals Handbook* contains functional descriptions of these units. Detailed descriptions are provided in associated equipment maintenance manuals. The handbook is provided with each system and each peripheral and option delivered is accompanied by its own maintenance manual.

Table 5-1
PDP-11/40 Peripherals and Options

Function	Equipment
Input/Output	Teletype PC11 High-Speed Reader/Punch LP11 High-Speed Line Printer CM11/CR11 Card Reader LA30 DECwriter
Magnetic Tape Storage	TC11/TU56 DECtape TM11/TU10 Magtape
Display	VT01A Storage Display VR01A Oscilloscope VR14 Point Plot Display VT05 Alphanumeric Terminal RT01 DEClink Terminal
Disk Storage	RC11/RS64 DECdisk Memory RF11/RS11 Disk and Control RK11-C/RK02, RK03, RK05 DEC Pack Disk Cartridge System

Table 5-1 (Cont)
PDP-11/40 Peripherals and Options

Function	Equipment
Bus Extension	DB11 Bus Repeater DT11-A, DT11-B Bus Switches
Communications	DC11 Asynchronous Line Interface DN11 Automatic Calling Unit Interface DP11 Synchronous Interface DM11 Asynchronous 16-Line Single Speed Multiplexer DL11 Full Duplex 8-bit Asynchronous Line Interface
DATA Acquisition and Control	AFC11 Low Level Analog Input Subsystem AD01D Analog to Digital Conversion Subsystem AA11D Digital to Analog Conversion Subsystem

CHAPTER 6
EQUIPMENT MOUNTING AND POWER

6.1 SCOPE

This chapter provides detailed information on the PDP-11/40 equipment mounting and power system.

The BA11-FC Mounting Box is basic to PDP-11/40 equipment mounting and is discussed in Paragraph 6.2. System unit allocations as well as processor and basic memory slot allocations are noted for the basic box. This information covers mounting space within the basic system cabinet and in adjacent cabinets (Paragraph 6.3).

The power system is duscussed in Paragraph 6.4 and consists of the 861 Power Controller (Paragraph 6.4.1), the H742 Power Supply (Paragraph 6.4.2), two H744 +5V Regulators (Paragraph 6.4.3), two H745 -15V Regulators (Paragraph 6.4.4), a power distribution panel, and interconnection and distribution cabling. Power controller interconnection, power system cable harnesses, and dc power distribution are discussed in Paragraphs 6.4.5, 6.4.6, and 6.4.7, respectively.

6.2 SYSTEM MOUNTING BOX

The major components of the PDP-11/40 System, with the exception of the power system and console I/O device, are mounted in a single BA11-FC Mounting Box. Space for additional memory and/or peripheral interfaces is also provided within this mounting box.

The BA11-FC Mounting Box is mounted in a standard DEC H960-C Cabinet, shown in Figure 6-1. The box is mounted on chassis slides that enable it to be pulled out for maintenance and/or installation of logic modules; the power supply, however, remains within the cabinet. Cooling fans are mounted on top of the box to provide proper cooling of the logic elements within the box. The KY11-D Programmer's Console is located on the front of this box.

The mounting box is capable of holding nine system units or equivalents. Each system unit casting contains four slots for mounting logic modules. An alternate double system unit contains nine slots because it has no center casting. This double system unit is used for the KD11-A Processor and MF11-L Memory.

Allocation of logic within the box is shown in Figure 6-2. A double system unit (with nine slots) is used for the processor and processor options. Another double system unit is used for the MF11-L Core Memory, which includes three modules to provide a basic 8K memory. This leaves space for five additional system units (or equivalents) for additional memory and/or peripheral interfaces. Note that core memory should always be placed as close to the processor as possible. The basic mounting box provides mounting space and cooling for these additional (expansion) units. Module allocations for the processor, and memory, are covered in Paragraphs 6.2.1 and 6.2.2, respectively. Programmer's console mounting is covered in Paragraph 6.2.3.

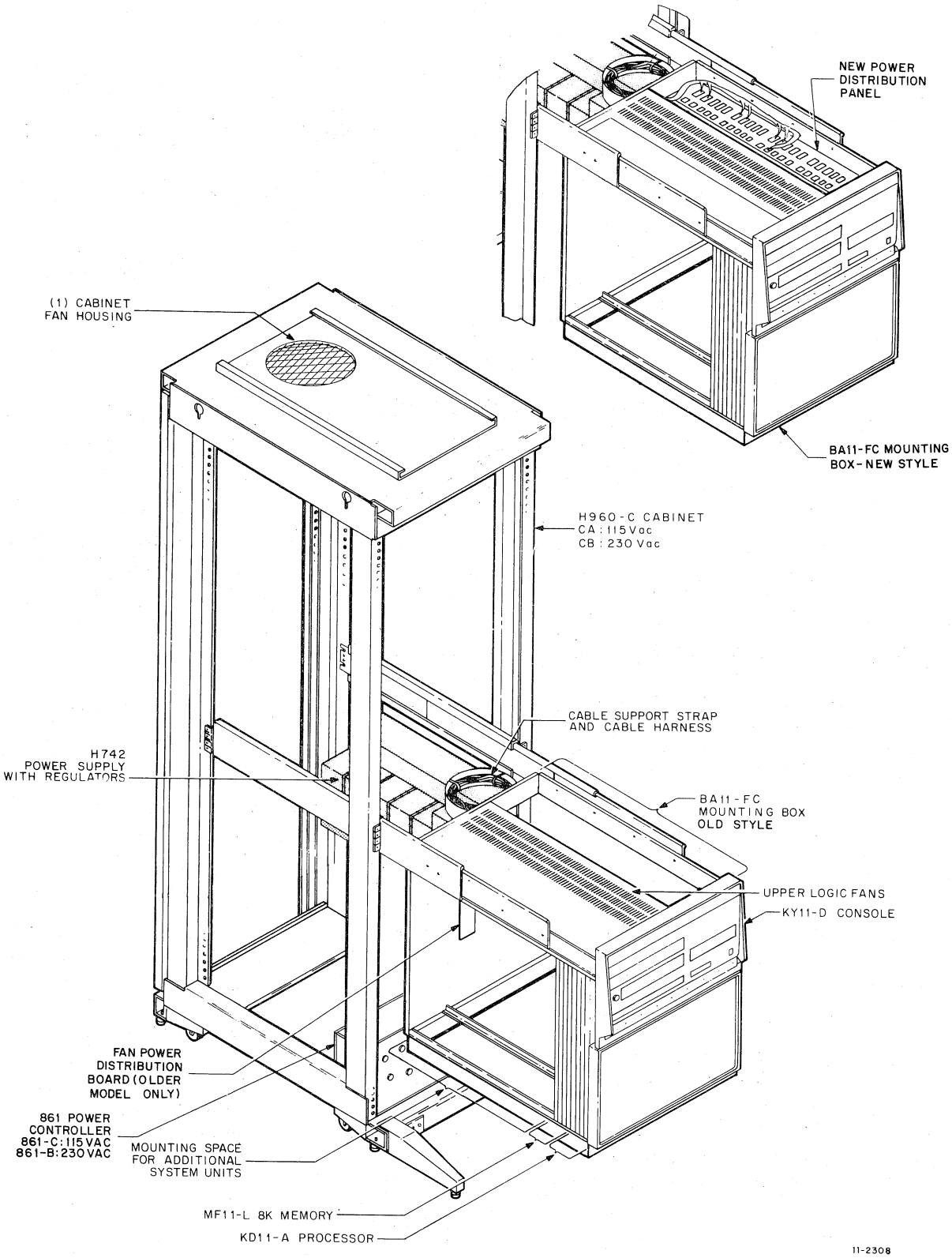


Figure 6-1 PDP-11/40 System Cabinet

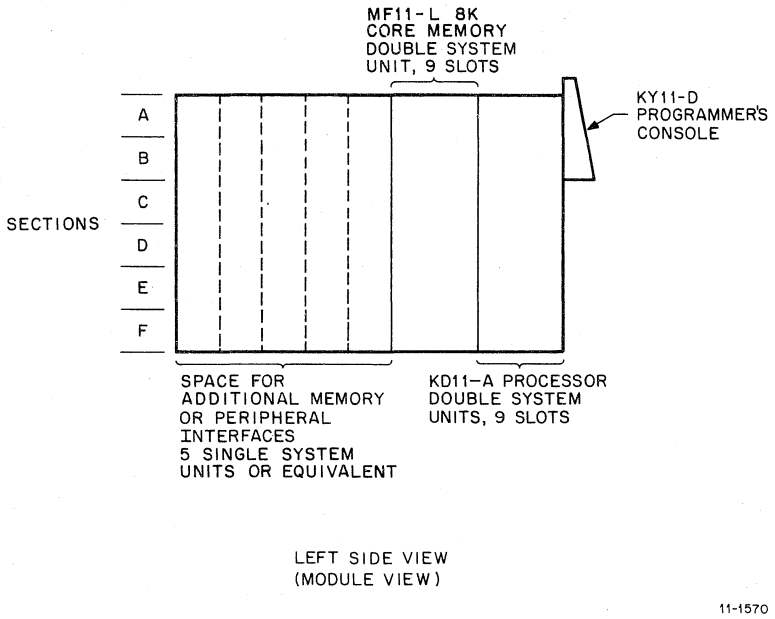


Figure 6-2 PDP-11/40 Mounting Box (BA11-FC)

6.2.1 Processor Module Allocations

Figure 6-3 shows the module allocation for the basic KD11-A Processor and processor options. The modules noted with an asterisk are the standard basic modules and must always be present. Other modules are optional with the specific option designation noted on the figure. The KT11-D Memory Management Option requires the KJ11-A M7237 module in addition to the M7236 module. The KM11-A Maintenance Console Option may be plugged into either slot F01 or E01, depending on whether the user is monitoring the basic KD11-A Processor or one of three processor options (KT11-D Memory Management, KE11-E Extended Instruction Set, or KE11-F Floating Instruction Set). Note that the maintenance console option is not installed during normal system operation.

6.2.2 Memory Module Allocations

Figure 6-4 shows the module allocation for the MF11-L Memory system. The basic MF11-L Memory consists of a single MM11-L 8K memory segment mounted on a double system unit backplane. The modules comprising the basic MF11-L Memory are indicated by an asterisk. If two additional MM11-L 8K segments are installed in slots four through nine as shown, the memory is expanded to 24K.

6.2.3 Programmer's Console Mounting

The KY11-D Programmer's Console is mounted on the front of the BA11-FC Mounting Box, shown in Figure 6-1. Mounting is integral with the bezel and panel mounting. The console interfaces directly with the processor. It provides control signals and Switch register information to the processor and receivers status and data information and operating power from the processor.

6.3 CABINET AND SYSTEM MOUNTING

Because of the modularity of the PDP-11/40 System, a variety of peripherals may be added to the basic system. Depending on the type and number of peripherals selected, the unused space in the basic system cabinet may be sufficient. If necessary, additional cabinets may be added to the system. The basic system cabinet is discussed in Paragraph 6.3.1; multiple-cabinet systems are discussed in Paragraph 6.3.2

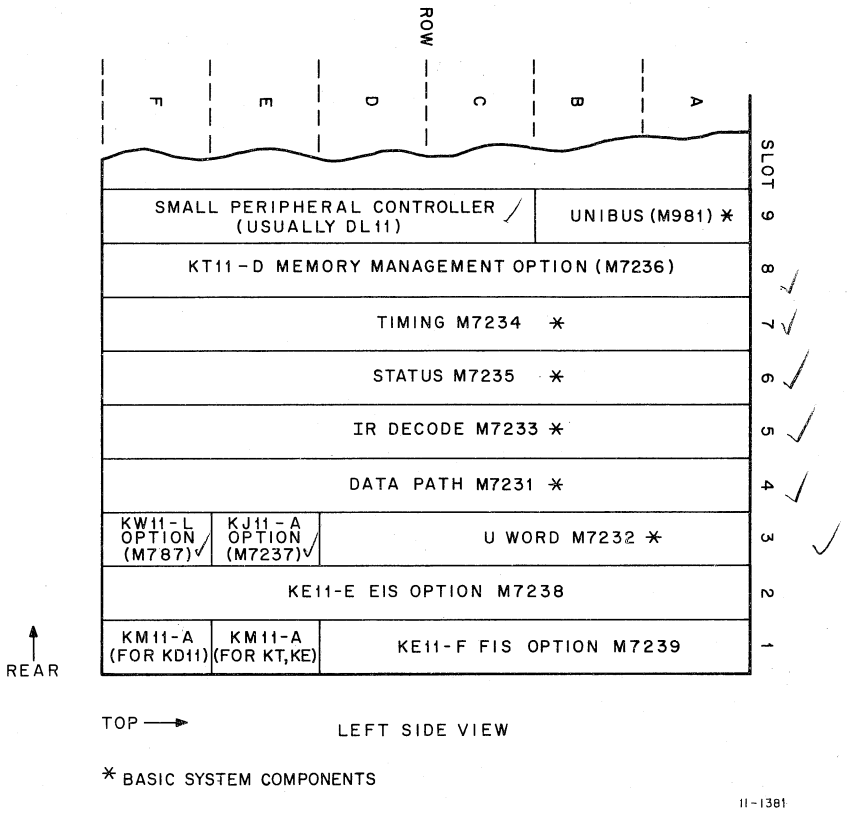
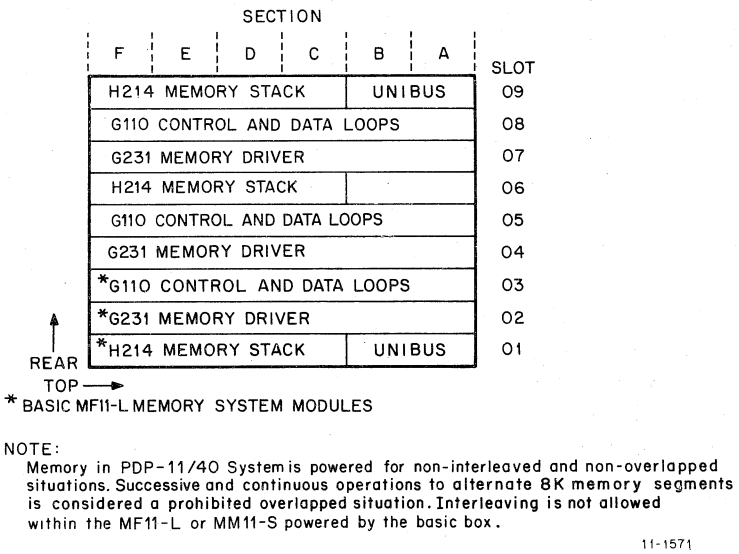


Figure 6-3 Module Allocation – KD11-A Processor, Basic and Options



NOTE:
Memory in PDP-11/40 System is powered for non-interleaved and non-overlapped situations. Successive and continuous operations to alternate 8K memory segments is considered a prohibited overlapped situation. Interleaving is not allowed within the MF11-L or MM11-S powered by the basic box.

11-1571

Figure 6-4 Module Allocation – MF11-L Memory, Basic and Optional MM11-Ls

6.3.1 System Cabinet

The cabinet housing the basic PDP-11/40 is divided into six levels (Figure 6-5). The bottom level (level six) is reserved for cable entry, however, power supplies and the AD01-D option may be installed there. Levels four and five contain the BA11-FC Mounting Box which houses the basic system. Levels one through three provide space for mounting up to three peripherals, each having a front panel height of 10-1/2 inches. If a high-speed paper-tape reader is added to the basic system, it is always installed directly above the BA11-FC Mounting Box. There are certain restrictions to mounting peripherals in cabinets (Paragraph 6.3.2). With the basic system cabinet, any free-standing peripheral (system I/O device, card reader, etc.) can be no further from the cabinet than the maximum length of the interconnecting cable between the interface in the cabinet and the device itself.

6.3.2 System Configuration

In many cases, the number and types of peripherals added to a basic system necessitate additional mounting cabinets. The standard cabinet layout for PDP-11 systems starts at the right and evolves to the left. Another standard practice is to define the equipment in the processor cabinet first, then move to the next cabinet not defined for a specific device. It is always necessary to keep in mind the overall Unibus chain to keep Unibus length to a minimum. Cooling, cabling, and logic interaction are all system considerations that must be accommodated.

Generally, configuring multiple cabinet systems requires that no full-depth device or combination of devices should be placed at the top position (level one) or bottom position (level six) of a cabinet. This restriction is necessary to ensure unrestricted cable entry at the bottom and proper air flow at the top. Devices can be placed in the unused cabinet space of another device provided the installation does not interfere with the operation of that device. Disk cabinets are normally used only for mounting a specific disk system and its options.

In any cabinet, the top position (level one) should be used only for rigidly fixed equipment. Levels two through five may be used for either rigidly fixed equipment or slide-mounted equipment. In any cabinet, levels two through five may be used for a peripheral device or for mounting an extension mounting box which is then used to house various device interfaces at the discretion of the user. Figure 6-5 illustrates typical mounting information for a multiple cabinet system.

A major logic interaction consideration in multiple cabinet systems is latency. Latency is defined as the longest time a device can be left unserviced before data is lost. Latency is usually a problem only in extremely large systems but should be considered for optimum system performance. A recommended priority scheme has been established to determine which peripherals should be mounted electrically closer to the processor to compensate for timing characteristics of the NPR devices and latency requirements for BR devices. These priorities are listed in Tables 6-1 and 6-2, respectively. The typical mounting information of Figure 6-5 accommodates these priorities. Additional information on system configuration is contained in PDP-11 Configuration Worksheet and the PDP-11/10,40 Site Preparation Worksheet.

Table 6-1
Timing Characteristics of PDP-11 NPR Devices

NPR Priority	Device	Worst Case Latency (μs)	Time Between Data Available (μs)
1	RK11/RK03	8.5	11.1
2	RP11	11	14.8*
3	RC11	12	16
4	RF11	13	16
5	RK11/RK02	19	22.2
6	TM11	29	32 (at 800 bpi)
7	TC11	67	200
8	DM11	100	119 (at 1200 baud)
9	CD11	800	
10	DR11-B	Dependent on customer use	

*The RP11 transfers two words each 14.8 microseconds.

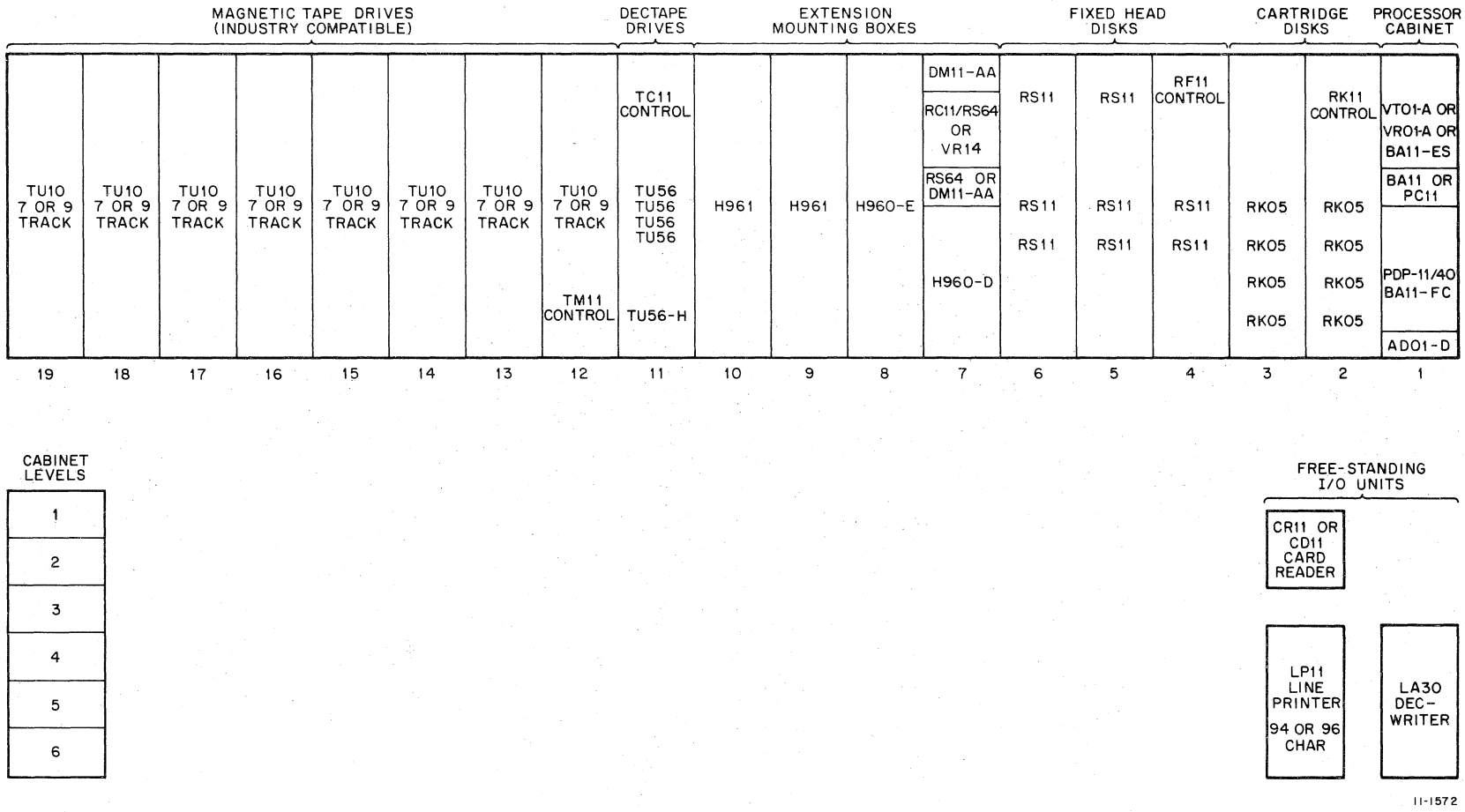


Figure 6-5 Typical Multiple Cabinet System Configuration

Table 6-2
Priority of Devices Affected by BR Latency

BR Level Priority	BR Levels			
	BR7	BR6	BR5	BR4
1	AD01*	KW11-L	DP11 @ 9600 baud or higher	KL11
2	DT11-B	TC11	DC11 @ 1800 baud	UDC11†
3		CR11	DP11 @ 4800 baud	AFC11**
4		CM11	DC11 @ 1200 baud	
5		KW11-P	DP11 @ 2400 baud	
6		UDC11†	DC11 @ 600 baud	
7			DC11 @ 2000 baud	
8			DC11 @ 300 baud	
9			DM11	
10			DR11-A**	
11			DR11-B	

*For AD01 sampling at high rates. Can be assigned to a lower level for slow input applications.
**Priority positions depend on customer application.
†UDC immediate = BR6; UDC deferred = BR4.

6.4 POWER SYSTEM

The PDP-11/40 power system converts a single phase, 115 or 230V, 47–63 Hz line voltage to dc voltages required by the system. In addition, the power system distributes ac power to drive cooling fans and generates power fail early warning signals and a clock signal.

The basic power system (Figure 6-6) consists of an 861 Power Controller, an H742 Power Supply, three H744 +5V Regulators, two H745 -15V Regulators, cooling fans, a power distribution panel, and interconnection and power distribution cabling. One H754 +20, -5V regulator may be substituted for an H745 if the MF11-U/UP is installed in an 11/40 mounting box. Two H754s may replace two H745s in an expansion box. One H754 can power two MF11-U/UP backplanes (up to 64K).

The power system block diagram (Figure 6-6) illustrates component interconnection and power and signal distribution within the power system.

All power system input power flows through the 861 Power Controller. The power controller output is switched on and off by the programmer's console OFF/POWER/LOCK switch. The H742 Power Supply and the cabinet fan obtain 115 or 230 Vac power from the power controller output connectors. Jumper wires are used to adapt the H742 to 115 or 230V input power. The H742 distributes 115 Vac to the logic fans, power supply fan and regulator fans, and 20–30 Vac to each of the regulators. The H742 also generates a +15V output, power fail early warning signals, and clock control signals which are distributed along with the regulator dc outputs to the power distribution panel. The power distribution panel provides a central distribution point for all dc voltages and control signals. Three power distribution expander boxes, mounted on the panel, provide input and output connectors that route power to the processor and memory power distribution harnesses.

The following paragraphs are detailed descriptions of power system components as well as dc power distribution. Prints referenced in the following discussions are contained in the *PDP-11/40 System Engineering Drawings.*

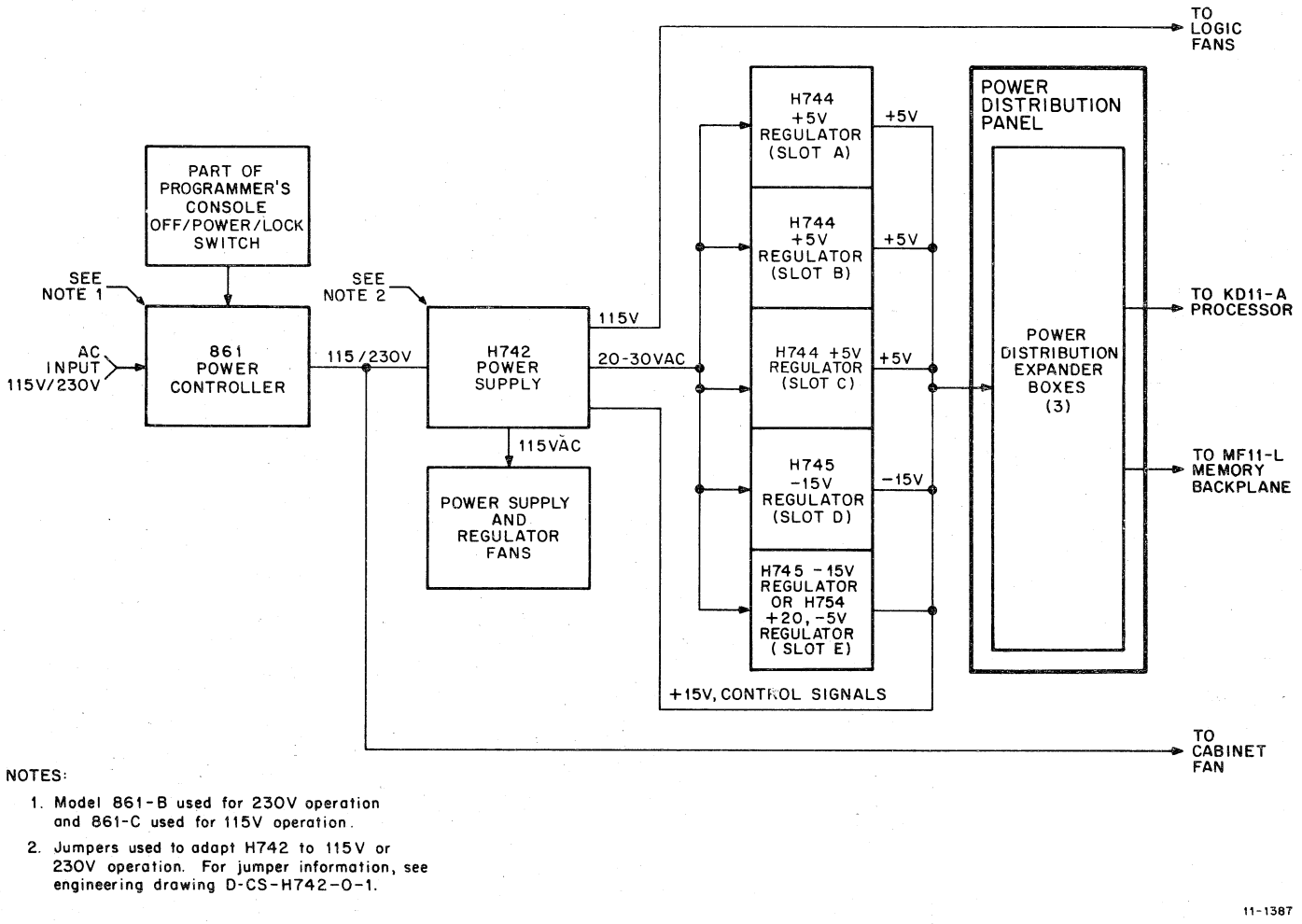


Figure 6-6 PDP-11/40 Power, System Block Diagram

6.4.1 861 Power Controller

The 861 Power Controller centralizes control of all system power. All power for one or several equipment cabinets is controlled by a single master switch. The ac input power cord (one per cabinet) is connected to the 861 Power Controller; the controller also provides two sets of ac power output connectors. One set of connectors can be switched on and off locally (via the power controller LOCAL/OFF/REMOTE switch) or remotely (via the programmer's console OFF/POWER LOCK switch) and is referred to as the switched ac output. The other set of connectors provides a continuous (uncontrolled) ac output power and is referred to as the unswitched ac output. All system units and peripherals are normally connected to the switched ac output. The unswitched ac output is provided for peripherals that require continuous power.

The power controller also provides protection against circuit overloading and excessive heat or fire in the equipment cabinet. If excessive current is drawn (30A @ 115V, 20A @ 230V), the input circuit breaker trips and all input power is removed. If there is excessive heat in the cabinet (160°F), the thermal switch closes and removes power from the power controller switched ac output.

For a complete description of the 861 Power Controller, refer to the *861-A, B, C Power Controller Maintenance Manual,* DEC-00-H861A-A-D. Note that the PDP-11/40 uses model 861-B for 230V operation and model 861-C for 115V operation.

For information on interconnecting 861 power controllers installed in separate equipment cabinets plus information on connecting the H720 Power Supply to 861 Power Controller, refer to Paragraph 6.4.5.

6.4.2 H742 Power Supply

The H742 Power Supply is functionally divided into two major parts:

a. Power Supply (drawing D-CS-H742-0-1) – used to provide the various ac input voltages required by the fans, regulators, and power control board.

b. Power Control Board (drawing C-CD-5409730-0-1) – used to provide +15V, line clock, and AC LO and DC LO signals for system use.

The PDP-11/40 power system operates with 115 or 230 Vac primary power inputs. Although different models of the 861 Power Controller are used, only one power supply (H742) is necessary. Jumpers are used on the H742 terminal strip (TB1) to adapt it to a 115 or 230 Vac primary power. If 115 Vac primary power is used, jumpers are placed between pins 1 and 2, and between pins 3 and 4 of TB1. If 230 Vac primary power is used, a jumper is connected between pins 2 and 3.

Line power is applied through TB1 to the primary of transformer T1. The transformer secondaries provide 20–30 Vac and 15–24 Vac input power for the power control board and 20–30 Vac for the regulators. Power to cooling fans is taken from transformer primary. 115 Vac is provided for fan operation with either 115 or 230 Vac prime power input.

The power control board portion of the power supply (drawing C-CS-5409730-0-1) provides a +15V output to power the Small Peripheral Controller, a clock output used to drive the KW11-L or KW11-P clock option, and the AC LO and DC LO control signals used to warn the processor of imminent power failure. The power control board circuits, which generate these outputs, are discussed in Paragraphs 6.4.2.1 through 6.4.2.3.

6.4.2.1 H742 +15V Output – The power control board of the H742 Power Supply contains a +15V/+8V dc supply and is shown on print C-CS-5409730-0-1. This dc supply receives 15–24 Vac from the secondary of transformer T1. This ac input is full-wave rectified by diode bridge D1. The resultant dc is applied to Darlington power amplifier Q1, through fuse F1. The bias on Q1 is controlled to provide +15 Vdc at output pins 2 and 3 with respect to output pins 4, 5, and 6 (ground). If the Q1 collector voltage starts to increase, the bias at the base of Q2 increases, and Q2 conducts slightly more current to maintain a constant output voltage. Zener diode D7 provides approximately +8 Vdc at output pin 1. The +8V output is not used in the PDP-11/40 System. When DC LO is grounded at output pin 9, Q2 conducts hard to cut off Q1 completely, thus removing the +15V output.

6.4.2.2 H742 Clock Output – The CLOCK output is derived off one leg of full-wave rectifier bridge D1 by voltage divider R10 and R11, and Zener diode D2. The CLOCK output is a 0 to 5V square wave at the line frequency of the input power source (47 to 63 Hz). The CLOCK output is used to drive the KW11-L Line Time Clock Option, which mounts in slot F03 of the processor backplane or the KW11-P option, which can be mounted in the Small Peripheral Controller slot. Operation of the KW11-L option is described in the *KW11-L Line Time Clock Manual,* EK-KW11L-TM-002; operation of the KW11-P option is described in the *KW11-P Programmable Real-Time Clock Manual,* EK-KW11P-MM-002.

6.4.2.3 AC LO and DC LO Circuits – The AC LO and DC LO control signals are used to warn the processor that a power failure is imminent, allowing the processor time to perform a power-fail sequence. If there is an ac power failure (line power or power supply failure), AC LO is asserted on the bus followed by DC LO. Sufficient time exists between these signals to allow storage of volatile data and the conditioning of peripherals. Note that the DC LO control signal is also used by the MF11-L Memory to inhibit memory operation.

The 20–30 Vac input from the secondary of transformer T1 is applied to the AC LO and DC LO sensing circuits on the power control board. The ac input is rectified and filtered by diodes D8 through D11 and capacitor C3. A common reference voltage is derived by resistor R18 and Zener diode D12. Both sensing circuits operate in a similar manner, and each contains a differential amplifier, a transistor switch, and associated circuits. The major difference is that the base of Q6 in the AC LO circuit differential amplifier is at a slightly lower value than that of Q9 in the DC LO differential amplifier. The operation of both sensing circuits depends upon the voltage across capacitor C3.

When AC LO is being sensed, the 20–30 Vac input is rectified and stored in capacitor C3 which charges and discharges at a known rate whenever the ac power is switched on or off. Thus, the voltage that is applied to the emitters of differential amplifier Q6/Q7 through R17 is a rising or falling waveform of known value. For example, when power fails or is shut down, the dc voltage decays at a known rate as determined by the RC time constant. If the voltage decreases to approximately 20V, the base of Q6 becomes negative with respect to the base of Q7. The increased forward bias on Q6 causes it to conduct more and the resultant decrease in Q7 causes it to cut off. This removal of voltage across R16 causes Q5 and Q4 to conduct, grounding the AC LO line at pin 8. The AC LO signal is applied through the cable harness and processor backplane to the processor power-fail initialize logic so that the power-fail sequence can be started.

The DC LO sensing circuit operates in a similar manner to the AC LO sensing circuit. The prime difference being the voltage level at which they "trip." For example, if the ac input starts to decrease, as a result of a power failure or shutdown, the AC LO lines are grounded before the DC LO lines. As power is restored, the ground is removed from the DC LO lines before it is removed from the AC LO lines. The DC LO signal is also applied to the power-fail initialize logic.

A description of how the AC LO and DC LO control signals are used in the KD11-A Processor is provided in the *KD11-A Processor Maintenance Manual.* For a description of how the DC LO control signal is used by the MF11-L Memory, refer to the *MM11-S, MF11-F, and MF11-LP Core Memory System Manual.*

6.4.3 H744 +5V Regulator

Two H744 +5V Regulators are used in the basic PDP-11/40 power system. The H744 circuit schematic is shown in drawing D-CS-H744-0-1. The following paragraphs describe the regulator circuit, overcurrent sensing circuit, and overvoltage crowbar circuit.

6.4.3.1 H744 Regulator Circuit – The 20–30 Vac input is a full wave which is rectified by bridge D1 to provide a dc voltage (24 to 40V, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on precision voltage regulator E1 which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 6-7. Regulator E1 is a monolithic integrated circuit that is used as a precision voltage regulator. It consists of a temperature-compensated reference amplifier, error amplifier, series-pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q2, pre-drivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15V for E1. Q5 is used as a level shifter; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary since the raw input voltage is well above that required for E1 operation. This +15V input is supplied while still retaining the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

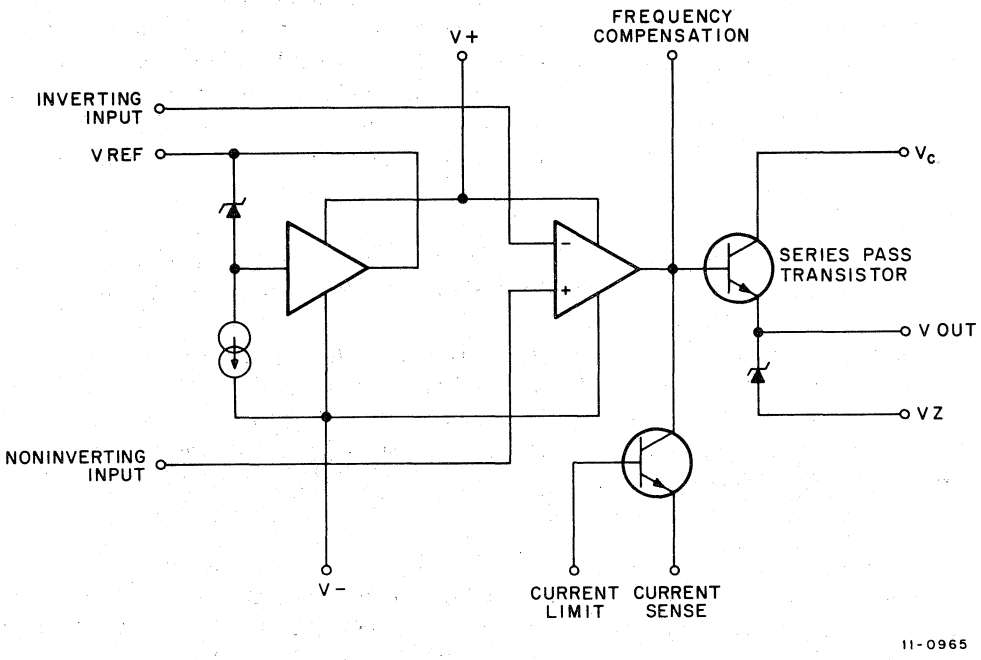


Figure 6-7 Precision Voltage Regulator E1, Simplified Diagram

The output circuit is standard for most switching regulators and consists of "free-wheeling" diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Free-wheeling diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, thus providing a discharge path for L1.

In operation, Q2 is turned on and off generating a square wave of voltage which is applied across D5 at the input of the LC filter (L1, C8 and C9). This type circuit is basically only an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, thus supplying regulation. The output voltage is sensed and fed back to E1 where it is compared with a fixed reference voltage. E1 turns pass transistor Q2 on and off according to whether the output voltage level decreases or increases. Defined upper and lower limits for the output are approximately +5.05V and +4.95V.

During one full cycle of operation the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30V) is applied across L1. If the output is already at a +5V level, then a constant +25V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time,

output capacitors C8 and C9 absorb this changing current and voltage, causing the output level (+5V at this point) to increase. When the output which is monitored by E1 reaches approximately +5.05V, E1 shuts off turning Q2 off, and the emitter of Q2 is clamped to ground. L1 discharges into capacitors C8, C9, and the load. Pre-drivers Q3 and Q4 are used to increase the effective gain of Q2 to ensure that Q2 can be turned on and off in a relatively short period of time.

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95V will be reached causing E1 to turn on which in turn causes Q2 to conduct, beginning another cycle of operation. Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05V) and minimum (+4.95V) values by E1. When +5.05V is reached, E1 turns Q2 off and when +4.95V is reached, E1 turns Q2 on. This type of circuit action is also referred to as a "ripple regulator."

6.4.3.2 H744 Overcurrent Sensing Circuit – The overcurrent sensing circuit consists of: Q1, R3 through R6, R25, R26, Q7, and C4. Transistor Q1 is normally not conducting; however, if the output exceeds 30A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the anode gate of Q7, Q7 turns on and E1 is biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35A (approximately) and the regulator is "short-circuit" protected. The regulator continues to oscillate in this new mode until the overload condition is removed.

6.4.3.3 H744 Overvoltage Crowbar Circuit – The overvoltage crowbar circuit consists of the following components: Zener diode D3, silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6.

Under normal conditions, the trigger input to the SCR (D7) is at ground because the voltage across Zener diode D3 is too small to cause it to conduct. As the +5V line approaches 6V, Zener diode D3 conducts and the voltage drop across resistor R23, draws gate current, and triggers the SCR. The SCR shorts the +5V line to ground through resistor R21, which is a current-limiting resistor. The SCR remains on until the capacitors discharge.

6.4.4 H745 -15V Regulator

Two H745 -15V Regulators are included in the PDP-11/40 power system. Operation of the H745 is basically the same as that of the +5V regulator. The H745 schematic is shown in drawing C-CS-H745-0-1. Input power (20 to 30 Vac) is taken from the secondary of transformer T1 and applied to the full-wave bridge rectifier (d1). The output of D1 is a variable 24 to 40 Vdc and is applied across capacitor C1 and resistor R1. The following paragraphs discuss the regulator circuit, overcurrent sensing circuit, and the overvoltage crowbar circuit.

6.4.4.1 H745 Regulator Circuit – Regulator operation is almost identical to that of the +5V regulator; however, the +15V input that is required for operation of E1 is derived externally and is applied across capacitor C2 to E1 and the inverting and noninverting inputs to E1 are reversed. In addition, the polarities of the various components are reversed. For example, Q5, which is used as a level shifter, is an NPN transistor on the +5V regulator but a PNP is required on the -15V regulator to allow the regulator to operate below ground (at -15V).

Under normal operating conditions, regulator operation centers around linear regulator E1 and pass transistor Q2, which is controlled by E1. Predetermined output voltage limits are -14.85V (minimum) and -15.15V (maximum). When the output reaches -15.15V, E1 shuts off, turning Q2 off, and L1 discharges into C8 and C9. When the output reaches -14.85V, E1 conducts, causing Q2 to turn on, increasing the output voltage.

6.4.4.2 H745 Overcurrent Sensing Circuit – The -15V regulator overcurrent sensing circuit is basically made up of the same components as the +5V regulator except Q1 is an NPN transistor in the -15V regulator. Transistor Q1 is normally not conducting; however, once the output exceeds 15A, Q1 turns on and C3 charges. When C3 reaches the same value as the anode gate of Q7, E1 is biased off, which turns Q2 off, thereby stopping current flow and turning the -15V regulator off. Thus, the regulator is short-circuit protected.

6.4.4.3 H745 Overvoltage Crowbar Circuit – When SCR D5 is fired, the -15V output is pulled up to ground and latched at ground until input power, or the +15V input is removed. A negative slope on the +15V line can be used to trip the crowbar for power-down sequencing, if desired.

6.4.4a H754 +20, -5V Regulator

If the system contains an option requiring +20 and -5V, such as the MF11-U/UP, H754 regulator(s) must be added. They are mounted into slot E of the PDP-11/40 cabinet or into slots D and/or E of an expander cabinet. Note that the installation of an H754 reduces the amount of available -15V power, because an H745 must be removed.

a. Regulator Circuit – The circuit (refer to schematic D-CS-H754-0-1) is very similar to that of the other regulators: like the H746, it has a voltage doubler input, but the output consists of two shunt regulator circuits, one for the +20V, the other for the -5V. The +20V shunt regulator consists of transistors Q4, Q10 and Q11; the -5V shunt regulator, of Q6 and Q9. Q10 and Q9 are the pass transistors.

   The output of the basic regulator is 25V (-5 to +20V). The shunt regulators are connected across this output, with a tap to ground between pass transistors Q9 and Q10. The voltage at the bases of Q6 and Q4 will vary with respect to ground, depending on the relative amount of current drawn from the +20V and -5V outputs of the regulator. If the +20V current increases, while the -5V current remains constant, the output voltage at the +20V output will tend to go more negative with respect to ground; this will cause the -5V output to go more negative also, since the output of the basic regulator is a fixed 25V. This change is sensed at the bases of Q6 and Q4; Q6 will conduct, causing Q9 to conduct also, thus increasing the current between -5V and ground until the balance between the +20V and the -5V is restored. At this time, neither Q6 nor Q4 will be conducting. If the -5V current increases, Q4 and Q10 will conduct to balance the outputs.

b. Overvoltage Crowbar Circuits – There are two crowbar circuits in the H754: Q7 and its associated circuitry for the +20V, and Q12 and its circuitry for the -5V. Either one will trigger SCR D9.

c. Overcurrent Sensing Circuit – The overcurrent circuit is comprised of Q1, Q8, Q13, Q14, and associated circuitry. The total peak current is sampled through R4. When the peak current reaches approximately 14A, Q1 turns on sufficiently to establish a voltage across R7 and R38, thus firing Q8. This pulls the voltage on pin 4 of the 723 up above the reference voltage on pin 5, thereby shutting off Q2. D6 now conducts, and the current through R37 turns on Q14, which turns on Q13. This keeps Q8 on for a time which is determined by the output voltage and L1. This action, in turn, allows the off-time of Q2 to be greater than the on-time; the off-time increases as the overload current increases, thereby changing the duty cycle in proportion to the load. The output current is thus limited to approximately 10A.

d. Voltage Adjustment – The +20V adjustment is located on the side of the H754; and the -5V potentiometer is on the top, next to the connector. To set the output voltages: power down, disconnect the load, power up, adjust for a 25V reading between the +20 and -5V outputs with the 20V potentiometer, then set the -5V between its output and ground. Power down, reconnect the load, power up, and then check and adjust the outputs again. This procedure is necessary because the +20V potentiometer (R17) actually sets the overall output of the regulator (25V from +20 to -5V), while the -5V adjustment (R21) controls the -5V to ground output. Refer to schematic drawing D-CS-H754-0-1.

6.4.5 861 Power Controller Interconnection

The 3-pin Mate-N-Lok connectors on the 861 Power Controller serve a multiple purpose. They are used along with the power controller bus cabling to (Figure 6-8):

a. connect the programmer's console OFF/POWER/LOCK switch to the 861 Power Controller, thus enabling remote control.

b. interconnect 861 Power Controllers in adjacent equipment cabinets when more than one cabinet is used in a system, thus enabling all power controllers to be controlled by the programmer's console switch.

c. connect H720 Power Supplies to the 861 Power Controller (H720 Power Supplies must be used whenever PDP-11/20 memories are used in the PDP-11/40 System).

d. connect optional cabinet-mounted thermal switches (cabinet-mounted thermal switches must be connected to pin 2 of any available connector, normally the same connector used for the programmer's console switch).

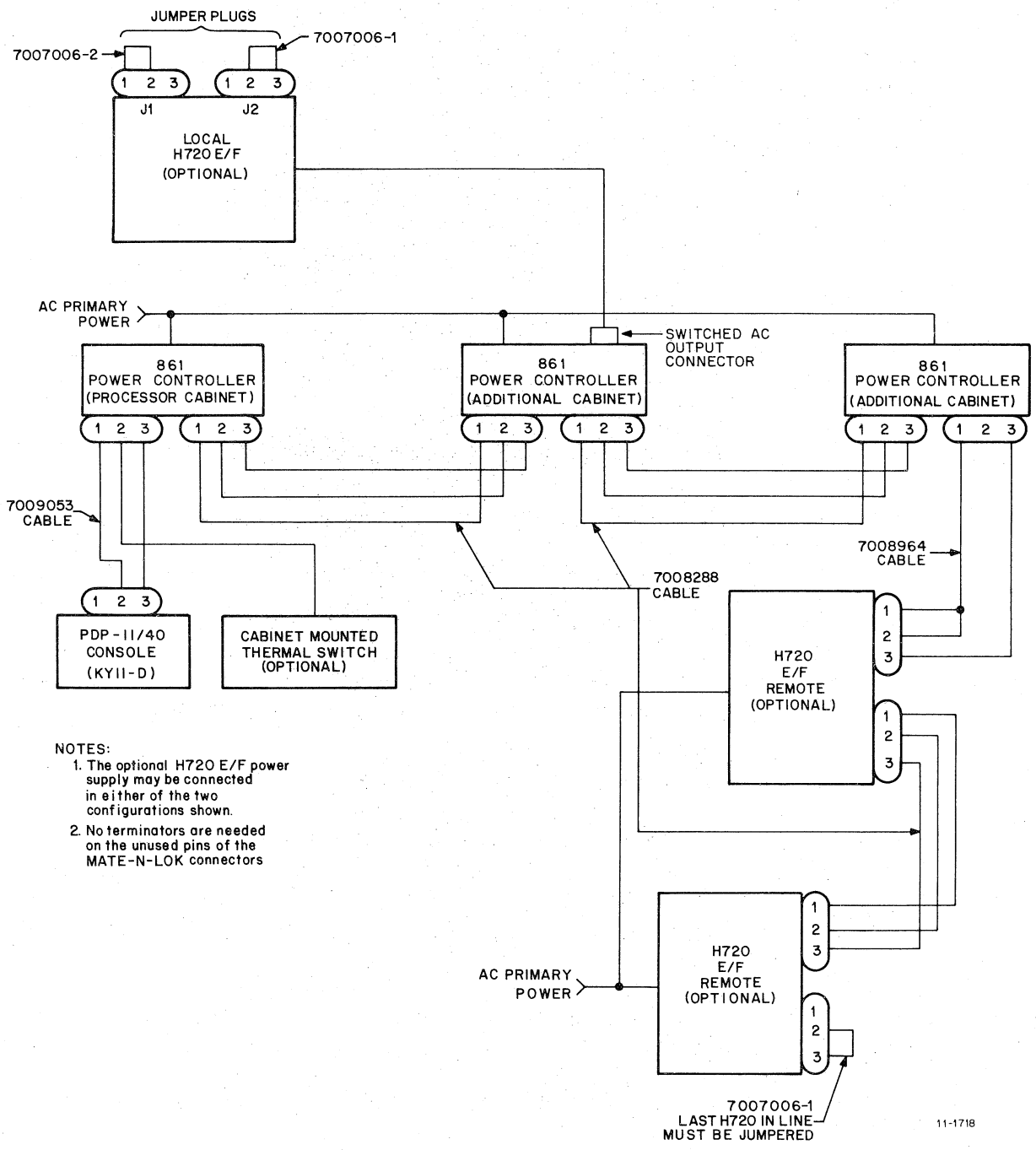


Figure 6-8 Power Control Interconnection

6.4.6 Power System Cable Harnesses

The overall layout of the PDP-11/40 power system is shown in Figures 6-10 for the early systems, and 6-13 for the newer ones. Four cable harnesses are shown on these drawings, which interconnect all power system units and provide power to the logic fans and the KD11-A Processor and MF11-L Memory backplanes. These harnesses and their functions are listed below:

a. H742 to 11/40 Power Harness – interconnects the H742 Power Supply, the H744 and H745 regulators, the logic fans and the power distribution panel (refer to Figures 6-11 and 6-14 for detailed wiring information on these harnesses).

   Harness Numbers: *OLD:* 7008754; *NEW:* 7009566

b. Console to Power Controller Harness – connects programmer's console OFF/POWER/LOCK switch to a 3-pin Mate-N-Lok connector on the 861 Power Controller (enables system power to be turned on and off by the programmer's console switch).

   Harness Numbers: *OLD:* 7009053; *NEW:* 7009053

c. PDP-11/40 Processor Power Harness – routes dc power and control signals from the power distribution panel to the KD11-A Processor backplane.

   Harness Numbers: *OLD:* 7009046; *NEW:* 7009564

d. First Memory (11/40) Power Harness – routes dc power and control signals from the power distribution panel to the basic MF11-L Memory backplane.

   Harness Numbers: *OLD:* 7009103; *NEW:* 7009565

A fifth cable harness, not shown on Figures 6-10 and 6-13, is used to connect any additional MF11-L Memories that may be installed in the basic BA11-FC Mounting Box to the power distribution panel. This harness is referred to as the MF11-L Power Harness (BA11-FC) and its cable number is 7009174 (OLD) or 7009560 (NEW).

If any DD11 type system units requiring the G772 module are installed in the basic BA11-FC Mounting Box, they are connected to the power distribution panel by cable harness 7009177 (OLD) or 7009562 (NEW).

For additional information on the DD11 system unit and its installation, refer to Chapter 2 of the *PDP-11 Peripherals Handbook.*

Appendix A lists all system unit power harnesses.

6.4.7 DC Power Distribution

Two different power distribution systems may be found in the PDP-11/40 and H960-D, -E Expansion Cabinets. The newer systems (serial number 6000 and higher) are easily distinguished from the older ones by observing the BA11-FC Mounting Box (see Figure 6-1): the newer machines have a horizontal power distribution panel, while the early ones have a vertical one. Harness numbers for the various system unit options are given in Appendix A.

The early systems are explained in Paragraph 6.4.7.1; the newer ones in Paragraph 6.4.7.2.

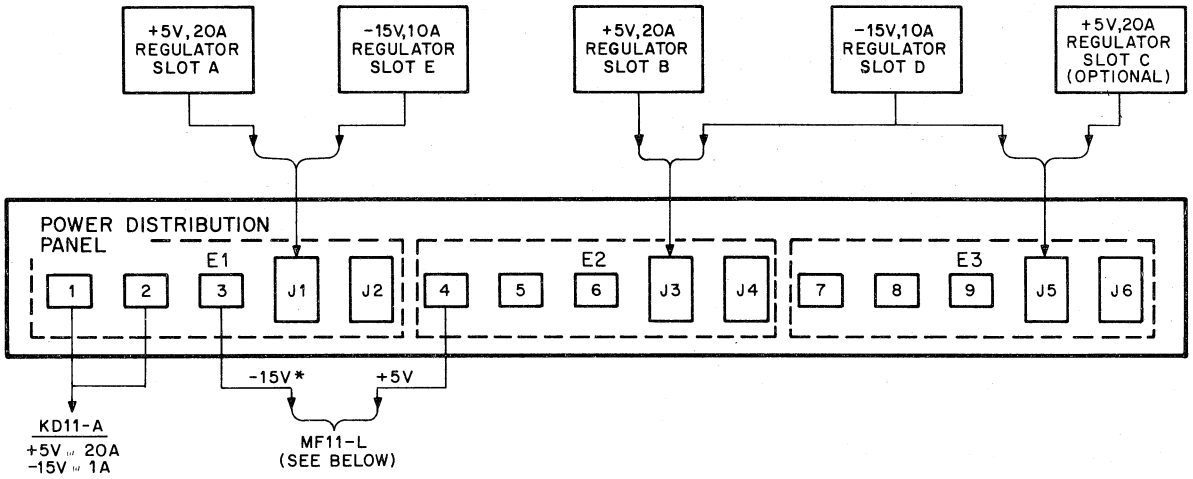
6.4.7.1 Early Power Distribution Systems (Refer to Figures 6-9 and 6-10) – DC power and control signals generated by the H742 Power Supply and the H744 and H745 regulators are distributed to three power distribution expander boxes that are mounted on the power distribution panel (Figure 6-9). Each expander box contains two input connectors and three output connectors. The three output connectors are wired in parallel, and all signals applied to the input connectors are applied to each of the output connectors.

Expander boxes E1 and E2 distribute power to the KD11-A Processor and the MF11-L Memory backplanes. Connector J1 receives dc power from the +5V regulator in slot A and the -15V regulator in slot E. This power is distributed through output connectors 1 and 3 and is totally committed to the KD11-A Processor and MF11-L Memory. Connector J3 receives dc power from the +5V regulator in slot B and the -15V regulator in slot D. Output connector 4 distributes +5V to the MF11-L Memory. Note that a 24K MF11-L Memory only requires 6.4A of +5V power, leaving 13.6A for distribution to expansion units.

Expander box E3 distributes power for expansion units. Connector J5 receives power from the +5V regulator in slot C and the -15V regulator in slot D. Care must be taken when connecting expansion units to avoid overloading the -15V regulator which is also connected to J3 on expander box E2.

Note that the H742 +15V and control signal outputs are not shown on Figure 6-9. The +15V output is applied to input connectors J1, J3, and J5. The control signal outputs are applied to input connectors J2, J4, and J6. Refer to Figure 6-11 for detailed information on the power distribution (harness 7008754).

In the case of an 11/40 CPU cabinet only (not in an H960-D or -E expansion cabinet), the Console to Power Control harness 7009053 is tied in with the main power harness.



* There are only two wires on this cable one black, one blue.

MF11-L POWER REQUIREMENTS (NON-INTERLEAVED)

BASIC MEMORY	OPTIONAL MEMORY	
8K	16K	24K
+5V @ 3.4A -15V @ 6.0A	+5V @ 4.9A -15V @ 6.5A	+5V @ 6.4A -15V @ 7.0A

11-1717

Figure 6-9 Regulated DC Power Distribution

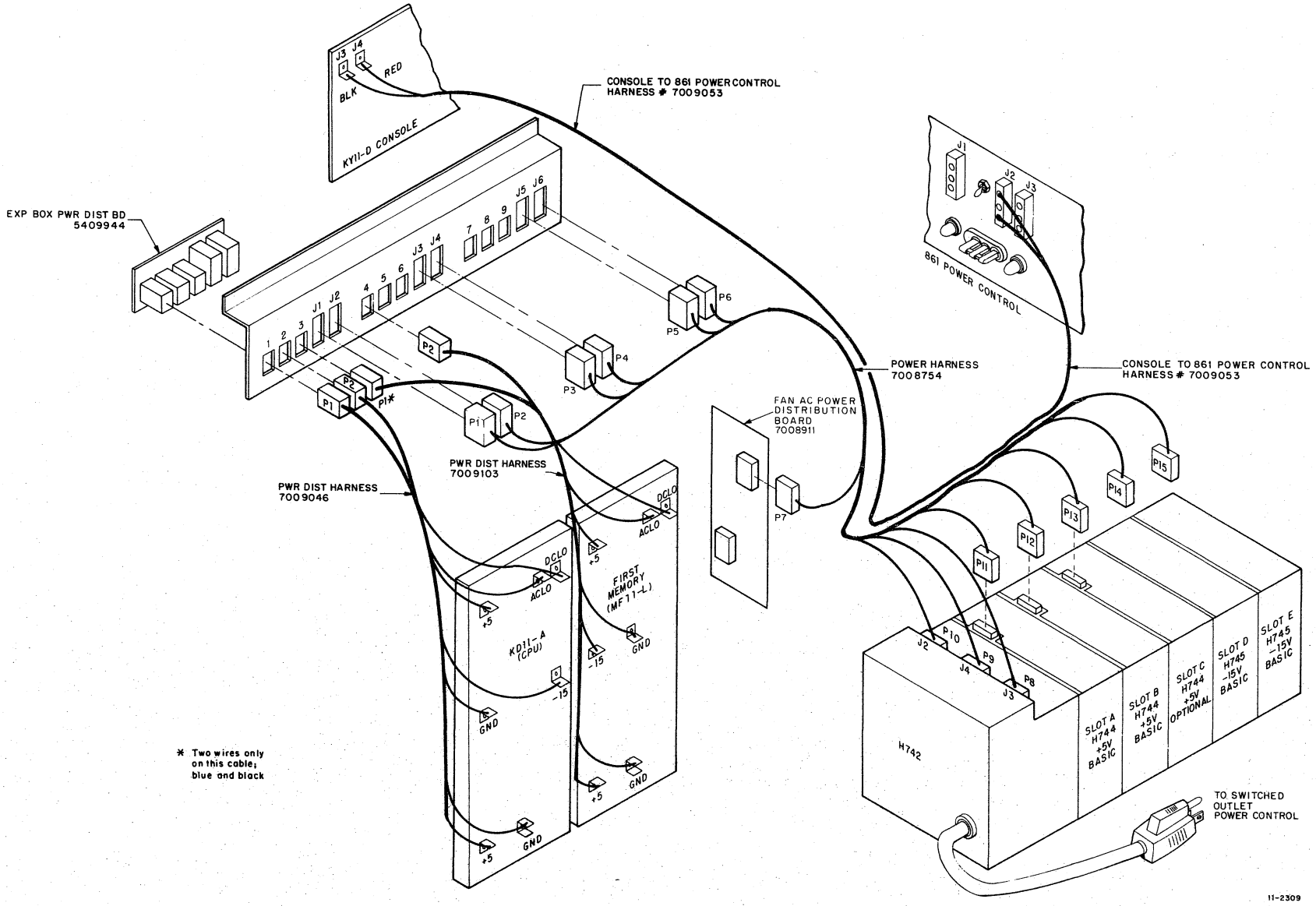


Figure 6-10 Power Distribution – Early Units with System Serial No. 5999 and Lower

Installation of MF11-U/UP in Early Units (See Figure 6-12) – A 7009569 conversion harness must be used between the H754 +20, -5 Vdc regulator and the backplane, in addition to a 7009568 harness between the backplane and the Power Distribution panel. One 7009569 can power two MF11-U/UP backplanes. If only one backplane is used, the jumpers to the second backplane should be cut. One 7009568 harness is required per backplane.

The H754 Regulator should be installed in slot E; the blue -15V wire between P1-1 and P15-1 should be removed; a jumper wire should be installed between P1-1 and P3-2. This will allow the H745 in slot D to supply -15 Vdc to the entire box.

The FM11-U field modification kit permits installation of up to two MF11-U/UP backplanes of 16K memory.

Refer to the field modification kit print set for installation procedures (DD-FM11-U).

6.4.7.2 Newer Power Distribution Systems (Refer to Figure 6-13) – Three 5410590 Power Distributors transmit the power generated by the H742 and its voltage regulators to the system units. Each distributor has five 15-pin power and five 6-pin signal connectors. Two of the power connectors on each distributor are used by the harness plugs, thus leaving three for connection to system units. The 6-pin signal connector is used only on the 5410590 Power Distributor closest to the CPU. A jumper harness connects the 6-pin plugs on the other distributors to this one (harness number 7009573).

The two power distributors closest to the front of the mounting box handle power for the KD11-A Processor and to the first MF11-L Memory. The CPU gets its +5 Vdc from the H744 in slot A and its -15 Vdc from the H745 in slot E. The MF11-L, as in the early power distribution system, gets its +5 Vdc from the H744 in slot B and its -15 Vdc from the H745 in slot E. The KD11-A uses harness number 7009564, and the first MF11-L number 7009565, to connect to the power distribution panel. The first MF11-L is connected as follows: the -15V connector (15 pin, 2 wire: blue and black) and the 6 pin signal connector plug into the first power distributor (the same one as the KD11-A); the +5V connector (the other 15 pin) plugs into the second power distributor. Any additional MF11-Ls require harness 7009560 and obtain power from a single power distribution connector, as would any other system units in the mounting box.

Figure 6-14 shows details of the new power distribution system (harness 7009566). Note that in the case of an 11/40 CPU cabinet only (not in an H960-D or -E expansion cabinet) there is a Console to Power Control harness 7009053 which is tied in with the main power harness.

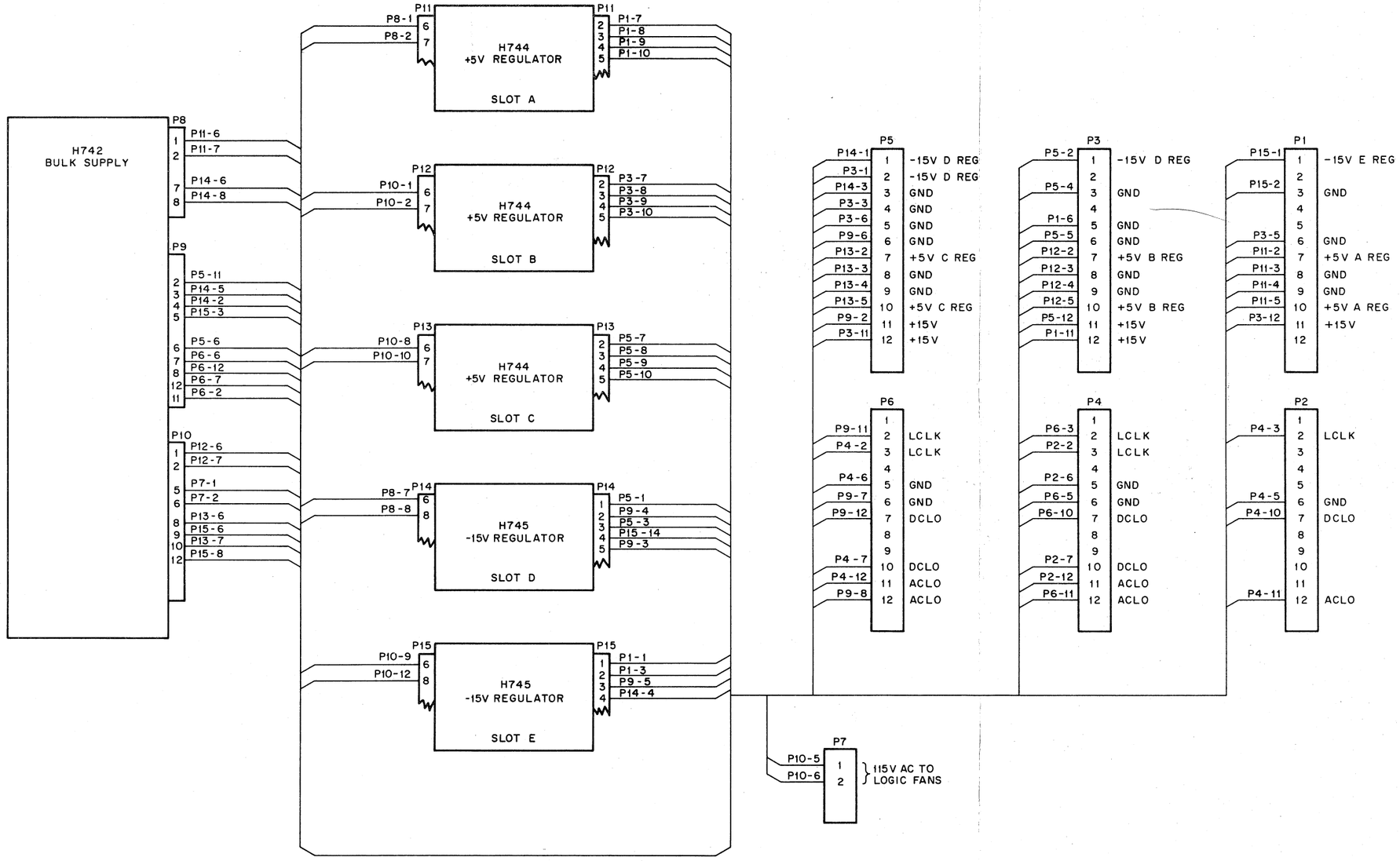
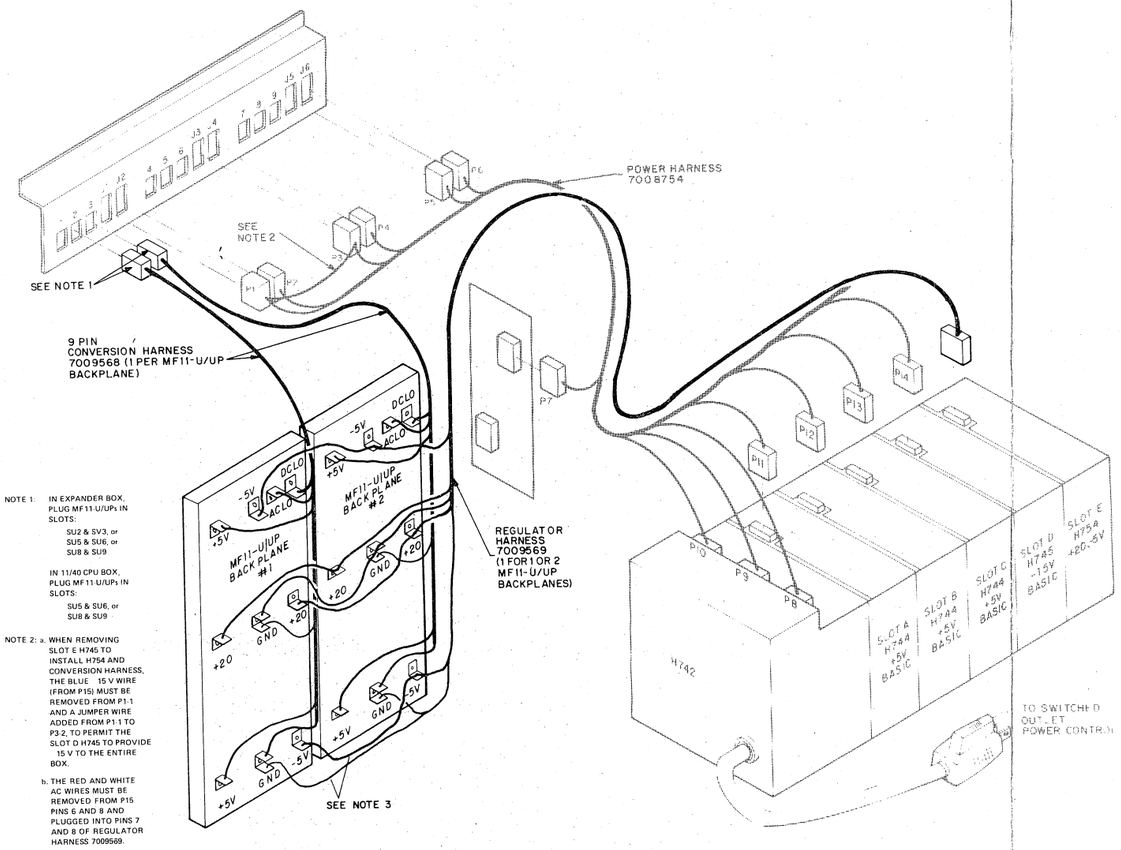


Figure 6-11 Power Distribution Schematic – Early Systems
(System Serial No. 5999 and lower)



NOTE 1: IN EXPANDER BOX, PLUG MF11-U/UPs IN SLOTS:
SU2 & SV3, or
SU5 & SU6, or
SU8 & SU9

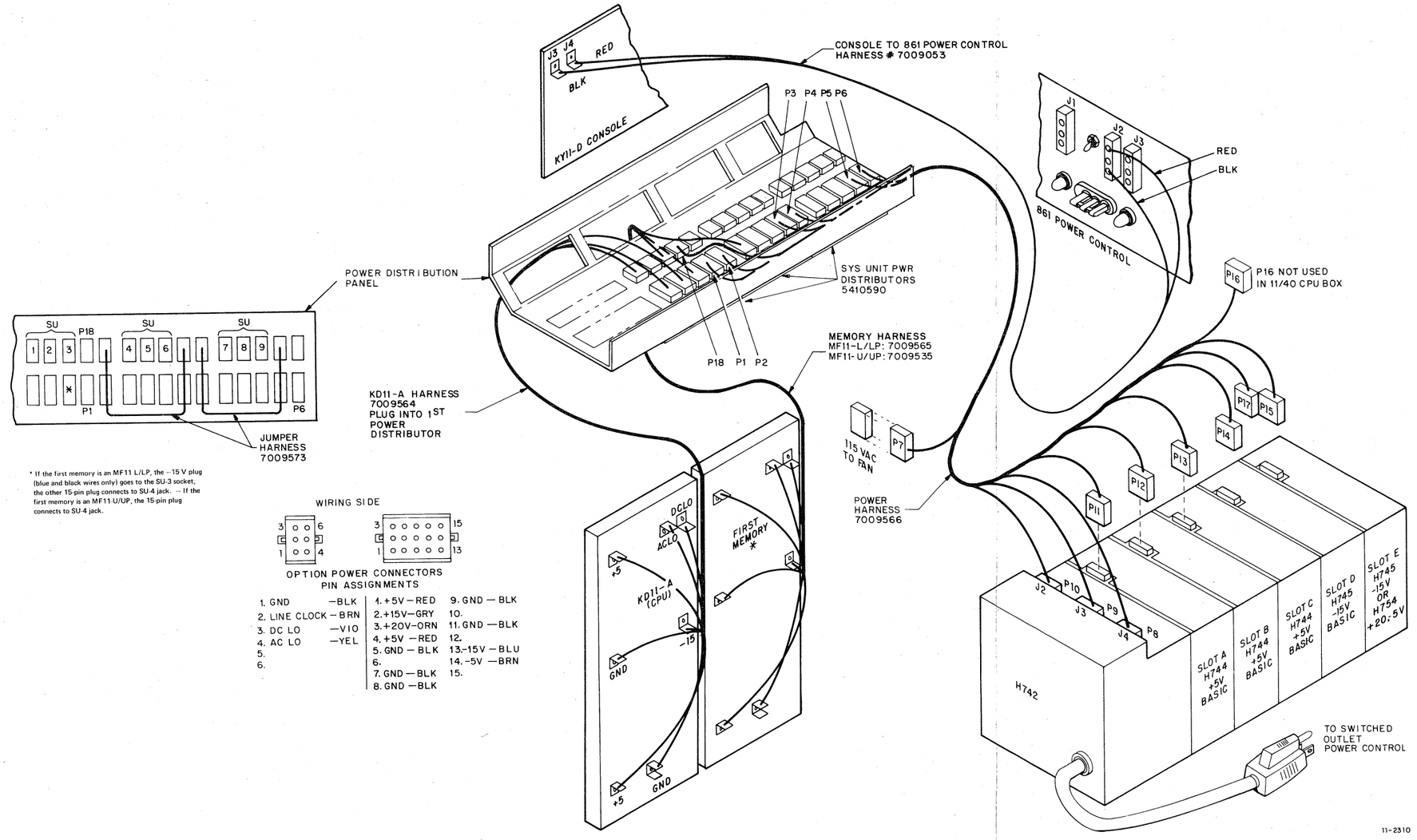
IN 11/40 CPU BOX, PLUG MF11-U/UPs IN SLOTS:
SU5 & SU6, or
SU8 & SU9

NOTE 2: a. WHEN REMOVING SLOT E H745 TO INSTALL H754 AND CONVERSION HARNESS, THE BLUE 15 V WIRE (FROM P15) MUST BE REMOVED FROM P1-1 AND A JUMPER WIRE ADDED FROM P1-1 TO P3-2, TO PERMIT THE SLOT D H745 TO PROVIDE 15 V TO THE ENTIRE BOX.

b. THE RED AND WHITE AC WIRES MUST BE REMOVED FROM P15 PINS 6 AND 8 AND PLUGGED INTO PINS 7 AND 8 OF REGULATOR HARNESS 7009569.

NOTE 3: IF ONLY ONE MF11-U/UP IS USED, CUT THE UNUSED JUMPER WIRES AT THE CONNECTOR TO PREVENT POSSIBLE SHORT CIRCUITS.

Figure 6-12 MF11-U/UP Installation – Early Systems



* If the first memory is an MF11 L/LP, the −15 V plug (blue and black wires only) goes to the SU-3 socket; the other 15-pin plug connects to SU-4 jack. − If the first memory is an MF11-U/UP, the 15-pin plug connects to SU-4 jack.

WIRING SIDE

OPTION POWER CONNECTORS
PIN ASSIGNMENTS

1. GND	—BLK	1. +5V — RED	9. GND — BLK
2. LINE CLOCK	— BRN	2. +15V — GRY	10.
3. DC LO	—VIO	3. +20V — ORN	11. GND — BLK
4. AC LO	—YEL	4. +5V — RED	12.
5.		5. GND — BLK	13. −15V — BLU
6.		6.	14. −5V — BRN
		7. GND — BLK	15.
		8. GND — BLK	

Figure 6-13 Power Distribution – Newer Unit with System Serial No. 6000 and Higher

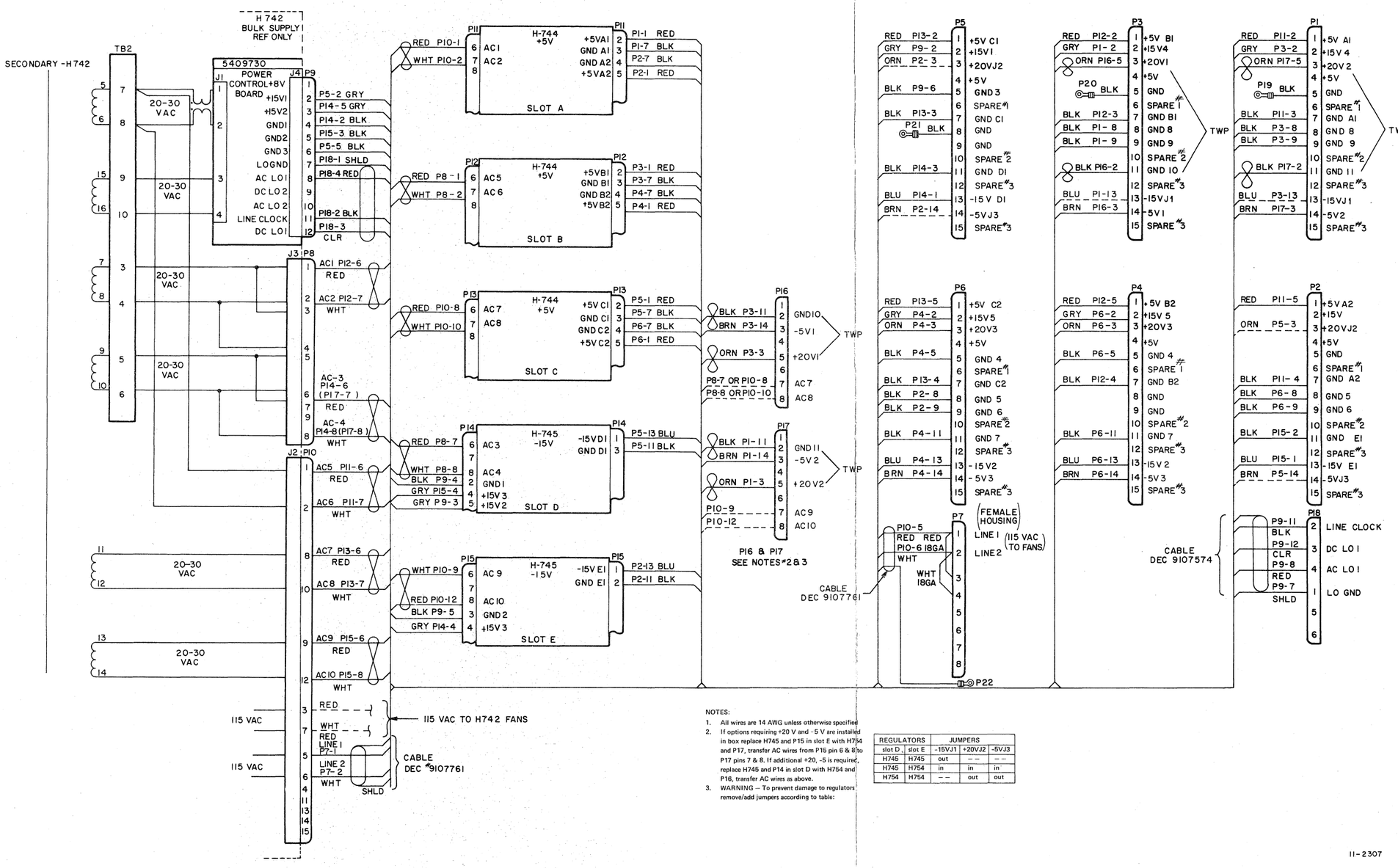


Figure 6-14 Power Distribution Schematic – Newer Systems (System Serial No. 6000 and Higher)

CHAPTER 7
GENERAL MAINTENANCE

7.1 SCOPE

This chapter provides general maintenance information for the PDP-11/40 System and includes: preventive maintenance of mechanical assemblies, diagnostic programs, system power checks, and power supply maintenance.

Maintenance information related to the processor and memory components of the basic PDP-11/40 System is presented in the associated maintenance manuals. Maintenance of Unibus peripherals requires not only the associated maintenance manual, but also an understanding of Unibus operation.

In addition to the maintenance information contained in the processor, memory, and peripherals manuals of the PDP-11/40, significant maintenance information is available in the diagnostic programs documentation. The diagnostic programs are a major tool for detecting and isolating machine faults, and preventive maintenance should include their regular use. Diagnostic programs are discussed in Paragraph 7.5.

7.2 OVERALL MAINTENANCE TECHNIQUES

Maintenance of the PDP-11/40 System requires:

- knowledge of proper hardware operation,
- ability to detect and isolate an error condition, and
- means to repair the error condition.

The above conditions are true for all but the preventive maintenance procedures for mechanical assemblies and for the relatively simple power check-out procedures. This section outlines techniques for performing maintenance on the PDP-11/40. Note, however, that the essential starting point is to have knowledgeable and capable service personnel.

7.2.1 Knowledge of Proper Hardware Operation

Training courses and machine documentation provide information on hardware operation and are available at the programming, systems, and individual device levels.

The training courses available for the PDP-11/40 System include:

PDP-11/40 Hardware Familiarization (10 days)
KD11-A Maintenance (3 days)
PDP-11/40 Options Maintenance (5 days)
Interfacing the PDP-11 (5 days)

Other courses are available on Paper Tape Software, Disk Operating System Software, and Resource Timesharing System Software. Information on these and other PDP-11 courses is available from either the Digital Account Representative or from the Digital Education Centers.

Documentation pertinent to the PDP-11/40 System includes documents produced specifically for the PDP-11/40, and common PDP-11 documents on programming and Unibus interfacing. All of the relevant documents are listed in Table 1-2.

A special effort has been expanded in production of documents relating to the PDP-11/40 processor (KD11-A) and processor options (KE11-E, KE11-F, KJ11-A, KW11-L, KM11-A, and KT11-D). Innovations include: print set formats, tables and notes on the prints, and wire list print notations. These are provided to facilitate initial learning but, more importantly, to provide instant reminders of specific details during maintenance. Information describing the print sets appears in the processor and options maintenance manuals.

7.2.2 Detection and Isolation of Error Conditions

Malfunctioning hardware is normally indicated by either software failure or peripheral malfunctions. Failures can occur with customer's system software or during the periodic operation of various MAINDEC diagnostic programs. If the failure occurs with system software, verification by MAINDEC diagnostic programs is suggested.

The PDP-11/40 maintenance philosophy requires that service personnel be well trained on the PDP-11/40 System and experienced in computer maintenance. While MAINDEC diagnostic programs are provided to isolate faults to a specific program operation or device, service personnel must fully understand hardware and software operation and system documentation to use the diagnostics effectively. This understanding can only come through training and experience.

Once the fault has been isolated to a device, the level of repair determines the difficulty and/or expense involved in making the repair. In the power system for example, regulator units such as the H744 or H745 are replaced if their output voltages are in error; the circuit board of the H742 unit is replaced if the AC LO or DC LO control signals are in error. Replacement of KD11-A Processor modules is suggested for situations requiring minimum downtime. While module replacement is usually the most expeditious method of repair, experienced service personnel may find integrated circuit (IC) replacement a practical alternative to the cost or transportation of modules.

7.2.3 Means of Repairing Error Conditions

The method of repairing an error condition is directly related to the levels of fault isolation mentioned in the previous paragraph. If, for example, fault isolation and repair is to be at the IC level, then the parts identified in the machine documentation must be available and suitable repair and rework techniques must be followed to avoid equipment damage. If module or subassembly level of fault isolation and repair is to be used, these modules and subassemblies must be available. Spare part kits are available for the PDP-11/40 (SP11-KF for processor and SP11-PD for the power supply) and the various Unibus devices. Repair is normally at the module or subassembly level when downtime is critical or when a large number of machines are involved.

NOTE

Memory module replacement may require readjustment of the strobe delay. Refer to *MM11-S, MF11-L, and MF11-LP Core Memory System,* EK-MM11S-TM-003 for adjustment procedure.

Verification of repair at any level is made by running the appropriate MAINDEC diagnostic programs.

7.2.4 Digital Field Service

The present state-of-the-art in complex computer systems requires qualified service personnel. Installation and 90-day warranty service are provided by such personnel from Digital Field Service. These people are trained both in basic PDP-11/40 components (processor, console, and memory) and in peripherals that may be placed on the Unibus. Material support exists both at the IC level (directly equivalent parts) and at the module and subassembly level.

Digital Field Service support may be continued beyond the warranty period with a Digital Service Agreement. Total equipment maintenance programs are available. Details of this service may be obtained from the Digital Account Representative at the local Field Service Office.

7.3 MAINTENANCE EQUIPMENT REQUIRED

Maintenance procedures for the PDP-11/40 require the standard equipment (or equivalent) listed in Table 7-1. Especially important in analyzing operation of the processor, or processor options, is the KM11 option consisting of the W131 Module and the W130 or W133 module and associated overlays. Use of the KM11 maintenance displays and switches is covered in the processor and processor options maintenance manuals. The module extender board (W900) is also an important diagnostic tool and is discussed in Paragraph 7.6.

7.4 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks performed periodically; its major purpose is to prevent future failures caused by minor damage or progressive deterioration due to aging. Any equipment defects or deterioration detected during preventive maintenance checks should be documented in a maintenance log book. This maintenance log, compiled over an extended period of time, can be very useful in anticipating possible component failures, resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to conditions at the particular installation site such as environmental conditions, usage, etc. Mechanical checks should be performed as often as required to allow the fans and air filters to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 1000 operation hours or every three months, whichever occurs first.

7.4.1 Physical Checks

The following procedure contains the necessary steps required for mechanical checks and physical care of the PDP-11/40:

1. Clean the exterior and interior of the cabinet with a vacuum cleaner or a clean cloth moistened with nonflammable, noncorrosive solvent.

2. Ensure that the fans are not obstructed in any way. Vacuum clean the air vents of the upper and lower logic fan housings, and upper and lower regulator fan housings. Remove and wash the filters in the cabinet fan, located in the top of the cabinet.

3. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering.

4. Inspect the following for mechanical security: LED or lamp assemblies, jacks, connectors, switches, power supply regulators, fans, capacitors, etc. Tighten or replace as required.

5. Inspect all module mounting panels; ensure that each module is securely seated in its connector and the locking-releasing mechanism is functioning properly.

6. Inspect power supply capacitors for leaks, bulges, or discoloration and replace as required.

7. Inspect module guides for wear, damage, and secure fastening.

7.4.2 Electrical Checks and Adjustments

Make the following checks when the system is first installed and whenever a new component is installed in the system (such as an additional regulator, processor option module, interface module, etc.).

Table 7-1
Maintenance Equipment Required

Equipment or Tool	Manufacturer	Model, Type, or Part No.	DEC Part No.
Oscilloscope	Tektronix	453*	
Volt/Ohmmeter (VOM)	Triplett		29-13510
Unwrapping Tool	Gardner-Denver (Cat. H812A)	505 244-475	29-18387
Hand Wrap Tool	Gardner-Denver (Cat. H811A)	A-20557-29	29-18301
Diagonal Cutters	Utica	47-4	29-13460
Diagonal Cutters	Utica	466-4 (modified)	29-19551
Miniature Needle Nose Pliers	Utica	23-4-1/2	29-13462
Wire Strippers	Millers	101S	29-13467
Solder Extractor	Solder Pullit	Standard	29-13467
Soldering Iron (30 watts)	Paragon	615	29-13452 (IC type head)
Soldering Iron Tip	Paragon	605	29-19333
16-pin IC Clip	AP Inc.	AP923700	29-10246
24-pin IC Clip	AP Inc.	AP923714	29-19556
KM11 Option Maintenance Console Modules	DEC	KM11-A	W131 and W130 or W133**
Maintenance Card Overlay (KD11-A)	DEC		559081-0-12
Maintenance Card Overlay (KE11-E, F, KT11-D)	DEC		5509081-0-13
Module Extender Board	DEC		W900
Regulator Extender Cable	DEC		70-08850-0-1

*Tektronix Type 453 Oscilloscope is adequate for most test procedures;Type 454 (or equivalent) may be required for some measurements.

**W133 is a dual version of W130. It provides the drivers for two W131 maintenance cards. The W130 may still be used, but two units would be required for simultaneous monitoring of the basic processor and options. Two W131s are required for simultaneous monitoring in any case.

7.4.2.1 Processor Clock Adjustment Check – Perform the processor clock adjustment according to the clock adjustment procedure on the KD11-A timing module (M7234) print K4-2.

7.4.2.2 Voltage Regulator Checks – Perform the power system checks listed in Table 7-2. Use a VOM to check the output voltages under normal load conditions at logic backplanes. Use an oscilloscope to measure the peak-to-peak ripple content of all dc outputs. Each voltage regulator has an adjustment potentiometer located just below the output indicator lamp. If the regulator output is not within the specified tolerance, adjust as required to obtain an acceptable output (use a nonconducting adjustment tool). If a voltage regulator cannot be adjusted to meet specifications, remove and replace the regulator.

Table 7-2
DC Output Voltages

Regulator	Slots	Voltage and Tolerance	Output Current (max)	Ripple
H744	A,B,C	+5 Vdc ± 5%	25A	200 mV
H745	D,E	-15 Vdc ± 5%	10A	450 mV
H754	D,E	+20 Vdc ± 5% -5 Vdc ± 5%	8A 1A	——— ———
H742	———	+15 Vdc ± 10% +8 Vdc ± 15% 20–30 Vac (5 outputs)	3A } (1) 1A } 300W ea output, 1 kW max. total output	——— ———

Note 1: Total not to exceed 3A continuously.

7.4.2.3 861 Power Controller – Operate the REMOTE/OFF/LOCAL switch on the 861 Power Controller to verify that power is turned on in the LOCAL position and disconnected in the OFF position. Return the switch to the REMOTE position after performing this test. Paragraph 6.4 references a detailed description of the 861 Power Controller.

7.4.2.4 AC Power Connector Receptacles – Test the output voltage at each plug and ensure that 115 or 230 Vac power is available.

7.4.3 ASR 33 Teletype

7.4.3.1 Preventive Maintenance Checks – Check the following ASR 33 items during system preventive maintenance:

a. Check distributor plates for deposits.

b. Check platen and typewheel for deposits.

c. Check wires around distributor area for secure mechanical and electrical connections.

d. Check the print hammer and replace if worn.

e. Rotate the mainshift manually and check that movement is free. If movement is restricted, check clutch assemblies.

f. Check typewheel pinion racks, and gears for dirt.

7.4.3.2 Lubrication – Use a 50-50 mixture of 20 weight, non-detergent oil and STP oil additive for viscosity improvement to perform the following lubrication, except where otherwise noted:

a. Oil all clutch assemblies.

b. Oil all felts until saturated.

c. Lightly oil all pivot points.

d. Oil drive motor at both lubrication points provided.

e. Oil print carriage bearings.

f. Oil main shaft bearings.

g. Oil bearing on function shaft.

h. Oil the eye ends of all springs.

i. Oil the typewheel pinion and gear.

j. Oil repeat mechanism in keyboard assembly.

k. Clean the dashpot assembly and lubricate it with graphite dust.

NOTE
Do not put oil in the dashpot.

l. Grease the teeth on spacing ratchet.

7.4.4 LA30 DECwriter Preventive Maintenance

A maintenance manual is provided with the LA30 DECwriter. Refer to Chapter 5 of that manual for detailed preventive maintenance procedures.

7.4.5 PC05 High-Speed Paper-Tape Reader/Punch Option

The PC05 High-Speed Paper-Tape Reader/Punch includes a Roytron 500 Series Reader/Punch mechanism. Complete lubrication and preventive maintenance instructions for this mechanism are contained in the Preventive Maintenance Section of the *Roytron Maintenance Manual,* which is supplied with the PC05. In addition to the preventive maintenance procedures listed in that manual, perform the following mechanical and electrical checks as part of the system preventive maintenance procedure.

7.4.5.1 Mechanical Checks – Inspect the PC05 as follows:

1. Visually inspect the general condition of the tape reader.

2. Clean the PC05, inside and out, using a vacuum cleaner or a clean cloth moistened with a nonflammable solvent.

3. Lubricate the chassis slide mechanism with a light machine oil. Wipe off excess oil.

4. Inspect all wiring and replace any defective wiring or defective cables.

5. Check that the READER FEED switch, READER ON/OFF LINE switch light condenser, phototransistor assembly, depressor arm, hold-down bracket, all connectors and circuit modules, tape feed motor, front cover, and resistor assembly are mechanically secure.

7.4.5.2 **Electrical Checks** – Perform power supply output tests listed in the following chart:

Output	Pin Number	Tolerance	Ripple (peak-to-peak V)
+5V	A1A2	±0.25V	0.1V
-15V	A1B2	±1.0V	0.1V
-18V	B8V2	±2.0V	1.0V
-36V	A8V2	+4.0V	1.0V

Use a VOM to measure output voltage and an oscilloscope to check ripple voltage. The +5 and -15V outputs are adjustable; the -18 and -36V outputs are not adjustable.

7.5 DIAGNOSTIC PROGRAMS

7.5.1 General Description

The following groups of diagnostic programs are applicable to the basic PDP-11/40 System and options:

a. PDP-11/40 System Diagnostics

b. KD11-A Processor Diagnostics

c. Core Memory Diagnostics

d. KE11-E Extended Instruction Set Diagnostics

e. KE11-F Floating Instruction Set Diagnostics

f. KT11-D Memory Management Diagnostics

g. KJ11-A Stack Limit Register Diagnostic

h. KW11-L Line Frequency Clock Diagnostics

Diagnostic programs for peripherals and I/O devices in the system are listed and described in their associated maintenance manuals. Detailed descriptions and specific operating procedures for each diagnostic program are provided in related diagnostic program description (MAINDEC) documentation.

Generally, all diagnostic programs are loaded into the lowest 4K words of physical memory. All diagnostic programs start at address 200_8 and run in kernel mode.

Any trap or interrupt vectors not used by the test in progress are set up as "trap catchers"; the new Program Counter (PC), stored in the first word of the vector, points to the second word of the vector, which contains a 0. When the 0 is fetched as an instruction, the processor interprets it as a HALT instruction. The instruction being executed when the trap occurred can be identified as follows:

1. Examine R6 (777706).

2. Set the number found in R6 in the Switch register and do a LOAD ADRS operation.

3. Do an EXAM operation to determine the contents of the top word in the stack. This is the PC at the time the false trap/interrupt occurred.

4. Generally, the PC is pointing at the instruction following the instruction that caused the trap or interrupt. Use this value and the program listing to determine the instruction being executed when the trap or interrupt occurred.

The available diagnostic programs are listed in Table 7-3.

Table 7-3
PDP-11/40 Diagnostic Programs

Title	Code
System Exercisers	
Communications Test Program (CTP)	MAINDEC-11-DZQCA-
General Test Program (GTP)	MAINDEC-11-DZQGA-
System Sizer	MAINDEC-11-DZSSA-
Processor Test 17 System Exerciser	MAINDEC-11-DZQKB-
Processor Tests	
Processor Test 14 Traps	MAINDEC-11-DBKDM-
– PDP-11/40, 11/45 Instruction Exerciser	MAINDEC-11-DCQKC-
Processor Power Fail Test	MAINDEC-11-DZKAQ-A-
PDP-11/40 Basic CP Test SXT	MAINDEC-11-DCKBA-
PDP-11/40 Basic CP Test SOB	MAINDEC-11-DCKBB-
PDP-11/40 Basic CP Test XOR	MAINDEC-11-DCKBC-
PDP-11/40 Basic CP Test MARK	MAINDEC-11-DCKBD-
PDP-11/40 Basic CP Test RTT	MAINDEC-11-DCKBE-
Memory Tests	
– 0–124 Memory Exerciser	MAINDEC-11-DZQMB-
CPU Parity Test*	MAINDEC-11-DBKBR-
KE11-E (EIS) Option Tests	
PDP-11/40 Basic CP Test ASH	MAINDEC-11-DCKBI-
PDP-11/40 Basic CP Test ASHC	MAINDEC-11-DCKBJ-
PDP-11/40 Basic CP Test MUL	MAINDEC-11-DCKBK-
PDP-11/40 Basic CP Test DIV	MAINDEC-11-DCKBL-
MUL-DIV Random Exerciser	MAINDEC-11-DCQKA-

*Use only with parity memory systems.

Table 7-3 (Cont)
PDP-11/40 Diagnostic Programs

Title	Code
KE11-F (FIS) Option Tests	
KE11F Instruction Tests	MAINDEC-11-DBKEA-
KE11F Exerciser	MAINDEC-11-DBKEB-
KE11F Systems Exerciser (GTP) Overlay	MAINDEC-11-DBKEO-
KT11-D Memory Management Option Tests	
KT11D Basic Logic Test	MAINDEC-11-DBKTA-
KT11D Access Keys Test	MAINDEC-11-DBKTB-
MTPI/MFPI with Memory Management Test	MAINDEC-11-DBKTC-
KT11D Processor States Test	MAINDEC-11-DBKTD-
Memory Management Abort Tests	MAINDEC-11-DBKTF-
KT11D Exerciser	MAINDEC-11-DBKTG-
KJ11-A Stack Limit Register Option Test	
PDP-11/40 Basic CP Test Stack Limit	MAINDEC-11-DCKBF-
KW11-L Line Frequency Clock Test	MAINDEC-11-DZKWA-
LA30 Serial – 300 baud	MAINDEC-11-DZLAB-
KL11/DL11A Teletype Tests	MAINDEC-11-DZKLA-
1s and 0s Test Tape	MAINDEC-00-D2G2-PT
Special Binary Count Pattern Tape	MAINDEC-00-D2G4-PT
Maintenance Loader	MAINDEC-11-D9EA-

7.5.2 Diagnostic Program Utilization

Diagnostic programs are designed to facilitate maintenance of the PDP-11/40 System and its options. Their specific purpose is to aid in the definition and isolation of error conditions; this is accomplished in greater detail than is possible with system operational software.

There is a definite order in which diagnostics should be run. When problems occur or are suspected, a system type exerciser (GTP or CTP) should be run to isolate the failure to a specific Unibus device. Once the fault is isolated to a specific Unibus device, the programs designed to checkout that device should be run. This naturally assumes that programs can be loaded and run.

Relative to the PDP-11/40 processor, an effort has been made to correlate a specific diagnostic program error with a particular module failure. Table 7-4 correlates the processor and processor option diagnostic programs to the modules most likely to be at fault in the event an error is detected. The diagnostics are listed in the order they should be run (top to bottom), and the modules are listed in the order of failure probability (left to right). The percentage of failure probability is also noted. Be advised that Table 7-4 presents the initial effort to correlate diagnostic programs to specific module failures and should not be considered an absolute error indicator.

Table 7-4
PDP-11/40 Processor Preliminary
Diagnostic Program Error Analysis

	Module Replacement									
Diagnostics*	1st	Prob. (%)	2nd	Prob. (%)	3rd	Prob. (%)	4th	Prob. (%)	5th	Prob. (%)
Test 1 Branch	M7232	30	M7233	30	M7231	10	M7235	10	M7234	10
Test 2 Con Branch	M7235	80	M7233	5	M7231	5				
Test 3 Unary	M7233	60	M7235	30						
Test 4 Unary & Binary	M7233	50	M7232	50						
Test 5 Rotate/Shift	M7232	45	M7233	45						
Test 6 Compare	M7232	45	M7233	45						
Test 7 Compare NOT	M7232	45	M7233	45						
Test 8 Move	M7232	80	M7233	15						
Test 9 BIS, BIC, and BIT	M7232	45	M7233	45						
Test 10 ADD	M7232	45	M7233	45						
Test 11 Subtract	M7232	45	M7233	45						
Test 12 JMP	M7232	45	M7233	45						
Test 13 JSR, RTS, RTI	M7232	70	M7235	15	M7233	8				
SXT Instruction	M7232	90	M7233	8						
SOB Instruction	M7232	90	M7233	8						
XOR Instruction	M7232	90	M7233	8						

Table 7-4 (Cont)
PDP-11/40 Processor Preliminary
Diagnostic Program Error Analysis

	Module Replacement									
Diagnostics*	1st	Prob. (%)	2nd	Prob. (%)	3rd	Prob. (%)	4th	Prob. (%)	5th	Prob. (%)
MARK Instruction	M7232	90	M7233	8						
RTT Instruction	M7232	90	M7233	8						
Test 14 Traps Test	M7232	80	M7234	10	M7233	5				
KJ11-A Stack Limit Option Test	M7237	90	M7231	5						
KE11E Option Tests**	M7238	90	M7232	3	M7233	3				
KE11F Option Tests**	M7238	70	M7239	20	M7231	4	M7233	4		
Test 18 Power Fail	M7235	80	M7234	10						
Test 15 11 Family Instruction Test	M7232	55	M7233	35						

*See Table 7-3 for diagnostic program complete title and code. Tests 1–13 are listed primarily for reference purposes. These diagnostics are not part of the standard set (LIBKIT-11/40-BASE-A-K, August 22, 1973), but may be purchased on special order.

**This test consists of several separate diagnostics. See Table 7-3 for complete listing.

7.6 USE OF MODULE EXTENDERS

The W900 Module Extender is a double-height, multi-layer etch board that provides one-to-one connections between module connectors and corresponding processor backplane connector slots. Thus, three W900 Module Extenders can be used to extend a PDP-11/40 hex-size module from the processor backplane to provide access to ICs and discrete components for test purposes under active operating conditions.

CAUTION

Do not attempt to extend more than one module at a time while performing tests. Note that the processor clock may have to be adjusted to allow operation with the modules extended. See processor timing module (M7234) print K4-2 for clock adjustment procedure.

7.7 PDP-11/40 POWER SYSTEM MAINTENANCE

WARNING

Dangerous voltages (115/230 Vac) are present in the power system. All electrical safety precautions must be observed.

For the most part, maintenance of the power system in the field consists of replacing defective modules, such as voltage regulators. Paragraph 6.4 provides the theory operation of the power system. When a failure occurs, the recommended troubleshooting approach is to visually inspect the power system and then, if necessary, check voltages at specific points in the power system to isolate the fault to a particular module.

7.7.1 Visual Inspection

If a power system fault is suspected, visually inspect the system components for obvious fault indications. For example, each of the voltage regulator modules is provided with an output indicator lamp that is on when the output voltage is within range. If a single indicator lamp within the group is off, the fault is probably within that voltage regulator module. In the case of the H744 +5V Regulator, this can be verified by swapping H744 regulators.

CAUTION

Because there are two +5V and two −15V regulators in the PDP-11/40 System, a common troubleshooting technique would be to swap an operating regulator with a faulty regulator. If this is done, first check regulator input voltages to prevent damage to the second regulator in the event the fault lies in the H742 Power Supply.

If none of the voltage regulator output indicator lamps in the group are on, the fault is probably in the associated H742 Power Supply or 861 Power Controller. Visually inspect the power indicator lamps and circuit breakers provided with these components to determine whether the fault can be isolated to either the H742 or the 861.

7.7.2 Power System Checks

Table 7-5 provides a procedure that can be used as a guide to locating defective modules.

Table 7-5
Power System Troubleshooting Guide

Step	Test	Procedure	Results
1	Verify that proper ac voltage input to H742 Power Supply is present.	115V system – measure between pin 1 or 2 and pin 3 or 4 of TB1 on H742 Power Supply. 230V System – measure between pin 1 and 4 of TB1.	Correct – proceed to step 2. Incorrect – indicates failure may be in 861 Power Controller or input line. Refer to Chapter 5 of the *861-A, B, C Power Controller Manual* and troubleshoot the 861 Power Controller.
2	Verify that H742 Power Supply is providing the proper ac outputs.	20–30 Vac should be present on the following pins: J1 – pins 1, 2 J2 – pins 1, 2 J2 – pins 8, 10 J2 – pins 9, 12 J3 – pins 1, 2 J3 – pins 3, 4 J3 – pins 5, 6 J3 – pins 7, 8 15–24 Vac should be present between pins 3 and 4 of J1.	Correct – proceed to step 3. Incorrect – indicate failure of H742 transformer. If all voltages are correct except one, problem could be either transformer secondary or a wiring malfunction.
3	Verify that the proper input voltage is present at the regulator.	+5V Regulator – check for 20–30 Vac at pins 6 and 7 of J1. -15V Regulator – check for 20–30 Vac at pins 6 and 8 of J1. Check for +15V at pins 4, 5 of J1. +20, -5V Regulator – check for 20–30 Vac at pins 7 and 8 of J1.	Correct – proceed to step 4. Incorrect – indicates failure is probably in the wiring between the H742 and the regulator. If the +15V for the -15V regulator is not present, the trouble may be in the H742 Power Control Board.

Table 7-5 (Cont)
Power System Troubleshooting Guide

Step	Test	Procedure	Results
4	Verify that proper output voltage is being produced by the regulator.	+5V Regulator – measure between pins 2, 5 (+5) and 3, 4 (GND) of J1. Output must be between +5.05 and +4.95V. -15V Regulator – measure between pin 1 (-15V) and pins 2, 3 (GND) of J1. Output must be between -15.15 and -14.85V. Backplane voltage measurement with proper voltmeter is occasionally necessary. +20, -5V Regulator – a. Measure between pins 5 (+20V) and 2 (GND). Output must be between +19 and +21V. b. Measure between pins 3 (-5V) and 2 (GND). Output must be between -4.75 and -5.25V.	Correct – check remaining regulators. If all regulators are within tolerance, the power system is not malfunctioning and the problem exists elsewhere. Incorrect – If the +5V regulator is not functioning, check fuse F1 in the regulator. If the -15V regulator is not functioning, check fuse F1 in the regulator. If this does not correct the problem, replace the respective regulator.

APPENDIX A
SUMMARY OF EQUIPMENT SPECIFICATIONS

This table gives mechanical, environmental, and programming information for PDP-11 optional equipment. The equipment is arranged in alphanumeric order by Model Number.

NOTES

1. Mounting Codes

   CAB = Cabinet mounted. If a cabinet is included with the option, it is indicated by an X in the "Cab Incl" column.

   FS = Free standing unit. Height X Width X Depth dimensions are shown in inches.

   TT = Table top unit.

   PAN = Panel mounted. Front panel height is shown in inches. An included cabinet is indicated when applicable.

   SU = System Unit. SU mounting assembly is included with the option.

   SPC = Small Peripheral Controller. Option is a module that mounts in a quad module, SPC slot.

   MOD = Module. Height is single, double, or quad.

   ( ) = Option mounts in the same space as the equipment shown within the parentheses.

   Some options include 2 separate physical parts and are indicated by use of a plus (+) sign.

2. Cabinet and peripheral equipment (such as magnetic tape) are included in the specifications.

3. Relative humidity specifications mean without condensation.

4. Equipment that can supply current is indicated by parentheses ( ) around the number of amps in the POWER section. *MEMORY POWER:* MF11- and MM11- require the same amount of power. In this table, MF11- power figures show the power required when the memory is active, while MM11- figures reflect that required by an inactive unit.

5. Non-Processor Request devices are indicated by an X in the "NPR" column.

6. 7008855 in 11/45-11/50 CPU; 7008909 in H960-D and 11/40.

7. 7009174. If first MF11-L in 11/40, use 7009103.

8. 7009560. If first MF11-L in 11/40, use 7009565.

9. H960-C, D only (not CPU Cabinet): one 7009568 per backplane (9 pin conversion) and one 7009569 for two backplanes (regulator harness).

CONVERSION FACTORS

(inches)	X 2.54	= (cm)
(lbs)	X 0.454	= (kg)
(Watts)	X 3.41	= (Btu/hr)
$[(^{\circ}C) \times \frac{9}{5}] + 32$		= ($^{\circ}F$)

Model Number	Description	MECHANICAL: Mounting Code	Size H X W X D (inches)	Cab Incl	Weight (lbs)	Power Harness: Early	Power Harness: New	ENVIRONMENTAL: Oper Temp (°C)	Rel Humid (%)	POWER: Cur needed/(supplied) +5 V	115 Vac / Other (amps)	Power Dis (W)	PROGRAMMING: 1st Reg Address	Int Vector	UNIBUS: BR Level	NPR	Bus Loads	Model Number
AA11-D	D/A Subsystem	SU				Note 6	7009562	10–50	20–95	3	0.5	60	776 756	140,144	4,5		1	AA11-D
AD01-D	A/D Subsystem	PAN	5¼					0–55	10–95		0.5	60	776 770	130	4–7		1	AD01-D
AFC11	A/D Subsystem	CAB						10–55	10–95		15	1700	772 570	134	4		1	AFC11
BA11-ES	Mounting Box	PAN	10½		100													BA11-ES
BA614	D/A Converter	(AA11-D)																BA614
BB11	Blank Mntg Panel	SU																BB11
BB11-A	Blank Mounting Panel (non-slotted blocks)	SU																BB11-A
BC11A	UNIBUS Cable																	BC11A
BM792-Y	Bootstrap Loader	SPC								0.3							1	BM792-Y
CB11	Telephone Switching Interface	Cab		X	300			10–50	10–90		5.6	650	764 000	float	4–7		1,2	CB11
CD11-A	Card Reader	SU + TT	14 X 24 X 18		85	Note 6	7009562	10–50	10–90	2.5	4	450	772 460	230	4	X	1	CD11-A
CD11-E	Card Reader	SU + TT	38 X 24 X 38		200	Note 6	7009562	10–50	10–90	2.5	6	700	772 460	230	4	X	1	CD11-E
CM11-F	Card Reader	SPC + TT	11 X 19 X 14		60			10–50	10–90	1.5	4	400	777 160	230	6		1	CM11-F
CR11	Card Reader	SPC + TT	11 X 19 X 14		60			10–50	10–90	1.5	4	400	777 160	230	6		1	CR11
DA11-B	UNIBUS Link	SU				Note 6	7009562			4			772 410	124	5	X	1	DA11-B
DA11-F	UNIBUS Window	SU				7009099	7009563			5				float	7	X	1	DA11-F
DB11	Bus Repeater	SU				Note 6	7009562	5–50	10–95	3.2							1 + 1	DB11
DC11-A	Asynch Line Inter	SU				Note 6	7009562	10–50	20–90		see Product Bull.		774 000	float	5		1	DC11-A
DD11	Periph Mntg Panel	SU				7009099	7009563											DD11-A
DECkit 01-A	Remote Analog Data Concentrator: 8 Channels, Serial	PAN	5¼ X 19 X 13		15			0–50	10–95		1.5 @ 115 Vac 0.75 @ 230 Vac	175						DECkit 01-A
DECkit 11-F	I/O Interface: 3 Words In/4 Words Out	SU				Note 6		0–70	10–95	1.84			User	User	7		4	DECkit 11-F
DECkit 11-H	I/O Interface: 4 Words In/4 Words Out	SU				Note 6		0–70	10–95	3.91			User	User	5–6		4	DECkit 11-H
DECkit 11-K	I/O Interface: 8 Words In	SU				Note 6		0–70	10–95	1.97			User				2	DECkit 11-K
DECkit 11-M	I/O Interface: Instrumentation Interface	SU				Note 6		0–70	10–95	1.75			User	User	4		2	DECkit 11-M
DF01-A	Acoustic Coupler	TT	6 X 7 X 12		6			0–60			0.3							DF01-A
DF11	Line Sig Cond	DF slot									see Product Bull.							DF11
DH11	Asynch Line MX	2 SU				7009466	7009561	5–45	10–95	8.4	0.24 A @ -15 V		float	float	5	X	2	DH11
DJ11	Asynch Line MX	SU				7009099	7009563			5	see Product Bull.		float	float	5		1	DJ11
DL11-A	Terminal Control	SPC								1.8	0.15 A @ -15 V		777 560	060,064	4		1	DL11-A
DL11 (others)	Asynch Line Inter	SPC								1.8	0.15 A @ -15 V		776 500	float	4		1	DL11 (others)
DM11-BB	Modem Ctr. MUX	(DH11)								2.8			775 000	float			1	DM11-BB
DN11	Auto Calling Unit	SU				Note 6	7009562	0–40	20–90	1.4	0.10 A @ ± 15 V		775 200	float	4		1	DN11
DP11	Synch Line Inter	SU				Note 6	7009562	0–40	20–90	2.5	0.10 A @ ± 15 V		774 400	float	5		1	DP11
DQ11	DMA Sync Line Interface	SU				7009099	7009563	10–50	10–90	5.7	0.04 A @ +15 V 0.07 A @ -15 V		float	float	5	X	1	DQ11
DR11-B	DMA Interface	SU				Note 6	7009562	10–50	20–90	3.3			772 410	124	5	X	1	DR11-B
DR11-C	General Interface	SPC						10–50	20–90	1.5			767 770	float	5		1	DR11-C
DT03-F	UNIBUS Switch	PAN	5¼								2			user	7		1 + 1	DT03-F
DX11	IBM Chan. Interface	CAB		X	180			10–55	10–90		2.5	300	776 200	float	4–7	X	1	DX11-B
GT40	Graphics Terminal	TT	18 X 20 X 24		150			15–35	20–80		15	1500	float	float			1	GT40

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER				PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size (H X W X D) (inches)	Cab Incl	Weight (lbs)	Power Harness Early	Power Harness New	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V (amps)	Cur needed/(supplied) 115 Vac / Other (amps)		Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
H312-A	Null Modem																		H312-A
H720-E	Power Supply	(BA11)			30			0–50	20–95	(22)	6	(10A) @ -15 V	700						H720
H722	Transformer	(PC11-A)										1.5 A @ 230 Vac							H722
H742	Power Supply	(H960-D)									8	(1 A) @ +15 V							H742
H744	+5 V Regulator	(H742)								(25)									H744
H745	-15 V Regulator	(H742)										(10 A) @ -15 V							H745
H746	MOS Regulator	(H742)										(1.6 A) @ 23.2 V (3.3 A) @ 19.7 V (1.6 A) @ -5 V							H746
H754	+20, -5 V Regulator	(H742)										(8 A) @ +20 V (1 A) @ -5 V							H754
H933-C	Mounting Panel (H803 blocks)	SU																	H933-C
H933-D	Mounting Panel (H808 blocks)	SU																	H933-D
H960-C	Cabinet	FS	72 X 21 X 30	X	120														H960-C
H960-D	Cab (1 drawer)	FS	72 X 21 X 30	X	300	7008754	7009566			(75)	8	(20 A) @ -15 V	900						H960-D
H960-E	Cab (2 drawers)	FS	72 X 21 X 30	X	470	7008754	7009566			(150)	16	(40 A) @ -15 V	1800						H960-E
H961-A	Cab w/o side pan	FS	72 X 21 X 30	X	120														H961-A
KE11-A	Ext. Arith. Elem.	SU				Note 6	7009562			4				777 300				1	KE11-A
KG11-A	Comm Arith Unit	SPC								1.5				770 700				1	KG11-A
KW11-L	Line Clock	MOD	single ht							0.8				777 546	100	6		1	KW11-L
KW11-P	Programmable Clock	SPC								1				772 540	104	6		1	KW11-P
LA30	DECwriter	FS	31 X 21 X 24		110			15–35	20–80		3		300						LA30
LC11-A	LA30 Control	SPC								1.5				777 560	060,064	4		1	LC11-A
LP11-F	Printer (80 col)	SPC + FS	46 X 24 X 22		200			10–43	15–80	1.5	2		250	777 514	200	4		1	LP11-F
LP11-J	Printer (132 col)	SPC + FS	46 X 48 X 25		575			10–43	15–80	1.5	4		500	777 514	200	4		1	LP11-J
LP11-R	Ptr (heavy duty)	SPC + FS	48 X 49 X 36		800			10–43	15–80	1.5	17		2000	777 514	200	4		1	LP11-R
LPS11	Lab Periph System	PAN	5¼		80			5–43	20–80		3		300	float	float	4–6	opt	2	LPS11-S
LS11	Line Printer	SPC + TT	12 X 28 X 20		155			5–38	5–90	1.5	3		300	777 514	200	4		1	LS11
LT33	Teletype	FS	34 X 22 X 19		60			15–35	20–80		2		200						LT33
LV11	Electrostatic Ptr	SPC + FS	38 X 19 X 18		160			10–43	20–80	1.5	5		600	777 514	200	4		1	LV11
M105	Adrs Select Module	MOD	single ht							0.34									M105
M783	Bus Transmitter	MOD	single ht							0.2									M783
M784	Bus Receiver	MOD	single ht							0.2									M784
M785	Bus Transceiver	MOD	single ht							0.3									M785
M792	Diode ROM	SPC								0.23				773 000				1	M792
M795	Word Count	MOD																	M795
M796	Bus Control	MOD																	M796
M920	Bus Jumper	MOD																	M920
M930	Bus Terminator	MOD	double ht							1.25									M930
M1501	Bus Input Interface	MOD	single ht					0–70	10–95	0.3									M1501
M1502	Bus Output Interface	MOD	double ht					0–70	10–95	0.75									M1502
M1621	DVM Data Input Interface	MOD	quad ht					0–70	10–95	0.78									M1621
M1623	Instrument Remote Control Interface	MOD	quad ht					0–70	10–95	1.6									M1623
M1710	Unibus Interface Foundation	MOD & SPC	quad ht					0–70	10–95	0.79							opt		M1710
M1801	16-Bit Relay Output Interface	MOD	quad ht					0–70	10–95	1.46									M1801

Model Number	Description	MECHANICAL: Mounting Code	Size (H X W X D) (inches)	Cab Incl	Weight (lbs)	Power Harness: Early	Power Harness: New	ENVIRONMENTAL: Oper Temp (°C)	ENVIRONMENTAL: Rel Humid (%)	POWER: Cur needed/(supplied) +5 V (amps)	POWER: Cur needed/(supplied) 115 Vac / Other (amps)	Power Dis (W)	PROGRAMMING: 1st Reg Address	PROGRAMMING: Int Vector	UNIBUS: BR Level	UNIBUS: NPR	UNIBUS: Bus Loads	Model Number
M7820	Interrupt Control	MOD	single ht															M7820
M7821	Interrupt Control	MOD	single ht															M7821
ME11-L	Core Memory (8K)	PAN	5¼					0–50	10–90		5	125					1	ME11-L
MF11-L	Core Memory (8K)	2 SU				Note 7	Note 8	0–50	10–90	3.4	6 A @ -15 V	125					1	MF11-L
MF11-LP	Parity Memory (8K)	2 SU				Note 7	Note 8	0–50	10–90	4.9	6 A @ -15 V	125					2	MF11-LP
MF11-U	Core Memory (16K)	2 SU				Note 9	7009535	0–50	0–90	4.5	3.5 A @ 20 V 0.5 A @ -5 V	120					1	MF11-U
MF11-UP	Parity Memory (16K)	2 SU				Note 9	7009535	0–50	0–90	6	3.4 A @ 20 V 0.5 A @ -5 V	120					2	MF11-UP
MM11-L	Core Memory (8K)	(MF11-L)						0–50	10–90	1.7	0.5 A @ -15 V	125					1	MM11-L
MM11-LP	Parity Memory (8K)	(MF11-LP)						0–50	10–90	1.7	0.5 A @ -15 V	125					1	MM11-LP
MM11-U										4.5	0.5 A @ 20 V 0.5 A @ -5 V							MM11-U
MM11-UP	Parity Memory (16K)	(MF11-UP)						0–50	0–90	4.5	0.5 A @ 20V 0.5 A @ -5 V							MM11-UP
MR11-DB	Bootstrap	2 SPC								0.6							2	MR11-DB
MS11	Semiconductor Mem	(11/45)						0–50	10–80				772 100	114			1	MS11
PC11	Paper Tape	SPC + PAN	10½		50			13–38	20–95	1.5	3	350	777 550	070,074	4		1	PC11
PDM70	Programmable Data Mover	TT	5¼ X 19 X 23	X	55			0–40	10–95		115 Vac 230 Vac	250 250						PDM70
PR11	Paper Tape (rdr)	SPC + PAN	10½		50			13–38	20–95	1.5	3	350	777 550	070	4		1	PR11
RC11-A	Disk & Control	PAN	10½		115			17–50	20–80		2.2	250	777 440	210	5	X	1	RC11-A
RF11-A	Disk & Control	PAN + PAN	16 + 16	X	500			17–33	20–55		6.5	750	777 460	204	5	X	1	RF11-A
RK05	Disk Drive	PAN	10½		110			15–43	20–80		2	160						RK05
RK11-D	Disk & Control	SU + PAN	10½	X	250	7008992	7009562	15–43	20–80	7.5	2	200	777 400	220	5	X	1	RK11-D
RP03	Disk Drive	FS	40 X 30 X 24		415			15–33	10–80		6 A @ 230 Vac	1300						RP03
RP11-C	Disk & Control	CAB + FS		X	740			15–33	10–80		7 6 A @ 230 Vac	2100	776 710	254	5	X	1	RP11-C
RS11	Disk Drive	PAN	16		100			17–33	20–55		2	200						RS11
RS64	Disk	PAN	10½		65			17–50	20–80		2.2	250						RS64
RT01	Numeric Data Entry Terminal	TT	6.5 X 12.5 X 15	X	12			0–40	10–90		0.25 @ 115 Vac 0.12 @ 220 Vac	30						RT01
RT02	Alphanumeric Data Entry Terminal	TT	6.3 X 14.4 X 16	X	14			0–40	10–90		110 Vac 220 Vac	50 50						RT02
TA11	Cassette	SPC + PAN	5¼					10–40	20–80	1.5	1	120	777 500	260	6		1	TA11
TC11-G	DECtape & Control	PAN + PAN	10½ + 10½	X	250			15–27	40–60		9	870	777 340	214	6	X	1	TC11-G
TM11	Magtape & Control	PAN + PAN	26 + 10½	X	500			15–27	40–60		9	1000	772 520	224	5	X	1	TM11
TU10	Magtape Transport	PAN	26	X	450			15–27	40–60		9	1000						TU10
TU56	DECtape Transport	PAN	10½		80			15–27	40–60		3	350						TU56
UDC11	I/O Subsystem	CAB						5–50	10–90		15	1700	771 774	234	4,6		2	UDC11
VR01	Display	PAN	10½		30			10–50	10–90		1	120						VR01
VR14	Display	PAN	10½		75			10–50	10–90		4	400						VR14
VT01	Display	TT	12 X 12 X 23		50			0–50	10–80		2.2	250						VT01
VT05	Alphanum Terminal	TT	12 X 19 X 30		55			10–43	8–90		2	130						VT05

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