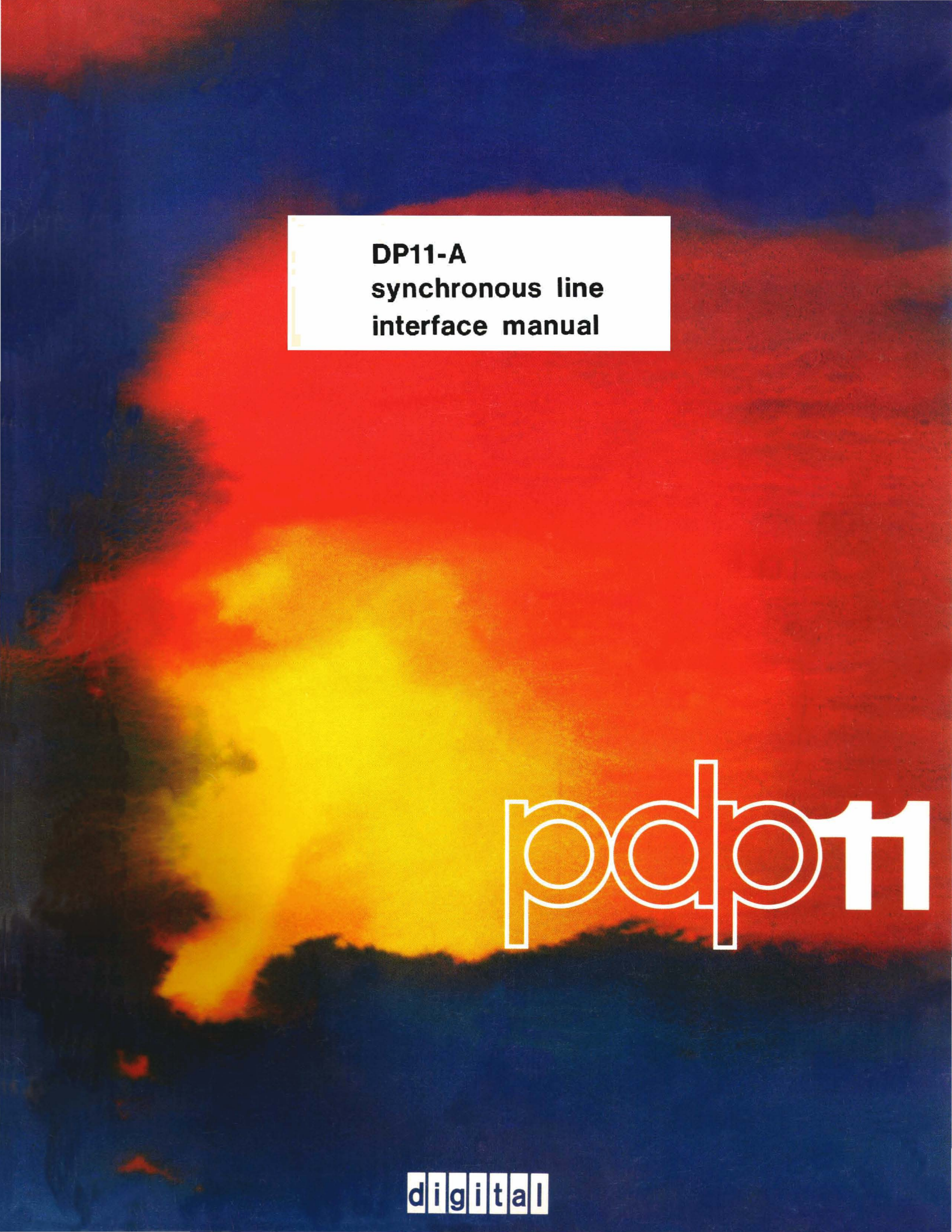
DP11-A synchronous line interface manual



digital

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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

FOREWORD

This manual provides the user with the thoery of operation and logic diagrams necessary to understand and maintain the DP11-A Synchronous Line Interface (hereafter referred to as DP11). The level of discussion assumes that the user is familiar with basic digital computer theory and basic PDP-11 operation.

Although signals and data are transferred between the DP11 and the PDP-11 Unibus, this manual does not cover operating of the Unibus. A detailed description of the Unibus is presented in the *PDP-11 Peripherals and Interfacing Handbook.*

The DP11 is an interface control between the PDP-11 and the Bell 201, 301, and 303 modems, or any equivalent modems. However, this manual does not describe the operation of the Bell units. For a detailed description of the Bell 200 and 300 series modems, the user is referred to their respective *Bell System Communications Technical Reference Manuals.*

A copy of this manual is supplied with each DP11. Throughout the text of this manual, engineering drawings are referenced; a reduced set of engineering drawings is provided in a separate document (also supplied with the equipment) entitled *DP11 Synchronous Communication Interface Engineering Drawings.* This document reflects the updated drawings for the DP11 at the time the equipment is shipped and is to be used in conjunction with this manual.

This manual is divided into five chapters:

a. general description

b. installation planning

c. operational programming

d. detailed description

e. maintenance

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DP11 provides a double-buffered, program-interrupt interface between a PDP-11 and a serial synchronous line. With this interface, the PDP-11 can be used in remote batch and remote concentrator applications; the PDP-11 can also be used as a front end synchronous line controller to handle remote and local synchronous terminals. The PDP-11 Unibus functions as a multiplexer for adding multiple synchronous lines to the PDP-11.

For additional flexibility, the DP11 interface handles a wide variety of terminals and line disciplines (i.e., line control procedures and error control techniques). A programmer can vary the Sync character, data character size, and modem control leads of the DP11. Automatic Sync character stripping and automatic idling are also program selectable. While idling, the DP11 transmits the contents of the Sync buffer instead of transmitting the contents of the data buffer.

The DP11 interface provides individual interrupt vectors and hardware interrupt priority assignments for the transmitter and receiver. Interrupt priority is jumper selectable, which, when coupled with the automatic transmit idle capability, enables dynamic system adjustment to peak message activity. For example, the programmer can temporarily ignore the transmitter if receiver activity is high.

The basic DP11 system unit, which requires the same mounting space as a single PDP-11 system unit, consists of a pre-wired assembly and a fixed set of modules. Some of the optional equipments are: level converters; modem cables for various modems (e.g., EIA RS-232-C for Bell 201, or equivalent modems); the internal crystal clocking source; and character expansion to 12 bits maximum (8 bits are standard). The basic module set is listed below:

1 M7075 Transmit Module
1 M7065 Receive Module
1 M7223 Control Module
1 G8000 +8V Filter Network
1 M105 Address Selector Module
1 M7820 Interrupt Control Module
1 BR5 DEC #5408778 Jumper

1.2 FUNCTIONAL DESCRIPTION

The DP11 is a serial synchronous line interface that is capable of program-controlled, full- or half-duplex operation with a serial modem device. The DP11 interface provides serial-to-parallel and parallel-to-serial data conversion, level conversion, and modem control. In addition, the DP11 has three programmable character lengths: 6,

7, or 8 bits. The character length can be extended to 10, 11, or 12 bits, all optional. The DP11 is program selectable for Sync code and Sync character stripping and is also capable of data transfer line speeds of up to 50,000 baud. The unit is interface-compatible to Bell 201, 301, and 303, or equivalent modems. The DP11 Control provides an auto-answering capability in addition to the features described above.

1.2.1 DP11 Modem Devices

The DP11 interface is compatible with Bell 201, 301, or 303 data set modem devices; detailed information on these units is contained in their respective *Bell System Data Communications Technical Reference Manuals,* supplied with the equipment. However, it is important to describe the modem *handshaking* sequence in relation to the DP11. For purposes of this description, the Bell 201-A Type Modem is used as an example (for procedures that apply to other modems, consult the appropriate reference manual). The handshaking sequence sets up the computer, the DP11, and the modem for data communications. Handshaking is accomplished through call and acknowledge signals between these three units. To set up a data communications channel, the DP11 translates the call and acknowledge signals between the computer and the modem through the DP11 transmitter status register.

Thus, to establish a data communication channel, the modem at the computer is called by another remote modem (see Figure 1-1), and a RING signal from that modem is sent to the DP11. The RING signal initiates an interrupt to the computer, if Interrupt Enable (Status Interrupt) is set. The software determines that the interrupt was caused by a RING signal and, through a service routine in the software, issues a TERMINAL READY signal. This TERMINAL READY signal causes the data set to answer the call; a CARRIER signal is then sent to the caller. The caller acknowledges the CARRIER signal with its own CARRIER signal, which causes the modems to latch into the data mode. Through this sequence, a data channel is established between the caller and the computer, and the DP11 is now ready to receive or transmit data. The only prerequisites for the handshaking sequence are: the software service routines must be in use, and the Interrupt Enable (Status Interrupt) must be set in the DP11 logic.

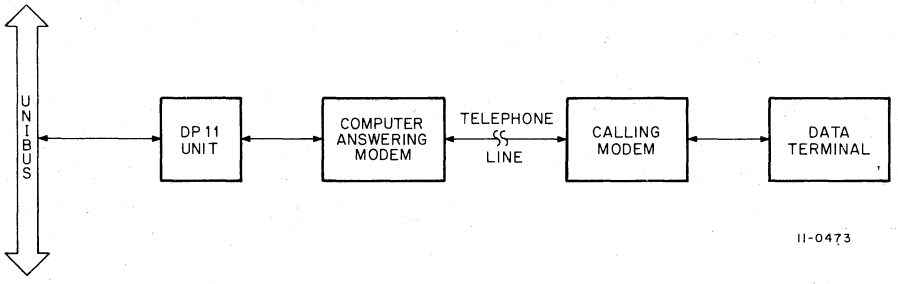


Figure 1-1 Synchronous Data Communication Block Diagram

1.2.2 DP11 Modem Interface

The DP11 is a fully character-buffered synchronous serial line interface that translates serial and parallel data (see Figure 1-2). Output characters are transferred in parallel from the computer to a buffer register; from the buffer register, the characters are serially shifted to the communication line. Input characters from the modem are shifted into a shift register, transferred to a buffer register, and then made available to the PDP-11 on an interrupt basis. Both the transmitter and receiver are double-buffered; as a result, a full character time is allowed in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is normally provided by the associated high-speed synchronous modem. However, the internal clocking option can be used for local terminals when no external clocking is available.

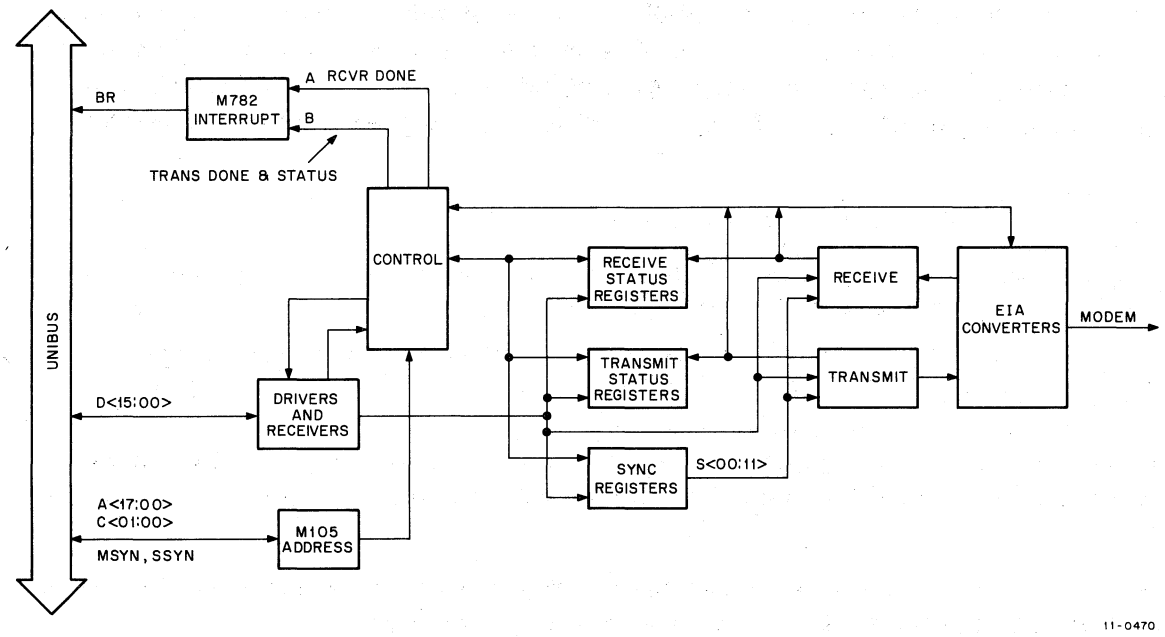


Figure 1-2 DP11 Synchronous Line Interface Block Diagram

Essentially, the DP11 performs two major functions:

a. it receives data from the modem in serial form and transfers the data to the computer in parallel form.

b. it converts parallel data from the computer to serial data and transmits it to the remote terminal near the modem.

When the handshaking procedure has established a data channel between a modem and the computer, the DP11 in Receiver operation must be synchronized with the transmitting data terminal. Synchronization is accomplished through the established Sync Character Code. Because the Sync Character Code and the character size are programmable, the programmer must load them into the Sync Register and Receiver Status Register (refer to Chapter 3) prior to synchronization. When the DP11 has the Sync Character Code and character size, it is able to scan the incoming bit stream until it finds two sequential Sync characters. When two sequential Sync characters are found, the Receive Active Flag is set and synchronization is achieved.

The standard Sync characters are as follows:

a. 8-bit ASCII is 026_8 (00010110 binary bit stream)

b. 8-bit IBM BISYNC is 32_{16} (00110010 binary bit stream)

c. and EBCDIC is 062_8.

When synchronization is achieved, serial data can be received continuously (no start or stop bits are needed). The first character following two or more Sync characters causes an interrupt if the RECEIVE INTERRUPT is enabled (if STRIP SYNC is set, an interrupt occurs at the first data character). This interrupt occurs each time a data character is received by the DP11, and it is one of two DP11 independent interrupt request levels and vectors.

The other interrupt request is for the transmitter and DP11 status. A receive interrupt request is generated as the receive character is transferred into the receive buffer. If the program does not remove the receive character from the buffer before the next character is transferred, a DATA OVERRUN ERROR bit is set in the DP11 Status Register. If the STATUS INTERRUPT ENABLE bit is set, this error condition causes a DP11 status interrupt request.

When receiving data, the DP11 operates in one of two modes:

a. All Sync characters are stripped automatically from the incoming data stream, if the RECEIVE ACTIVE bit *is set* and the STRIP SYNC bit *is set.*

b. Sync characters are treated as normal data and cause an interrupt request when transferred, if the RECEIVE ACTIVE bit *is set* and the STRIP SYNC bit *is not* set.

Incoming characters to the Receiver logic appear right-justified in the receive data buffer. The first bit received from each character appears as the right-most bit in the receive buffer. The parity of this bit can be tested by the programmer.

The transmitter of the DP11 synchronizes identically to the receiver. When synchronization is achieved, serial data can be transmitted to a modem. The transmitter operates in one of two modes:

a. When the IDLE SYNC bit *is not* set, the transmitter must be refreshed in approximately one character time (i.e., 1/baud X number of bits per character – 1/2 second), or the DP11 stops transmitting (i.e., holds the TRANSMITTED DATA line to the modem in the binary one-mark position). This also sets the REQUEST TO SEND line to the modem to OFF.

b. When the IDLE SYNC bit *is set,* the logic will transmit from the Sync buffer if the programmer does not refresh the transmitter in approximately one character time (i.e., 1/baud X number of bits per character – 1/2 second).

The transmitter, as indicated previously, has a separate INTERRUPT ENABLE control bit from the receiver. When the transmitter interrupt is enabled, an interrupt request is generated each time the leading edge of a data character is presented to the modem synchronous line. In the idle mode, transmission from the Sync buffer does not cause an interrupt. Only the transmission of data characters can cause an interrupt.

With the buffer loaded on IDLE SYNC asserted, the SEND REQUEST (modem control) lead asserts when data is ready for transmission. The first data bit is presented to the modem on the first transition of the clock following the assertion of the CLEAR TO SEND lead. Additionally, provided that the HALF-DUPLEX bit is set, the assertion of SEND REQUEST inhibits the Receiver logic, which prevents the transmitter from causing a Receive "A" interrupt. When terminating the transmitter operation (i.e., the transmit buffer is empty and IDLE SYNC clear), SEND REQUEST is negated on the second positive transition of the transmit clock, after the last data bit has been delivered to the modem.

In addition to the signals transmitted between the modem and the DP11 during the handshaking sequence, other control signals and data are transmitted between these units through the modem control leads, provided to interface the DP11 to the Bell 201, 301, 303 or equivalent modems. These leads allow the DP11 to be used in *switched* or *dedicated* full- or half-duplex configurations. The DP11 status interrupts have a separate interrupt enable bit but share the bus request level and interrupt vector address with the transmitter. In relation to the modems, if STATUS INTERRUPT is enabled (same as INTERRUPT ENABLE of the handshaking sequence), a CARRIER FLAG, DATA OVERRUN, or RING will generate interrupt requests. The control leads are fail-safe (i.e., they appear OFF if the modem loses power). For the actual control lead designations of the cable interface between the Bell 201, 301, and 303 modems and the DP11, refer to Chapter 2.

1.3 SPECIFICATIONS

The DP11 specifications are grouped into five general categories:

a. physical description

b. environmental limits

c. operational interface characteristics

d. modem compatibility

e. power requirements

1.3.1 Physical Description

One DP11 Synchronous Line Interface unit occupies (see Figure 1-3) one PDP-11 System unit within the PDP-11 System mounting box. The DP11 interface unit (including all options) consists of:

a. a PDP-11 System unit,

b. two M7075 Transmit Modules,

c. two M7065 Receive Modules,

d. M7223 Control Module,

e. M105 Address Selector Module,

f. M7820 Interrupt Control Module,

g. G8000 +8V Filter,

h. M920 Unibus Connector,

i. M405 Crystal Clock,

j. M239 Counter Module,

k. Level Converter Module (depending on the modems interfaced),

l. Modem Cable Connector Module (depending on the modems interfaced), and

m. DP11 Power Connections.

The level converter and cable connector options are described in the configuration option section of Chapter 2. Figure 1-3 illustrates the module layout for a general DP11 System. The cable options with the cable connection module are listed in the cable requirement section of Chapter 2.

NOTE

If the DP11 system unit is the last unit connected to the PDP-11 Unibus, then the last M920 Module is replaced by a BC11A or M930 Bus Terminator.

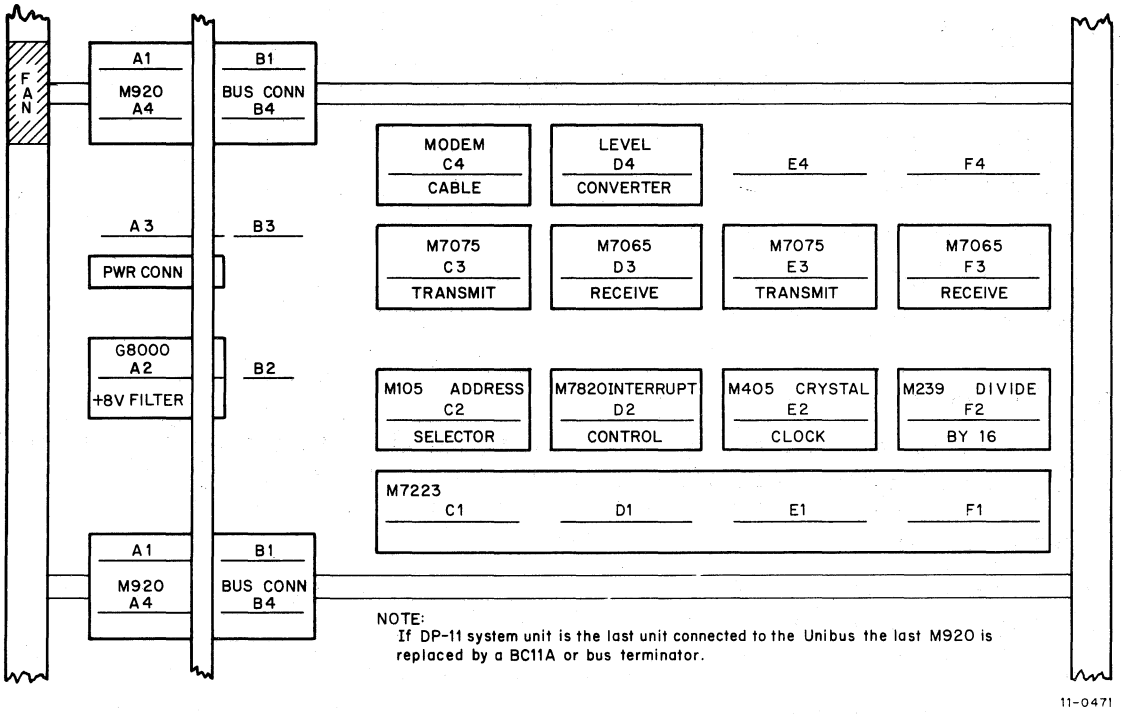


Figure 1-3 DP11 System Unit Layout

Strip Sync: The Receiver has the programmable feature of stripping incoming Sync characters from the data stream.

Idle Mode: This programmable feature transmits the contents of Sync Register if the program fails to refresh the transmit buffer.

Order of Bit Transmission: Low-order bit first.

Program Response Time:

Receive: 1/baud X bits per character seconds.

Transmit: 1/baud X bits per character – 1/2 second.

Parity: Parity check bit provided on incoming characters.

Program Interrupt: Conditions are Receive Done, Transmit Done, and Status (CARRIER FLAG, RECEIVE OVERRUN, and RING). There are two independently selectable Bus Request (BR) priorities: one for Receive Done, and the other for Transmit Done and Status.

Data and Modem Control Signals: Most leads of the Bell 201, 301, and 303 modems are brought into the unit. All leads are EIA RS-232-C and CCITT-compatible for the 201 modem. All leads for the 300 series modems are current mode, as defined in the appropriate reference manual.

Bus Load: One line unit (DP11) represents one unit load to the PDP-11 Unibus. The Unibus provides 20 unit loads. To add more than 20 unit loads, a bus extender (DB11-A) must be used.

Physical Connection: For 201 modems, a 25-ft cable with RS-232-C compatible, 25-pin male connector (BC01R-25) is used. For 300 series modems, a 25-ft coaxial cable is used with appropriate connectors for the 301 and 303 modems, respectively (BC01T-25 and BC01Y-25).

1.3.2 Environmental, Interface, Modem, and Power Specifications

The environmental limits, operational interface characteristics, modem capabilities, and power requirements are as follows:

Environmental Limits

Temperature: 10°C to 50°C
Humidity: 20% to 90% non-condensing

Operational Interface Characteristics

Operating Transfer Mode:

Modem: Full- or half-duplex, selected under software control.
PDP-11: Interrupt mode for parallel data and status.

Maximum Data Rates: At EIA/CCITT/10,000 baud (for 200 series modems). Current mode is program limited (300 series modems) to 50,000 baud.

Data Format: Character size is variable under program control to 6, 7, or 8 bits (additional 10, 11 or 12 bits optional).

Clocking: Synchronous clock from the external modem, (Internal clock optional).

Sync Character: Identifiable Sync character is programmable.

Sync Detection: Two successive Sync characters are required to activate the DP11 Receiver. The DP11 has no other character recognition feature.

Modem Compatibility (Typical)

Type	Communications Channel	Speed (Baud)
Bell 201A	(Direct Distance Dialing Network – Type 3002 (C2))	2,000
Bell 201B	(Leased Line Only – Type 3002 (C2))	2,400
Bell 301B	(Leased Line Only – Group (12 Voiceband Line))	40,800
Bell 303B	(Leased Line Only – Half Group (6 Voiceband Lines))	19,200
Bell 303C	(Leased Line Only – Group (12 Voiceband Lines))	50,000

Power Requirements

Current Drawn (maximum):

DP11-CA +5V: 0.77A @ 3.85W or 13.2 BTU/hr
DP11-KA +5V: 0.18A @ 0.9W or 3.08 BTU/hr
DP11-DA +5V: 2.56A @ 12.8W or 43.8 BTU/hr
DP11-DA -15V: 0.07A @ 1.05W or 3.59 BTU/hr
DP11-DA +8V: 0.04A @ 0.32W or 1.09 BTU/hr

1.4 RELATED DOCUMENTS

A list of documents pertaining to the DP11 as a peripheral interface for the PDP-11 computer is provided in Table 1-1.

Table 1-1
Related Documents

Title	Number	Description
GENERAL		
PDP-11/20/15/R20 Processor Handbook	112.01071.1855	Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data.
Instruction List	None	Pocket-size list of instructions. List group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader.
Logic Handbook	DEC, 1970	Presents functions and specifications of the M-Series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11.
HARDWARE		
PDP-11 Peripherals and Interfacing Handbook	112.01071.1854	Used in conjunction with this manual. Provides detailed theory, flow, and logic descriptions of Unibus and external device logic. Discusses methods of interface construction and provides examples of typical interfaces.
PDP-11 Conventions	DEC-11-HR6A-D	*a.* General Maintenance *b.* Logic Symbology *c.* Drawing Set Explanation *d.* Processor Signals *e.* Product Identification Code *f.* Glossary *g.* Abbreviations
SOFTWARE		
Paper-Tape Software Programming Handbook	DEC-11-GGPA-D	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble and debug PDP-11 programs. Also included is a discussion of input/output programming and the floating-point and math package.

Table 1-1 (Cont)
Related Documents

Title	Number	Description
DATA SETS		
Bell System Data Communications Data Set 201 Technical Reference Manual	None	Data Set Interface specifications. Data Set description and options including interface signals and timing.
Bell System Data Communications Data Set 301 Technical Reference Manual	None	Data Set Interface specifications. Data Set description and options including interface signals and timing.
Bell System Data Communications Data Set 303 Technical Reference Manual	None	Data Set Interface specifications. Data Set description and options including interface signals and timing.

CHAPTER 2
DP11 INSTALLATION PLANNING

2.1 INTRODUCTION

This chapter contains the information necessary to install and operate DP11. All necessary power and interface connections, priority and address assignments, and optional system configurations are also included in this chapter.

2.2 CONFIGURATIONS

Table 2-1 lists the available DP11 options, their prerequisites, and a brief description.

Table 2-1
DP11 Options

DEC No.	Prerequisite	Description
DP11-DA	PDP-11	Full/half duplex synchronous line module set. Double buffered, 6, 7, or 8-bit characters. EIA/CCITT termination suitable for direct use with 201 modems. Includes 25-ft modem cable.
DP11-DB	PDP-11	Same as above except suitable for direct use with 301 modems. Includes 25-ft modem cable.
DP11-DC	PDP-11	Same as above except suitable for direct use with 303 modems. Includes 25-ft modem cable.
DP11-CA	DP11-DA DP11-DB DP11-DC	Allows the DP11 to handle 10, 11, or 12 bits per character, in addition to the standard 6, 7, and 8 bits per character. Jumper "D4" on M7065 Module must be removed at F03.
DP11-KA	DP11-DA or DP11-DB or DP11-DC	Internal Clock. Clocking source to be used for direct connection of DP11 to local synchronous terminal or a local synchronous computer interface (without modems). For following baud rates: 2400, 4800, 9600, 19.2K and 40.8K, baud rate must be specified.
H312A	DP11-DA	Synchronous/asynchronous null modem jumper box. Allows direct connection of a PDP-11 to any peripheral with a modem type interface that conforms to EIA RS-232-C and CCITT specifications. Also allows direct serial synchronous computer to computer data transfers between two PDP-11s. Each PDP-11 must have a DP11-DA and a DP11-KA. The maximum separation must not exceed 50 ft.

The basic DP11 consists of the module layout for a particular option (refer to Chapter 1). However, the DP11 can connect a variety of terminals or synchronous lines to the PDP-11 System, either remotely or locally. These possible configurations are shown in Figure 2-1. The DP11 is ideally suited for interfacing the PDP-11 to high-speed synchronous lines for remote batch, remote data collection, and remote concentration applications.

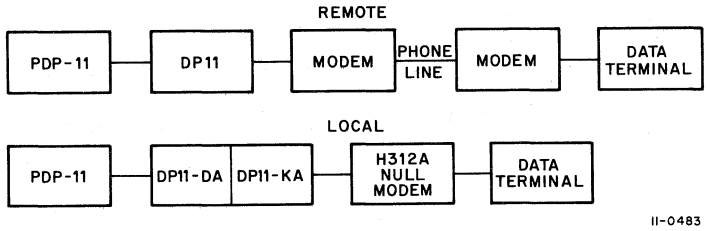


Figure 2-1 Modem Configurations

Multiple DP11s enable a PDP-11 System to be used as a synchronous line concentrator or front-end synchronous controller to a larger computer. In these cases, the PDP-11 Unibus acts as a multiplexer for the synchronous lines of the various DP11s. The DP11 can also connect two PDP-11s or a PDP-11 and a larger computer (e.g., the IBM 360). These connections can be either remote or local. Two possible configurations are shown in Figure 2-2.

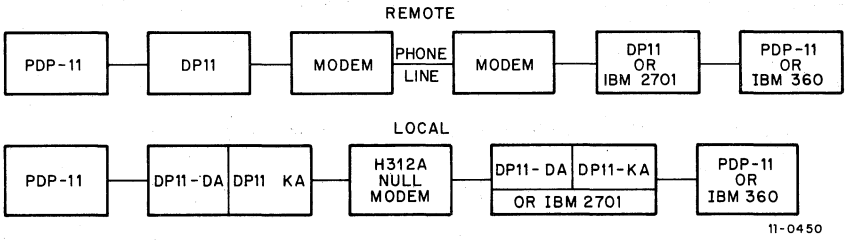


Figure 2-2 Interface Configurations for Two Computers

2.3 CABLING AND TERMINATIONS

The DP11 provides an interface to the PDP-11 Unibus and the synchronous modem interface. The DP11 presents one unit load to the Unibus and meets all Unibus electrical specifications. Also, the DP11 provides data and control leads compatible with modem types 201A, 201B, 301 and 303 modems, or equivalent. The 201 series interfacing conforms to EIA CCITT specifications; the 300 series interfaces are current mode. Table 2-2 shows all the data and control leads utilized for both the standard type modems and the DP11. Unless otherwise specified, the 201 levels are bipolar; the 301 and 303 levels are current mode. The control and data leads are interfaced to the DP11 through the cable modules listed below:

Modem	Cable	Connector
200 series	BC01R-25 (25 ft)	DP25P Cannon or Cinch 25-pin
303 series	BC01W-25 (25 ft)	Burndy

NOTE
These components are supplied with the particular configuration delivered.

For the 200 series modems, a EIA/CCITT Level Converter (RS-232-C) Module is needed from the DF11-A series (M594). The 300 series level conversion is provided by the DF11-G Current Mode Level Converter. Electrical specifications for both RS-232-C and current mode interfacing are given in Appendix A. The RS-232-C Interface Pin Assignments and Equivalent CCITT for each data and control lead are also included in Appendix A.

Table 2-2
Data and Control Leads

DP11A Interface	Model 301	Model 303	Model 201
Send Data	Send Data	Send Data	Send Data
Received Data	Received Data	Received Data	Received Data
Send Request	Send Request	Send Request	Send Request
Clear to Send	Clear to Send	Clear to Send	Clear to Send
Interlock/Data Set Rdy	Interlock	Data Set Rdy	Interlock
Carrier/AGC	Carrier on-off	AGC Lock	Carrier on-off
Serial Clock Transmit	Serial Clock Transmit	Serial Clock Transmit	Serial Clock Transmit
Serial Clock Rcve	Serial Clock Rcve	Serial Clock Rcve	Serial Clock Rcve
Terminal Rdy		Data Terminal Rdy*	Remote Control
Ring		Ring Indicator*	Ring Indicator 1
External Timing	Serial Clock Transmit (external)	Serial Clock Transmit (external)	External Timing

*Bipolar

2.4 ADDRESS AND PRIORITY ASSIGNMENTS

The DP11 is addressed through the M105 Address Selector Module; the DP11 interrupt vector is determined by the M7820 Interrupt Control Module. Each DP11 unit uses a different set of vector addresses. These addresses are pre-assigned and are listed in Paragraph 3.4. The priority assignment is determined by the jumper connections that plug into the M7223 Module. The normally supplied priority for the DP11 is Bus Request Line 5 (BR5). The Bus Request levels for transmit and receive are independently selected; however, the user can assign another priority level. The respective BR level connectors with part numbers are as follows:

BR Level	Part No.
BR4 (priority 4)	5408776
BR5 (priority 5)	5408778
BR6 (priority 6)	5408780
BR7 (priority 7)	5408782

2.5 POWER CONNECTIONS

The PDP-11 System or BA11 Mounting Box provide the power connections to the DP11 (see Figure 1-3). Because the DP11 occupies a typical PDP-11 System unit, it receives power from the PDP-11. These power connections are discussed in detail in the *PDP-11 Peripherals and Interfacing Handbook.*

2.6 INSTALLATION TESTING

Installation testing is performed to ensure that the DP11 has been properly installed and is completely operational. Installation testing is accomplished by running the diagnostic supplied with the DP11 (MainDEC-11-D8DA). This program is contained on the diagnostic tape supplied with the DP11. Instructions for running the diagnostic are included with the program tape (refer to Chapter 5).

CHAPTER 3
OPERATIONAL PROGRAMMING

3.1 INTRODUCTION

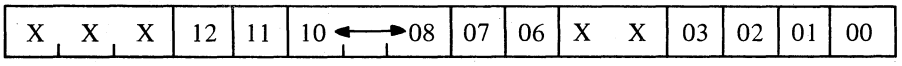
The software-related aspects of the DP11 hardware operation are discussed in this chapter. Descriptions of the addressable hardware registers, addressing utilization, Bus Request priorities and interrupt vectors, synchronous timing considerations, and data format are also included.

3.2 DEVICE REGISTERS

The following paragraphs provide the register address assignments, definitions of each register bit, and bit map diagrams for each of the six device registers of the DP11.

3.2.1 Receiver Control and Status Register (RCSR)

Address: 774XX0



Bit	Bit Designation	Description
00	STRIP SYNC	If set, all Sync characters following Receive Active are stripped from the incoming serial data. This bit is Read/Write and cleared by Initialize.
01	HALF DUPLEX	If set, Request to Send On inhibits the Receive logic. This bit is Read/Write and cleared by Initialize.
02	MAINTENANCE MODE	Maintenance Mode provides an internal data loop that connects the transmitter output to the Receiver input. Additionally, the Clear to Send lead is simulated by the hardware. This mode of operation provides its own clock, which handles data at approximately 3000 baud. Maintenance Mode, coupled with the Read and/or Write Status bit, exercises approximately 85% of the DP11's logic. This is excluding the EIA converters, modem cable, modem status, and the interrupts caused by the modem status. This bit is Read/Write and is cleared by Initialize.
03	MISC RECEIVE	Miscellaneous Receive is provided to monitor any nonstandard modem status required by the user. Changes can be implemented by Computer Special Systems or by the user. Production units will be wired to secondary Receive (i.e., 202D). This bit is Read Only.

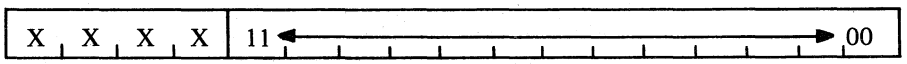
Bit	Bit Designation	Description
04–05	Not Used	Not Applicable
06	INTR EN (RX DONE)	The Receive Done Interrupt Enable allows an "A" interrupt to occur when the Receive Done Flag is set. This bit is Read/Write and is cleared by Initialize.
07	RECEIVE DONE FLAG (RX DONE)	The Receive Done Flag indicates that the receive buffer contains an assembled character. If the program does not respond to this flag in 1/baud x bits per character, the Receive Overflow Flag will be set causing a "B" interrupt. This bit is Read/Write and is cleared by Initialize and by gating the receive buffer to the Unibus.
08–10	BITS PER CHARACTER	Selects 6, 7, 8, 10, 11 or 12 bits per character as follows:

Data Bits			Select
10	9	8	
0	0	0	8 bits per character
0	0	1	7 bits per character
0	1	0	6 bits per character
0	1	1	Not used
1	0	0	12 bits per character
1	0	1	11 bits per character
1	1	0	10 bits per character
1	1	1	Not used

11	RECEIVE ACTIVE	Receive Active is set when the hardware recognizes *two* consecutive Sync characters. This bit is Read/Write Zero and is cleared by Initialize. The M7065 module provides jumpers for operation with one Sync character, but this mode of operation is not software supported.
12	CHARACTER PARITY	Character Parity (VRC) indicates the parity of the last character assembled and contained in the receive buffer. A 1 indicates odd character parity; a 0 indicates even parity. This bit is changed at the same time the Receive Done Flag is set. This bit is Read Only and is cleared by Initialize.
13–15	Not Used	Not Applicable

3.2.2 Receiver Buffer Register (RBUF)

Address: 774XX2



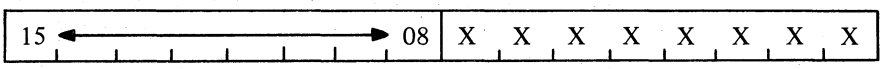
Bit	Description
00–11	Provides a 12-bit Data Buffer Register for each character received from the modem and sent to the DP11.

NOTE
Least significant bit is right justified.

3.2.3 Sync Register (Sync)

Address: 774XX3

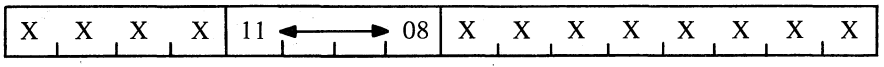
Sync Register (high byte)



Bit	Bit Designation	Description
15–08	SYNC 7–0	High byte (MOVE) address XX3 accesses the Sync Register for standard configurations of maximum 8-bit character lengths. Sync 7–0 is Read/Write and is not cleared by Initialize.

Address: 774XX7

Sync Register (high byte)

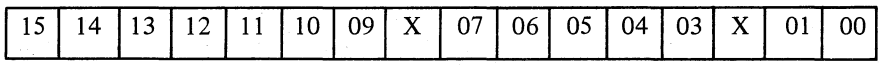


Bit	Bit Designation	Description
11–08	SYNC 11–08	High byte (MOVE) address XX7 accesses the additional Sync Register for expanded configurations to maximum 12-bit character lengths. Sync 11–08 is Read/Write and is not cleared by Initialize.

NOTE
High byte is not addressable from the PDP-11 Console.

3.2.4 Transmitter Control and Status Register (TCSR)

Address: 774XX4



Bit	Bit Designation	Description
00	TERMINAL RDY	Controls switching of the data communication equipment to the communication channel. Auto Dial and manual call origination: maintains the established call. Auto answer: allows handshaking in response to RING signal. This bit is Read/Write and is cleared by Initialize.
01	IDLE SYNC	Allows transmission from the Sync Buffer. TRANSMIT DONE is set (if enabled) as the first bit of each data character is presented to the line. If the IDLE SYNC bit is set when the transmitter is inactive, the logic will raise Request to Send and begin transmitting from the Sync Register. Once active, the Transmits Shift Register will be loaded from the Sync Register if the program has *not* responded to Transmit Done in 1/baud X bits (bits per character – 1/2 second) time. This bit is Read/Write and is cleared by Initialize.

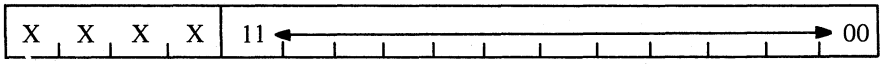
NOTE
IDLE does not cause TRANSMIT DONE.

Bit	Bit Designation	Description
02	Not Used	Not Applicable
03	MISC TRANSMIT	Provided for variety of uses, such as: new sync, rate selector. This lead is to be wired by Computer Special Systems or the end user. Production units are wired for secondary transmit data (R.C. 202). Additionally, the secondary transmit data line is used to generate the Receive and Transmit Clock in the external loop test configuration (refer to Chapter 5). **NOTE** **The external loop diagnostic configuration will not operate if the Miscellaneous Transmit lead is reassigned.** This bit is Read/Write and is cleared by Initialize.
04	Unassigned	Write-only flip-flop. Its use is specified by end user or Computer Special Systems. This bit is cleared by Initialize.
05	INTR EN (STATUS)	Interrupt enable (status). If set, allows interrupt "B" to be set by Carrier Flag, Receive O'Run Flag and by Ring Flag. This bit is Read/Write and is cleared by Initialize.
06	INTR EN (TX DONE)	Interrupt Enable TX DONE. If set, allows interrupt "B" to be set by TRANSMIT DONE. This bit is Read/Write and is cleared by Initialize.
07	TRANSMIT DONE FLAG (TX DONE)	The Transmit Done Flag is set to a 1 when the leading edge of the first bit of each character is presented on the line. Additionally, this flag causes a "B" interrupt if INTR EN (TX DONE) is set. This bit is Read/Write and is cleared by Initialize and by loading the Transmit Buffer Register.
08	Not Used	Not Applicable
09	REQUEST TO SEND	Request to Send is a hardware function. This bit is set on the second positive transition of the Transmit Clock if the transmit buffer is loaded or if the IDLE SYNC bit is set. This bit is Read Only and is cleared by Initialize. If IDLE SYNC is not set, and the transmit buffer was not refreshed in 1/baud X (bits per character – 1/2 second) time after TRANSMIT DONE was set, then Request to Send will go to 0 on the second positive transition of the Transmit Clock following the end of the last bit presented to the line.
10	CLEAR TO SEND	This bit reflects the current state of the Modem Clear to Send lead. An "ON" state indicates that the modem is ready to transmit data. This signal is a result of the Request to Send lead in half-duplex configuration. This lead is Read Only.
11	CARRIER	This bit reflects the current state of the Modem Carrier Control (AGC if 300 Series Modem) lead. An OFF indicates that no signal is being received or that the received signal is unsuitable for demodulation. This lead is Read Only.
12	MODEM RDY	This bit reflects the current state of the Data Set Rdy (also interlock) lead. This bit indicates that the modem is powered and not in test, talk, or dial mode. This lead is Read Only.

Bit	Bit Designation	Description
13	RING FLAG	A 1 indicates that a RING signal has been received by the Modem. Also, the flag causes a "B" interrupt if INTR EN (STATUS) is set. This lead is Read/Write and is cleared by Initialize.
14	RX O'RUN FLAG	This bit is set if the receive buffer was not read in 1/baud X bits per character time, following the Receive Done Flag. This flag indicates a loss of at least one data character and suggests that a re-transmission be requested. This bit is Read/Write and is cleared by Initialize.
15	CARRIER (↓) FLAG	This bit is set if the Modem Carrier lead made an ON to OFF transition. A transition occurring on this lead (while data is being received) indicates a high probability of data errors. Also, the Receive Synchronism with the incoming data bits is no longer reliable, and a new Sync sequence should be established. The Sync sequence can be established by writing a 0 into the Receive Active bit and requesting a re-Sync (i.e., Sync, Sync, Sync) from the remote modem terminal.

3.2.5 Transmitter Buffer Register (TBUF)

Address: 774XX6



Bit	Description
11–00	Provides a 12-bit buffer register for each 6- to 12-bit character of data being transmitted onto a modem line from the DP11.

3.3 ADDRESS UTILIZATION

Each DP11 utilizes six addresses. The transmitter and receiver buffer and status registers each have one assigned address; the Sync Register has an assigned address for each byte. Up to a maximum of 32 DP11s can be interfaced, and an address range from 774777 to 774400 is provided. The address utilization for multiple DP11's is as follows:

1st DP11	RCSV	774770
	RBUF	774772
	TCSV	774774
	TBUF	774776
	SYNC 0–7	774773
	SYNC 8–11	774777
2nd DP11	RCSV	774760
	RBUF	774762
	TCSV	774764
	TBUF	774766
	SYNC 0–7	774763
	SYNC 8–11	774767
32nd DP11	RCSV	774400
	RBUF	774402
	TCSV	774404
	TBUF	774406
	SYNC 0–7	774403
	SYNC 8–11	774407

3.4 BUS REQUEST PRIORITY AND INTERRUPT VECTORS

Two Bus Request (BR) levels are available to the DP11 per synchronous modem. The BR levels are selected by two BR connectors on the control module. These BR levels and their equivalent interrupts are as follows:

Level	Interrupt
BR "A" =	RECEIVE DONE
BR "B" =	TRANSMIT DONE
	RECEIVE OVERRUN
	RING
	CARRIER

NOTE

BR "A" is electrically closer to the PDP-11 than BR "B" when both are at the same priority levels.

All production units are tested, accepted, and shipped with BR levels of "A" and "B" set at BR5. The customer can change this BR level by changing the mini connector on the control module.

Each synchronous modem DP11 interface requires two interrupt vectors: one for Receive Done and one for Transmit Done and Status (Carrier Flag, Receive Overrun, and Ring). The vector addresses are assigned from 300 to 777. The DP11 follows the DC11 and the KL11 in contiguous vector address assignments from 300 (i.e., the first vector address of the DP11 starts after the vector addresses of the DC11 and KL11).

3.5 TIMING CONSIDERATIONS

The DP11 has two basic timing considerations: baud rate and program response time. The baud rate or bits per second of data transfer speed under normal DP11 operation is totally dependent on the modem speed. The modems and their various speeds are listed in Chapter 1. However, employment of the clocking option allows the baud rate to be selected to the rate desired (refer to Paragraph 1.3, under DP11-KA option). This optional clock baud rate is program limited. The program response time for the DP11 is equivalent to the time the logic has to transfer a character. For a receive transfer, the program response time is the time it takes for the bus to remove the character from the receive buffer before the next character arrives. This time is defined as 1/baud X bits per character seconds. The transmit response time is the time necessary to input a new character to the transmit buffer (TBUF) before the last character is transferred onto a synchronous line. This time is defined as 1/baud X bits per character – 1/2 second.

CHAPTER 4
DETAILED DESCRIPTION

4.1 INTRODUCTION

The DP11 can be divided into seven major functional groups:

a. selection logic

b. interrupt logic

c. clock logic

d. converter logic

e. receiver operation

f. transmitter logic

g. maintenance mode

Each of these areas is presented separately in the following paragraphs. A brief description of the task of each functional unit is outlined below:

Selection Logic – The selection logic determines if the DP11 unit has been selected for use, and what type of operation (transmit or receive) has been selected. The logic consists of the M105 Address Selector Module and portions of the M7223 Module.

Interrupt Logic – The interrupt logic permits the DP11 to gain bus control and perform an interrupt program. The priority level of the bus request (BR) line can be changed by the user. This logic consists of the M7820 Interrupt Control Module and portions of the M7223 Control Module.

Clock Logic – The clock logic provides the clocking baud rate signals from the modems to the DP11 logic for clocking transfer rates. An internal clocking option is available for other desired baud rates. The optional logic consists of the M405 Clock Module and the M239 Divide By 16 Module.

Converter Logic – The converter logic converts TTL logic levels to levels suitable for synchronous data transmission. The M594 Level Converter converts EIA and CCITT bipolar signals for the 200 series modems. Other DF11 series level converters (M595) are used for compatibility levels with the 300 and 303 series modems.

Receiver Operation – The receiver logic converts serial data from a synchronous line into parallel data for transmission to the bus. This logic consists of M7065 Receiver Module, and the control logic (RCSR) is located on the M7223 Control Module.

Transmitter Operation – The transmitter logic converts parallel data from the bus to serial data for transmission on the synchronous lines. This logic consists of the M7075 Transmitter Module, and the control logic (TCSR) is located in the M7223 Control Module.

NOTE

The DP11 unit performs two basic operations: Receiving and transmitting data. When receiving data, it is inputting data from the data lines and outputting data to the bus; conversely, when transmitting data, it is inputting data from the bus and outputting data onto the data lines.

A reduced set of engineering drawings entitled *DP11 Synchronous Line Interface Engineering Drawing Manual* is supplied with each DP11; these drawings support the text of this chapter.

4.2 SELECTION LOGIC

The DP11 selection logic is used to decode the address on the bus lines and to determine if the DP11 unit has been selected for use. A unique address is assigned to both the receiver and transmitter; consequently, the incoming address determines if a character is to be received off the data lines or transmitted onto the data lines.

The DP11 consists of six registers with six bus addresses (refer to Paragraph 3.3). The selection logic is used to control the flow of information between the Unibus and the device registers. The selection logic produces SELECT lines and gating IN and OUT signals that determine the register that has been selected, and whether the register is to perform a receive or transmit function, respectively. The selection logic consists of an M105 Address Selector Module, gating logic, and bus drivers and receivers.

4.2.1 Address Selector Module

The M105 Address Selector Module decodes the address information from the bus and provides three gating signals and four select line signals (see drawing D-BD-DP11-AA-2) that are used to activate appropriate DP11 circuits for the selected function. The M105 Module jumpers are arranged to permit the module to respond to only the standard device register addresses. Although these addresses have been selected by DEC as the standard assignments for the DP11, the customer can change the jumpers to any addresses desired. However, they will not be software supported by DEC. The description provided herein is a basic description; for a more detailed description, refer to the *PDP-11 Peripherals and Interfacing Handbook.*

4.2.2 Gating Logic

The gating signals and select line signals from the M105 Address Selector Module are applied to the gating logic (see drawing D-CS-M7223-0-1, sheet 2), which generates the register and bus, gating and loading signals. These pulses enable the bus drivers and receivers that are connected to the DP11 device registers and initiate the receive and transmit functions.

Table 4-1 lists the gating and loading signals generated for the DP11 transmitting and receiving functions. The four register select signals (SELECT 0, SELECT 2, SELECT 4, and SELECT 6) indicate the register being referenced. In addition, the assertion of A00 provides for the odd address Sync Register bytes. When asserted, A00 refers to the Sync Register (not addressable from the console), and when unasserted, the address is even and one of the other device registers is being selected. The three gating signals IN, OUT LOW, and OUT HIGH indicate the direction of data flow in reference to the Unibus. The gating signals either gate data from the DP11 to the bus (IN), or gate data from the bus into the DP11 (OUT). In Table 4-1, for receiver operations either LDRX STAT DATA to BUS generates "A" INTR EN which momentarily disables receiver interrupts. "B" INTR EN is momentarily disabled by either TX LD or LD TX STAT. The momentary disabling of the interrupts provides a "reset" for the M7821 Interrupt Control Module.

Table 4-1
Gating and Select Line Signal Generation

Select Lines 0 2 4 6	A00 L	Gating Signal	Signal Generated	Signal Function
0 0 0 1	1	IN	SYNC 8–11 to BUS	Gates Sync bits 8 through 11 onto the bus for program use.
0 1 0 0	1	IN	SYNC 0–7 to BUS	Gates Sync bits 0 through 7 onto the bus for program use.
0 1 0 0	0	IN	DATA to BUS	Gates data bits converted by the receiver logic from serial to parallel onto the bus for each character being received. Also clears RX DONE.
1 0 0 0	0	IN	RX STAT to BUS	Gates the contents of the Receiver Control and Status Register to the bus.
0 0 1 0	0	IN	TX STAT to BUS	Gates contents of Transmitter Control and Status Register onto the bus.
1 0 0 0	0	OUT LOW	LD RX STAT	Loads the Receiver Control and Status Register from the bus data lines.
0 0 1 0	0	OUT LOW	LD TX STAT	Loads the Transmitter Control and Status Register from the bus data lines.
0 1 0 0	1	OUT HIGH	LD SYNC 0–7	Loads Sync 0–7 (Sync character) from the bus data lines.
0 0 0 1	1	OUT HIGH	LD SYNC 8–11	Loads Sync 8–11 (extended Sync character) from the bus data lines.
0 0 0 1	0	OUT LOW	TX LD	On its low transition, this signal clears the TX DONE flag and resets the M7820 interrupt "B". Also the low transition loads the B INTR EN of TCSR.

4.2.3 Bus Drivers and Receivers

The bus drivers and receivers are logic gates that are used to pass signals (see drawing D-CS-M7223-0-1, sheets 1 through 6) between the Unibus and the DP11 while maintaining the transmission-line characteristics of the bus. These logic gates have high input impedance and proper logic thresholds required by the bus signals. For a more detailed description of the drivers and receivers, refer to the *PDP-11 Peripherals and Interfacing Handbook.*

4.3 INTERRUPT CONTROL

The M7821 Interrupt Control Module enables the DP11 unit to gain control of the bus (become bus master) and perform an interrupt operation. When the last bit of a data character is in the receiver buffer, the RX DONE bit is set. If the INTR EN "A" (bit 6) in the RCSR is set, the interrupt control is activated, and the interrupt software service routine is entered. This is for Receiver operation only and is on the "A" interrupt level for the DP11. When TX DONE is set (bit 7) in the TCSR and INTR EN "B" (TX DONE) (bit 6) is set, the interrupt control is activated, and the transmit interrupt service routine is entered. The jumpers on the M7820 Module determine the vector address for the interrupt.

The transmitter (TSCR) initiates an interrupt, if INTR EN "B" (STATUS) (bit 5) in the TCSR is set, with the presence of CARRIER FLAG, RECEIVE O'RUN, and RING. These conditions are the status interrupts for the DP11 and use the same "B" level as the transmitter (TX DONE) interrupt level. The standard priority level is determined by the MainDEC program's reference level of 5 and is set at the BR5 level for the DP11 "A" and "B" interrupts. Though these "A" and "B" interrupts are at the same level, they are independent levels for the interrupt control. Although BR5 is a standard level, the priority levels can be changed by the user. For a more detailed description of the M7821, refer to the *PDP-11 Peripherals and Interfacing Handbook.*

4.4 CLOCK LOGIC

In both the receiver and transmitter, clocking is provided by the interfaced modem. The receiver is clocked by RECEIVE CLOCK and converted to SCR in the level converter. In the control module (see drawing D-CS-M7223-0-1 sheet 3), SCR is gated to generate the RX CLOCK signal, when the DP11 is not in maintenance mode (MAINT MODE clear). If the DP11 is operating in half-duplex mode, the RX CLOCK signal is inhibited, provided the REQUEST TO SEND signal is asserted; however, this is caused by half-duplex transmitter operation only. Half-duplex receiver operation does not inhibit the TX CLOCK signal. The transmitter clocking is initiated by TRANSMIT CLOCK off; the modem is then converted to SCT in the level converter and input to the control module. In control mode, the TX CLOCK signal is generated when the DP11 is not in MAINT MODE. Both the TX CLOCK and RX CLOCK signals are input to the respective Transmit and Receive modules to clock the data being transferred.

The DP11 can utilize an internal clocking source (DP11-KA optional) to transfer data (both receive and transmit) at desired baud rates. This clock option (M405 Crystal Clock Modules and M239 Divide By 16 Module) outputs to the level converter and generates the SCR and SCT clocking signals to the control module through the modems or null modem. The modem clocking is enabled by inserting a wire from D04S1 on the level converter to C04H1 on the modem cable connector. This option provides standard baud rates of 2400, 4800, 9600, 19.2K and 40.8K (program limited).

4.5 CONVERTER LOGIC

The converter logic for the 201 series modems consists of the M594 Level Converter Module, which converts TTL logic levels to EIA-compatible bipolar signals and vice versa. The M594 Module is shown on drawing C-CS-M594-0-1; the gating network on the right portion of the drawing converts the TTL logic levels to EIA, bipolar signals for the synchronous line. The left-hand portion of the drawing contains the gating network that converts the EIA, bipolar synchronous line signals to TTL logic levels for the DP11 logic. For the 301 and 303 series modems, Bell 301- and 303-compatible level converters are used (M595). These converters are part of the DF11 series of level converters. The 301 and 303 electrical signal specifications for level conversion are given in Appendix A; the electrical specifications for the 200 series modems (RS-232-C) including the interface pin assignments and equivalent CCITT are also provided in Appendix A.

4.6 INITIALIZATION LOGIC

When power is applied to the PDP-11 System, the computer processor generates the BUS INIT signal to all devices on the Unibus. This signal inputs the DP11 as INIT, where it generates the signals INI and CLEAR (see drawing D-BS-M7223-0-1, sheet 6). These two signals are used in the DP11 for clearing all the registers and flip-flops in the DP11 logic.

4.7 RECEIVER OPERATION

When a data channel is established between the DP11, the Unibus, and a modem, Receiver operation is initiated by addressing the Receiver registers. The RCSR is loaded with the correct character length and operating mode, and the Sync Register is loaded with the correct Sync character to be recognized. These registers are program loaded off the bus data lines and are located in the DP11 Control Module (M7223). The DP11 Receiver is now ready for data transfer; data transfer is activated by recognition of two consecutive Sync characters off the modem line. This recognition synchronizes the Receiver logic and timing for the serial-to-parallel conversion of the modem character stream. For each character (including Sync, if desired), the Receiver initiates an interrupt to transfer the character in parallel onto the bus. The Receiver can be program controlled for STRIP SYNC (bit 00 of the RCSR) which removes the Sync characters from the serial data input. Bit 12 of the RCSR indicates the character parity of each character transferred. The Sync Register receiver status conditions (RCSR) are located in the control logic (see drawing D-CS-M7223-0-1 sheets 2 through 6) as well as the gating logic for these registers and characters being transferred. The Receiver logic (see drawing D-CS-M7065-0-1) contains the logic that detects the Sync character and the logic for converting data from serial-to-parallel format. The control logic defines the interrupt to the interrupt control, which initiates the bus transfer. The following paragraphs describe in detail character length and sync character control, Sync Character detection, Receiver synchronization, and Receiver character transfer.

4.7.1 Character Length and Sync Character Control

To perform correct data transfers, the DP11 must be program-prepared with the correct character length and the correct Sync character before receiving any data from a modem. Knowledge of both of these factors enables the DP11 to synchronize properly with the modem and to convert the data characters correctly. The character length is program-loaded in the control logic off bus data lines D08, D09, and D10. The gating logic signal LD RX STAT clocks these lines into the three Bit flip-flops. These three flip-flops represent the octal code for the character length and input the BITS/CHAR DCDR. D08 is the least significant bit and the decoder outputs the signals (see drawing D-CS-M7223-0-1, sheet 5), for the six possible character lengths. The signal (decoded) generated by the decoder for the selected character length is input to the Receiver logic where it sets up the shift register to operate on the correct character length. The decoded signals 11 BITS, and 12 BITS are for the expander option to the M7065 and input the same as the 6 BIT, 7 BIT, and 8 BIT signals. The expander provides an extension of the Receiver logic for four more bits. The assertion of either 8 BIT, 7 BIT, or 6 BIT qualifies either of the gating inputs to the E3 shift register when SERIAL INPUT asserts, with SERIAL INPUT being the (control logic gated data stream) RECEIVE DATA from the modem. Therefore, the character length signals load the shift register at the proper bit position for the character length designated. For example, if an 8-bit character length is selected, the signal 8 BITS asserts and, with SERIAL INPUT, qualifies that input to the E3 portion of the receiver shift register. This input incoming bit of SERIAL DATA is loaded into E3 when E3 is clocked. When the first bit is loaded in the shift register, it is again input to the next bit position with the negation 7 BIT. At the next clock, this is loaded into the shift register at bit 7; the next bit off the data stream is loaded at bit 8. This procedure occurs at the next clock with 6 BIT negated and again for bit position 5 in the shift register at the following clock. Thus, the E3 portion of the shift register shifts through a character in this manner. Selection of a smaller character length (7 BIT or 6 BIT) causes the SERIAL INPUT data stream to enter the shift register at the respective bit position, and the E3 shifts the bits through as before. The output of bit 5 of E3 inputs the E11 portion of the shift register, which shifts the bits through to bit position 00 internally, one bit position for each clock. The clock inputs the E3 and E11 portions at pin 6.

The Sync character is loaded into the control logic (Sync Register) off the designated bus data lines (see drawing D-CS-M7223-0-1, sheets 4, 5, and 6). Sync bits 0 through 7 are loaded by the gating signal LD SYNC 0–7, and if

the expander option is employed, Sync bits 8 through 11 are loaded by LD SYNC 8–11. In either case, the Sync character must be the same value as the character to be received from the modem; it must also be the same and correct character length as the data. The contents of the Sync register are input to the Receiver logic; the contents are then compared with the incoming characters of SERIAL INPUT for Sync detection. If the proper selection of character length corresponds with the data characters, the shift register is able to correctly assemble the Sync from the modem and compare it with the Sync Register. The comparator network in the Receiver logic performs this comparison bit by bit. Therefore, Sync control and character length selection are the two major program-controlled functions for proper DP11 Receiver operation.

4.7.2 Sync Character Detection and Receiver Synchronization

Sync detection occurs when the comparator network of the Receiver logic detects a favorable comparison between the Sync Register and the contents of the shift register. For the favorable comparison to occur, the character from the modem must be assembled in the shift register. In addition to the SERIAL INPUT data stream from the modem, the modem clocking source of RECEIVE CLOCK inputs which clocks for each bit of the data stream. This clocking signal can be optionally supplied by the internal clock option. The assertion of RECEIVE CLOCK clears the E14 flip-flop, thus enabling RECEIVE CLOCK to be gated to clock the E3 and E11 shift registers. This clock also clocks the CYCLE DONE flip-flop. Meanwhile, SERIAL INPUT for each RECEIVE CLOCK pulse to the shift register inputs a bit to the shift register at the bit position qualified by the character length selection signal. When the SERIAL INPUT data stream is shifted through to fill the shift register, the entire character inputs to the exclusive Sync comparison network. This occurs for each clock until Sync is detected, which generates SYNC DET OUT. When SYNC DET OUT signal is generated, a Sync character has been found, and the logic now keys for another consecutive Sync character to fully synchronize the Receiver to an active state.

The presence of the SYNC DET OUT signal and the OFF state of the SYNC flip-flop (cleared previously by INI) direct sets the CYCLE DONE flip-flop. The setting of CYCLE DONE clocks the RBUF (DATA B0 through DATA B7), and the character is loaded into the RBUF from the shift register. This also generates REC DP, which sets the E14 flip-flop. The setting of E14 inputs two pulse circuits with a high level. A general description of the pulse circuit is contained in Appendix B. One of the pulse circuits provides a pulse that clears the shift register; the other pulse circuit provides a longer pulse that combines with the RECEIVE CLOCK pulse train, causing an additional pulse to be input to the shift register, therefore, clocking it an extra time. The previous setting of CYCLE DONE asserted an input to the SERIAL INPUT gate of the shift register. This extra clock pulse clocks in this CYCLE DONE assertion as a first bit in the most significant bit position of the shift register. This bit is used later to generate loading clock pulses to the RBUF for each data character. When CYCLE DONE has caused the clock to load the RBUF, it also clocks the SYNC flip-flop, which sets with the presence of SYNC DET OUT. The setting of SYNC disqualifies the direct input to CYCLE DONE, and CYCLE DONE then goes off at the next clock, which is the clock that loads the 1 bit in the most significant bit position of the shift register. CYCLE DONE causes only one additional clock pulse in the RECEIVE CLOCK pulse train to the shift register and only that one extra bit is loaded into the shift register.

The next character is loaded into the shift register in the same manner as the first character, with each RECEIVE CLOCK shifting the register. The logic is now searching for a second Sync character to activate the Receiver for data transfer. When the extra bit caused by CYCLE DONE of the previous character reaches the end of the shift register, shift register out is generated. The SHIFT REG OUT signal is tied back, inputting at IN LAST BIT to both receiver modules (if expander option is employed). The IN LAST BIT signal sets CYCLE DONE at the next RECEIVE CLOCK pulse. This next RECEIVE CLOCK pulse also loads the entire character into the shift register, and, if it is the second Sync character, SYNC DET OUT is generated again. The setting of CYCLE DONE (just like the first character) clocks the character to the RBUF, clears the shift register, and generates the extra clock

pulse in the RECEIVE CLOCK pulse train, which with CYCLE DONE's ON state, loads a 1 bit into the most significant bit position of the shift register designated by the character length signal. When SYNC DET OUT is generated, the clock that loads the RBUF also sets ACTIVE. The ACTIVE flip-flop is held on its 0 output, holding the clock input to ACTIVE high. The Receiver is now completely synchronized and ready to convert data and transmit it onto the bus.

4.7.3 Receiver Character Transfer

To transfer received characters from the Receiver to the bus, receive interrupts must be generated to the computer. For the interrupts to occur, the RX INTR EN signal in the RCSR must be asserted by the program. If the RX INTR EN signal is set, an interrupt condition is presented to the M7820 Interrupt Control Module when the RX DONE flip-flop sets. Therefore, the RX DONE flip-flop must be set to instruct the program to transfer data from the Receiver to the bus. The Sync characters received can be optionally transferred or not. This transfer process is controlled by the STRIP SYNC bit of the RCSR. Setting of the STRIP SYNC bit inhibits the setting of the RX DONE flip-flop for Sync characters. Consequently, when STRIP SYNC is set and SYNC DET OUT is generated, the data input to the RX DONE flip-flop is inhibited, which inhibits the transferring of Sync characters to the bus. When STRIP SYNC is clear, the input to the RX DONE flip-flop is no longer inhibited. This STRIP SYNC bit in the RCSR is program-controlled and loaded off the bus data lines with LD RX STAT. To transfer the Sync characters to the bus, the third and future Sync characters will be transferred, because the ACTIVE flip-flop must set to enable the setting of the RX DONE flip-flop. In the Sync detection area, the ACTIVE flip-flop is set only for the second Sync character. However, there can be as many Sync characters above two as desired, and they are recognized as such and either transferred or not according to the STRIP SYNC state. The setting of the RX DONE flip-flop, therefore, occurs only when the ACTIVE flip-flop asserts and when REC DP clocks it. The REC DP clock occurs when the contents of the shift register is clocked to the RBUF. Therefore, because the ACTIVE flip-flop remains set until cleared by the program, REC DP sets the RX DONE flip-flop as each character is loaded into the RBUF (DATA B0 through DATA B11). Each character of data is operated on in the Receiver logic in the same manner as the second Sync character; thus, CYCLE DONE generates REC DP to set RX DONE, to load the RBUF, and to generate the extra clock pulse that loads an extra bit into the shift register, which sets CYCLE DONE for the next character.

The setting of the RX DONE flip-flop initiates the interrupt for removing the character from the RBUF and asserting it on the bus. The interrupt communications has one character time for the computer to take the character; otherwise, a data overrun occurs (RX O'RUN). The computer takes the character from the RBUF through the selection signal DATA TO BUS. The DATA TO BUS signal, when generated, also clears the RX DONE flip-flop. If the DATA TO BUS signal has not returned to clear the RX DONE flip-flop when REC DP asserts to set RX DONE for the next character, RX O'RUN is set in the control logic. This condition, with INTR EN (STATUS) set in the TCSR, causes a status interrupt to be generated to the computer.

The control logic of the DP11 also parity checks each character and indicates the character parity for received characters in the CHARACTER PARITY bit of the RCSR (bit 12). In the control logic (see drawing D-CS-M7223-0-1, sheet 3), the ONES flip-flop sets for each one bit of SERIAL INPUT and is clocked by RECEIVE CLOCK. The output of ONES is PARITY COUNT which clocks the COUNT ONES flip-flop (sheet 6). Whenever the COUNT ONES flip-flop is set, the character has an odd number of ones at that point. When REC DP asserts indicating the word is fully assembled in the Receiver, it clocks the ODD PARITY flip-flop with the state of the COUNT ONES flip-flop. If the COUNT ONES was set, then ODD PARITY sets and the character has odd parity and CHARACTER PARITY is set in the RCSR. REC DP also clears COUNT ONES for the next character. If COUNT ONES was off when REC DP asserted, ODD PARITY would not set and the CHARACTER PARITY would be even.

4.8 TRANSMITTER OPERATION

When a data channel is established between the modem, the DP11, and the Unibus Transmitter, operation is initiated by addressing the transmitter registers. Through the gating logic, the Transmitter status is program-loaded (TCSR). Also, the character length is program-chosen, and the Sync character is loaded into the Sync Register bits. These bits are loaded in the M7223 Control Module off the bus data lines. The addressing of the transmitter also generates the TX LD signal, which initiates the Transmitter logic. The DP11 Transmitter is now ready for data transmission and activation of the modem. The Transmitter logic generates a REQUEST TO SEND signal to modem; the modem returns CLEAR TO SEND and activates the transmission of characters to the modem. Initial transmission should be multiple Sync characters, which are followed by the transmission of data characters to the modem. The choice of character length sets up the Transmitter shift register at the correct character limit for converting the character from parallel-to-serial format. Transferring a character from the transmit buffer (TBUF) to the shift register initiates an interrupt to the computer for loading the next character into the TBUF (D00 through D11). The Transmitter can be operated in either a normal mode or with the IDLE SYNC bit set in the TCSR (bit 01). The IDLE SYNC bit causes the transmission of the contents of the Sync Register if the program has not loaded the next character into the TBUF in 1 character time (refer to Paragraph 3.2.4). The Sync Register and Transmitter status conditions (TCSR) are located in the M7223 Control Logic (see drawing D-CS-M7223-0-1, sheets 2 through 6) as well as the gating logic. The Transmitter logic (see drawing D-CS-M7075-0-1) contains the logic that provides for IDLE SYNC operation and converts parallel data to serial format. The control logic also defines the Transmitter interrupt to the M7820 Interrupt Control Module to initiate bus transfer. The following paragraphs describe in detail Transmitter initiation, character length control, transmitter transfer, and IDLE SYNC control.

4.8.1 Transmitter Initiation

To initiate the Transmitter logic, the TX LD signal must be generated from the gating logic of the control module. This signal is generated for each character addressed to the TBUF by the Selection logic. The TX LD signal direct sets the CHAR RDY SYNC flip-flop (see drawing D-CS-M7075-0-1) and clocks the character into the TBUF (D00 through D11) from the bus. On the next negative transition of the TRANSMIT CLOCK from the modem (or optional internal clock), CHAR RDY sets. The setting of the CHAR RDY flip-flop qualifies the output multiplexer gates of the TBUF to the inputs of the shift register (E3 and E13). Also, the CHAR RDY flip-flop generates a REQUEST TO SEND signal on the modem line two TRANSMIT CLOCK pulses later. The transmitter now waits for the return of a CLEAR TO SEND signal from the modem to begin converting data characters to serial format and transmitting them to the modem line.

4.8.2 Character Length Control

The selected character length signal from the control logic inputs the transmitter logic to establish the bit positions of the transmitter shift register (E3, E13). These character length signals are the same as those for the Receiver with the 10-, 11-, and 12-bit character length signals inputting the Transmitter Expander option. Selection of 8 BITS qualifies the inputs to the E4 flip-flop with CHAR RDY set and the shift register clear. When a CLEAR TO SEND signal is asserted from the modem, the direct clear input is unasserted and the E4 sets. The setting of E4 inputs a 1 to pin 4 of the E3 portion of the shift register on the next TRANSMIT CLOCK pulse. If 8 BITS is not the character length chosen, the E4 flip-flop will not set at all. Thus, inputting a 1 is similar to the function of the extra bit in the Receiver logic only in the transmitter the 1 trails the character through the shift register. When this extra bit reaches the bit 1 position (D01), END CYCLE OUT asserts, indicating the last bit has been presented to "DATA OUT". The assertion of 7 BITS or 6 BITS also generates this trailing bit. If 7 BITS is chosen, the D07 (eighth bit position) is inhibited by 7 BITS. Also at this D07 bit position, 7 BITS asserts a 1 to the shift register.

This 1 is the extra trailing bit that defines the end of the character. The 6 BITS signal does the same for the next least significant bit position, D06. These extra trailing bits are loaded when the character is loaded into the shift register from the TBUF. This loading is enabled by the return of a CLEAR TO SEND signal, which begins the data transfer to the modem line.

4.8.3 Transmitter Transfer

When a CLEAR TO SEND signal is asserted from the modem, the ACTIVE flip-flop is set at the next positive transition of the TRANSMIT CLOCK pulse. The CLEAR TO SEND signal also qualifies the gating that inputs the shift register at pin 13. This input, through its input gating, is normally high and is defined as the shift enable input; i.e., when this input is asserted high, each clock causes the shift register to shift. When a CLEAR TO SEND signal is asserted and the CHAR RDY flip-flop is already set, the presence of an END CYCLE OUT H signal (indicates shift register is empty) causes the shift input to go low, which turns off the shifting and enables loading of the shift register in parallel. The shift register, therefore, is loaded with contents of the TBUF (or Sync Register) at the next clock. This same TRANSMIT CLOCK loads a trailing bit into the flip-flop associated with the 6, 7, or 8 bits of selected input. If 8 BITS is the selected character length, the clock that loads the shift register loads the 8-bit extra trailing bit. The next clock pulse performs the first shift on the loaded character. In order for the shift register to resume shifting, the shift input (pin 13) must return high. This occurs as soon as the shift register is loaded with the character, causing END CYCLE OUT to go unasserted. This disqualifies the input gate to the shift input. For each character, END CYCLE OUT asserts to enable loading as the extra trailing bit moves to bit 01 position in the shift register (D01), and then unasserts as the shift loads a new character. END CYCLE OUT is generated by the hard-wired OR function of bit positions 2 through 7 of the shift register; therefore, it is asserted only when all of these bits are 0.

When the character is loaded into the shift register, the unasserted state of END CYCLE OUT returns the shift input to the shift register and also causes CHAR RDY SYNC to clear. On the next negative transition of the clock, CHAR RDY clears. This occurs if no new character is loaded. When END CYCLE OUT goes low indicating that shift is loaded, the first bit is presented to the modem line. The CHAR RDY SYNC low transition direct sets the TX DONE flip-flop in the control logic, which with TX DONE INT EN set, causes an interrupt request through the M7820 Interrupt Control Module. This interrupt requests the assertion of another character on the bus data lines for loading (TX LD) into the TBUF. TX LD is generated from the address lines of the character, and the new character is loaded into the TBUF (D00 through D07). This new character and TX LD must be presented to the transmitter within one character time of the assertion of DONE.

When the character in the shift register is shifted up so the trailing bit reaches bit 01, END CYCLE OUT asserts again, generating another low to the shift input of the shift register, and the last word from the buffer is loaded.

During the shifting, END CYCLE OUT low cleared the CHAR RDY SYNC, which, in turn, cleared CHAR RDY. When END CYCLE OUT goes high to load the last word, the input to E5 Pin 2 is disabled. Loading the last word into the shift register causes END CYCLE OUT to go low again until the last bit is presented to DATA OUT L, where it goes high again. Now loading the shift register is disabled, because no new word has been loaded and, therefore, END CYCLE OUT remains high. The REQUEST TO SEND signal is dropped, because CHAR RDY clears when END CYCLE OUT is asserted to disable the SEND RQSR input. To resume transferring, the Transmitter logic must be reinitiated to generate a REQUEST TO SEND signal and to receive a CLEAR TO SEND signal.

The first two characters (minimum) transferred when a CLEAR TO SEND signal activates the shift register loading should be Sync characters. These characters synchronize the modem that is to receive transmission. Therefore, if the Transmitter is not loaded in time with another character, the Transmitter must be initiated again by trans-

mitting two consecutive Sync characters. This process is carried out by the program, and the Sync characters are loaded in the same manner as data characters, i.e., off the bus data lines into the TBUF. The Sync characters are also used to prevent the shutting down of the Transmitter if a late character occurs when IDLE SYNC is set (refer to Paragraph 4.8.4).

When the interrupt caused by TX DONE inputs a new character in sufficient time, TX LD again sets CHAR RDY SYNC, which, in turn, sets CHAR RDY on the next negative transition of TRANSMIT CLOCK. This new TX LD can assert before END CYCLE OUT's low transition, and the next negative clock transition can cause the CHAR RDY flip-flop to clear. In either case, if no character is late, either CHAR RDY or END CYCLE OUT holds the REQUEST TO SEND signal asserted, which causes a CLEAR TO SEND signal to stay asserted and the ACTIVE flip-flop remains set. These two maintained conditions keep the input gate to shift register pin 13 (shift) input qualified; thus, the END CYCLE OUT transitions load the shift register for each character. This process continues until the computer stops transmitting characters, whereupon the transmitter action stops.

4.8.4 IDLE SYNC Control

When the programmer sets the IDLE SYNC bit of the TCSR in the control logic, the input gating to the shift input (pin 13) of the shift register remains qualified. Therefore, a REQUEST TO SEND signal is held asserted, and a CLEAR TO SEND signal remains input to the Transmitter from the modem. When CHAR RDY clears due to END CYCLE OUT going low, the input parallel gating multiplexers to the shift register data inputs are disqualified. When they are qualified, the contents of the Sync Register are made available to the parallel inputs of the shift register. When a new character has not been loaded, CHAR RDY does not reassert to gate the D00 through D07 lines to the shift register, and END CYCLE OUT going high enables the loading of the shift register on the next TRANSMIT CLOCK pulse with the contents of the Sync Register. This process occurs because IDLE SYNC was asserted, allowing the low pulse to the shift input when END CYCLE OUT goes high, which enables the loading of the shift register. Therefore, with IDLE SYNC set, any missed words are substituted by the Sync character to maintain transmitter operation without re-initiation.

When the transmitter is inactive, the assertion of IDLE SYNC will generate a REQUEST TO SEND signal with TRANSMIT CLOCK. A CLEAR TO SEND signal coming back causes the shift register to load on the next TRANSMIT CLOCK. Because CHAR RDY is off, the shift register loads with the contents of the Sync Register. This character shifts out the shift register, and END CYCLE OUT going high loads the Sync again. This procedure continues until IDLE SYNC is clear, which is a program function. Thus, setting the IDLE SYNC bit of the TCSR causes the transmission of Sync characters when the transmitter is inactive. Also, when the transmitter is active, IDLE SYNC transmits Sync characters when the TBUF is not refreshed in time with the next character.

4.8.5 Half-Duplex Operation

When the HALF-DUPLEX bit of the RCSR in the control logic is set, the DP11 is prohibited from performing simultaneous Receive and Transmit operations. This condition is achieved by inhibiting the RECEIVE CLOCK signal whenever transmission is occurring with HALF-DUPLEX set. Half-duplex operation is necessary because some modems and modem configurations prohibit full-duplex communications and can only perform half-duplex communications. In the control logic (see drawing D-CS-M7223-0-1, sheet 3), the setting of HALF-DUPLEX disables the generation of RECEIVE CLOCK, whenever SEND REQUEST is generated. SEND REQUEST indicates a Transmit function and, therefore, the Receive function is prohibited. If no Transmit function is occurring, SEND REQUEST is unasserted and RECEIVE CLOCK is not inhibited.

4.9 MAINTENANCE MODE

The maintenance mode is used to check (off-line) the operation of the DP11 logic. Maintenance mode is program-initiated by setting bit 02 of the RCSR in the control logic. In maintenance mode, when a character is loaded into the TBUF off the bus, the transmitted serial data is fed back into the Receiver, which is then converted back into parallel data. If the character received by the bus is identical to the transmitted character, then both the transmitter and receiver are functioning properly. This maintenance mode of operation is utilized by the diagnostic programs discussed in Chapter 5.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

Maintenance can be performed on the DP11 by using the diagnostic programs supplied with the unit. A diagnostic program consists of a tape and a printout containing descriptions and explanations of the diagnostic tests. The diagnostic performs two types of tests: Internal Loop for ON-LINE/OFF-LINE testing and External Loop for OFF-LINE testing exclusively. Each test is performed as outlined in the instructions supplied with the diagnostic (MainDEC-11-D8DA).

A diagnostic test is valid if five or more passes are performed without the occurrence of an error.

NOTE
If the S1 jumper at F03 and D03 is used in the particular system, it must be removed to operate the MainDEC-11-D8DA diagnostic. This jumper selects RECEIVE ACTIVE on one sync character.

5.2 INTERNAL LOOP TEST

The Internal Loop test (engaged by the Maintenance Mode bit of the RCSR) ties the transmitter output to the Receive Input. Additionally, the CLEAR TO SEND lead is simulated (allows the transmitter to shift), and the Transmit/Receive Clocks are replaced by a 3000-Hz Clock. The Internal Loop, coupled with the Read/Write Status bits, tests approximately 85% of the hardware of the DP11.

5.3 EXTERNAL LOOP TEST

The External Loop test utilizes a test connector to return the Transmit Data and Control (out) as Receive Data and Control (in). In this configuration, the Secondary Transmit lead (status bit noted as Miscellaneous Transmit) is returned to perform the Transmit and Receive Clock function. Table 5-1 illustrates how the data and control leads are affected by the test connector supplied with the DP11-DA. The connector types and pinning change for the DP11-DB and DP11-BC.

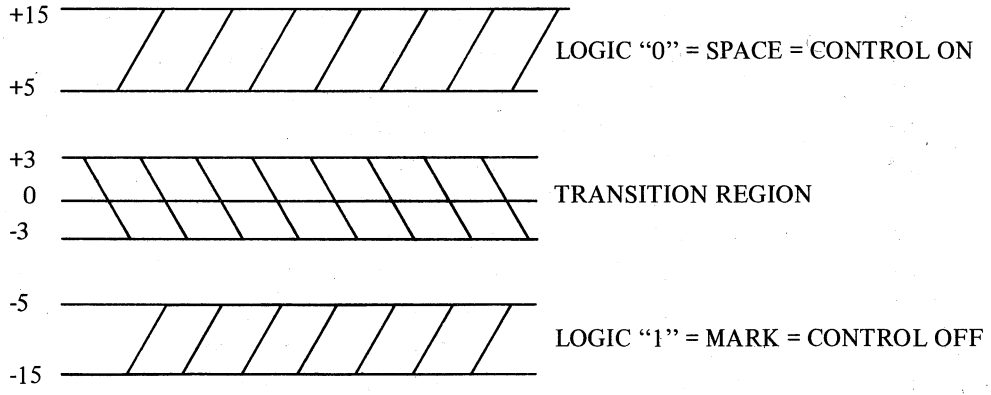
Table 5-1
Test Connector Configuration

DP11 Interface	Cable and Terminating Connector (DB25P or Burndy)	Test Connector (DB25S)	Connector (Burndy)
SEND REQUEST	→	4	D
CLEAR TO SEND	←	5	C
INTERLOCK DATA SET RDY	←	6	F
SEND DATA	→	2	E
REC DATA	→	3	K
SEC'Y TRANSMIT	→	11	B
SERIAL CLOCK RECEIVE	←	17	L
SERIAL CLOCK TRANSMIT	←	15	J
TERMINAL READY	→	20	M*
CARRIER/AGC	←	8	M
RING	←	22	F*
			*Outer Conductor

APPENDIX A
DP11 OPTION SPECIFICATIONS

A.1 RS-232-C ELECTRICAL SPECIFICATIONS

Driver output logic voltage levels with 3K to 7K load	$15V > Vo > 5V$ $-5V > Vo > -15V$
Driver output voltage with open circuit	$\|Vo\| < 25V$
Driver output impedance with power off	$20 > 300\Omega$
Output short circuit current	$I_o < 0.5A$
Driver slew rate	$\frac{dv}{dt} < 30V/\mu s$
Receiver input impedance	$7K\ \Omega > Rin > 3K\Omega$
Receiver input voltage	±15V compatible with driver
Receiver output with open circuit input	Mark
Receiver output with 300Ω to ground on input	Mark
Receiver output with +3V input	Space
Receiver Output with -3V input	Mark



A.2 EIA RS-232-C INTERFACE PIN ASSIGNMENTS

Pin Number	Circuit	Description
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send

Pin Number	Circuit	Description
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal ground (common return)
8	CF	Received Line Signal
9	–	(Reserved for Data Set Testing)
10	–	(Reserved for Data Set Testing)
11	–	Unassigned
12	SCF	Sec. Rec'd Line Sig. Detector
13	SCB	Sec. Clear to Send
14	SBA	Secondary Transmitted Data
15	DB	Transm. Signal Element Timing (DCE Source)
16	SBB	Secondary Received Data
17	DD	Received Signal Element Timing (DCE Source)
18	–	Unassigned
19	SCA	Secondary Request to Send
20	CD	Data Terminal Ready
21	CG	Signal Quality Detector
22	CE	Ring Indicator
23	CH/CI	Data Signal Rate Selector (DTE/DCE Source)
24	DA	Transmit Signal Element Timing (DTE Source)
25	–	Unassigned

A.3 EIA (RS-232-C) TO EQUIVALENT CCITT

Interchange Circuit	CCITT Equivalent	Description
AA	101	Protective Ground
AB	102	Signal Ground/Common Return
BA	103	Transmitted Data
BB	104	Received Data
CA	105	Request to Send
CB	106	Clear to Send
CC	107	Data Set Ready
CD	108.2	Data Terminal Ready
CE	125	Ring Indicator
CF	109	Received Line Signal Detector
CG	110	Signal Quality Detector
CH	111	Data Signal Rate Selector (DTE)
CI	112	Data Signal Rate Selector (DCE)
DA	113	Transmitter Signal Element Timing (DTE)
DB	114	Transmitter Signal Element Timing (DCE)
DD	115	Receiver Signal Element Timing (DCE)
SBA	118	Secondary Transmitted Data
SBB	119	Secondary Received Data
SCA	120	Secondary Request to Send
SCB	121	Secondary Clear to Send
SCF	122	Sec. Rec'd Line Signal Detector

A.4 CURRENT MODE ELECTRICAL SPECIFICATIONS

(Applicable to the Bell 300 series modem or equivalent)

Receiver input current/voltage levels with 100 Ω termination:

MARK	5 mA (-0.7<Eo<1)
SPACE	23 mA (Ein>1)

Driver output impednace with power off:

Not specified

Driver output short circuit current:

Not specified

Driver slew rate between the 7 mA and the 21 mA levels:

Typical	14 mA/100 ns
MAX	14 mA/50 ns
MIN	14 mA/200 ns

Receiver input Impedance:

120>Zin>90

Receiver output with open circuit input:

Logic 1 – MARK-OFF

Receiver output with input >23 mA:

Logic 0 – SPACE – ON

Receiver output with input <5 mA:

Logic 1 – MARK – OFF

Driver distortion limits:

Mark-to-space or space-to-mark must be achieved within 25% of bit interval.

Receiver Open Circuit Voltage:

0.8V to -1.3V

APPENDIX B
PULSE DELAY CIRCUIT

B.1 PULSE DELAY CIRCUIT

The pulse delay circuit is used in numerous areas throughout the DP11 logic. An explanation of the pulse delay circuit is required to understand the DP11 logic. Assume initially that the input line 1 (see Figure B-1) is low. If line 1 is low, the inverter on line 2 has that input high. When line 1 goes from a low-to-high transition, the state of line 1 immediately goes high. Because line 2 is already high, the output of the AND gate goes from a high-to-low transition. The low-to-high input transition is inverted by the inverter to a low and then delayed by the RC circuit at line 2. The extent of this delay is determined by RC time constant. In this case, the time constant is approximately 100 ns. Therefore, after approximately 100 ns line 2 will go low causing the AND output to go high again. Thus, this circuit generates a 100 ns (variable with C) low pulse for each low-to-high input transition.

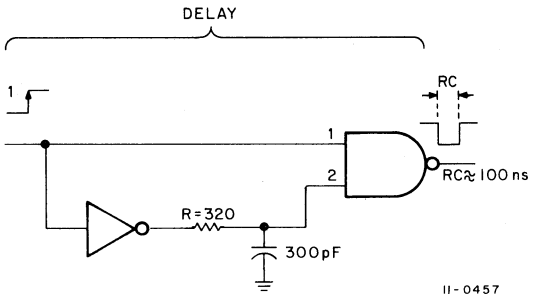
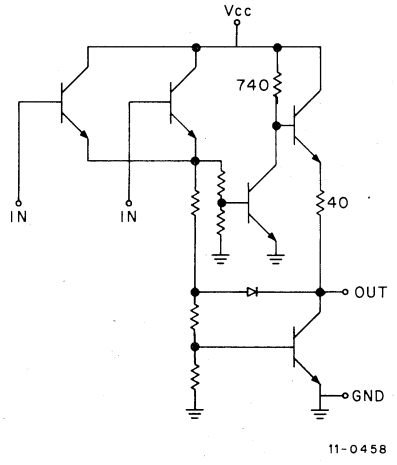
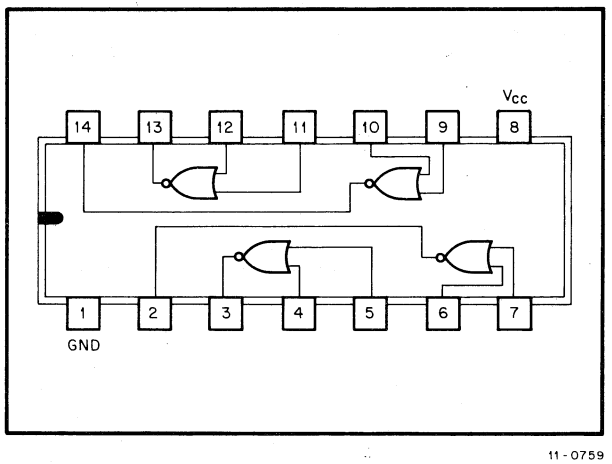


Figure B-1 Pulse Delay Circuit

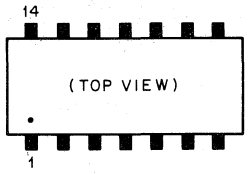
APPENDIX C
DP11 INTEGRATED CIRCUITS

380 QUAD 2-INPUT NOR GATE

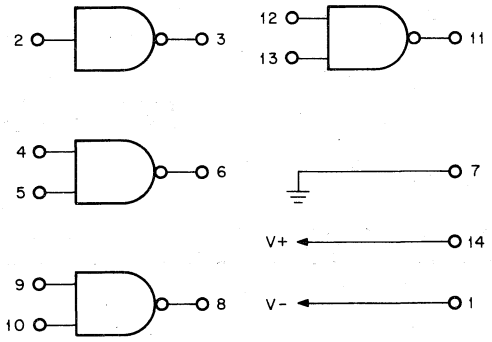




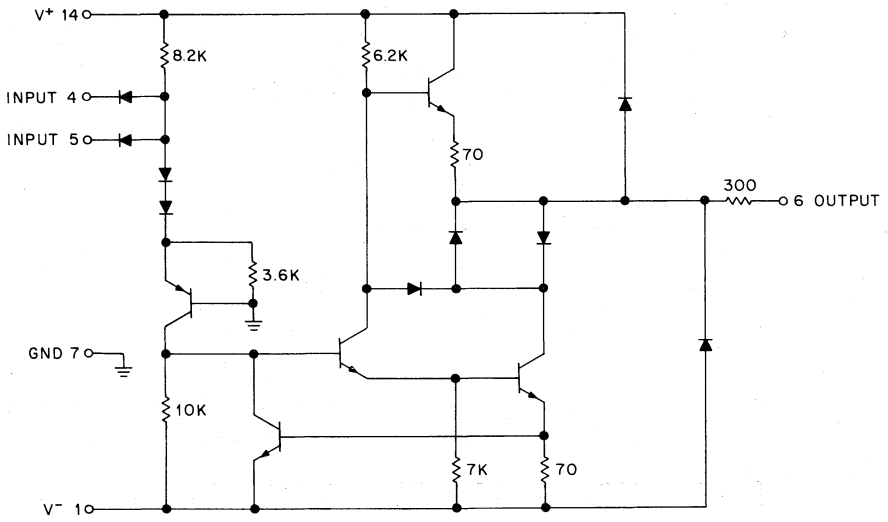
MC1488L QUAD LINE DRIVER



11-0486



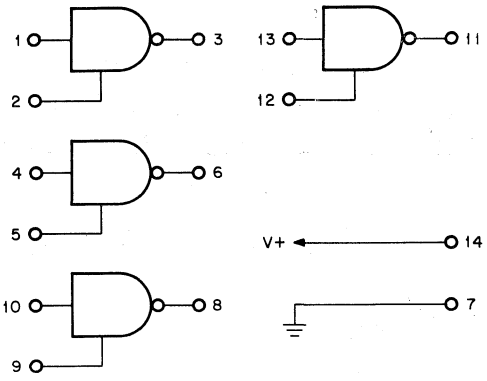
11-0459



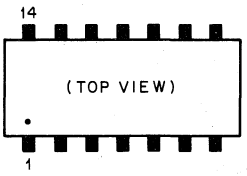
NOTE:
1/4 of circuit shown.

11-0760

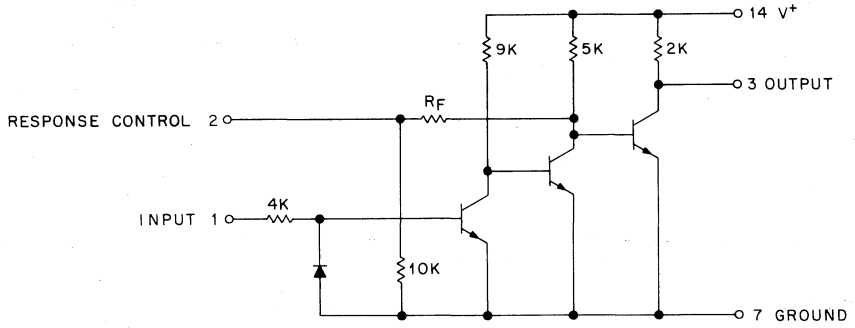
MC1489 QUAD LINE RECEIVER



11-0460



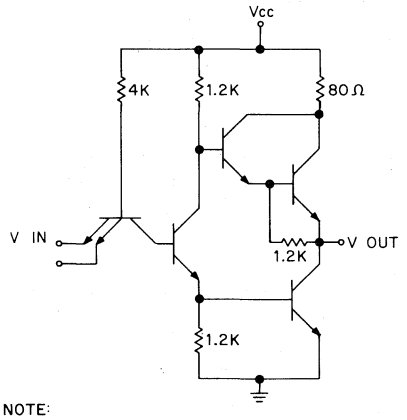
11-0486



NOTE:
1/4 of circuit shown.

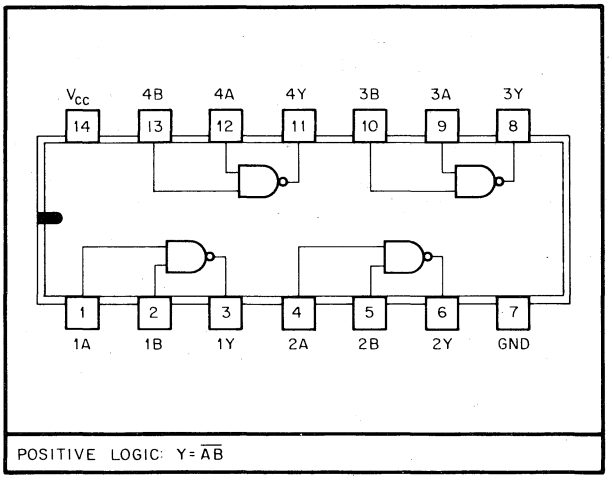
11-0761

7400 QUAD 2-INPUT POSITIVE NAND GATE



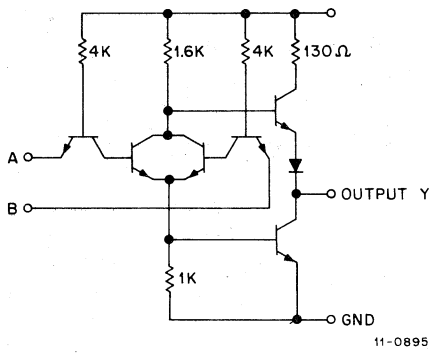
NOTE:
Component values are typical.

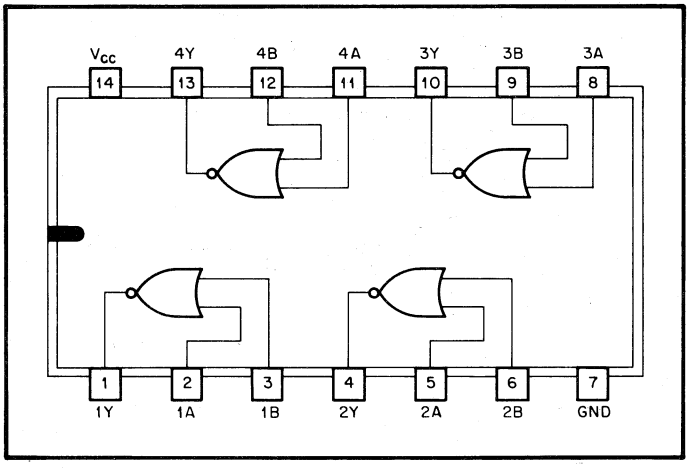
11-0461



11-0762

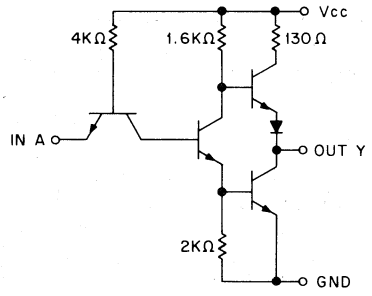
7402 QUAD 2-INPUT POSITIVE NOR GATE





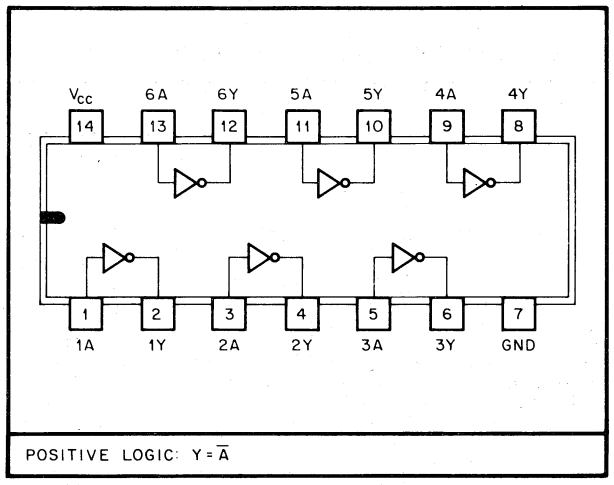
7404 HEX INVERTER

Schematic (each inverter)

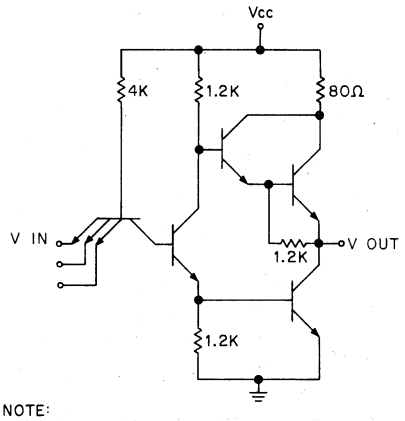


NOTE:
Component values shown are nominal.

11-0463

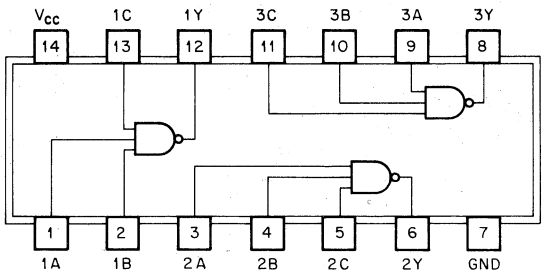


7410 3-INPUT POSITIVE NAND GATES



NOTE:
Component values are typical.

11-0464

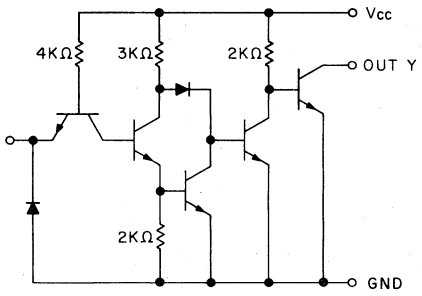


POSITIVE LOGIC: $Y = \overline{ABC}$

11-0764

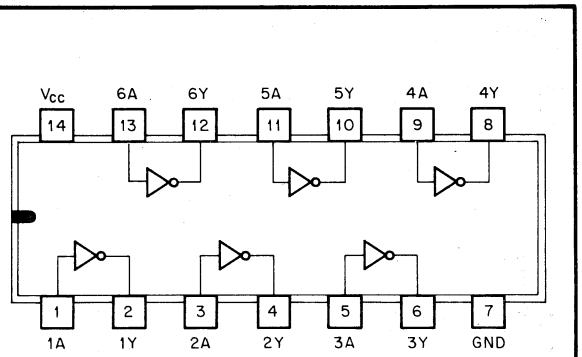
7416 HEX INVERTER BUFFERS/DRIVERS

Schematic (each inverter)



NOTE:
Component values shown are nominal.

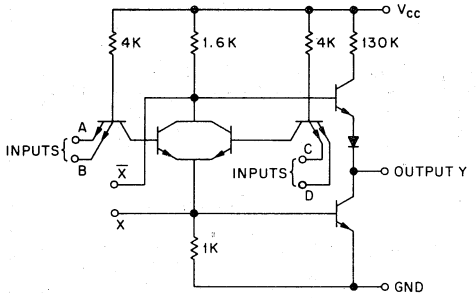
11-0465



POSITIVE LOGIC: $Y = \overline{A}$

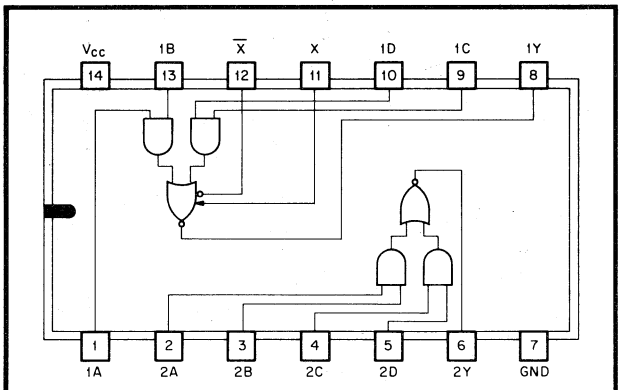
11-0765

7450 EXPANDABLE DUAL 2-WIDE, 2-INPUT AND-OR-INVERT GATES



NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave x and $\overline{x}$ pins open.
4. A total of four expander gates can be connected to the expander inputs.

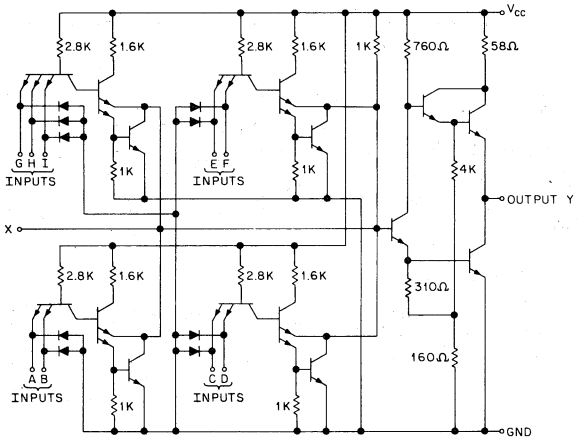
11-0899



POSITIVE LOGIC: $Y = \overline{(AB) + (CD) + (X)}$

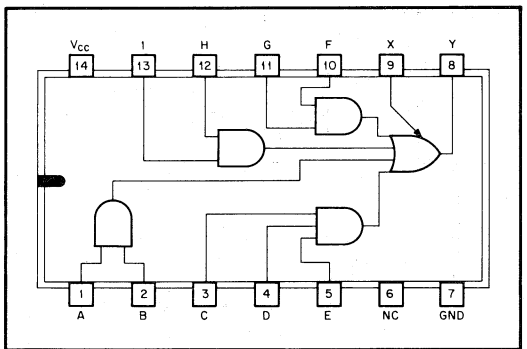
11-0900

74H52 EXPANDABLE 2-2-2-3-INPUT AND-OR GATES



NOTES:
1. Component values shown are nominal.
2. A total of six expander gates may be connected to the expander input X.
3. NC-No internal connection.

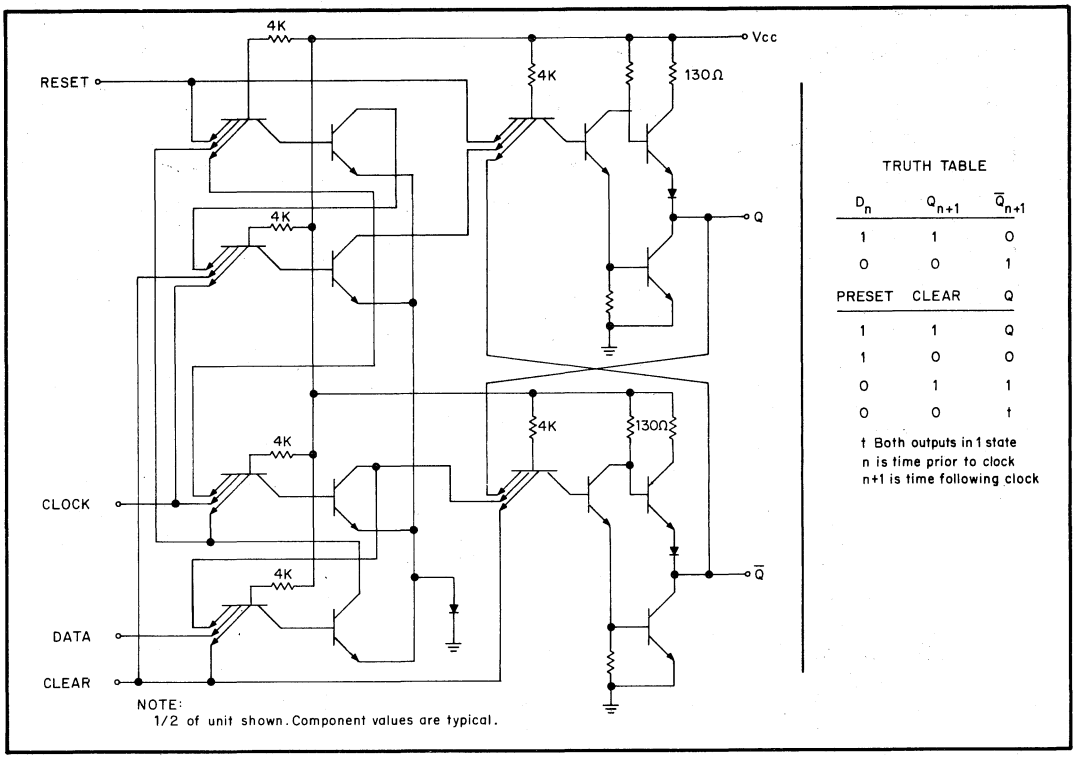
11-0897



POSITIVE LOGIC: $Y = (AB) + (CDE) + (FG) + (HI) + (X)$

11-0898

7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

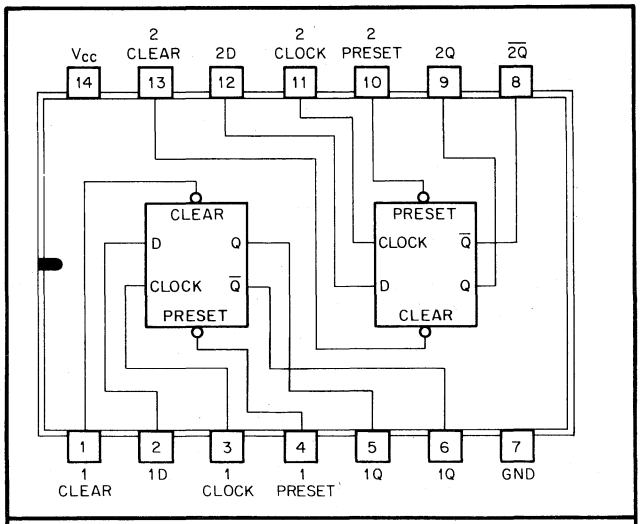


TRUTH TABLE

D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1
PRESET	CLEAR	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state
n is time prior to clock
n+1 is time following clock

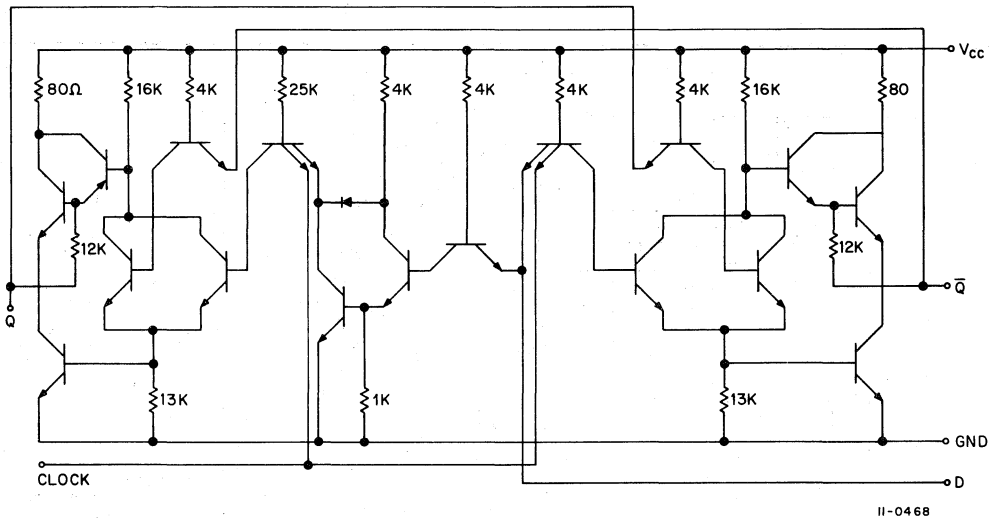
11-0469



POSITIVE LOGIC: LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

11-0766

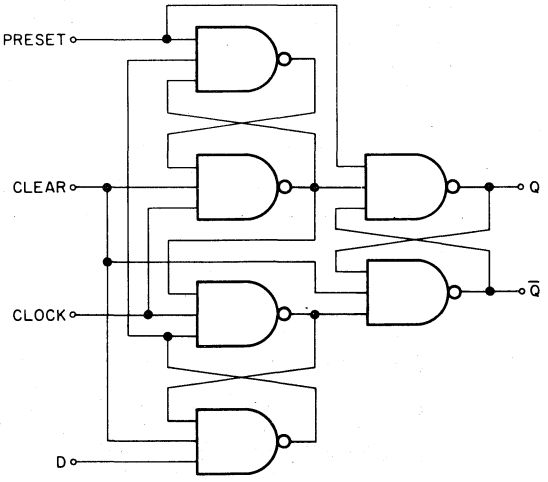
7475 QUAD BISTABLE LATCH



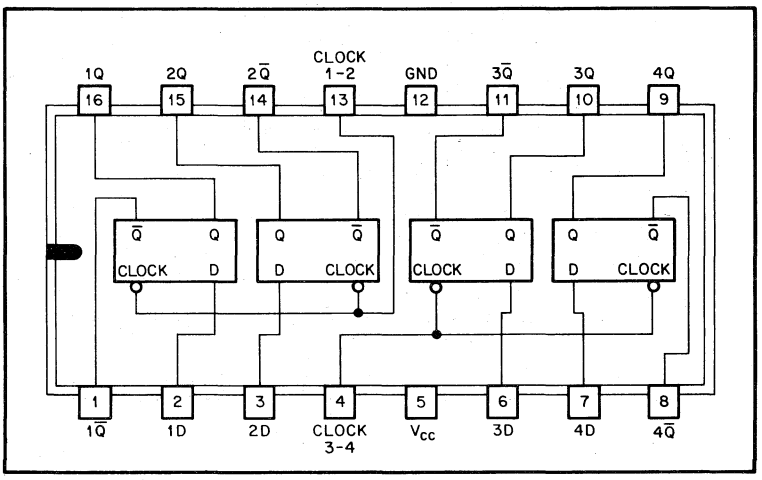
11-0468

TRUTH TABLE
(Each Latch)

t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1



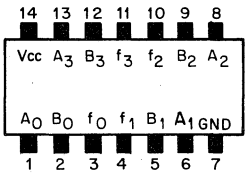
11-0767



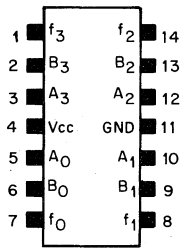
11-0894

8242 4-BIT DIGITAL COMPARATOR (QUAD EXCLUSIVE-NOR)

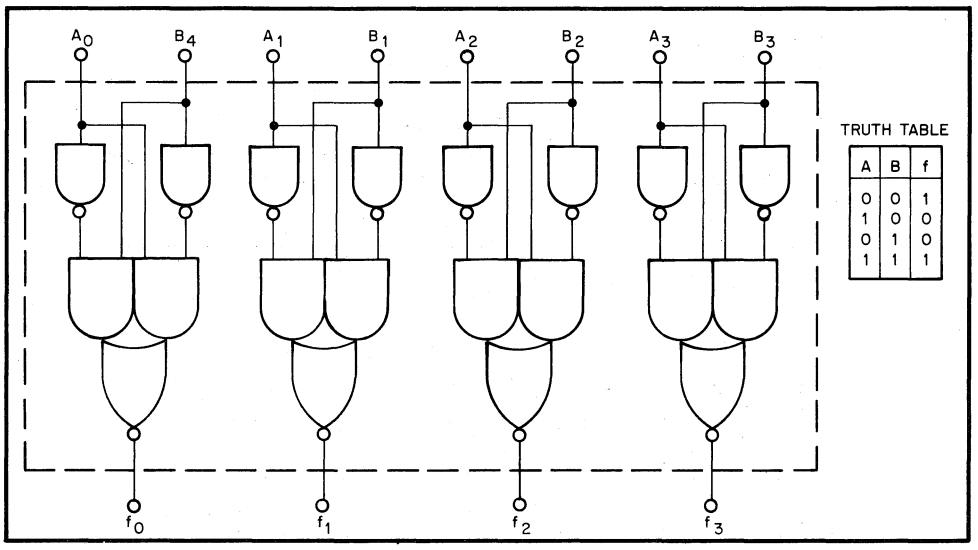
A or F PACKAGE



Q PACKAGE



11-0474

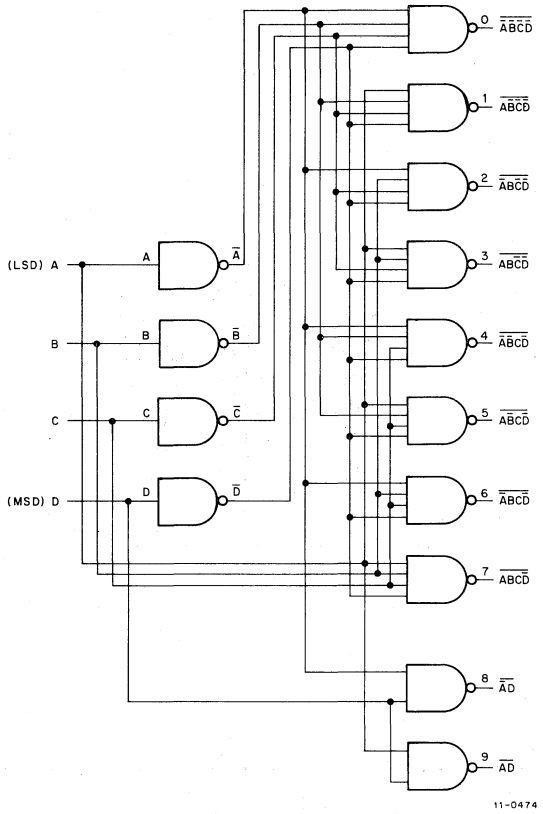


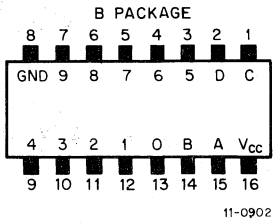
TRUTH TABLE

A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

11-0472

8251 BCD-TO-DECIMAL DECODER

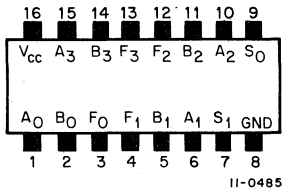




TRUTH TABLE

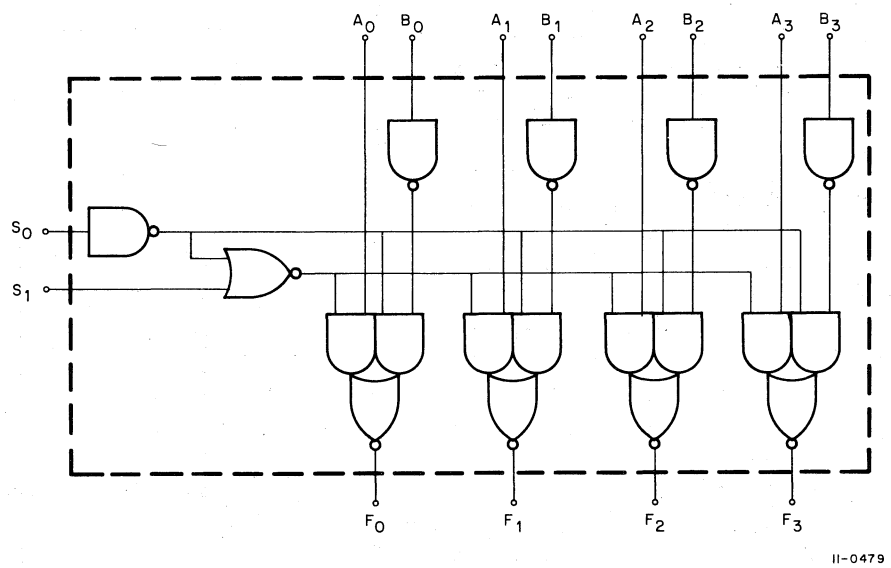
Input State				8251 Output States									
A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0

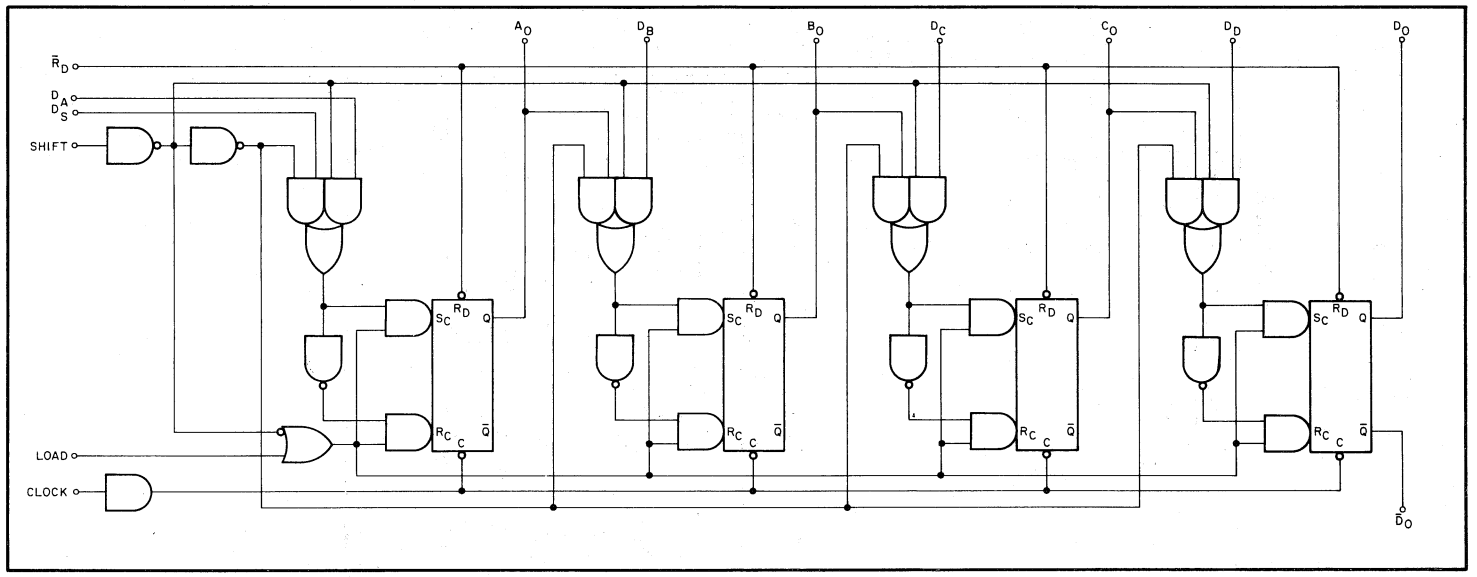
8266 2-INPUT, 4-BIT DIGITAL MULTIPLEXER



TRUTH TABLE

Select Lines		Output
S_0	S_1	f_n (0,1,2,3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	I



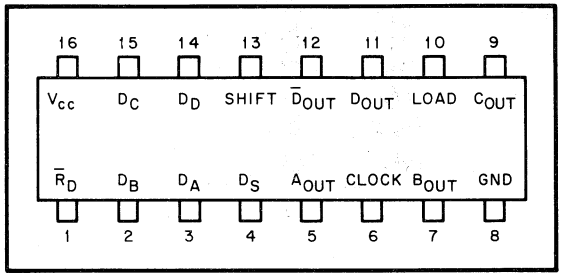


12-0327

TRUTH TABLE

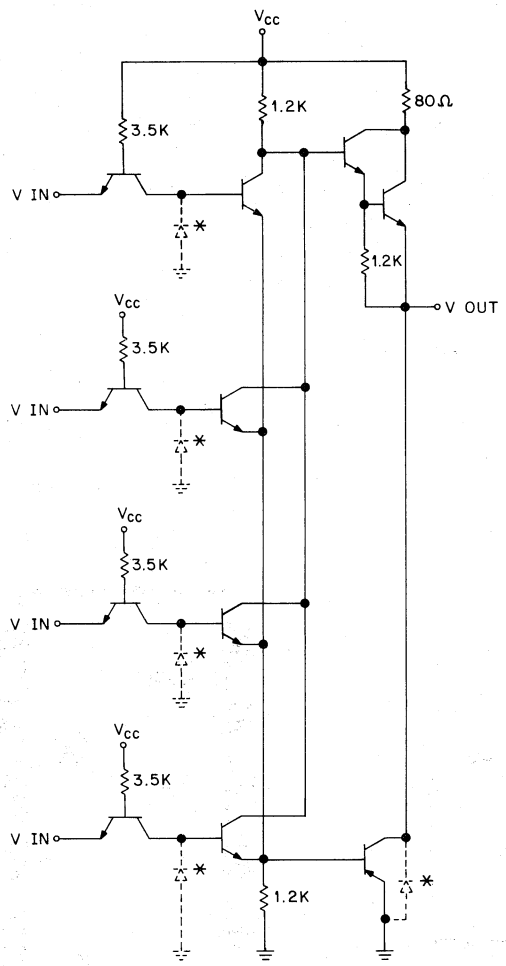
Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

8271B



12-0322

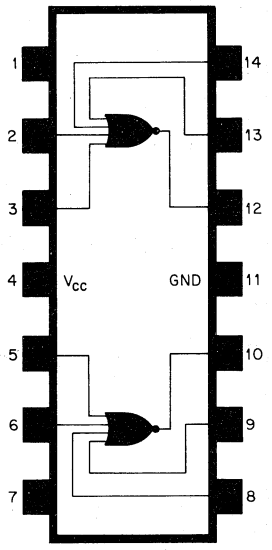
8815 DUAL 4-INPUT NOR GATE



NOTE:
Component values are typical

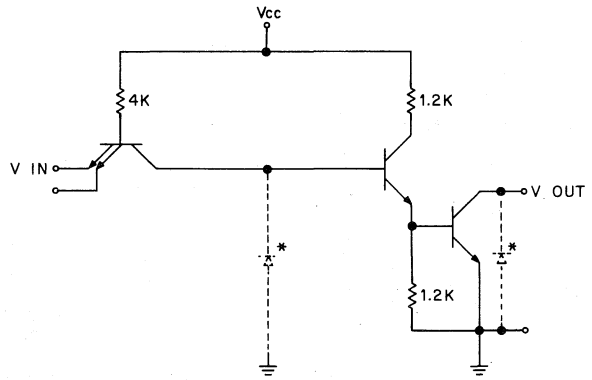
* Isolation Diode

11-0901



11-0757

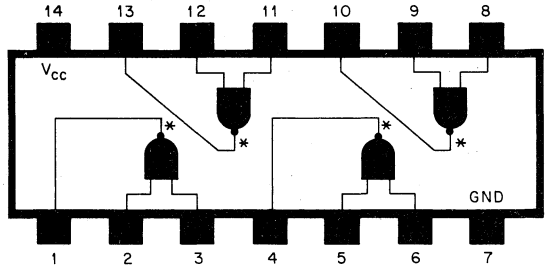
8881 QUAD 2-INPUT NAND GATES



NOTE:
1/4 of unit shown. Component values are typical.
*ISOLATION DIODE

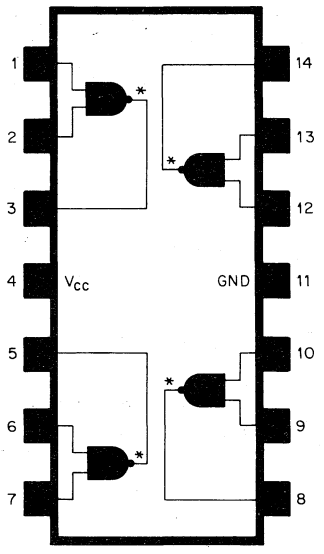
11-0480

A, F PACKAGE



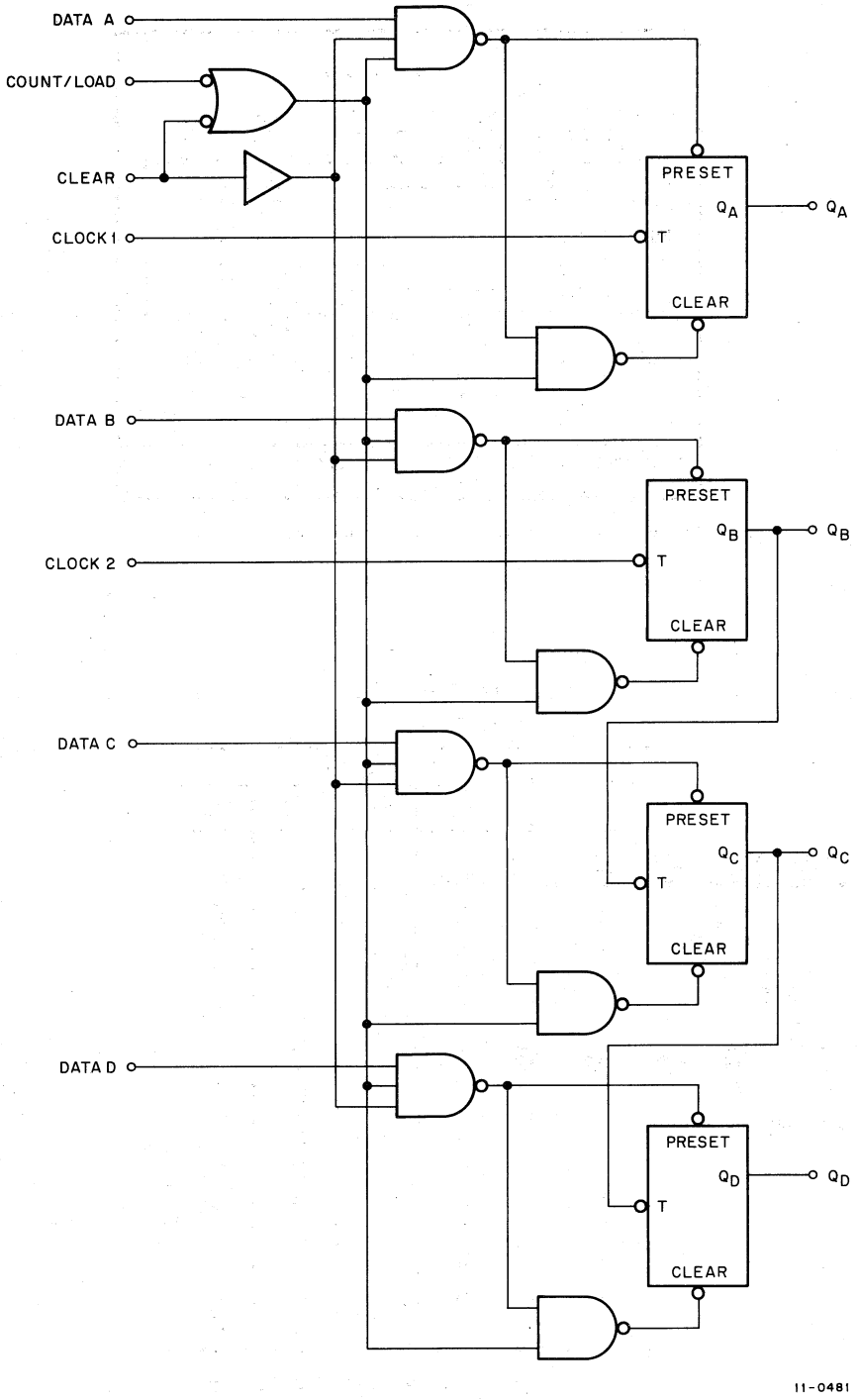
*No pull-up provided

J PACKAGE

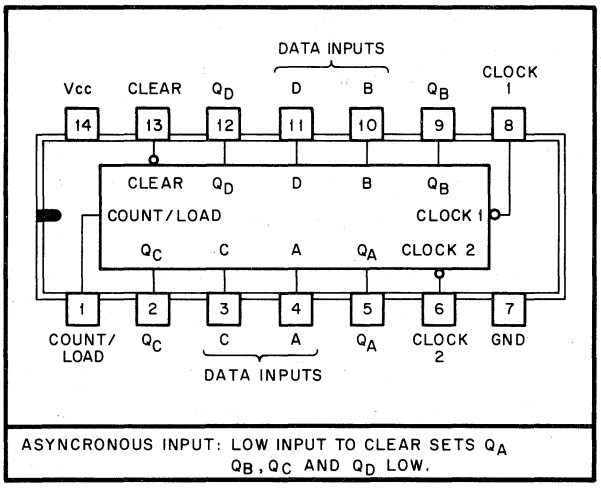


11-0758

74197 50-MHz PRESETTABLE DECADE AND BINARY COUNTER/LATCH



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A Q_B, Q_C AND Q_D LOW.

*Pin assignments for these circuits are the same for all packages.

11-0482

74197 TRUTH TABLE

(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.

READER'S COMMENTS

DP11-A ASYNCHRONOUS COMMUNICATIONS INTERFACE
DEC-11-HDPAA-C-D

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