M2351A/AF MINI-DISK DRIVE

CE MANUAL

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INTRODUCTION

This manual is for customer engineers who handle the new Mini-Disk Drive M2351A/AF. It describes how to operate, handle and maintain the drive.

This manual consists of the following seventeen chapters.

Chapter	1	GENERAL INFORMATION
Chapter	2	INSTALLATION
Chapter	3	OPERATION AND CHECKOUT
Chapter	4	SYSTEM INSTALLATION
Chapter	5	MECHANICAL ASSEMBLIES
Chapter	6	DATA FORMAT
Chapter	7	INTERFACE
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Chapter	10	READ/WRITE CIRCUIT
Chapter	11	VFO CIRCUIT
Chapter	12	DC POWER SUPPLY UNIT
Chapter	13	MAINTENANCE
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CHAPTER 1 GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The M2351 Disk Drive is a compact state-of-the-art moving head disk drive with a storage capacity of up to 474 megabytes (unformatted) in a very compact package. It uses Winchester type heads and platters, allowing higher recording density, data transfer rate, and greater reliability, while offering a faster access time. The media is non-removable. This drive is appropriate for large capacity, high speed data storage in an online and/or batch system.

Model M2351A is of the Non-Fixed-Head type, and model M2351AF is of the Fixed-Head type with an unformatted fixed-head capacity of 1.69 megabytes to further improve the system throughput.

Higher cost performance and improved reliability can be achieved in computer systems that utilize M2351 disk drives.

The drive is designed to meet the following standards:

1. UL478 Electronic Data Processing Unit and Systems.
2. CSA C22.2 No. 154-1975 Data Processing Equipment. (Under investigation)

Note: "Old version" denotes M2351A (∿ #1898) and "New version" denotes M2351A (#1899 ∿). Regarding to M2351AF, all drives are "New version".

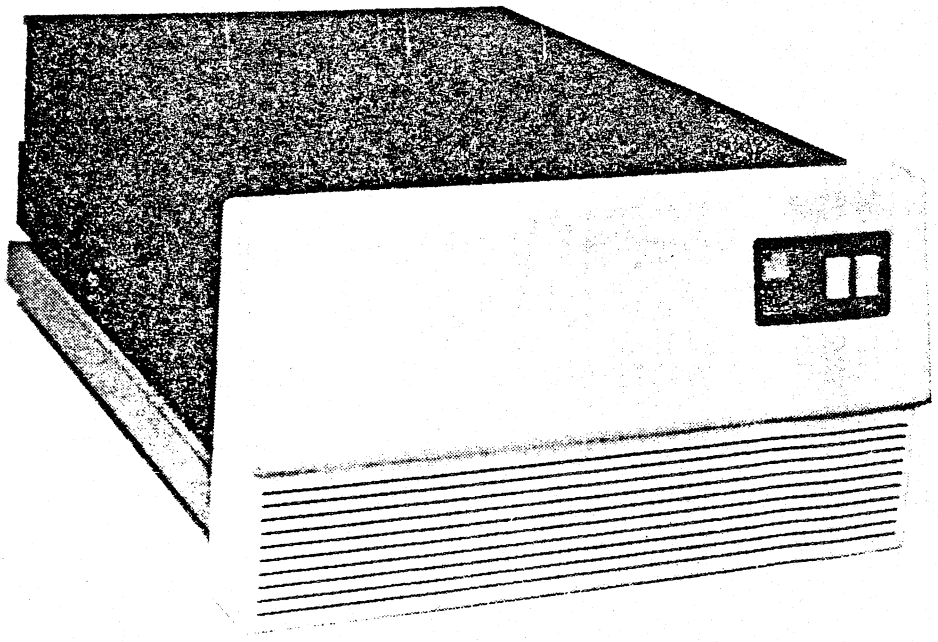


Fig. 1.1-1 External View of M2351A/AF

1.2 FEATURES

(1) Large Capacity and High Performance

- 474 megabytes of unformatted data can be stored on six disks.
- The M2351 disk drive provides exceedingly high performance characteristics such as 1.859 megabytes per second data transfer, 18 milliseconds average access time, and 7.58 milliseconds average latency time.

(2) Compact Size

The disk drive unit configured with Disk Enclosure (DE), DC power supply and LSI circuits, is available for mounting in a standard 19-inch rack.

(3) High Reliability

The disk enclosure includes a rotary actuator, a direct-drive spindle motor, the magnetic heads, disks and carriage. A completely sealed self-contained airflow system is used within the DE to assure a clean environment for low-flying heads, thus ensuring very high reliability.

(4) High Serviceability

- The DE can easily be removed for replacement in the field by CE.
- Serviceability is further improved by diagnostic information provided on the maintenance-aid display and/or sense information provided by the interface signals.

(5) Maintenance-free

The M2351 disk drive requires substantially reduced maintenance because of the completely sealed DE, a direct-drive DC Spindle motor and highly reliable printed circuit boards.

(6) Other Features

- High recording density with state-of-the-art technology
  A recording density of more than 10^7 bits per square inch is achieved with the advanced head and disk.

- Low power consumption

  Less than 0.62 KVA is required despite the large storage capacity.

- Fixed-head model

  The M2351AF has a fixed-head area of 1.69 megabytes (unformatted) capacity. The data in this area can be accessed without positioning time delay but with only latency time delay, thus providing high system throughput.

- Dual channel feature

  This option permits two controllers to access the same disk drive so that a file can be shared by two different systems.

- Modified SMD Interface

  The interface signals between the controller and the disk drive are partially modified from the standard SMD interface to agree with higher track capacity and higher maintainability.

The following are the major modified items.

(1) Data transfer rate
(2) Track capacity
(3) Timing of Read/Write operation
(4) Addition of Tag 4 and Tag 5

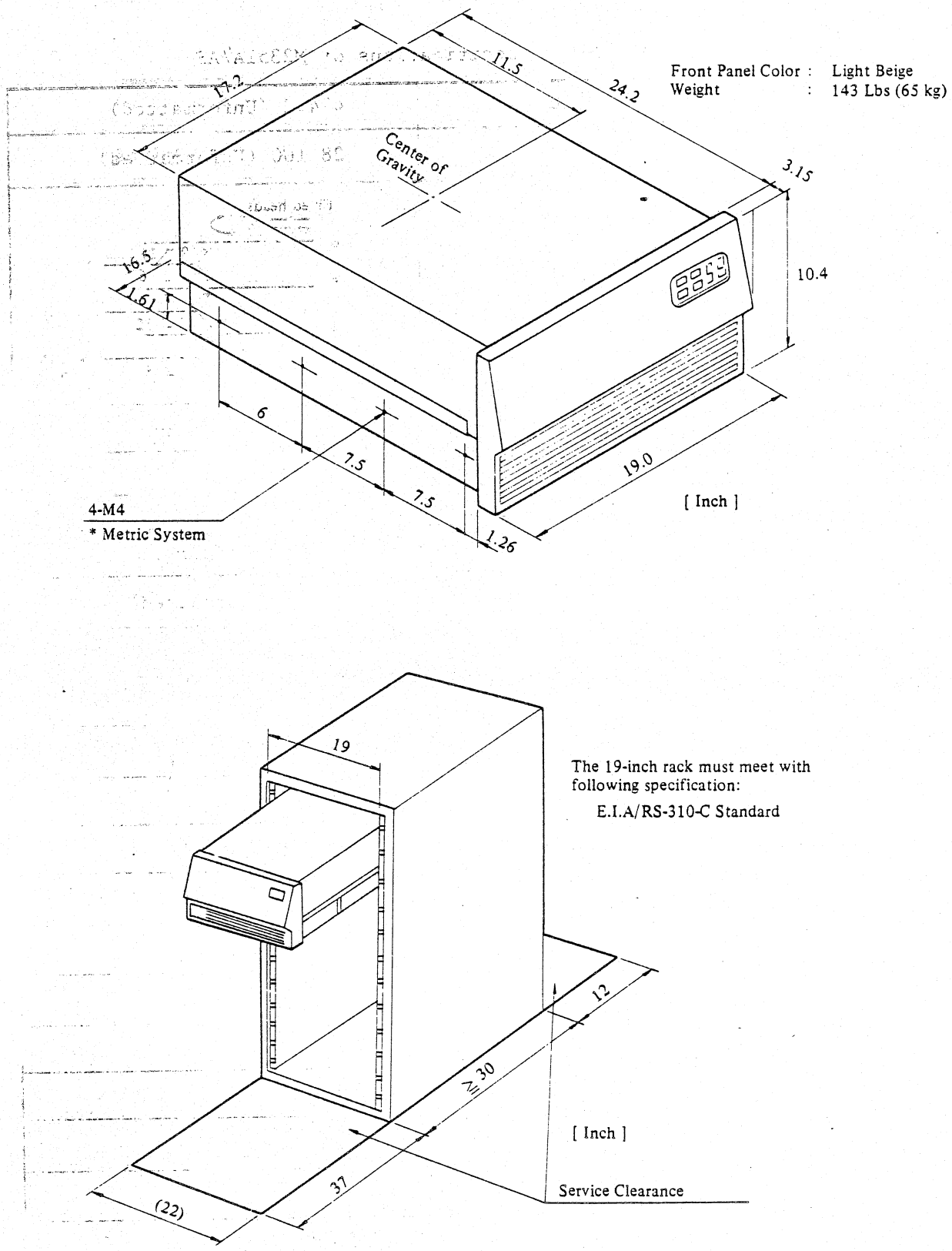
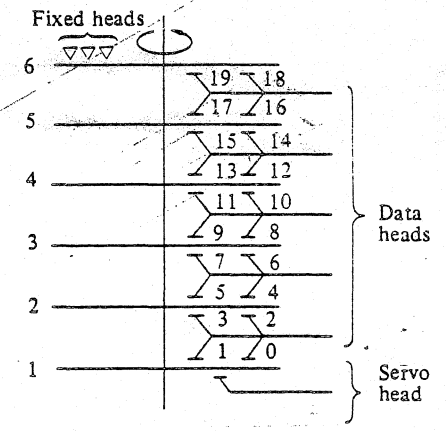


Fig. 1.1-2 Physical Dimensions

1.3 PERFORMANCE SPECIFICATIONS

Table 1.3-1 Specifications of M2351A/AF

Capacity	/Drive (MB)	474.2 (Unformatted)
	/Track (KB)	28.160 (Unformatted)
Configuration of Disks and Heads		
Fixed Head (M2351AF Only)	Tracks	60 (3 Cylinders)
	Capacity (MB)	1.69 (Unformatted)
Rotational Speed (RPM)		3,961
Latency (ms)		7.5
Disk	Diameter (Inch)	10.5
	Number	6
Heads	/Drive	20 + 1 (Servo)
	/Surface	2
Cylinders		842
Data Transfer Rate (MB/sec)		1.859
Positioning Time (ms)	Maximum	35
	Average	18
	Minimum	5
Track Density (TPI)		880
Bit Density (BPI)		12,800
Data Coding	on interface	NRZ
	on disk surface	MFM

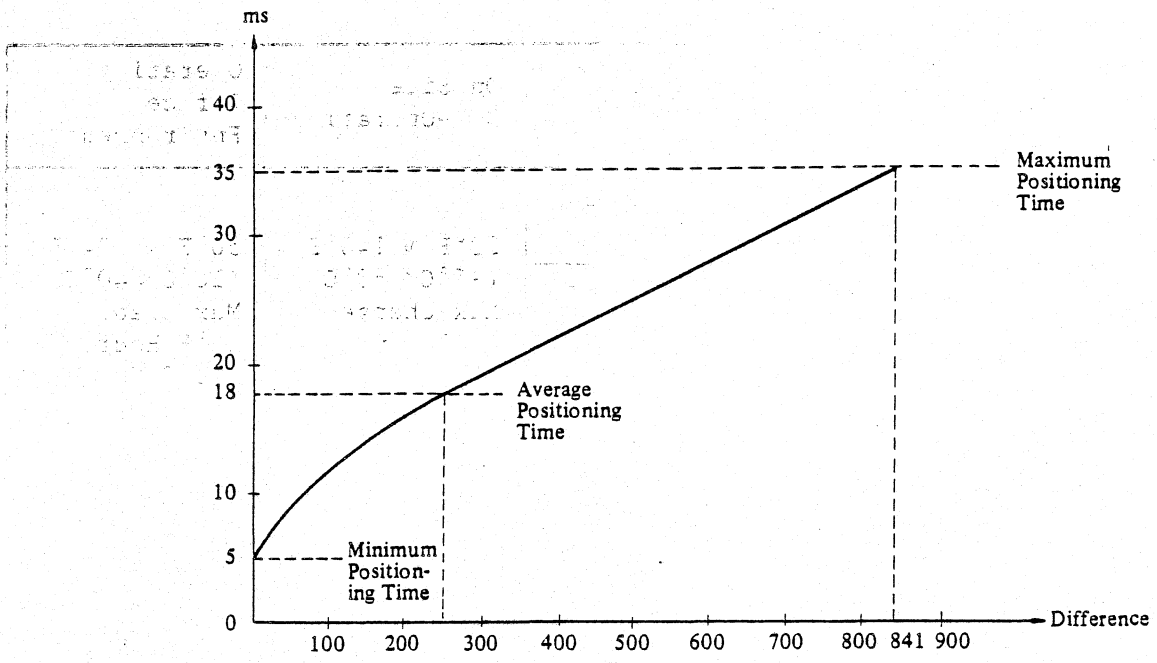


Fig. 1.3-1 Positioning Time vs. Difference

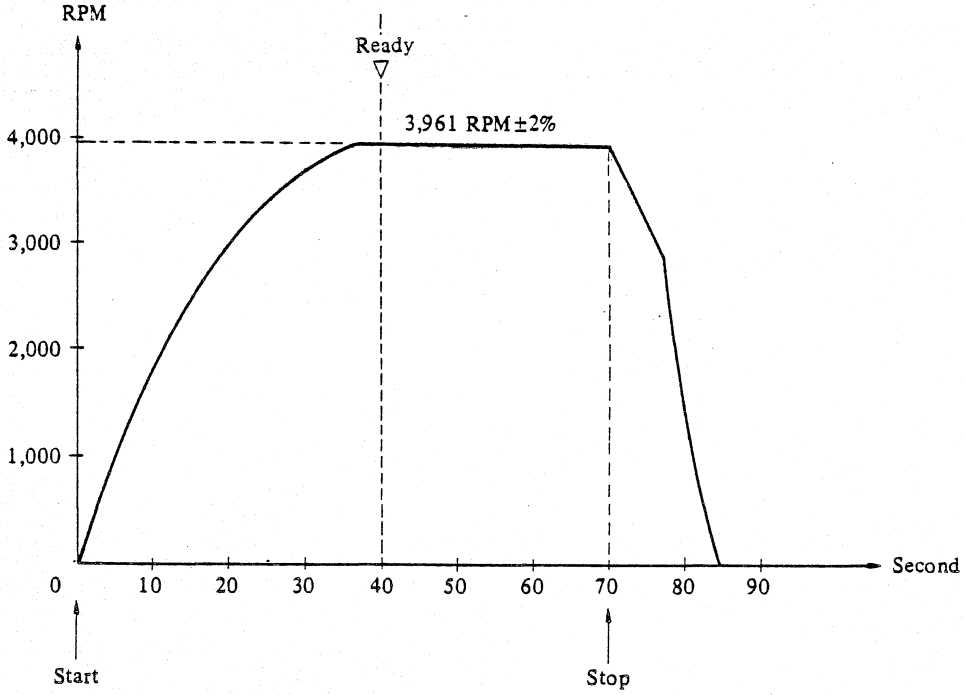


Fig. 1.3-2 Spindle Start/Stop Time

1.4 ENVIRONMENTAL SPECIFICATIONS

Table 1.4-1 Environmental Requirements

<table>
<tr><td>Environment</td><td colspan="2">Storage or transmit in packaged form</td><td>On Site Non-Operating</td><td>Operating Office Environment</td></tr>
<tr><td rowspan="2">Temperature*</td><td>Within 24 Hours</td><td>More than 24 Hours</td><td rowspan="2">23°F ∿ 140°F
(-5°C ∿ 60°C)
Max change
18°F/Hour
(10°C/Hour)</td><td rowspan="2">50°F ∿ 104°F
(10°C ∿ 40°C)
Max change
18°F/Hour
(10°C/Hour)</td></tr>
<tr><td>-40°F ∿ 140°F
(-40°C ∿ 60°C)
Max change
36°F/Hour
(20°C/Hour)</td><td>23°F ∿ 140°F
(-5°C ∿ 60°C)
Max change
18°F/Hour
(10°C/Hour)</td></tr>
<tr><td>Humidity</td><td colspan="2">5% ∿ 95% RH
Non-condensing</td><td colspan="2">20% ∿ 80% RH
Max change 10%/Hour
Non-condensing</td></tr>
<tr><td>Vibration</td><td colspan="2">3G (When locked for shipment)</td><td>0.2G
(10Hz ∿ 500Hz)</td><td>0.2G
(5Hz ∿ 50Hz)
1G
(50Hz ∿ 500Hz)</td></tr>
<tr><td>Shock</td><td colspan="2">5G (Max. 30 ms)</td><td>3G (Max. 10ms)</td><td>2G (Max. 10ms)</td></tr>
<tr><td>Altitude</td><td colspan="2">40,000 FT (12,000 m)</td><td colspan="2">10,000 FT (3,000 m)</td></tr>
<tr><td>Dust</td><td colspan="4">0.168 mg/m^3 (Stearic Acid Standard)</td></tr>
<tr><td>Air flow</td><td colspan="3">——</td><td>2.5 m^3/min.</td></tr>
<tr><td>Acoustic</td><td colspan="3">——</td><td>60 dBA</td></tr>
</table>

* $°C = \frac{5}{9}(°F-32)$

1.5 POWER SPECIFICATIONS

Table 1.5-1 Power Requirements (Typical Values)

Voltage (Vac±10%)	Frequency (Hz±2Hz)	Current (Aac)		Power Consumption (KVA)	Heat Dissipation (K•Cal/ Hour)	Heat Dissipation BTU/ Hour
		Starting*	Running			
100	50/60	40	5.7/5.4	0.57/0.54	460/420	1,800/1,600
120	60		4.6	0.55	430	1,700
220	50		2.8	0.62	510	2,000
240	50		2.6	0.62	510	2,000

* Starting current is specified as the maximum transient current lasting one-half cycle of the input AC power.

1.6 CABLE AND CONNECTOR SPECIFICATIONS

Table 1.6-1 Cables and Connectors

	Cable		Connector (Supplier)	
	Specification	Supplier	Drive Side	Cable Side
A-Cable (60-Pin)	Zo = 100±10Ω 28 AWG 7 Stands 100 FT. Max.	SPECTRA STRIP 455-248-60	FUJITSU FCN-704P060-AU/L	FUJITSU FCN-707J060-AU/B
			3M 3472-2303	3M 3334-6010
B-Cable (26-Pin)	Zo = 100±10Ω 28 AWG 7 Stands 50 FT. Max.	ANSLEY 174-26	FUJITSU FCN-705P026-AU/L	FUJITSU FCN-707J026-AU/B
			3M 3429-1303	3M 3399-6010
Power Cable A	See Figure 1.6-1			
Power Cable B	See Figure 1.6-2			
Power Cable C∿D	See Figure 1.6-3			

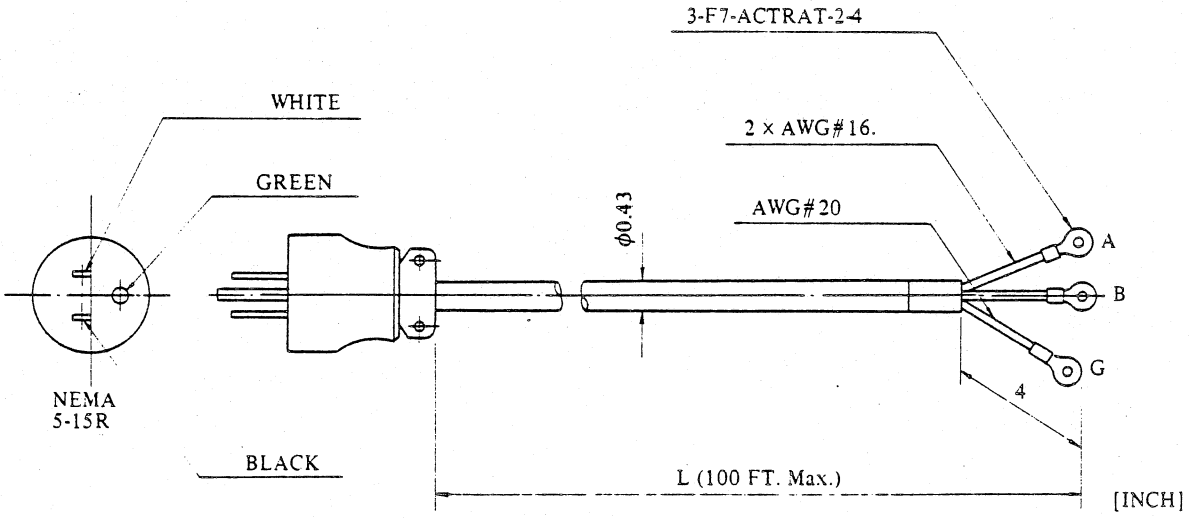


Fig. 1.6-1 Power Cable A

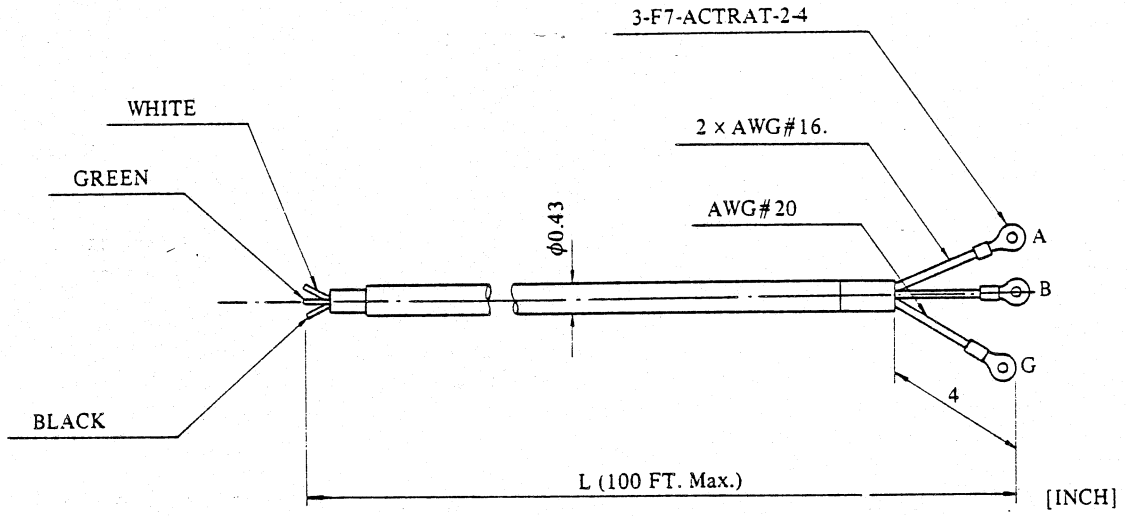


Fig. 1.6-2 Power Cable B

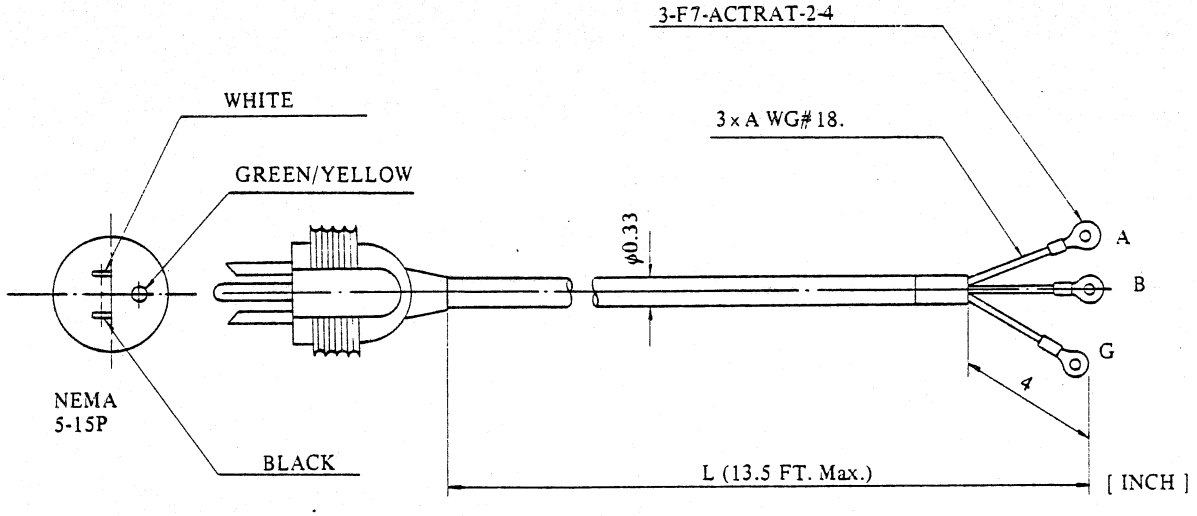


Fig. 1.6-3 Power Cable C ∿ D

1.7 OPTIONS

Table 1.7-1 Option List

No.	Name	Specification	Remark	
1	A-Cable	B660-1065-T006A	Non-shield	Cable length can be specified from 0.5 m to 30 m in 0.5 m increments
2		B660-1954-T904A	Shield	
3	B-Cable	B660-1065-T008A	Non-shield	Cable length can be specified from 0.5 m to 15 m in 0.5 m increments
4		B660-1954-T903A	Shield	
5	Power Cable A (UL only)	B660-1055-T027A	Cable length can be specified from 1 m to 30 m in 0.5 m increments. (100/120 Vac only)	
6	Power Cable B (UL, CSA)	B660-0620-T387A	Cable length can be specified from 1 m to 30 m in 0.5 m increments. (220/240 Vac only)	
7	Power Cable C (UL, CSA)	B660-1055-T033A	L = 2.5 m, (100/120 Vac only)	
8	Power Cable D (UL, CSA)	B660-1055-T034A	L = 3.5 m, (100/120 Vac only)	
9	Power Cable E (UL, CSA)	B660-1055-T035A	L = 4.5 m, (100/120 Vac only)	
10	Line Terminator (TCAMU)	B16B-4870-0010A#U	Note that two line terminators are required in dual channel system.	
11	Dual Channel Option	B03B-4655-0100A		
12	Slide Guide Option	B030-4655-V100A		
13	Front Panel Option	B210-1435-X012A		
14	Operator Panel Assembly	N860-3346-T001		
15	Hour Meter	B61L-0140-0011A #10000	10,000 hours	

Note that the Fixed-Head is not an option but a model change from the Non Fixed-Head drive.

Non Fixed-Head Drive; M2351A (B03B-4655-B002A)

Fixed Head Drive ; M2351AF (B03B-4655-B003A)

When M2351A or M2351AF is ordered alone, it does not include the front panel, operator panel, etc. listed in Table 1.7-1.

A-, B- and Power Cable A, B length must be specified by adding comment behind the cable specification.

Example: B660-1065-T006A #10.5 m (A-Cable, 10.5 meters)

1.8 SPARE PARTS

Table 1.8-1 Recommended Spare Parts List

No.	Name	Specification	Quantity		MTBF (K-hours)	RM	ETR (mo.)	Remarks	
			A	AF					
1	DE Assembly	B030-4610-T005A	1	–	30	R	4	Non-fixed heads type	M2351A (#1~#1898)
	DE Assembly	B030-4610-T007A	1	–	30	R	4		M2351A (#1899~)
2	DE Assembly	B030-4610-T006A	–	1	30	R	4	Fixed heads type	–
	DE Assembly	B030-4610-T008A	–	1	30	R	4		M2351AF (#1~)
3	DC Power Supply	B14L-5105-0073A	1	1	100	R	4		
4	Line Blower	B90L-1200-0101A	1	1	200	–	–		
5	Operator Panel Assembly	N860-3346-T001	1	1	200	R	3		
6	PCB TVHMU	B16B-8130-0010A#U	1	1	180	R	3	Power Amplifier	M2351A (#1~#1898) M2351AF (–)
	PCB TVKMU	B16B-8800-0010A#U	1	1	180	R	3		M2351A (#1899~) M2351AF (#1~)
7	PCB RFJAU	C16B-5500-0990#U	1	1	110	R	3	Read Amplifier	
8	PCB SVIAU	C16B-5501-0010#U	1	1	90	R	3	Servo Circuit	
9	PCB 512398	C16B-5123-0980#U	1	1	210	R	3	Logic Circuit	
10	PCB DQEMU	B16B-8140-0010A#U	1	1	250	R	3	Interface Circuit	
11	PCB HGAMU	B16B-7830-0010A#U	1	1	830	R	3	Indicator Unit	
12	PCB BQGMU	B16B-8160-0010A#U	1	1	720	R	3	Back Panel	
13	PCB DQFMU	B16B-8150-0010A#U	(1)	(1)	200	R	3	Interface Circuit (Dual Channel Option)	
14	Air Filter	B90L-0400-0303A	1	1	–	–	–		
15	Fuse	C60L-0020-0001 #MP05	1	1	–	–	–	Used in DC Power Supply (0.5 A)	

Notes: MTBF; Mean Time Between Failures (K•hours)

RM ; Repairable Mark (R; Repairable)

ETR ; Estimated Time To Repair (month) in Japan

1.9 MAINTENANCE TOOLS AND EQUIPMENT

Table 1.9-1 Maintenance Tools and Equipment

No.	Tools and Equipment	Specification	Remark
1	Extension Cable	B660-1060-T072A#L510R0	20 pins
2	Extension Cable	B660-1060-T074A#L510R0	50 pins
3	Extension Unit	C960-0030-T029	
4	Extractor	C960-0300-T001	One required
5	Oscilloscope	TEKTRONIX 475, or equivalent	
6	Oscilloscope Probe (X10)	TEKTRONIX P6053B or equivalent	
7	Digital Multimeter		
8	Screwdriver		
9	Hexagonal Wrenches		Metric system
10			
11			
12			
13			

1.10 RELIABILITY AND SERVICE GOALS

(1) MTBF

MTBF is defined as follows.

MTBF = operating time/the number of troubles the unit suffered

Operating time is the total time duration during which the power is ON except during maintenance work. Trouble of the unit means trouble that requires either repairs, adjustments, or replacement. Mishandling by the operator, power failure, control unit trouble, cable trouble and trouble due to bad environmental conditions are not included.

The MTBF of M2351A/M2351AF is more than 10;000 hours estimated value after an initial period of 200 hours.

(2) MTTR

MTTR is the average time a well-trained service mechanic should take to diagnose and repair the trouble. The M2351A/M2351AF are designed for an MTTR of 30 minutes or less.

(3) Preventive Maintenance Time

The air filter should be cleaned or replaced at one year intervals, or as required.

(4) Component Life

M2351A/M2351AF need not be overhauled for the first five years.

(5) Power Loss

If an abnormal condition occurs when the AC power is turned off, nothing happens to the data stored in the disk. However, if the power failure occurs during a WRITE operation, that data is not guaranteed.

(6) Read Error

Prior to determination of the read error rate, the data must be verified as correctly written and all identified media defects must be deallocated or skipped.

- Recoverable Error Rate ..... 10×10^{-11}
  While reading 10^{11} bits of data, less than 10 read errors would be encountered which are recoverable in 4 retries without using the ECC functions and the offset operation.
- Unrecoverable Error Rate ... 10×10^{-14}
  While reading 10^{14} bits of data, less than 10 read errors would be encountered which are unrecoverable in 5 retries without using the ECC function.

  Retry routine; after 4 times of re-reading with and without offset, RTZ must be performed.

(7) Seek Error Rate ..... 1×10^{-7}

(8) Quality Standards of Media at Shipment (Summary)

- The number of defects per DE shall not exceed 500.
- The number of defective tracks per DE shall not exceed 30.
  (A track containing two or more defects is defined as a defective track.)
- Head 0 and 1 at cylinder 0 should be perfect tracks.

Refer to Chapter 5.3 for detail.

CHAPTER 2 INSTALLATION

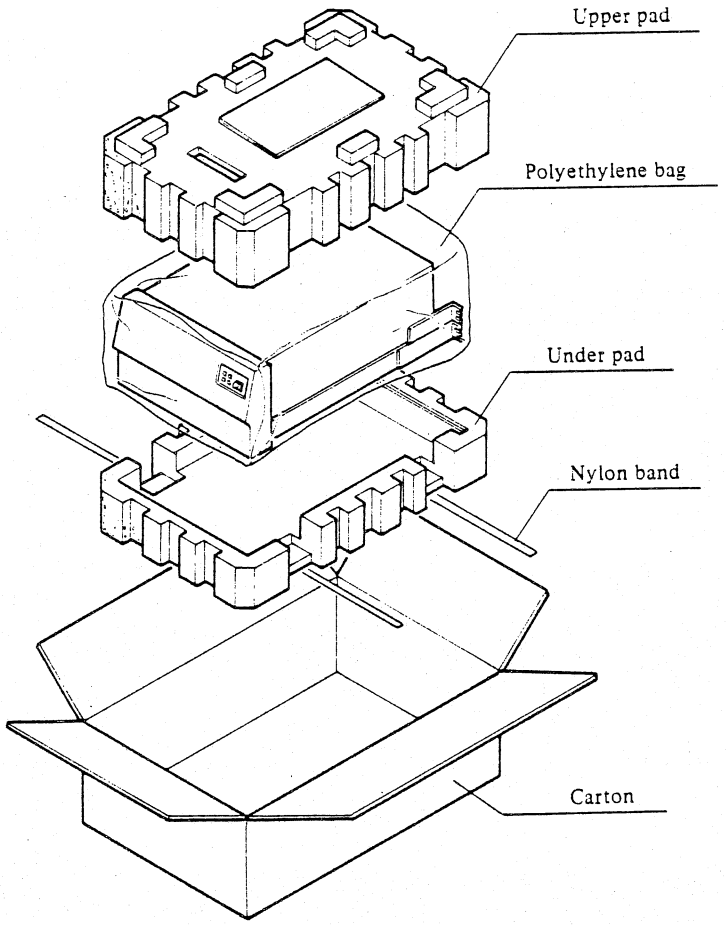
2.1 STORAGE

When the drive is stored for a prolonged period, avoid locations where the environment is extreme. Stored units should be properly packed and can be stored stacked vertically, two high. When the temperature difference between storage (or shipping) and the unpacking environment exceeds 20°C (36°F), the unit should be allowed to remain in packaged form for more than 3 hours to avoid condensation when unpacking.

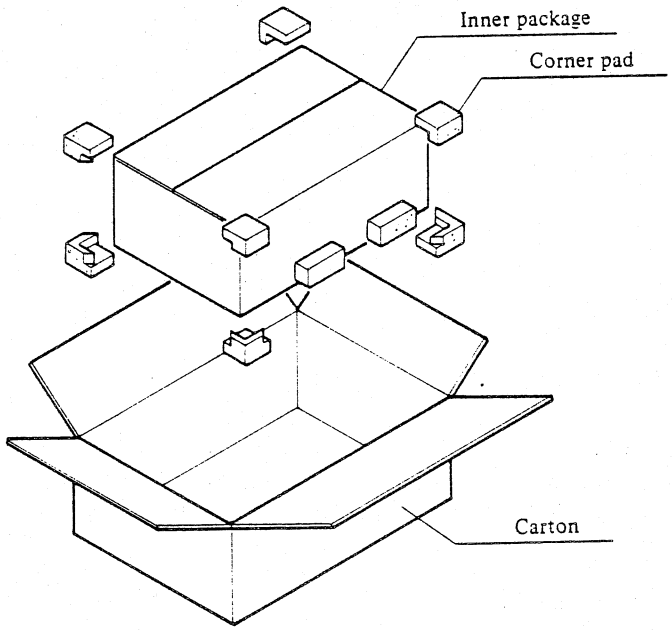
2.2 UNPACKING

(1) The M2351 is shipped in a carton surrounded by shock absorber as shown in Figure 2.2-1. (Note: the shipping carton is intended to be reuseable.) To unpack the unit, first the carton flaps to the left and right and then take out the unit. Do not grasp the front panel or cover of the unit to lift - use the sub-frame at the bottom to avoid the possibility of sub-assembly damage. Take care to move the unit carefully to avoid abrupt impact or shock.

(2) After unpacking the drive, check for scratches or dents. Remove the cover, (Figure 2.2-2) and visually inspect inside the drive as follows:

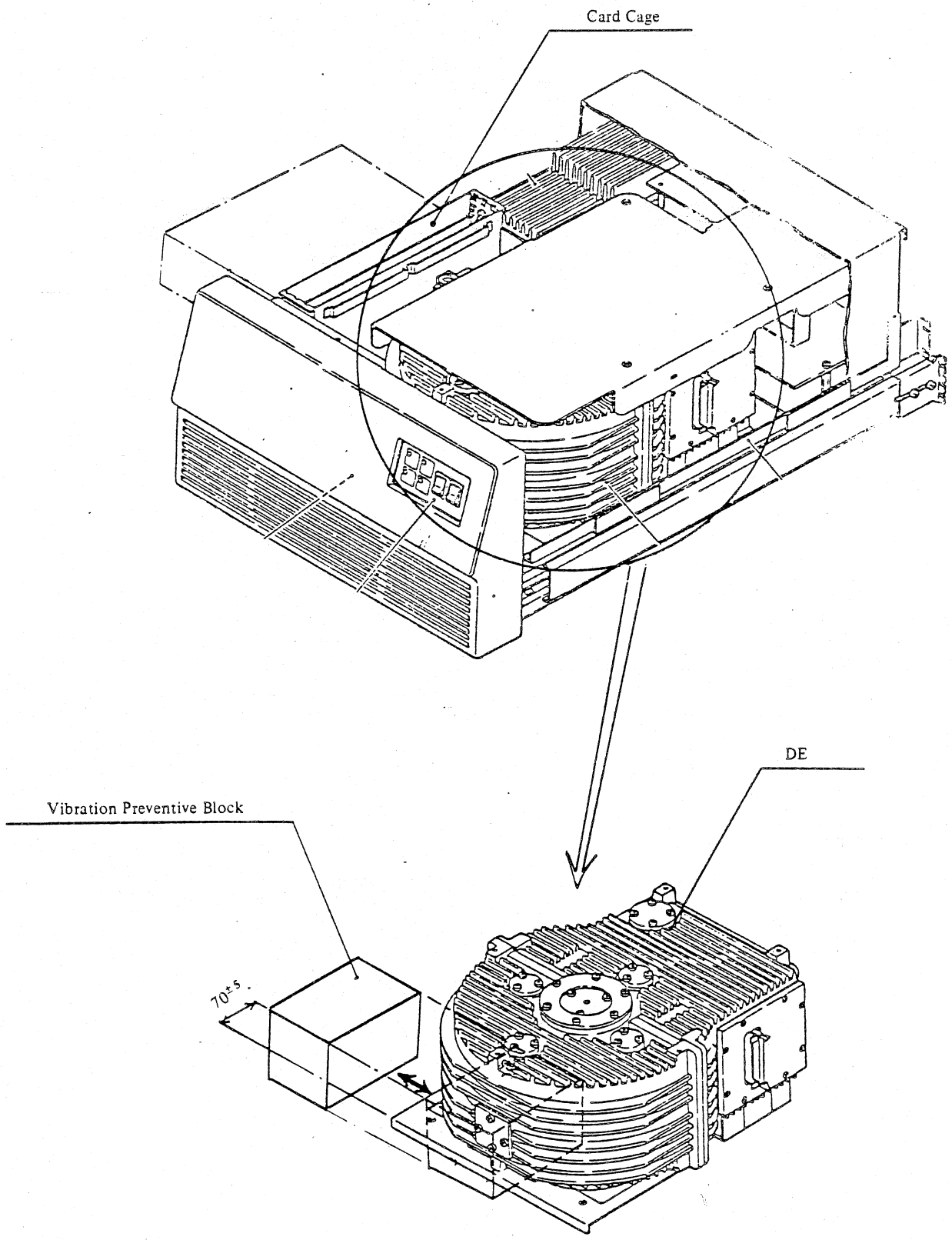


(a) Inner packaging



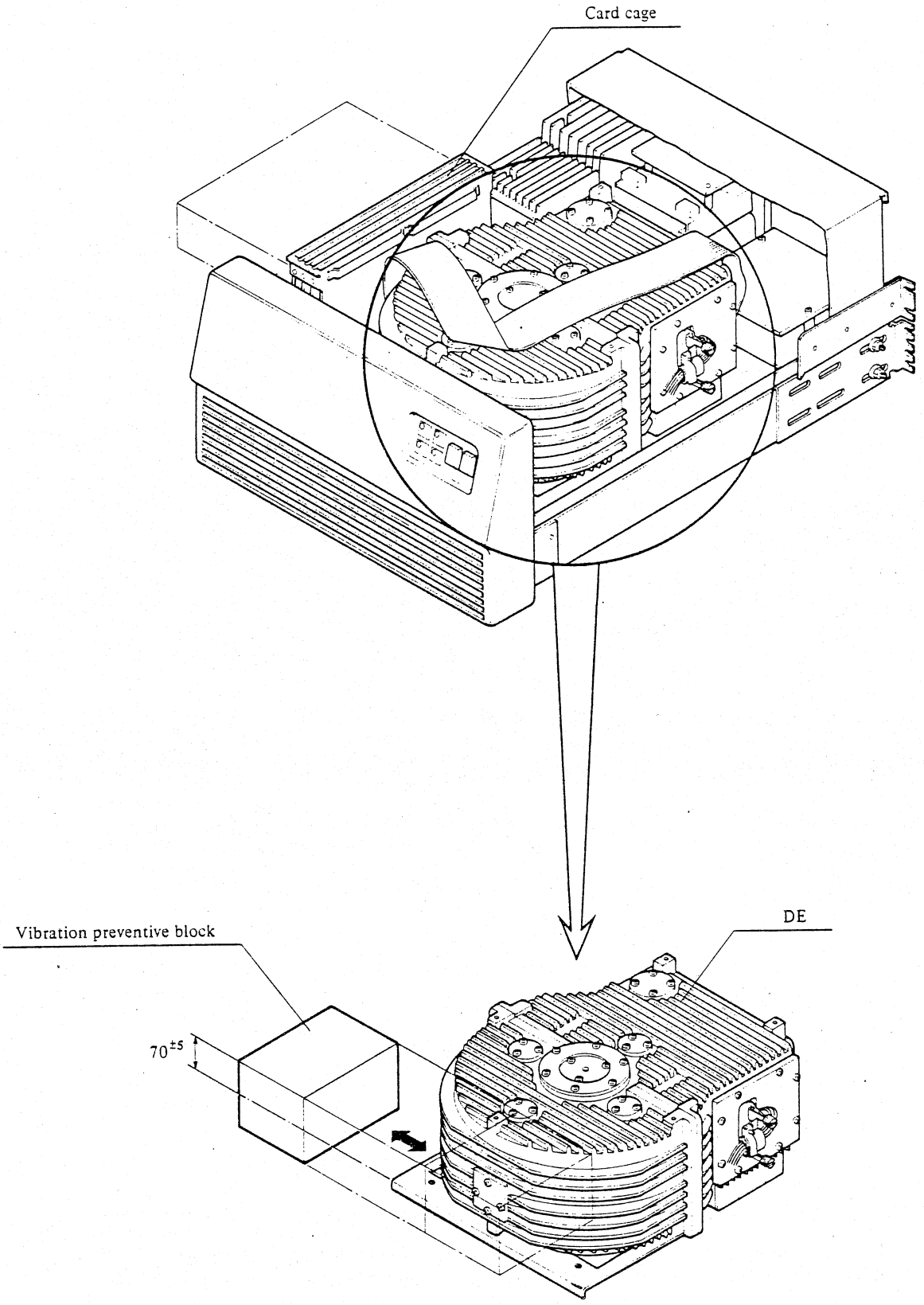
(b) Outer packaging

Figure 2.2-1 Exterior View and Construction of Carton



(a) Old version

Figure 2.2-2 Cover Removal



(b) New version

Figure 2.2-2 - Continued

2.3 ROTARY ACTUATOR UNLOCKING/LOCKING

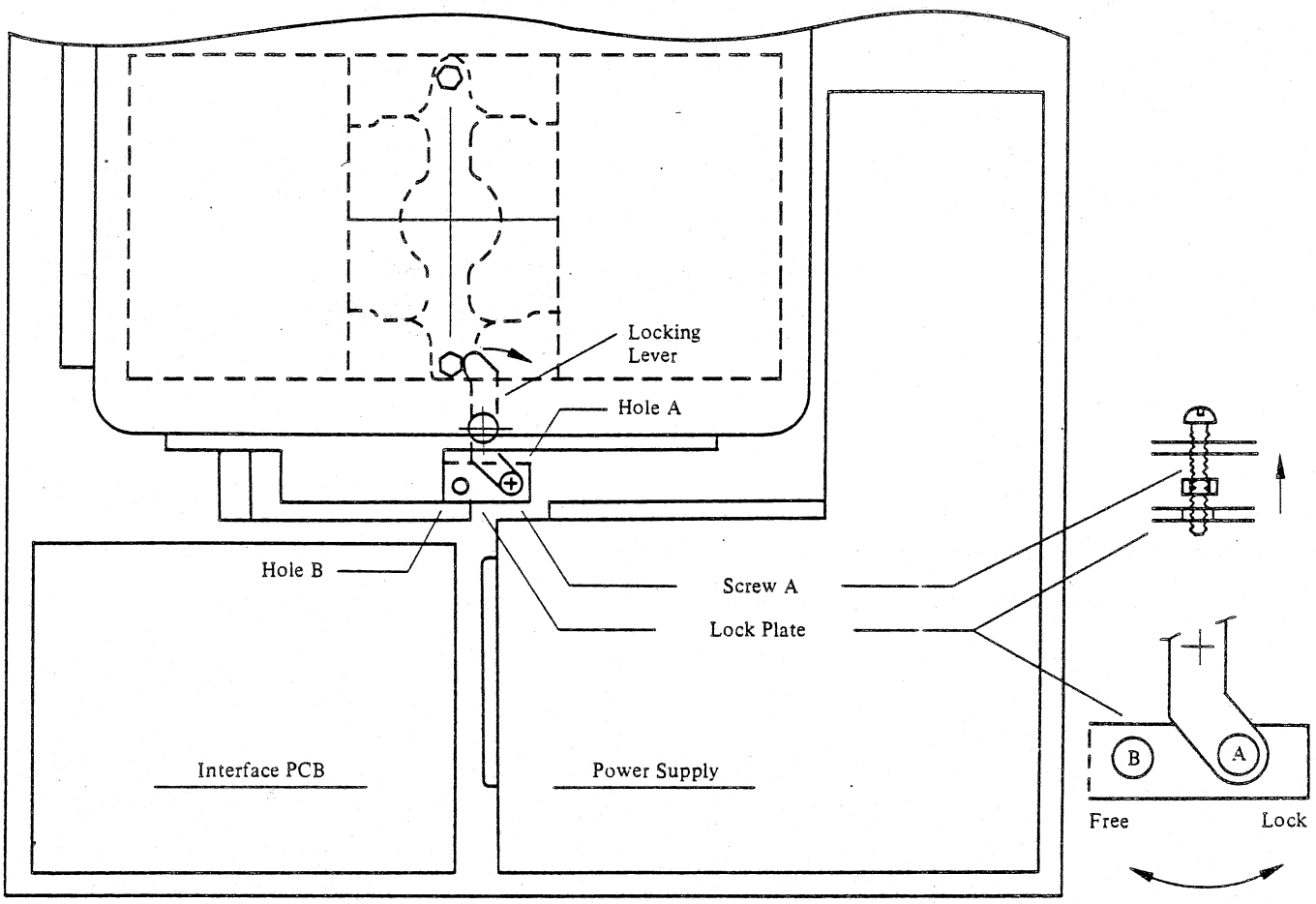


Figure 2.3-1 Rotary Actuator Unlocking/Locking
(Top View)

(1) Unlocking

This mechanism can be readily viewed from the rear of the drive by looking over the Interface PCB.

Loosen Screw A (by means of a phillips screwdriver, 8 inches or longer), sufficiently to free the screw tip from the hole in the Lock Plate. With the screwdriver, rotate the Locking Lever to the Unlocked position (Hole B), and secure in that position by gently tightening Screw A. (Refer to Figure 2.3-1)

(2) Locking

This mechanism can be readily viewed from the rear of the drive by looking over the Interface PCB.

Loosen Screw A (by means of a phillips screwdriver, 8 inches or longer), sufficiently to free the screw tip from the hole in the Lock Plate. With the screwdriver, rotate the Locking Lever to the Locked position (Hole A), and secure in that position by gently tightening Screw A. (Refer to Figure 2.3-1)

(a) Check for loose or missing parts, or foreign matter.

(b) Check that the PCB's are properly seated in the correct positions.

(c) Check that all connectors are secure and no cable chafing damage has occurred.

After inspection, (prior to operating the drive), unlock the rotary acutuator and secure in the unlocked position. (Refer to Figure 2.3-1) And then, lift the card cage vertically rotate over the side. Remove the vibration preventive block under the DE housing.

(3) Packing

Prior to packing the drive, insure that the rotary actuactor locking mechanism is secured in the locking position, (Refer to Figure 2.3-1) and the vibration preventive block properly inserted under the DE housing (Refer to Figure 2.2-2). When reshipping the drive, place it in a polyethelene bag and repack it in the Original carton with shock absorbers. (Refer to Figure 2.2-1)

2.4 SLIDE/MOUNTING INSTRUCTIONS

The drive can be slide-mounted in a standard 19-inch rack or built into a system cabinet. Installation procedures follow, and are illustrated in Figure 2.4-1.

(1) Slide Rail Installation and Mounting

a. Extend the slide guide and release from slide rail.

b. Install the slide guide (as shown) in the 19-inch rack or cabinet.

c. With both the slide guides installed and extended, lift the drive (with slide rails already attached) onto the extended guides. Be sure the rail is correctly seated and latched in the guide.

NOTE: The drive weight approximately 143 lbs (65 kg), and requires at least two people to install.

(2) Drive Removal

a. Fully extend the drive from the rack. Release the latching mechanism and, with a lifting-forward motion, lift the drive off the slide guides.

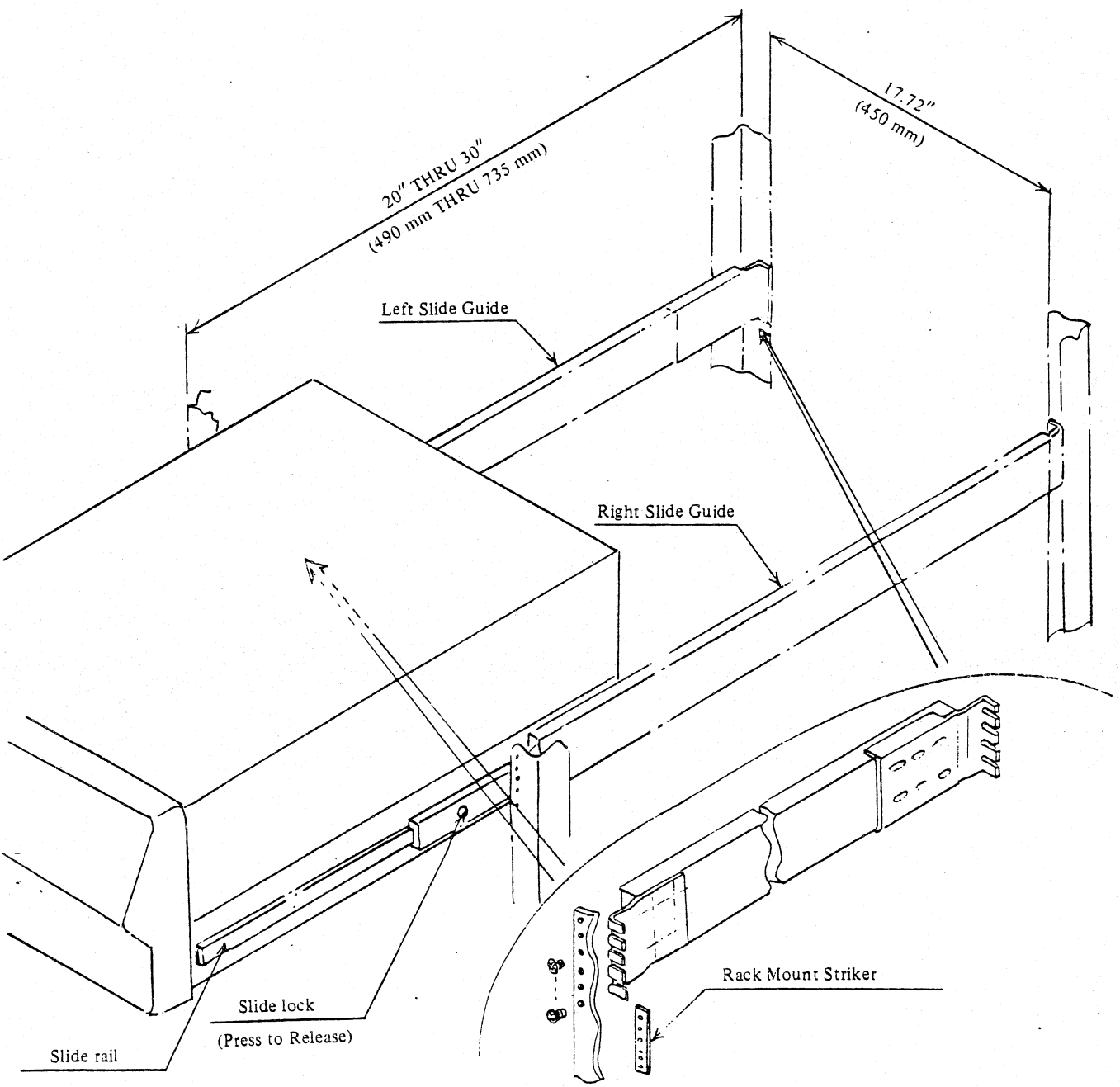


Figure 2.4-1 Rack Mount Installation

CHAPTER 3 OPERATION AND CHECKOUT

3.1 DC POWER SUPPLY UNIT

Control panel of the DC power supply unit is shown in Figure 3.1-1.

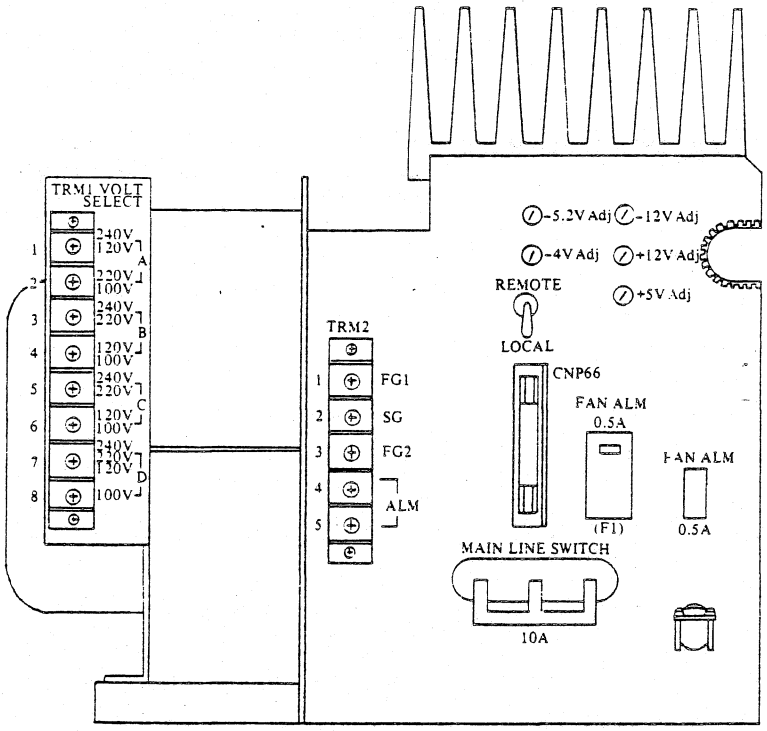


Figure 3.1-1 Control Panel of DC Power Supply Unit

(1) Main Line Switch (Non-Fuse Breaker)

Supplies AC power to the unit. If one of following failures occures, it goes off.

- Over current in the AC input
- Over current or voltage in the DC output
- Fan (Line-Blower) Alarm
- Over Temperature of the heat sink or of the transformer in the DC power supply unit.

(2) Fan ALM (Fuse)

Indicates fan alarm of the line-blower.

(3) Remote/Local (Switch)

When this is set to Remote, the spindle motor starts/stops rotating in accordance

with the commands (Power Sequence Pick/Hold) issued from the controller. When set to Local, rotation is under the control of the Start switch on the operator panel.

(4) TRM 1 (Terminal)

The taps on this terminal must be changed in accordance with the voltage and frequency of AC input power, as shown in Table 3.1-1

Table 3.1-1 Tap Number to be shortened

Vac (Hz)	Tap Number	
	(A) - (B)	(C) - (D)
100 (50/60)	2 - 4	6 - 8
120 (60)	1 - 4	6 - 7
220 (50)	2 - 3	5 - 7
240 (50)	1 - 3	5 - 7

(5) TRM 2 (Terminal)

FG1 ..... Frame Ground
SG ..... Signal Ground
FG2 ..... Frame Ground with a 510 kΩ resistor
ALM ..... Alarm Output (not used)

The Frame Ground and Signal Ground are completely isolated in the drive, and they are provided as FG1/FG2 and SG on this terminal.

As shown in Figure 3.1-2, FG1 is a frame ground itself, but FG2 is a frame ground to which a 510 kΩ resistor is provided in DC Power Supply.

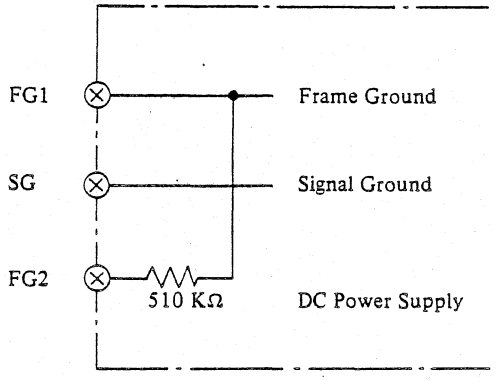


Figure 3.1-2 FG1/FG2 and SG

At the time of shipment, SG and FG2 are connected with a shorting plate.

Refer to Chapter 4.3 on the operation.

(6) Volt ADJ (Variable Resistors)

Although adjustment should not be required, variable resistors are provided to adjust the -5.2, -4, ±12, -5 Vdc output voltages within the tolerance specified, if necessary.

3.2 INTERFACE PCBs

(1) INTERFACE PCB ----- DQEMU (B16B-8140-0010A#U)

Drive logical address 0 to 7 can be set with three positions of the switch in binary code as shown in Table 3.2-1.

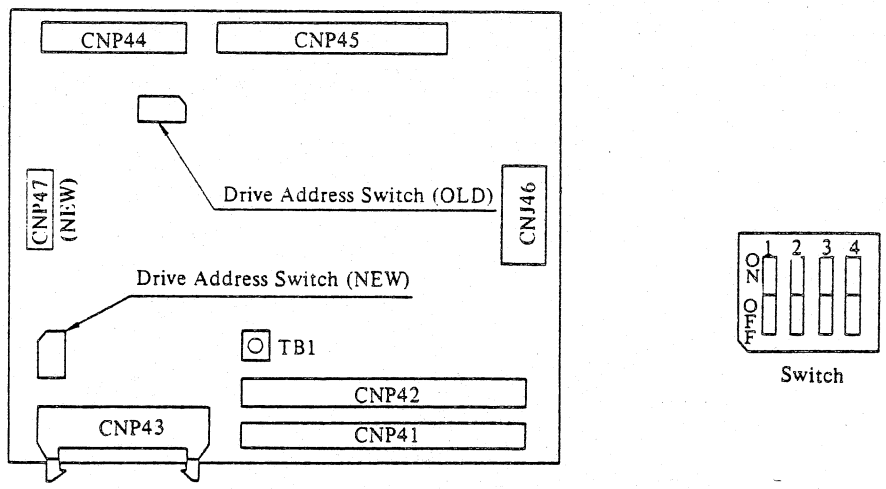


Figure 3.2-1 Drive Address Switch

Table 3.2-1 Drive Addressing

Drive Address	Switch Position			
	1	2	3	4
0	OFF	OFF	OFF	Not Used
1	ON	OFF	OFF	
2	OFF	ON	OFF	
3	ON	ON	OFF	
4	OFF	OFF	ON	
5	ON	OFF	ON	
6	OFF	ON	ON	
7	ON	ON	ON	

(2) DUAL CHANNEL INTERFACE PCB ----- DQFMU (B16B-8150-0010A#U)

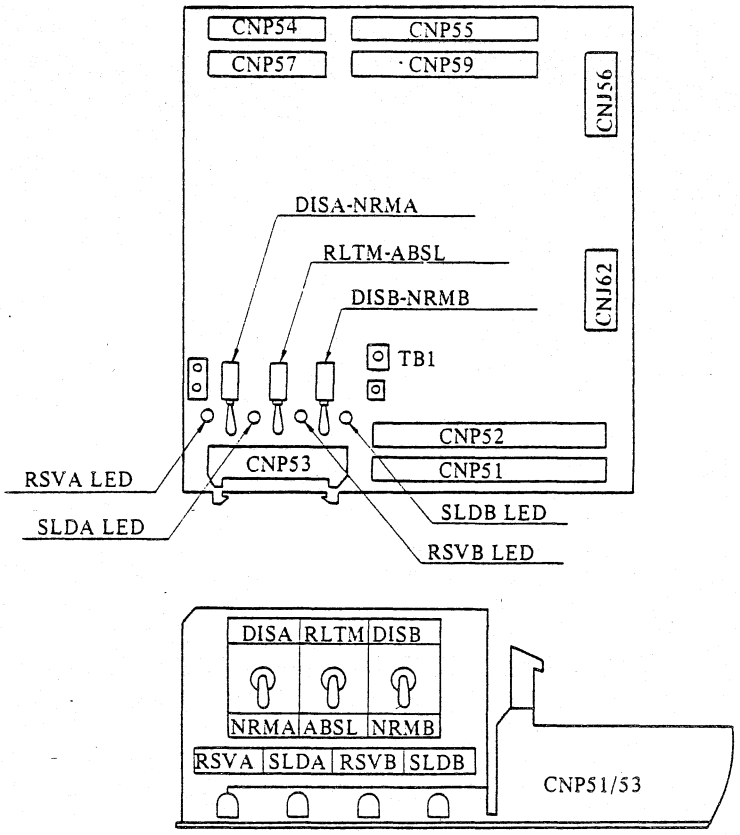


Figure 3.2-2 Switches and Indicators

LEDs

(1) RSVA (Channel A Reserved) ----- Orange

Indicates that the drive is reserved by A-channel.

(2) SLDA (Channel A Selected) ----- Green

Indicates that the drive is selected by A-channel.

(3) RSVB (Channel B Reserved) ----- Orange

Indicates that the drive is reserved by B-channel.

(4) SLDB (Channel B Selected) ----- Green

Indicates that the drive is selected by B-channel.

Switches

(1) DISA - NRMA (Disable A - Normal A)

Disconnects or connects the interface signals of A-channel.

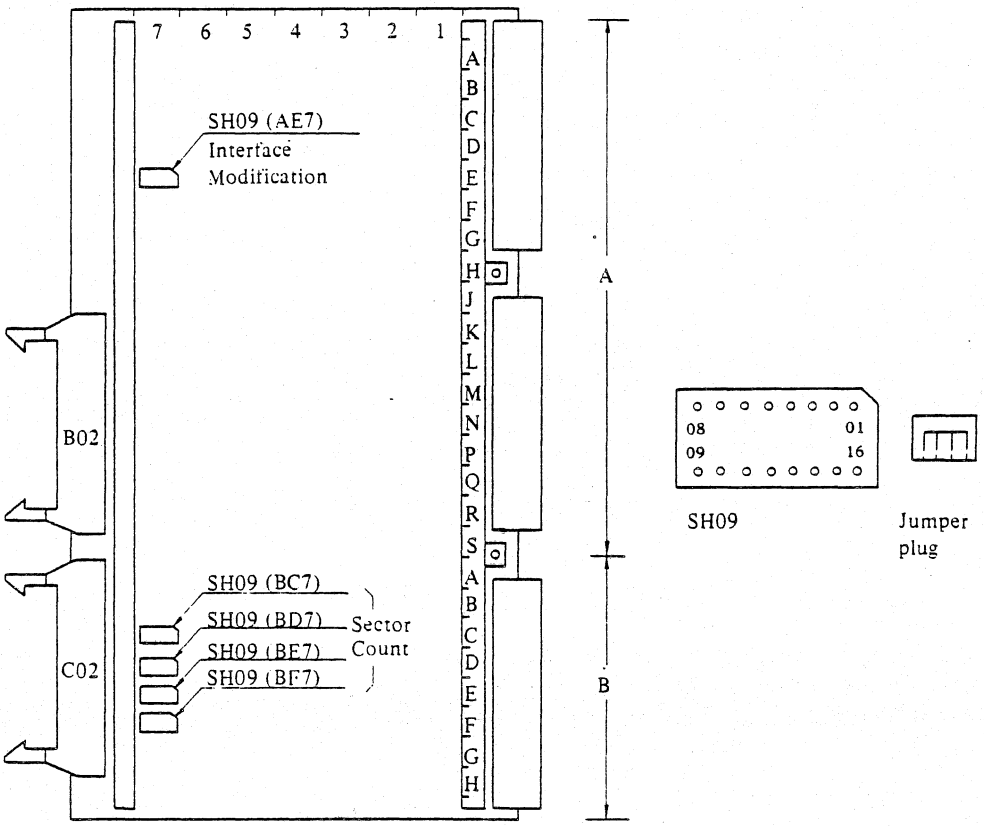
(2) RLTM - ABSL (Release Timer - Absolute)

When the switch is at RLTM side, reserved status will be released 500 ms after Unit Select Command if the Release Command has not already been issued. When the switch is at ABSL side, reserved status can be released only by the Release Command.

(3) DISB - NRMB (Disable B - Normal B)

Disconnects or connects the interface signals of B-channel.

Short circuits (SH09) and jumper plugs for setting sector count and changing interface requirements are provided.



( ) indicates location of short circuit on the PCB.

Figure 3.3-1 Sector Count and Interface Selection

Removal of the Logic PCB is required to set the sector count or change the interface options. This is accomplished with the extractor tools provided with the drive (refer to Table 1.9-1, item 4) as shown below.

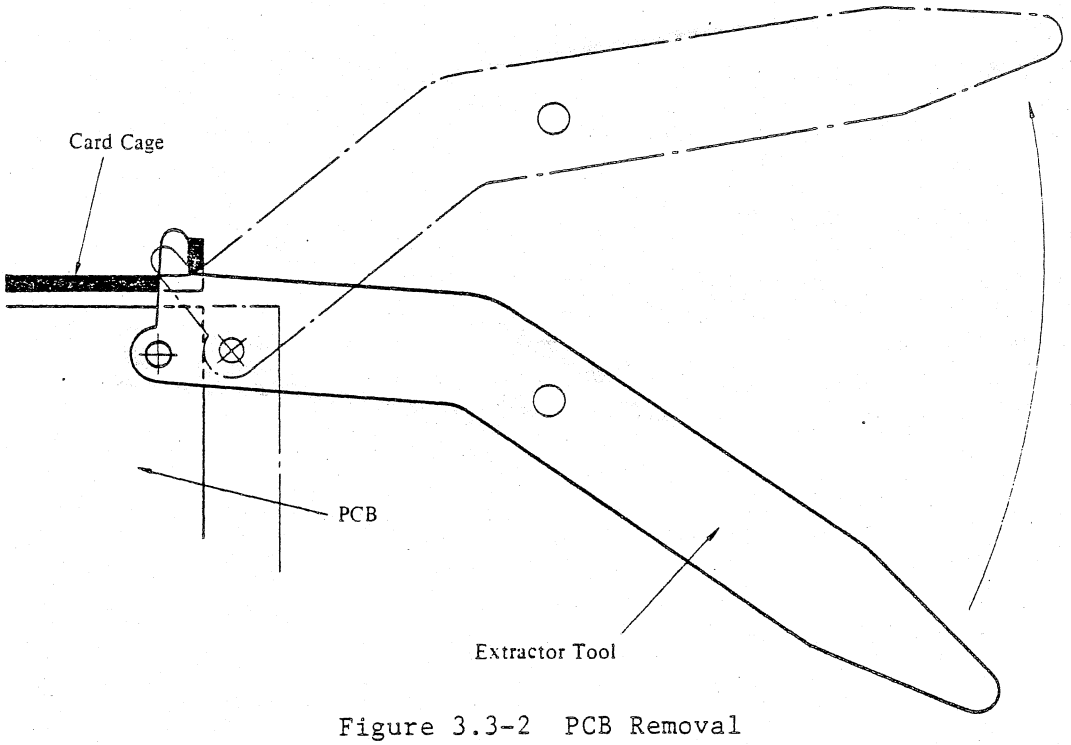


Figure 3.3-2 PCB Removal

(1) Interface Changing

The interface can be changed by shorting the appropriate pins with jumper plugs, as shown below.

Table 3.3-1 Interface Selection

Item	Pin number to be shortened	Default mode	Function
Incorporate TAG4, 5 Status Capability	03 - 02	o	Enable
	03 - 04		Disable
Operation of Seek End status	06 - 05		Seek End is not issued after Offset Command is reset.
	06 - 07	o	Seek End is issued after Offset Command is reset.
Response of Unit Ready	10 - 09	o	Unit Ready is issued even if the drive is in a fault condition.
	10 - 11		Unit Ready is not issued when the drive is in a fault condition.

3.4 SECTOR COUNT

The number of bytes per sector in Fixed Sector Format is determined by the location of jumper plugs according to the following table and example. .

Example; 9 Sectors/Track

$$\text{Bytes/Sector} = \frac{\text{Bytes/Track}}{\text{Sectors/Track}} = \frac{28,160}{9} = 3,128.89$$

If the above calculation results in a remainder, round it off to the next integer, i.e., Bytes/Sector = 3,129

Set this figure minus one with jumper plugs to allow the Byte Counter to start counting from zero.

$$3,129-1 = 3,128 = \underbrace{2,048 + 1,024}_{\text{BE7}} + \underbrace{32 + 16}_{\text{BD7}} + \underbrace{8}_{\text{BC7}}$$

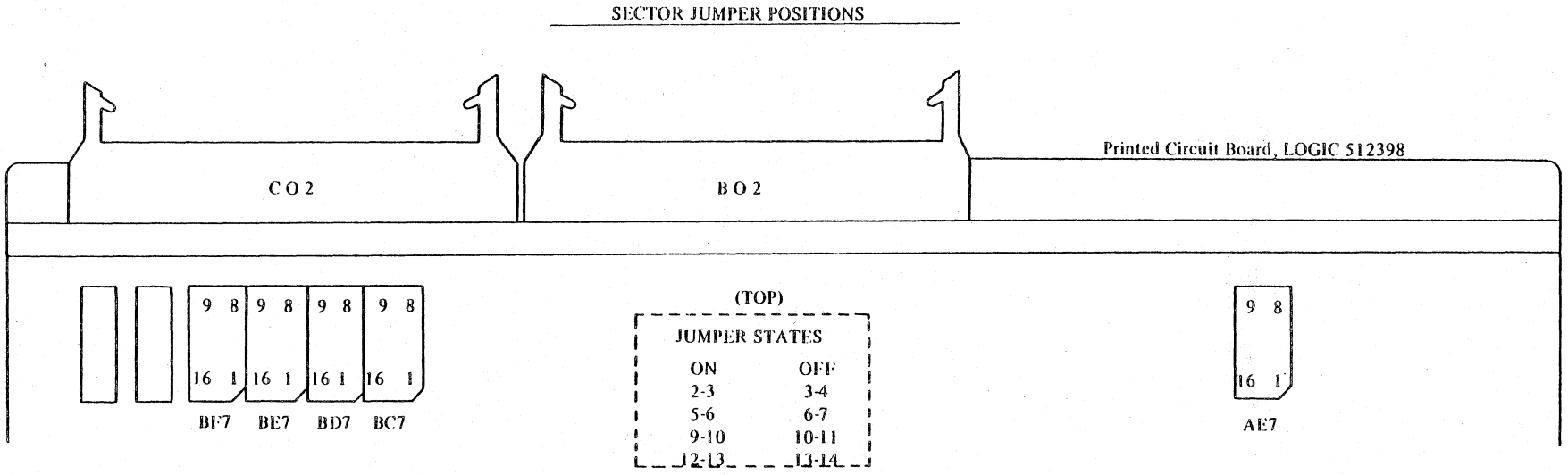
Therefore, jumper plugs should be placed on pins 13 - 12 and 10 - 9 of BE7, pins 06 - 05 and 03 - 02 of BD7, and pins 13 - 12 of BC7. However, those pins representing byte-count value not appearing in the calculation must also be jumpered (the complementary position).

In this case, the number of bytes in the last sector is calculated as follows.

$28,160 - 8 \times 3,129 = 3,128$

Namely, the last sector is one byte shorter than the others.

Table 3.4-1 Setting of Sector Count



Sector Count	Location BC7					Location BD7				Location BE7					Location BF7			Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
1	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	2-3	6-7	9-10	12-13	3-4	5-6	9-10	13-14	28160
2	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	3-4	5-6	9-10	13-14	2-3	5-6	10-11	13-14	14080
3	3-4	5-6	10-11	12-13	3-4	5-6	10-11	12-13	3-4	6-7	9-10	13-14	3-4	5-6	10-11	13-14	9387/9386
4	2-3	5-6	9-10	12-13	2-3	5-6	9-10	13-14	2-3	5-6	10-11	12-13	2-3	6-7	10-11	13-14	7040
5	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	2-3	6-7	9-10	13-14	2-3	6-7	10-11	13-14	5632
6	2-3	6-7	9-10	13-14	2-3	6-7	9-10	13-14	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	4694/4690
7	3-4	5-6	9-10	13-14	2-3	5-6	10-11	12-13	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	4023/4022
8	2-3	5-6	9-10	12-13	2-3	5-6	10-11	12-13	2-3	6-7	9-10	12-13	3-4	6-7	10-11	13-14	3520
9	3-4	6-7	10-11	12-13	2-3	5-6	10-11	13-14	3-4	6-7	9-10	12-13	3-4	6-7	10-11	13-14	3129/3128

Sector Count	Location BC7					Location BD7				Location BE7				Location BF7				Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
10	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	3-4	5-6	10-11	12-13	3-4	6-7	10-11	13-14	2816
11	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	2-3	6-7	10-11	12-13	3-4	6-7	10-11	13-14	2560
12	3-4	5-6	10-11	12-13	3-4	5-6	10-11	13-14	2-3	6-7	10-11	12-13	3-4	6-7	10-11	13-14	2347/2343
13	3-4	5-6	9-10	13-14	2-3	5-6	9-10	13-14	3-4	6-7	10-11	12-13	3-4	6-7	10-11	13-14	2167/2156
14	2-3	5-6	10-11	12-13	2-3	6-7	9-10	12-13	2-3	5-6	9-10	13-14	3-4	6-7	10-11	13-14	2012/2004
15	2-3	6-7	9-10	13-14	2-3	6-7	9-10	13-14	2-3	5-6	9-10	13-14	3-4	6-7	10-11	13-14	1878/1868
16	2-3	5-6	9-10	12-13	2-3	6-7	9-10	12-13	3-4	5-6	9-10	13-14	3-4	6-7	10-11	13-14	1760
17	3-4	6-7	10-11	12-13	2-3	5-6	9-10	13-14	3-4	5-6	9-10	13-14	3-4	6-7	10-11	13-14	1657/1648
18	3-4	6-7	9-10	12-13	2-3	6-7	10-11	13-14	3-4	5-6	9-10	13-14	3-4	6-7	10-11	13-14	1565/1555
19	3-4	5-6	10-11	12-13	3-4	6-7	9-10	12-13	2-3	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1483/1466
20	2-3	5-6	9-10	12-13	2-3	5-6	9-10	13-14	2-3	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1408
21	3-4	6-7	9-10	12-13	2-3	5-6	10-11	13-14	2-3	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1341/1340
22	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1280
23	3-4	6-7	10-11	12-13	3-4	6-7	9-10	12-13	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1225/1210
24	2-3	6-7	9-10	13-14	2-3	6-7	10-11	12-13	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1174/1158
25	3-4	5-6	9-10	13-14	3-4	5-6	9-10	13-14	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1127/1112
26	2-3	5-6	10-11	12-13	2-3	5-6	10-11	13-14	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1084/1060
27	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	1043/1042
28	2-3	6-7	9-10	12-13	3-4	5-6	9-10	12-13	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	1006/998
29	2-3	5-6	10-11	12-13	3-4	6-7	9-10	12-13	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	972/944
30	3-4	5-6	10-11	12-13	3-4	5-6	10-11	12-13	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	939/929
31	3-4	6-7	9-10	12-13	3-4	6-7	10-11	12-13	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	909/890
32	2-3	5-6	9-10	12-13	3-4	5-6	9-10	13-14	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	880

Sector Count	Location BC7					Location BD7				Location BE7				Location BF7				Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
33	2-3	6-7	9-10	13-14	2-3	6-7	9-10	13-14	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	854/832
34	3-4	6-7	9-10	12-13	2-3	5-6	10-11	13-14	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	829/803
35	3-4	6-7	9-10	13-14	3-4	5-6	10-11	13-14	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	805/790
36	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	2-3	5-6	10-11	13-14	3-4	6-7	10-11	13-14	783/755
37	2-3	6-7	10-11	12-13	2-3	5-6	9-10	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	762/728
38	2-3	6-7	9-10	13-14	3-4	5-6	9-10	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	742/706
39	3-4	5-6	10-11	13-14	2-3	6-7	9-10	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	723/686
40	2-3	5-6	9-10	12-13	2-3	5-6	10-11	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	704
41	3-4	5-6	9-10	12-13	3-4	5-6	10-11	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	687/680
42	3-4	5-6	9-10	12-13	2-3	6-7	10-11	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	671/649
43	3-4	5-6	9-10	12-13	3-4	6-7	10-11	12-13	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	655/650
44	2-3	5-6	9-10	12-13	2-3	5-6	9-10	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	640
45	2-3	6-7	10-11	13-14	2-3	5-6	9-10	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	626/616
46	3-4	6-7	9-10	13-14	3-4	5-6	9-10	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	613/575
47	2-3	5-6	9-10	13-14	2-3	6-7	9-10	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	600/560
48	3-4	5-6	10-11	12-13	3-4	6-7	9-10	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	587/571
49	3-4	5-6	9-10	12-13	2-3	5-6	10-11	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	575/560
50	2-3	5-6	10-11	13-14	2-3	5-6	10-11	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	564/524
51	3-4	6-7	10-11	12-13	3-4	5-6	10-11	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	553/510
52	2-3	6-7	9-10	12-13	2-3	6-7	10-11	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	542/518
53	2-3	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	532/496
54	2-3	6-7	10-11	12-13	3-4	6-7	10-11	13-14	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	522/494
55	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	512

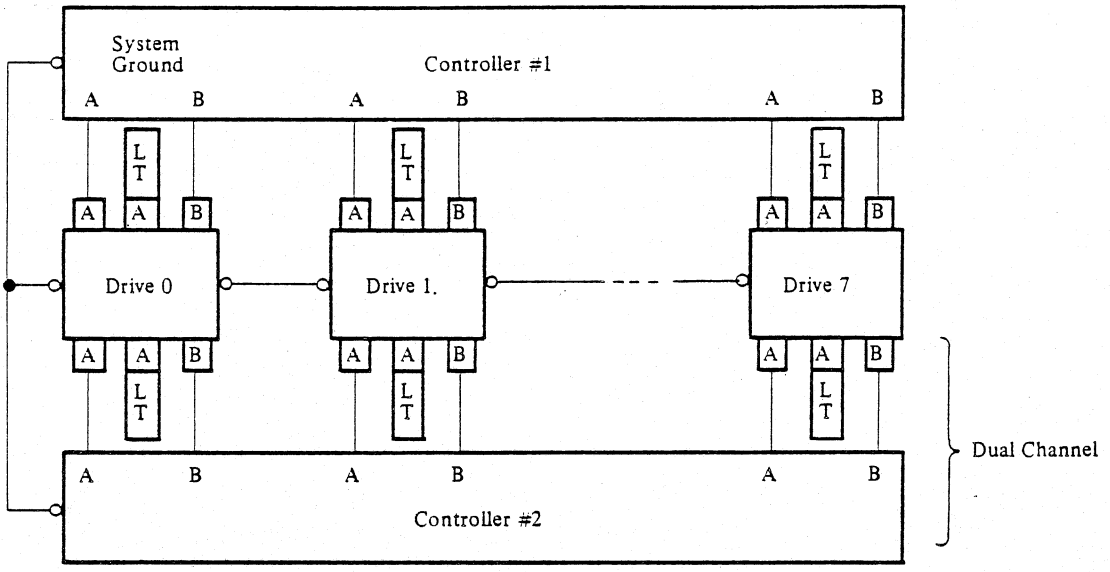
Sector Count	Location BC7					Location BD7				Location BE7				Location BF7			Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
56	3-4	5-6	9-10	13-14	2-3	5-6	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	503/495
57	3-4	5-6	9-10	12-13	3-4	5-6	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	495/440
58	2-3	6-7	9-10	13-14	3-4	5-6	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	486/458
59	2-3	6-7	9-10	12-13	2-3	6-7	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	478/436
60	2-3	6-7	9-10	13-14	2-3	6-7	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	470/430
61	2-3	6-7	9-10	12-13	3-4	6-7	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	462/440
62	3-4	5-6	9-10	13-14	3-4	6-7	9-10	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	455/405
63	3-4	5-6	9-10	12-13	2-3	5-6	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	447/446
64	2-3	5-6	9-10	13-14	2-3	5-6	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	440
65	2-3	6-7	10-11	13-14	2-3	5-6	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	434/384
66	3-4	5-6	10-11	12-13	3-4	5-6	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	427/405
67	3-4	6-7	9-10	13-14	3-4	5-6	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	421/374
68	3-4	5-6	9-10	12-13	2-3	6-7	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	415/355
69	3-4	6-7	10-11	12-13	2-3	6-7	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	409/348
70	3-4	5-6	10-11	13-14	2-3	6-7	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	403/353
71	3-4	6-7	9-10	12-13	3-4	6-7	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	397/370
72	2-3	5-6	9-10	13-14	3-4	6-7	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	392/328
73	2-3	6-7	10-11	13-14	3-4	6-7	10-11	12-13	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	386/368
74	3-4	6-7	9-10	12-13	2-3	5-6	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	381/347
75	2-3	5-6	9-10	13-14	2-3	5-6	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	376/336
76	3-4	5-6	10-11	13-14	2-3	5-6	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	371/335
77	2-3	6-7	9-10	12-13	3-4	5-6	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	366/344
78	2-3	6-7	10-11	12-13	3-4	5-6	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	362/286

Sector Count	Location BC7					Location BD7				Location BE7				Location BF7			Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
79	3-4	6-7	9-10	13-14	3-4	5-6	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	357/314
80	2-3	5-6	9-10	12-13	2-3	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	352
81	2-3	5-6	10-11	12-13	2-3	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	348/320
82	2-3	5-6	9-10	13-14	2-3	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	344/296
83	2-3	5-6	10-11	13-14	2-3	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	340/280
84	2-3	5-6	9-10	12-13	3-4	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	336/272
85	2-3	5-6	10-11	12-13	3-4	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	332/272
86	2-3	5-6	9-10	13-14	3-4	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	328/280
87	2-3	5-6	10-11	13-14	3-4	6-7	9-10	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	324/296
88	2-3	5-6	9-10	12-13	2-3	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	320
89	3-4	6-7	9-10	12-13	2-3	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	317/264
90	3-4	6-7	10-11	12-13	2-3	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	313/303
91	2-3	6-7	9-10	13-14	2-3	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	310/260
92	3-4	5-6	10-11	13-14	2-3	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	307/223
93	3-4	5-6	9-10	12-13	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	303/284
94	2-3	5-6	10-11	12-13	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	300/260
95	3-4	6-7	10-11	12-13	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	297/242
96	2-3	6-7	9-10	13-14	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	294/230
97	3-4	5-6	10-11	13-14	3-4	5-6	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	291/224
98	2-3	5-6	9-10	12-13	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	288/224
99	3-4	6-7	9-10	12-13	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	285/230
100	2-3	6-7	10-11	12-13	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	282/242
101	3-4	5-6	9-10	13-14	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	279/260

Sector Count	Location BC7					Location BD7				Location BE7				Location BF7				Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
102	3-4	6-7	9-10	13-14	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	277/183
103	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	274/212
104	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	271/247
105	3-4	6-7	9-10	12-13	3-4	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	269/184
106	2-3	6-7	10-11	12-13	3-4	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	266/230
107	2-3	5-6	9-10	13-14	3-4	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	264/176
108	3-4	6-7	9-10	13-14	3-4	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	261/233
109	3-4	5-6	10-11	13-14	3-4	6-7	10-11	13-14	2-3	6-7	10-11	13-14	3-4	6-7	10-11	13-14	259/188
110	2-3	5-6	9-10	12-13	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	256
111	2-3	6-7	9-10	12-13	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	254/220
112	2-3	5-6	10-11	12-13	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	252/188
113	2-3	6-7	10-11	12-13	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	250/160
114	2-3	5-6	9-10	13-14	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	248/136
115	3-4	6-7	9-10	13-14	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	245/230
116	3-4	5-6	10-11	13-14	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	243/215
117	3-4	6-7	10-11	13-14	2-3	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	241/204
118	3-4	5-6	9-10	12-13	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	239/197
119	3-4	6-7	9-10	12-13	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	237/194
120	3-4	5-6	10-11	12-13	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	235/195
121	3-4	6-7	10-11	12-13	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	233/200
122	3-4	5-6	9-10	13-14	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	231/209
123	3-4	6-7	9-10	13-14	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	229/222
124	2-3	5-6	10-11	13-14	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	228/116

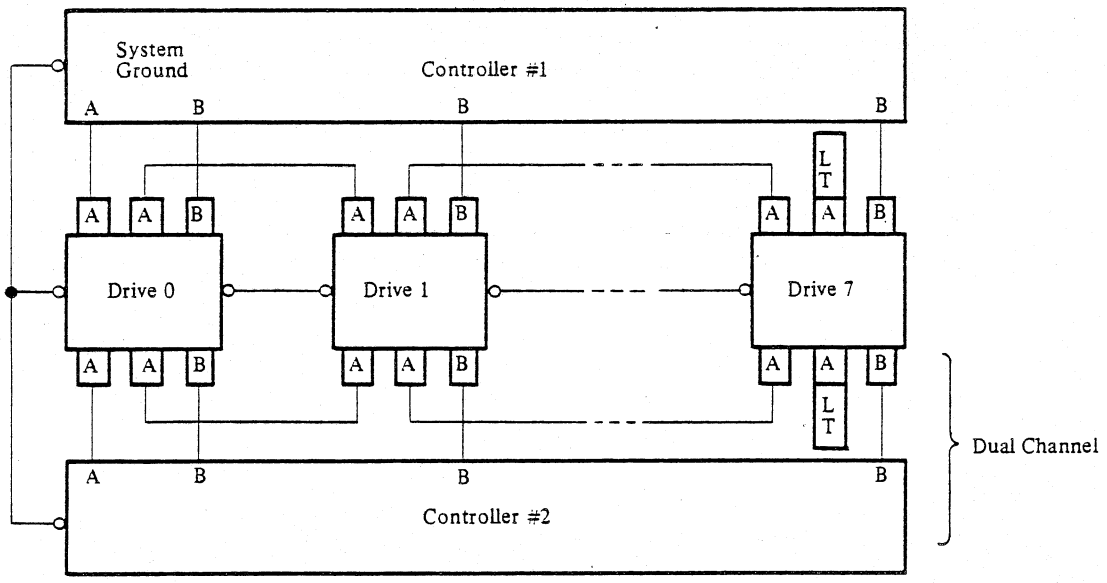
Sector Count	Location BC7					Location BD7				Location BE7					Location BF7			Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	spare	
125	2-3	6-7	10-11	13-14	3-4	5-6	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	226/136
126	2-3	5-6	9-10	12-13	2-3	6-7	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	224/160
127	2-3	6-7	9-10	12-13	2-3	6-7	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	222/188
128	2-3	5-6	10-11	12-13	2-3	6-7	9-10	12-13	3-4	6-7	10-11	13-14	3-4	6-7	10-11	13-14	220

One of the following interface cable configurations must be chosen depending on the feature of the controller. (Note; Dual Channel Feature is optional.)



Note that Line Terminators (LT) are required in each drive in a radial cable configuration.

Figure 3.5-1 Radial Cable Configuration



Note that a Line Terminator (LT) is required in the last drive in a daisy-chain cable configuration.

Figure 3.5-2 Daisy-Chain Cable Configuration

3.5 OPERATOR PANEL

Switches and indicators on the operator panel are shown in Figure 3.5-1.

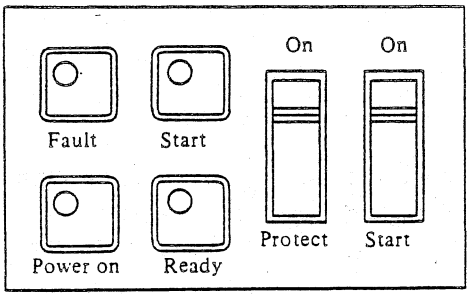


Figure 3.5-1 Operator Panel

(1) Start-On (Switch)

When the Remote/Local switch on the control panel of DC power supply unit is set to Local, this switch enables rotation of the spindle motor. The heads start Initial Seek operation and stop on the cylinder zero, approximately 40 seconds later, lighting the Ready lamp. The spindle motor stops rotating approximately 15 seconds after the switch is set to off position.

When the Remote/Local switch is set to Remote, the spindle motor starts and stops rotating in accordance with the Power Sequence Pick/Hold commands issued from the controller if the Start switch is On.

(2) Protect-On (Switch)

Inhibits Write operation. If a write command is issued from the controller while the switch is On, the Fault and Control Check conditions will be returned to the controller.

(3) Start (LED)

Indicates that the spindle is rotating.

(4) Ready (LED)

Indicates that the spindle has reached the rated speed and no fault condition exists in the drive. It goes off when the heads are seeking to the desired cylinder.

(5) Fault (LED and Switch)

Indicates a Fault condition (i.e., R/W check status) or a Seek Error. Depressing the indicator switch clears this condition.

(6) Power On

Indicates that the DC power supply unit is on.

3.6 INDICATOR UNIT ----- HGAMU (B16B-7830-0010A#U)

These switches and indicators are provided for aiding maintenance, and are shown in Figure 3.6-1.

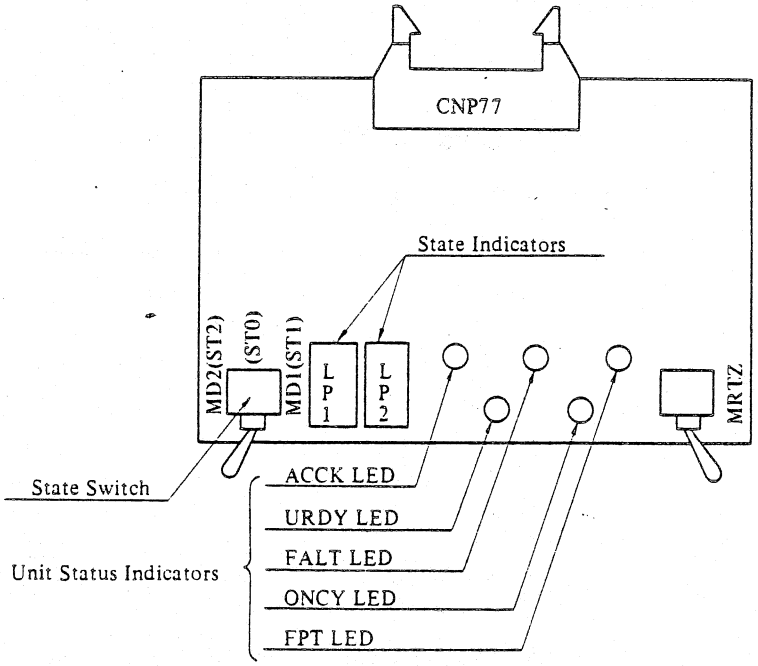


Figure 3.6-1 Switches and Indicators

(1) Unit Status Indicators (LEDs)

Indicate Unit Status as shown in Table 3.6-1. These statuses are also issued to the controller as States 0 to 4 when both Tag 4 and 5 are false if this feature is utilized.

Refer to item (2-1) ∿ (2-5) in Section 7.4 for detailed descriptions of each state.

Table 3.6-1 Unit Status Indicators

Name of LED	Color of LED	Content
URDY	Green	Unit Ready
ONCY	Green	On Cylinder
ACCK	Red	Seek Error (Access Check)
FALT	Red	Fault
FPT	Yellow	Write Protected (File Protect)

(2) State Switch and State Indicators (Toggle Switch and 7-Segment LEDs)

Two 7-segment LEDs indicate detailed drive states as shown in Table 3.6-2 in accordance with the position of the State Switch.

Table 3.6-2 Status and State

State Switch Position		Left (ST 2)	Center (ST 0)	Right (ST 1)
LED \ STATE / Bit		DE Sequence State	Write/Read Check State	Access State
LP1	1	DE Sequence Latch 1	Index Check	DE Sequence Check
	2	DE Sequence Latch 2	Control Check	Access Timeout Check
	4	DE Sequence Latch 4	Multi Head Check	Over Shoot Check
	8	Hall Alarm	Head Short Check	Rezero Mode Latch
LP2	1	Motor At Speed	Write Current on Read Check	Servo Latch
	2	Inhibit DE Seq. Recycle	Write Transition Check	Linear Mode Latch
	4	Unit Ready	Delta I Write Check	Control Latch
	8	Access Busy	Servo Off-Track	Wait Latch

DE Sequence Stage (ST 2)

DE Sequence 1, 2 and 4

Indicates that an abnormal Start/stop sequence of the DE occurred in the drive. Details are described in item (5-1) of Section 7.4.

Hall Alarm

Indicates that all output signals from the hall-elements used to detect the pole position of the rotor in the spindle motor are high or low level simultaneously.

Motor At Speed

Indicates that the spindle motor is rotating at 3,961 RPM ±2%.

Inhibit DE Sequence Recycle

Indicates that Run State Good goes false while the DE Sequence Latch is in State 7. Stop sequence of the DE may be inhibited hereafter. Switching off the drive power or pushing the Start switch to Off position clears this state.

Unit Ready

Indicates that the drive has reached the rated rotational speed and heads are positioned on track.

Access Busy

Indicates that the heads are in motion, i.e., heads are performing Seek, RTZ or Offset operation.

Write/Read Check State (ST 0)

Refer to item (4) in Section 7.4.

Access State (ST 1)

Refer to item (5) in Section 7.4.

(3) MRTZ (Manual RTZ) Switch

The head performs RTZ operation when this maintenance-aid switch is pressed.

3.7 STANDALONE CHECK

After the preceding Sections 3.1 through 3.6 have been applied as required (3.1, in particular), a basic standalone check of drive operation can be made. The rotary actuator must be unlocked (refer to Section 2.3). Proceed with the check as follows:

(1) With the circuit breaker and Start switch OFF, plug in the AC line cord.

(2) Turn the circuit breaker ON. The Power on LED on the operator panel should light. The blower motor starts and the 7-Segment display is 00.

(3) Press the Start switch on the operator panel to ON. The Start LED on the operator panel should light. The DC motor will begin to rotate. Unless a problem develops, the 7-Segment display will continue to show 00. Approximately 40 seconds later, the Ready LED on the operator panel should light, and the green On Cylinder and Unit Ready LEDs on the Indicator PCB should light.

(4) Depress the MRTZ switch on the Indicator PCB and note that the drive executes a RTZ operation. The On Cylinder and Unit Ready LEDs should blink during the carriage motion and remain On when locked on Cylinder 0.

This basic check has significance for initial Power On, Heads Load, Lock-on and RTZ capabilities.

HAPTER 4 SYSTEM INSTALLATION

4.1 CONTROL CABLE ("A" CABLE)

A description of the Control cable signals and Pin assignments will be found in Chapter 7.2.

"A" Cables may be installed radially or daisy-chained. Connect the "A" cable from the controller output port to the Interface PCB (DQEMU) or Dual channel PCB (DQFMU), (CNP 41 or 51), as shown in Figure 4.1-1. Note that Pin 1 is to the right when facing the rear of the drive.

In a daisy-chain configuration, the "A" cable will be continued by connecting another cable from the Terminator header, (CNP 42 or 52), to the next drives input (CNP 41 or 51).

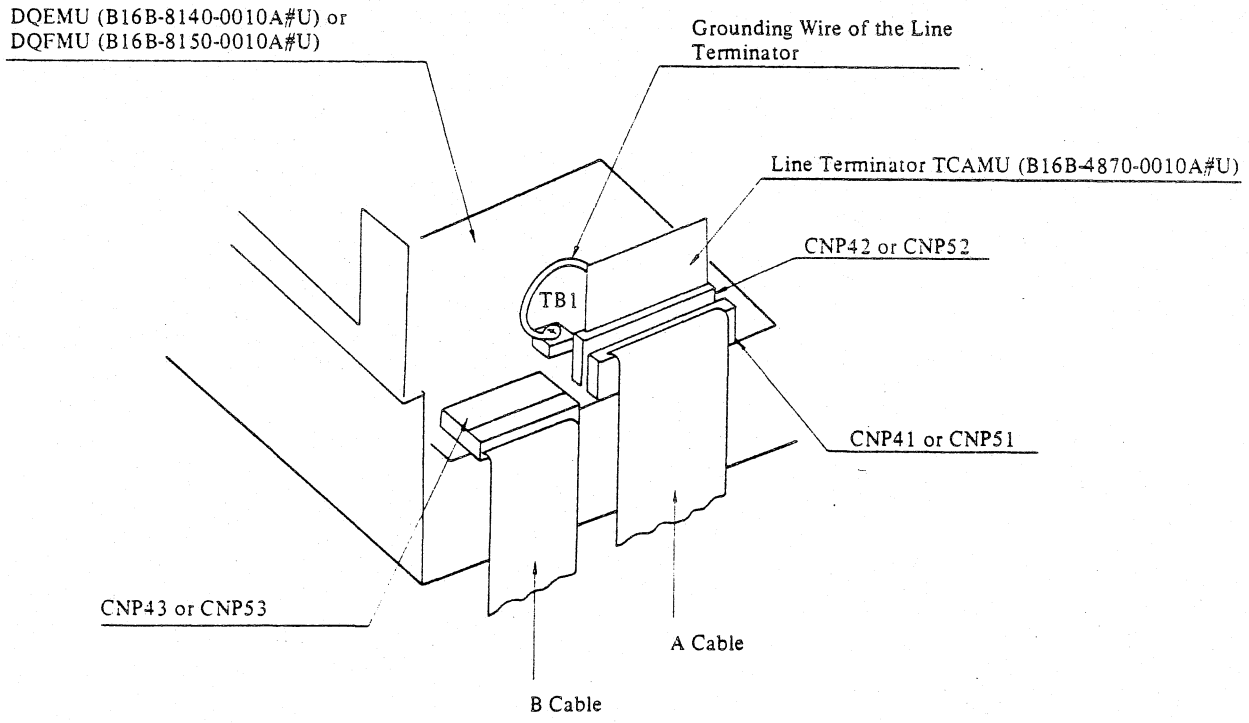


Fig. 4.1-1 Cable Connection

4.2 READ/WRITE CABLE ("B" CABLE)

A description of the Read/Write cable signals and Pin assignments will be found in Chapter 7.2.

"B" cables are always installed radially from the controller. Connect the "B" cable from the controller output port to the Interface PCB (DQEMU) or Dual Channel PCB (DQFMU), (CNP 43 or 53), as shown in Figure 4.1-1. Note that Pin 1 is to the right when facing the rear of the drive.

4.3 SYSTEM GROUNDING

(1) Definitions of SG, FG1 and FG2.

SG is Signal ground or DC ground and is isolated from AC ground within the drive.

FG1 is Frame ground or AC ground and is a direct short to chassis.

FG2 is a high impedance AC ground, connected to FG1 through a 510 Kohm resistor.

For shipment, SG is connected to FG2 with the shorting plate, as shown in Figure 4.3-1.

(2) Grounding Methods

It is always recommended that drives be grounded, and it is required if cable lengths longer than 10 ft. are used or if the drives are connected in the daisy-chain configuration. All grounding should be done with flat braided wire, preferably covered with a jacket or tubing.

Grounding methods vary with site and system integration design, and are commonly derived in a trial-and-error fashion. However, four approaches are offered in order of preference:

(a) Leave SG connected to FG2 (shipping configuration) and connect a flat braid wire to controller ground. If daisy-chained, daisy-chain the braid from SG to SG as shown in Figure 4.3-2.

(b) Connect SG to FG1 with the shorting plate. Connect a flat braid wire from SG to controller ground. If daisy-chained, daisy-chain the braid from SG to SG as shown in Figure 4.3-3.

(c) Remove the shorting plate, isolating SG and FG grounds. Connect a flat braid wire from SG to controller ground (preferably DC ground). In this case, the braided wire must be covered to prevent accidental shorting to chassis (AC ground).

(d) Leaving the same arrangement as in (c) above, connect another covered, braided wire from FG1 to controller chassis (AC ground).

(3) AC Considerations

(a) The controller should always be solidly connected to earth ground. The drives and the system are then grounded through the controller. (Controller AC-DC isolation is a function of design, and is assumed to be common in the four approaches described in (2) above.)

(b) It is always recommended that the drive, controller and CPU share a common AC branch circuit.

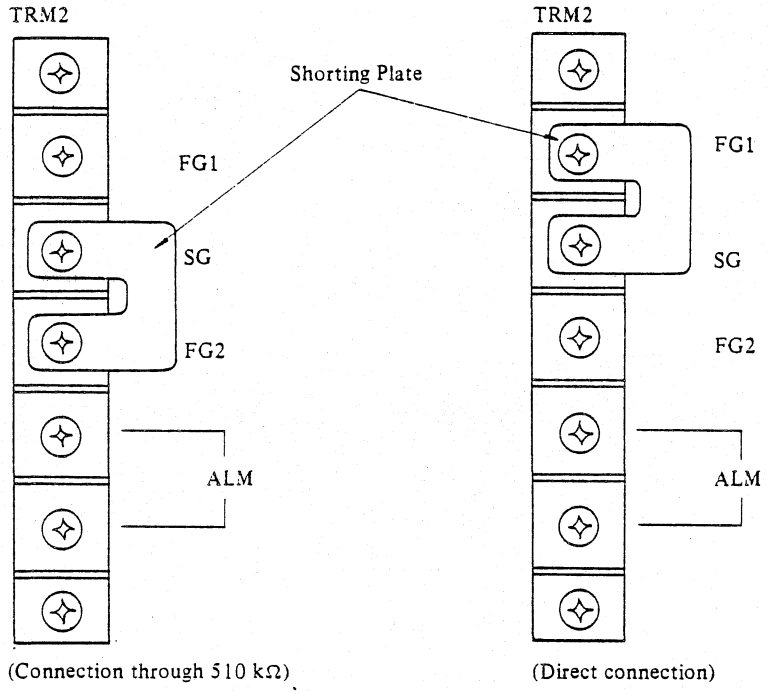


Fig. 4.3-1 Connection of FG and SG

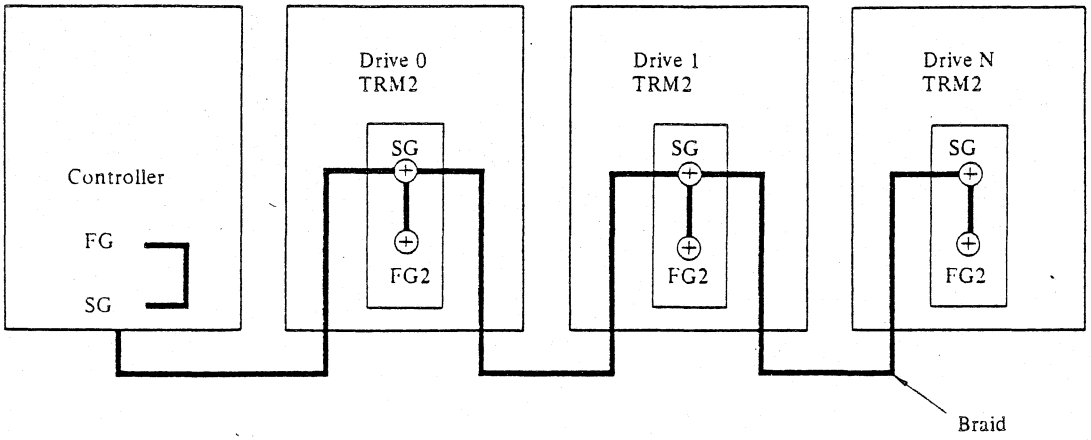


Fig. 4.3-2 SG/HI Z FG2 Common

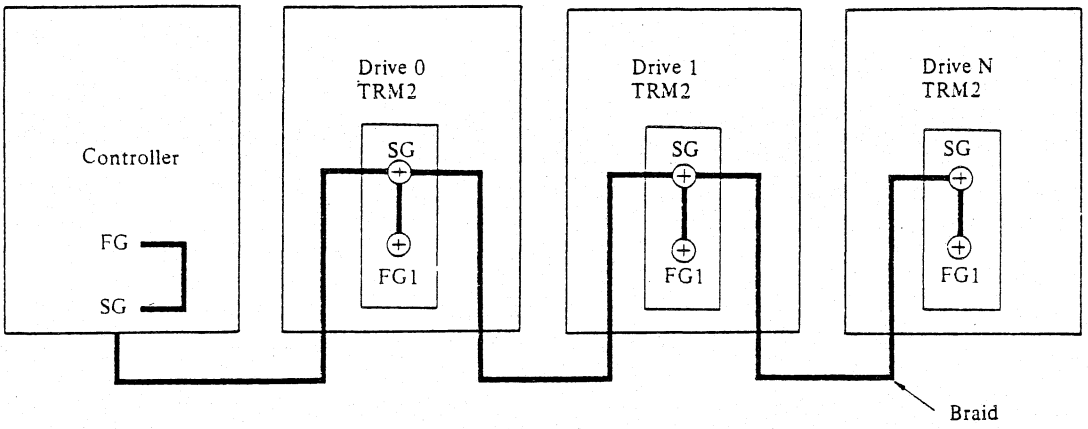


Fig. 4.3-3 SG/FG1 Common

CHAPTER 5 MECHANICAL ASSEMBLIES

5.1 CONSTRUCTION OF THE DRIVE

The overall construction is shown in Figure 5.1-1. The DE is supported horizontally at three points with rubber mounts for vibration and shock absorption. A shock sensor is provided on the DE to monitor for excess shock against the DE during shipping and handling. The rotary actuator is secured by a mechanical lock to prevent damage to the heads and disks during transportation. No mechanical lock is required for the spindle motor.

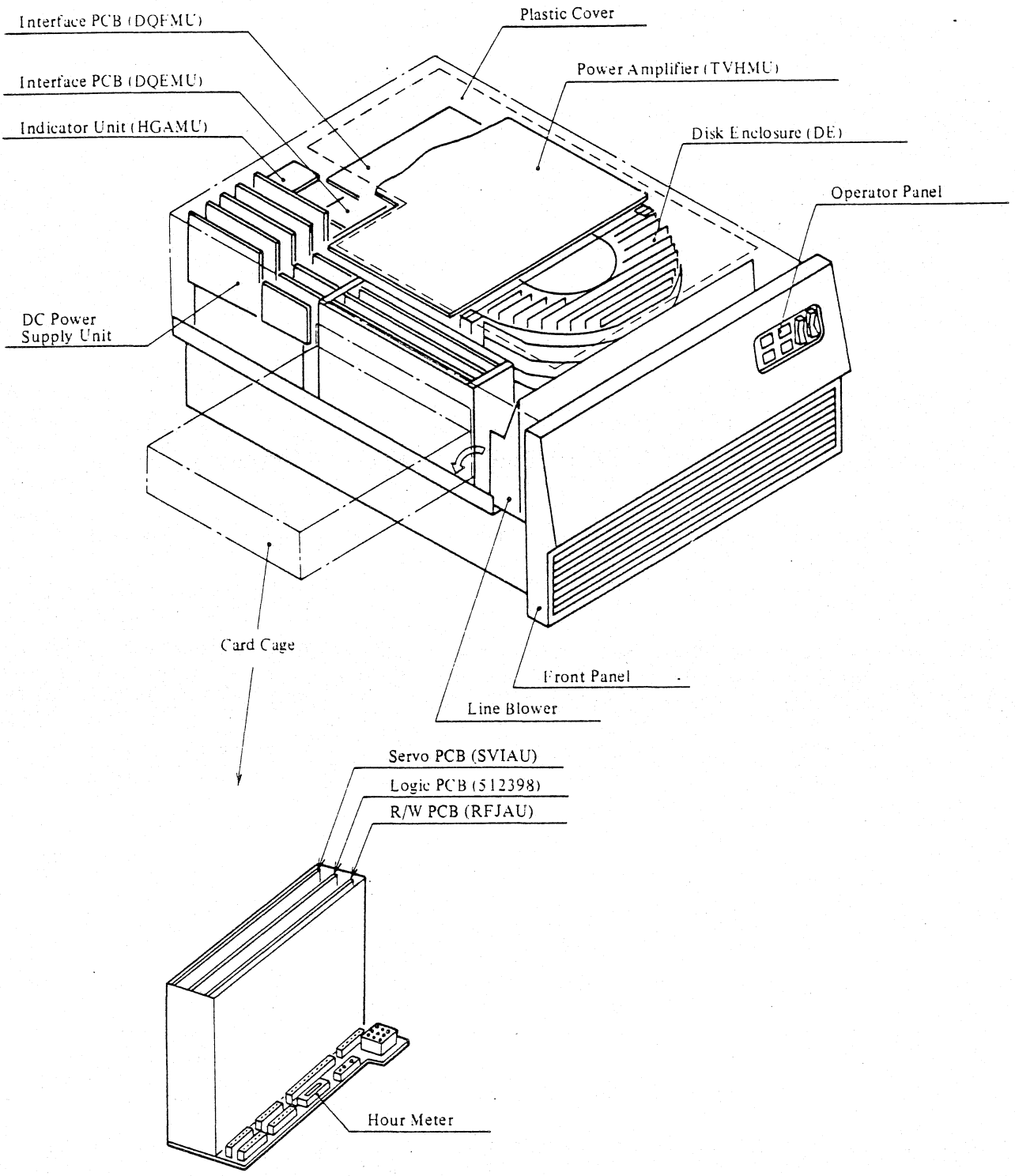
The Power Amplifier (TVHMU; B16B-8130-0010A#U or TVKMU; B16B-8800-0010A#U) which drives both spindle motor and rotary actuator is mounted horizontally above the DE (Old Version) or vertically behind the front panel (New Version).

Logic PCB (C16B-5123-0980#U), Servo Circuit (SVIAU; C16B-5501-0010#U) and Read/Write Circuit (RFJAU; C16B-5500-0990#U) are inserted in a card cage, and placed by the side of the DE. This card cage can be pulled up and turned 90 degrees for access to check signals on the back panel (BQGMU; B16B-8160-0010A#U).

Indicator unit (HGAMU; B16B-7830-0010A#U) is attached on top of the DC Power Supply, located at the rear of the drive. Five LEDs and two 7-segment LED displays provide the status of the drive.

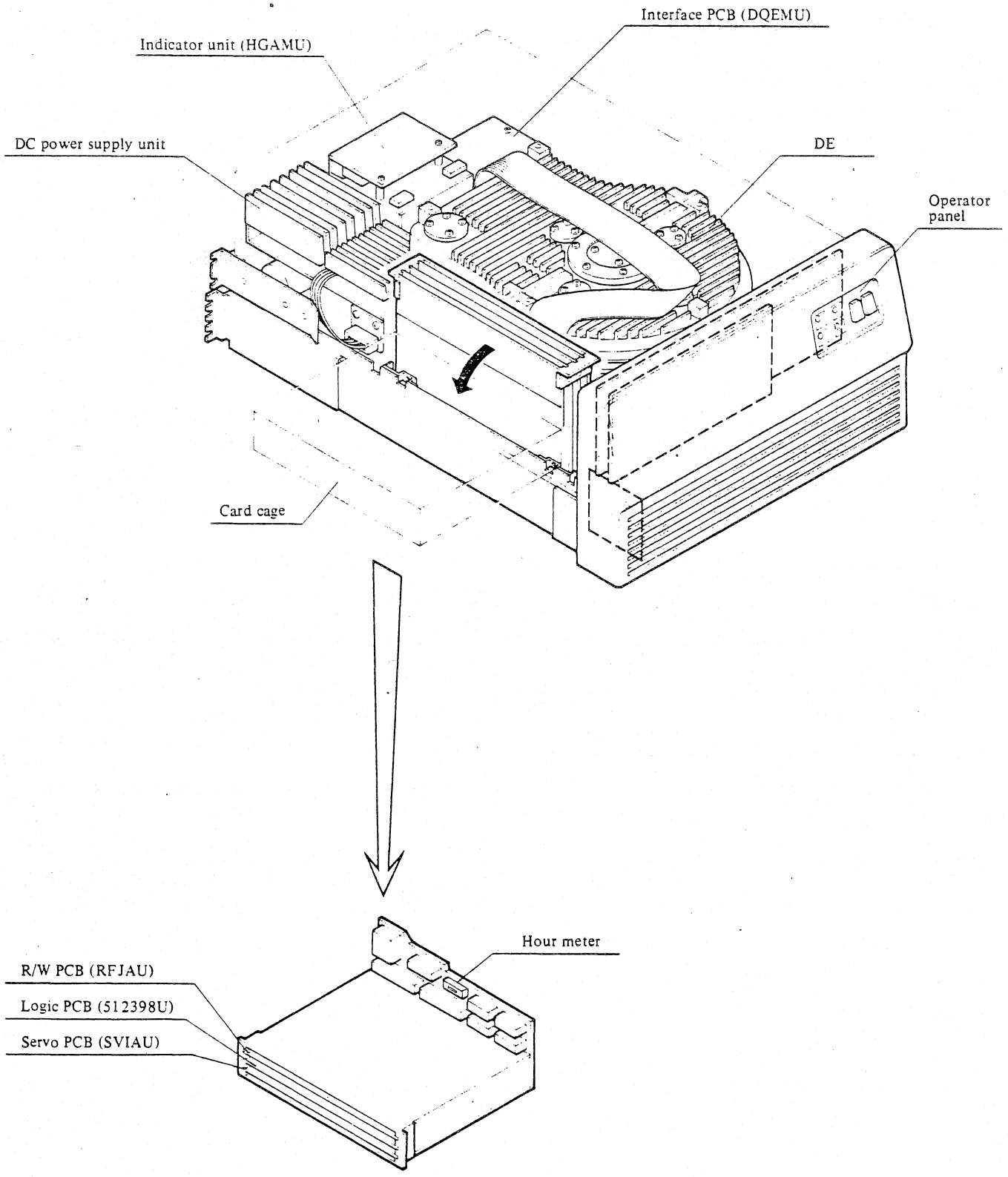
The interface PCBs are also located at the rear of the drive. When the sub-system is single channel, an interface PCB (DQEMU; B16B-8140-0010A#U) must be placed in the lower position. When the sub-system is dual channel, an additional interface PCB (DQFMU; B16B-8150-0010A#U) must be placed in the upper position.

The entire drive is cooled by a line blower located at the front of the drive.



(a) Old version

Figure 5.1-1 Construction of the Drive



(b) New version

Figure 5.1-1 - Continued

5.2 DISK ENCLOSURE (DE)

(1) Design Concept

The mechanical configuration of the DE shown in Figure 5.2-1 and 5.2-2 was designed to provide a compact, low power consumption, and maintenance-free file with enhanced performance. It features six 10.5 inch diameter disks and a rotary actuator with the fast average positioning time of 18 msec. The rotary actuator is completely balanced statically and dynamically by using a pair of moving coils, thereby avoiding undesired vibration that prolongs settling time.

(2) Spindle and Base Casting

The primary function of the spindle is to maintain precise and constant rotation of the assembled disks. The accuracy of rotation involves concentricity, precision, thermal and dynamic stability; all of which become more stringent as the track spacing gets tighter.

The dual-supported spindle construction reduces this problem. In this design, the supporting casting is divided into two pieces in a plane parallel to the spindle axis, with one of the divided pieces substantially retaining the rotating bearings. Thus, precise concentricity can be maintained.

With regard to the base casting, it is important to keep the relative dimension between the spindle and rotary actuator very rigid, especially in a dynamic mode. This has been given critical attention as track spacing and access time become smaller and shorter.

In the present drive, the rotary actuator is designed so that the rotating axis is pivoted at both ends, similar to the spindle. A pair of arms are extended from the spindle bearing part to the pivoting element of the rotary actuator. This technique, combined with the high rigidity of the actuator, provides resonant-free seek operation.

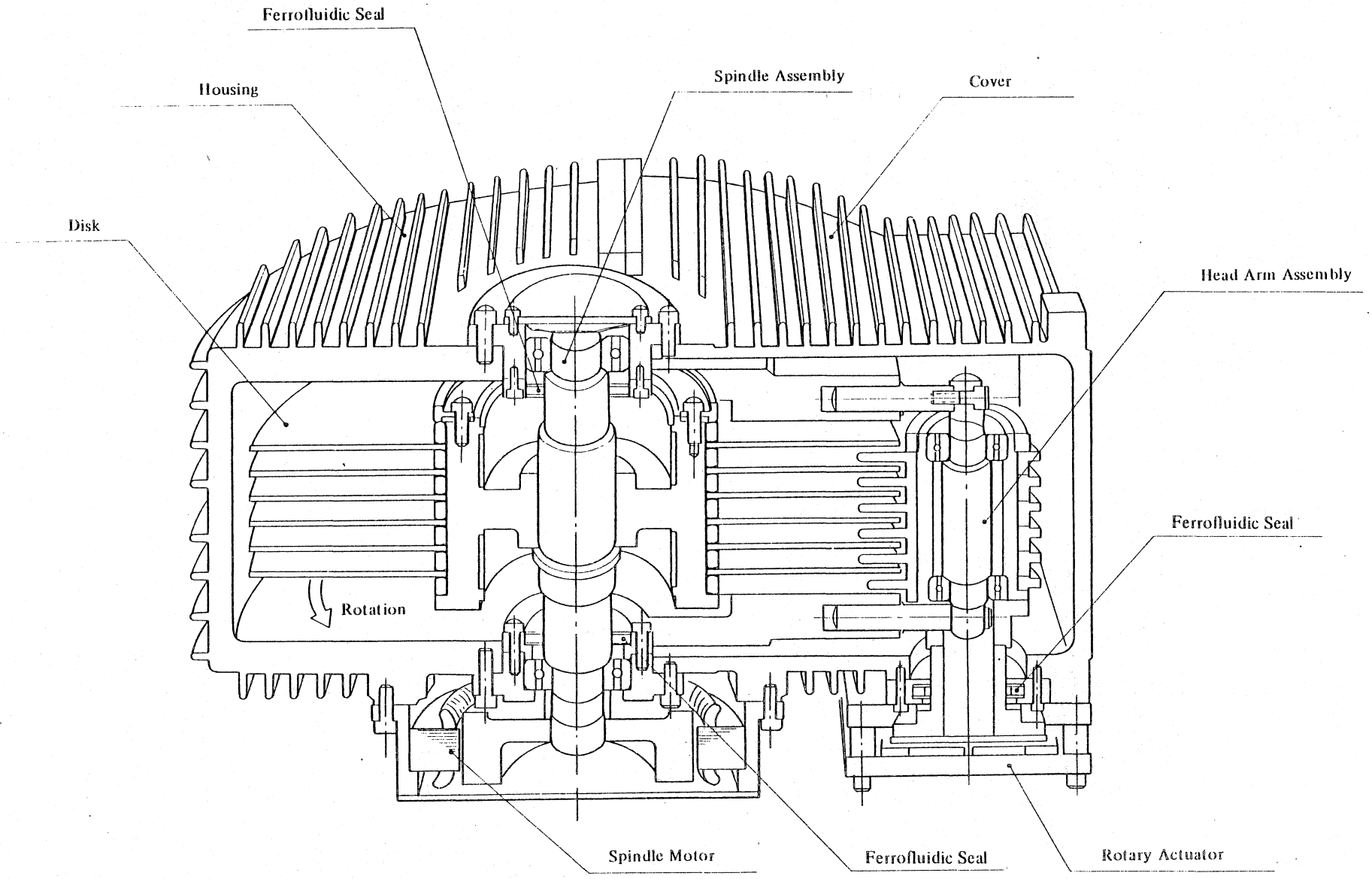


Figure 5.2-2 Cross Sectional View of the DE

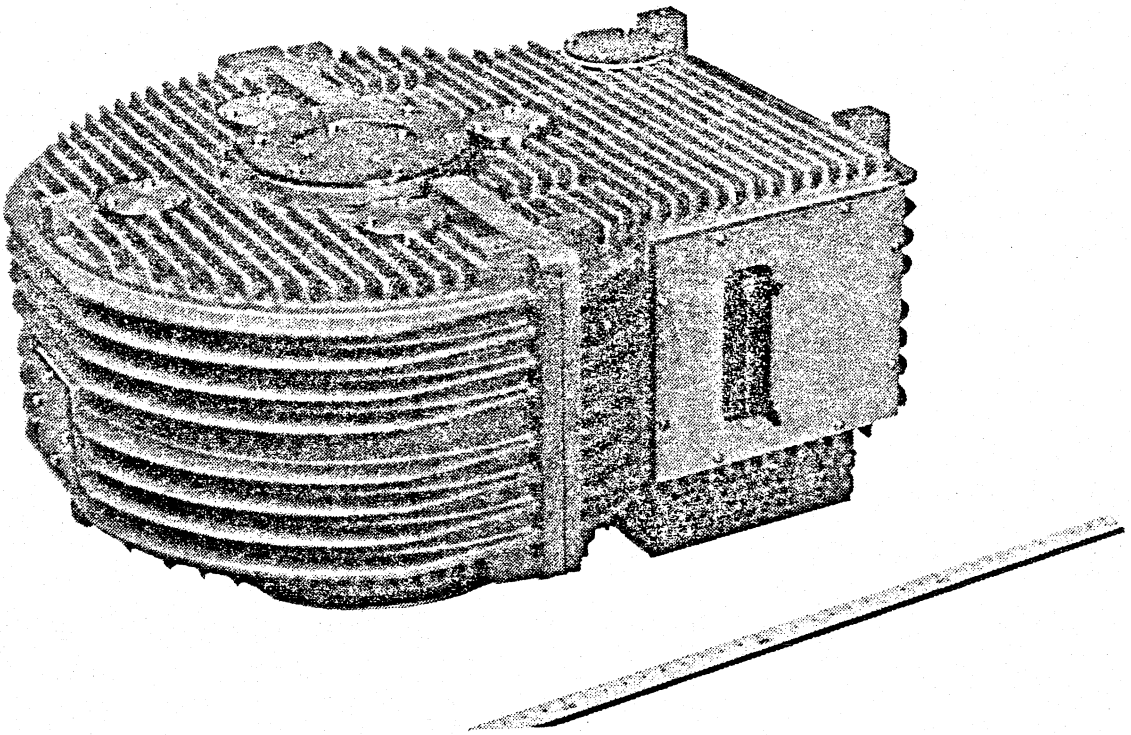


Figure 5.2-1 Outerview of the DE

(3) Air System

The fundamental and important function of the air system is to maintain an ultra-clean environment within the space of the DE to minimize the possibility of head-disk interference. In this DE, A new type of self circulating air system is provided. Features of the system are its simplicity and maintenance-free operation. Air flows through the disk spacings from the center to outside of the disks by the pressure difference between them, induced by the rotation of disks. An absolute filter, whose efficiency is 99.97 percent above 0.3 μm particle size dust, is attached within the spindle hub and is rotating with the disks. Partcile count goes very nearly zero in a few mintues from the start of rotation. Ferrofluidic seals are adopted to complete the elimination of air contamination.

To enhance the cooling efficiency, the housing is made entirely of aluminum casting with a high heat conductivity, and many fins formed around it. Air circulation is completely symmetrical in the disk stacking direction, and air flow

is well intermingled at the inside of disk hub for uniform and efficient cooling around the read/write heads along with the servo head.

5.3 ROTARY ACTUATOR

The drive shaft of the head-arm assembly in the DE is coupled directly to a bobbin supporting base to be driven by the rotary actuator outside the DE. Ferrofluidic seal is utilized to separate inside and outside the DE. Two coil-bobbins are attached to the bobbin supporting base, and two magnetic circuits are provided to supply torque to the coil bobbins, moving the head-arm assembly to the desired cylinder within a short access time.

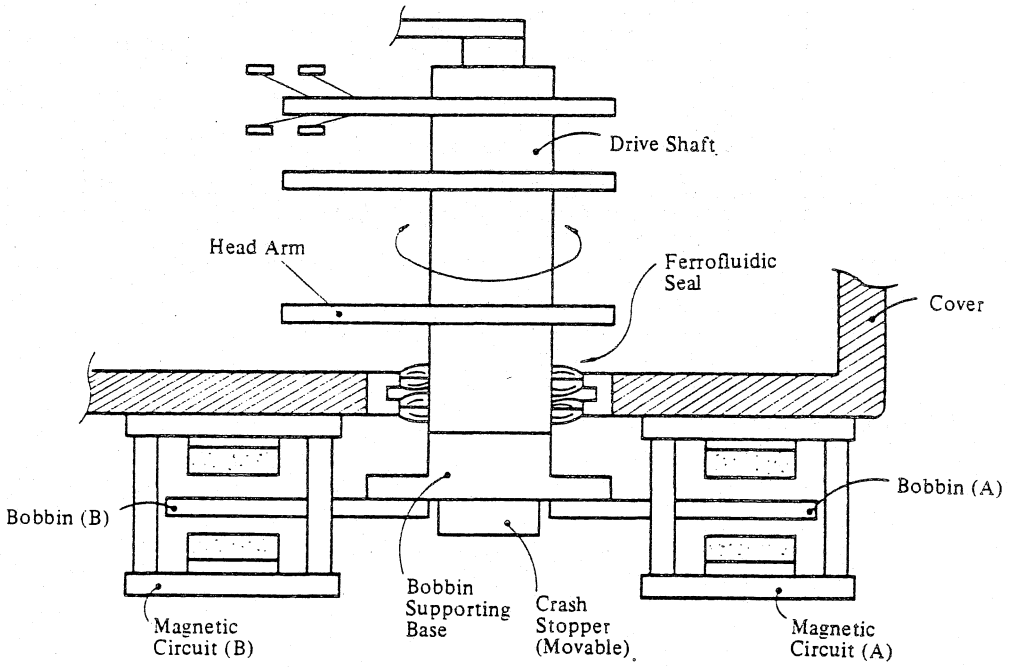


Figure 5.3-1 Construction of the Actuator

(1) Magnetic Circuit

The pair of magnetic circuits are constructed symmetrically as shown in Figure 5.3-2. Each circuit incorporates four permanent magnets (rare earth magnets) with two magnetic gaps in between. Each magnetic gap contains a uniformly spread magnetic field. The coil bobbin is inserted in it and generates torque proportional to the current in the coil and the intensity of the magnetic field. This torque is sufficient to move the head-arm assembly at the specified speed.

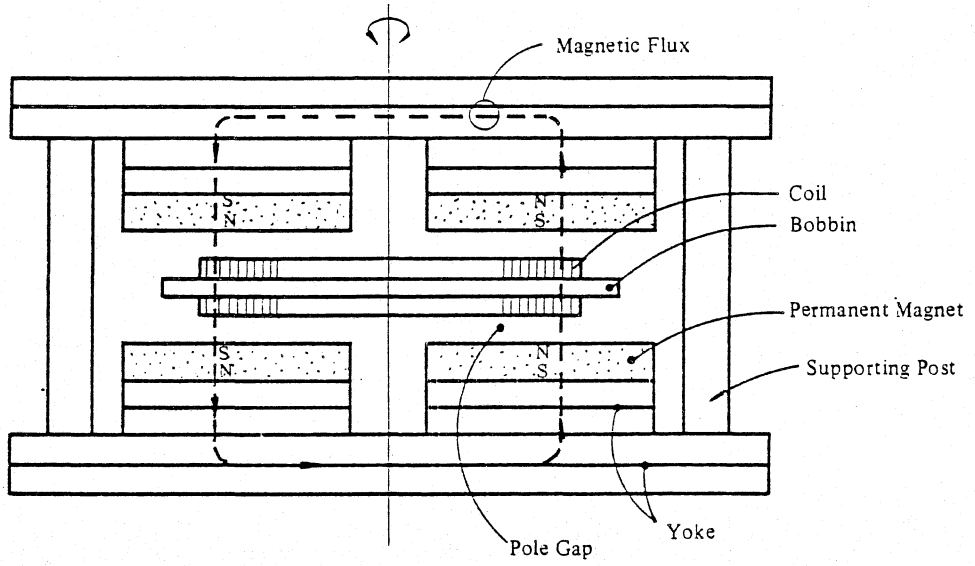


Figure 5.3-2 Magnetic Circuit

(2) Drive Coil

The two coil bobbins are identical. A pair of flat copper wire coils are attached on the front and rear side of each coil bobbin. The four coils are then connected in series to generate torque in the same direction due to the current flowing in each coil.

(3) Crash Stopper

The crash stopper consists of a moving part attached to the bobbin supporting base and fixed parts on the DE. It determines the movable range of the head-arm assembly, and provides safe deceleration in the event of an uncontrolled seek.

(4) Major Specifications

• Force coefficient	:	0.11	(kg-m/A)
• Movable section inertia	:	24×10^{-4}	($kg\text{-}m^2$)
• Coil resistance	:	10	(Ω) (20°)
• Moving angle	:	0.208	(rad)
• Magnetic circuit weight	:	2.4	(kg)

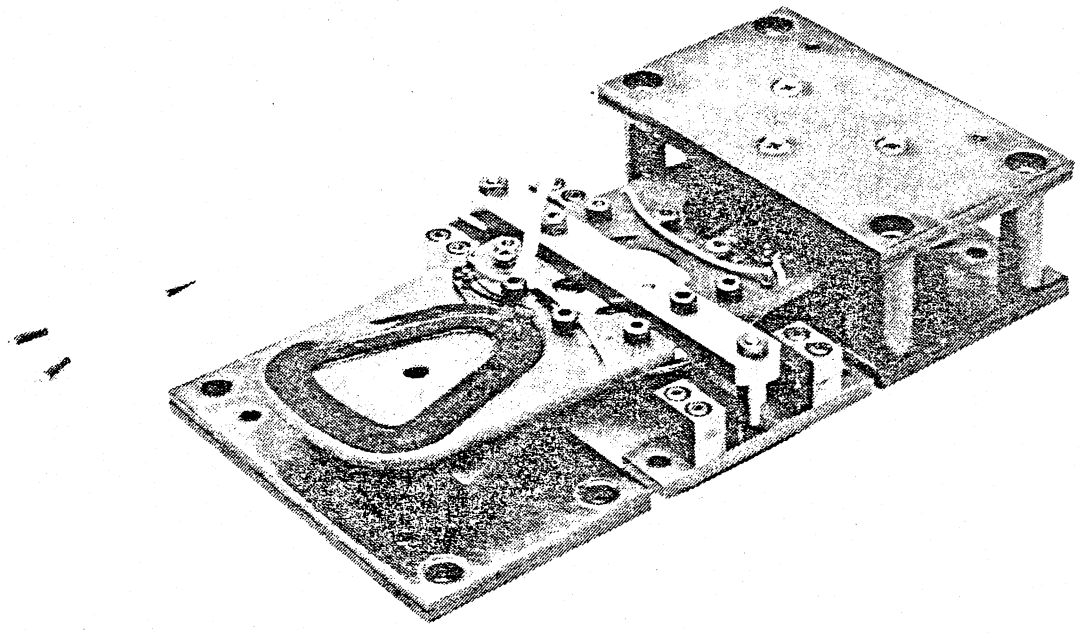


Figure 5.3-3 Outer view of Rotary Actuator

5.4 SPINDLE MOTOR

(1) Features

By adopting the brushless DC spindle motor and connecting the motor directly to the spindle shaft, the following are realized.

- The device becomes compact.
- Pulley and belts are unnecessary, therefore, no maintenance is required.
- Accuracy of rotational speed is improved.
- Vibration is reduced.
- Dynamic braking replaces mechanical brake

(2) Construction

Construction of the motor is shown in Figure 5.1-1. The rotor poles generate torque by the revolving magnetic field, and are connected directly to a single shaft to which magnetic disks are attached.
The stator winding generates the above mentioned revolving magnetic field by successively switching the current in it.
The rotor pole position detector determines the switching time of the current in the stator winding by detecting the position of rotor poles. The stator winding and rotor pole position detector are fixed in the motor housing, which is fixed on the DE base.

(3) Specification

Table 5.4-1 Specifications

Output	P	W	120
Rated torque	T	kg-cm	2.7
Rated revolution	N	rpm	3,961
Rated Current	I	A	4.0
Induced voltage constant	Ke	mV/rpm, O/P/phase	8.2
Winding resistance	Ra	Ω/phase at 20°C	1.12
Winding inductance	La	mH/phase	1.7
Winding phase number			3
Number of poles and pole pairs	2P		4
Position sensor		DN6839 Matsushita Electric	

The rated values are 3-phase, half drive (for 120° conduction)

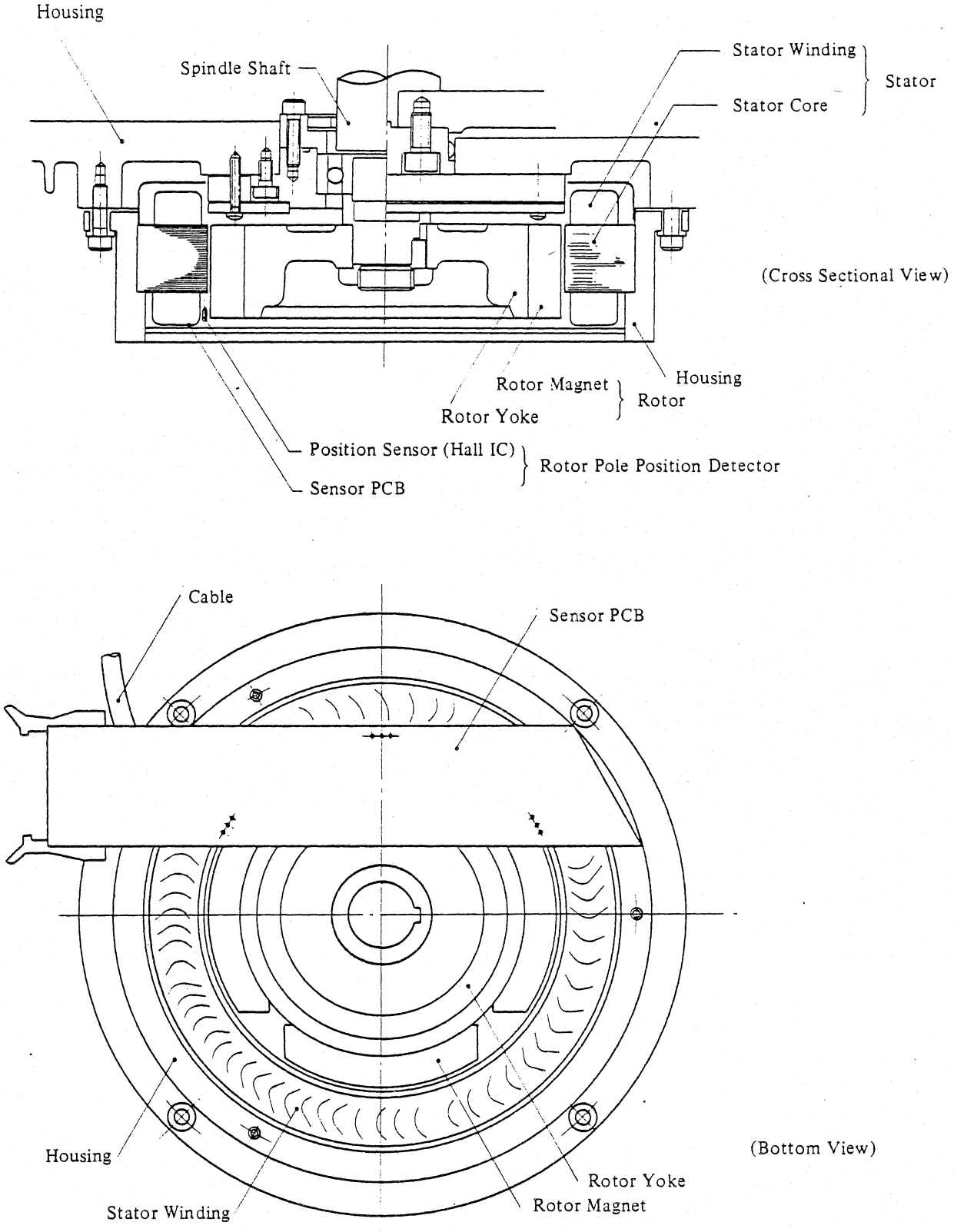


Figure 5.4-1 Construction of the Spindle Motor

(4) Principle of Operation

The brushless DC motor is made by replacing brushes and commutators of the ordinary DC motor with a rotor pole position detector and a semiconductor drive circuit. The schematic circuit of the 3-phase half-wave drive used is shown in Figure 5.4-2. The various waveforms when the DC motor is rotating in the regular direction are shown in Figure 5.4-3. Consequently, in an actual drive, the rotational force is obtained by energizing the windings in the order of C'-C → B'-B → A'-A.

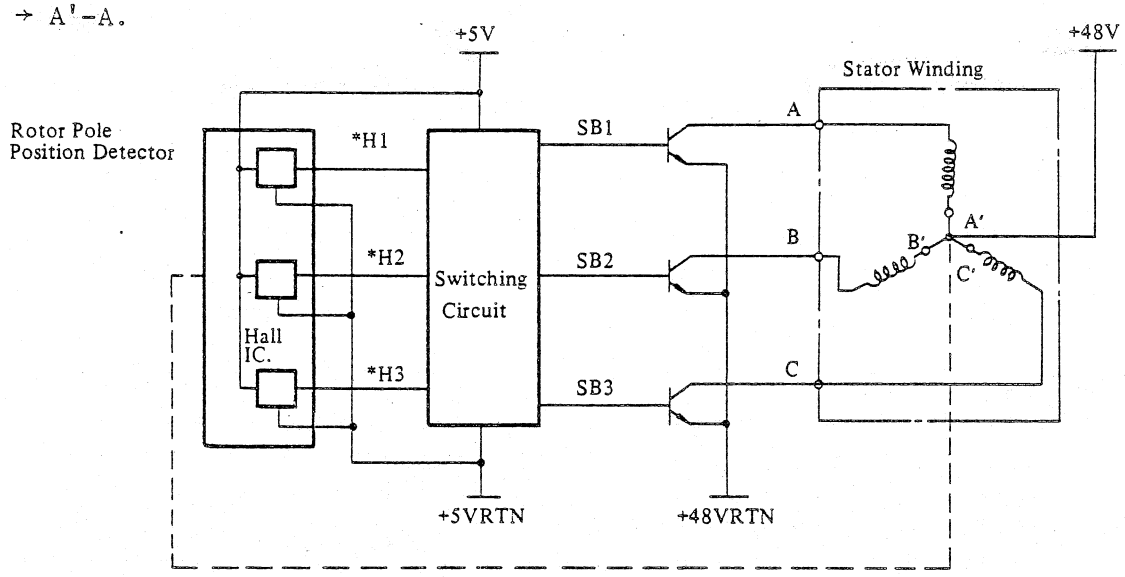


Figure 5.4-2 Schematic Diagram of the Drive Circuit

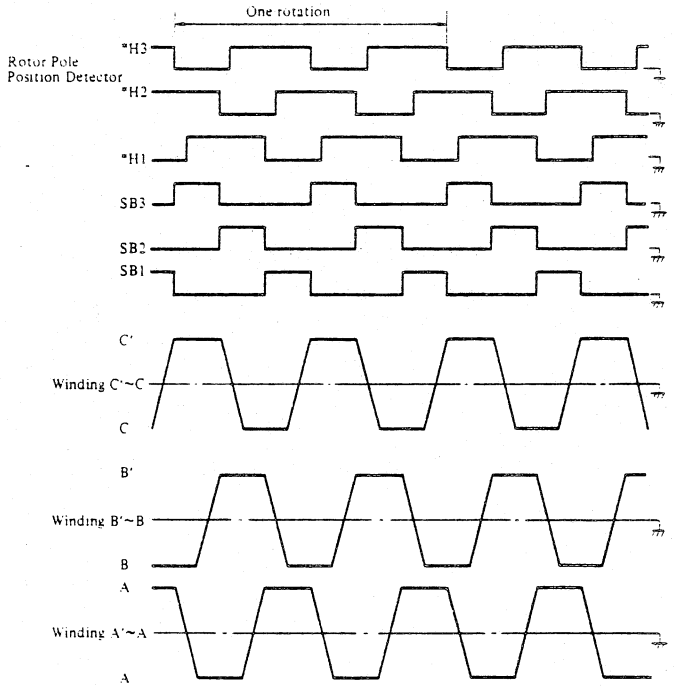


Figure 5.4-3 DC Motor Waveforms

5.5 MAGNETIC HEAD AND DISK

(1) Magnetic Head

To obtain a high recording density, advanced Winchester type CSS (Contact Start and Stop) heads are used for both moving and fixed heads. While the disks are not rotating, the heads rest on the disk surfaces in contact, but when the rotation starts, the heads begin to float over the disk surfaces. After the disks reach the specified rotational speed, the heads maintain the flying height with the balanced force of each load spring and the air-bearing between disk surfaces and the head sliders.

Therefore, to prevent wear caused by contact-start/stop, and to achieve minimum but stable flying height, the head is loaded slightly and its slider rails are tapered.

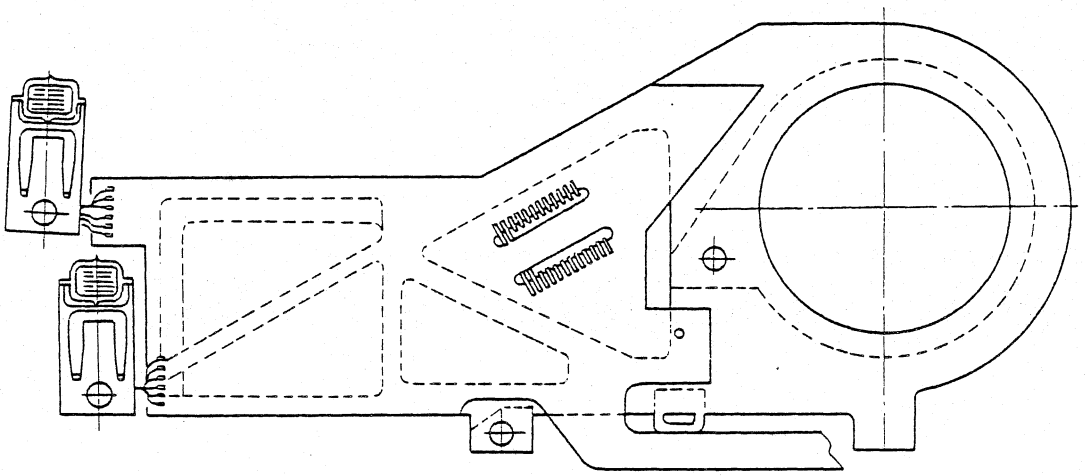


Figure 5.5-1 Moving Head Arm Assembly

There are two kinds of heads, i.e., moving head and fixed head. Both heads have a similar construction, but the moving head has only one Read/Write core whereas fixed head has four Read/Write cores, as shown in Figures 5.5-2 and 5.5-3 respectively. To increase the output voltage at high recording density, the core is made from Mn-Zn instead of Ni-Zn which is the commonly used material.

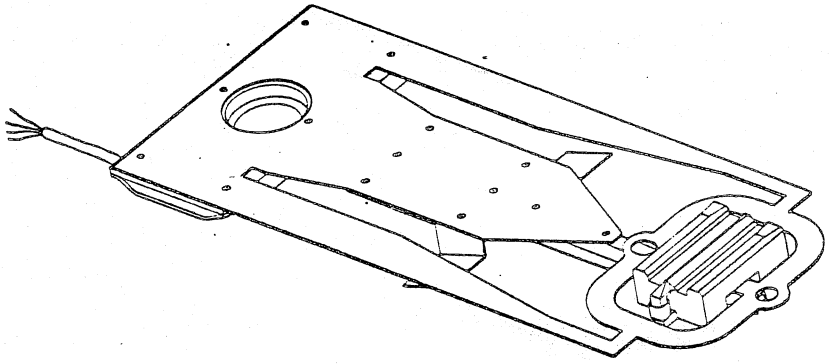


Figure 5.5-2 Moving Head

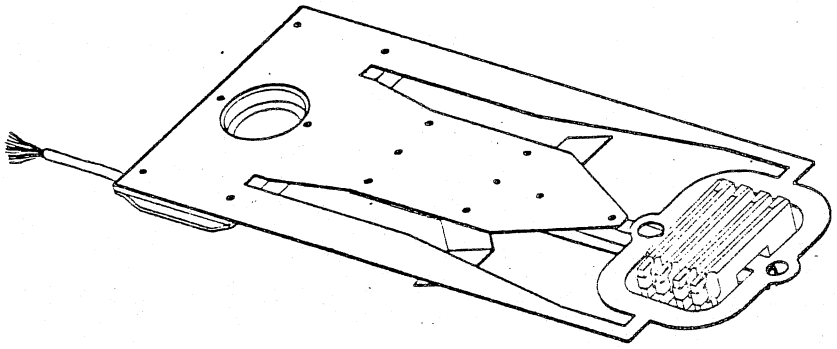


Figure 5.5-3 Fixed Head

(2) Disk

A magnetic disk has a diameter of 10.5 inches (268 mm) and is made of aluminum on which magnetic material is coated. Special coating is provided on the surface of this magnetic material in order to prevent wear caused by repeated contact-start/stop operations.

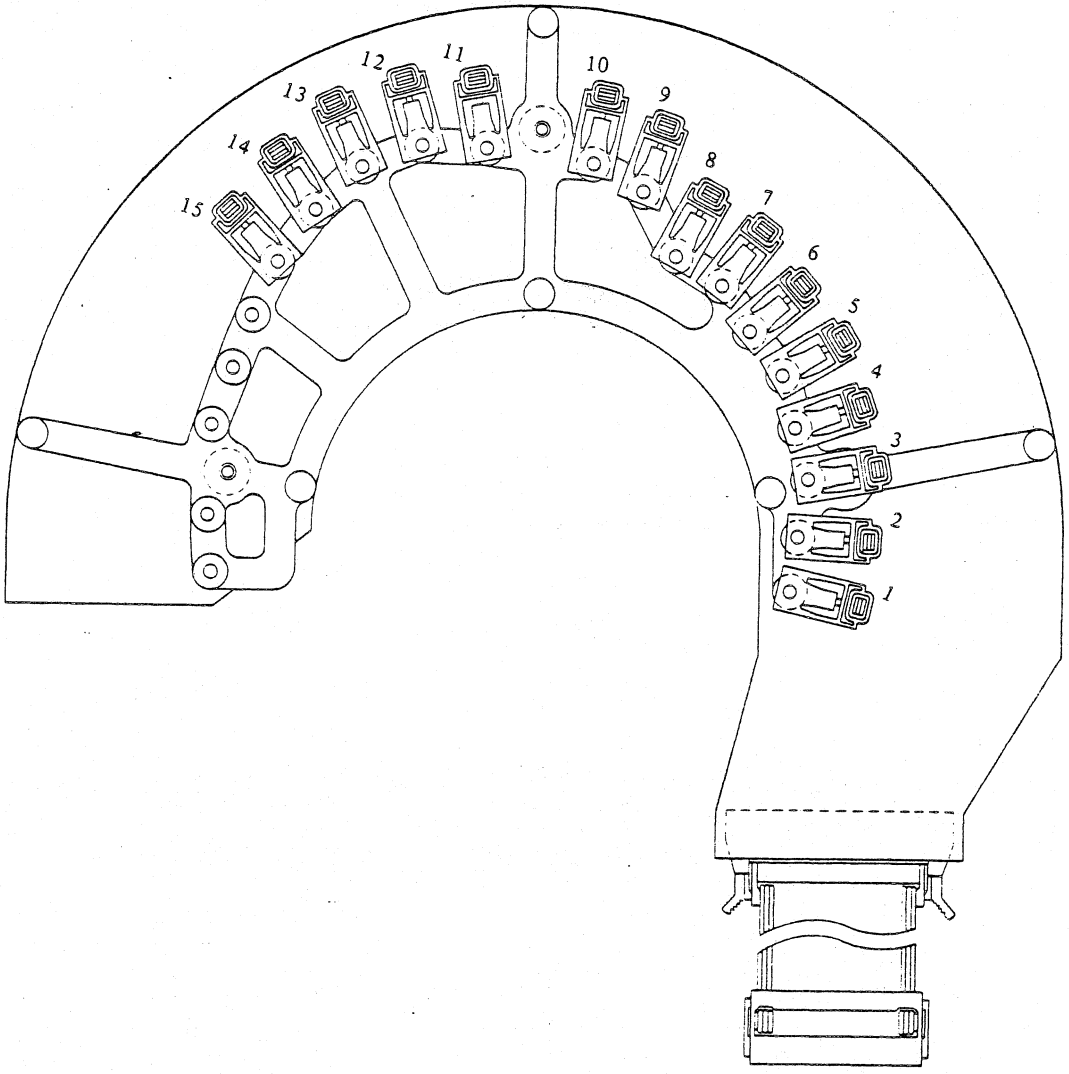
(3) Fixed Heads Block

Fixed heads are located at the top surface of the disks in the DE of M2351AF. Fifteen sliders having four cores each are attached to a fixed head block. Thus, there are 60 fixed head tracks in all, and are allocated to Cylinder 896 to 898 and Head 0 to 19 respectively.

A PCB with ICs (fifteen head pre-amplifiers and two decoders) is also attached to the block. Input and Output signals are transferred through a flat cable. The construction of the Fixed Head Block and address of each head are shown in Table 5.5-1 and Figure 5.5-4.

Table 5.5-1 Slider No. Vs. Cylinder/Head Address

Slider No.	Address		Slider No.	Address		Slider No.	Address	
	CYL	HD		CYL	HD		CYL	HD
1	897	08 ∿ 11	6	896	08 ∿ 11	11	898	00 ∿ 03
2	897	04 ∿ 07	7	896	12 ∿ 15	12	898	04 ∿ 07
3	897	00 ∿ 03	8	896	16 ∿ 19	13	898	08 ∿ 11
4	896	00 ∿ 03	9	897	12 ∿ 15	14	898	12 ∿ 15
5	896	04 ∿ 07	10	897	16 ∿ 19	15	898	16 ∿ 19



Numbers written in the firgure denote the slider numbers.

Figure 5.5-4 Fixed Head Block

5.6 COOLING SYSTEM

5.6.1 Cooling system of old version

The drive is cooled by a centralized cooling system using a line blower. The air is sucked in through the cooling hole of the front panel, passes through air filter, the line blower and the air duct, and is blown uniformly over the entire DE, card cage power amplifier, and interface PCBs. The air which passes over the card cage cools the DC power supply and the air which passes over the DE and the power amplifier cools interface PCBs, and is discharged.

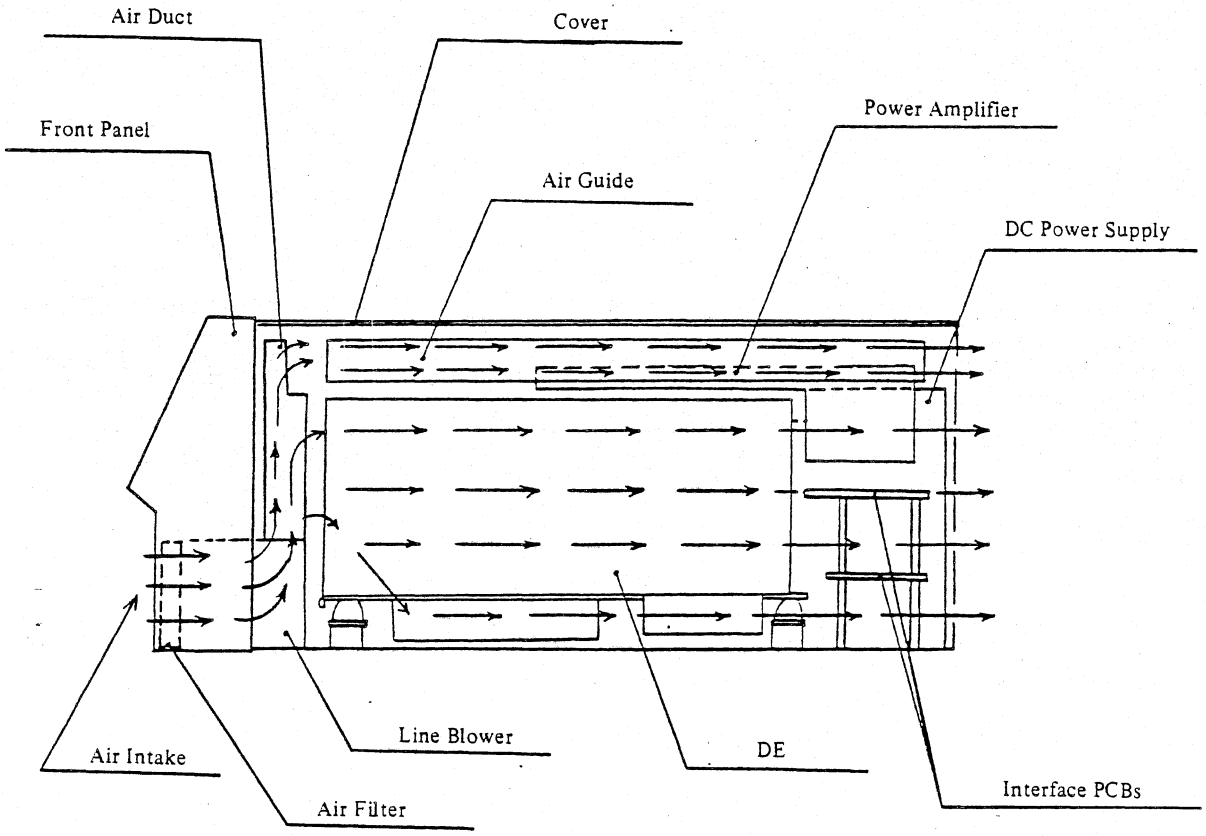


Figure 5.6-1 Air-Flow

5.6.2 Cooling system of new version

The drive is cooled by a centralized cooling system using a line blower. The air is sucked in through the colling slot of the front panel, passes through air filter, the line blower and Power amplifier, and is blown uniformly over the entire DE, card cage, and interface PCBs. The air which passes over the card cools the DC power supply and the air which passes over the DE cools interface PCBs, and is discharged.

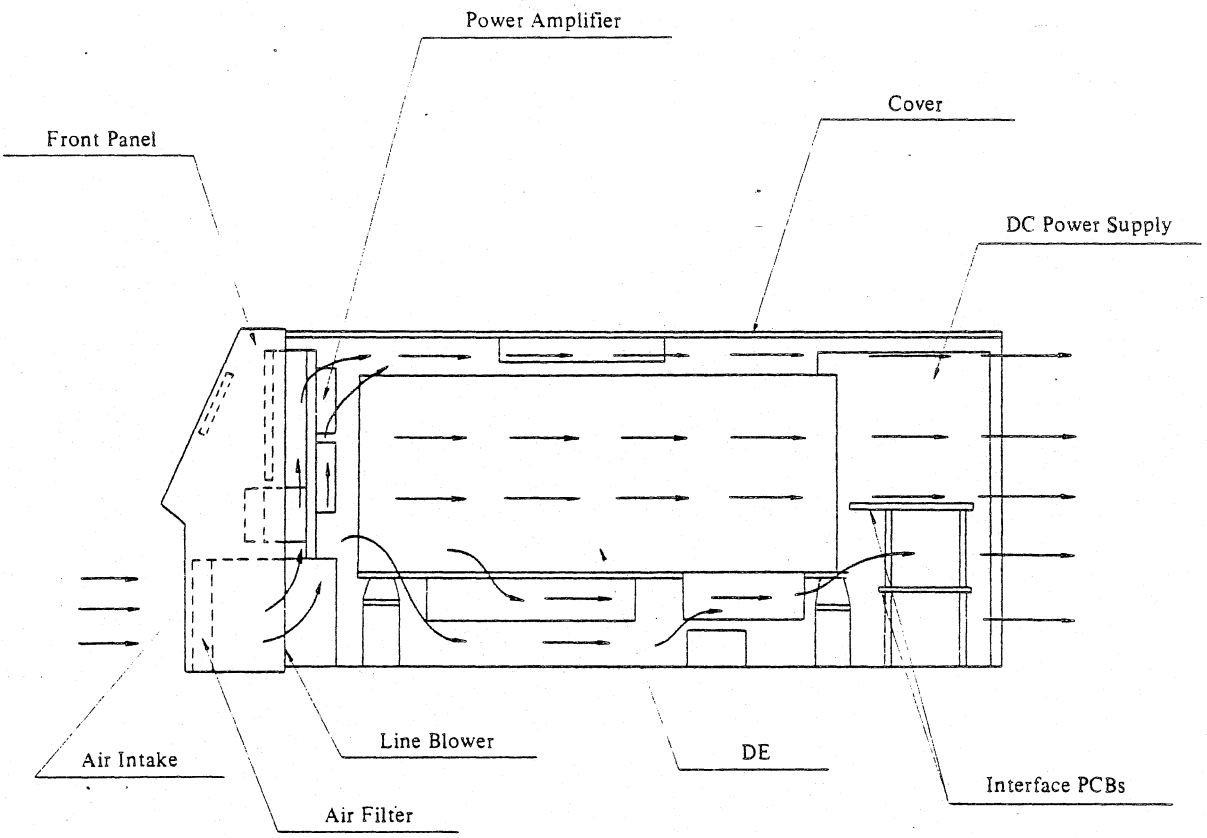


Figure 5.6-2 Air-Flow

5.7 ASSEMBLY DRAWINGS

The following drawings illustrate different levels of assembly in the disk drive. Each breakdown is followed by a corresponding table containing an Index No., Quantity, Composition (component parts of the larger assembly), Part Number and Description.

5.7.1 Old version (M2351A: ∿ #1898)

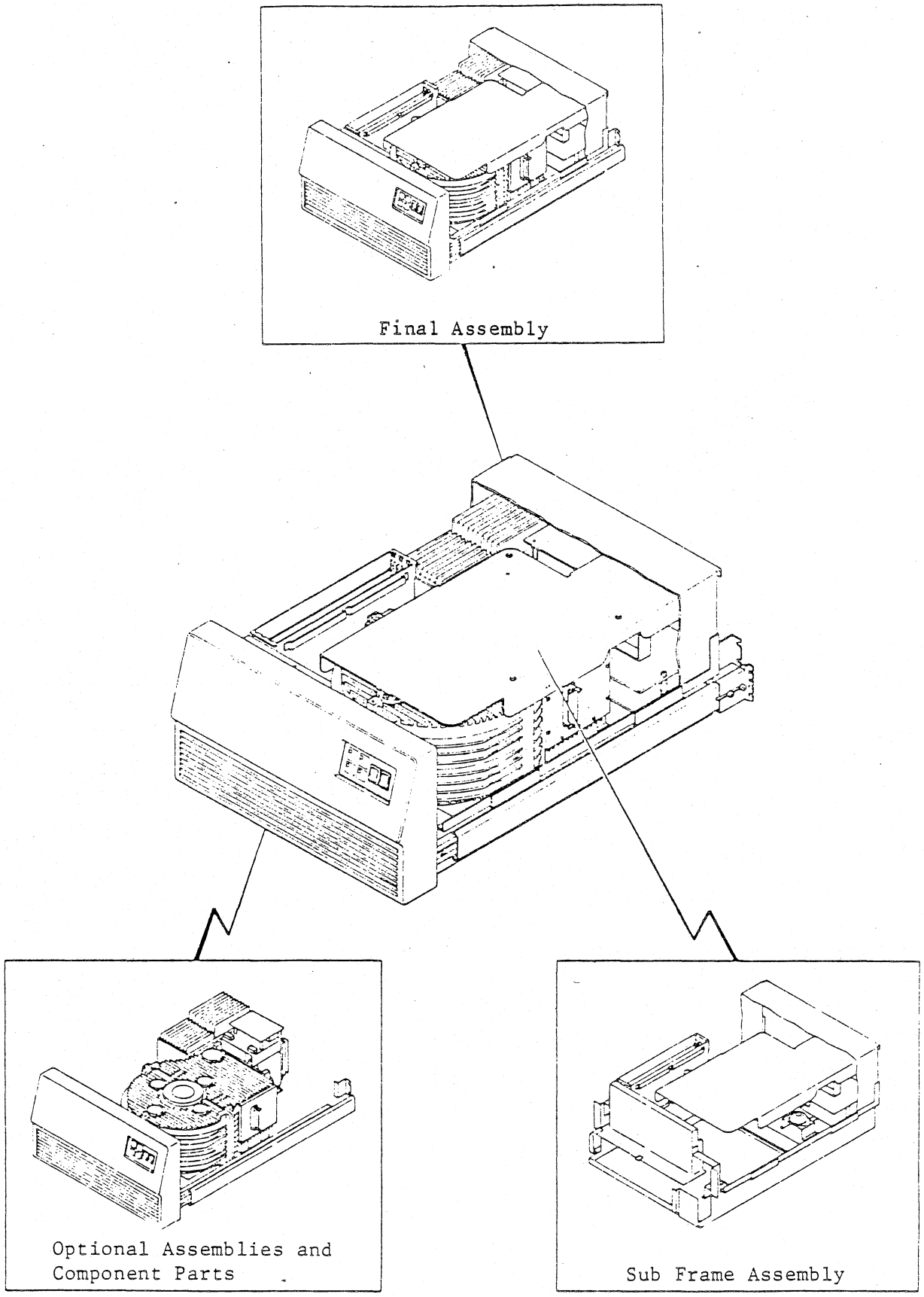


Figure 5.7-1 Visual Index Mini-Disk Drive

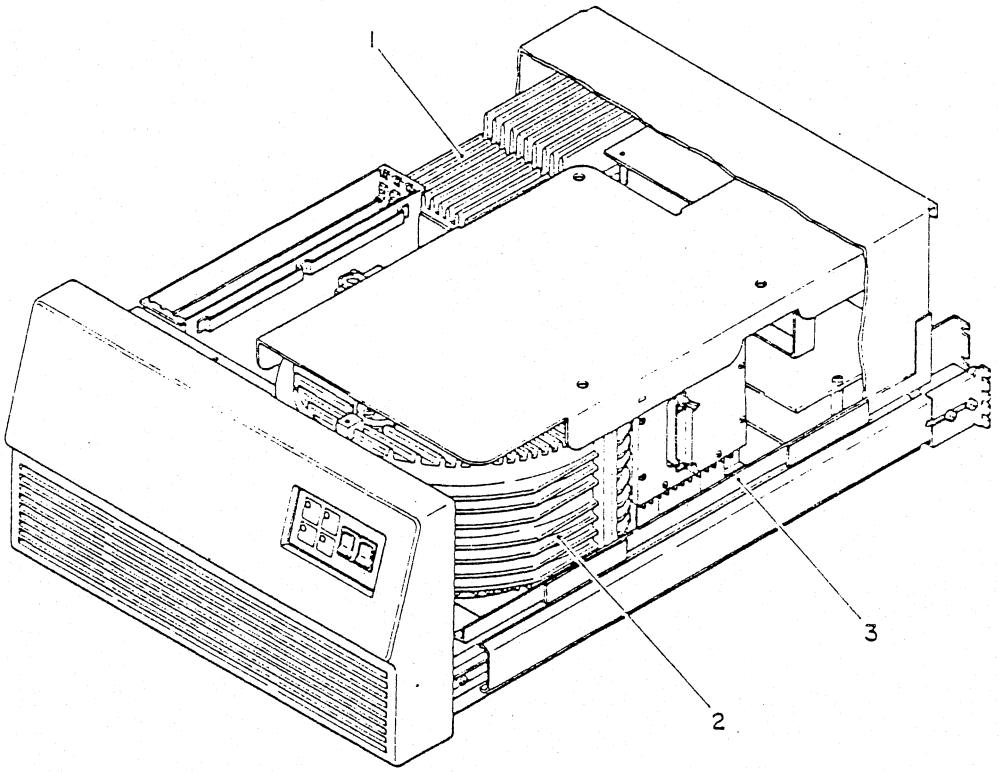


Figure 5.7-2

Table 5.7-1

Index No.	Composition & Quantity							Part Number	Description
	1							B03B-4655-B002A	M2351A Mini-Disk Drive
	1							B03B-4655-B003A	M2351AF Mini-Disk Drive
1		1						B14L-5105-0073A	DC Power Supply
2		1						B030-4610-T005A	DE Assembly (Non-Fixed Heads Type)
2		1						B030-4610-T006A	DE Assembly (Fixed Heads Type)
3		1						B210-1435-T001A	Sub-Frame Assembly

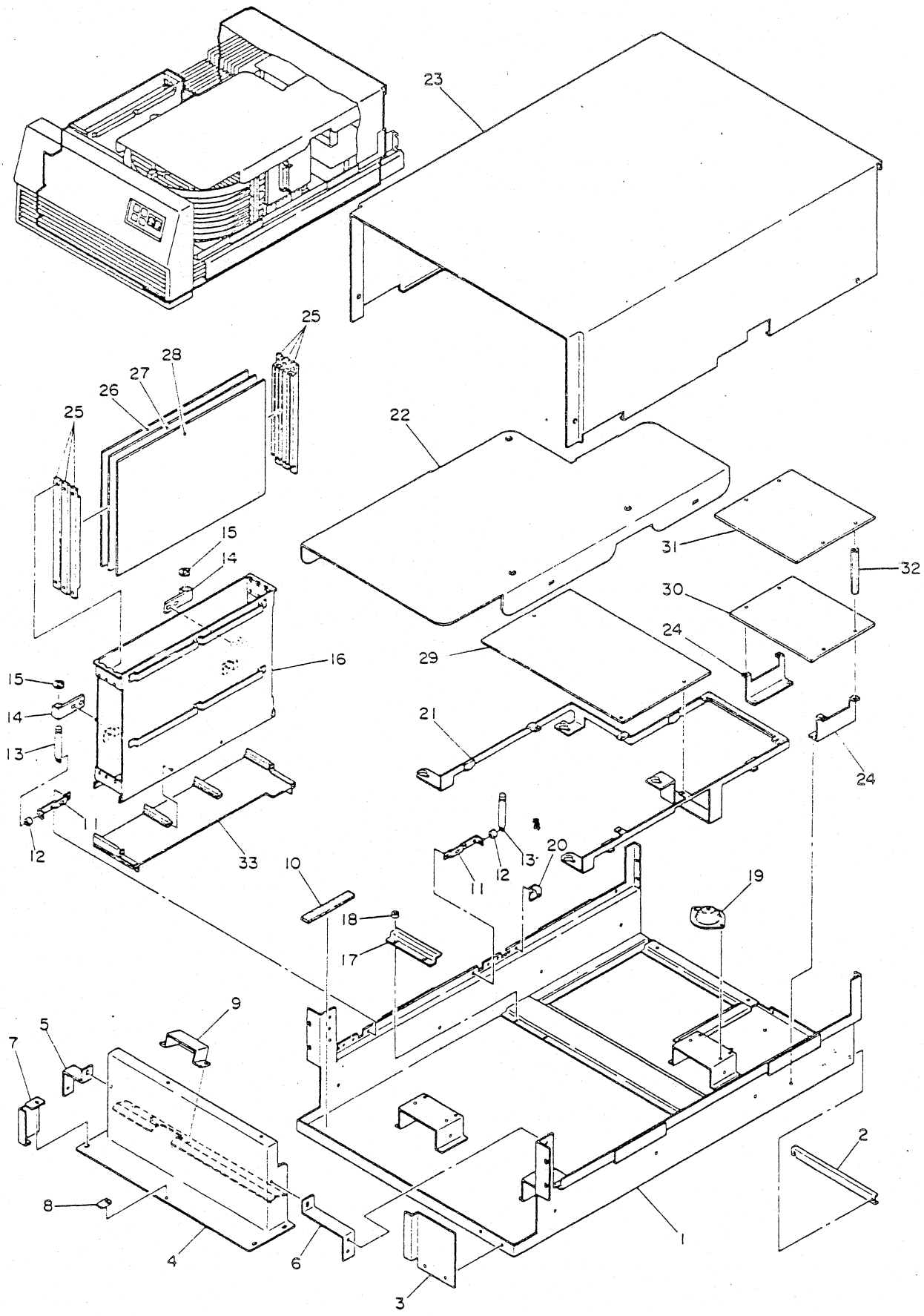


Figure 5.7-3 Sub-Frame Assembly

Table 5.7-2 Sub-Frame Assembly

Index No.	Composition & Quantity	Part Number	Description
	1	B210-1435-T001A	Sub-Frame Assy
1	1	B210-1435-W001A	Sub-Frame
2	1	B210-1435-X068A	Cable Pad
-	2	F6-SBD-4×16S-M-NI1A	Screw
3	1	B210-1435-X037A	Plate
-	2	F6-SSA-3×5S-M-NI1A	Screw
4	1	B210-1435-X017A	Duct
-	6	F6-SBD-4×6S-M-NI1A	Screw
5	1	B210-1435-X039A	Plate
6	1	B210-1435-X040A	Plate
-	4	F6-SSA-3×5S-M-NI1A	Screw
7	1	B210-1435-X070A	Guide
8	1	B210-1435-X071A	Plate
-	1	F6-SBD-4×6S-M-NI1A	Screw
9	1	B210-1435-X042A	Cover
-	2	F6-SBD-2.5×6S-M-NI1A	Screw
10	2	B210-1435-X018A	Rubber Plate
11	2	B210-1435-X056A	Plate
-	6	F6-SSA-3×6S-M-NI1A	Screw
12	2	B210-1435-X057A	Spacer
-	2	F6-SBD-4×16S-M-NI1A	Screw
-	2	F6-N1-4S	Nut
-	2	F6-SPK-4×4S	Spacer
13	2	B210-1435-X055A	Shaft
14	2	B210-1435-X058A	Bearing
-	4	F6-N1-4S	Nut
-	4	F6-WB-4S	Washer
-	4	F6-WM-4S	Washer
15	2	F6-ER-6	Retaining Ring
16	1	B210-1435-W045A	Gate Cover
-	2	F6-SBD-4×10S-M-NI1A	Screw
-	4	F6-SBD-4×6S-M-NI1A	Screw
17	1	B210-1435-X053A	Stopper

Table 5.7-2 - continued

Index No.	Composition & Quantity							Part Number	Description
18		1						B210-1435-X057A	Spacer
-		2						F6-SBD-4×6S-M-NI1A	Screw
19		3						B30L-1150-0003A	Dumper
-		6						F6-SBD-4×6S-M-NI1A	Screw
20		1						B210-1435-X054A	Plate
-		2						F6-SSA-3×6S-M-NI1A	Screw
21		1						B210-1435-W048A	Frame
22		1						B210-1435-X074A	Cover
23		1						B210-1435-X024A	Cover
24		2						B210-1435-X049A	Plate
-		4						F6-SSA-3×6S-M-NI1A	Screw
-		3						F6-BA-8×12-M-ZN1A	Bolt (for DE Assembly)
-		2						F6-SBD-4×6S-M-NI1A	Screw (for DC Power Supply)
-		8						F6-SBD-4×6S-M-NI1A	Screw (for Slide Guide)
25	6							C980-3010-X031	Card Guide
26	1							C16B-5510-0010#U	Servo Circuit
27	1							C16B-5123-0980#U	Logic Circuit
28	1							C16B-5500-0990#U	Read Amplifier
29	1							B16-8130-0010A#U	Power Amplifier
30	1							B16-8140-0010A#U	Interface Circuit
-	1							B03B-4655-0100A	Dual Channel (Option)
31		1						B16B-8150-0010A#U	Interface Circuit
32		4						F6-KKB1-3×70	Stud
33	1							B16B-8160-0010A#U	Back Panel

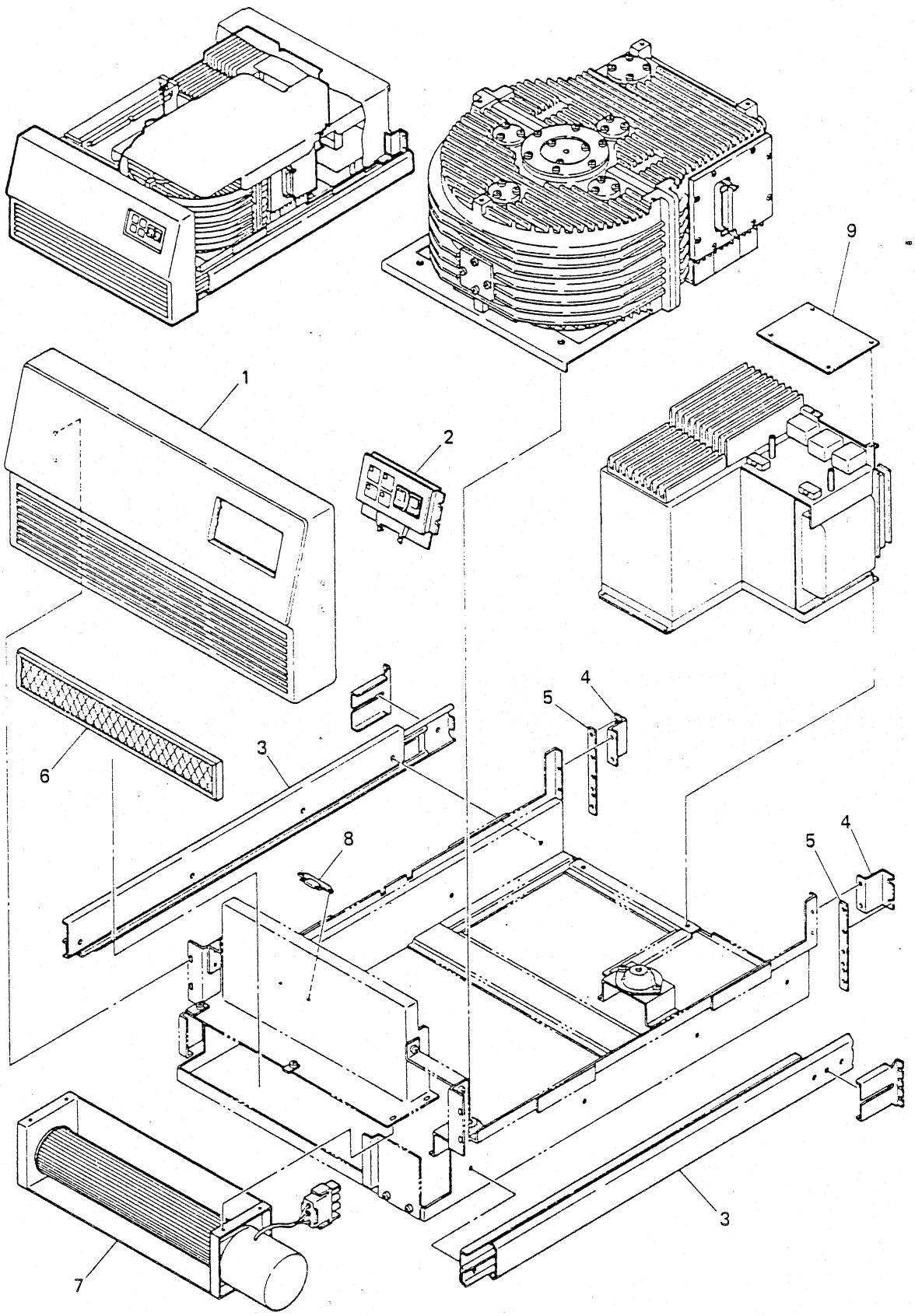


Figure 5.7-4 Optional Assemblies and Component Parts

Table 5.7-3 Optional Assemblies and Component Parts

Index No.	Composition & Quantity							Part Number	Description	
1	1							B210-1435-X012A	Front Panel	
2	1							N860-3346-T001	Operator Panel	
	1							B030-4655-V100A	Slide Guide	
3		1						B27L-0230-0010A	Slide Guide	(Option)
4		2						B210-1435-X902A	Metal Fitting	
5		4						B210-1435-X903A	Plate	
-		20						F6-SW2NA-5×10S	Screw with Washer	
6	1							B90L-0400-0303A	Air Filter	
7	1							B90L-1200-0101A	Line Blower	
8	1							B57L-0040-0003A	Fan Alarm	
9	1							B16B-7830-0010A#U	Indicator Unit	

5.7.2 NEW VERSION (M2351A: #1899~, M2351AF: #1~)

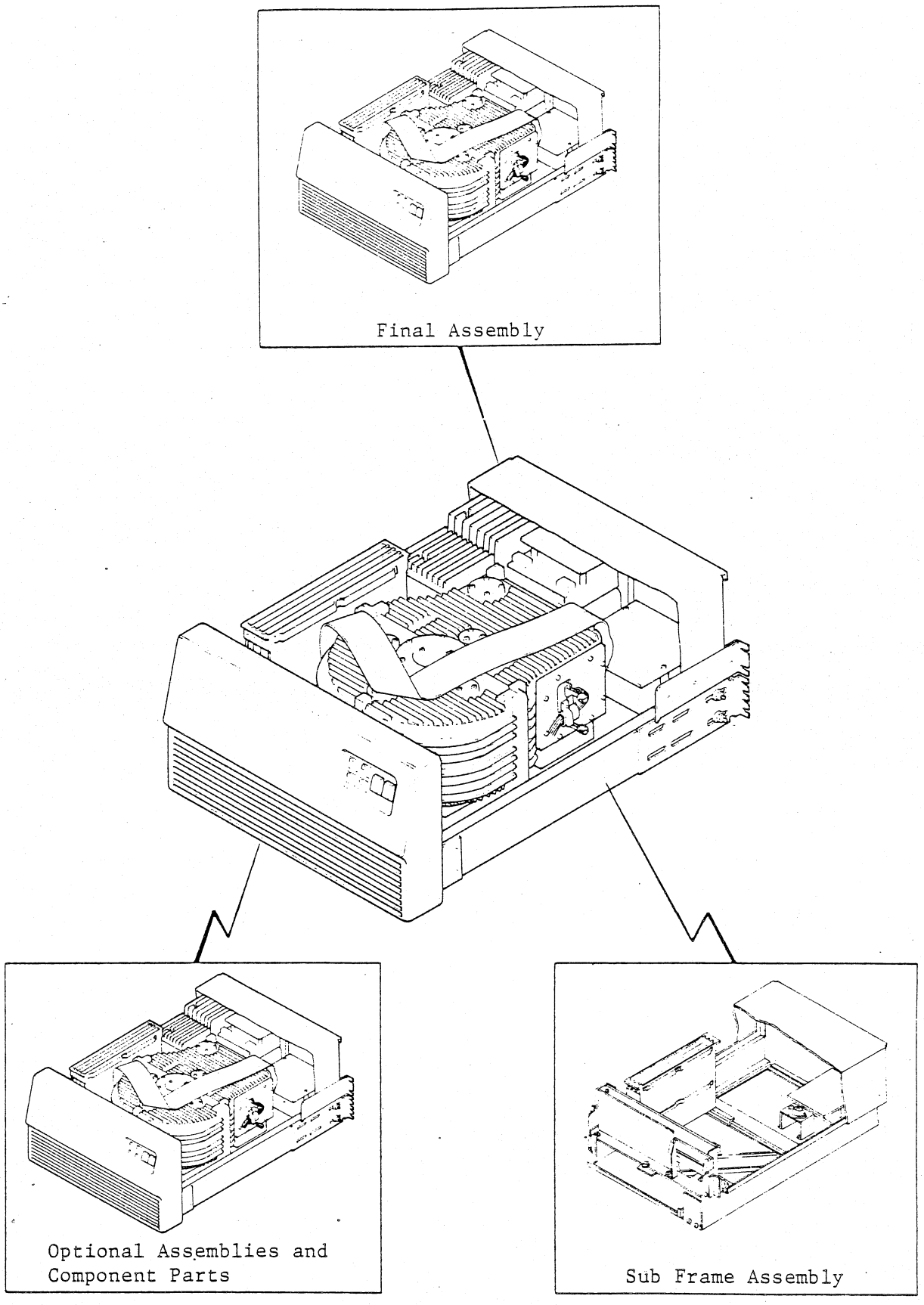


Figure 5.7-5 Visual Index Mini-Disk Drive

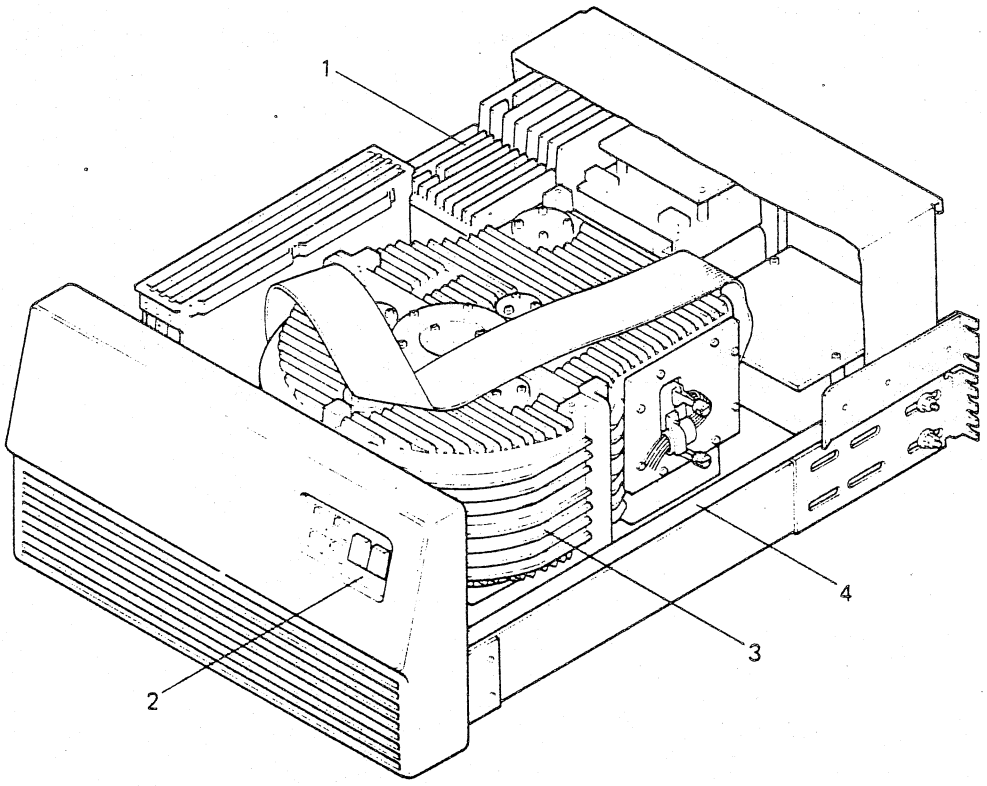


Figure 5.7

Table 5.7-4

Index No.	Composition & Quantity							Specifications	Description
	1							B03B-4655-B002A	M2351A Mini-Disk Drive
	1							B03B-4655-B003A	M2351AF Mini-Disk Drive
1		1						B14L-5105-0073A	DC Power Supply
2		1						B030-4610-T007A	DE Assembly (Non-Fixed Heads Type)
2		1						B030-4610-T008A	DE Assembly (Fixed Heads Type)
3		1						B210-1435-T002A	Sub-Frame Assembly

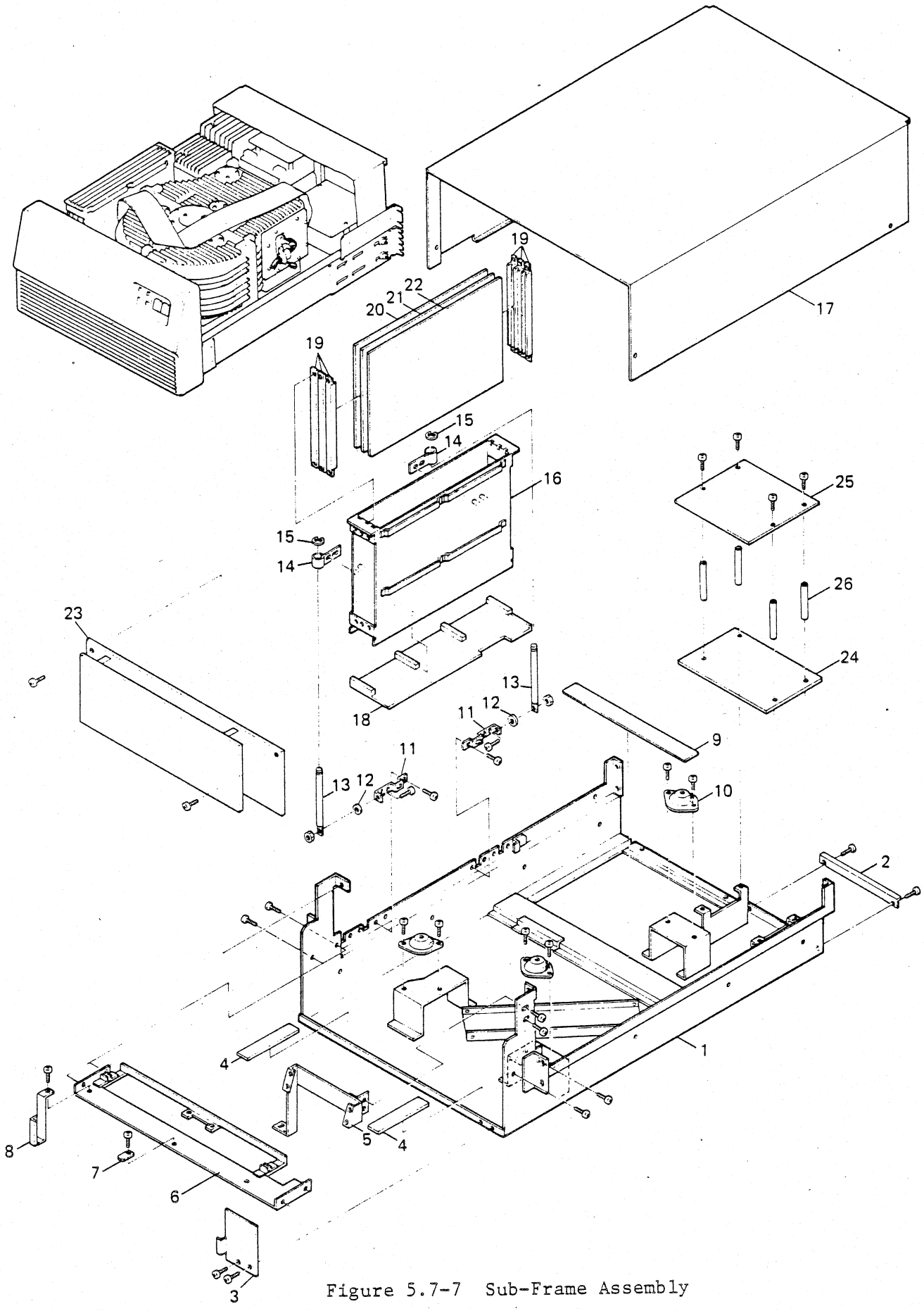


Figure 5.7-7 Sub-Frame Assembly

Table 5.7-5 Sub-Frame Assembly

Index No.	Composition & Quantity							Specifications	Description
	1							B210-1435-T002A	Sub-Frame Unit
1		1						B210-1435-W101A	Sub-Frame Assy
2		1						B210-1435-X068A	Cable Pad
-		2						F6-SW2NA-4×20S	Screw
3		1						B210-1435-X912A	Guide (right side)
-		2						F6-SSA-3×5S-M-NI1A	Screw
4		2						B210-1435-X112A	Rubber Plate
5		1						B210-1435-W115A	Bracket
-		4						F6-SW2NA-4×8S	Screw
6		1						B210-1435-W110A	Plate
-		4						F6-SSA-3×6S-M-NI1A	Screw
7		1						B210-1435-X071A	Plate
-		1						F6-SW2NA-4×8S	Screw
8		1						B210-1435-X911A	Guide (left side)
-		1						F6-SW2NA-4×8S	Screw
9		1						B210-1435-X122A	Packing
10		3						B30L-1150-0003A	Dumper
		1						B210-1435-W055A	Hinge Assy (left side)
		1						B210-1435-W056A	Hinge Assy (right side)
11			1					B210-1435-X056A	Plate
12			1					B210-1435-X057A	Spacer
-			1					F6-SBD-4×16S-M-NI1A	Screw
-			1					F6-N1-4S	Nut
-			1					F6-SPK-4×4S	Spacer
13			1					B210-1435-X055A	Shaft
14			1					B210-1435-X058A	Plate
15			1					F6-ER-6	Retaining Ring
16		1						B210-1435-W045A	Gate Cover
-		4						F6-N1-4S	Nut
-		4						F6-WB-4S	Washer
-		4						F6-WM-4S	Washer

Table 5.7-5 - continued

Index No.	Composition & Quantity							Specifications	Description
17		1						B210-1435-W120A	Cover
-		2						F6-SSA-3×6S-M-NI1A	Screw
-		2						F6-SW2NA-4×8S	Screw
18	1							B16B-8160-0010A#U	Back Panel PCB (BQGMU)
19	6							C980-3010-X031	Card Guide
20	1							C16B-5501-0010#U	Servo PCB (SVIAU)
21	1							C16B-5123-0980#U	Logic PCB (512398U)
22	1							C16B-5500-0990#U	R/W PCB (RFJAU)
23	1							B16B-8800-0010A#U	Power Amplifier PCB (TVKMU)
24	1							B16B-8140-0010A#U	Interface PCB (DQEMU)
	1							B03B-4655-0100A	Dual Channel Option
25		1						B16B-8150-0010A#U	Interface PCB (DQFMU)
26		4						F6-KKB1-3×70	Stud

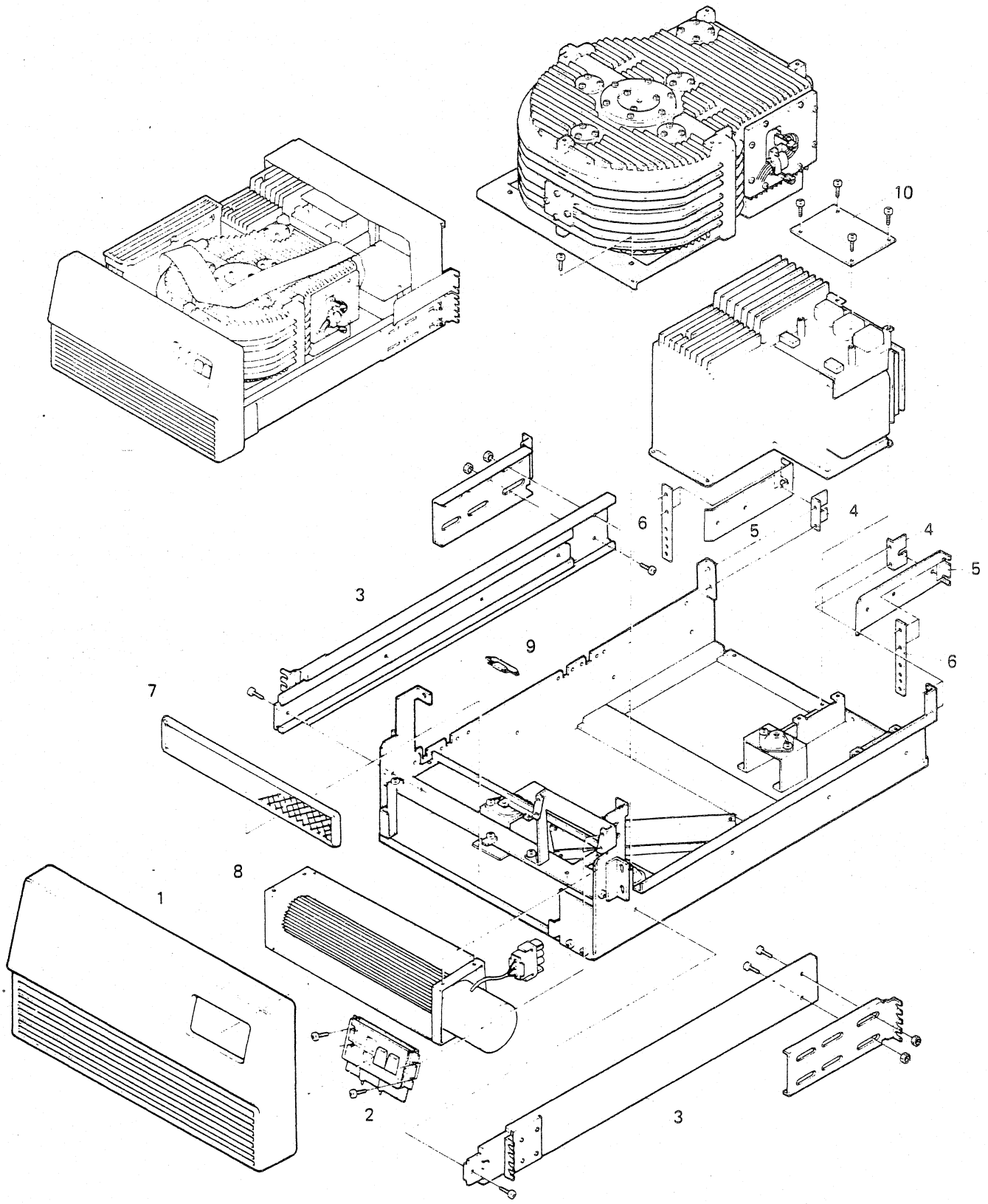


Figure 5.7-8 Optional Assemblies and Component Parts

Table 5.7-8 Optional Assemblies and Component Parts

Index No.	Composition & Quantity							Specifications	Description	
1	1							B210-1435-X012A	Front Panel	
2	1							N860-3346-T001	Operator Panel	
	1							B030-4655-V100A	Slide Guide Assy	
3		1						B27L-0230-0010A	Slide Guide	(Option)
4		2						B210-1435-X908A	Metal Fitting	
5		2						B210-1435-X909A	Guide Plate	
6		4						B210-1435-X903A	Plate	
-		20						F6-SW2NA-5×10S	Screw	
7	1							B90L-0400-0303A	Air Filter	
8	1							B90L-1200-0101A	Line Blower	
9	1							B57L-0040-0003A	Fan Alarm	
10	1							B16B-7830-0010A#U	Indicator PCB (HGAMU)	

CHAPTER 6 DATA FORMAT

The M2351A/AF can be used with two different formats, i.e., variable Sector Format and Fixed Sector Format, as determined by the controller. The former contains a 3-Byte DC erased area called the Address Mark (AM) prior to each Address Area (AA) indicating the beginning of a record. Therefore, Data Area (DA) with different lengths in a track can be written or read. On the other hand, record length is fixed in the Fixed Sector Format.

6.1 FORMAT

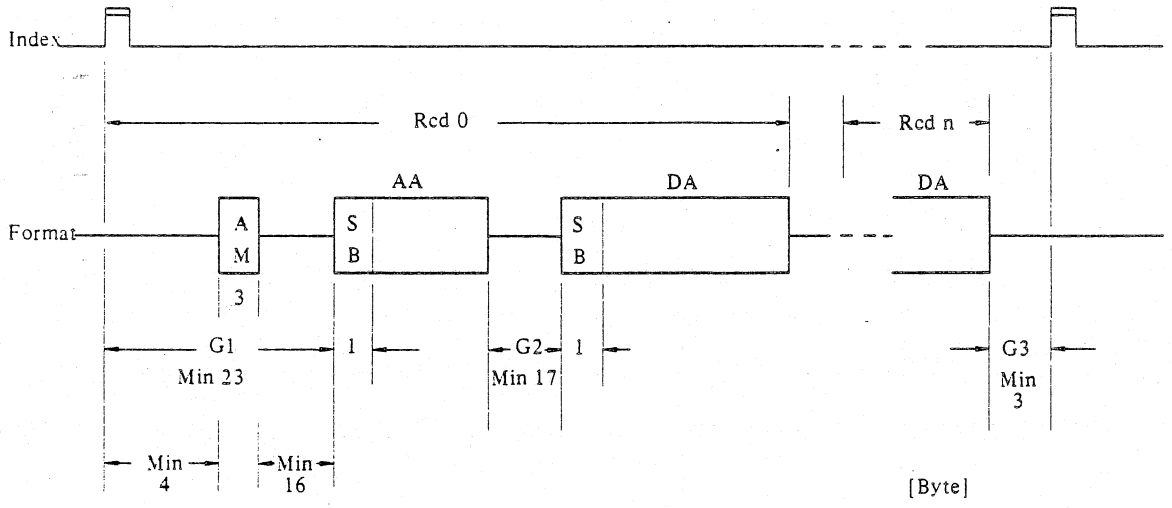


Figure 6.1-1 Variable Sector Format

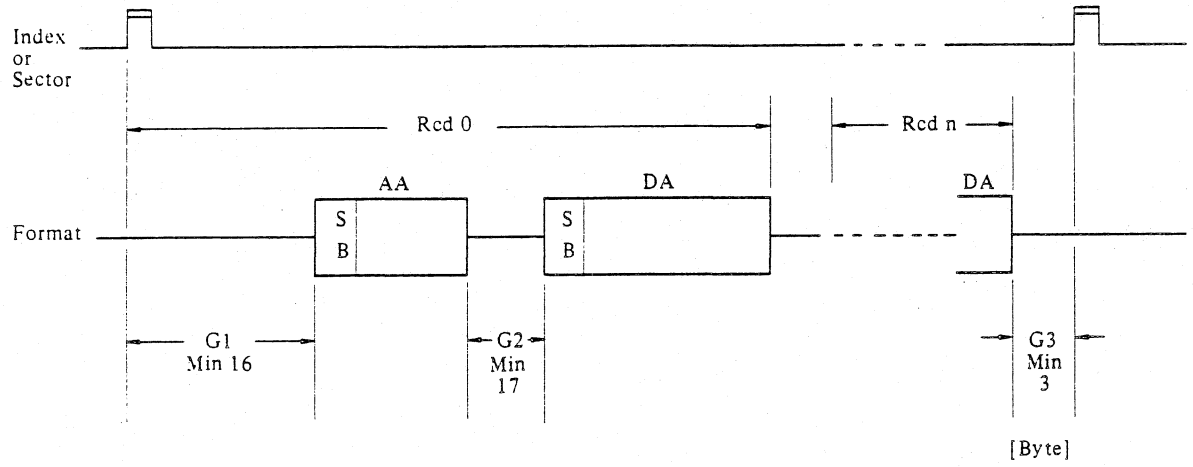


Figure 6.1-2 Fixed Sector Format

Description of Format Parameters

-G1, G2, G3 (Gap 1, 2 and 3)

Gaps between adjacent areas. They should be filled with all "0" s.

-SB (Sync Byte Pattern)

Indicates the beginning of Address or Data Area.

The pattern for both area can be varied but the recommended pattern is $(19)_{16}$ or $(0E)_{16}$.

-AA (Address Area)

The Address Area should contain the following information;

- Flag Byte which indicate various conditions of the track or sector, i.e., Primary/Alternate track/Sector, Good/Bad track/Sector
- Logical Drive Address
- Cylinder Address
- Head Address
- Sector Address or Record Number
- CRC to check whether the data has been read correctly or ECC to correct the data when a data error has been detected.

-DA (Data Area)

The area where the data should be recorded. CRC or ECC should be added.

6.2 TRACK EFFICIENCY

Table 6.2-1 shows examples of calculated results of track efficiency in Variable and Fixed Sector Formats. The following assumptions are made for this calculation.

- The length of Address Area including the SB is 8 Bytes.
- All gap lengths used are the shortest in Figures 6.1-1 and 6.1-2.
- The length of the data area is determined using the formula.

$$\text{Data Area} = \text{SB} + \text{DL (Data Length)} + \text{CRC}$$
$$= 1 + \text{DL} + 2 = \text{DL} + 3 \text{ (Bytes)}$$

- $\text{Efficiency} = \dfrac{\text{DL} \times \text{(Sector/Track)}}{28{,}160 \text{ (Bytes/Track)}} \times 100 \quad (\%)$

Table 6.2-1 Track Efficiency

	DL(B)	256	512	1,024	2,048
Variable Sector Format	Sector/Track	90	49	26	13
	Efficiency (%)	81.8	89.0	94.5	94.5
Fixed Sector Format	Sector/Track	92	50	26	13
	Efficiency (%)	83.6	90.9	94.5	94.5

6.3 MEDIA SPECIFICATIONS

The quality of all tracks are checked, and location and length of media flaws which may affect the reliability of stored data are recorded in the Header Areas of all tracks before the shipment of a drive from the factory. Therefore, by using techniques such as sector/track deallocation or skip displacement, valid data must not be written over known media flaws.

(1) Definition of Track Quality

Every track is classified into three grades dependent on number of defects on a track. They are:

Perfect track : A track containing no defects

Good track : A track containing one defect

Defective track: A track containing two or more defects, or a track containing flaws which may contribute to missing AM or false AM. If the track is defective, the high order bit of the first cylinder byte in the Header Area is set to one.

Here, defect is defined as media flaws grouped by the maximum flaw length of 64 bytes. 65 bytes of media flaws are treated as two defects, as an example.

(2) Quality Standards of Media at Shipment

- The number of defects per DE$\leq$500
- The number of defective tracks per DE$\leq$30
- Head 0 and 1 at cylinder 0 are perfect tracks
- There is at least one perfect track and no defective tracks at cylinder 841
- All tracks in fixed-heads area are not defective
- If there is a defect in the region of bytes 14-55 after the index mark, there is no defect in the region of bytes 69-164.
- If there is a defect in the region of bytes 56-104 after the index mark, there is no defect in the region of bytes 14-55 and 116-164.

A DE which does not meet these standards is rejected at its shipment.

(3) Header Format

The Header format is divided into two parts. The first part of the format is a Fixed Sector Format, and the second part is a Variable Sector Format. The Fixed Sector Format information is normally included in the first 56 bytes following the index mark. The Variable Sector Format information consists of 49 bytes and normally follows the Fixed Sector information.

Following are rules for the defect recording:

- The position of a defect is listed in bytes (Hex.) after the index mark, +/- 1 byte.
- The length of a defect is in bits (Hex.) +/- 1 bit.
- Unused defect locations are all zeros.
- Every track is recorded with this defect format whether defects exist or not.
- More than one defect on a track causes the track to be flagged as a defective track. The first four media defects on the track are logged.

Figure 6.3-1 shows the format when there are no defects in the first 105 bytes after the index mark.

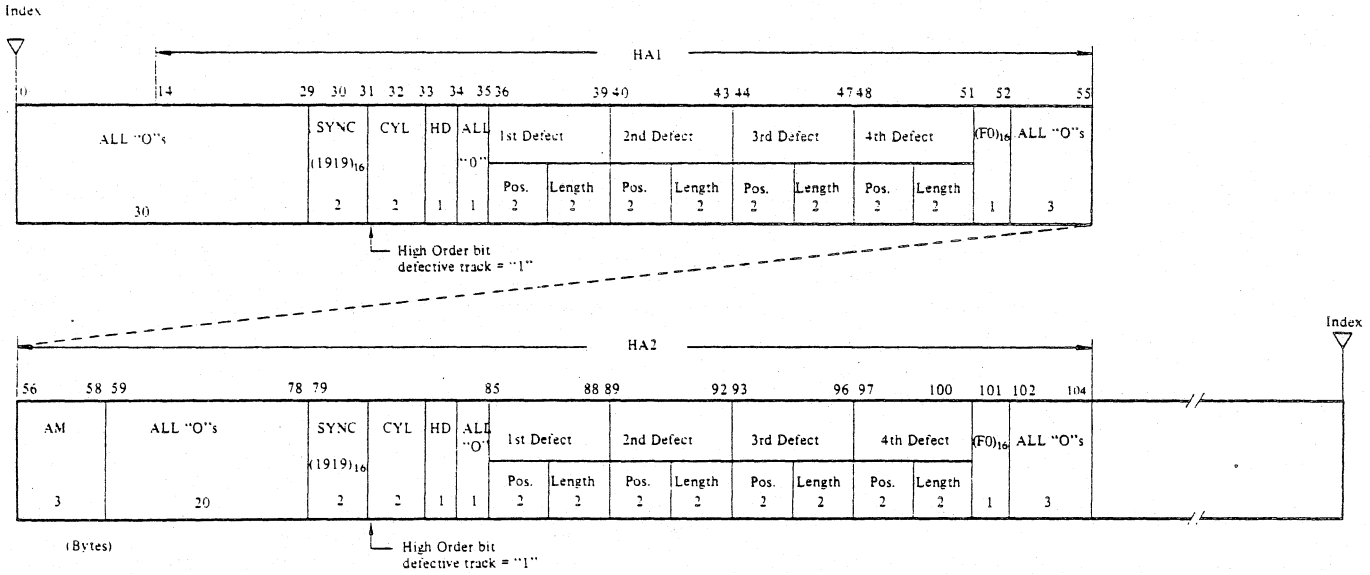


Figure 6.3-1 Format 1

If the beginning of a defect is located in the region of bytes 14 - 55, 60 bytes of zeros are added to Gap 1. Figure 6.3-2 shows an example of this format.

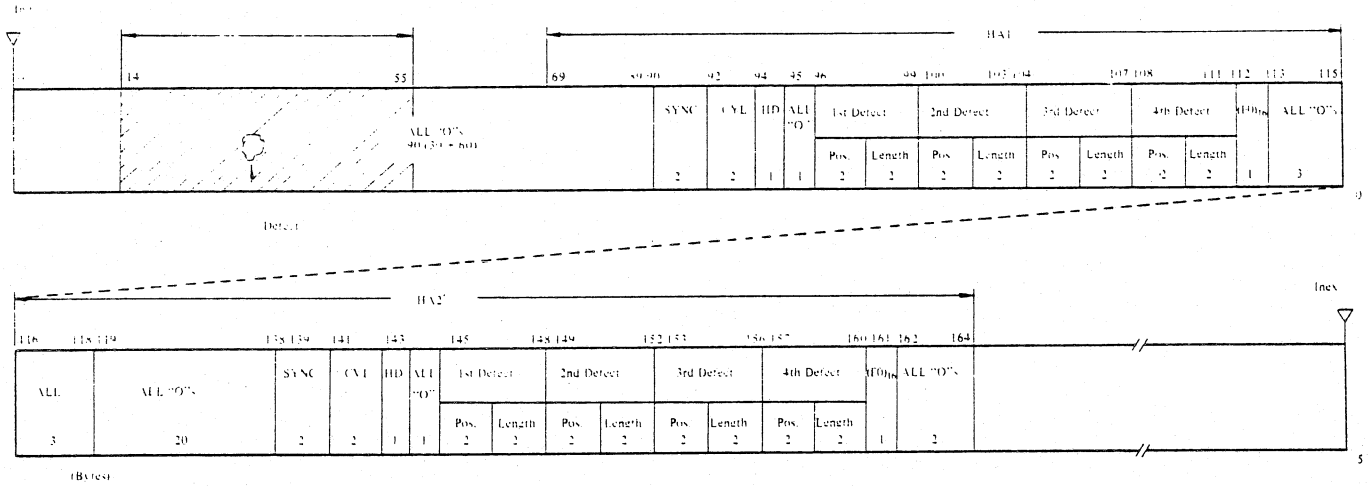


Figure 6.3-2 Format 2

If a defect is located in the region of bytes 56 - 104, the gap before the address mark is increased to 60 bytes. Figure 6.3-3 shows an example of this format.

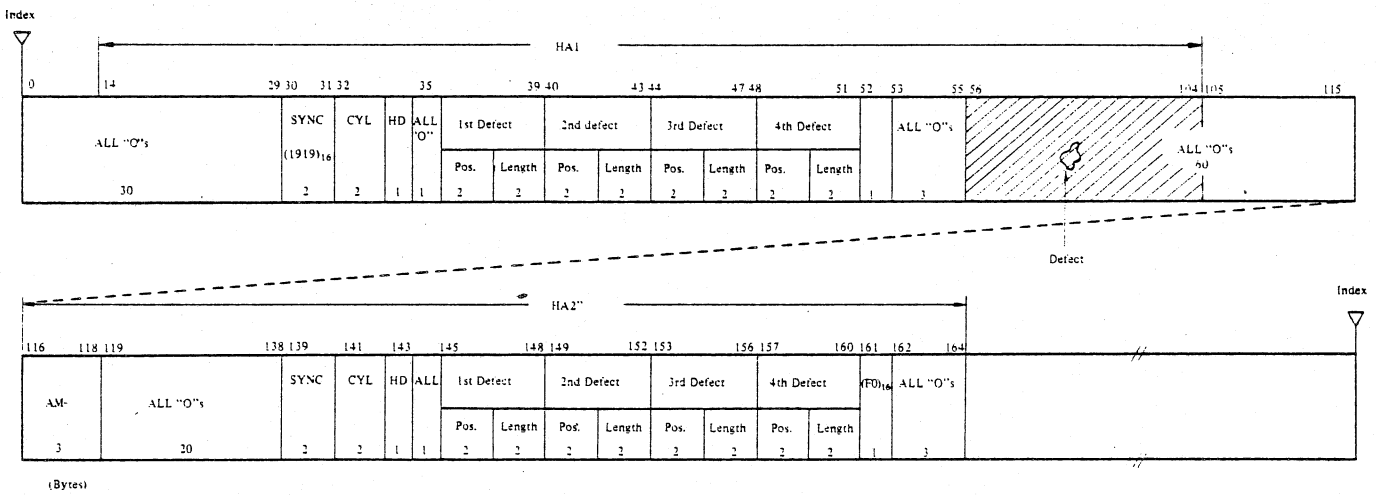


Figure 6.3-3 Format 3

In Figure 6.3-2 and 6.3-3, it is guaranteed that there are no defects in the regions where HA1 and HA2 are newly relocated due to a defect.

(4) Inspection Data Sheet

The location and length of media flaws are recorded in Header Areas as described in (3), as well as printed out on a sheet which is attached to each drive.

The contents of this sheet are listed below.

- Date (Year: Month: Day)
- Drive type (M2351A/M2351AF)
- Serial number of drive
- DE type (Non-fixed/Fixed head type)
- Serial number of DE
- Information about flaws
  - Cylinder address
  - Head address
  - Location of flaws in bytes after index mark
  - Length of flaws in bits
- Defective track address (Cylinder/Head address)
- Every perfect head address at cylinder 841

CHAPTER 7 INTERFACE

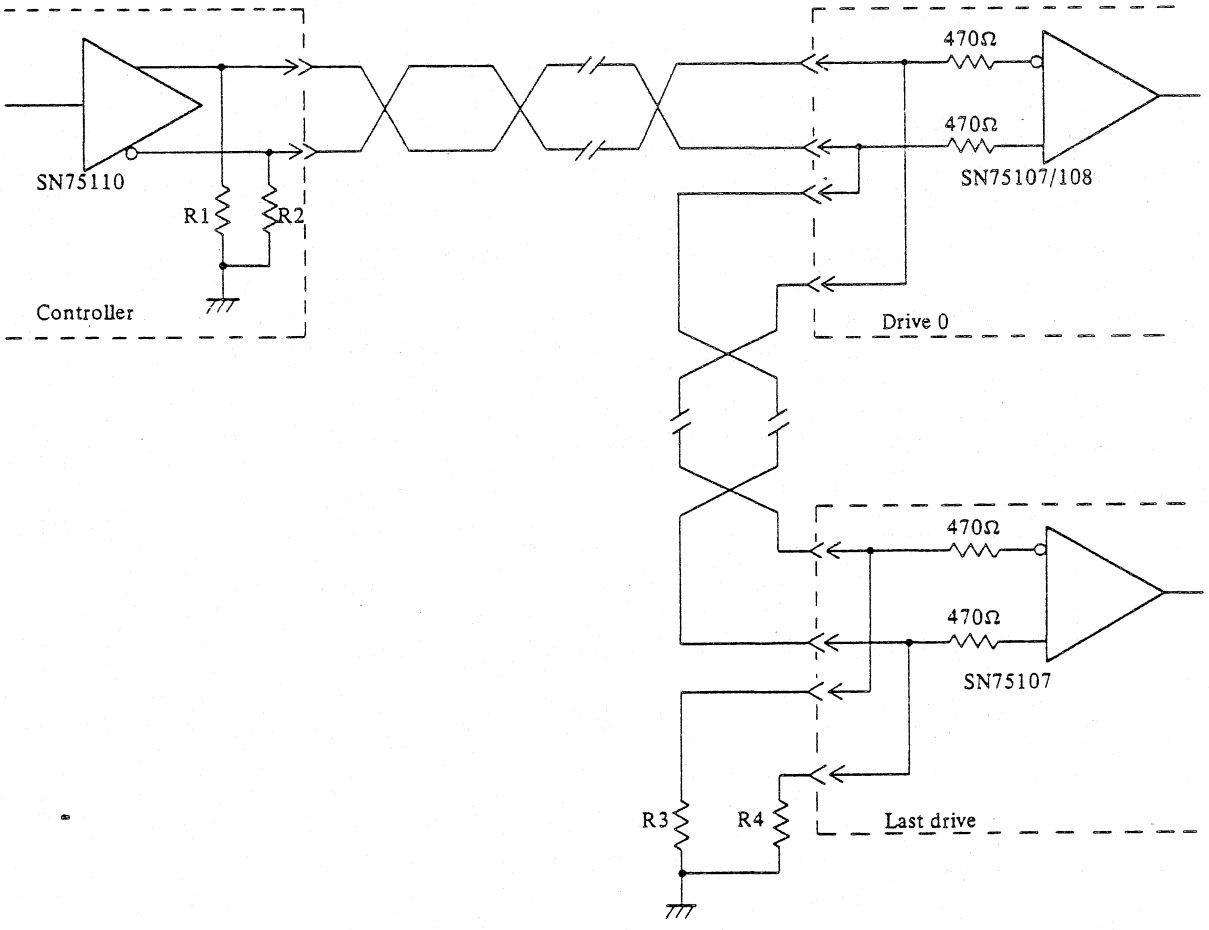
This chapter describes the physical and logical specifications of interface signals between the M2351A/AF and any controller.

7.1 SIGNAL TRANSMISSION DRIVER/RECEIVER

SN75110 Drivers and SN75107/108 Receivers are used to provide a terminated and balanced transmission system.

(1) A-Cable

All signals except Open Cable Detect and Power Sequence Pick/Hold signals must be terminated both in the drive and the controller as shown in Figure 7.1-1.



Note; (1) Line terminators are located in the drive and the controller. R1 to R4; 56 Ohms±10%.1/10W.
(2) The maximum cable length is 100 FT (30 m).

Fig. 7.1-1 Balanced Transmission of A-Cable

For the Open Cable Detect signal, two drivers of SN75110 would be required in parallel without termination to increase the drive current in the interface cable as shown in Figure 7.1-2.

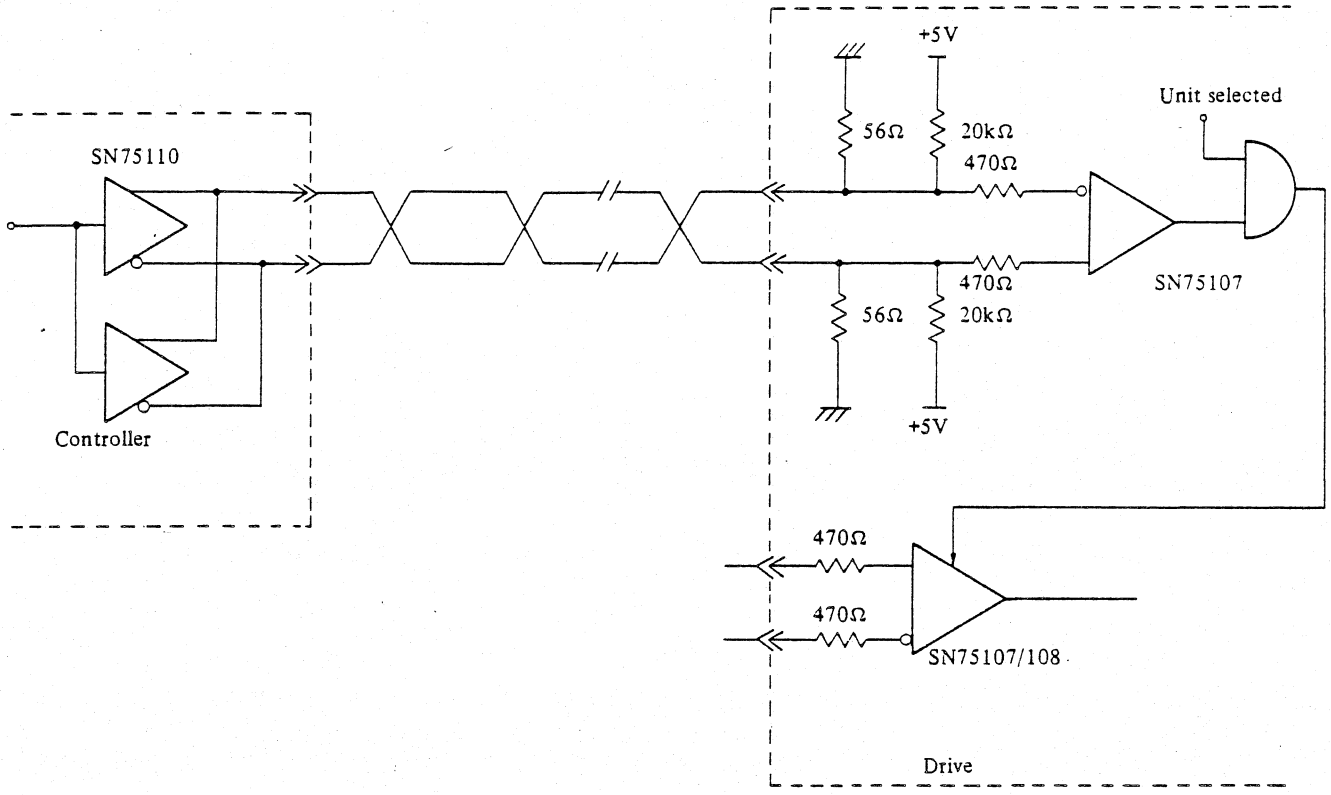


Fig. 7.1-2 Open Cable Detect

Power Sequence Pick and Hold must be set to ground in the controller.

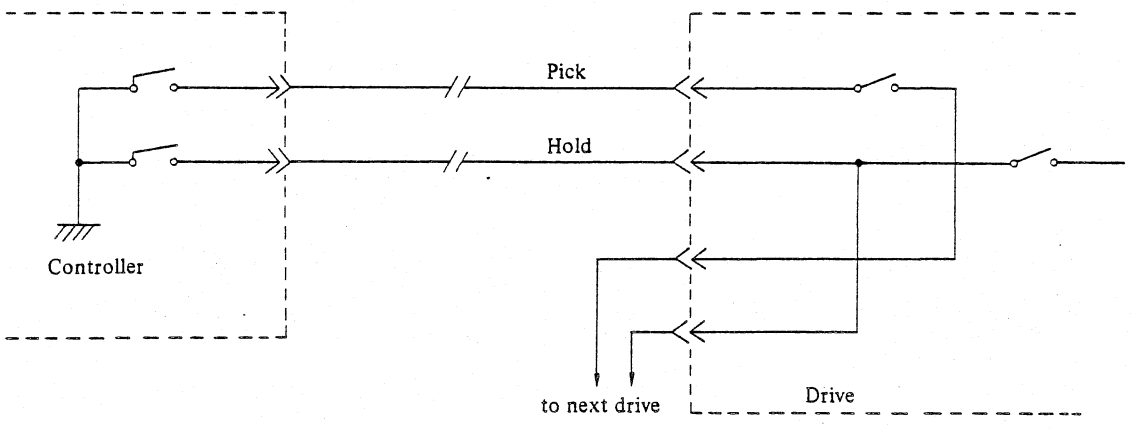
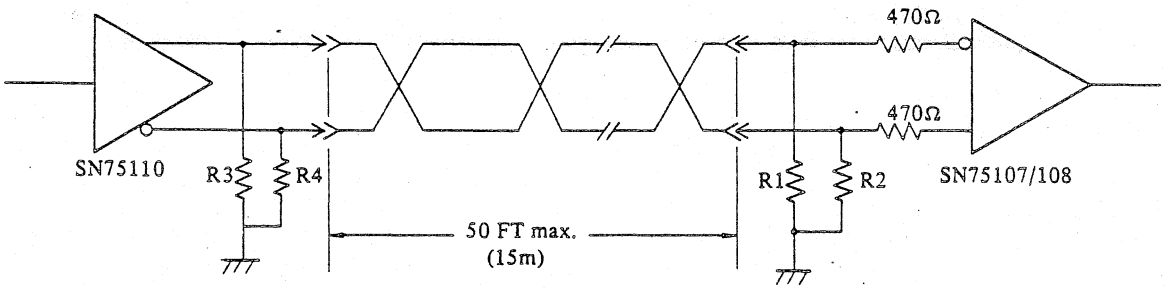


Fig. 7.1-3 Power Sequence Pick/Hold

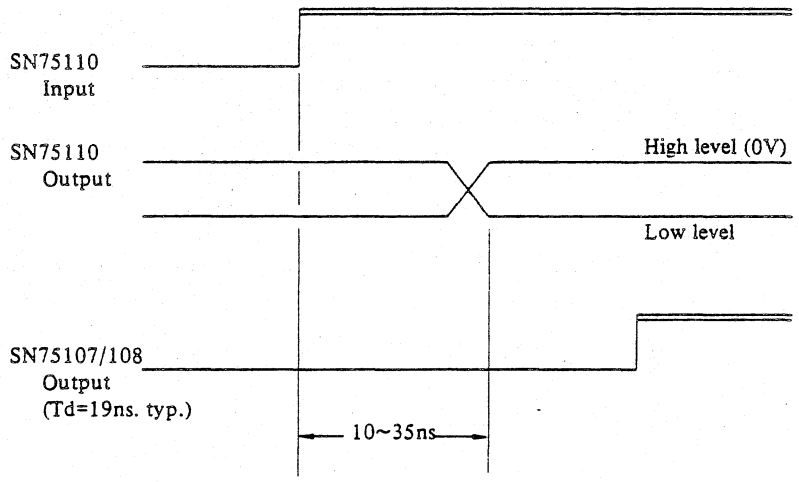
(2) B-Cable



Note; (1) Line terminators are located in the drive and the controller.
R1 to R4; 82 Ohms±5%, 1/10W.

Fig. 7.1-4 Balanced Transmission of B-Cable

(3) Input/Output Characteristics of Driver/Receiver



Typical output level of SN75110

	A-cable	B-cable
High level	0V	
Low level	−0.33V	−0.49V

Fig. 7.1-5 Input/Output Characteristics

		Low	High	
CONTROLLER	UNIT SELECT TAG	52	22	DRIVE
	UNIT SELECT 1	53	23	
	UNIT SELECT 2	54	24	
	UNIT SELECT 4	56	26	
	TAG 1	31	1	
	TAG 2	32	2	
	TAG 3	33	3	
	TAG 4	60	30	
	TAG 5	57	27	
	BUS 0	34	4	
	BUS 1	35	5	
	BUS 2	36	6	
	BUS 3	37	7	
	BUS 4	38	8	
	BUS 5	39	9	
	BUS 6	40	10	
	BUS 7	41	11	
	BUS 8	42	12	
	BUS 9	43	13	
	STATUS 0	49	19	
	STATUS 1	47	17	
	STATUS 2	46	16	
	STATUS 3	45	15	
	STATUS 4	58	28	
	STATUS 5	50	20	
	STATUS 6	48	18	
	STATUS 7	55	25	
	OPEN CABLE DETECT	44	14	
	BUSY	51	21	
	POWER SEQUENCE PICK	29		
	POWER SEQUENCE HOLD	59		

Fig. 7.2-1 A-Cable

		Low	High	
CONTROLLER	1F WRITE CLOCK	2	14	DRIVE
	READ CLOCK	5	17	
	READ DATA	3	16	
	WRITE CLOCK	6	19	
	WRITE DATA	8	20	
	UNIT SELECTED	22	9	
	SEEK END	10	23	
	INDEX	12	24	
	SECTOR	13	26	
	(GND)	1, 4, 7, 11, 15, 18, 21, 25		

Fig. 7.2-2 B-Cable

7.3 A-CABLE INPUT SIGNALS

(1) Unit Select Tag

This signal gates Unit Select 1, 2 and 4 to select the drive. Refer to timing of Unit Select (Figure 7.7-1 if dual channel option is not installed, or Figure 7.7-23 if dual channel option is installed). Elaboration of the dual channel select operation follows.

Suppose that the dual channel option is installed and the drive has been reserved by Unit Select command from channel-A, the drive is not selectable from channel-B until a Release command will be issued from channel-A or the internal 500 ms timer times out. However, Priority Select from channel-B can interrupt the reserved status at any time. (Refer to Figure 7.7-23)

On the other hand, if the dual channel option is installed and the drive has been reserved by a Priority Select command from channel-A, channel-B cannot reserve the drive with Unit Select or Priority Select command until a Release command from channel-A is issued. (Refer to Figure 7.7-24)

(2) Unit Select 1, 2 and 4

These three signals are binary-coded to select the drive and are validated by the leading edge of Unit Select Tag. The logical number of the drive (0 through 7) is selectable by means of a switch located on the PCB (DQEMU; B16B-8140-0010A#U).

Table 7.3-1 Tag/Bus

Bus	Tag 1	Tag 2	Tag 3	(With Unit Select Tag)
	Cylinder Address	Head Address	Control Select	
0	1	1	Write Gate	-
1	2	2	Read Gate	-
2	4	4	Servo Offset Plus	-
3	8	8	Servo Offset Minus	-
4	16	16	Fault Clear	-
5	32	-	AM Enable	-
6	64	-	RTZ	-
7	128	-	-	-
8	256	-	-	-
9	512	-	Release*	Priority Select*

* Dual Channel only.

(3) Cylinder Address (Tag 1)

The cylinder address is set by Tag 1 and Bus 0 to 9. Throughout Tag 1, the Bus must be stable. Refer to Figures 7.7-2 and -3.

The drive must be On Cylinder prior to Tag 1. When the Bus content is equal to or more than 896 for the drive with fixed heads, the Fixed Head area is selected. When the Fixed Head area is selected, no physical movement of the heads is performed in the drive.

Fixed Head and Movable Head Addresses are specified as follows. (Storage capacity shown is unformatted). Refer to Figure 7.3-1.

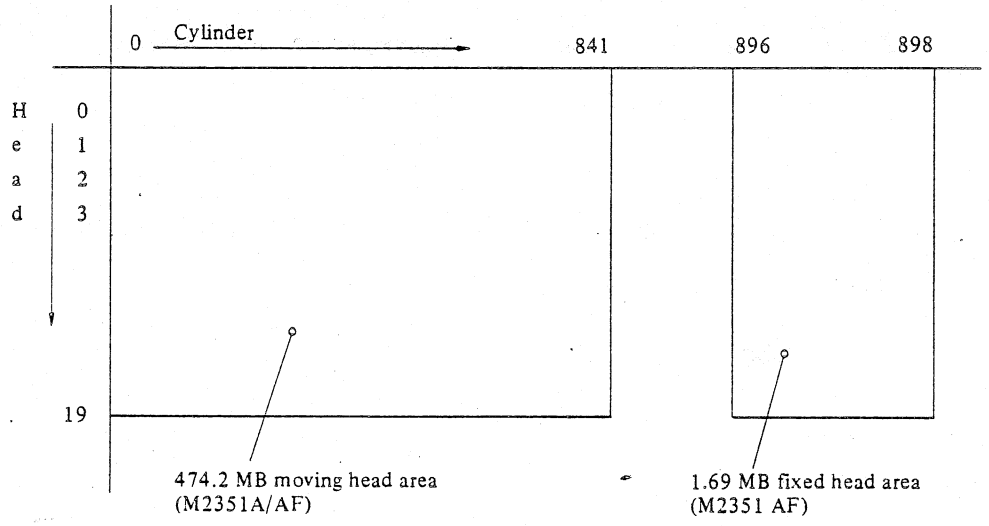


Fig. 7.3-1 Mapping

Detection of Over Cylinder;

Table 7.3-2 shows responses from the drive when illegal cylinder address is issued from the controller.

Table 7.3-2 Responses for Over Cylinder

CYL. / Drive	842 ∿ 895	896 ∿ 898	899 ∿
M2351A	Seek End and Seek Error		
M2351AF	Seek End and Seek Error	(No response)	

(4) Head Address (Tag 2)

The head address is set by Tag 2 and Bus 0 to 4. Throughout Tag 2, Bus 0 to 4 must be stable. Refer to Figures 7.7-4, -5, -6, -7 and -8.

If the Head Address transferred from the controller is equal to or more than 20, no response is generated in the drive.

(5) Control Select (Tag 3)

Bus 0 to 9 gated by Tag 3 have a different meaning in each bit. All signals are defined as control signals.

(5-1) Write Gate (Bus 0)

Enables the write operation on the specified track. It is validated under the following conditions;

Unit Ready ---------- True
On Cylinder --------- True
Seek Error ---------- False
Fault --------------- False
Open Cable Detect --- True
File Protected ------ False
Servo Offset -------- False
Read Gate ----------- False

If Write Gate is turned on in cases other than the above mentioned conditions, Fault occurs and the Write operation is inhibited immediately. See Figures 7.7-4, -7, -20, -21 and -22.

(5-2) Read Gate (Bus 1)

Enables the Read operation on the specified track. It is validated under the following conditions;

Unit Ready ---------- True
On Cylinder --------- True
Seek Error ---------- False
Fault --------------- False
Open Cable Detect --- True
Write Gate ---------- False

See the Read Gate timing chart in Figures 7.7-4, -7, -21 and -22.

(5-3) Servo Offset Plus (Bus 2)

When this signal is true, the head is offset 100 micro-inches away from nominal On Cylinder position in the outer direction with the response of Seek End and On Cylinder after 5 ms. Data cannot be written in the offset mode.

See Figure 7.7-9.

When Servo Offset Plus and Minus are sent simultaneously, Servo Offset Plus will be effective.

(5-4) Servo Offset Minus (Bus 3)

When this signal is true, the head is offset 100 micro-inches away from nominal On Cylinder position in the inner direction with the response of Seek End and On Cylinder after 5 ms. Data shall not be written while in the offset mode.

See Figure 7.7-9.

(5-5) Fault Clear (Bus 4)

This signal clears the fault status i.e., Write/Read Check Status, however, if the cause of the Fault condition still exists, the status will not be cleared.

See Figure 7.7-10.

(5-6) AM Enable (Bus 5)

AM Enable, in conjunction with Write Gate or Read Gate, is used in a Variable Sector Format. When AM Enable is true while Write Gate is true, an AM of three bytes (DC erase) is written on the track.

Refer to Figure 7.7-11.

When AM Enable is true while Read Gate is true, the read circuit searches an AM of three bytes. When the AM is found, the drive will issue Address Mark Found to the controller.

See Figure 7.7-12.

(5-7) RTZ (Bus 6)

Wherever the movable heads are located, they return to cylinder zero and head zero when the RTZ signal is received. Also, the RTZ signal is functional in the fixed head area and resets Fixed Head Select latch. This signal clears the Seek Error.

Refer to Figure 7.7-13.

(5-8) Release (Bus 9); Dual Channel only

After the drive is reserved by Unit Select or Priority Select, Release command becomes valid at Tag 3 and Bus 9. Enabling this signal will release the reserved status in the drive, making alternate channel access possible after selection by the other channel. (Refer to Figures 7.7-23 and -24.)

If the drive has been reserved by Unit Select and the Release Timer Switch on the optional dual channel PCB (DQFMU; B16B-8150-0010A#U) is set to RLTM side, the drive will automatically release the reserved condition approximately 500 ms after the Unit Select command is issued.

(6) Priority Select (Bus 9 with Unit Select Tag and Unit Select 1, 2, 4)

By sending Priority Select (Bus 9) along with Unit Select Tag, Unit Select 1, 2, 4, a controller can select the drive even if it has been selected or reserved by the other channel, except when its own channel is disabled by the Disable switch or the drive is priority selected by the other channel.

With this command, the drive is set in the unconditionally reserved state with respect to that channel. Once it is unconditionally reserved, the control becomes exclusive, i.e., the other channel cannot access the drive until the drive is released from the controller which has reserved the drive. If the drive is unconditionally reserved, all the signals including Unit Selected, and Busy signals are inhibited with respect to the other channel. (Refer to Figure 7.7-24).

(7) Open Cable Detect (Channel Ready)

This signal is used to prevent damage of data caused by interface disturbances when the power to the controller is lost. Therefore, this signal must be stable when the controller is available, and must be disabled before logic levels decay on the interface when a power failure occurs in the controller.
Refer to Figure 7.7-14.

(8) Tag 4 and 5

Unit Status, Sector Status, Write/Read Check Status and Access Status can be sensed through Status 0 ∿ 7 lines with a combination of those two coded signals. Status 0 to 5 for Unit Status are always displayed by 5 LEDs and Status 0 to 7 for DE Sequence State, Write/Read Check State and Access State are also displayed by 7-segment LEDs on the PCB (HGAMU; B16B-7830-0010A#U) for maintenance aid.

See Table 7.4-1 for information about these Tags.

Note that Unit Status can always be on the interface by shorting a circuit on the Logic PCB (C16B-5123-0980#U) with a shorting plug. (Refer Table 3.3-1)

See Figure 7.7-15 for time specifications.

(9) Power Sequence Pick/Hold

Power Sequence is required when the Remote/Local switch on the power supply unit is set to Remote. In this mode, when the controller sets the Pick and Hold lines to ground, the first drive's spindle starts rotating if the start switch has been pressed. Approximately five seconds later the Pick signal is transferred to the next drive, and this is repeated until all drives are sequenced up. When both signals go false, the spindle stops rotating. If the mode switch on the power supply unit is set to Local, each Start Switch must be pressed manually to start the spindle rotating. Refer to Figure 7.7-16.

7.4 A-CABLE OUTPUT SIGNALS

(1) Status 0 to 7

The Status 0 to 7 lines indicate status information determined by combinations of Tag 4 and Tag 5 signals. Information available is specified in Table 7.4-1.

Table 7.4-1 Status

Tag 4	False	True	False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Status	Write/Read Check Status	Access Status
0	Unit Ready	Sector 1	Index Check	DE Sequence Check
1	On Cylinder	Sector 2	Control Check	Access Time-Out Check
2	Seek Error	Sector 4	Multi Head Check	Over Shoot Check
3	Fault	Sector 8	Head Short Check	Rezero Mode Latch
4	Write Protected	Sector 16	Write Current on Read Check	Servo Latch
5	Address Mark Found	Sector 32	Write Transition Check	Linear Mode Latch
6	Index	Sector 64	Delta I Write Check	Control Latch
7	Sector	Sector 128	Servo Off-Track	Wait Latch

(2) Unit Status

When both Tag 4 and 5 are False, Status 0 ∿ 7 indicate the basic information required for the Seek, Read and Write operations.

(2-1) Unit Ready (Status 0)

When this signal is true and the drive is selected, this signal indicates that the drive has reached the rated speed. Note that when the drive is in fault condition, Unit Ready may or may not be issued depends on the position of a jumper plug as described in Table 3.3-1.

(2-2) On Cylinder (Status 1)

Indicates that the heads are located on the specified track. This signal goes false for approximately 3 ms at the beginning and at the end of the offset operation. For a zero Track Seek, On Cylinder will go false for max. 10 μs.

Refer to Figures 7.7-3 and -9.

(2-3) Seek Error (Status 2)

Indicates that a Seek Error has occurred. In this case, On Cylinder does not go true. The Seek Error is cleared when an RTZ (Tag 3 and Bus 6) is received or by pushing the Fault Clear Switch on the operator panel or maintenance-aid MRTZ Switch on the PCB (HGAMU; B16B-7830-0010A#U). The Seek Error status is defined as follows;

1. Seek or RTZ operation is not complete within the specified time.
2. Heads travel to a position outside the recording area.
3. An illegal cylinder address is issued to the drive.
4. Head overshoots to an unspecified cylinder address.
5. Seek command is received by the drive during the not On Cylinder status, when the heads are in motion, or during a Write/Read operation.

(2-4) Fault (Status 3)

Indicates that a fault condition for Write/Read operation exists in the drive. Fault conditions are described in the Write/Read Check status in detail.

If one of the Fault conditions occurs, writing is immediately inhibited and the Fault signal is issued to the controller.

The Fault status can be cleared by one of the following operations;

1. Fault Clear on Tag 3 and Bus 4
2. Fault Clear switch on the operator panel
3. Pushing on the maintenance-aid MRTZ Switch on the PCB (HGAMU; B16B-7830-0010A#U)
4. Switching off the power to the drive
5. Stopping rotation of the spindle motor

Fault Status turns on the check lamp on the operator panel as well as Maintenance Aid LED on the PCB.

(2-5) Write Protected (Status 4)

Indicates that the drive is in the write-protected mode. The write-protect function is enabled by the File Protect Switch on the operator panel, and becomes active while the drive is not selected. If the drive is selected and the write-protect-function is desired, the drive must be momentarily deselected.

(2-6) Address Mark Found (Status 5)

Address Mark Found is an 8-Byte pulse which is sent to the controller at least 2 Bytes after the recognition of a 3-Byte DC-erased area.

(2-7) Index (Status 6)

Index mark is derived from the servo information. It occurs once per revolution and is used for reference in Write/Read operation.

Refer to Figure 7.7-17 for the timing of Index and Sector.

(2-8) Sector (Status 7)

The Sector mark is also derived from the servo information. The number of sectors per revolution is selectable by 15 jumper plugs and is determined by counting Byte Clock. The short circuits are located on the Logic PCB (C16B-5123-0980#U). Each pin of the short circuit represents a binary number minus 1 of Byte Clock to be counted in each sector.

(3) Sector Status (Status 0 ∿ 7)

Indicates the current sector address from 1 to 255 in the drive. Refer to Figure 7.7-17 for timing of Sector Address.

(4) Write/Read Check Status

Indicates the fault status while in the Write or Read operation. When one of these conditions occurs in the drive, the Fault signal in the Unit Status is issued as a summary to the controller. It can be cleared by a Fault Clear Signal from the controller.

(4-1) Index Check (Status 0)

Indicates that the Index signal is not detected where it should be or was detected where it should not have been while performing Write/Read operations.

(4-2) Control Check (Status 1)

The following fault conditions cause Control Check.

1. Wire and Read Gate are issued at the same time.
2. Write operation during offset mode.
3. Write Gate is issued in the write protect mode.

(4-3) Multi-Head Check (Status 2)

Indicates that two or more head ICs are selected simultaneously. (One DE has five head ICs and four heads are connected to one head IC.)

(4-4) Head Short Check (Status 3)

Indicates that abnormal current was sensed in the Write Select line during write operation.

(4-5) Write Current on Read Check (Status 4)

Indicates that write current was sensed during a read operation.

(4-6) Write Transition Check (Status 5)

Indicates that write current has not been switched for writing data. The detection is continued from byte-8 after Write Gate is true until the end of the Write operation.

(4-7) Delta I Write Check (Status 6)

Indicates that an abnormal write current was sensed in the inner head, outer head or fixed head.

(4-8) Servo Off-Track (Status 7)

Indicates the following fault conditions.

1. The head is ±100 micro inches off the desired track during the Write/Read operation.
2. Write/Read Gate is received by the drive during not On Cylinder status, heads in motion or seek error.

(5) Access Status

Indicates access status of the head in Seek and RTZ operation. It also indicates start and stop sequence of the spindle motor.

(5-1) DE Sequence Check (Status 0)

Indicates that an abnormal start/stop sequence of the DE occurred in the drive. Latch 4, Latch 2, and Latch 1 of DE SEQ represent the various DE sequence status as shown in the following table:

Table 7.4-2 Contents of DE Sequence Latches

State No.	Latch 4	Latch 2	Latch 1	Status
0	0	0	0	Wait status
1	0	0	1	The START/STOP switch on the operator panel is set to START.
3	0	1	1	The spindle motor starts rotating.
2	0	1	0	Sequence Rezero starts approximately 40 seconds after State 3.
6	1	1	0	Sequence Rezero is completed and seek operation is possible.
7	1	1	1	DE Stop Sequence State results and the head begins to return to the home position. (Go Home)
5	1	0	1	Go Home operation is completed and the spindle motor stops rotating.
4	1	0	0	Approximately 40 seconds have passed since State 5. (Returns to State 0.)

One of the following errors occurred as DE Sequence State advanced:

1. Initial State Good (Motor At Speed and Hall Alarm are not present) does not result in State 1.
2. Run State Good (not Hall Alarm and Motor At Speed are sent out) cannot be obtained for approximately 40 seconds in State 3.
3. Run State Good goes off during State 6.

It cannot be cleared by the Fault Clear Switch on the operator panel or Fault Clear signal on the interface but only by stopping rotation of the spindle.

(5-2) Access Time-Out Check (Status 1)

During an RTZ or Seek operation, On Cylinder failed to appear within 250 ms ±30% after Access Start. It can be cleared by RTZ operation.

(5-3) Over-Shoot Check (Status 2)

Indicates the heads go past the desired track during Seek or RTZ operation or go into the Guard Band during a Seek operation.

It also indicates that the heads are moving at abnormal speed during RTZ operation.

Over-Shoot Check can be cleared by RTZ operation.

(5-4) Rezero Mode Latch (Status 3)
Servo Latch (Status 4)
Linear Mode Latch (Status 5)
Control Latch (Status 6)
Wait Latch (Status 7)

These five latches observe the sequence of seek and RTZ operations. Whenever an error occurs during Seek or RTZ, the content of these latches are frozen at that time, so that they are beneficial for error analysis. They can be cleared by RTZ operation. The relationship between access state and the contents of latches is shown in Table 7.4-3.

Table 7.4-3 Access States

Rezero Mode Latch	Servo Latch	Linear Mode Latch	Control Latch	Wait Latch	State	Mode
0	0	0	0	1	Wait State	Reset
0	0	0	0	0	Start RTZ	RTZ
1	0	0	0	0	Move In	
1	0	0	1	0	Turn Around	
1	0	1	1	0	Move Out	
0	0	1	1	0	RTZ Linear Mode	
0	1	1	1	0	On Track	
0	1	0	1	0	Accelerate	Seek
0	1	0	0	0	Decelerate	
0	1	1	0	0	Seek Linear Mode	
0	1	1	1	0	On Track	

(6) Busy (Dual Channel only)

If the drive has been already reserved and/or selected, a Busy signal will be issued together with Unit Selected to the other channel attempting the select. Busy signal will remain true until Unit Select Tag is dropped or the Busy condition in the drive is released.

It is necessary to gate Busy signal by Unit Selected signal at the controller.

7.5 B-CABLE INPUT SIGNALS

(1) Write Data

Carries NRZ data which is to be written on the disk surface and must be synchronized with Write Clock. Refer to Figure 7.7-18.

(2) Write Clock

Write Clock is a return signal of the 1F Write Clock issued from the drive as shown in Figure 7.5-1, and must be synchronized with the NRZ Write Data. Refer to Figure 7.7-18.

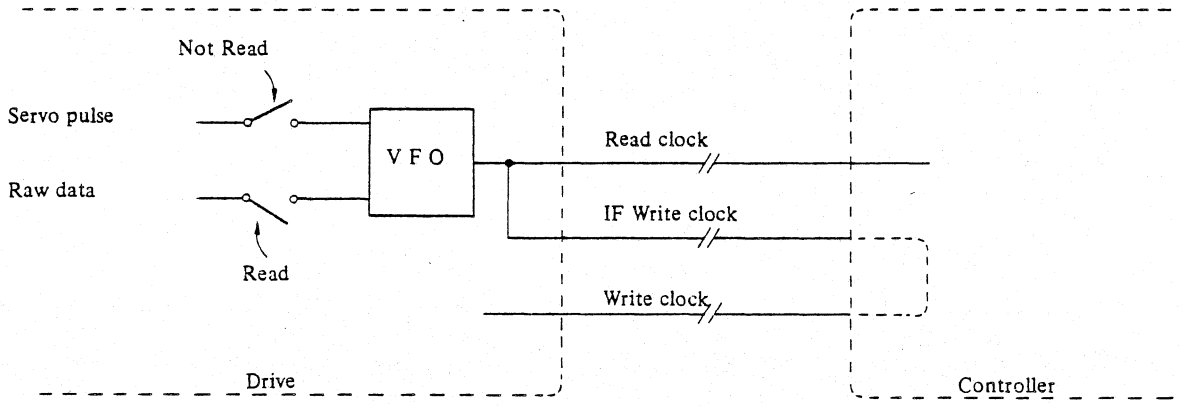


Fig. 7.5-1 Generation of Write/Read Clock

7.6 B-CABLE OUTPUT SIGNALS

(1) 1F Write Clock

Used by the controller to synchronize Write Data and Write Clock. It is synchronized to the Servo Pulse while in the Write operation and to the Raw Data during in a Read operation. Refer to item (1) of Chapter 7.5 and Figure 7.7-18.

(2) Read Data

Transmits the recovered data in the form of NRZ data synchronized with the Read Clock. Refer to Figure 7.7-19.

(3) Read Clock

Transmits Read Clock which defines the beginning of a bit cell. The Read Data is synchronized with the Read Clock. Refer to Figure 7.7-19.

(4) Unit Selected

When three Unit Select lines match with the logical address of the drive, and the leading edge of Unit Select Tag is received, the Unit Selected goes true and is issued to the controller. This signal activates all signals in the A-Cable. Refer to Figure 7.7-1.

(5) Seek End

In a combination with On Cylinder or Seek Error, Seek End goes true after a Seek or RTZ, indicating that a Seek or RTZ operation has terminated. Seek End goes false for 3 ms at the beginning and end of an Offset operation in default mode. In the other mode, Seek End never goes false at resetting offset as described in Table 3.3-1.

For a Zero Track Seek, it will go false for max. 10 μs. Note that Seek End and On Cylinder do not change when a fixed head is selected. Refer to Figures 7.6-2, -3, -6, -9 and -13.

In case of dual channel sub-system, Seek End is always true to the other channel (unselected channel). Suppose that channel-A attempts to select the drive which has already been selected by channel-B. When channel-B releases Selected and Reserve Condition, Seek End goes false for approximately 30 μs for channel-A which has been waiting.

(6) Index

Same as Index signal in the A-Cable which is described in item (2-7) of Chapter 7.4. This signal is available with or without the dual channel feature.

(7) Sector

Same as Sector signal in the A-Cable which is described in item (2-8) of Chapter 7.4. This signal is available with or without the dual channel feature.

7.7 TIME SPECIFICATIONS

Timings are specified at the connector position of the drive. It is necessary for signal timings to consider both the delay time of the interface cable and the circuit of the controller.

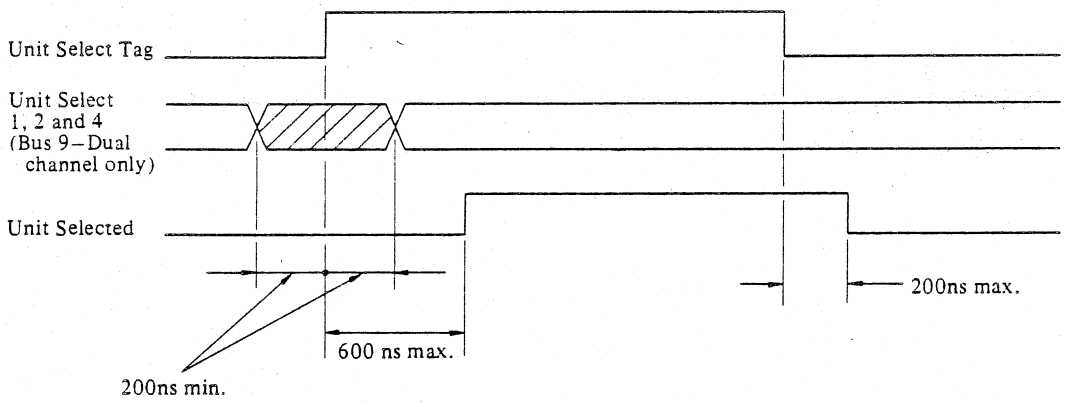
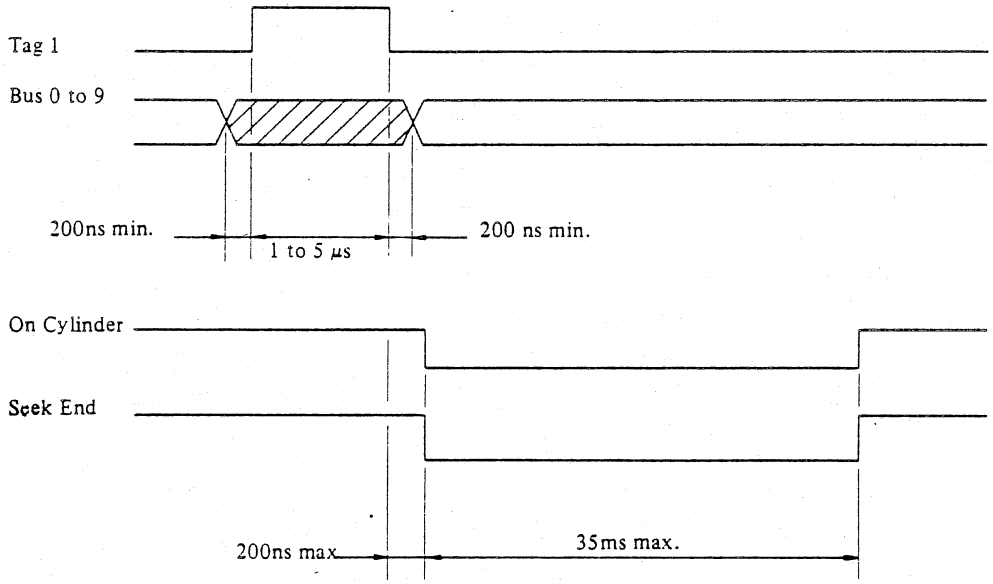


Fig. 7.7-1 Unit Select Timing



Note; The cylinder address must be less than 841 to select a movable head.

Fig. 7.7-2 Seek Timing

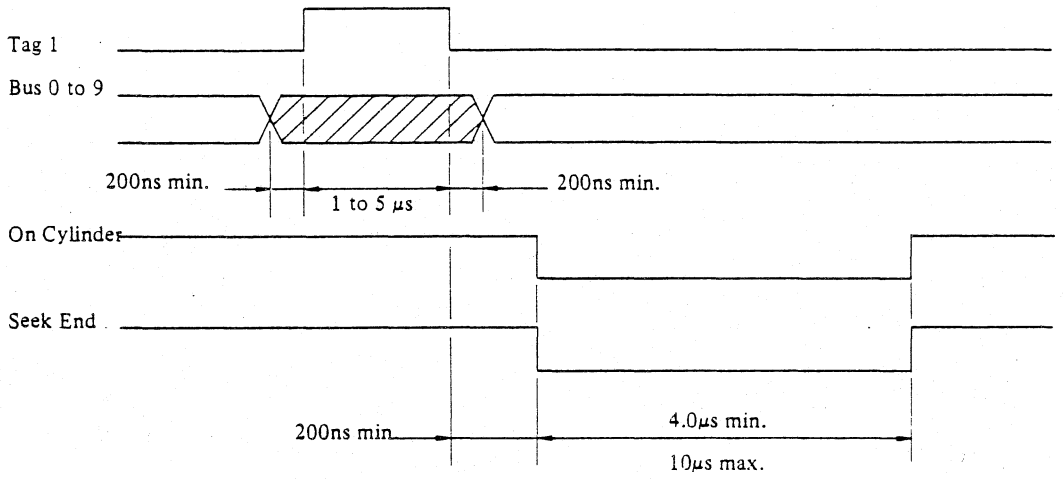


Fig. 7.7-3 Zero Track Seek Timing

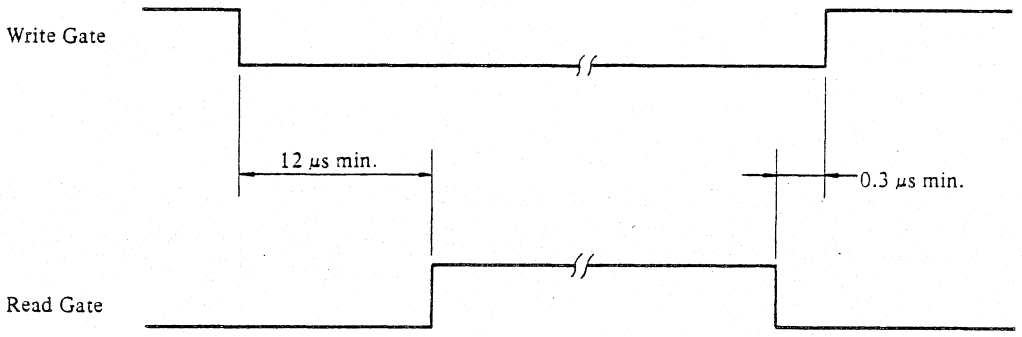
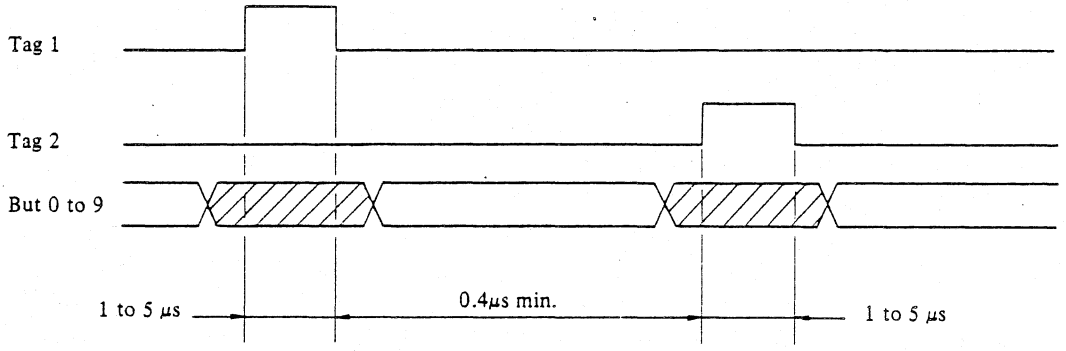
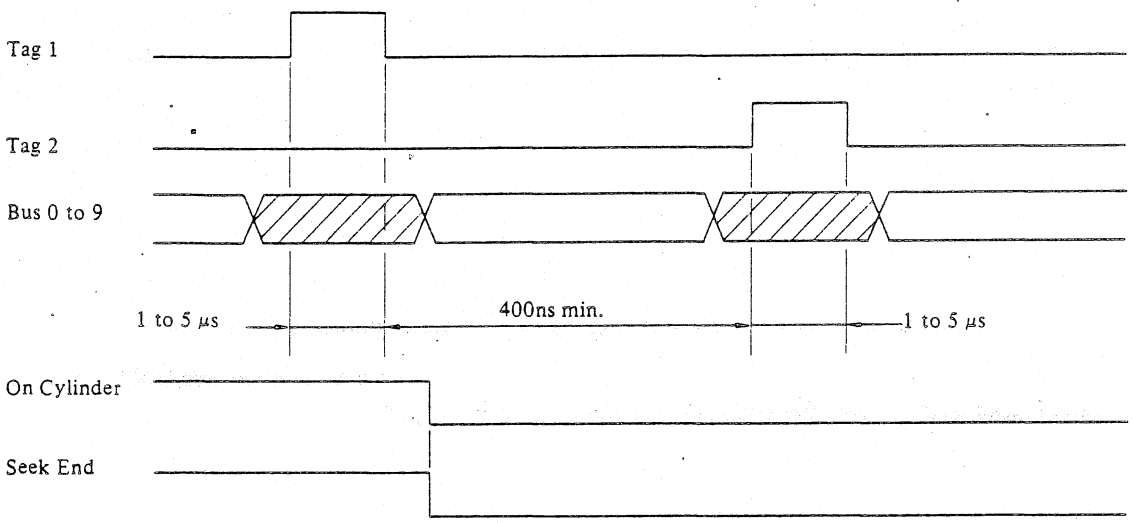


Fig. 7.7-4 Read after Write and Write after Read Timing



Note; When the cylinder address is more than or equal to 896, the cylinder address is defined as a fixed head area and the subsequent Tag 2 is defined as fixed head.

Fig. 7.7-5 Addressing for Fixed Head



Note; Tag 2 can be set during seek operation.

Fig. 7.7-6 Addressing for Movable Head

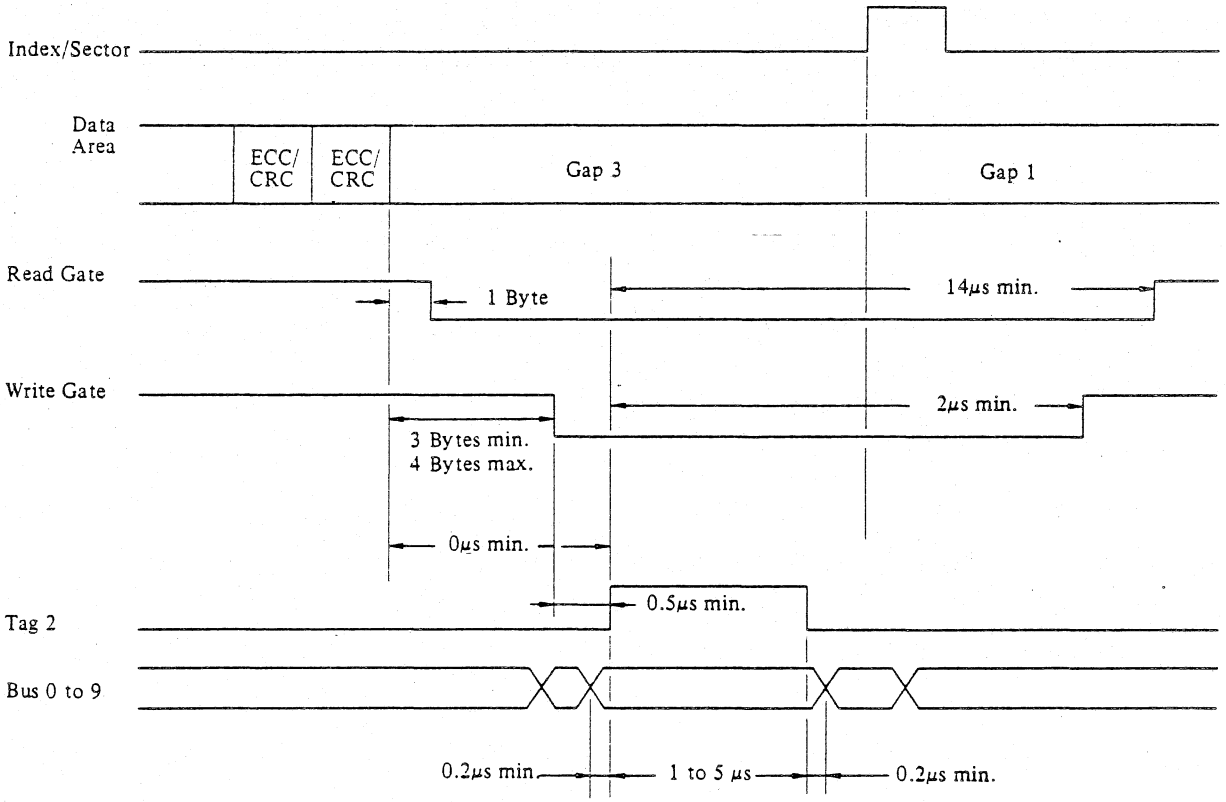


Figure 7.7-7 Head Address Change at the Last Gap

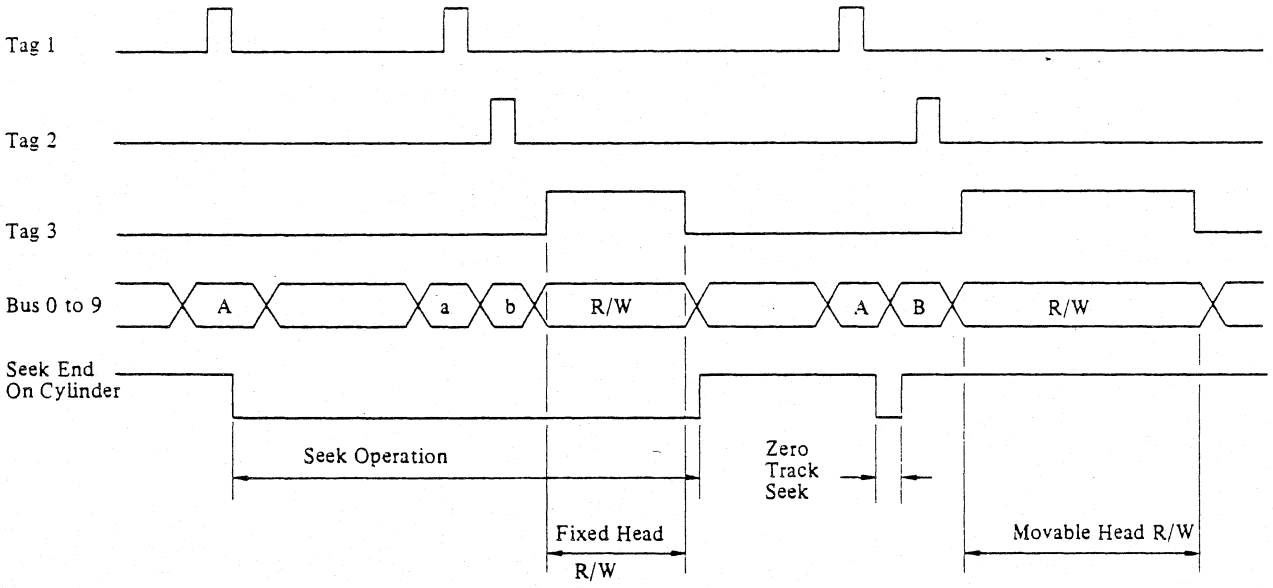


Fig. 7.7-8 Fixed Head Addressing During Seek

The normal sequence of this operation would be in the following order;

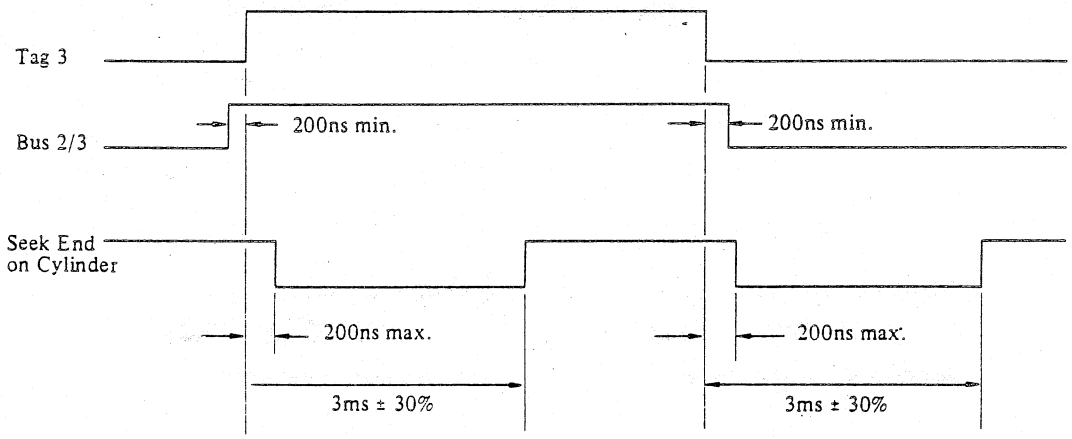
(1) The controller issues Tag 1 (Cylinder Select) with the desired cylinder address (A) of the moving head. On Cylinder and Seek End will go false.

(2) The controller accesses the desired fixed head area with the appropriate cylinder (896-898) (a) and head (b) select signals.

(3) The controller can read or write on the fixed head area while the movable heads are in motion. Reading or writing in the fixed head area during the absence of On Cylinder and Seek End will not cause a Fault.

(4) At the completion of the seek on the movable heads, On Cylinder and Seek End will go true.

(5) After the write or read operation in the fixed head area, the controller must readdress the movable head by sending the appropriate cylinder select (A) (Zero Track Seek) and head select (B) signals. The cylinder select Tag 1 resets the fixed head mode.



Note that Seek End does not go false at offset-reset operation depending on the position of a jumper plug as described in Table 3.3-1.

Fig. 7.7-9 Offset Timing

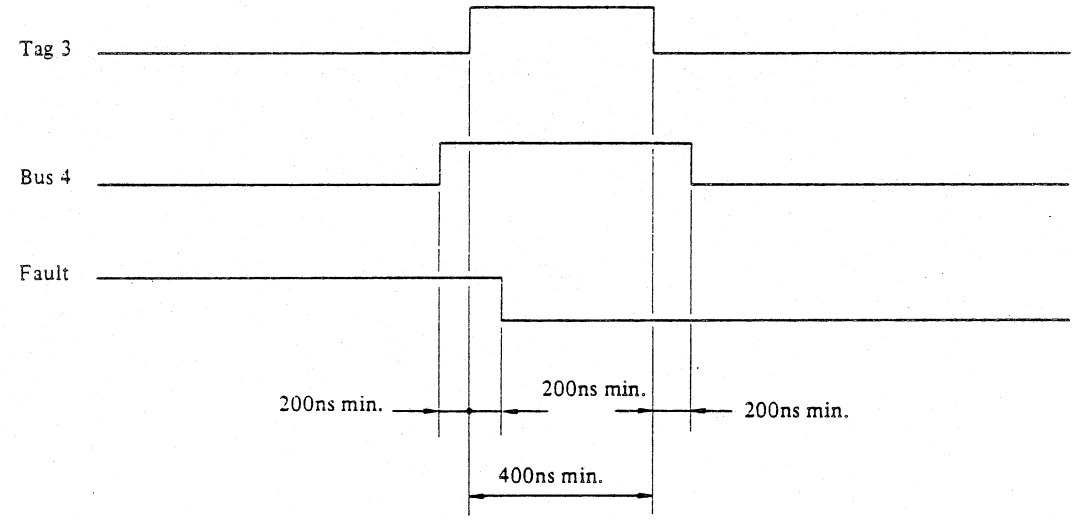


Fig. 7.7-10 Fault Clear Timing

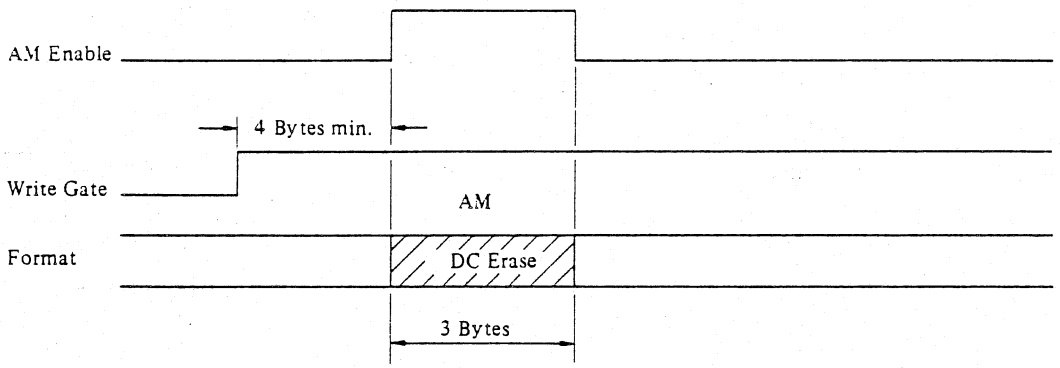


Fig. 7.7-11 AM Write

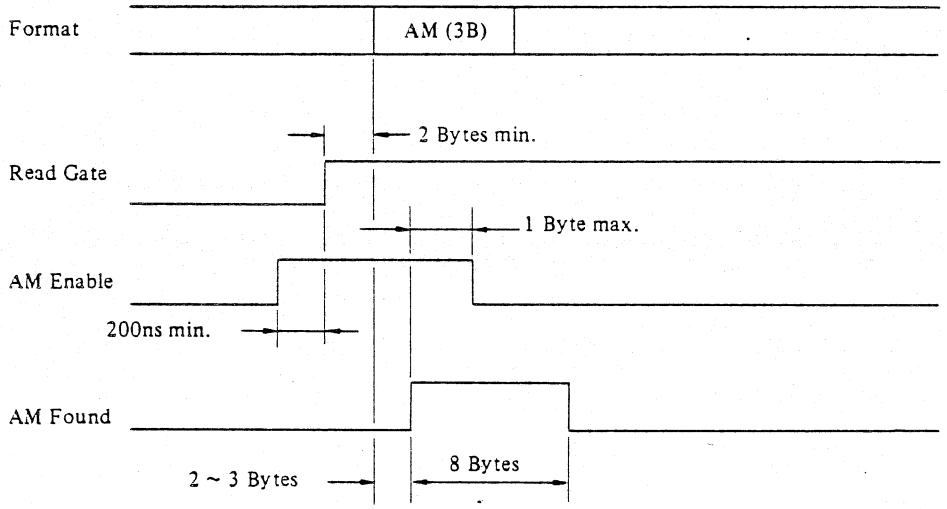
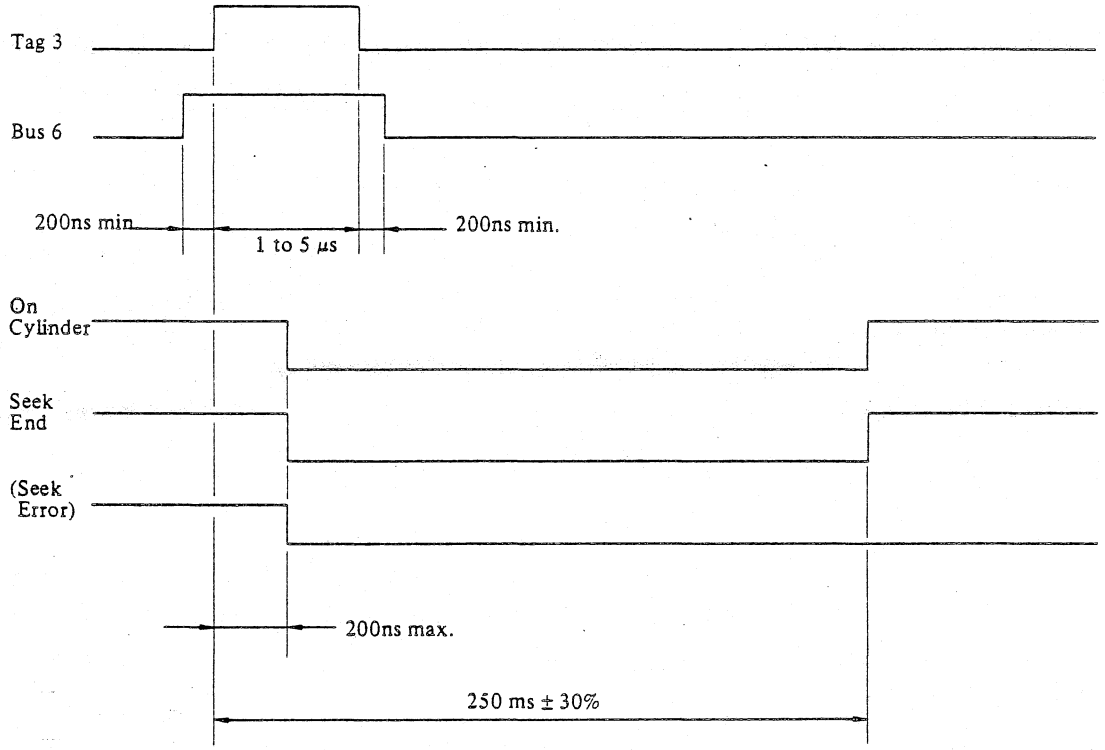
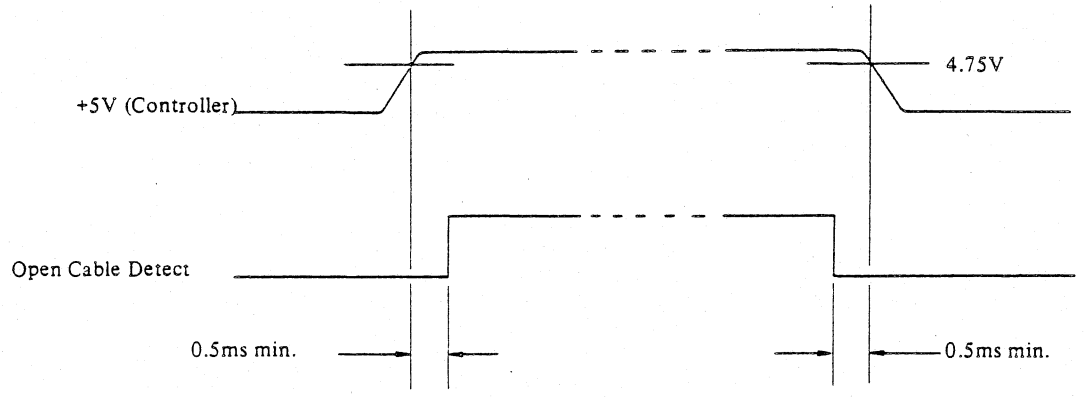


Fig. 7.7-12 AM Detection



Note; On Cylinder is not always set if Seek Error occurs.

Fig. 7.7-13 RTZ Timing



Note; Two Drivers of SN75110 would be required in parallel without termination to increase the drive current in the interface cable.

Fig. 7.7-14 Open Cable Detect Timing

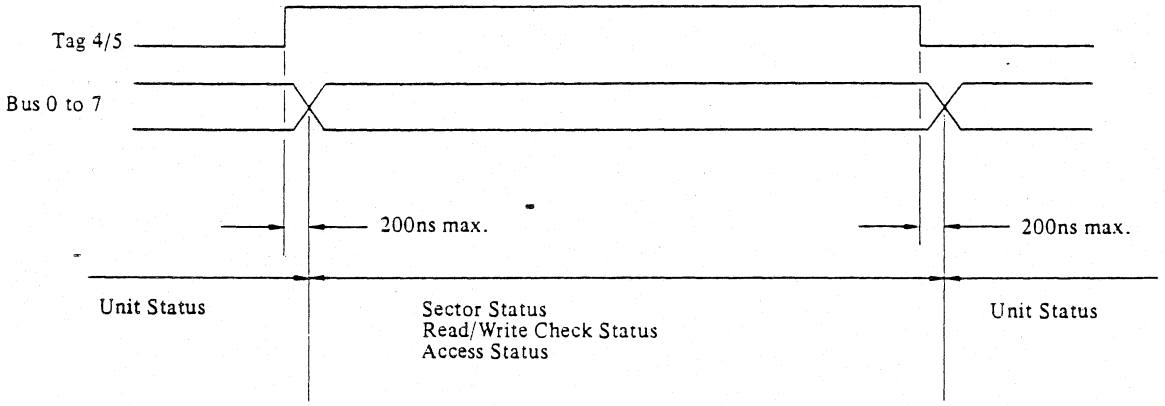


Fig. 7.7-15 Tag 4/5 Timing

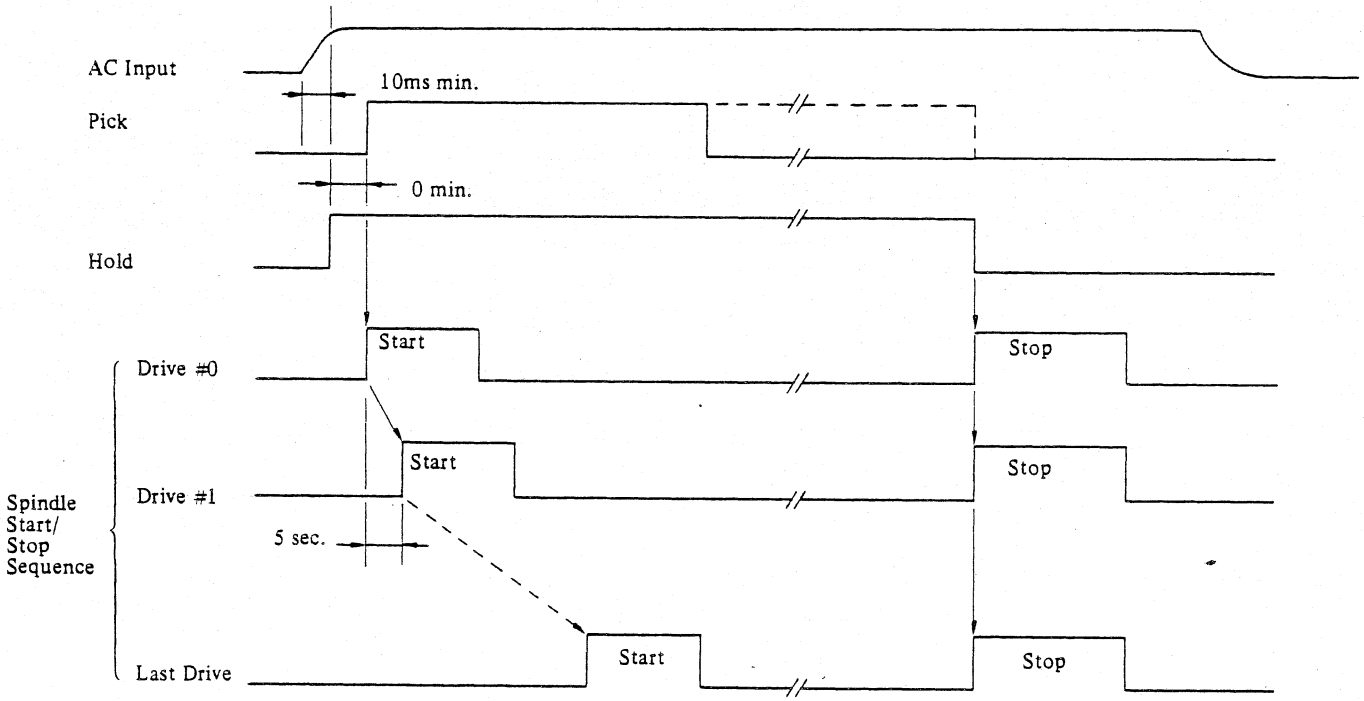


Fig. 7.7-16 Power Sequence Pick/Hold Timing

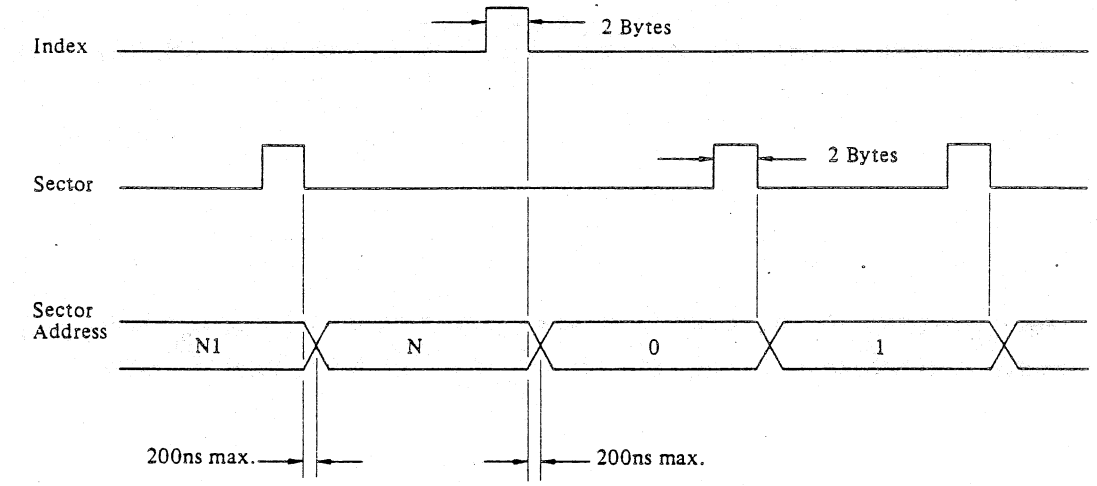
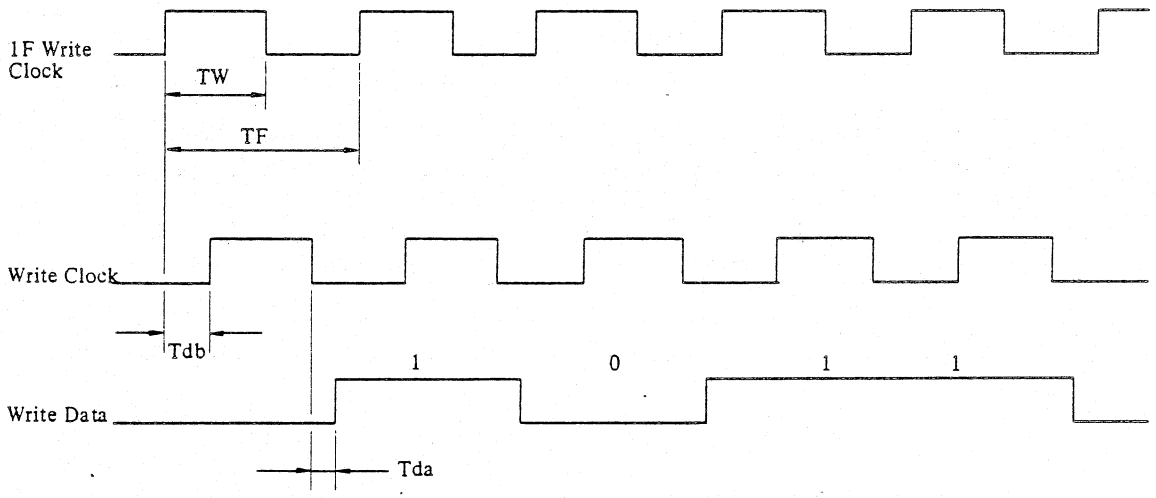


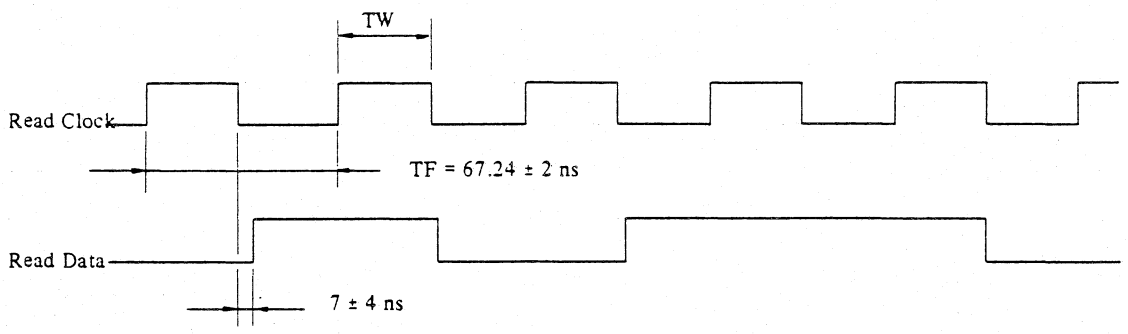
Fig. 7.7-17 Index and Sector Timing



TW = TF/2 = 33.62±2 ns
TF = 67.24±2 ns
Tdb = Continuous delay within 4 bits
Tda = 0±15 ns

Note; (1) Write Data and Write Clock timing shall be specified at the output connector of the controller.
(2) The tolerance of TF includes the rotational speed tolerance and the jitter of servo signal.
(3) NRZ Write Data issued from the controller is put in to the MFM-modulator and then written on the disk surface with write-compensation.

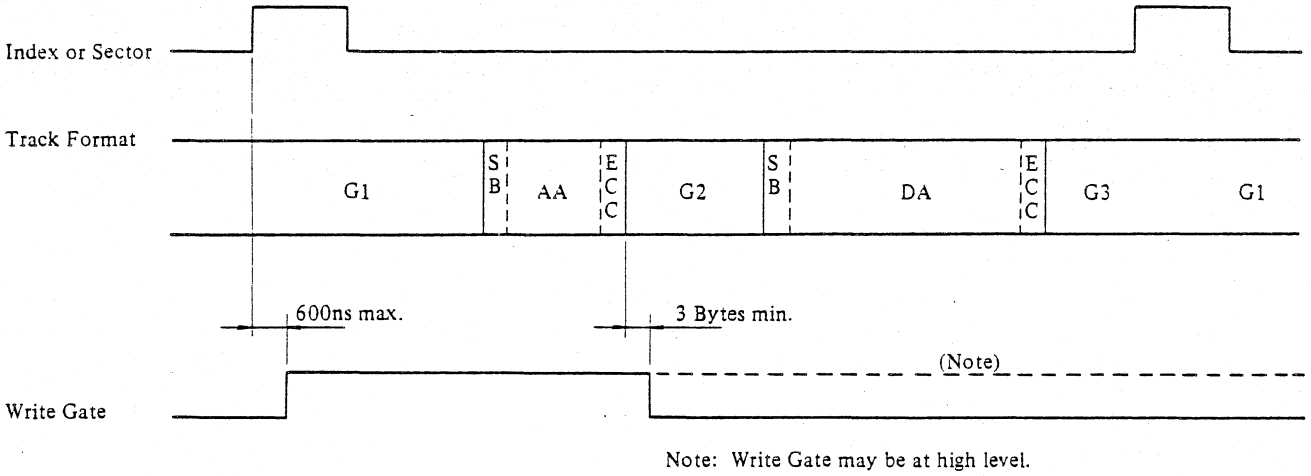
Fig. 7.7-18 Write Clock and Write Data Timing



TW = TF/2 = 33.62±2 ns

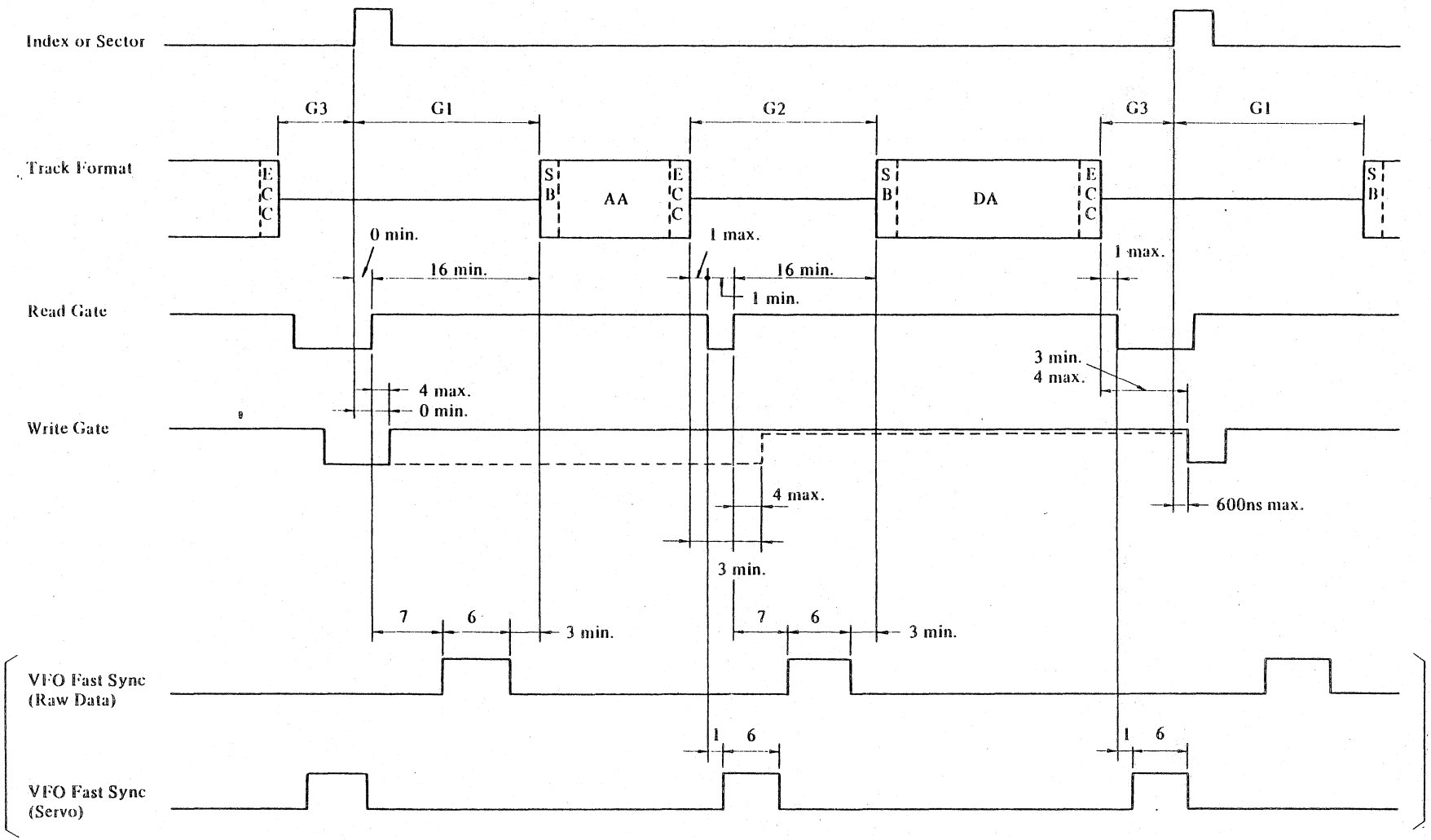
Note; (1) Read Clock and Read Data timing shall be specified at the output connector of the drive.
(2) Read Data signal should be clocked at the positive-going edge of Read Clock in the controller.

Fig. 7.7-19 Read Clock and Read Data Timing



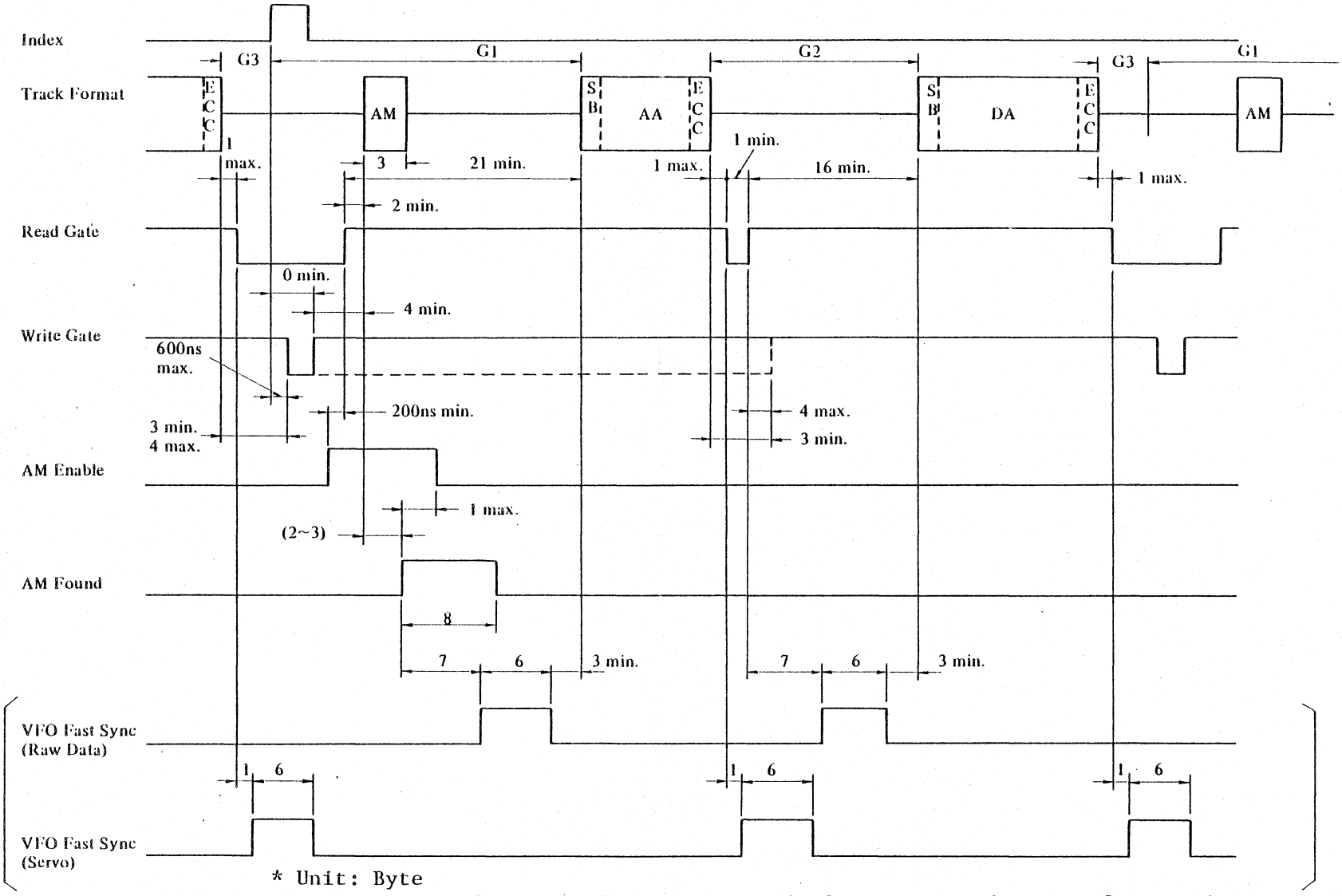
Note: Write Gate may be at high level.

Fig. 7.7-20 Format Write Timing



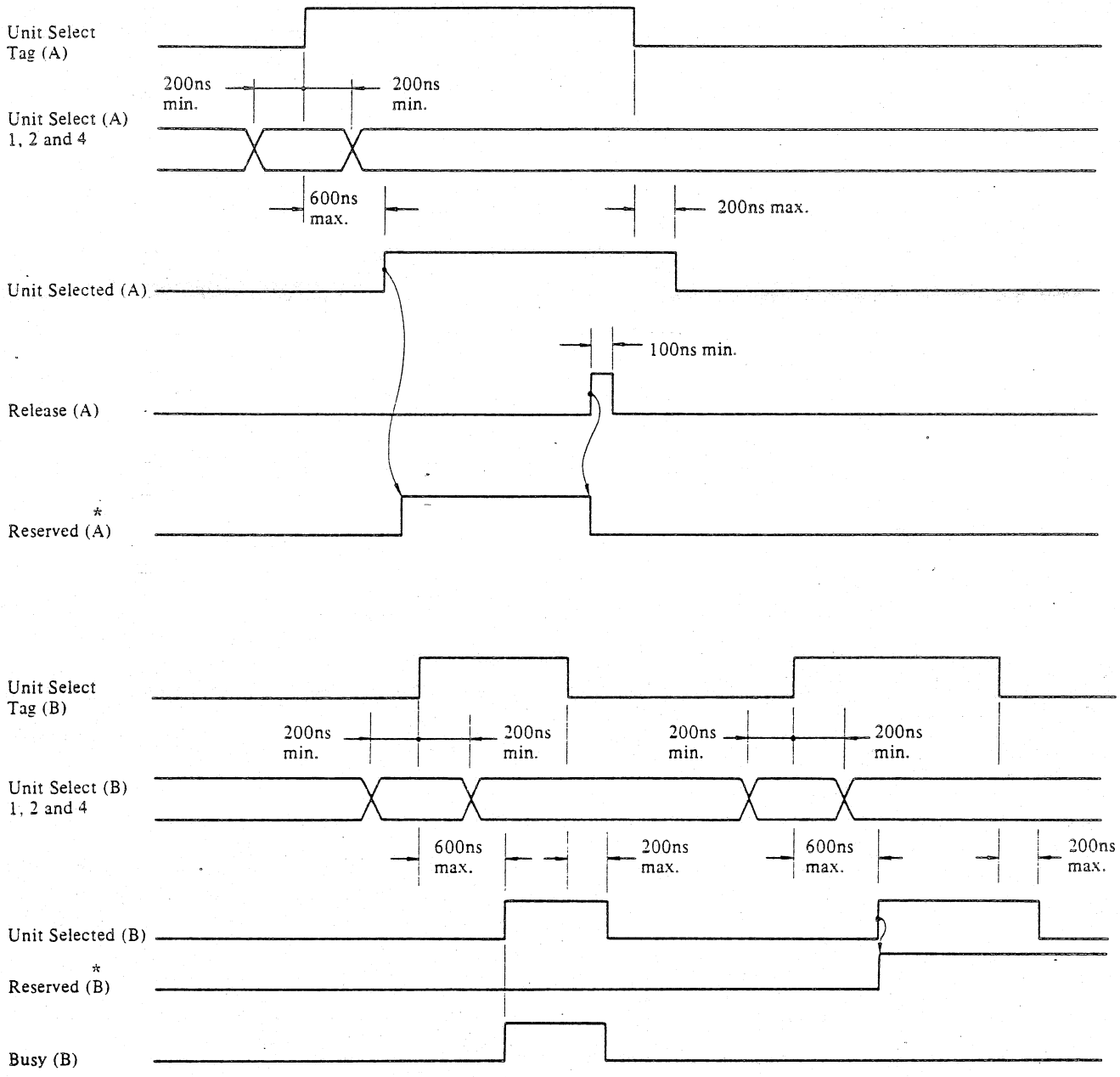
* Unit: Byte
* Not including head switching time, read-after-write and write-after-read transient time.
* VFO Fast Sync (Raw Data and Servo) are signals in the drive.

Fig. 7.7-21 Fixed Sector Format Timing



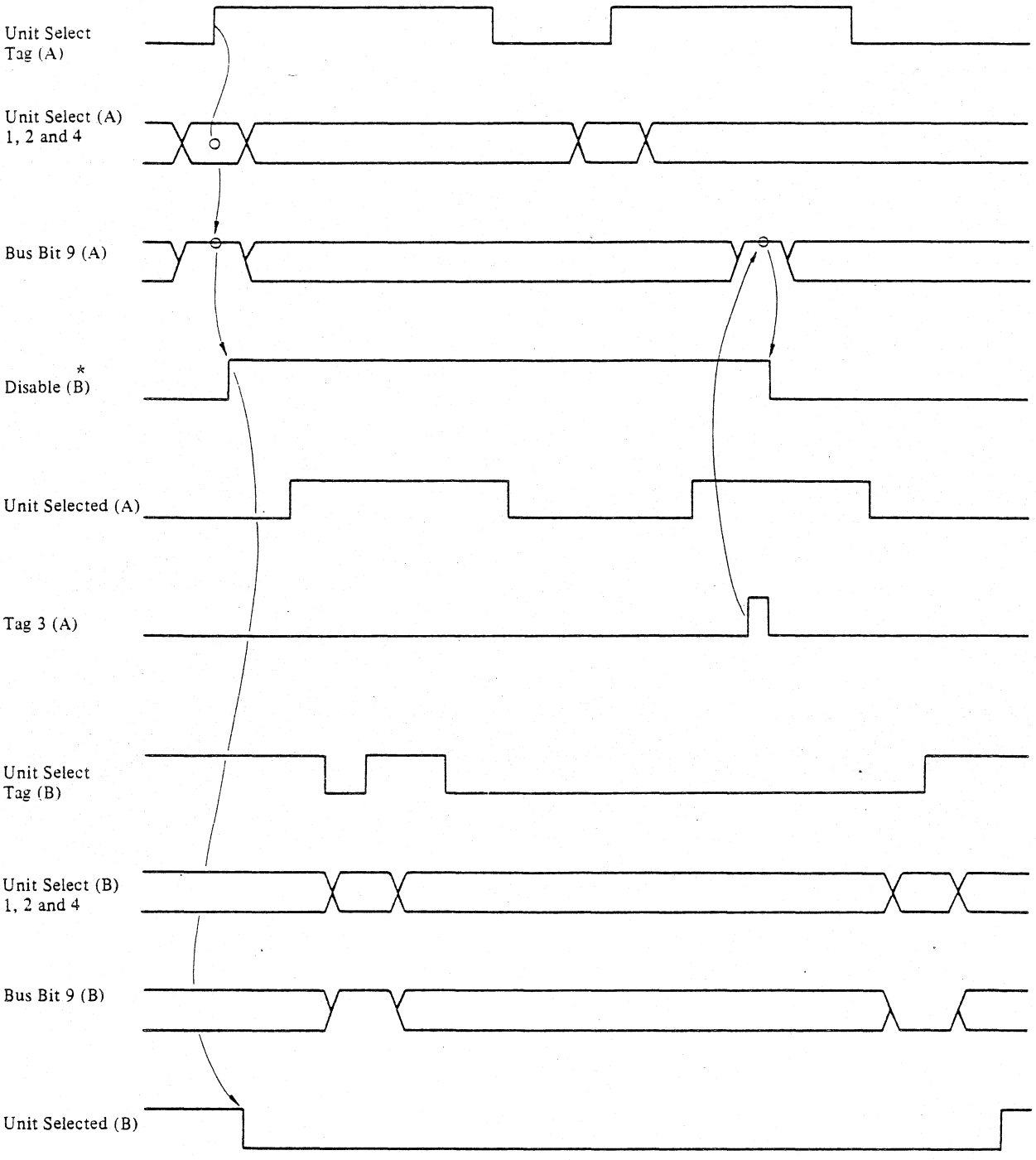
* Unit: Byte
* Not including head switching time, read-after-write and write-after-read transient time.
* VFO Fast Sync (Raw Data and Servo) are signals in the drive.

Fig. 7.7-22 Variable Sector Format Timing



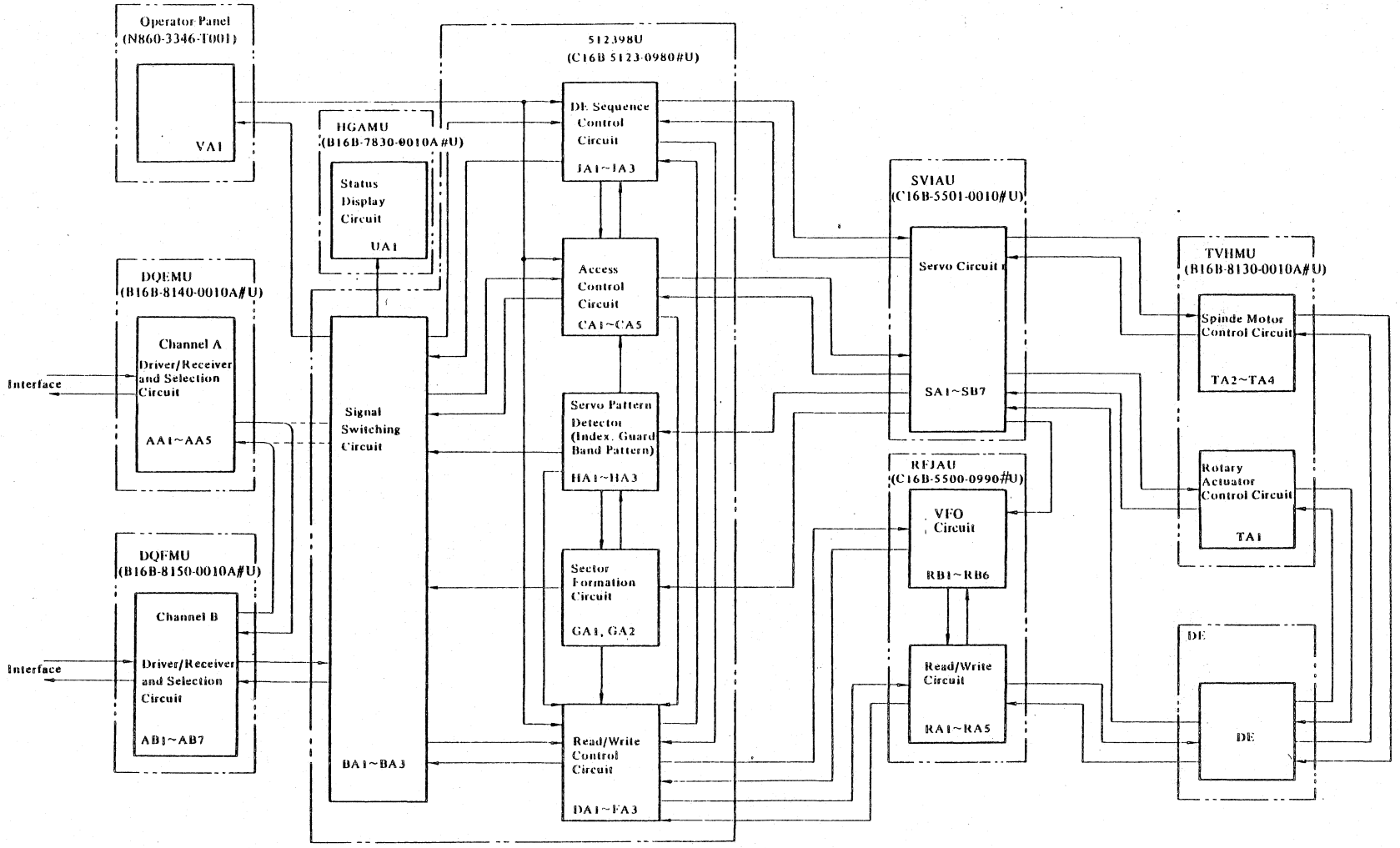
Note; Reserved (*) is a signal within the drive.

Fig. 7.7-23 Unit Select Timing (Dual Channel Only)



Note; (1) Disable (*) is a signal within the drive.
(2) A sequence example of the above is as follows: Channel B Select → Channel A Priority Select → Channel B Priority Select Try → Channel A Release → Channel B Select

Fig. 7.7-24 Priority Select Sequence (Dual Channel Only)



The number at the bottom of each box indicates the circuit diagram number in chapter 17.

Fig. 8.1-1 Drive Circuit Configuration Diagram (Included Dual Channel Option)

8.2 DE SEQUENCE

The drive can execute instructions (TAG1, TAG2, TAG3) sent from the controller after the START switch on the operator panel is set to ON, the disk comes up to the rated speed, the head is moved from the CSS area to cylinder 00 (hereafter called sequence RTZ), and the disk becomes ready. The operations performed between the moment the START switch is set to ON and the moment the drive becomes ready is called the DE Start Sequence. When the START switch is set to OFF, the drive stops the rotation of the disk after the head is moved to the CSS area. The operations performed between the moment the START switch is set to OFF and the moment the disk stops is called the DE Stop Sequence.

Each of these sequences is divided into several states (five states for the DE Start Sequence, and three states for the DE Stop Sequence), which are determined by decoding DE sequence latches 1, 2, and 4 (hereafter called DESQL1, DESQL2, and DESQL4) and are named states 0 to 7 (hereafter called ST0 ∿ ST7). Figure 8.2-1 shows the states of a drive.

DE Start Sequence and Its States

(1) State 0

When power is turned on, DESQL1, DESQL2, and DESQL4 are reset by the Initial Reset signal (PWRST).

(2) State 1

When the START switch on the operator panel is set to ON in state 0 (STARTS is set high), the start latch (STARTL) is set and DESQL1 is set. At this time, if the Initial Good signal is low [INSTG = Hall Alarm signal is low (*HALRM) and Motor Speed signal is low (*MTRSP)], the DE sequence check latch (DESQCKL) is set, DESQL1 is reset, and the operation returns to state 0. When the START switch is set to ON again (OFF → ON), DESQCKL is reset and the operation enters state 1.

(3) State 3

When the INSTG state occurs, DESQL1 and DESQL2 are set in this order and the operation enters state 3. When DESQL2 is set, the disk starts rotation. When the state 3 signal (ST3) goes high, the Start Timer signal (STTMR) is set high,

causing the timer to be started. If the Run State Good signal (RNSTG = *HALRM• MTRSP) remains low about 60 seconds after it has started (EN60S), DESQCKL and DESQL4 are set and the operation enters state 7.

(4) State 2

If RNSTG is high when EN25S is high in state 3, DESQL1 is reset and the operation enters state 2.
The state 2 signal (ST2) goes high, causing the sequence RTZ (SQRTZ) operation to be started.

(5) State 6

The interrupt signal (ACCMP) generated upon completion of the SQRTZ operation sets DESQL4 and the operation enters state 6. In this state, the Unit Ready signal may be sent to the controller.
If one of the following conditions occur during state 6, DESQL1 is set and the operation enters state 7:

1 The START switch on the operator panel is set to OFF.
2 The MTRSP signal goes low.
3 The HALRM signal goes high.

DE Stop Sequence and Its States

(1) State 7

When the State 7 signal goes high, the ANGHM signal is set high, causing the head to start moving to the CSS area (GO HOME).

(2) State 5

The interrupt signal (GHCMP) generated upon completion of the Go Home operation resets DESQL2, and the operation enters state 5. The State 5 signal (ST5) causes the timer to be started.

(3) State 4

The EN11S signal generated upon completion of the timer operation resets DESQL1, and the operation enters state 4.

(4) State 0

The State 4 signal (ST4) resets DESQL4, and the operation enters state 0 to indicate the end of the DE Stop Sequence.

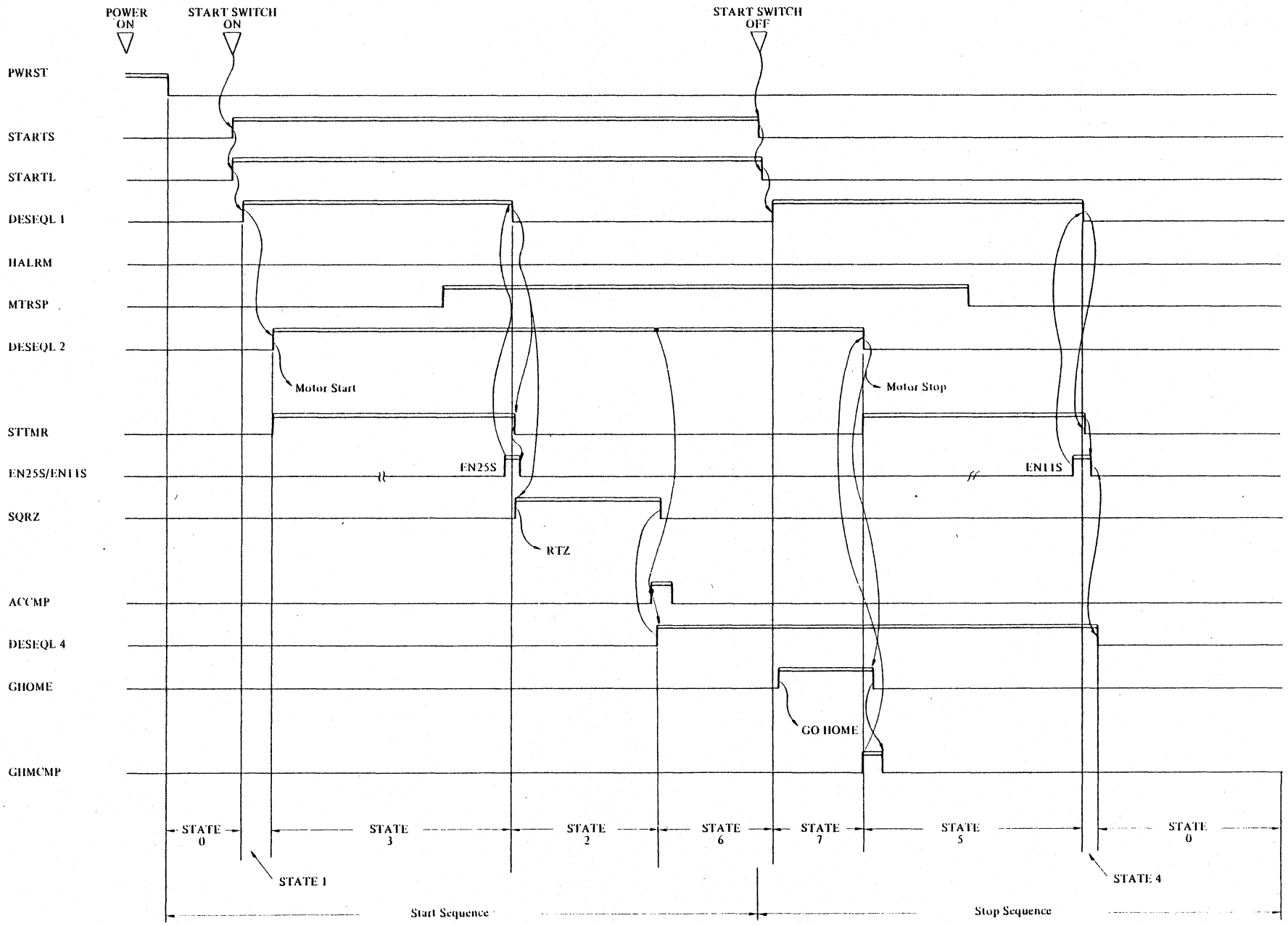


Figure 8.2-1 DE Start/Stop Sequence

8.3 SELECTION

The unit selection must be performed before instructions, such as Seek, Reed/Write, are sent from the controller.

When a drive receives Unit Select Tag (USLTG) and Unit Select 1, 2, 4 (USLCT1, USLCT2, and USLCT4), the drive compares it with its own address. The drive address is set by SW1 on the PCB, DQEMU. If the address sent from the controller matches the address of the drive when the Open Cable Detector (OCDTR) and Power Ready (PWRDY) signals are high, Select Latch (SLCTL) is set, Enable signal (ENABL) is generated, Unit Selected (SLCTD) is sent to the B-cable, and, at the same time, the driver/receiver for the A-cable are enabled for transmission.

While the drive is selected, instructions (Seek, RTZ, Read/Write, and others) may be received. The drive is released when one of USLTG, OCDTR, PWRDY goes low.

Figure 8.3-1 shows the unit selection sequence timing diagram.

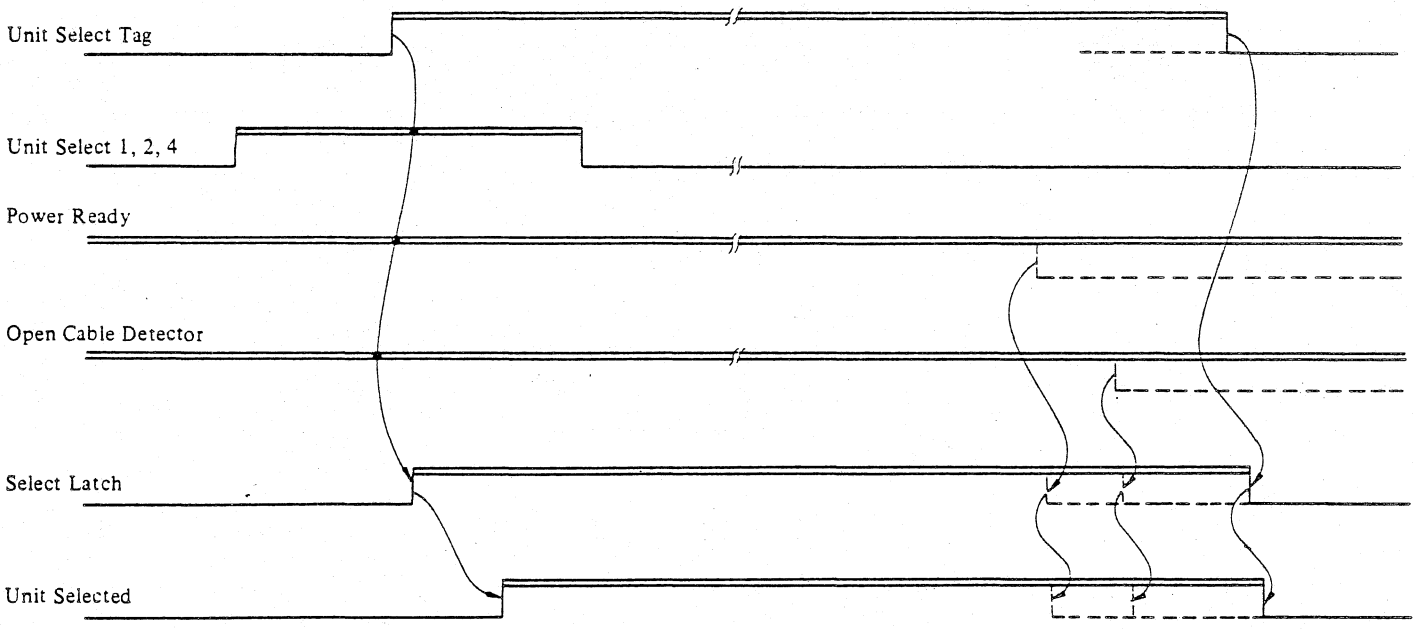


Figure 8.3-1 Unit Selection

8.4 OUTLINE OF ACCESS CONTROL

The access control circuit has five latches for controlling access operation. The operation modes and the outputs of the latches are as follows:

(1) Sequence RTZ

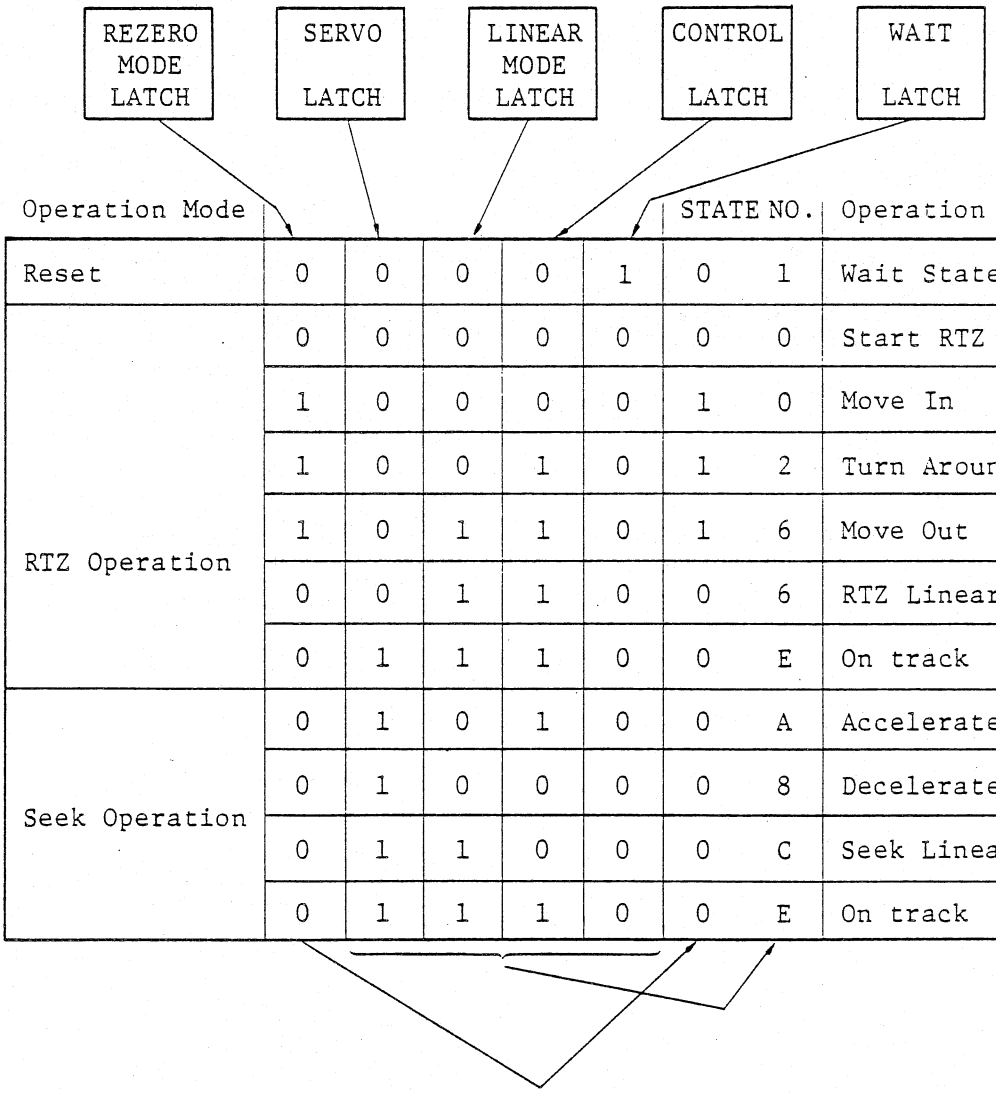
(2) System RTZ

(3) Manual RTZ

(4) Direct seek

(5) Fine control

Table 8.4-1 Access Mode Latches



Operation Mode	REZERO MODE LATCH	SERVO LATCH	LINEAR MODE LATCH	CONTROL LATCH	WAIT LATCH	STATE NO.		Operation State
Reset	0	0	0	0	1	0	1	Wait State
RTZ Operation	0	0	0	0	0	0	0	Start RTZ
	1	0	0	0	0	1	0	Move In
	1	0	0	1	0	1	2	Turn Around
	1	0	1	1	0	1	6	Move Out
	0	0	1	1	0	0	6	RTZ Linear Mode
	0	1	1	1	0	0	E	On track
Seek Operation	0	1	0	1	0	0	A	Accelerate
	0	1	0	0	0	0	8	Decelerate
	0	1	1	0	0	0	C	Seek Linear Mode
	0	1	1	1	0	0	E	On track

8.5 SEQUENCE RTZ

In this mode, the head is moved from the CSS zone to cylinder 00 during the DE Start Sequence. Figure 8.5-1 shows the timing diagram.

(1) State 01 (Wait state)

When Power On Reset goes high, Wait Latch (WAITL) is set high. Control Latch (CNTL), Linear Mode Latch (LNML), Servo Latch (SRVL), and Rezero Mode Latch (RZML) are low.

(2) State 00 (Start RTZ)

When the State 2 (ST2) signal goes high in the DE Start Sequence, Sequence Rezero (SQRZ) and Any Rezero (ANYRZ) are set high and WAITL is set low.

(3) State 10 (Move In)

When ANYRZ goes high, Start Rezero (STRZ) and Rezero Mode Latch (RZML) are set high. STRZ initializes the head address register and the cylinder address register. When RZML is set high, Rezero Mode (RZMOD) is set high and is sent to the servo control circuit.
At this time, the servo head is located at the innermost position of the CSS zone.

(4) State 12 (Turn Around)

When guard band pattern 2 (GBP2) in the CSS zone is detected, Control Latch (CNTL) is set high and, at the same time, High Velocity Set (HVLST) and Move Out Gate (MVOTG) are set high and are sent to the servo control circuit. Upon reception of these signals, the servo control circuit moves the head from guard band pattern 2 (GBP2) to guard band pattern 1 (GBP1) at the REZERO High Speed.

(5) State 16 (Move Out)

As the head is moved through the GBP2 zone in the outer direction, GBP1 is detected. Upon detection of GBP1, Linear Mode Latch (LNML) is set high and, at the same time, HVLST is set low.
From this moment, the head movement speed is reduced to the REZERO Low Speed, and the head is moved in the direction of cylinder 00 (outer direction).
At the end of the GBP1 zone is reached, Guard Band Latch (GRDBL) is set low and,

after that, the head speed is controlled by the Position Curve generated from the Position signal.

(6) State 06 (RTZ Linear mode)

When the head speed reaches the speed determined by the Position Curve, the servo control circuit sets End Decelerate (ENDDC) high and, then, RZML is set low. When RZML goes low, the head is controlled in the Position Error Mode. If the head reaches within a specified distance from the center of cylinder 00 (On Track is high), the monostable multivibrator is activated. If On Track is high again at the end of the monostable multivibrator operation, Track Following Timer (TFTMR) is set high.
The operation mode controlled by Position Error is called Fine Control.

(7) State 0E (On Track)

If Valid Index (VLIX) goes high while TFTMR is high, Servo Latch (SRVL) is set high and Unit Ready, Seek End (SKEND), and On Cylinder (ONCYL) are sent to the controller.
If the sequence RTZ is unsuccessful, that is, if Overshoot Check (OVSCK) or Time Out Check (TMOCK) is detected, Access Check (ACCCK) is set high and the carriage is released. At this time, Unit Ready (UNRDY), Seek End (SKEND), and Seek Error are sent to the controller.
Over Shoot Check (OVSCK) is set high when the head is moved at an abnormal speed during the RTZ operation (VG20I is set high if the speed exceeds 20 inches/second), or when Guard Band Pattern [Inner Guard Band Pattern (GBP2 and GBP1) or the Outer Guard Band Pattern (OGB)] is detected during the fine control, or when the head is not on the track and Track Crossing Pulse (TRXGP) is set high three or more times.
Time Out Check (TMOCK) is set high if the operation is set high and the operation is not terminated within 250 ms.

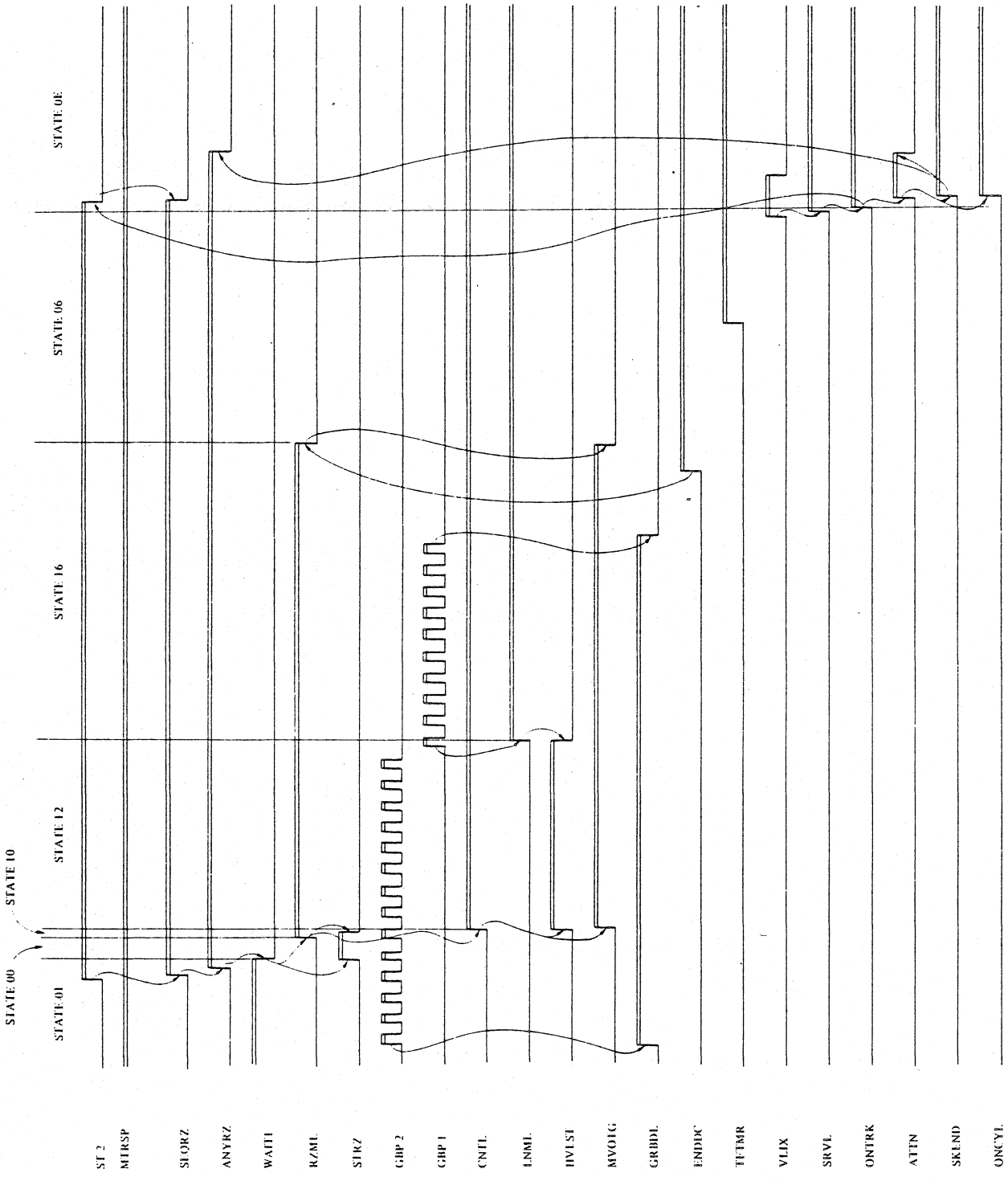


Figure 8.5-1 Sequence RTZ

8.6 SYSTEM RTZ/MANUAL RTZ

In the system RTZ (SYSRZ) and manual RTZ (MRTZL) modes, the head is moved to cylinder 00 regardless of the position at which the head is currently located. The system RTZ operation (SYSRZ) is started, upon receipt of Tag 3/bit 6 (RTZ) from the controller, when the drive is selected and is not performing the seek or RTZ operation or when a seek error occurs. The manual RTZ operation (MRTZL) is started by switch 2 (SW2) on the PCB, HGAMU, when the drive is not performing the seek, RTZ, offset, or read/write operation. Figures 8.6-1 and 8.6-2 show how SYSRZ and MRTZL are started, respectively. Figure 8.6-3 shows the sequence that is performed after RZML is set high.

(1) State 01 (Wait state)

When SYSRZ or the MRTZL operation is performed, ANYRZ is set high.
Then, WAITL is set high, and the access mode latches (RZML, SRVL, LNML, CNTL) and Seek Error (Access Check: ACCCK) are set low.

(2) State 00 (Start RTZ)

When the SYSRZ operation is performed, the access mode latches are set low and, then, WAITL is set low.
When the MRTZL operation is performed, WAITL is set high while SW2 is high.
When SW2 goes low, WAITL is set low.

(3) State 10 (Move In)

When WAITL is set low, STRZ and RZML are set high.
Before the head detects Guard Band Patterns 1 and 2 (GBP1 and GBP2), the carriage is moved in the inner direction at the RTZ High Speed. When the carriage passes cylinder 00 and GBP1 is detected, Guard Band Latch 1 is set high and the speed is reduced to the low speed.
If the head is on GBP1 at the start of this state, the carriage is moved at the low speed from the beginning.

(4) State 12 (Turn Around)

When the head passes GBP1 and detects GBP2, CNTL is set high and, at the same time, HVLST and MVOTG are set high. In this case, the head is moved at the high speed to the outer direction.

(5) State 16 (Move Out)

Same as that of sequence RTZ.

(6) State 06 (Rezero Linear Mode)

Same as that of sequence RTZ.

(7) State 0E (On Track)

Same as that of sequence RTZ.

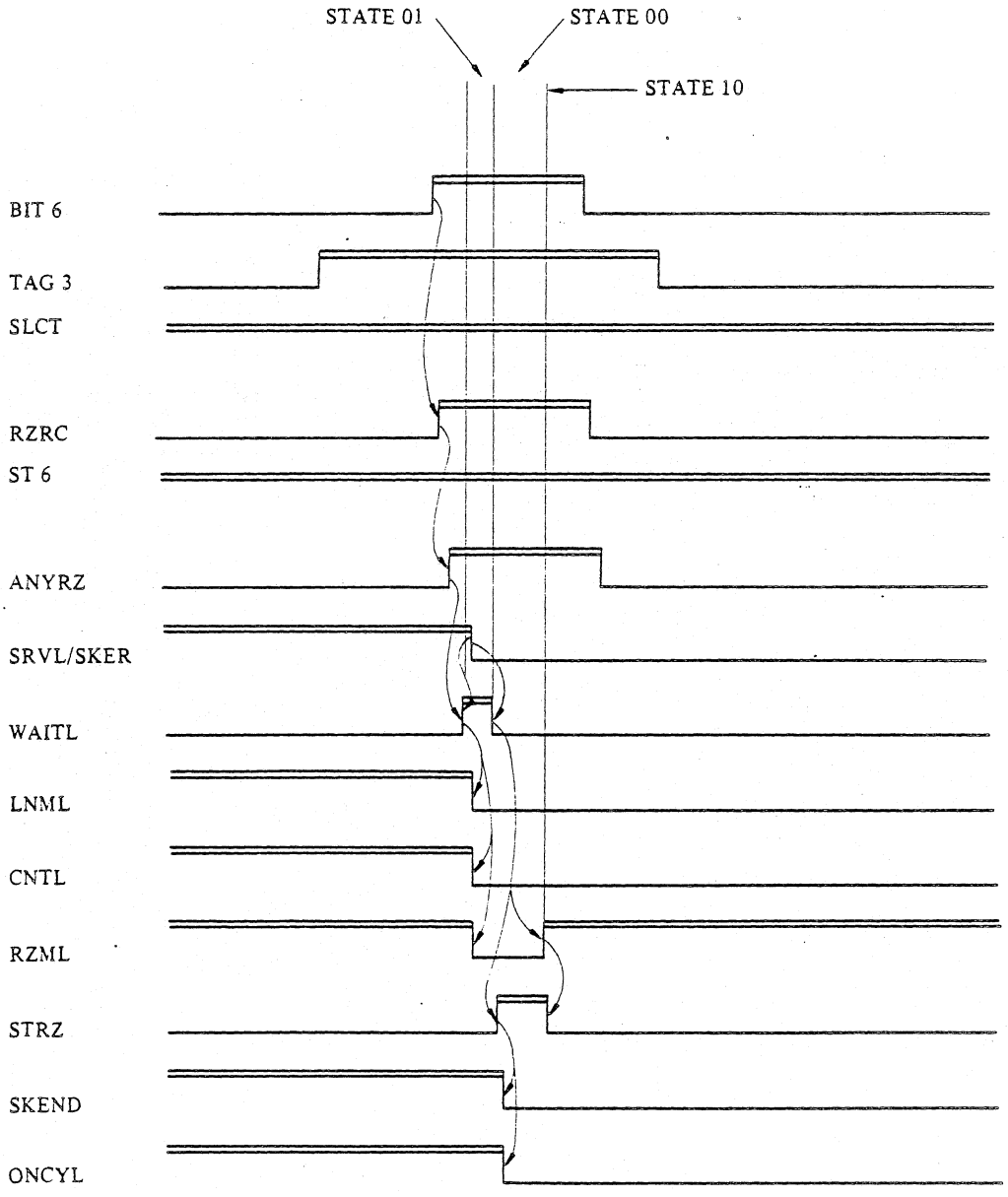


Figure 8.6-1 System RTZ Sequence

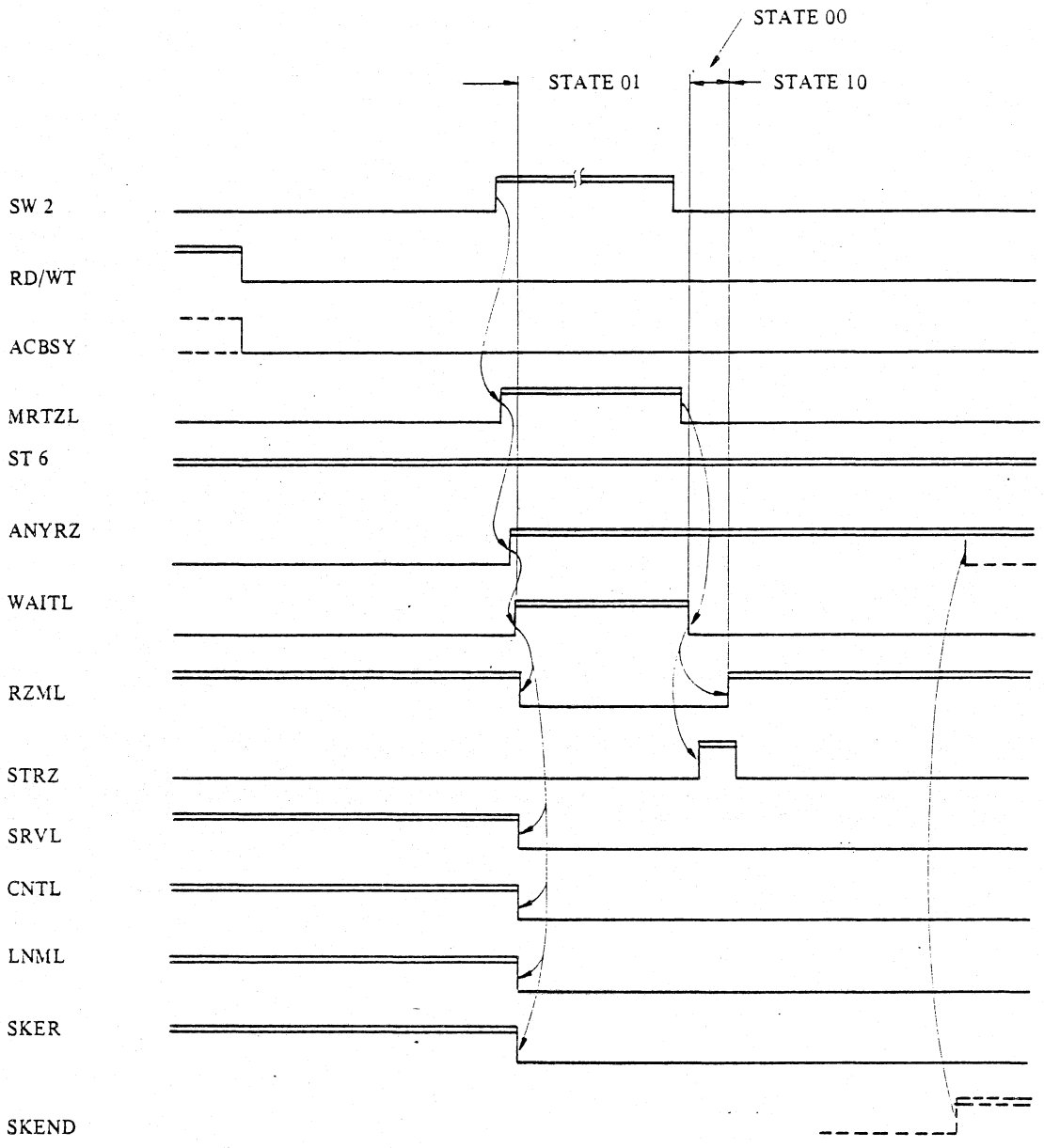


Figure 8.6-2 Manual RTZ Sequence

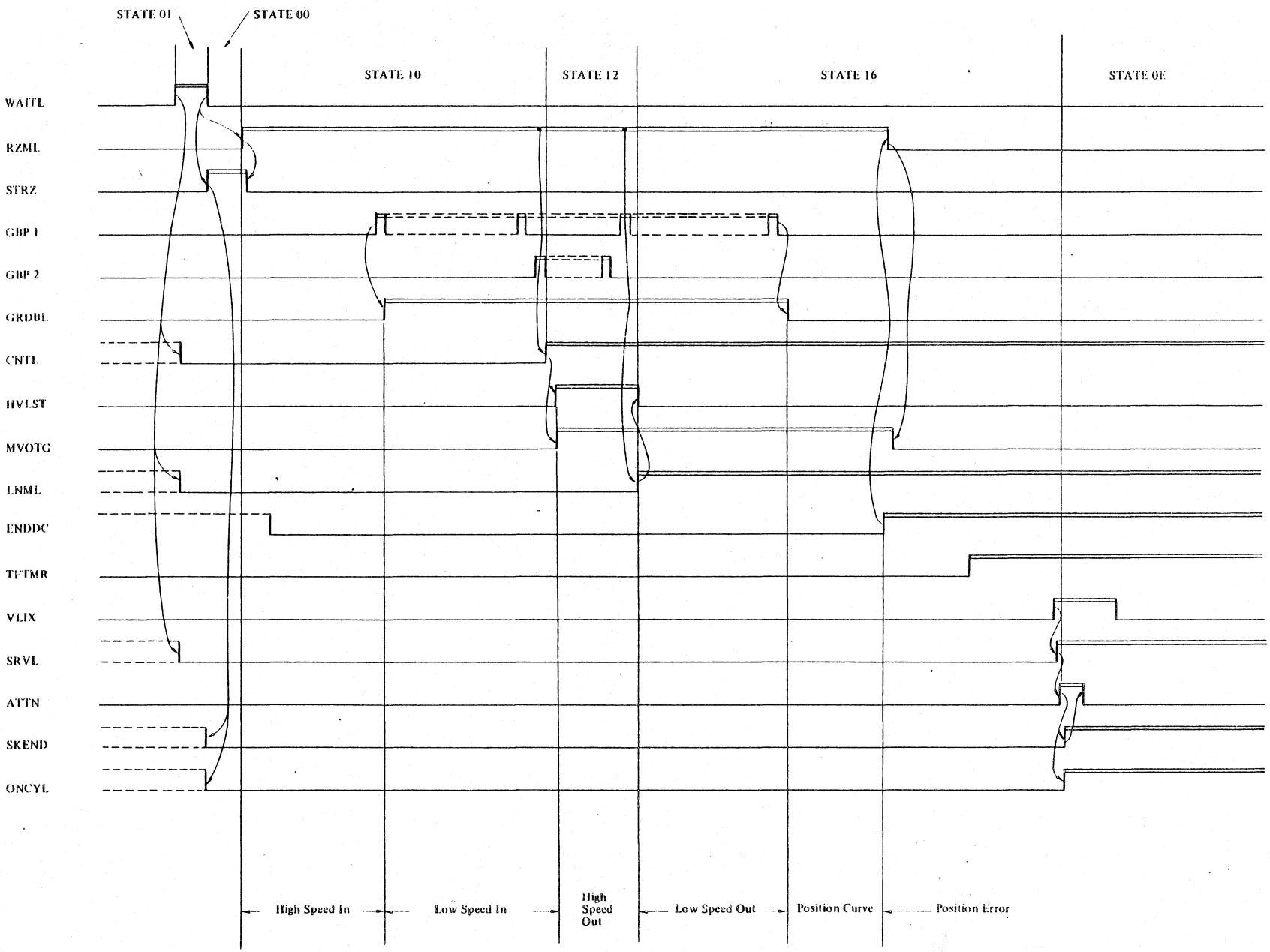


Figure 8.6-3 System/Manual RTZ Sequence (Continued)

8.7 SEEK

The head is moved to the cylinder specified by TAG1/bits 0 - 9 sent from the controller. Figure 8.7-1 shows the timing diagram.

(1) State 0A (Accelerate)

When TAG1 goes high, the contents of bits 0 to 9 are set in the new cylinder address register (NCAR). The address of the cylinder on which the head is currently located is stored in the present cylinder address register (PCAR). The difference between the address stored in the NCAR and that in the PCAR is calculated and is output in the binary code (D1 - D128). If the difference is 144 or greater (NCAR - PCAR > 144), D1 - D128 is set to a value of all 1 bits and is sent to the servo control circuit. The servo control circuit forms the desired speed curve according to the value indicated by D1 - D128.

If the value indicated by the NCAR is greater than that indicated by the PCAR, Move Out Gate (MVOTG) is set high to cause the head to be moved in the outer direction; conversely, if the value indicated by the NCAR is smaller than that indicated by the PCAR, MVOTG is set low to cause the head to be moved in the inner direction.

Then, when TAG1 goes low, Set CAR Off Pulse (SCAROFP) is set high, SKEND, ONCYL, TFTMR, and LNML are set low, and Access Mode (ACCMD) is set high.

The servo control circuit moves the head according to the desired speed curve and generates Track Crossing Pulse (TRXGP) whenever the head crosses a cylinder. TRXGP is sent to the PCAR to increment the register when the head is moved in the outer direction, or to decrement the register when the head is moved in the inner direction. Thus, the output of the difference counter (D1 - D128) is decremented by one at a time.

(2) State 08 (Decelerate)

If the head is moved at a speed higher than that indicated by the desired speed curve, the servo control circuit generates End Accelerate (ENDAC) and sets CNTL low. The speed of the head is then reduced so that the head is moved according to the desired speed curve.

(3) State 0C (Seek Linear Mode)

When the head detects On Cylinder at the desired cylinder (NCAR=PCAR), the servo control circuit generates End Decelerate (ENDDC) and, at the same time, starts the 2.5 ms-timer and sets LNML high. Then, the operation mode of the head is changed from the position curve control mode to the position error control mode.

(4) State 0E (On Track)

If the head is on the desired track when the operation of the 2.5 ms-timer is ended, TFTMR is set high. CNTL is set high and, at the same time, SKEND and ONCYL are set high. This means that the seek operation is terminated. When a no-motion seek command is issued from the controller, the 5 µs-timer is activated and, at the completion of the timer, SKEND and ONCYL are set high.
If an illegal cylinder address is sent (a value greater than 842 for M2351A, or a value between 842 and 895 for M2351AF, SKER and SKEND are set high after about 5 µs. If the seek operation is not terminated normally, that is, if the seek operation is not terminated within 250 ms (TMOCK), or if the Inner or Outer Guard Band are detected during the seek operation, or if TRXGP is detected three times or more after the head is reached to the desired cylinder (OVSCK), SKER and SKEND are set high.

When SKER is set high, the head is released.

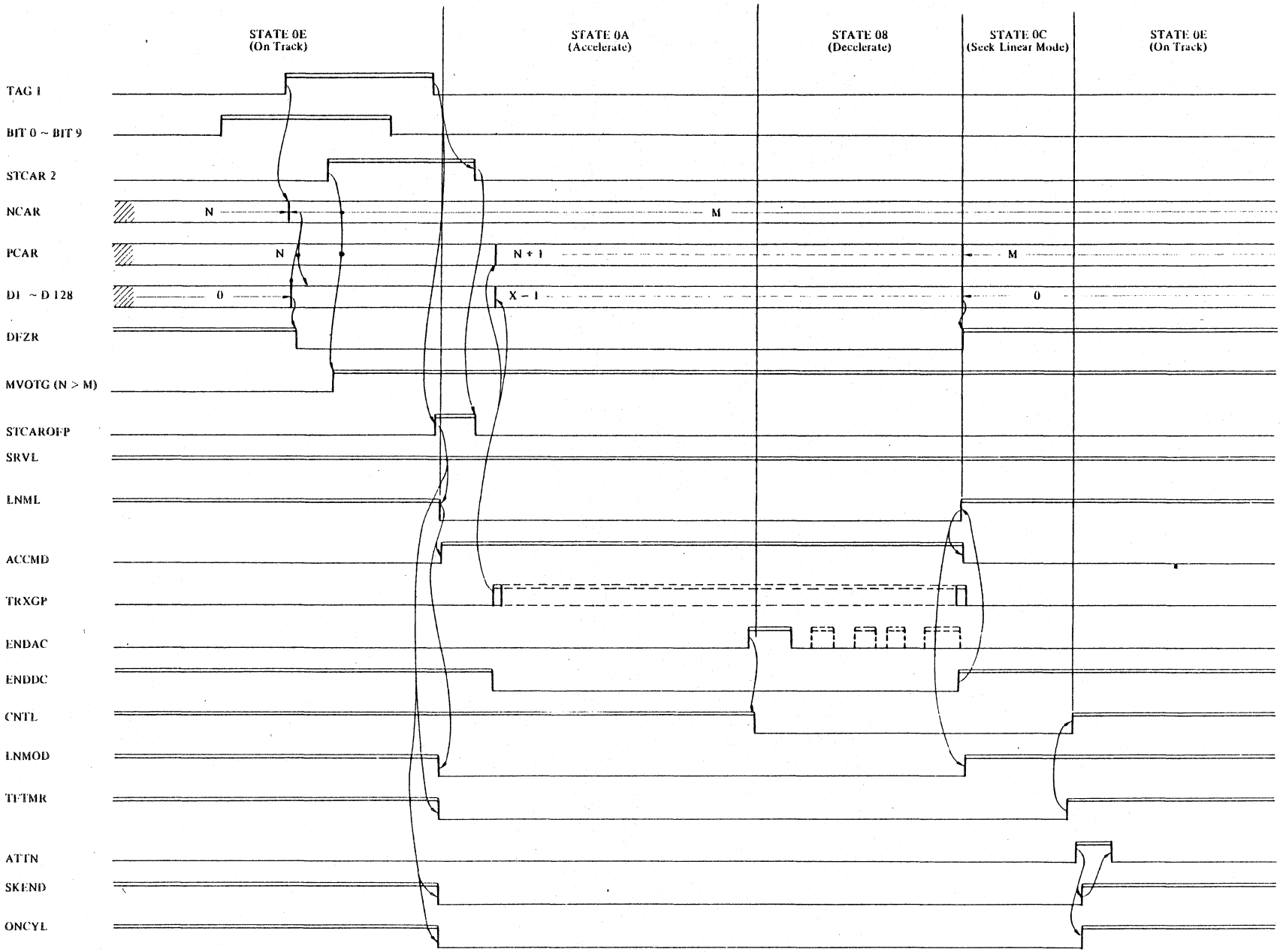


Figure 8.7-1 Seek Sequence

8.8 OFFSET

The head being at the center of a track (On Track) is moved 100μ inches in the direction specified by bit 2 or 3 of TAG3 sent from the controller. The fine control method is used in this operation mode. Figure 8.8-1 shows the timing diagram.

While the drive is selected (SLCT), Offset Plus (OFSTP) is set high when bit 2 of TAG3 is set to 1 by the controller and, at the same time, Offset Out (OFSOT) is set high. If the drive is not in the abnormal condition (ABN) at this time, Offset Active (OFACT) is set high and, at the same time, Difference 16 (GD16) is set high. Then, the servo control circuit moves the head in the outer direction; i.e., the servo control circuit starts the offset operation and moves the head to the location 100μ inches outward of the on-track position. This operation is terminated within 5 ms.

When OFACT goes high, Offset Active Pulse (OFACP) is set high and the 5 ms-timer is started (M5MS). At the same time, Seek End (SKEND) and On Cylinder (ONCYL) are set low. SKEND and ONCYL are set high when the timer operation is terminated.

When bit 3 of TAG3 is set to 1, Offset Minus (OFSTM) is set high and, by holding OFSOT low, the head is moved in the inner direction.

When bit 2 or bit 3 of TAG3 is set to 0 and OFSTP, OFSTM, OFSTA, and GD16 are set low, the head is returned to the on-track position. This operation is terminated within 5 ms.

When OFACT goes low, OFACP is set high, the 5 ms-timer (M5MS) is started and, at the same time, SKEND and ONCYL are set low. When M5MS goes low, SKEND is set high and, if the head is at the on-track position, ONCYL is set high.

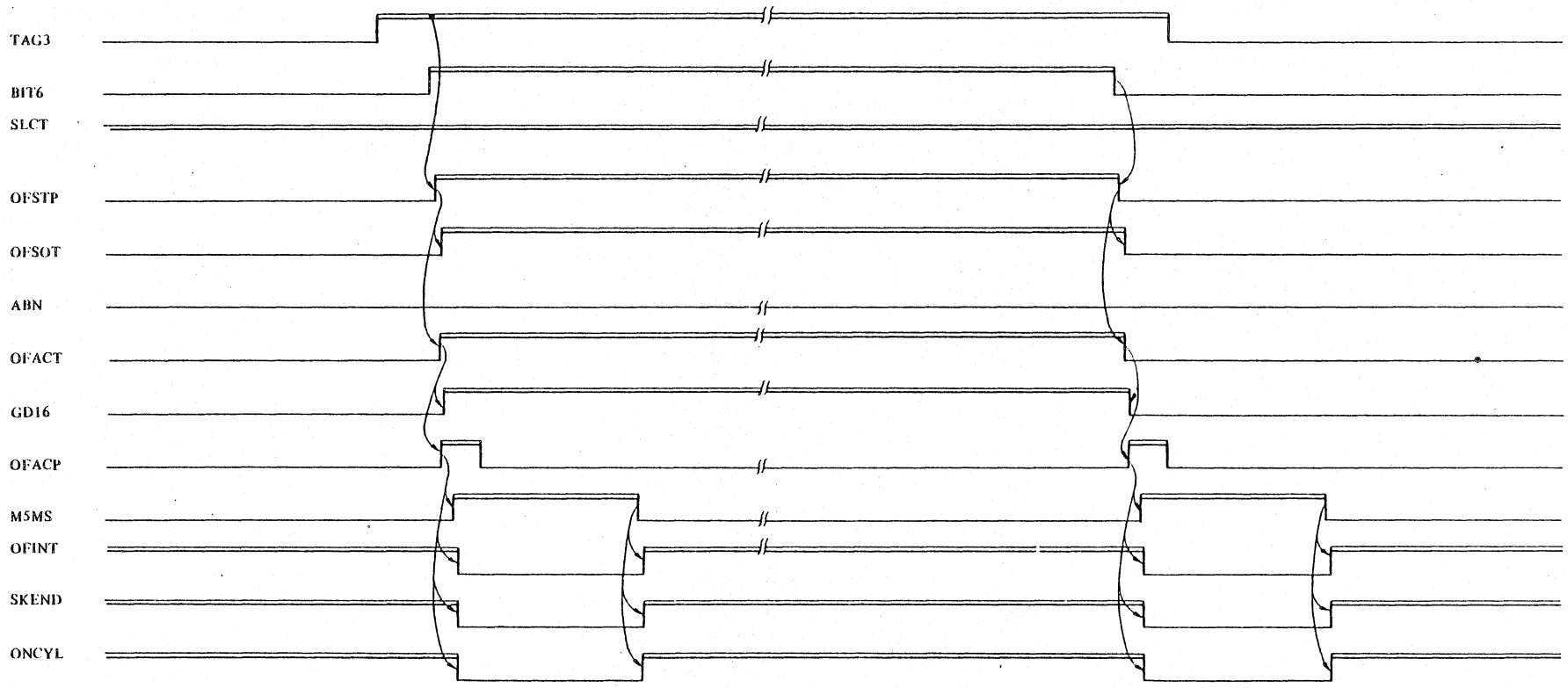


Figure 8.8-1 Offset Sequence

8.9 FAULT AND ERROR DETECTION

Faults and errors detected in the drive are displayed by the maintenance - aid LEDs on the indicator unit (HGAMU; B16B-7830-0010A#U) and reported to the controller through the interface lines.

(1) Fault Register

If the following errors occur, the Fault register will be set and Fault line will be enabled.

Table 8.9-1 Write/Read Check Conditions

No.	Write/Read Check State	Conditions	State 1	LP
1	Index Check	(RG+WG)•IDXCK	Bit 1	LP1
2	Control Check	RG•WG OFACT•WG RONLY•WG	Bit 2	
3	Multi-Head Check	(RG+WG)•MCPSL	Bit 4	
4	Head Short Check	(RG+WG)•HDSHT	Bit 8	
5	Write Current On Read Check	RG•MUSFV	Bit 1	LP2
6	Write Transition Check	WG•$\overline{\text{AMCTL}}$•MUSFV	Bit 2	
7	Delta I Write Check	WG•DIECK	Bit 4	
8	Servo Off-Track	WG•$\overline{\text{RWCAP}}$•($\overline{\text{URDY}}$+$\overline{\text{TFTMR}}$+ACCK) RG•$\overline{\text{EQUAL}}$•	Bit 8	

These fault status can be cleared by one of the followings;

① Depressing the Fault Clear switch on the operator panel

② Fault Clear signal sent from the controller

(2) Seek Check Latch

If seek error occurs in the drive, the error will set Seek Check Latch, enabling Seek Error to the controller, and light the mainteance-aid LED.

Table 8.9-2 Seek Error Fault Conditions

No.	Access State	Conditions	State 3	LP
1	Access Timeout Check	Timeout in direct or RTZ seek	Bit 2	LP1
2	Over Shoot Check	Any Guard Band in direct seek, or Over track-crossing pulse in settling	Bit 4	

CHAPTER 9 SERVO CIRCUIT

The following explains the servo format and how the head positioning control circuit operates:

The seek control operation and the rezero seek control operation are outlined first, followed by the function of each component of the head positioning control circuit, and the spindle motor control method.

9.1 DATA AND SERVO ZONE

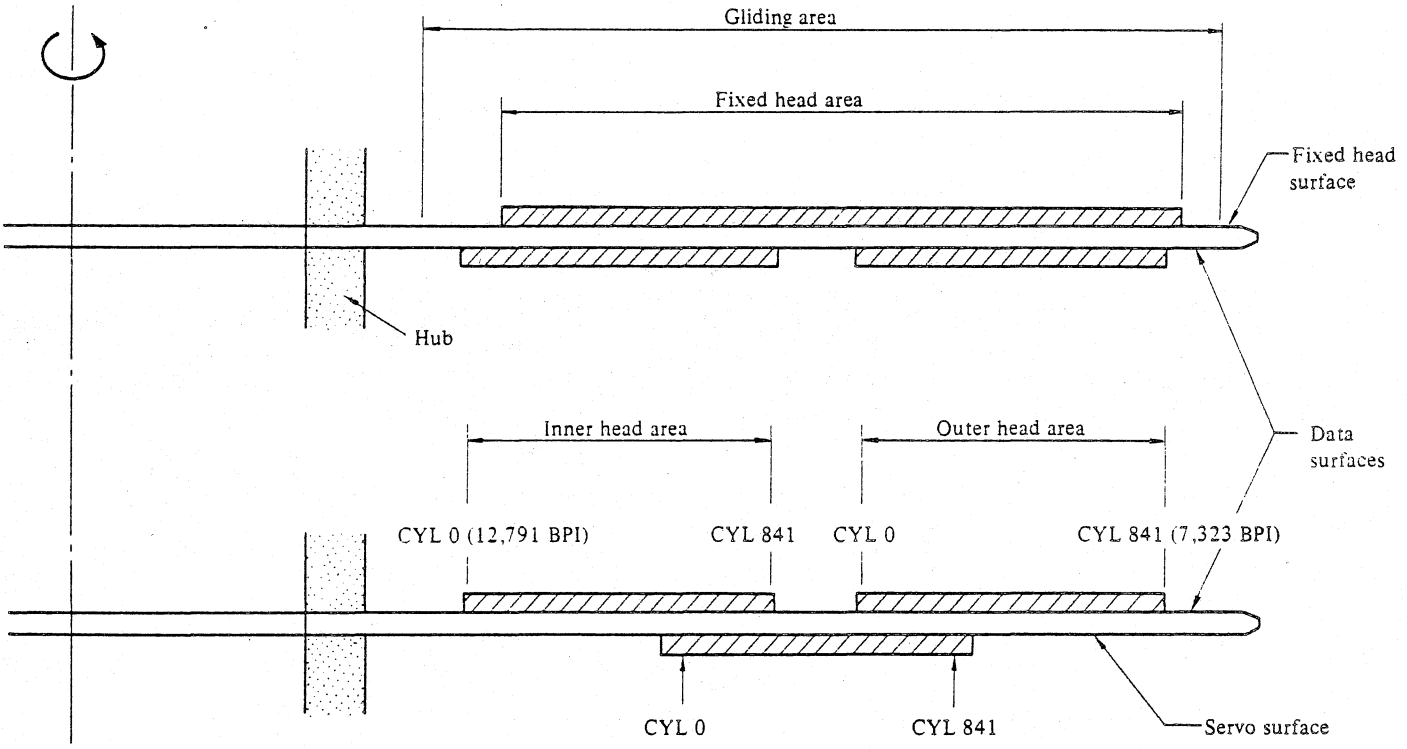


Figure 9.1-1 Data and Servo Area Locations

Though the rotational angle of arm assemblies is constant for all tracks (2.27×10^{-4} radians per track), the track pitch for the servo, inner, and outer R/W heads varies as shown in Figure 9.1-2 depending on the mechanical arrangement of the head-arm and the cores.

The track width of the inner R/W head is made wider than that of the outer R/W head to avoid decrease of time margin for the read operation.

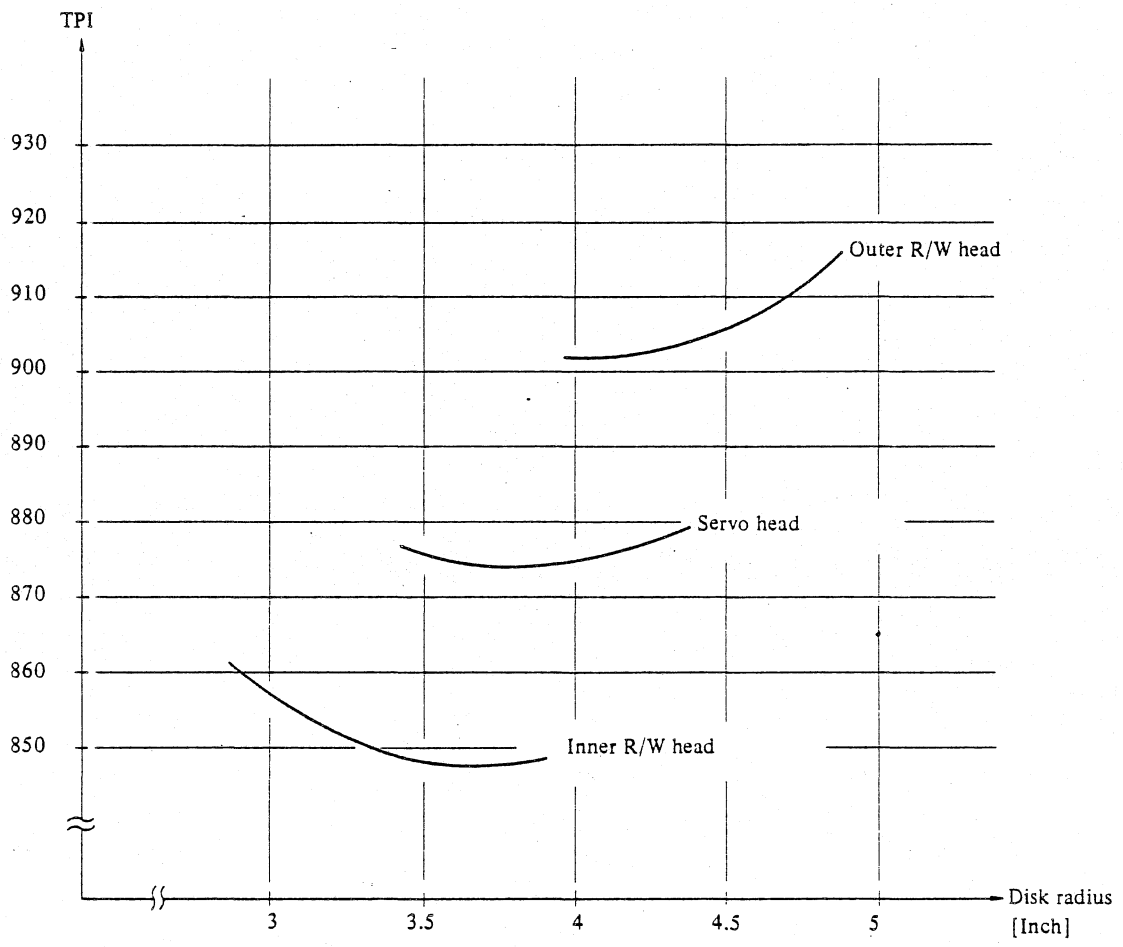


Figure 9.1-2 Track Pitch

9.2 SERVO FORMAT

The two-phase composite servo signal is pre-recorded on the bottom servo surface. This signal is read by the servo head, and the index signal, sector count clock signal, read/write PLO signal, and two types of position signals, 90 degrees out of phase with each other, are generated. The two-phase servo signal makes the effective track width of the servo signal (29μm), one-half of the actual track width (58μm).

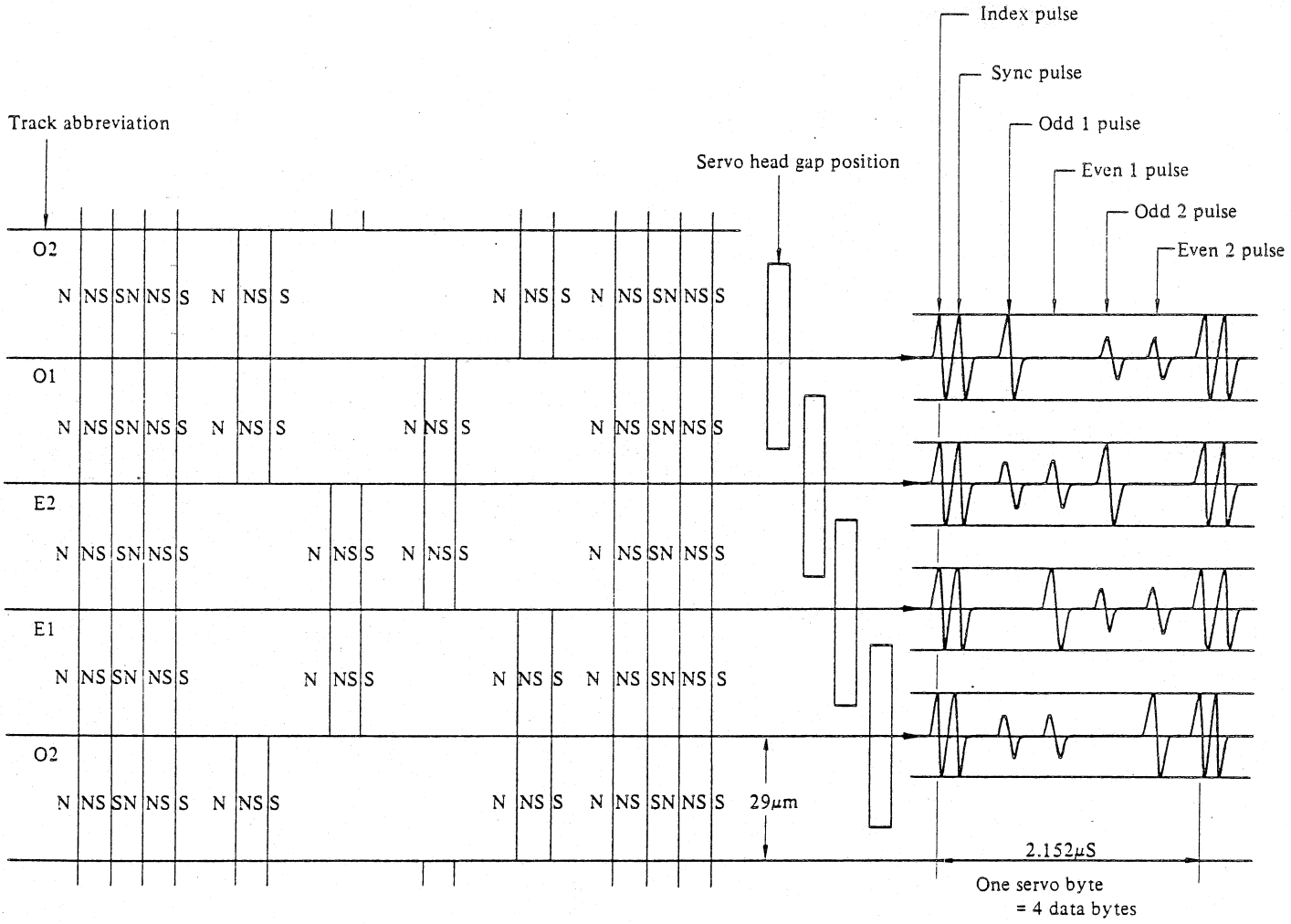
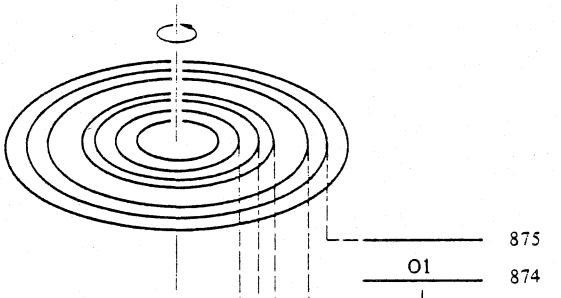
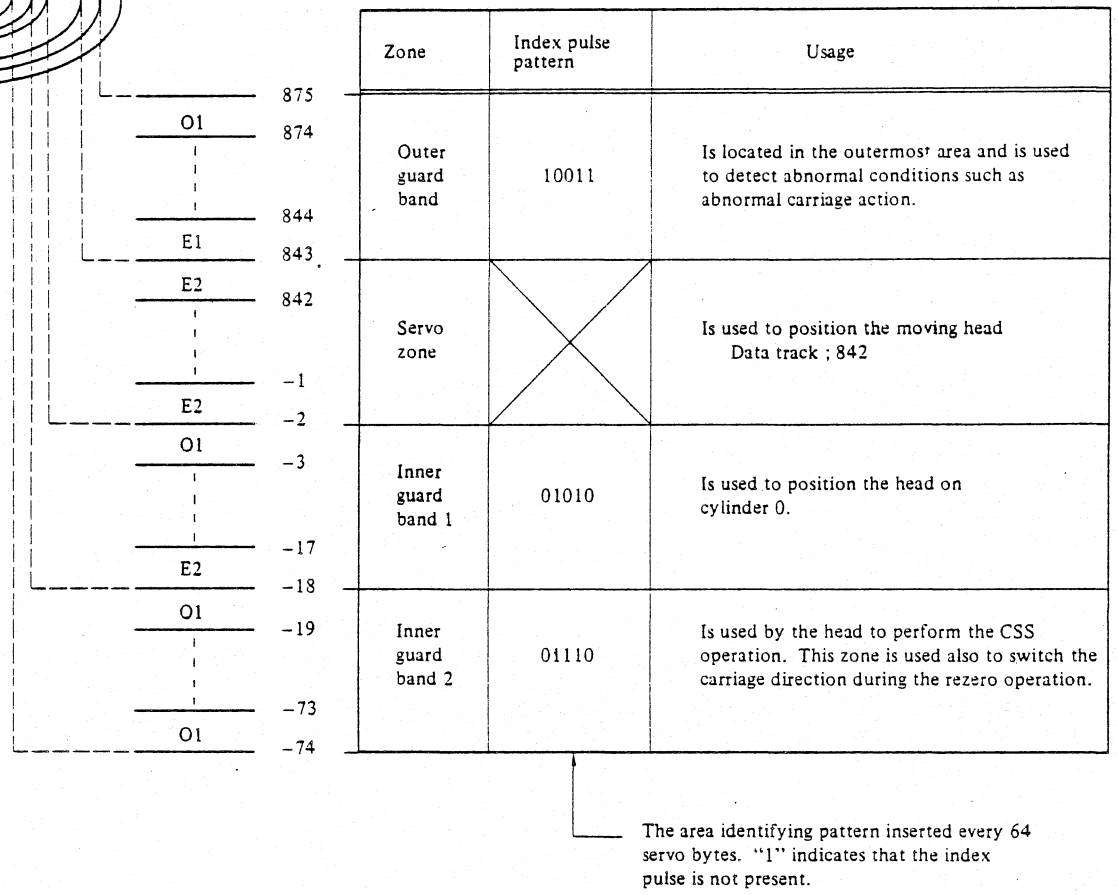


Figure 9.2-1 Magnetized Pattern of Two-phase Servo Signal and Read Signal





Zone	Index pulse pattern	Usage
Outer guard band	10011	Is located in the outermost area and is used to detect abnormal conditions such as abnormal carriage action.
Servo zone		Is used to position the moving head Data track ; 842
Inner guard band 1	01010	Is used to position the head on cylinder 0.
Inner guard band 2	01110	Is used by the head to perform the CSS operation. This zone is used also to switch the carriage direction during the rezero operation.

The area identifying pattern inserted every 64 servo bytes. "1" indicates that the index pulse is not present.

Figure 9.2-2 Zone Allocation on Servo Surface

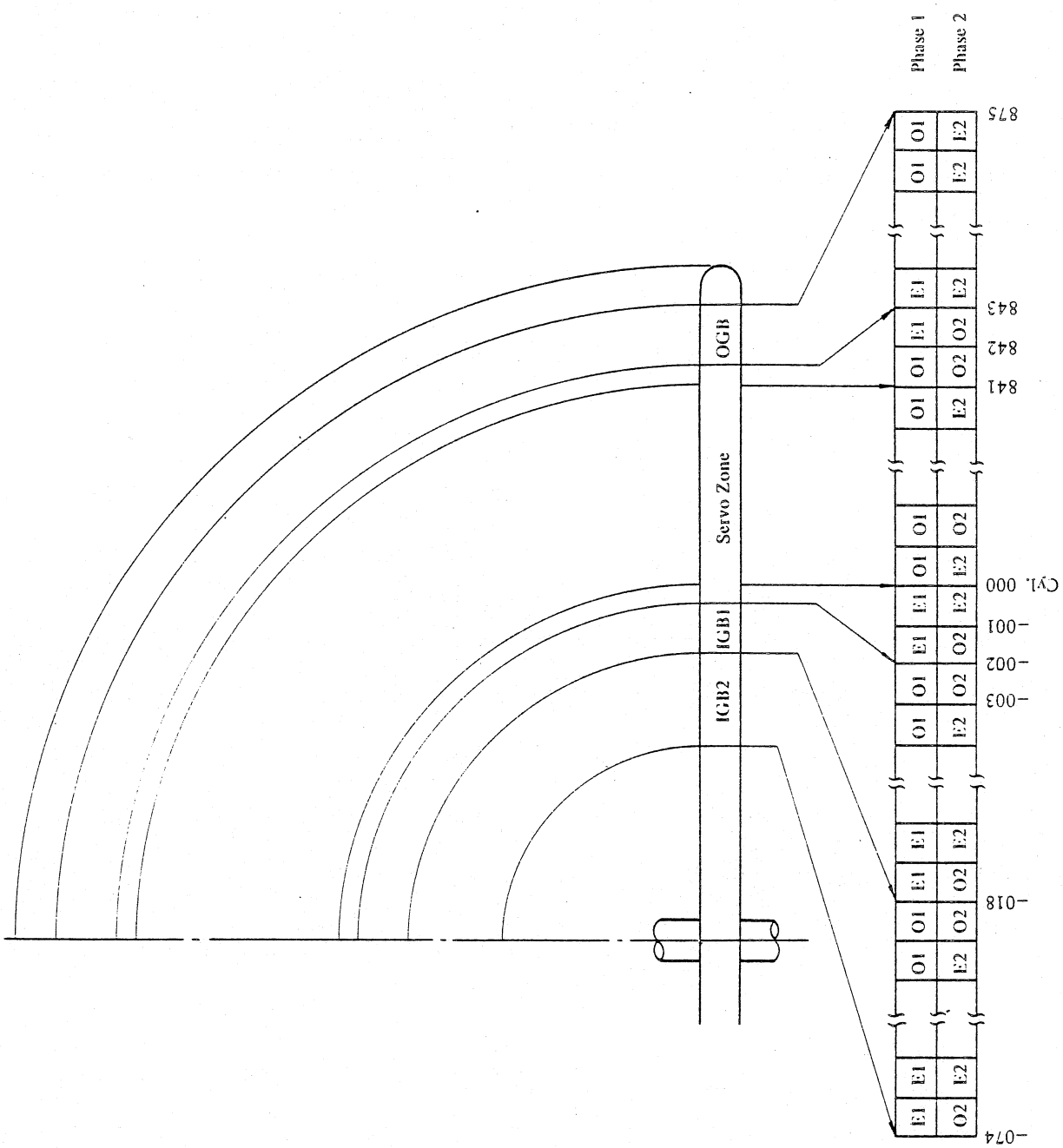
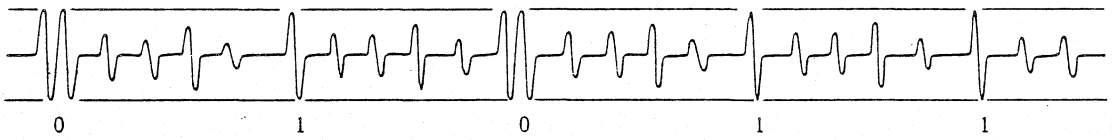


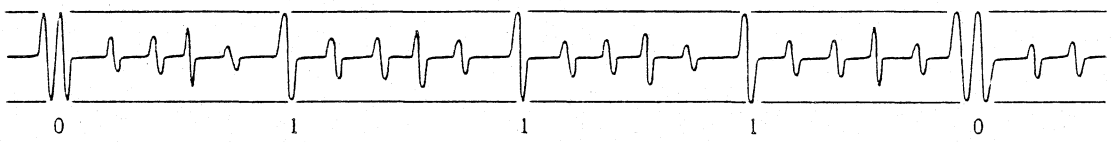
Figure 9.2-3 Servo Track Configuration

Index pulse pattern

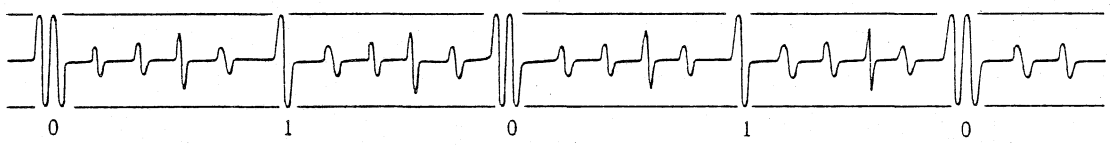
Each area is identified by the index pulse (0:present, 1: sbsent) preceding the sync pulse. The valid index pattern, detedted once per rotation, indicates the physical starting point. Inner Guard Band 1 and 2 and the Outer Guard Band are written every 64 servo bytes; this means that there are 110 locations at which these patterns are written. However, if any of the 110 locations coincides with the location at which the valid index pattern is written, the valid index pattern is effective.



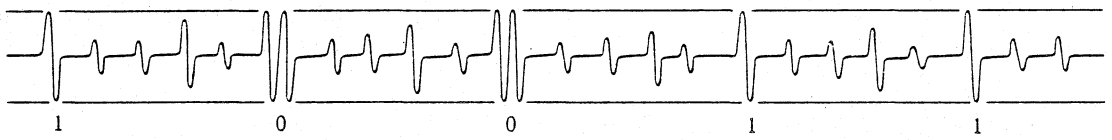
Valid index pattern



Inner Guard Band 2 pattern



Inner Guard Band 1 pattern



Outer Guard Band pattern

Figure 9.2-4 Index Pulse Pattern

9.3 SEEK CONTROL OPERATION

The seek control operation is classified roughly into the coarse control operation and fine control operation.

(1) Coarse control operation

The coarse control operation is performed to move the head to the desired cylinder position. That is, the head is moved with a speed feedback loop at a high speed by comparing the target speed, derived from the position difference between the desired position sent from the logic circuit and the actual position, with the actual speed derived from the position signal read from the servo surface with the servo head.

The speed is decreased as the position defference is reduced and, when the head reaches near the neighborhood of the desired cylinder, the speed becomes very slow.

(2) Fine control operation

When the head reaches near the desired cylinder and the defference between the desired position and the current position is within the specified range (on track), the coarse control operation is switched to the fine control operation. During the fine control operation, the position signal is fed back to ensure that the head is always on the desired cylinder notwithstanding mechanical vibration and temperature change.

The speed signal is used as the damping factor. The signal generated by integrating the position signal is also used to increase stiffness.

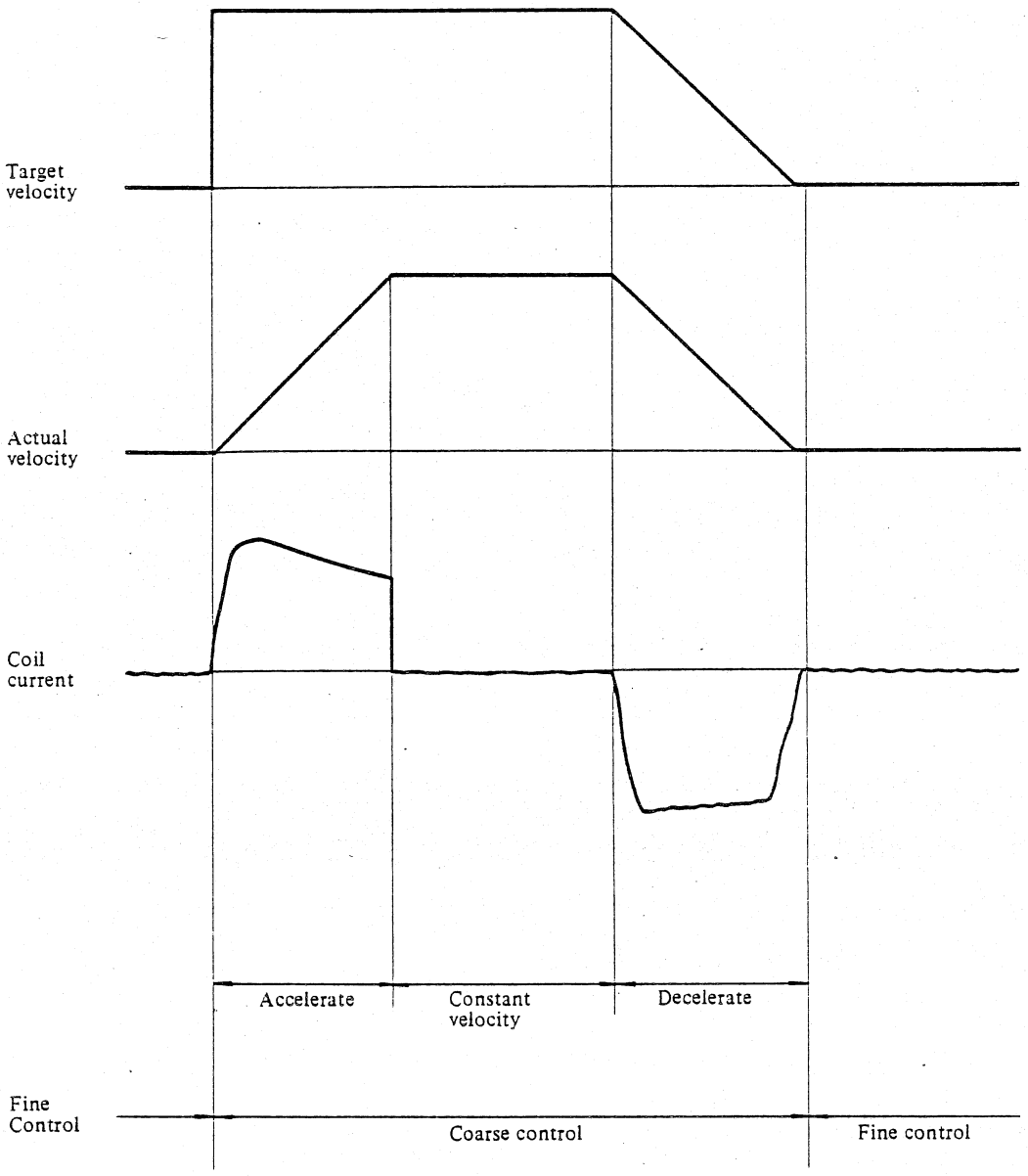


Figure 9.3-1 Seek Control

9.4 REZERO CONTROL OPERATION

The head is returned to the reference cylinder (cylinder 0). The rezero seek operation is classified into the coarse control operation and the fine control operation as with the seek control operation; however, unlike the seek control operation, the target speed is determined by the signal generated by the reference voltage. The following explains how the rezero seek operation is performed, assuming that the head is not in the Inner Guard Band.

(1) High Speed In (HSPIN)

The head is moved in the inner direction about 8 inches per second until Inner Guard Band 1 (IGB1) is detected.

(2) Low Speed In (LSPIN)

The head is moved in the inner direction at about 2.5 inches per second between the moment when IGB1 is detected in the neighborhood of cylinder-2 (minus 2) and the moment when Inner Guard Band 2 (IGB2) is detected.

(3) High Speed Out (HSPOT)

The direction in which the head is to be moved is inverted, and the head is moved in the outer direction at about 3.5 inches per second between the moment when IGB2 is detected in the neighborhood of cylinder-18 (minus 18) and the moment when IGB1 is detected.

(4) Low Speed Out (LSPOT)

The head is moved in the outer direction at about 0.8 inches per second after being returned to IGB1.

(5) Rezero Out (RZOUT)

When the head enters the servo zone from IGB1 after it travels in the neighborhood of cylinders-2 (minus 2), the head is moved to cylinder 0 with the target speed signal generated from the position signal.

(6) Fine control

After On Track is detected when the head is in the neighborhood of cylinder 0, the Position control is performed in the same manner as the seek contol operation.

The rezero operation is performed from (2) if the head is to be returned from IGB1, or from (3) if the head is to be returned from IGB2; after that, the same control method is performed until the head is positioned on cylinder 0.

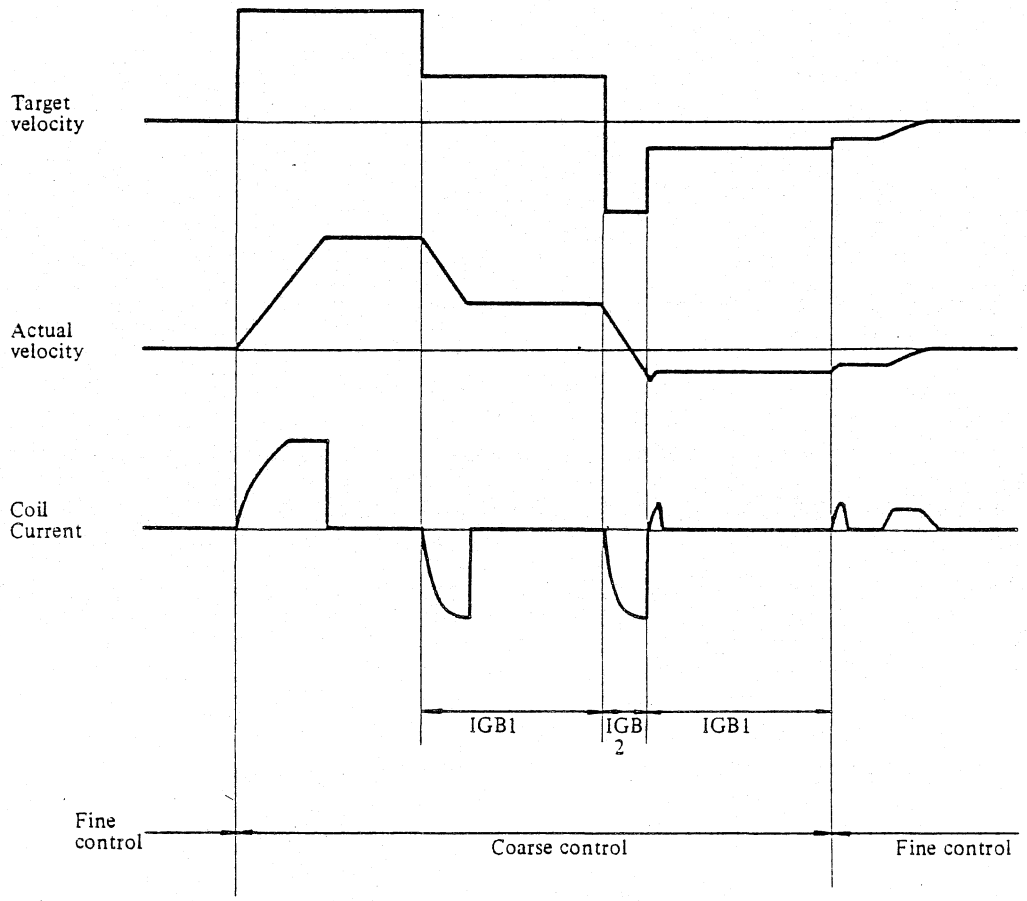


Figure 9.4-1 Rezero Control

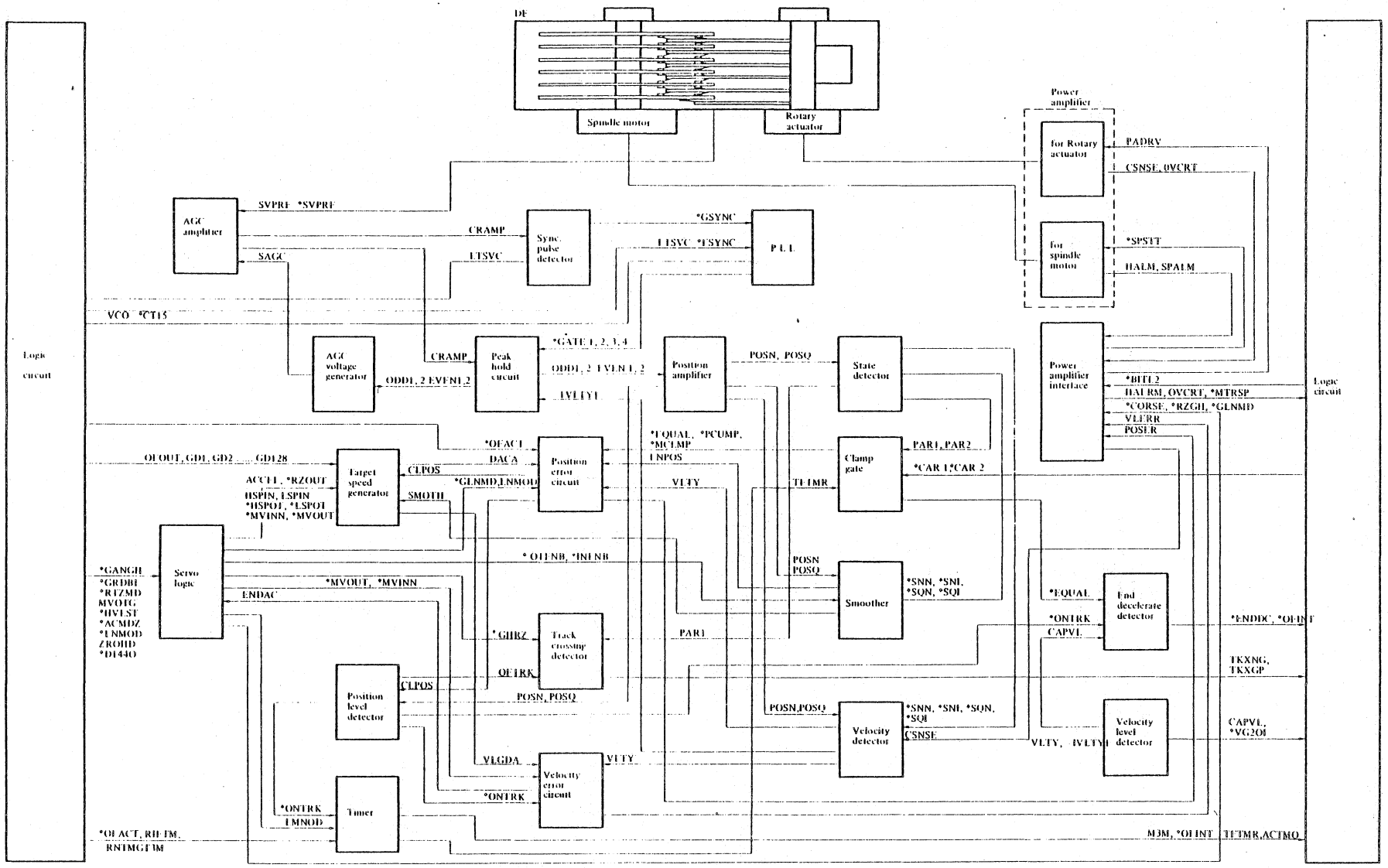


Figure 9.5-1 Servo Block Diagram

(1) AGC amplifier

The AGC amplifier amlifies the output signal from the servo head (SVPRE and *SVPRE) to generate the carrier amplifier signal (CRAMP). The amplifier gain is controlled by the output (SAGC) of the AGC voltage generating circuit to compensate for level fluctuation on the servo surface.

(2) Peak hold circuit

The peak hold circuit receives gate signals (*GATE1 - 4) from PLL to sample ODD1, EVEN1, ODD2, and EVEN2 pulse from the output of an AGC amplifier (CRAMP).
This circuit uses the output (-|VLTY|) from the speed detect circuit in order to vary the descharge time constant of the sampling curcuit according to the head travelling speed.

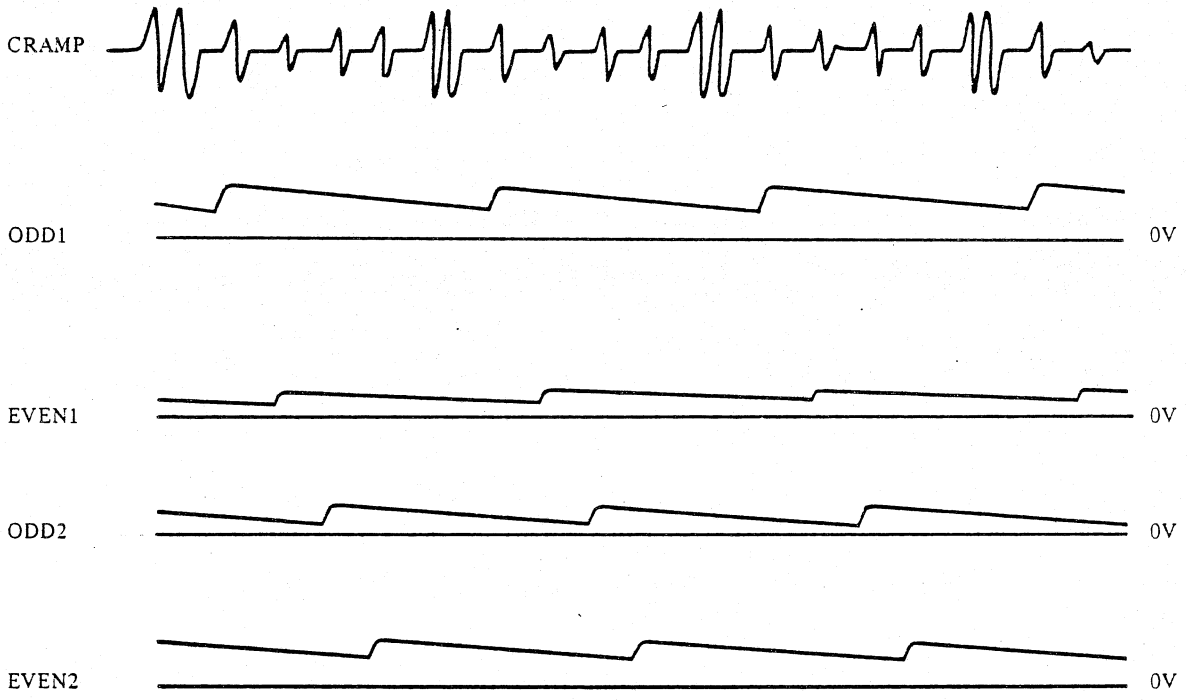


Figure 9.5-2 Peak Hold Circuit

(3) AGC voltage generator

This circuit generates the AGC amplifier gain control signal SAGC by means of ODD1, EVEN1, ODD2, and EVEN2 which are generated by the peak hold circuit. If the output voltage of the servo head falls due to variations in the level of the signal read from the medium, the amplitude of the carrier amplifier output decreases and the output voltage of the peak hold circuit falls, lowering the SAGC voltage. When the control voltage SAGC of the AGC amplifier falls, the gain is increased to compensate for the drop in the output voltage level of the servo head. Conversely, when the output voltage rises, it is compensated for in the same manner.

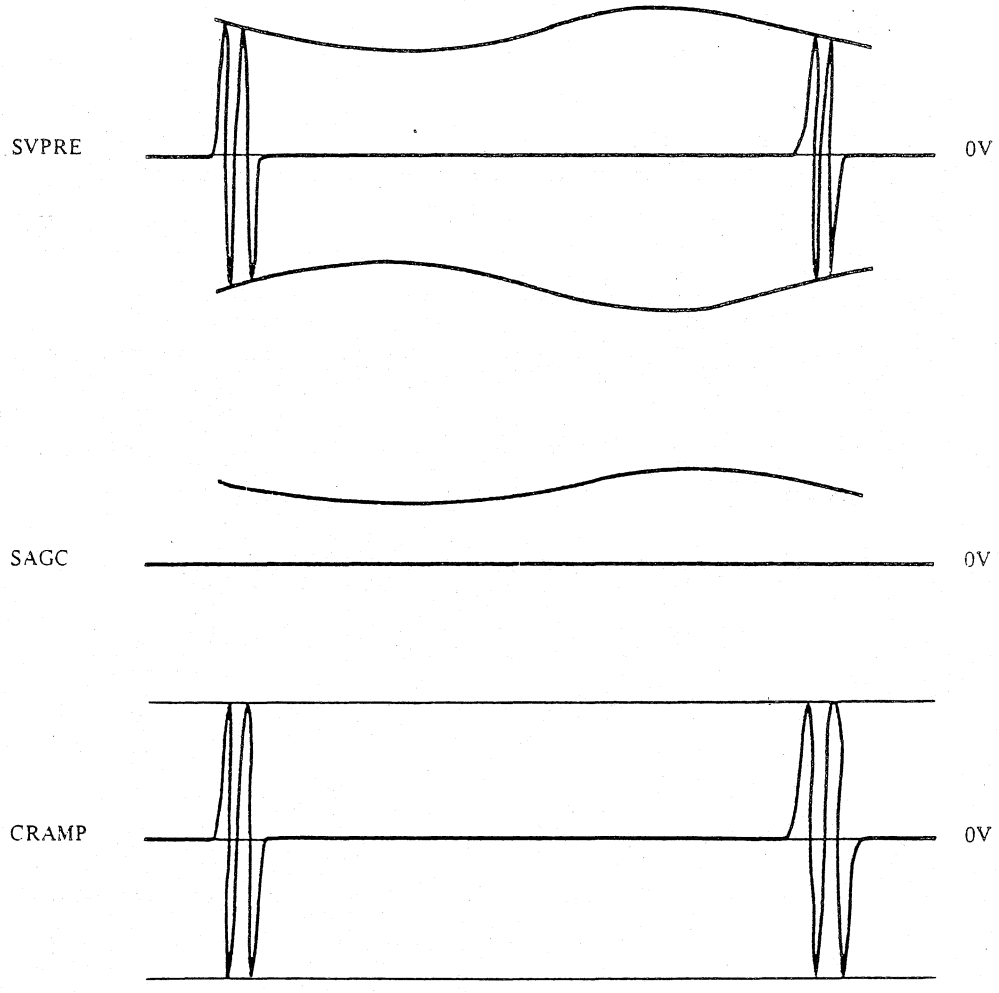


Figure 9.5-3 Function of AGC

(4) Sync pulse detector

The gated sync pulse signal (*GSYNC) is generated using the signal generated by slicing the carrier amplifier signal (CRAMP). *GSYNC is absent at the locations where the index pulses in the valid index pattern and the Guard Band patterns are written. This signal is used for the VCO and logic circuits to detect patterns.

*GSYNC is generated by ANDing TP4 and the LTSVC signal generated by the logic circuit.

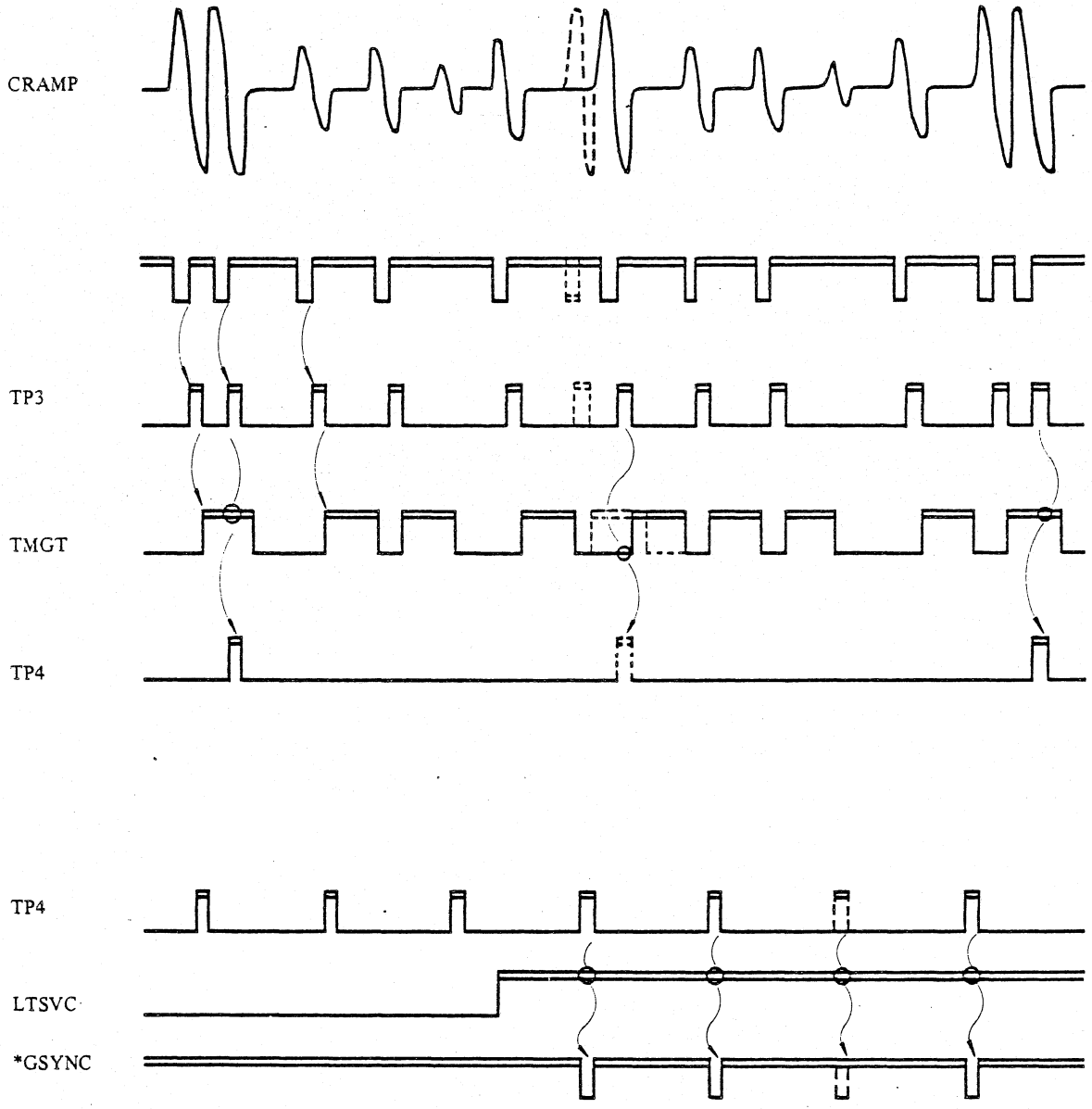


Figure 9.5-4 Detection of Sync Pulse

(5) PLL

The PLL circuit, consisting of the phase detector, charge pump, VCO, counter, and decoder, generates gate signals uded to sample ODD1, ODD2, EVEN1, and EVEN2 of the carrier amplifier. Even in the area where the index pulse is absent, the circuit generates gate signals.

- Phase detector

This circuit detects the difference in phase between *CT7, generated by VCO which devides *GSYNC by 16, and *GSYNC. It outputs *INC or *DEC according to a shift in phase.

- Charge pump

The charge pump raises or lowers the PLO analog (PLOAN) voltage depending on the signal from the phase detector (*INC/*DEC). The output voltage of PLOAN is 0 when the disk is rotating at the specified constant speed.

- VCO, counter, and decoder

The VCO converts the DC voltager to the pulse oscillation frequency. The PLOAN voltage is proportional to the oscillation frequency. When the disk is rotating at the specified speed, the oscillating frequency of the VCO is 7.44 MHz, 16 times as high as the frequency of *GSYNC. The output of the VCO is sent to the logic circuit and counted by the four-bit binary counter. The output of the counter is decoded and *CT7 is sent to the phase detector and *GATE1 - *GATE4 to the peak hold circuit. *CT15 is sent to the logic circuit to detect the valid index pattern and Guard Band Patterns.

(6) Position amplifier

The position amplifier generates POSN by the difference between ODD1 and EVEN1, and POSQ by the defference between ODD2 and EVEN2. These two position signals are 90 degrees out of phase with each other.

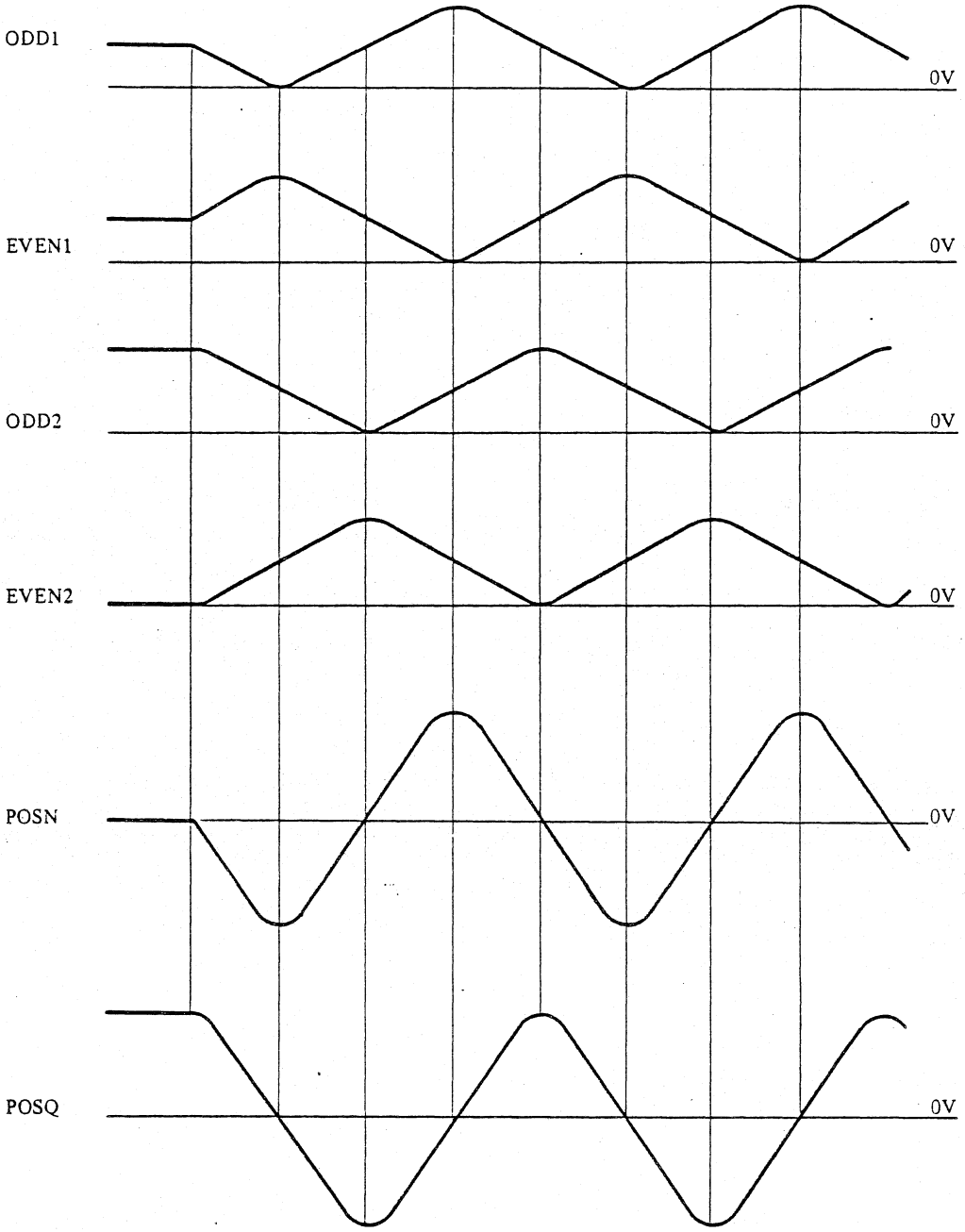


Figure 9.5-5 Position Signals

(7) State detector

The state detect circuit detects the low-order two bits of the present head position by two position signals, POSN and POSQ.

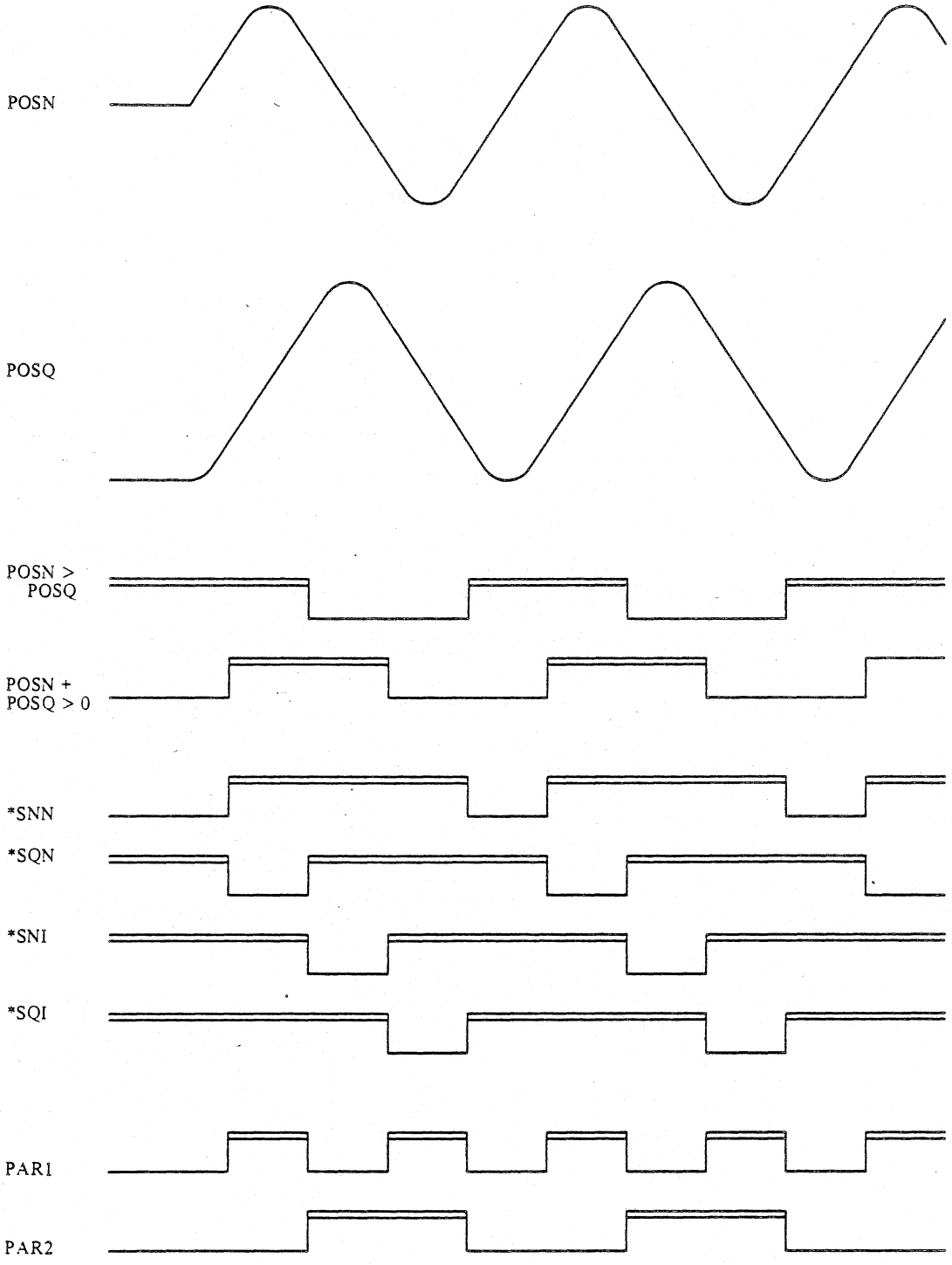


Figure 9.5-6 State of Position Signals

(8) Smoother

The position signal (FNPOS) for fine control is generated by selecting POSN or POSQ by means of *SNN, *SNI, *SQN, and *SQI generated from the state detect circuit. Switching the polarity of FNPOS according to the carriage movement direction, the interpolation signal (SMOTH) is generated for smoothing the stair step signal from the DA converter.

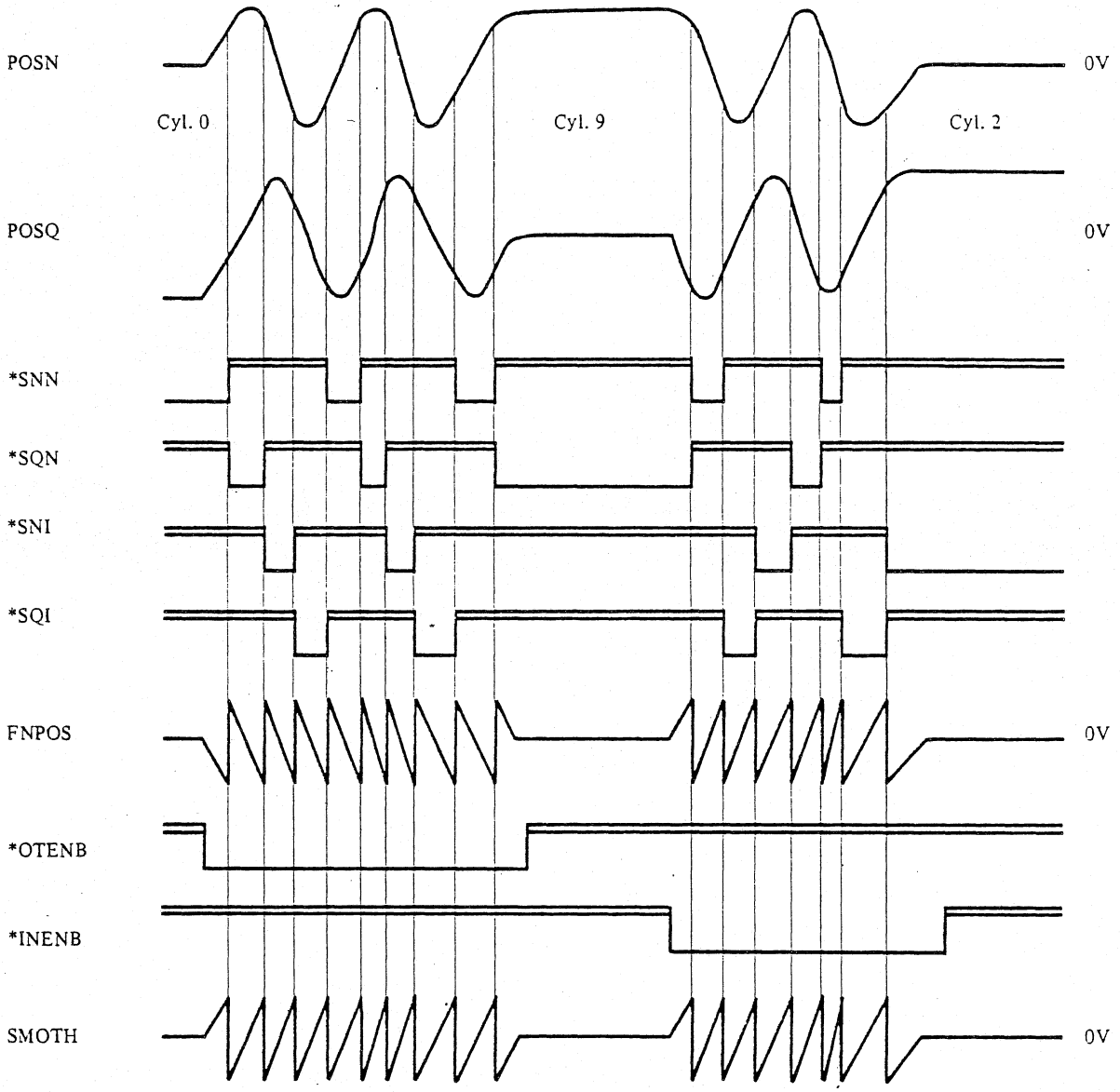


Figure 9.5-7 Output Signal of Smoother

(9) Clamp gate

The clamp gate holds the position signal at the specified level when the signal voltage is higher or lower than the specified level in order to extend the distance over which the head can be controlled. It generates *EQUAL, *PCLMP, and*MCLMP by comparing the low-order two bits of the desired position sent from the logic circuit with the low-order two bits of the present head position sent from the state detect circuit.

(10) Position error circuit

The position error circuit generates the position signal (CLPOS) for position control by means of FNPOS generated from the smoother circuit and *EQUAL, *PCLMP, and *MCLMP signals sent from the clamp gate circuit. It then combines CLPOS and the velocity signal (VLTY) to generate the position error signal (POSER), the error signal for fine control. At offset operation, this circuit combines the output (DACA) from the DA converter with the position signal. Figure 9.5-8 shows how the clamp circuit works when the head is moved from cylinder 0 to cylinder 9 (*CAR1=0, *CAR2=1).

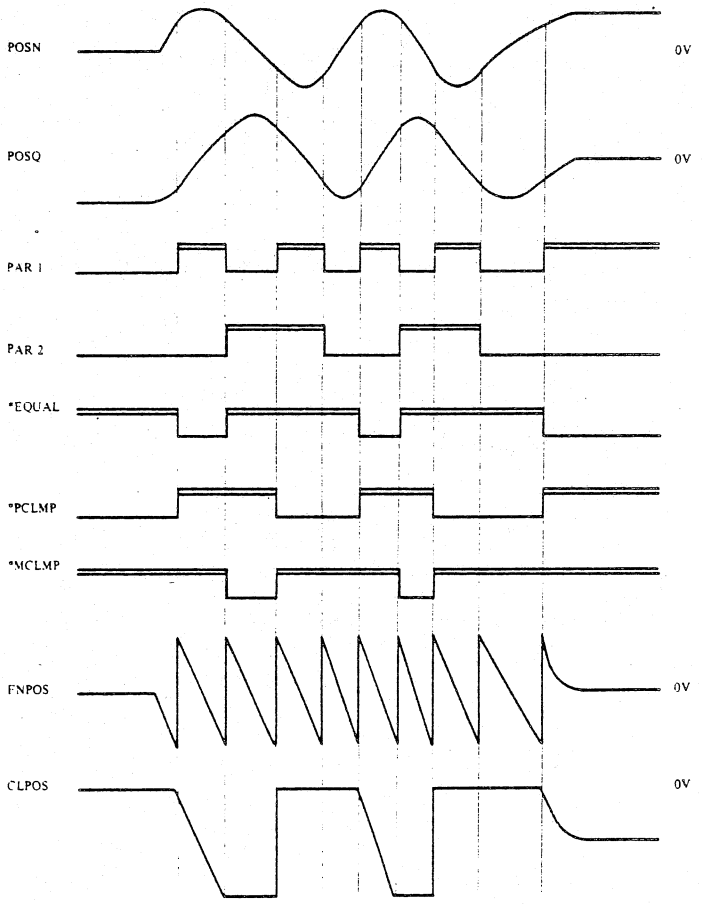


Figure 9.5-8 Clamped Position Signal

(11) Track crossing detector

The track crossing detect circuit generates the track crossing signal (TKXNG) by means of PAR1 sent from the state detect circuit and OFTRK sent from the position level detect circuit. The track crossing pulse (TKXGP) used to decrement the difference counter is generated on the rising edge of TKXGP. At rezero operation, *GHRZ is activated to prevent TDXGP from being generated.

(12) Position level detector

The position level detect circuit generates the off-track signal (OFTRK) by slicing the position signal (POSN, POSQ) and also generates the on-track signal (*ONTRK) by slicing the clamped position signal (CLPOS) output from the position error circuit. OFTRK is used in the circuit which generates the track crossing pulse for decrementing the difference counter in the logic circuit. *ONTRK is used to generate switching signal (*ENDDC) which changes the control method from the coarse control to the fine control, the signal (ENDAC) which indicates the end of carriage acceleration, and the signal (TFTMR) which indicates, after the control is switched to the fine control, that the head is positioned properly.

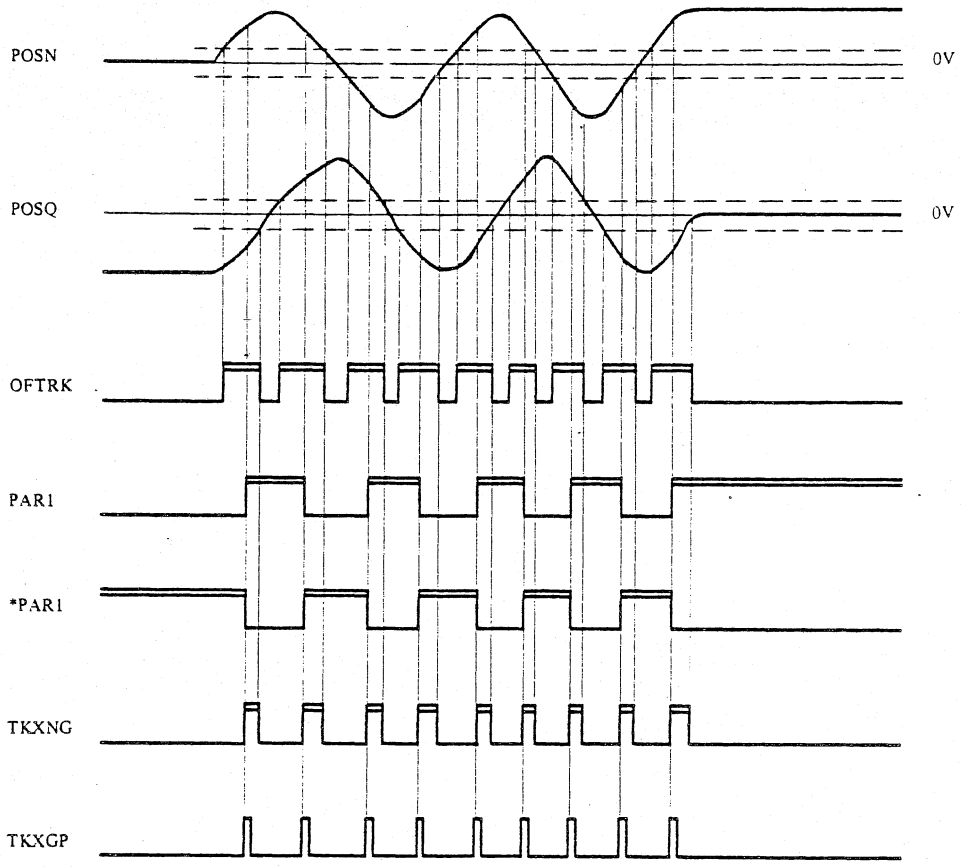


Figure 9.5-9 Position Level Detector

(13) Target speed generator

The target speed generator, consisting of the DA converter, nonlinear circuit, and switching circuit, determines the carriage traveling speed at seek or rezero operation.

- DA converter

The DA converter converts the digital positional difference (held to 144 when the number of remaining cylinders is not less than 144) stored in the difference register (the number of cylinders over which the carriage is to be moved is set and is decremented whenever the track crossing pulse is detected) to the analog stair step waveform which decreases as the carriage approaches the desired cylinder. The DA converter is also used in converting the offset amount (3-bit degital amount) to the corresponding analog voltage at offset operation.

- Non-linear circuit

The nonlinear circuit combines the stair step signal sent from the DA converter with the signal sent from the smoother to smooth the waveform and, at the same time, generates the deceleration curve which is optimum from viewpoints of decelerating current and the access time. In addition, it applies the output from the charge-discharge circuit, which is controlled by the acceleration signal (ACCEL), to prevent excessive accelerating force from being applied to the carriage.

- Switching circuit

The switching circuit selects the target velocity for seek operation, and rezero operation generated based on the reference voltage by means of various logic signals generated by the servo logic circuit.

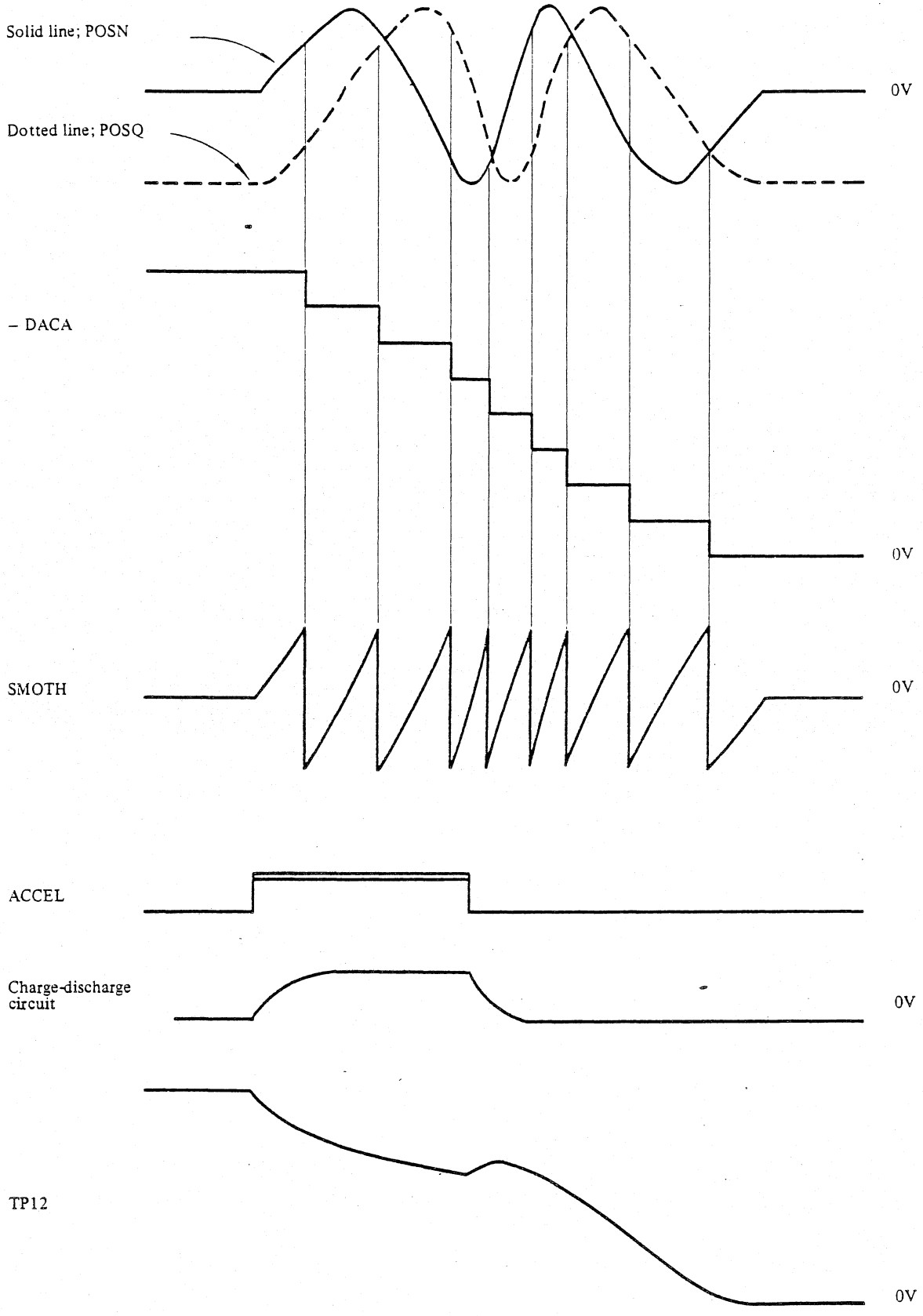


Figure 9.5-10 Target Speed

Figure 9.5-11 is the timing chart of the signals at the rezero operation:

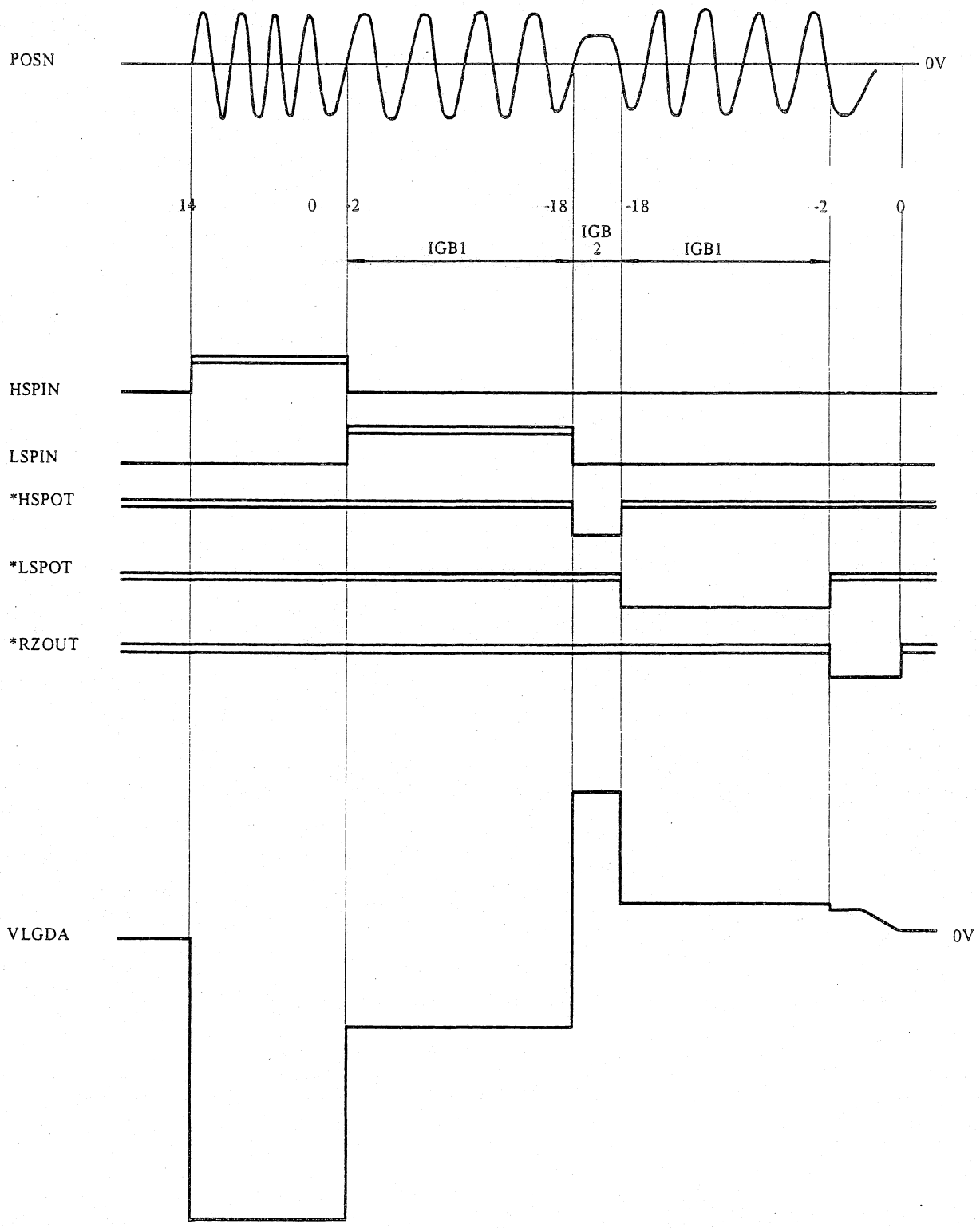


Figure 9.5-11 Signals in Rezero Operation

(14) Velocity detector

The velocity detect circuit generates the velocity signal by composing the differentiated value of the position gignal (POSN and POSQ) for the linear portion with the integrated value of the coil current (CSNSE) in the rotary actuator. The output of the state detect circuit is used to select the linear portion of the position signal.

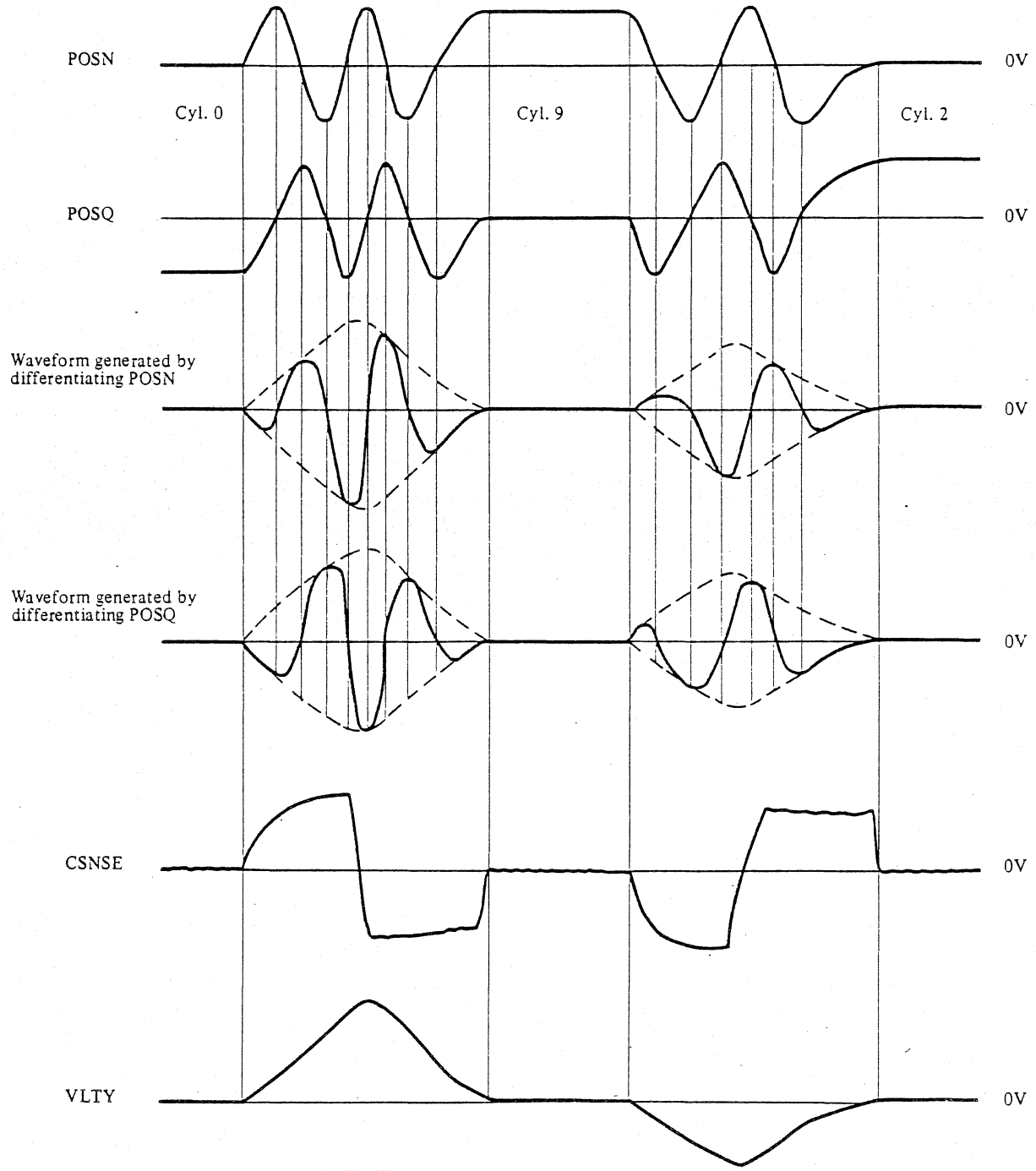


Figure 9.5-12 Velocity

(15) Velocity level detector

The velocity level detect circuit slices the velocity signal (VLTY) and sends CAPVL and *VG20I signal to the logic circuit. CAPVL, which indicates the carriage velocity is lower than the specified value, is used to prevent the rezero operation from being started while the carriage is being moved at high speed and also used to provide switching moment from coarse control to fine control. *VG20I, which indicates the carriage velocity is too high during the rezero operation, is used to monitor the access mechanism.

(16) Velocity error circuit

The velocity error circuit generates the velocity error signal (VLERR) which indicates a difference between the target velocity signal VLGDA and the actual velocity signal VLTY. It also generates, by slicing VLERR, the end accelerate signal (ENDAC) which indicates the end of acceleration.

(17) End decelarate detector

The end decelarate detect circuit generates the end decelerate signal (*ENDDC) which indicates switching of the control mode from the coarse control to the fine control. That is, the circuit generates *ENDDC after the specified time has elapsed from the moment *ONTRK goes low and *EQUAL is low. At this time, CAPVL is used to indicate that the velocity is lower than the specified velocity.

(18) Timer

The timer is used to generate the track following timer signal (TFTMR) which informs the logic circuit that the access operation has been completed normally after the specified time period from the moment the control mode had been switched to the fine control or, it sends the access timeout signal (ACTMO), which indicates that the opration has not been completed within the specified time period after the start of movement. It also provides the time setting signal (M3M, *OFINT) to be used during an offset operation.

(19) Reference voltage generator

The reference voltage generator generates -4V and +6V reference DC voltages to be supplied to the head IC on the servo head assembly. They are also used as reference voltages for various level detect circuits and the desired velocity level during a rezero operation.

(20) Servo logic

The servo logic generates various signals used in coarse control and fine control based on the control logic signals sent from the logic circuit.

(21) Power amplifier interface

This is the interface between the power amplifier for driving the rotary actuator and spindle motor and the servo circuit. When the coarse control operation is performed, the interface selects VLERR by means of *CORSE. When the fine control is performed, the interface selects POSER by means of *GLNMD. One of these signal is sent to the power amplifier as the power amplifier drive signal (PADRV). When the rezero operation is pefrormed, the amplifier gain of PADRV is reduced to avoid the excessive acceleration force to be applied to the carriage and the head. In addition, a DC bias circuit is provided to prevent the head from moving away from the CSS area when the spindle motor rotation is lower than the specified rotational speed (3,961 rpm -2%). The interface for the power amplifier of the rotary actuator includes the current sense signal (CSNSE) which is proportional to the current in the drive coil and the overcurrent signal (OVCRT) which indicates an excessive current flows. The interface for the power amplifier of the spindle motor includes the spindle start signal (*SPSTT) which indicates the start/stop of the motor, the speed alarm signal (SPALM) which indicates that the rotational speed is not in the range of 3961 rpm ± 2%, and the hall alarm signal (HALM) which indicates an abnormal condition of the hall-effect element used for monitoring the spindle motor rotation.

(22) Power amplifier for rotary actuator

This amplifier provides drive coil current proportional to PADRV sent through the power amplifier interface and sends CSNSE to the servo circuit upon detection of coil current. In addition, it sets OVCRT high to indicate an abnormal condition when current of 5A or more flows for 0.7 seconds or longer.

(23) Power amplifier for spindle motor

This amplifier controls the spindle motor so that it rotates at the specified speed (3961 rpm) when the spindle start signal (*SPSTT) is "0". The rotational speed is checked by the output of three hall-effect elements which are equipped in the motor. The rotational speed is compared with the specified speed each time the disk rotates; if the speed is lower than 3961 rpm, the amplifier provides current and, if the speed is higher than 3961 rpm, current does not flow, allowing

the disks to be rotated by the force of inertia. The speed alarm signal (SPALM) is changed from "1" to "0" when the rotational speed comes up to 3961 rpm, and changed to "1" again when the rotational speed is not within the specified range. The rotational speed monitor circuit is reset when the disk is restarted. The following diagram shows the outputs of the hall-effect elements.

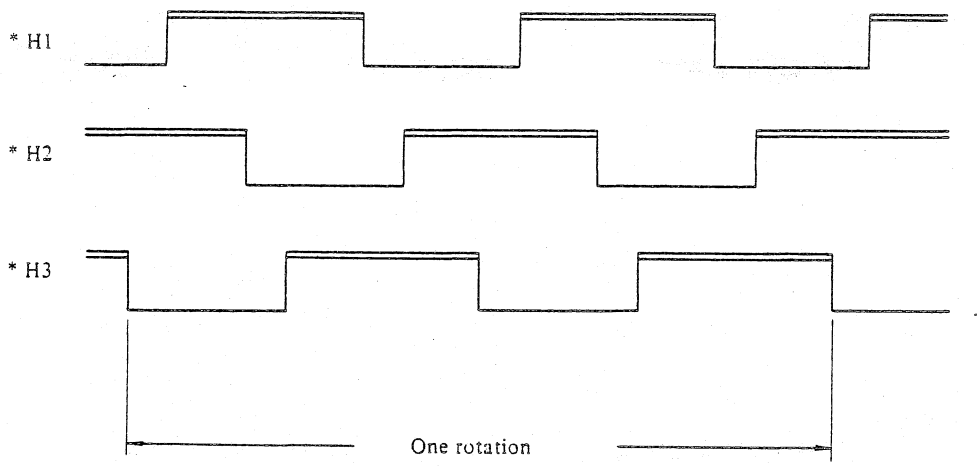


Figure 9.5-13 Outputs of Hall-Effect Elements

CHAPTER 10 READ WRITE CIRCUIT

10.1 WRITE CIRCUIT

When a write command is issued from the controller after head selection, Write Data and Write Clock signals are sent to the drive. Through the MFM modulator and write compensation circuit, Write Data in NRZ code is converted into WDATA in MFM code.

The block diagram of Read/Write circuit is shown in Figure 10.1-1, and the block diagram of circuits in the DE is shown in Figure 10.1-2.

(1) Head Select - Movable Heads

Movable heads are selected by Head Address Register outputs (*HAR1 through *HAR16). *HAR4, *HAR8 and *HAR16 are also decoded and used as Chip Select signals (*CHP0 ~ *CHP4).
One of the 5 head ICs on the head arm assemblies is selected according to the Chip Select signals.
The low-order two bits of Head Address Register (*HAR1 and *HAR2) are converted from TTL to ECL level and used as Head Select signals to select one of the 4 heads.

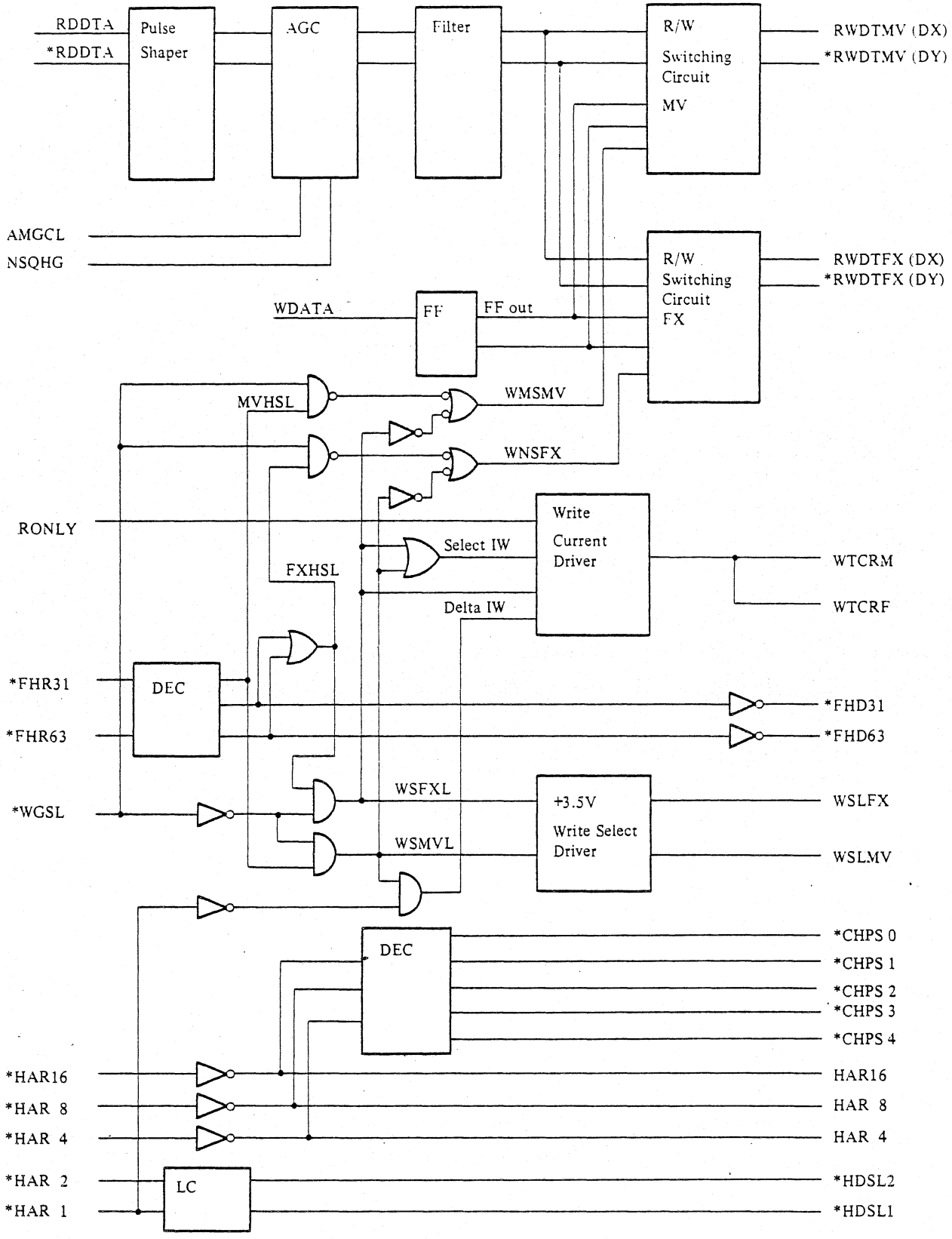


Fig. 10.1-1 Read/Write Circuit Block Diagram

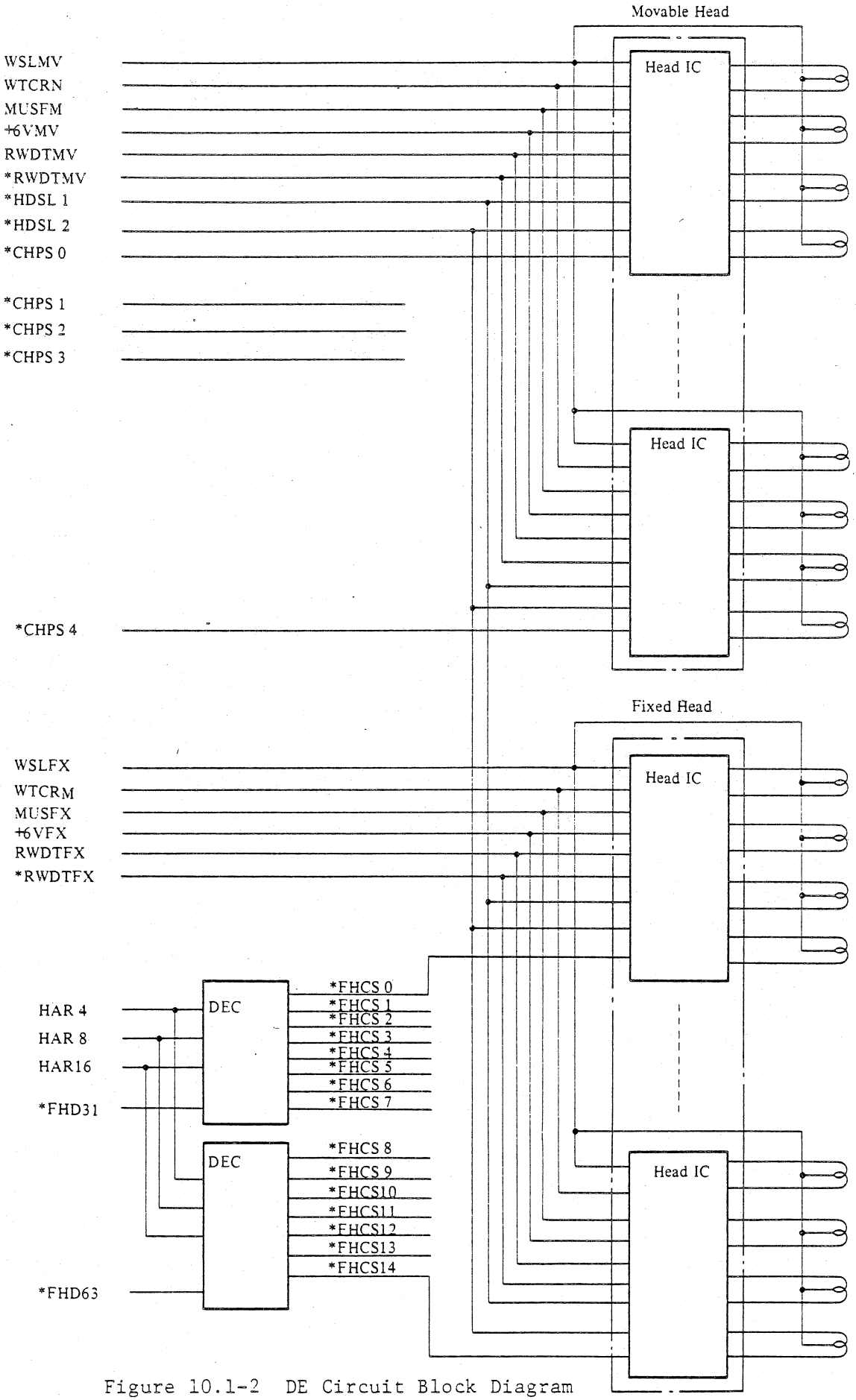


Figure 10.1-2 DE Circuit Block Diagram

(2) Head Select - Fixed Heads

Fixed heads are selected by Fixed Head Register outputs (*FHR31 and *FHR63) and Head Address Register outputs (*HAR4, *HAR8 and *HAR16). *HAR4, *HAR8 and *HAR16 are inverted and, in conjunction with *FHR31 and *FHR63, are sent to two decoders in the DE. These decoders provide Fixed Head Chip Select signals (*FHCS0 through *FHCS14) to select one of the 15 fixed head ICs which are mounted on the PCB in the DE. *HDSL1 and *HDSL2 then select one of the four cores in the fixed head.

(3) Write Select

Write Select Fixed Head (WSLFX) and Write Select Movable Head (WSLMV) signals are constant-voltage +3.5 volts in the active state and are connected to the head center taps during a write operation. Write Gate Select (*WGSL) is low during a write operation, enabling Write Select Movable Head (*WSLMV) and Write Select Fixed Head (*WSLFX). Depending on the mode selected (fixed or movable), the +3.5 volt Write Select drive (WSLFX or WSLMV) is sent to the respective heads in the DE.

(4) Write Current Source

The write current driver is a constant-current power source which supplies write current to the head. The write current varies depending on the signals Select IW, *WSLFX and Delta IW as follows:

Odd number movable head: (Inner movable head)	20 mA
Even number movable head: (Outer movable head)	25 mA
Fixed head 0 ∿ Fixed head 31:	40 mA
Fixed head 32 ∿ Fixed head 59:	45 mA

The write current driver is disabled by Read Only signal (RONLY).

(5) Write Data

Write data (WDATA) is sent out from the MFM modulator and the write compensation circuit in the VFO. The flip-flop is clocked by the positive-going edge of the WDATA signal, and its output is sent to two (bidirectional) Read/Write switching circuit. The write data is switched to the DX, DY inputs to the DE if either *WSLFX (fixed) or *WSLMV (movable) is active.

The DX, DY signals from the respective switching circuit drives the Head IC as Write Data. A timing chart of the Read/Write flip-flop circuit is shown in Figure 10.1-3.

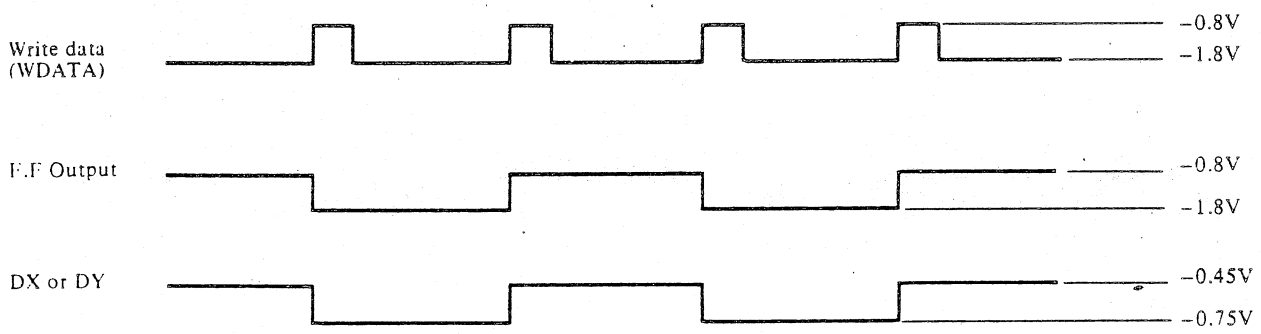


Fig. 10.1-3 Read/Write Flip-Flop Timing Chart

10.2 READ CIRCUIT

When a read command (Tag 3, Bus 1) is issued by the controller, Read Gate signal becomes active and the read operation is initiated. The Read/Write circuit block diagram is shown in Figure 10.1-1.

(1) Read/Write Switching Circuit

The read circuit is enabled anytime Write Mode Select Movable Head (WMSMV) and Write Mode Select Fixed Head (WMSFX) signals are inactive. The DX, DY signals from the Head IC output are applied to the Read/Write switching circuit IC (MB4316), amplified and sent to a low pass filter circuit. The block diagram is shown in Figure 10.2-1.

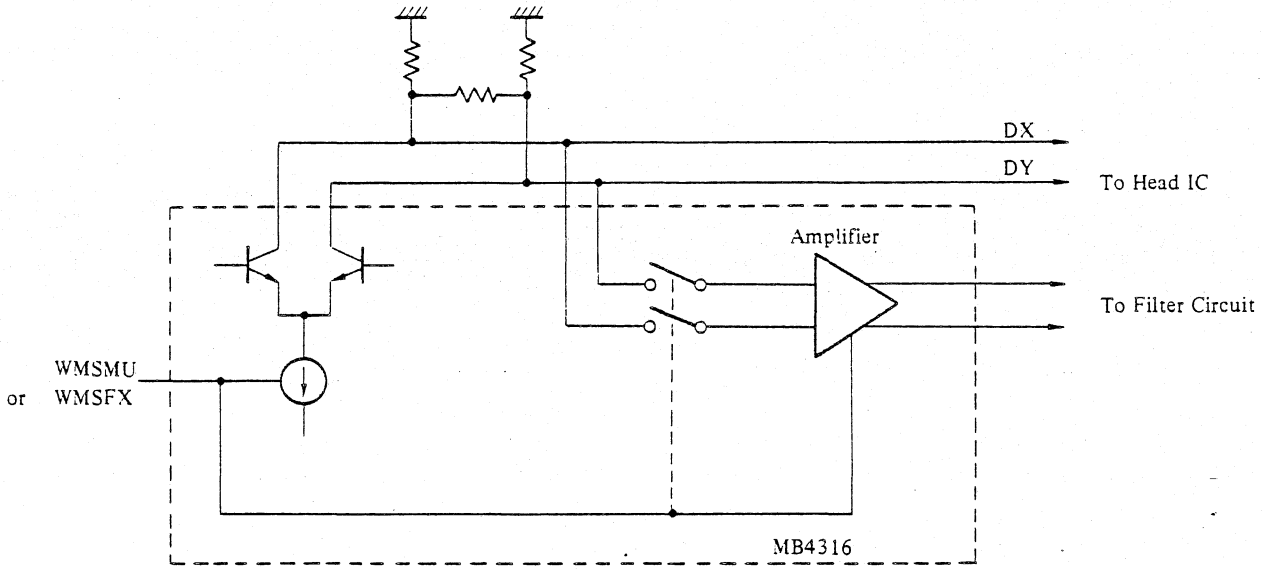


Fig. 10.2-1 Read Write Switching Circuit

(2) Low Pass Filter Circuit (LPF)

The purpose of the low pass filter is to attenuate high-frequency noise. The filter is a Butterworth, with a cut-off frequency of approximately 14 MHZ.

(3) AGC Circuit

The AGC loop consists of an AGC amplifier IC (MB4303) and a level senser IC (MB4311). The LPF output signal is applied to the AGC amplifier, and sent to the level senser IC. Here, it is further amplified (about 10 times) before being applied to the level senser and charge pump (LSCP) circuit and out to a pulse shaper circuit.

The LSCP circuit compares the peak of AC voltage of the AGC output signal with the DC reference voltage 1 (RFV1) and 2 (RFV2). If the voltage of the AGC output signal is lower than the voltage of the RFV1 signal, the LSCP discharges the capacitor 1 (C1) and the voltage VAGC decreases. The decreasing VAGC causes the AGC Amplifier to increase amplitude (gain). The AGC output signal is amplified about 2.6 volts peak to peak. Figure 10.2-2 is a block diagram of the AGC loop circuit.

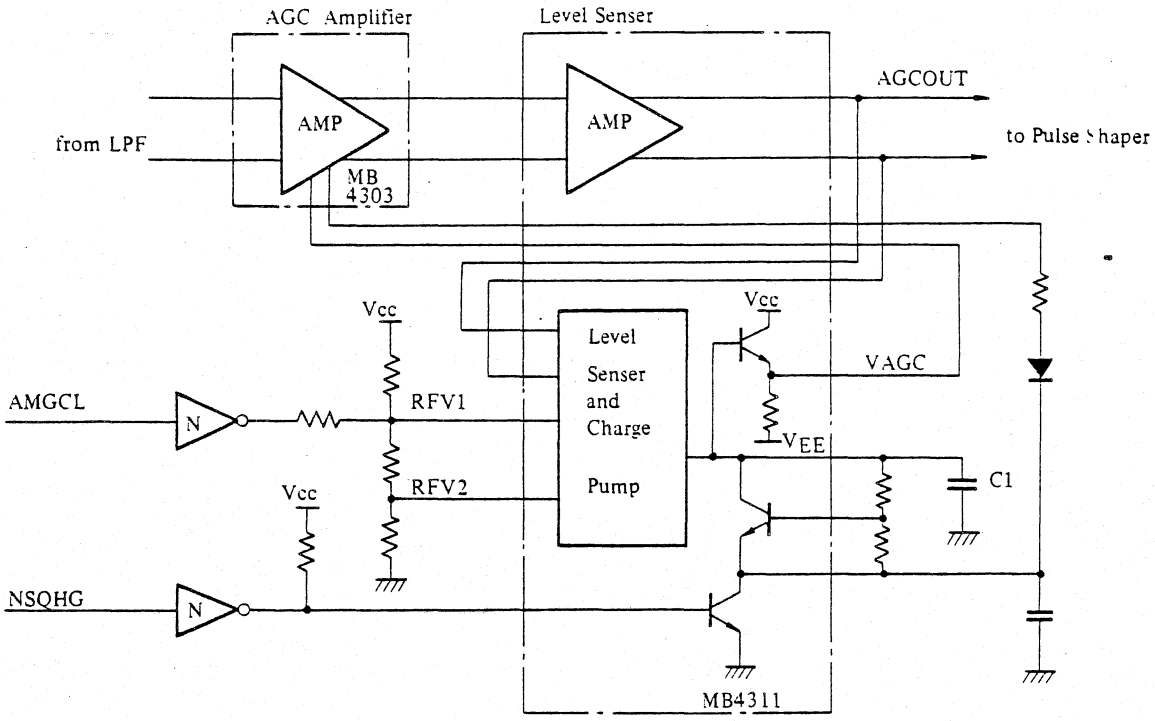


Fig. 10.2-2 AGC Loop Circuit

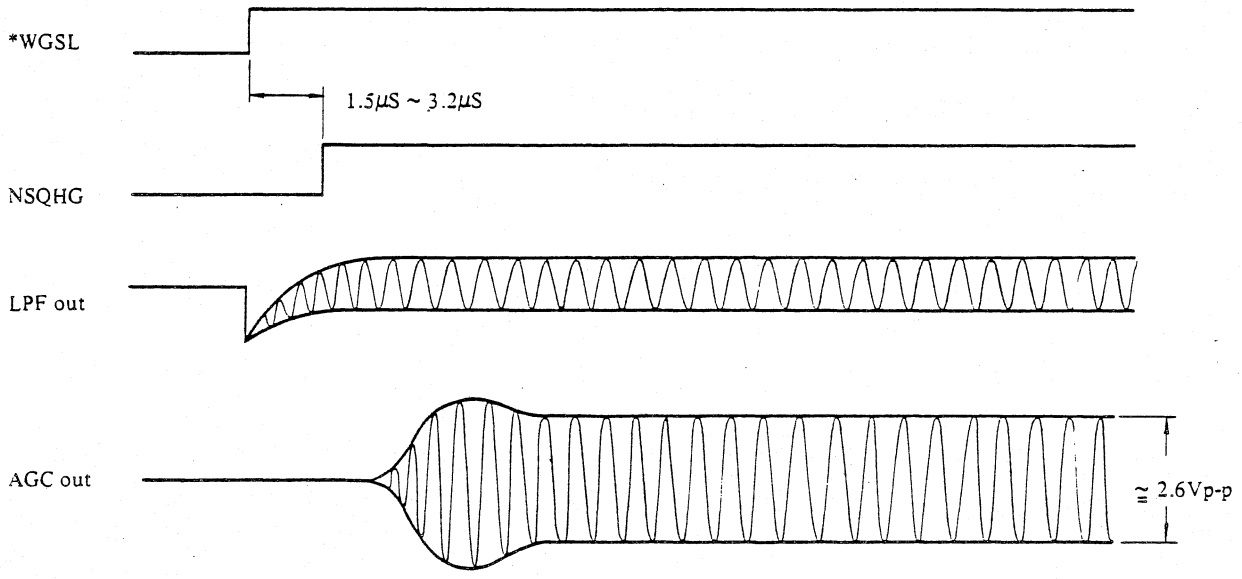


Fig. 10.2-3 AGC Squelch Function

When Write Gate Select signal (*WGSL) is deactivated, the read circuit is activated. However, a read transient caused by the DC unbalance of the read pre-amplifier will occur. Therefore, Not Squelch Gate signal (NSQHG) is enabled about 2 μsec after the Write Gate Select signal (*WGSL) goes high.

The NSQHG signal suppresses this read transient. The AGC squelch function is shown in Figure 10.2-3.

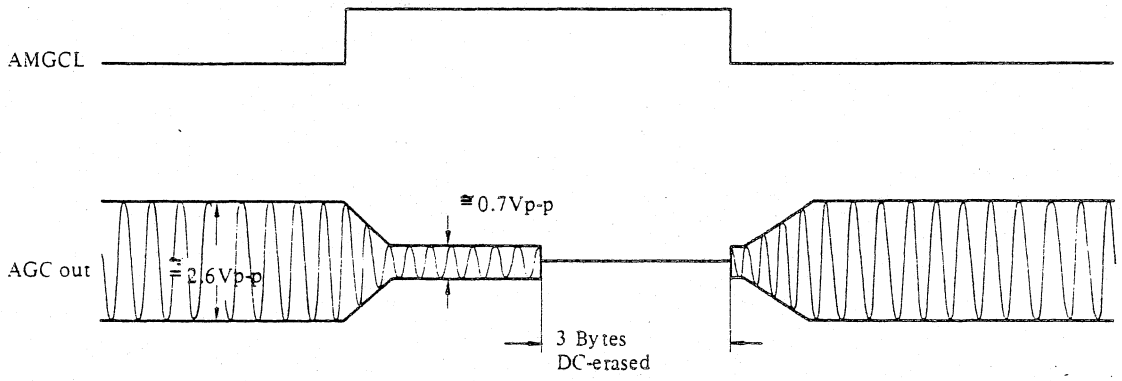


Fig. 10.2-4 AM Search Function

In the variable sector format mode, the address mark (AM), which is a three-bytes DC-erased area, is used for detecting the beginning of a sector. When the controller issues an AM read command, AM Gate Control signal (AMGCL) goes high and decreases the DC voltage of RFV1.

This suppresses the gain of the AGC circuit to avoid false AM detection caused by external noise or media noise in the DC-erased area.

The AM search function is shown in Figure 10.2-4.

(4) Pulse Shaper Circuit (Analog-to-digital converter)

The analog-to-digital converter or pulse shaper has two fandamental circuit; a differentiator which differentiates the AGC output signal and then converts the peaks (flux transition) into zero-crossing signals; and, an integrator which AC-slices the AGC output signal (floating slice) and then generates data window pulse signals.

The block diagram is shown in Figure 10.2-5 and the timing chart in Figure 10.2-6.

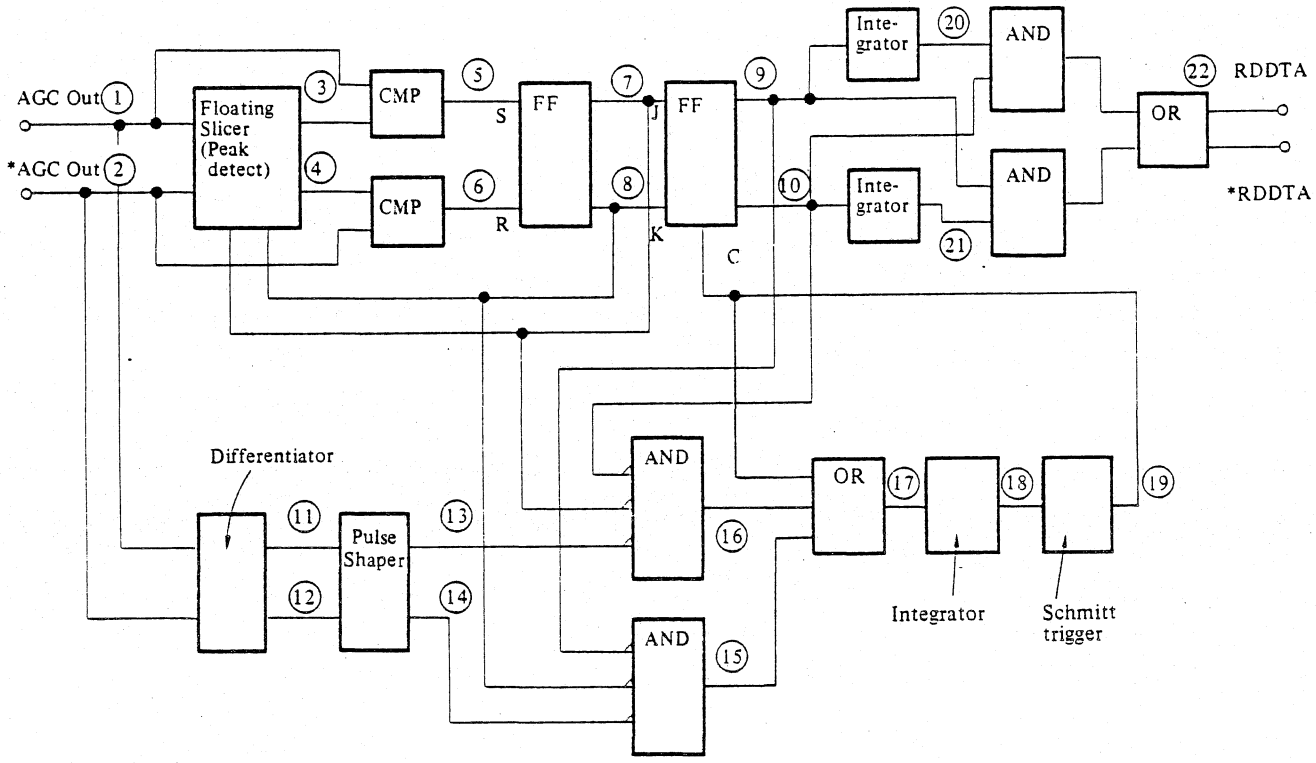


Fig. 10.2-5 Pulse Shaper Circuit Block Diagram

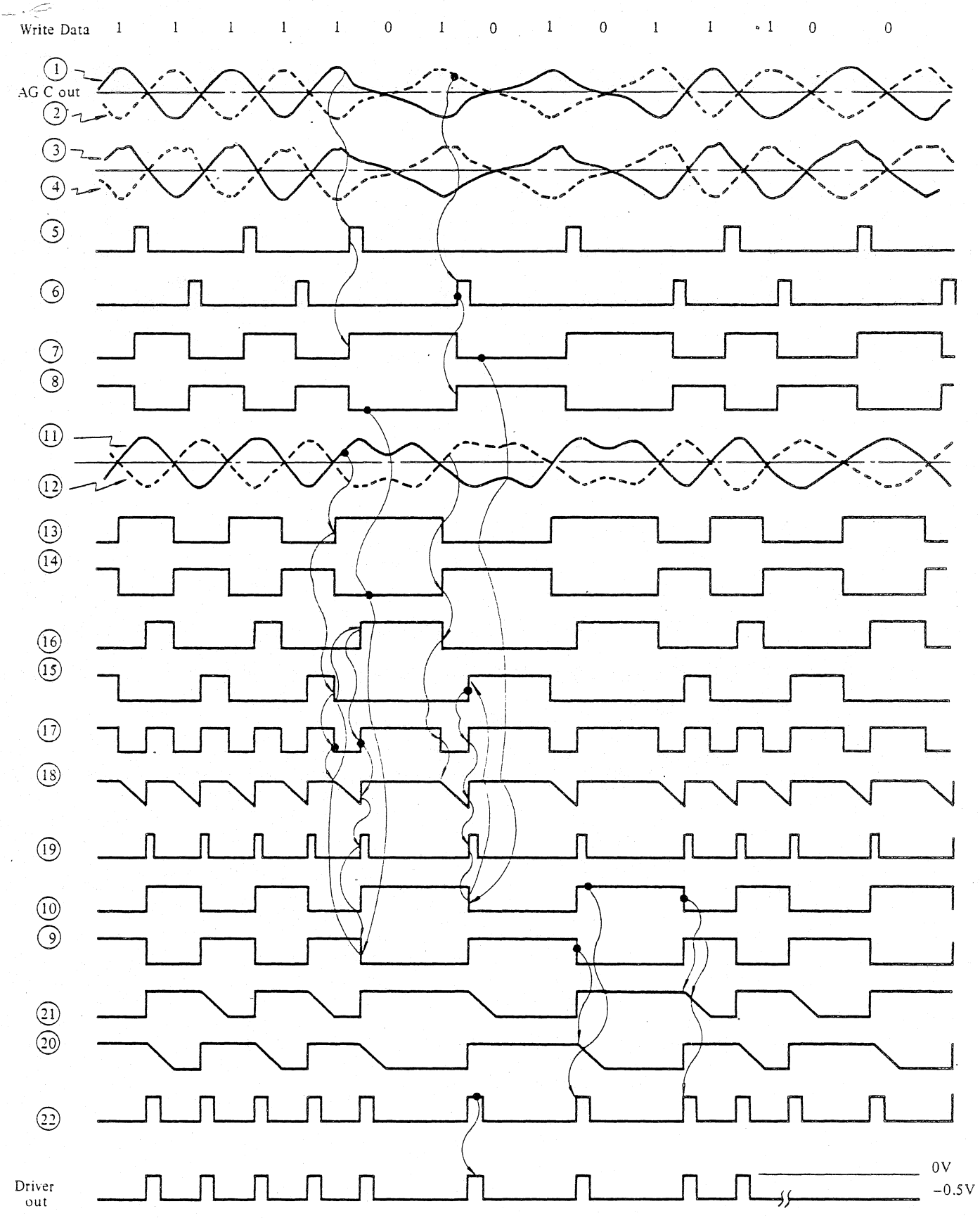


Fig. 10.2-6 Pulse Shaper Circuit Timing Chart

10.3 ERROR DETECTING CIRCUIT

The Read/Write circuit has the following error detecting circuits:

(1) Head Short Check

This circuit detects any abnormal current flowing in Write Select Line during Write operations. The block diagram is shown in Figure 10.3-1.

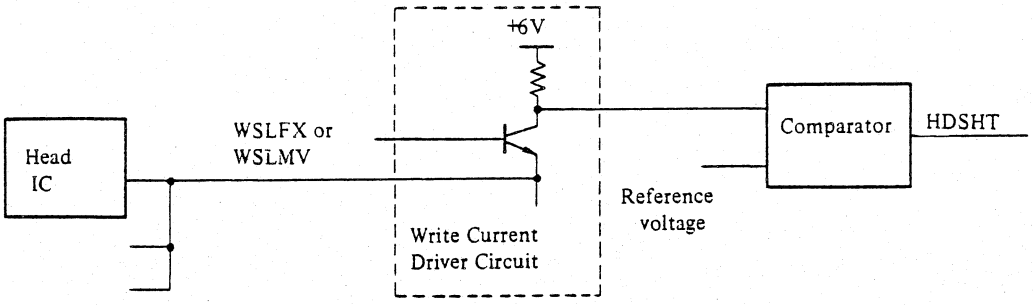


Fig. 10.3-1 Head Short Check Block Diagram

(2) Multi Head Check

This circuit detects that two or more head ICs have been selected. The block diagram is shown in Figure 10.3-2.

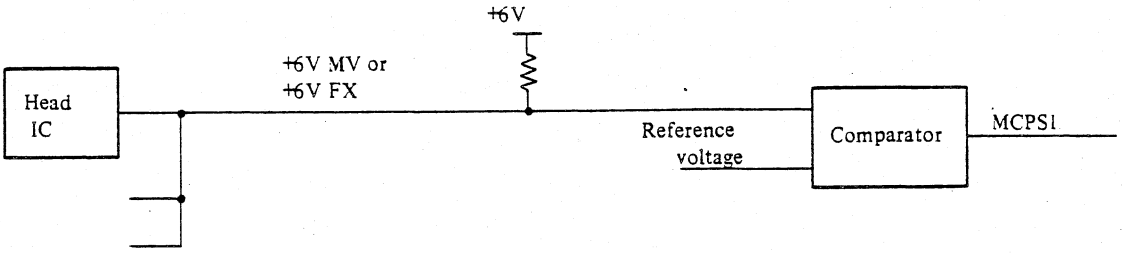


Fig. 10.3-2 Multi Head Check Block Diagram

(3) Delta I Write Check

This circuit checks for normal write-current supplied to the Head IC and Head. The write-current source contains three circuits; Main IW circuit, Delta IW1 circuit and Delta IW2 circuit.

If an even number movable head is selected, for example, Select I write (SLIW) and Gated I Write 1 (GDIW1) signals are enabled. Then Main IW circuit and Delta IW1 circuit are activated and supply about 25 mA of write-current.

But, in this case, if the Delta IW1 circuit is not active, the detector senses this and Delta I Write Check signal goes high.

The block diagram is shown in Figure 10.3-3.

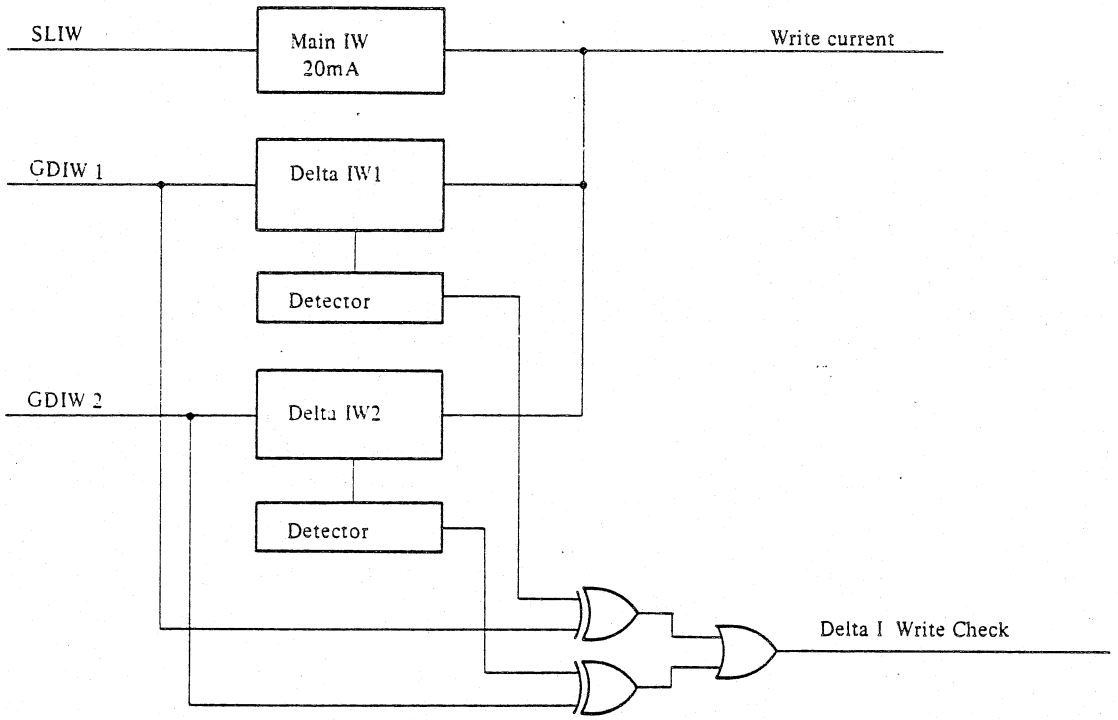


Fig. 10.3-3 Delta I Write Check Block Diagram

(4) Write Transition Check

During a write operation, the write-current in a data head coil flows in alternate directions according to the write data pulse train.

If this write-current transition is not performed, the Mars Unsafe Fixed Head or Movable Head (MUSFX, MUSMV) signal goes high and the FF will set the Write Transistion Check signal to high about 12 bytes after the leading edge of the Write Gate.

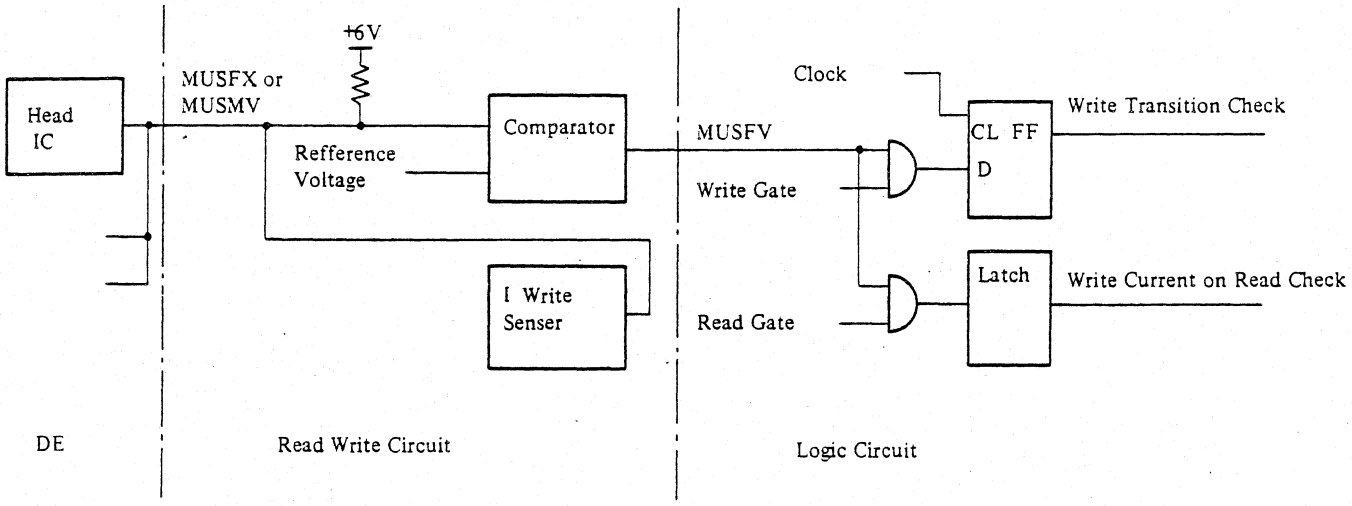


Fig. 10.3-4 Write Transition Check and Write Current on Read Check Block Diagram

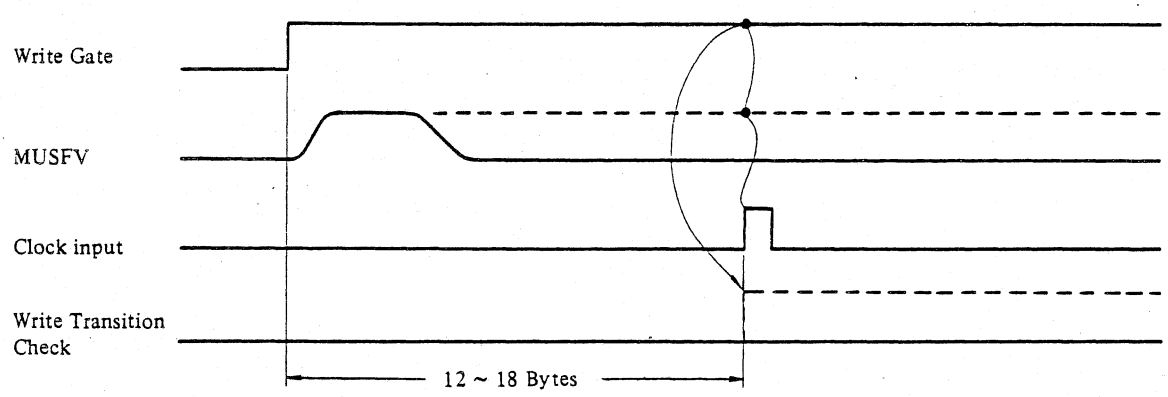


Fig. 10.3-5 Write Transition Check Timing Chart

The write transition check block diagram is shown in Figure 10.3-4 and timing chart in Figure 10.3-5.

(5) Write Current on Read Check

This circuit detects any write current during a not write operation. The block diagarm is shown in Figure 10.3-4.

10.4 DE INTERFACE

The interfaces between the DE (Disk Enclosure) and the printed circuit board are shown in Table 10.4-1. The DE circuit block diagram is shown in Figure 10.1-2.

Table 10.4-1 DE Interface

Signal Name	Level		DE Connector	Pin No.
	Select	Non-Select		
*CHPS 0	0 ∿ +0.4V	≙6V	CND	03
" 1	"	"	"	05
" 2	"	"	"	07
" 3	"	"	"	09
" 4	"	"	"	11
*HDSL 1	ECL Low	ECL High	"	36
" 2	"	"	"	38
HAR 4	"	"	"	17
" 8	"	"	"	15
" 16	"	"	"	13
*FHD 31	"	"	"	23
" 63	"	"	"	21
*FHFB	0V	Open	"	01
WTCRM	Special	Special	CNE	09
WTCRF	"	"	"	10
WSLMV	+3.5V 0.3V	0V 0.1V	CND	28
WSLFX	"	"	"	30
MUSFM	Special	Special	"	32
MUSFX	"	"	"	34
+6VMV	*	*	"	25
+6VFX	*	*	"	26
+5VFX	*	*	CNE	19
-4VDE	*	*	"	13,14,15
RWDTMV	Special	Special	"	06
*RWDTMV	"	"	"	05
RWDTFX	"	"	"	01
*RWDTFX	"	"	"	02

Description of signals

(1) *CHIP SEL 0 ∿ 4

CHIP SEL is the signal which selects one of the 5 movable head ICs. Two or more movable head ICs must not be selected simultaneously. Simultaneously selecting two or more movable head ICs causes Multi Head error.

(2) *HDSL 1 and 2

Each HEAD IC has 4 read/write channels. These signals are used to select one of the four heads connected to each channel.

(3) *HAR 4, 8, and 16

These signals are used to select a fixed head. These signals are used in conjunction with the *FHD31 and *FHD63 signals to generate the 15 Chip Select signals in the fixed head block.

(4) *FHD31 and 63

See the above.

(5) *FHFB

This signal is clamped to 0 V when the Fixed Head block is installed in the DE.

(6) WTCRM, WTCRF

This is the line through which the write current is supplied to the head.

(7) WSLMV, WSLFX

These signals are the write gate signals for the head IC and head center tap voltage.

(8) MUSFM, MUSFX

These signals are used to detect the transient during write operations. These signals also detect the fact that Write current is flowing during read operations.

(9) +6VMV, +6VFX

These are the DC voltages to be supplied to the head IC. If no head IC is selected, there is no load current. If a head IC is selected, the load current for one head IC is constant. When the load current exceeds the specified value for one head IC, Multi Head Check occurs.

(10) (*)RWDTMV, (*)RWDTFX

The write data is sent to DE during a write operation, and the read data is sent from the DE during a read operation.

CHAPTER 11 VFO CIRCUIT

The VFO circuit consists of Switching Gate, Time-margin Measurement Monostable multivibrator (TMM), Reference Monostable multivibrator, Latch, Phase Comparator and Charge Pump, Low Pass Filter, Voltage Controlled Oscillator, MFM Demodulator, MFM Modulator and Write Compensator, as shown in Figure 11.1-1.

11.1 MFM MODULATOR AND WRITE COMPENSATION CIRCUIT

When the bit density (BPI) is high on a disk surface, and a read operation is performed, peak shift phenomenon appears. A bit span tends to widen the narrow part of the bit spacing because of mutual magnetic interference of the bits.

When such a phenomenon appears, reading of the data will deviate from the correct bit spacing, causing data errors. The write compensation circuit measures the peak shift direction and amount that will occor during the read operation, and generates pre-shifted write data in the opposite direction. Figure 11.1-2 shows the block diagram of the MFM Modulator and Write Compensation Circuit, and Figure 11.1-3 shows the timing chart.

The NRZ Write Data (WRDT) sent from the controller is clocked by the positive-going edge of the WTCL, and then the WTDT is synchronized with the internal VFO write clock by a Sync Decision Window circuit at the negative-going edge of the Write Gate Select (*WGSL).

The NRZ write data, synchronized with the internal write clock, is applied to a four-bit shift register. Each output of the four-bit shift register is applied to a MFM Modulator and Write Compensation circuit, and then converted into a modified frequency modulated and pre-shifted data pulse train, according to the truth table as shown in Table 11.1-1.

The pre-shift timing of write compensation is defined by 2F Early 1 (2FE1), 2F Early 2 (2FE2), 2F On-time (2FOT) and 2F Late (2FLT) clock signals.

Table 11.1-1 MFM Modulator and Write Compensation Trunk Table

Shift Register Status				MFM & Write Comp. Data							
				Data Bit				Clock Bit			
SR0	SR1	SR2	SR3	EY1	EY2	OT	LT	EY1	EY2	OT	LT
o	1	1	*	1	o	o	o	o	o	o	o
o	1	o	*	o	1	o	o	o	o	o	o
1	1	1	*	o	o	1	o	o	o	o	o
1	1	o	*	o	o	o	1	o	o	o	o
1	o	o	o	o	o	o	o	1	o	o	o
1	o	o	1	o	o	o	o	o	1	o	o
o	o	o	o	o	o	o	o	o	o	1	o
o	o	o	1	o	o	o	o	o	o	o	1

* = Don't Care

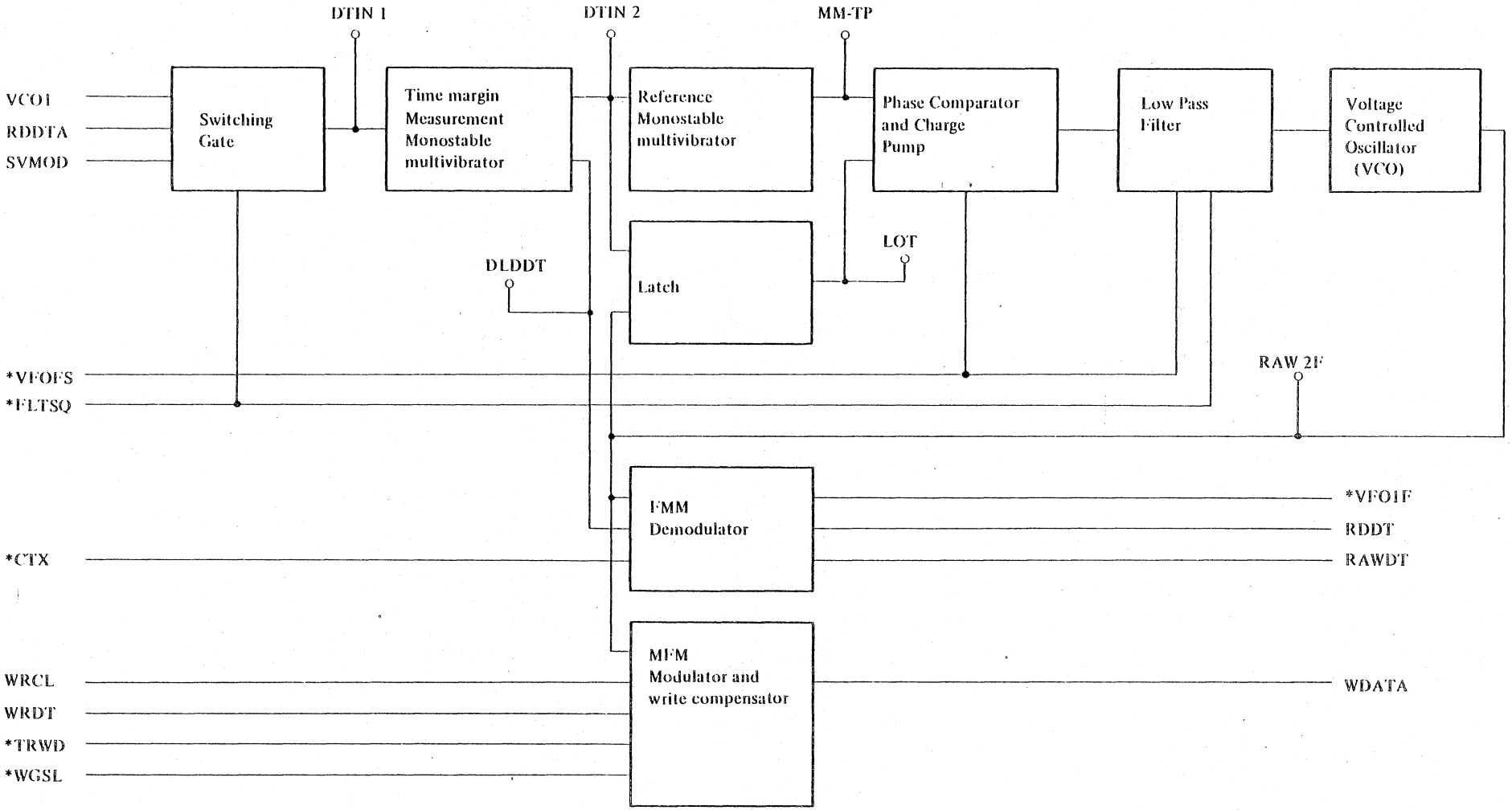


Fig. 11.1-1 VFO Block Diagram

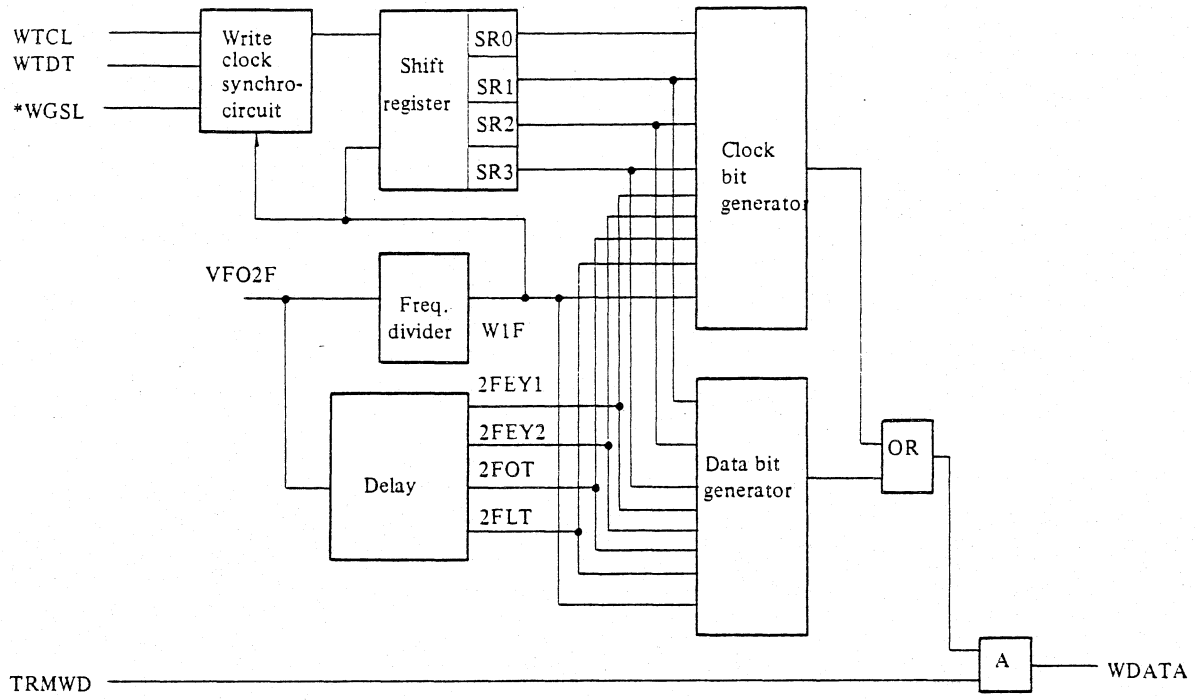


Fig. 11.1-2 MFM Modulator and Write Compensator Block Diagram

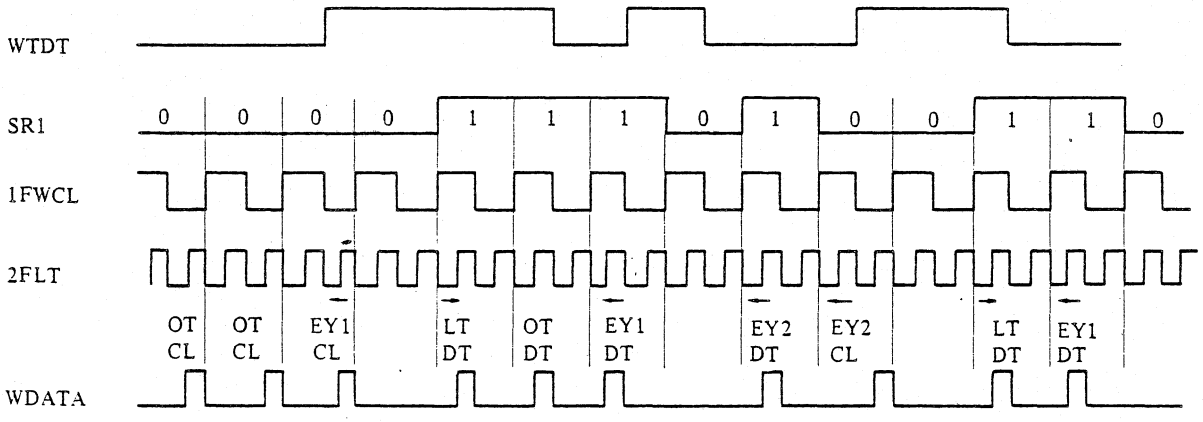


Fig. 11.1-3 MFM Modulator and Write Compensator Timing Chart

11.2 VFO AND MFM DEMODULATOR CIRCUIT

The Variable Frequency Oscillator (VFO) circuit synchronizes with a VCO1 signal from the servo track during a Not-Read operation, and with the Raw Data (RDDTA) signal from the data track during a Read operation. The block diagram of the VFO circuit is shown in Figure 11.1-1.

(1) Switching Gate

The Switching Gate controls the VFO input. During an initial seek operation or a RTZ operation, this circuit inhibits an input data into the VFO circuit by enabling the Filter Squelch (*FLTSQ).

This causes the VCO to oscillate at the free-running frequency. During a Not-Read operation, the VCO1 is applied to the VFO circuit by enabling the Servo Mode (SVMOD).

During a Read operation, the RDDTA is applied by disabling the SVMOD. The Switching Gate output, Data Input 1 (DTIN1), is applied to the Time-margin Measurement Monostable multivibrator (TMM) circuit.

(2) Time-margin Measurement Monostable multivibrator (TMM)

The TMM circuit issues a Data Input 2 (DTIN2) to the Phase Comparator and the Latch, and it also issues a Delayed Data (DLDDT) to the MFM Demodulator. The timing relation between DTIN2 and DLDDT is adjusted by potentiometer RV6 and it determines the time-margine of read data.

(3) Reference Monostable multivibrator

The positive-going edge of the DTIN2 triggers the Reference Monostable multivibrator, which issues 14 nsec Reference Pulse to the Phase Comparator and Charge Pump.

(4) Latch

The positive going edge of the DTIN2 sets the Latch and the negative going edge of the RAW2F reset it.
The Latch issues Latch Output (LOT) to the Phase Comparator and Charge Dump circuit.

(5) Phase Comparator and Charge Pump

The Phase Comparator and Charge Pump circuit issues Decrease Frequency (DECFR) when the VFO input signal is leading, and an Increase Frequency (INCFR) when the VFO input signal is late, comparing the phase between DTIN2 and RAW2F.

The Charge Pump circuit, a constant-current driver, charges or discharges the capacitor in the Low Pass Filter circuit by INCFR or DECFR.

(6) Low Pass Filter

The Charge Pump output signal is applied to Low Pass Filter circuit which attenuate a high-frequency noise.

During an initial seek operation or a RTZ operation, the FLTSQ clamps the Charge Pump output to 0V to recalibrate the VFO function. During an initial data read operation, the VFO Fast Synchronization (*VFOFS) is issued to the VFO circuit.

This increases the loop gain of the VFO circuit to widen the pull-in range and shorten the pull-in time for synchronization with input data.

The output of the Low Pass Filter is the control voltage signal (VCX).

(7) Voltage Controlled Oscillator (VCO)

The VCO circuit is controlled by the VCX.

The VCO output signal (RAW2F) frequency increases when the VCX goes high, and decreases when the VCX goes low.

(8) MFM Demodulator

The MFM Demodulator circuit generates NRZ Read Data (RDDT) and VFO1F Clock (VFO1F) from MFM Read Data.

The MFM Demodulator circuit is controlled by RAW2F, Delayed Data (DLDDT) and Count X (*CTX) during the read operation.

11.3 PRINCIPLE OF SYNCHRONIZATION AND DEMODULATION

MFM Demodulator circuit block diagram is shown in Figure 11.3-1 and timing chart is shown in Figure 11.3-2. During a read operation, the RDDTA is applied to the VFO circuit by disabling the SVMOD signal.

The TMM circuit generates two output signals, the DTIN2 and the DLDDT, by triggering two monostable multivibrators at the positive going edge of the RDDTA.

The positive-going edge of the DTIN2 triggers the Reference Monostable multivibrator. The Reference Monostable multivibrator output signal (MM-TP) has a pulse width about 14 nsec, and the VFO circuit operates to synchronize the negative-going edge of the MM-TP with the positive going-edge of the RAW2F.

The 2F Main Clock (*2FMCL) is derived from the RAW2F delayed by a delay line. The delay line supplies 2F Early 1, 2F Early 2, 2F On time and 2F Late clock signals which are used in the MFM Modulator and Write Compensation circuit.

The positive-going edge of the *2FMCL clocks two Flip-Flops (FF1 and FF2). The FF1 and FF2 circuits divide the frequency of the *RAW2F in two, and then the divided signals are used for the Pre-data Window (PRWD) and Data Window (DTWD).

The DLDDT can trigger FF3 to generate Separated Data (SPD) if the DTWD keeps high when the DLDDT goes high.
The FF3 is reset by Reset Pulse A (RSPA) when CTX is in active and is reset by Reset Pulse B (RSPB) when CTX is active.
The CTX can be activated only in a Gap and the SPD in a Gap must be read only logical zero, but if FF3 generates logical one signal as SPD during CTX is high, the RSPB is issued from AND Gate and force to change the phase of PRWD and DTWD 180 degrees. This causes the SPD to read all zeros.
The DTWD clocks the FF5 circuit relative to the PRRD and generates NRZ Read Data (RDDTA) synchronized with the VFO1F clock. The FF5 output signal (RDDT) is held reset until Read Data Gate (*RDDGT) goes low.

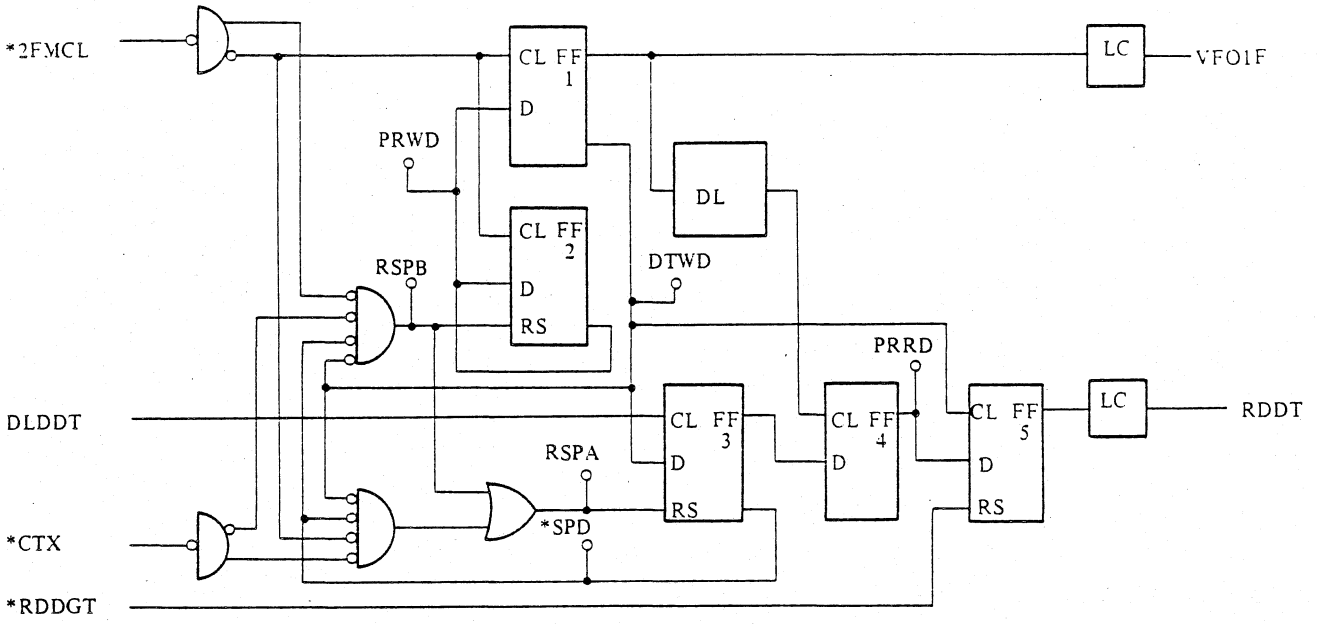


Fig. 11.3-1 MFM Demodulator Circuit Block Diagram

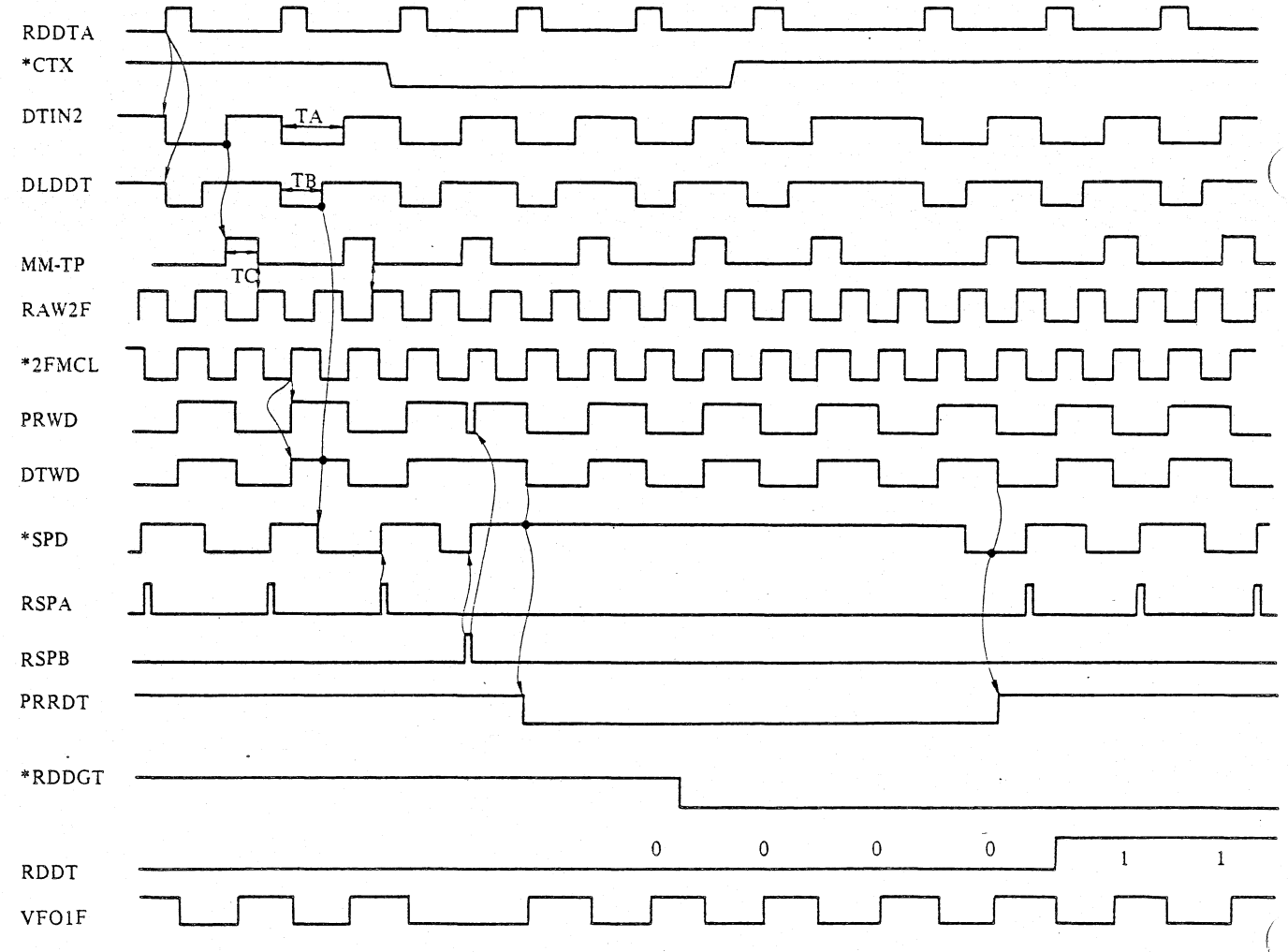


Fig. 11.3-2 MFM Demodulator Circuit Timing Chart

11.4 VFO CONTROL

(1) Initial VFO Control

The VFO control circuit controlls the input of the VFO circuit.
In a start up sequence, the initial seek completion sets a Servo Latch (SRVL), and then sets the Filter Squelch (*FLTSQ) to enable the synchronization of the VFO circuit.

The leading edge of the SRVL triggers the initial VFO fast sync circuit, which issues 15-byte pulse of the *VFOFS followed by a 1-byte pulse of the *CTX.

The negative-going edge of *VFOFS sets the Servo Mode Latch (SVMOD), which is applied to the VFO circuit, selecting the VCO1 as the VFO input data.

The timing chart of an initial VFO control is shown in Figure 11.4-1.

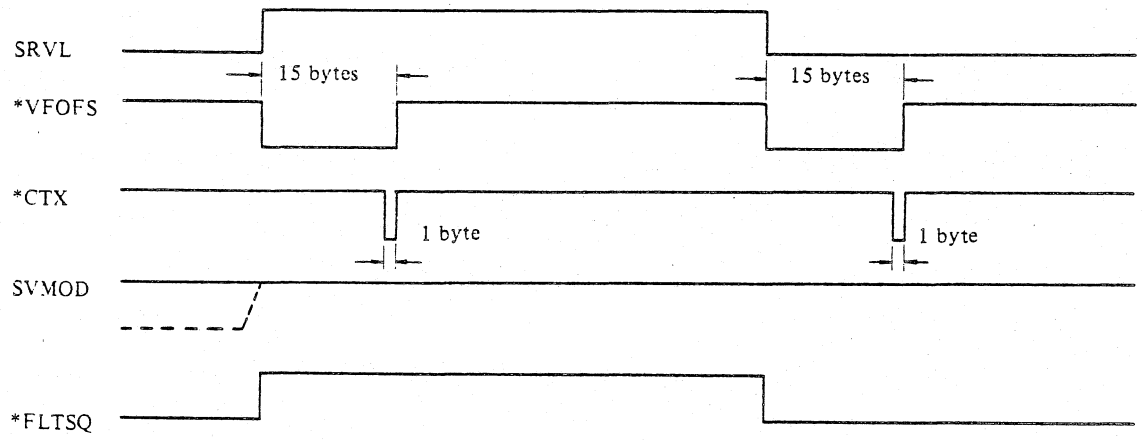


Fig. 11.4-1 Initial VFO Control Timing Chart

(2) VFO Control in Fixed Sector Format

When executing a Read/Write operation, the VFO control circuit generates *VFOFS, SVMOD and *CTX signals triggered by negative and positive-going edges of the Read Gate Control signal (RGC).

The positive-going edge of RGC clocks the VFO control counter circuit to issue a 6-byte pulse of the *VFOFS 7 bytes after the negative going edge of the RGC.

The negative going edge of the *VFOFS sets the SVMOD. The RGC must be held low at least 1 byte or more in a read operation.

The VFO control in Fixed Sector Format timing chart is shown in Figure 11.4-2.

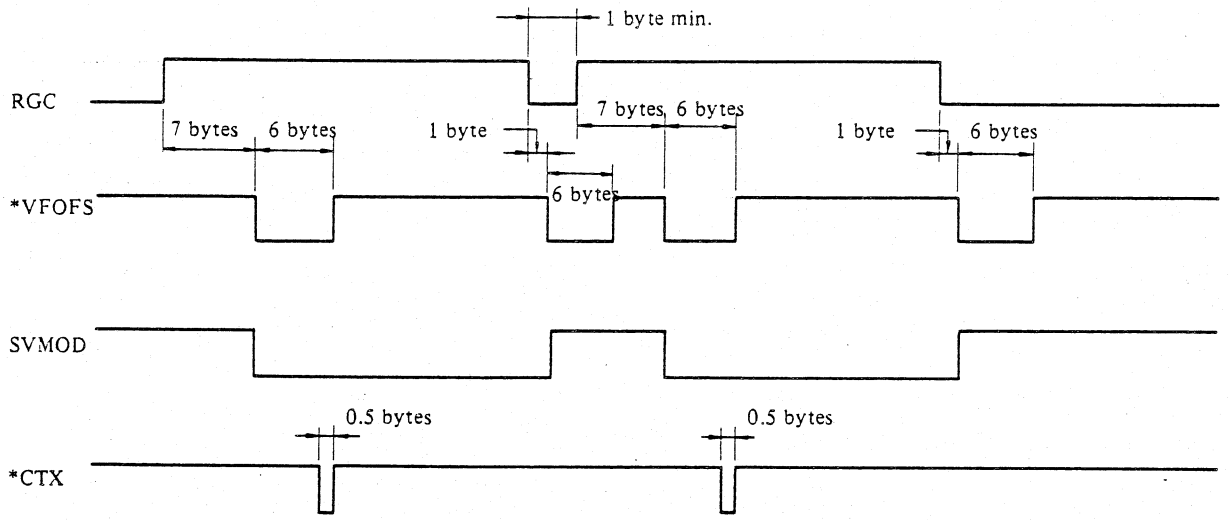


Fig. 11.4-2 VFO Control in Fixed Sector Format Timing Chart

(3) VFO Control in Variable Sector Format

In Variable Sector Format, the controller issues AM Search to the drive. The drive circuit searches for an AM and, when found, issues AM Found (AMFD) with an 8-byte pulse to the controller.

The leading edge of the AMFD triggers the VFO control counter circuit to issue a 6-byte pulse of the *VFOFS 7 bytes after the leading edge of the AMFD.

The remaining operation of the VFO control circuit is the same as that of the Fixed Sector Format.

The VFO control in Variable Sector Format timing chart is shown in Figure 11.4-3.

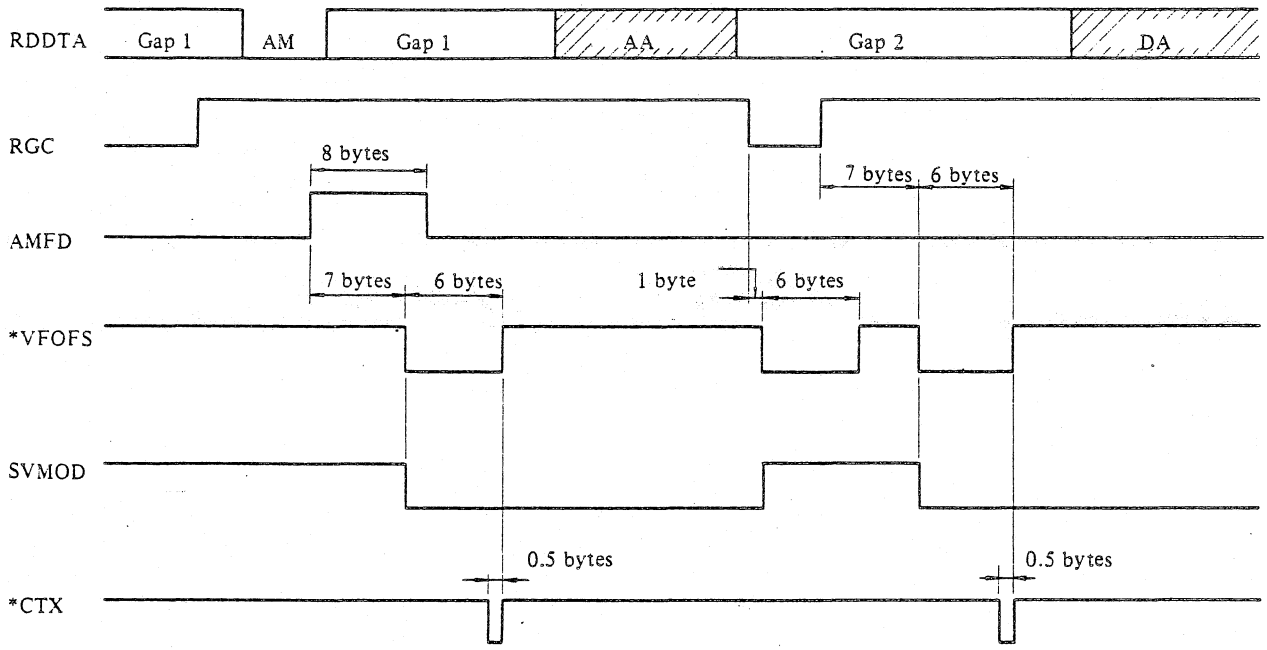


Fig. 11.4-3 VFO Control in Variable Sector Format Timing Chart

CHAPTER 12 DC POWER SUPPLY UNIT

The DC power supply unit does not have a fan for cooling. It is cooled by the airflow from the line blower which cools the entire drive. When the Main Line Switch is turned on, AC power is supplied to this line blower. The Main Line Switch is automatically turned off when it detects an over-voltage or over-current in any of the various DC power supplies, when the transformer or heat sink is overheated, or when a fan alarm occurs.

A sequence control circuit is incorporated. It remotely controls the start/stop operations of the spindle motor with the Pick and Hold signals in the interface signals.

The power supply can be set for different input voltages/frequencies by changing the connections of the terminals located on the control panel of the unit. (Refer to Table 3.1-1)

The AC input cable is shown in Figure 1.7-1. It passes through a cable clamp in the DC power supply unit and is attached to the line filter. The drive is shipped in this condition.

The power supply utilizes a multi-purpose 3-pole circuit breaker. Two poles are used conventionally for primary power interrupt. One of these poles has a trip coil available for remote applications (TRM-4 and -5). The third pole is used for over-current protection of the 48 VDC supplied to the spindle and voice coil motors. It also has a trip coil which is used in the DC over-current/voltage and over-heat detection circuits noted in Table 12.3-1.

12.1 INPUT REQUIREMENT

Input requirements of the DC power supply are those listed for the drive itself. (Refer to Table 1.6-1)

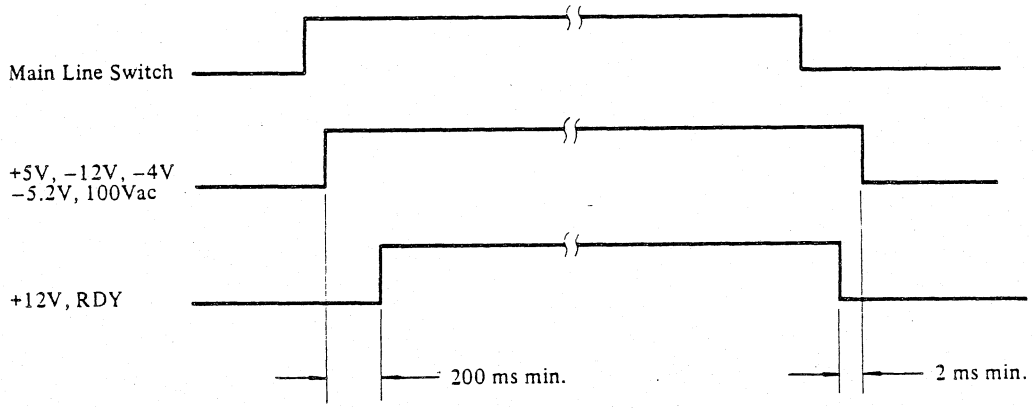


Figure 12.2-1 Output Sequence

12.2 OUTPUT CONDITIONS

Output conditions will be found in Table 12.2-1.

Table 12.2-1 Output Conditions

Voltage		Protection		Current	Variable Range (%)	Usage
Vdc	Tolerance %	Over-Voltage	Over-Current	Adc		
+5	±4	With	With	4 ∿ 5	±5	PCBs
+12	±4	Without	With	0.3 ∿ 1.0	±5	
-12	±4	Without	With	0.3 ∿ 0.5	±5	
-4	±4	Without	With	0.2 ∿ 1.3	±5	
-5.2	±4	Without	With	3.0 ∿ 6.0	±5	
+48	+20 -11	Without	With	3.3 ∿ 5.3 (Peak; 9.6)		Rotary Actuator Spindle Motor
(100Vac)	+13 -15	Without	Without	(0.8 Aac)		Line Blower

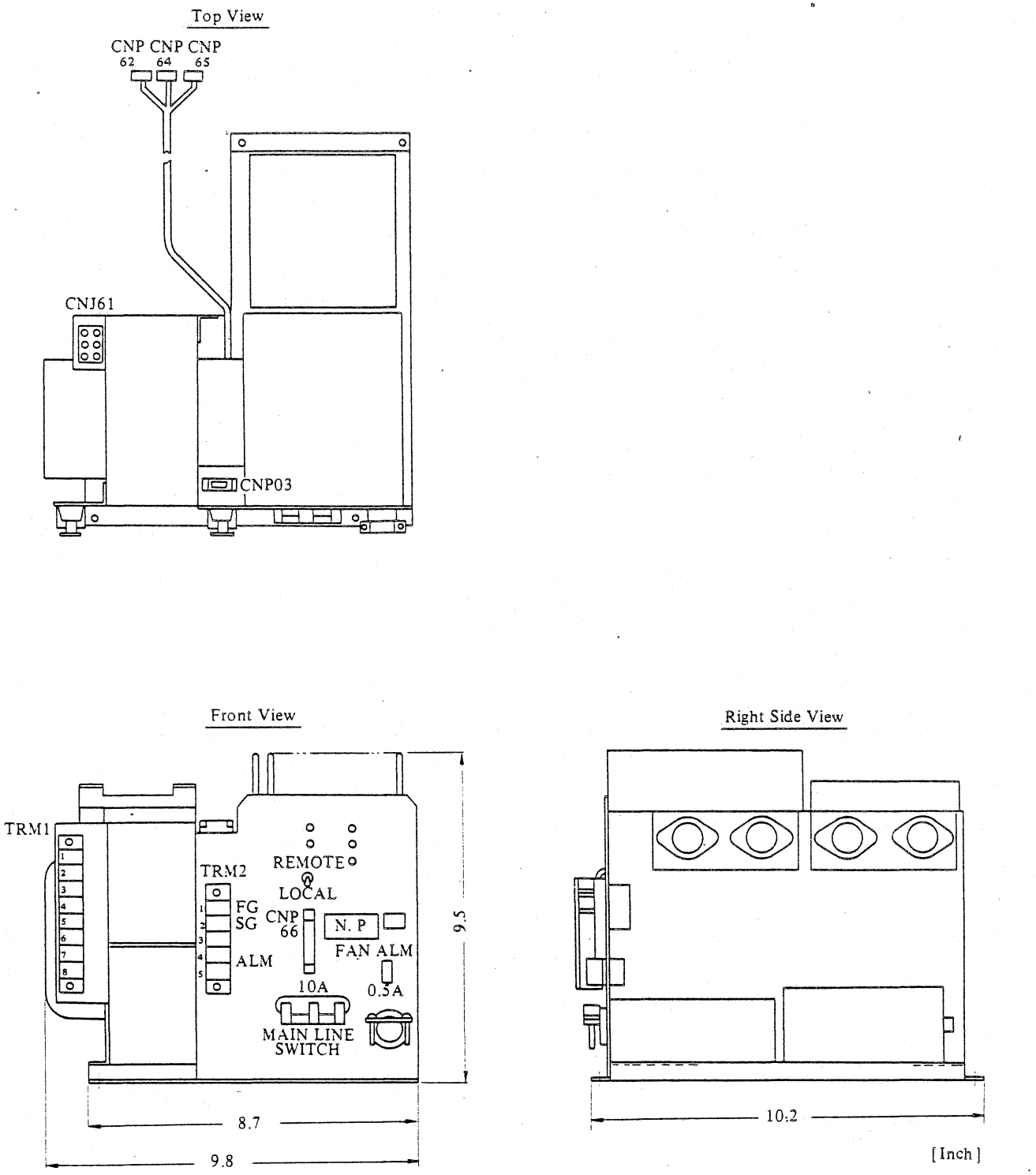


Figure 12.1-1 DC Power Supply Unit

12.3 ALARM DETECTIONS

The causes of various alarms and the indications when they occur are listed in Table 12.3-1.

Table 12.3-1 Indications of Alarm

Alarm	Cause	Indication		(Note)
		Main Line Sw.	Fan Alm Fuse	
Power Alarm	Over-current of AC input	Break		
	Over-current/voltage of DC output			
	Overheat of transformer (139°C)			A thermal fuse embeded in the transformer blows out.
	Overheat of heat-sink (90°C)			
Fan Alarm	Stopping of line blower		Cut	

12.4 CONTROL OF SPINDLE MOTOR

The start/stop operations of the spindle motor are under control of sequence circuit in DC power supply unit. It is described in Figure 12.4-1 and 12.4-2.

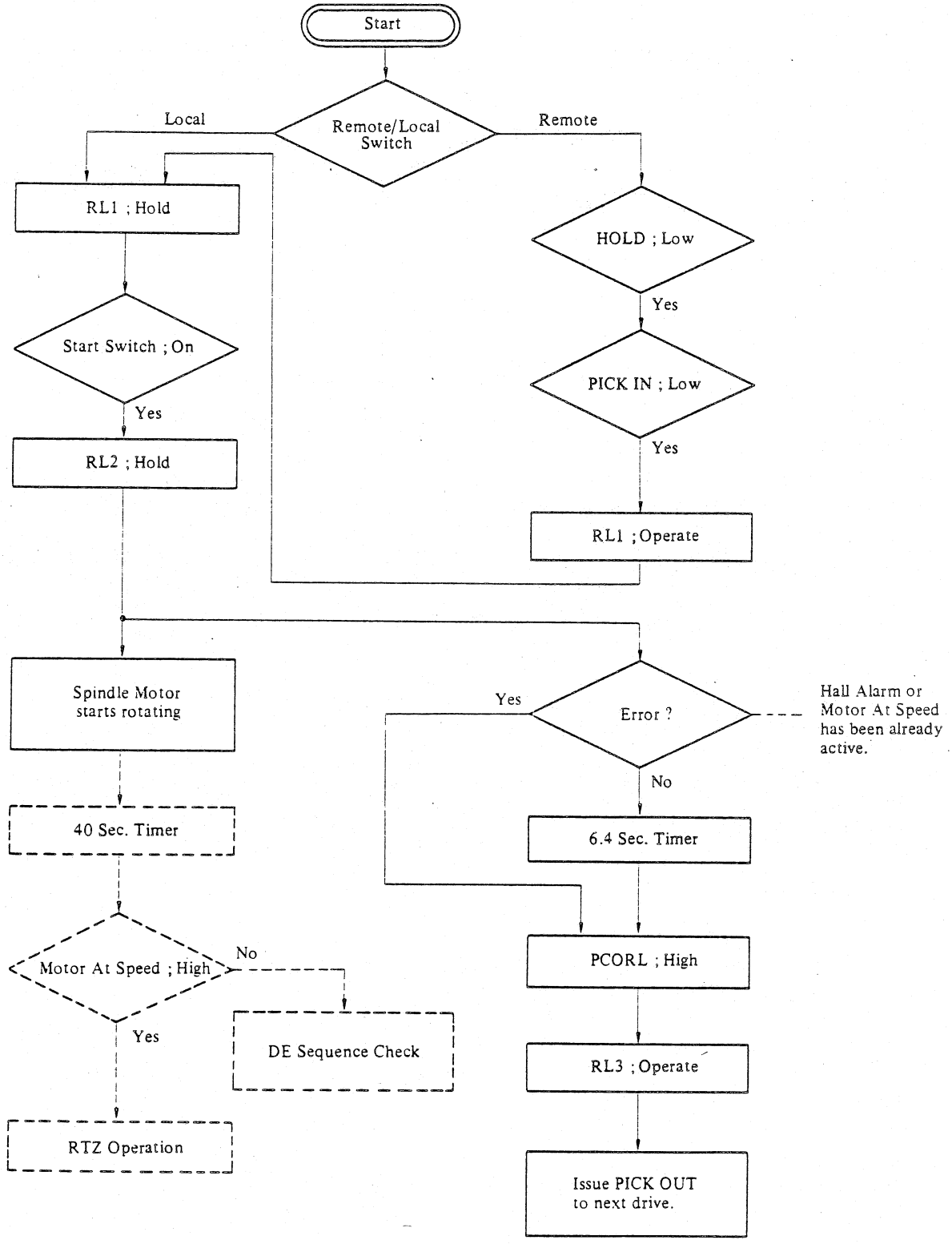


Figure 12.4-1 Flow Chart of Spindle Motor Control

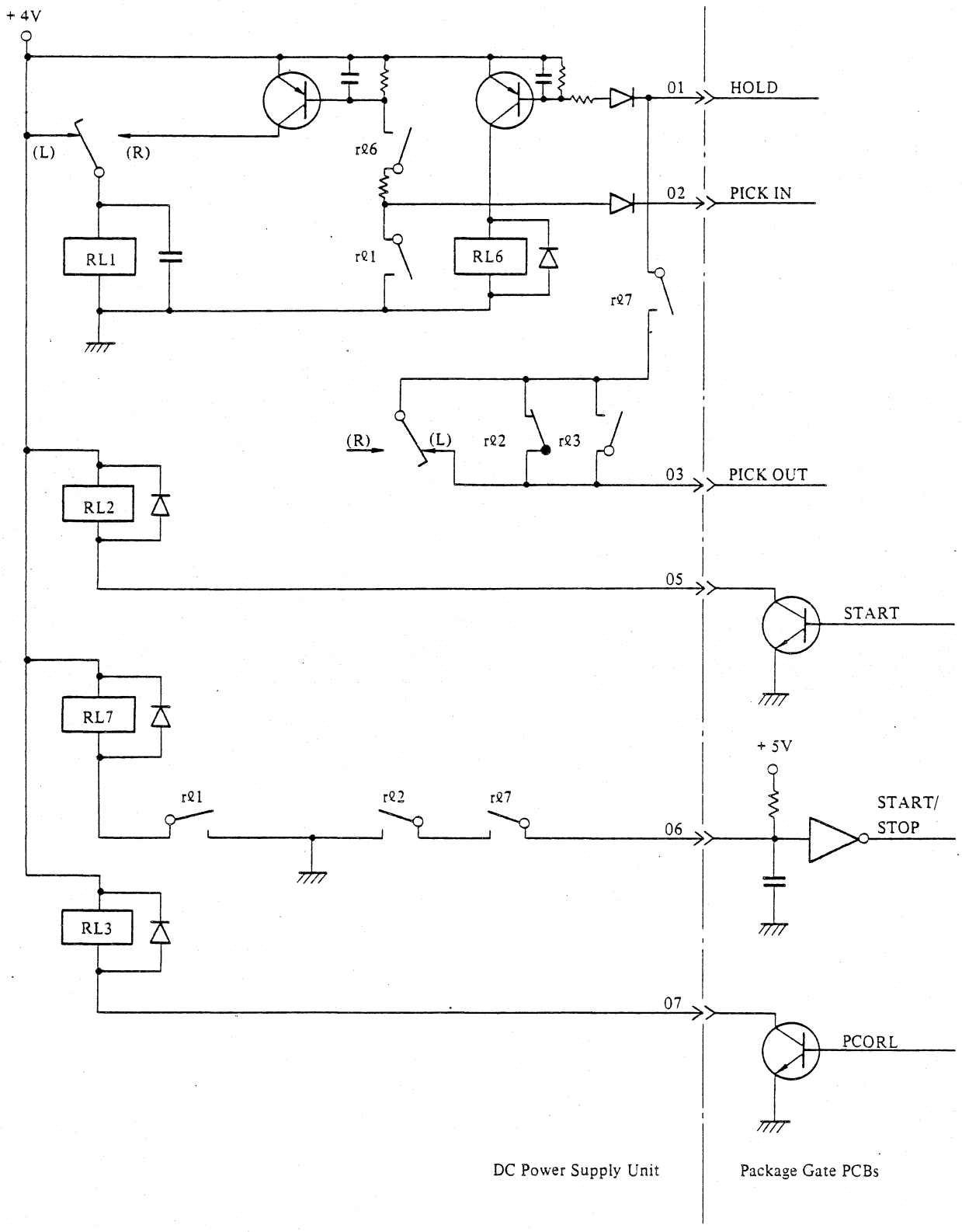


Figure 12.4-2 Spindle Motor Control Circuit

A functional block diagram will be found in Figure 12.5-1.

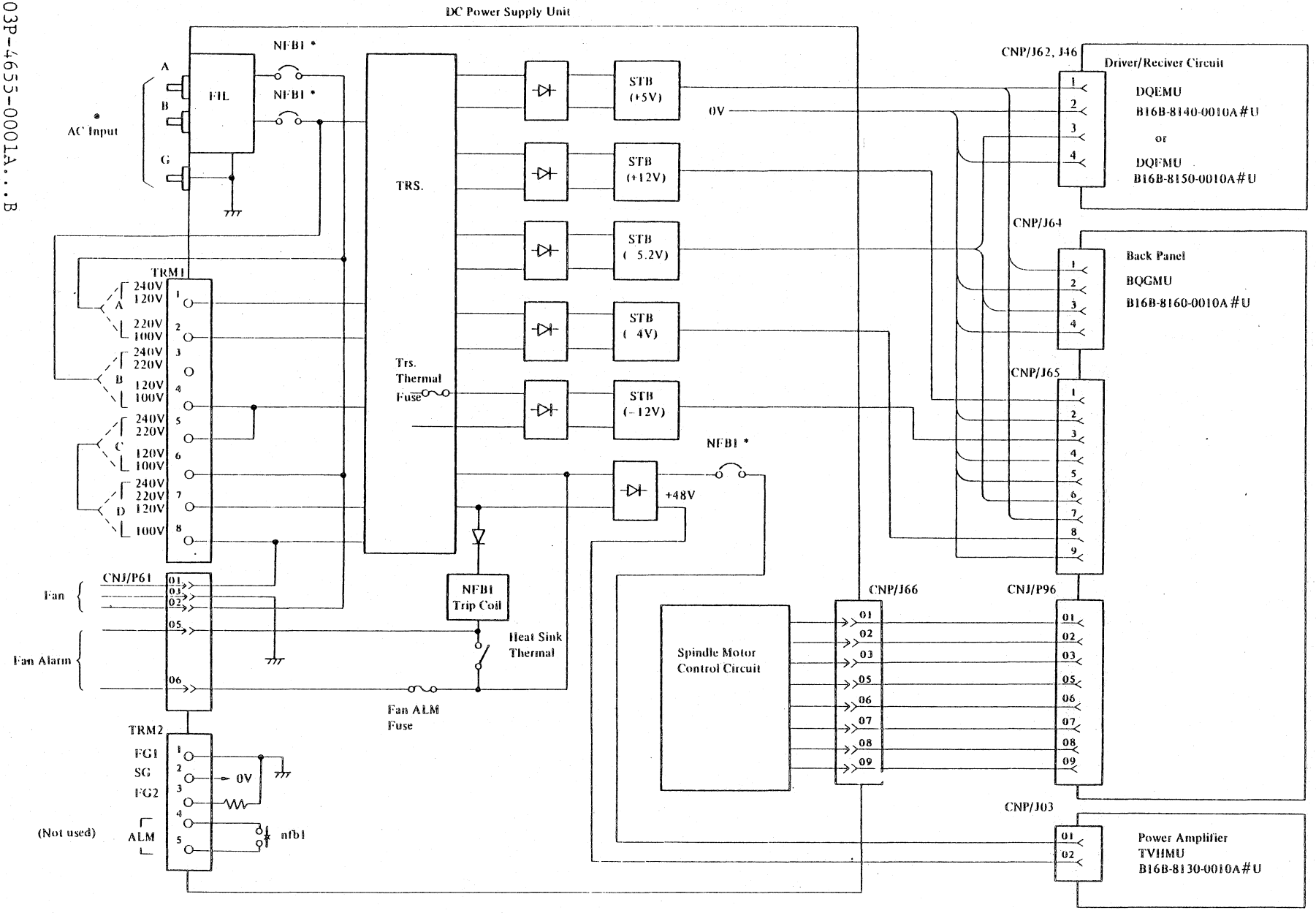


Figure 12.5-1 Functional Block Diagram of the DC Power Supply Unit

CHAPTER 13 MAINTENANCE AND PARTS REPLACEMENT

This chapter covers the maintenance of the drive, namely, general precautions and replacement procedures (including options).

13.1 GENERAL PRECAUTIONS

(1) Power ON/OFF

- Check the operating condition of the drive before turning the power on or off.
- Before turning the power on after the maintenance has been finished, check that all parts are properly Re-assembled.

(2) Removing/Installing connectors

- Always turn the power off before removing or inserting connectors.
- Verify all connectors are inserted correctly.

(3) Replacement

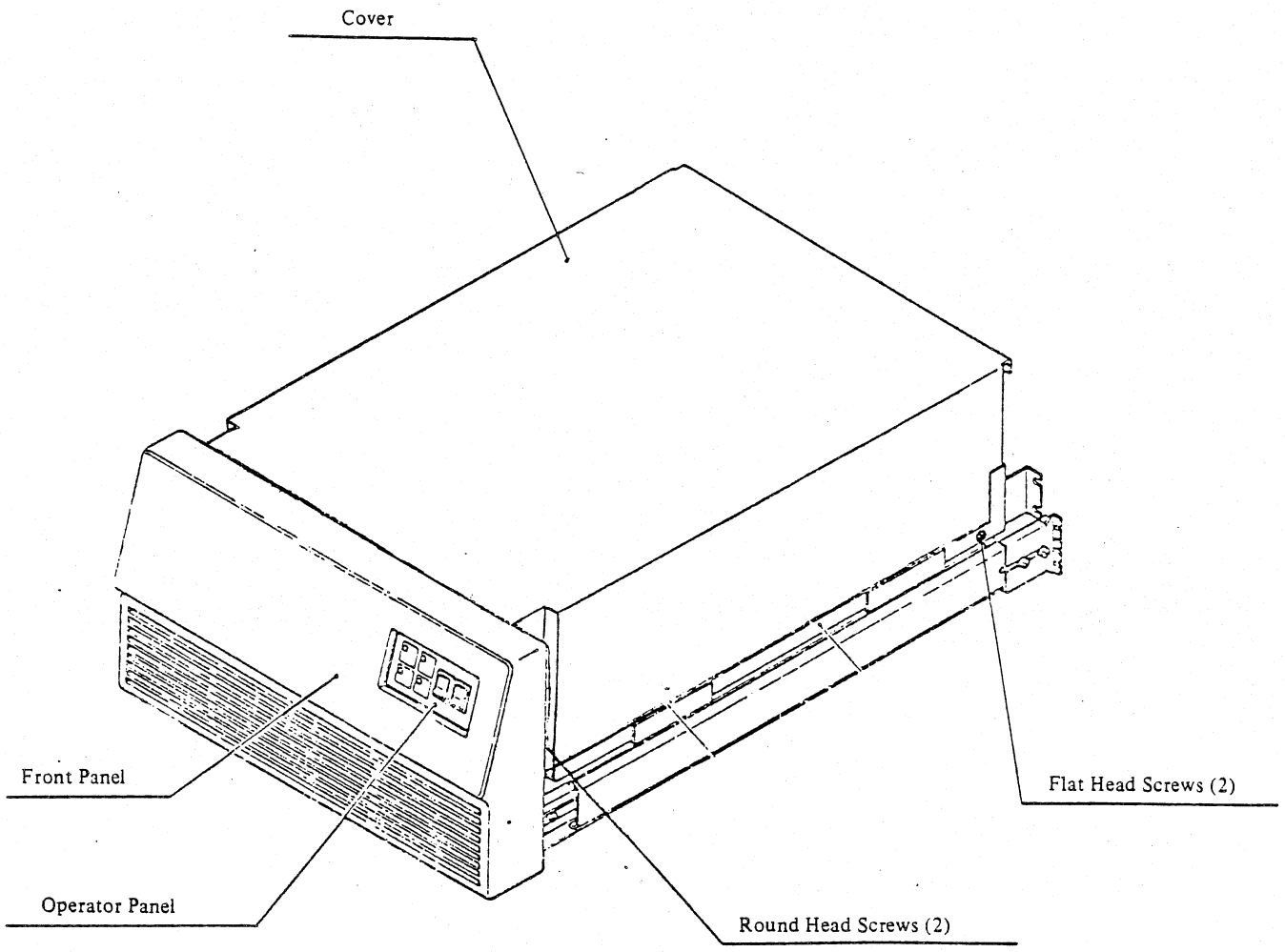
- Use screwdrivers, wrenches and other tools suitable for the screws and bolts to be installed or removed.
- Do not leave removed screws in the drive.
- Tighten all screws with proper torque.

(4) Others

- Use test equipment which is calibrated correctly.
- Always record the trouble-shooting data for later reference.

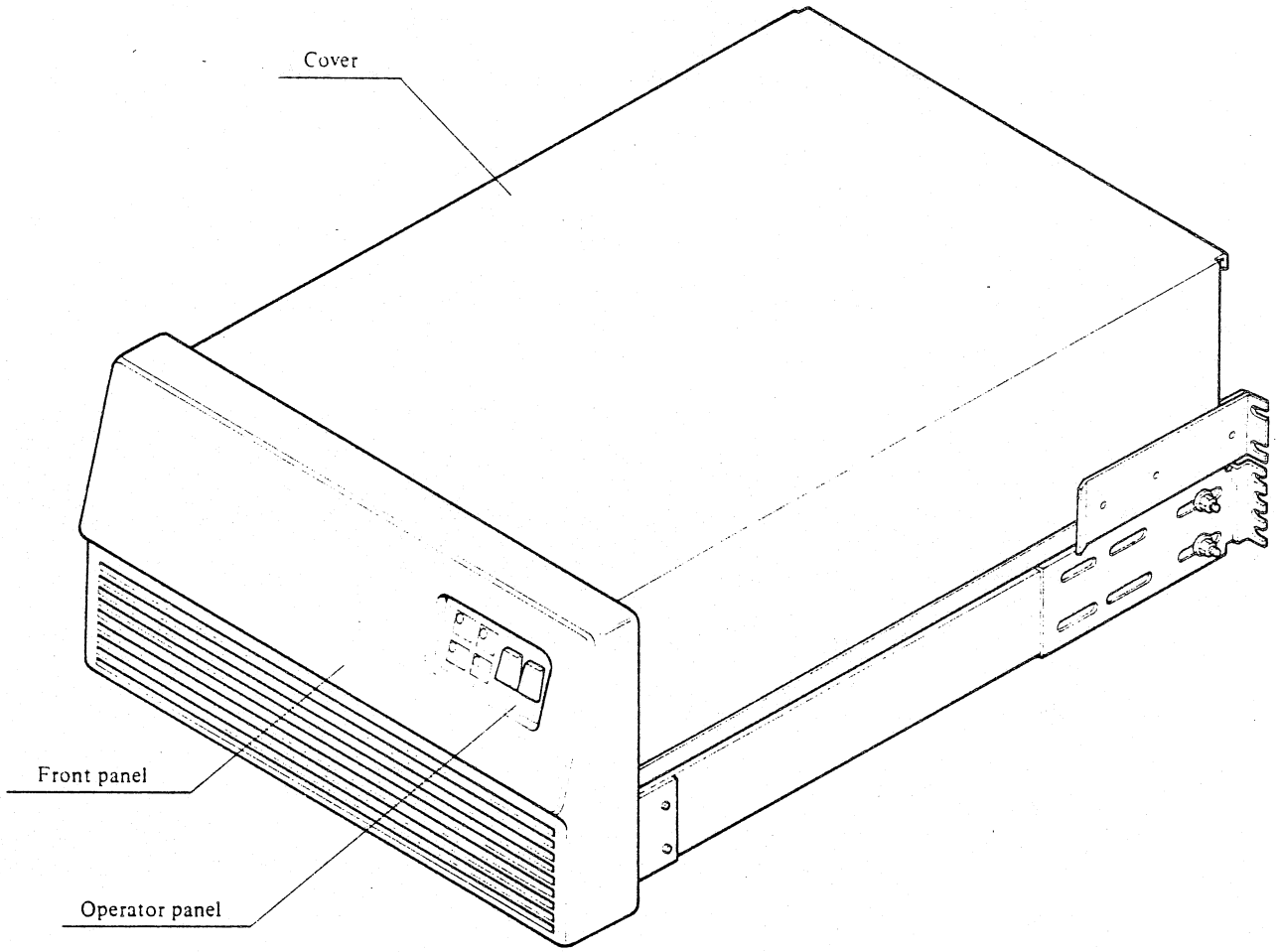
(5) Replacement of Mechanical Parts

Prior to the replacement of mechanical parts, fully extend the drive and remove the cover. The cover is held by 4 screws. Always lock the rotary actuator when replacing mechanical parts.



(a) Old version

Figure 13.1-1 Exterior View of M2351 DKU



(b) New version

Figure 13.1-1 - Continued

13.2 DE REPLACEMENT

13.2.1 DE replacement of old version

(1) REMOVAL

1. Lock the rotary actuator. (Refer to 2.3)
2. Remove the Plastic Cover.
3. Disconnect CNJ01, CNJ02, CNJ03, CNP504 and CNP505 from the TVHMU PCB.
4. Remove the 6 screws (Refer to Figure 13.2-1-⏃-) holding the TVHMU PCB and remove the entire TVHMU PCB.
5. Remove the 4 screws (Refer to Figure 13.2-1-⏃-) holding the TVHMU mounting bracket.
6. If it's a single port drive, remove CNP44 and CNP45 cables to clear the DE area.
7. If the Dual Channel option is installed, remove CNJ56, CNJ62, CNP54, CNP55, CNP57 and CNP59 from DEFMU PCB. (Refer to 13.8-(2))
8. Remove the DQFMU PCB by removing 4 screws and locate cables so as to clear the DE area. (Refer to 13.8-(2))
9. Remove CNJ506 and CNJ508 from the side of the DE.
10. Remove the three hexagon socket-head bolts (Refer to Figure 13.2-1, ✳) from the shock mounts.
11. Carefully lift the DE from the drive. Three cables will come out with the DE. Use care because the DE weighs approximately 58 lb, (25kg).

(2) INSTALLATION

1. To install a DE, be sure the three cables (CNJ502, CNJ504 and CNJ505) are attached/connected and held to the sides of the DE.
2. Gently Lower the DE on the shock mounts, taking care to watch the area all around the DE so cables aren't pinched.
3. Follow, in reverse order, the instructions for removal.

Note: The three hexagon socket-head bolts must be tighten at the torque of about 120 kg·cm.

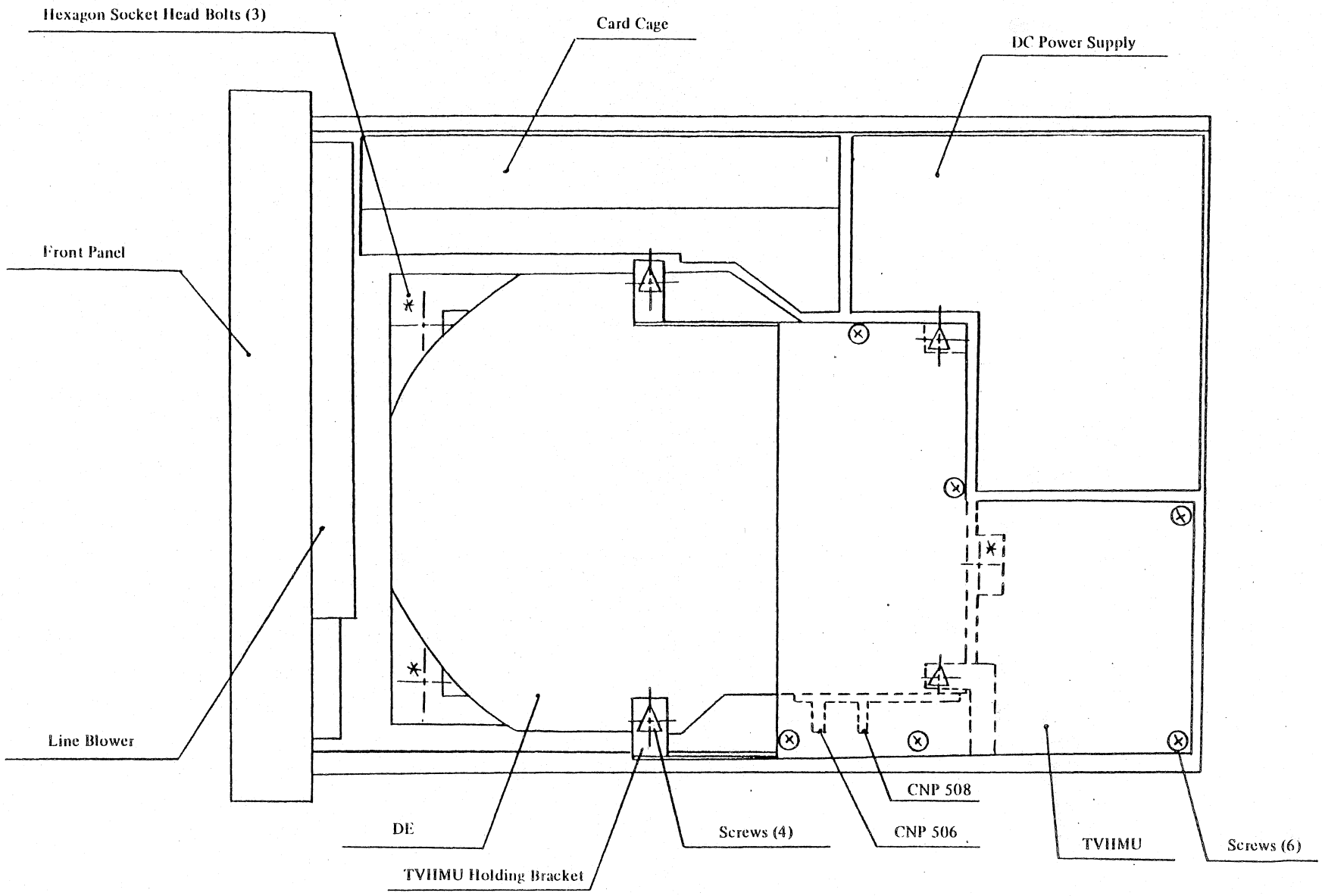


Figure 13.2-1 DE Replacement (Top View) .... Old version

13.2.2 DE replacement of New version

(1) REMOVAL

1. Lock the rotary actuator. (Refer to 2.3)
2. Disconnect CNJ02, CNP504 and CNP505 from the TVKMU PCB.
3. Remove the screw (Refer to Figure 13.2-1) and the wire.
4. If it's a single port drive, remove CNP45 cable to clear the DE area.
5. If the Dual Channel option is installed, remove CNJ56, CNJ62, CNP54, CNP55, CNP57 and CNP59 from DEFMU PCB. (Refer to 13.8-(2))
6. Remove the DQFMU PCB by removing 4 screws and locate cables so as to clear the DE area. (Refer to 13.8-(2))
7. Remove CNJ506 and CNJ508 from the side of the DE.
8. Remove the three hexagon socket-head bolts (Refer to Figure 13.2-1, *) from the shock mounts.
9. Carefully lift the DE from the drive. Three cables will come out with the DE. Use care because the DE weighs approximately 58 lb, (25 kg).

(2) INSTALLATION

1. To install a DE, be sure the cable (CNJ502, are attached/connected and held to the sides of the DE.
2. Gently Lower the DE on the shock mounts, taking care to watch the area all around the DE so cables aren't pinched.
3. Follow, in reverse order, the instructions for removal.

Note: The three hexagon socket-head bolts must be tighten at the torque of about 120 kg·cm.

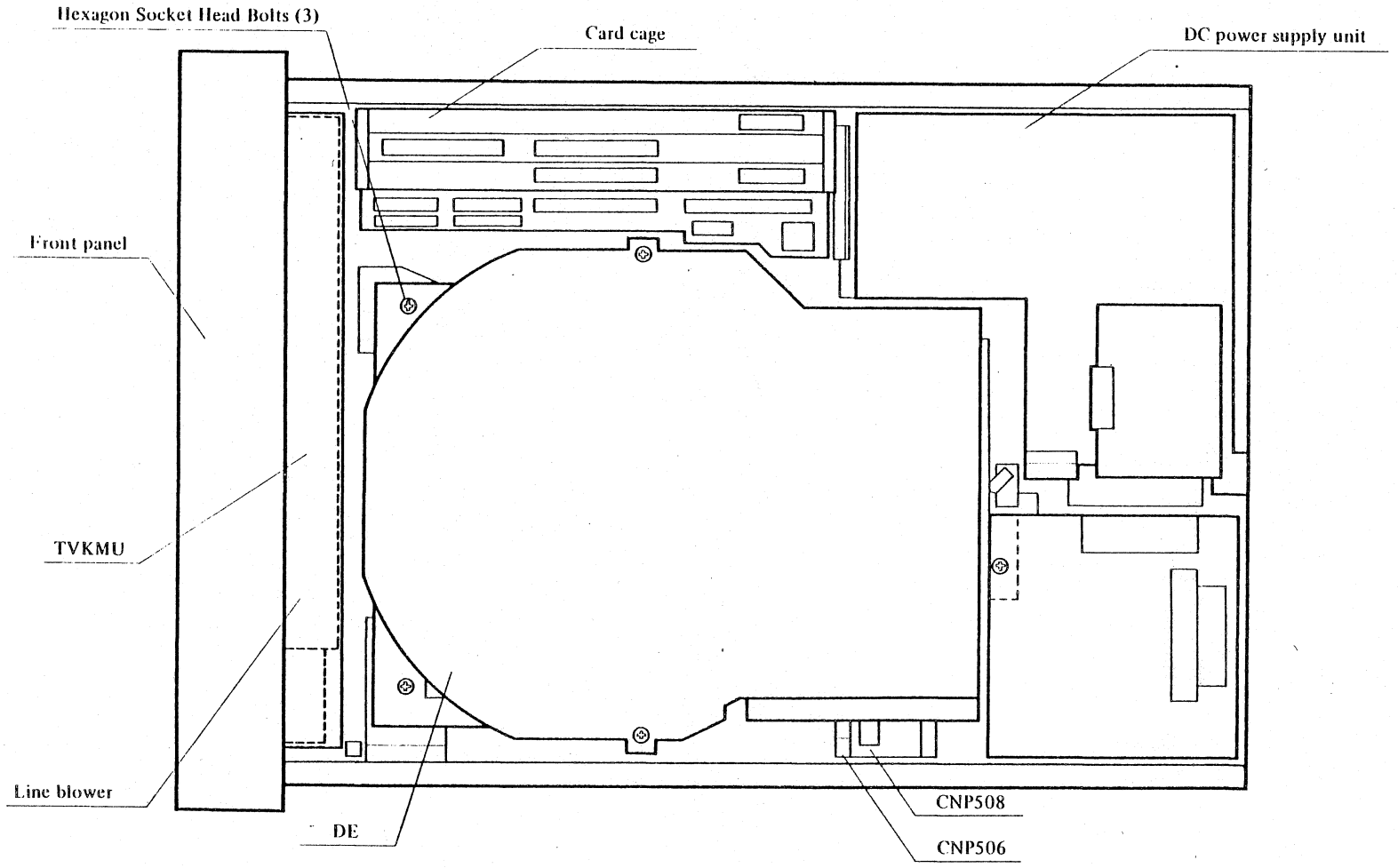


Figure 13.2-2 DE Replacement (Top View) .... New version

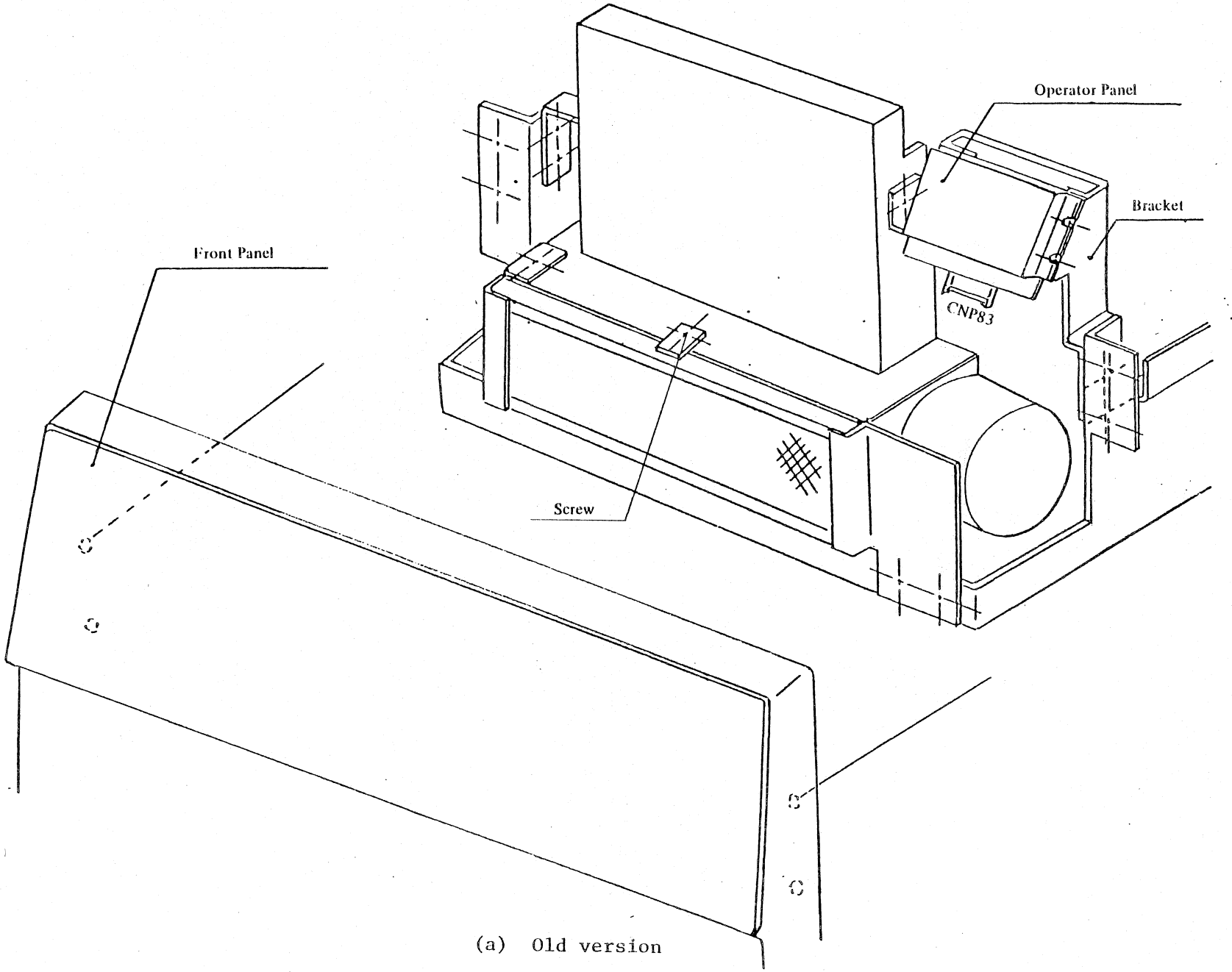
13.3 FRONT PANEL AND OPERATOR PANEL

(1) Removal

1. Remove the 4 screws holding the front panel to the frame.
2. Remove CNP83 from the Operator Panel PCB, and remove the 4 screws holding the Operator Panel to the bracket.

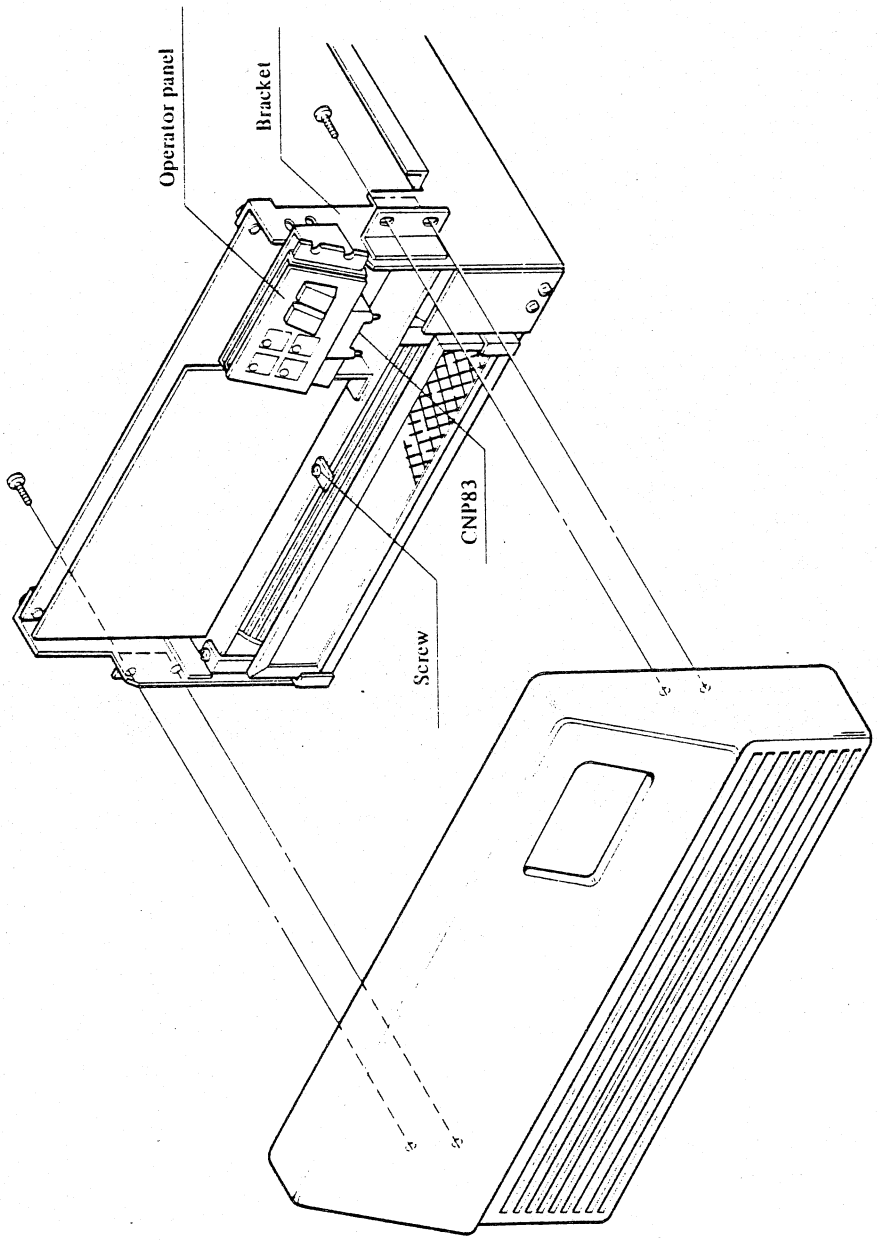
(2) Installation

1. Follow, in reverse order the procedure for removal.



(a) Old version

Figure 13.3-1 Front Panel and Operator Panel Removal



(b) New version

Figure 13.3-1 - Continued

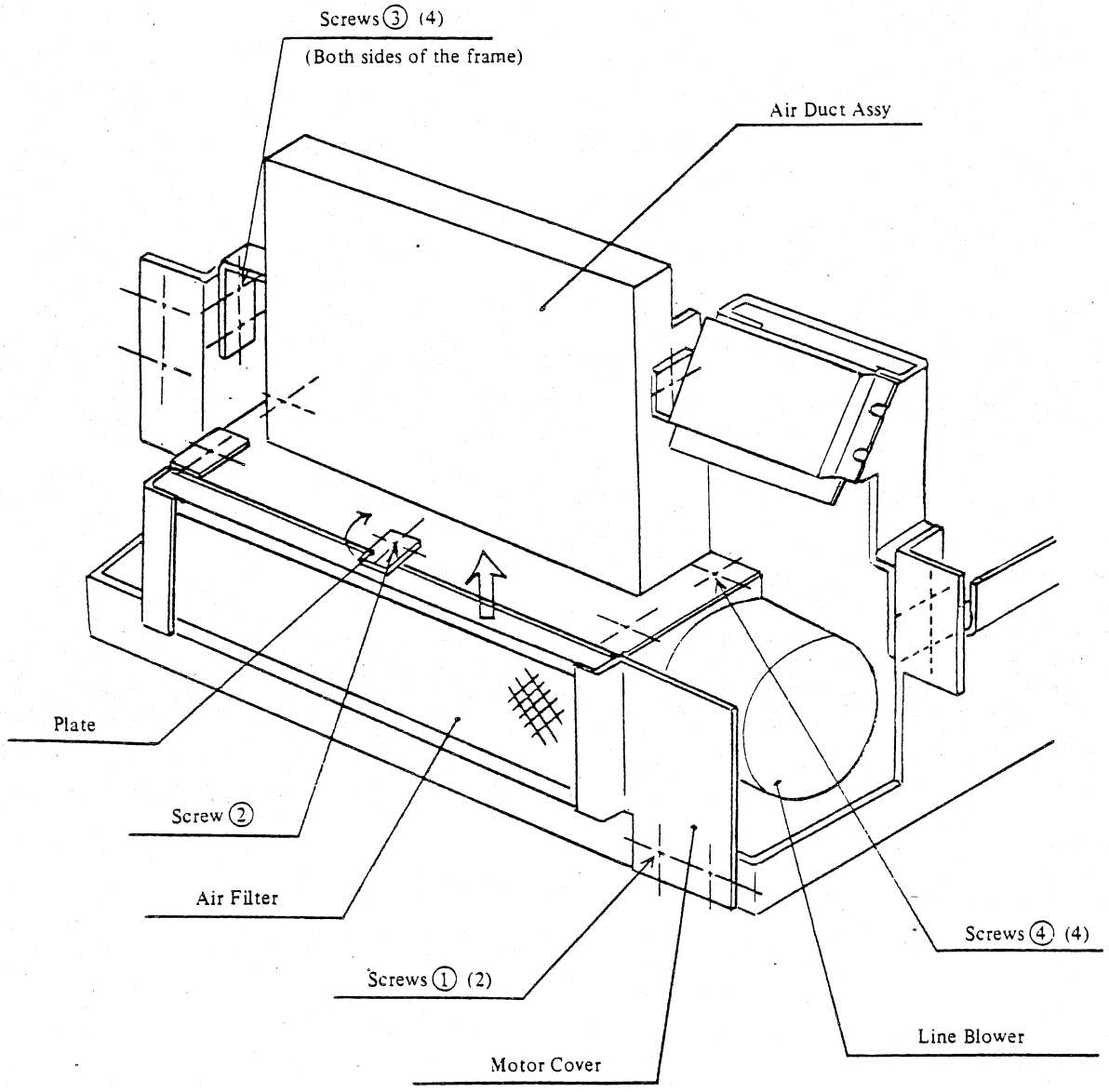
13.4 AIR FILTER

(1) Removal

1. Remove the front panel. (Refer to 13.3-(1))
2. Loosen a screw and rotate the plate.
3. Remove the Air Filter by pulling it in directions of arrow in Figure 13.4-1.

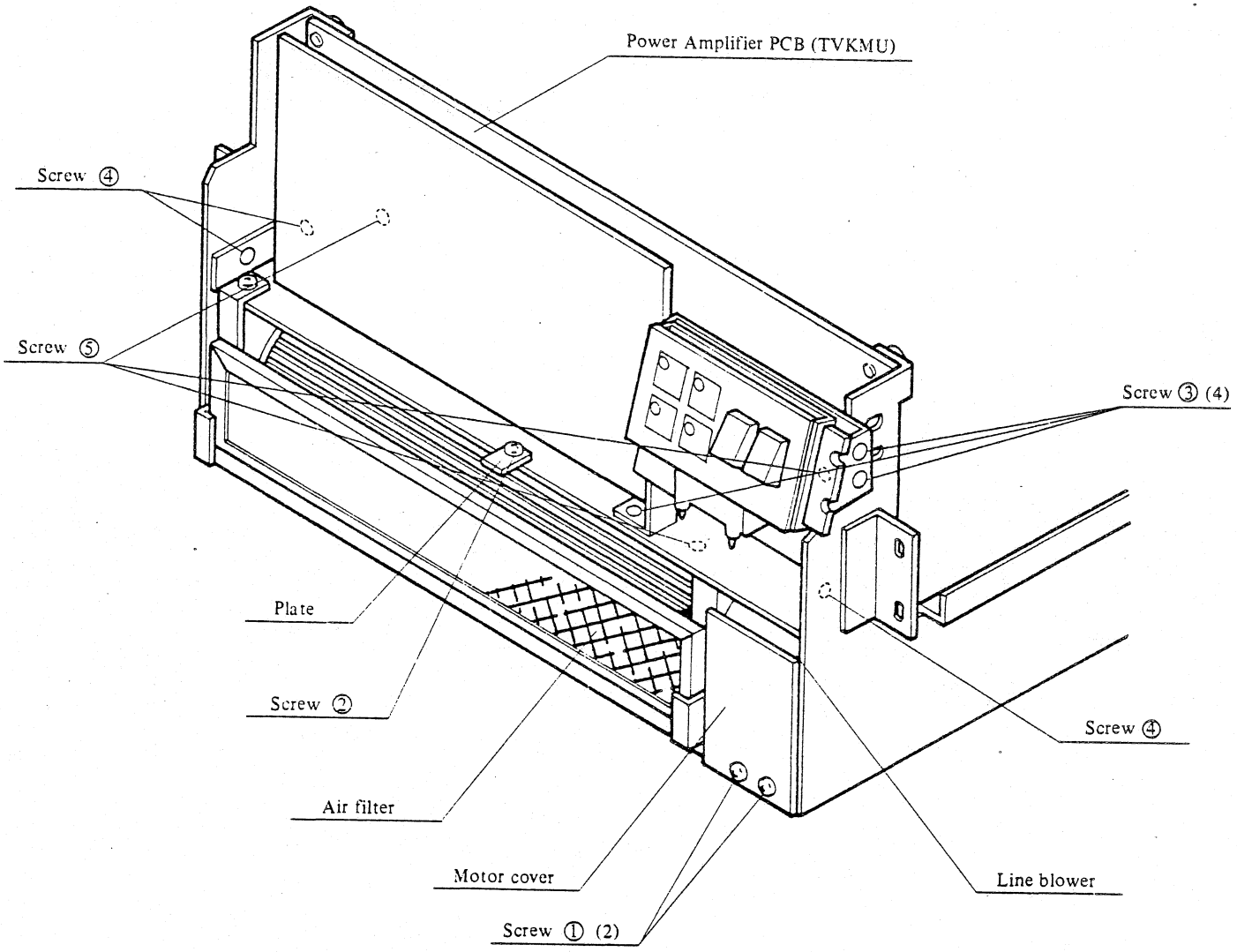
(2) Installation

1. Insert the Air Filiter in front of the Line Blower.
2. Rotate the plate to upper position of the Air Filter and fasten the screw.
3. Install the front Panel (Refer to 13.3-(2))



(a) Old version

Figure 13.4-1 Air Filter and Line Blower Replacement



(b) New version

Figure 13.4-1 - continued

13.5 LINE BLOWER

13.5.1 Old version (Refer to Figure 13.4-1 (a))

(1) Removal

1. Remove the front Panel (Refer to 13.3-(1)).
2. Remove the 2 screws (①) holding the motor cover and remove this cover.
3. Rotate the screw (②) and remove the air filter.
4. Remove the 4 screws (③).
5. Disconnect the motor plug, CNP71. Remove the 4 screw (④) and lift the air duct assy slightly, and remove the line blower forward.

(2) Installation

1. Follow, in reverse order, the procedure for line blower removal.

13.5.2 New version (Refer to Figure 13.4-1 (b))

(1) Removal

1. Remove the front Panel (Refer to 13.3-(1)).
2. Remove the 2 screws (①) holding the motor cover and remove this cover.
3. Rotate the screw (②) and remove the air filter.
4. Remove the 4 screws (③), holding the operator panel bracket and remove this panel assy.
5. Remove the TVKMU pulling out two fastening latches.
6. Remove the 4 screws (④).
7. Disconnect the motor plug, CNP71. Remove the 4 screw (⑤) and remove the line blower forward.

(2) Installation

1. Follow, in reverse order, the procedure for line blower removal.

13.6 BACK PANEL (BQGMU)

(1) Removal

1. Remove the PCBs from the card cage.
2. Remove screws (2) and then, lift the card cage vertically. Rotate over the side and remove all connectors (9) to back panel.
3. Remove nuts (4) washers (8) (Refer to Figure 13.6-1).
4. Remove the card cage and 7 screws (7).
5. Remove the back panel.

(2) Installation

1. Follow, in reverse order, the procedure for back panel removal.

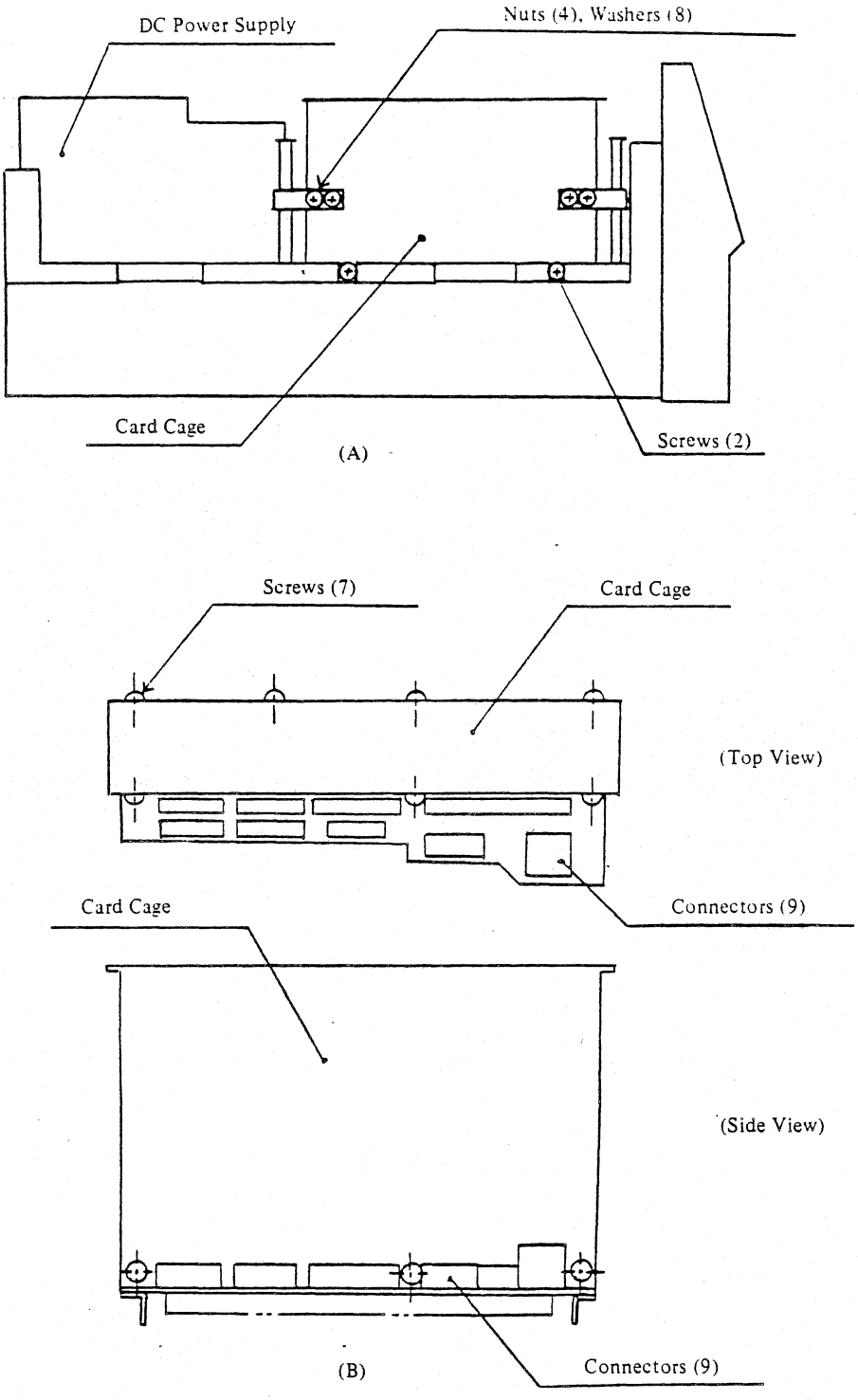


Figure 13.6-1 Back Panel Replacement

13.7 HOUR METER

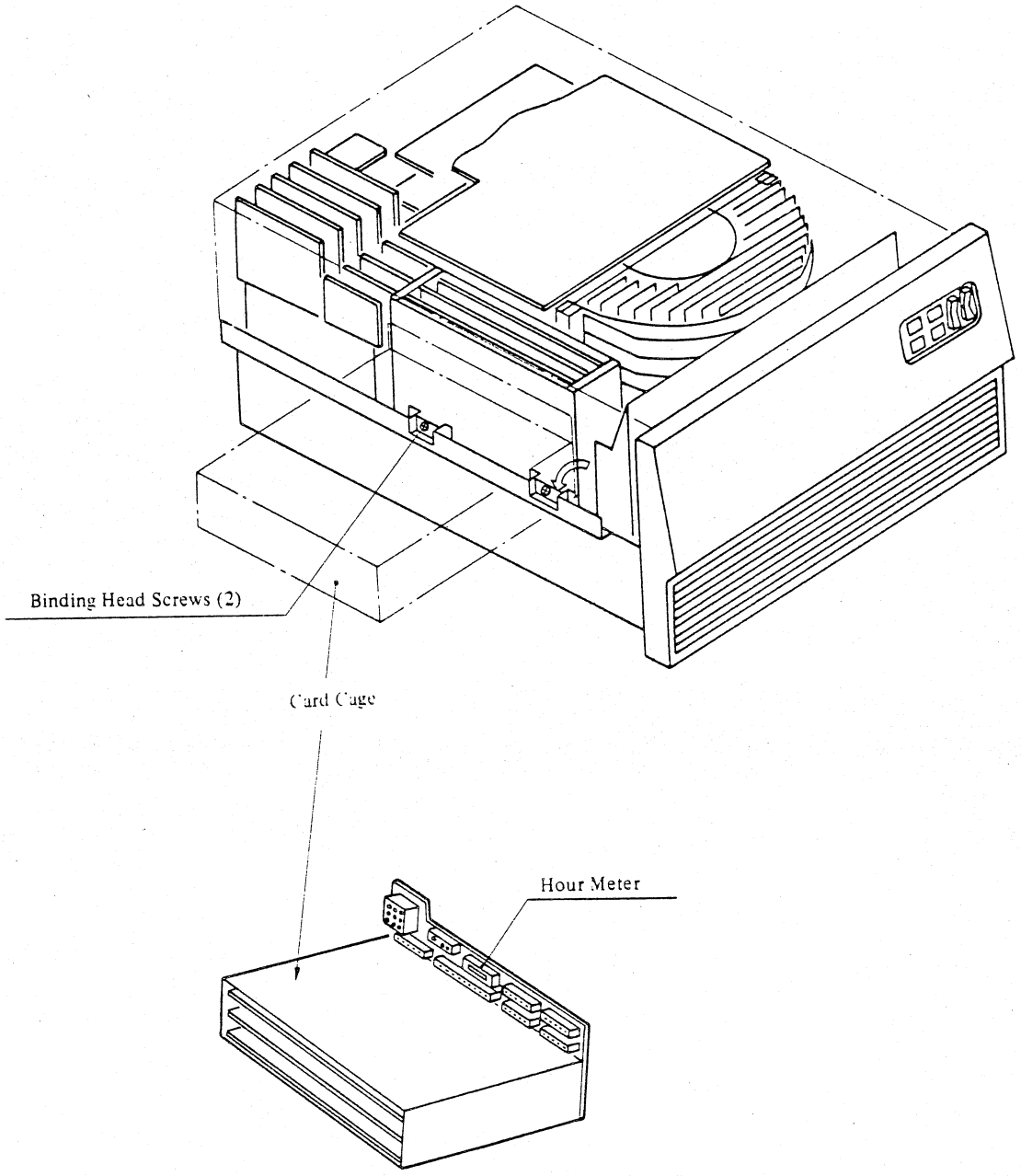
(1) Installation

1. Remove 2 binder-head screws holding the card cage.
2. Lift the card cage vertically and rotate over the side.
3. Install the Hour Meter in the connector, as indicated in Figure 13.7-1.

Note: The arrow of the hour meter must be the same direction of the socket, and then if the indicator will fully change red, pull out this indicator and plug in again reversely.

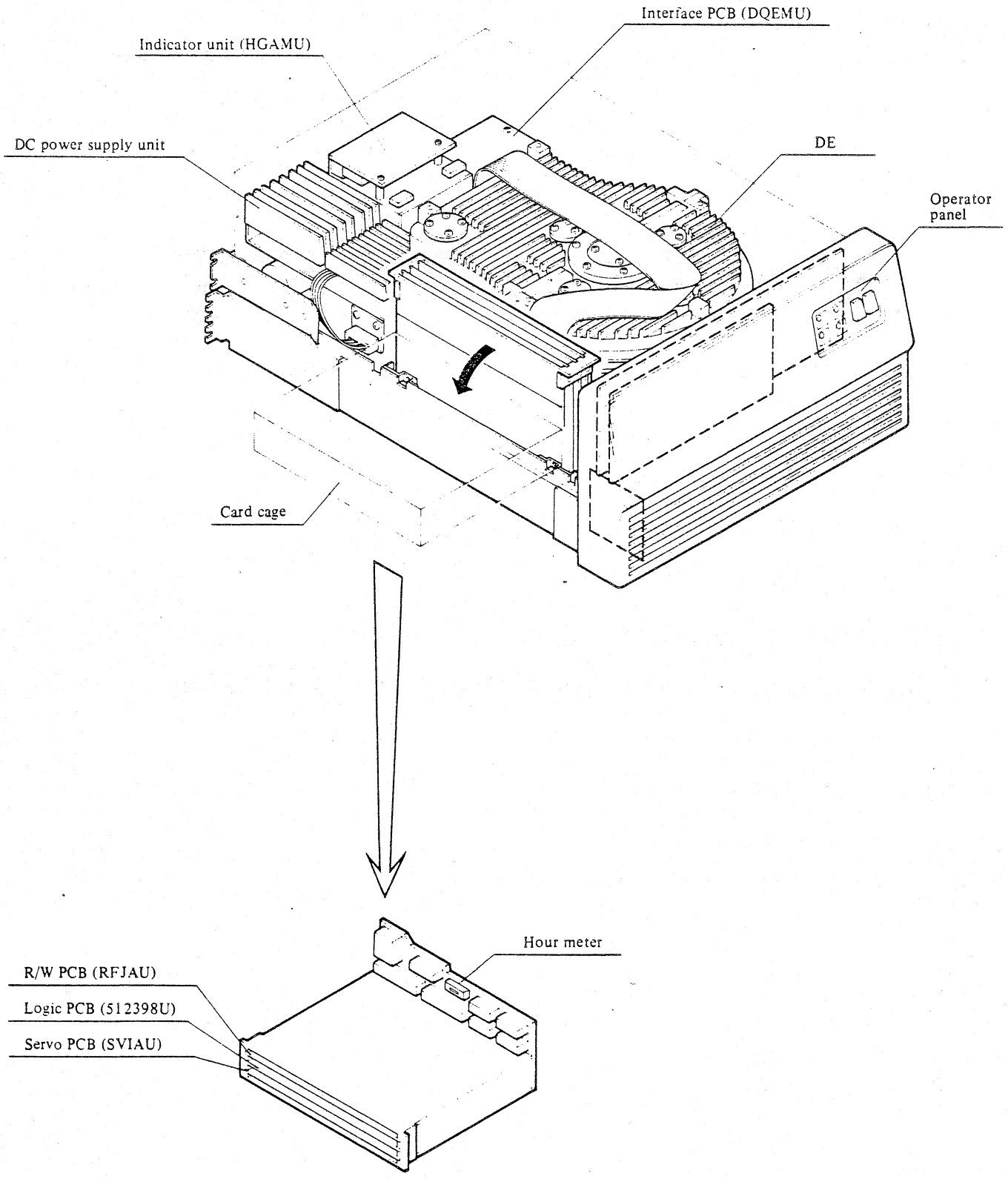
(2) Removal

Follow, in reverse order, the instructions for installation.



(a) Old version

Figure 13.7-1 Installation of Hour Meter



(b) New version

Figure 13.7-1 - Continued

13.8 DUAL CHANNEL OPTION

(1) Installation

1. Remove the TVHMU PCB. (Refer to 13.2-(1)) (Old version only)
2. If standoffs are not already in place on interface PCB (DQEMU), remove the 4 screws holding DQEMU and install 4 standoffs.
3. Disconnect CNP44, CNP45 and CNP62/46 cables.
4. Connect jumper cables (between the interface and dual channel PCBs) in the headers on the interface PCB (DQEMU).
5. Install dual channel PCB (DQFMU) on the 4 standoffs and secure with 4 screws.
6. Connect the other end of the jumper cables from DQEMU to CNP54, CNP55 and CNJ62 of the DQFMU PCB.
7. Connect cables CNP44, CNP45 and CNP62/46 to CNP57, CNP59 and CNJ56.
8. Install the TVHMU PCB (Refer to 13.2-(2)). (Old version only)

(2) Removal

Follow, in reverse order, the instructions for installation.

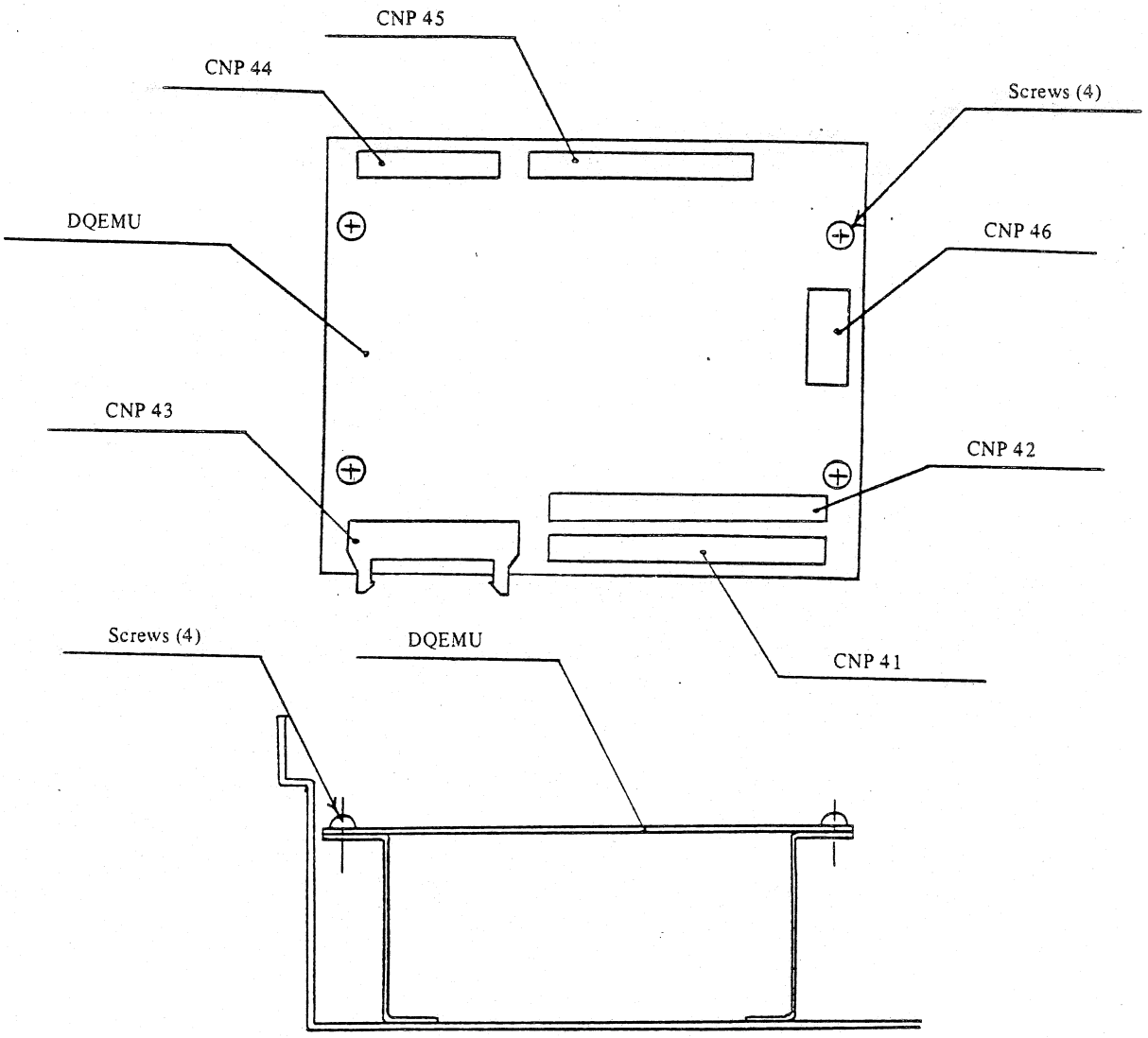


Figure 13.8-1 Installation of Dual Channel Option

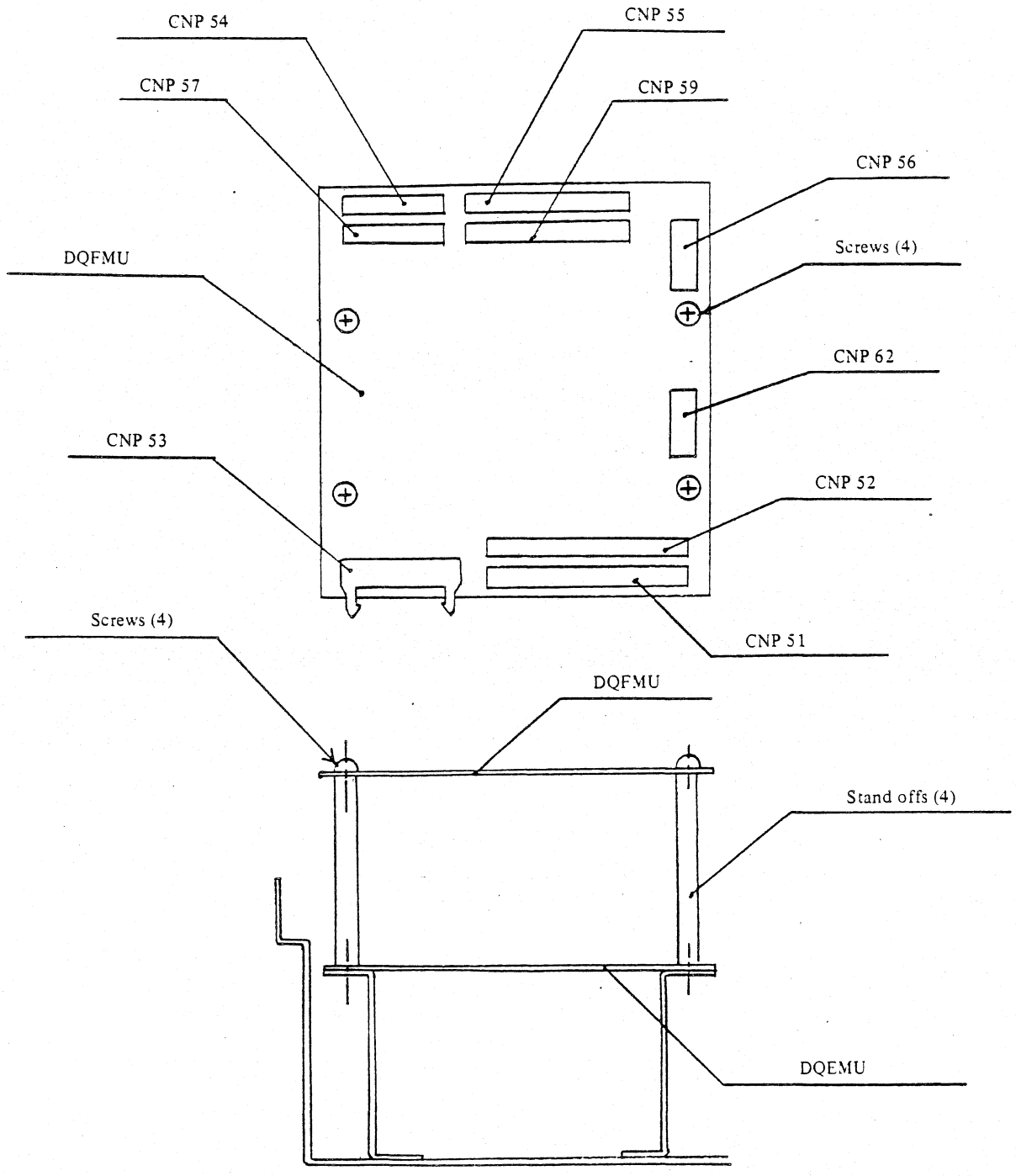


Figure 13.8-2 Installation of Dual Channel Option

13.9 DC POWER SUPPLY UNIT

(1) Removal

1. Remove the PCB (HGAMU).
2. Remove connectors (CNP03, CNP61, CNP62, CNP64, CNP65, CNJ66) that go out from the power supply unit.
3. Remove the screws (2) which hold the power supply unit to the frame of the drive.
4. Carefully slide the power supply unit back and remove.
5. Remove the input AC power cable. (Refer to 13.10)

(2) Installation

Follow, in reverse order, the procedure for DC power supply removal.

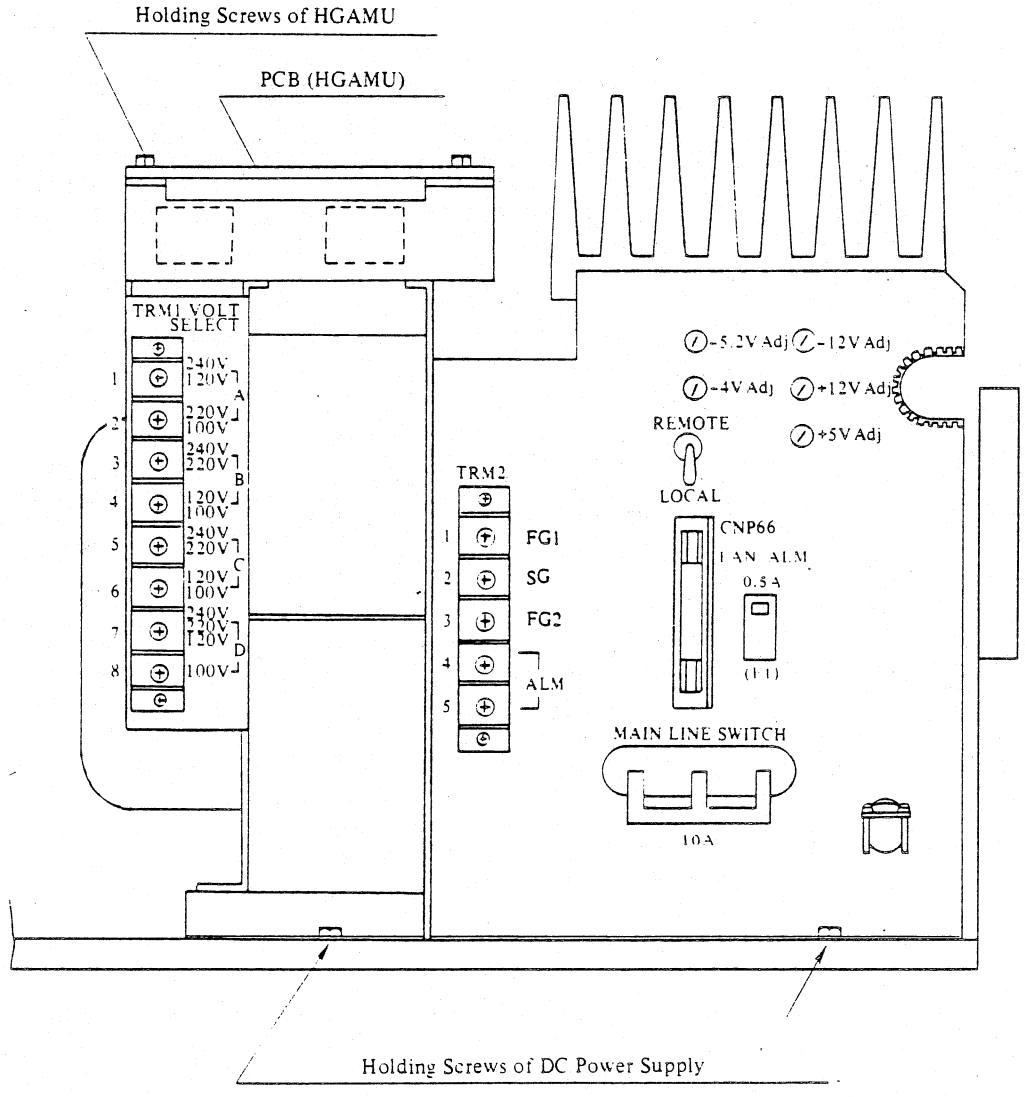


Figure 13.9-1

(3) Adjustment of DC Voltages

Check the DC voltages at the check pins of Back Panel (BQGMU) using digital multimeter. The check pins' configuration is shown in Figure 13.9-2. If a DC voltage is out of the acceptable range of Table 13.9-1, readjust the corresponding RV shown in Figure 13.9-1.

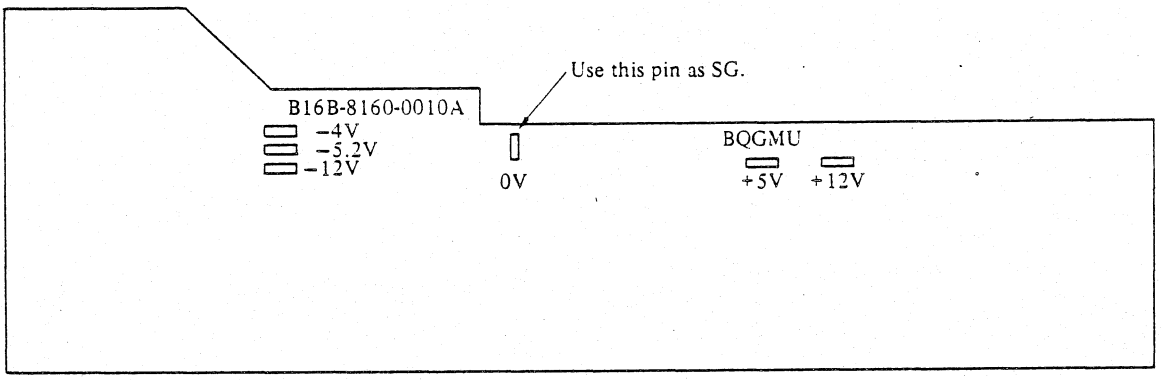


Figure 13.9-2 Top View of Back Panel

Table 13.9-1 Acceptable Range of DC Voltages

DC Voltage	Acceptable Range
+12 V	11.4 ∿ 12.6 V
+5 V	4.75 ∿ 5.25 V
-4 V	-3.8 ∿ -4.2 V
-5.2 V	-4.94 ∿ -5.46 V
-12 V	-11.4 ∿ -12.6 V

13.10 POWER CABLE

CAUTION: Check to be certain that the AC cable is not plugged in.

(1) Removal

1. Remove the DC power supply (Refer to 13.9).
2. Remove the side cover by loosening 4 screws as shown in Figure 13.10-1.
3. Loosen cable clamp.
4. Remove terminals A and B (AC power) and terminal G (ground).
5. Remove the AC cable.

(2) Installation

1. Follow, in reverse order, the procedure for power cable removal.

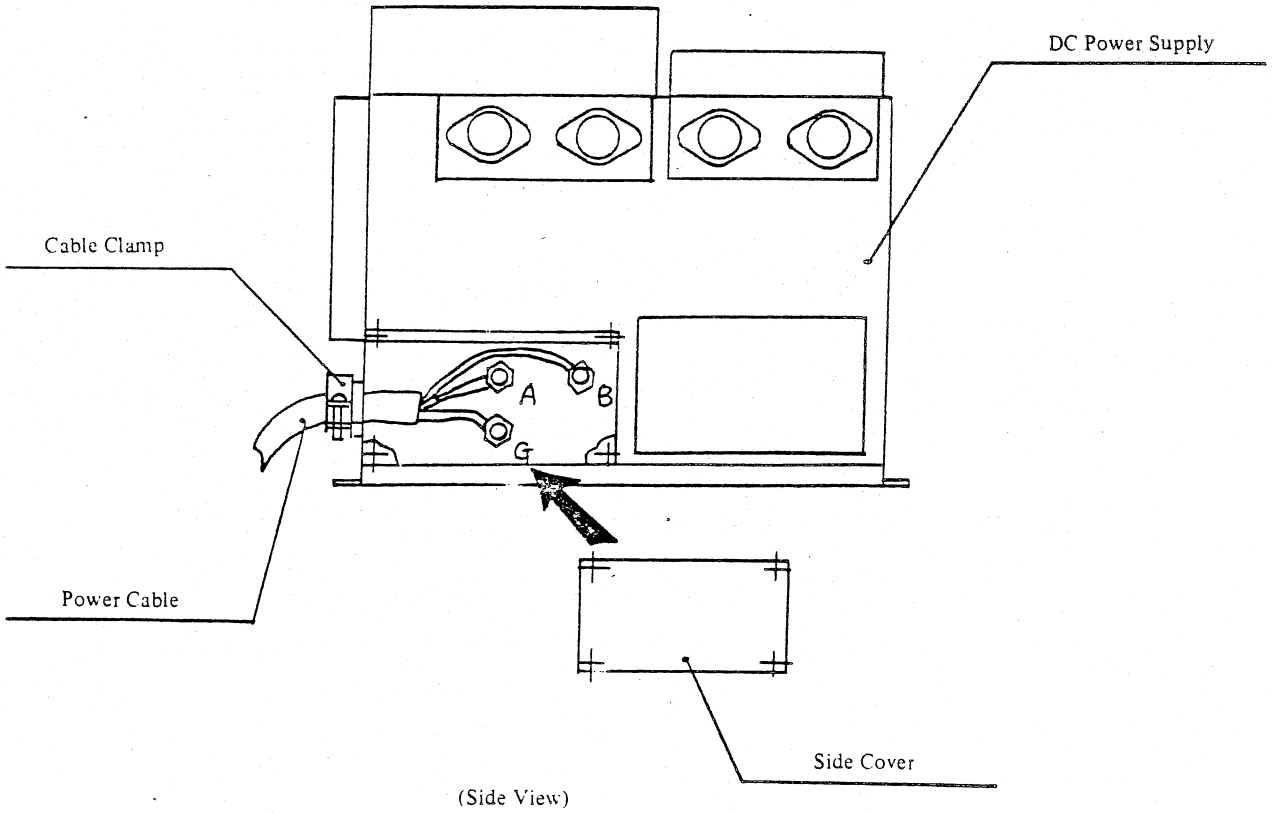


Figure 13.10-1 Installation of a Power Cable

(3) Adjustment of DC Voltages

Check the DC voltages at the check pins of Back Panel (BQGMU) using digital multimeter. The check pins' configuration is shown in Figure 13.9-2. If a DC voltage is out of the acceptable range of Table 13.9-1, readjust the corresponding RV shown in Figure 13.9-1.

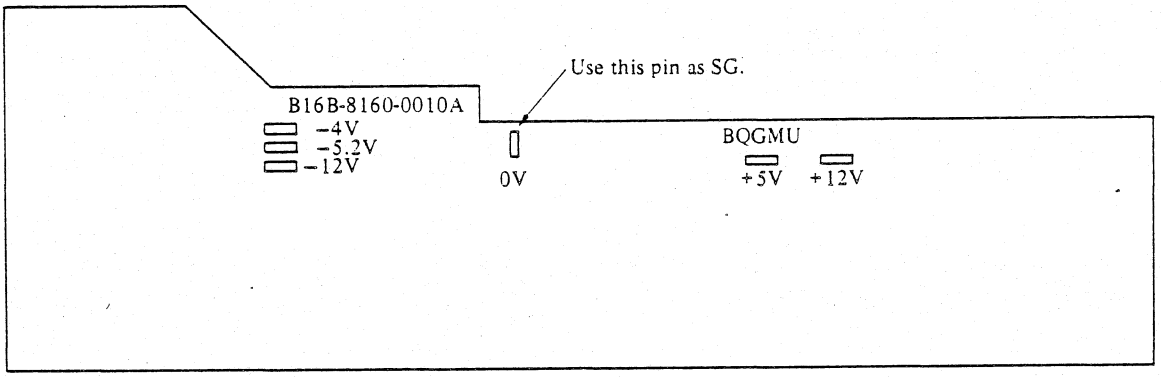


Figure 13.9-2 Top View of Back Panel

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+12 V	11.4 ∿ 12.6 V
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-5.2 V	-4.94 ∿ -5.46 V
-12 V	-11.4 ∿ -12.6 V

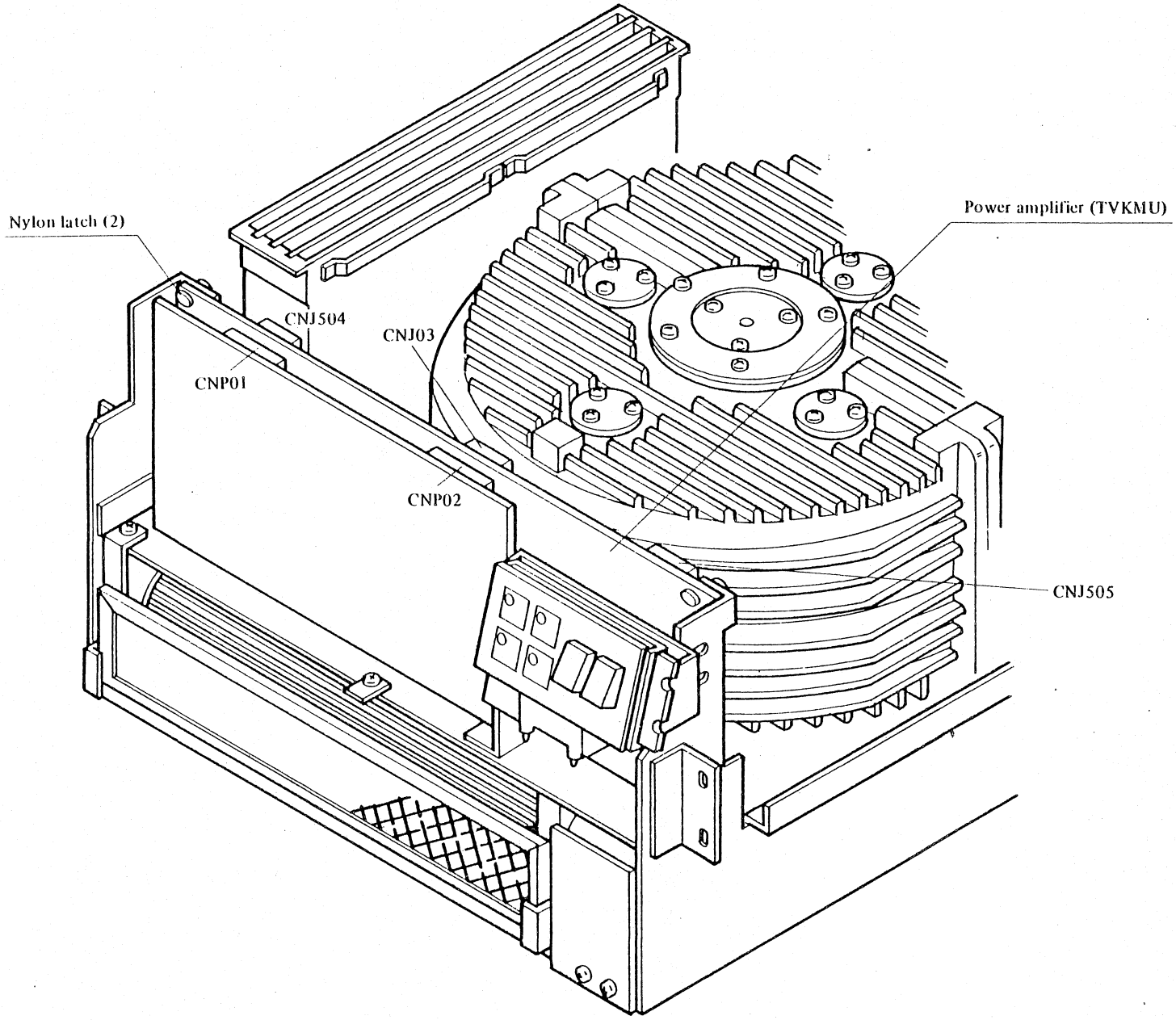


Figure 13.11-1 Power amplifier replacement

CHAPTER 14 ELECTRICAL TEST AND ADJUSTMENT

14.1 GUIDE TO PCBs AND LOGIC DIAGRAMS (SCHEMATICS)

Circuit diagrams contain input and output signal names (mnemonics), coordinate locations of ICs, input origines, destination coordinates of output signals, IC pin numbers and IC types. Figure 14.1-1 shows how to read circuit diagrams.

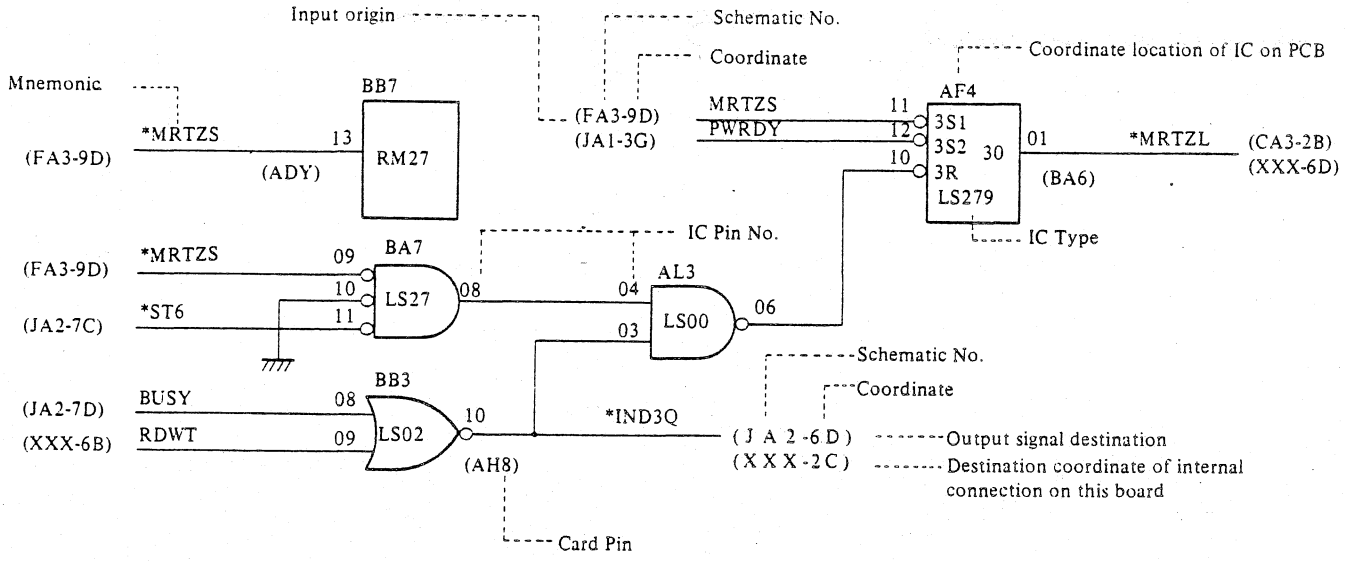


Figure 14.1-1 Logic Symbols

Figure 14.1-2 shows the IC location of PCB 512398.
Figure 14.1-3 shows the pin numbering of PCB.
Figure 14.1-4 shows the pin numbering of Back Panel.

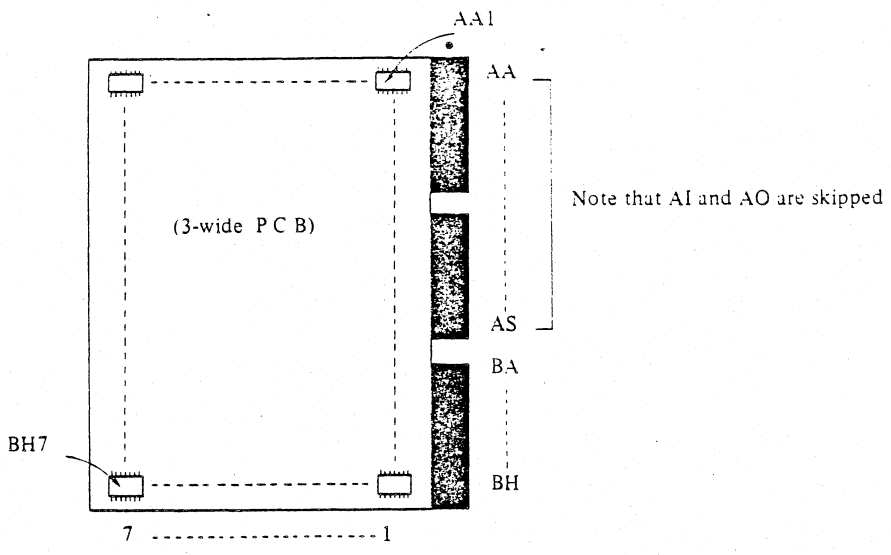


Figure 14.1-2 IC Location

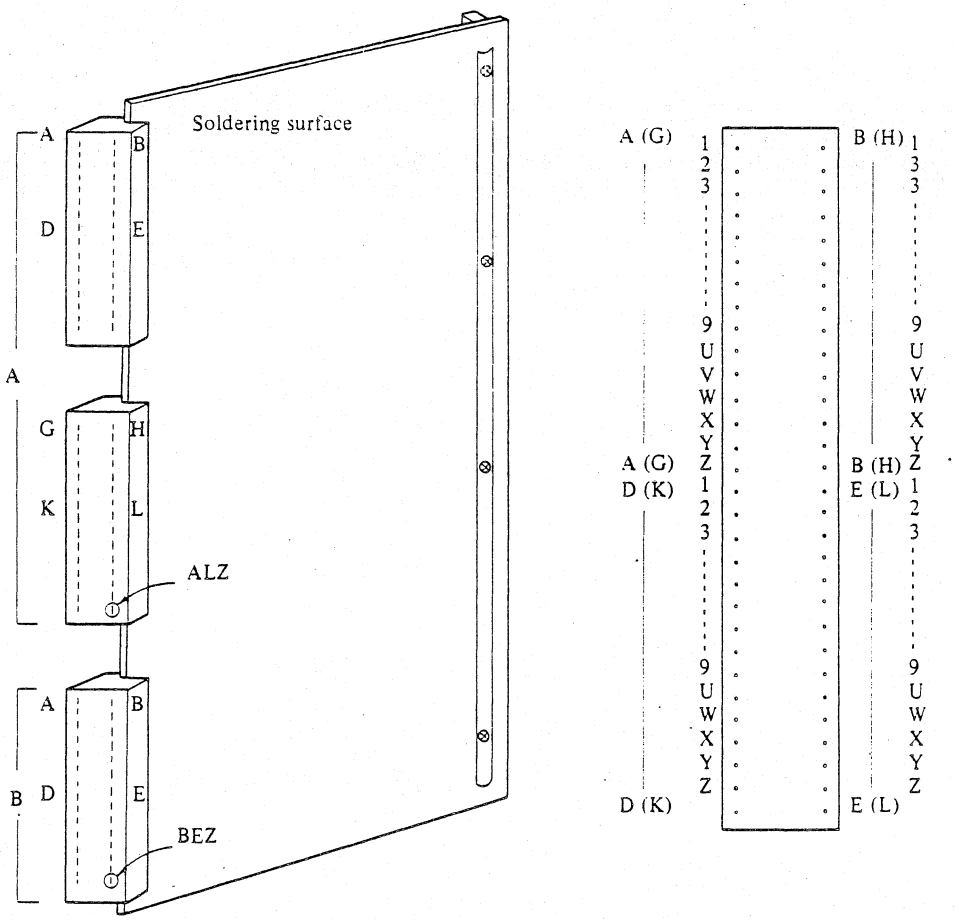


Figure 14.1-3 PCB Pin Numbering

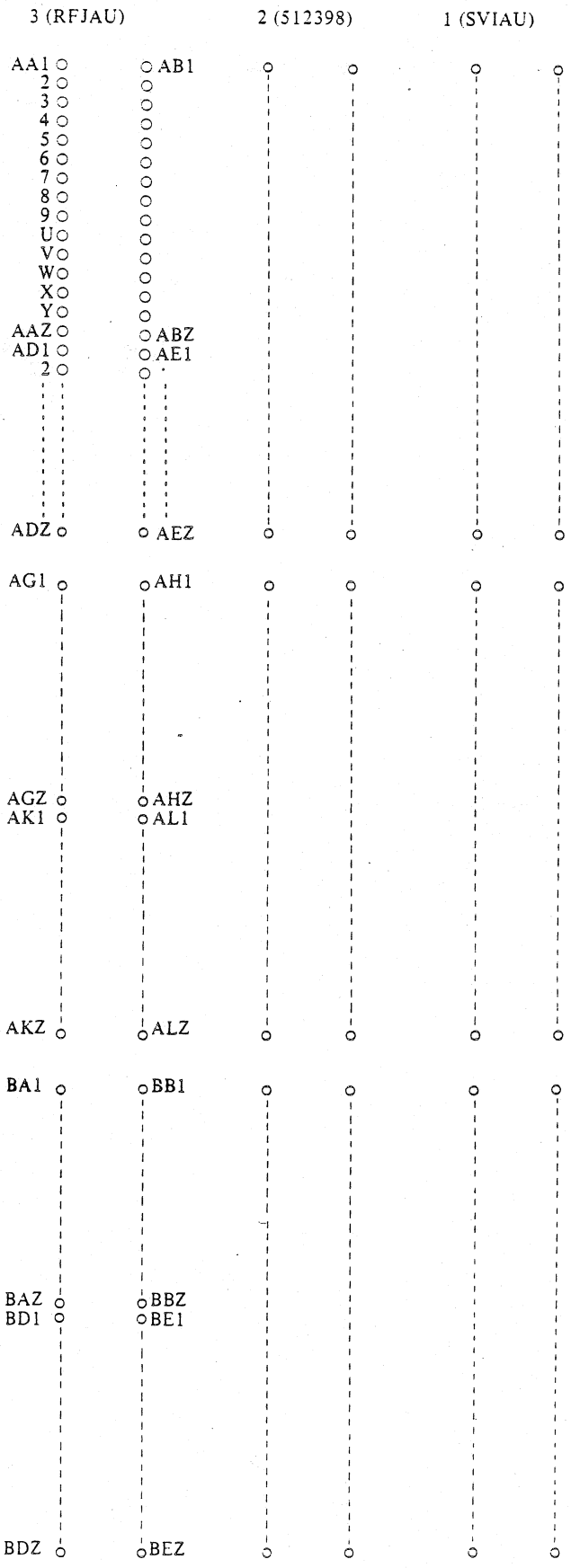


Figure 14.1-4 Back Panel Pin Numbering (Bottom View)

14.2 ADJUSTMENT OF SERVO CIRCUIT

(1) Introduction

The following flow chart shows how to adjust and test the servo circuit.

If none of variable resistors have been adjusted, both "Static Adjustment" and "Dynamic Adjustment" are necessary. After changing the DE or PCB SVIAU, only "Dynamic Adjustment" is needed, that is, RVs 1, 2, 3, 10 and 13 are needed to be adjusted.

Prior to the "Static Adjustment", stop the spindle, power off and pull out connector CNP504 (Output cable of Power Amplifier to the rotary actuator).

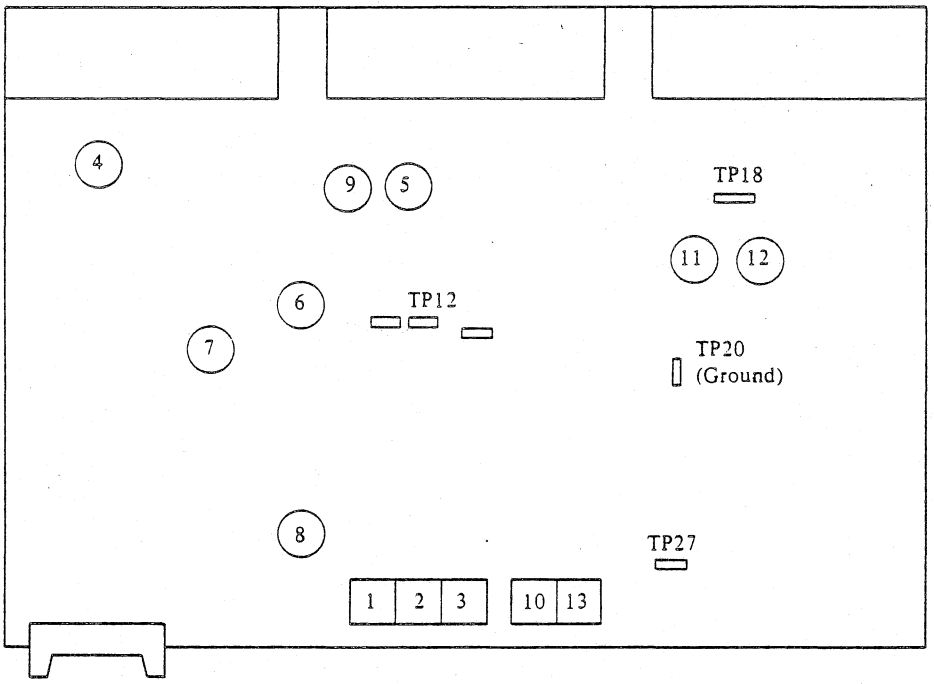


Figure 14.2-1 RVs and TPs on PCB SVIAU/01

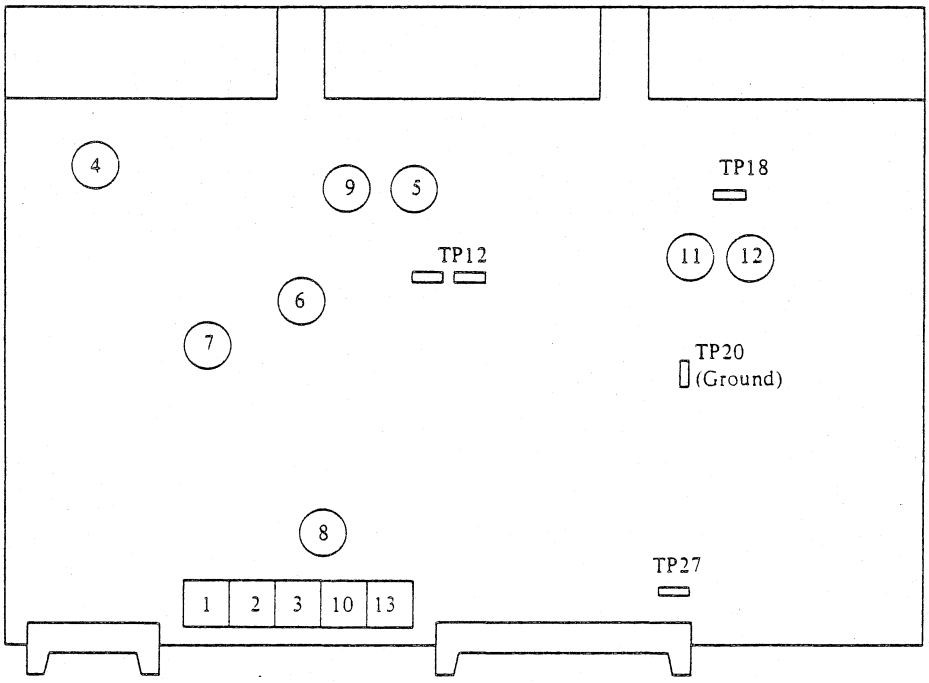


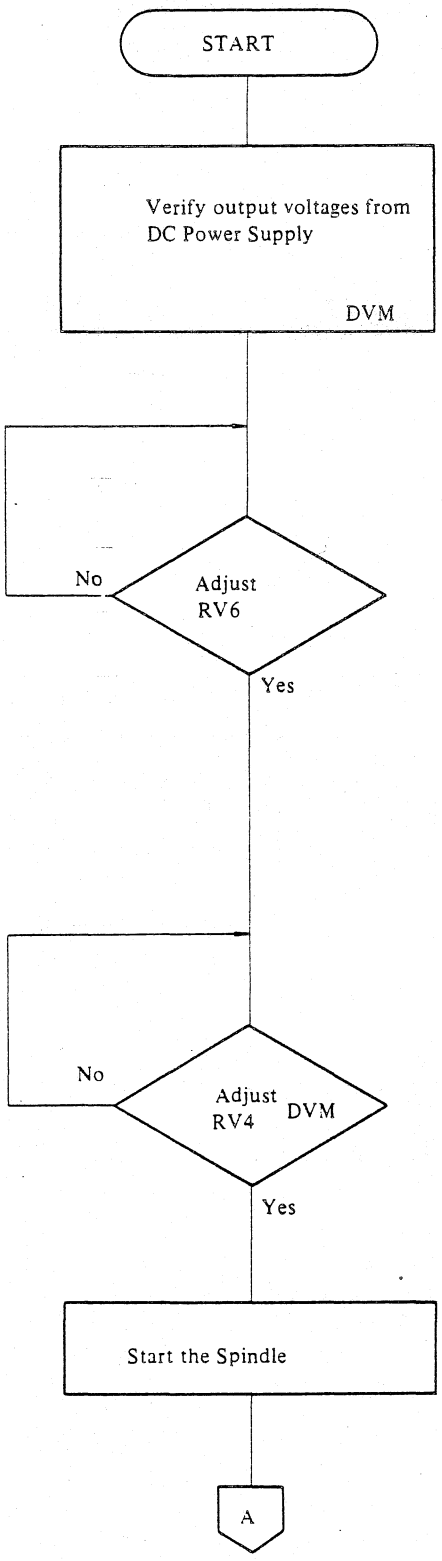
Figure 14.2-2 RVs and TPs on PCB SVIAU/02

Table 14.2-1 Function of RVs

RV No.	Function/Adjustment	Sealed*
1	AGC Amplifier gain	No
2	Over - shooting	No
3	Access time	No
4	-4V	Yes
5	Offset voltage of the desired velocity curve	Yes
6	VCO free - running frequency	Yes
7	Timer - Gate pulse width	Yes
8	Sync. - Gate timing	Yes
9	D/A Converter gain	Yes
10	Velocity offset	No
11	Access Time Out pulse width	Yes
12	Track Following Timer pulse width	Yes
13	Settling in Fine Control	No

* Do not touch the sealed RVs unless adjustments are required.

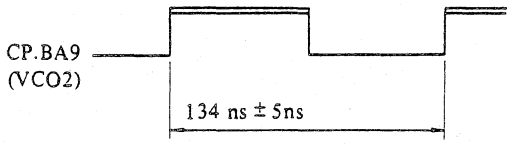
(2) STATIC ADJUSTMENT



The card cage must be opened (lifted and rotated 90°) to expose the Back Panel.

+12V; CP.AA1
+5V; CP.AAZ
-5.2V; CP.ABZ
-12V; CP.AEZ
(Ground; CP.AD2)

VCO Free-Running frequency
Connect CP.AEW to ADW (Ground)



After the adjustment, disconnect CP.AEW from Ground.

CP.AA6; -4V ±0.1V
CP.AA5; +6V ±0.1V
(Ground; CP.AD2)

Turn on the Start/Stop switch on the operator panel and check that the spindle is rotating.

Figure 14.2-3 Static Adjustment of Servo Circuit (Sheet 1 of 5)

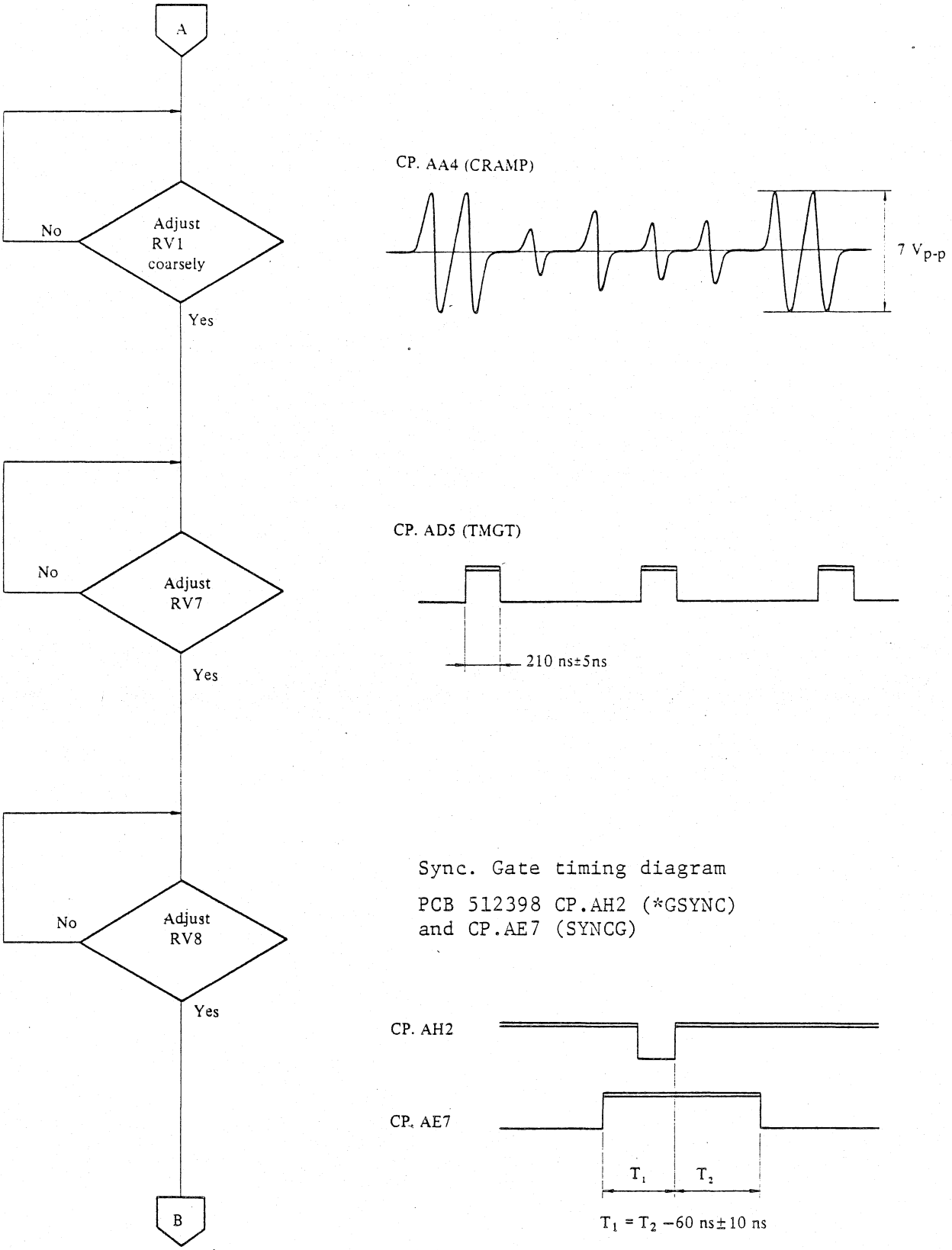


Figure 14.2-3 Static Adjustment of Servo Circuit (Sheet 2 of 5)

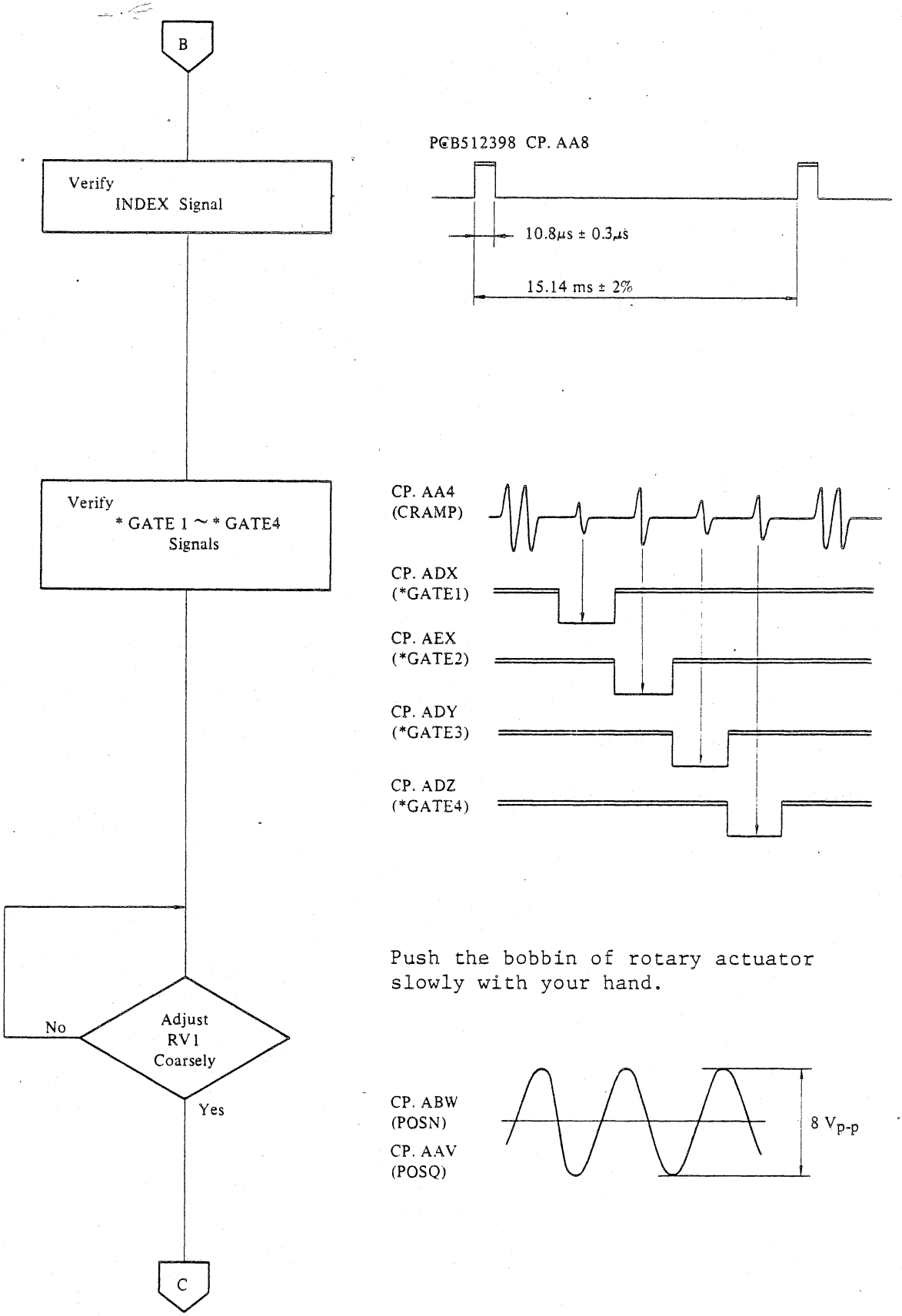
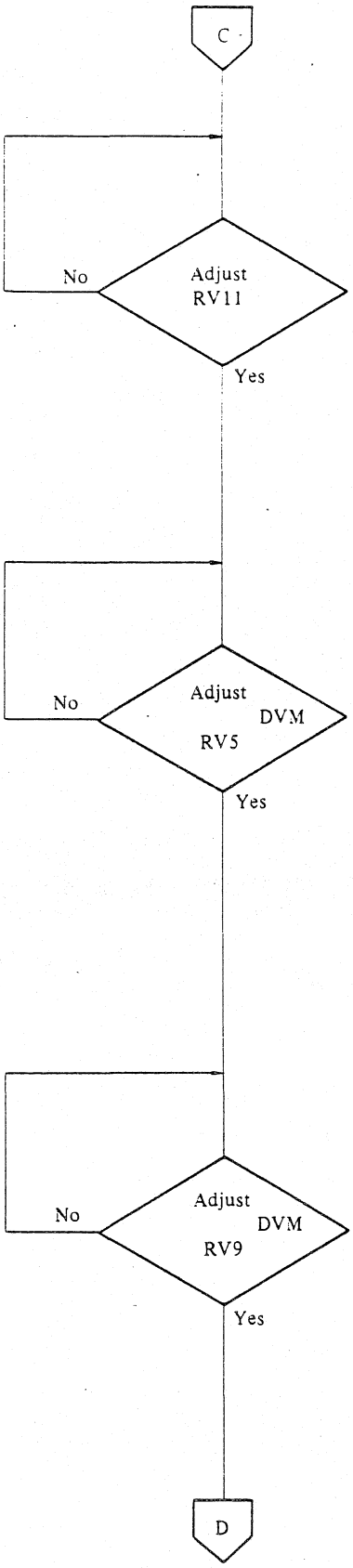
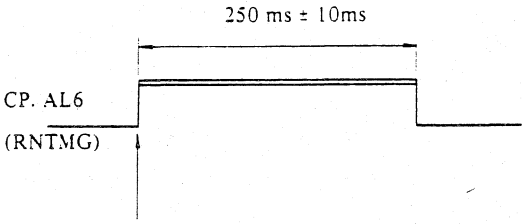


Figure 14.2-3 Static Adjustment of Servo Circuit (Sheet 3 of 5)



Access Time Out



Turn on the MRTZ switch on the PCB HGAMU.

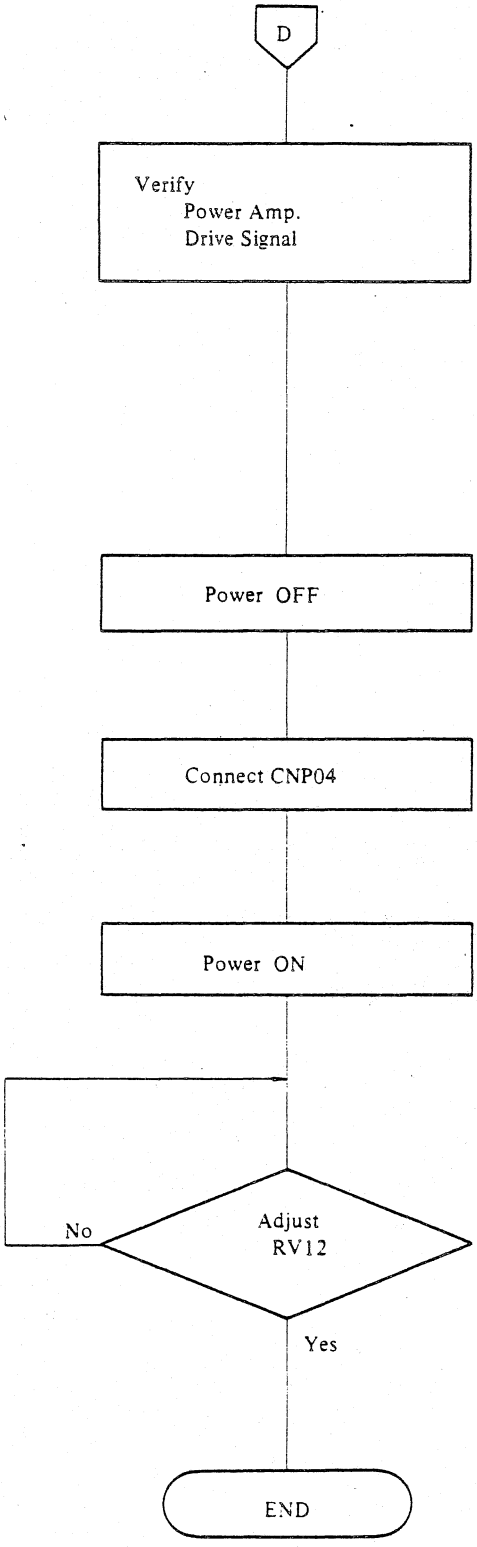
Offset voltage of the desired velocity curve

TP12, CP.AB3; 0V ±10mV
(FG)
When GD1 ∿ GD128 are all inactive.

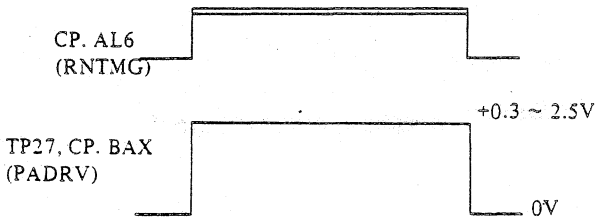
Digital to analog converter gain

TP12, CP.AB3; +6V ±0.1V
(FG)
When the difference register contains a value greater than 144.

Figure 14.2-3 Static Adjustment of Servo Circuit (Sheet 4 of 5)



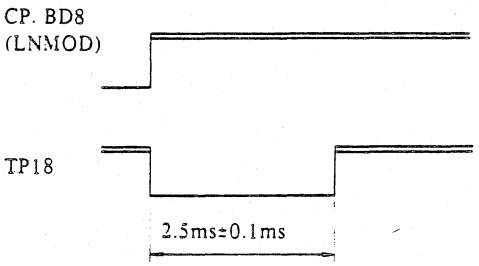
Turn on the MRTZ switch on the PCB HGAMU.



Connect the output cable of Power Amplifier to the rotary actuator.

Turn on the MRTZ switch on the PCB HGAMU.

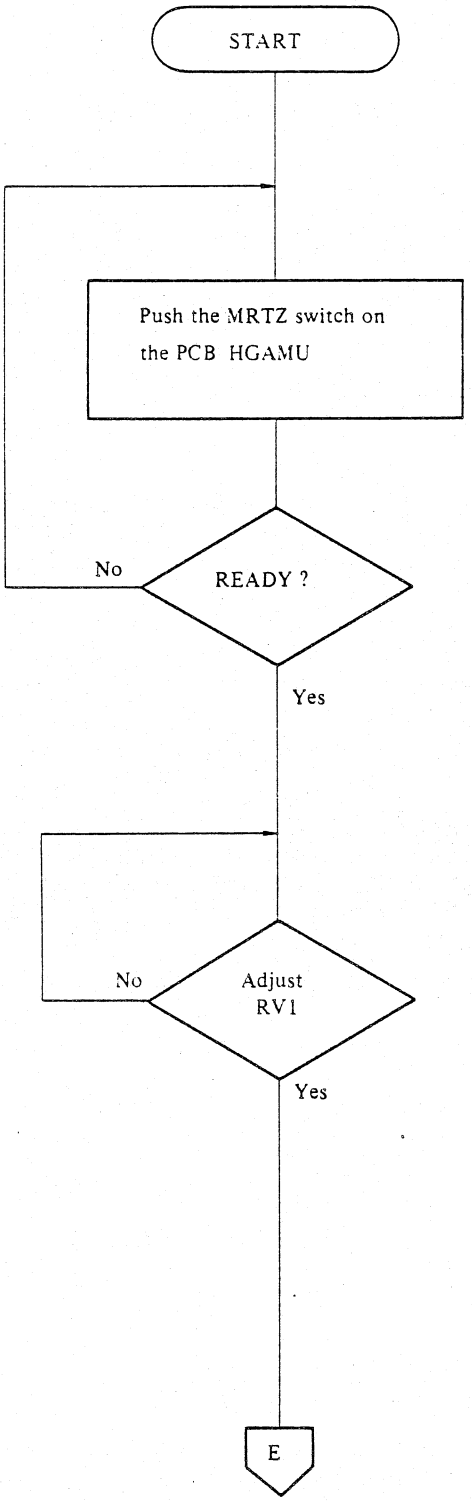
Track following Timer pulse width



Adjust RV3 by trial and error until the READY lamp light after RTZ operation.

Figure 14.2-3 Static Adjustment of Servo Circuit (Sheet 5 of 5)

(3) DYNAMIC ADJUSTMENT



Adjust RV3 by trial and error until the READY lamp on the operator panel light after RTZ operation.

Performing RTZ operation from cylinder 841 repetitively, adjust RV1 as follows.

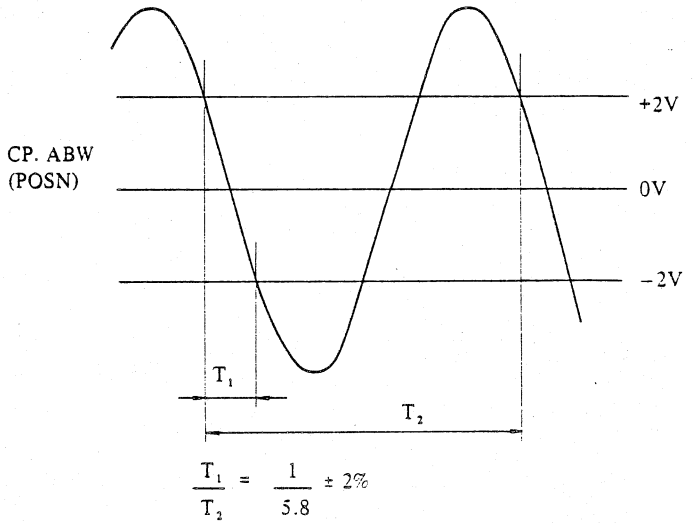


Figure 14.2-4 Dynamic Adjustment of Servo Circuit (Sheet 1 of 3)

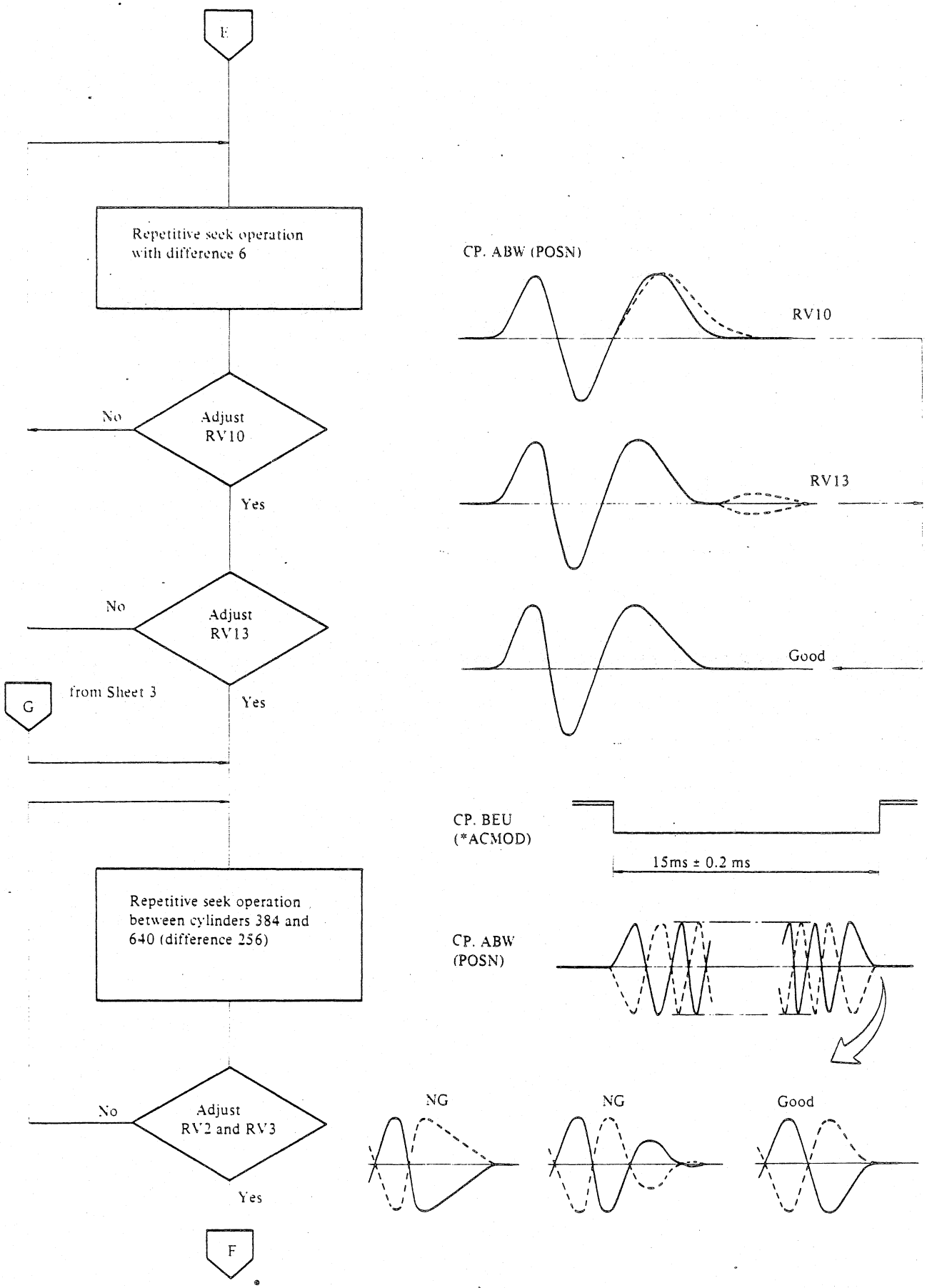
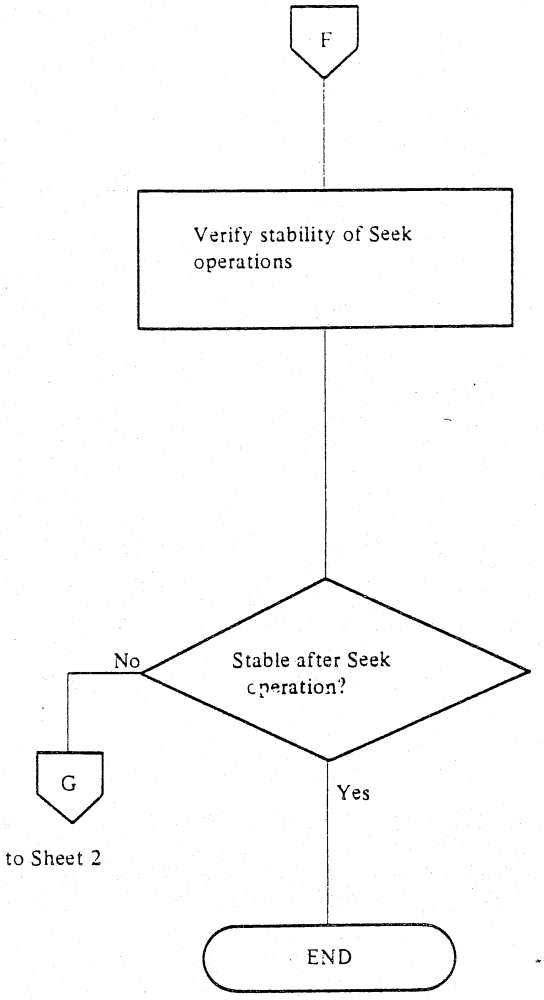


Figure 14.2-4 Dynamic Adjustment of Servo Circuit (Sheet 2 of 3)



Verify stability and vibration while performing seek operations by varying seek distance and time interval.

CP.AL3 (FNPOS)

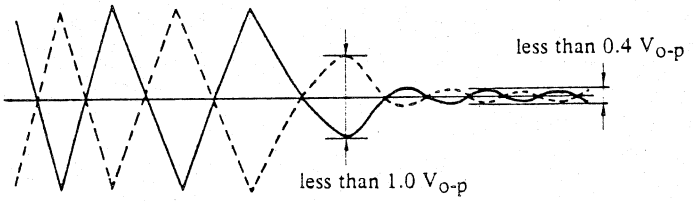


Figure 14.2-4 Dynamic Adjustment of Servo Circuit (Sheet 3 of 3)

14.3 ADJUSTMENT OF READ/WRITE CIRCUIT

The following describes how to adjust and test the Read/Write circuit in case none of variable resistors have been adjusted.

The card cage must be opened (lifted and rotated 90°) to expose the Back Panel.

PCB RFJAU must be inserted in Extender Unit.

Refer to Table 14.3-1 and Figure 14.3-1 for monitor point and location.

Table 14.3-1 Variable Resistors in Read/Write Circuit

Item	RV No.	Test point	Specification
-5.2V (DC Voltage)	RV1	AB2 (or W3)	-5.2V±0.2V
+6V (DC Voltage)	RV5	W15	+6V±0.2V
Balance of Read Signal	RV2	W7 W8 (ADX, AEX)	Refer to (1)
Write Current	RV3	W1 W2	Refer to (2)
Jitter of Read Signal	RV4	W49	Refer to (3)

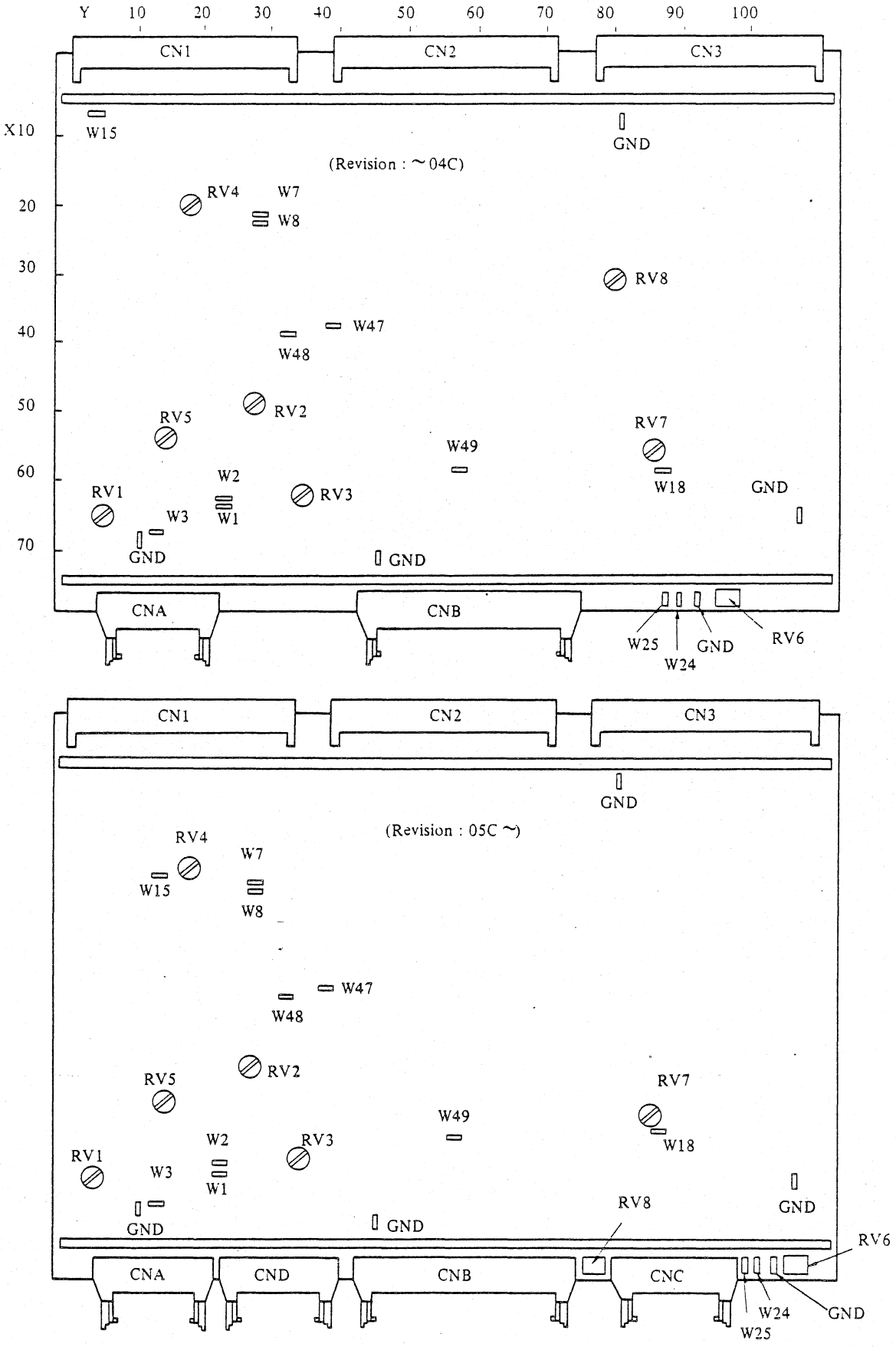


Figure 14.3-1 Variable Resistors on PCB RFJAU

(1) Balance of Read Signal (RV2)

Read the data recorded in Variable Sector Format on Cylinder 00 and Head 01, and adjust RV2 so that the read signal matches Figure 14.3-2.

If the data is recorded in Sector Format, the AMGCL signal is clamped low and the Differencial Output continues 2.6 Vp-p ±10%.

Verify that, this balanced waveform is maintained on Cylinder 256, 512 and 841 for Head 00 and 01.

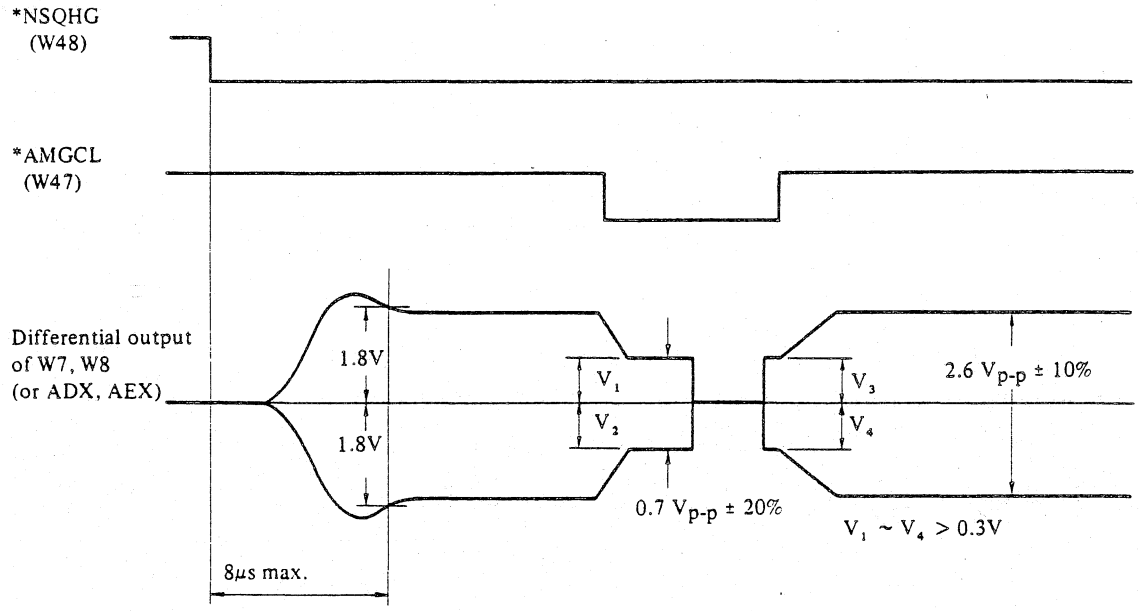


Figure 14.3-2 Balance of Read Signal

(2) Write current (RV3)

Adjust RV3 so that the differential output voltage V5 (W1 and W2) is 400 mV ±20 mV while writing any data on Cylinder 00 Head 01 (Refer to Figure 14.3-3). Verify that, the voltage is 500 mV ±50 mV on Cylinder 00 Head 00.

For Fixed Head Option, verify that the voltage is 800 mV ±80 mV at Cylinder 896 Head 00 and is 900 mV ±100 mV at Cylinder 897 Head 00 while writing any data.

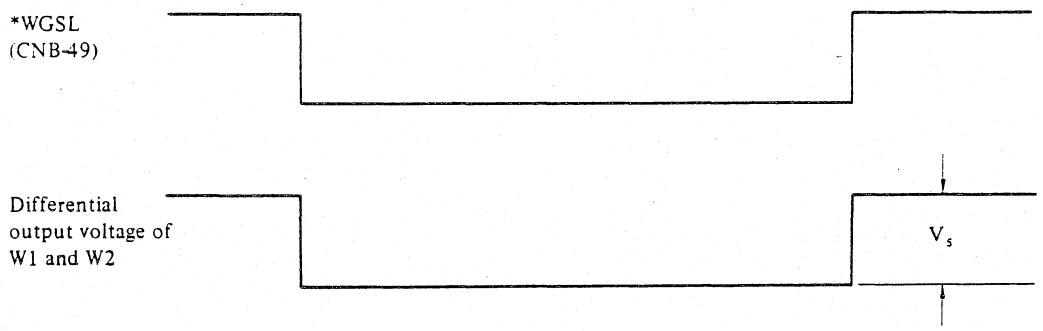


Figure 14.3-3 Write Current Adjustment

(3) Jitter of Read Signal (RV4)

Read the data pattern of "AAAA --- AA", recorded on Cylinder 00 and Head 00.

Adjust RV4 to minimize the jitter at the negative-going edge of the pulses as shown in Figure 14.3-4.

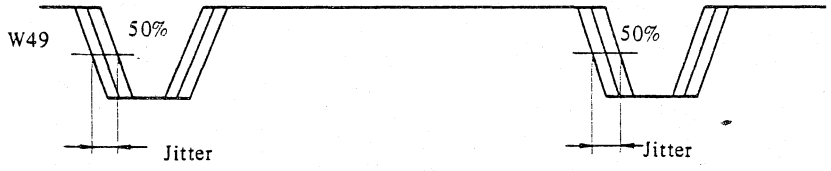


Figure 14.3-4 Jitter of Read Signal Adjustment

14.4 ADJUSTMENT OF VFO CIRCUIT

The following describes how to adjust and test the VFO (Modulator and Demodulator) circuit (PCB RFJAU) in case none of variable resistors have been adjusted. Refer to Table 14.4-1 and Figure 14.3-1 for monitor point and location.

Table 14.4-1 Variable Resistors in VFO Circuit

Item	RV No.	Test point	Specification
VCO Free-running Frequency	RV8	BA9 (or W24)	Refer to (1)
Reference Pulse Width	RV7	W18	Refer to (2)
Phase Adjustment	RV6	W24 W25	Refer to (3)

(1) VCO Free-running Frequency (RV8)

Connect CNB-24 (Connector B, Pin 24) to ground, and adjust RV8 so that the pulse period or frequency of BA9 or W24 matches Figure 14.4-1.

Disconnect the cable between CNB-24 and ground after adjust or confirm the item.

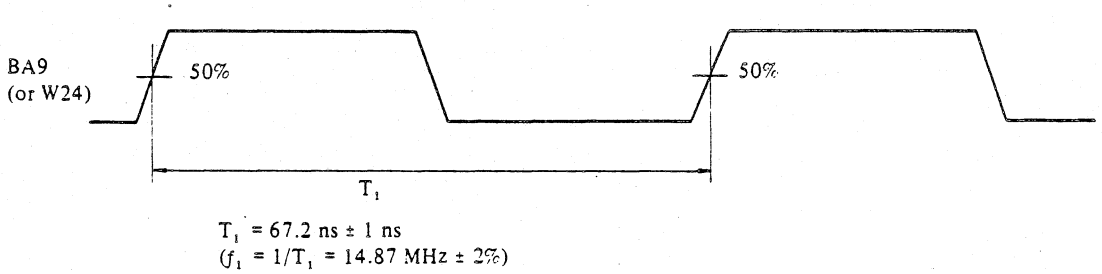


Figure 14.4-1 VCO Free-running Frequency Adjustment

(2) Reference Pulse width (RV7)

Read or write any data, and adjust RV7 so that the pulse width of W18 matches Figure 14.4-2.

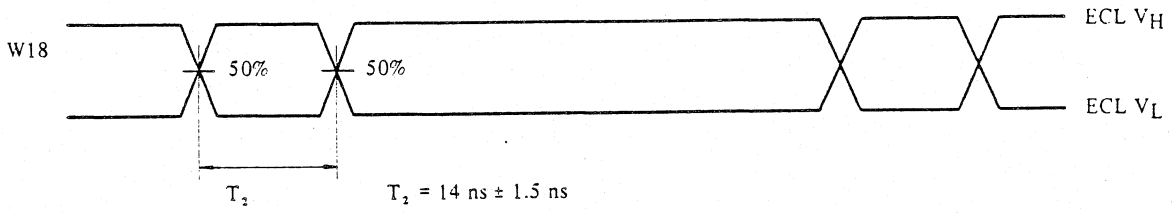


Figure 14.4-2 Reference Pulse width Adjustment

(3) Phase adjustment (RV6)

Read the data pattern of "FF...FF", and adjust RV6 so that the phase between W24 and W25 matches Figure 14.4-3.

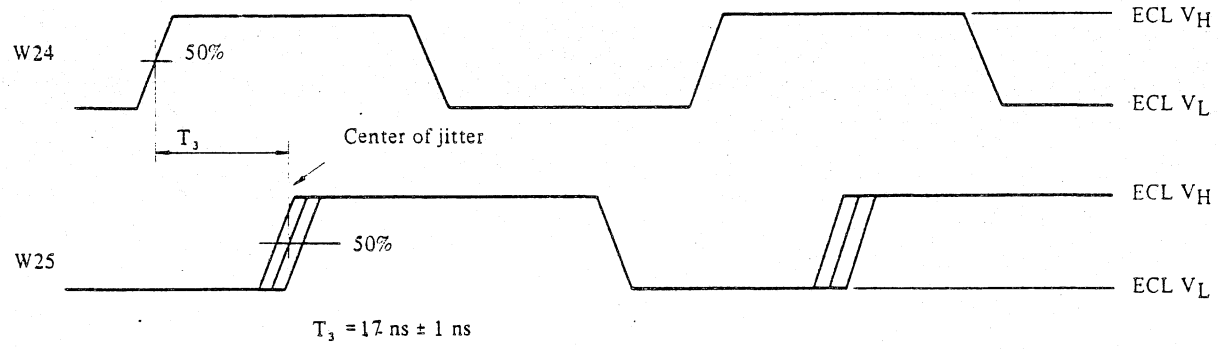


Figure 14.4-1 Phase Adjustment

CHAPTER 15 TROUBLE SHOOTING

15.1 INTRODUCTION

This section contains trouble shooting flow charts according to the error status on the disk unit and control unit.

It is recommended that before any operations, maintenance personnel read carefully Chapter 12 Maintenance and fully understand the details of the procedures and tools required.

Inspect the following items before applying power to the unit.

(1) Ensure that the AC line conditions satisfy the unit's requirements.

(2) If the control unit does not utilize Pick/Hold power sequencing lines, select "Local" mode on the power supply unit.

(3) Verify all connectors are inserted correctly.

(4) If the unit is in daisy chain with another unit, make sure that the last unit has a line terminator (LTN) installed.

(5) Verify that the rotary actuator is unlocked.

(6) Ensure that the logical unit number (LUN) is selected properly and is assigned to only one unit.

(7) In case of Hard sector mode (fixed sector length), ensure that the correct sector count is set on the PCB 512398.

(8) Ensure that Tag 4/5, seek end status and responce of unit ready are set correctly according to the system configuration.

(9) Ensure that all PCB assemblies are firmly seated.

15.2 ERROR STATE

The disk unit and the control unit will issue the following statuses.

Table 15.2-1 Error Status

NOT READY	Not Ready status indicates disk drive is not ready
FAULT	Fault status indicates a fault condition has occurred in the unit
SEEK ERROR	Seek Error status indicates a seek error has occurred in seek operation
READ ERROR	Read Error status indicates a data error has occurred in read operation
AM MISSING	AM Missing status indicates that AM (Address Mark) has not found in read operation

Maintenance Personnel can see the unit status and error state on the Indicator Unit (HGAMU) and the Operator Panel. Refer to Section 3.7 for detailed unit status and error state, and how to know the error state by unit state indicators (colored LEDs), state indicators (7-segment LEDs) and state switch (Toggle Switch) mounted on the Indicator PCB.

The trouble shooting guide is provided with the Error State which is defined by indicators on the PCB and the Operator Panel.

The Error State is shown in Table 15.2-2.

Table 15.2-2 Error State

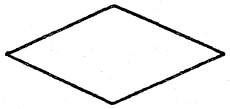
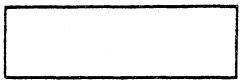
Error Status	Indicator Unit (HGAMU)						Indicators on the Operator Panel			Error State		Figure
	Unit State Indicator (LEDs)			State Switch	State Indicator Lamp							
					Lamp 1	Lamp 2						
	URDY	ACCK	FALT		Bit 1 2 4 8	Bit 1 2 4 8	Fault	Power on	Ready			
Not Ready	Off	-	-	-	- - - -	- - - -	-	Off	Off	Power Alarm	Not Ready	15.4-1
	Off	-	-	0	- - - 1	- - - -	-	-	Off	Hall Alarm		
	Off	-	-	2	- - - -	1 - - -	-	-	Off	DE Sequence Check		
Fault	-	-	On	1	1 - - -	- - - -	On	-	-	Index Check		15.4-2
	-	-	On	1	- 1 - -	- - - -	On	-	-	Control Check		
	-	-	On	1	- - 1 -	- - - -	On	-	-	Multi Head Check		
	-	-	On	1	- - - 1	- - - -	On	-	-	Head Short Check		
	-	-	On	1	- - - -	1 - - -	On	-	-	Write Current On Read Check		
	-	-	On	1	- - - -	- 1 - -	On	-	-	Write Transition Check		
	-	-	On	1	- - - -	- - 1 -	On	-	-	Delta I Write Check		
	-	-	On	1	- - - -	- - - 1	On	-	-	Servo Off-Track		
Seek error	-	On	-	2	- 1 - -	- - - -	-	-	-	Access Timeout Check		15.4-3
	-	On	-	2	- - 1 -	- - - -	-	-	-	Over Shoot Check		
Read error	-	-	-	-	- - - -	- - - -	-	-	-	Read Error		15.4-4
AM Missing	-	-	-	-	- - - -	- - - -	-	-	-	AM Missing		15.4-5

15.3 TROUBLE SHOOTING SYMBOL

The trouble shooting flow charts contain the procedures to pursue trouble causes starting from error status information.

The following conventions are provided to aid understanding the symbols used in the trouble shooting flow charts as shown in Table 15.3-1

Table 15.3-1 Symbol of Flow Chart

Symbol	Description
	Terminal. Starting point of the trouble.
 ( )	Decision, go ahead according with YES or NO. (Reference test point.)
	Connector, go ahead same-numbered symbol in the same sheet.
	Connector, go ahead same-numbered symbol in another sheet.
	Process.

15.4 TROUBLE SHOOTING FLOW CHART

In this paragraph, the following charts are provided.

Figure 15.4-1 Not Ready
Figure 15.4-2 Fault
Figure 15.4-3 Seek Error
Figure 15.4-4 Read Error
Figure 15.4-5 AM Missing (for only Soft Sector Mode)

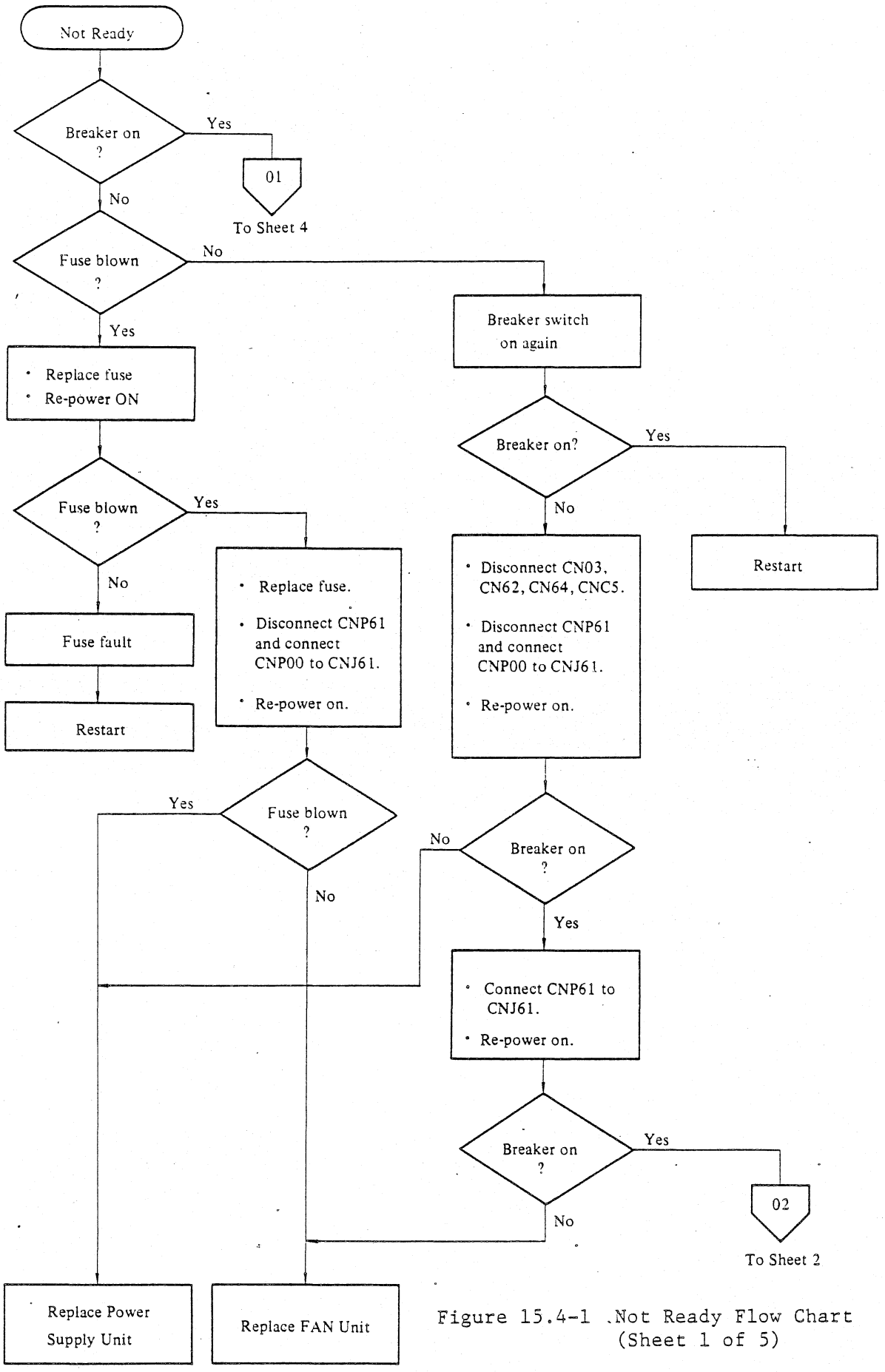


Figure 15.4-1 Not Ready Flow Chart
(Sheet 1 of 5)

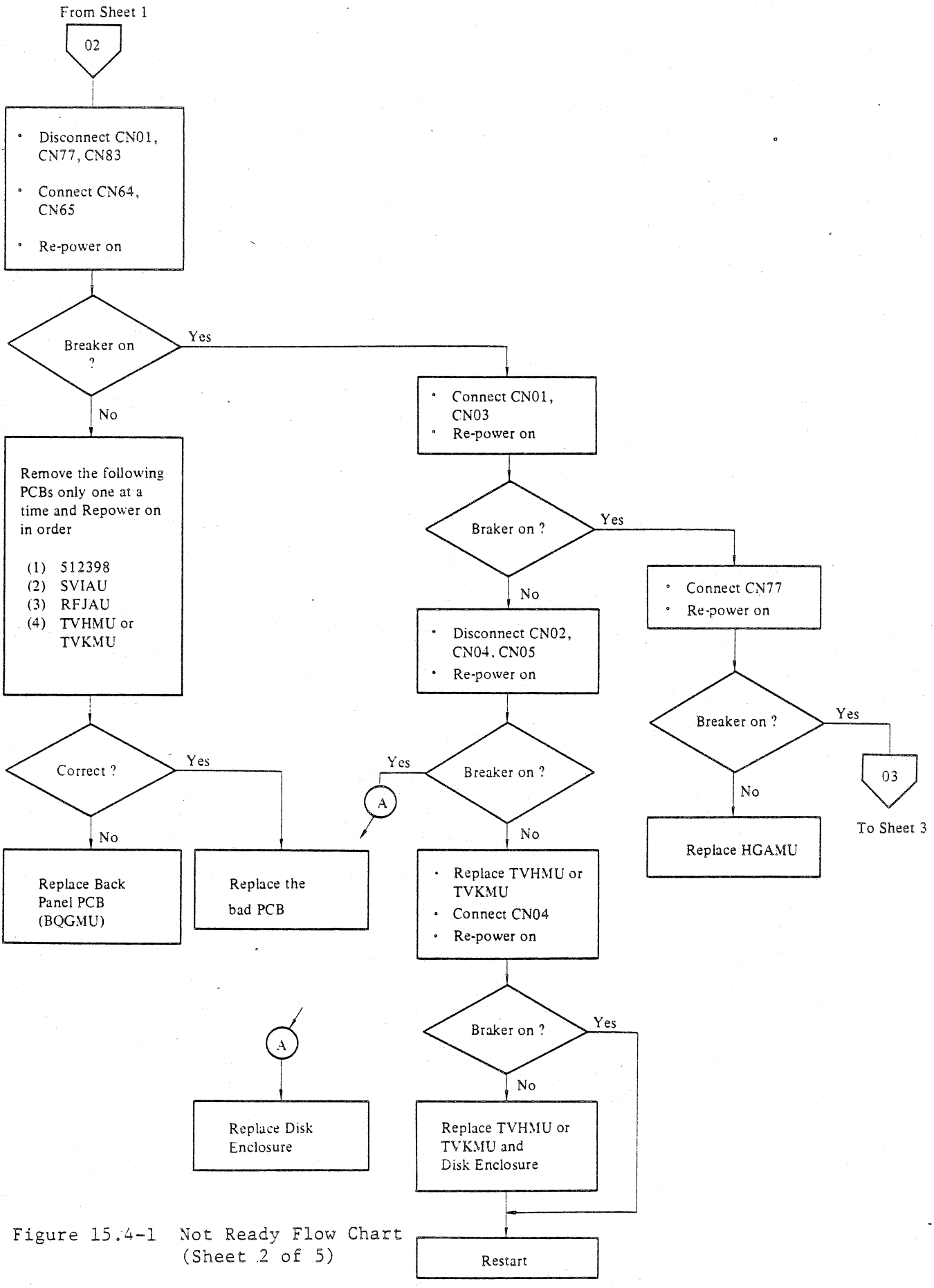


Figure 15.4-1 Not Ready Flow Chart (Sheet 2 of 5)

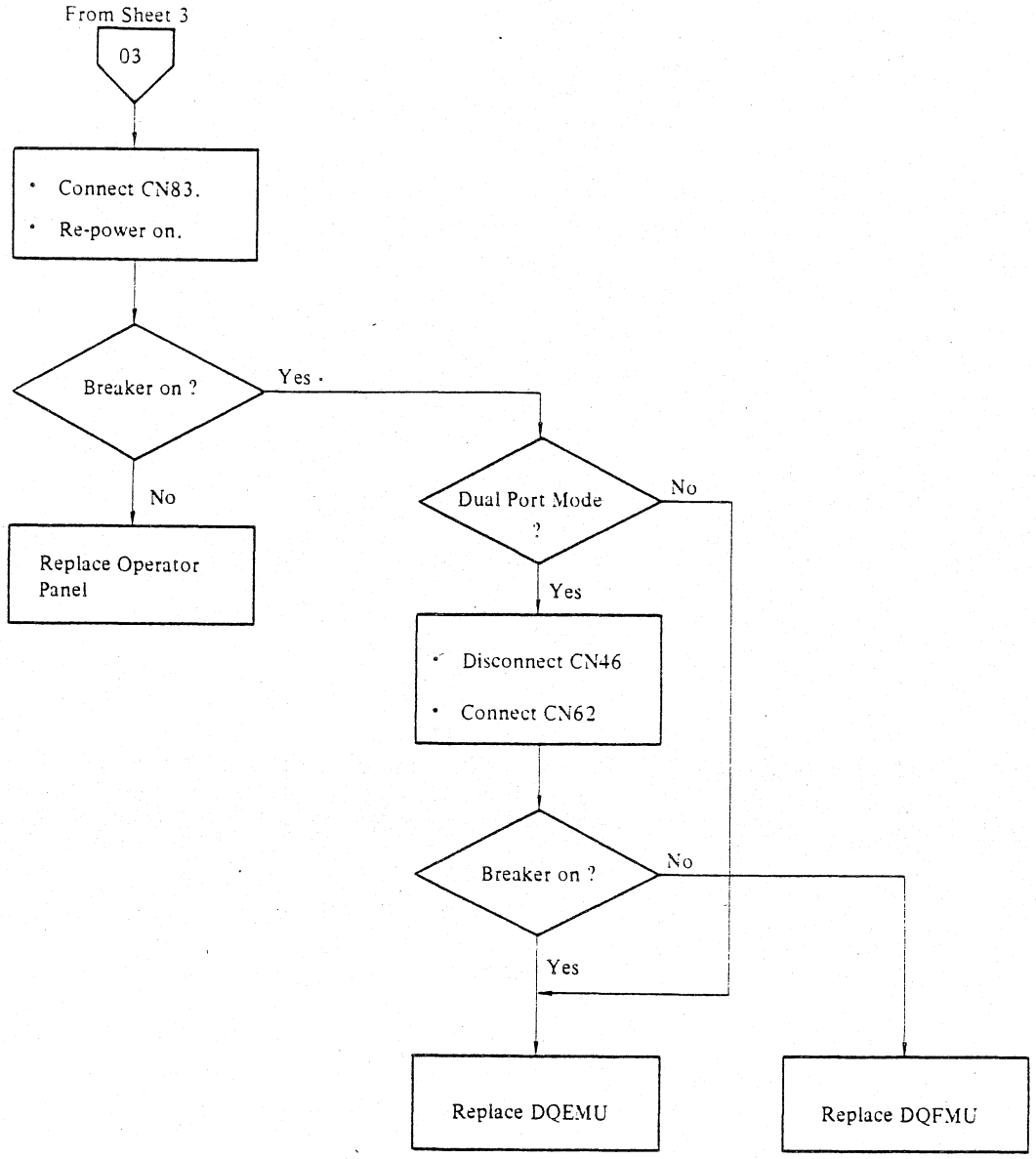


Figure 15.4-1 Not Ready Flow Chart
(Sheet 3 of 5)

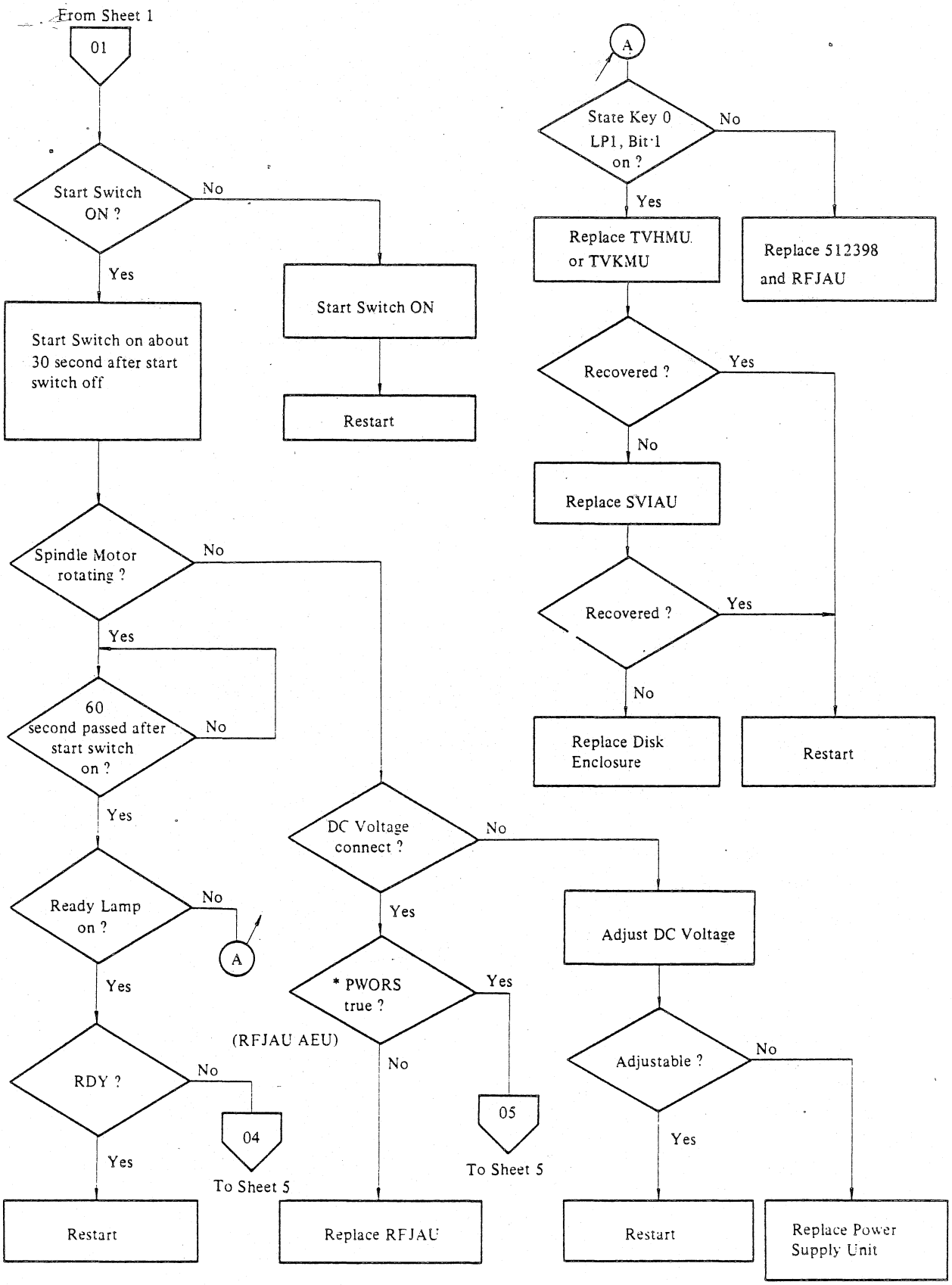


Figure 15.4-1 Not Ready Flow Chart
(Sheet 4 of 5)

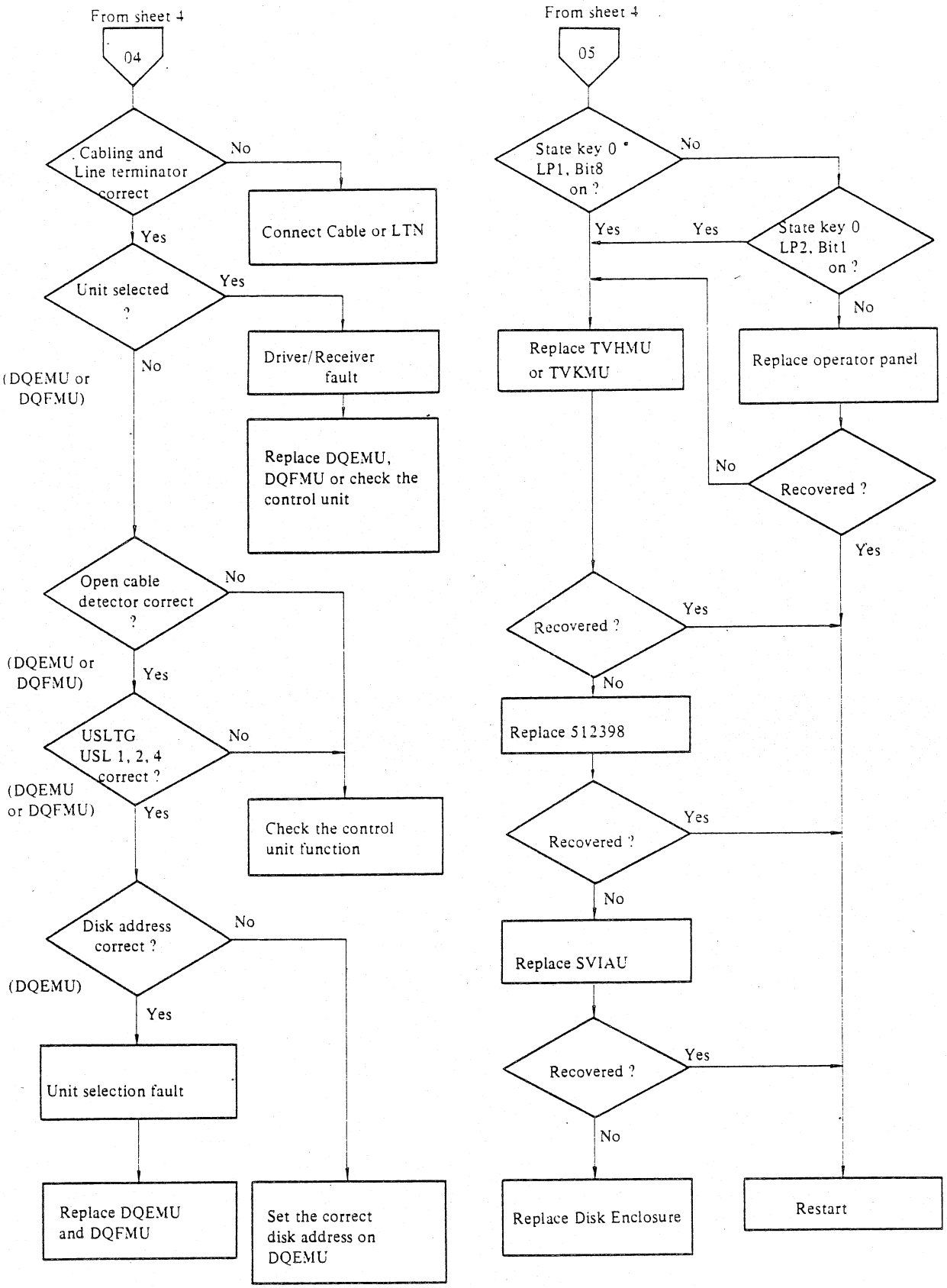
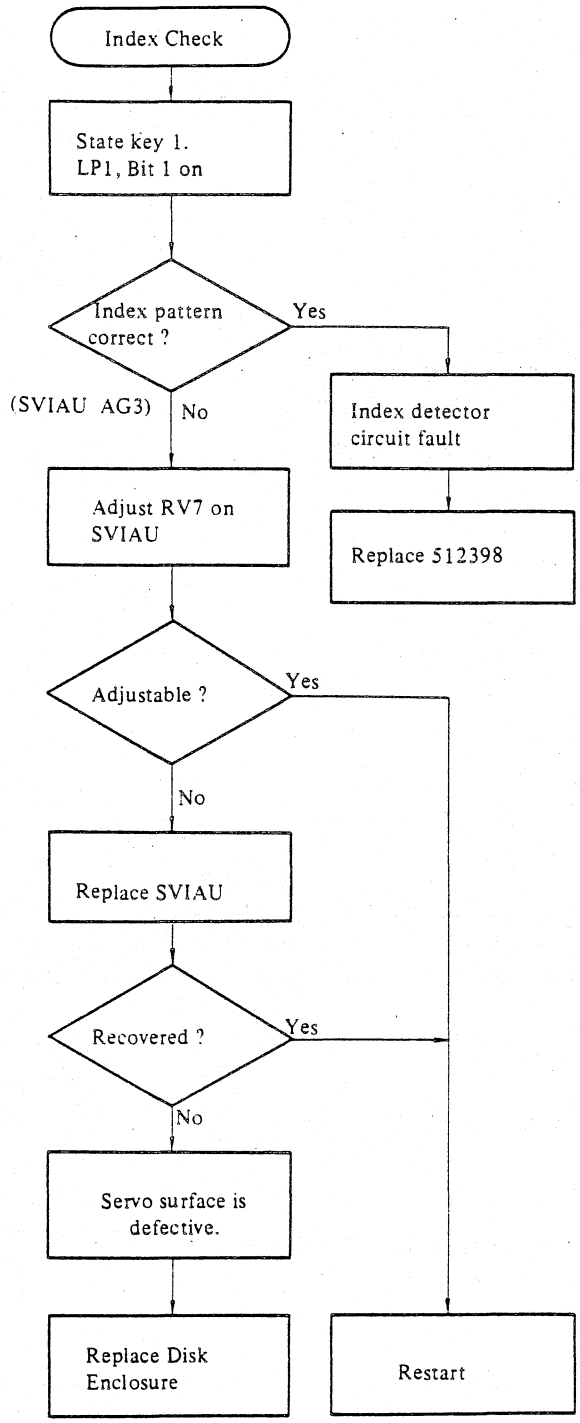


Figure 15.4-1 Not Ready Flow Chart
(Sheet 5 of 5)



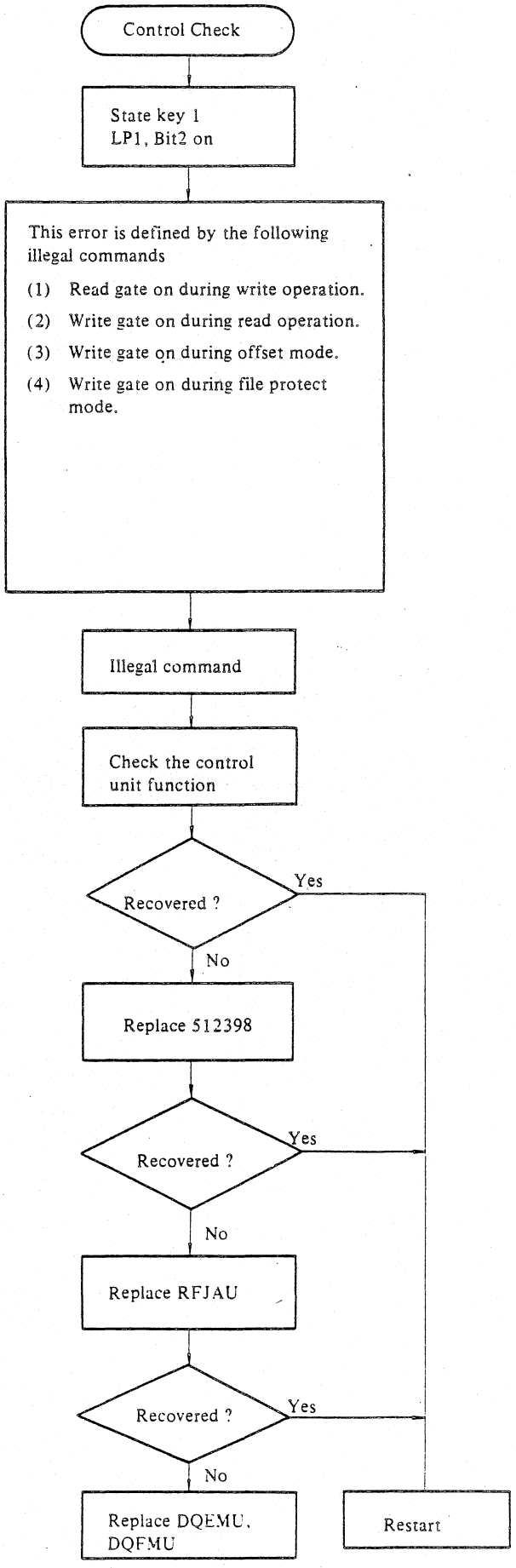


Figure 15.4-2 Fault Flow Chart
(Sheet 1 of 4)

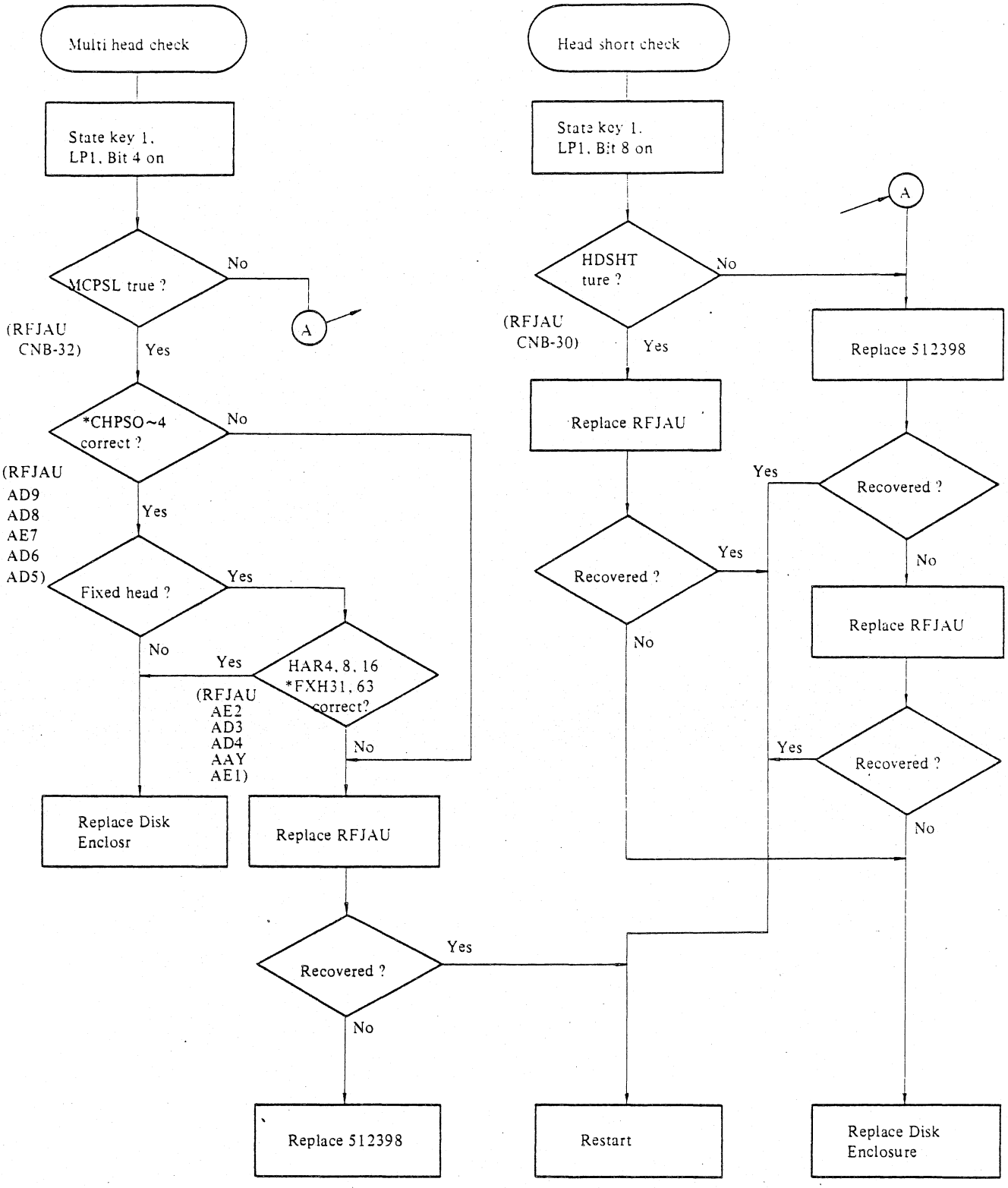


Figure 15.4-2 Fault Flow Chart (Sheet 2 of 4)

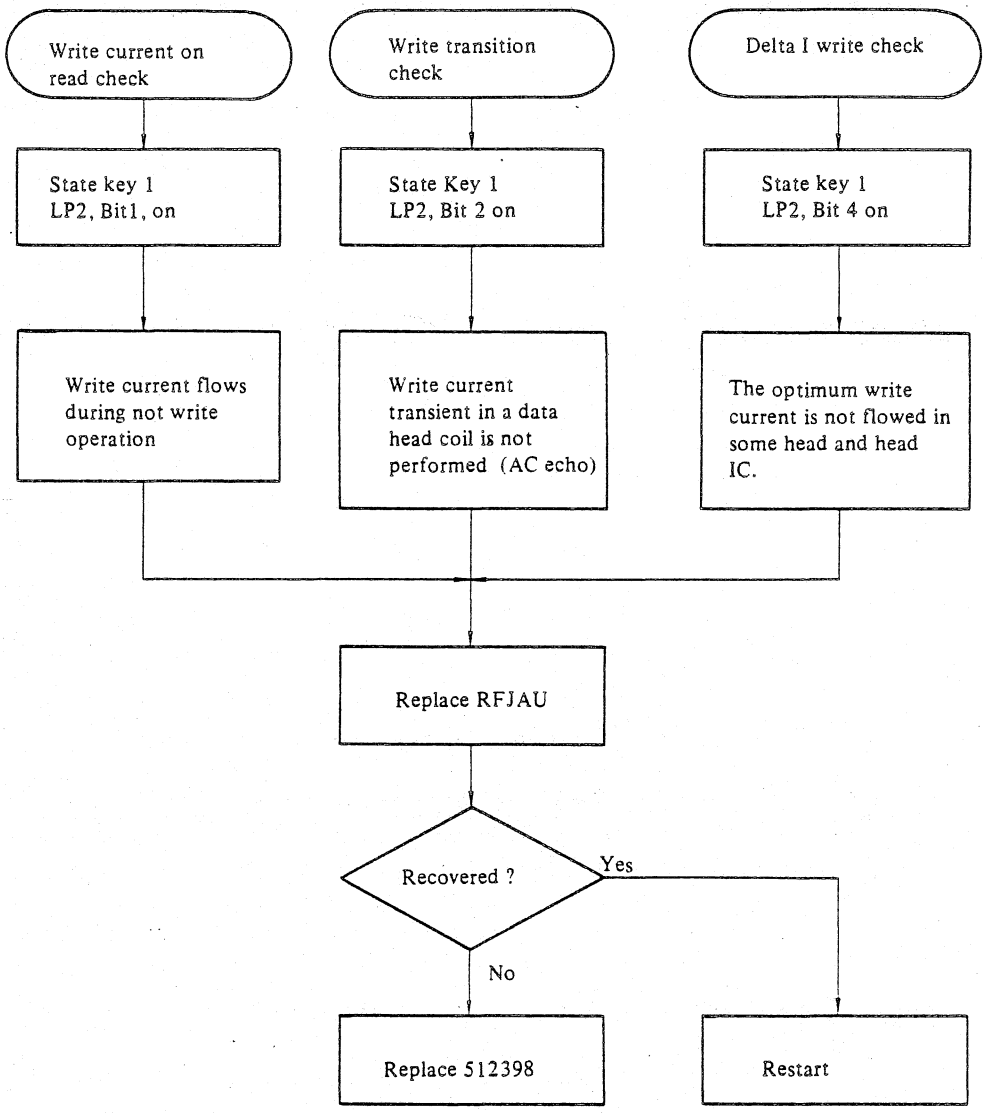


Figure 15.4-2 Fault Flow Chart (Sheet 3 of 4)

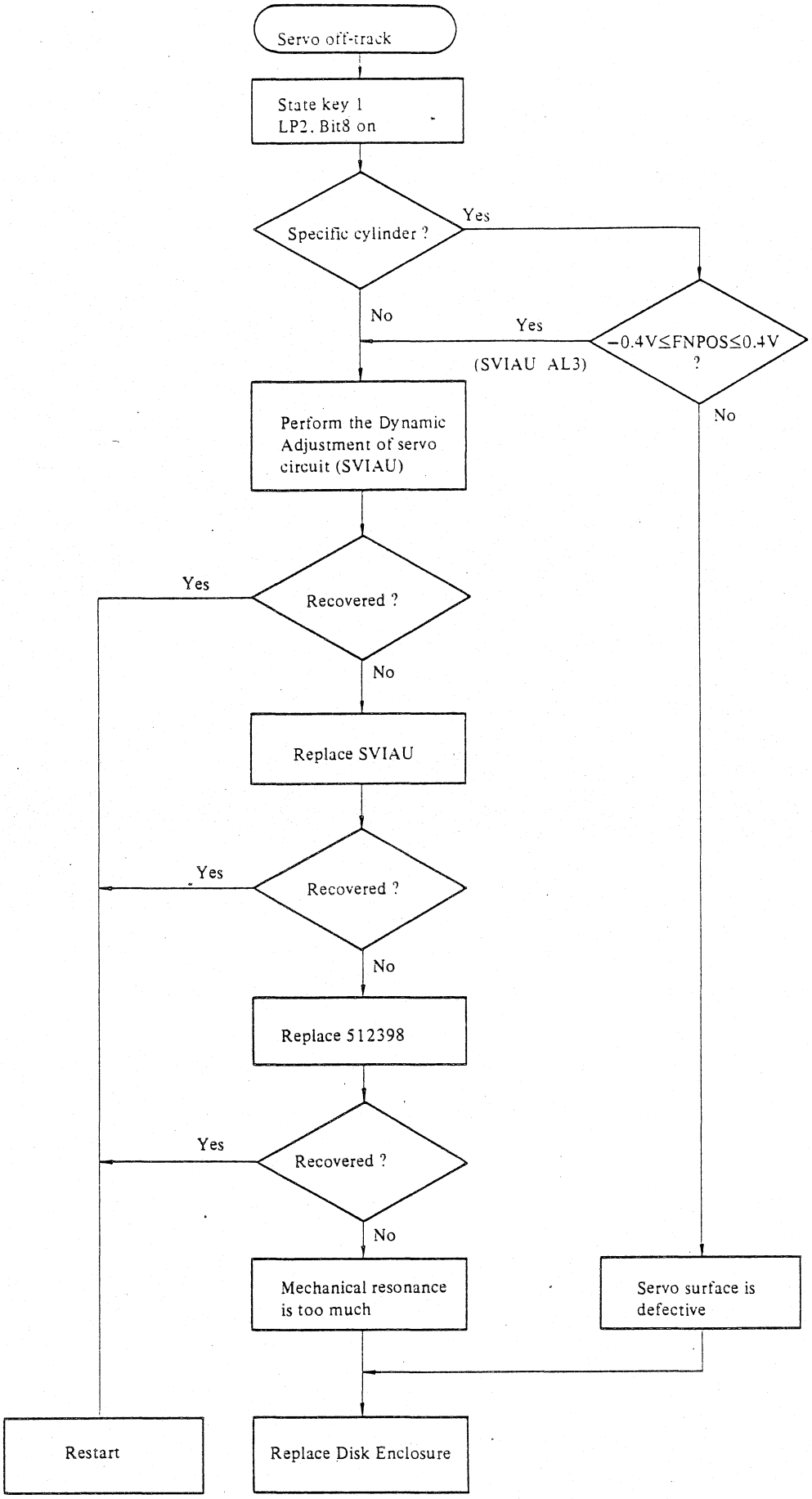


Figure 15.4-2 Fault Flow Chart (Sheet 4 of 4)

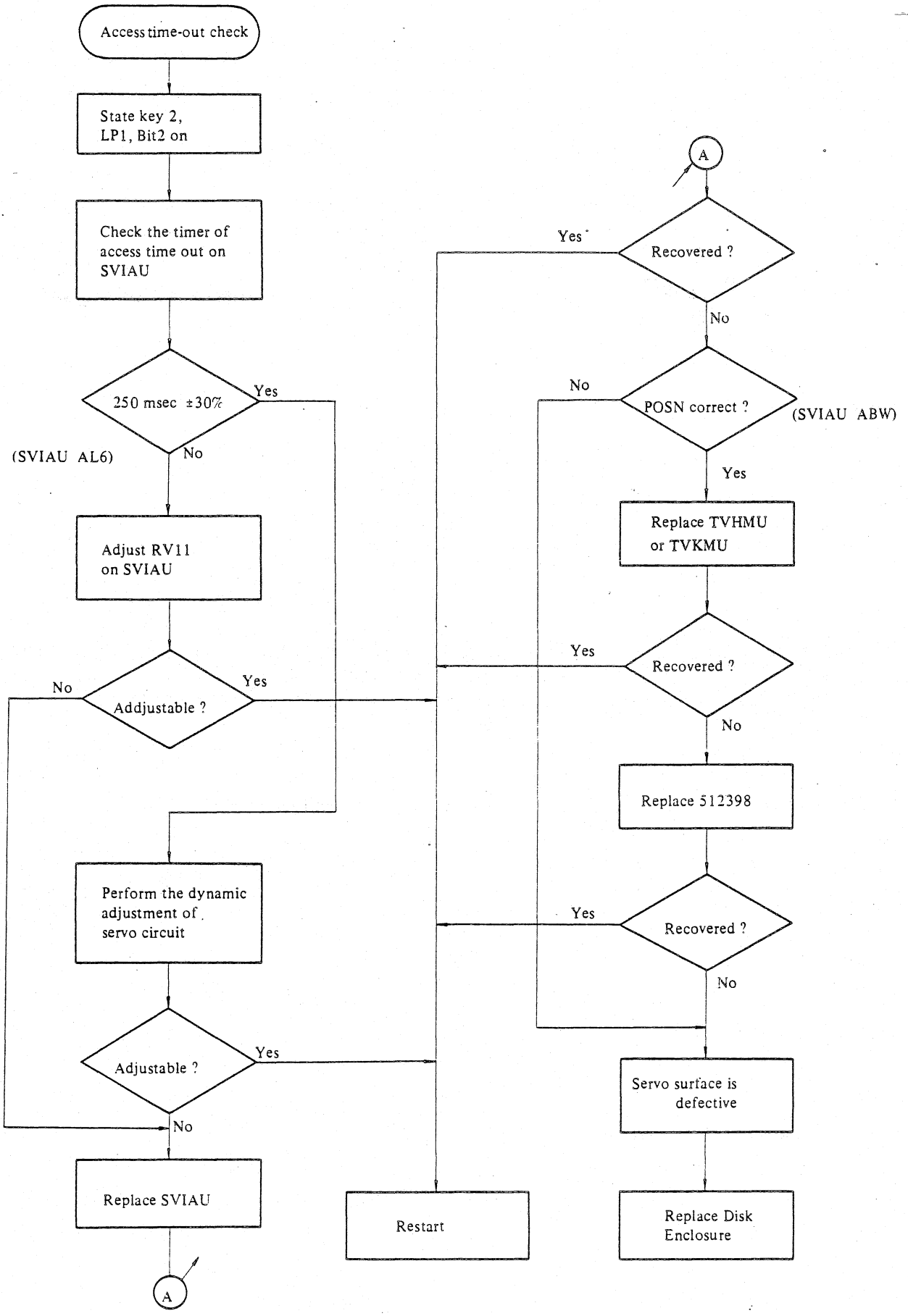


Figure 15.4-3 Seek Error Flow Chart (Sheet 1 of 2)

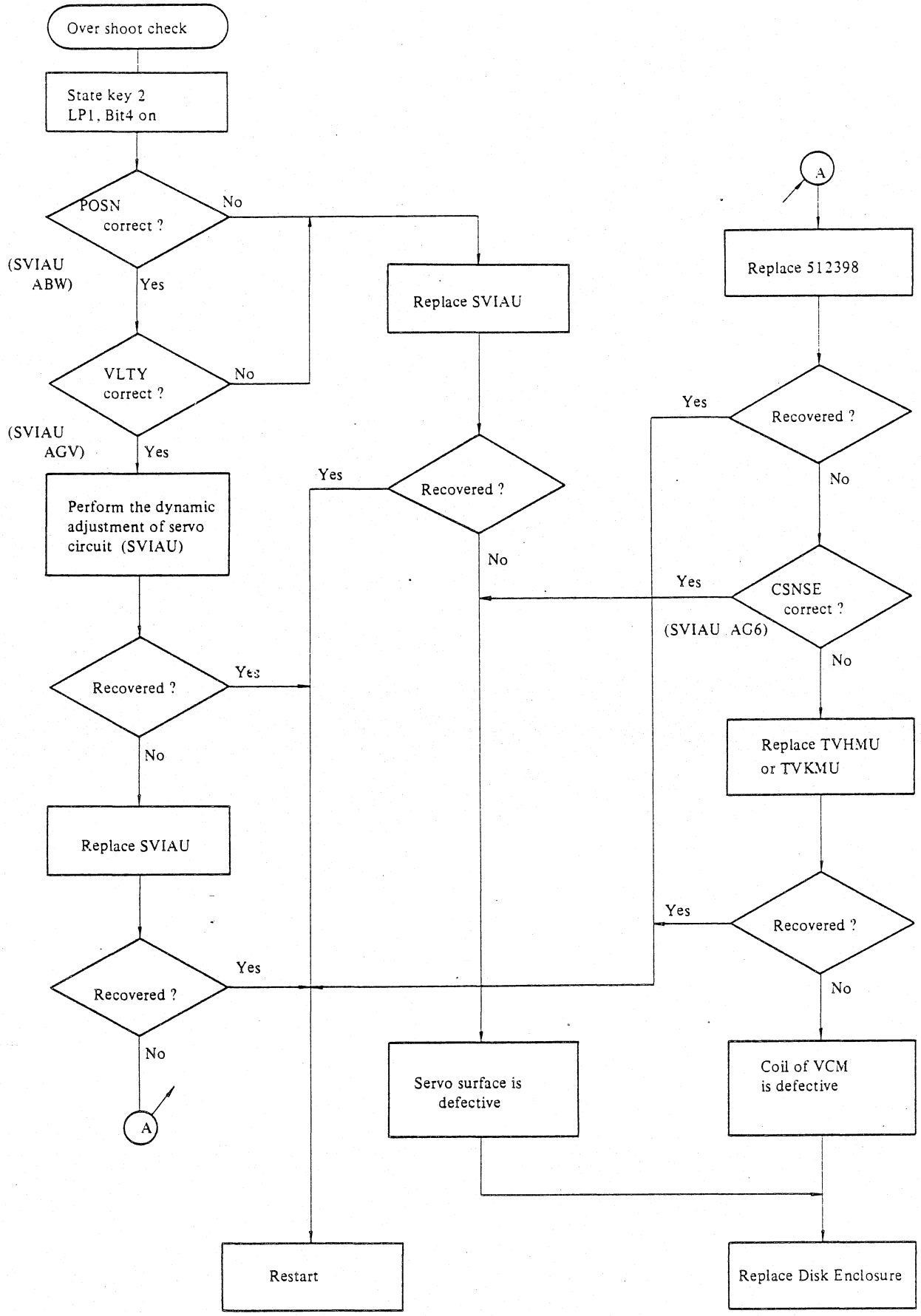
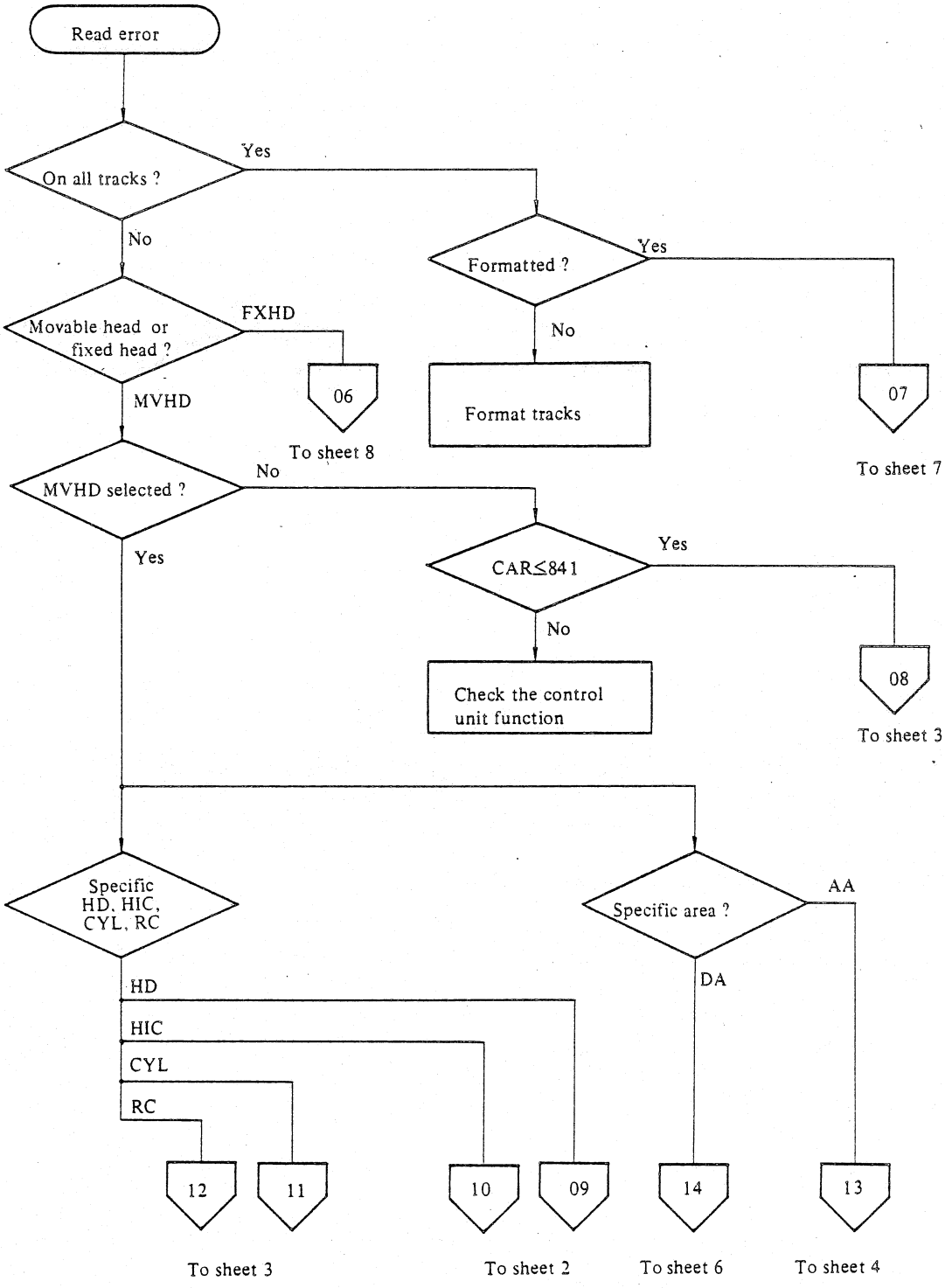


Figure 15.4-3 Seek Error Flow Chart (Sheet 2 of 2)



Note : AA is address area
DA is data area
HD is head
HIC is head IC (or chip)
CYL is cylinder
RC is record

Figure 15.4-4 Read Error Flow Chart (Sheet 1 of 8)

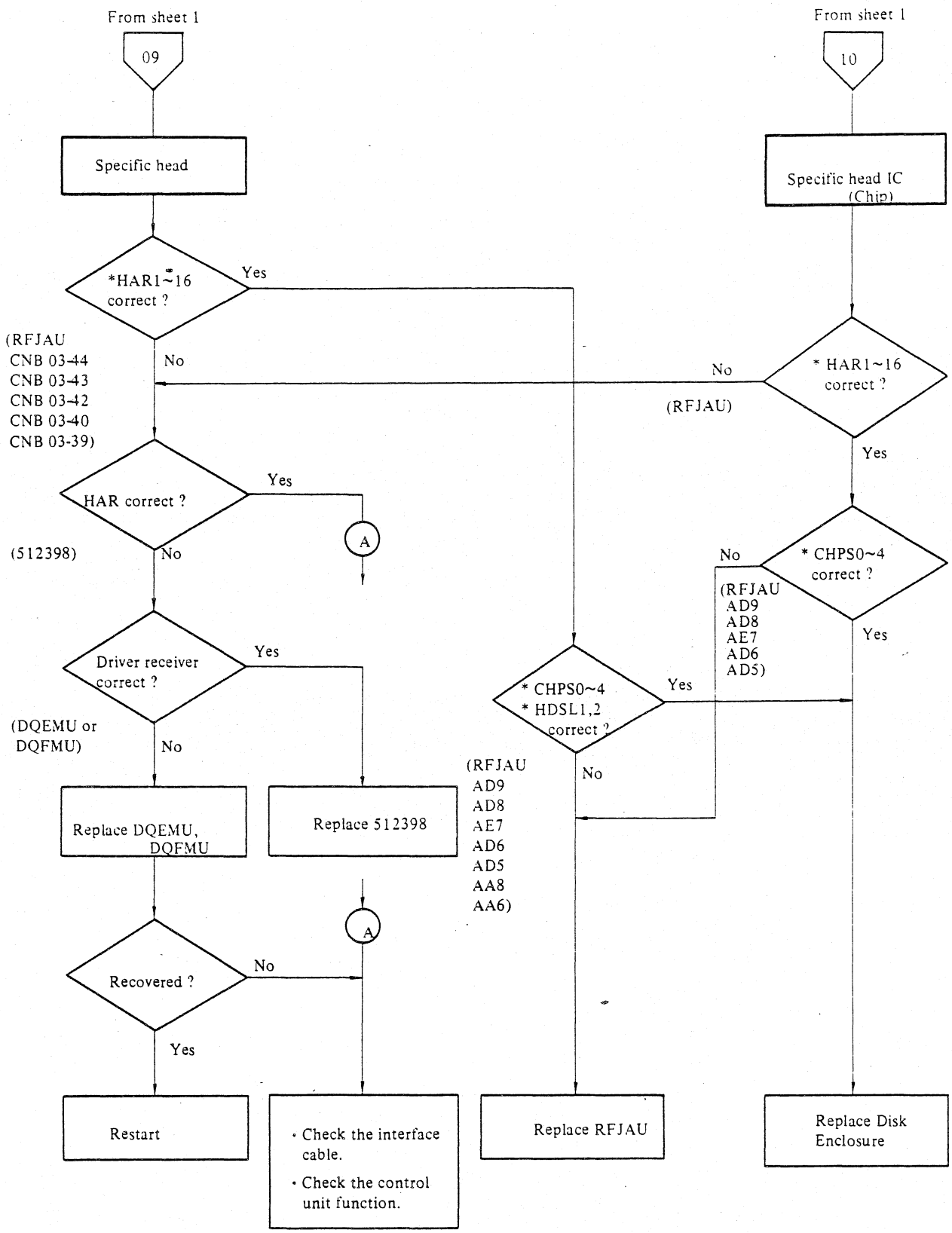


Figure 15.4-4 Read Error Flow Chart (Sheet 2 of 8)

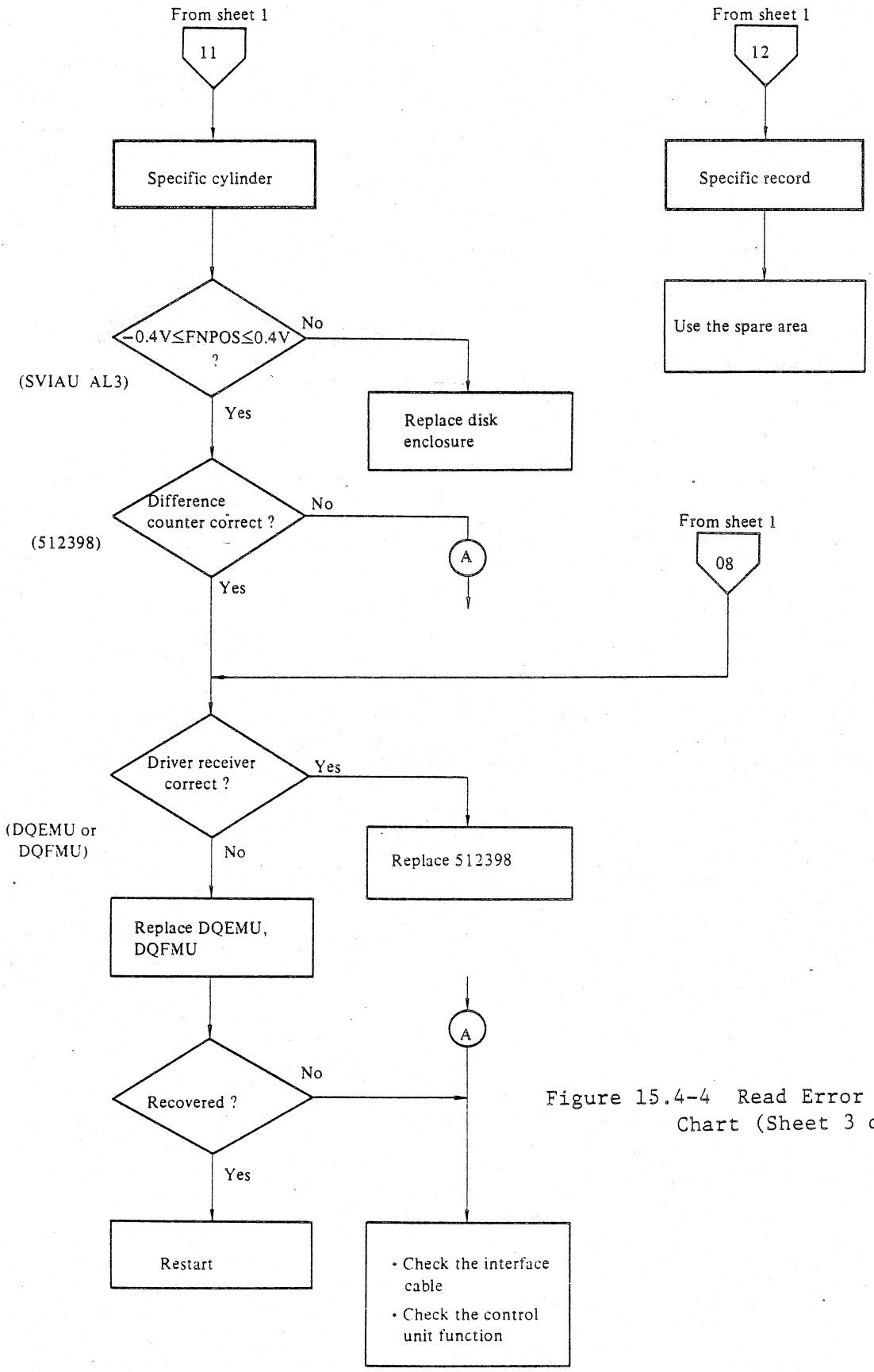


Figure 15.4-4 Read Error Flow Chart (Sheet 3 of 8)

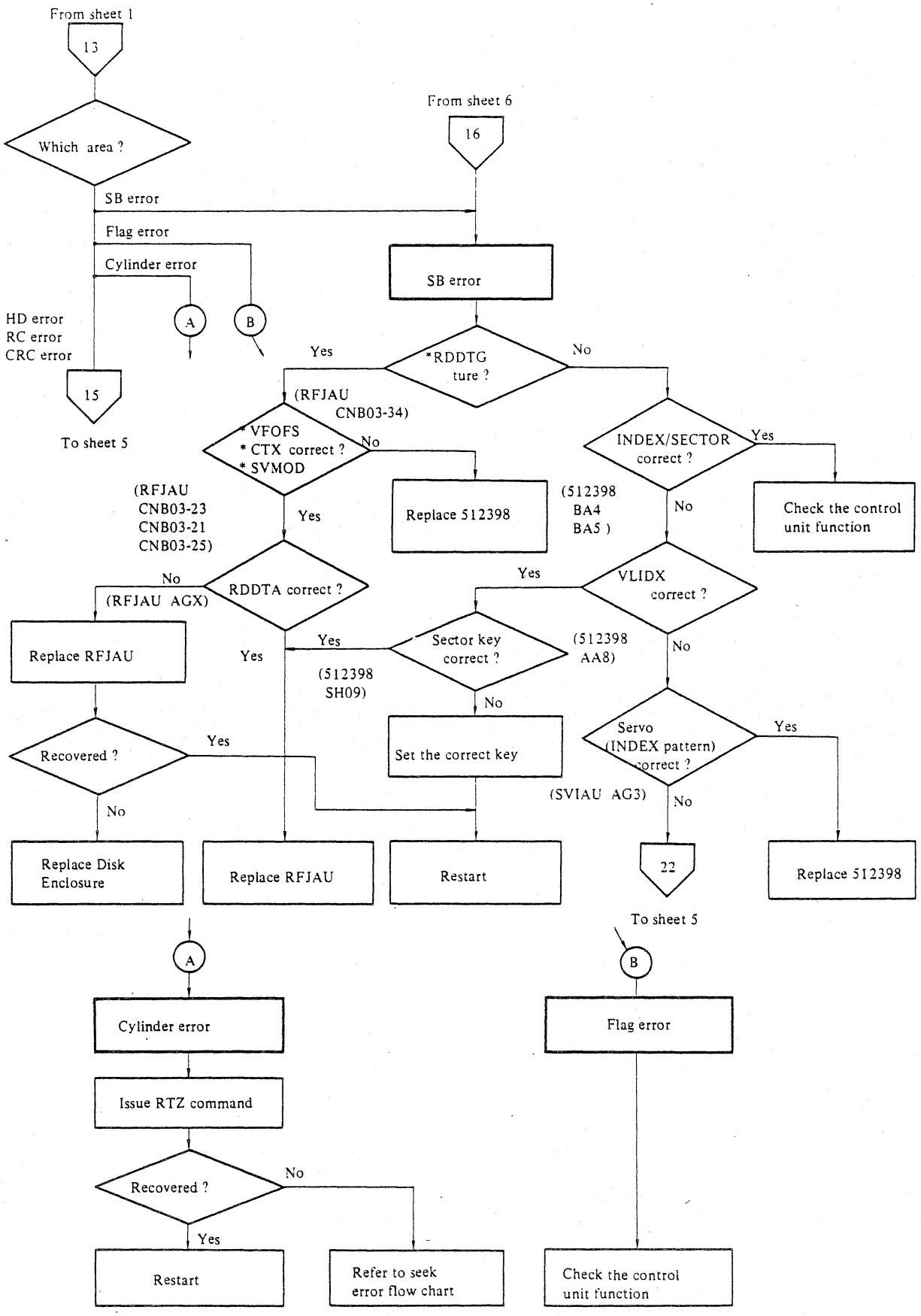


Figure 15.4-4 Read Error Flow Chart (Sheet 4 of 8)

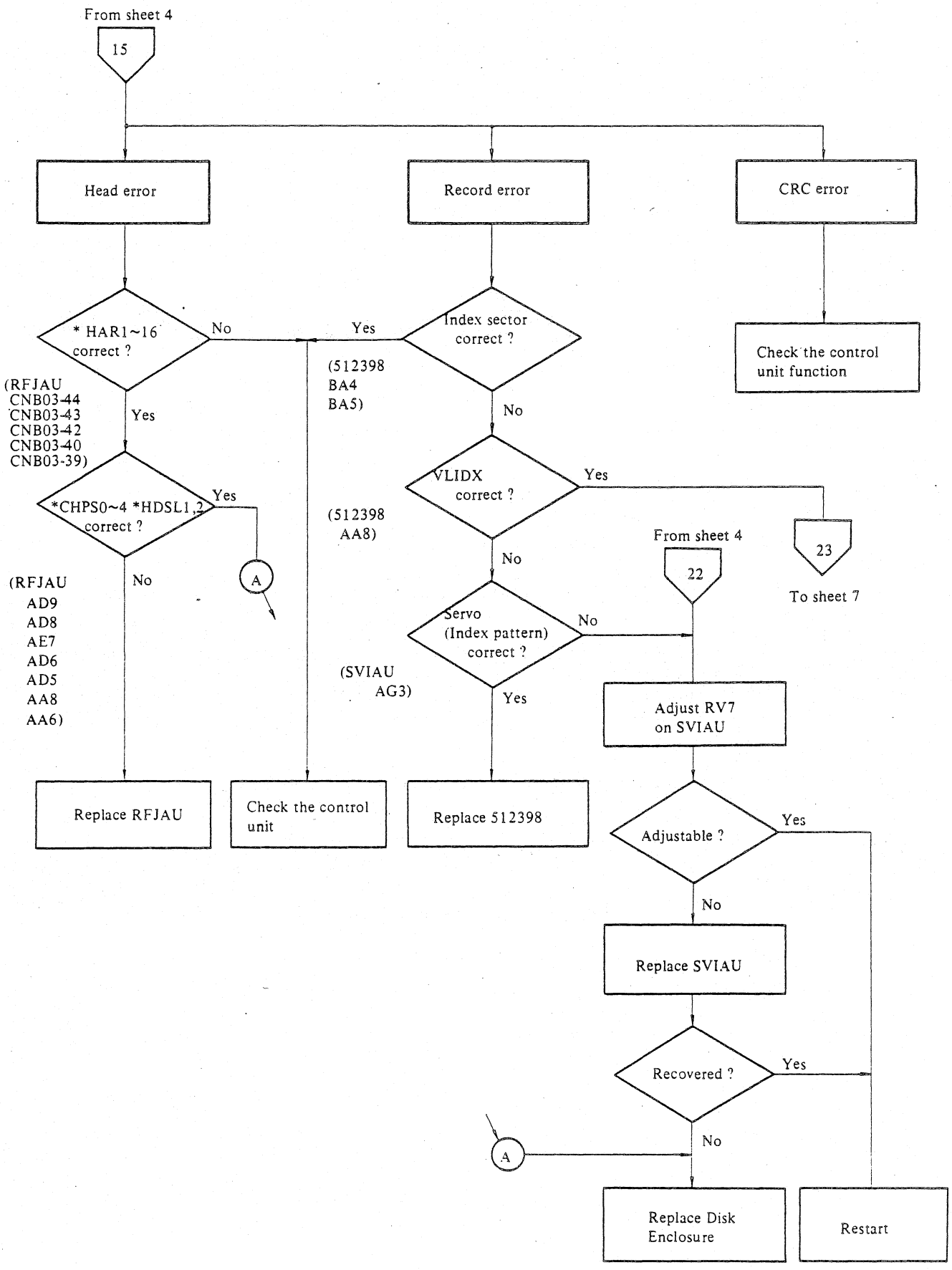


Figure 15.4-4 Read Error Flow Chart (Sheet 5 of 8)

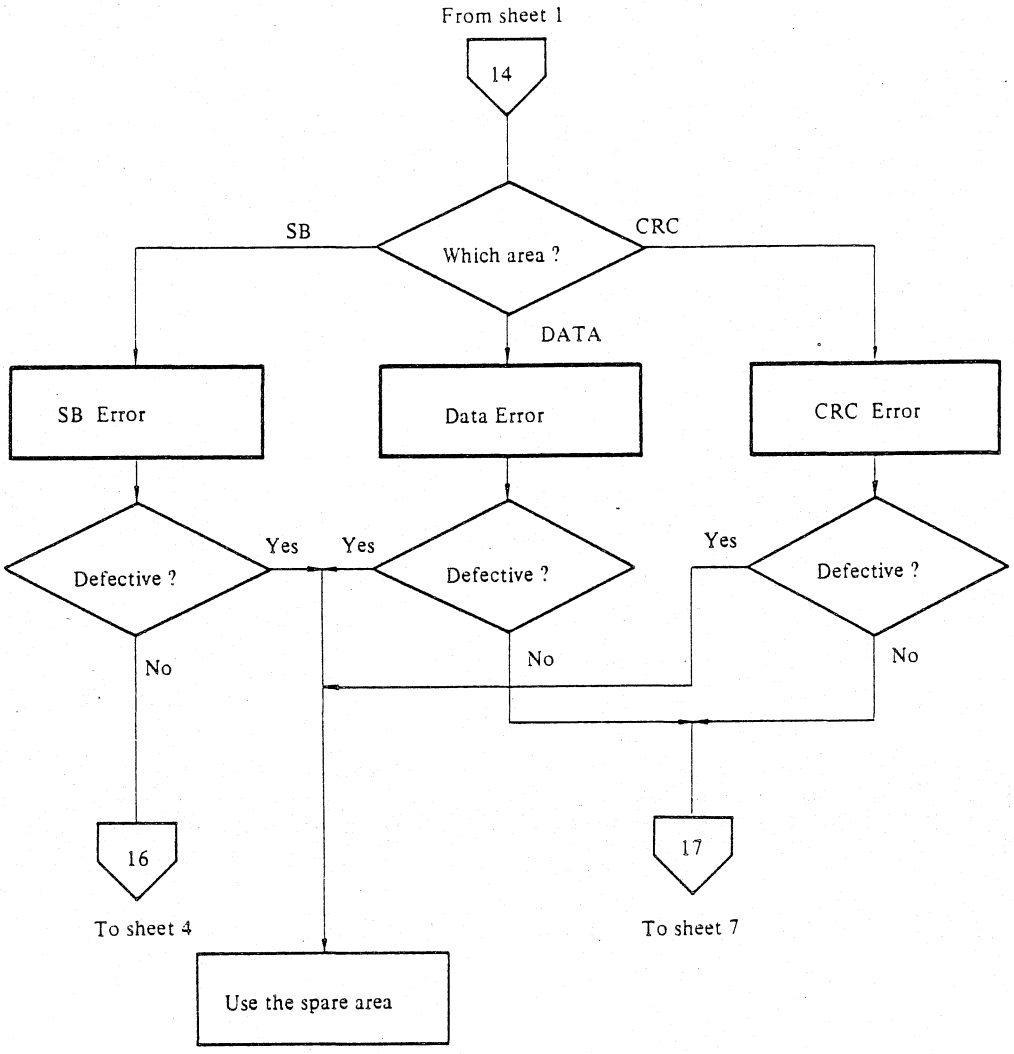


Figure 15.4-4 Read Error Flow Chart (Sheet 6 of 8)

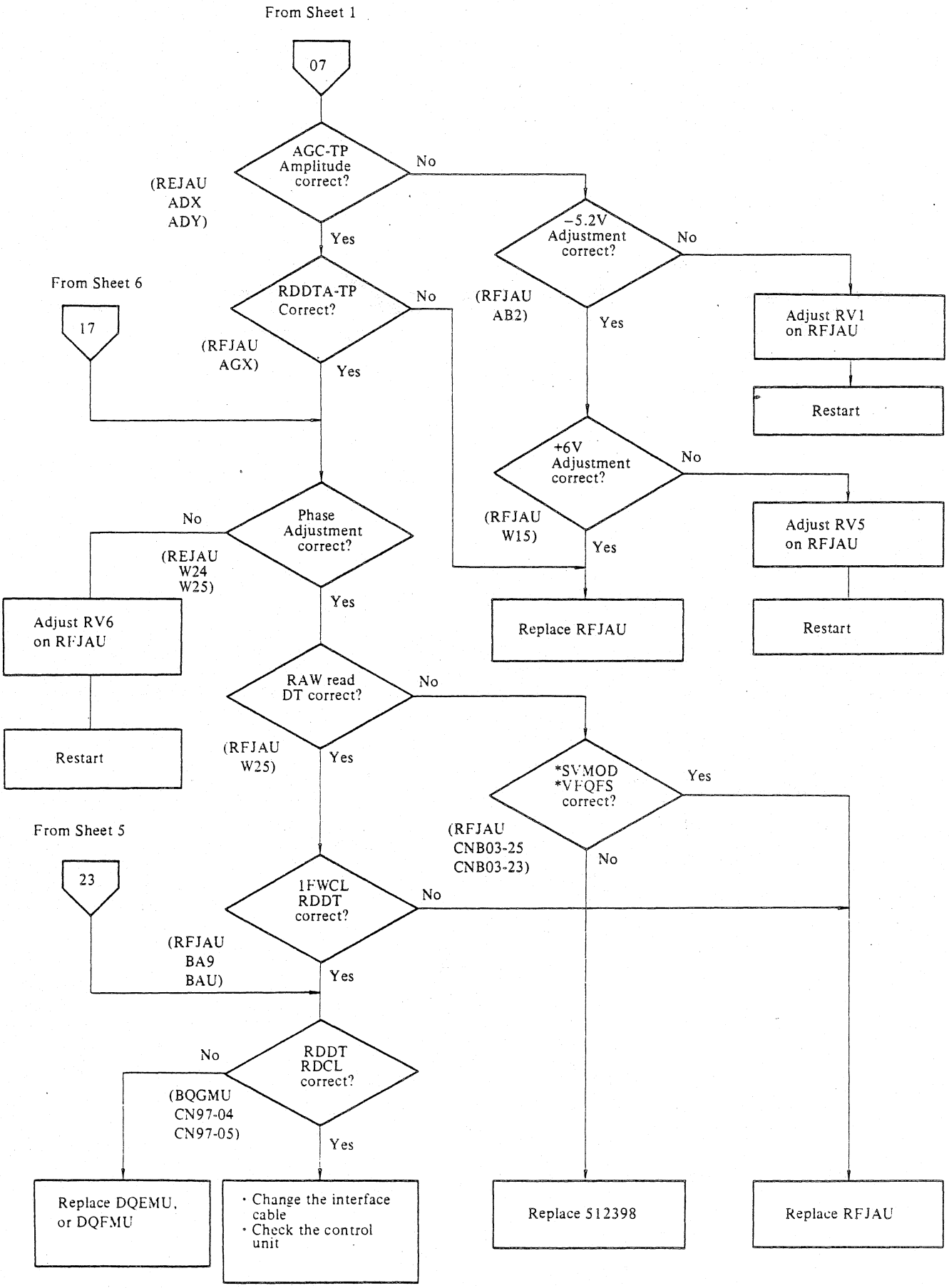


Figure 15.4-4 Read Error Flow Chart (Sheet 7 of 8)

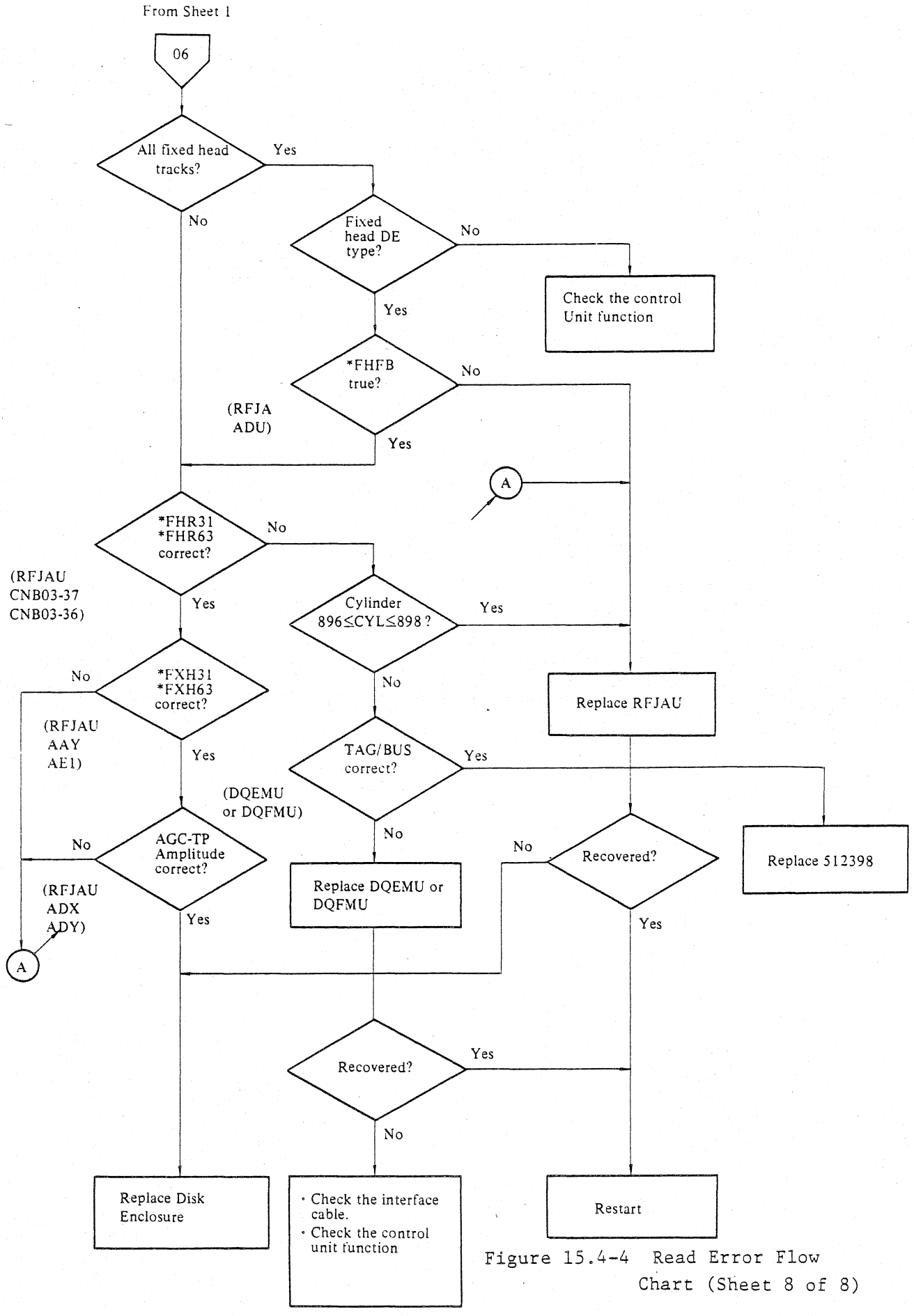


Figure 15.4-4 Read Error Flow Chart (Sheet 8 of 8)

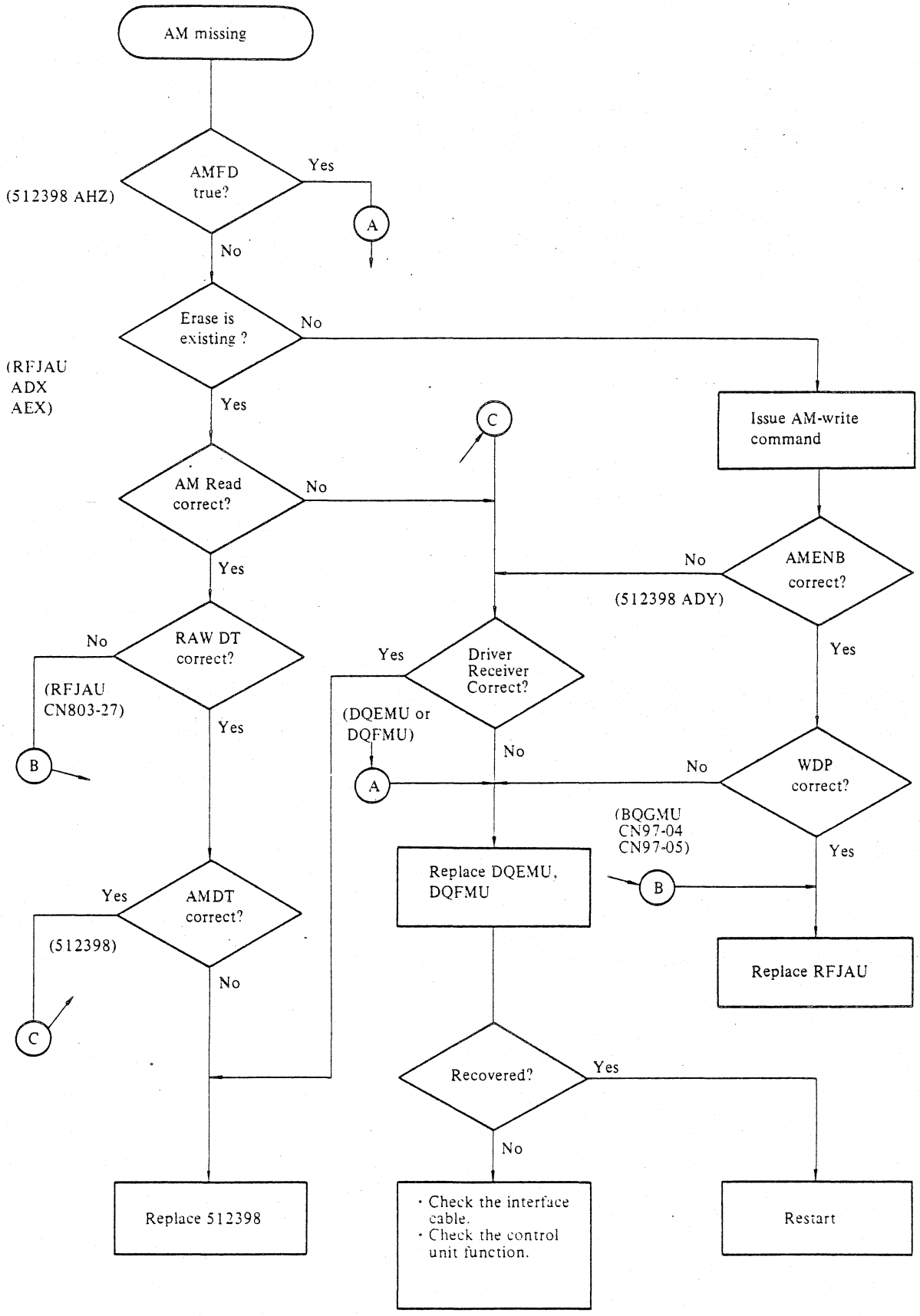


Figure 15.4-5 AM Missing Flow Chart (Sheet 1 of 1)

CHAPTER 16 DESCRIPTION OF ICs

16.1 INTRODUCTION

This section describes the functions and interchangeability of TTL, ECL and Linear ICs used in the drive.

The specifications of input and output voltage level for each kind of IC are listed in Table 16.1-1.

Table 16.1-1 Input/Output Level

	Input (V)		Output (V)	
	High	Low	High	Low
TTL Medium Speed	5.5 ~ 2.0	0.8 ~ -0.5	5.25 ~ 2.4	0.4 ~ 0
TTL Schottkey	5.5 ~ 2.0	0.8 ~ -0.3	5.25 ~ 2.7	0.5 ~ 0
TTL Low Power Schottkey	5.5 ~ 2.0	0.8 ~ -0.3	5.25 ~ 2.7	0.4 ~ 0
ECL	-0.81 ~ -1.105	-1.475 ~ -1.85	-0.81 ~ -0.98	-1.63 ~ -1.85

Logical "1" and "0" correspond to high and low level respectively for input or output of each kind of IC.

16.2 INTERCHANGEABILITY

(1) TTL (SSI/MSI)

FUJITSU		Direct	Function	Ref.
Type No.	Marking	Replacement		No.
MB74LS00M	LS00	SN74LS00N	Quad 2-Input NAND	1
MB74LS01M	LS01	SN74LS01N	Quad 2-Input NAND . Open Collector	2
MB74LS02M	LS02	SN74LS02N	Quad 2-Input NOR	3
MB74LS04M	LS04	SN74LS04N	Hex Inverter	5
MB74LS05M	LS05	SN74LS05N	Hex Inverter . Open Collector	6
MB74LS08M	LS08	SN74LS08N	Quad 2-Input AND	8
MB74LS10M	LS10	SN74LS10N	Triple 3-Input NAND	9
MB74LS11M	LS11	SN74LS11N	Triple 3-Input AND	10
MB74LS20M	LS20	SN74LS20N	Dual 4-Input NAND	11
MB74LS21M	LS21	SN74LS21N	Dual 4-Input AND	12
MB74LS27M	LS27	SN74LS27N	Triple 3-Input NOR	13
MB74LS32M	LS32	SN74LS32N	Quad 2-Input OR	14
MB74LS37M	LS37	SN74LS37N	Quad 2-Input NAND Buffer	1
MB74LS42M	LS42	SN74LS42N	BCD to Decimal Decoder	16
MB74LS74AM	LS74	SN74LS74N	Dual D-Type Flip-Flop	17
MB74LS85M	LS85	SN74LS85N	4-bit Magnitude Comparator	18
MB74LS86M	LS86	SN74LS86N	Quad 2-Input EOR	19
MB74LS107M	LS107	SN74LS107N	Dual J-K Flip-Flop	20
MB74LS153M	LS153	SN74LS153N	Dual 4 to 1 Data Selector/Multiplexer	21
MB74LS155M	LS155	SN74LS155N	Dual 2 to 4 Decoder	22
MB74LS161AM	LS161	SN74LS161N	4-bit Binary Counter	23
MB74LS164M	LS164	SN74LS164N	8-bit Shift Register	24
MB74LS175M	LS175	SN74LS175N	Quad D-Type Flip-Flop	15
MB74LS191M	LS191	SN74LS191N	4-bit Up/Down Counter	25
(None)	LS279	SN74LS279N	Quad R-S Latch	26
MB74LS283M	LS283	SN74LS283N	4-bit Full Adder	27
(None)	LS123	SN74LS123	Dual Monostable	28
(None)	LS221	SN74LS221	Dual Monostable	29
MB400M	LA01	SN7400N	Quad 2-Input NAND	1
MB418M	LA18	SN7404N	Hex Inverter	5
MB463M	463	SN7438N	Quad 2-Input NAND . Open Collector	30
MB434M	434	SN75451BP	Dual 2-Input AND Buffer	31
MB435M	435	SN7437N	Quad 2-Input NAND Buffer	32
MB439M	439	SN75450BN	Dual 2-Input AND Buffer	33
MB440M	440	SN74123N	Dual Monostable	28
MB443M	LA23	SN74145N	BCD to Decimal Decoder	34
(None)	LX32	SN7406	Hex Inverter	7
(None)	LX26	SN74157	Quad D-Type Flip-Flop	15
(None)	LX34	SN74193	4-bit Binary Up/Down Counter	35
(None)	LX27	SN74221	Dual Monostable	29
(None)	LX16	SN75452	Dual NAND Driver	36
MB74S00M	S00	SN74S00N	Quad 2-Input NAND	1
MB74S03M	S03	SN74S03N	Quad 2-Input NAND . Open Collector	4
MB74S04M	S04	SN74S04N	Hex Inverter	5
MB74S11M	S11	SN74S11N	Triple 3-Input AND	10
(None)	S112	SN74S112N	Dual J-K Flip-Folp	37
(None)	S153	SN74S153N	Dual 4 to 1 Data Slector /Multiplexer	21
(None)	75107A	SN75107AN	Dual Receiver	38
(None)	75108A	SN75108AN	Dual Receiver	38
(None)	75110	SN75110A	Dual Dreiver	39

Note: Direct replacements are ICs of TEXAS INSTRUMENTS INCORPORATED.

(2) TTL (Bipolar 500-Gate Master Slice LSI)

FUJITSU		Direct	Function	Ref.
Type No.	Marking	Replacement		No.
MB15139C	15139	(None)	Access Control	40
MB15140C	15140	(None)	HDA Sequencer	41

Note: All ICs are FUJITSU original.

(3) TTL (Bipolar 200-Gate Master Slice LSI)

FUJITSU		Direct	Function	Ref.
Type No.	Marking	Replacement		No.
MB14601M	14601	(None)	Linear Motor Control	42
MB14613M	14613	(None)	Servo Pattern Detector	43

Note: All ICs are FUJITSU original.

(4) ECL 10K

FUJITSU		Direct	Function	Ref.
Type No.	Marking	Replacement		No.
MB10101C	101	MC10101L	Quad 2-Input OR/NOR	44
MB10102C	102	MC10102L	Quad 2-Input NOR	45
MB10105C	105	MC10105L	Triple 2-3-2 OR/NOR	46
MB10106C	106	MC10106L	Triple 4-3-3 NOR	47
MB10109C	109	MC10109L	Dual 4-5 Input OR/NOR	48
MB10116C	116	MC10116L	Triple Line Receiver	49
MB10124C	124	MC10124L	Quad TTL to ECL Translator	50
MB10125C	125	MC10125L	Quad ECL to TTL Translator	51
MB10131C	131	MC10131L	Dual D-Type Flip-Flop	52
MB10135C	135	MC10135L	Dual J-K Flip-Flop	53
(None)	(None)	HD103107	Voltage Controlled Oscillator	54

Note: MC is MOTOROLA Semiconductor Products Inc..
HD is Hitachi, Ltd..

(5) Analog Master-Slice LSI

FUJITSU		Direct	Function	Ref.
Thpe No.	Marking	Replacement		No.
MB4306C	A4306	(None)	Voltage Controlled Oscillator A	55
MB4311C	A4311	(None)	Level Senser	56
MB4313C	A4303	(None)	AGC Amp.	57
MB4316C	A4316	(None)	Read/Write Bus Switch C	58
MB4319C	A4319	(None)	Peak Hold	59
MB4112	A4112	SSI105	Disk Head IC (Fixed Head)	60
MB4113	A4113	(None)	Disk Head IC (Movable Head)	60

Note: SSI is Silicon Systems Inc..

(6) Analog IC

FUJITSU		Direct	Function	Ref.
Tyte No.	Marking	Replacement		No.
MB4002M	A4002		High Speed Differential Comparator	61
MB3607M	A1458	MC1458	Dual Operational Amplifier	62
MB3501M	A733	μA733DM	Differential Video Amplifier	63
MB5365AM	Q5365M		NPN Dual Transistors	64
(None)	A142	μPC142A	Negative Voltage Regulator	65
(None)	A741	μPC151C	Frequency Compensated Op . Amp.	66
(None)	A318	μPC159A	High Speed Wide Band Op. Amp.	67
(None)	A311	μPC271C	Voltage Comparator	68
(None)	A610	μPC610D	10-Bit D/A Converter	69
(None)	Q049AX	μPA49A	PNP Dual Transistors	70
(None)	A201	DG201BK	Quad Analog Switches	71
(None)	A555M	M51841P	Timing Circuit	72
(None)	A1590	MC1590G	AGC Amplifier	73

Note: MC is MOTOROLA Semiconductor Products Inc..
μA is Fairchild Camera and Instrument Corporation.
μPC and μPA are NIPPON Electric Co., Ltd..
DG is Siliconix Incorporated.
M is Mitsubishi Electric Co., Ltd..

(7) Memory IC

FUJITSU		Direct	Function	Ref.
Type No.	Marking	Replacement		No.
MB7055C	7055	(None)	1024 × 8 (8192) Bit PROM	74

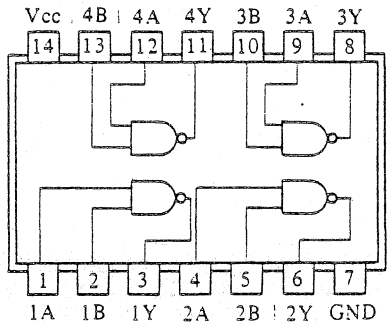
16.3 DETAIL OF ICs

(1) MB74LS00M (SN74LS00N)
MB400M (SN7400N)
MB74S00M (SN74S00N)
MB74LS37M (SN74LS37N)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic: $Y = \overline{AB}$

(Top view)

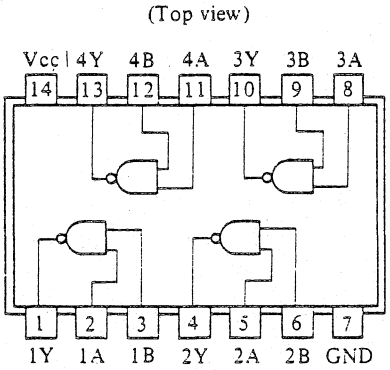


(2) MB74LS01M (SN74LS01N)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic: $Y = \overline{AB}$

(Top view)

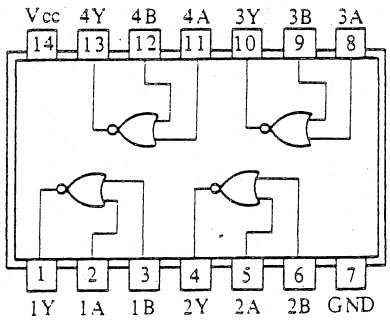


(3) MB74LS02M (SN74LS02N)

QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

positive logic: $Y = \overline{A+B}$

(Top view)

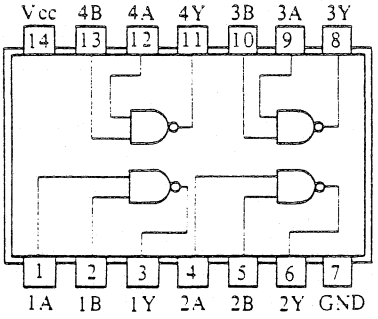


(4) MB74S03M (SN74S03N)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic: $Y = \overline{AB}$

(Top view)



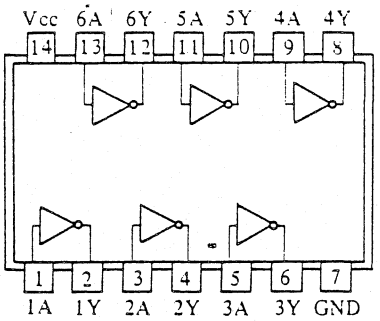
(5) MB74LS04M (SN74LS04N)
MB418M (SN7404N)
MB74S04M (SN74S04N)

HEX INVERTERS

positive logic:

$Y = \overline{A}$

(Top view)



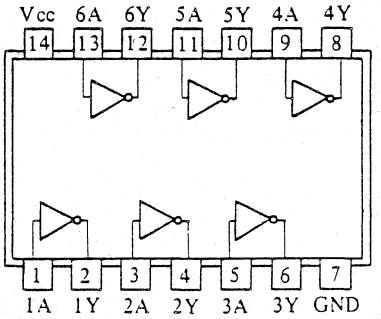
(6) MB74LS05M (SN74LS05N)

HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A}$

(Top view)



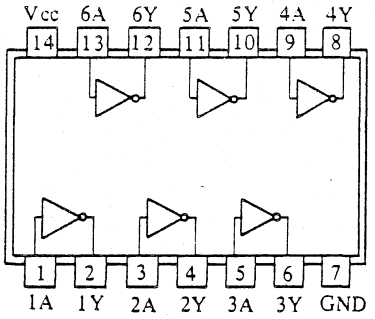
(7) SN7406

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$

(Top view)



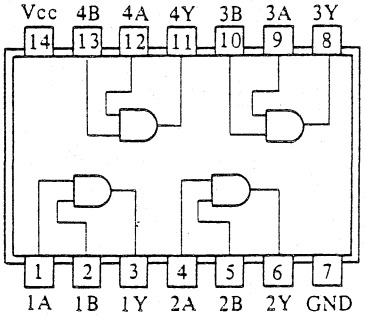
(8) MB74LS08M (SN74LS08N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

positive logic:

$Y = AB$

(Top view)

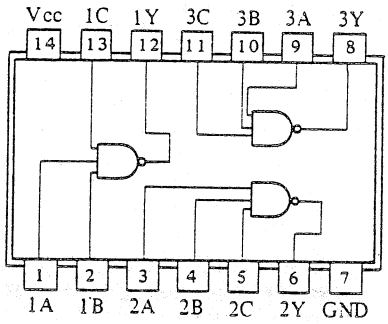


(9) MB74LS10M (SN74LS10N)

TRIPLE 3-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABC}$

(Top view)

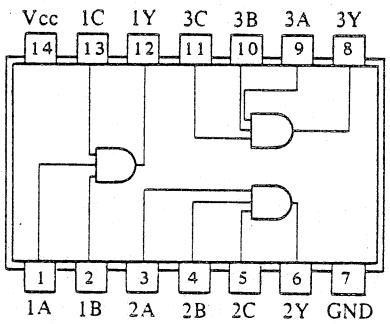


(10) MB74LS11M (SN74LS11N)
SN74 S11N

TRIPLE 3-INPUT
POSITIVE-AND GATES

positive logic:
Y = ABC

(Top view)

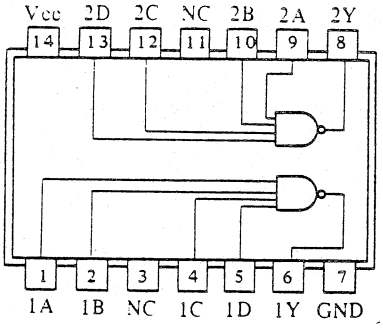


(11) MB74LS20M (SN74LS20N)

DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$

(Top view)

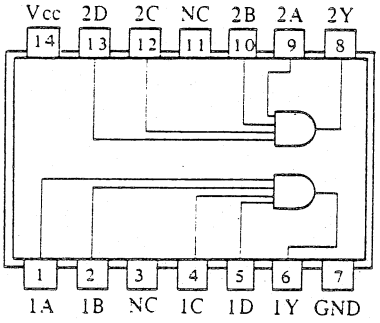


(12) MB74LS21M (SN74LS21N)

DUAL 4-INPUT
POSITIVE-AND GATES

positive logic:
Y = ABCD

(Top view)

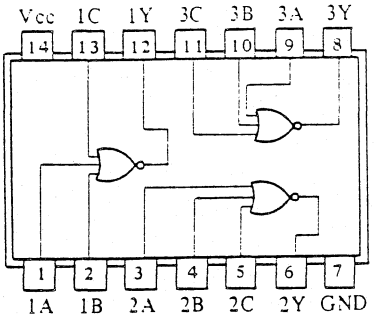


(13) MB74LS27M (SN74LS27N)

TRIPLE 3-INPUT
POSITIVE-NOR GATES

Positive logic:
$Y = \overline{A+B+C}$

(Top view)

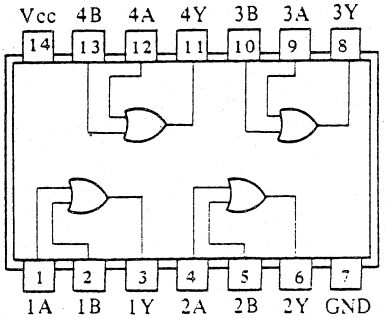


(14) MB74LS32M (SN74LS32N)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

positive logic:
$Y = A+B$

(Top view)



(15) SN74175

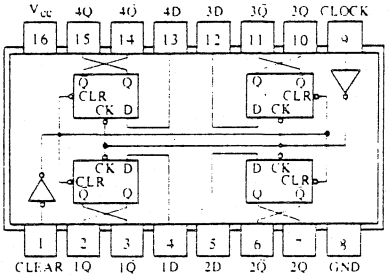
QUADRUPLE D-TYPE FLIP-FLOPS

Positive logic;

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUT			OYTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$↑
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

(Top view)



H = High level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q_0 = the level of Q before the indicated steady-state input conditions were established.

(16) MB74LS42M (SN74LS42N)

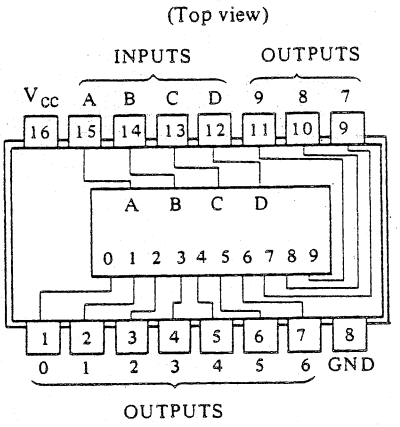
BCD TO DECIMAL DECODER

Positive logic;

FUNCTION TABLE

No.	BCD INPUT D C B A	DECIMAL OUTPUT 0 1 2 3 4 5 6 7 8 9
0	L L L L	L H H H H H H H H H
1	L L L H	H L H H H H H H H H
2	L L H L	H H L H H H H H H H
3	L L H H	H H H L H H H H H H
4	L H L L	H H H H L H H H H H
5	L H L H	H H H H H L H H H H
6	L H H L	H H H H H H L H H H
7	L H H H	H H H H H H H L H H
8	H L L L	H H H H H H H H L H
9	H L L H	H H H H H H H H H L
INVALID	H L H L	H H H H H H H H H H
	H L H H	H H H H H H H H H H
	H H L L	H H H H H H H H H H
	H H L H	H H H H H H H H H H
	H H H L	H H H H H H H H H H
	H H H H	H H H H H H H H H H

H = high level L = low level



(17) MB74LS74AM (SN74LS74N)

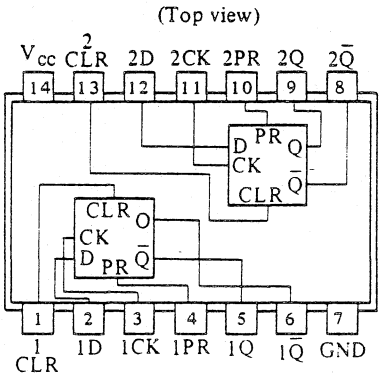
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Positive logic;

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCD	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



(18) MB74LS85M (SN74LS85N)

4-BIT MAGNITUDE COMPARATOR

These four-bit magnitude cimparatórs perform comparison of straight binary and straig BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B output of a stage handling less-significant bits are connected to the corresponding A>B, A<B, and A=B inputs of the next stage handling more-significant bits.

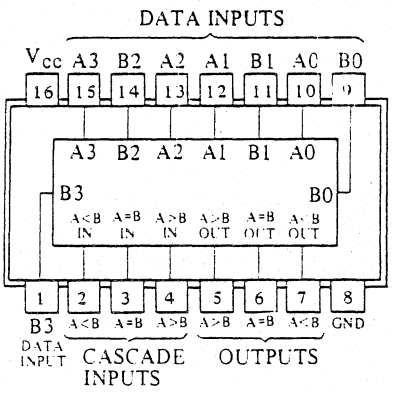
Positive ligic;

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B2	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = gigh level L = low level X = irrelevant

(Top view)



(19) MB74LS86M (SN74LS86M)

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

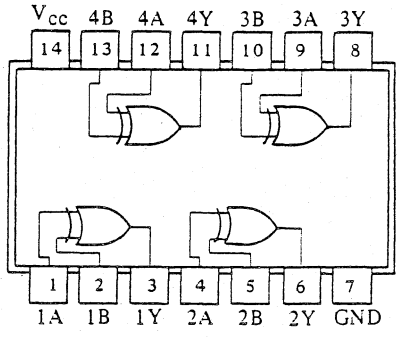
Positive logic: $Y = A + B = \overline{AB} + \overline{AB}$

FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

(Top view)

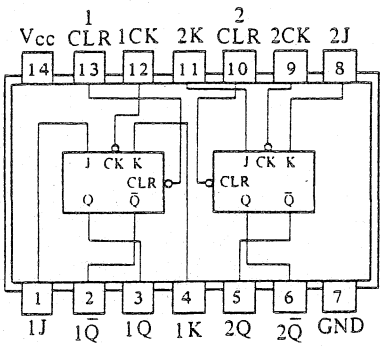


(20) MB74LS107M (SN74LS107N)

DUAL J-K FLIP-FLOPS WITH CLEAR

positive logic;

(Top view)



FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q
L	X	X	X	L	H
H	⎍	L	L	Q_0	Q_0
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGLE	

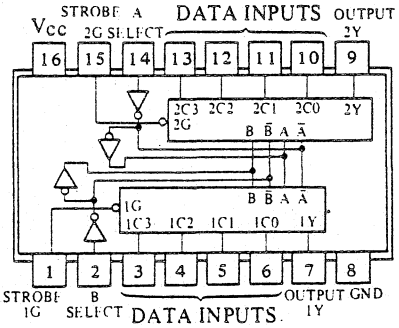
(21) MB74LS153N (SN74LS153N)

S153

QUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

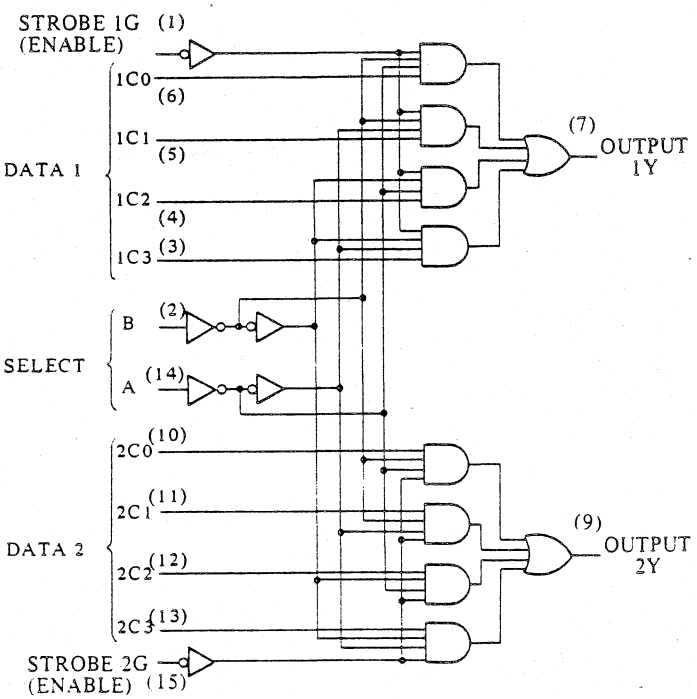
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)

(Top view)



Each of these monolithic, data selectors/ multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

functional block diagram



positive logic;

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H=high level, L=low level, X=irrelevant

(22) MB74LS155M (SN74LS155N)

DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLESERS

This monolithic transistor-transistor-logic (TTL) circuit features dual 1-line-to 4-line dimultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 10 is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

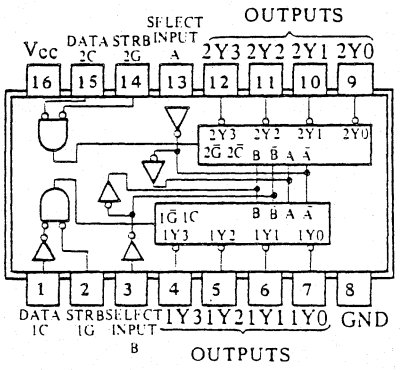
Positive logic;

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	1G	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	2G	2C				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

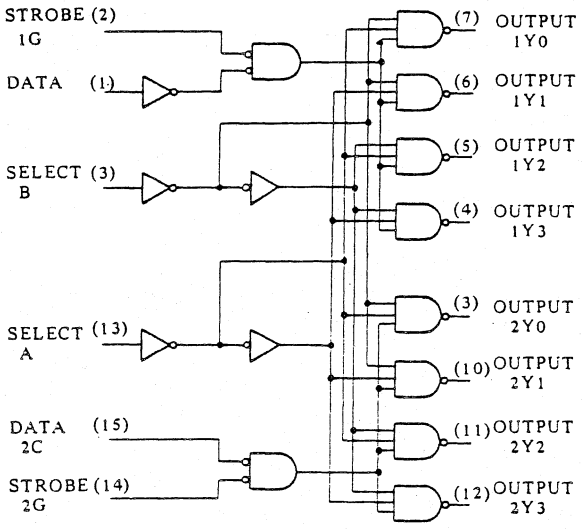
(Top view)



functional block diagram and logic

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L



C = inputs 1C and 2C connected together, G = inputs 1G and 2G connected together
H = high level, L = low lever, X = irrelevant

(23) MB74LS161A (SN74LS161N)

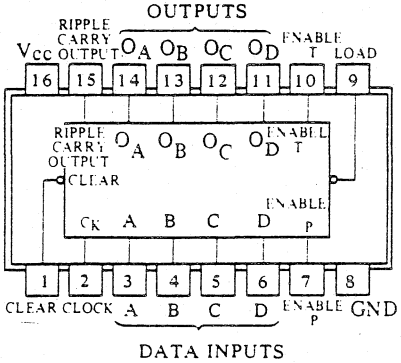
SYNCHRONOUS 4-BIT BINARY COUNTERSWITCH DIRECT CLEAR

This synchronous, presettable counters features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

The counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low lwvel at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is asynchronous and a low lwvel at the clear input sets all four of the flip-flop putputs low regardless of the levels of clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit sychronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a gigh-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

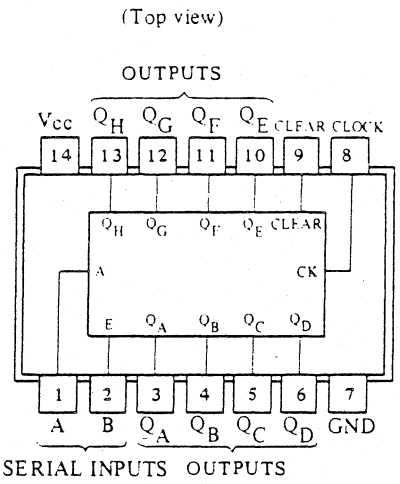
It features a fully independent clock circuit. Changes at control inputs (enable P or T, or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.



(Top view)

(24) MB74LS164M (SN74LS164N)

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS



These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete co-trol over incoming data as a low at either (or both) input(s) ingibits entry of the new data and resets the first flip-flop to the low level at he next clock pulse. A high-elvel input enables the other input which will then determine the state of the first flip-flop. Data at the ser-al inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

positive logic;

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	$Q_B \cdots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)

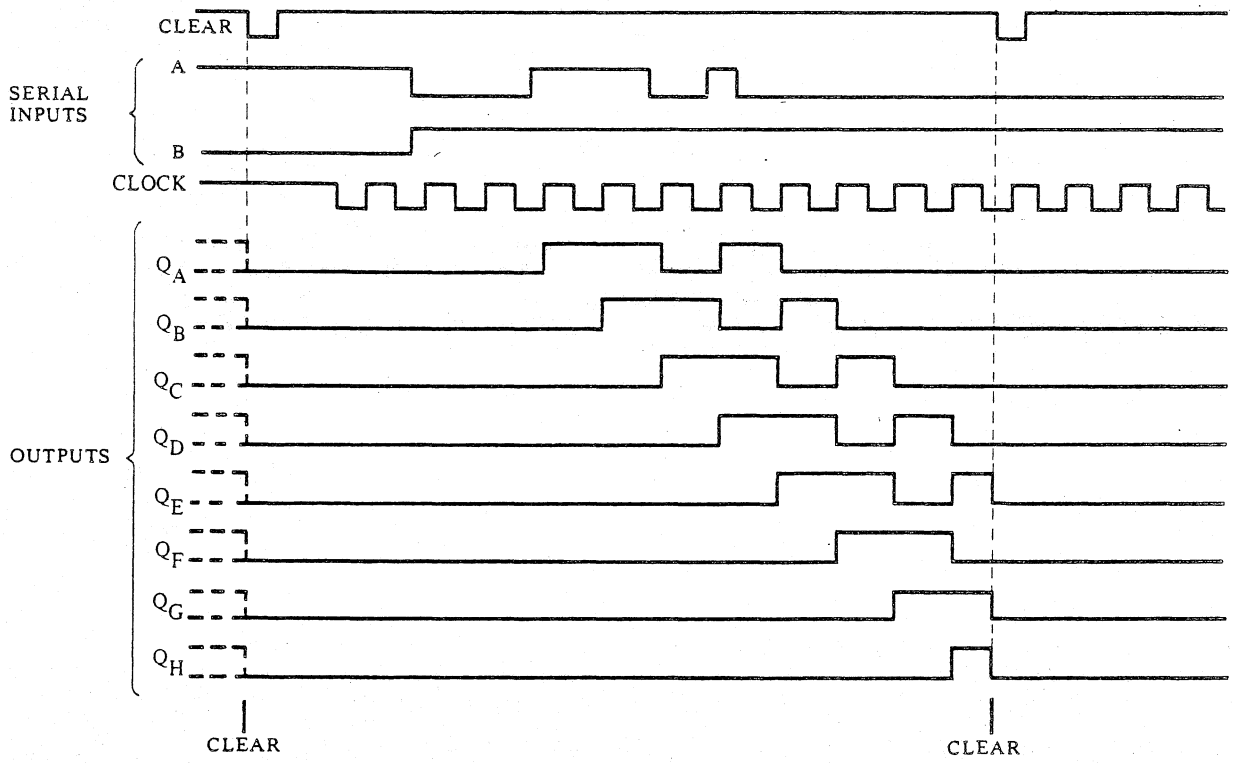
X = irrelevant (any input, including transitions)

↑ = transition from low to high level

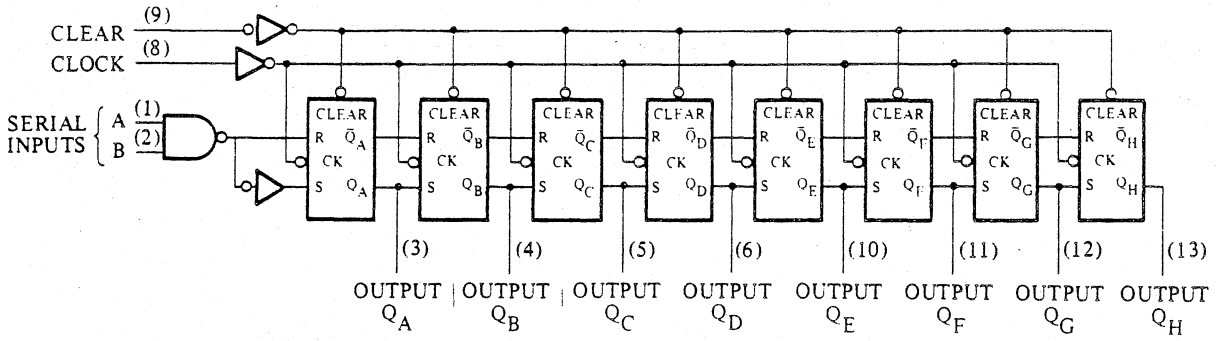
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift

typical clear, shift, and clear sequences



functional block diagram



(25) MB74LS191M (SN74LS191N)

SYNCHRONOUS 4-BIT UP/DOWN COUNTER

The LS191 is synchronous, reversible up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flipflops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

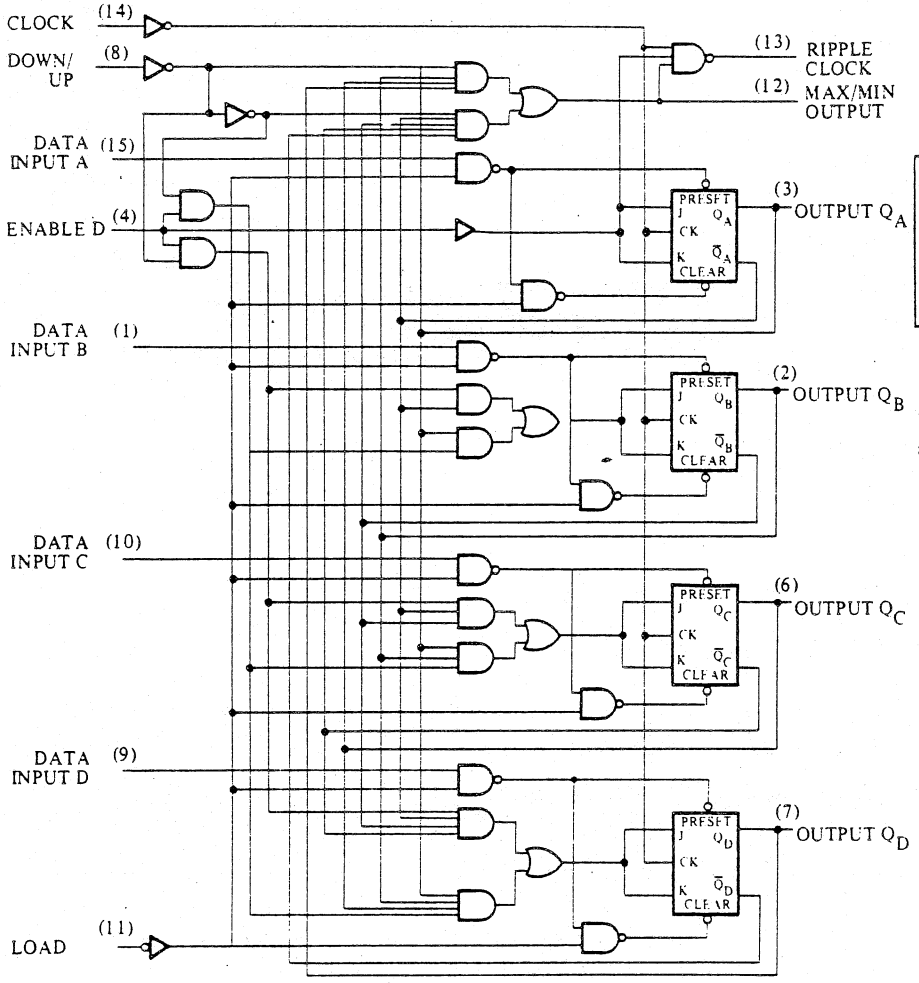
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The derection of the count is determined by the level of the down/up input. When low, the counter counts up and when gigh, it counts down. Level changes at the down/up input should be made only when the clock input is high.

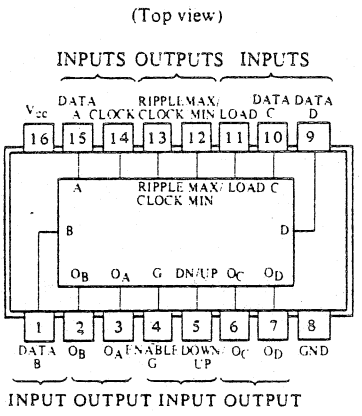
These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree withe the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulaw with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. Ther ripple clock output produces a low-level outpu pulse equal in which to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look ahead for high-spped operation.

positive logic:





asynchronous inputs:
Low input to load sets Q_A=A, Q_B=B, Q_C=C, and Q_D=D

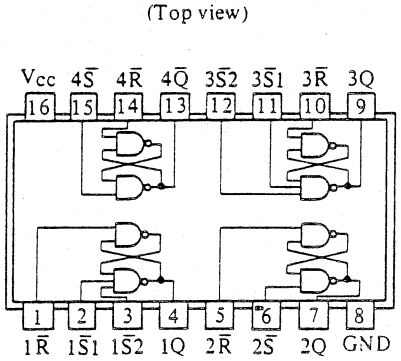
(26) SN74LS279N

QUAD $\overline{S}$-$\overline{R}$ LATCHES

DIODE-CLAMPED INPUTS
TOTEM-POLE OUTPUTS

FUNCTION TABLE

INPUTS $\overline{S}$	INPUTS $\overline{R}$	OUTPUT Q
H	J	Q_O
L	H	H
H	L	L
L	L	*



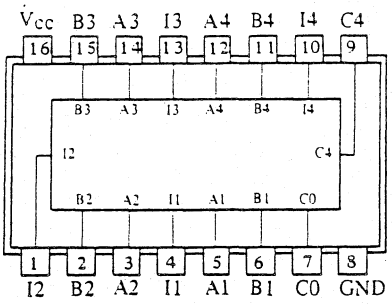
H = high level
L = low level
Q_O = the level of Q before the indicated input conditions were established.

* This output level is pseudo stable, that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs retrn to their inactive (high) level.
For latches with double $\overline{S}$ input.
H = both $\overline{S}$ input high
L = one or both $\overline{S}$ inputs low

(27) MB74LS283M (LN74LS283M)

4-BIT BINARY FULL ADDER

(Top view)



This full adder perfoms the addition of two 4-bit binary works. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These address feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds typically. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true from. End around carry can be accomplised without the need for logic or level inversion.

positive logic;

FUNCTION TABLE

INPUT				OUTPUT					
				WHEN CO-L			WHEN CO-H		
						WHEN C2-L			WHEN C2-H
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

(28) MB440M (SN74123)
SN74LS123N

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

This monolithic TTL retriggerable monostable multivibrator features d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provides overriding direct clear inputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. The output pulse is primarily a function of the external capacitor and resistor.

For Cext 1000pF, the output pusle width (tw) is defined as:

$$tw = 0.32RtCext\ (1 + \frac{0.7}{Rt})$$

tw : ns

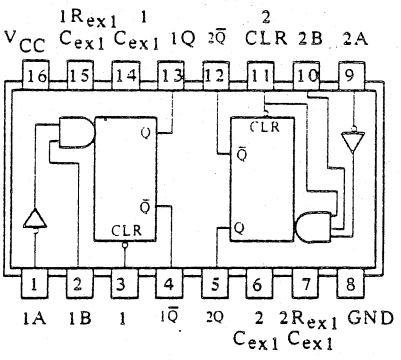
Rt : kohms

Cext : pF

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

(Top view)



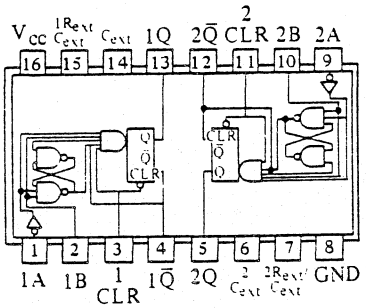
(29) SN74LS221N
SN74221N

DUAL MONOSTABLE MULTIVIBRATORS

The SN74LS221N and SN74221N are monolithic dual multivibrators. Each multivibrator features a negative-transition-triggered input and a posi-ive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to Vcc noise of typically 1.5 volts is also provided by internal latching circuitry.

(Top view)



Positive logic: Low input to clear resets Q low and $\bar{Q}$ high regardless of d-c levels at A or B inputs.

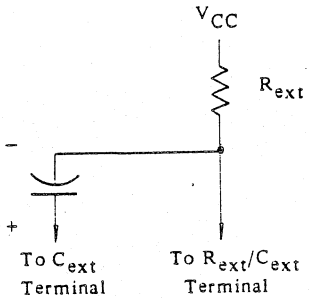
FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	⊓	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

The output pulse width (tw) defined as:

$$tw = 0.7 R_{ext} C_{ext}$$

tw ; ns, R_{ext} : kohms, Cext : pf



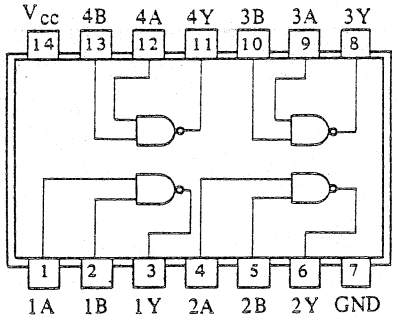
TIMING COMPONENT CONNECTIONS

(30) MB463M (SN7438N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic: $Y = \overline{AB}$

(Top view)



(31) MB434M (SN75451BP)

DUAL PERIPHERAL POSITIVE-AND DRIVERS

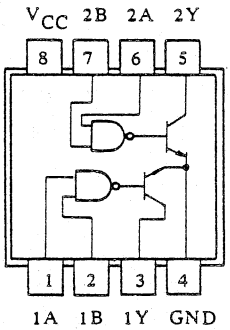
positive logic: $Y = AB$

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on stage)
H	H	H (off state)

H=gigh level, L=low level

(Top view)

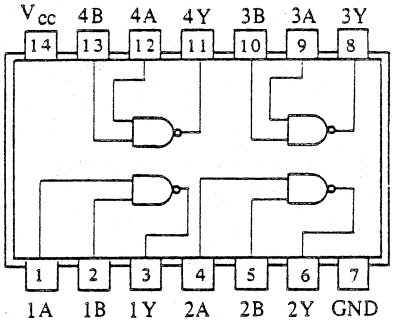


(32) MB435M (SN7437N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

positive logic: $Y = \overline{AB}$

(Top view)

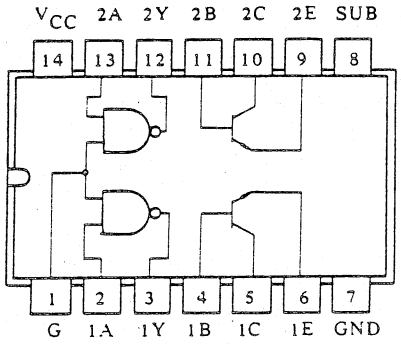


(33) MB439M (SN75450BN)

DUAL PERIPHERAL POSITIVE-AND DRIVERS

positive logic:
$Y = \overline{AG}$ (gate only)
C = AG (gate and transistor)

(Top view)

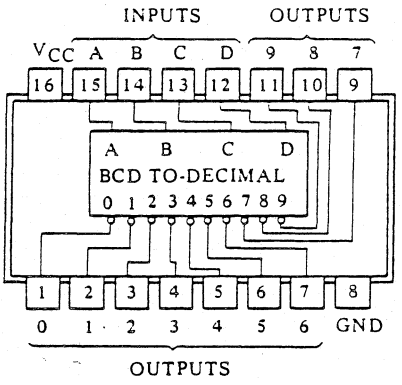


(34) MB443M (SN74145N)

BCD-TO-DECIMAL DECODERS/DRIVERS

This monilithic BCD-to-decimal decoder/drivers consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full dedoding of valid BCD input logic endures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as spen-collector logic-circuit drivers. Each of the high-breakdwn output transistors (15 volts) will sink up to 80 milliamperes of current. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits.

(Top view)



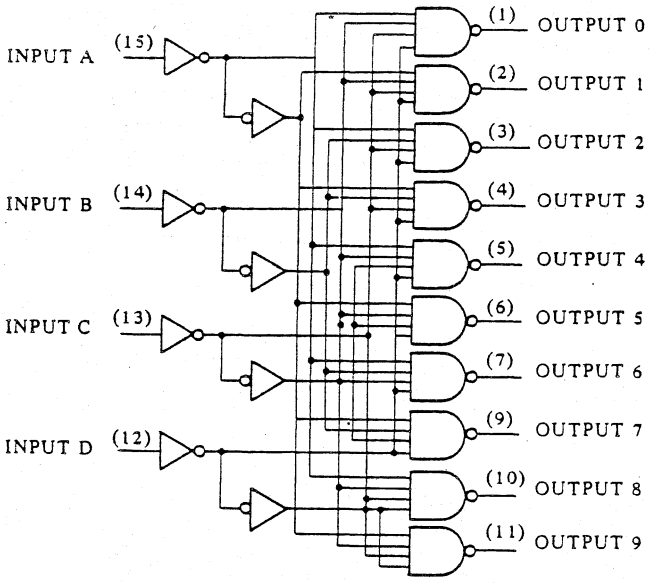
Positive logic

FUNCTION TABLE

No.	INPUTS D	C	B	A	OUTPUTS 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off),
L = low level (on)

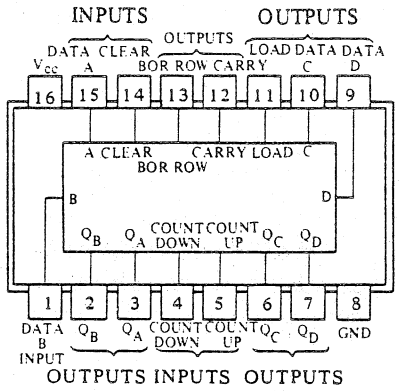
functional block diagram



(35) SN74193

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.



(Top view)

logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

(36) SN75452

DUAL PERIPHERAL POSITIVE-NAND DRIVERS

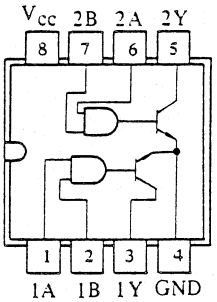
positive logic: $Y = \overline{AB}$

FUNCTION TABLE
(EACH DRIVER)

A	B	
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level

(Top view)



(37) SN74S112N

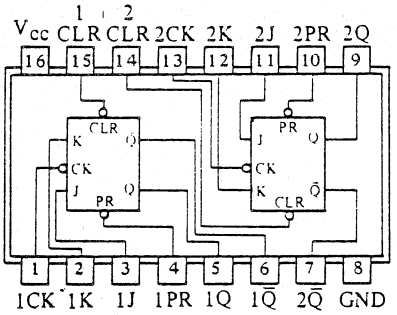
DUAL J-K ENGATEVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET AND CLEAR

positive logic;

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	L	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	Q_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	Q_0

(Top view)



(38) SN75107AN
SN75108AN

DUAL LINE RECEIVERS

The 107A, and 108A line receivers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

These receivers feature indipendent channels with common voltage supply and ground terminals. The 107A features TTL-compatible active pull-up (totem-pole) outputs. The 108A is also TTL-compatible, but features an open-collector output configuration that permits the wired-AND logic connection with similar outputs. This permits a level of logic to be implemented without extra delay.

The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

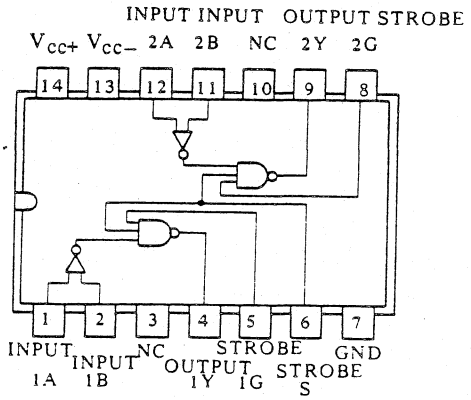
The receivers feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity is particularly impoutant when data is to be detected aththe end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. These line receivers are designed to detect input signals of 25 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} > 25mV$	X	X	H
$-25mV < V_{ID} < 25mV$	X	L	H
	L	X	H
	H	H	INDETERMINATE
$V_{ID} < -25mV$	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level,
X = irrelevant



NC – No internal connection

(Top view)

(39) SN75110A

DUAL LINE DRIVERS

These drivers feature independent channels with common voltage supply and tround terminals. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The putput current can be switched off (inhibited) by low logic levels on the inhibit inputs. The output current is nominally 12 milliamperes.

The inhibit feature is provided so the circuits can be used in party-line or data-bus appl-cations. Astrobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The putput impedance of the driver in the inhibited mode is very high-the putput impedance of a transistor biased to cutoff.

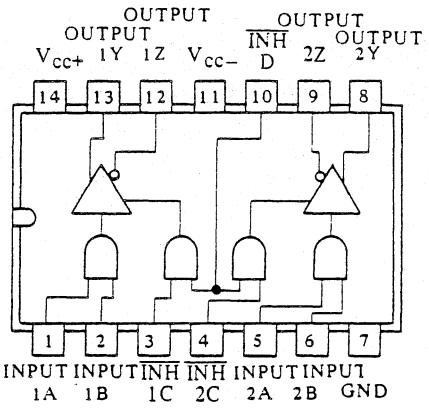
The driver outputs have a common-mode voltage range of -3 volts to 10 volts, allowing common-mode voltage on the line without affecting driver performance.

FUNCTION TABLE

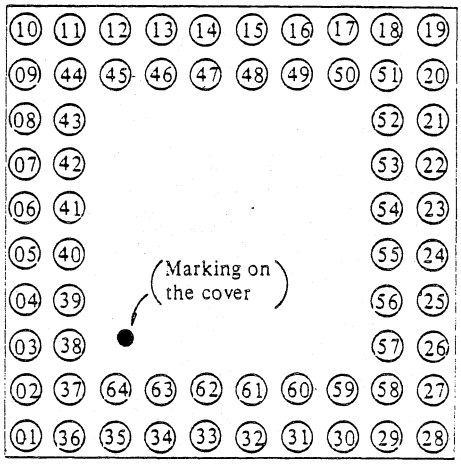
LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = high level, L = low level,
X = irrelevant

(Top view)



(Bottom view)



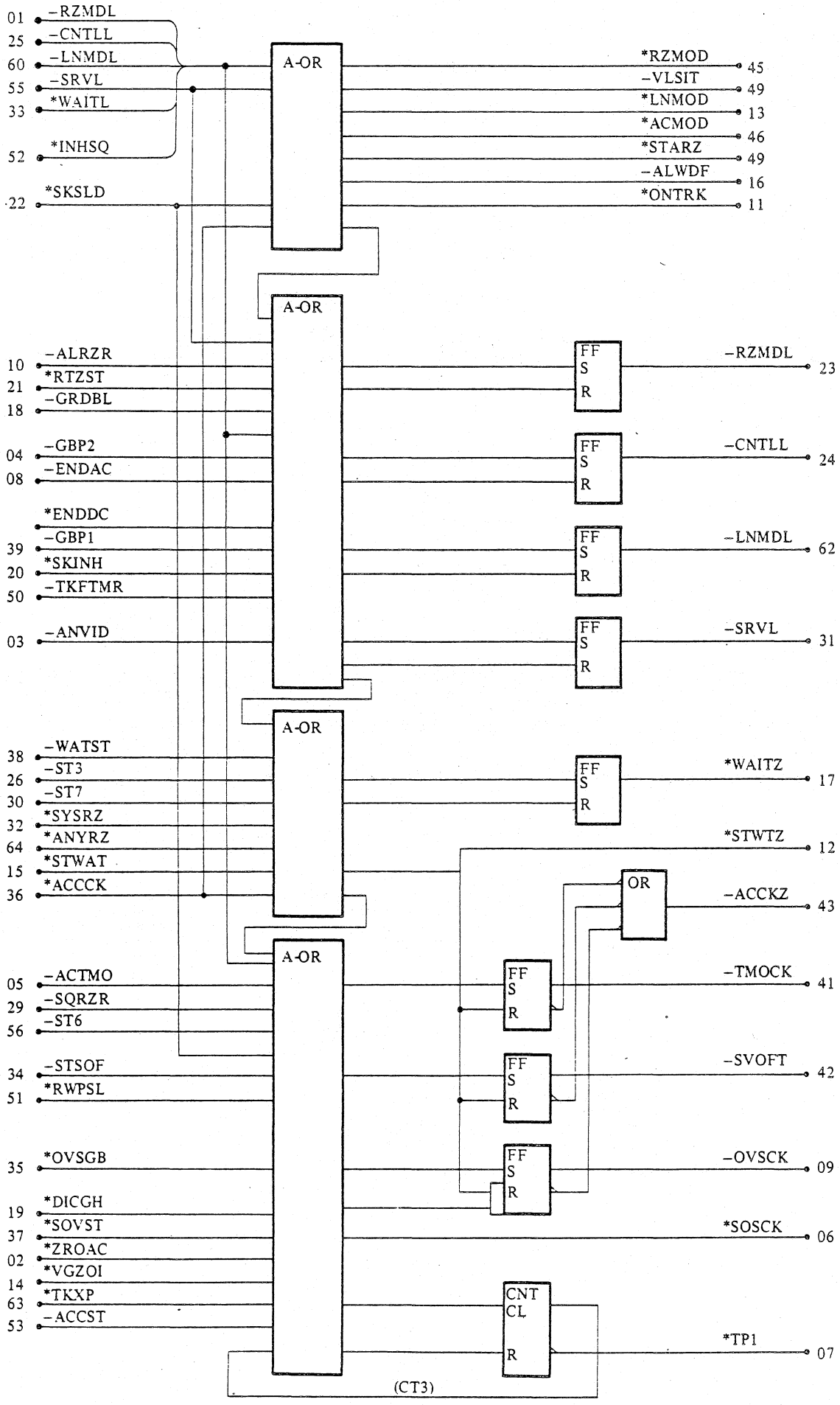
(40) MB15139C

ACCESS CONTROL

This Bipolar 500-Gate LSI has features to contol and check the rezero and seek operation of disk drive.

Package; 64-pin RIT

Pin-
+5V ; 47, 61
0V; 40, 54


01 -RZMDL
25 -CNTLL
60 -LNMDL
55 -SRVL
33 *WAITL
52 *INHSQ
22 *SKSLD
A-OR
*RZMOD 45
-VLSIT 49
*LNMOD 13
*ACMOD 46
*STARZ 49
-ALWDF 16
*ONTRK 11
A-OR
10 -ALRZR
21 *RTZST
18 -GRDBL
04 -GBP2
08 -ENDAC
*ENDDC
39 -GBP1
20 *SKINH
50 -TKFTMR
03 -ANVID
FF S R
-RZMDL 23
-CNTLL 24
-LNMDL 62
-SRVL 31
A-OR
38 -WATST
26 -ST3
30 -ST7
32 *SYSRZ
64 *ANYRZ
15 *STWAT
36 *ACCCK
*WAITZ 17
*STWTZ 12
OR
-ACCKZ 43
A-OR
05 -ACTMO
29 -SQRZR
56 -ST6
34 -STSOF
51 *RWPSL
35 *OVSGB
19 *DICGH
37 *SOVST
02 *ZROAC
14 *VGZOI
63 *TKXP
53 -ACCST
-TMOCK 41
-SVOFT 42
-OVSCK 09
*SOSCK 06
CNT CL R
*TP1 07
(CT3)

(41) MB15140C

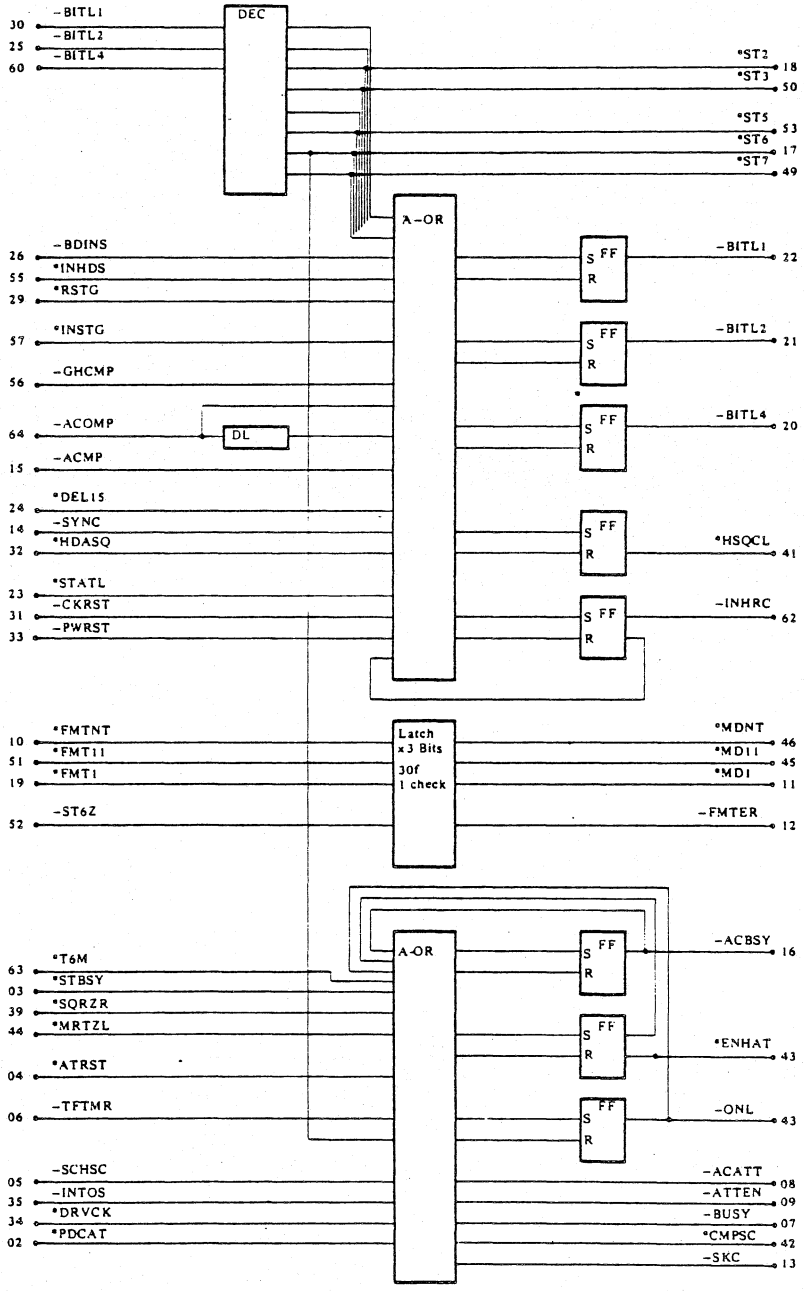
HDA SEQUENCER

This Bipolar 500-Gate LSI has the following functions when used in the desk drive.

- Sequence control of spindle motor
- Generation of machine status information

Package ; 64-pin, RIT

functional block diagram

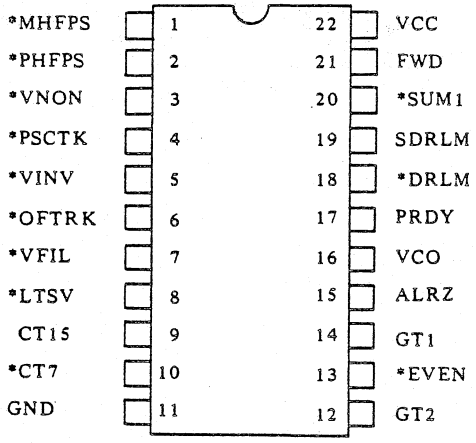


(42) MB14601C

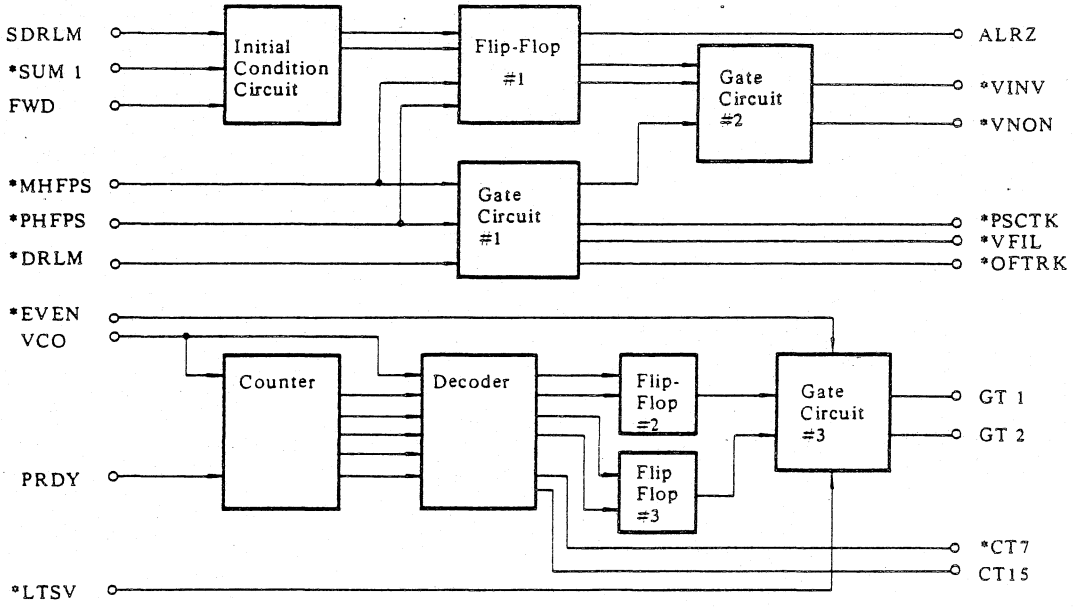
LINEAR MOTOR CONTROL

This Bipolar 200-Gate LSI generates gating signals to sense both the position signal and the velocity signal. The position logic portion in the IC forms a PLL circuit in conjunction with a VCO. The velocity logic portion contains a polarity check circuit and a gate signal generator for velocity signal demodulation.

(Top view)



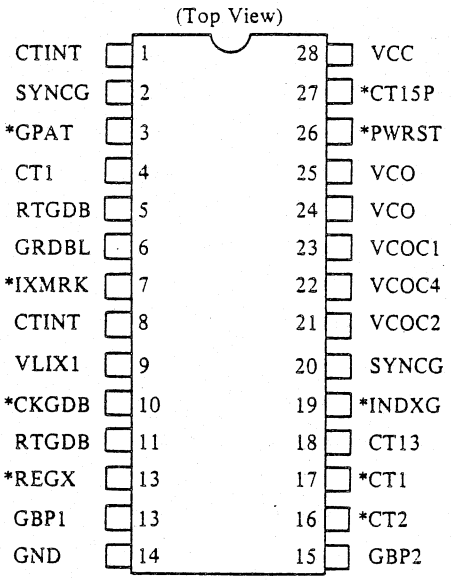
functional block diagram



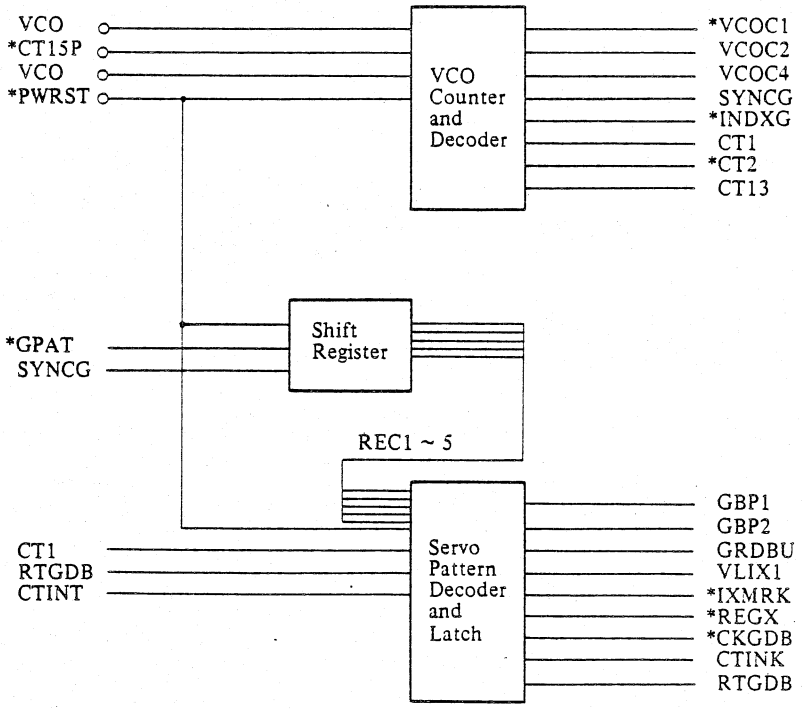
(43) MB14613C

Servo Pattern Detector

This circuit identifies the Servo Patterns and detects guard band 1, guard band 2, index and the outer guard band.



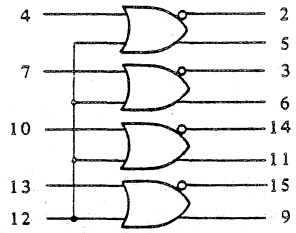
functional block diagram



(44) MB10101C (MC10101)

QUAD 2-INPUT OR/NOR GATES

POSITIVE LOGIC

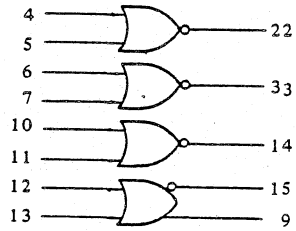


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

(45) MB10102C (MC10102)

QUAD 2-INPUT NOR GATES

POSITIVE LOGIC

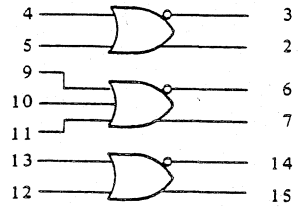


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

(46) MB10105C (MC10105)

TRIPLE 2-3-2 INPUT OR/NOR GATES

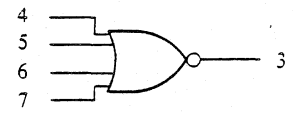
POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

(47) MB10106C (MC10106)

TRIPLE 4-3-3 NOR GATES

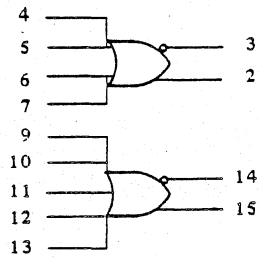


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

(48) MB10109 (MC10109)

DUAL 4-5 INPUT OR/NOR GATES

POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

(49) MB10116 (MC10116)

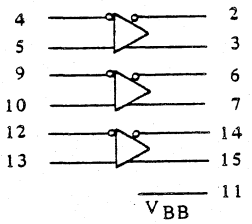
TRIPLE LINE RECEIVERS

The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base gias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input function.

POSITIVE LOGIC



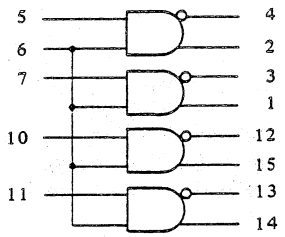
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

(50) MB10124 (MC10124)

QUAD MTTL TO MECL TRANSLATORS

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

POSITIVE LOGIC



Gnd = Pin 16
Vcc (+5V) = Pin 9
V_{EE} (−5.2V) = Pin 8

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in MECL 10,000 out.

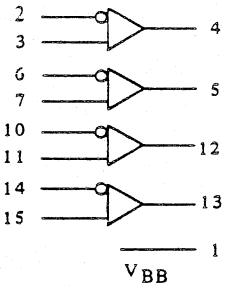
An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

(51) MB10124 (MC10125)

QUAD MECL TO MTTL TRANSLATORS

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky MTTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting teanslator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

POSITIVE LOGIC



Gnd = Pin 16
Vcc (+5V) = Pin 9
V_{EE} (−5.2V) = Pin 8

Power supply requirements are ground, +5.0 Volts and 05.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

An abvantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

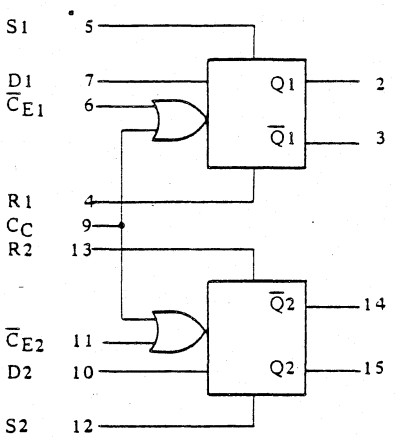
(52) MB10131 (MC10131)

DUAL D-TYPE MASTER-SLAVE FLIP-FLOPS

The MC10131 is a dual master-slave type D flip=rlop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) input. Each flip-flip-flop may be clocked Separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not after the output information at any other time due to master slave construction.

POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rese and fall times have been optimized to provide relaxation of system design and layout criteria.

RS TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care

$C = \overline{C}_E + C_C$

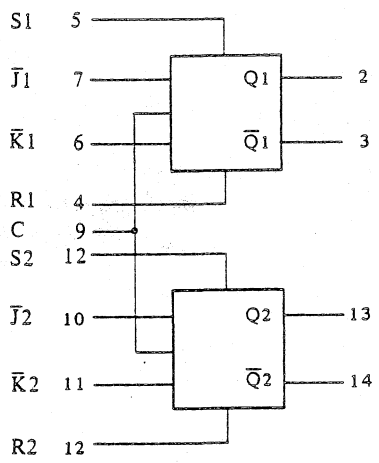
A clock H is a clock transition from a low to a high state.

(53) MB10135C (MC10135)

DUAL J-K MASTER-SLAVE FLIP-FLOPS

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.
A common clock is provided with separate $\overline{J}$ $\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not dffect the output.
The output states of the flip-flop change on the positive transition of the clock.
Input pulldown resistors eliminat the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

R	S	Q_{n+1}
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCK J-K TRUTH TABLE

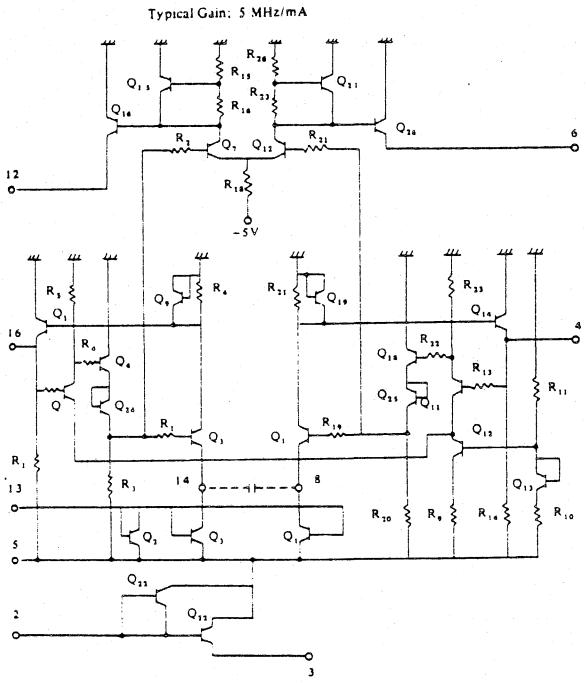
J	K	Q_{n+1}
H	L	Q_n
L	H	H
H	H	Q_n

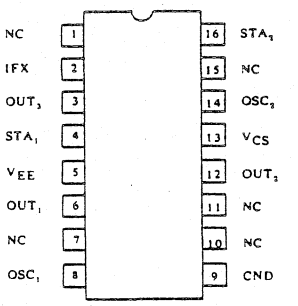
Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

(54) HD103107

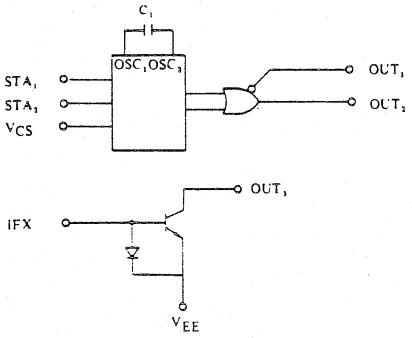
VOLTAGE CONTROLLED OSCILLATOR

Typical Gain; 5 MHz/mA





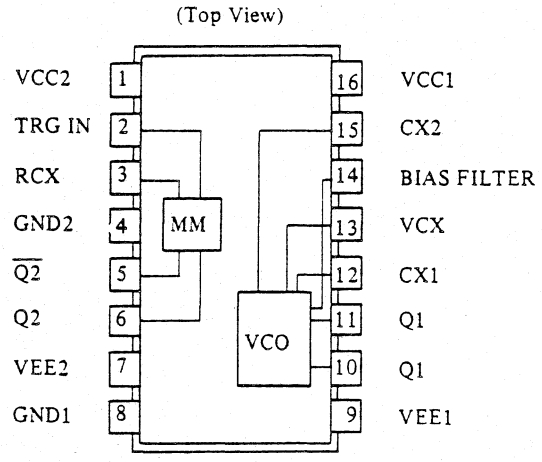
Functional block diagram



(55) MB4306C

VOLTAGE CONTROLLED OSCILLATOR

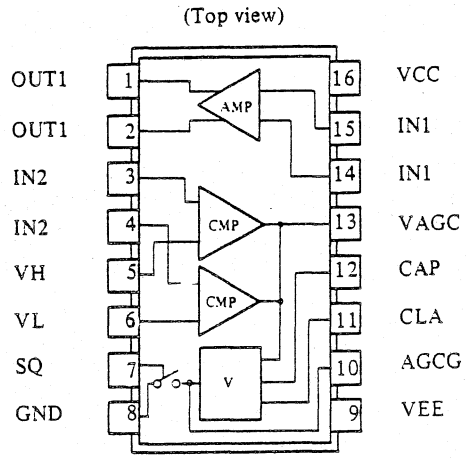
The MB4306C is mainly used as an oscillator with its oscillating frequency synchronou with the rotational speed of the disks. The output clock signal is used to modulate and demodulate the write and read data. The circuit consists of two portions, one is oscillator whose output frequency varies with the input control voltage level, and the other is a monostable multi-vibrator which is generally used in demodulating the read data.



(56) MB4311C

LEVEL SENSOR

The MB4311C is used in conjunction with the MB4303C (AGC Amplifier) to keep the read out signal derived from a magnetic head at a constant level. It also contains an amplifier with a gain of 10.

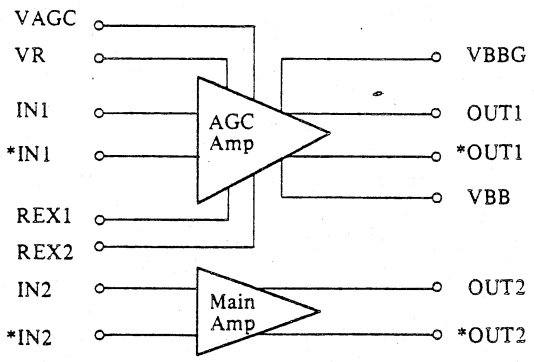


(57) MB4303C

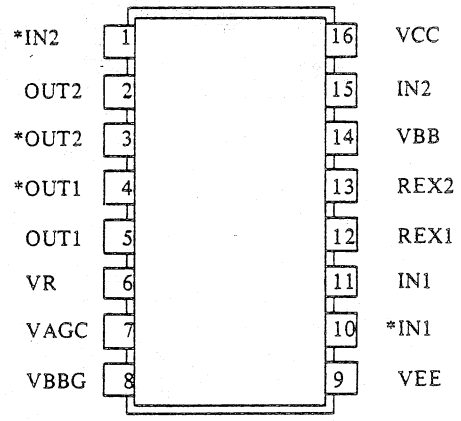
AGC AMPLIFIER

The MB4303C is used in conjunction withe the MB4311C (Level Sensor) to keep the read out signal derived from a magnetic head at a constant level. It also contains an amplifier.

Functional block diagram



(Top view)

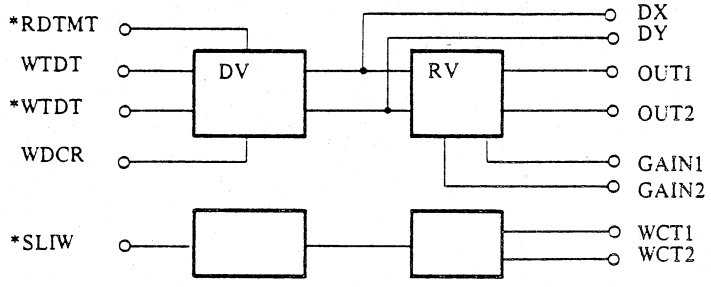


(58) MB4316C

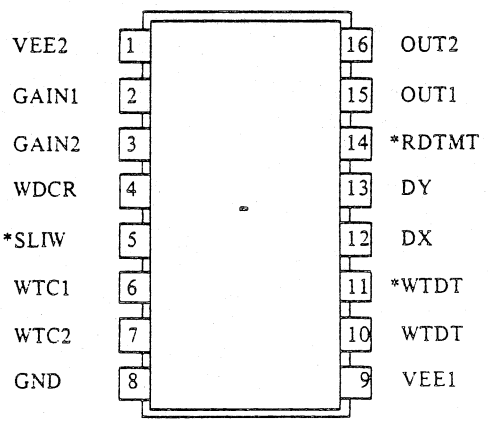
READ/WRITE BUS SWITCH C

The MB4316C contains a driver and a receiver circuit to transmit write/read data to/from the Head IC. It also generates the write-current which flows in a magnetic head during a write operation.

Functional block diagram



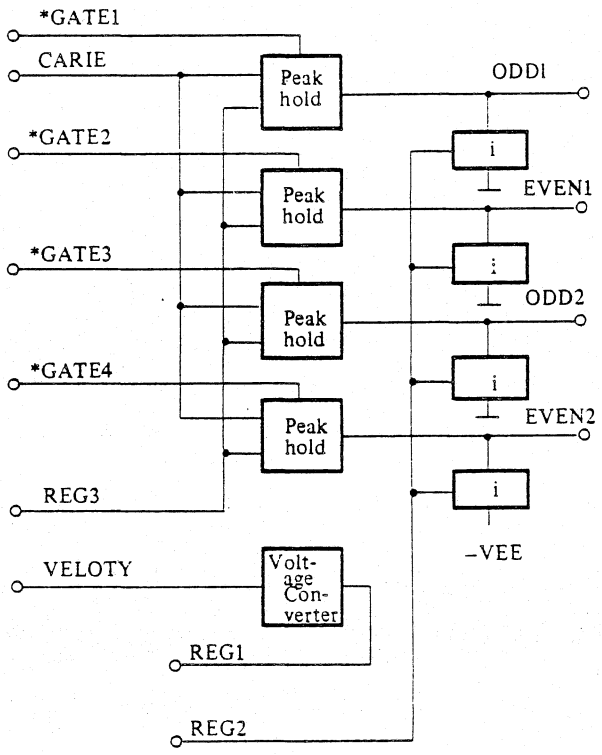
(Top view)

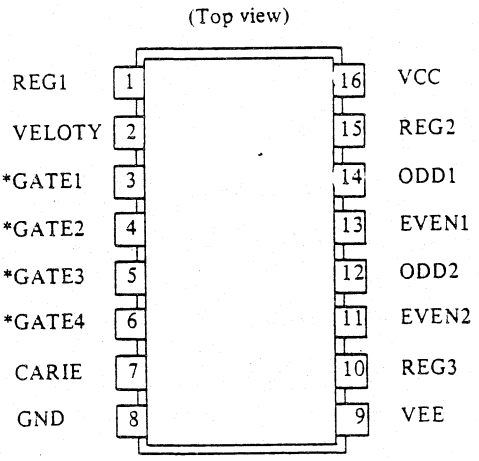


(59) MB4319C

PEAK HOLD

The MB4319C is used in the position sensing circuit of the disk drive. The peak-voltage of raw-servo signal is hold for demodulating inot the position signal.





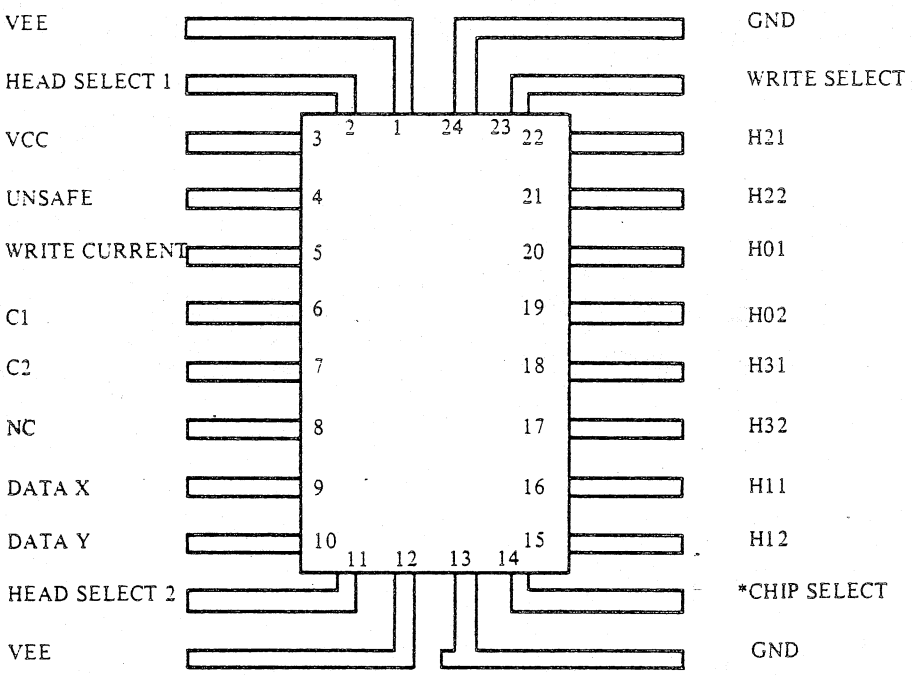
(60) MB4112 (SS1105)
MB4113

DISK HEAD IC (FIXED/MOVABLE)

The MB4112 and MB4113 are analog LSIs for Fixed-Head and Movable-Head respectively used in the disk drive. The MB4112 has lower amplifier gain depending on characteristics of magnetic head. Both can control up to four heads and contain the vollowing circuits.

- Read amplifier
- Write amplifier
- RAS circuit
- Head select circuit

(Top view)

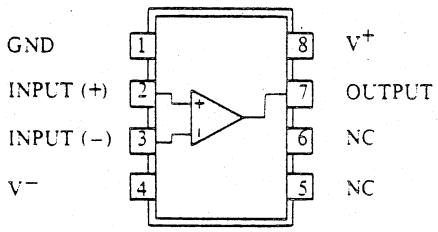


(61) MB4002M

HIGH SPEED DIFFERENTIAL COMPARATOR

The MB4002M is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. The device is useful as a variable threshold Schmitt trigger, a pulse height descriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

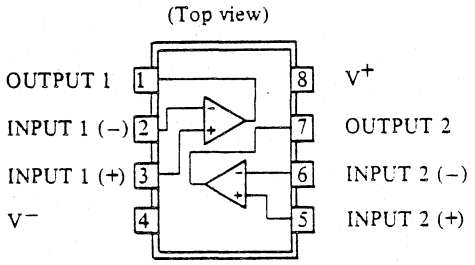
(Top view)



(62) MB3607M (μpC251C, MC1458C)

DUAL OPERATIONAL AMPLIFIERS

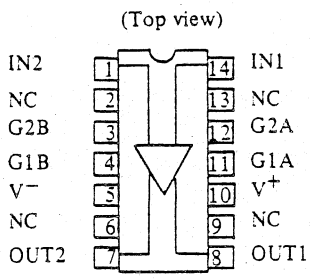
The MB3607M is designed for use as a summing amplifier integrator, or amplifier with operating characteristics as a function of the external feed-back components.



(63) MB3501M (μA733DM)

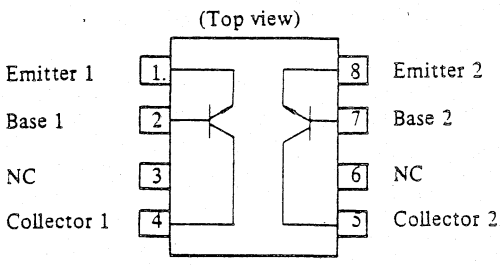
DIFFERENTIAL VIDEO AMPLIFIER

The MB3510M is a monolithic tow-stage Differential Input and Output Video Ampifier. Internal series-shunt feedback is used to obtain wide bandwidth, low phase destortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitime loads and all stages are current-source biased to obtain high power supply and common mode rejection rations. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed this film or plate wire memories. Other applications applications include general purpose video and pulse amplifiers where wide bandwidth, low phase dhift, and excellent gain stability are required.



(64) MB5365M

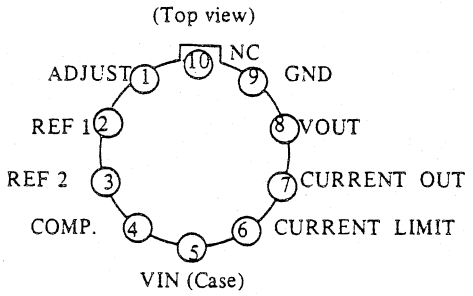
NPN DUAL TRANSISTORS



(65) μPC142A

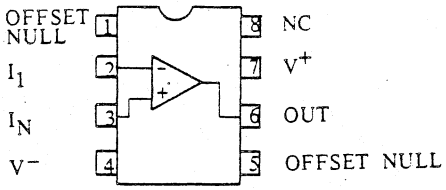
NEGATIVE VOLTAGE REGULATOR

The μPC142A is a precision negative voltage regulator, consisting of temperature-compensated reference constant current source and a differential error amplifier with emitter follower input. The output voltage is adjustable from -0.035V to 030V. In addition, an external pass transistor enhances output current capability up to 10A. The current limiting circuit is incorporated and the limiting current is externally adjustable. The applications include nagative voltage supply for operational amplifiers.



(66) μPC151C

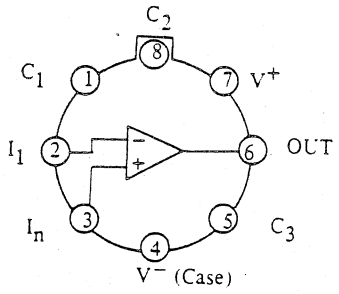
FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER



(67) μPC159A

HIGH SPEED WIDE BAND OPERATIONAL AMPLIFIER

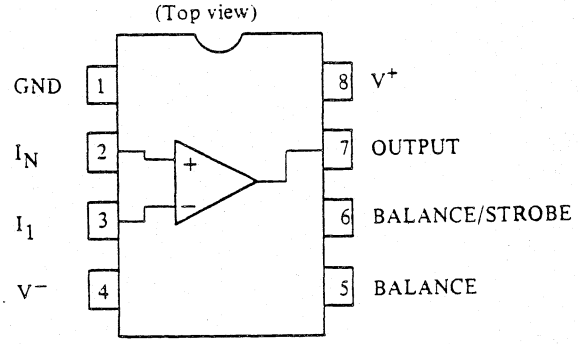
(top view)



(68) μPC271C

VOLTAGE COMPARATOR

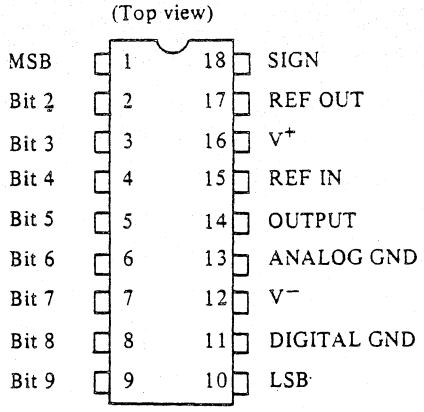
This is a single high-speed voltage comparator. This device is designed to operate from a wide range of power supply voltage, including ±15V supplies for operational amplifiers and +5 supplies for logic systems. The output level is compatible with most DTL, TTL, and MOS circuits. This comparator is capable of driving Lamps or relays and switching voltage up to 50V at 50mA. All inputs and outputs can be isolated from system ground. The output can drive loads referenced to ground, Vcc+, Vcc-. Offset balancing and strobe capability are available and the output can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the defferential input.



(69) μPC610D

10-BIT D/A CONVERTER

The μPC610D is a complete 10 bit plus sign D/A convertor. All elements of a complete sign/magnitude DAC are included-precision voltage reference, current steering logic, current sources, R-2R resister network, logic controlled polarity switch and high speed internally compensated output of amp. The wide power supply range, low power consumption, choice of full scale output voltages and sign/magnitude coding assure utility in a wide range of applications.



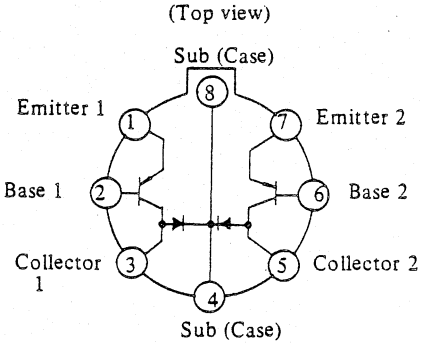
(70) μPA49A

PNP DUAL TRANSISTORS

IC = -50 mA

f_T = 250 MHz

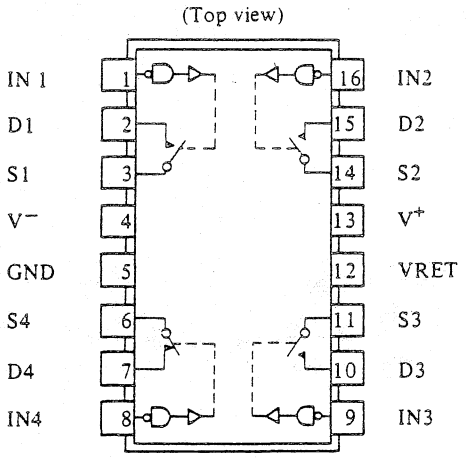
Pc = 300 mW/UNIT



(71) DG201BK

QUAD ANALOG SWITCHES

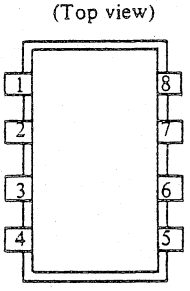
The DG201 is a 4-channel single pole signal throw analog switch which employs CUOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no fooset voltage in the ON condition, and block voltages up to 30V peak-to-peak in the OFF condition. The)N-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (OVto 0.8V) the switch will be ON, and a logic "1" (214V to 15V) will turn the switch OFF. Switch action is break-before-make.



LOGIC	SWITCH
0	ON
1	OFF

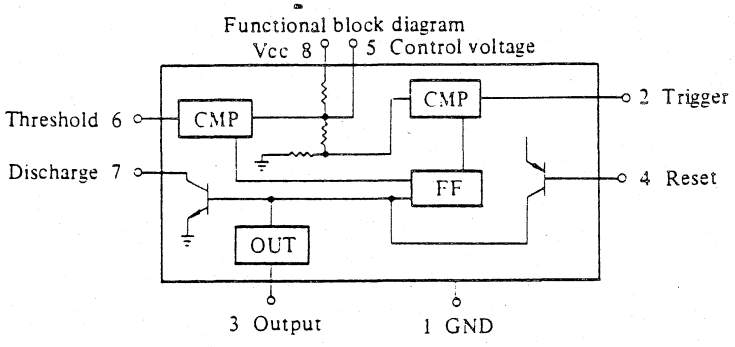
(72) M51841P

TIMING CIRCUIT



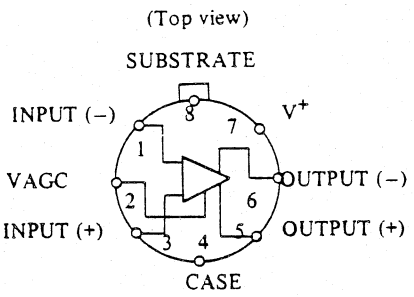
This monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

functional block diagram



(73) MC1590G

AGC AMPLIFIER

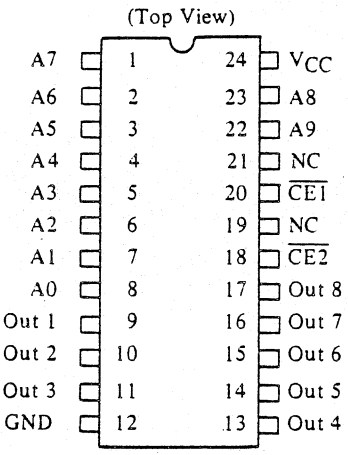


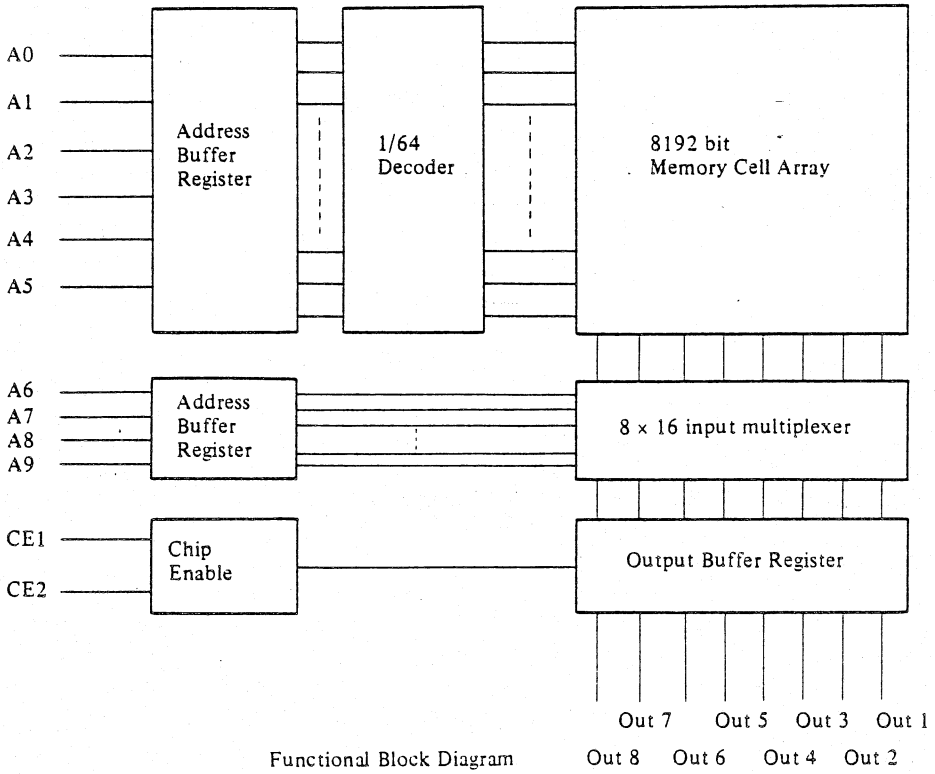
(74) MB7055C

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MB7055C is a 1024 × 8 bit bipolar programmable read only memory

A0 ~ A9 ; Address input
Out1 ~ Out8; Data Output
CE1 CE2 ; Chip enable
Vcc ; +5V





Functional Block Diagram

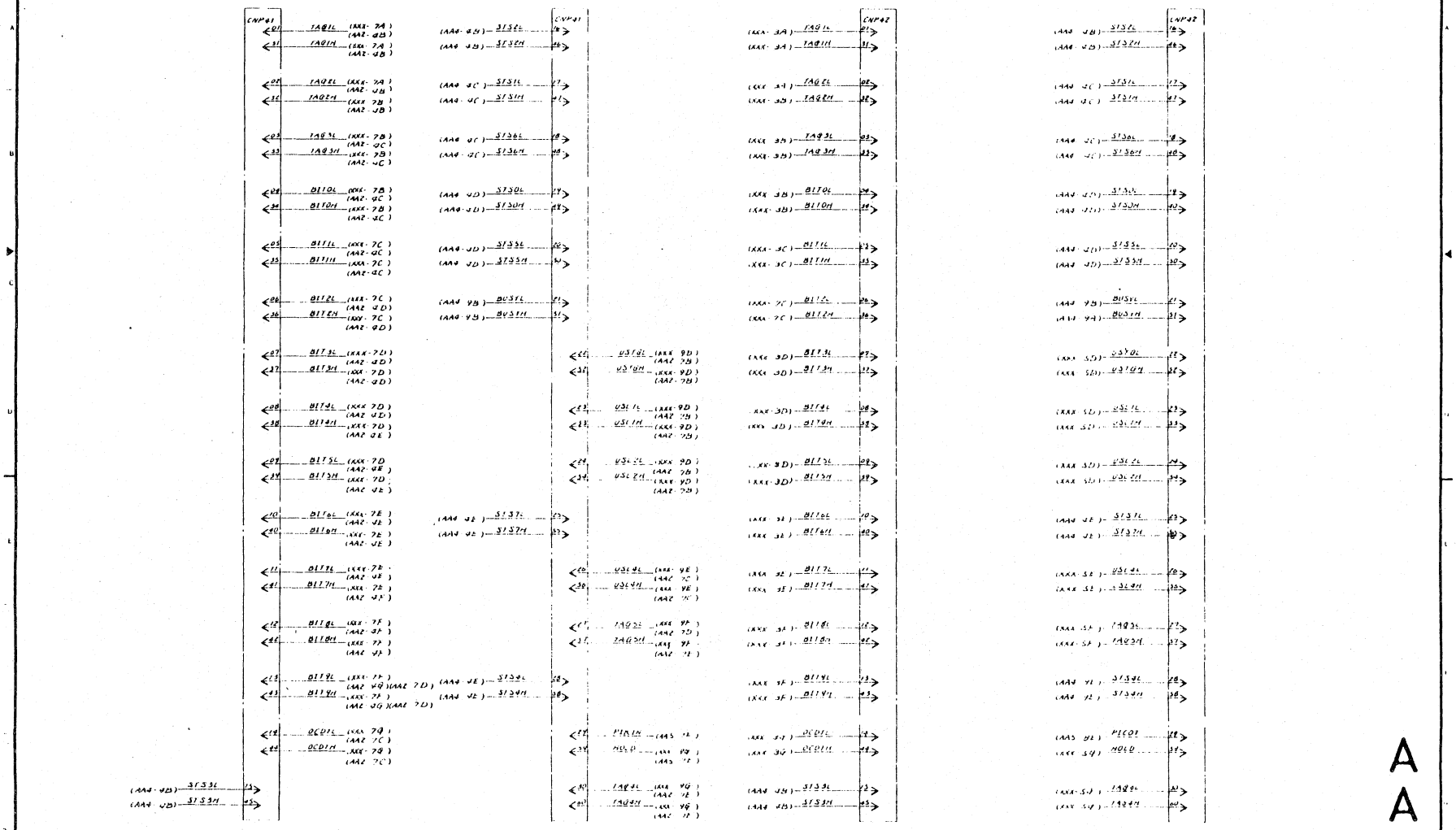
SHEET	ARRN	TITLE
001		Schematics/Drawings List
002	AA1	CH.A Interface Circuit Diagram (1)
003	AA2	CH.A Interface Circuit Diagram (2)
004	AA3	CH.A Interface Circuit Diagram (3)
005	AA4	CH.A Interface Circuit Diagram (4)
006	AA5	CH.A Interface Circuit Diagram (5)
007	AB1	CH.B Interface Circuit Diagram (1)
008	AB2	CH.B Interface Circuit Diagram (2)
009	AB3	CH.B Interface Circuit Diagram (3)
010	AB4	CH.B Interface Circuit Diagram (4)
011	AB5	CH.B Interface Circuit Diagram (5)
012	AB6	CH.B Interface Circuit Diagram (6)
013	AB7	CH.B Interface Circuit Diagram (7)
014	BA1	Interface Circuit Diagram (1)
015	BA2	Interface Circuit Diagram (2)
016	BA3	Interface Circuit Diagram (3)
017	CA1	Access Control Circuit Diagram (1)
018	CA2	Access Control Circuit Diagram (2)
019	CA3	Access Control Circuit Diagram (3)
020	CA4	Access Control Circuit Diagram (4)
021	CA5	Access Control Circuit Diagram (5)
022	DA1	Head Address Register Circuit Diagram
023	FA1	R/W Control Circuit Diagram (1)
024	FA2	R/W Control Circuit Diagram (2)
025	FA1	VFO Control Circuit Diagram (1)
026	FA2	VFO Control Circuit Diagram (2)
027	FA3	VFO Control Circuit Diagram (3)
028	GA1	Sector Control Circuit Diagram (1)
029	GA2	Sector Control Circuit Diagram (2)
030	HA1	Servo Pattern Detector Circuit Diagram (1)

SHEET	ARRN	TITLE
031	HA2	Servo Pattern Detector Circuit Diagram (2)
032	HA3	Servo Pattern Detector Circuit Diagram (3)
033	JA1	OP Sequencer Circuit Diagram (1)
034	JA2	OP Sequencer Circuit Diagram (2)
035	JA3	OP Sequencer Circuit Diagram (3)
036	KA1	Servo Circuit Diagram
037	LA1	Read Amplifier Circuit Diagram
038	MA1	Internal Connection Circuit Diagram (1)
039	MA2	Internal Connection Circuit Diagram (2)
040	MA3	Internal Connection Circuit Diagram (3)
041	MA4	Internal Connection Circuit Diagram (4)
042	MA5	Internal Connection Circuit Diagram (5)
043	MA6	Internal Connection Circuit Diagram (6)
044	MA7	Internal Connection Circuit Diagram (7)
045	MA8	Internal Connection Circuit Diagram (8)
046	MB1	Internal Cable Connection Diagram (1)
047	MB2	Internal Cable Connection Diagram (2)
048	PA1	Power Unit Circuit Diagram (1)
049	PA2	Power Unit Circuit Diagram (2)
050	RA1	Read Amplifier Circuit Diagram (1)
051	RA2	Read Amplifier Circuit Diagram (2)
052	RA3	Read Amplifier Circuit Diagram (3)
053	RA4	Read Amplifier Circuit Diagram (4)
054	RA5	Read Amplifier Circuit Diagram (5)
055	RB1	Variable Freq. Osc. Circuit Diagram (1)
056	RB2	Variable Freq. Osc. Circuit Diagram (2)
057	RB3	Variable Freq. Osc. Circuit Diagram (3)
058	RB4	Variable Freq. Osc. Circuit Diagram (4)
059	RB5	Variable Freq. Osc. Circuit Diagram (5)
060	RB6	Variable Freq. Osc. Circuit Diagram (6)

SHEET	ARRN	TITLE
061	SA1	Position Sensing Circuit Diagram (1)
062	SA2	Position Sensing Circuit Diagram (2)
063	SA3	Position Sensing Circuit Diagram (3)
064	SB1	Servo Control Circuit Diagram (1)
065	SB2	Servo Control Circuit Diagram (2)
066	SB3	Servo Control Circuit Diagram (3)
067	SB4	Servo Control Circuit Diagram (4)
068	SB5	Servo Control Circuit Diagram (5)
069	SB6	Servo Control Circuit Diagram (6)
070	SB7	Servo Control Circuit Diagram (7)
071	TA1	Power Amplifier Circuit Diagram (1)
072	TA2	Power Amplifier Circuit Diagram (2)
073	TA3	Power Amplifier Circuit Diagram (3)
074	TA4	Power Amplifier Circuit Diagram (4)
075	UA1	Indicator Circuit Diagram
076	VA1	Operator Panel Circuit Diagram
077		Logic Circuit 5129980 Mounting Diagram
078		Read Amplifier RFJAU Mounting Diagram
079		Servo Circuit SVIAU Mounting Diagram
080		Indicator Circuit HGAMU Mounting Diagram
081		Indicator Circuit HGAMU Mounting Diagram
082		Power Amplifier TVHMU Mounting Diagram
083		Driver Receiver DQPMU Mounting Diagram
084		Driver Receiver DUPMU Mounting Diagram

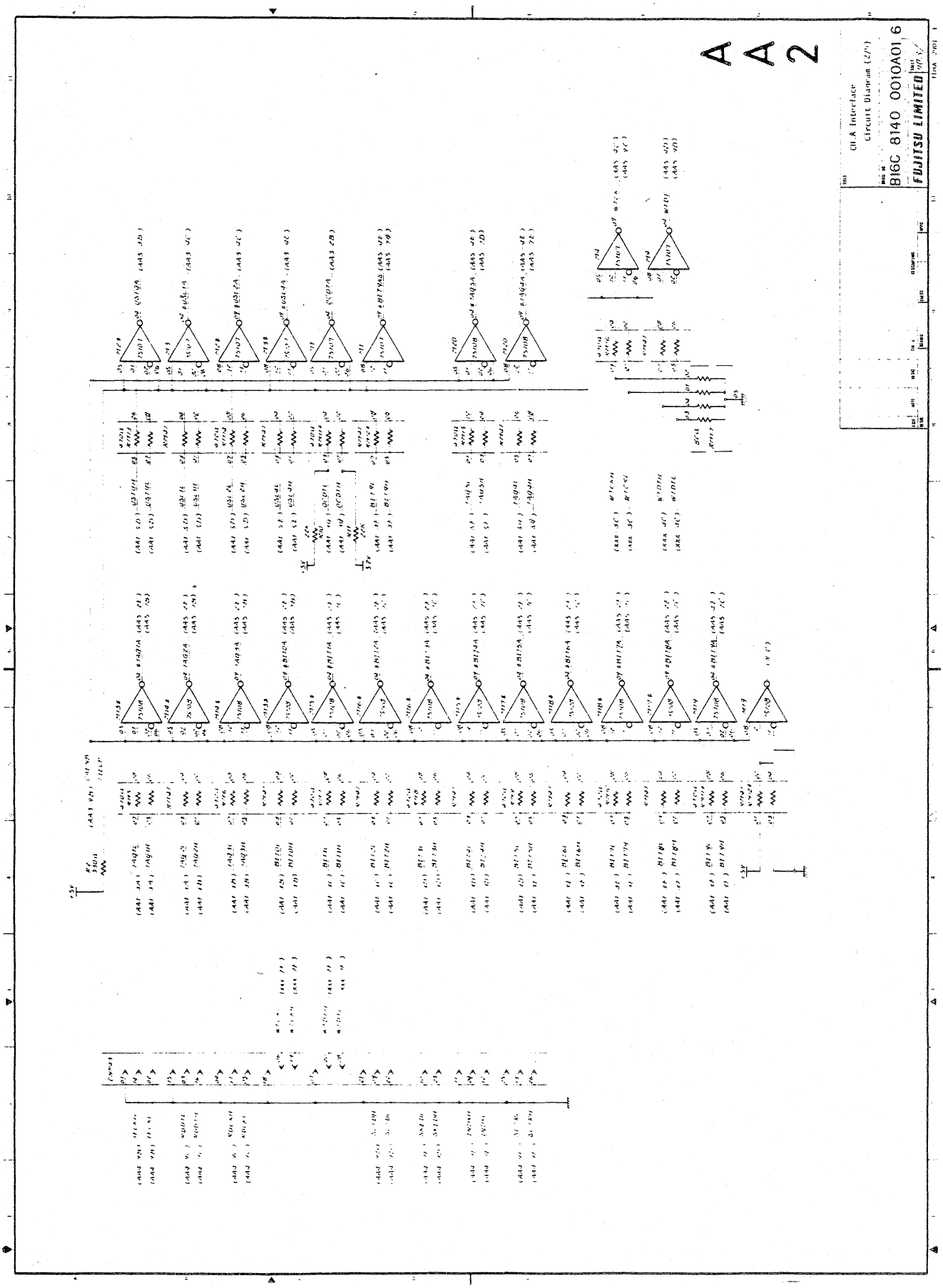
Schematics/Drawings List

FUJITSU LIMITED 001/



A
A
1

TITLE	CH A Interface Circuit Diagram (1/5)
B16C-8140 0010A01 6	
FUJITSU LIMITED	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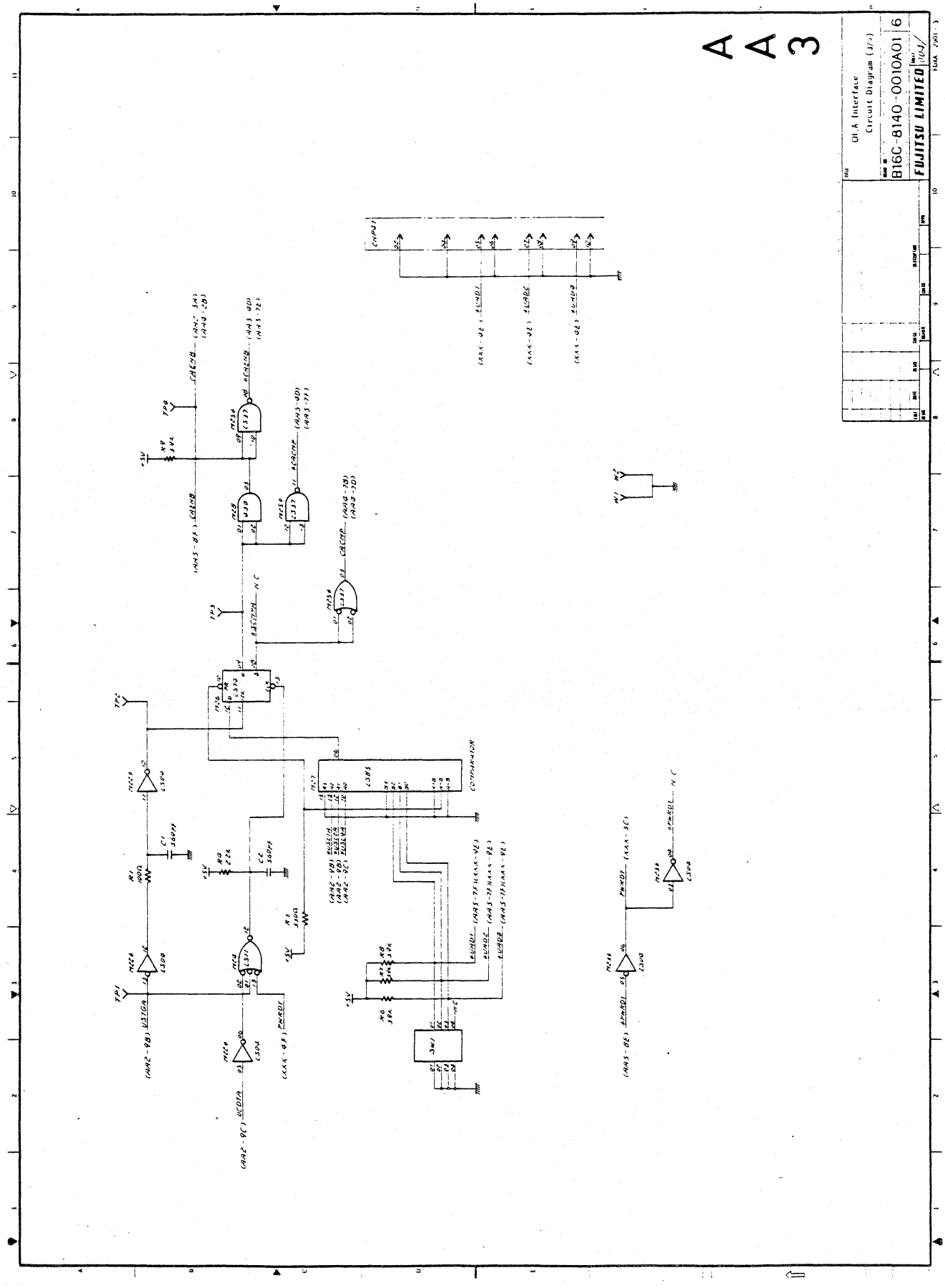
A
2
GIA Interface
Circuit Diagram (2/4)
B16C 8140 0010A01.6
FUJITSU LIMITED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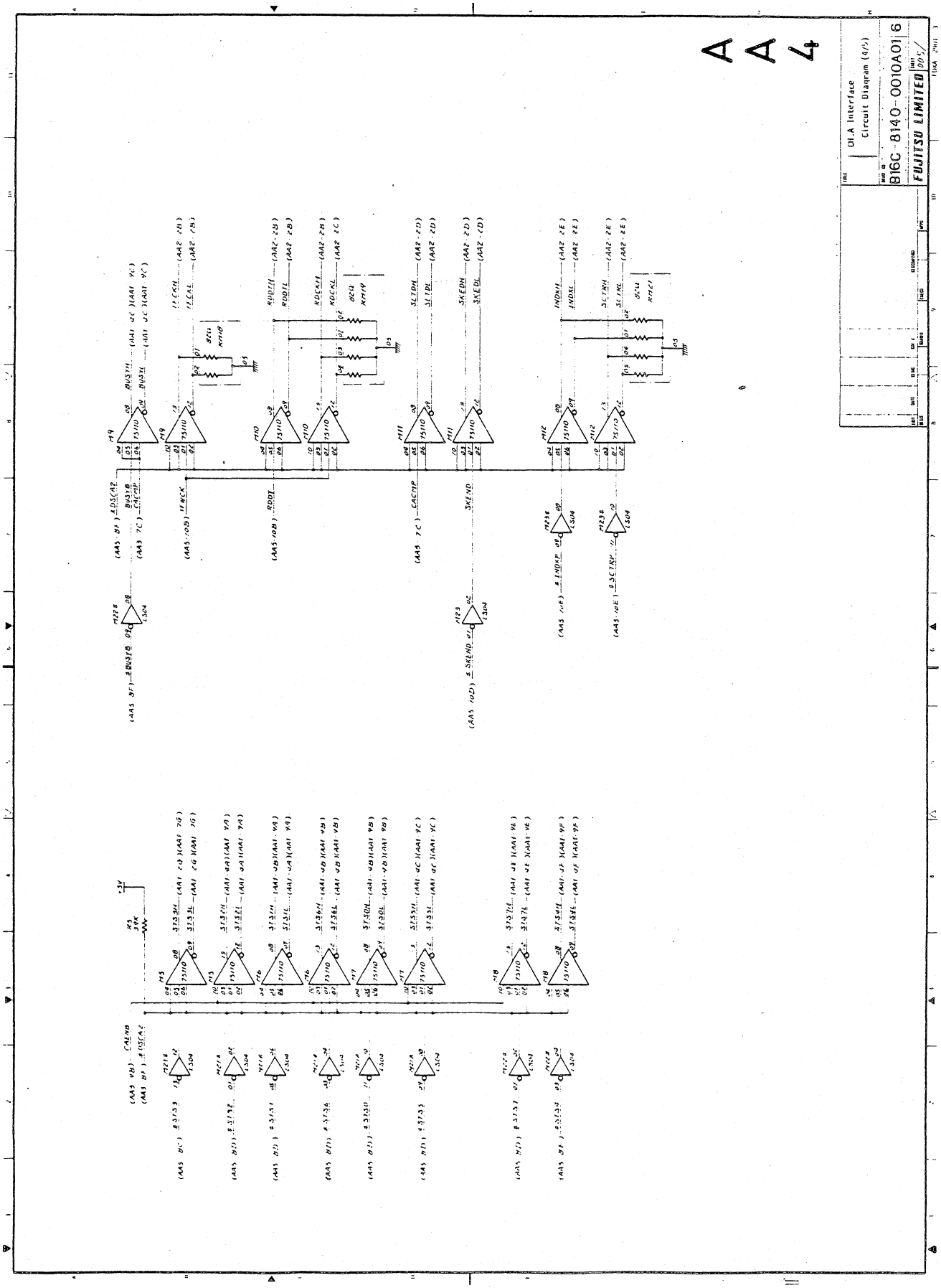
CH.A Interface
Circuit Diagram (1/2)
B16C-8140-0010A01
6
FUJITSU LIMITED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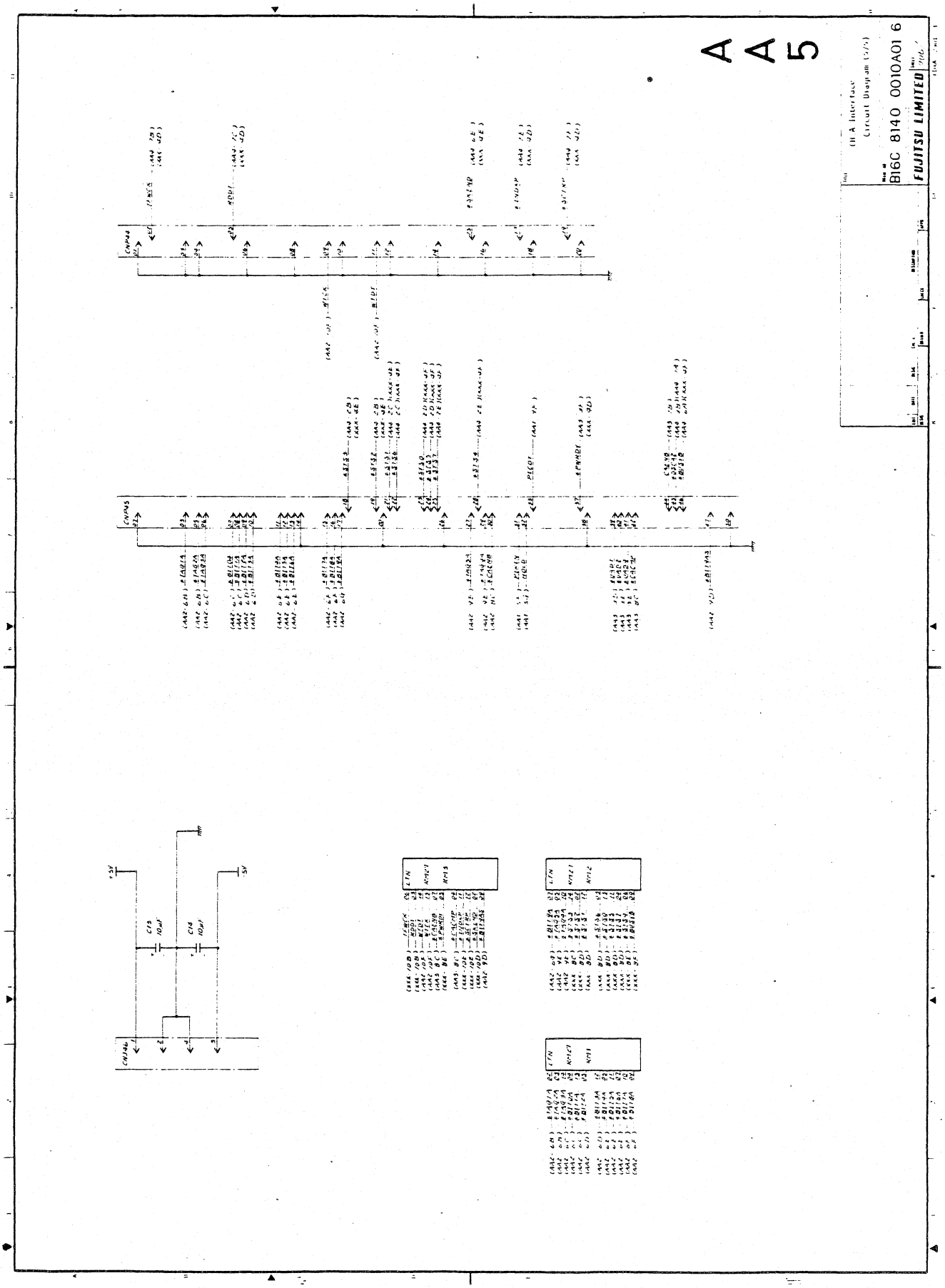
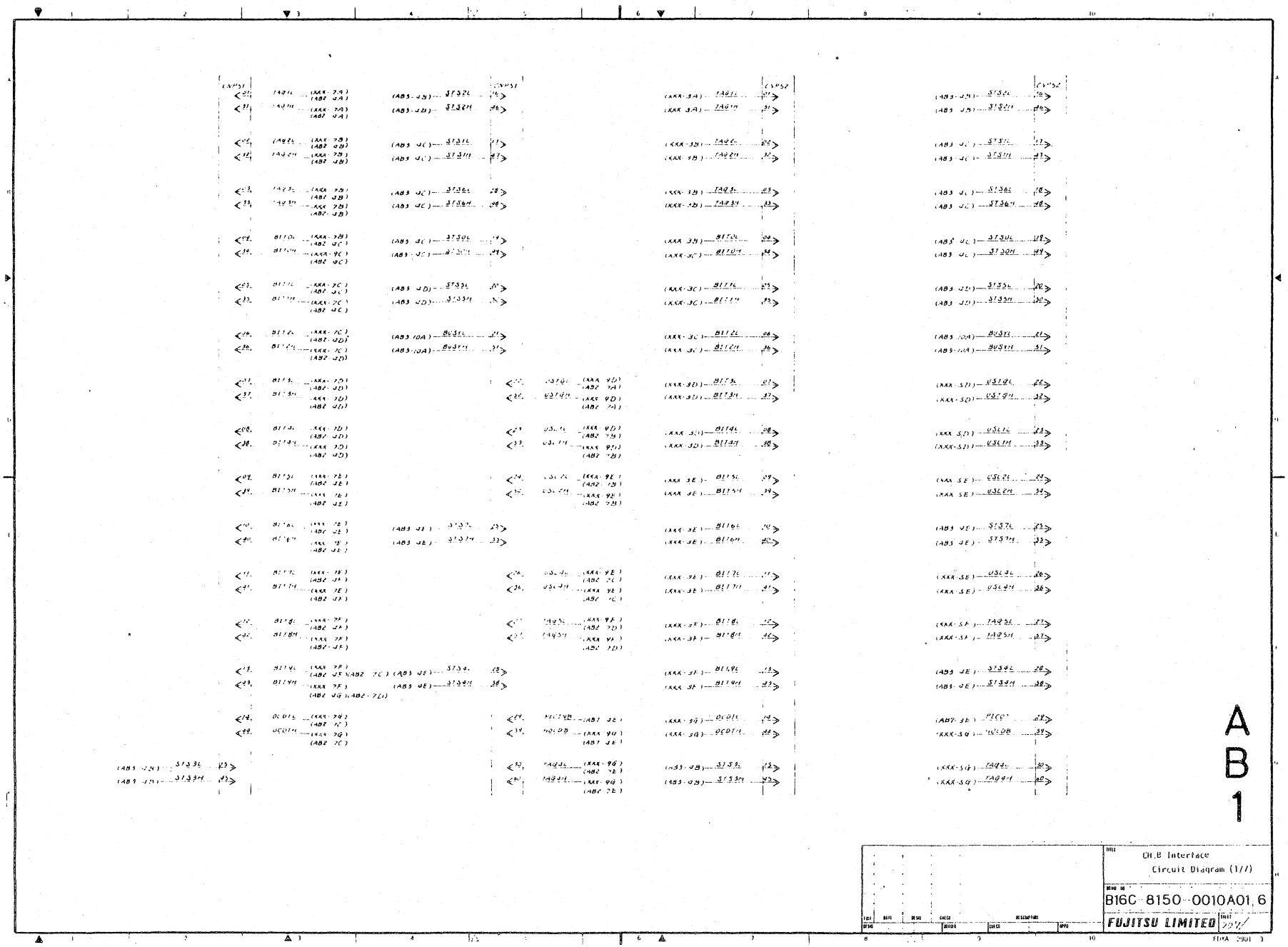
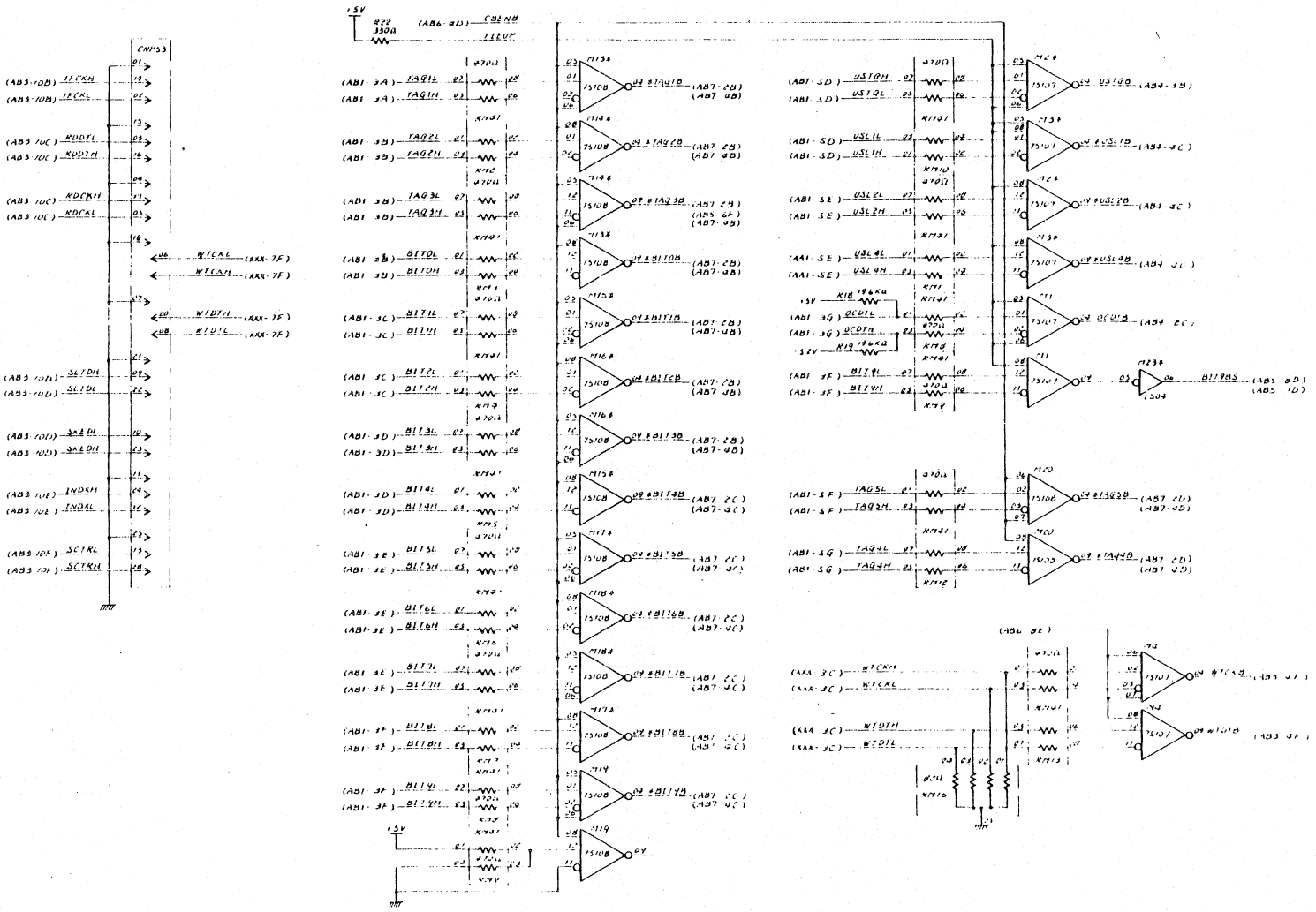
4
FUJITSU LIMITED
B16C-8140-0010A01
CI.A Interface
Circuit Diagram (4/5)


A
A
5
FUJITSU LIMITED
B16C 8140 0010A01 6
Circuit Diagram
I/F A Interface



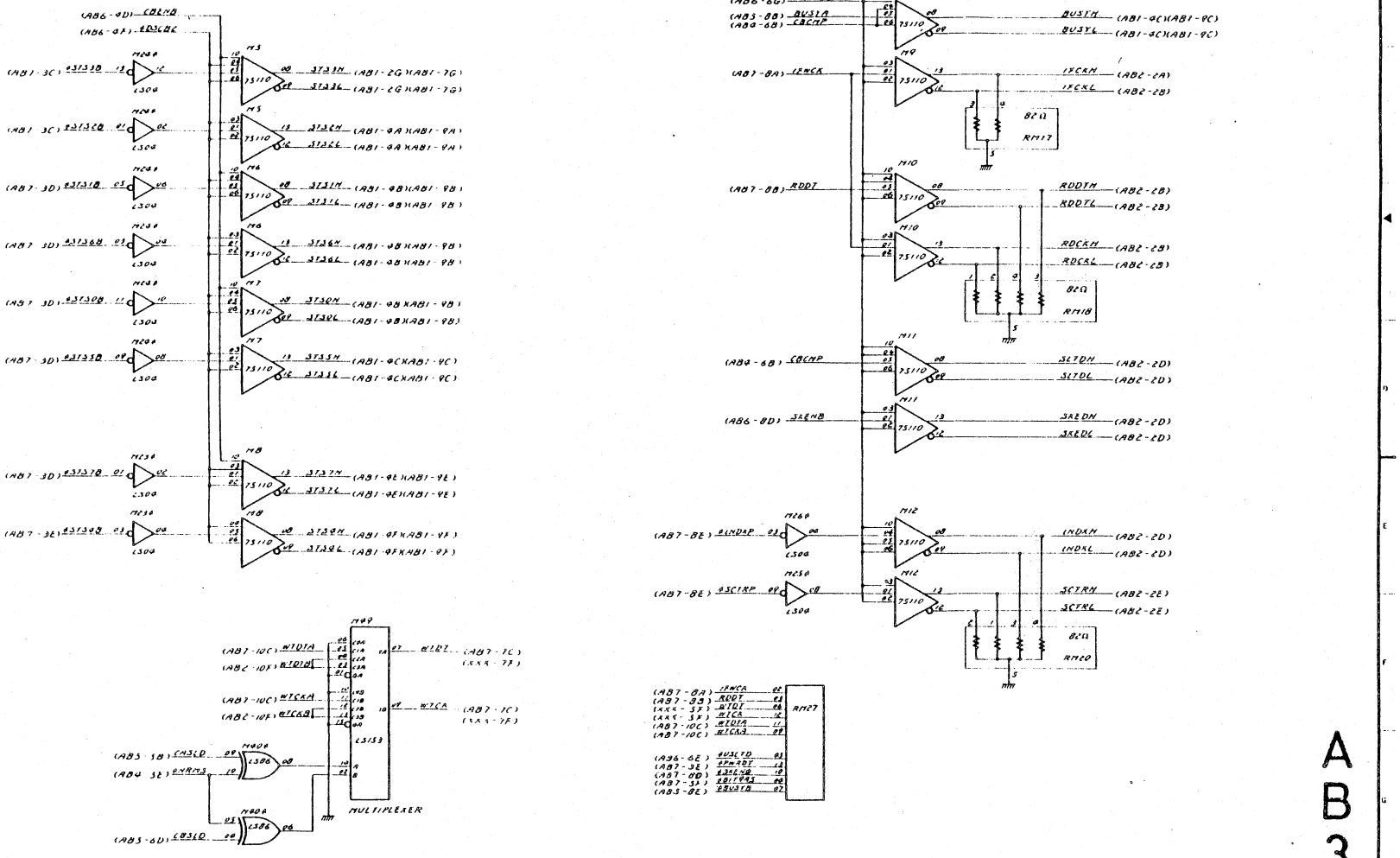
TITLE	CH.B Interface Circuit Diagram (1/7)
DRAWING NO	B16C-8150-0010A01,6
	FUJITSU LIMITED

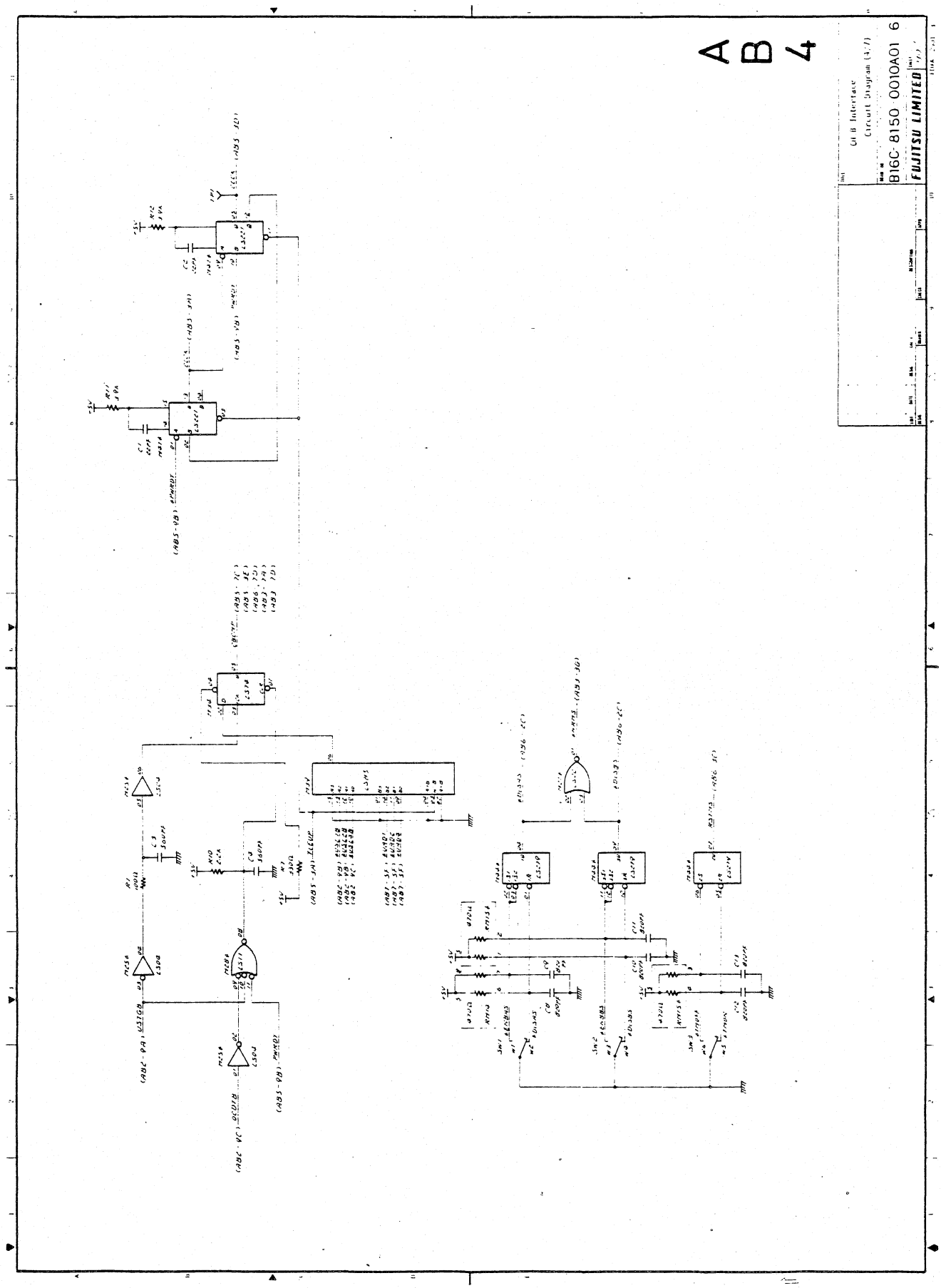
A
B
1

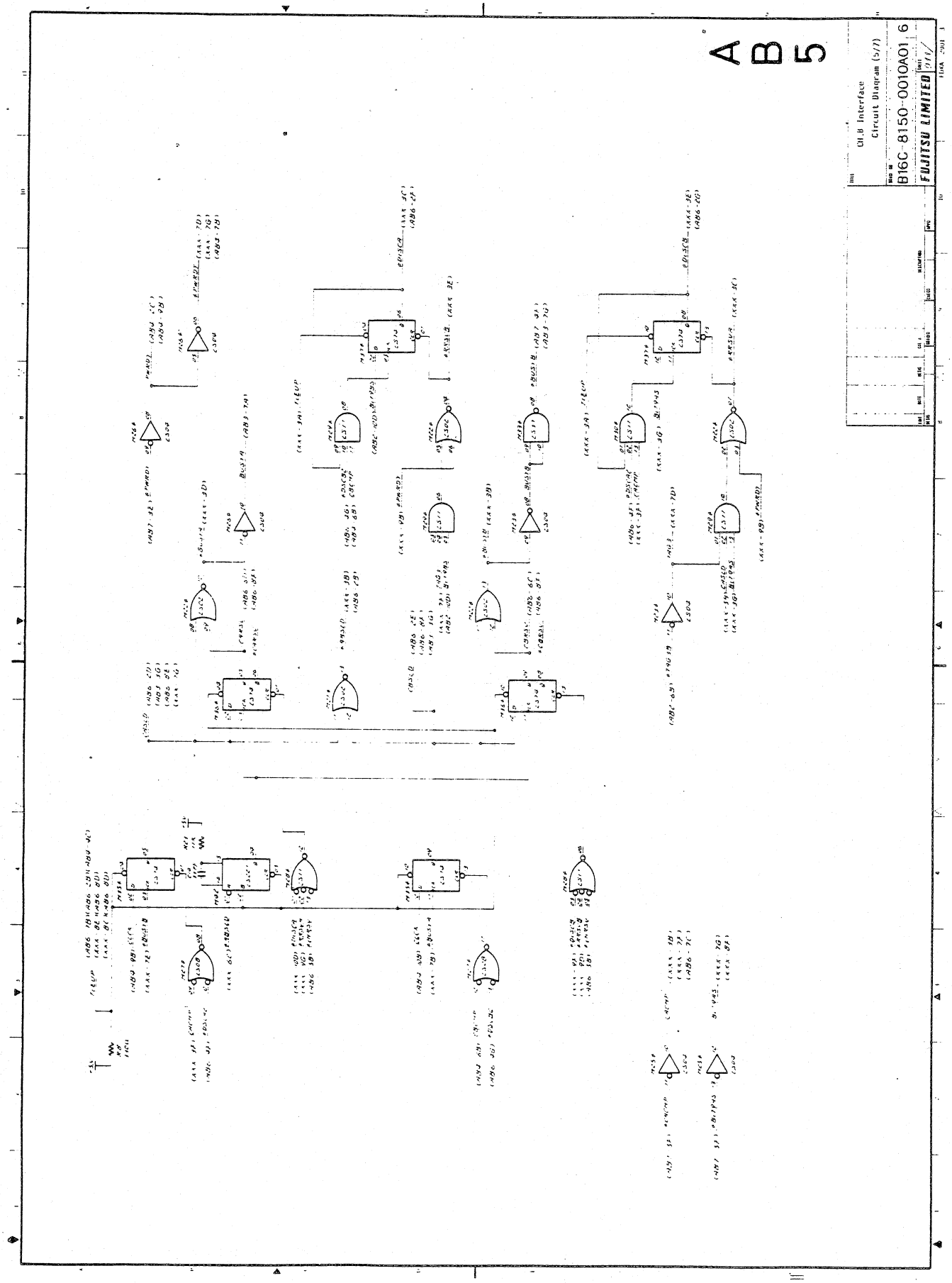


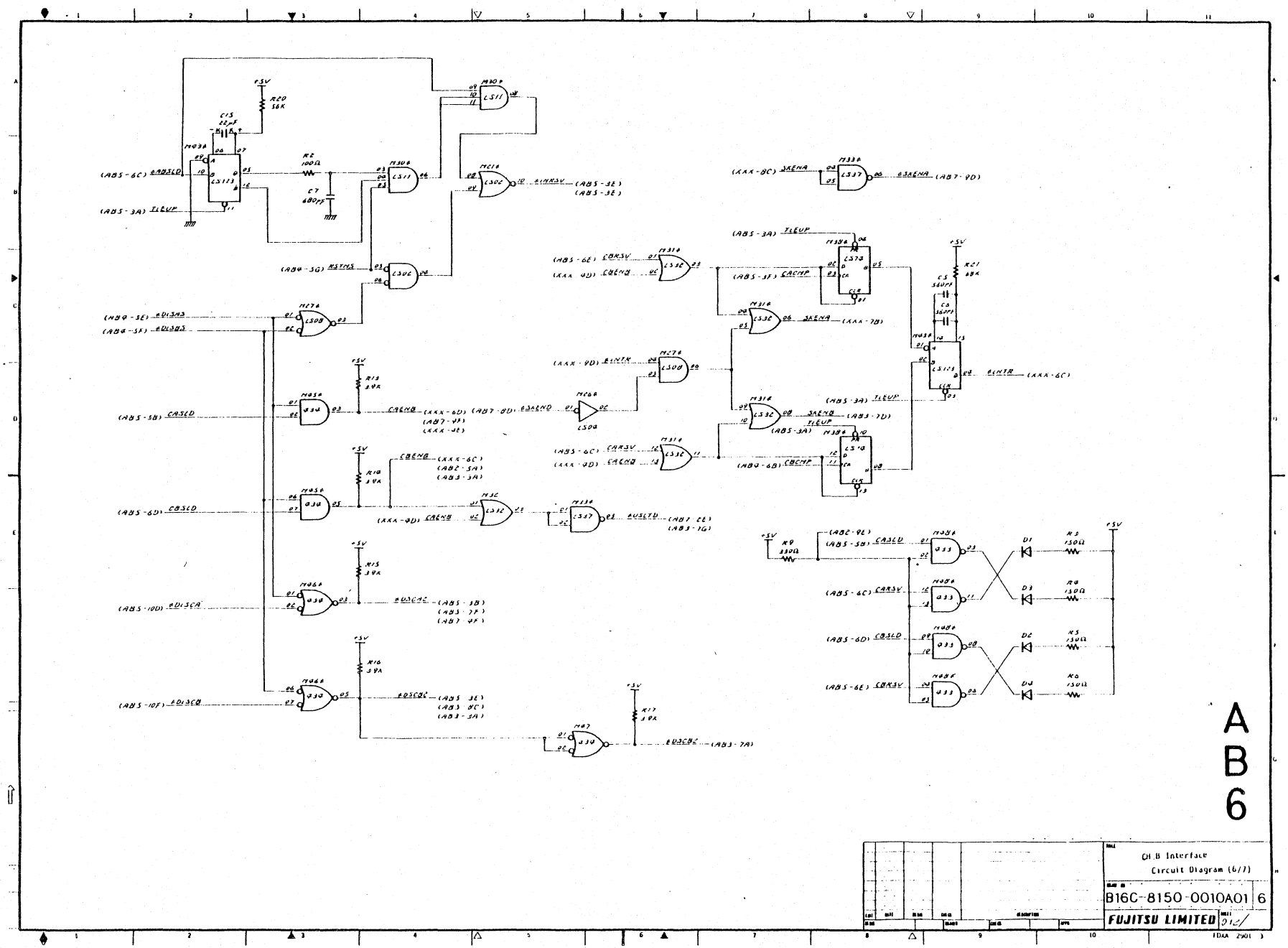
A
B
2

	OI B Interface
	Circuit Diagram (2/7)
	B16C 8150-0010A01 6
	FUJITSU LIMITED


MULTIPLEXER
RM17
RM18
RM19
RM20
FUJITSU LIMITED
CH_B Interface
Circuit Diagram (3/7)
B16C-8150-0010A01
6
FDXA-2901-3

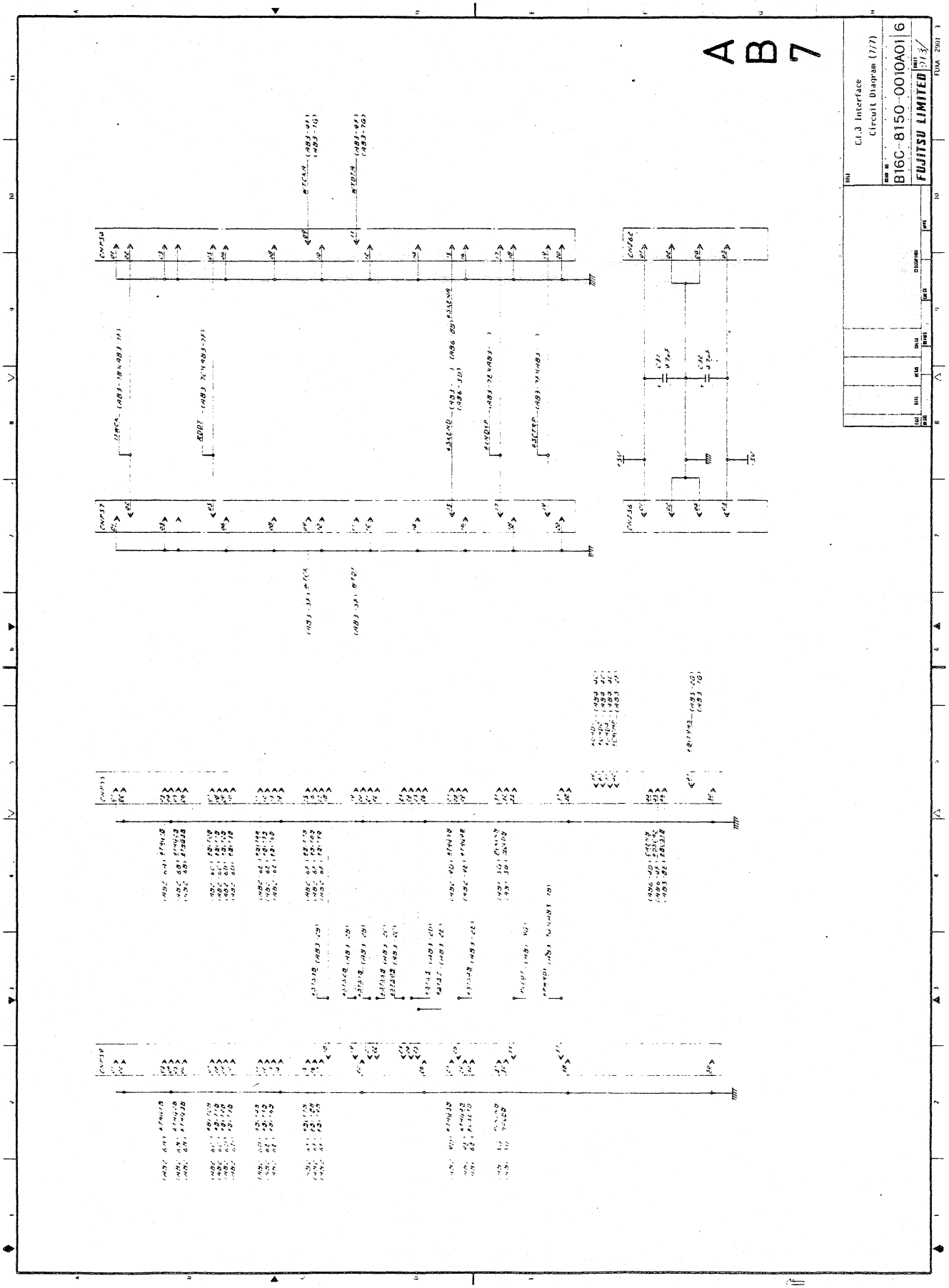

A
B
4
FUJITSU LIMITED
B16C-8150-0010A01 6
GP-IB Interface
Circuit Diagram (4/7)

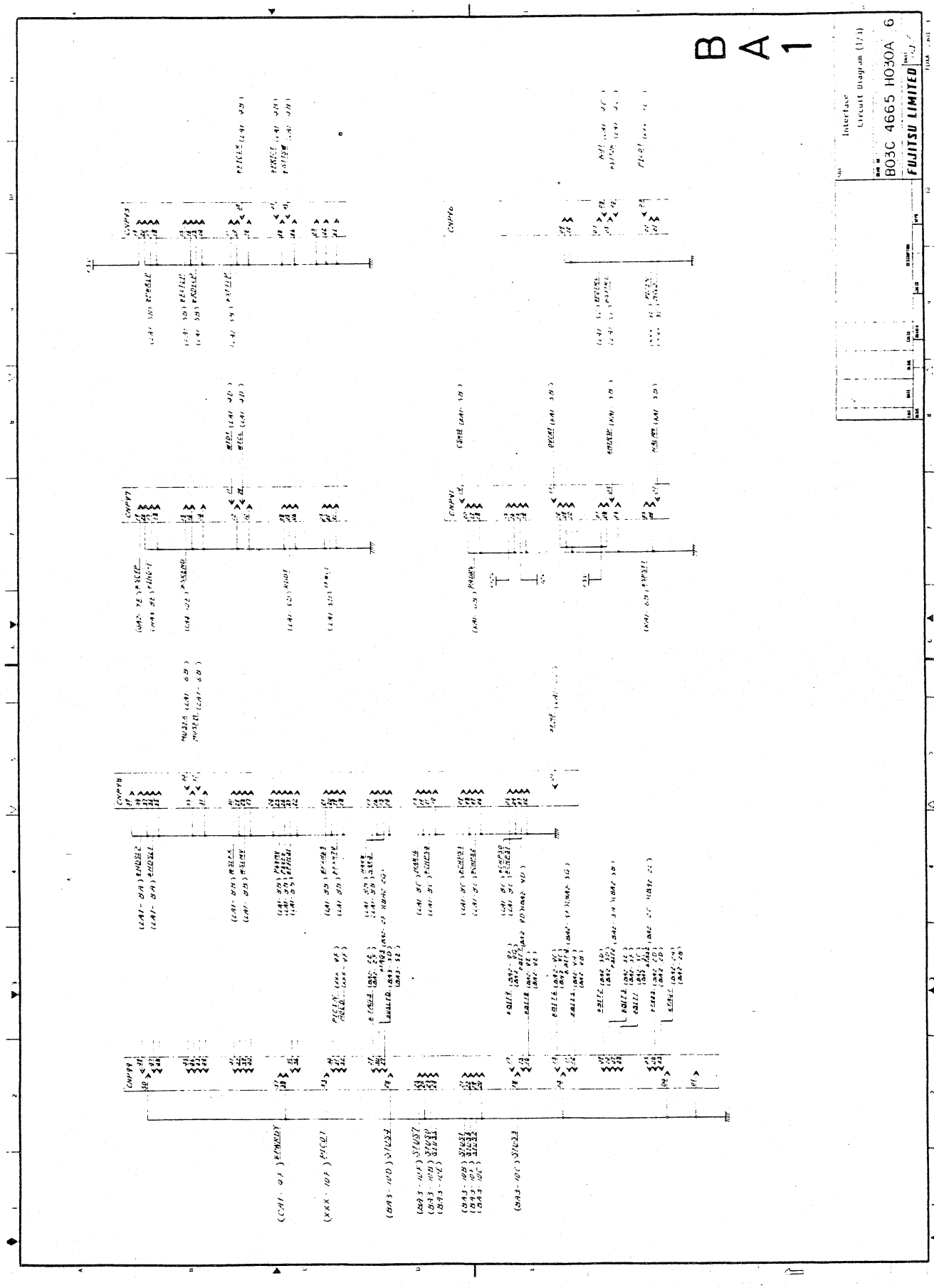

A
B
5
FUJITSU LIMITED
B16C-8150-0010A01-6
Circuit Diagram (5/7)
I/F B Interface

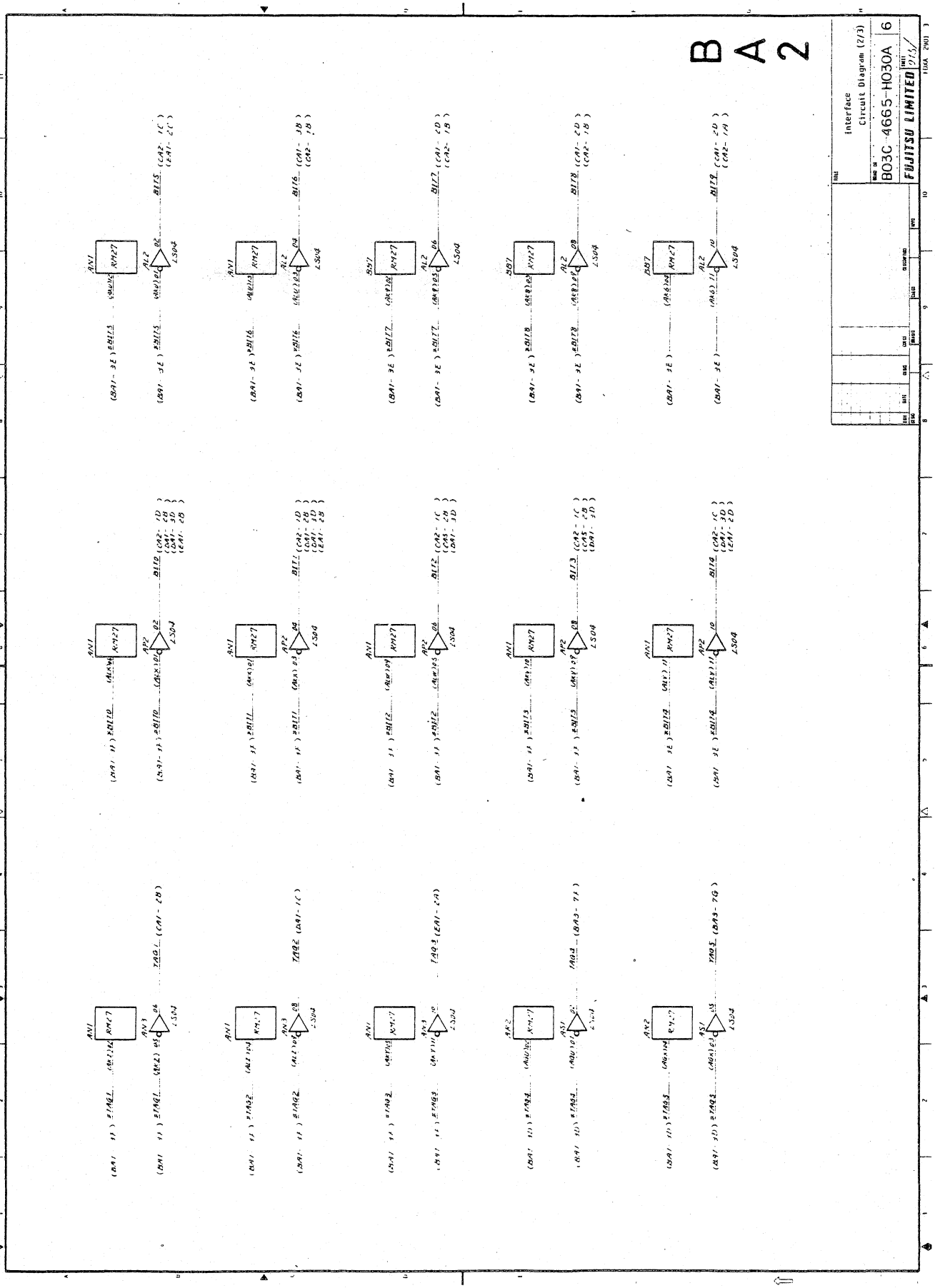


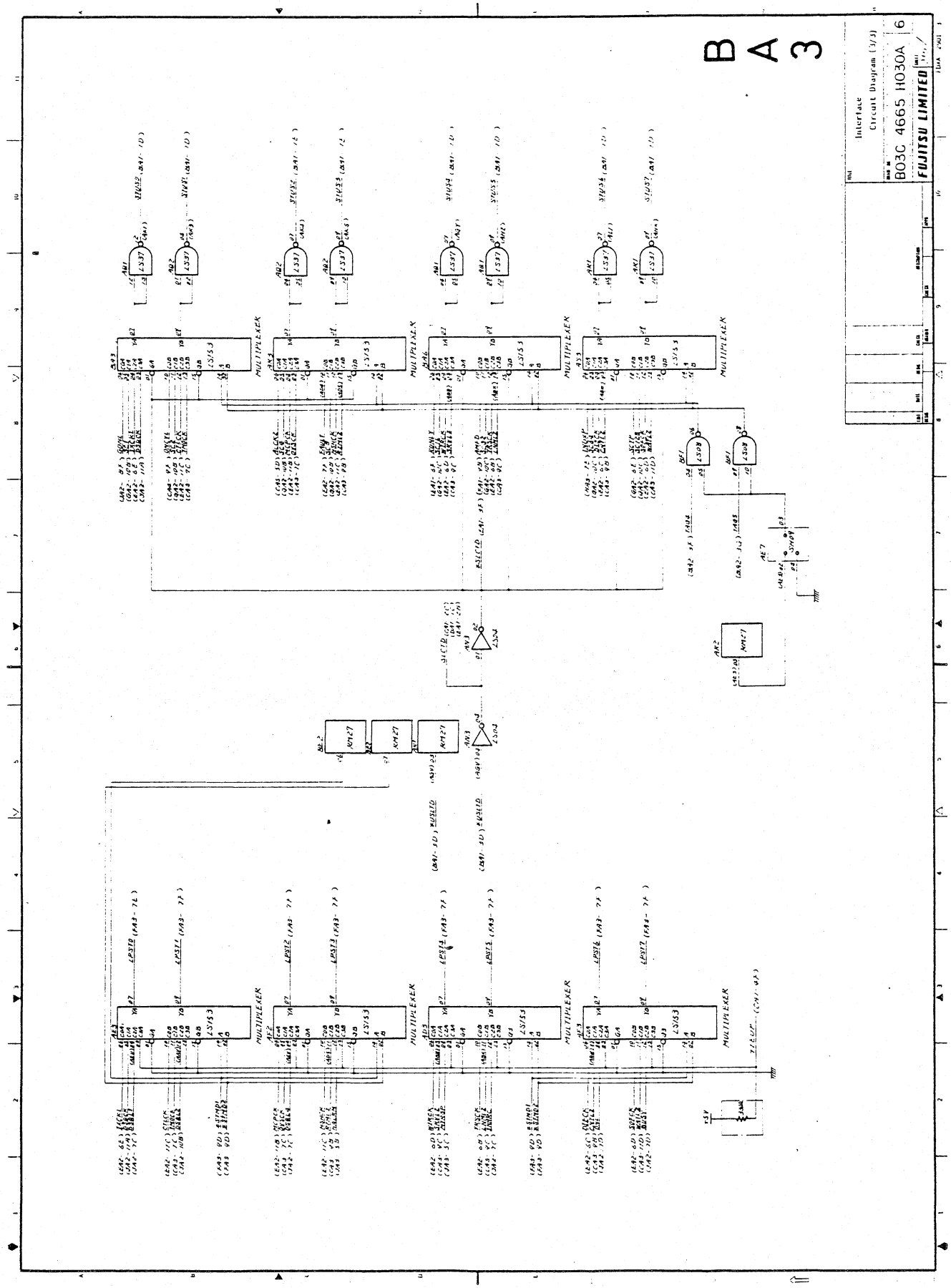
A
B
6

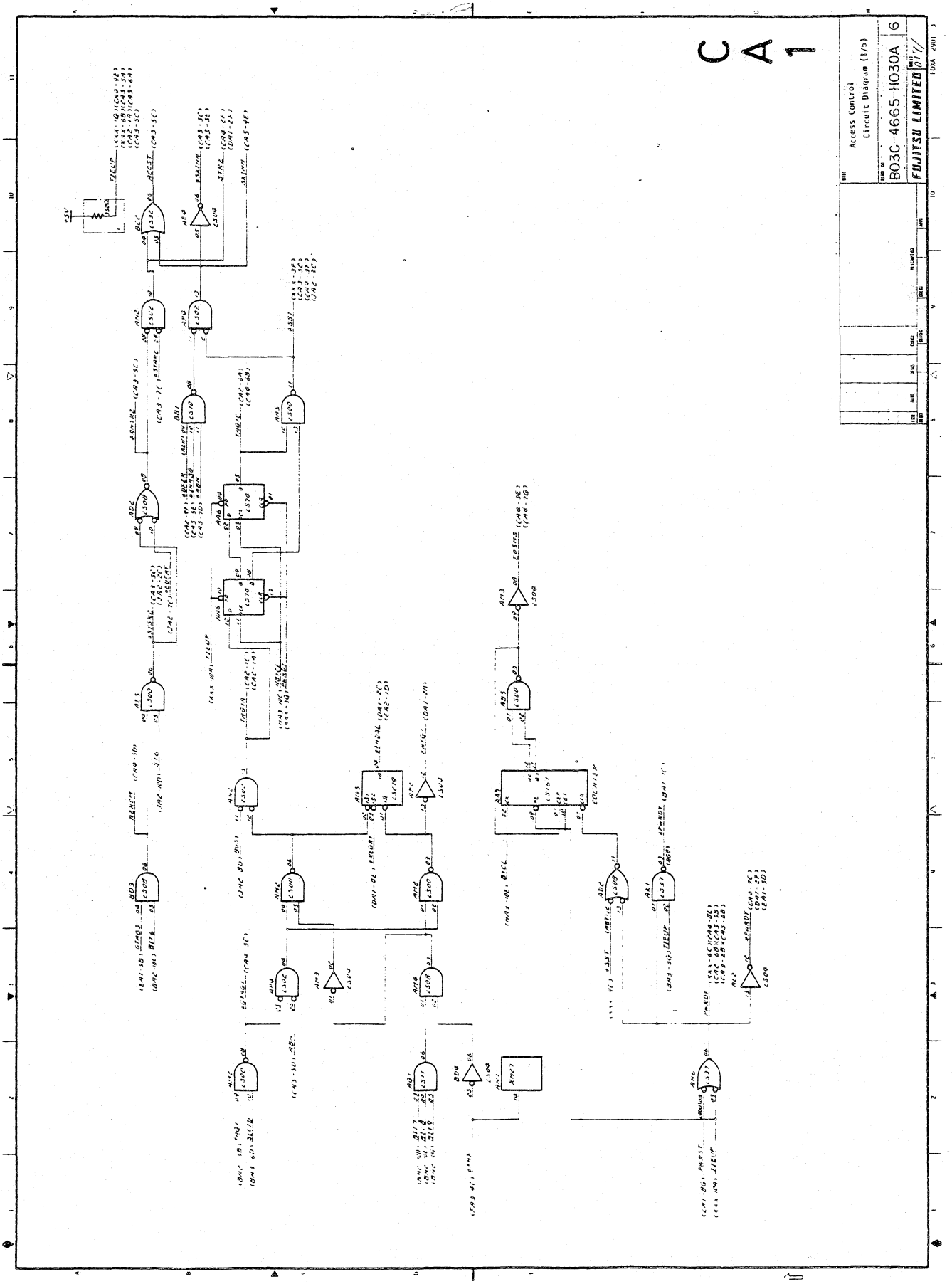
	CH.B Interface
	Circuit Diagram (6/7)
	B16C-8150-0010A01 | 6
	FUJITSU LIMITED

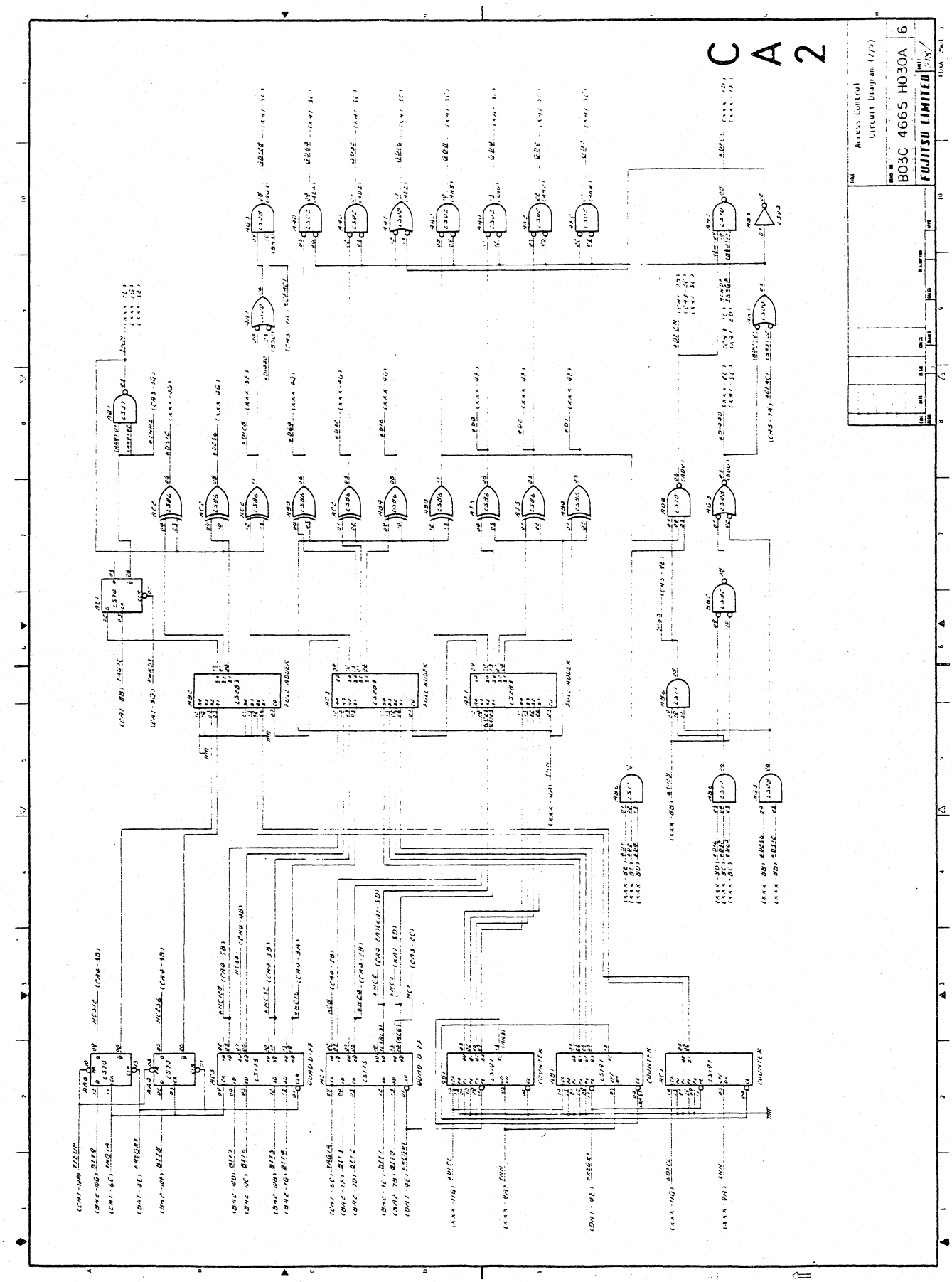

A
B
7
C.I.3 Interface
Circuit Diagram (7/7)
B16C-8150-0010A01
6
FUJITSU LIMITED

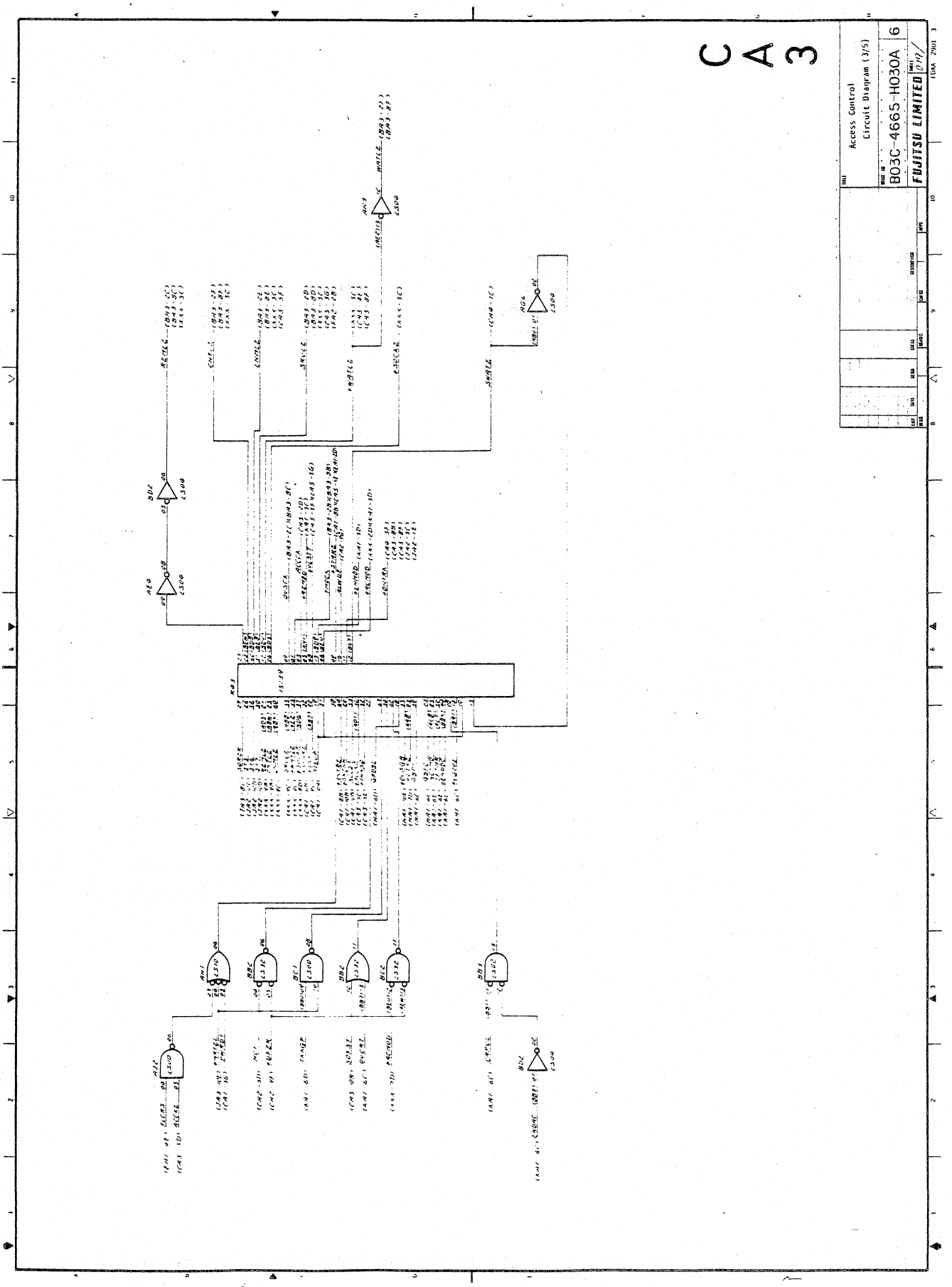

B
A
1
Interface
Circuit Diagram (1/1)
B03C 4665 H030A 6
FUJITSU LIMITED

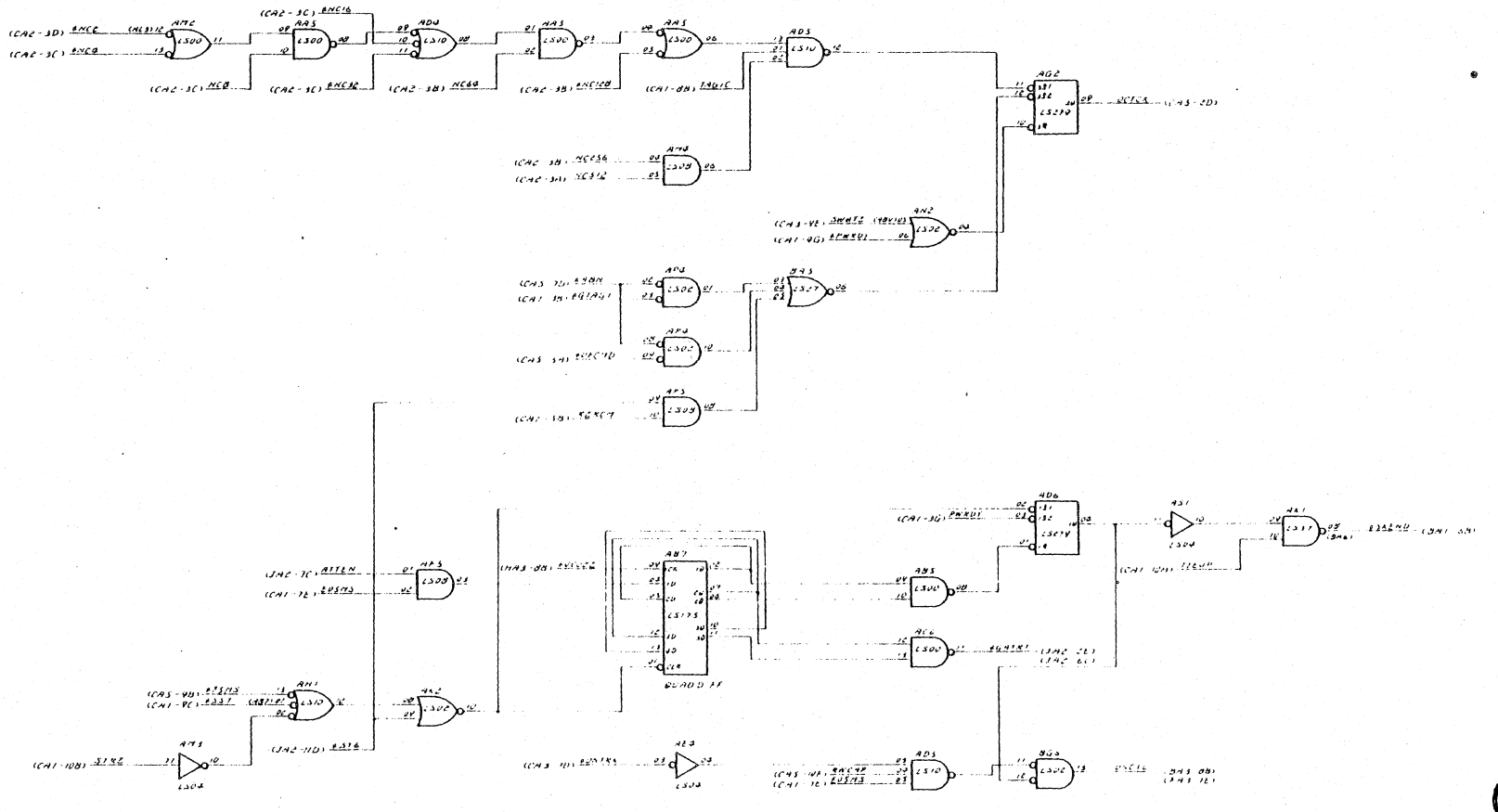

Interface
Circuit Diagram (2/3)
B03C-4665-H030A
6
FUJITSU LIMITED


B
A
3
Interface
Circuit Diagram (3/3)
B03C 4665 H030A
6
FUJITSU LIMITED


C A 1
Access Control
Circuit Diagram (1/3)
B03C-4665-H030A
6
FUJITSU LIMITED


Access Control
Circuit Diagram (2/3)
B03C 4665-H030A 6
FUJITSU LIMITED


C A 3
Access Control
Circuit Diagram (3/5)
B03C-4665-H030A
6
FUJITSU LIMITED

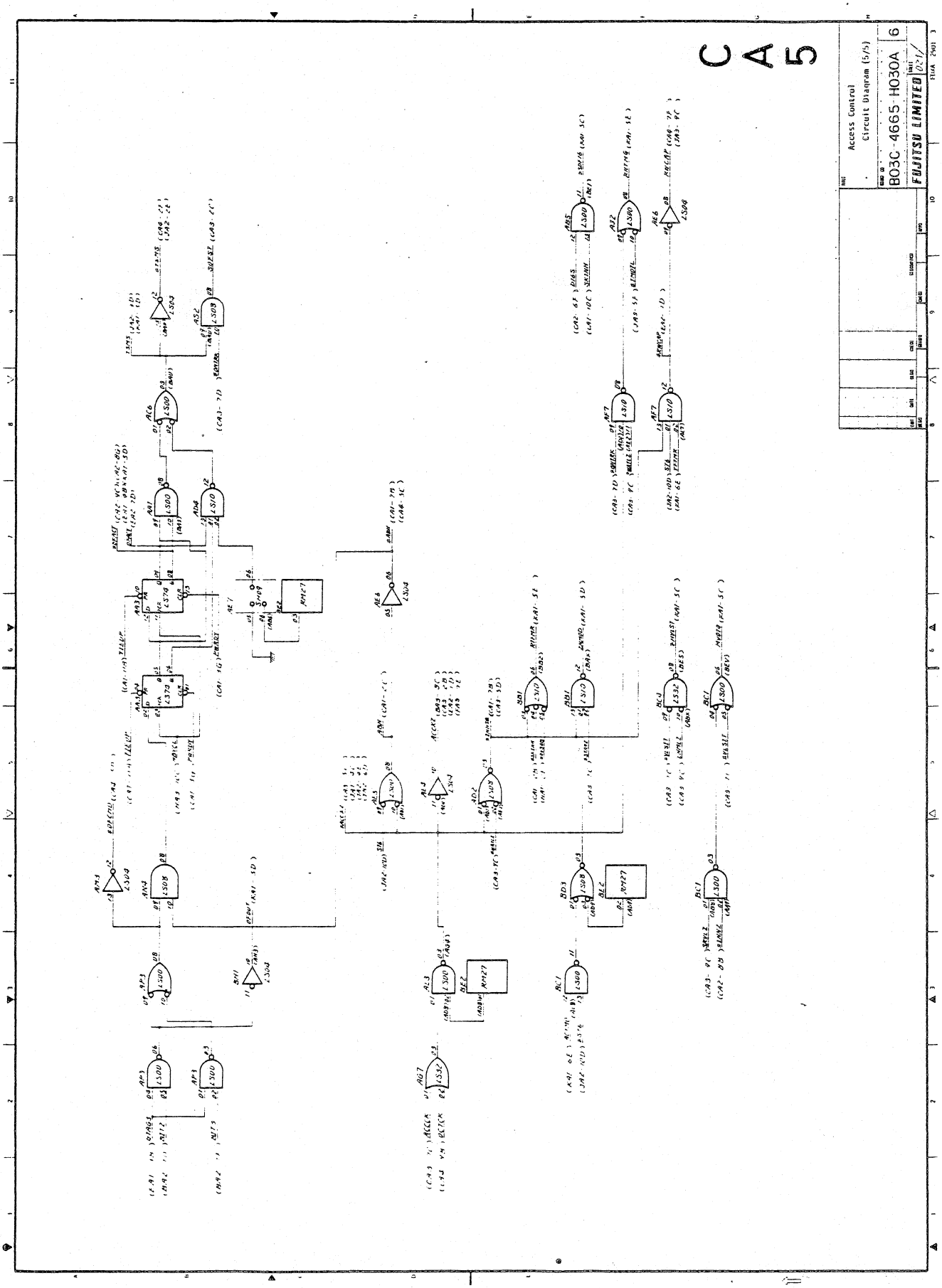


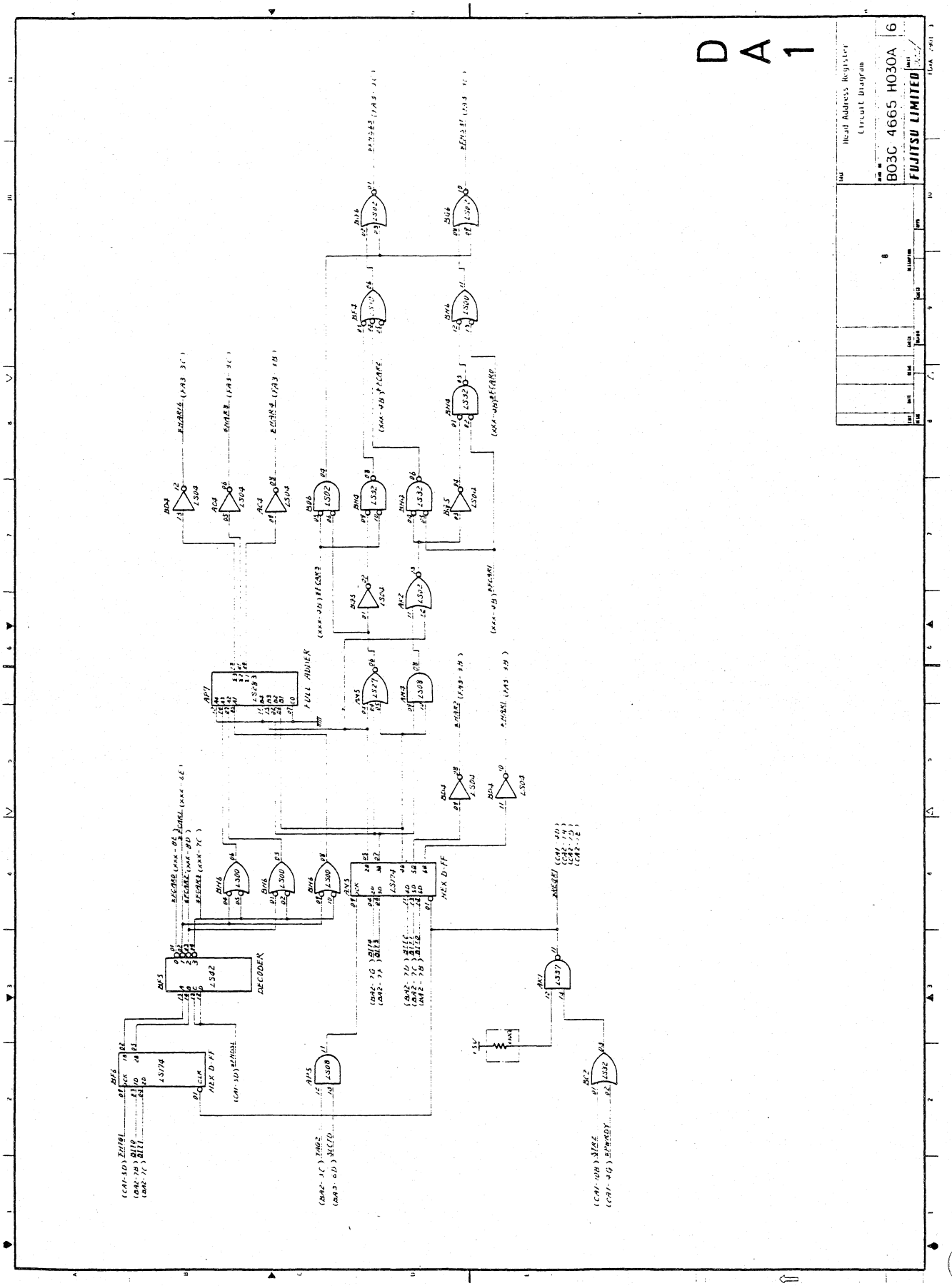
C
A
4

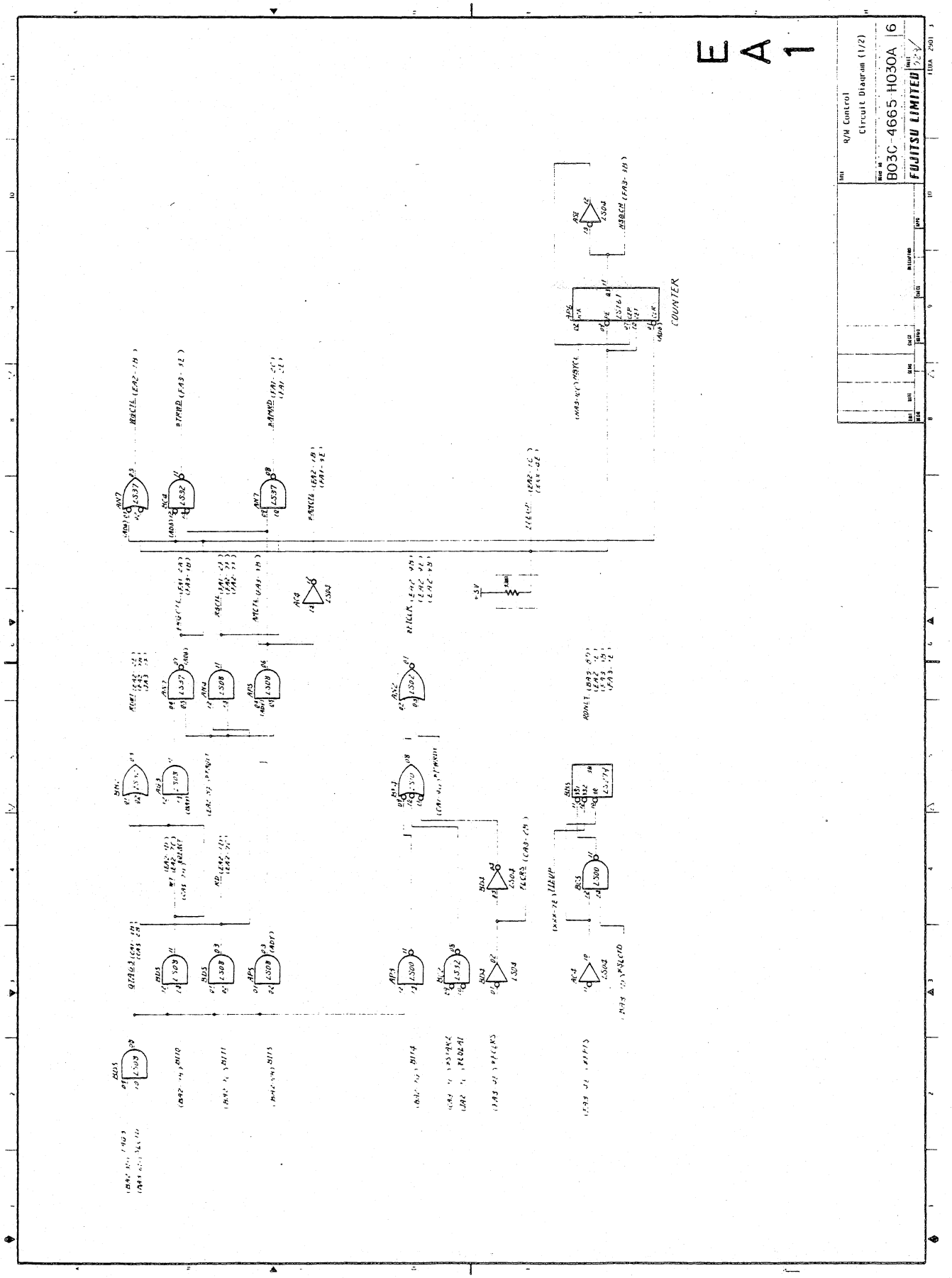
Access Control
Circuit Diagram (4/5)

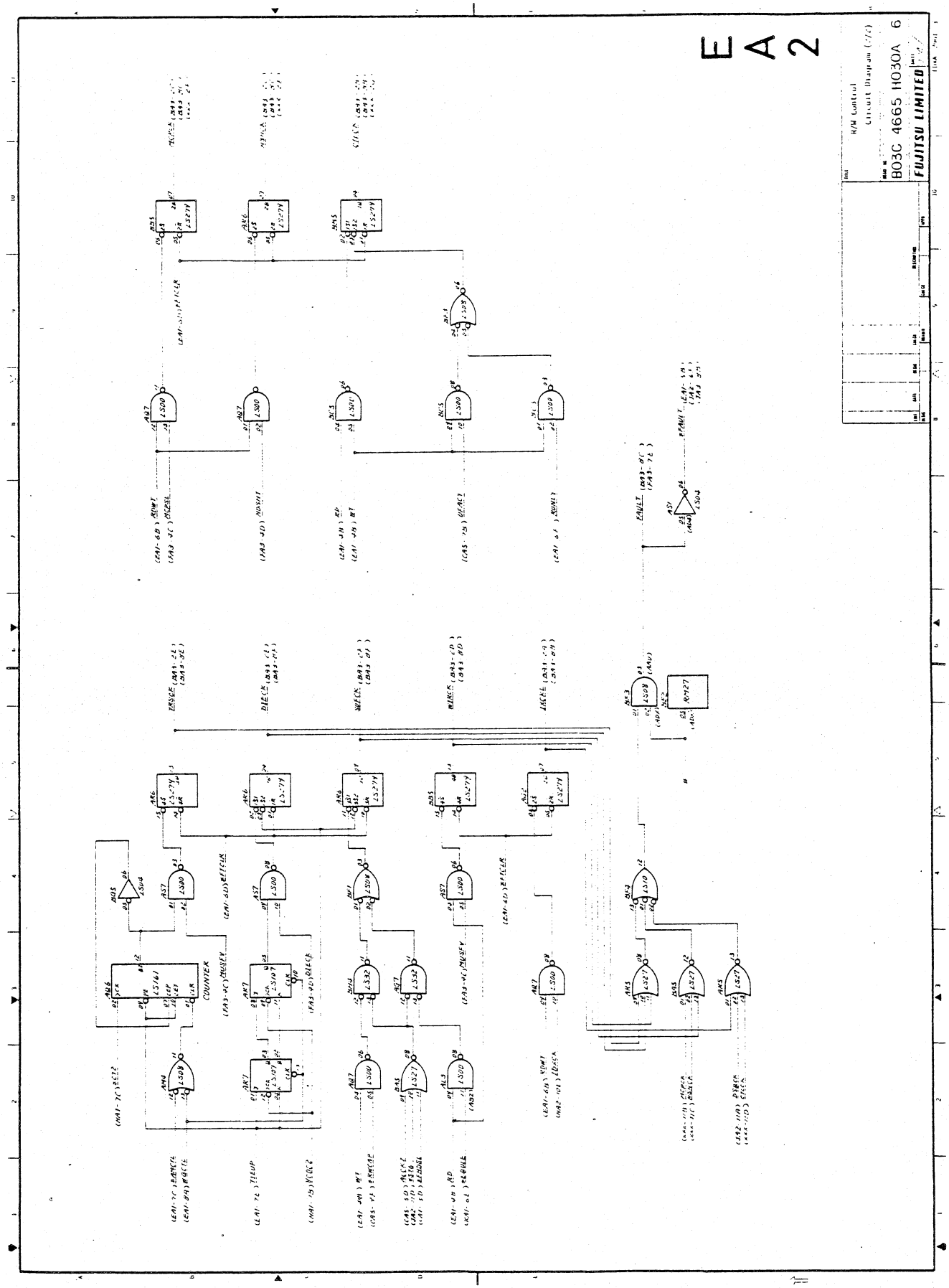
B03C 4665 H030A 6

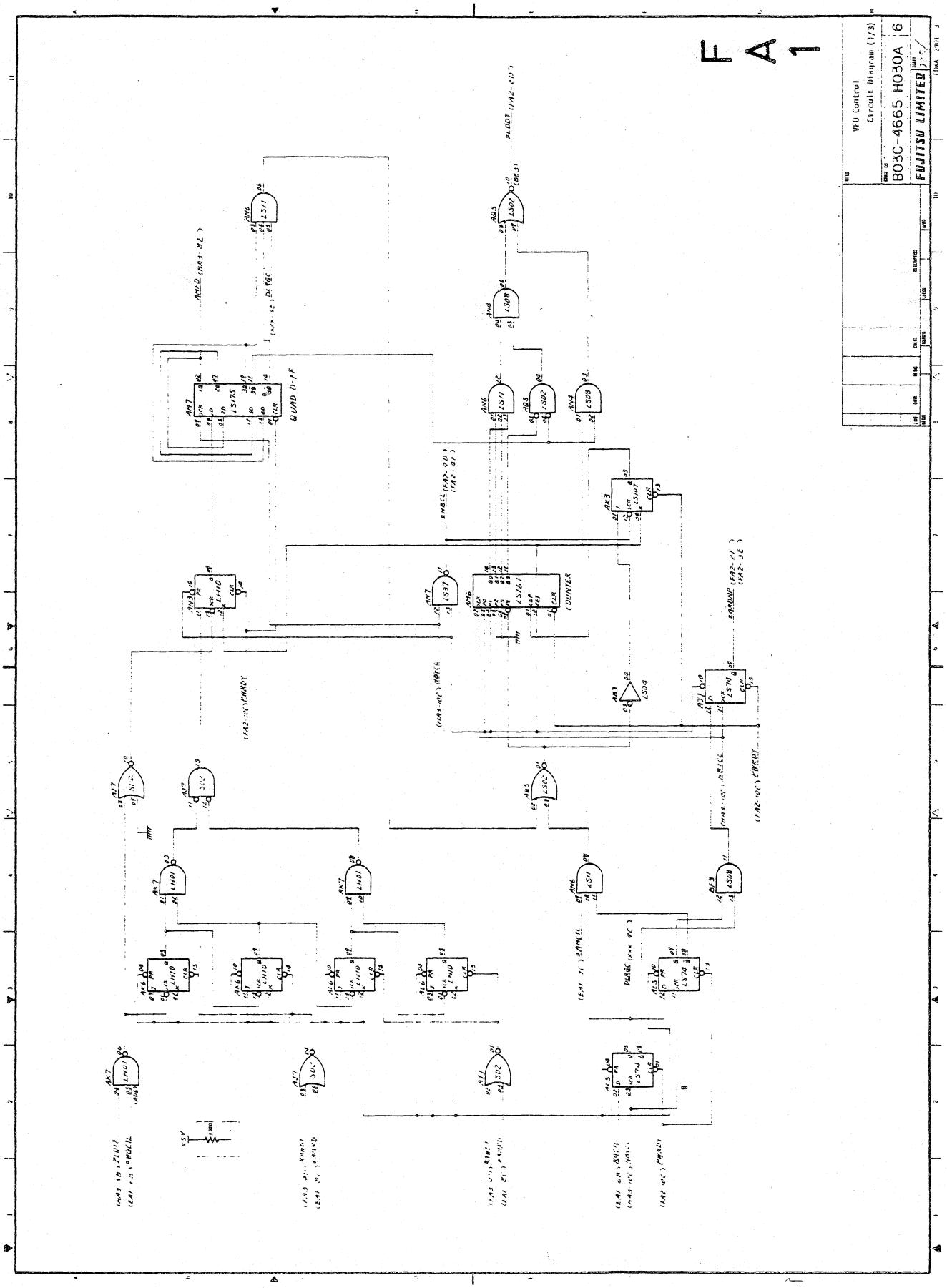
FUJITSU LIMITED

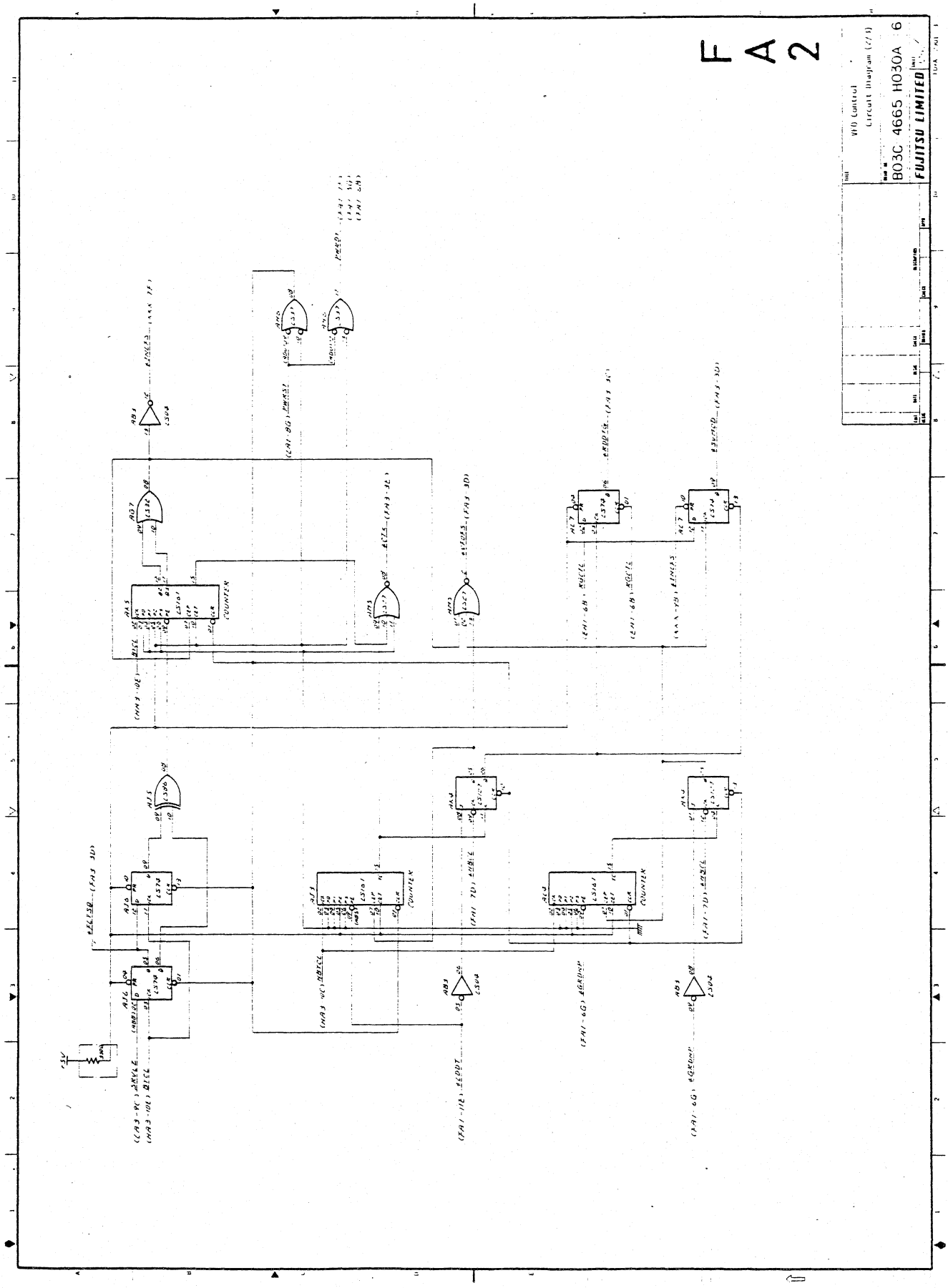

CA5
Access Control
Circuit Diagram (5/5)
B03C-4665-H030A
6
FUJITSU LIMITED

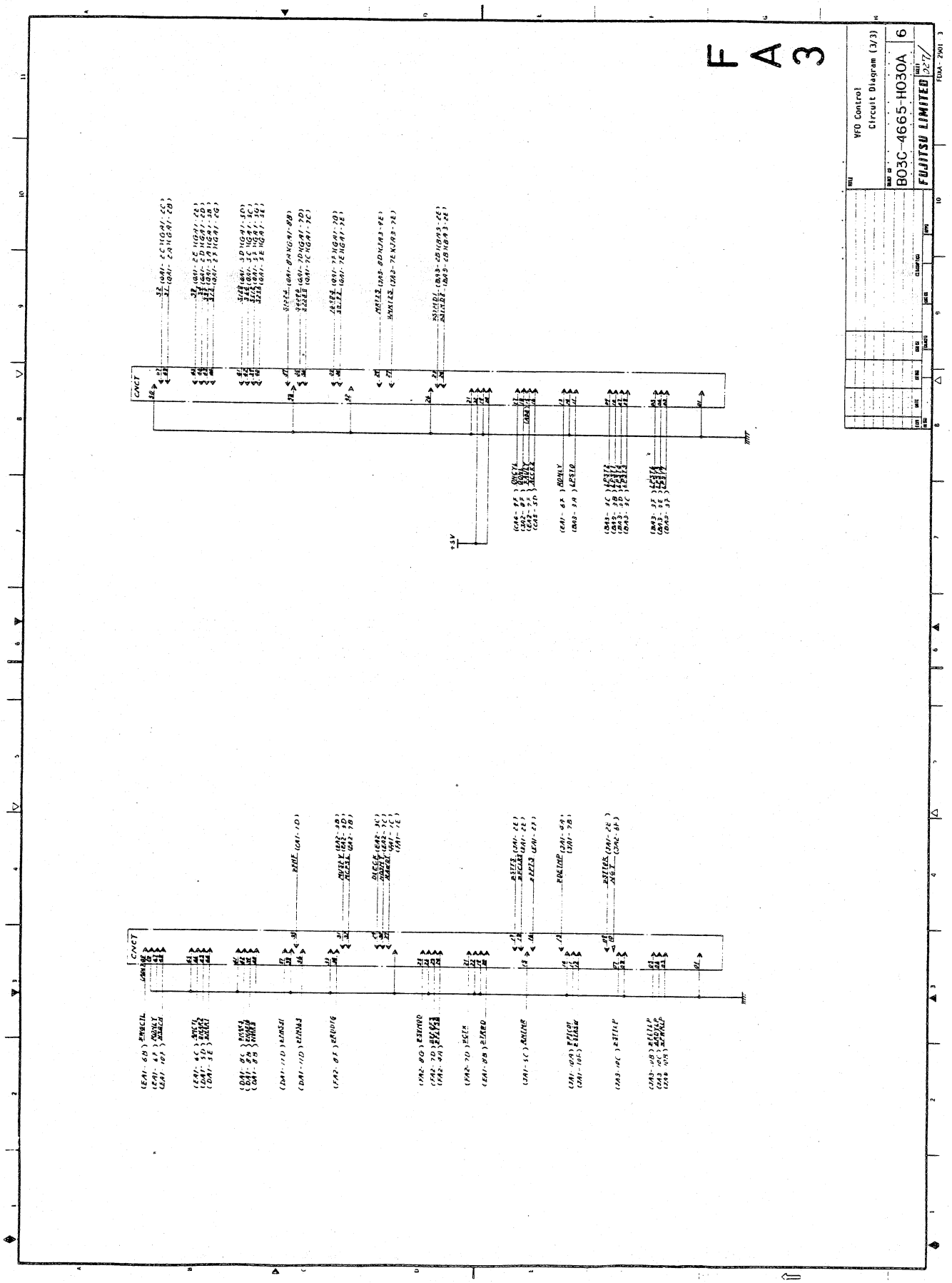

D
A
1
Head Address Register
Circuit Diagram
B03C 4665 H030A
6
FUJITSU LIMITED
DECODER
HEX D-FF
FULL ADDER

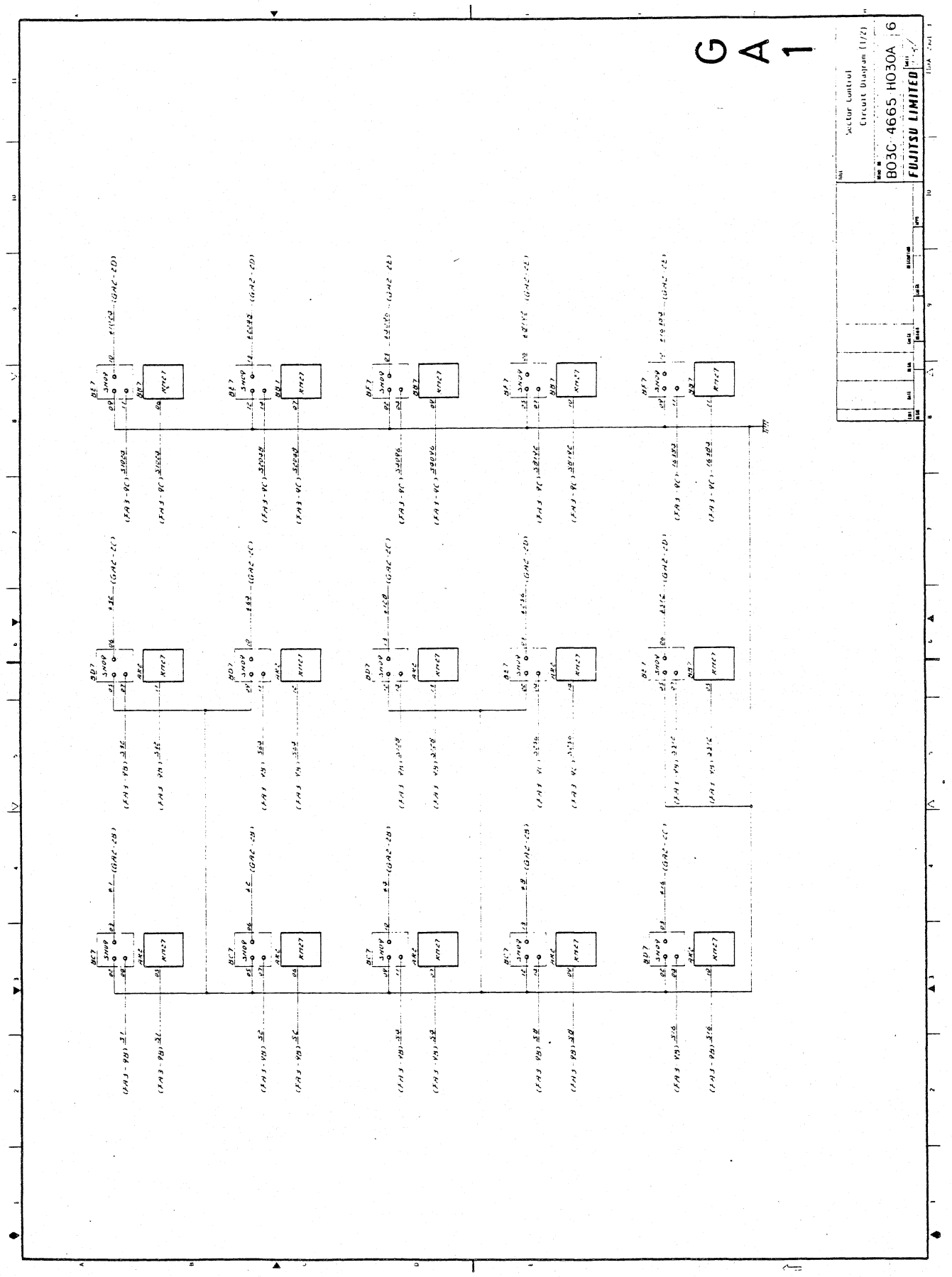

E A 1
R/W Control
Circuit Diagram (1/2)
B03C-4665-H030A
6
FUJITSU LIMITED
COUNTER

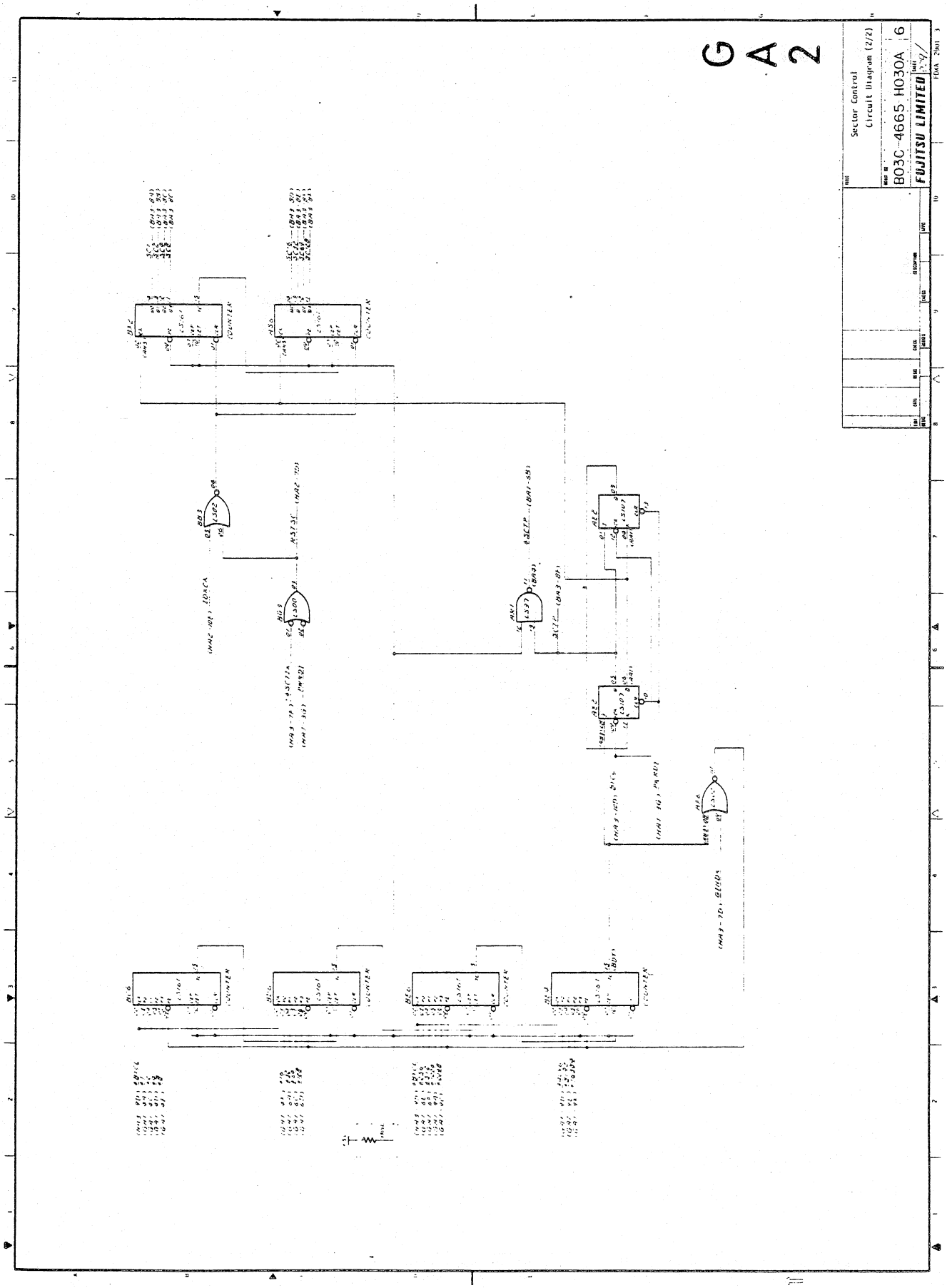

E A 2
B03C 4665 H030A 6
FUJITSU LIMITED
COUNTER

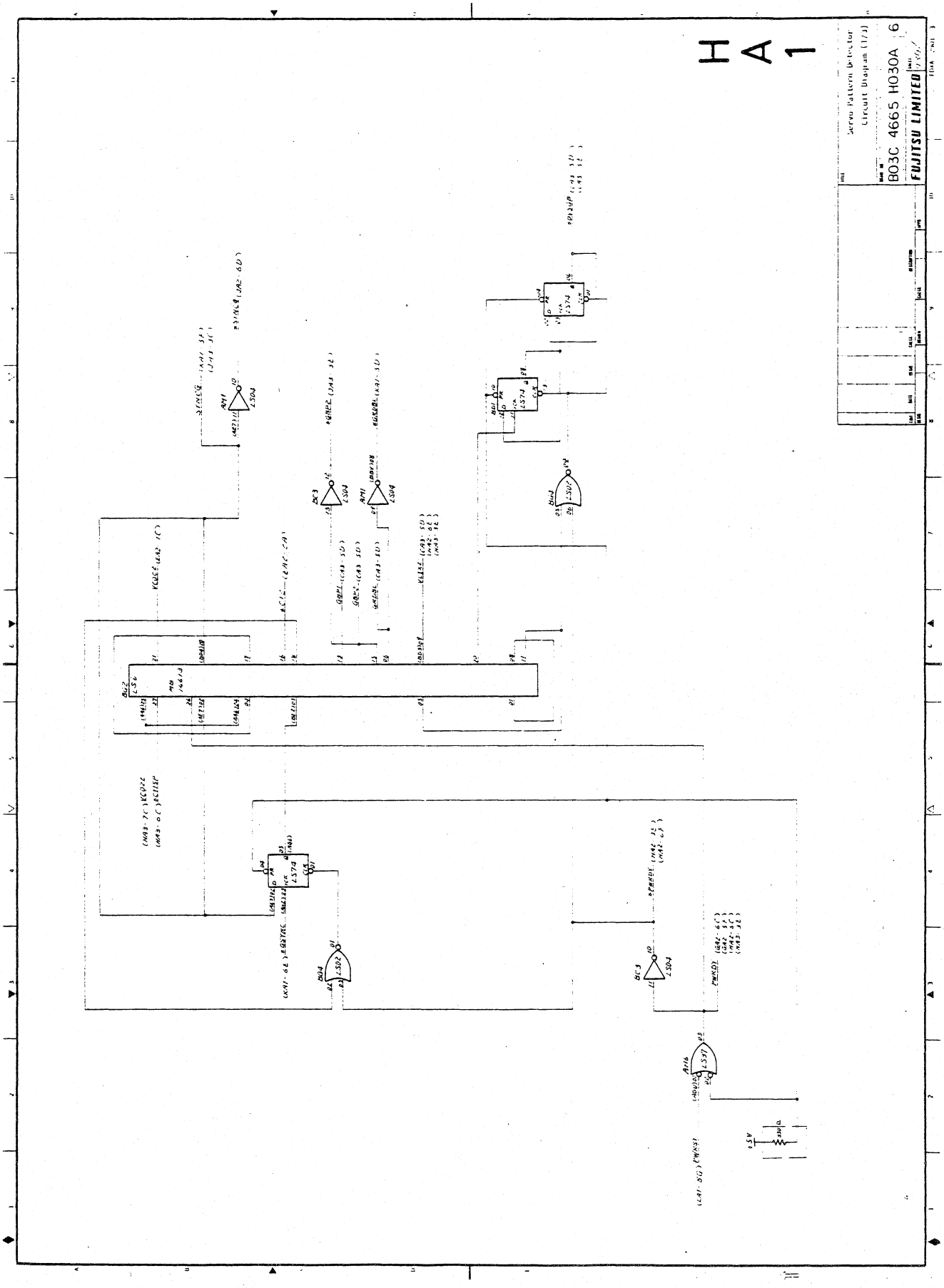

F A 1
VFO Control
Circuit Diagram (1/3)
B03C-4665-H030A
6
FUJITSU LIMITED
QUAD D-FF
COUNTER

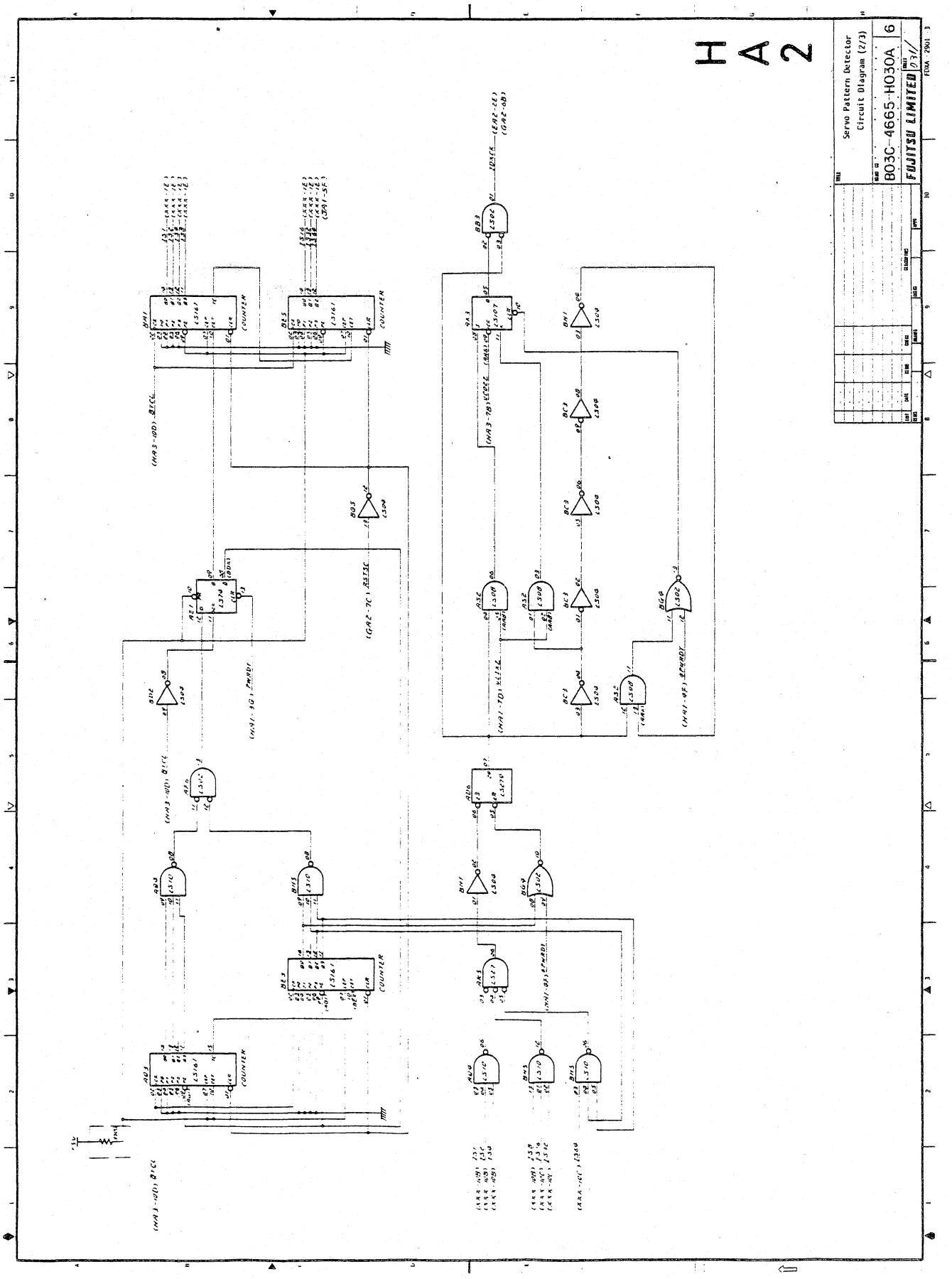

F A 2
VFO Control
Circuit Diagram (2/3)
B03C 4665 H030A 6
FUJITSU LIMITED

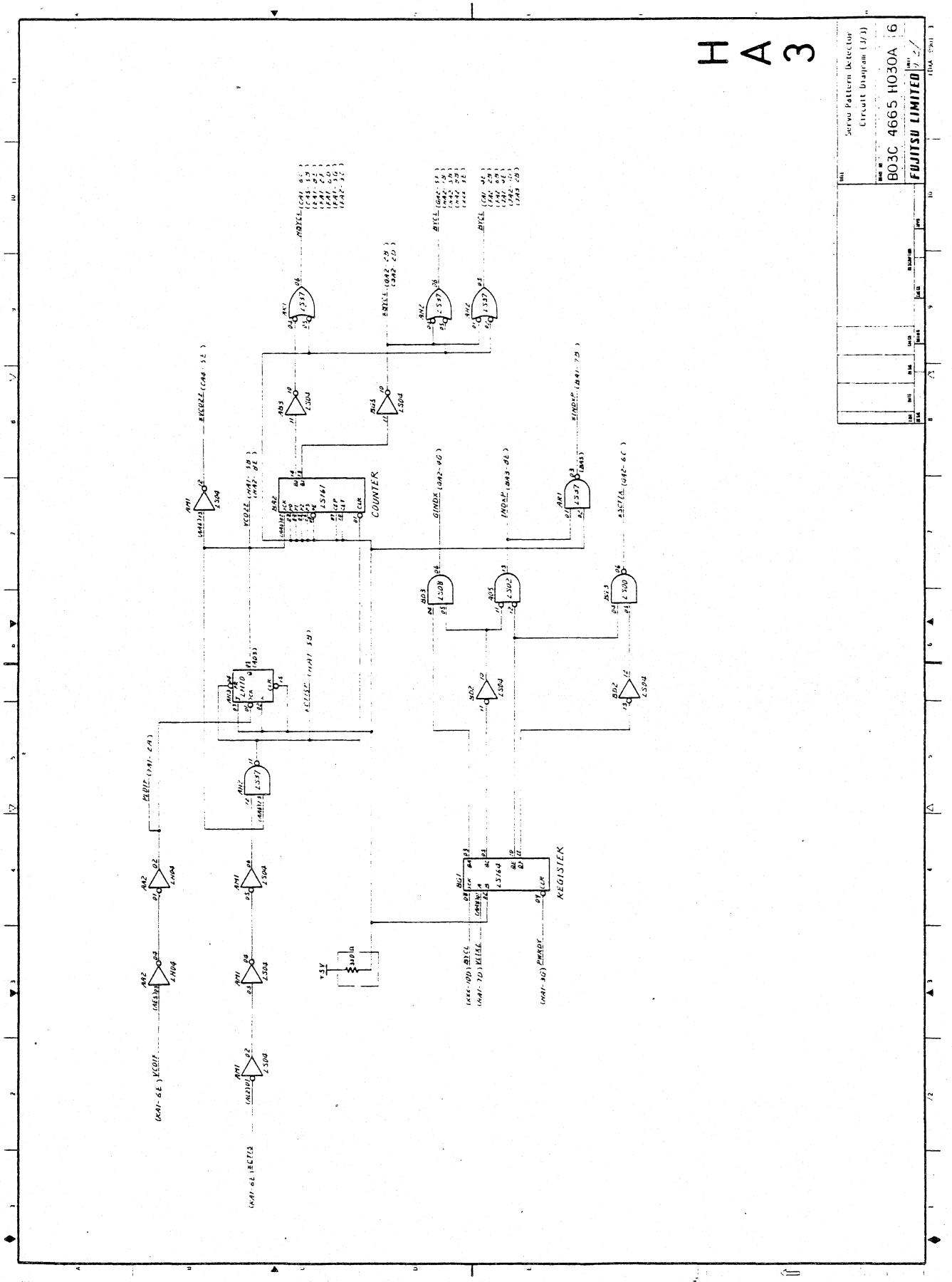

F A 3
VFO Control
Circuit Diagram (3/3)
B03C-4665-H030A
6
FUJITSU LIMITED
FUJA-2901 3

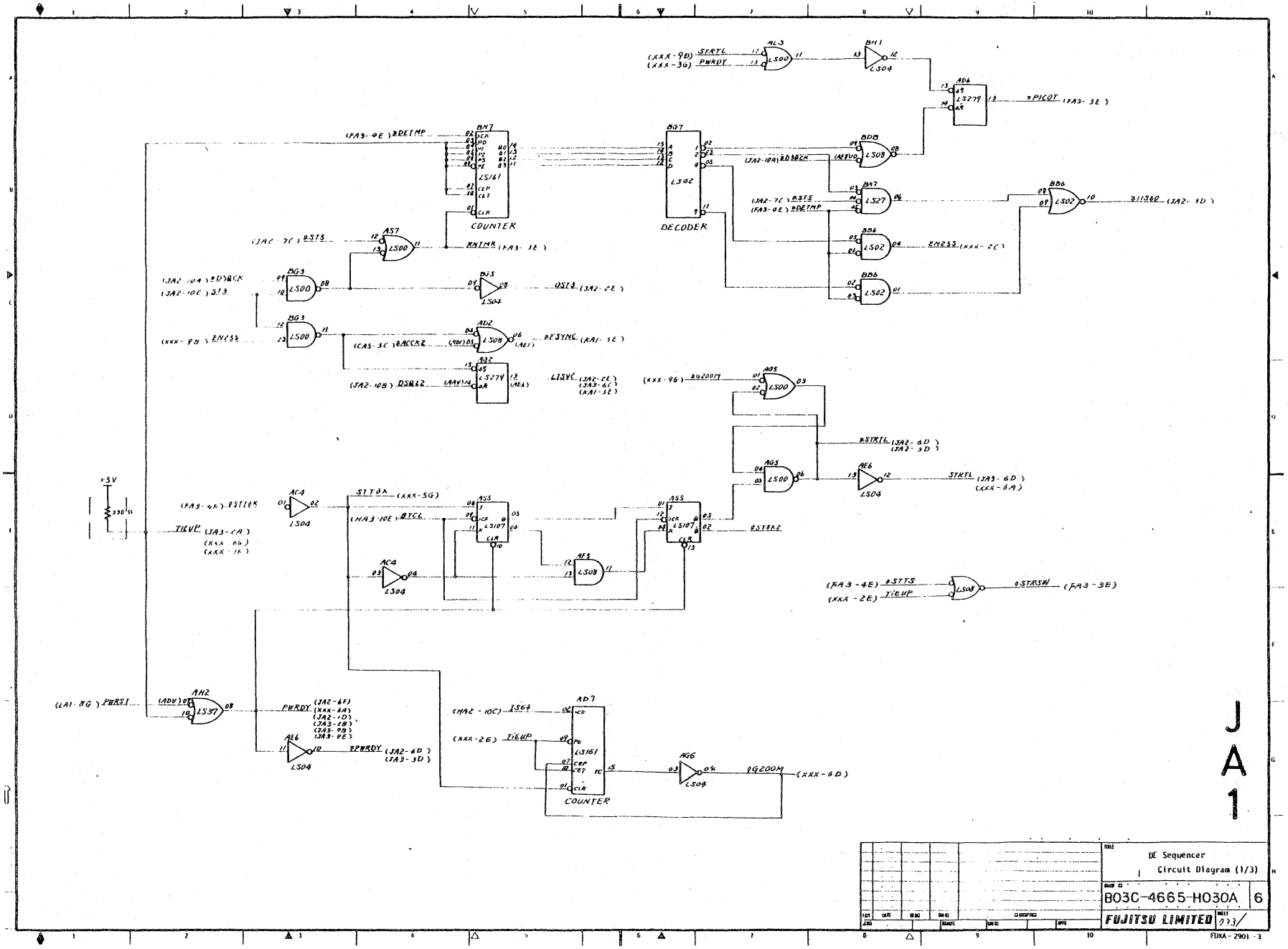

G
A
1
Sector Control
Circuit Diagram (1/2)
B03C-4665-H030A
6
FUJITSU LIMITED

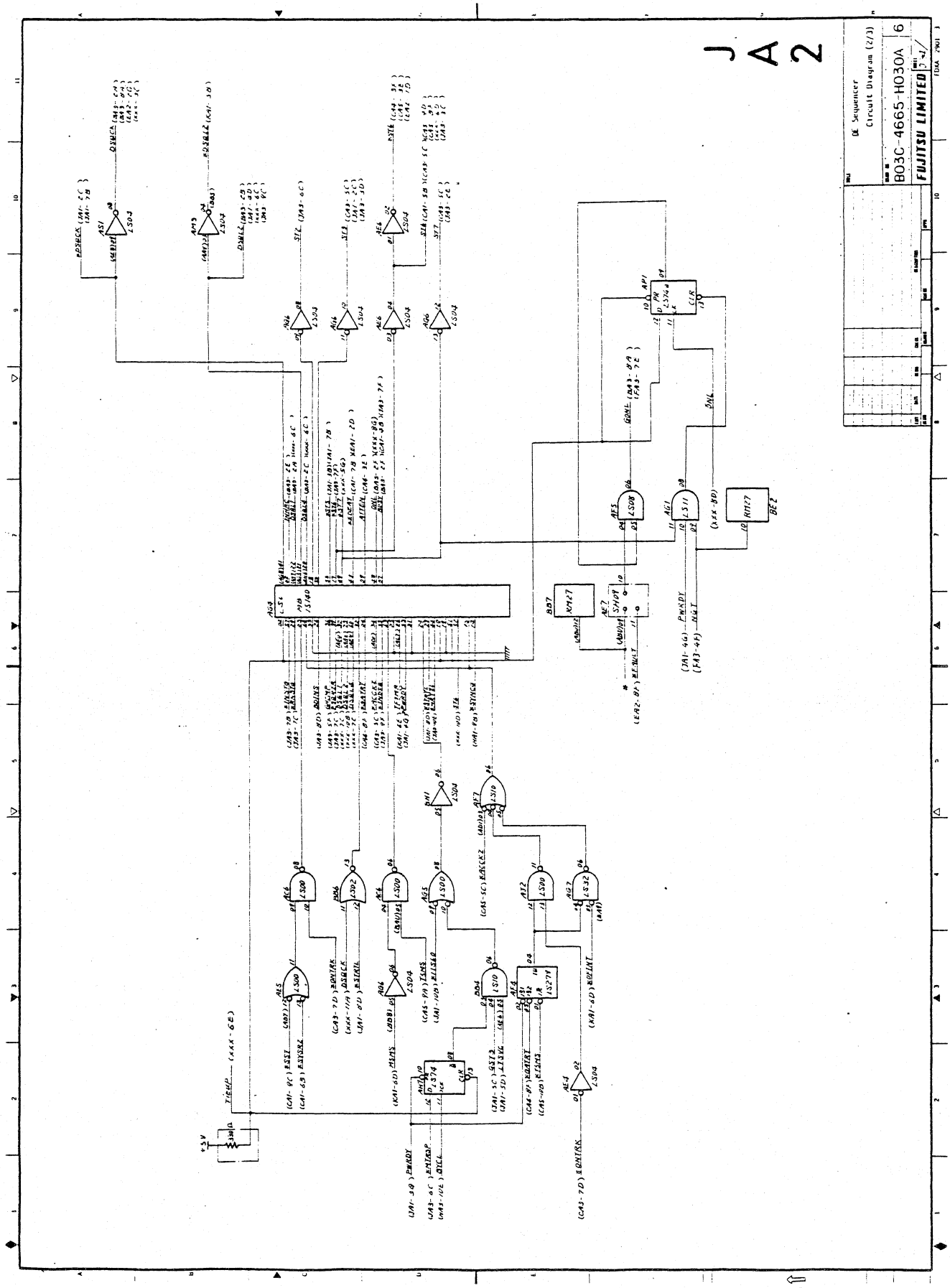

G A 2
Sector Control
Circuit Diagram (2/2)
B03C-4665-H030A 6
FUJITSU LIMITED

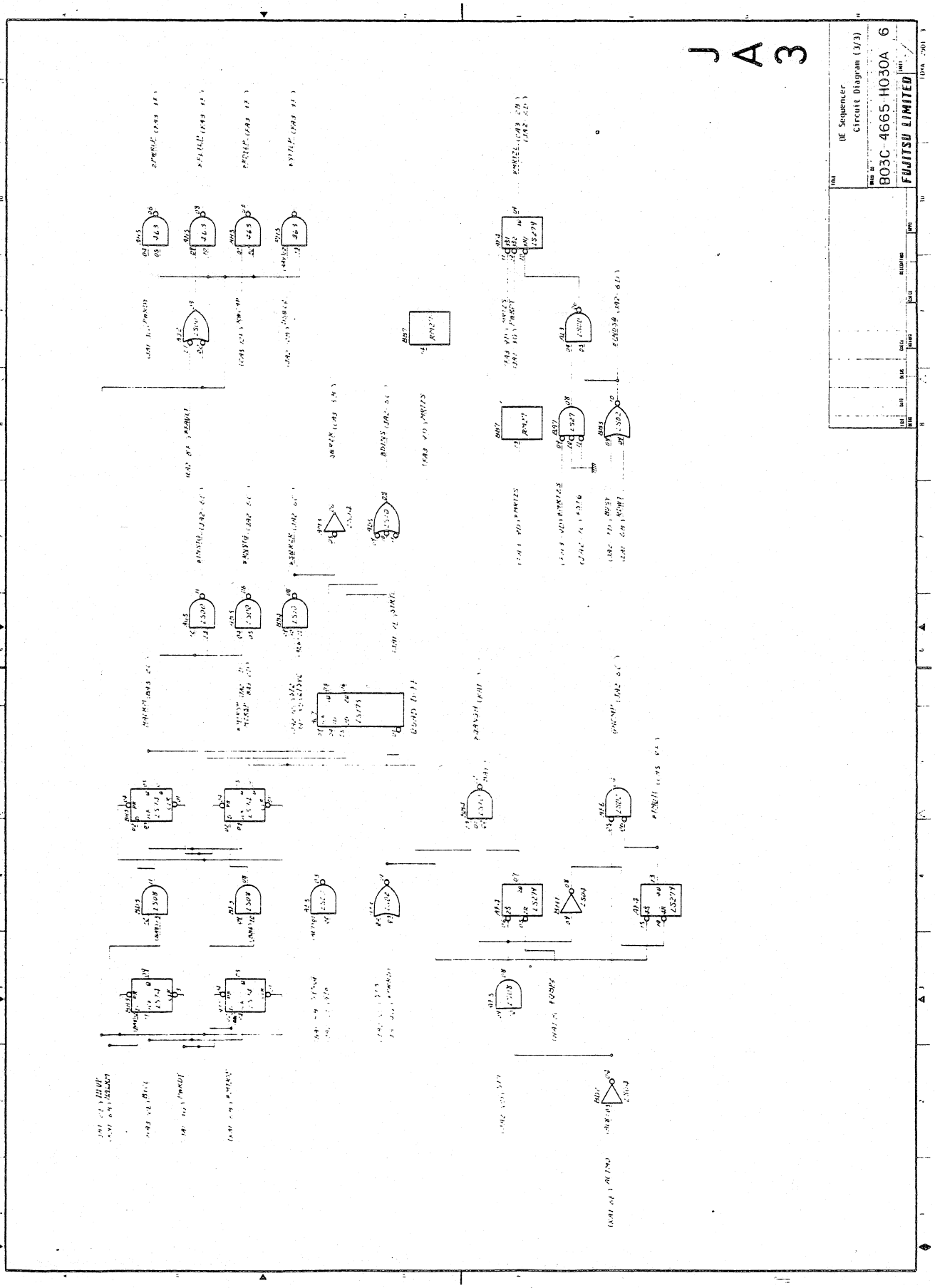

H
A
1
Servo Pattern Detector
Circuit Diagram (1/3)
B03C 4665 H030A 6
FUJITSU LIMITED

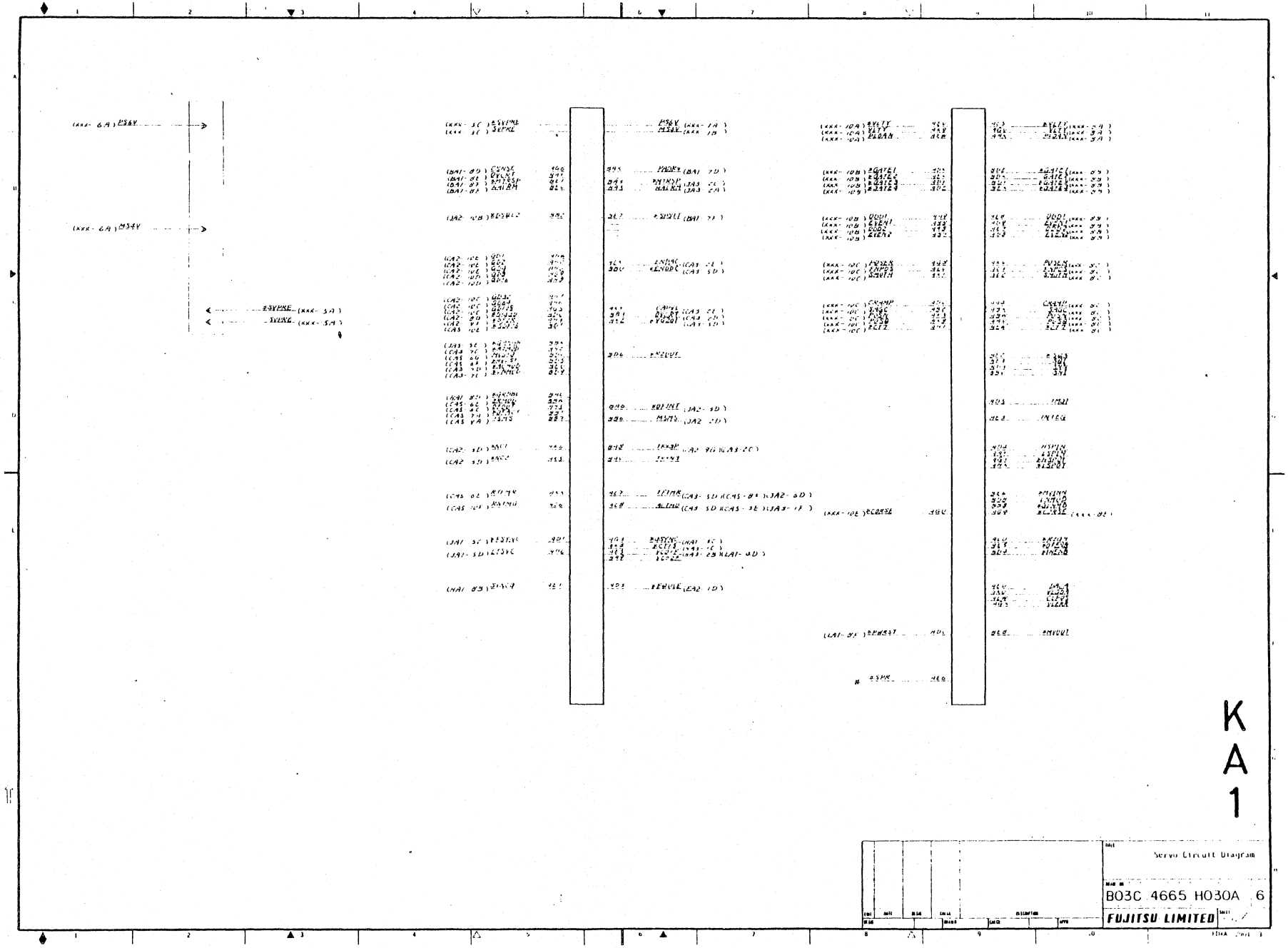

H
A
2
Servo Pattern Detector
Circuit Diagram (2/3)
B03C-4665-H030A
6
FUJITSU LIMITED

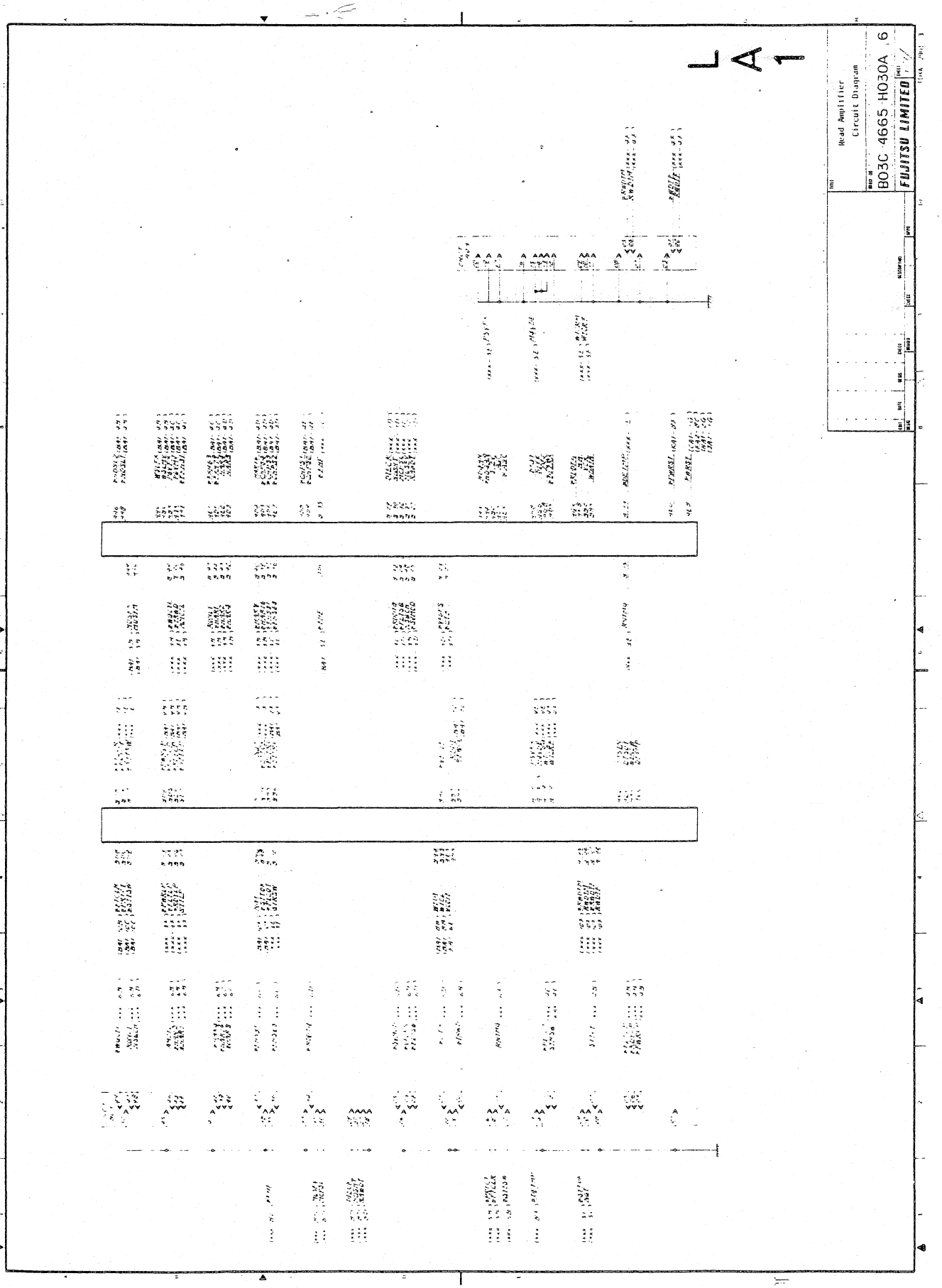

H A 3
Servo Pattern Detector
Circuit Diagram (3/3)
B03C 4665 H030A 6
FUJITSU LIMITED
COUNTER
REGISTER

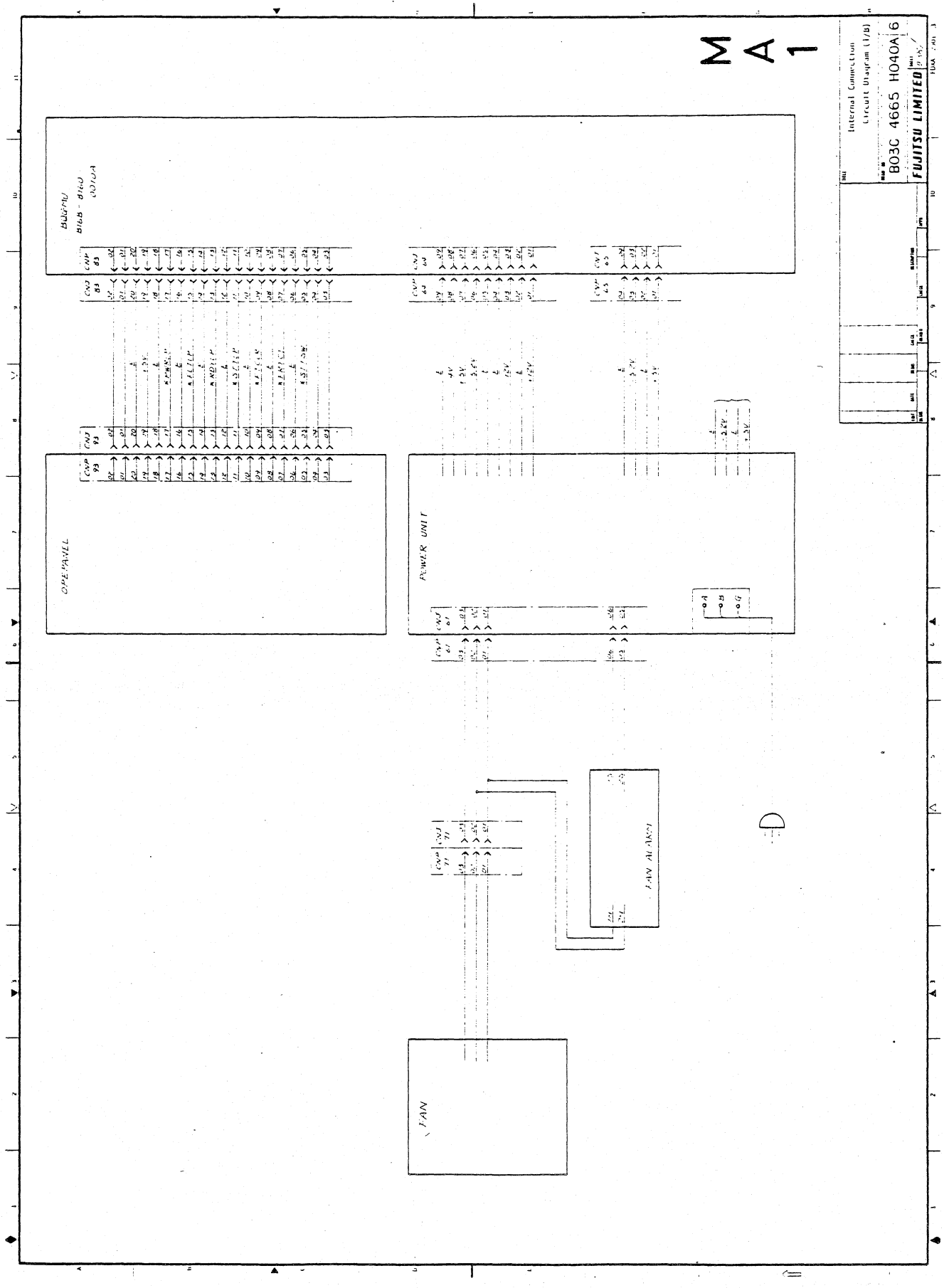

COUNTER
DECODER
COUNTER
+5V
330Ω
J
A
1
DE Sequencer
Circuit Diagram (1/3)
B03C-4665-H030A
6
FUJITSU LIMITED
FDXA-2901-3

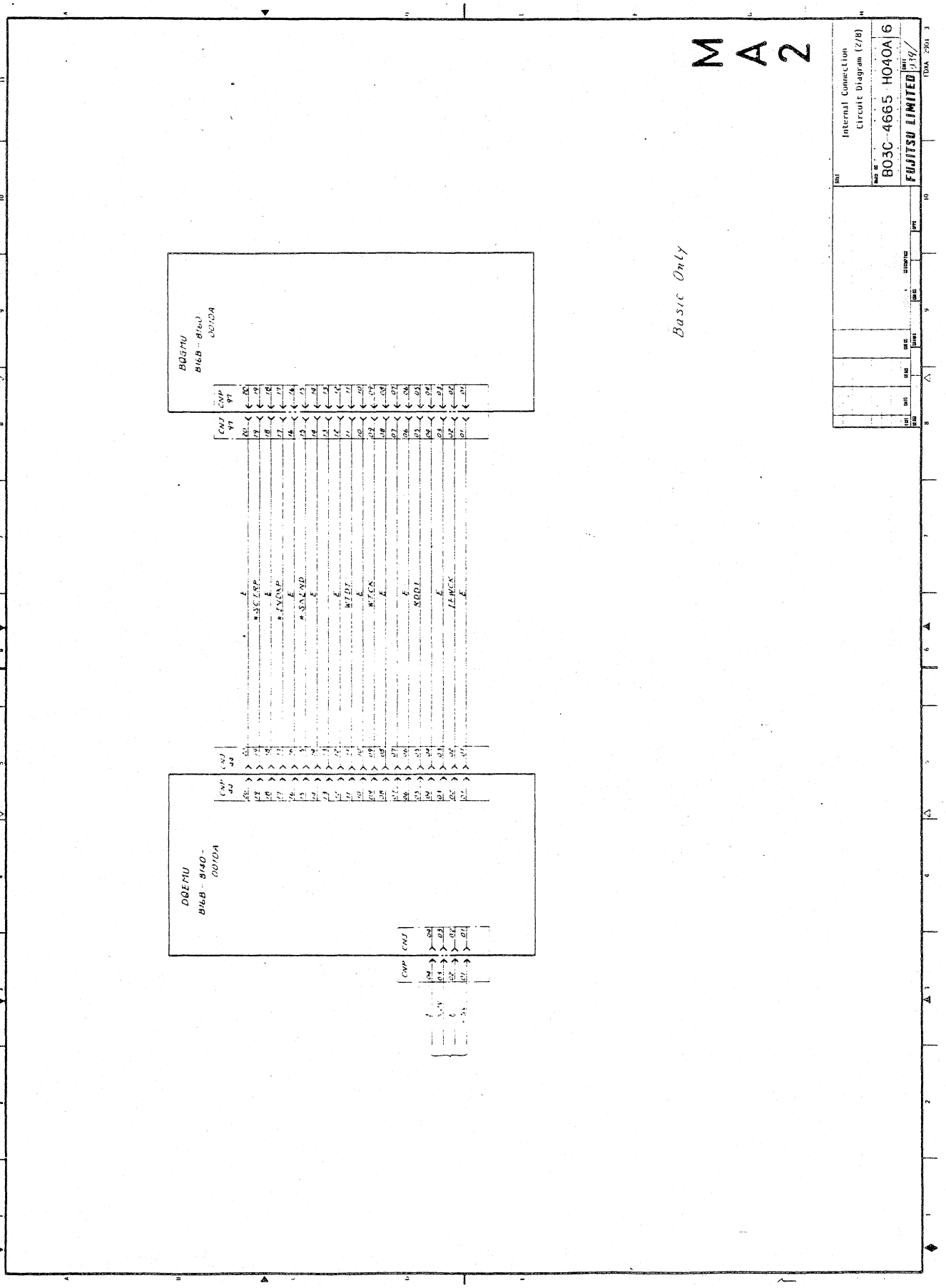

J
A
2
DE Sequencer
Circuit Diagram (2/3)
B03C-4665-H030A
6
FUJITSU LIMITED

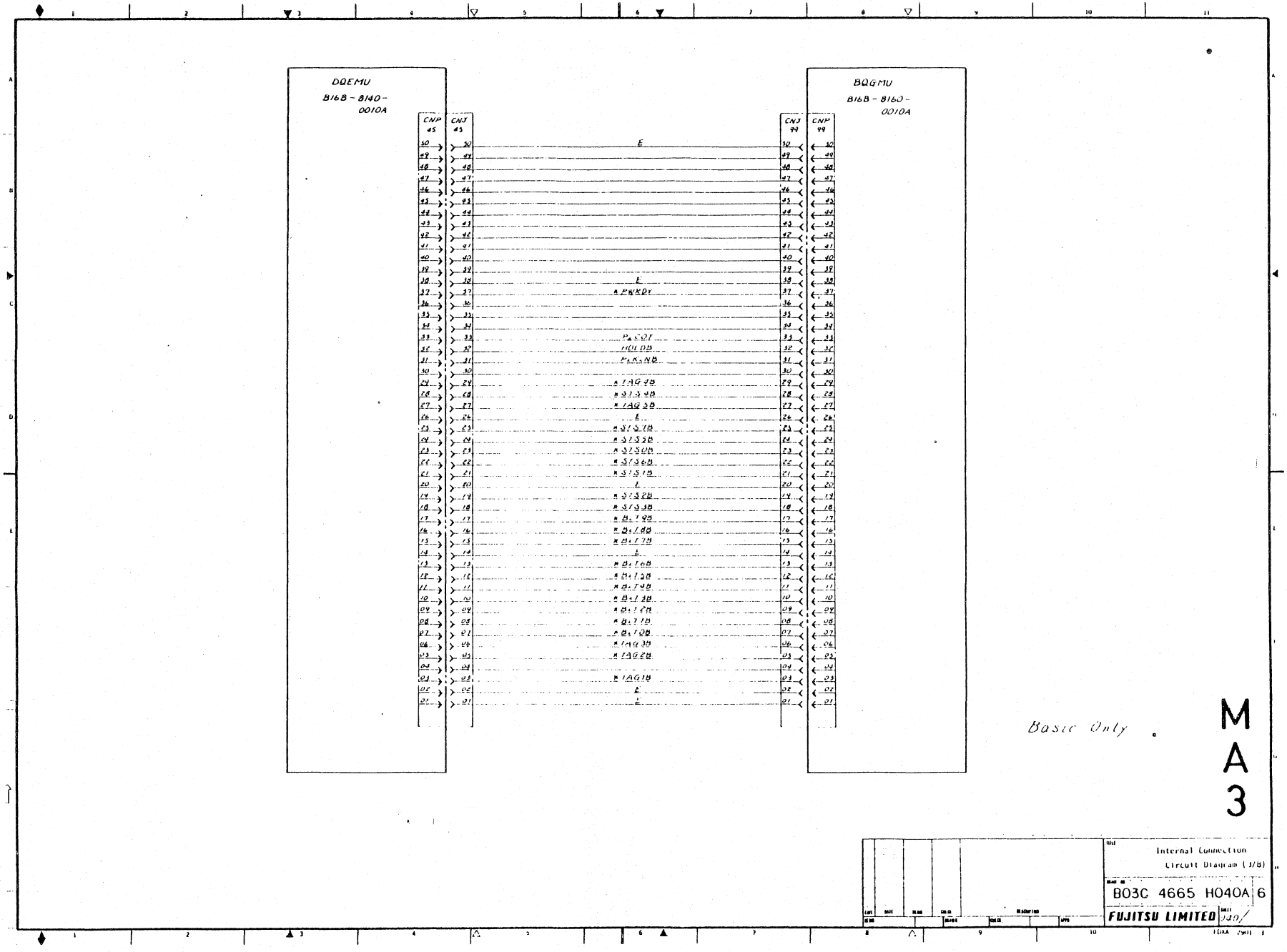

J
A
3
DE Sequencer
Circuit Diagram (3/3)
B03C-4665-H030A 6
FUJITSU LIMITED


K
A
1
Servo Circuit Diagram
B03C 4665 H030A 6
FUJITSU LIMITED


Read Amplifier
Circuit Diagram
B03C-4665-H030A
FUJITSU LIMITED


MA1
Internal Connection
Circuit Diagram (1/8)
B03C 4665 H040A|6
FUJITSU LIMITED
BUSPNL
OPE.PANEL
POWER UNIT
FAN
FAN MOTOR


MA2
Basic Only
Internal Connection
Circuit Diagram (2/8)
B03C-4665-H040A 6
FUJITSU LIMITED
BQSMU
BQEMU
*SCLKP
*LYONP
*SAEND
WTDT
WTCK
RDDT
LEWCK



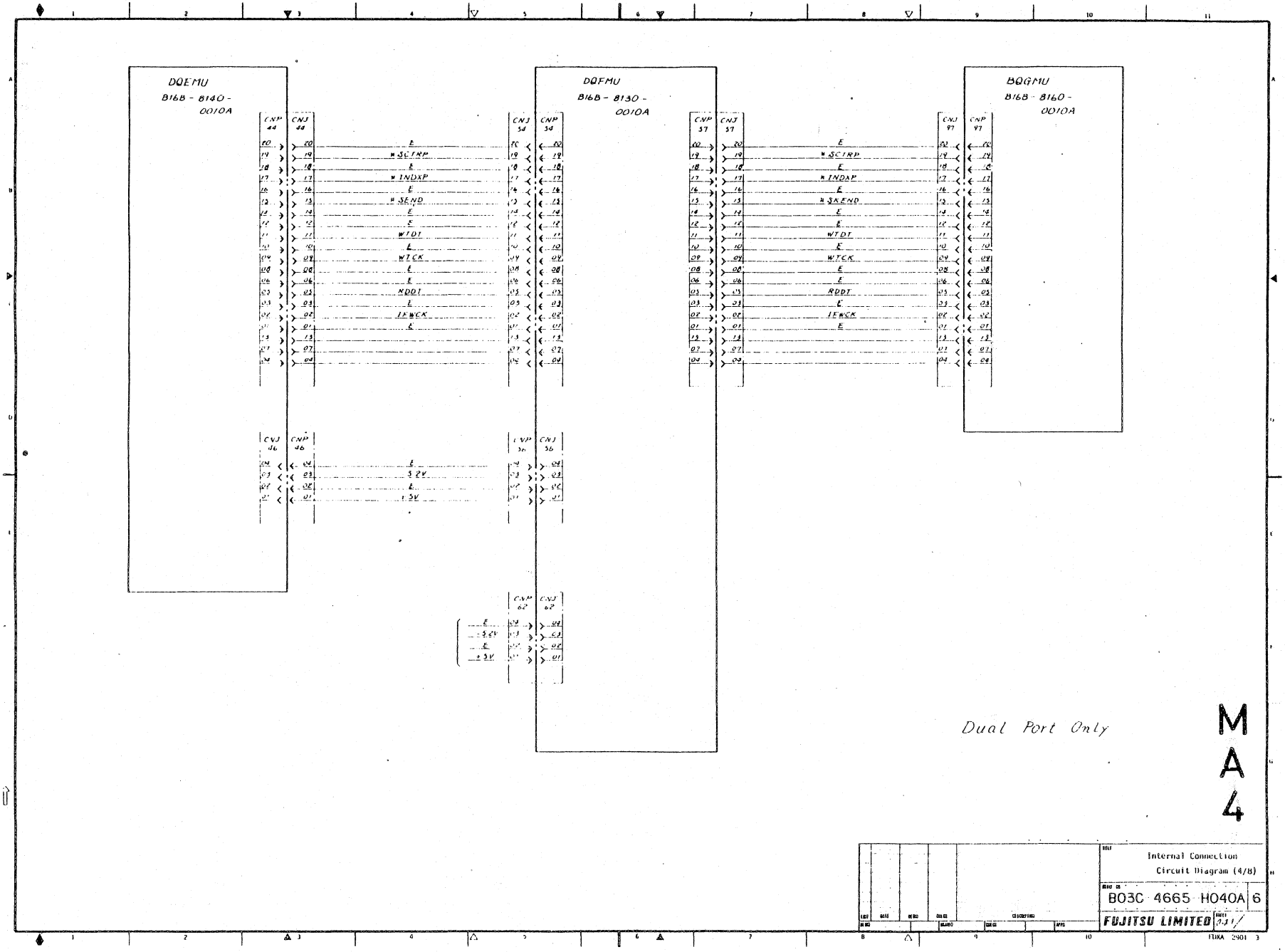
Basic Only

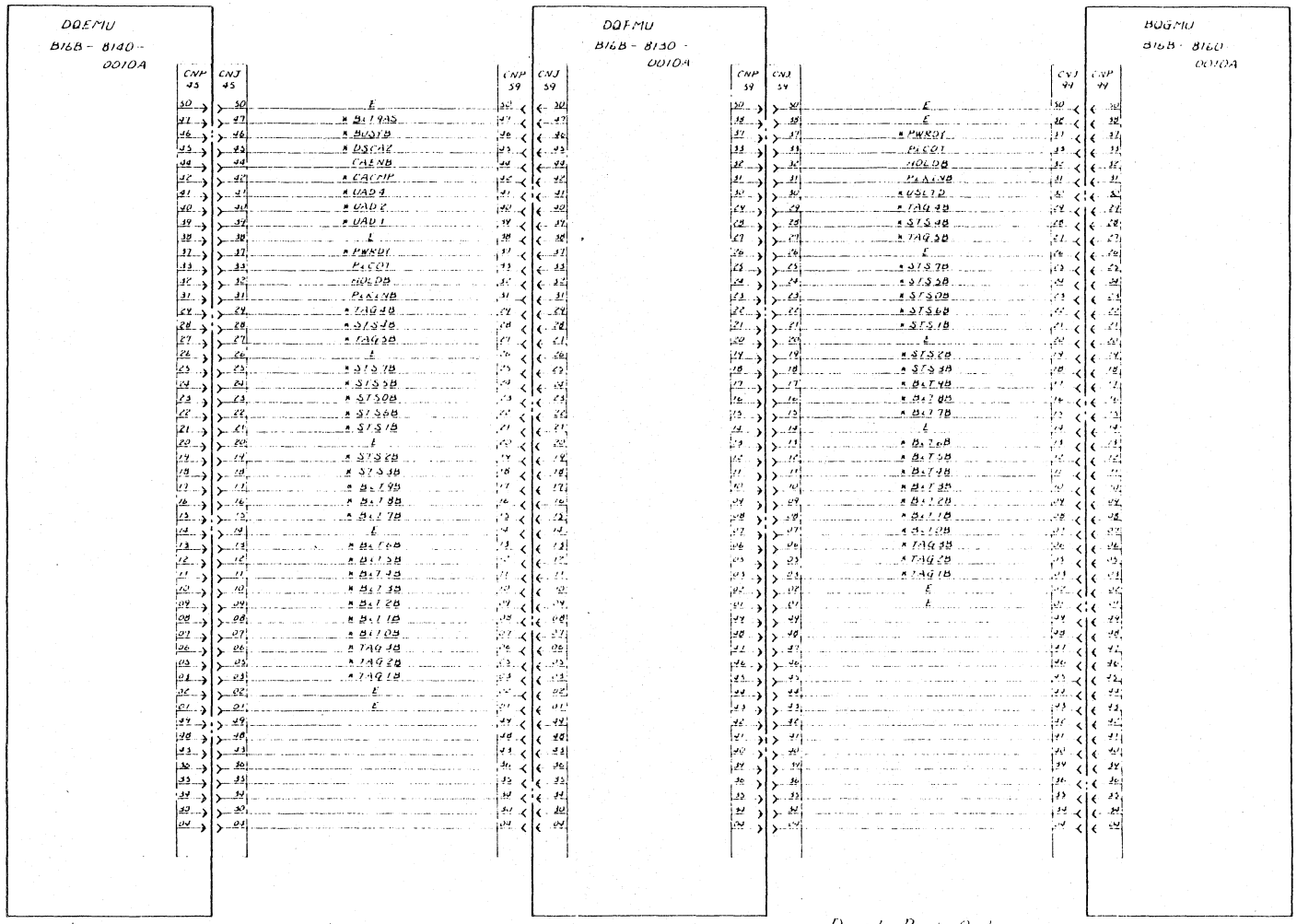
M
A
3

Internal Connection
Circuit Diagram (1/8)

B03C 4665 H040A 6

FUJITSU LIMITED


DQEMU
B16B-8140-0010A
DQFMU
B16B-8130-0010A
BQGMU
B16B-8160-0010A
CNP 44
CNJ 44
CNJ 54
CNP 54
CNP 57
CNJ 57
CNJ 97
CNP 97
CNJ 46
CNP 46
CNP 56
CNJ 56
CNP 62
CNJ 62
E
M SCINP
E
M INDXP
E
M SEND
E
E
WTDT
E
WTCK
E
E
RDDT
E
IFWCK
E
M SKEND
+5.2V
+5V
Dual Port Only
M
A
4
Internal Connection
Circuit Diagram (4/8)
B03C 4665 H040A 6
FUJITSU LIMITED
FDXA 2901 3

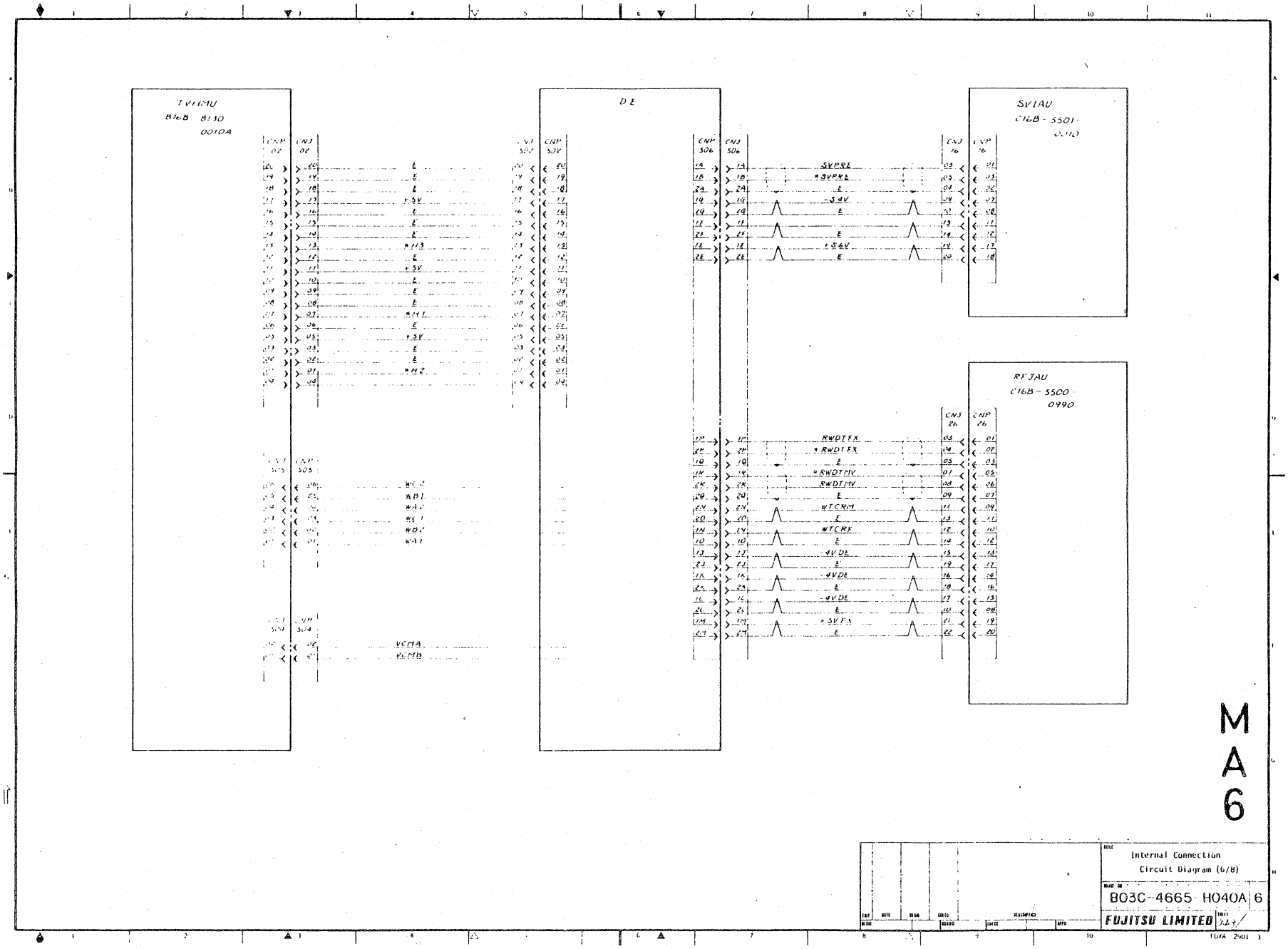


M
A
5

Internal Connection
Circuit Diagram (5/8)

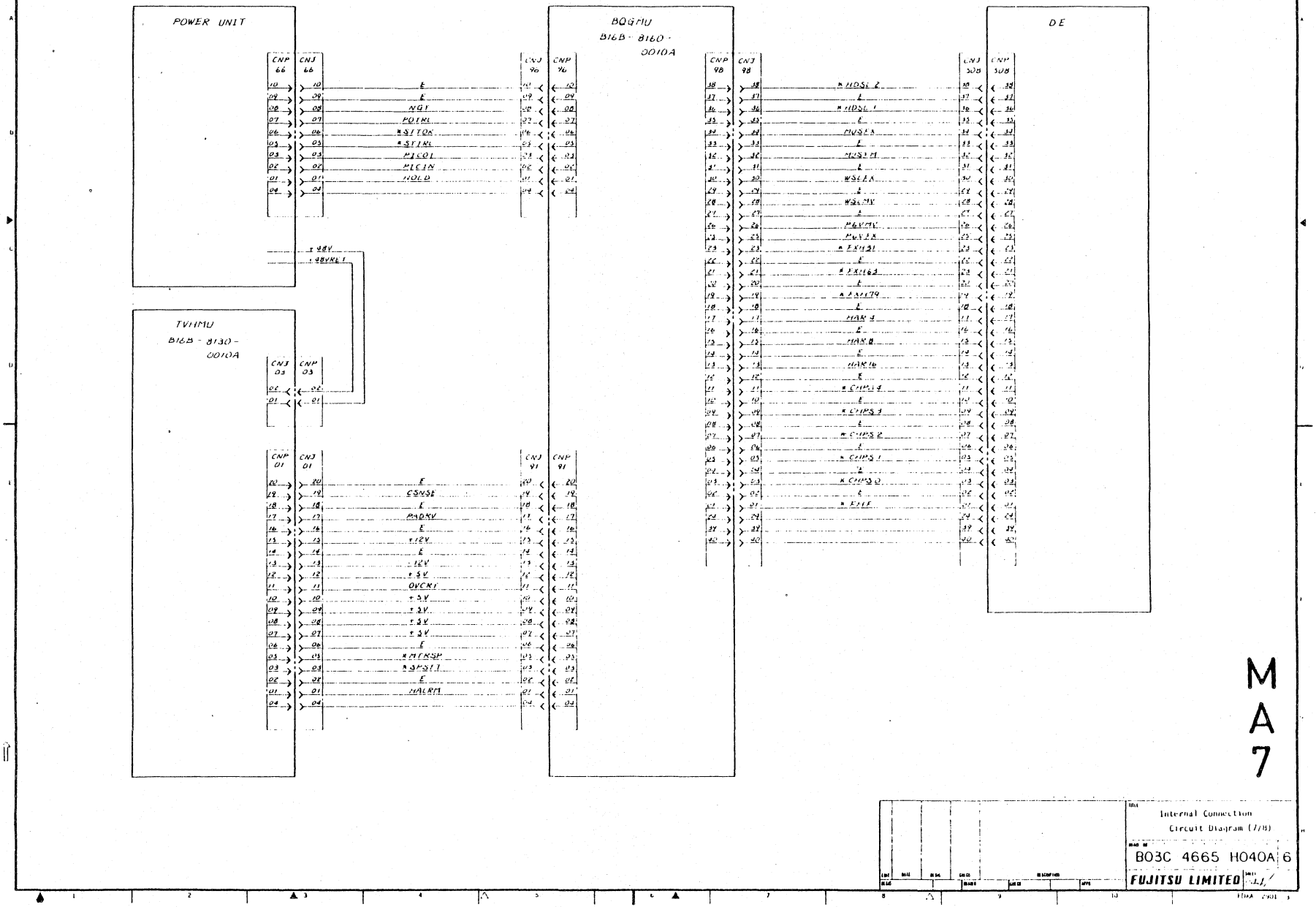
B03C 4665 H040A 6

FUJITSU LIMITED



M
A
6

TITLE	Internal Connection Circuit Diagram (6/8)
DRAW NO	B03C-4665-H040A 6
FUJITSU LIMITED	

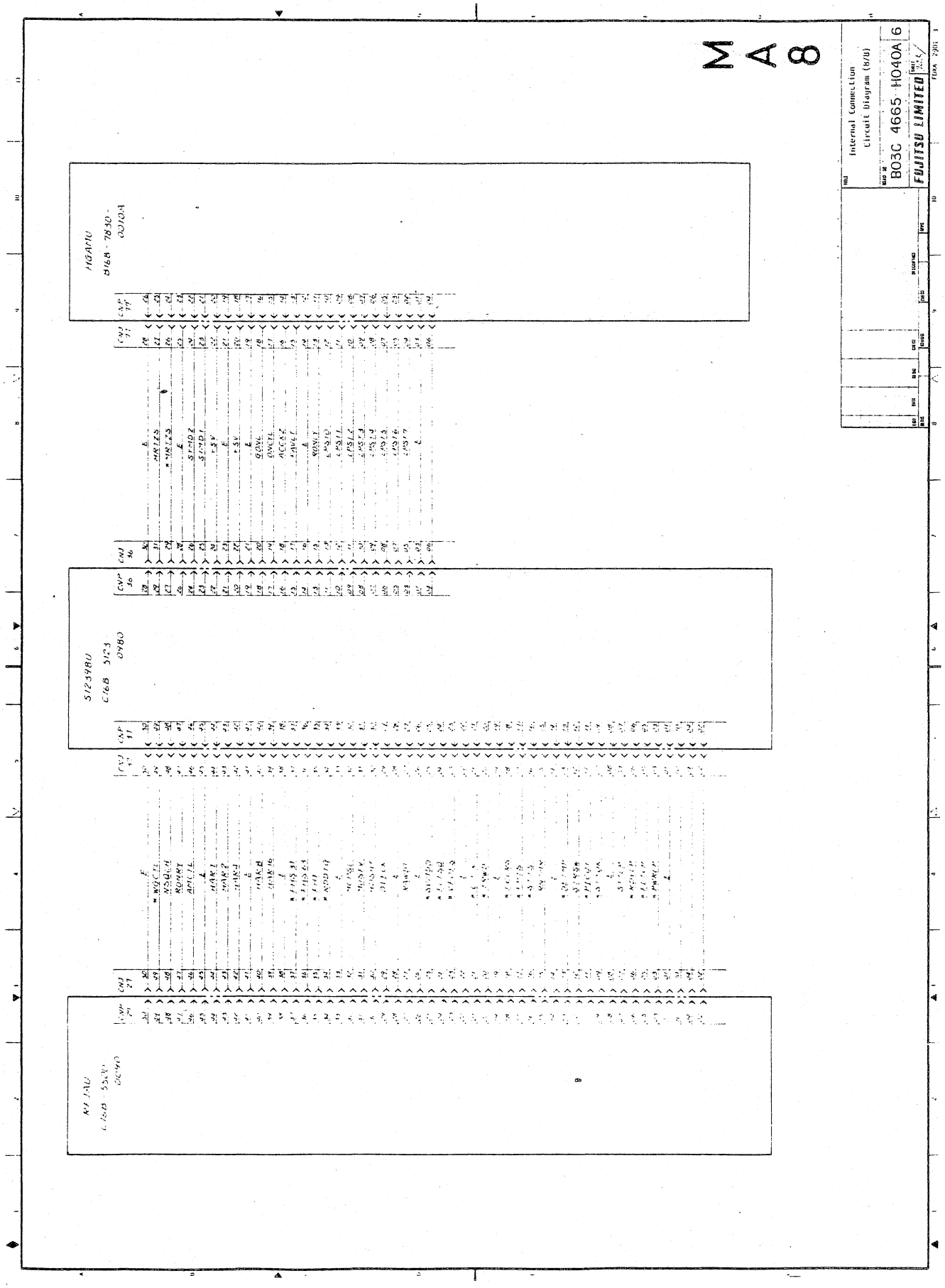


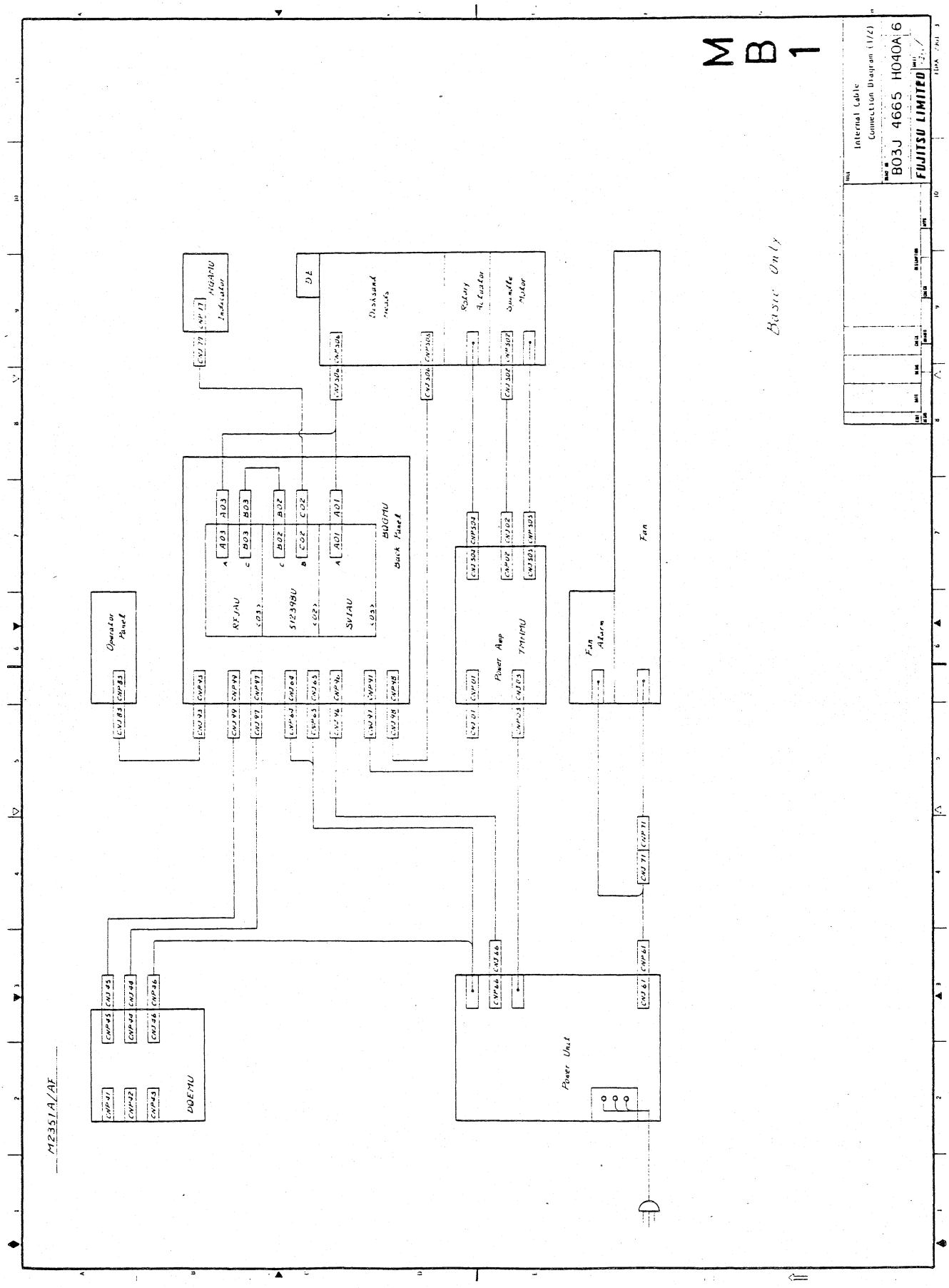
MA7

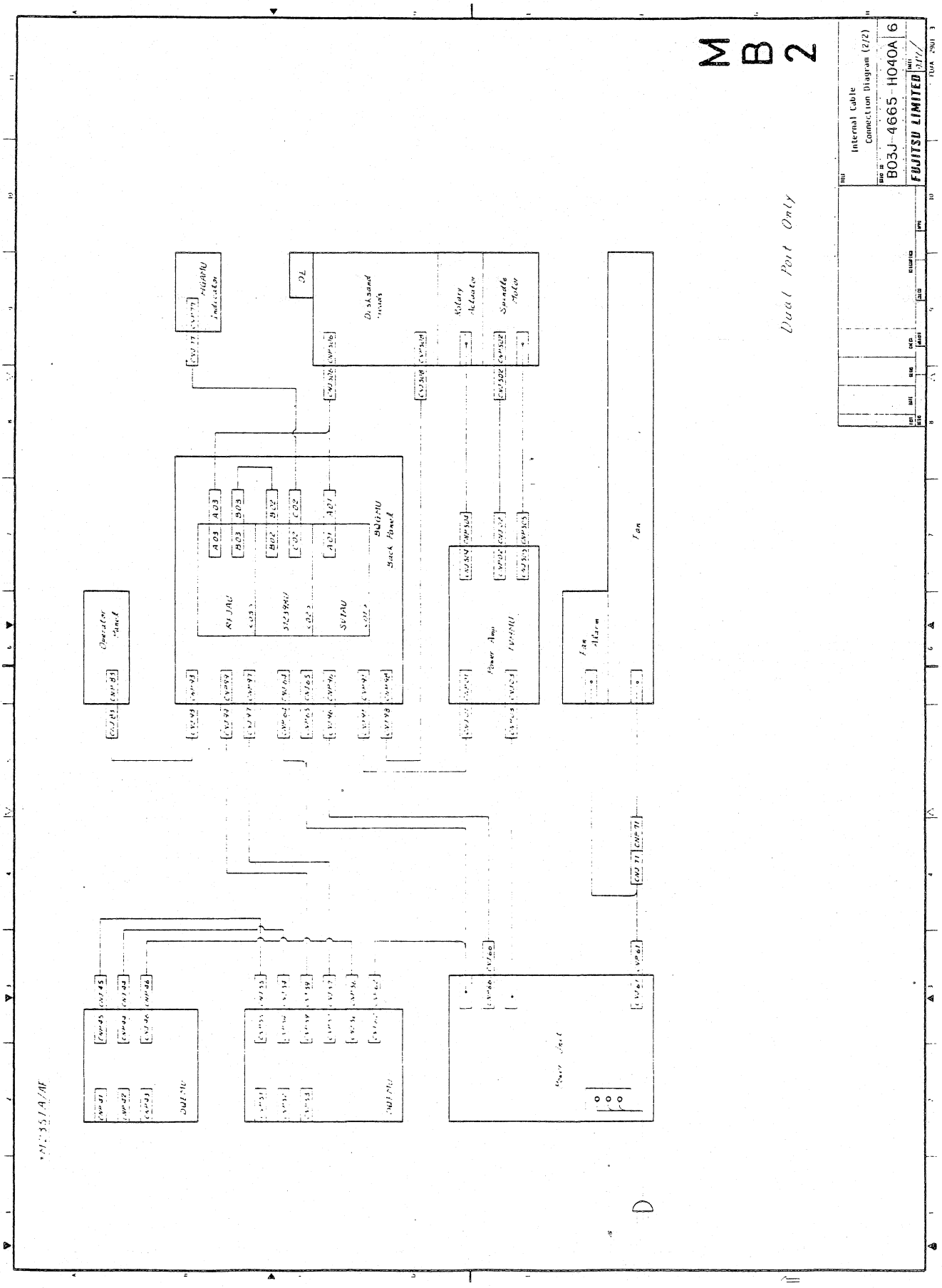
Internal Connection Circuit Diagram (1/8)

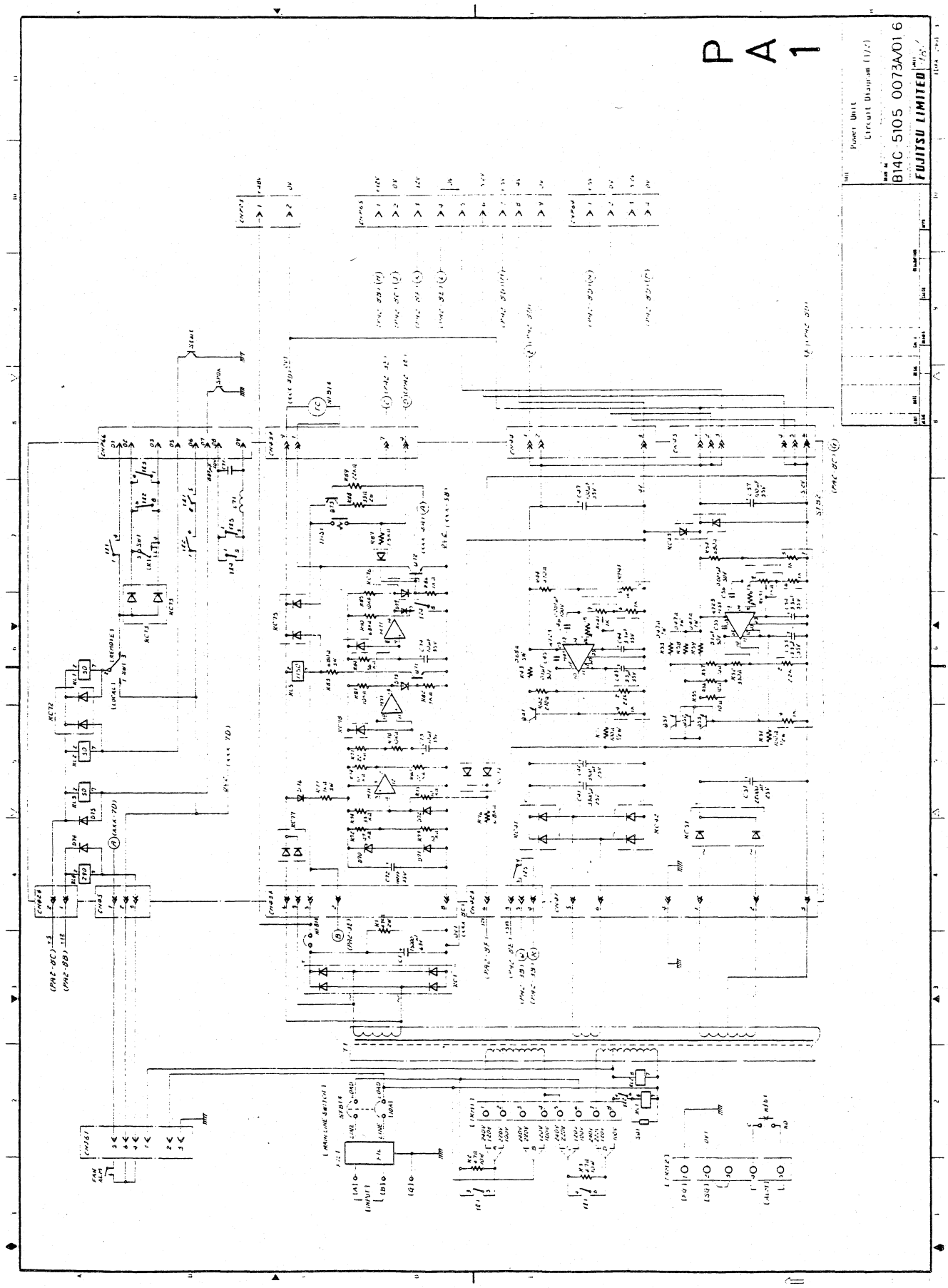
B03C 4665 H040A 6

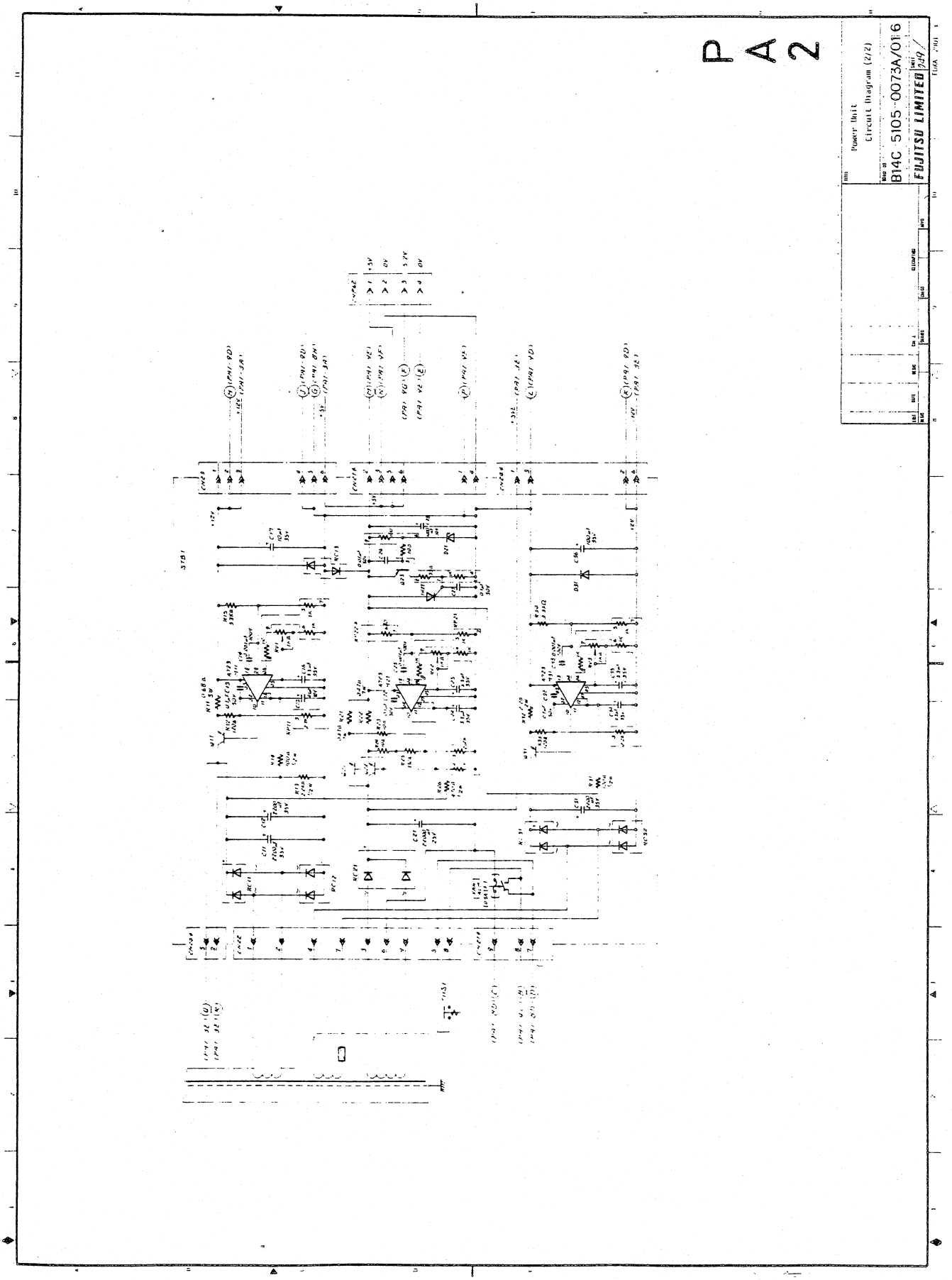
FUJITSU LIMITED

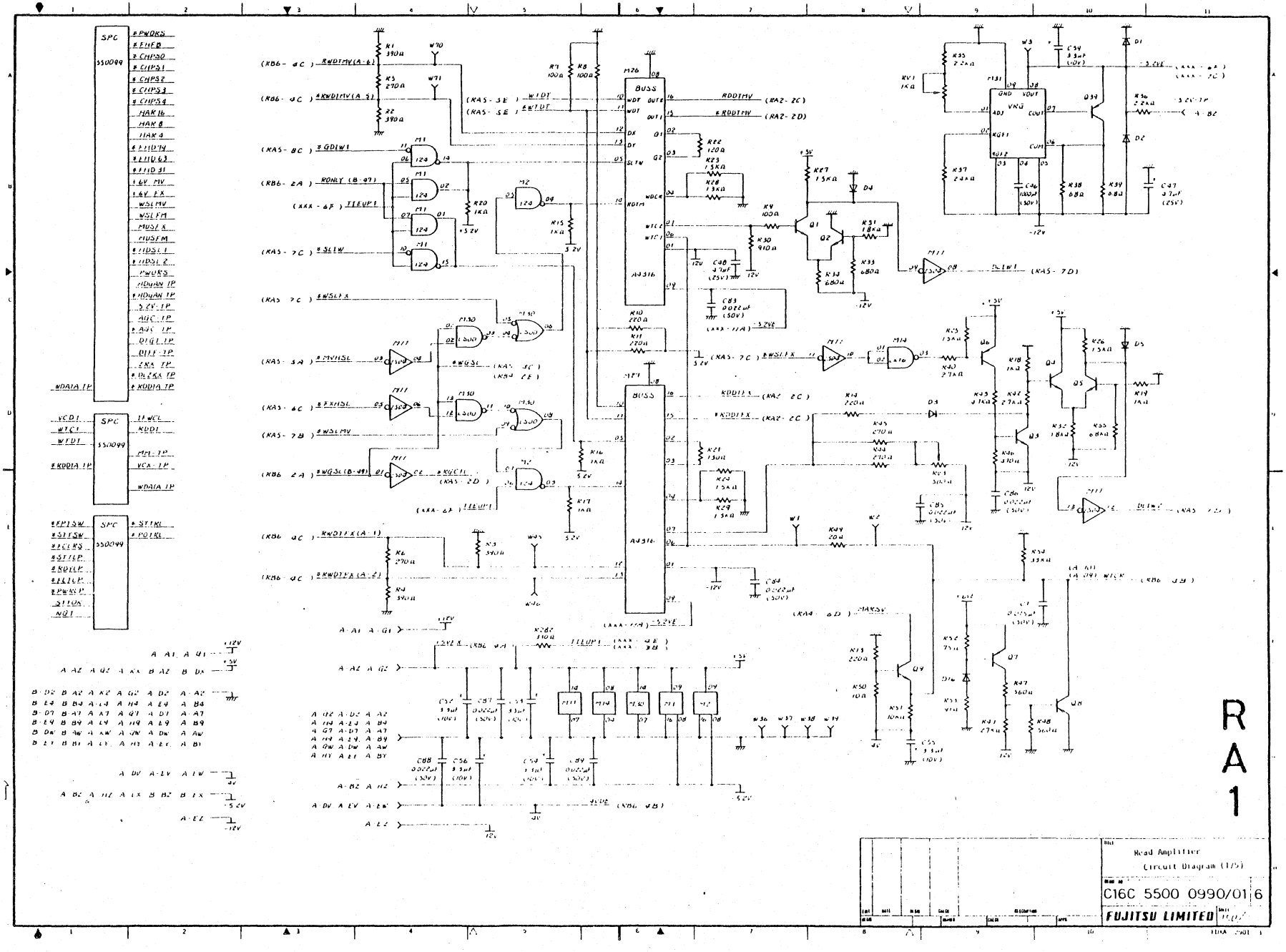

MA8
Internal Connection
Circuit Diagram (8/8)
B03C 4665 H040A 6
FUJITSU LIMITED

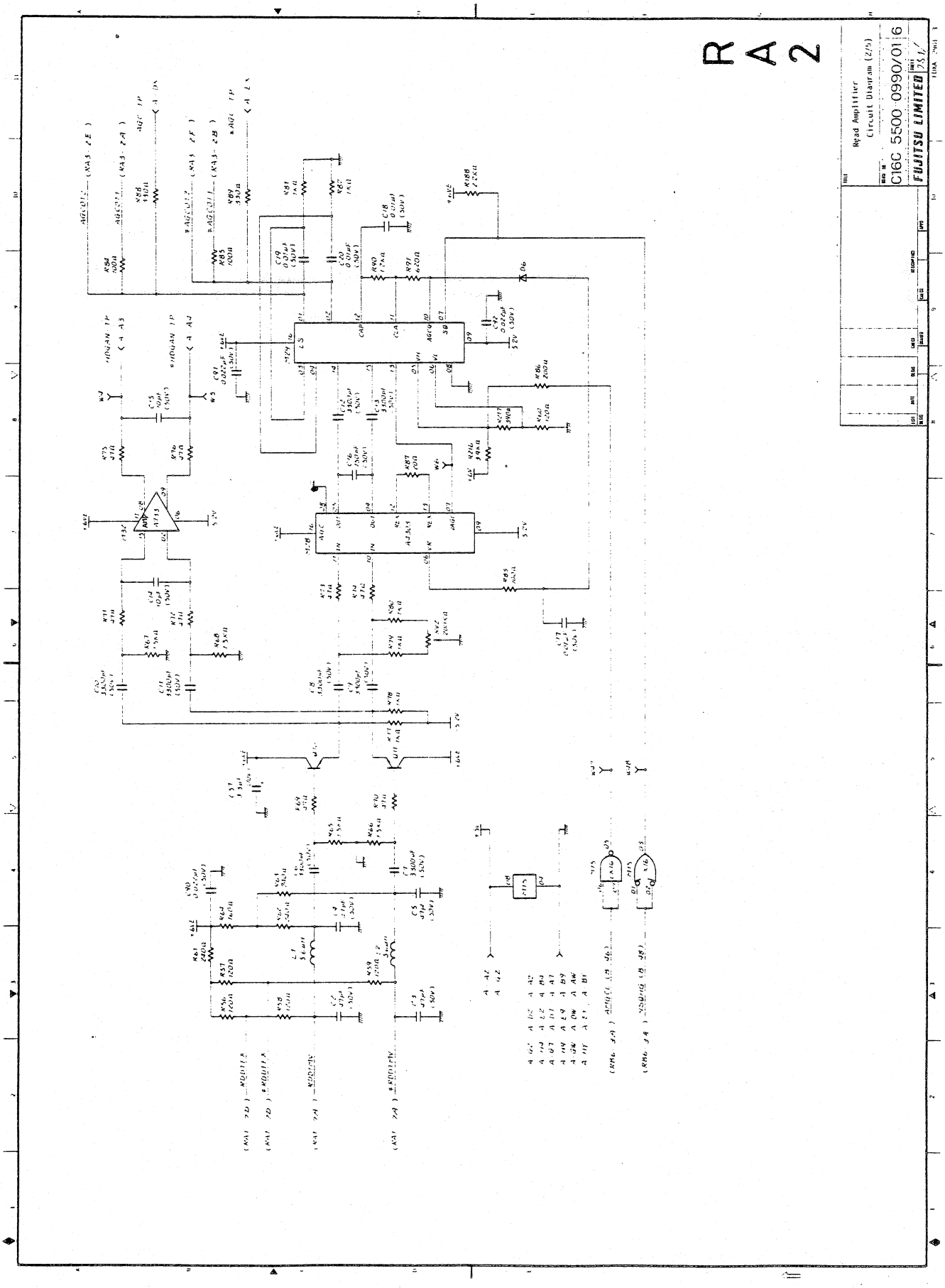

M B 1
Internal Cable Connection Diagram (1/2)
B03J 4665 H040A-6
FUJITSU LIMITED
Basic Only
M2351A/AF
Operator Panel
DUEMU
Power Unit
Power Amp
Fan
Fan Alarm
Back Panel
Rotary Actuator
Remote Motor

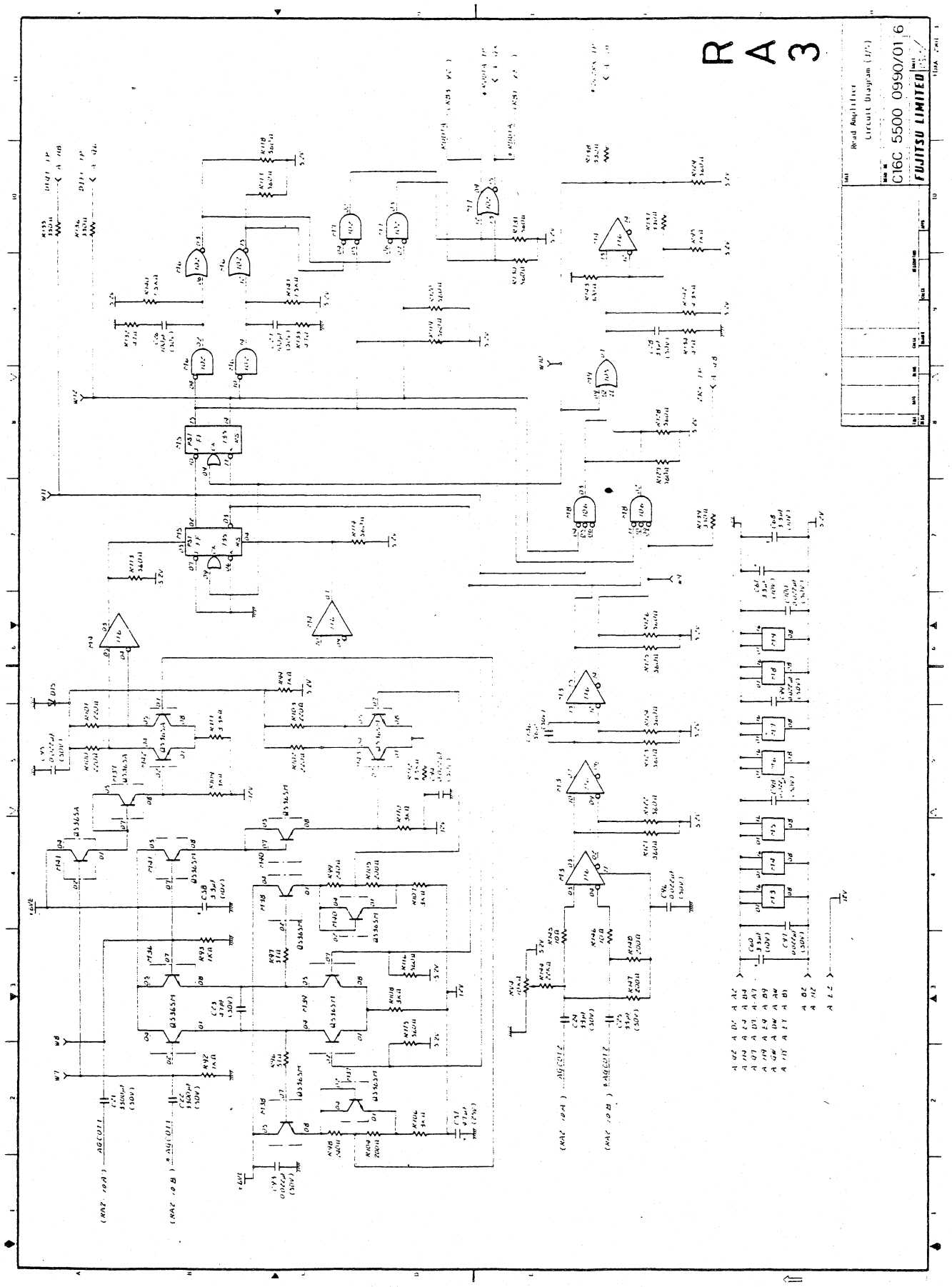

MB2
Internal Cable
Connection Diagram (2/2)
B03J-4665-H040A
FUJITSU LIMITED
Dual Port Only
Operator Panel
Power Supply Unit
Fan
Fan Alarm
Disk Drives
Rotary Actuator
Spindle Motor
Back Panel
Power Panel
Power Unit
Fan
D

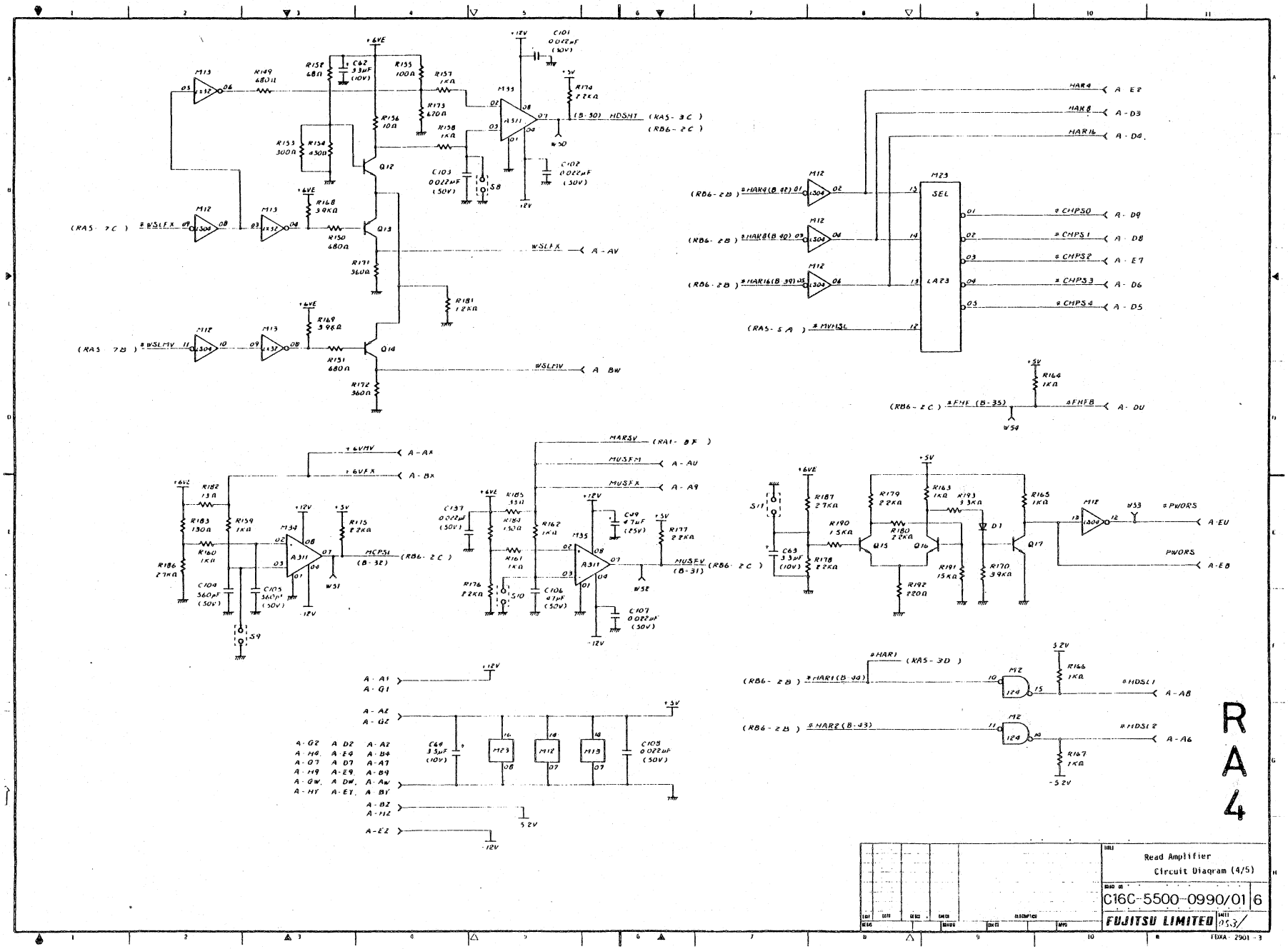

P A 1
Power Unit
Circuit Diagram (1/2)
B14C 5105 0073A/016
FUJITSU LIMITED

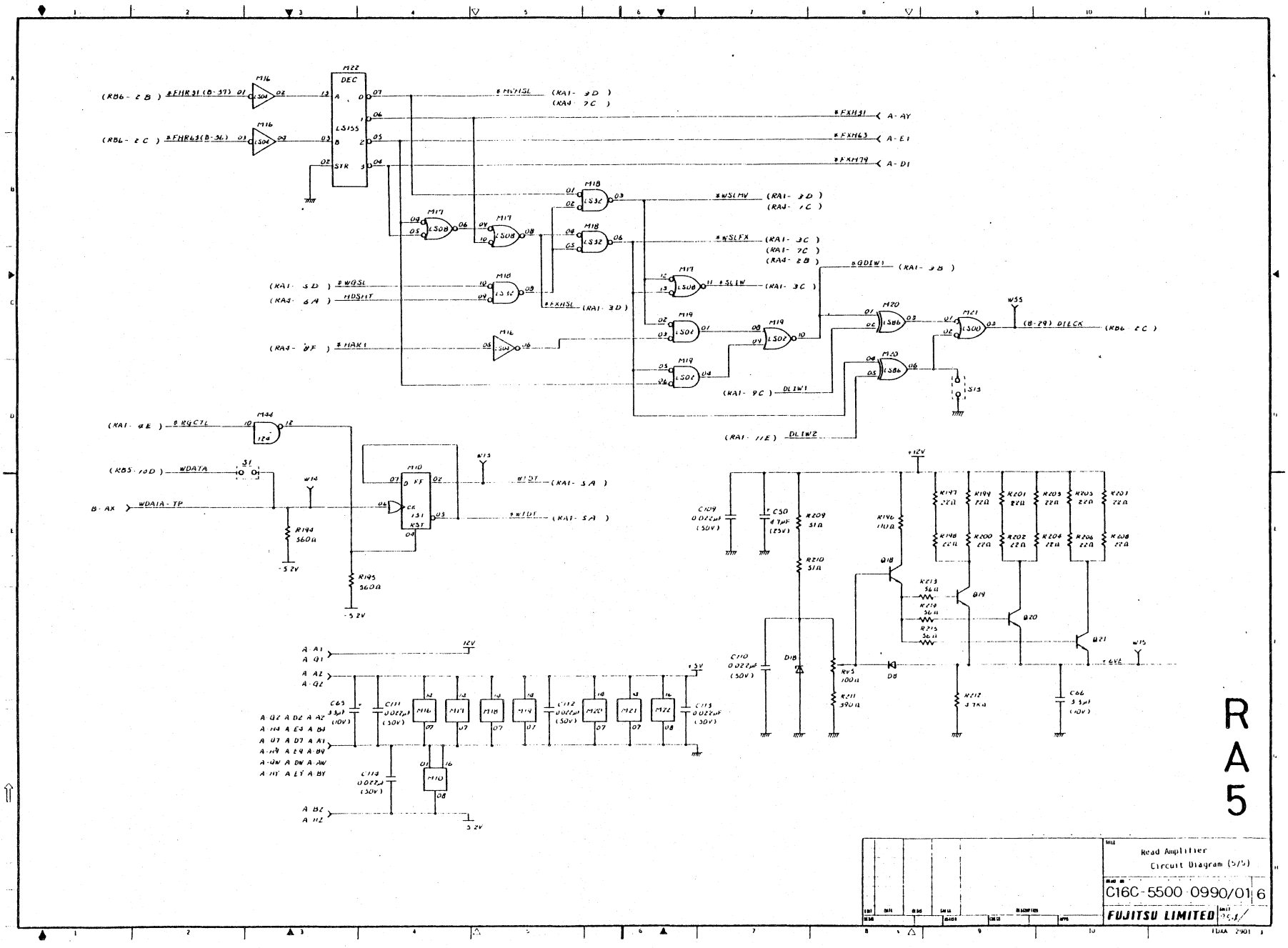

PA2
Power Unit
Circuit Diagram (2/2)
B14C-5105-0073A/016
FUJITSU LIMITED

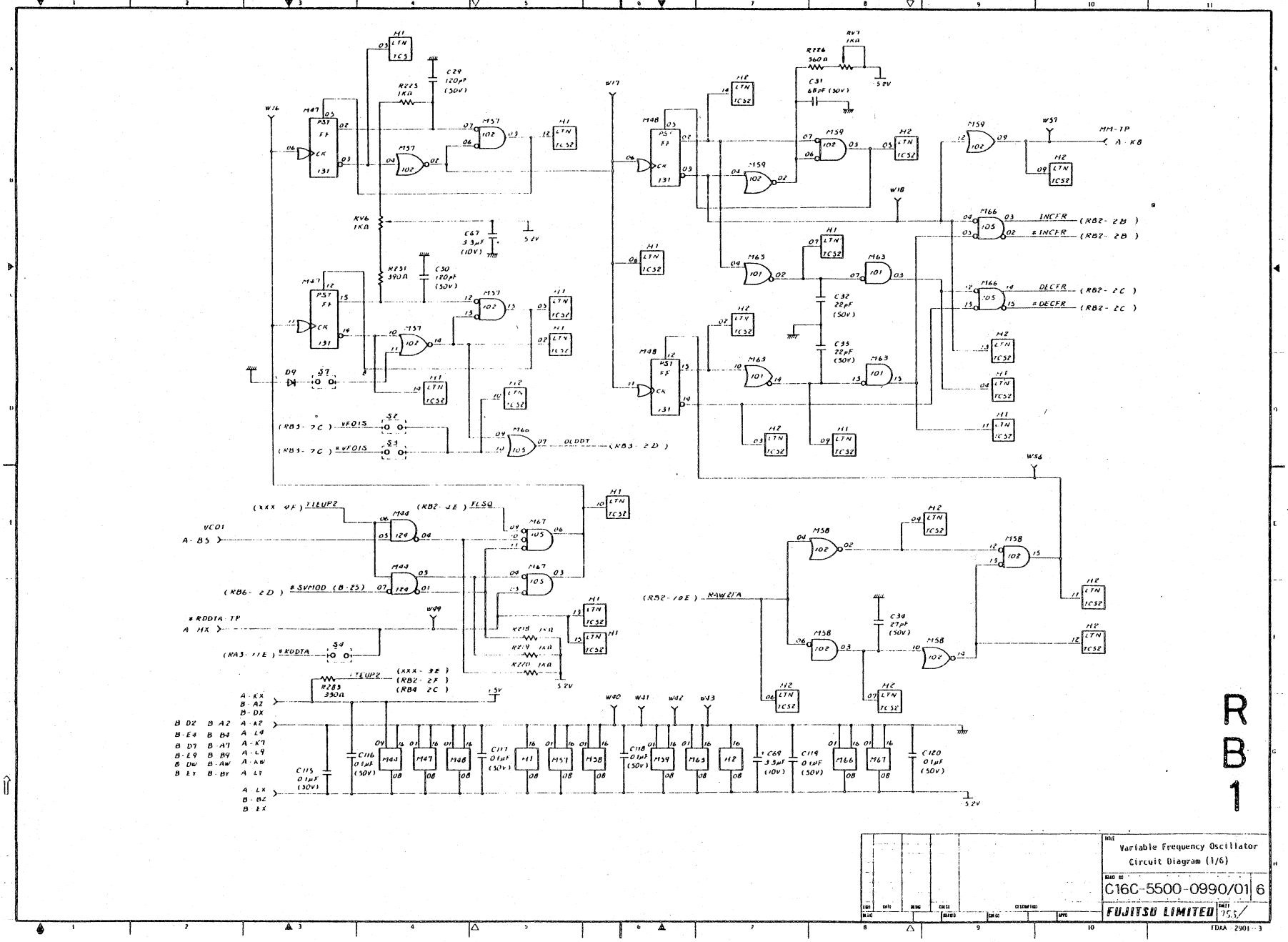

Read Amplifier
Circuit Diagram (1/5)
C16C 5500 0990/01 6
FUJITSU LIMITED
R
A
1

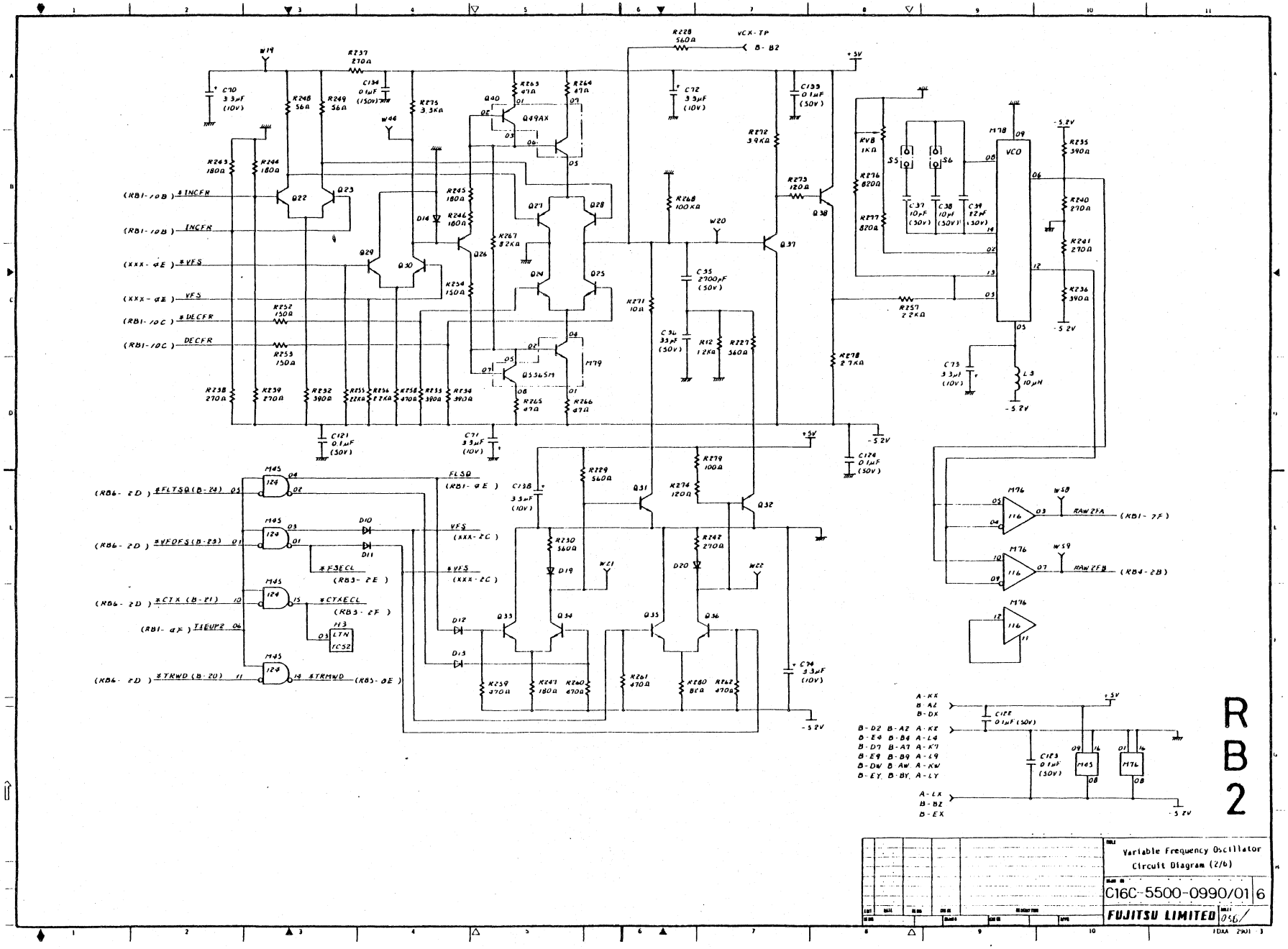

R
A
2
Read Amplifier
Circuit Diagram (2/3)
C16C 5500 0990/01 6
FUJITSU LIMITED

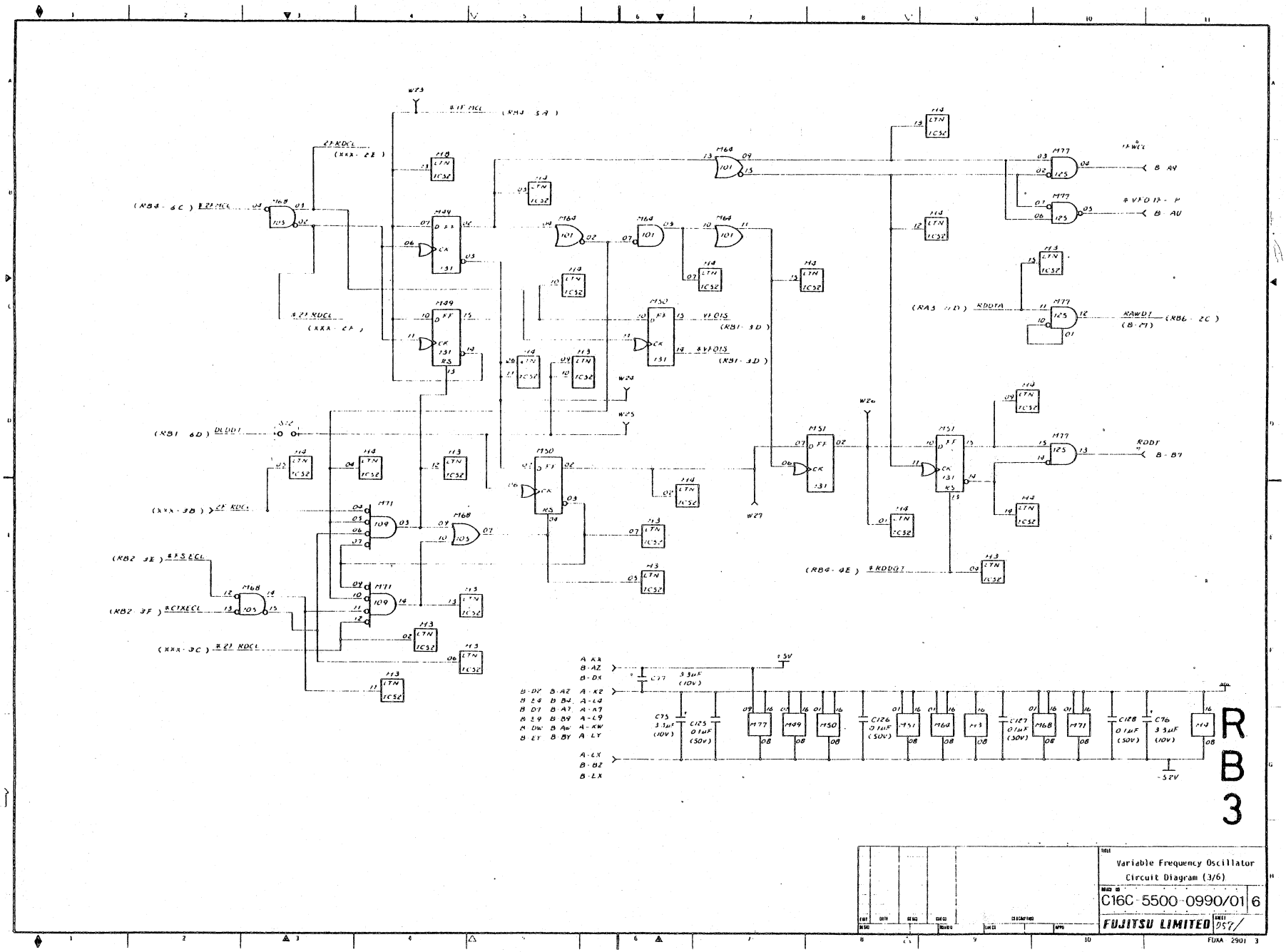

R A 3
Read Amplifier
Circuit Diagram (1/2)
C16C 5500 0990/01 6
FUJITSU LIMITED

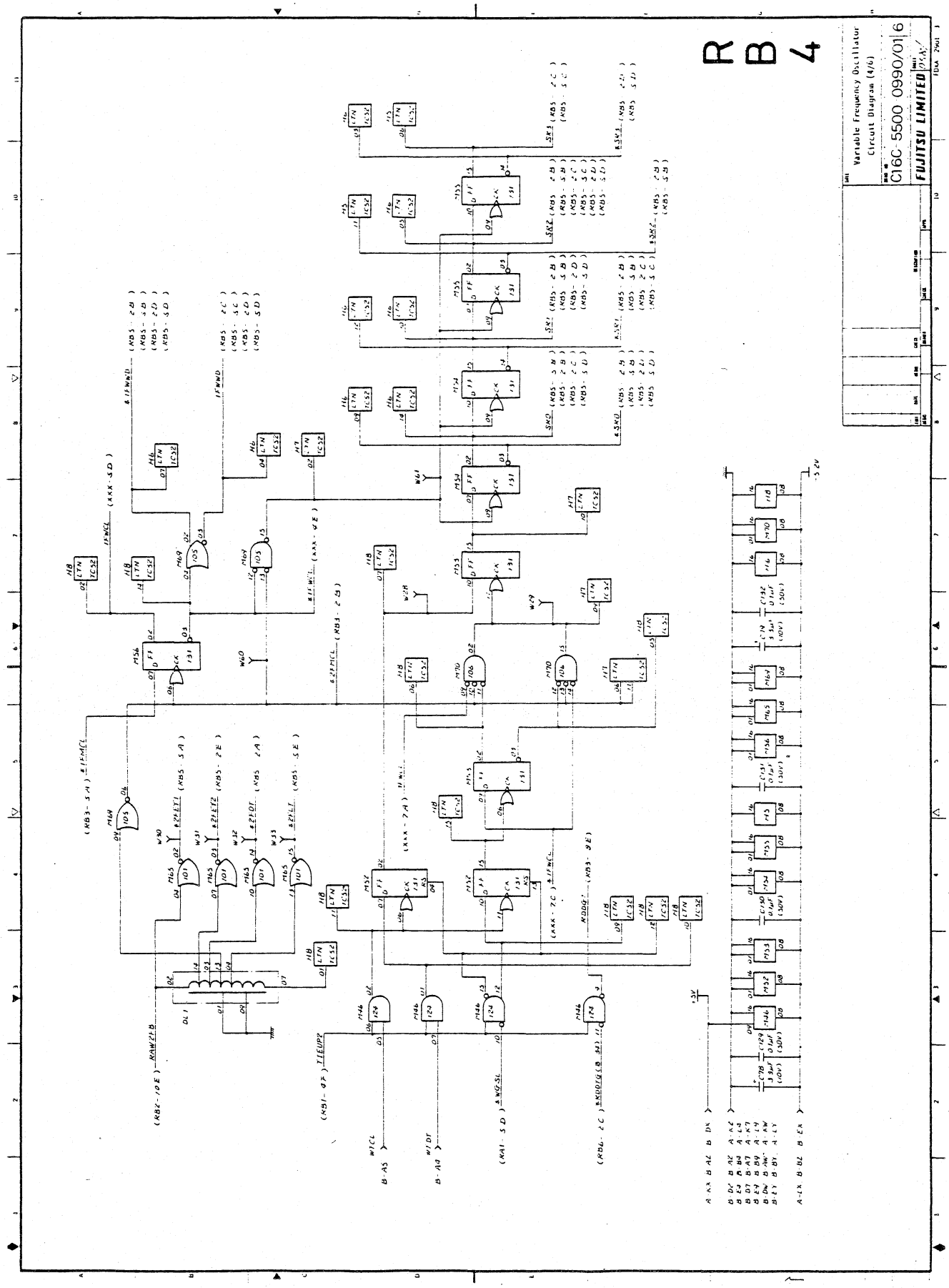

Read Amplifier
Circuit Diagram (4/5)
C16C-5500-0990/01 6
FUJITSU LIMITED
R A 4

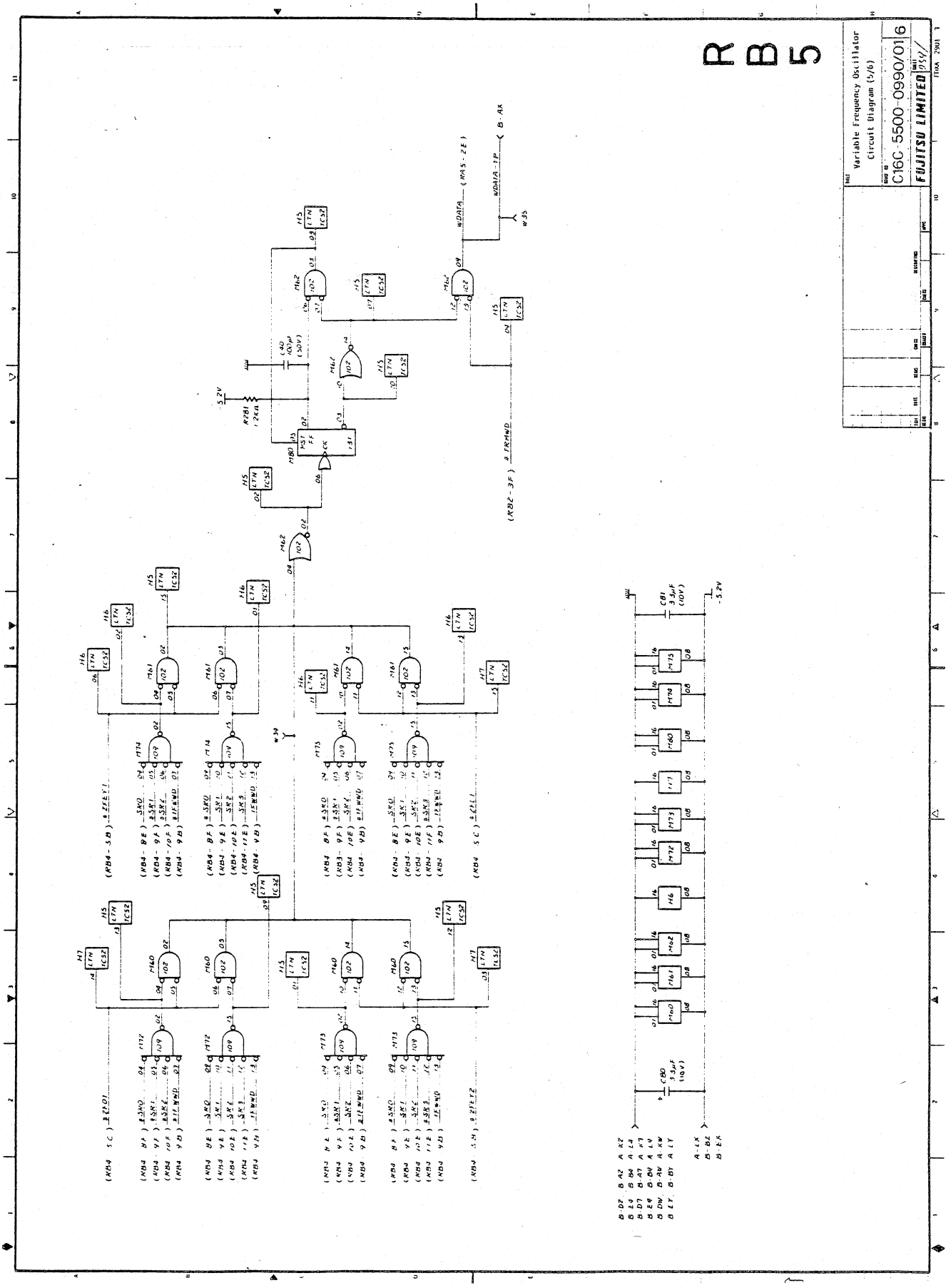

M22
DEC
LS155
M16
LS04
M17
LS08
M18
LS32
M19
LS02
M20
LS86
M21
LS00
M24
LS74
M10
LS74
(RB6-2B) *EHR31(B-37)
(RB6-2C) *EHR63(B-36)
*MYHSL (RA1-3D) (RA4-7C)
*EXH31 A-AY
*EXH63 A-E1
*EXH79 A-D1
*WSLHV (RA1-3D) (RA4-7C)
*WSLFX (RA1-3C) (RA1-7C) (RA4-2B)
*GDIW1 (RA1-3B)
*SLIW (RA1-3C)
*EXHSL (RA1-3D)
DLIW1 (RA1-9C)
DLIW2 (RA1-11E)
(RA1-3D) *WGSL
(RA4-6A) HDSHIT
(RA4-8F) *HAK1
(RA1-4E) *RGCTL
(RB5-10D) WDATA
WDATA-TP
*WTDT (RA1-5A)
(B-29) DIECK (RB6-2C)
R194 560Ω
R195 560Ω
-5.2V
+12V
+5V
C109 0.022μF (50V)
C50 47μF (25V)
R209 51Ω
R210 51Ω
R196 110Ω
R197 22Ω
R198 22Ω
R199 22Ω
R200 22Ω
R201 22Ω
R202 22Ω
R203 22Ω
R204 22Ω
R205 22Ω
R206 22Ω
R208 22Ω
Q18
Q19
Q20
Q21
R213 56Ω
R214 56Ω
R215 56Ω
C110 0.022μF (50V)
D18
D8
R5 100Ω
R211 390Ω
R212 3.3kΩ
C46 3.3μF (10V)
C63 3.3μF (10V)
C111 0.022μF (50V)
C112 0.022μF (50V)
C113 0.022μF (50V)
C114 0.022μF (50V)
A-A1
A-Q1
A-A2
A-Q2
A-Q2 A-D2 A-A2
A-H4 A-E3 A-B4
A-Q7 A-D7 A-A1
A-H9 A-E9 A-B9
A-QW A-DW A-AW
A-HT A-ET A-BY
A-B2
A-H2
RA5
Read Amplifier
Circuit Diagram (5/5)
C16C-5500-0990/01 6
FUJITSU LIMITED

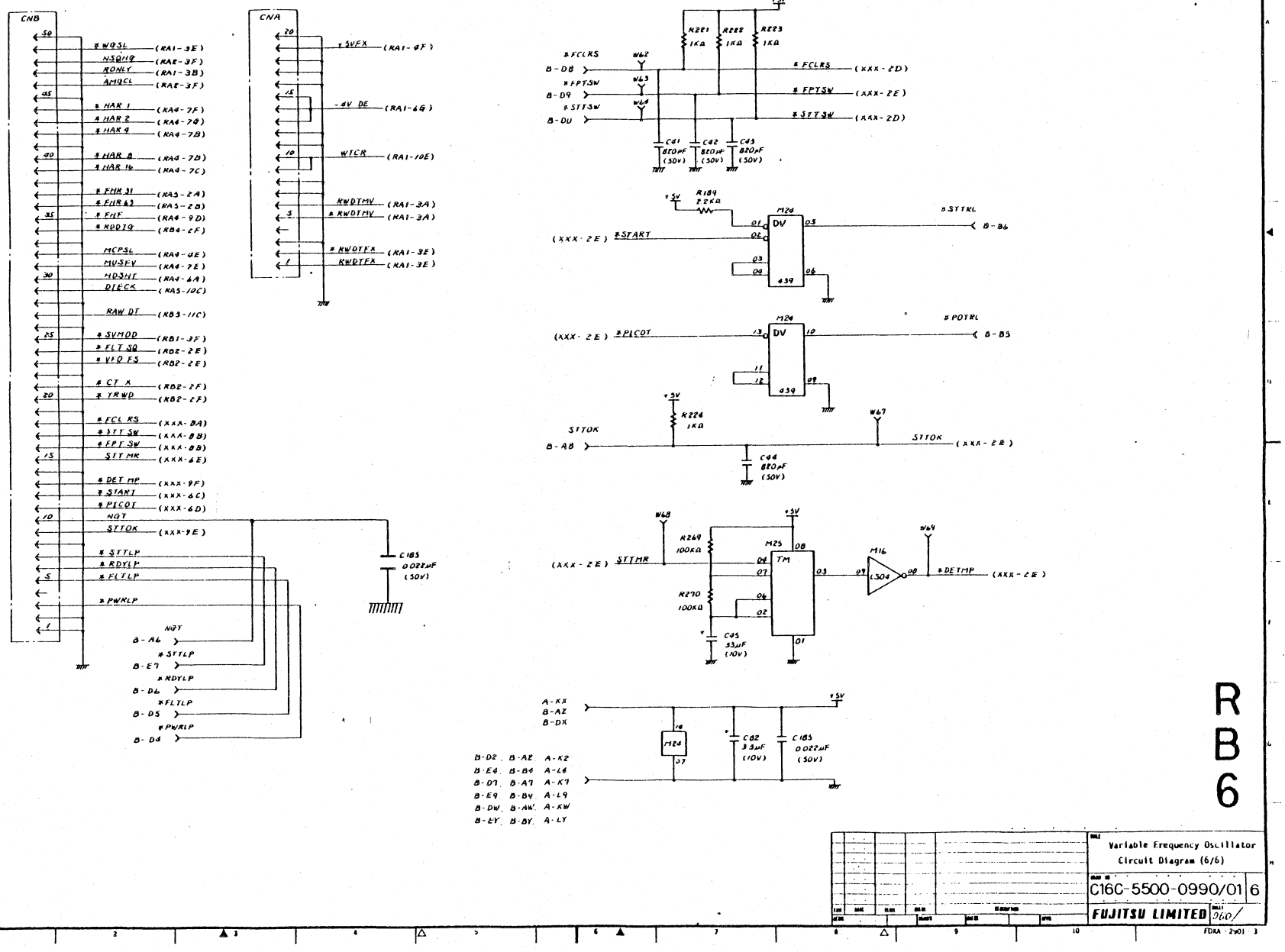

Variable Frequency Oscillator
Circuit Diagram (1/6)
C16C-5500-0990/01 6
FUJITSU LIMITED
FDRA-2901-3
R B 1


Variable Frequency Oscillator
Circuit Diagram (2/6)
C16C-5500-0990/01 6
FUJITSU LIMITED
RB2
VCO
VCX-TP
INCFR
DECFR
VFS
FLSQ
RAW2FA
RAW2FB
+5V
-5.2V


Variable Frequency Oscillator
Circuit Diagram (3/6)
C16C-5500-0990/01 6
FUJITSU LIMITED
RB3
+5V
-5V


Variable Frequency Oscillator
Circuit Diagram (4/6)
C16C-5500-0990/01 6
FUJITSU LIMITED
R
B
4

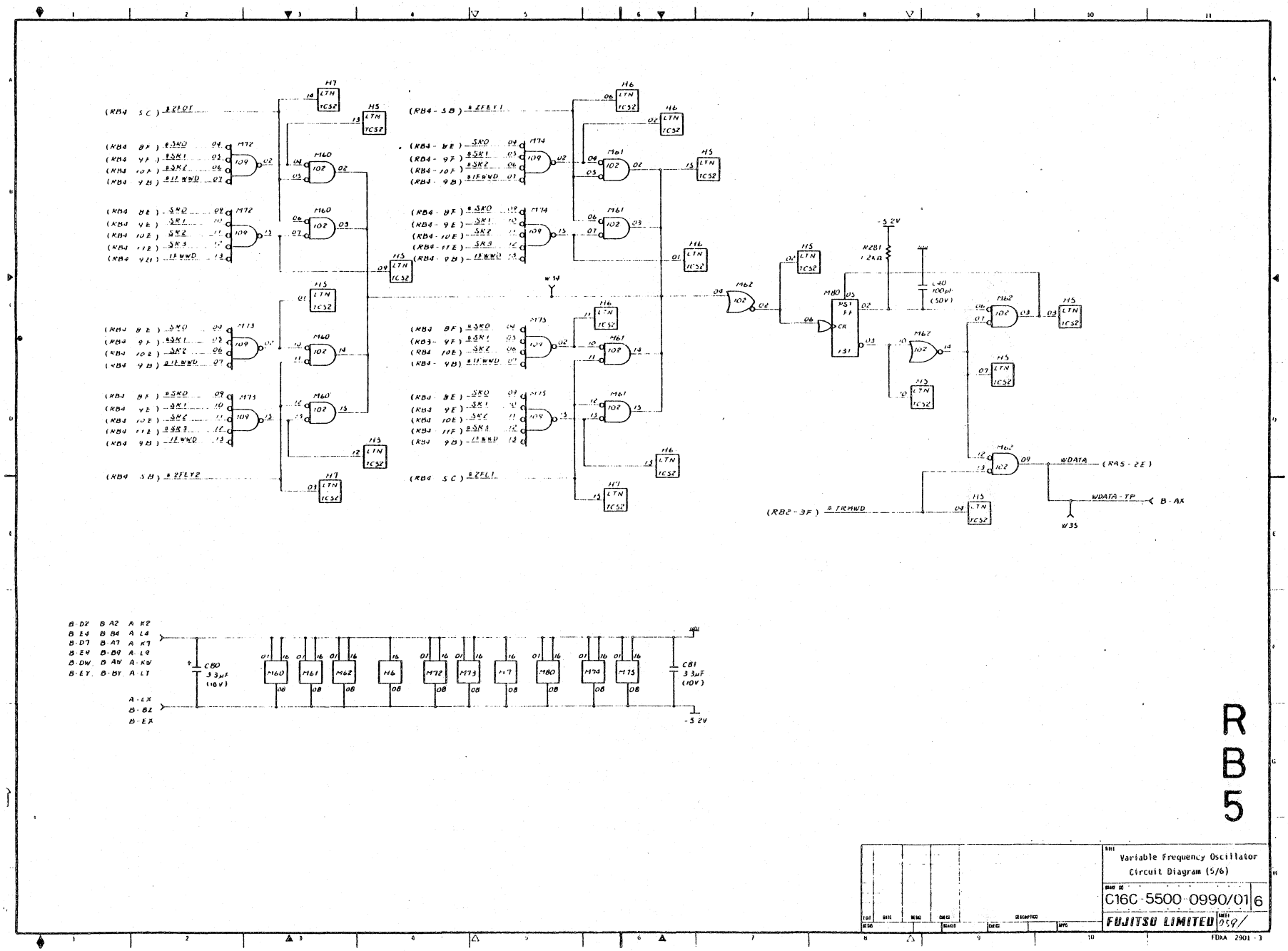

R B 5
Variable Frequency Oscillator
Circuit Diagram (5/6)
C16C-5500-0990/01 6
FUJITSU LIMITED



RB6

Variable Frequency Oscillator Circuit Diagram (6/6)	
C16C-5500-0990/01	6
FUJITSU LIMITED	060/

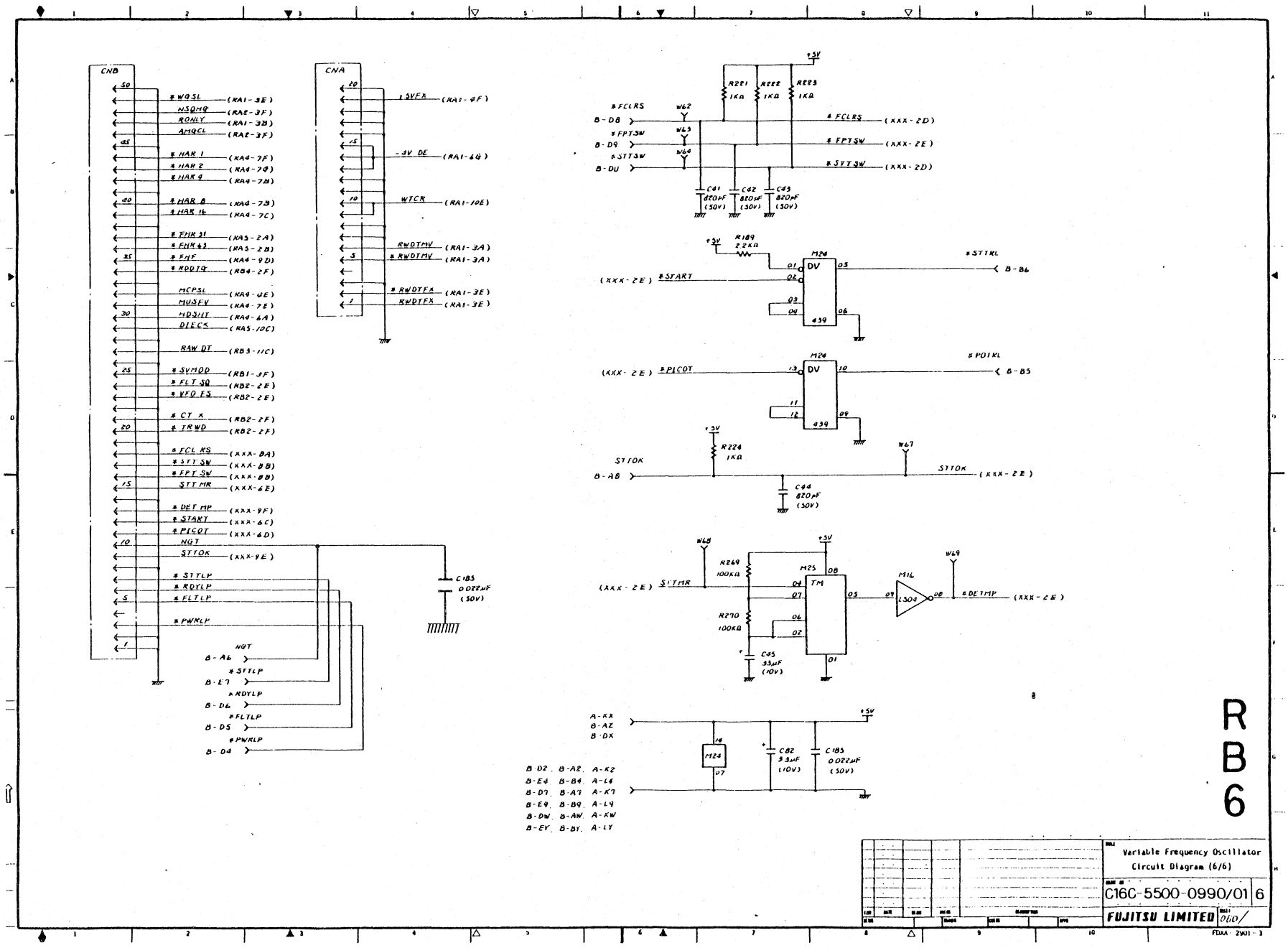
FDAA-2901 3

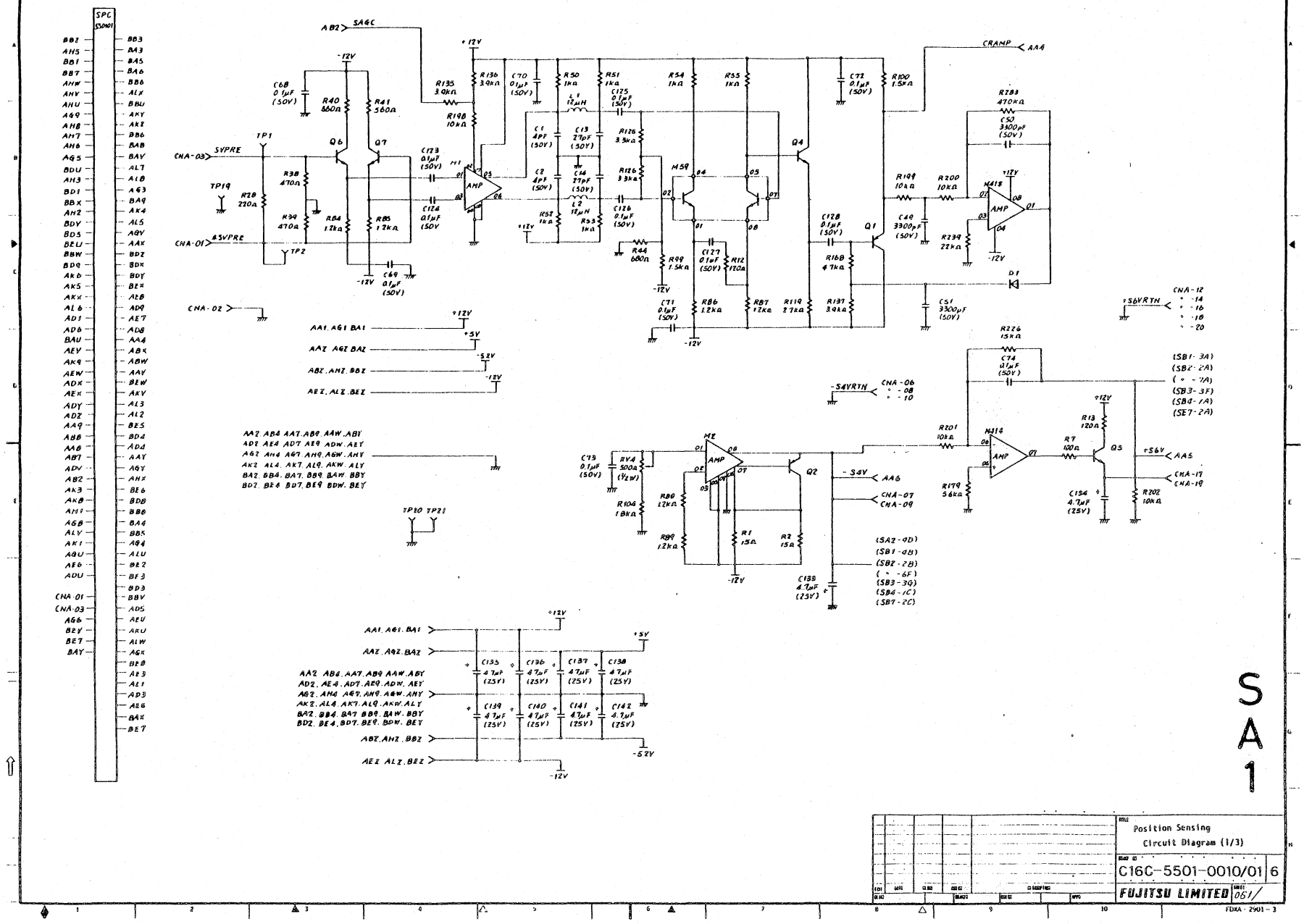


RB5

TITLE	Variable Frequency Oscillator Circuit Diagram (5/6)
DRAWING NO	C16C-5500-0990/01 6
FUJITSU LIMITED	SHEET 059/

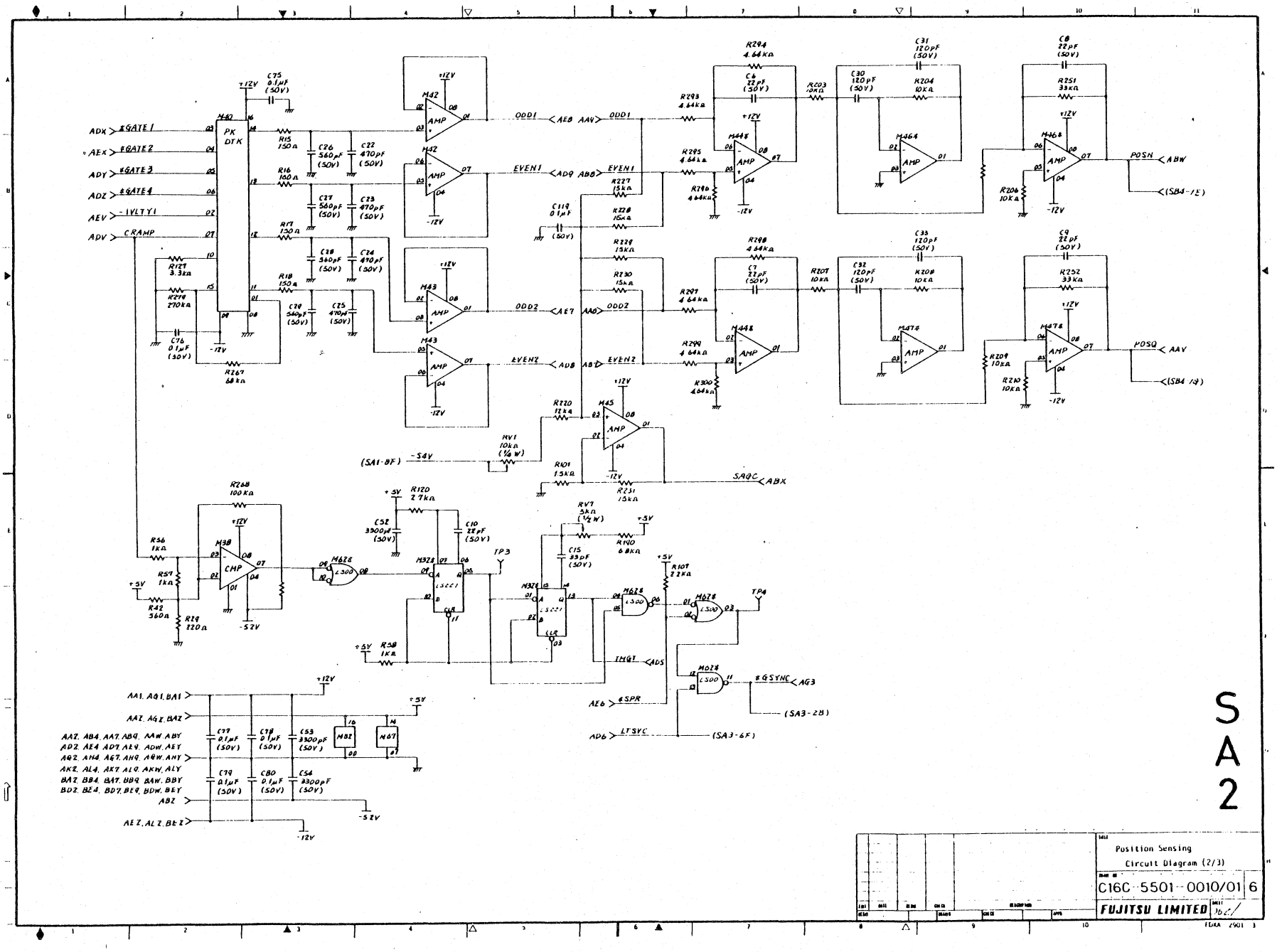
FDXA 2901-3

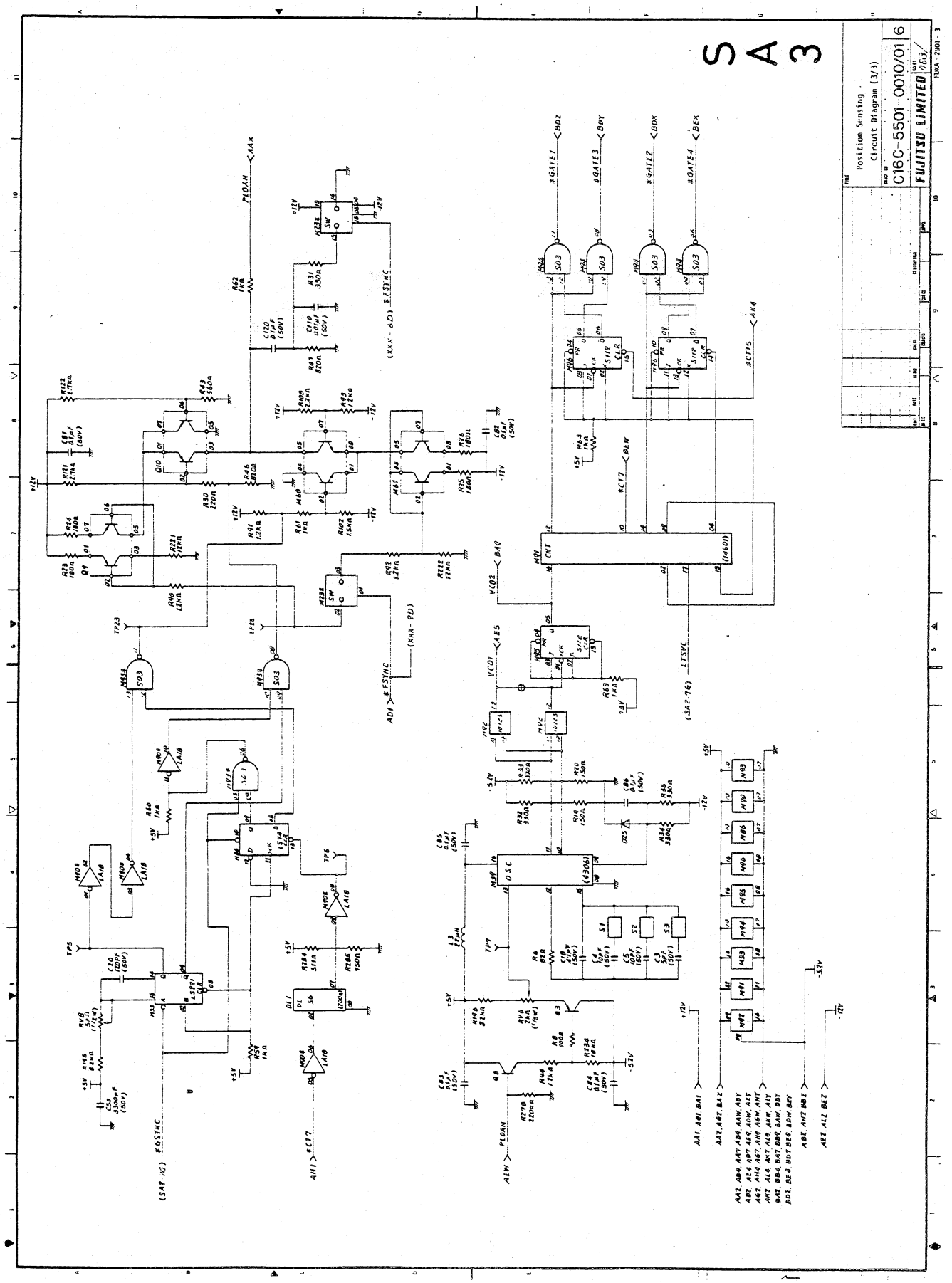

CNB
CNA
+5V
R221 1KΩ
R222 1KΩ
R223 1KΩ
W62
W63
W64
C61 820pF (50V)
C62 820pF (50V)
C63 820pF (50V)
R189 22KΩ
M124
DV
439
R224 1KΩ
W67
C64 820pF (50V)
W68
W69
R269 100KΩ
R270 100KΩ
C65 33μF (10V)
M25
TM
M16
LS04
C82 33μF (10V)
C183 0.022μF (50V)
C185 0.022μF (50V)
RB6
Variable Frequency Oscillator
Circuit Diagram (6/6)
C16C-5500-0990/01 6
FUJITSU LIMITED
FDXA-2901-3

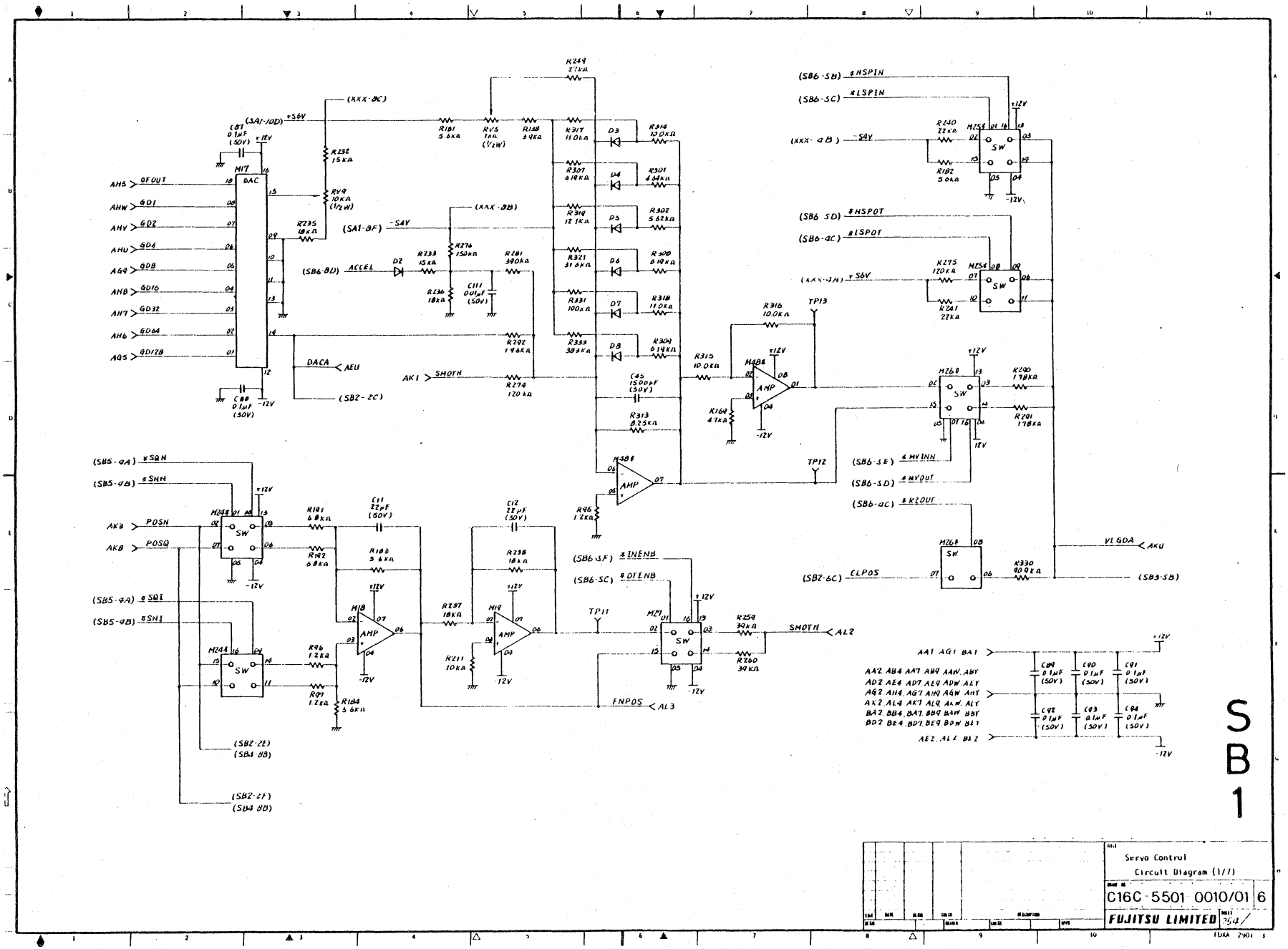


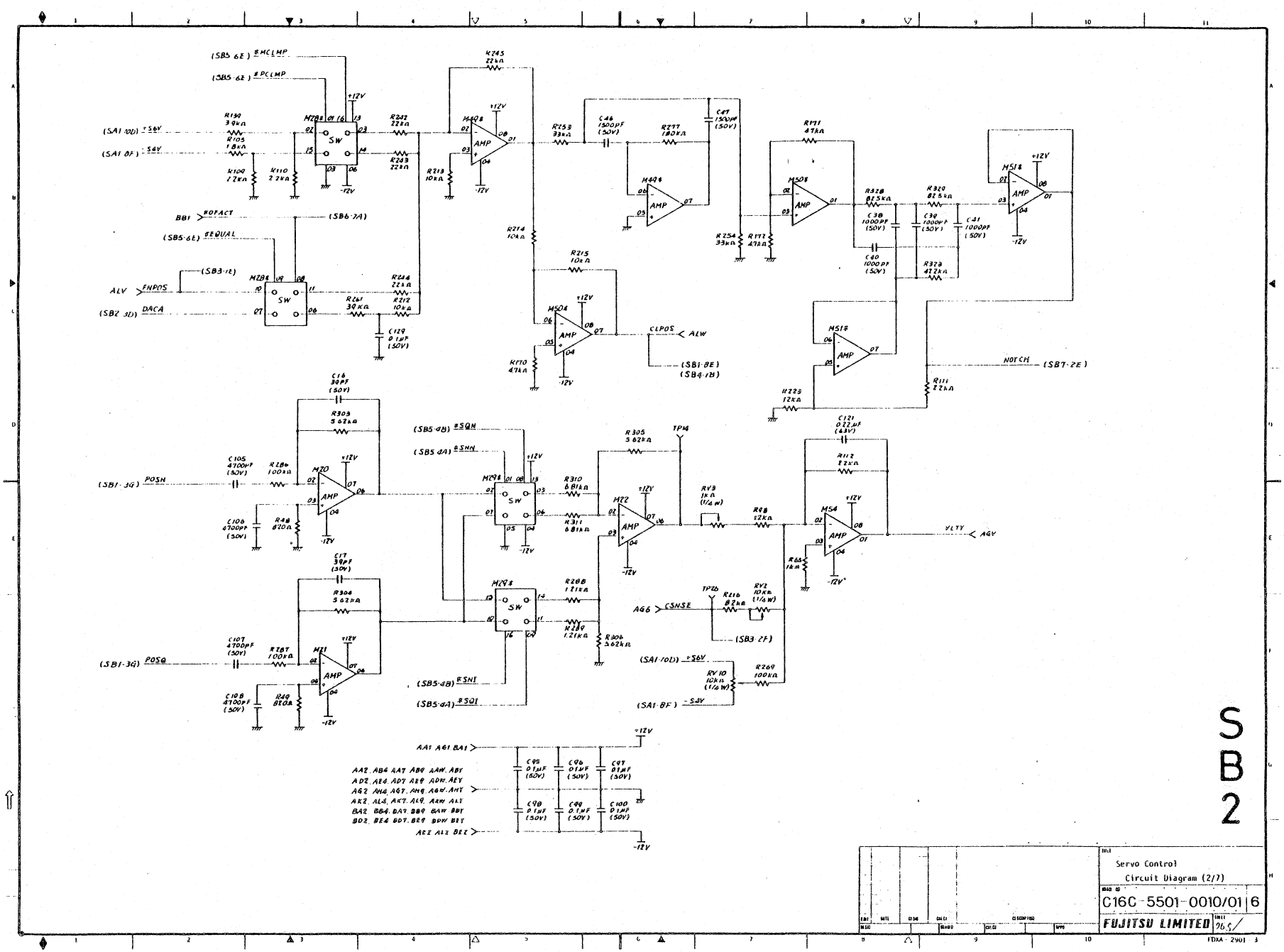
TITLE	Position Sensing Circuit Diagram (1/3)
BOARD ID	C16C-5501-0010/01 6
	FUJITSU LIMITED
SHEET	051/

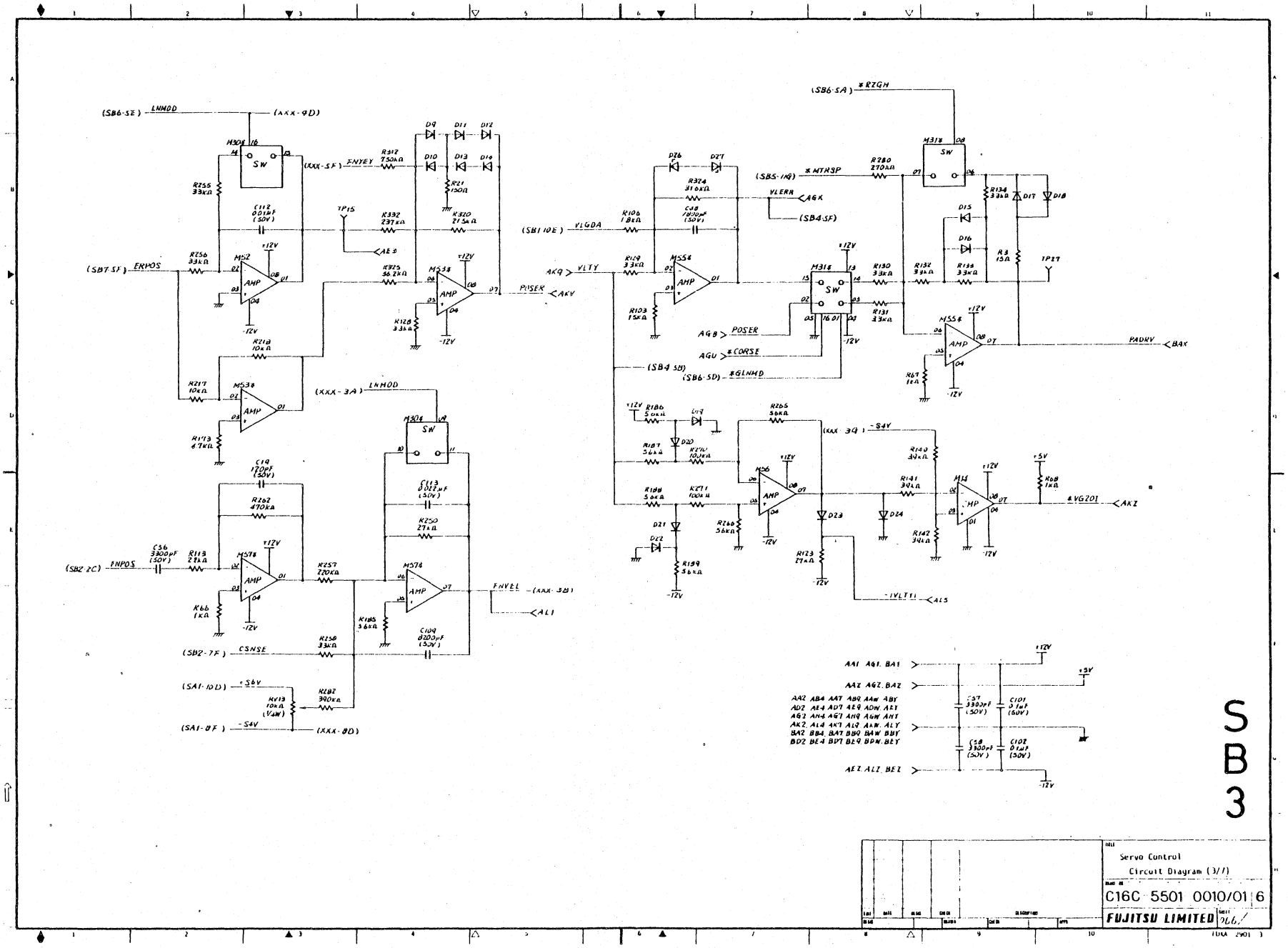
FDKA-2901-3


ADX
AEX
ADY
ADZ
AEV
ADV
*GATE1
*GATE2
*GATE3
*GATE4
-IVLTY1
CRAMP
PK DTK
+12V
-12V
+5V
-5V
ODD1
EVEN1
ODD2
EVEN2
POSN
POSQ
ABW
AAV
ABX
SA0C
(SB4-1E)
(SB4-1F)
(SB4-1H)
(SA1-8F)
-54V
TP3
TP4
IMGT
ADS
*SPR
AE6
AD6
LTSYC
*GSYNC
AG3
(SA3-2B)
(SA3-6F)
AA1, AB1, BA1
AA2, AB2, BA2
ABZ
AEZ, ALZ, BEZ
SA2
Position Sensing
Circuit Diagram (2/3)
C16C-5501-0010/01
6
FUJITSU LIMITED


SA3
Position Sensing
Circuit Diagram (3/3)
C16C-5501-0010/01 6
FUJITSU LIMITED


Servo Control
Circuit Diagram (1/7)
C16C-5501 0010/01 6
FUJITSU LIMITED
SB1
DAC
SW
AMP
(SA1-10D) +56V
(XXX-8C)
(SA1-8F) -54V
(XXX-8B)
(SB6-8D) ACCEL
AK1 SMOTH
DACA AEU
(SB2-2C)
AH5 DFOUT
AHW GD1
AHV GD2
AHU GD4
AGQ GD8
ANB GD16
AH7 GD32
AH6 GD64
AG5 GD128
(SB6-5B) *HSPIN
(SB6-5C) *LSPIN
(XXX-8B) -54V
(SB6-5D) *HSPOT
(SB6-4C) *LSPOT
(XXX-8A) +56V
TP13
TP12
TP11
(SB6-5E) *MVINN
(SB6-5D) *MVOUT
(SB6-4C) *KZOUT
(SB2-6C) CLPOS
VLGDA AKU
(SB3-5B)
(SB5-4A) *SQN
(SB5-4B) *SNN
AK3 POSN
AK0 POSQ
(SB5-4A) *SQI
(SB5-4B) *SNI
(SB2-2E) (SB3-8B)
(SB2-2F) (SB4-8B)
(SB6-5F) *INENB
(SB6-5C) *OTENB
FNPOS AL3
SMOTH AL2
AA1 AG1 BA1
AE2 AL4 BL2
+12V
-12V


SB2
Servo Control
Circuit Diagram (2/7)
C16C-5501-0010/01 6
FUJITSU LIMITED
FDXA-2901

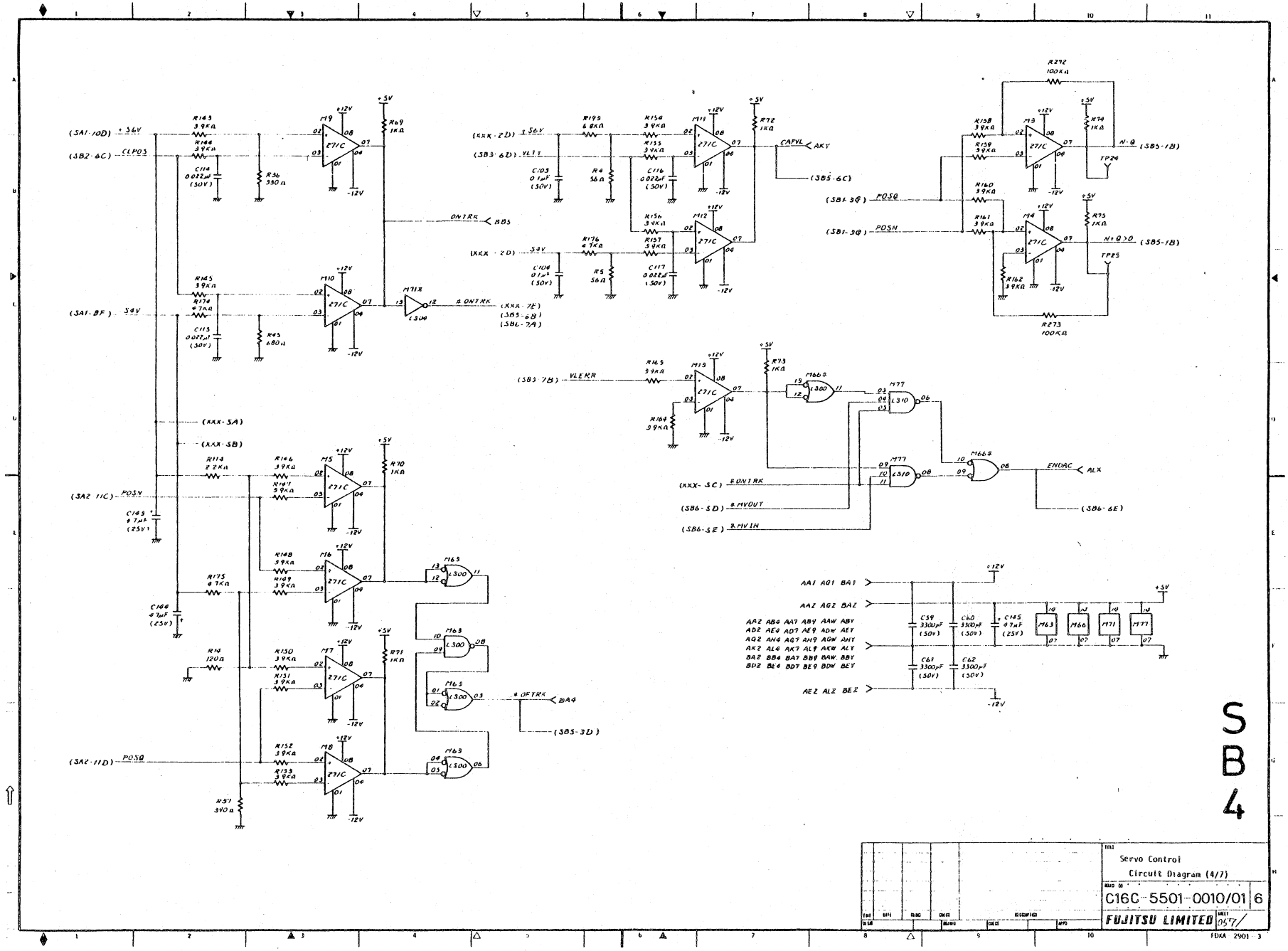


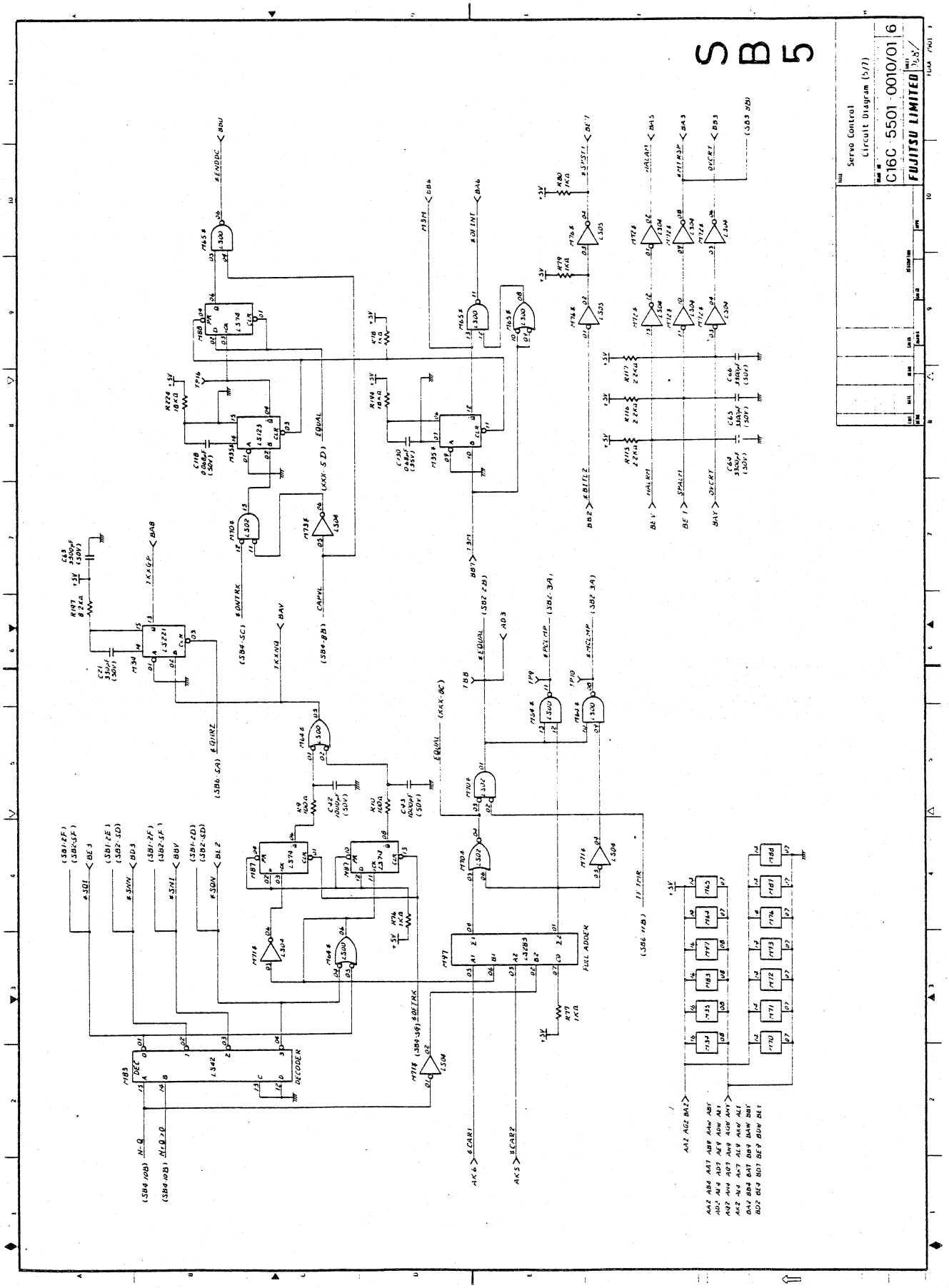
SB3

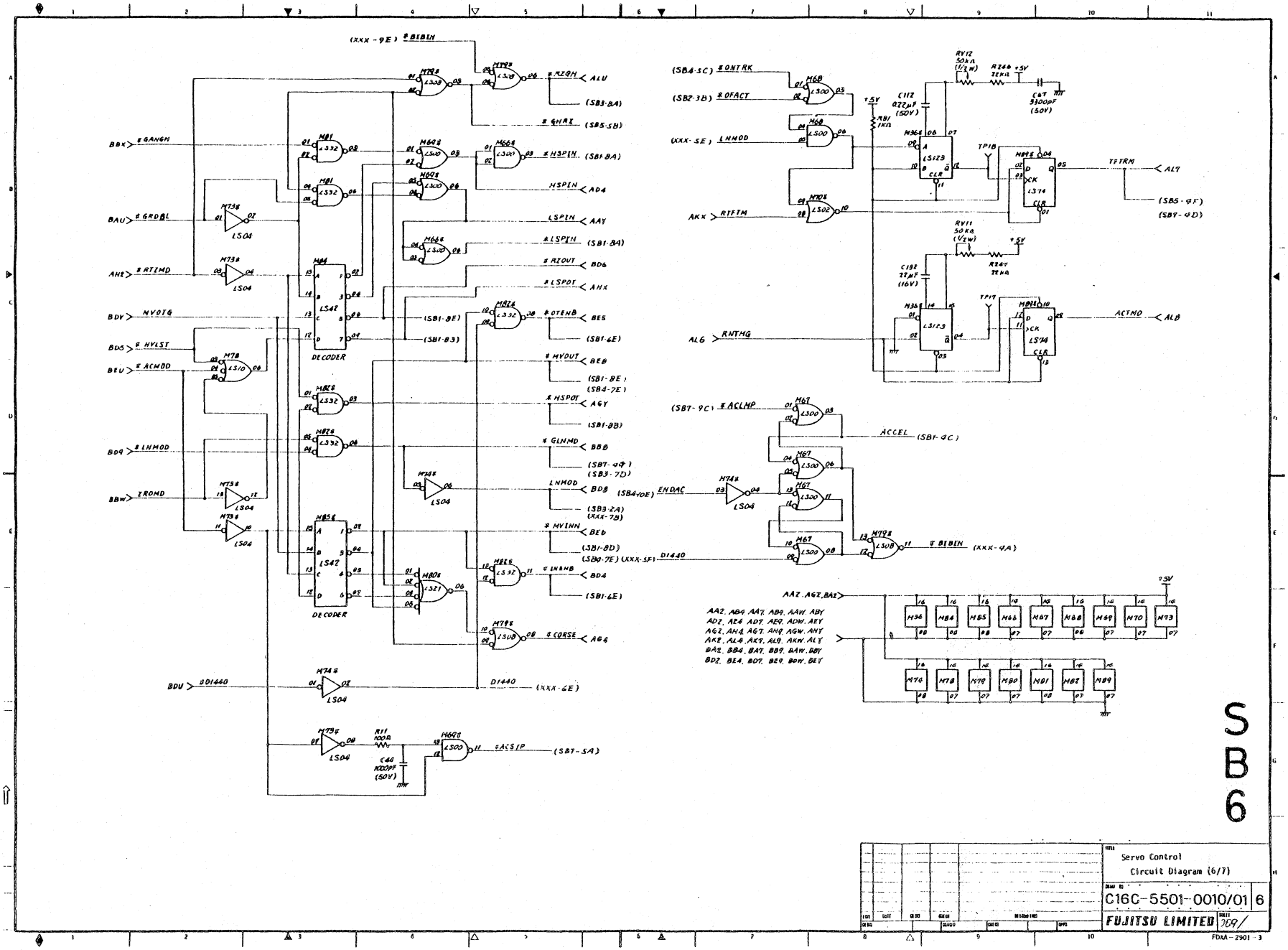
Servo Control
Circuit Diagram (3/7)

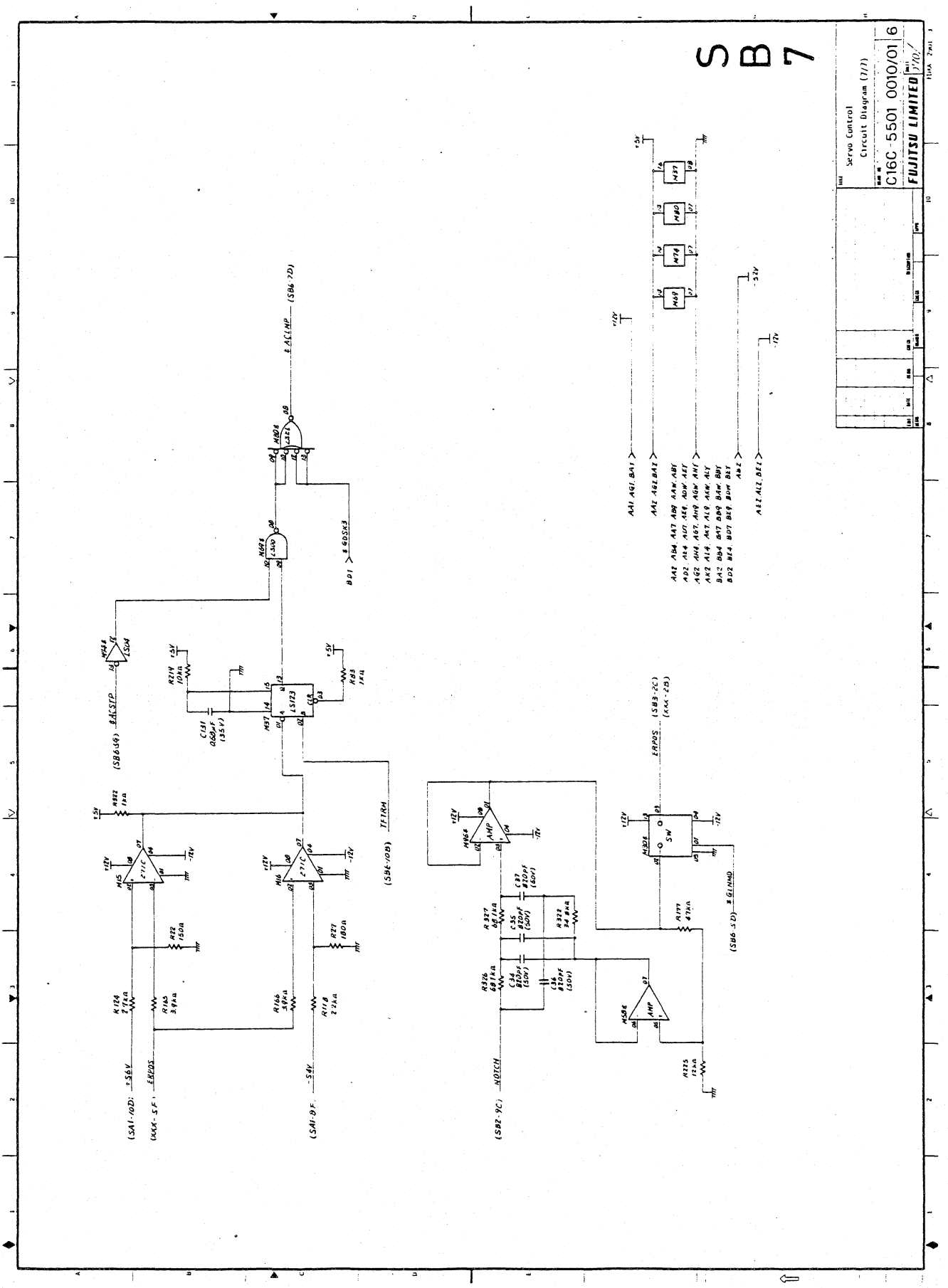
C16C-5501-0010/01 6

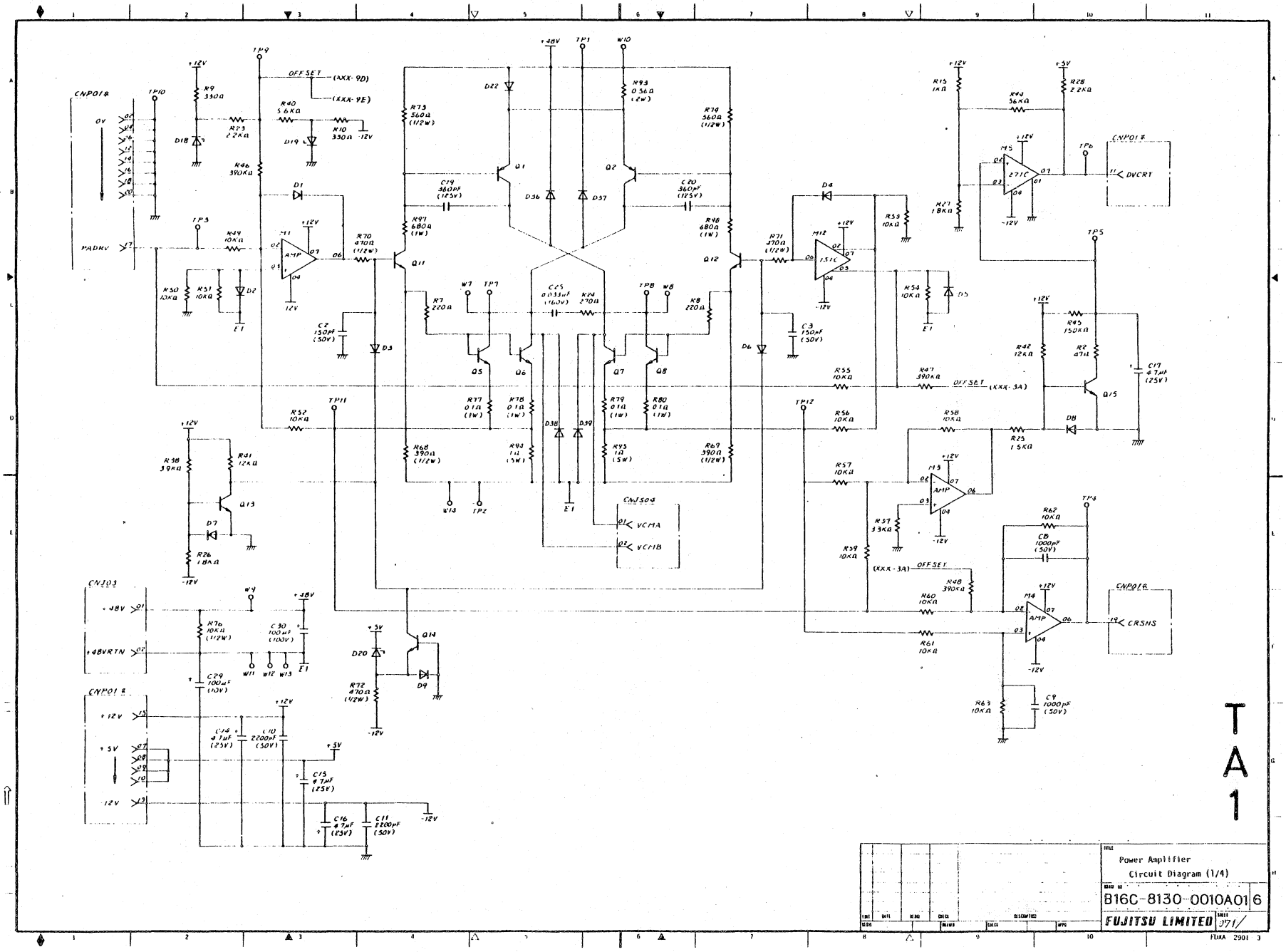
FUJITSU LIMITED

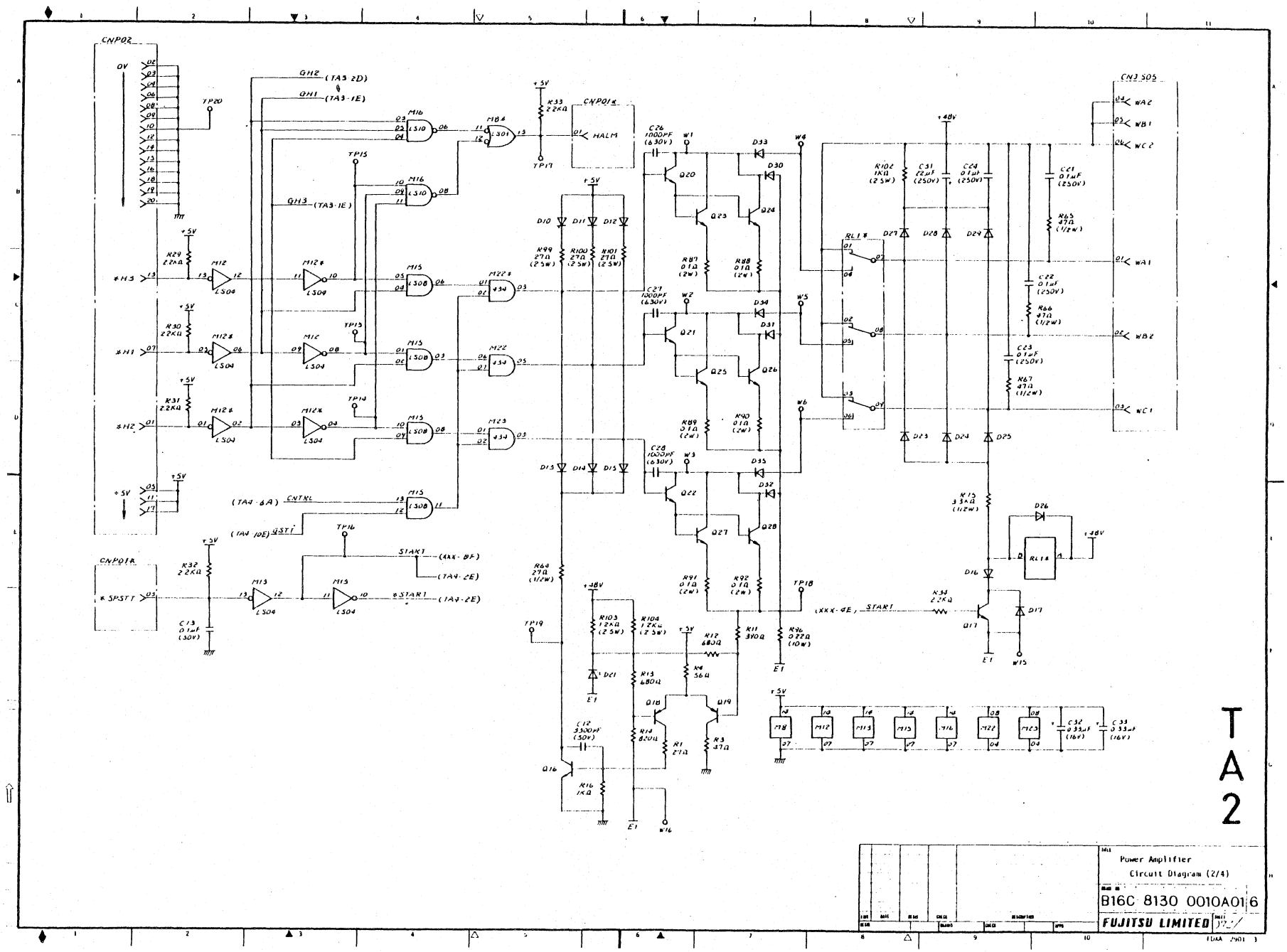

Servo Control
Circuit Diagram (4/7)
C16C-5501-0010/01 6
FUJITSU LIMITED
FDXA 2901-3
SB4

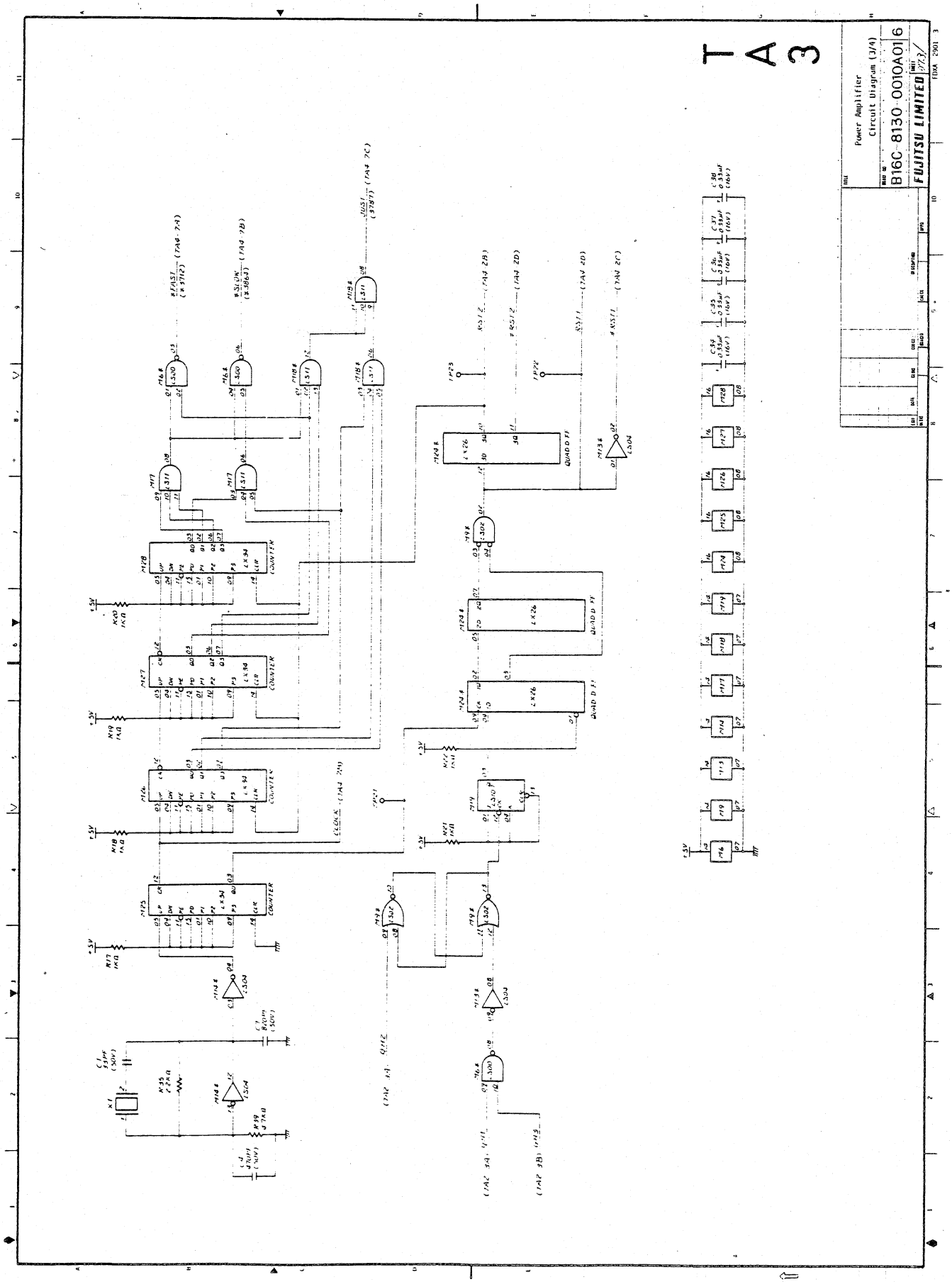

SB5
Servo Control
Circuit Diagram (5/7)
C16C-5501-0010/01 6
FUJITSU LIMITED
DECODER
FULL ADDER
DECODER

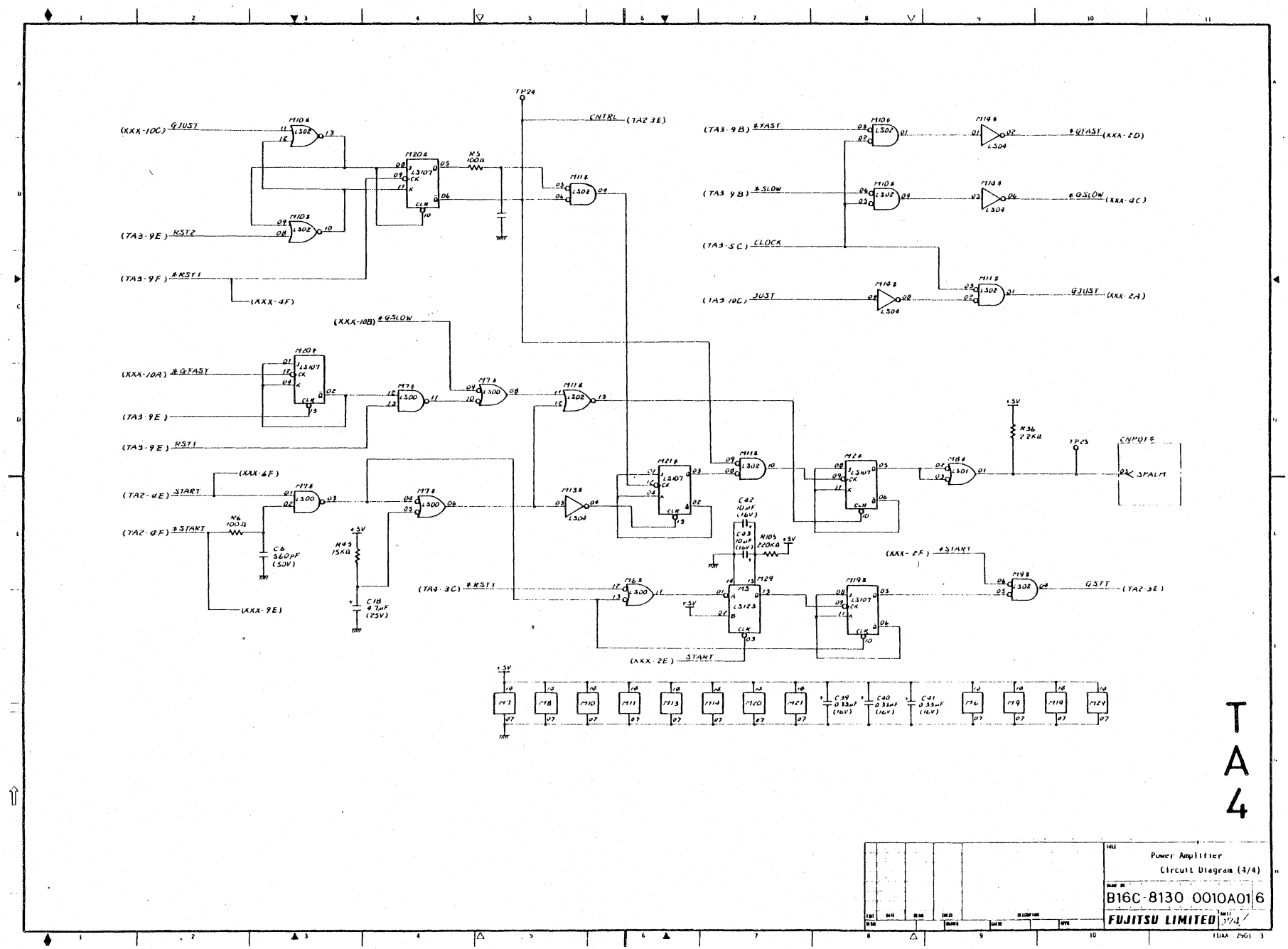

SB6
Servo Control
Circuit Diagram (6/7)
C16C-5501-0010/01 6
FUJITSU LIMITED
FDXA-2901-3
DECODER
DECODER
LS04
LS42
LS32
LS00
LS02
LS08
LS21
LS03
LS123
LS74
LS10
LS27
LS38
LS01
LS04
LS157
LS374
ACCEL (SB1-9C)
ENDAC
D1440
ACTMD
TFTRM
RVI2 50kΩ (1/2W)
RVII 50kΩ (1/2W)
+5V


SB 7
Servo Control
Circuit Diagram (1/1)
C16C-5501 0010/01 6
FUJITSU LIMITED


Power Amplifier
Circuit Diagram (1/4)
B16C-8130-0010A01 6
FUJITSU LIMITED
TA1


CNP02
CNP01A
CNP01B
CNJ505
TA2
Power Amplifier
Circuit Diagram (2/4)
B16C 8130 0010A01 6
FUJITSU LIMITED


TA3
Power Amplifier
Circuit Diagram (1/4)
B16C-8130-0010A01
FUJITSU LIMITED

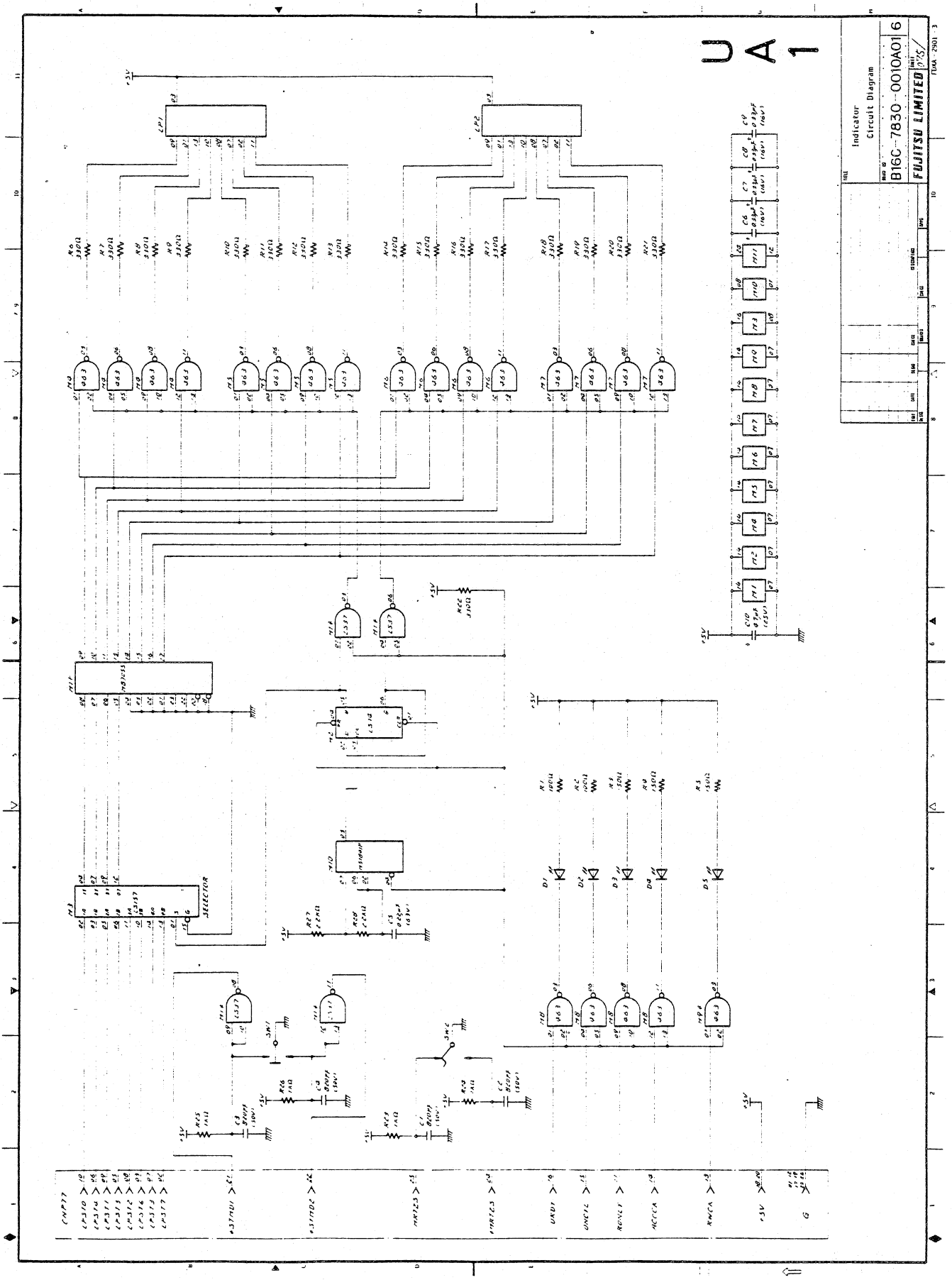


T
A
4

Power Amplifier
Circuit Diagram (4/4)

B16C-8130 0010A01 6

FUJITSU LIMITED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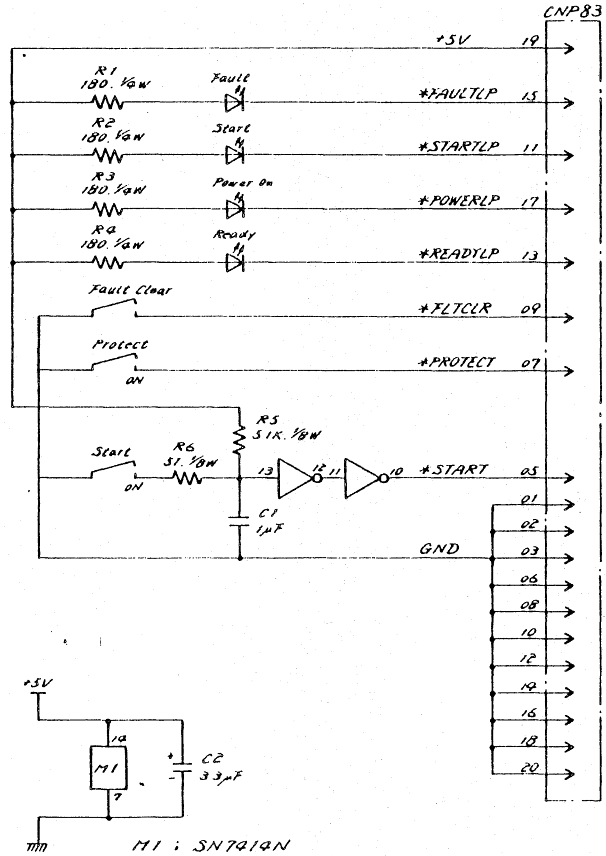

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Operator Panel
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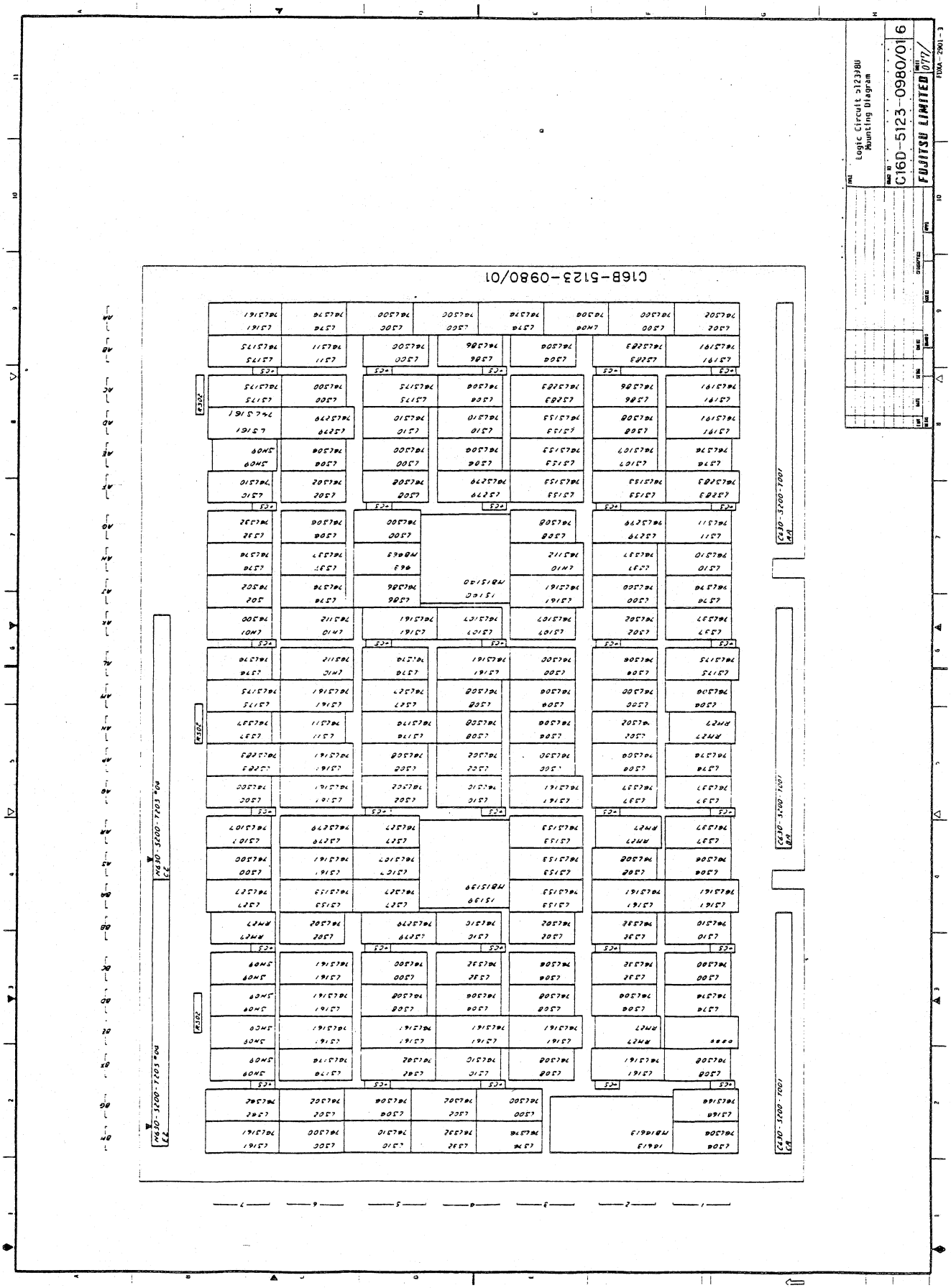
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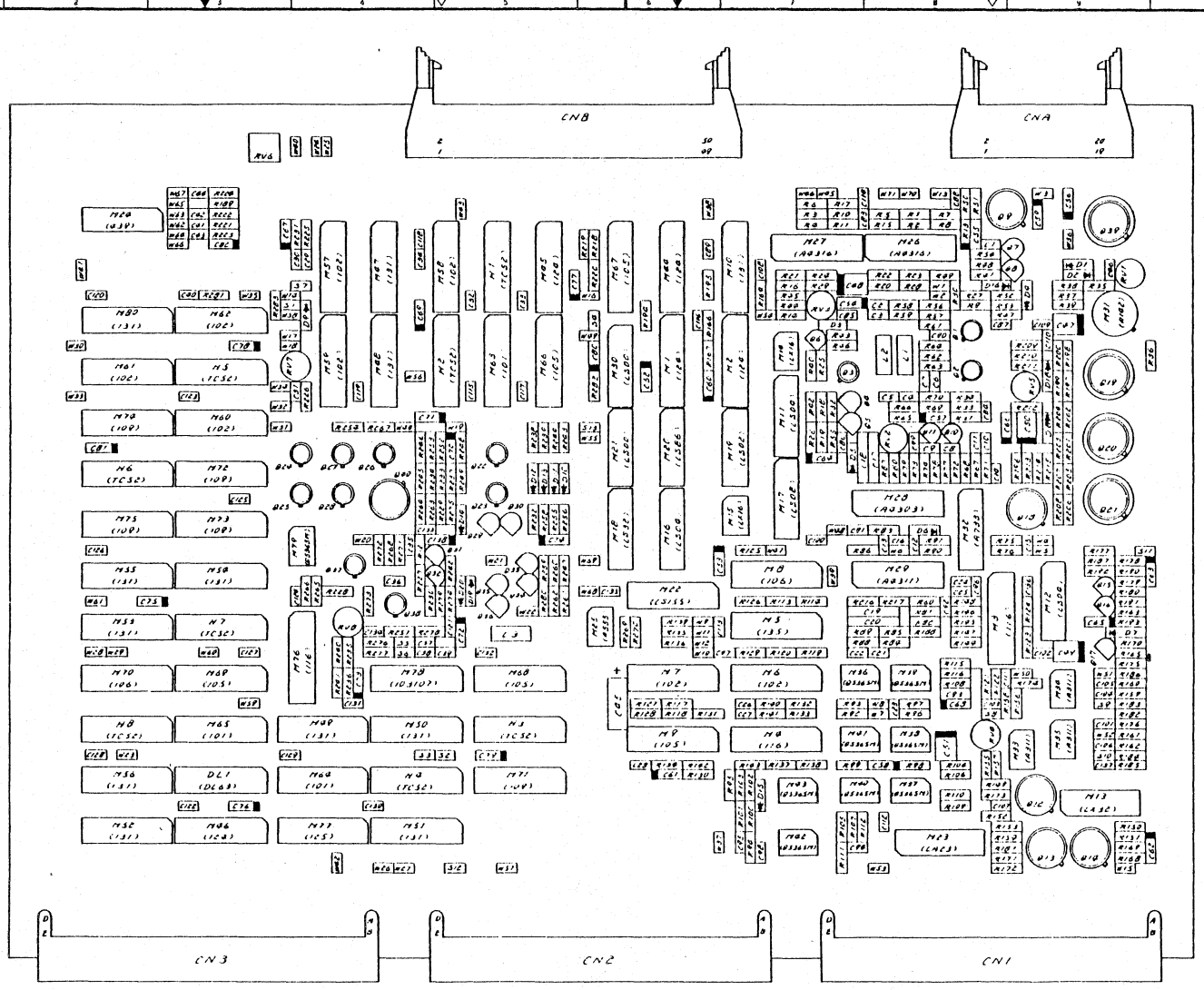
C16D-5123-0980/01
FUJITSU LIMITED



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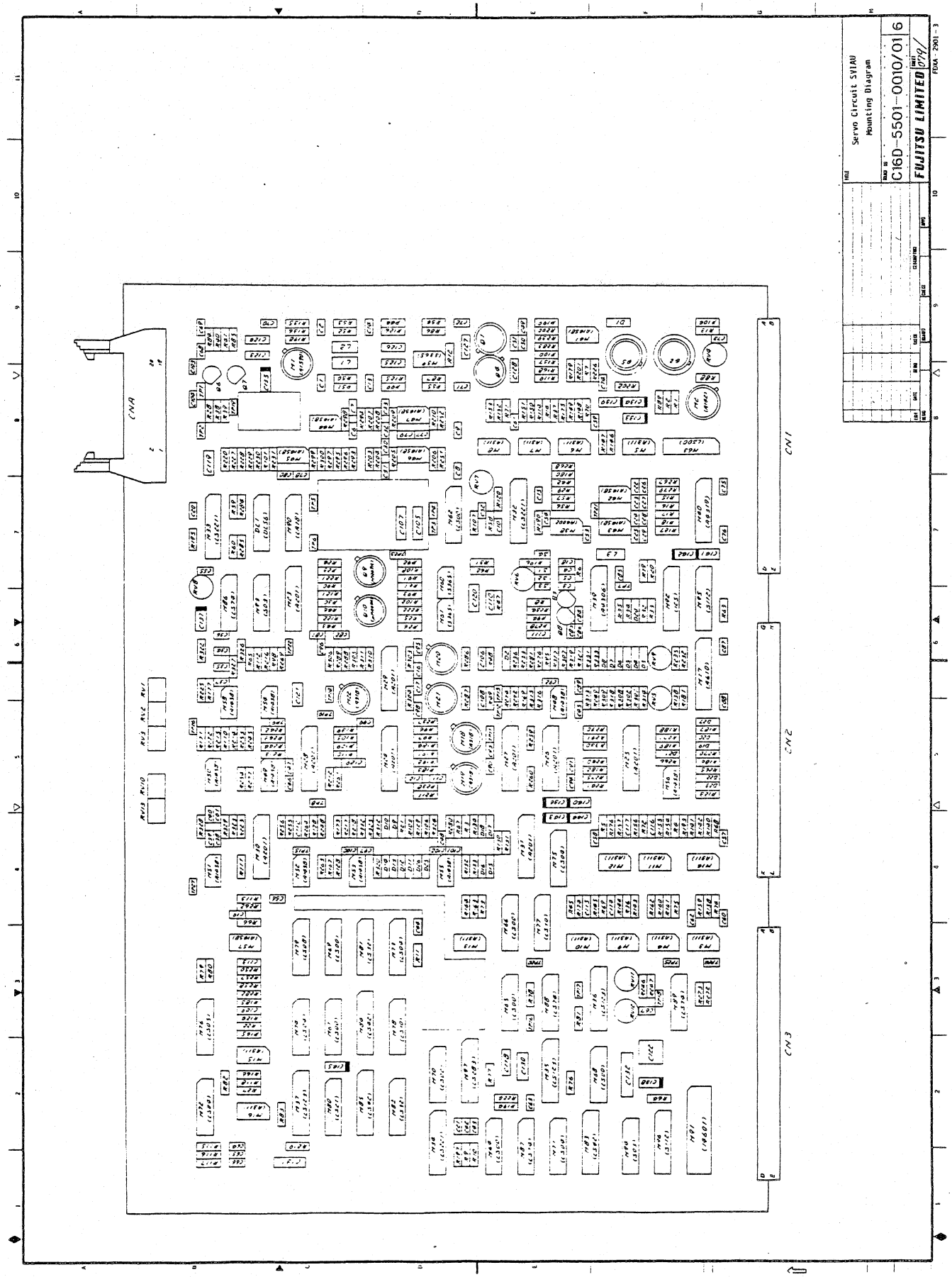
DWG NO	C16D-5500-0990/016
	FUJITSU LIMITED
SHEET	018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Mounting Diagram
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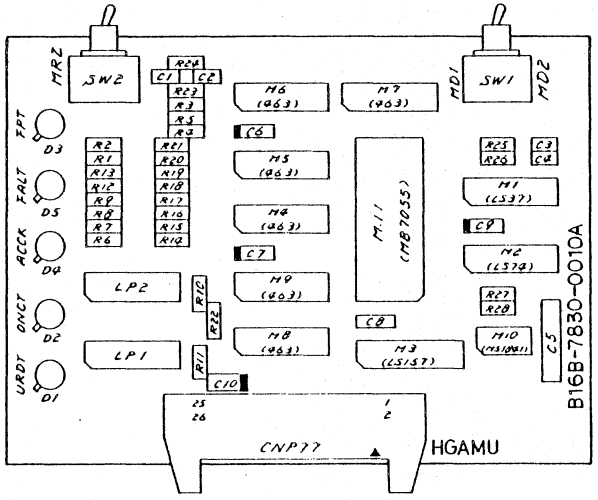
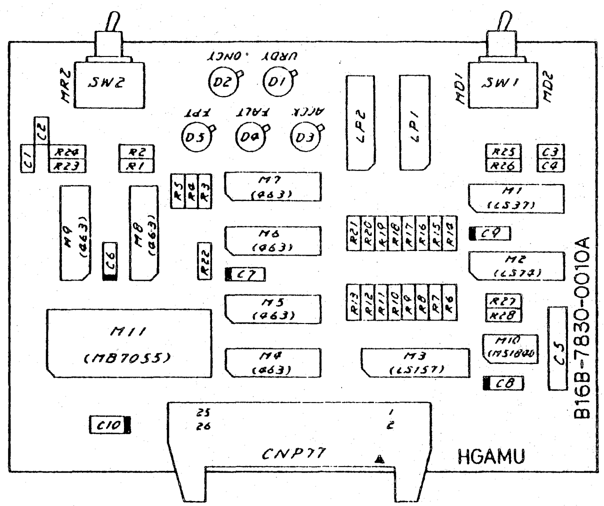
6
FUJITSU LIMITED
CN1
CN2
CN3
CN4



					Indicator Circuit HGAMU Mounting Diagram
					B16D-7830-0010A01 6
					FUJITSU LIMITED SHEET 350/

B03P-4655-0001A...B



Indicator Circuit HGAMU

Mounting Diagram

EDIT	DATE	DESIG	CHECK	DESCRIPTION
DESIG		DRAWN	CHECK	APPD

DRAW NO B16D-7830-0010A02 6

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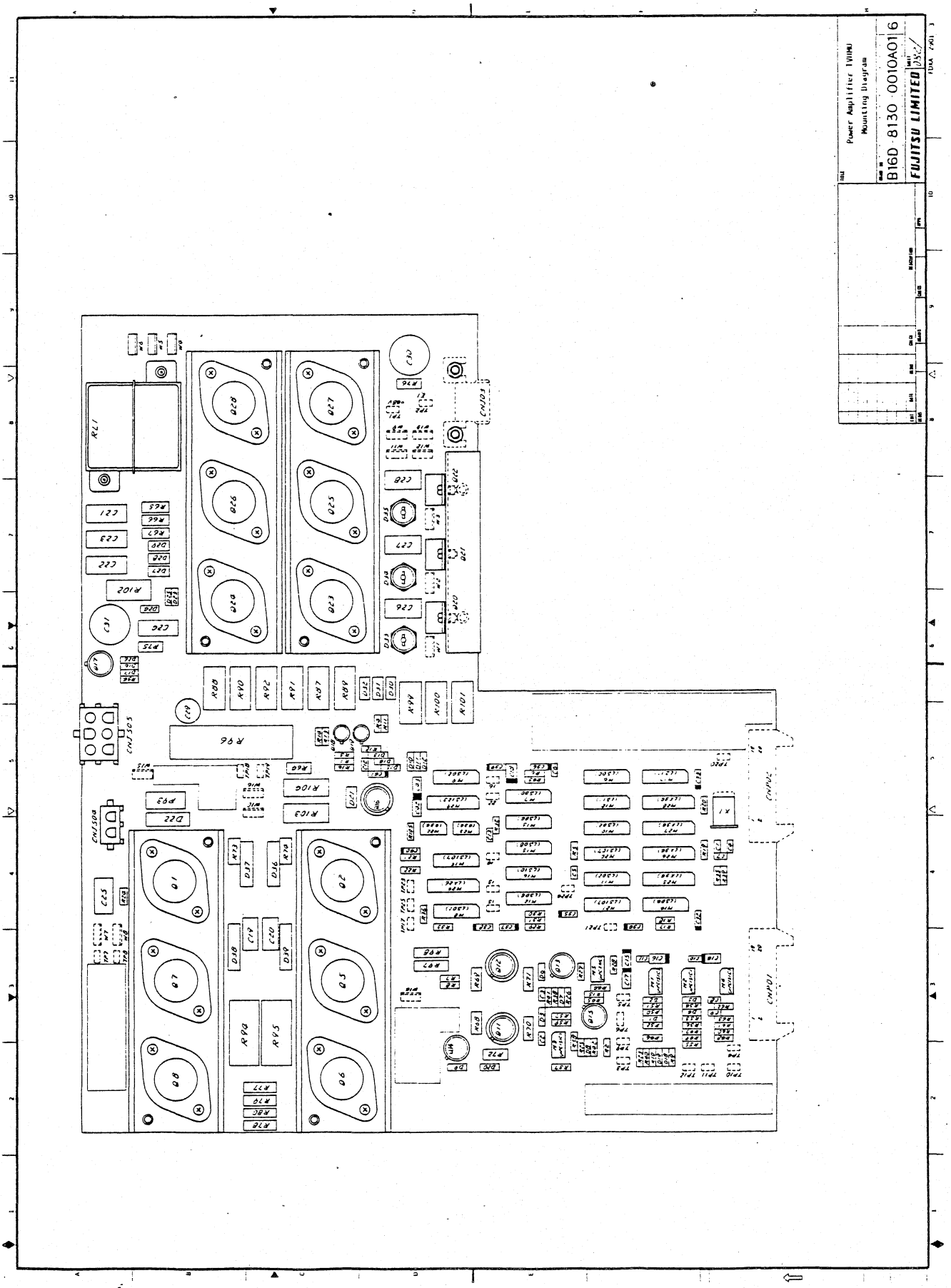
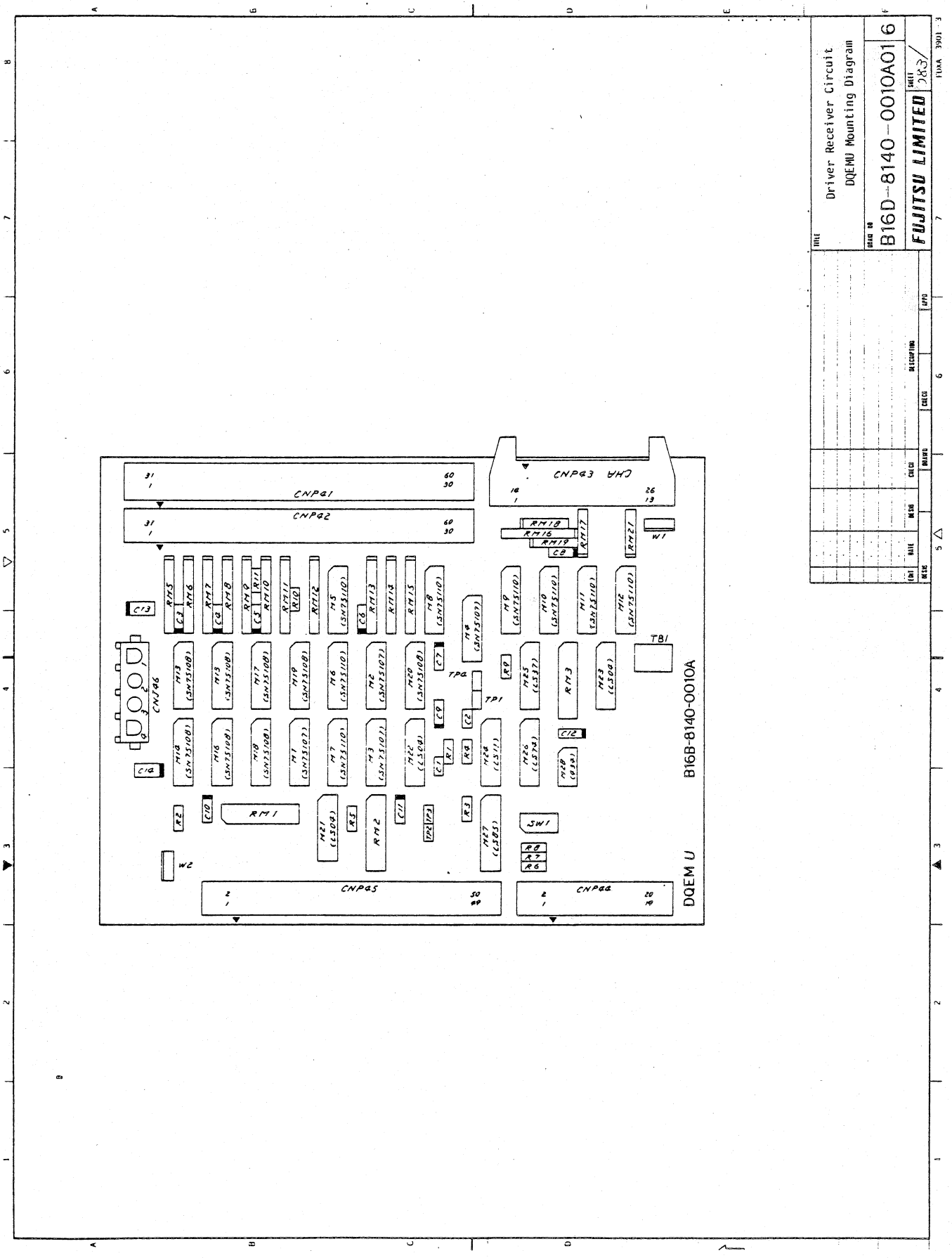
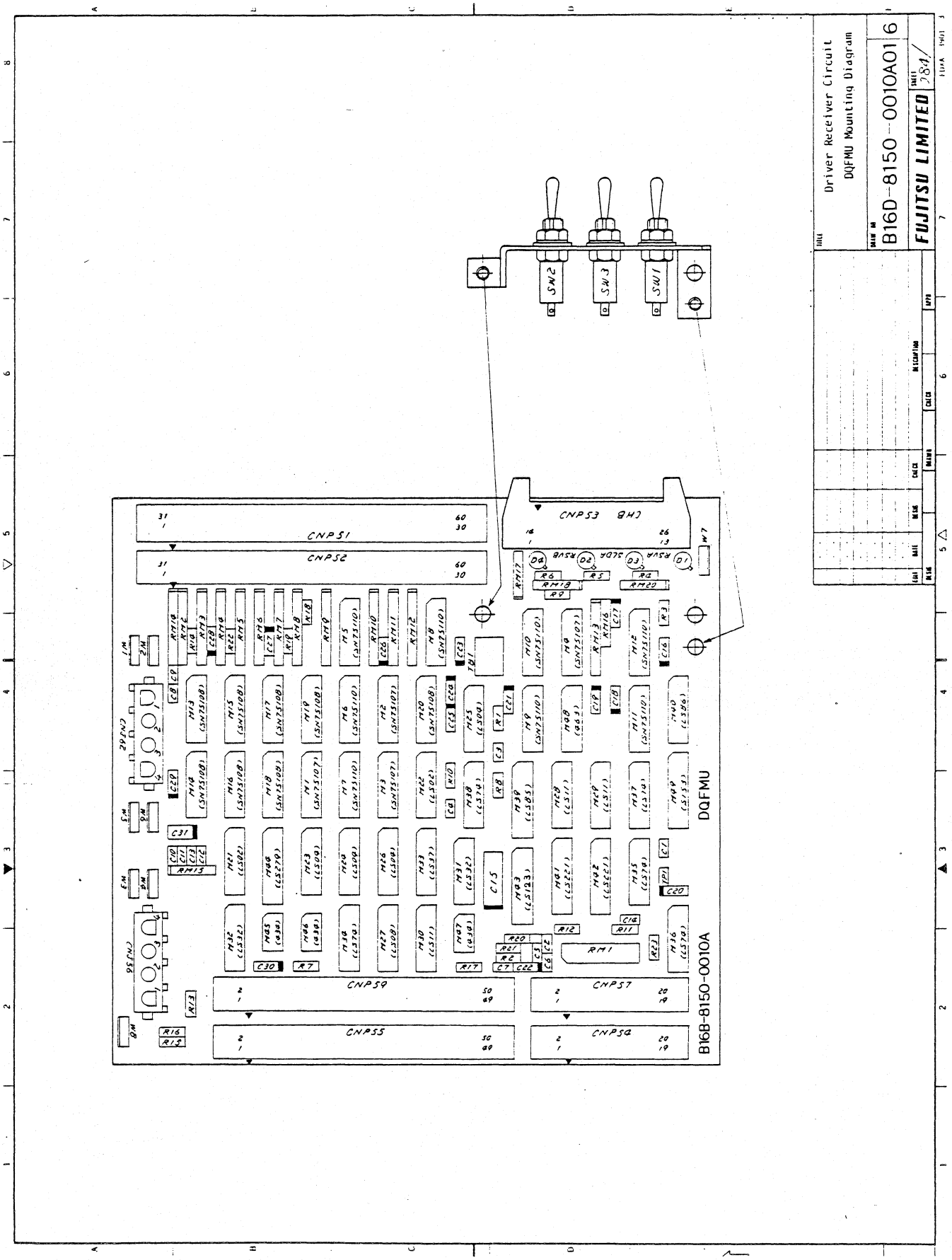
SHEET 081/

FDXA 3901 3


Power Amplifier 1WHMJ
Mounting Diagram
B16D-8130-0010A01 6
FUJITSU LIMITED


Driver Receiver Circuit
DQEMU Mounting Diagram
B16D-8140-0010A01 6
FUJITSU LIMITED
B16B-8140-0010A
DQEM U
CNP41
CNP42
CNP43
CNP45
CNP46
TB1
SW1
TP1
TP2
W1
W2


Driver Receiver Circuit
DQFMU Mounting Diagram
B16D-8150-0010A01 6
FUJITSU LIMITED
SHEET 284
DQFMU
B16B-8150-0010A
CNPS1
CNPS2
CNPS3
CNPS4
CNPS5
CNPS6
CNPS7
CNPS8
CNPS9
SW1
SW2
SW3

17.2 ABBREVIATIONS

	Abbreviation	Full Name
A	ABN	Abnormal
	ABSLD	A/B Channel Selected
	ACCCK	Access Check
	ACCEL	Acceleration
	ACCST	Access Start
	ACLMP	Acceleration Clamp
	ACMOD	Access Mode
	ACSTP	Access Start Pulse
	ACTMO	Access Time Out
	AGC	Automatic Gain Control
	AGC-TP	Automatic Gain Control - Test Point
	AGCOT1 ∿ AGCOT2	Automatic Gain Control Output 1 ∿ 2
	ALWDF	Allow Difference
	AMCTL	Address Mark Control
	AMENB	Address Mark Enable
	AMFD	Address Mark Found
	AMFD3	Address Mark Found 3
	AMGCL	Address Mark Gate Control
	AMRD	Address Mark Read
	AM8BT	Address Mark Round 8-Byte
	ANYRZ	Any Rezero
	ATTEN	Attention
B	BDINS	Bad Initial Status
	BIBIH	Bibration Inhibit
	BIBIN	" "
	BITL2	Bit Latch 2
	BIT0 ∿ BIT9	Bit 0 ∿ 9
	BIT0A ∿ BIT9A	Bit 0 ∿ 9 (Channel-A)
	BIT0B ∿ BIT9B	Bit 0 ∿ 9 (Channel-B)
	BIT0H ∿ BIT9H	Bit 0 ∿ 9 High
	BIT0L ∿ BIT9L	Bit 0 ∿ 9 Low
	BIT9AS	Bit 9 (Channel-A Priority Select)
	BIT9BS	Bit 9 (Channel-B Priority Select)
	BIT9S	Bit 9 (Priority Select)
	BTC1 ∿ BTC8	Bit Counter 1 ∿ 8
	BUSY	Busy
	BUSYA/BUSYB	Busy (Channel-A/B)
	BUSYH/BUSYL	Busy High/Low
	BYCL	Byte Clock

	Abbreviation	Full Name
C	CACMP	Channel-A Compare
	CAENB	Channel-A Enable
	CAPVL	Capture Velocity
	CARSV	Channel-A Reserved
	CAR1 ∿ CAR2	Cylinder Address Register 1 ∿ 2
	CASLD	Channel-A Selected
	CBCMP	Channel-B Compare
	CBENB	Channel-B Enable
	CBRSV	Channel-B Reserved
	CBSLD	Channel-B Selected
	CHPS0 ∿ CHPS4	Chip Select 0 ∿ 4
	CKGDB	Check Guard Band
	CLCK	Clock
	CLOCK	Clock
	CLPOS	Clamped Position
	CL1 ∿ CL219	Clock Counter 1 ∿ 219
	CNCT	Connect
	CNTRL	Control
	CORSE	Coarse
	CRAMP	Carrier Amp
	CRSNS	Current Sense
	CSNSE	Current Sense
	CTINT	Counter Initialize
	CTLCK	Control Check
	CTX	Count X Signal
	CTXECL	Count X ECL Level
	CT1 ∿ CT15	Count 1 ∿ Count 15
	CT15P	Count 15 Pulse
D	DACA	Digital to Analog Converter A
	DAMFD	Delayed Address Mark Found
	DECFR	Decrease Frequency
	DETMP	DE Timer Pulse
	DFCL	Difference Clock
	DFGT1 ∿ DFGT2	Difference Gate 1 ∿ 2
	DFZR	Difference Zero
	DIECK	Delta I Write Check
	DIFF	Differentiator
	DIFF-TP	Differentiator - Test Point
	DISAS	Disable Channel-A Switch
	DISBS	Disable Channel-B Switch
	DISCA	Disable Channel-A
	DISCB	Disable Channel-B
	DLDAM	Delayed Address Mark
	DLDDT	Delayed Data
	DLIW1 ∿ DLIW2	Delta I Write 1 ∿ 2
	DLIXW	Delayed Index Window

	Abbreviation	Full Name
D	DLMSP	Delayed Moter at Speed
	DLRGC	Delayed Read Gate Control
	DLZRX	Delayed Zero Cross Data
	DLZRX-TP	Delayed Zero Cross Data - Test Point
	DSCA/DSCB	Disable Channel-A/B
	DSCA2	Disable Channel-A2
	DSCB2	Disable Channel-B2
	DSQCK	DE Sequence Check
	DSQL1 ∿ DSQL4	DE Sequence Latch 1 ∿ 4
	DTFSC	Data Fast Sync.
	DTFSP	Data Fast Sync. Pulse
	DTGT	Data Gate
	DTGT-TP	Data Gate - Test Point
	D1 ∿ D512	Difference 1 ∿ 512
	D1440	Difference 144 Over
	D16S	Difference 16 or Smaller
E	EDEAT	Enable DE Attention
	ENBAS	Enable Channel-A Switch
	ENBBS	Enable Channel-B Switch
	ENDAC	End Accelerate
	ENDDC	End Decelerate
	EN11S ∿ EN60S	End 11 Seconds ∿ End 60 Seconds
	EQUAL	Equal
	EQULE	Equal
	ERPOS	Error Position
	EVEN1 ∿ 2	Even 1 ∿ 2
	E05MS	End 5 Micro-Seconds
	E5MS	End 5 Milli-Seconds
F	FAST	Fast
	FAULT	Fault
	FCAR0 ∿ FCAR3	Fix Cylinder Address Register 0 ∿ 3
	FCLRC	Fault Clear Command
	FCLRS	Fault Clear Switch
	FG	Function Generator
	FHDSL	Fixed Head Select
	FHF	Fixed Head Feature
	FHR31 ∿ FHR63	Fixed Head Register 31 ∿ 63
	FHS31 ∿ FHS95	Fixed Head Select 31 ∿ 95

	Abbreviation	Full Name
F	FHTG1	Fixed Heat Tag 1
	FLCLR	Fault Clear
	FLCRS	Fault Clear Switch
	FLSQ	Filter Squelch
	FLTLP	Fault Lamp
	FLTSQ	Filter Squelch
	FNPOS	Fine Position
	FNVEL	Fine Velocity
	FPTS	File Protect Switch
	FPTSW	File Protect Switch
	FSECL	Fast Synchronization ECL
	FSYNC	Fast Synchronization
	FTCLR	Fault Clear
	FXHSL	Fixed Head Select
G	GANGH	Gated Any Go Home
	GATE1 ∿ GATE4	Gate 1 ∿ Gate 4
	GATRT	Gate Attention Reset
	GBP1 ∿ GBP2	Guard Band Pattern 1 ∿ 2
	GDIW1	Gated I Write 1
	GDSK3	Gated Difference Seek 3
	GD1 ∿ GD128	Gated Difference 1 ∿ 128
	GENAC	Gated End Accelerate
	GFAST	Gated Fast
	GHCMP	Go Home Complete
	GHRZ	Go Home or Rezero
	GH1 ∿ GH3	Gated Hall Element 1 ∿ 3
	GINDX	Gated Index
	GJUST	Gated Just
	GLNMD	Gated Linear Mode
	GONL	Gated On Line
	GPAT	Gated Pattern
	GRDBL	Guard Band Latch
	GRDNP	Gated Read Down Pulse
	GSLOW	Gated Slow
	GSTT	Gated Start
	GST3	Gated State 3
	GSYNC	Gated Synchronous Pulse
	GTAG1 ∿ GTAG5	Gated Tag 1 ∿ 5
	GTKXP	Gated Track Crossing Pulse
	G1440	Gated Difference 144 Over

	Abbreviation	Full Name
H	HALRM	Hall Alarm
	HAR1 ∿ HAR16	Head Address Register 1 ∿ 16
	HA1 ∿ HA16	Head Address 1 ∿ 16
	HBYCL	Half Byte Clock
	HDGAN	Head Gain
	HDGAN-TP	Head Gain-Test Point
	HDSHT	Head Short
	HDSL1 ∿ HDSL2	Head Select 1 ∿ 2
	HOLD	Hold
	HOLDB	Hold Channel-B
	HSHCK	Head Short Check
	HSPIN	High Speed In
	HSPOT	High Speed Out
	HVLST	High Velocity Set
	H1 ∿ H3	Hall Element 1 ∿ 3
I	IDXCK	Index Check
	IHRSV	Inhibit Reserve
	IHTAG	Inhibit Tags 4 and 5
	INCFR	Increase Frequency
	INDSQ	Inhibit DE Sequence
	INDXG	Index Gate
	INDXH/INDXL	Index High/Low
	INDXP	Index Pulse
	INENB	Inner Enable
	INHRC	Inhibit Recycle
	INHSQ	Inhibit Sequencer
	INLFS	Initial Fast Sync
	INN	Inner
	INSTG	Initial State Good
	INTEG	Integrated Position
	IS1 ∿ IS128	Index Sector Counter 1 ∿ 128
	IXCKG	Index Check Gate
	IXCKL	Index Check Latch
	IXMRK	Index Mark
	IXW	Index Window
J	JUST	Just

	Abbreviation	Full Name
L	LDBYT	Load Byte
	LDDT	Load Data
	LNML	Linear Mode Latch
	LNMOD	Linear Mode
	LPST0 ∿ LPST7	Lamp Status 0 ∿ 7
	LSPIN	Low Speed In
	LSPOT	Low Speed Out
	LTSVC	Lock to Servo Clock
M	MARSV	MARS Voltage
	MCLMP	Minus Clamp
	MCPCK	Multi Chip Check
	MCPSL	Multi Chip Select
	MLEVL	Minus Level
	MM	Mono-Stable Multivibrator
	MM-TP	Mono-stable Multivibrator - Test Point
	MRTZL	Manual Rezero Latch
	MRTZS	Manual Rezero Switch
	MS4V	-4V
	MTRSP	Motor at Speed
	MUSFM	MARS Unsafe Movable Head
	MUSFV	MARS Unsafe Voltage
	MUSFX	MARS Unsafe Fixed Head
	MVHSL	Movable Head Select
	MVINN	Move Inner
	MVOTG	Move Out Gate
	MVOUT	Move Outer
	M12V	-12V
	M25M	Mono-Stable 2.5 Milli-Second
	M3M	Mono-Stable 3 Milli-Second
	M4VDE	-4V DE
	M5MS	Mono-Stable 5 Milli-Second
N	N-Q	Normal Minus Quadrature
	N+Q>0	Normal Plus Quadrature Greater Than Zero
	NC1 ∿ NC512	New Cylinder Address Register 1 ∿ 512
	NGT	Noise Gate
	NOTCH	Notch Filter
	NRMS	Normal Switch
	NSQCH	Not Squelch
	NSQHG	Not Squelch Gate

	Abbreviation	Full Name
O	OCDTA/OCDTB	Open Cable Detect Channel-A/B
	OCDTH/OCDTL	Open Cable Detect High/Low
	OCTCK	Over Cylinder and Control Check
	ODD1 ∿ 2	Odd 1 ∿ 2
	OFACT	Offset Active
	OFCMD	Offset Command
	OFSET	Offset
	OFINT	Offset Interrupt
	OFOUT	Offset Out
	OFTRK	Off Track
	ONCYL	On Cylinder
	ONL	On Line
	ONTRK	On Track
	OSC	Oscillator
	OTENB	Out Enable
	OVCRT	Over Current
	OVCY	Over Cylinder
	OVSCK	Over-Shoot Check
	OVSGB	Over-Shoot Guard Band
P	PADRV	Power Amp. Drive
	PCLMP	Plus Clamp
	PC1 ∿ PC512	Physical Cylinder Address Register 1 ∿ 512
	PICIN	Pic-In
	PICINB	Pic-In Channel-B
	PICOT	Pic-Out
	PLEVL	Plus Level
	PLOAN	PLO Analog
	PLO1F	PLO 1F
	POSER	Position Error
	POSN	Position Normal
	POSQ	Position Quadrature
	POTRL	Pick Out Relay
	PRTCT	Protect
	PS6V	+6V
	PWORS	Power On Reset
	PWRDY	Power Ready
	PWRLP	Power Lamp
	PWRST	Power On Reset
	P12V	+12V
	P5V	+5V
	P5VFX	+5V for Fixed Heads
	P6VMV	+6V for Movable Heads

	Abbreviation	Full Name
R	RAWDT	Raw Read Data
	RAW2FA/RAW2FB	Raw 2F A/B
	RD	Read
	RDCKH/RDCKL	Read Clock High/Low
	RDDGT	Read Data Gate
	RDDT	Read Data
	RDDTA	Read Data
	RDDTA-TP	Read Data - Test Point
	RDDTFX	Read Data Fixed Head
	RDDTG	Read Data Gate
	RDDTH/RDDTL	Read Data High/Low
	RDDTMV	Read Data Movable Head
	RDWT	Read/Write
	RDYLP	Ready Lamp
	REGRT	Register Reset
	RGCTL	Read Gate Control
	RGDNP	Read Gate Down Pulse
	RGUPP	Read Gate Up Pulse
	RNTMG	Run Timer Gate
	RNTMR	Run Timer
	RONLY	Read Only
	RRSVA/RRSVB	Reset Reserve Channel A/B
	RSKEN	Reset Seek End
	RSSCT	Reset Index Sector Counter
	RST	Reset
	RSTMS	Release Timer Switch
	RSTSC	Reset Sector Counter
	RST1 ∿ 2	Reset 1 ∿ 2
	RTBTC	Reset Bit Counter
	RTFTM	Reset Track Following Timer
	RTGDB	Reset Guard Band
	RTZMD	Rezero Mode
	RWCAP	Read/Write Capable
	RWDTF	Read/Write Data for Movable Head
	RWDTFX	Read/Write Data for Fixed Head
	RWDTM	Read/Write Data for Movable Head
	RWDTMV	Read/Write Data for Movable Head
	RZGH	Rezero or Go Home
	RZML	Rezero Mode Latch
	RZMOD	Rezero Mode
	RZOUT	Rezero Out
	RZRCM	Rezero Command
	RZRST	Rezro Start

	Abbreviation	Full Name
S	SAGC	Servo AGC
	SCMPA/SCMPB	Selecte Compare Channel-A/B
	SCTCL	Sector Clock
	SCTLX	Sector Index
	SCTP	Sector Pulse
	SCTRH/SCTRL	Sector High/Low
	SCTRP	Sector Pulse
	SC1 ∿ SC128	Sector Counter 1 ∿ 128
	SDF16	Seek Difference 16
	SHORT	Short
	SKEDA/SKEDB	Seek End Channel-A/B
	SKEDH/SKEDL	Seek End High/Low
	SKENA/SKENB	Seek End Channel-A/B
	SKEND	Seek End
	SKINH	Seek Inhibit
	SLCTD	Selected
	SLIW	Select I Write
	SLOW	Slow
	SLTDH/SLTDL	Selected High/Low
	SMOTH	Smoother
	SNI	Select Normal Invert
	SNN	Select Normal Non-Invert
	SOFCK	Servo Offtrack Check
	SOFST	Set Servo Offset
	SOSCK	Set Over-Shoot Check
	SPALM	Speed Alarm
	SPR	Spare
	SPSTT	Spindle Start
	SQI	Select Quadrature Invert
	SQN	Select Quadrature Non-Invert
	SQRZR	Sequence Rezero
	SRVL	Servo Latch
	SR0 ∿ SR3	Shift Register 0 ∿ 3
	SST	Seek Start
	START	Start
	STMD1 ∿ 2	Status Mode 1 ∿ 2
	STRSW	Start Switch
	STRTL	Start Latch
	STRZ	Start Rezero
	STSOF	Set Servo Offtrack Check
	STS0 ∿ STS7	Status 0 ∿ 7
	STS0B ∿ STS7B	Status 0 ∿ 7 Channel B
	STS0H ∿ STS7H	Status 0 ∿ 7 High
	STS0L ∿ STS7L	Status 0 ∿ 7 Low
	STTLP	Start Lamp
	STTMR	Start Timer
	STTOK	Start OK
	STTRL	Start Relay
	STTSW	Start Switch
	STUS0	Status 0
	STWAT	Set Wait
	SVLVL	Servo Level

	Abbreviation	Full Name
S	SVMDG	Servo Mode Gate
	SVMDP	Servo Mode Pulse
	SVMOD	Servo Mode
	SVOFT	Servo Off-Track
	SVPRE	Servo Pre-Amp.
	SYNCG	Sync. Gate
	SYSRZ	System Rezero
	S1 ∿ S16384	Sector Switch 1 ∿ 16384
T	TAG1 ∿ TAG5	Tag 1 ∿ 5
	TAG1A ∿ TAG5A	Tag 1 ∿ 5 Channel-A
	TAG1B ∿ TAG5B	Tag 1 ∿ 5 Channel-B
	TAG1C	Tag 1 C
	TAG1H ∿ TAG5H	Tag 1 ∿ 5 High
	TAG1L ∿ TAG5L	Tag 1 ∿ 5 Low
	TFTMR	Track Following Timer
	TIEDN	Tie-Down
	TIEUP	Tie-Up
	TIEUP1 ∿ 2	Tie-Up 1 ∿ 2
	TKXGP	Track Crossing Pulse
	TKXNG	Track Crossing
	TMGT	Timer Gate
	TMOCK	Time Out Check
	TMOFF	Timer Off
	TMON	Timer On
	TMOTL	Time Out Latch
	TMOUT	Time Out
	TRMWD	Transmit Write Data
	TRSCK	Transition Check
	TRWD	Transmit Write Data
	T3M	Trigger 3 Milli-Second
	T5MS	Trigger 5 Milli-Second
U	UAD1 ∿ UAD4	Unit Address 1 ∿ 4
	USLTD	Unit Selected
	USL1A ∿ USL4A	Unit Select Bit 1 ∿ 4 Channel-A
	USL1B ∿ USL4B	Unit Select Bit 1 ∿ 4 Channel-B
	USL1H ∿ USL4H	Unit Select Bit 1 ∿ 4 High
	USL1L ∿ USL4L	Unit Select Bit 1 ∿ 4 Low
	USTGA/USTGB	Unit Select Tag Channel A/B
	USTGH/USTGL	Unit Select Tag High/Low

	Abbreviation	Full Name
V	VCMA/VCMB	Voice Coil Motor A/B
	VCOC1 ∿ VCOC4	VCO Counter 1 ∿ 4
	VCO1F/VCO2F	VCO 1F/2F
	VCX	Voltage Control Signal
	VCX-TP	Voltage Control Signal - Test Point
	VCO1/VCO2	Voltage Controlled Oscillator 1/2
	VFOFS	VFO Fast Sync
	VFO1F	VFO 1F
	VFO1S	VFO 1 Shifted Clock
	VFS	VFO Fast
	VG20I	Velocity Greater Than 20 Inch/Sec
	VLERR	Velocity Error
	VLGDA	Velocity Guide
	VLIX1	Valid Index 1
	VLSIT	Velocity
	VLTY	Velocity
W	WATL	Wait Latch
	WATST	Wait Set
	WDATA	Write Data
	WDATA-TP	Write Data - Test Point
	WGCTL	Write Gate Control
	WGSL	Write Gate Selected
	WIRCK	Write Current On Read Check
	WSLFX	Write Select Fixed Head
	WSIMV	Write Select Movable Head
	WT	Write
	WTCA/WTCB	Write Clock Channel-A/B
	WTCK	Write Clock
	WTCKA/WTCKB	Write Clock Channel-A/B
	WTCKH/WTCKL	Write Clock High/Low
	WTCL	Write Clock
	WTCR	Write Current
	WTCRF	Write Current Fixed Head
	WTCRM	Write Current Movable Head
	WTDT	Write Data
	WTDTA/WTDTB	Write Data Channel-A/B
	WTDTH/WTDTL	Write Data High/Low

	Abbreviation	Full Name
Z	ZRACM	Difference Zero Access Mode
	ZRMOD	Zero Mode
	ZRX	Zero Cross Data
	ZRX-TP	Zero Cross - Test Point
	1 ∿ 16384	Sector Switch Input 1 ∿ 16384
	1FCKH/1FCKL	1F Write Clock High/Low
	1FMCL	1F Main Clock
	1FWCK	1F Write Clock
	1FWCL	1F Write Clock
	1FWWD	1F Write Window
	11S60	11 Second or 60 Second
	2FEY1/2FEY2	2F Early Clock 1/2
	2FLT	2F Late Clock
	2FMCL	2F Main Clock
	2FOT	2F On Time Clock
	2FRDCL	2F Read Clock
	-S4V	Servo -4 Volt
	-S4VRTN	Servo -4 Volt Return
	-|VLTY|	Negated Absolute Velocity
	-4VDE	-4 Volt to DE
	-5.2V-TP	-5.2 Volt - Test Point
	-5.2VE	-5.2 Volt
	+S6V	Servo +6 Volt
	+S6VRTN	Servo +6 Volt Return
	+48VRTN	+48 Volt Return
	+5VFX	+5 Volt to Fixed Head
	+6VE	+6 Volt
	+6VFX	+6 Volt to Fixed Head
	+6VMV	+6 Volt to Movable Head