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91S16 AND 91S32
SERVICE MANUAL ADDENDUM
TO THE DAS 9100 SERIES SERVICE MANUAL
(PART NUMBER 062-5848-00, -01, AND UP)

This Tektronix Manual Addendum supports the 91S16 and 91S32 Programmable Pattern Generator Modules. This addendum contains the general information, specifications, operating instructions, theory of operation, test and adjustment procedures, and troubleshooting information for the modules. Parts location drawings and schematics are also included.

The 062-5848-00 manual set is a package consisting of loose leaf binders with manuals and addenda. Each manual and addendum in the set has its own part number starting with prefix 070.

This addendum contains service information for the 91S16 and 91S32 Programmable Pattern Generator Modules.

Refer to the DAS 9100 Series Service Manual for information on other DAS products, including mainframes, instrument modules, probes, and options.

How to Use This Addendum. This addendum is organized similarly to the DAS 9100 Series Service Manual: sections in the addendum correspond to the sections in the service manual. You can either leave the addendum whole and place it in one of the service manual binders, or you can separate the sections and insert them after the corresponding section in the main manual.

NOTE: You can order an extra service manual binder (Vol.III) by using P/N 016-0769-00.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL

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TABLE OF CONTENTS

Section 1 -- INTRODUCTION AND SPECIFICATIONS

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (cont.)

Section 4 -- THEORY OF OPERATION

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (cont.)

LIST OF ILLUSTRATIONS

GENERAL INFORMATION

DESCRIPTION

The 91S16 and 91S32 Pattern Generator modules are second generation pattern generator cards. Each module can be used alone, and each has specialized features that make it particularly suited to a field of applications. However, the 91S16 can also be used to control the operation of up to five 91S32s, giving you the advantage of both cards' feature sets.

NOTE

The 91S16 and 91S32 replace the first generation 91P16/32 pattern generator modules. You cannot operate a 91S16 or 91S32s if a 91P16 is installed in the DAS.

91S16 ALGORITHMIC PATTERN GENERATOR

The 91S16 is an algorithmic pattern generator. The 91S16 differs from stored-pattern (all vectors stored in RAM) pattern generators in that loops, conditional branches, and a wide variety of interactions with the circuit under test are allowed. A large pattern generator memory is not necessary with algorithmic pattern generators since the capability to branch and loop within the program allows you to keep the system under test stimulated without writing lengthy programs.

The 91S16 also allows you to have a great deal of real-time interaction with the circuit under test via the 91S16's optional P6460 External Control probe (Data Acquisition probe). This probe can be used to acquire the following external signals: External Jump, Interrupt Request, Interrupt Request Qualifier, Pause, and External Inhibit signals. You can also use this probe to acquire an external clock signal.

There are two phono connectors on the back of the 91S16 module; one accepts an external start signal, and the other provides an external trigger signal.

The 91S16 provides two 8-bit data registers (or one internal 16-bit data register) which can be used as counters or as an alternate source for pattern output. The 91S16 instruction set includes nine instructions ranging from simple *JUMP to label* commands to *IF Register = 0 JUMP to label*. Fifteen different labels can be programmed. You can also program a special interrupt service routine.

The 91S16 Pattern Generator module provides 16 data output channels, 2 clock, and 2 strobe lines. Strobes can be used as additional data channels. The master clock can be supplied either from the DAS internal clock or from an external device. Maximum clock speed is 50 MHz. Data output is normally synchronous with the master clock, but individual data and strobe lines can be programmed ± 10 ns relative to the master clock (± 5 ns relative to pod clock). Pattern memory is 1024 sequence lines (vectors) deep.

Only one 91S16 can be installed in the DAS, however the 91S16 can be used as a controller for up to five 91S32s.

91S32 STORED-PATTERN PATTERN GENERATOR

The 91S32 is a stored-pattern (all vectors stored in RAM) pattern generator. Not all pattern generator applications require as much interaction with the system under test as is provided by the 91S16. Instead, many applications require straightforward test patterns that are often quite lengthy, and frequently require wide data patterns. The 91S32 is designed to serve these "wide and deep" applications.

The 91S32 is traditionally programmed to execute its program in a sequential beginning-to-end fashion. However, if you use the 91S32 in conjunction with a P6452 probe attached to the DAS Trigger/Time Base module, you can use inputs from that module to supply External Clock, External Start, External Inhibit, and Pause signals. Data output is normally synchronous with the master clock's rising edge, but individual pods can be adjusted ± 5 ns and individual channels have an additional ± 5 ns range.

Each 91S32 provides 32 channels of data, four strobes, and four clock lines. You can install up to six 91S32s in a single DAS for a total of 192 data channels, 24 strobes, and 24 clock lines. In addition, the strobe lines can be used as extra data channels. Maximum clock speed is 50 MHz. Pattern depth for all channels is 2048 sequence lines (vectors), however there are features available that allow you to split the memory into two 1024-line pages and reload alternate pages of memory while the pattern generator is outputting data (this requires a 91S16). The 91S32 can also be programmed to execute its program repeatedly.

91S16 AS CONTROLLER FOR 91S32s

One 91S16 can serve as a controller for up to five 91S32s. In this configuration, you can supply up to 16 data channels with a memory depth of 1024 lines, plus 160 data channels with a memory depth of 2048 lines (two 1024-line pages). There are also 22 clock lines and 22 strobe lines available.

In addition, this configuration provides all the branching instructions and interactive features available with the 91S16 along with the large numbers of data channels and pattern depth afforded by the 91S32s.

There are two different operating modes available when the 91S16 and 91S32 are used together: Sequential mode and Follows 91S16 mode.

Sequential Mode. This operating mode allows the 91S16 and 91S32 to operate simultaneously. The 91S16 will supply the clock signal to the 91S32, however each card will execute its program independently. In other words, the 91S16 can perform branching operations while the 91S32s execute their program in a sequential line-by-line manner. When the 91S32 reaches the end of its memory, it can be set to automatically restart from the beginning. This will keep all data channels active for as long as is desired.

In this mode, the 91S32's memory is configured as a single 2048-line program.

Follows 91S16 Mode. This operating mode allows the 91S16 to have much more active control over the output of the 91S32s. The 91S32 will follow instructions governing sequence line execution programmed in the 91S16.

In Follows 91S16 mode, the vector memory address register of the 91S16 becomes the vector address register for the 91S32s via an interconnect cable. This means that if the 91S16 executes a loop, the 91S32s will also loop. For example, if 91S16 SEQ 10 (sequence line 10) contained an instruction transferring pattern execution to SEQ 5, the 91S32s would also jump to SEQ 5 and continue outputting data sequentially from that line.

The 91S16 also supplies the master clock to the 91S32 modules. Usually, you would want the 91S16 and 91S32 to output data according to the same clock, but you can program the 91S32 to execute its program at one-half or one-fourth the clock rate supplied by the 91S16 module.

In Follows 91S16 mode, the memory of the 91S32 is divided into two 1024-line pages called Page A and Page B. The size of these pages matches the memory depth of the 91S16. The 91S16 has control over which memory page the 91S32 will execute. As an example, you can program two different programs in the 91S32 (one in each page) and use the 91S16 to switch between the programs based on some signal sensed by the 91S16's optional P6460 External Control probe.

Pattern Download From Host

One major feature provided by Follows 91S16 mode is the automatic Pattern Download From Host feature. There are two versions of Pattern Download From Host. The Pattern Download For Static Devices version can be used with or without a 91S16 installed. It can be implemented using either Option 02 or Option 06 GPIB interface commands. The Pattern Download For Dynamic Devices version uses the Keep-Alive feature programmed into the 91S16. This version is only available when you have a 91S16 and at least one 91S32 installed; you must use the Option 06 GPIB interface commands.

Pattern Download For Static Devices. If your pattern generator program is very large, or if you have developed the program on a host computer, the entire program may be too large to fit into the 91S32's memory. Follows 91S16 mode allows you to output 2047-lines of vectors, reload the pattern generator's memory from a host computer, output the new block of vectors, and continue this process until the entire program has been executed. Instructions for communicating with the host computer or external storage device are programmed into the 91S16. The Pattern Download From Host feature uses either DAS Option 02 GPIB, the RS-232 master/slave interface using GPIB commands, or DAS Option 06 GPIB (high speed GPIB).

Pattern Download For Dynamic Devices (Keep-Alive) When using the Pattern Download For Static Devices feature, the pattern generator alternates between outputting patterns and sitting idle while the next block of vectors is downloaded from the host computer. This can cause a problem with dynamic circuit elements that require constant clock and vector inputs. The 91S16/32 combination provides a Keep-Alive function to supply clock and a few vectors to keep the circuit under test active until the 91S32 memory has been reloaded. Keep-Alive is essentially a subroutine you program into the 91S16; static devices being tested won't require this feature. Keep-Alive is only available when you are using DAS 9100 Option 06: I/O Communication Interface (with HSPAT GPIB command).

SIGNAL CHARACTERISTICS

The purpose of the pattern generator is to exercise a system under test. The pattern generator outputs clock and data signals which can be used to simulate circuit bus activity, or to directly stimulate circuit elements. At the same time, it interacts with the system under test by responding to a variety of external signals. The external signals available depend on whether you are using a 91S16 module, a 91S32 module, or a combination of the two modules.

Figure 1-1 illustrates the basic functions of the pattern generator and its input and output signals. The characteristics of these signals are set up and enabled via the Pattern Generator menus.

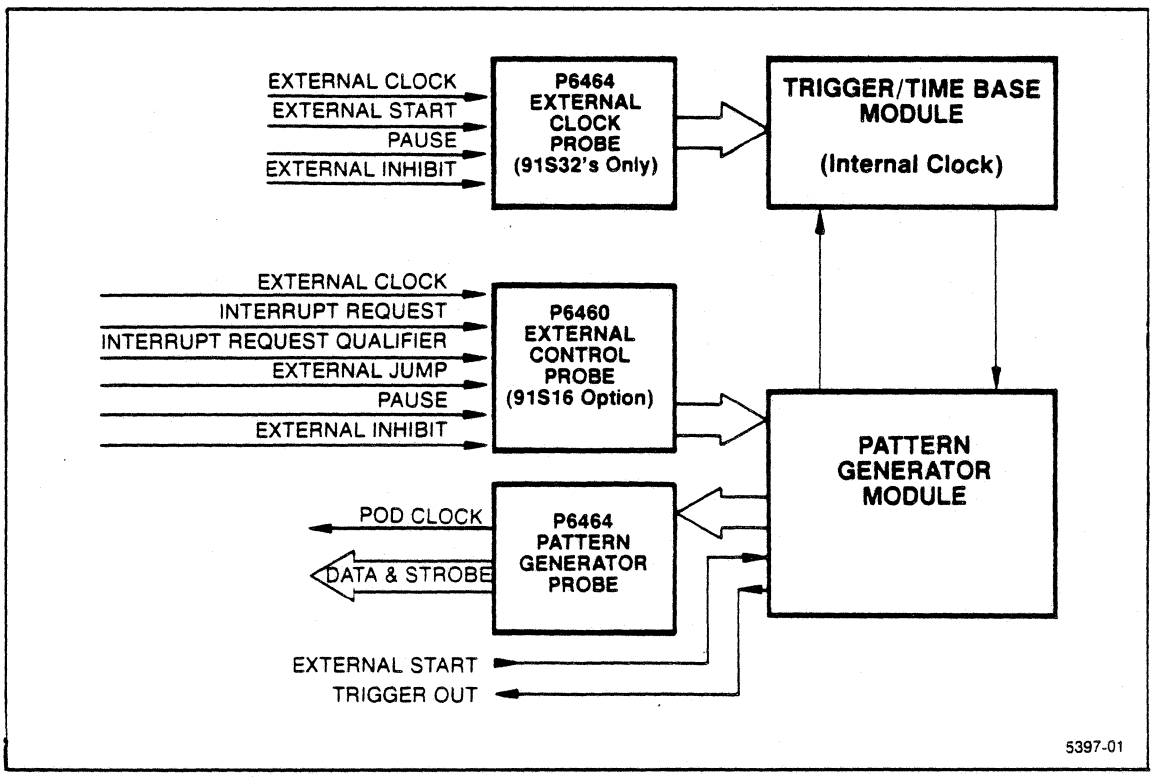

Figure 1-1. 91S16/32 block diagram.

Refer to the specification tables later in this section for technical parameters related to these signals.

CLOCKING

The pattern generator is associated with two types of clocks: the master input clock and the output clocks.

The pattern generator's master input clock controls the rate of the output clock and data. The master clock may be the DAS internal clock or the rising or falling edge of an external clock source. The external clock is supplied via the optional P6460 probe for the 91S16, or via the P6452 external control probe attached to the DAS Trigger/Time Base module for stand-alone 91S32s. The maximum clock rate is 50 MHz for the 91S16 with either internal or external clock source. 91S32s operating without a 91S16 controller can run at 50 MHz. using an internal clock source, or at 25 MHz. using an external clock source. A 91S16 operating with 91S32s can operate at up to 50 MHz., but there are some restrictions on the pod clock delay settings.

Here is a summary of the timing restrictions:

91S16	Up to 50 MHz with internal or external clock; no pod clock restrictions.
91S32 Stand-Alone	Up to 50 MHz. with internal clock if all pod clocks are set to 0 ns delay. Up to 25 MHz. with either an internal or external clock with no pod clock restrictions.
91S16 with 91S32s	Up to 50 MHz. with internal clock if all pod clock delays are set to −5 ns.

The output clock (pod clock) signals are derived from the master input clock. The output clock's rising edge is synchronized with the selected master clock edge, whether rising or falling.

Each P6464 Pattern Generator probe supplies one output clock line, labeled CLK. Each P6464 probe also supplies eight data channels and one strobe line. Each probe connects to a specific pod connector on the back of the pattern genrator module. Pod connectors are assigned letters to help with identification. The 91S16 accepts two P6464 probes and one optional P6460 External Control Probe; the P6464s attach to pods A and B, and the P6460 probe attaches to Pod C. Each 91S32 has four P6464 probes and which attach to pods labeled Pod A through Pod D.

In addition to the simple relationship of the pattern generator master clock to the rising or falling edge of the input clock, each pod has a clock line that can be adjusted relative to the master clock. Pod clocks can be skewed ± 5 ns relative to the master clock, and data and strobe outputs can be skewed an additional ± 5 ns, allowing a maximum skew between data outputs (from two differnt pods) of 20 ns. All pod timing adjustments are made relative to the master clock. Data and strobe timing adjustments are made relative to the pod clocks.

When a 91S16 controlls one or more 91S32s in Follows 91S16 mode, the 91S16 supplies the master clock to the 91S32s. You can program the 91S32's clock rate to be one-half, one-fourth, or the same as the 91S16's clock.

DATA OUTPUT

Data output from the pattern generator is normally parallel on all channels. Each channel's timing is adjustable up to ± 5 ns relative to its pod clock via the Setup: Timing sub-menu. Each pod clock is adjustable an additional ± 5 ns relative to the master clock.

Each pattern generator probe provides eight data channels labeled 0 through 7. Each probe also provides one strobe line which can be used as an additional data channel.

INTERRUPT REQUEST

The 91S16 provides an Interrupt Request (IRQ) line via its optional P6460 External Control (Data Acquisition) probe. The 91S16 can be programmed to perform a special interrupt service routine every time the IRQ line is asserted. The 91S16 can also be programmed to ignore an interrupt call during certain segments of program memory.

There is also an interrupt request qualifier line provided by the 91S16's optional P6460 probe. This line allows you to qualify when the IRQ line is valid.

PAUSE

Both the 91S16 and the 91S32 have the capability to respond to an external pause signal. Pause causes the pattern generator to stop executing program lines but still hold the P6464 outputs at their current levels. The 91S16 PAUSE signal is supplied via its optional P6460 External Control probe. The stand-alone 91S32 PAUSE signal must be supplied via the P6452 External Clock Probe attached to the DAS Trigger/Time Base module.

INHIBIT

There are two kinds of inhibit signals used by the 91S16 and the 91S32: internally programmed inhibits and external inhibits. Either kind of inhibit signal causes some or all of the P6464 data lines to be tri-stated.

The 91S16 can have internal inhibits programmed in its Program: Run sub-menu. External inhibit signals are provided via its optional P6460 External Control probe. The 91S32 can also have internal inhibits programmed in its Program: Run sub-menu, and external inhibit signals are provided either by the 91S16's P6460 probe, or, if no 91S16 is installed, via a P6452 External Clock probe attached to the DAS Trigger/Time Base module.

The 91S16 and 91S32 Configuration sub-menus provide fields that allow you to select the polarity of the internal and external inhibit signals. They also allow you to use logical operators to combine these inhibit signals.

Both 91S16 and 91S32 modules provide bit-selectable inhibit masks for data channels in their program sub-menus. Inhibit masks for clock and strobes lines appear in the Configuration sub-menus.

EXTERNAL START

Both the 91S16 and the 91S32 can respond to External Start signals. These signals are supplied via a phono connector for the 91S16, and via the P6452 probe (attached to the DAS Trigger/Time Base module) for stand-alone 91S32s.

KEYBOARD CONTROLS

Figure 1-2 illustrates the keyboard overlay supplied with each 91S16 and 91S32. Apply this overlay over the existing Pattern Generator keys in the lower left corner of the DAS keyboard.

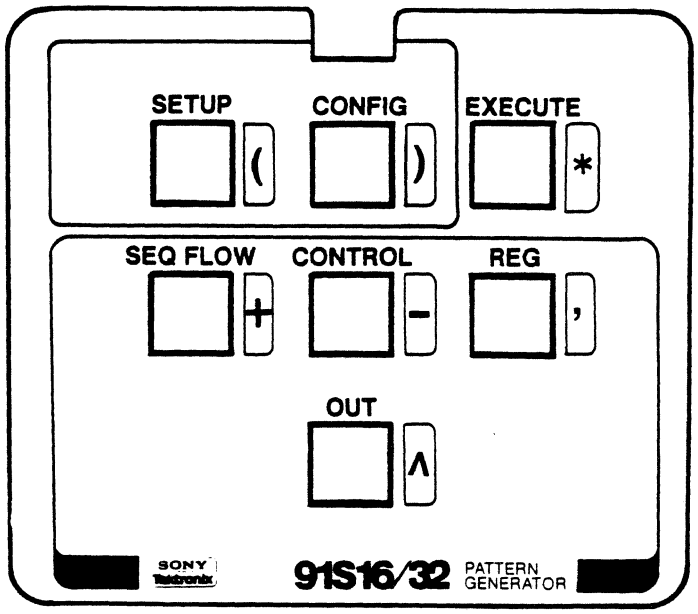

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Figure 1-2. 91S16/32 keyboard overlay.

The 91S16/32 Pattern Generator keys are arranged in three major groups. Group one consists of keys used to call up the various sub-menus on the display. This group includes the PATTERN GENERATOR key, the SETUP key, and the CONFIG key. Group two contains only the EXECUTE key. The third group consists of the SEQ FLOW, CONTROL, REG, and OUT keys. Key groups are outlined on the 91S16/32 keyboard overlay.

NOTE

The SETUP and CONFIG keys will not operate unless you have already entered the patten generator Program Run sub-menu. To enter the Setup and Configuration sub-menus, press the PATTERN GENERATOR key first, and then press either the SETUP or CONFIG key.

PATTERN GENERATOR This is the first key you will press when you want to call up any pattern generator sub-menu from the DAS power-up menu. After pressing the PATTERN GENERATOR key, the DAS will display the 91S16 Run sub-menu if a 91S16 is installed, otherwise it will display the 91S32 Run sub-menu.

SETUP This key causes the SETUP sub-menu to be displayed. There are two different setup sub-menus for each pattern generator module: PROBE and TIMING. See the *Introduction to 91S16 and 91S32 Sub-menus* section later in this manual for a description of these sub-menus. The 91S16 SETUP sub-menu will be displayed if a 91S16 is installed, otherwise the 91S32 SETUP sub-menu will be displayed.

CONFIG This key causes the Configuration sub-menu to be displayed. See the *Introduction to 91S16 and 91S32 Sub-menus* section for a description of this sub-menu. The 91S16 Configuration sub-menu will be displayed first whenever a 91S16 is installed in the DAS.

EXECUTE This key marks the end of data entry during an edit operation. Pressing this key tells the DAS you have finished making entries in an edit command and starts the operation.

SEQ FLOW This key is only used when programming branch instructions for the 91S16. SEQ FLOW stands for Sequence Flow, the order in which sequence lines are executed. See the 91S16 Program Run sub-menu for details.

CONTROL This key is used when programming the 91S16 to control the operation of one or more 91S32s operating in FOLLOWS 91S16 mode. This key also selects the TRIGGER instructions which issues a trigger signal via a phono connector on the back of the 91S16.

REG This is another 91S16 programming key used to control the function of the 91S16 internal register. REG instructions can include load, increment, or decrement the contents of the internal register.

OUT This key instructs the 91S16 to output the contents of its internal data register as data in place of the regular vector programmed for that sequence line. This key also provides an instruction that causes the pattern generator to ignore both the current Pod A pattern and register values and instead output the previous Pod A vector again.

INTRODUCTION TO 91S16 AND 91S32 SUB-MENUS

The 91S16 and 91S32 Pattern Generator modules provide a number of different sub-menus tailored to particular tasks. Because the 91S16 and 91S32 can each operate independently, or with the 91S16 as a controller for up to five 91S32s, the two types of pattern generator modules have similar sub-menus. In other words, the 91S16 and the 91S32 both have Run, Trace, and Step sub-menus. However, because the 91S16 and the 91S32 have different features, sub-menus with the same name for each card may not operate in exactly the same way. Also, when the 91S16 is used to control one or more 91S32s, the function of both cards' sub-menus changes slightly.

This section of the manual is designed to familiarize you with the names and functions of each type of sub-menu, let you know what other sub-menus are available, and help you move from one sub-menu to another easily. Detailed descriptions for each sub-menu are provided later in this addendum.

MAJOR SUB-MENU TYPES

Both the 91S16 and the 91S32 provide three basic types of sub-menus. These sub-menus are the Configuration, Setup, and Programming sub-menus. Figure 1-3 illustrates the grouping of the sub-menus within their major headings.

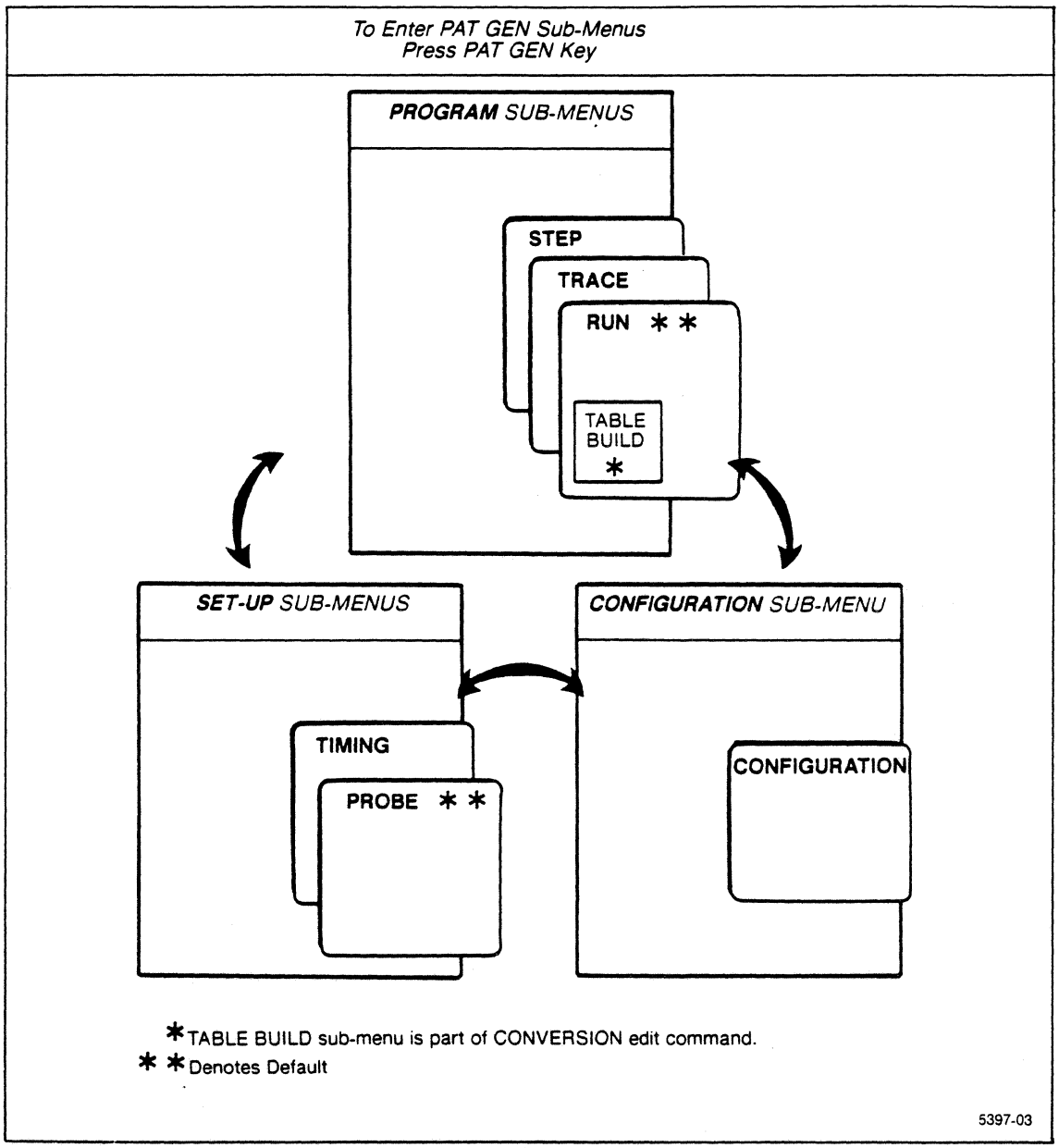


Figure 1-3. 91S16/32 sub-menu structure.

In order to access most of the pattern generator sub-menus, you must first press the PATTERN GENERATOR key. Once you have displayed a pattern generator sub-menu, you can easily move to and from the other sub-menus by pressing the appropriate key. Figure 1-4 illustrates how to use the DAS pattern generator keys to move between the various sub-menus.

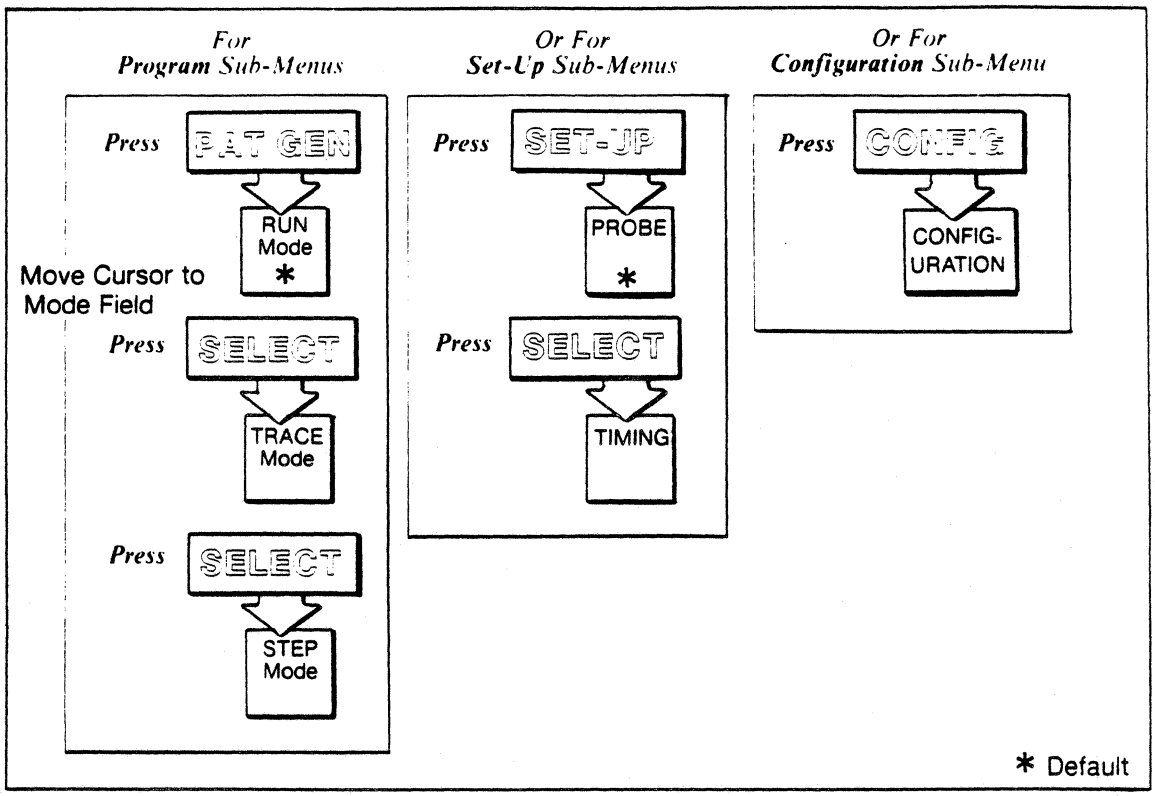


Figure 1-4. How to move between 91S16/32 Pattern Generator sub-menus.

CONFIGURATION SUB-MENUS

The 91S16 and 91S32 Configuration sub-menus are primarily used to set signal levels, signal polarities, pod delays, and various inhibit masks--the kinds of things you do once per test environment. They are also used to select major operating modes when 91S16 and 91S32 cards are used together.

Press the CONFIG key on the DAS keyboard to display the Configuration sub-menu. If you have a 91S16 installed in the DAS, the 91S16 Configuration sub-menu will be displayed first. Press the SELECT key to display the 91S32 sub-menu if you have both types of pattern generators installed.

NOTE

Some additional 91S32 Configuration sub-menu fields are available when the 91S32 is used in conjunction with a 91S16 module.

SETUP SUB-MENUS

There are two different Setup sub-menus: Probe, and Timing. Press the SETUP key to display the Probe sub-menu. If an 91S16 is installed in the DAS, the 91S16 Probe sub-menu will be displayed. If only 91S32s are installed, the 91S32 Probe sub-menu will be displayed. You cannot display the 91S32 Probe sub-menu if a 91S16 is installed in the DAS.

The Probe sub-menu allows you to enter parameters for external control signals. The 91S16 accepts external control signals through its optional P6460 External Control (Data Acquisition) Probe. The 91S16 also has two phono connectors on the back of the module; the top phono connector provides a trigger out signal (for an oscilloscope), and the bottom phono connector accepts an external start signal. The external start signal is enabled in this sub-menu. The 91S32, in stand-alone configuration, uses the P6452 External Clock (Data Acquisition) Probe connected to the DAS Trigger/Time Base module for its external control probe.

Because of the differences in these probes, the 91S16 and the 91S32 Probe sub-menus are quite different. The 91S16 Probe sub-menu will be the only Probe sub-menu available any time a 91S16 is installed in the DAS. If you are not using any extenal control signals with your pattern generator modules, you do not need to enter anything into these sub-menus.

The Timing sub-menu is exactly the same for both the 91S16 and the 91S32. To view the Timing sub-menu, move the screen cursor to the top-most field in the Probe sub-menu and press the SELECT key.

The Timing sub-menu adjusts the timing relationships between the clock, data, and strobe lines of a single P6464 Probe. You will use this sub-menu to select the master clock and adjust the timing relationships between various data and strobe lines.

This sub-menu allows you to adjust the time when each data channel outputs its signal relative to the master clock. You can use the fields in this sub-menu to move the clock (pod clock) supplied by a particular probe ± 5 ns relative to the master pattern generator clock. You can also individually program each of the data and strobe lines associated with that probe up to an additional ± 5 ns in 1 ns increments.

The Timing sub-menu also allows you to select the master pattern generator clock, either as a function of the clock supplied by the DAS, or in the case of the 91S16, as an external clock supplied by the P6460 External Control probe. 91S32s in stand-alone configuration can receive an external clock via a P6452 External Clock Probe attached to the DAS Trigger/Time Base module.

PROGRAMMING SUB-MENUS

The 91S16 and 91S32 Pattern Generator modules have three types of Programming sub-menus: Run, Trace, and Step. These sub-menu names reflect the three major pattern generator operating modes: Run mode, Trace mode, and Step mode. The Run sub-menu is the default sub-menu displayed when the PATTERN GENERATOR key pressed. It is also the most frequently used sub-menu. In addition, the Run sub-menu has a special sub-menu called TABLE BUILD used for editing existing data patterns.

You will use the Run sub-menu to enter the pattern used to stimulate your circuit under test, along with all associated programming instructions. Trace and Step sub-menus control features that help you monitor the pattern generator as it interacts with the system under test.

The Run sub-menu displays sequence lines that indicate the order of program execution. In the case of the 91S32, pattern generation will start with the lowest-numbered sequence line and progress sequentially until it reaches the highest-numbered sequence line. The 91S16 Run sub-menu allows loops and conditional branch instructions, but the same general order of execution holds true.

Each sequence line contains one or more fields in which you enter the data you want output via the P6464 pattern generation probes. Additional fields are provided for strobe and inhibit bits. The 91S16 provides additional fields for its specialized instructions.

Both the 91S16 and 91S32 Run sub-menus provide nine pattern editing instructions: CONVERT, COPY, DELETE, DISPLAY, FILL, INSERT, MODIFY, MOVE, and SEARCH. The CONVERT editing instruction displays the Table Build sub-menu. The Table Build sub-menu is used to convert an existing pattern generator program's data from one coding system to another (for example, from normal binary to the Gray code).

Trace and Step sub-menus simply display the number of clocks, sequence line being executed, and data vectors output so you can monitor program flow. Trace mode allows the pattern generator to execute its program automatically, but at a rate slow enough for you to see sequence jumps, loops, interrupt subroutines, and other structural demands on your pattern generator program. Step mode allows you to do exactly the same thing, but requires you to press the START PAT GEN key for each sequence line you want executed.

STANDARD AND OPTIONAL ACCESSORIES

91S16 PATTERN GENERATOR MODULE

The following lists include the standard and optional accessories for the 91S16 Pattern Generator Module.

Standard Accessories

2	010-6464-01	P6464 TTL/ECL Pattern Generator Probes
1	334-6094-00	91S16/32 Keyboard Overlay
1	070-5396-00	91S16, 91S32, and P6464 Operator's Addendum (English)
1	070-5398-00	91S16, 91S32 Operator's Reference Guide
1	334-6230-00	"EXTERNAL CONTROL PROBE" Label for optional P6460 Probe

Optional Accessories

010-6460-00	P6460 Data Acquisition Probe (External Control Probe)
020-1392-00	Controlled-Width Podlet
175-9676-00	Phono-to-Phono Cable (9-inch) For external start signal.
175-8165-00	Phono-to-BNC Cable (2-meters) For Trig Out signal.
070-5397-00	91S16, 91S32, and P6464 Service Addendum
003-1134-00	Delay Line Adjustment Tool

91S32 PATTERN GENERATOR MODULE

The following lists include the standard and optional accessories for the 91S32 Pattern Generator Module.

Standard Accessories

4 010-6464-01 P6464 TTL/ECL Pattern Generator Probes

1 175-9700-00 Interconnect Cable (six connector)

1 334-6094-00 91S16/32 Keyboard Overlay

1 070-5396-00 91SS16, 91S32, and P6464 Operator's Addendum (English)

1 070-5398-00 91S16, 91S32 Operator's Reference Guide

Optional Accessories

020-1392-00 Controlled-Width Podlet

003-1134-00 Delay Line Adjustment Tool

070-5397-00 91S16, 91S32, and P6464 Service Addendum

175-9782-00 Extender Interconnect Cable

P6464 TTL/ECL PATTERN GENERATOR PROBE

The following lists include the standard and optional accessories for the P6464 TTL/ECL Pattern Generator Probe.

Standard Accessories

1 070-5475-00 P6464 TTL/ECL Pattern Generator Probe Instruction Sheet

1 013-0217-00 Package of Grabber Tips (23 per probe)

1 334-6093-00 Package of Podlet Identification Labels

1 196-2963-00 Package of Lead-Sets (10 per probe)

SPECIFICATIONS

Table 1-1
ELECTRICAL SPECIFICATIONS: POWER REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
Input Power Used by 91S16		+5 V ± 3% at 8 A maximum +6 V ± 5% at 43 mA maximum +12 V ± 1.5% at 30 mA maximum −12 V ± 10% at 30 mA maximum
Input Power Used by 91S32		+5 V ± 3% at 8 A maximum +6 V ± 5% at 36 mA maximum
Output Power from Mainframe to Each P6464		+5 V ± 5% at 700 mA maximum
Output Power from Mainframe to P6460		+5 V ± 3% at 600 mA maximum −5 V ± 3% at 100 mA maximum

Table 1-2
ELECTRICAL SPECIFICATIONS: 91S16 PATTERN PROCESSOR

Characteristic	Performance Requirement	Supplemental Information
Sequence Number		0 to 1023, 1024 lines Multiple micro instructions can be programmed in the same sequence as long as instruction is different.
Internal Registers		2 8-bit registers: RA and RB RA and RB can be configured into one 16-bit register named R.
Sequence Flow Instructions		Program flow control: *(Advance to next line) IF RA=0 JUMP *to label* IF RB=0 JUMP *to label* IF R=0 JUMP *to label* IF EXT JUMP *to label* IF IRQ JUMP *to label* IF FULL JUMP *to label* IF END JUMP *to label* JUMP *to label* RETURN CALL RMT HALT Register Operation: *(Hold register value) INCR register value DECR register value LOAD register value Output Control: *Out data pattern OUT register value OUT REPeat Note: * : Default Operation () : Displayed as Blank

Table 1-3
ELECTRICAL SPECIFICATIONS: 91S32 CONTROL

Characteristic	Performance Requirement	Supplemental Information
Operating Mode		
91S32 with 91S16		
Follows 91S16		91S32 receives the clock and high speed address (up to 1K range) from 91S16. 91S32 memory divided into two 1K pages, and changes between pages when 91S16 executes INCR PAGE.
Sequential		91S32 receives only the clock from 91S16. The 91S32 address and page counter are incremented automatically by the clock.
91S32 Stand-alone		Sequential operation only
Repeat		1 to 65535 Free Run This field specifies the number of times the 91S32s will loop through their programs.
End Sequence		0 to 2047 This number specifies the last sequence line in the program; after executing the sequence line specified, the 91S32 restarts. The END SEQ field can be used when 91S32s are operating with a 91S16 in sequential mode or in 91S32 stand-alone mode.

Table 1-4
ELECTRICAL SPECIFICATIONS: PATTERN DATA

Characteristic	Performance Requirement	Supplemental Information
Number of Pattern Vectors		
91S16		1024 maximum
91S32		2048 maximum
Pattern Width		
91S16		16 parallel channels (2 strobes/91S16)
91S32		32 parallel channels (4 strobes/91S32)
		Expandable up to 176 channels with one 91S16 and five 91S32's. 16+ (32 × 5)
		Expandable up to 192 channels with six 91S32's. (32 × 6)
Data Channel Maximum Skew within Pod	1 ns at P6464 connector (no edge positioning)	Any data channels within a pod will be valid at P6464 connector within 1 ns of each other when Edge Positioning is not programmed.
Data Channel Maximum Relative Error within Pod	2 ns at P6464 connector (edge positioned)	Any data channels within a pod will be valid at P6464 connector within 2 ns + Edge Position of each other when Edge Positioning is programmed.
Data Channel Edge Positioning		Any data channel can be placed ±5 ns in 1 ns steps at P6464 probe tip centered on the Pod Clock. This is a function of the P6464 programmed via the Timing sub-menu.
Tri-State		Each data channel may be individually tri-stated (inhibited) by the pattern generator inhibit signal.
		The pattern generator inhibit signal sent to the P6464 is derived from microcode (Run sub-menu) and/or P6460 External Control Probe if 91S16 exists. or from P6452 External Clock Probe through Trigger/Timebase Module if only 91S32s installed.

Table 1-4 (cont.)
ELECTRICAL SPECIFICATIONS: PATTERN DATA

Characteristic	Performance Requirement	Supplemental Information
Vector Source for Pod A (91S16 only)		Data pattern, RA, RB, R (Low byte only) or Repeat previous Pod A value (OUT REP)
Vector Source for Pod B (91S16 only)		Data pattern or R (High byte only) *NOTE: Not RB, and not high byte of OUT REP*

Table 1-5
ELECTRICAL SPECIFICATIONS: STROBE AND CLOCK OUTPUTS

Characteristic	Performance Requirement	Supplemental Information
Strobe Output		1 strobe line per P6464
Number of Strobes		
91S16		2 strobes
91S32		4 strobes
Strobe Polarity		Strobe polarity can be programmed the same as pattern data.
Strobe Maximum Skew Relative to Data Channels Within Pod		
ECL	1 ns at P6464 connector (no edge positioning)	Strobe will be valid at P6464 connector within 1 ns (ECL) or 1.5 ns (TTL) with respect to other data channels in the same pod when Edge Positioning is not programmed.
TTL	1.5 ns at P6464 connector (one TTL load) (no edge positioning)	
Strobe Maximum Relative Error Within Pod	2 ns at P6464 connector (edge positioned)	Strobe will be valid at P6464 connector within 2 ns + Edge Position with respect to other data channels in the same pod when Edge Positioning is programmed.
Strobe Edge Positioning		Strobe can be positioned ±5 ns in 1 ns steps at P6464 probe tip centered on the Pod Clock. This function is controlled in the Timing sub-menu.
Tri-State		Strobe may be tri-stated (inhibited) by the inhibit signal. The pattern generator inhibit signal sent to the P6464 is derived from microcode (Run-sub menu) and/or P6460 External Control Probe if 91S16 exists, or from P6452 External Clock Probe through Trigger/Time Base Module if only 91S32's used.
Pod Clock Output		1 clock line per P6464 probe can be used as a Pod Clock.
Number of Pod Clocks		
91S16		2 Pod Clocks
91S32		4 Pod Clocks
Pod Clock Polarity		Rising or Falling Edge, menu-selectable

Table 1-5 (cont.)
ELECTRICAL SPECFICATIONS: STROBE AND CLOCK OUTPUTS

Characteristic	Performance Requirement	Supplemental Information
Pod Clock Pulse Width (at P6464 Connector)		
Internal Clock		⩾ 8 ns
External Clock		Input pulse width ±6 ns Clock pulse comes from P6460 External Control Probe if 91S16 exists, or from P6452 External Clock Probe through Trigger/Time Base Module if only 91S32's used.
Pod Clock Delay from External Clock Input		102 ns typical. Refer to Figure 1-5.

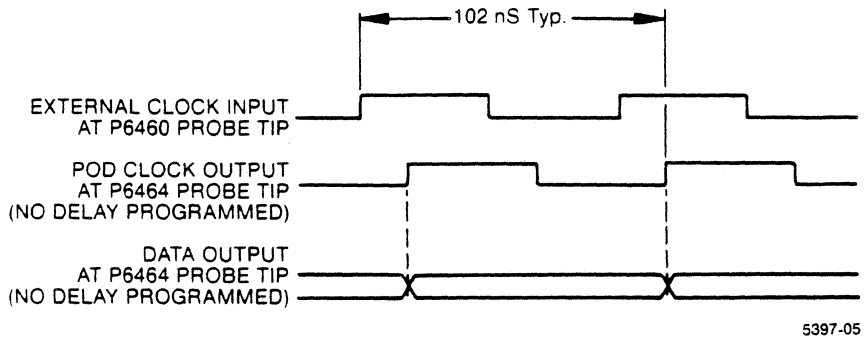


Figure 1-5. Pod Clock/Data Output Delay from External Clock Input.

Table 1-5 (cont.)
ELECTRICAL SPECFICATIONS: STROBE AND CLOCK OUTPUTS

Characteristic	Performance Requirement	Supplemental Information
Pod Clock Maximum Skew Between Pods		Add 3 ns for maximum skew at P6464 probe tip if adjusted without probe.
Within 91S16 or 91S32	2 ns at P6464 connector (no edge positioning)	Edge of any Pod Clock within 91S16 or within 91S32 will occur at P6464 connector within 2 ns of each other when Edge Positioning is not programmed.
Between 91S16 and First 91S32	3 ns (adjusted as a set) 7ns (adjusted as a module) at P6464 connector (no edge positioning)	Edge of any Pod Clock within 91S16 and first 91S32 will occur at P6464 connector within 3 ns (adjusted as a set) or 7 ns (adjusted as a module) of each other when Edge Positioning ia not programmed.
Between 91S32's	4 ns (adjusted as a set) 8 ns (adjusted as a module) at P6464 connector (no edge positioning)	Edge of any of 91S32 Pod Clock will occur at P6464 connector within 4 ns (adjusted as a set) or 8 ns (adjusted as a module) of each other when Edge Positioning is not programmed.
Pod Clock Maximum Relative Error between Pods		Add 3 ns for maximum relative error at P6464 probe tip if adjusted without probe.
Within 91S16 or 91S32	4 ns at P6464 connector (edge positioned)	Edge of any Pod Clock within 91S16 or within 91S32 will occur at P6464 connector within 4 ns + Edge Position of each other when Edge Positioning is programmed.
Between 91S16 and First 91S32	5 ns (adjusted as a set) 9 ns (adjusted as a module) at P6464 connector (edge positioned)	Edge of any Pod Clock and first 91S32 will occur at P6464 connector within 5 ns + Edge Position (adjusted as a set) or 9 ns + Edge Position (adjusted as a module) of each other when Edge Positioning is programmed.
Between 91S32's	6 ns (adjusted as a set) 10 ns (adjusted as a module) at P6464 connector (edge positioned)	Edge of any 91S32 Pod Clock will occur at P6464 connector within 6 ns + Edge Position (adjusted as a set) or 10 ns + Edge Position (adjusted as a module) of each other when Edge Positioning is programmed.

TABLE 1-5 (cont.)
ELECTRICAL SPECFICATIONS: STROBE AND CLOCK OUTPUTS

Characteristic	Performance Requirement	Supplemental Information
Pod Clock Edge Positioning	±5 ns in 5 ns steps	Pod Clock can be positioned in −5 ns to +5 ns range in 5 ns steps. Programmable.
Tri-State		Pod Clock may be tri-stated (inhibited) by the inhibit signal. The pattern generator inhibit signal sent to the P6464 is derived from microcode (Run sub-menu) and/or P6460 External Control Probe if 91S16 exists. or from P6452 External Clock Probe through Trigger/Time Base Module if only 91S32's used.

Table 1-6
ELECTRICAL SPECIFICATIONS: CLOCK RATE

Characteristic	Performance Requirement		Supplemental Information
Operating Rate, Run Mode			
91S16			Up to 50 MHz (20 ns cycle time) internal clock or external clock
91S32			
With 91S16			Up to 50 MHz (20 ns cycle time) internal clock (Pod clock delay set to −5 ns) or 25 MHz (40 ns cycle time) external clock
Stand-Alone			Up to 50 MHz (20 ns cycle time) internal clock (Pod clock delay set to 0 ns)
			Up to 25 MHz (40 ns cycle time) external clock
Clock			
Source			Internal or external, selectable
Internal			From Trigger/Time Base Module of the Mainframe
External			From P6460 External Control Probe if 91S16 exists, or from P6452 External Clock Probe through Trigger/Timebase Module if only 91S32's used.
Polarity			Rising or falling edge, selectable
	91S16	91S32 (Stand-Alone)	
Period	20 ns min	20 ns int. ck. 40 ns ext. ck.	
Pulse High	9 ns min	19 ns min	
Pulse Low	9 ns min	19 ns min	

Table 1-7
ELECTRICAL SPECIFICATIONS: 91S16 EXTERNAL CONTROL SIGNALS

Characteristic	Performance Requirement	Supplemental Information
Using P6460 Probe		External control signals for 91S16 are obtained from P6460 External Control Probe.
Input Threshold Range	−6.40 V to +6.35 V in 50 mV steps	
Threshold Accuracy		Indicated value ±.5% ± 6.5 mV
Minimum Logic Swing		0.5 V peak-to-peak, centered on the threshold
External Clock Input		1 external clock line (edge selectable) 9 ns minimum puise width
Interrupt Input		1 interrupt line (edge selectable)
Interrupt Processing Cycle Delay		1 cycle When a valid interrupt request is logged in, the first interrupt vector appears at P6464 probe tip in the cycle where the interrupt has been sampled.
Interrupt Minimum Pulse Width		15 ns
Interrupt Input Timing Window Prior to External Clock Input		10 ns typical To be recognized in a certain cycle. assert the interrupt request in a range of 10 ns prior to the selected edge of the external clock, otherwise it will be recognized in the next cycle.
Interrupt Input Timing Window Prior to Pod Clock Output		104 ns typical To be recognized in a certain cycle, assert the interrupt request in a range of 104 ns prior to Pod clock selected edge output, otherwise recognized in the next cycle.
Interrupt Latency		1 cycle time Second interrupt can be latched in the next cycle after the first interrupt has been started.
Interrupt Service Call		1 level The stack used to save the return address for the interrupt service call has 1 level.

Table 1-7 (cont.)
ELECTRICAL SPECIFICATIONS: 91S16 EXTERNAL CONTROL SIGNALS

Characteristic	Performance Requirement	Supplemental Information
Interrupt Mask		Mask bit in microcode disables receipt of an interrupt as long as it is "1".
Interrupt Mask Timing Window		11 ns typical. Refer to Figure 1-6. 11 ns typical after the rise/fall edge selected to 11 ns typical to the next rise/fall edge selected the external clock
Interrupt Qualifier Input		1 qualifier line (level selectable) An interrupt is recognized if the selected edge is detected on the interrupt line only when the qualifier line stays high or low as specified.
Interrupt Qualifier Input Minimum Pulse Width		15 ns
Interrupt Qualifier Input Setup Time Relative to Interrupt		15 ns minimum Maintain qualifier line high or low for 15 ns prior to the selected edge of the interrupt.
Interrupt Qualifier Input Hold Time Relative to Interrupt		0 ns maximum Maintain qualifier line high or low after the selected edge of the interrupt.
External Jump Input		1 external jump (level selectable) Pattern will branch on "IF EXT JUMP" instruction if the EXT JUMP line is activated when the instruction is tested.
External Jump Minimum Pulse Width		15 ns
External Jump Input Setup Time Relative to External Clock Input		15 ns minimum 10 ns typical Assert the external jump request 15 ns prior to the selected edge of the external clock.
External Jump Input Hold Time Relative to External Clock Input		0 ns maximum Assert the external jump request 0 ns after the selected edge of the external clock.
External Jump Input Setup Time Relative to Pod Clock Output		105 ns + 1 clock cycle typical Assert the external jump request 105 ns + 1 clock cycle prior to the Pod Clock selected edge output.

Table 1-7 (cont.)
ELECTRICAL SPECIFICATIONS: 91S16 EXTERNAL CONTROL SIGNALS

Characteristic	Performance Requirement	Supplemental Information
External Inhibit Input		1 external inhibit line (level selectable) External inhibit is ANDed/ORed with internal inhibit according to selection in Probe sub-menu.
External Inhibit Minimum Pulse Width		15 ns
External Inhibit Delay		40 ns typical. Refer to Figure 1-7.
Pause Input		1 pause line (level selectable) Freezes the current data outputs while pause line remains true.
Pause Input Minimum Pulse Width		15 ns
Pause Input Setup Time Relative to External Clock Input		15 ns minimum 10 ns typical Assert the pause request 15 ns prior to the selected edge of the external clock.
Pause Input Hold Time Relative to External Clock Input		0 ns
Pause Input Setup Time Relative to Pod Clock Output		59 ns typical Assert the pause request 59 ns prior to the selected edge of the Pod Clock output.

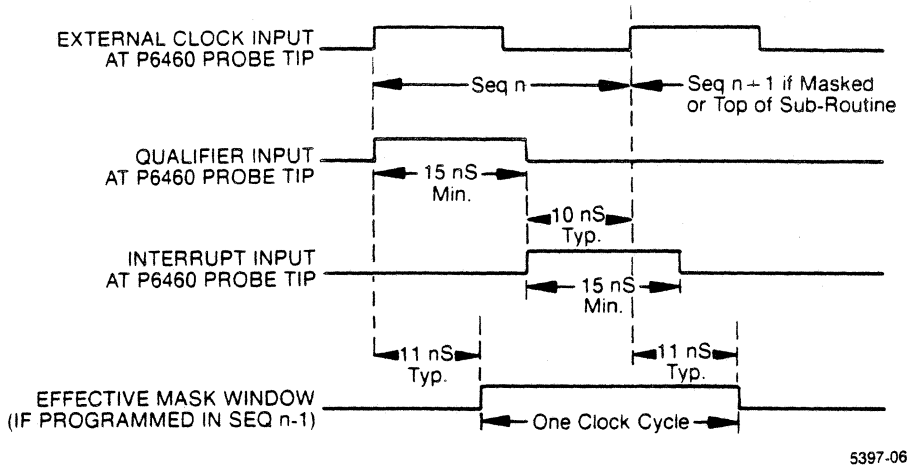


Figure 1-6. Interrupt/qualifier and mask timing.

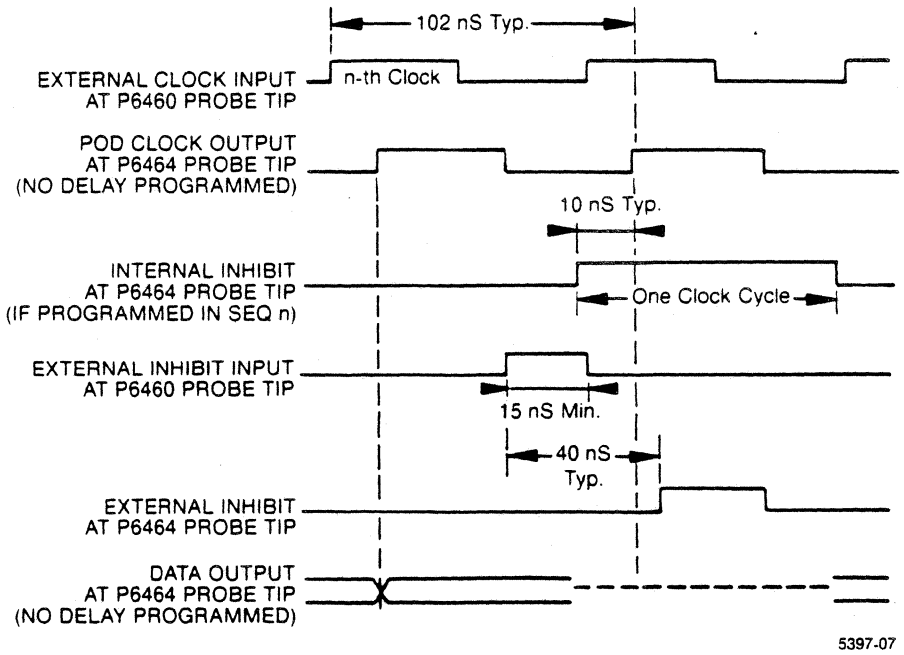


Figure 1-7. Internal and external inhibit timing diagram.

Table 1-8
ELECTRICAL SPECIFICATIONS: EXTERNAL START INPUT AND TRIGGER OUTPUT

Characteristic	Performance Requirement	Supplemental Information
External Start Input		TTL-level input (edge selectable); phono connector; 2 LS TTL fan-in The pattern generator automatically starts when the external start signal is asserted after once pressing the START PAT GEN or START SYSTEM key on the keyboard.
External Start Input Minimum Pulse Width		15 ns minimum
Trigger Output		TTL-level output; phono connector; 5 STD TTL fan-out A TTL high-level signal occurs on the trigger output for 1 clock cycle when the 91S16 executes the TRIGGER instruction.
Trigger Output Timing		
Relative to Pod Clock Output		−46 ns Trigger signal occurs 46 ns prior to the selected edge of the pod clock output when no delay is programmed.
Relative to External Clock Input		56 ns Trigger signal occurs 56 ns after the selected edge of the external clock.

Table 1-9
ELECTRICAL SPECIFICATIONS: 91S32 EXTERNAL CONTROL SIGNALS

Characteristic	Performance Requirement	Supplemental Information
Using P6452 Probe		External control signals for 91S32 in stand-alone configuration are obtained from P6452 External Clock Probe attached to DAS Trigger/Time Base Module.
Input Threshold Range		−2.5 V to +5.00 V in 50 mV steps
Input Threshold Accuracy		Menu-selected value ±2% ±100 mV
Minimum Logic Swing		0.5 V peak to peak centered on the threshold.
External Clock Input		1 external clock line (edge selectable) 19 ns minimum pulse width
External Inhibit Input		1 external inhibit line (level selectable) External inhibit is ANDed/ORed with internal inhibit according to menu selections in the Probe sub-menu.
External Inhibit Minimum Pulse Width		19 ns
External Inhibit Delay		76 ns minimum. When external inhibit line is asserted. the data outputs will be inhibited or tri-stated 76 ns after the external inhibit signal is asserted.

Table 1-9 (cont.)
ELECTRICAL SPECIFICATION: 91S32 EXTERNAL CONTROL SIGNALS

Characteristic	Performance Requirement	Supplemental Information
Pause Input		1 pause line (level selectable) Freezes the current data outputs while pause line remains true.
Pause Input Minimum Pulse Width		19 ns
Pause Input Setup Time Relative to External Clock Input		19 ns minimum Assert the pause request 19 ns prior to the selected edge of the external clock.
Pause Input Hold Time Relative to External Clock Input		0 ns max Assert the pause request 0 ns after the selected edge of the external clock.
Pause Input Setup Time Relative to Pod Clock Output		120 ns minimum 108 ns typical Assert the pause request 120 ns prior to Pod Clock selected edge output.
External Start Input		The pattern generator automatically starts when the external start signal is asserted after once pressing the START PAT GEN or START SYSTEM key on the keyboard.
External Start Input Minimum Pulse Width		19 ns minimum
External Start Input Setup Time Relative to External Clock Input		14 ns minimum 5 ns typical
External Start Input Hold Time Relative to External Clock Input		5 ns minimum 0 ns typical

Table 1-10
P6464 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
Clock In, Maximum Frequency	50 MHz (20 ns)	
Power Required		Power required per channel from user's circuit. Voltages referenced to instrument ground.
V_H		−.5 V to +5.5 V at 55 mA + I load (user's more positive supply voltage)
V_L		+.3 V to −5.5 V at 63 mA + I load (user's more negative supply voltage)
$V_H - V_L$		4.8 V to 5.2 V (within individual probes)
Pin Driver Outputs: Data, Clock, Strobe		
TTL Mode	$V_{L\ OUT} = V_L + .75$ V $V_{H\ OUT} = V_H - 1$ V	
Drive Capability	sink or source > 20 mA	
Transition Time		3.5 ns maximum (20% to 80% of logic level), resistive load
ECL Mode	$V_{L\ OUT} = V_H - 1.65$ V $V_{H\ OUT} = V_H - 1$ V	Nominal open emitters
Drive Capability	20 mA (50Ω to V_H −2 V)	50 pF maximum
Transition Time		2.5 ns maximum (20% to 80% of logic level), resistive load

Table 1-11
P6464 ENVIRONMENTAL SPECIFICATIONS

Characteristic	Description
Temperature	
Operating	0°C to +50°C
Storage	−55°C to +75°C
Humidity	90% to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft.) maximum
Storage	15 km (50,000 ft.) maximum

Table 1-12
P6460 ELECTRICAL SPECIFICATIONS

Characteristic	Description
User's Ground Sense	<100 Ω to user's ground
Input Impedance	1 MΩ ± 1%, 5 pF nominal; lead set adds approx. 5 pF
Max. Non-Destructive Input Voltage Range	± 40 V (DC + peak AC)
Max. Voltage Between Any Two Inputs	± 60 V (DC + peak AC)
Operating Input Voltage Range	From −40 V to input threshold's voltage + 10 V (+30 V for RS-232 only)
Threshold Offset and Accuracy	± 0.25% of threshold ± 50 mV
Minimum Input Swing	0.5 V peak-to-peak, centered on the threshold
Minimum Pulse Width (with input 250 mV over the threshold from +0.5 V and −0.5 V)	4 ns at threshold

Table 1-13
P6460 ENVIRONMENTAL SPECIFICATIONS

Characteristic	Description
Temperature	
Operating	−15° C to +55° C
Storage	−62° C to +75° C
Humidity	95% to 97% relative humidity
Altitude	
Operating	4.5 km (15,000 ft.) maximum
Non-operating	15 km (50,000 ft.) maximum

LIST OF ILLUSTRATIONS (cont.)

LIST OF TABLES

OPERATOR'S SAFETY SUMMARY

The general safety information in this summary is for both operator and service personnel. Specific cautions and warnings are found throughout the addendum where they apply but may not appear in this summary.

TERMS IN THIS ADDENDUM

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS AS MARKED ON EQUIPMENT

 **DANGER** - High voltage.

 Protective ground (earth) terminal.

 **ATTENTION** - refer to manual.

GROUNDING THE PRODUCT

The mainframe in which this product is installed is intended to operate from a power source that does not apply more than 250 V rms between the supply conductors or between either supply conductor and ground.

This product is grounded through the mainframe in which it is operating. To avoid electrical shock, plug the power cord of the mainframe into a properly wired receptacle before connecting to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

OPERATOR'S SAFETY SUMMARY (cont.)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective ground connection, all accessible conductive parts (including keys and controls that may appear to be insulated) can render an electric shock.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury, do not operate this product without mainframe covers or panels installed. Circuit boards and components can become very hot during operation.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been spefically certified for such operation.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operator's Safety Summary.

DO NOT SERVICE ALONE

Do not perform service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before soldering or replacing components.

DO NOT WEAR JEWELRY WHEN SERVICING

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages.

NOTE

Observe safety precautions stated in the DAS 9100 Series Service Manual concerning CRT safety, X-ray emission, and loose objects.

OPTIONS

There are no options to the 91S16 or 91S32 Pattern Generator modules.

SECTION 3
OPERATING INSTRUCTIONS

This section describes installation requirements for the 91S16 and 91S32 Pattern Generator modules and their probes. It also provides a description of operator's checkout procedures for the modules and probes. If your instrument has a lower serial number, have a qualified service technician verify that you have the 22 ampere supply installed. Refer the technician to *Service Information: Verifying Installation of the Upgraded + 5 V Power Supply* in the *Test and Verification* section of this addendum.

Repackaging Information. All 9100 Series products are shipped in specially designed transportation packaging. Keep this packaging for use whenever you ship DAS products. If the original packaging is no longer fit for use, contact your nearest Tektronix Field Office and obtain new DAS packaging.

If you need to ship any part of your 91S16 or 91S32 system to a Tektronix Service Center, please send in all parts of your system: the 91S16 and/or 91S32s and all of their probes.

When you ship a product to a Tektronix Service Center, be sure to attach an identifying tag to the product (inside the packaging). On this tag include your name, the name of your company, the name and serial number of the enclosed product, and a description of the service requested.

CONFIGURATION AND UPDATE REQUIREMENTS

CONFIGURATION REQUIREMENTS

The 91S16 module can be installed in any DAS slot supplied by the upgraded 22 ampere 5 volt power supply (p/n 620-0296-01). DAS 9100 instruments with the following serial numbers and greater will automatically have the upgraded power supply installed:

- Monochrome DAS 9109, serial numbers B050326 and higher
- Color DAS 9129, serial numbers B060100 and higher
- DAS 9119, serial numbers B010102 and higher

If your instrument has a lower serial number, have a qualified service technician verify that you have the 22 ampere supply installed. Refer the technician to the section at the back of this addendum (behind the goldenrod page) titled *Service Information: Verifying Installation of the Upgraded + 5 V Power Supply.*

Only one 91S16 module may be installed in the DAS system. If first generation 91P16/P32 Pattern Generator modules are installed in the DAS, you must remove them; you cannot have both 91S16/S32 and 91P16/P32 modules installed at the same time.

The 91S32 module can be used as a channel expander for the 91S16 or as discrete pattern generator. A maximum of five 91S32 modules can be installed with one 91S16 module, or a maximum of six 91S32s can be installed without a 91S16. 91S32s can be installed in any DAS slot supplied by the upgraded 22 ampere 5 volt power supply.

When more than one pattern generator module is installed in the DAS, the modules are connected by a ribbon cable which attaches to the top of each circuit board. This ribbon cable distributes clock signal to each module, and provides addresses and control signals to the 91S32s when used in FOLLOWS 91S16 mode.

As an expander, the first 91S32 module must be in the slot next to the 91S16. Additional 91S32 modules need to be in adjacent slots.

NOTE

91A04A and 91AE04A Data Acquisition Modules must be installed in slot numbers higher than the 91S16 and 91S32 modules.

91S32 TERMINATOR CONNECTORS. 91S32 modules contain a series of terminator connectors immediately below the interconnect cable card-edge connectors. These connectors are used to terminate the clock, address, and control signals passed over the interconnect cable. Only the 91S32s at the end of the signal path should have these terminators in place; you should remove the terminators from all intermediary boards.

When a 91S16 is used to control 91S32s, the 91S16 provides the clock and address signals. Hence, only the 91S32 farthest from the 91S16 should have its terminators installed (15 terminators). The following pin numbers should have terminators in place: J202, J204, J302, J304, J306, J308, J310, J312, J314, J316, J318, J320, J322, J324, and J102. J102 is located below and to the right of the other terminator connectors. The only pins that should not have terminators installed are J206 and J208. Refer to Figure 3-1.

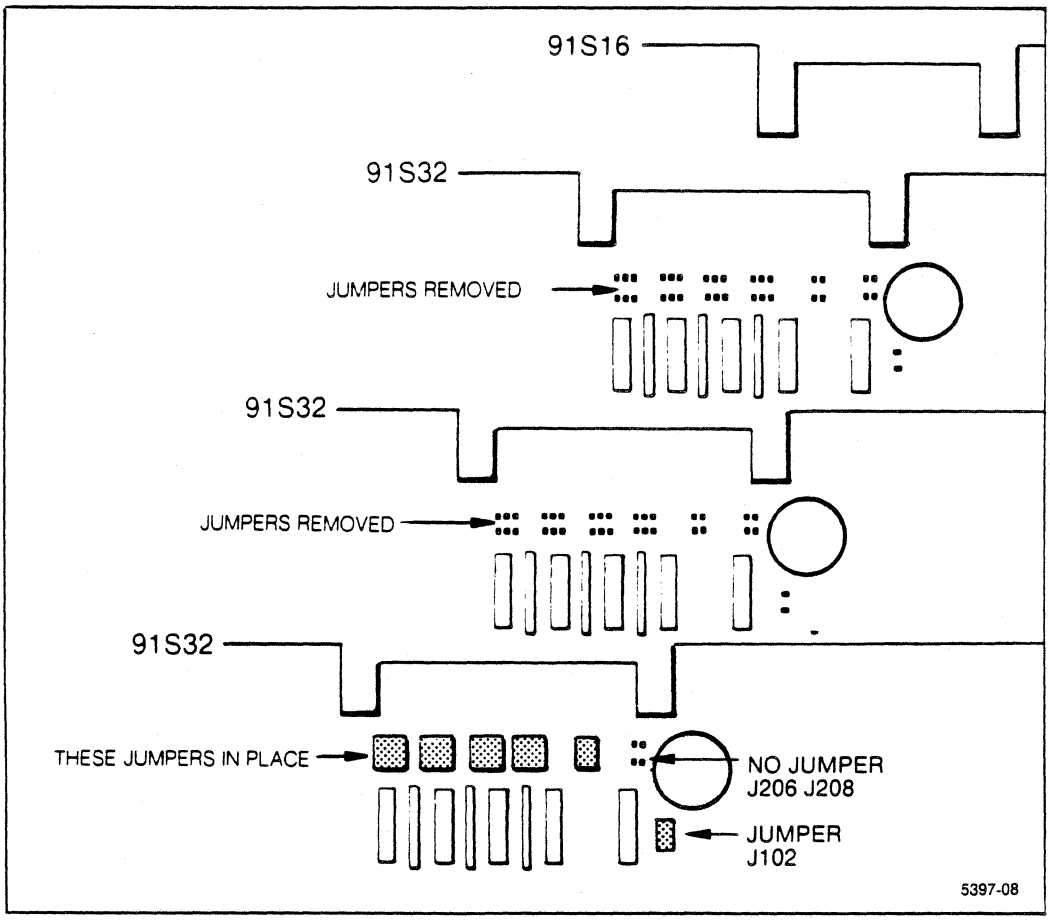


Figure 3-1. Terminator configuration for 91S32s with 91S16.

When 91S32s are used without a 91S16 module, the outermost 91S32 modules should have the following terminators in place: J206 and J208. Remove the rest of the terminators. Any intermediate 91S32 modules should have all their card-edge connector terminators removed. (No terminator on J102.) Refer to Figure 3-2.

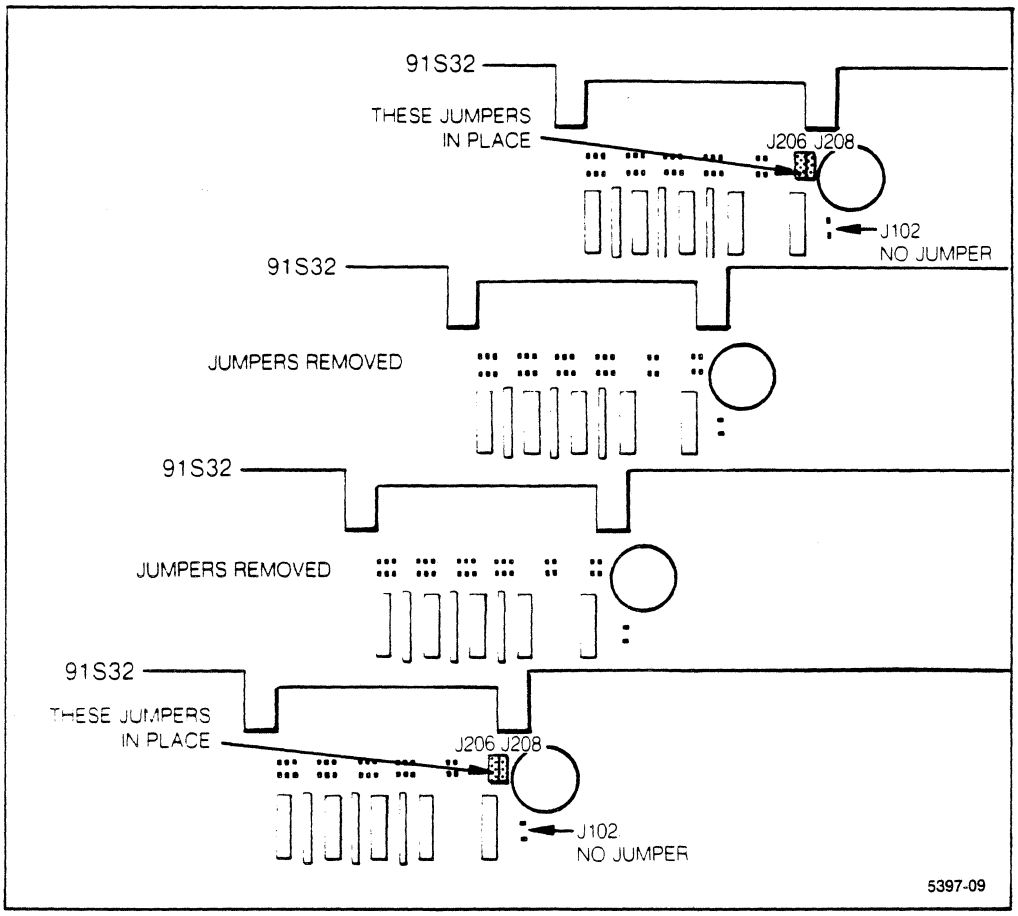


Figure 3-2. Terminator configuration for stand alone 91S32s.

MODULE INSTALLATION

The following paragraphs assume you are already familiar with the procedures for removing the mainframe top panel and cover, and with the procedures for installing modules into the mainframe bus slots. If you are not familiar with these procedures, refer to the *Operating Instructions* section of the *DAS 9100 Series Operator's Manual.*

Do not remove or install a 91S16 or 91S32 module until you have read the following warnings, cautions, and configuration requirements.

WARNING

When installing or removing instrument modules, the operator may gain access to the mainframe's module compartment only. Unless you are a qualified service technician, do not open any other compartments within the mainframe. Other compartments contain hazardous voltages.

CAUTION

When modules are being installed, the mainframe should be turned off and unplugged from its power source. Damage to the module's circuitry may occur if the module is installed while the mainframe is receiving power.

Installing a Module into the DAS

Figure 3-3 illustrates the location of a module in the mainframe. Refer to the figure while reading the following instructions.

CAUTION

If a 91S16 or 91S32 module is installed in a slot that is not supplied by the 22 amp 5 volt power supply, the module may not function correctly due to current overload.

As long as all DAS bus slots are supplied by the 22 amp +5 V power supply, there are no power-related slot restrictions.

- Be sure power is off and the power cord is unplugged before attempting to install a module.
- Refer to *Section 2: Operating Instructions* in the *DAS 9100 Series Service Manual* (p/n 062-5848-00) for instructions on removing the mainframe top panel and module compartment cover.

CAUTION

The module may be damaged if it is installed or removed while the mainframe is receiving power.

1. Remove the mainframe top panel and module compartment cover. *Do not remove the power supply cover.*
2. Position the module over the selected bus slot, with the yellow rejector tab toward the front of the mainframe. Make sure this tab is parallel to the module.
3. Insert the module between the guide slots at the top of the mainframe. This procedure is easiest if you align the module with the rear guide first.
4. Slide the module down through the slots until its connectors rest on top of the bus slot connectors on the interconnect board.
5. Push the module down into the bus slot connectors. Press firmly on the board but do not press on components.

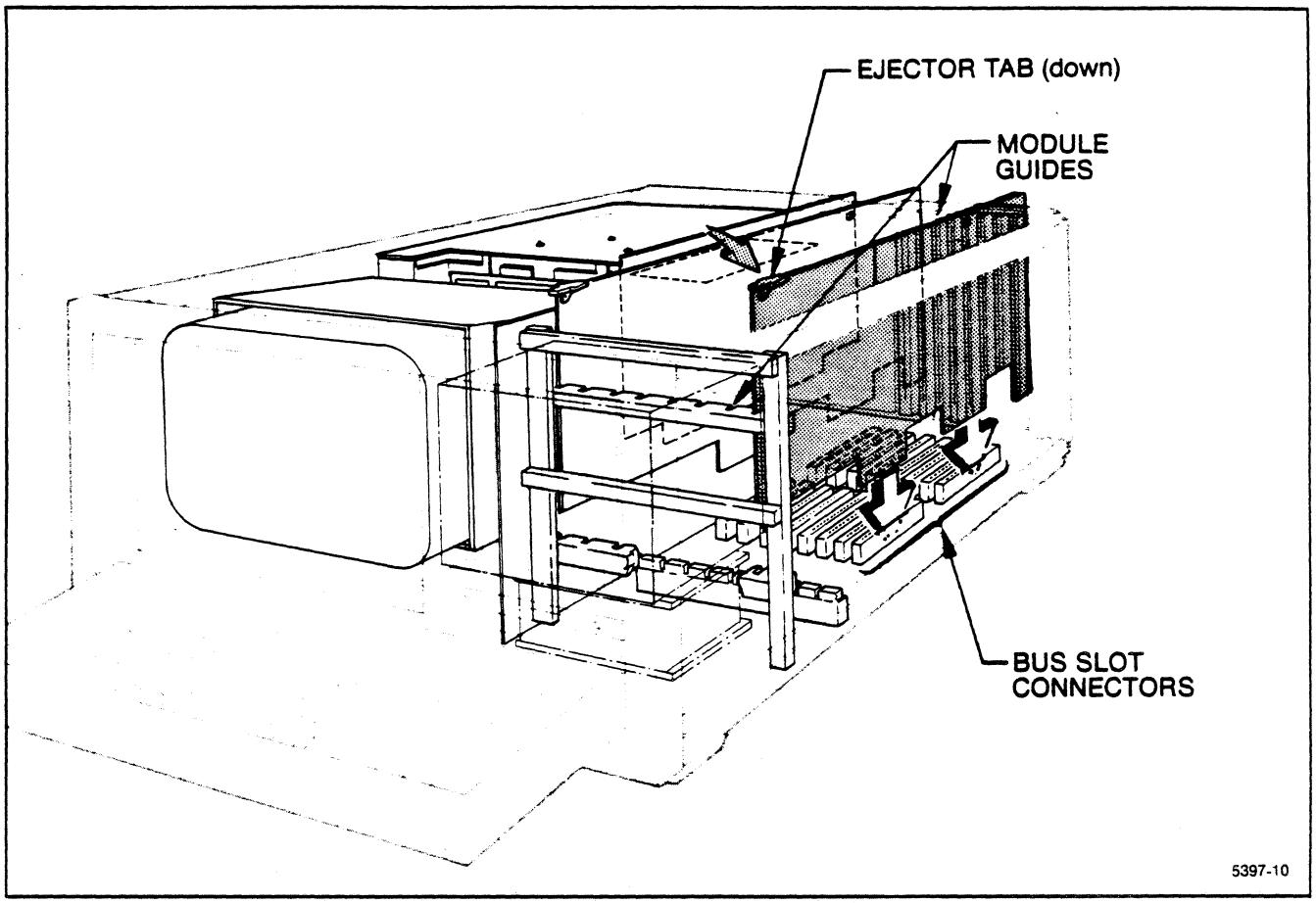


Figure 3-3. Installing an instrument module in the mainframe.

Installing the Interconnect Cable

Each 91S32 is shipped with a six-connector interconnect cable. This cable distributes the clock signal from the 91S16, or from the 91S32 nearest the Trigger/Time Base module, to the rest of the 91S32s installed in the DAS. It also distributes the vector RAM address to the 91S32s when operating in Follows 91S16 mode.

You must cut any unnecessary connector blocks off of your interconnect cable or system performance will be degraded. Use a sharp razor blade to trim the unneeded cable and connector blocks off. Make your cut as close to the last needed connector block as possible. Do not leave any frayed ends.

To install the interconnect cable, simply align the connector blocks with the card edge connectors on top of each 91S16 and 91S32 module, and press the connector blocks firmly in place. When seated, the top of the connector blocks should be roughly level with the top of the circuit boards. The red line on the interconnect cable should face toward the back of the DAS mainframe.

CONNECTING THE PATTERN GENERATOR PROBES

The 91S16 and 91S32 Pattern Generator modules use both pattern generator probes (to output singals) and an external control probe (to acquire external clock, inhibit, pause, etc.). The P6464 Pattern Generator probe supplies the pattern to the system under test for both 91S16 and 91S32 modules. The external control probe acquires external clock, interrupt, pause, (etc.) signals from an external device and provides them to the pattern generator. There are two different external control probes; one used when a 91S16 is installed in the DAS, and a different probe for when only 91S32s are present.

The 91S16 uses a P6460 Data Acquisition probe as an external control probe. This optional probe is refered to as the P6460 External Control Probe in this addendum. Any time a 91S16 module is installed in the DAS, the P6460 serves as the external control probe. The 91S16 also has two miniature phono connectors on the back of the module for EXT START (external start) and TRIG OUT (trigger-out) signals.

If only 91S32s are installed in the DAS, the P6452 Data Acquisition Probe attached to the DAS Trigger/Time Base module serves as the external control probe. This DAS standard accessory probe is referred to as the P6452 External Clock Probe in this addendum.

Specifictions for the P6464 and P6460 probes can be found in the *Specifications* section of this addendum. Specifications for the P6452 probe can be found in the *DAS 9100 Series Operator's Manual.*

Connecting P6464 Pattern Generator Probes

The P6464 can be used with either 91S16 or 91S32 Pattern Generator modules. The 91S16 has three pod connector locations (from top to bottom: A, B, and C). The first two locations can accommodate one P6464 TTL/ECL Pattern Generator Probe each. The bottom connector is for the optional P6460 Data Acquisition Probe. The 91S32 has four pod connector locations (from top to bottom: A, B, C, and D). All four locations accommodate one P6464 each.

When connecting a probe to a module, first find the bus slot where that module is installed. Once you have identified the correct bus slot, look through the back-panel opening and locate the pod connectors.

WARNING

Stop the pattern generator before connecting or disconnecting a probe. Failure to stop the pattern generator may result in damage to the pattern generator module.

NOTE

When connecting probes to a module with more than one pod connector, it is easiest to connect the first probe to the bottom connector and then work up.

NOTE

If you inadvertently connect an acquisition probe to a pattern generator pod (or vice versa) on the 91S16 or 91S32, the DAS will not notify you of this error. Damage will not occur to the probe.

Refer to Figure 3-4. when reading the following paragraphs.

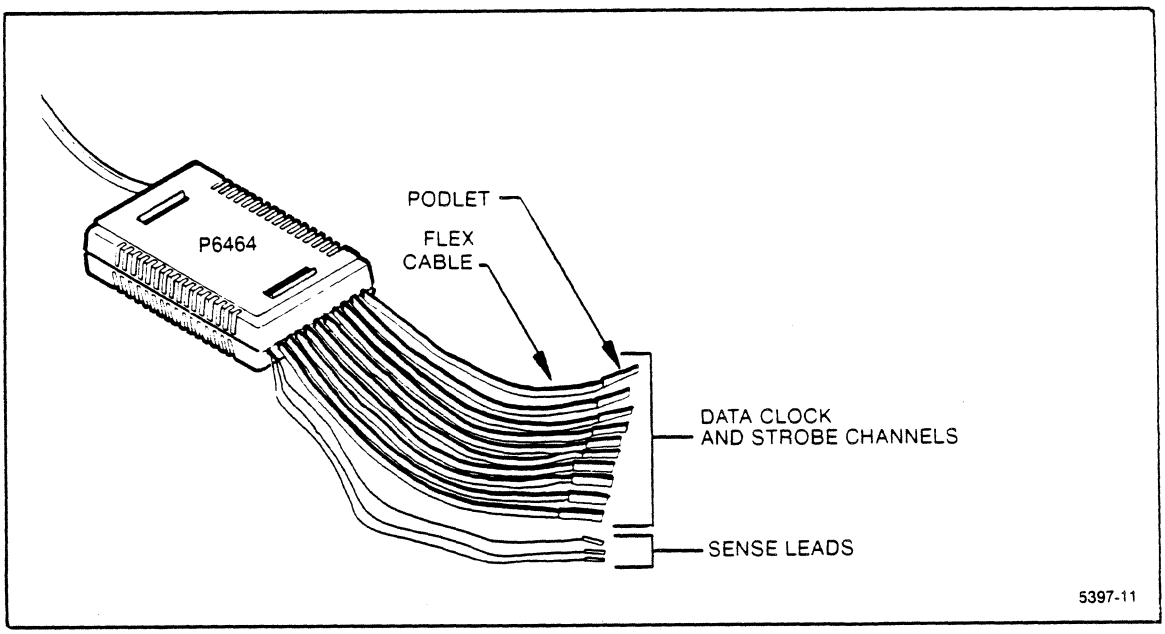


Figure 3-4. P6464 Pattern Generator Probe.

The stimulus output of the P6464 probe consists of eight data channels, one clock line, and one strobe line. Each output consists of an active pin driver (podlet) at the end of an individual flex cable. The podlets are designed to slip over .025 inch square pins on your circuit. The square pins should be on 0.1 inch centers (0.125 inch centers between pairs of square pins). Use gold-plated pins to prevent corrosion within the podlet connectors.

If your circut does not have square pins, use the grapper tips and lead sets that are provided. One end of each lead set plugs into the podlet and the other ends slip inside the grapper tips.

The P6464 recieves power from your circuit through three sense leads conncted to the front on the probe. The red lead (VH) is connected to the higher voltage, the black (VL) lead is connected to the lower voltage , and the green lead is connected to ground. VH must be connected to a power source of −0.5 V to +5.5 V. VL must be connected to a power source of +0.3 V to −5.5 V. However, the difference between VH and VL must be 4.8 to 5.2 V.

Connecting the P6460 External Control Probe to the 91S16

The P6460 External Control Probe should be connected to Pod C of the 91S16 Pattern Generator module. If you connect this probe to the wrong pod connector, the DAS will not indicate an error; however, no damage will occur.

The optional P6460 External Control Probe used with the 91S16 Pattern Generator module is the same probe labeled P6460 Data Acquisition Probe used with the 91A24 and 91AE24 Data Acquisition Modules. For our purposes, attach the self-adhesive "P6460 EXTERNAL CONTROL PROBE" label supplied with the 91S16 module. This label should be applied directly over the existing label on the top of the probe.

Figure 3-5 illustrates the various elements and features of the P6460 probe. Refer to this figure when reading the following paragraphs.

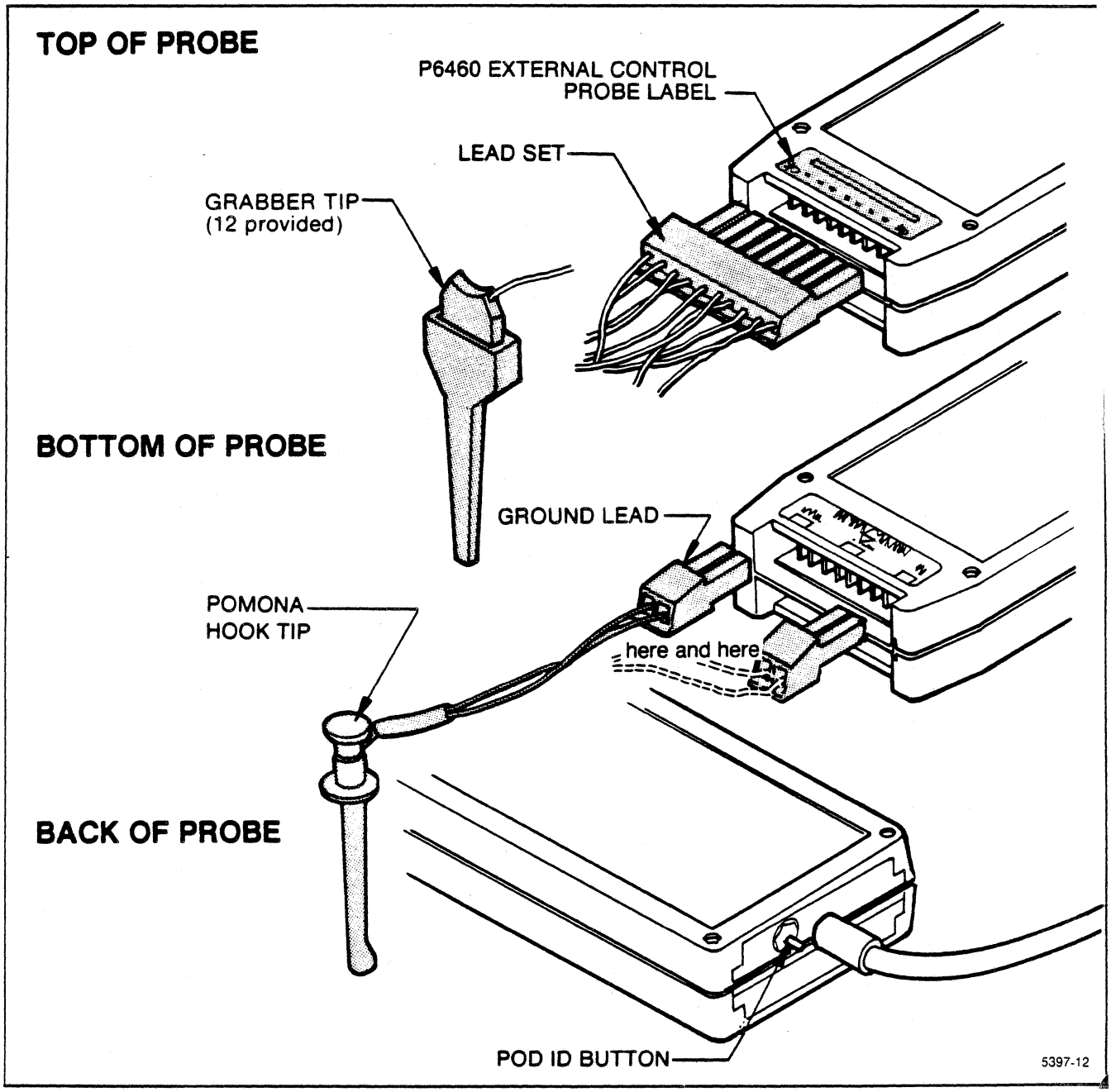


Figure 3-5. P6460 External Control Probe.

Probe Leads and Tips. Each P6460 probe is supplied with a 10-inch lead set and a package of 12 probe tips (grabber type). Figure 12 shows the connection of leads and tips.

Connect the lead set to the probe, making sure that the set's white lead is on the side of the probe housing labeled CK (clock). Push the lead set's connector into the probe housing. To disconnect the lead set, pull on its connector; do not pull on the leads.

Ground Lead Connections. Also provided with each P6460 are two 5-inch ground sense leads with Pomona Hook tips, and two alligator-clip lead tips. Plug both sets of ground leads into the probe housing's connectors labeled USERS GND as shown in Figure 3-5.

The middle GND connector, labeled ⚠, should only be used when the diagnostic lead set is connected to the probe.

Maximum Non-Destructive Input Voltage. The maximum input voltage which may be used with the P6460 probe is ±40 V peak.

Probe circuitry may be damaged if the P6460 is connected to a voltage source greater than ±40 V peak.

Connecting the EXT START and TRIG OUT Phono Connectors to the 91S16

The 91S16 has two minature phono connectors below the probe connectors on the back of the module. The top phono jack (J180) outputs the external trigger (TRIG OUT) signal to some external device (typically an oscilloscope). Use the optional 2-meter phono-to-BNC connector cable for this purpose.

The bottom minature phono jack (J160) receives the external start signal. Typically, you will use the 9-inch phono-to-phono cable to connect the output of an acquisition module to this external start input jack.

Connecting the P6452 External Clock Probe to the Trigger/Time Base Module (91S32 Stand Alone)

Instructions for connecting the P6452 External Clock Probe to the DAS Trigger/Time Base module can be found in the *Operating Instructions* section of the *DAS 9100 Series Operator's Manual.* The P6452 probe can be used as the external signal source for the 91S32 Pattern Generator modules in stand alone configuration; the optional P6460 probe serves as the external control probe whenever a 91S16 is installed in the DAS.

To connect a probe to any DAS module:

1. Once you have identified the correct pod connector, grasp the probe's cable holder.

2. Align the cable connector with a square-pin pod connector. Be sure the raised tab on the cable holder is facing towards bus slot 0, and is aligned with the opening on the pod connector.

3. Gently push the cable connector onto the pod connector. Do not force the connection.

Figure 3-6 demonstrates probe connection procedures.

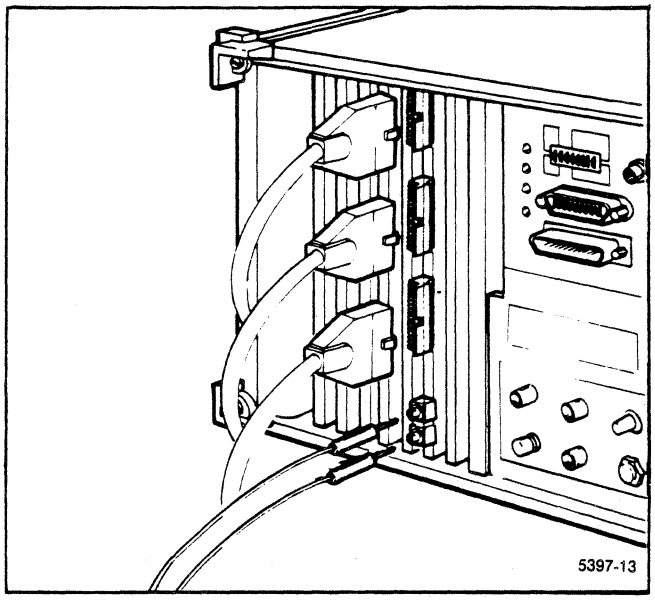


Figure 3-6. Installing a probe to a pod connector.

To remove a probe from a pod connector, firmly grasp the cable connector and gently pull straight out; do not pull on the cable itself.

OPERATOR'S CHECKOUT PROCEDURE

When the DAS mainframe is powered up, all installed 91S16 and 91S32 modules will appear on the power-up configuration display. PASS or FAIL notations appear next to each module to show the results of that module's power-up testing. Table 3-1 lists and defines the power-up error conditions for 91S16 and 91S32 modules.

Table 3-1
POWER-UP ERROR CONDITIONS

Error Condition	Definition
91S16 Pattern Generator Module FAIL	The 91S16 module has failed the power-up test. The module will not operate properly. Refer the 91S16 module with probes to qualified service personnel. This failure does not affect the operation of any installed data acquisition module. If the 91S16 is being used to control 91S32s, the 91S32s may also be disabled by a failure in the 91S16.
91S32 Pattern Generator Module FAIL	The 91S32 module has failed the power-up test. The module will not operate properly. Refer the 91S32 module and its probes to qualified service personnel. Make sure the interconnect cable is attached before the DAS is turned on, otherwise the 91S32s will fail diagnostics. If multiple 91S32's fail on power-up, it is probably because: 1. The interconnect cable is not properly attached. 2. There may be a broken line in the interconnect cable. 3. The terminating jumpers on the 91S32s have not been properly set. If there is only one 91S32 failure when multiple 91S32s are installed, refer that 91S32 for service. Adjust the remaining modules so that there are no empty slots between modules.

91S16 CONFIGURATION SUB-MENU FIELDS AND VALUES

NOTE

The 91S16 Configuration sub-menu appears only when a 91S16 module is installed in the DAS.

The following paragraphs explain how to use the 91S16 Configuration sub-menu to set up the 91S16 Pattern Generator module. They discuss each menu field and explain the optional values.

Figure 3-7 illustrates the 91S16 Configuration sub-menu and its fields. The field names, which appear in reverse video on the screen, are bracketed [ ] throughout the text. Use the four directional cursor keys and the NEXT key to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-7 when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.

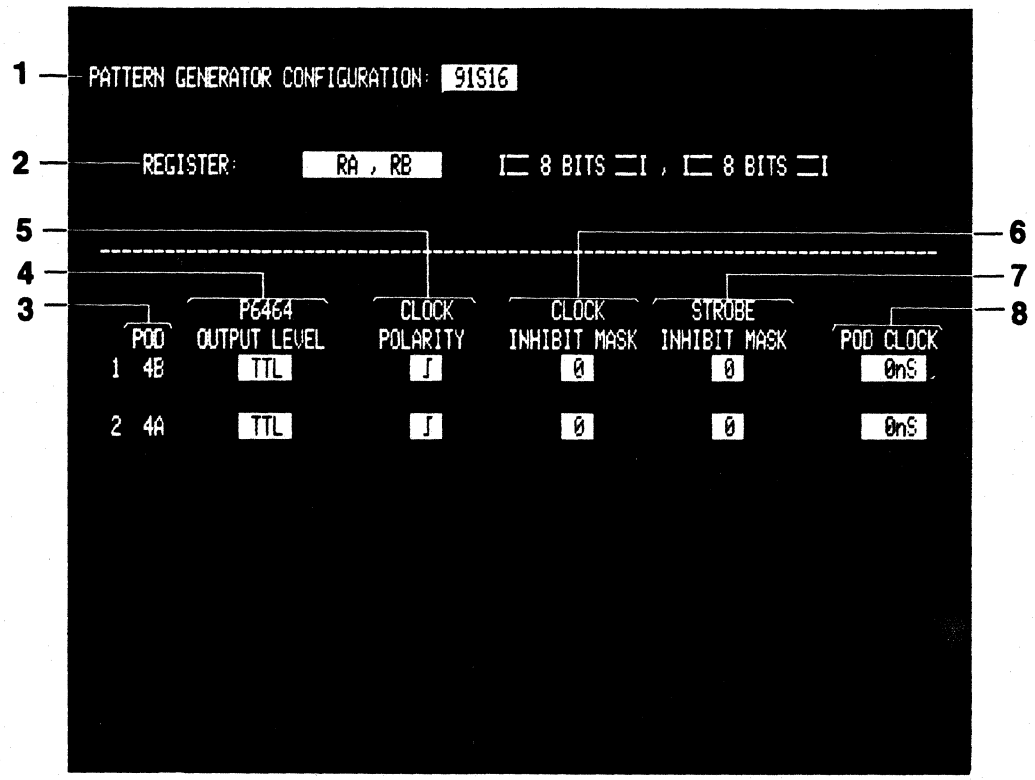


Figure 3-7. 91S16 Configuration sub-menu.

Pattern Download From Host Feature. For information about downloading programs and vectors from a host computer to the 91S16 module, see the section of this addendum titled *GPIB Programming*. If you are using 91S16 and 91S32 modules together, also see the paragraphs titled *Pattern Download From Host* in the *91S32 Configuration Sub-Menu When Used With 91S16* section of this addendum.

1 PATTERN GENERATOR CONFIGURATION Field

The field directly to the right of the menu title is used to select either the 91S16 Configuration sub-menu or the 91S32 Configuration sub-menu.

NOTE

When a 91S16 is installed with one or more 91S32s, the 91S32 Configuration menu has some fields that are not displayed when only 91S32s are installed in the DAS. If you are using both 91S16 and 91S32 Pattern Generator modules, you will need to enter parameters in both the 91S16 Configuration sub-menu and the 91S32 Configuration sub-menu.

When a 91S16 is installed in the DAS, the 91S16 Configuration sub-menu will be displayed as the default menu. Press the SELECT key when the screen cursor is in this field in order to view the 91S32 Configuration sub-menu. (The 91S32 Configuration sub-menu is only available if there is at least one 91S32 installed in the DAS.)

2 REGISTER Field

The REGISTER field is used to select the configuration of the 91S16's internal register. This register can be used as an incrementing or decrementing counter for program loops or to supply an alternate source of pattern for some program line.

The 91S16 internal register at power-up is configured to be two 8-bit registers named RA and RB, however you can use the REGISTER field to select a single 16-bit register named R. When RA and RB are concatenated into register R, RB bits become the high-order bits of R, and RA bits become the low-order bits of R.

NOTE

If you have selected the register to be two 8-bit registers, only instructions relating to RB and RA will be displayed. If you have selected the internal register to be "R," a single 16-bit register, only instructions relating to R will be displayed in any of the 91S16 menus; no instructions relating to RB or RA will be displayed. If you have programmed any instructions that use the register in one configuration, you cannot select the other register configuration until you have deleted those instructions from the program.

To select the 91S16 internal register's configuration:

1. Move the screen cursor to the REGISTER field.
2. Press the SELECT key until the desired value appears in the field.

3 POD Heading

The POD heading is used to display the name of the pods associated with the 91S16's data probes. The DAS employs a numbering scheme using bus slot numbers to identify specific circuit boards and letters to identify specific probes attached to each circuit board.

Each P6464 Pattern Generator probe and P6460 External Control Probe is connected to a specific socket on the back of the 91S16 card referred to as a pod connector. The name of each pod connector is called the pod I.D. (pod identification).

A pod I.D. consists of a number and a letter. The number corresponds to the DAS slot number where the 91S16 card resides. The letter refers to the pod on that particular 91S16. For instance, a pod labeled 6B would correspond to the second pod on the 91S16 installed in DAS slot 6.

In the case of the 91S16, Pod A and Pod B are reserved for P6464 Pattern Generator Probes; Pod C is reserved for the optional P6460 External Control Probe.

4 P6464 OUTPUT LEVEL Field

The P6464 OUTPUT LEVEL field is used to select the output level for the P6464 Pattern Generator Probe. This probe outputs the data, strobe, and clock to a circuit/device under test. The P6464 Probe has two output levels, TTL and ECL. You can select the output levels for each pod independently.

To select the output level for the P6464 probe:

1. Move the screen cursor to the P6464 OUTPUT LEVEL field.

   P6464
   OUTPUT LEVEL
   [TTL]

2. Press the SELECT key until the desired output level appears in the field.

   [ECL]

5 CLOCK POLARITY Field

The CLOCK POLARITY field is used to specify whether the clock supplied to the device under test is a rising edge signal or a falling edge signal at the start of each cycle. Each pod has its own clock line, and you can set the clock edge for each pod independently. At power-up, all the clocks are set to rising edge signals.

To specify the clock's edge:

1. Move the screen cursor to the CLOCK POLARITY field.

   CLOCK
   POLARITY
   [⌐¬]

2. Press the SELECT key until the desired value appears in the field.

   The DAS displays optional values in this order:
   [⌐¬]
   [¬⌐]

6 CLOCK INHIBIT MASK Field

The CLOCK INHIBIT MASK field is used to specify whether or not the clock output responds to the inhibit signal. If the CLOCK INHIBIT MASK field is set to 0 (unmasked), the clock signal for that data pod will be tri-stated whenever the inhibit signal is asserted. If the CLOCK INHIBIT MASK field is set to 1 (masked), the clock signal for that particular pod will continue to be output even if the inhibit signal is asserted. The default value for this field is 0 (unmasked).

To set the CLOCK INHIBIT MASK Field:

1. Move the screen cursor to the CLOCK INHIBIT MASK field:

```
    CLOCK
INHIBIT MASK
     [0]
```

2. Use the data entry keys to enter a 1 (masked).

```
    CLOCK
INHIBIT MASK
     [1]
```

7 STROBE INHIBIT MASK Field

The STROBE INHIBIT MASK field is used to specify whether or not the strobe output responds to the inhibit signal. If the STROBE INHIBIT MASK field is set to 0 (unmasked), that particular pod's strobe line will be tri-stated whenever the inhibit signal is asserted. If the STROBE INHIBIT MASK field is set to 1 (masked), that pod's strobe line will not be tri-stated, even if the inhibit signal is asserted. The default value for this field is 0 (unmasked).

To specify the strobe inhibit mask:

1. Move the screen cursor to the STROBE INHIBIT MASK field.

```
    STROBE
INHIBIT MASK
     [0]
```

2. Use the data entry keys to enter a 1 .

```
     [1]
```

8 POD CLOCK Field

The POD CLOCK field is used to select the pod clock delay relative to the start of the pattern generator cycle. This feature allows you to adjust the timing of one pod relative to another. You could set one pod to output its data and clock signal 5 ns before the main clock edge, and set another pod to output data 5 ns after the main clock edge. The timing difference between the two pods would then be 10 ns.

Use the INCR or DECR keys to select a pod clock delay value. You can set each pod individually to output its data, strobe, and clock signals up to 5 ns before or 5 ns after the pattern generator clock edge. This field adjusts timing in 5 ns increments. The default value for this field is 0 ns.

Note: If you are running the 91S16 with 91S32s at 50 MHz. there are some restrictions on the pod clock delay value. Refer to the Timing sub-menu description for details.

To increase or decrease the POD CLOCK delay:

1. Move the screen cursor to the POD CLOCK field.

```
POD CLOCK
     [ 0nS]
```

2. Use the INCR key to increase the delay value, or the DECR key to decrease it. The DAS displays the delay values in this order:

```
     [−5nS]
     [  0nS]
     [+5nS]
```

91S32 STAND ALONE CONFIGURATION SUB-MENU FIELDS AND VALUES

NOTE

The 91S32 Configuration menu is available only when 91S32 Modules are installed in the DAS. A slightly different version of the 91S32 Configuration sub-menu is displayed if both 91S16 and 91S32 Pattern Generator modules are installed in the DAS at the same time. See the section of this addendum titled 91S32 Configuration Sub-Menu When Used With 91S16 *if you are using both types of pattern generator modules together.*

The following paragraphs explain how you can use the 91S32 Configuration sub-menu to set up the pattern generator. Each sub-menu field is described and its optional values explained.

Figure 3-8 illustrates the 91S32 Configuration sub-menu and its fields. The fields, which appear in reverse video on the screen, are bracketed [ ] throughout the text. The four directional cursor keys and the NEXT key can be used to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-8 when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.

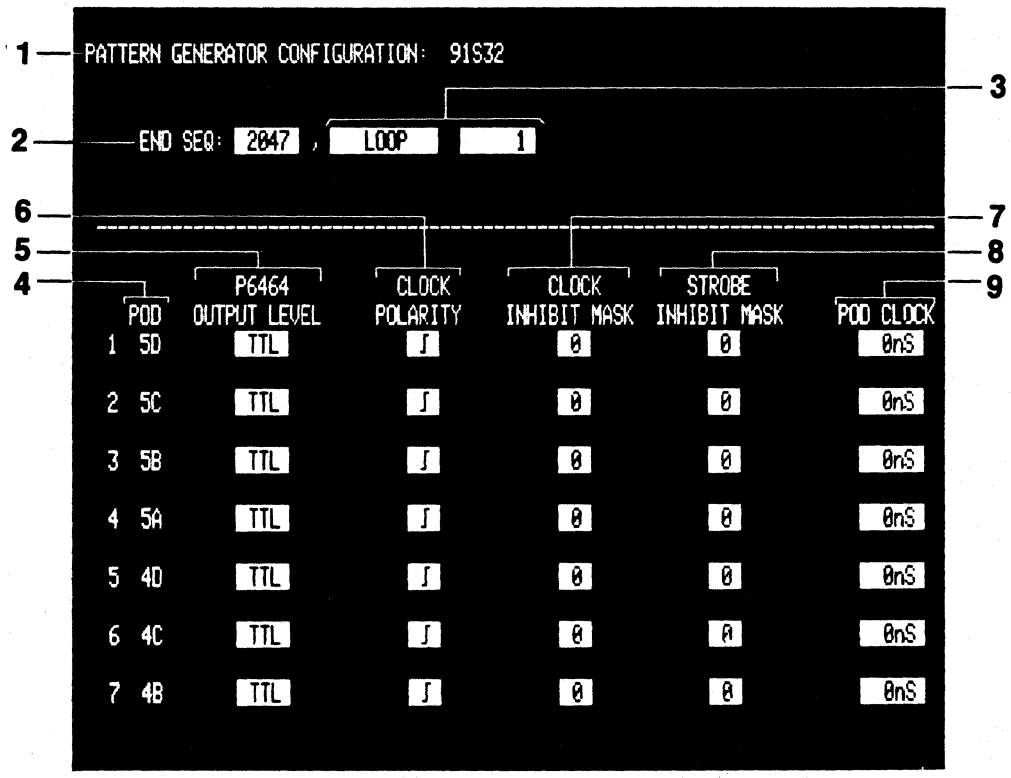


Figure 3-8. 91S32 Stand Alone Configuration sub-menu.

Pattern Download From Host Feature. 91S32 modules can use the static device version of the Pattern Download From Host feature (91S16 optional). This feature allows you to download extensive programs into the pattern generator from a GPIB controller. Refer to the *GPIB Programming* section of this manual for details. You should also read the paragraphs titled *Pattern Download From Host* in the *91S32 Configuration Sub-Menu When Used With 91S16* section of this addendum.

1 PATTERN GENERATOR CONFIGURATION Field

This field (directly to the right of the menu title) indicates the title of the 91S32 Configuration sub-menu. The 91S32 Configuration sub-menu is the only option available when 91S32s are the only pattern generator modules installed in the DAS.

NOTE

If you are using a 91S16 with 91S32s, this field will default to the 91S16 Configuration sub-menu. See the section of this addendum titled 91S32 Configuration Sub-Menu When Used With 91S16.

2 END SEQ Field

The 91S32 pattern generator normally executes all the sequence lines in memory and then automatically restarts from the beginning. However, not all patterns require the full 2047 lines of available memory. This field allows you to specify some smaller number to reset pattern execution to the first sequence. This number can be any value between 0 and 2047 (ASEQ) or A 0 and B 1023 (RSEQ).

The 91S32 modules will repeatedly execute the program entered between the number in the START SEQ: field of the 91S32 Program: Run sub-menu (usually SEQ 0) and the sequence number specified in the END SEQ field.

The default value for the END SEQ field is END SEQ 2047. Note that this field will display END SEQ 2047 if you have set the SEQ field to ASEQ (absolute sequence) in the 91S32 Run sub-menu. If you have set the SEQ field to RSEQ (relative sequence), the allowable range will be Page A, 0 through 1023, and Page B, 0 through 1023. See the 91S32 Program: Run sub-menu section SEQ field description for details about the ASEQ and RSEQ options.

To specify the END SEQ:

1. Move the screen cursor to the END SEQ field.

   END SEQ [2047]

2. Use the data entry keys to enter the END SEQ number. For example, to enter sequence number 500:

   END SEQ [500]

3 LOOP Field

This field is used to specify the 91S32 operating mode. There are two possible selections for this field: LOOP and FREE RUN. The 91S32 normally executes all the sequence lines entered into memory starting with sequence 0 and running through to the sequence number specified in the END SEQ field, or until the end of memory if no END SEQ value has been specified. The pattern generator will execute this program repeatedly until you press the STOP key. This is called FREE RUN mode.

If you only want the pattern generator to loop through its program a certain number of times and then stop, select LOOP. Loop mode displays a special LOOP field where you can enter the number of times you want the pattern generator to execute its program. Maximum value for this field is 65535.

To select FREE RUN or LOOP mode:

1. Move the screen cursor to the field immediately to the right of the END SEQ field:

   END SEQ [2047] [LOOP] [1]

   2. Press the SELECT key until the desired value appears in the field.

   END SEQ [2047] [LOOP] [1]
   [FREE RUN]

To enter a value for the [LOOP] field:

1. Move the screen cursor to the field immediately to the right of the LOOP field.
2. Use the data entry keys to enter the number of times you want the pattern generator to execute its program. For example, to run through the loop 1000 times, and then stop, enter 1000:

   END SEQ [2047] [LOOP] [1000]

4 POD Heading

The POD heading is used to display the number of 91S32 boards installed in the DAS and the name of each data pod available. A POD refers to the specific connector on the back of the 91S32 where a P6464 probe is connected.

The name of each pod is referred to as pod I.D. (pod identification). A pod I.D. consists of a number and a letter. The number corresponds to the DAS slot number where that particular 91S32 card resides. The letter refers to the pod on that particular 91S32. For instance, a pod labeled 6C would correspond to the third pod on the 91S32 installed in DAS slot 6.

5 P6464 OUTPUT LEVEL Field

The P6464 OUTPUT LEVEL field is used to select the output level for the P6464 Pattern Generator Probe. This probe outputs the data, strobe, and clock to a circuit/device under test. The P6464 Probe has two output levels, TTL and ECL. You can select the output levels for each pod independently.

To select the output level for the P6464 Probe:

1. Move the screen cursor to the P6464 OUTPUT LEVEL field.

```
   P6464
OUTPUT LEVEL
   [TTL]
```

2. Press the SELECT key until the desired output level appears in the field.

```
   [ECL]
```

6 CLOCK POLARITY Field

The CLOCK POLARITY field is used to specify whether the clock supplied to the device under test is a rising edge signal or a falling edge signal at the start of each cycle. Each pod has its own clock line, and you can set the clock edge for each pod individually. In default, all the clocks are set to rising edge signals.

To specify the clock's edge:

1. Move the screen cursor to the CLOCK POLARITY field.

```
  CLOCK
POLARITY
  [⌐ ]
```

2. Press the SELECT key until the desired value appears in the field.

   The DAS displays optional values in this order:

```
[⌐ ]
[¬ ]
```

7 CLOCK INHIBIT MASK Field

The CLOCK INHIBIT MASK field is used to specify whether or not the clock output responds to the inhibit signal. If the CLOCK INHIBIT MASK field is set to 0 (unmasked), the clock signal for that data pod will be tri-stated whenever the inhibit signal is asserted. If the CLOCK INHIBIT MASK field is set to 1 (masked), the clock signal for that particular pod continues to be output even if the inhibit signal is asserted. The default value for this field is 0 (unmasked).

To set the CLOCK INHIBIT MASK Field:

1. Move the screen cursor to the CLOCK INHIBIT MASK field.

```
   CLOCK
INHIBIT MASK
     [0]
```

2. Use the data entry keys to enter a 1 (masked).

```
   [1]
```

8 STROBE INHIBIT MASK Field

The STROBE INHIBIT MASK field is used to specify whether or not the strobe output responds to the inhibit signal. If the STROBE INHIBIT MASK field is set to 0 (unmasked), that particular pod's strobe line will be tri-stated whenever the inhibit signal is asserted. If the STROBE INHIBIT MASK field is set to 1 (masked), that pod's strobe line will never be tri-stated, even if the inhibit signal is asserted. The default value for this field is 0 (unmasked).

To specify the strobe inhibit mask:

1. Move the screen cursor to the STROBE INHIBIT MASK field.

   STROBE
   INHIBIT MASK
   [0]

2. Use the data entry keys to enter a 1 (masked).

   [1]

9 POD CLOCK Field

The POD CLOCK field selects the pod clock delay value relative to the start of the pattern generator cycle. This feature allows you to adjust the timing of one pod relative to another. You could set one pod to output its data and clock signal 5 ns before the main clock edge, and set another pod to output data 5 ns after the main clock edge. The timing difference between the two pods would then be 10 ns.

Use the INCR or DECR keys to select a pod clock delay value. You can set each pod individually to output its data, strobe, and clock signals up to 5 ns before or 5 ns after the pattern generator clock edge. This field adjusts timing only in 5 ns increments. The default value for this field is 0 ns.

Note: If you have selected a clock rate of 50 MHz., all pod clock values must be set to 0 ns.

To increase or decrease the POD CLOCK delay:

1. Move the screen cursor to the POD CLOCK field.

   POD CLOCK
   [0 nS]

2. Use the INCR key to increase the delay value, or the DECR key to decrease it. The DAS will display the delay values in the following order:

   [−5 nS]
   [0 nS]
   [+5 nS]

91S32 CONFIGURATION SUB-MENU WHEN USED WITH 91S16

NOTE

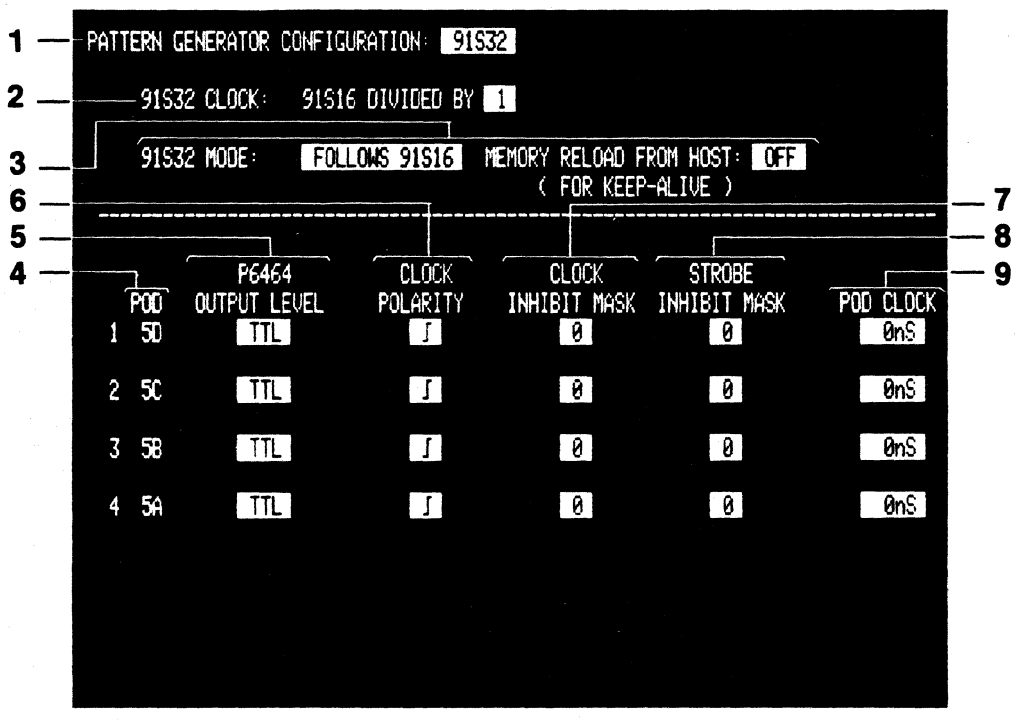
This version of the 91S32 Configuration sub-menu only appears when both 91S16 and 91S32 modules are installed in the DAS at the same time.

The following paragraphs explain how to use the 91S32 Configuration sub-menu when both 91S16 and 91S32 pattern generator modules are installed in the DAS. Refer to the preceding sub-section titled *91S32 Stand-Alone Configuration Sub-Menu* if you do not have a 91S16 installed.

Figure 3-9 illustrates the 91S32 Configuration sub-menu as it appears when both 91S16 and 91S32 modules are installed. There are several small differences between this sub-menu and the 91S32 Configuration sub-menu that appears when only 91S32s are installed; most of these differences are concerned with Follows 91S16 mode and the keep-alive feature.

Fields that appear in reverse video on the DAS screen are bracketed [ ] throughout the text. Use the four directional cursor keys and the NEXT key to move the blinking cursor from one field to another.

Refer to the numbered callouts in Figure 3-9 when reading the following paragraphs. These numbers are visual references only and do not imply sequence of use.



5397-16

Figure 3-9. 91S32 Configuration sub-menu when used with 91S16.

1 PATTERN GENERATOR CONFIGURATION Field

This field (directly to the right of the menu title) is used to select either the 91S16 or the 91S32 Configuration sub-menu display. If only 91S32s are installed, a slightly different version of the 91S32 Configuration sub-menu will be displayed; this version of the sub-menu is described in a separate section titled *91S32 Stand-Alone Configuration Sub-Menu.*

If both 91S16 and 91S32 modules are installed, the 91S16 Configuration sub-menu will be displayed first; the 91S32 Configuration sub-menu will only be displayed if you press the SELECT key when the screen cursor is in this field. Pressing SELECT repeatedly causes the DAS to alternately display the 91S16 and 91S32 Configuration sub-menus.

To alternately display the 91S16 or 91S32 Configuration sub-menus:

1. Move the screen cursor to the field directly to the right of the menu title.

   PATTERN GENERATOR CONFIGURATION: [91S16]

2. Press the SELECT key until the 91S32 Configuration sub-menu appears in the field.

   PATTERN GENERATOR CONFIGURATION: [91S32]

3. Press SELECT again if you want to return to the 91S16 Configuration sub-menu.

2 91S32 CLOCK Field

NOTE

The 91S32 CLOCK field will only appear if a 91S16 is installed in the DAS. If no 91S16 is installed, the 91S32's clock rate is set in the Timing sub-menu.

When 91S32 modules are used with a 91S16 module, the 91S32 modules receive their system clock from the 91S16 module. The 91S32 modules usually operate at the same clock rate as the 91S16 module, but they can be operated at one-half or one-fourth the clock rate of the 91S16.

For example, if you enter a 2 in the 91S32 CLOCK field, you can then program the 91S16 clock to run at 50 MHz (programmed in the Timing sub-menu) and the 91S32 modules will run at 25 MHz.

Even at slower clock rates, you may find it convenient to run the 91S16 faster than the 91S32s. The default divisor is 1.

Note: There are some pod clock delay restrictions when operating 91S16 and 91S32 modules at 50 MHz. Refer to the Timing **sub-menu.**

To change the clock divisor for the 91S32 modules:

1. Move the screen cursor to the 91S32 CLOCK field.

   91S32 CLOCK: 91S16 CLOCK DIVIDED BY [1]

2. Press the INCR key to increase the divisor value or the DECR key to decrease the value. The DAS will display increasing divisor values in a 1-2-4 sequence. For example, to change the divisor to 2, press the INCR key once.

   91S32 CLOCK: 91S16 CLOCK DIVIDED BY [2]

NOTE

The 91S16 and 91S32 combination can not run faster than 25 MHz (40 ns). If you program the 91S16 to run at 50 MHz and set the 91S32 CLOCK field to 91S16 DIVIDED BY 1, the 91S32 modules may not work properly.

3 91S32 MODE Field

The 91S32 module has two operating modes when used with a 91S16 module: Follows 91S16 mode and Sequential mode. Follows 91S16 mode is the default mode.

FOLLOWS 91S16 Mode and the MEMORY RELOAD FROM HOST Field

In Follows 91S16 mode, the 91S32s receive both its clock and vector-memory addresses from the 91S16 module via the interconnect cable. In this mode, when the 91S16 program executes a jump from SEQ 100 to SEQ 50, the 91S32s will also jump from SEQ 100 to SEQ 50. The 91S32s follow the sequence flow instructions programmed in the 91S16.

In Follows 91S16 mode the 91S32's memory is divided into two 1024-vector pages called Page A and Page B. Each memory page matches the 1024-vector depth of the 91S16's memory. When the pattern generator is started, the 91S16 outputs its 1024-vector pattern while the 91S32s output the pattern in Page A. When the 91S16 reaches an INCR PAGE (Increment Page) command, it instructs the 91S32s to switch to Page B. (Note: Pattern Download From Host does not use the INCR PAGE command to switch between Page A and Page B.)

Pattern Download From Host

Follows 91S16 mode also provides a Pattern Download From Host feature that allows you to reload the 91S32's vector memory from a host computer or mass storage device while the pattern generator is running. The Pattern Reload From Host feature allows you to use a pattern longer than 2047 lines. It also enables you to develop a pattern generator program on a host computer and enter it into the DAS remotely.

NOTE

In order to use the Pattern Download From Host feature, the DAS must be connected to a host computer using General Purpose Interface Bus (GPIB) connections and protocols. Instructions for making these connections and formating the data to be downloaded to the pattern generator cards can be found in the section of this addendum titled GPIB Programming, *the* DAS Option 06: I/O Communication Interface Operator's Manual Addendum, *and in* Section 12: GPIB Programming *in the* DAS 9100 Series Operator's Manual.

There are two versions of Pattern Download From Host. Pattern Download For Static Devices can be used with either a 91S16, 91S32s, or a combination of the two. Pattern Download For Dynamic Devices (Keep-Alive) requires a 91S16 and at least one 91S32 module.

Pattern Download For Static Devices. This version of the Pattern Download feature can be implemented using DAS Option 02 or DAS Option 06 (GPIB commands via the GPIB or RS-232 interfaces). Using Pattern Download For Static Devices, the pattern generator outputs all its vectors, maintains the last vector at the probe tips while the next block of vectors is downloaded from the host computer, and then resumes outputting vectors. This process can be repeated until the entire program has been executed.

Pattern Download For Dynamic Devices (Keep-Alive). This version of the Pattern Download feature provides some clock and vector output during the interval when the 91S32's memory is being reloaded. Pattern Download For Dynamic Devices is only available when using the Option 06 HSPAT command over the GPIB interface. You must have a 91S16 and at least one 91S32 installed, and the pattern generator clock rate is limited to 25 MHz.

Some types of circuitry require constant clock and data inputs. Pattern Download For Static Devices, described above, does not provide any circuit stimulation while the host computer is downloading the next block of vectors. For static circuit elements this is not a problem; the device under test can just wait for the next block of vectors to finish being reloaded. But for dynamic circuit elements (such as dynamic RAMs), some clock and vector input is necessary to keep the device active while the reload process is being completed. The 91S16/32 Pattern Generator modules provide a feature called Keep-Alive to stimulate the circuit until the other page of memory is ready.

In order to use the Keep-Alive feature, you must set the MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) Field to ON.

NOTE

Selecting ON *in the* MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) *field is only valid if you are using DAS 9100 Option 6: Fast GPIB Programming to perform memory reload. This field enables some instructions in the 91S16 Program: Run sub-menu that are only valid using Option 6 GPIB. See the* GPIB *of this addendum for detailed instructions about using Keep-Alive. Reloading the 91S32 memory from a host is possible via RS-232 or slow GPIB when this field is set to OFF, but the Keep-Alive feature will not be available.*

Keep-Alive is basically a subroutine programmed into the 91S16 that outputs a limited number of vectors to the device under test while frequently testing to see if the memory reload operation has been completed.

Following 91S16 control, the 91S32s execute one 1024-line page of vectors while reloading the other page. However, it takes longer to reload a page of vectors than it does to execute a page of vectors. The Keep-Alive sub-routine programmed into the 91S16 provides some circuit stimulation while the 91S32 reload process is being completed. The 91S16 is programmed with instructions that test if the other page of memory has been reloaded. If the other page has been reloaded, the 91S16 instructs the 91S32s to switch execution to the newly refilled memory page; if the other page has not been reloaded, the 91S16 loops back through its sub-routine and the pattern generator continues to output some vectors.

An example of a Keep-Alive routine is provided in the *GPIB* section of this addendum.

SEQUENTIAL Mode and the END SEQ Field

When 91S32s are in Sequential mode with a 91S16, the two types of modules are clocked together but execute their programs independently. Pattern generation begins with the lowest numbered sequence line specified in the 91S32 Program: Run sub-menu (usually SEQ 0) and progresses sequentially until reaching the sequence number specified in the END SEQ field. Program execution in the 91S32 modules is not affected by branching instructions executed by the 91S16 program. For example, if the 91S16 is programmed to jump from SEQ 100 to SEQ 50, the 91S32s will not jump, but continue to execute their program sequentially at SEQ 101.

While 91S32s in Sequential mode are not affected by 91S16 branch instructions, they are affected by 91S16 halt and pause conditions since the 91S16 provides the clock to the 91S32 modules.

The END SEQ field allows you to specify a sequence line number smaller than Page B SEQ 1023 as the last line in your pattern generator program. The END SEQ field only appears when Sequential mode has been selected.

The advantage of Sequential mode is that you can program the 91S16 to perform conditional branching and loops while allowing the 91S32s to supply the usual sequential patterns. One example of this kind of application occurs when you are using the 91S16 to provide addresses to some memory device while the 91S32s supply the test vectors.

The default value for the END SEQ field is 2047. The numbering scheme for END SEQ field is dependent on whether you have selected ASEQ (absolute sequence) numbers or RSEQ (relative sequence) numbers in the 91S32 Program: Run sub-menu. If you have selected ASEQ in that sub-menu, the maximum allowable END SEQ field value is 2047. If you have selected RSEQ, the maximum allowable END SEQ field value is Page B 1023. The END SEQ field format will indicate which numbering scheme is being used.

To select either FOLLOWS 91S16 or SEQUENTIAL mode:

1. Move the screen cursor to the 91S32 MODE field.

   91S32 MODE: [FOLLOWS 91S16] MEMORY RELOAD FROM HOST: [OFF]
   (FOR KEEP-ALIVE)

2. Press the SELECT key until the desired mode appears in the field. The DAS will display the modes in this order:

   [FOLLOWS 91S16]
   [SEQUENTIAL]

NOTE

You cannot switch from FOLLOWS 91S16 mode to SEQUENTIAL mode if CALL RMT, IF FULL, or IF END instructions are programmed in the 91S16 Program: Run sub-menu, or if the MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) Field is set to ON.

To enable or disable the KEEP-ALIVE feature in FOLLOWS 91S16 mode:

1. Move the screen cursor to the 91S32 MODE field and select FOLLOWS 91S16 mode. Then move the cursor to the MEMORY RELOAD FROM HOST sub-field.

   91S32 MODE: [FOLLOWS 91S16] MEMORY RELOAD FROM HOST: [OFF]
   (FOR KEEP-ALIVE)

2. Press the SELECT key until the desired value appears in the field.

   91S32 MODE: [FOLLOWS 91S16] MEMORY RELOAD FROM HOST: [ON]
   (FOR KEEP-ALIVE)

To enter a value in the SEQUENTIAL mode END SEQ: sub-field:

1. Move the screen cursor to the 91S32 MODE field and select SEQUENTIAL mode. Then move the cursor to the END SEQ sub-field.

   91S32 MODE: [SEQUENTIAL] END SEQ [2047]

2. Use the data entry keys to enter the END SEQ number. For example, enter 500:

   91S32 MODE: [SEQUENTIAL] END SEQ [500]

4 POD Heading

The POD heading is used to display the number of 91S32 boards installed in the DAS and the names of each data pod available. A POD refers to the specific connector on the back of the 91S32 where a P6464 probe is connected.

The name of each pod is referred to as pod I.D. (pod identification). A pod I.D. consists of a number and a letter. The number corresponds to the DAS slot number where that particular 91S32 card resides. The letter refers to the pod on that particular 91S32. For instance, a pod labeled 6C would correspond to the third pod on the 91S32 installed in DAS slot 6.

5 P6464 OUTPUT LEVEL Field

The P6464 OUTPUT LEVEL Field is used to select the output level for the P6464 Pattern Generator Probe. This probe outputs the data, strobe, and clock to a circuit/device under test. The P6464 Probe has two output levels, TTL and ECL. You can select the output levels for each pod individually.

To select the output level for the P6464 Probe:

1. Move the screen cursor to the P6464 OUTPUT LEVEL field.

   P6464
   OUTPUT LEVEL
   [TTL]

2. Press the SELECT key until the desired output level appears in the field.

   [ECL]

6 CLOCK POLARITY Field

The CLOCK POLARITY field is used to specify whether the clock supplied to the device under test is a rising edge signal or a falling edge signal at the start of each cycle. Each pod has its own clock line, and you can set the clock edge for each pod individually. In default, all the clocks are set to rising edge signals.

To specify the clock's edge:

1. Move the screen cursor to the CLOCK POLARITY field.

   CLOCK
   POLARITY
   [⌐]

2. Press the SELECT key until the desired value appears in the field.

   The DAS displays optional values in this order:
   [⌐]
   [¬]

7 CLOCK INHIBIT MASK Field

The CLOCK INHIBIT MASK field is used to specify whether or not the clock output responds to the inhibit signal. If the CLOCK INHIBIT MASK field is set to 0 (unmasked), the clock signal for that data pod will be tri-stated whenever the inhibit signal is asserted. If the CLOCK INHIBIT MASK field is set to 1 (masked), the clock signal for that particular pod will continue to be output even if the inhibit signal is asserted. The default value for this field is 0 (unmasked).

To set the CLOCK INHIBIT MASK Field:

1. Move the screen cursor to the CLOCK INHIBIT MASK field:

   CLOCK
   INHIBIT MASK
   [0]

2. Use the data entry keys to enter a 1 (masked).

   CLOCK
   INHIBIT MASK
   [1]

8 STROBE INHIBIT MASK Field

The STROBE INHIBIT MASK field is used to specify whether or not the strobe output responds to the inhibit signal. If the STROBE INHIBIT MASK field is set to 0 (unmasked), that particular pod's strobe line will be tri-stated whenever the inhibit signal is asserted. If the STROBE INHIBIT MASK field is set to 1 (masked), that pod's strobe line will never be tri-stated, even if the inhibit signal is asserted. The default value for this field is 0 (unmasked).

To specify the strobe inhibit mask:

1. Move the screen cursor to the STROBE INHIBIT MASK field.

   STROBE
   INHIBIT MASK
   [0]

2. Use the data entry keys to enter a 1 (masked).

   STROBE
   INHIBIT MASK
   [1]

9 POD CLOCK Field

The POD CLOCK field is used to select the pod clock delay relative to the start of the pattern generator cycle. This feature allows you to adjust the timing of one pod relative to another. You could set one pod to output its data and clock signal 5 ns before the master clock edge, and set another pod to output data 5 ns after the master clock edge. The timing difference between the two pods would then be 10 ns.

Use the INCR or DECR keys to select a pod clock delay value. You can set each pod individually to output its data, strobe, and pod clock signals up to 5 ns before or 5 ns after the pattern generator master clock's selected edge. This field adjusts timing only in 5 ns increments. The default value for this field is 0 ns.

Note: When operating 91S16 and 91S32 modules together at 50 MHz. you must set all pod clock delay values to −5 ns.

To increase or decrease the POD CLOCK delay:

1. Move the screen cursor to the POD CLOCK field.

   POD CLOCK
   [0nS]

2. Use the INCR key to increase the delay value, or the DECR key to decrease it. The DAS displays the delay values in this order:

   [−5nS]
   [0nS]
   [+5nS]

91S16 PROBE SUB-MENU FIELDS AND VALUES

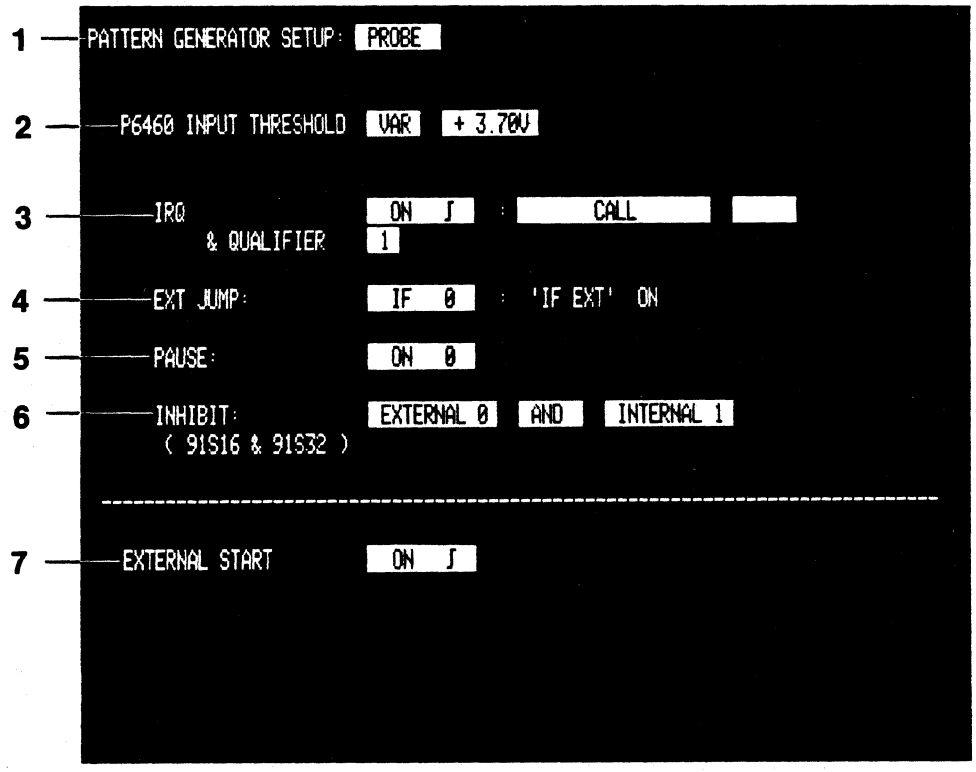
NOTE

The 91S16 Setup: Probe sub-menu appears only when the 91S16 Module is installed in the DAS.

The following paragraphs show how to use the 91S16 Setup: Probe sub-menu to set up the 91S16's P6460 External Control Probe. They discuss each menu field and explain all the optional values.

Figure 3-10 illustrates the 91S16 Setup: PROBE sub-menu and its fields. The fields, which appear in reverse video on the screen, are bracked [ ] throughout the text. The four directional cursor keys and the NEXT key can be used to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-10 when reading the following paragraphs. These numbers are intended to be a visual reference and do not imply sequence of use.



5397-17

Figure 3-10. 91S16 Setup: Probe sub-menu.

1 PATTERN GENERATOR SETUP Field

The field directly to the right of the menu title is used to select either the 91S16 Setup: PROBE or the 91S16 Setup: TIMING sub-menu display. In default, the 91S16 PROBE sub-menu is displayed whenever a 91S16 is installed in the DAS.

2 P6460 INPUT THRESHOLD Field

The P6460 INPUT THRESHOLD field is used to set the threshold level for the P6460 External Control Probe. This probe supplies the 91S16 pattern generator's external clock, interrupt request, interrupt request qualifier, external jump, pause, and external inhibit lines. In default, the INPUT THRESHOLD field is set to TTL + 1.40 V.

To change the INPUT THRESHOLD field from TTL to ECL or VAR (variable):

1. Move the screen cursor to the INPUT THRESHOLD field.
2. Press the SELECT key until the desired threshold level appears in the field. The DAS will display the optional values in this order:

   [TTL] + 1.40 V
   [VAR] [+ 3.70 V]
   [ECL] - 1.30 V

When VAR has been selected, a new field appears to allow you to set the variable voltage level. The range for this field is between − 6.40 V and + 6.35 V in 50 mV increments. Use the INCR and DECR keys to set the value for this field.

3 IRQ Field AND QUALIFIER Field

The interrupt signal is supplied to the 91S16 module via the optional P6460 External Control Probe. This signal line must be connected to an external source. In order to use the interrupt signal to control the 91S16, you must abide by the following three rules:

1. For the internal interrupt to be true for a given clock cycle, the external interrupt signal must have a 15 ns set-up time relative to the selected edge of the external input clock. In other words, if you are running the 91S16 at 50 Mhz (20 ns clock cycles) the external interrupt signal must occur during the first 5 ns of the current clock cycle or else the interrupt will not be recognized until the next clock cycle.
2. The interrupt qualifier signal must stay true for 15 ns prior to the interrupt signal becoming active.
3. The interrupt mask must be set to 0 (unmasked).

The IRQ (Interrupt Request) field is divided into two parts. The first part specifies whether the interrupt is disabled or enabled. If it is enabled, another field appears which allows you to specify whether the interrupt will occur on the rising or falling edge of the external interrupt signal. The second part of the IRQ field specifies the mode the 91S16 uses to handle interrupts.

IRQ enabled, CALL <label> Mode and IF IRQ Mode

The 91S16 provides two modes for handling external interrupts. The options are CALL and IF IRQ. The first method uses a special interrupt servicing routine that suspends program execution when an interrupt is detected, executes a small subroutine, and then resumes program execution on the sequence line following the one where the interrupt was received. To use this method you will select CALL mode in the IRQ field.

The second method of handling interrupts allows you to program IF IRQ JUMP commands into specific program lines and transfer program flow without saving a return address. To use this method you will select IF IRQ mode in the IRQ field.

If you select CALL mode, you must enter the label for an interrupt service routine in the field next to CALL. You will then enter the same label name in a routine in the 91S16 Program: Run sub-menu. The last line of your servicing routine must contain the RETURN instruction to return program flow to the line following the one where the interrupt was detected.

The first sequence line of this routine must not contain a sequence flow instruction like JUMP or RETURN. If the first line does contain a sequence flow instruction, that instruction will be ignored.

If a second interrupt is detected while the pattern generator is performing an interrupt service routine, the second interrupt will be serviced after the first routine has been completed.

If you select IF IRQ mode, the IRQ line can be tested at convenient points in the pattern generator program by programming IF IRQ JUMP instructions in the 91S16 Program: Run sub-menu. In this mode, when an interrupt is detected, the pattern generator will automatically jump to another place in the program and continue executing sequence lines from that point. Different JUMP destinations can be programmed for each IF IRQ JUMP instruction programmed.

One advantage of the IF IRQ mode is that interrupts will only be serviced at convenient times. (Interrupt masking is possible with CALL mode too, by using the M column in the 91S16 Program: Run sub-menu. The disadvantage is that this method takes longer to program.)

NOTE

If you select CALL in the IRQ mode field, IF IRQ JUMP commands will not be available in the 91S16 Program: Run sub-menu. When in IF IRQ mode, the RETURN instruction will not be available in the Run sub-menu. If you have already programmed IF IRQ JUMP commands in the Run sub-menu, you can not change from IF IRQ to CALL mode in this menu. Similarly, if you have programmed the RETURN instruction in the Run sub-menu, you will not be able to change from CALL to IF IRQ mode in this menu. To change from one mode to the other, you will have to remove the mode-specific instructions from the 91S16 Program: Run sub-menu and then return to the Probe sub-menu to select the other mode.

NOTE

The 91S16 Pattern Generator Module automatically resets the interrupt line before beginning pattern execution. Therefore, if the IF IRQ instruction is programmed on the first line executed (usually SEQ 0) the interrupt signal may not meet the required set-up and hold times necessary for the interrupt to be recognized for this clock cycle; the pattern generator may not jump from this sequence line.

NOTE

GPIB commands use hardware memory address, not labels, to control the pattern generator program flow. IRQ ENABLED CALL <label> *mode reserves the first hardware memory location for the interrupt routine address, thereby shifting all program lines down one memory location.* IRQ DISABLED *and* IRQ ENABLED IF IRQ *mode do not reserve the first memory location. You must remember which IRQ mode is selected when programming jump addresses via GPIB. See the section of this addendum titled* GPIB Programming *for detailed information.*

To enable an interrupt and select either the rising or falling edge:

1. Move the screen cursor to the IRQ field

   IRQ [DISABLED]

2. Press the select key. The IRQ field will display a rising edge symbol.

   [ON ⎍]

3. Press the SELECT key again to rotate through the list of optional values.

   [DISABLED]
   [ON ⎍]
   [ON ⎏]

To specify either CALL or IF IRQ mode:

1. When the IRQ feature has been turned on, a new field appears to the right of the IRQ field. Move the screen cursor to this new field. The default value for this field is "IF IRQ" ENABLED".

   IRQ [ON ⎍] ["IF IRQ" ENABLED]

2. Press the SELECT key until the desired mode appears in the field.

   [ON ⎍] ["IF IRQ" ENABLED]
   [CALL] [ ]

CALL mode requires you to enter the label of the interrupt service routine in the new field to the right of CALL.

To enter the label value for CALL mode:

1. Move the screen cursor to the new field that appears to the right of CALL.
2. Use the data entry keys to enter the LABEL name. You must enter this same LABEL name in the 91S16 Program: Run sub-menu on the first line of the interrupt service routine. For example, you could call the interrupt service routine INTR.

   IRQ [ON ⎍] [CALL] [INTR]

Interrupt Qualifier Field

When the IRQ field has been enabled, a new QUALIFIER field appears on the screen immediately below the IRQ field. This QUALIFIER field can be used to qualify whether or not the 91S16 responds to the interrupt request line.

The QUALIFIER signal is supplied via the P6460 External Control Probe. The interrupt qualifier signal must be connected to an external source for this feature to be available. You are not required to use the qualifier line in order to use the IRQ line. The QUALIFIER field defaults to DON'T CARE.

You can set the qualifier signal to be asserted for either high or low logic states. The QUALIFIER signal must have a 15 ns setup time relative to the selected edge of the IRQ signal. Hold time is 0 ns.

To set the QUALIFIER field's active state:

1. Move the screen cursor to the QUALIFIER field.

   QUALIFIER [X]

2. Use the data entry keys to enter either a 1 (positive-true) or a 0 (negative-true) value into the field.

   [1]

4 EXT JUMP Field

The EXT JUMP (External Jump) signal is tested by the IF EXT JUMP instruction which can be programmed in the 91S16 Program: Run sub-menu. The EXT JUMP field is used to select either positive-true (IF 1) or negative-true (IF 0) logic states for the external jump signal.

This signal is supplied via the optional P6460 External Control Probe. The EXT JUMP line must be connected to an external source. For the EXT JUMP signal to be asserted, it must have a 15 ns set-up time relative to the selected edge of the pattern generator clock. Hold time is 0 ns.

NOTE

The EXT JUMP field can not be disabled if you have programmed an IF EXT JUMP instruction in the 91S16 Program: Run sub-menu. To disable this field, you must first remove all IF EXT JUMP instructions.

To set the EXT JUMP active state:

1. Move the screen cursor to the EXT JUMP field.

   EXT JUMP [DISABLED]

2. Press the SELECT key until the desired value appears in the field:

   [IF 0]
   [IF 1]

5 PAUSE Field

The PAUSE signal is used to freeze the output of the pattern generator in its present state. While the pause signal is active, all pattern generator data, clock and strobe lines maintain their current levels. The PAUSE field is used to specify whether a pause condition is asserted as either a positive-true or a negative-true input signal. In default, the PAUSE field is disabled.

The pause signal is supplied via the optional P6460 External Control Probe. This signal line must be connected to an external source. To be asserted, the pause signal must have a 15 ns setup time relative to the selected edge of the pattern generator clock. Hold time is 0 ns.

To set the PAUSE field to be either positive-true or negative-true:

1. Move the screen cursor to the PAUSE field.

   PAUSE [DISABLED]

2. Press the SELECT key until the desired condition appears in the field:

   [ON 0]
   [ON 1]

6 INHIBIT (91S16 & 91S32) Field

The inhibit signal is used by both the 91S16 and 91S32 to selectively tri-state the outputs of the P6464 Pattern Generator probes. When the inhibit signal is asserted, any data line not masked by the INHIBIT MASK in the Program: Run sub-menu will be tri-stated.

The inhibit signal can be determined by logically combining the external inhibit line and the internal inhibit bit programmed in the Run sub-menu. You can choose to assert the inhibit signal as a simple reaction to either the internal inhibit bit, the external inhibit signal, or a combination of the two either ANDed or ORed together.

NOTE

The pattern generator will continue to execute its program even though an inhibit signal has been asserted. Some data may be output by the P6464 probes while an inhibit is asserted if those bits have been protected by the INHIBIT MASK in the Program: Run sub-menu.

The INHIBIT field is used to specify whether the internal and external inhibit signals are enabled on a positive-true (1) or negative-true (0) condition. Additional fields will appear when the INHIBIT field is enabled to allow you to combine the two inhibits using logical operators. In default, the INHIBIT field is disabled.

To set the asserted state for the internal and external inhibit signals:

1. Move the screen cursor to the INHIBIT field.

   INHIBIT [DISABLED]

2. Press the SELECT key until the desired condition appears in the field:

   [EXTERNAL 0] [ONLY]
   [EXTERNAL 1] [ONLY]
   [INTERNAL 0] [ONLY]
   [INTERNAL 1] [ONLY]

To select a logical relationship between the internal and external inhibits:

1. Move the screen cursor to the new field immediately to the right of the first condition field.
2. Press the SELECT key until the desired logical operator appears in the field.

   INHIBIT [EXTERNAL 0] [ONLY]
   [AND] [ ]
   [OR] [ ]

3. A new field appears to the right of the logical operator field. This field allows you to set the asserted state for the other inhibit signal. Move the screen cursor to this new field and press select until the desired value you want appears in the field. For example:

   [INTERNAL 0] [OR] [EXTERNAL 0]
   [EXTERNAL 1]

7 EXTERNAL START Field

The external start signal works like an external trigger. If the EXTERNAL START field has been set to ON and the START SYSTEM or START PAT GEN key has been pressed, the pattern generator will begin program execution when the external start signal is received.

The external start signal is supplied via the External Start Input phono connector located on the back of the 91S16 module. This is the bottom phono connector on the back of the circuit board. This connector must be connected to an external TTL-level signal source. To be asserted, the external start signal must have a minimum 15 ns pulse width.

The EXTERNAL START field is used to enable the external start feature on either the rising or falling edge of the input signal. In default, the EXTERNAL START field is disabled.

To select either the rising or falling edge to enable the external start signal:

1. Move the screen cursor to the EXTERNAL START field.

   EXTERNAL START [DISABLED]

2. Press the SELECT key until the desired value appears in the field.

   [ON ⌐]
   [ON ¬]

91S32 PROBE SUB-MENU FIELDS AND VALUES

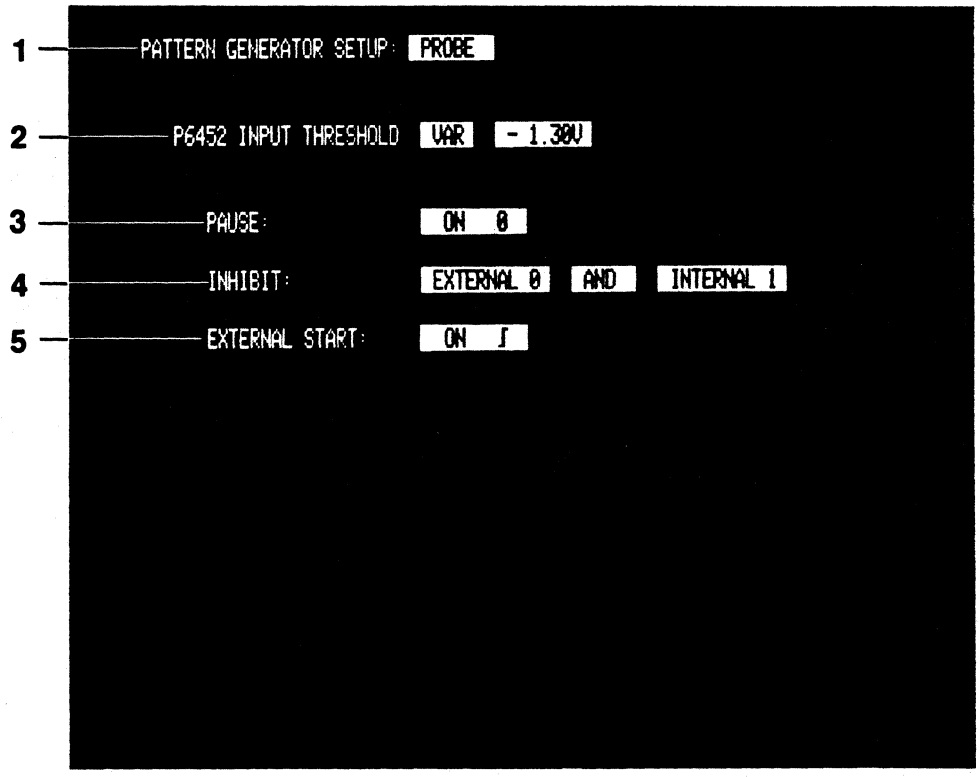
NOTE

The 91S32 Setup: Probe sub-menu will appear when 91S32 Modules are the only pattern generator cards installed. This menu will not appear if a 91S16 is installed.

The following paragraphs explain how you can use the Setup: Probe sub-menu to set up the P6452 External Clock (Data Acquisition) Probe when 91S32 modules are used without a 91S16 controller. (The P6452 probe connects to the DAS Trigger/Time Base module.) Each menu field is described and its optional values are explained.

Figure 3-11 illustrates the Probe sub-menu and its fields. The fields, which appear in reverse video on the screen, are bracketed [ ] throughout the text. The four directional cursor keys and the NEXT key can be used to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-11 when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.



5397-18

Figure 3-11. 91S32 Setup: Probe sub-menu.

1 PATTERN GENERATOR SETUP Field

Use this field (directly to the right of the menu title) to select either the Probe or the Timing sub-menu display. Refer to the description of sub-menu selections in the *Introduction to 91S16 and 91S32 Sub-Menus* section earlier in this addendum. The Probe sub-menu is the default display.

2 P6452 INPUT THRESHOLD Field

Use the P6452 INPUT THRESHOLD field to set the threshold level for the P6452 External Clock Probe. This probe supplies the pattern generator's external clock, pause, external inhibit, and external start signals.

NOTE

The P6452 External Clock Probe also supplies the external clock signal to the 91A32 Data Acquisition Modules. Therefore, any changes made to the probe's threshold in this menu will also affect the 91A32 external clock threshold. (Refer to the Trigger Specification Menu *section of this manual.)*

The P6452 External Clock Probe has a threshold-range switch. If this switch is set to NORM, the probe operates with a TTL/VAR threshold. If the switch is set to AUX, the probe operates with a MOS threshold. Once the probe switch has been set, the threshold field can be used to select the varying voltage levels for these thresholds.

If the probe is set to NORM, the threshold field defaults to TTL +1.40 V. This threshold can be changed to VAR (variable).

To change the P6452 INPUT THRESHOLD level field:

1. Move the screen cursor to the threshold field.

   [TTL] +1.4 V

2. Press the SELECT key until the desired threshold level appears in the field.

   The DAS displays optional threshold values in this order:

   [TTL] +1.40 V
   [VAR] [−1.30 V]

When VAR threshold is selected, a new field appears for setting the variable voltage level. The settings for this field range between +5.00 V and −2.50 V in 0.5 V increments. The voltage level may be changed by using the INCR and DECR keys.

If the P6452's threshold range switch has been set to AUX, the threshold field will show the MOS voltage range. This field may be set to a voltage level ranging between +20.00 V and −10.00 V in 0.20 V increments. Use the INCR and DECR keys to change the voltage level.

3 PAUSE Field

The pause signal is supplied via the P6452 External Clock Probe. This signal line must be connected to an external source. To be asserted, the pause signal must have a 19 ns set-up time and a 0 ns hold time (19 ns pulse width) relative to the selected edge of the clock.

The pause signal keeps the pattern generator outputs fixed at their last voltage states. While the pause line is enabled, all the pattern generator data and clock signals are held at their current levels.

The PAUSE field is used to specify whether a pause is enabled on a positive-true (1) or negative-true (0) condition. In default, the pause feature is disabled.

To set the PAUSE signal to be active-high (1) or active-low (0):

1. Move the screen cursor to the PAUSE field.

   PAUSE [DISABLED]

2. Press the SELECT key until the desired condition appears in this field.

   [DISABLED]
   [ON 0]
   [ON 1]

4 INHIBIT Field

The inhibit signal is generated by a logical operation of the internal and external inhibit signals. The internal inhibit signal can be programmed in the 91S32 Program Run sub-menu. The external inhibit signal line must be connected to an external source. Either inhibit signal can cause the pattern generator probes to be tri-stated.

NOTE

The pattern generator will continue to execute its program even though an inhibit signal has been asserted. Some data may be output by the P6464 probes while an inhibit is asserted if those bits have been protected by the INHIBIT MASK in the Program: Run sub-menu.

The INHIBIT field is used to specify whether the inhibit signals (internal and external) are enabled on a positive-true (1) or negative-true (0) transition. This field also allows you to select the logical operator combining the two inhibit signals. In default, the INHIBIT signal is disabled.

To set the INHIBIT field condition:

1. Move the screen cursor to the INHIBIT field.

   INHIBIT [DISABLED]

2. Press the SELECT key until the desired condition appears in the field.

   [EXTERNAL 0] [ONLY]
   [EXTERNAL 1] [ONLY]
   [INTERNAL 0] [ONLY]
   [INTERNAL 1] [ONLY]

To select the logical operator:

1. Move the screen cursor to the field following the first inhibit selection.

```
[ EXTERNAL 0 ] [ONLY]
               [AND ] [      ]
               [ OR ] [      ]
```

2. Press the SELECT key until the desired logical operator appears in the field. For example, select OR:

```
[ INTERNAL 0 ] [OR] [EXTERNAL 0]
```

3. A new field appears to the right of the logical operator field. This field allows you to set the asserted state for the other inhibit signal. Move the screen cursor to this new field and press select until the desired value you want appears in the field. For example:

```
[ INTERNAL 0 ] [OR] [EXTERNAL 0]
                    [EXTERNAL 1]
```

5 EXTERNAL START Field

The external start signal is supplied by the P6452 External Clock Probe. This external start line must be connected to an external source. To be asserted, the external start signal must have a 19 ns minimum pulse width.

The external start signal works line an external trigger. If the EXTERNAL START field is set to enabled and the DAS START SYSTEM or START PAT GEN key has been pressed, the pattern generator will begin pattern execution when the external start signal is received.

The EXTERNAL START field is used to enable the external start on either the rising or falling edge of the input signal. In default, the EXTERNAL START feature is disabled.

To select either the rising of falling edge to enable the external start feature:

1. Move the screen cursor to the EXTERNAL START field.

```
EXTERNAL START: [DISABLED]
```

2. Press the SELECT key until the desired value appears in the field.

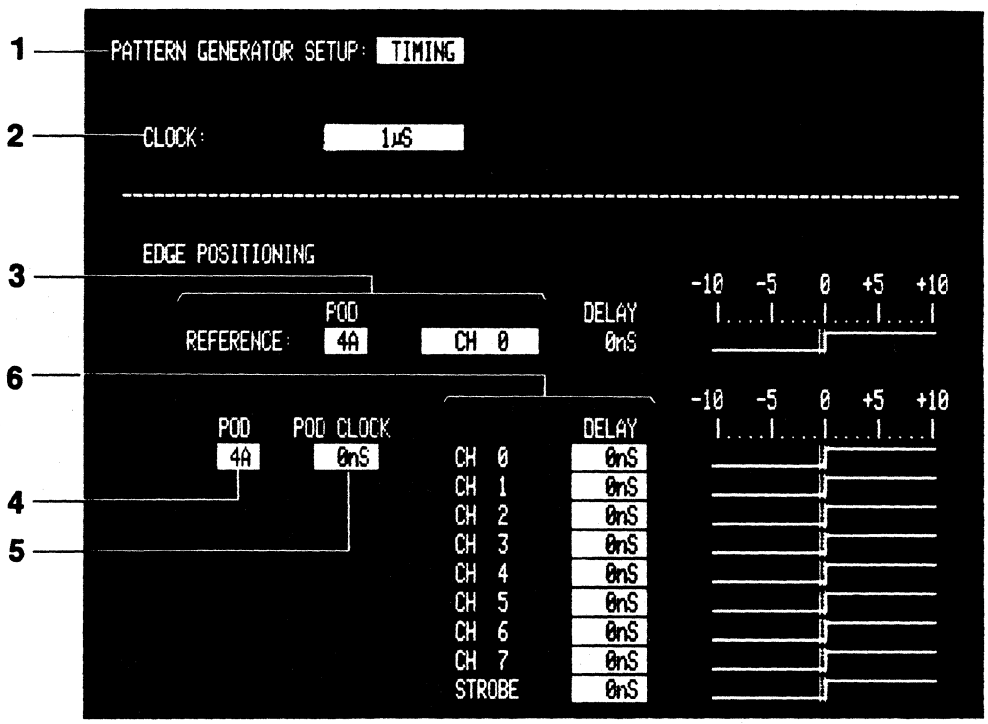
```
[ ON ⎍ ]
[ ON ⎏ ]
```

91S16 AND 91S32 TIMING SUB-MENU FIELDS AND VALUES

The following paragraphs explain how to use the Timing sub-menu to set up and adjust the 91S16 and 91S32 pattern generator pod and data channel timing relationships relative to the pattern generator master clock. Each menu field is described and all optional values are discussed.

Figure 3-12 illustrates the Timing sub-menu and its fields. The fields, which appear in reverse video on the screen, are bracketed [ ] throughout the text. The four directional cursor keys and the NEXT key can be used to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-12 when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.



5397-19

Figure 3-12. 91S16 and 91S32 Setup: Timing sub-menu.

1 PATTERN GENERATOR SETUP Field

The field directly to the right of the menu title is used to select either the Probe or the Timing sub-menu display. Refer to the *Introduction to 91S16 and 91S32 Sub-Menus* section earlier in this addendum. In default, the Probe sub-menu will be displayed.

To change the sub-menu to the TIMING sub-menu:

1. Move the screen cursor to the field directly to the right of the menu title.

   PATTERN GENERATOR SETUP: [PROBE]

2. Press the SELECT key until the Timing sub-menu appears in the field:
   [TIMING].

2 CLOCK Field

Use the CLOCK field to select the master input clock for the pattern generator. This clock is fed into the pattern generator (usually from the DAS Trigger/Time Base board) and is used to control the rate at which the pattern generator outputs clock and data signals to the circuit under test. The master clock can be supplied by an external clock source. In this case, the 91S16 External Clock signal is supplied via an optional P6460 External Control Probe. The External Clock signal, when only 91S32s are installed, is supplied via a P6452 External Clock Probe connected to the DAS Trigger/Time Base Module.

The CLOCK field optional settings depend on whether you are using just a 91S16, just 91S32s, or a combination of both. The optional values are as follows:

- 91S16 only

  DAS internal clock, selections ranging from 5 ms through 20 ns
  An external clock source: 50 MHz maximum (20 ns)

- 91S16 with 91S32s

  DAS internal clock, selections ranging from 5 ms through 20 ns
  at 50 MHz. all pod clock delays must be set to −5 ns
  An external clock source: 50 MHz. (20 ns)

- 91S32s only

  DAS internal clock, selections ranging from 5 ms through 20 ns.
  at 50 MHz. all pod clock delays must be set to 0 ns
  An external clock source can supply clocking signals between 5 ms and 40 ns.

NOTE

The DAS provides two internal clocks. These clocks are shared by the 91A32 and 91A08 data acquisition modules and the 91S16/32 pattern generator modules. Since it is possible to specify a different clock for each of these modules while only two are available, you must make sure that no more than two different clocks have been specified. Refer to the Start and Stop *section of the* DAS 9100 Series Operator's Manual *for details.*

The default CLOCK setting is the DAS internal clock, with an interval of 1 μs. Use the INCR and DECR keys to increase or decrease the clock interval as needed.

To increase or decrease the internal clock rate:

1. Move the screen cursor to the CLOCK field.

   CLOCK [1 μS]

2. Press the INCR key to increase the value or the DECR key to decrease the value.

   The DAS will display increasing or decreasing clock values in a 1-2-5 sequence.

An external clock source can also be selected using this field. You can also specify either the rising or falling edge of the external clock signal. The external clock for the 91S16 is supplied via an optional P6460 External Control Probe connected to Pod C on the back of the 91S16 module. The external clock for 91S32s used without a 91S16 is supplied via the P6452 External Clock Probe attached to the DAS Trigger/Time Base Module.

When an external clock source is selected for the 91S16, the P6460 INPUT THRESHOLD level is displayed in the field following the CLOCK field for reference purposes.

To select an external clock source:

1. Move the screen cursor to the CLOCK field.

   CLOCK [1 μs]

2. Press the SELECT key until the desired clock value appears in the field.

   The DAS will display the available clock values in this order:

   [1 μs]
   [EXTERNAL ⌐]
   [EXTERNAL ¬]

3 REFERENCE Field

The REFERENCE field is used to select any data channel, strobe, or pod clock line you choose to use as a timing reference when programming the edge position of a particular pod's data and strobe channels.

The REFERENCE field is divided into two parts: POD, which specifies the pod I.D. for your reference channel; and the field following POD, which specifies a data channel, strobe, or pod clock line. The delay value of the reference signal relative to the pattern generator master clock is displayed in the DELAY field for your information; the value cannot be changed in this field. The delay value is also graphically represented as a positive-true signal for ease of comparison.

The default channel for the REFERENCE field is CH 0 of pod A anytime a 91S16 is installed. When only 91S32s are installed, the REFERENCE field default channel will be Channel 0 of pod A from the 91S32 installed in the highest-numbered DAS slot; for instance: CH 0, POD 6A.

To specify a different reference channel:

1. Move the screen cursor to the POD field.

   ```
                        POD
   REFERENCE [6A] [CH 0]
   ```

2. Use the data entry keys to enter any available pod I.D. For example, 5B.

   [5B] [CH 0]

To select the data channel, strobe, or pod clock:

1. Move the screen cursor to the field following the POD field.

   ```
                        POD
   REFERENCE [6A] [ CH 0]
   ```

2. Press the SELECT key until the desired reference channel appears in the field.

   The DAS displays the data channels, strobe, and clock lines in this order:

   [CH 0]
   [CH 1]
   [CH 2]
   [CH 3]
   [CH 4]
   [CH 5]
   [CH 6]
   [CH 7]
   [STROBE]
   [POD CLOCK]

4 POD Field

The POD field is used to specify the name of the pod you want displayed. Any available pod I.D. can be entered. The POD field defaults to either the 91S16 Pod A when a 91S16 is installed, or Pod A for the 91S32 in the highest-numbered DAS slot when only 91S32s are installed.

To select a pod for timing adjustment:

1. Move the screen cursor to the POD field.

   POD
   [6A]

2. Use the data entry keys to enter any available pod I.D. For example, enter 5B:
   [5B]

5 POD CLOCK Field

The POD CLOCK field is used to adjust the timing of all the signals associated with this pod at one time. The adjustment is made in relation to the pattern generator's master clock. The master clock determines the start of each cycle.

Use the INCR or DECR keys to set the POD CLOCK delay value. The POD CLOCK delay value can be set ± 5 ns relative to the master clock. Each pod may have a different POD CLOCK delay value. In default, all the pod clocks have a delay value of 0 ns. The POD CLOCK delay values may also be changed in the Configuration sub-menu.

Remember that 91S32s operating at 50 MHz. with a 91S16 must have their pod clock delays set to −5 ns. 91S32s operating at 50 MHz. without a 91S16 must have thier pod clock delays set to 0 ns.

To increase or decrease the POD CLOCK delay:

1. Move the screen cursor to the POD CLOCK field:

   POD CLOCK
   [0 nS]

2. Use the INCR key to increase the delay value, or the DECR key to decrease it. The adjustment can be made in 5 ns intervals, displayed by the DAS in the following order:

   [−5nS]
   [0nS]
   [+5nS]

6 DELAY Field

The DELAY field is used to set the delay value for each of the data channels and the strobe lines relative to the pod clock. Each data channel and strobe line may have a different delay value. Use the INCR or DECR keys to adjust the delay value in 1 ns increments within a −5 ns to +5 ns range relative to the pod clock.

The DAS will display the total delay relative to the pattern generator's master clock for each channel (including the pod clock delay) in the DELAY field. The delay value for each data channel and the strobe line will be graphically represented as a rising edge in the timing diagram. In default, all the delay values are set to 0 ns.

NOTE

If you have used the Timing menu to adjust for pulse misalignment at the P6464 probe tips, the delay values and graphic representation of timing relationships shown in this menu will be misleading. You must remember to account for any data skew adjustments made via this menu. Alternatively, there is a deskew procedure using internal delay lines that will not affect the timing relationships shown in this menu; that procedure can be found in the DAS 9100 Series 91S16/32 Service Addendum *(p/n 070-5397-00).*

To increase or decrease the data channel and strobe delay:

1. Move the screen cursor to the DELAY field.

   CH 0 [0nS]
   CH 1 [0nS]
   CH 2 [0nS]
   CH 3 [0nS]
   CH 4 [0nS]
   CH 5 [0nS]
   CH 6 [0nS]
   CH 7 [0nS]
   STROBE [0nS]

2. Use the INCR key to increase the delay value, or the DECR key to decrease it.

   The delay value can be adjusted in 1 ns increments from −5 ns to +5 ns relative to the pod clock.

91S16 PROGRAM: RUN MODE SUB-MENU

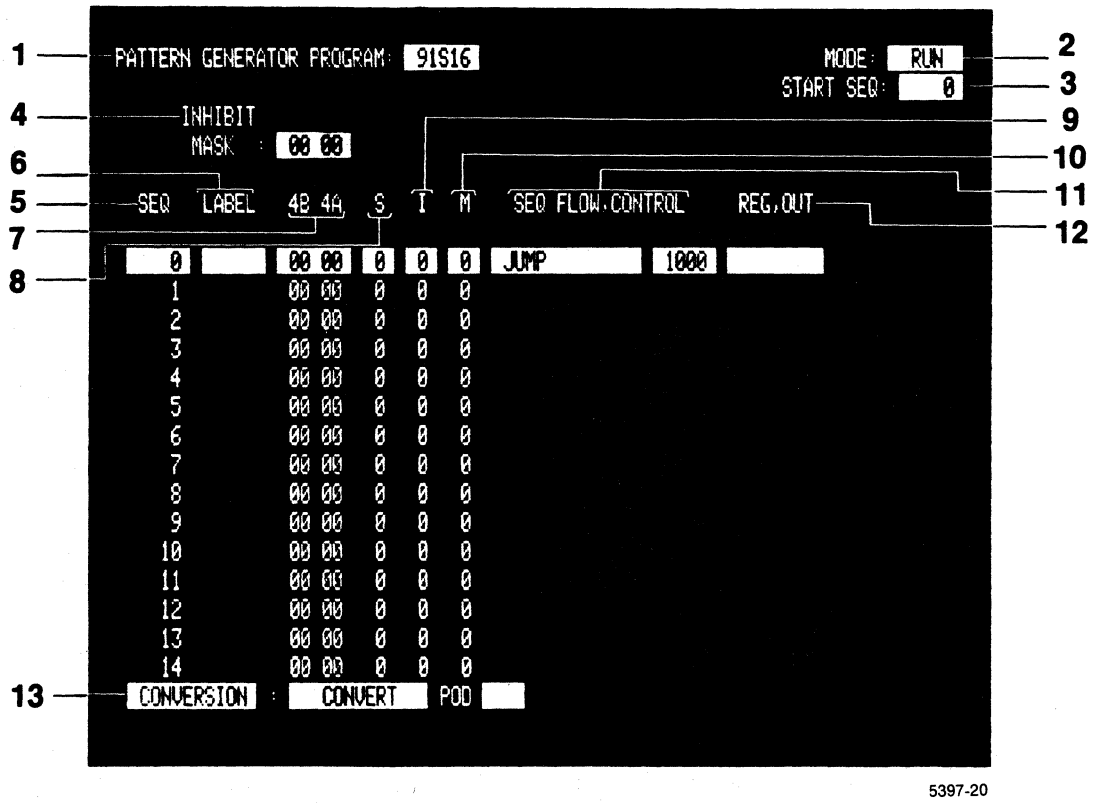
NOTE

The 91S16 Program Run Mode sub-menu appears only when the 91S16 Module is installed.

The following paragraphs show how to use the 91S16 Program Run Mode sub-menu to enter instructions and patterns for the 91S16 Pattern Generator Module. They discuss each menu field and explain all optional values.

Figure 3-13 illustrates the 91S16 Pattern Generator Run Mode sub-menu and its fields. The fields, which appear in reverse video on the screen, are bracketed [ ] throughout the text. The four directional cursor keys and the NEXT key can be used to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-13 when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.



5397-20

Figure 3-13. 91S16 Program: Run sub-menu.

NOTE

In the following discussion, the 91S16 Module is assumed to reside in slot 4.

1 PATTERN GENERATOR PROGRAM Field

Use this field (directly to the right of the menu title) to select either the 91S16 or the 91S32 sub-menu display. Refer to the *Introduction to 91S16 and 91S32 Sub-Menus* section of this addendum. In default, the 91S16 Program: Run sub-menu is displayed whenever a 91S16 Module is installed in the DAS.

2 MODE Field

Use the MODE field to select the pattern generator's operating mode. The pattern generator normally outputs data in real-time, synchronously with the clock signal. This mode of operation is called Run mode, hence the name of this menu. For debugging purposes ,the pattern generator can also output data at much slower rates, or even one step at a time. These modes of operation are called Trace and Step, and are described under the *Trace and Step Mode Sub-Menus* sections of this addendum. Descriptions of Trace and Step sub-menus are listed separately for the 91S16 and the 91S32.

Press the SELECT key while the screen cursor is in the MODE field to change between Run, Trace, and Step modes. The MODE field defaults to Run mode on power-up.

3 START SEQ Field

Use the START SEQ field to set the first sequence number the pattern generator will execute when the START PAT GEN key or the START SYSTEM key is pressed. The START SEQ field may be set to any number between 0 and 1023 as long as no interrupt service routine is programmed. If an interrupt service routine has been programmed, the START SEQ field can be set to any number between 0 and 1022.

To set the START SEQ field:

1. Move the screen cursor to the START SEQ field.

   START SEQ: [0]

2. Use the data entry keys to enter the number of the sequence line where you want program execution to begin. For example, 500. The value you enter will appear in the field.

   START SEQ: [500]

4 INHIBIT MASK Field

Use the INHIBIT MASK field to specify whether or not the data output channels respond to the inhibit (tri-state) signal. If the inhibit mask for a given data channel is set to 0 (unmasked), the data channel is tri-stated whenever the inhibit signal is asserted. If the inhibit mask is set to 1 (masked), then the inhibit signal is masked out and that data channel is not tri-stated, even though the inhibit signal has been asserted. The inhibit mask can be set for each individual data channel by specifying a value in the INHIBIT MASK field (default radix is hexadecimal). The default value for this field is 0, unmasked for all data channels.

To set the INHIBIT MASK field:

1. Move the screen cursor to the INHIBIT MASK field.

```
INHIBIT
 MASK    : [00 00]
```

2. Use the data entry keys to specify the desired inhibit mask. The value you enter will appear in the field. The display radix of this field matches the radix you have selected for the data fields. This example shows hexadecimal values.

```
         : [F0 A0]
```

5 SEQ (Sequence) Field

The SEQ field consists of a column of numbers on the left side of the display. Each number in this column corresponds to one program line. The program lines are displayed sequentially starting with SEQ 0. There is a total of 1024 sequence lines labeled 0-1023. Only a portion of these sequence lines are displayed at any given time.

Several methods are available to enable you to display different sequence lines. The first method is to use the scroll keys. These keys can be used at any time, and when the cursor is in any field.

To scroll through the sequence lines:

Press the up (↑) or down (↓) scroll key. Additional sequence lines will scroll up from the bottom or down from the top of the display.

The second method used to view different sequence lines is to enter the desired sequence number directly into the SEQ field. This method allows you to jump forward or backward and display specific blocks of sequence lines.

To move forward and display larger-numbered sequence lines:

1. Move the screen cursor to the sequence number you wish to change. For example, move the cursor to SEQ 11:

```
   SEQ

[  11]
```

2. Use the data entry keys to enter the first sequence number you wish to have displayed. For example, SEQ 200. The DAS will display [200] in place of [11], and then update the rest of the sequence lines following that position.

```
SEQ
  0
  1
  2
  3
  4
  5
  6
  7
  8
  9
 10
[ 200]   SEQ 11 is changed to SEQ 200,
 201     and the rest of the sequence
 202     numbers are automatically updated
 203     from that position through the
 204     bottom line of the display.
 205
```

NOTE

When using the above procedures, observe the following two rules. First, if the cursor is positioned below the top sequence number on the display, you cannot enter a number smaller than the number directly above the cursor location. Second, you cannot enter a number greater than 1023 (1022 if IRQ CALL is used).

To move backward to a smaller-numbered block of sequence lines:

1. Move the screen cursor to the SEQ field of the line where you want the smaller sequence number to be displayed. For example, SEQ 200.

```
SEQ
[ 200]
```

2. Press the DON'T CARE key.

   The DAS will enter a 0 at this sequence number location.

NOTE

The number you enter must be larger than the number in the SEQ field immediately above the cursor location. Use the top field in the display if you want to view SEQ lines smaller than any currently displayed.

3. Use the data entry keys to enter the sequence number you wish to display. For example, SEQ 15. The DAS will display 15 at that sequence number location, and then update the remaining sequnce numbers on the screen from that position.

```
SEQ

  0
  1
  2
  3
  4
  5
  6
  7
  8
  9
 10
[ 15]  SEQ 200 is changed to SEQ 15
 16    and the display is updated
 17    from this position to the
 18    bottom of the screen.
 19
 20
```

6 LABEL Field

Use the LABEL field for labeling specific program lines. These labels serve as destinations for three types of pattern generator instructions: JUMP, IF <*condition*> JUMP, and INTERRUPT CALL. (IF <*condition*> JUMP instructions include IF R=0, IF KEY, IF IRQ, etc.) All three of these instruction types transfer program flow to a line containing a specific label; they do not specify a destination according to a sequence line number.

You can assign a total of 15 labels in a 91S16 program. Each label may be up to four characters wide, and may include letters, numbers, and spaces.

To assign a label for a specific program line:

1. Move the screen cursor to the LABEL field associated with that program line.

```
SEQ     LABEL     4B 4A
[   0]  [     ]   [00 00]
```

2. Use the data entry keys to enter the label. For example, INIT. The DAS will display INIT in the LABEL field for that particular sequence line.

```
SEQ     LABEL     4B  4A
[   0]  [INIT]    [00 00]
```

To remove a label:

1. Move the screen cursor to the LABEL field you wish to remove.

```
 SEQ    LABEL    4B  4A
[  0]   [INIT]   [00 00]
```

2. Press the DON'T CARE (X) key. The label will be deleted from the field.

```
 SEQ    LABEL    4B  4A
[  0]   [    ]   [00 00]
```

7 #A and #B Pattern Fields

The A and B fields that appear on the menu are used to specify the data pattern you wish to output through the P6464 probes. The A field header designates the data pattern output through Pod A, and the B field header designates Pod B. The number that appears before the A and the B corresponds to the slot in the DAS where the 91S16 card resides.

Enter data patterns you wish to output line by line, one pod at a time. Use the DISPLAY editing command if you wish to change the radix of the data you are entering. The default radix is hexadecimal. Data patterns always default to 0.

See the *DISPLAY Editing Command* paragraphs later in this section for information about changing the display radix of the data columns and inhibit mask.

To enter data on any program line:

1. Move the screen cursor to the pattern field in the line you wish to program. Position the cursor under the label for the pod you wish to program.

```
 SEQ  LABEL    4B 4A
[  0] [    ]   [00 00]
```

2. Use the data entry keys to program the pattern you desire. The DAS will display the data values you have entered in the field and then shift the cursor one space to the right. For example, enter the value 30*hex* for Pod B.

```
 SEQ  LABEL    4B 4A
[  0] [    ]   [30 00]
```

3. Continue entering data values until both pods have been programmed. Then press the NEXT key to move the cursor to the first data field of the next line.

8 S (Strobe) Field

Use the S (Strobe) field to select whether or not the strobe channels associated with each pod will output signals when this particular program line is executed. Setting a 0 value for this field means that neither the Pod A nor the Pod B strobe will be output. Setting a 1_{hex} means that only the Pod-A strobe is output, while a 3_{hex} means that both Pod A and Pod B strobes are output. You can program this field on a line-by-line basis, or you can use the FILL command to program whole blocks of sequence lines in one operation. See the *FILL Editing Command* paragraphs later in this section for details.

Strobe transitions are synchronous with the output clock. In default, the strobe field is set to 0 (no strobes).

To assert a strobe:

1. Move the screen cursor to the S field on the line you wish to program.

```
SEQ   LABEL   4B 4A      S
[   0] [    ] [00 00]    [0]
```

2. Use the data entry keys to enter the data value you desire. The 91S16 Strobe field contains 2 bits; the left bit correspods to Pod B, and the right bit corresponds to Pod A. Default display radix is hexadecimal.

   For example, to assert both the Pod A and Pod B strobes, enter a *3hex*.

```
SEQ   LABEL   4B 4A      S
[   0] [    ] [00 00]    [3]
```

9 I (Inhibit) Field

Use the I (Inhibit) field to set the internal inhibit signal. It is used to temporarily tri-state the output of either Pod A or Pod B. (Tri-state is TTL-level high impedance, and ECL-level logical low.) The polarity of both the internal and external inhibit signals is programmable in the 91S16 Setup: Probe sub-menu. The probes can also be programmed to react to a logical combination of the internal and external inhibit signals. See the *91S16 Setup: Probe Sub-Menu* section in this manual.

For the following example, assume the following values have been set for the internal and external inhibits: External Inhibit 1 **OR** Internal Inhibit 1, positive-true signals.

Setting a 0 in the I (Inhibit) field means that neither pod is tri-stated and both pods will continue to output data, clock, and strobe lines. Setting a *1hex* in this field will tri-state the outputs of Pod A. Setting a *3hex* will cause both Pod A and Pod B to be tri-stated.

Note that some data may still be output from a pod that has been tri-stated, because any value you set in the INHIBIT MASK field will cause specific data lines to ignore the inhibit signal.

You must set values for the I (Inhibit) field for every sequence line. The default value is 0 (no pods are tri-stated) and the default radix is hexadecimal. The internal inhibit signal becomes effective synchronously with the output clock.

To set an internal inhibit:

Move the screen cursor to the line you wish to program and position the cursor over the I field. Use the data entry keys to enter the appropriate value. For example, to assert the internal inhibits for both Pod A and Pod B, (with the Setup: Probe sub-menu INHIBIT field set to [INTERNAL 1]) enter a 3*hex*.

SEQ	LABEL	4B 4A	S	I
[0]	[ ]	[00 00]	[0]	[3]

10 M (Interrupt Mask) Field

Use the M (Interrupt Mask) field to mask out external interrupt signals received from the P6460 probe. Entering a 1 in the M field of a particular sequence line causes the pattern generator to ignore external interrupt signals during execution of that program line. This feature allows you to protect certain programming routines from being interrupted.

The M field must be set to 1 in each line you wish to protect. In default, the M field is set to 0 (unmasked).

To mask an interrupt:

Move the screen cursor to the M field in the line you wish to program. Use the data entry keys to enter a 1. The DAS will display a 1 in the M field.

SEQ	LABEL	4B 4A	S	I	M
[0]	[ ]	[00 00]	[0]	[3]	[1]

11 SEQ FLOW, CONTROL Fields

The SEQ FLOW and CONTROL fields displayed on the DAS screen correspond to the identically named keys grouped on the left-hand side of the DAS keyboard. SEQ FLOW (sequence flow) identifies a series of programming instructions that affect the order of sequence line execution (i.e.. branching, conditional branching, and halt). Selecting a SEQ FLOW instruction may cause other fields to appear. The CONTROL key allows you to select instructions that control 91S32 pattern generator cards, or issue triggering cues to some external device. CONTROL instructions are optional and will appear in the same field as SEQ FLOW instructions.

There are five basic types of SEQ FLOW instructions and two CONTROL instructions. The default for both types of instruction is no operation, which means the SEQ FLOW, CONTROL field will be blank and the pattern generator will output its data and then advance to the next sequence line.

SEQ FLOW instructions include IF <*condition*> JUMP <*label*>, JUMP <*label*>, CALL RMT (call remote), RETURN, and HALT.

CONTROL instructions are INCR PAGE (increment page) and TRIGGER. INCR PAGE issues a command to 91S32s operating in Follows 91S16 mode (INCR PAGE is only available when the Memory Reload From Host field is set to OFF). TRIGGER causes a trigger signal to be output to some external device (e.g., an oscilloscope) via the trigger-out phono connector on the back of the 91S16 module.

NOTE

When entering SEQ FLOW and CONTROL instructions, position the screen cursor on any reverse-video field associated with the sequence line you wish to program.

To enter SEQ FLOW and CONTROL instructions on a sequence line:

1. Move the screen cursor to any field on the line you wish to program.
2. Press the SEQ FLOW or CONTROL key until the instruction you desire appears in the field. The DAS displays the SEQ FLOW instructions in the following order:

```
[HALT          ]
[JUMP          ][      ]
[IF RA=0 JUMP ][      ]
[IF RB=0 JUMP ][      ]
[IF R=0 JUMP   ][      ]
[IF IRQ JUMP   ][      ]
[IF EXT JUMP   ][      ]
[IF KEY JUMP   ][      ]
[IF FULL JUMP  ][      ]
[IF END JUMP   ][      ]
[RETURN        ]
[CALL RMT      ]
```

The DAS displays the optional CONTROL instructions in this order:

```
[TRIGGER   ]
[INCR PAGE ]
```

To remove an instruction from a SEQ FLOW, CONTROL field:

Move the screen cursor to the SEQ FLOW, CONTROL field containing the instruction you wish to remove. For example, to remove the IF RA=0 instruction, place the screen cursor in the SEQ FLOW, CONTROL field and press the DON'T CARE key. The DAS will remove the instruction and leave the field blank.

To add a SEQ FLOW, CONTROL field to a sequence line:

1. Move the screen cursor to the SEQ FLOW, CONTROL field of the sequence line you wish to program.
2. Press the ADD LINE key on the DAS keyboard to add a new SEQ FLOW, CONTROL field. This will not add a new numbered sequence line; it simply creates space for you to program additional SEQ FLOW or CONTROL instructions affecting the current sequence line. The new SEQ FLOW, CONTROL field will appear in place of the field you already programmed and the original field will be displayed one line below.

   You may add up to two additional CONTROL fields for each sequence line (only one SEQ, FLOW instruction per line allowed). For example, if you want to output the external trigger signal at this point and switch any 91S32s operating in Follows 91S16 mode from one page of memory to the other, you can program those instructions as follows:

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[INCR PAGE] [TRIGGER] [IF RB=0 JUMP]	[*label*]

The SEQ FLOW, CONTROL instructions may be entered in any order. When the instruction sequence is redisplayed, it is displayed in a pre-defined order that reflects the order of execution. All instructions programmed on a give sequence line will be executed.

To delete a SEQ FLOW, CONTROL field that has been added:

1. Move the cursor to the SEQ FLOW, CONTROL field you wish to delete.
2. Press the DELETE LINE key as many times as necessary. The DAS will delete a SEQ FLOW, CONTROL field each time the DELETE LINE key is pressed.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[INCR PAGE] [IF RB=0 JUMP]	[*label*] [ ] [*label*]

NOTE

If you press the DELETE LINE key while the cursor is on a single line, all the instructions on that line will be removed.

Each SEQ FLOW and CONTROL instruction has individual performance characteristics. Several of these instructions require labels as additional parameters. The following paragraphs briefly describe each instruction and its capabilities.

HALT. Normally, the pattern generator runs through all 1024 sequence lines before stopping program output (assuming no loop or branch instructions are programmed). By using the HALT instruction, you may program the pattern generator to stop output on any sequence line.

When the pattern generator encounters a HALT instruction, it outputs the clock, data, and strobe values associated with that sequence line and then halts. If the HALT instruction is encountered on the first line the pattern generator executes, data and strobe signals are sent to the probe tips, but not the clock signal; no clock transition occurs.

When entered on a program line, the HALT instruction appears like this:

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[HALT]	

JUMP. Use the JUMP instruction to implement program jumps. Normally, the pattern generator outputs data in a straightforward line-by-line sequence. The JUMP instruction, however, alters this sequential flow by specifying a jump from one program line to another. Sequential program execution then resumes at that point.

When entered on a program line, the JUMP instruction appears like this:

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[JUMP]	[*label*]

Use the empty field next to JUMP to enter the LABEL of the sequence line where you want program execution to resume. For instance:

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
98	[INIT]	00 00	0	0	0	[ ]	
99	[ ]	00 00	0	0	0	[ ]	
100	[ ]	00 00	0	0	0	[JUMP]	[INIT]

INIT could be the name of a block of patterns used to test the initialization software in the device under test. In this case, you would type INIT in the LABEL field of the line you wished to jump to. Information about entering a name in the LABEL field is located in the *LABEL Field* paragraphs found later in this *91S16 Run Menu* section. Enter the label by using the data entry keys on the the DAS keyboard.

IF <conditional> JUMP. Use the IF <conditional> JUMP instruction to implement test and branch instructions. Normally, the pattern generator outputs data in a straightforward line-by-line sequence. The IF <conditional> JUMP instruction, however, alters this sequential flow when the conditions of the IF statement are satisfied. When the IF condition is satisfied, program flow is transferred to the line containing the label specified after JUMP.

For example:

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
98	[INIT]	00 00	0	0	0	[ ]	
99	[ ]	00 00	0	0	0	[ ]	
100	[ ]	00 00	0	0	0	[IF R=0 JUMP]	[INIT]

When executed, this program line tests the pattern generator's register to see if it has the value 0. If R does equal 0, then program execution would resume at the sequence line that contained INIT in the LABEL field.

The DAS displays the conditional tests for the IF <conditional> JUMP instruction in this order:

RA=0
RB=0
R=0
IRQ
EXT
KEY
FULL
END

The following paragraphs briefly describe each conditional test.

IF RA=0 JUMP, IF RB=0 JUMP. The RA=0 and the RB=0 tests instruct the pattern generator to examine the contents of either register RA or register RB. IF RA=0 JUMP instructs the pattern generator to examine the contents of register RA and branch if the value in RA equals 0.

IF R=0 JUMP. The IF R=0 JUMP conditional test works the same as the IF RA=0 and IF RB=0 tests described above, only this test is performed on the combined 16-bit register named "R" (where R = RA + RB).

NOTE

The instruction for R=0 is not displayed in the list of possible instructions if you have configured the pattern generator register to be two 8-bit registers named RA and RB. Similarly, the conditional tests RA=0 and RB=0 are not included if you have configured the pattern generator register to be one 16-bit register called R. See the 91S16 Configuration Menu *section for more information about using the 91S16 Pattern Generator's internal register.*

IF IRQ JUMP. The IF IRQ JUMP conditional test instructs the pattern generator to examine the status of the P6460's IRQ (interrupt request) line. If the P6460 has detected a transition on this line prior to this clock cycle, the condition is considered to be true. When a transient on the IRQ line meets the following conditions, it can be recognized as an interrupt:

1. IRQ polarity and level as specified in the 91S16 Probe sub-menu have been satisfied.
2. The QUALIFIER line is driven to satisfy the level specified in the 91S16 Probe sub-menu.
3. The Interrupt Mask bit (M) is set to 0 (unmasked) in the 91S16 Program sub-menu.
4. The selected IRQ edge must occur 15 ns prior to the selected edge of the external clock (minimum pule width is 15 ns).

NOTE

When the IRQ is disabled or the CALL is selected in the 91S16 Probe sub-menu, the IF IRQ JUMP instruction is not included in the list of conditional tests.

NOTE

Since the pattern generator resets all the lines from the P6460 External Control Probe at the start of execution, any external control signal test in the first sequence line executed will fail to meet its setup and hold time specifications. If the first line executed contains an IF IRQ JUMP instruction, the pattern generator will not jump even if an interrupt has been requested.

IF EXT JUMP. The IF EXT JUMP conditional test instructs the pattern generator to examine the status of the EXT JUMP (external jump) line of the P6460 External Control Probe. If the the EXT JUMP line meets the threshold level specified in the 91S16 Probe sub-menu, then the condition is considered to be true. Program execution will resume at the sequence line containing the label specified.

NOTE

When EXT JUMP is disabled in the 91S16 Probe sub-menu, the IF EXT JUMP conditional test is not displayed in the list of options.

NOTE

Since the pattern generator resets all the lines from the P6460 External Control Probe at the start of execution, the EXT JUMP signal will not meet its setup and hold time specifications for the first sequence line executed. If the first line executed contains an IF EXT JUMP instruction, the pattern generator will not jump even if the EXT JUMP line has been asserted.

IF KEY JUMP. The IF KEY JUMP conditional test instructs the pattern generator to determine whether the SHIFT START PAT GEN key on the DAS keyboard has been pressed. If the key was pressed before this sequence line was executed, the condition is considered to be true. This conditional test allows communication between the user and the pattern generator while the system is running. In this way, you can advance control of the pattern generator from one linked looping routine to another by pushing the SHIFT START PAT GEN KEY.

IF FULL JUMP and IF END JUMP. The IF FULL and IF END conditional tests are used to support the 91S16's Pattern Download From Host feature. In order to use these tests, you must be using a 91S16 to control the output of one or more 91S32s. Refer to the *91S32 Configuration Sub-Menu When Used With 91S16* section of this addendum for a description of the Pattern Download From Host feature.

Large patterns downloaded from a host computer often require more memory than the 2048-line maximum available with the 91S32. The Pattern Download From Host feature enables you to divide a larger pattern generator program into 1024-line blocks, output one block of program lines, download another block of sequence lines, output the new page of vectors, and continue the process until the entire program has be executed. The Pattern Download For Static Devices version does not output any vectors while a new block of vectors is being downloaded from the host.

The Pattern Download For Dynamic Devices (Keep-Alive) version does provide some 91S16 vectors to the system under test while the 91S32s are being reloaded. This mode of operation allows you to keep dynamic circuit elements active while the pattern generator is reloaded. Keep-Alive is only available with the Option 06 GPIB interface. IF FULL JUMP and IF FULL END are used to support the Keep-Alive subroutine. See the section of this addendum titled *GPIB Programming* for detailed instructions about Keep-Alive programming.

IF FULL tests to see if the GPIB controller has sent key code 47 to the DAS. Key code 47 indicates that the data transfer is complete. IF FULL then causes the 91S32s to switch program execution to the newly refilled memory page.

IF END tests to see if the GPIB controller has sent key code 46 to the DAS. Key code 46 indicates that all data transfers have been complete. IF END JUMP *<label>* then transfers program execution to some final sequence lines designated by the label.

NOTE

The IF FULL and IF END conditional tests are not displayed in the list of field options if the 91S32 Configuration *sub-menu MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) field has not been set to ON.*

RETURN. The RETURN instruction is used in conjunction with the IRQ enabled CALL *<label>* instruction programmed in the 91S16 Probe sub-menu. When the Probe sub-menu IRQ field has been set to CALL, a label field appears. You can then enter a label name in this field that corresponds to a set of sequence lines specifically designed to service the interrupt request. For example, call the label RSET.

```
PATTERN GENERATOR SETUP:   [PROBE]

  P6460 INPUT THRESHOLD    [TTL ] + 1.4V

    IRQ                    [ ON ⌐ ] : [  CALL  ] [RSET]
        & QUALIFIER        [ 1 ]

    EXT JUMP:              [DISABLED]

    PAUSE:                 [DISABLED]

    INHIBIT:               [DISABLED]
    (91S16 & 91S32)

    ------------------------------------------------

    EXTERNAL START     [DISABLED]
```

When an interrupt request has been detected on the IRQ line from the P6460 External Control Probe, program execution transfers to the sequence line containing the label given in the Probe sub-menu. (It is possible to mask out the interrupt signal using the M field in the Program Run sub-menu.) In the example, suppose the pattern generator was executing sequence 100 at the time the interrupt request was detected. After executing line 100, the pattern generator would execute the sequence line containing RSET in the label field. Pattern execution will continue sequentially from that line until a RETURN instruction is encountered in the SEQ FLOW, CONTROL field. Pattern execution will then resume at sequence line 101.

NOTE

The RETURN instruction must only be used in conjunction with the IRQ CALL instruction. If a RETURN is executed before a IRQ CALL, the RETURN instruction acts like a call to itself, and the pattern generator will become caught in an endless loop.

```
SEQ   LABEL    4B 4A    S   I   M   SEQ FLOW, CONTROL   REG, OUT
 100  [     ]  00 00    0   0   0
  .
  .
  10  [RSET]   FF FF    0   0   0   [                  ]
  11           AF 00    0   0   0   [                  ]
  12           AA 1E    0   0   0   [ RETURN           ]
  .
  .
 101           00 00    0   0   0   [                  ]
```

The RETURN instruction is programmed in the SEQ FLOW, CONTROL field in the last sequence line designed to service the interrupt request. Program flow continues on the sequence line following the one being executed when the interrupt request was detected.

NOTE

The RETURN instruction will not be displayed in the instruction list if the 91S16 Probe sub-menu's IRQ field is set to DISABLED or IF IRQ JUMP.

CALL RMT The CALL RMT (call remote device) instruction is part of the Pattern Download for Dynamic Devices (Keep-Alive) feature that allows the pattern generator to reload its memory from an external device. The other instructions associated with the Keep-Alive feature are IF FULL JUMP, and IF END JUMP.

CALL RMT is enabled when you set the MEMEORY RELOAD FROM HOST (FOR KEEP-ALIVE) field to ON in the 91S32 Configuration sub-menu.

NOTE

CALL RMT is only available when you are using DAS Option 06 GPIB. All restrictions that apply to Keep-Alive also apply to the CALL RMT instruction. Refer to the GPIB Programming *section of this addendum.*

The CALL RMT instruction issues an SRQ on the GPIB bus. This command is normally programmed to signal a host computer or external memory device that one page of the 91S32's pattern memory is ready to be reloaded. This signal can also be used in other situations, such as in automated test equipment (ATE), when you want to signal any external device when the pattern generator executes a certain program line.

NOTE

The CALL RMT instruction is not a subroutine. It is a control instruction which asserts an SRQ on the GPIB bus. When the controller performs a serial poll of the DAS, status byte 197 is returned to the controller. This instruction does not save a return address on the stack.

NOTE

Another CALL RMT instruction is valid only after the IF FULL JUMP instruction has been executed.

NOTE

If no 91S32 module is installed, or the MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) field is set to OFF in the 91S32 Configuration sub-menu, the CALL RMT instruction is not included in the instruction selection list.

TRIGGER. Use the TRIGGER instruction to generate an external device trigger signal. The trigger signal appears at the trigger output phono connector located near the probe connectors on the back of the 91S16. Use the optional 79-inch phono-to-BNC cable to connect the trigger output connector to an external device (such as an oscilloscope). This trigger signal is a positive-true, TTL-level, NRZ (non-return-to-zero) signal. It stays TTL-high for one cycle each time it is programmed.

NOTE

If the TRIGGER instruction is programmed for several consecutive sequence lines, the pulse width of the TRIGGER signal will widen in proportion to the number of TRIGGER instructions. For example, if you program the TRIGGER instruction in line 100 and line 101, the TRIGGER output signal will stay high for two clock cycles.

INCR PAGE The INCR PAGE (increment page) instruction is used when 91S32s are used in Follows 91S16 mode and the 91S32 Configuration sub-menu Memory Reload From Host field is set to OFF. Because the 91S32s have twice as much memory as the 91S16, it is often convenient to divide that memory into two 1024-line pages. These pages are called Page A and Page B. You may want to repeat the program loaded into Page A until a certain event occurs, and then switch to Page B. The INCR PAGE command switches 91S32 execution from one page of memory to the other.

12 REG, OUT Fields

The REG, OUT column heading designates the fields used to control operation of the two 8-bit, or one 16-bit, pattern generator registers. (Designating the pattern generator register as either two 8-bit registers or one 16-bit register is accomplished in the 91S16 Configuration sub-menu.) REG stands for register, and OUT is a reminder that the instructions in this field control when the contents of the register are output as pattern via the P6464 probes.

The REG key on the DAS keyboard corresponds to the REG instructions. REG instructions include LOAD R, INCR R (increment R), and DECR R (decrement R). If you configure the pattern generator register to be two 8-bit registers, you can select LOAD RA and LOAD RB, instead of LOAD R. If you don't program any REG instruction, the register will simply maintain its previous value.

The OUT key on the DAS keyboard corresponds to the OUT field and instructions. OUT instructions include OUT R (output the contents of register R as data), and OUT REP. OUT REP instructs the pattern generator to repeat whatever Pod A pattern it output on the previous sequence line. This could be a data value or a register value.

Program any REG or OUT instruction by pressing the corresponding instruction selection key. The instruction selected will be displayed under the REG, OUT field heading. Sometimes both REG and OUT instructions are programmed on the same line. If you want to program more than one REG or OUT instruction for a sequence line, you must press the ADD LINE key on the DAS keyboard. This will cause another REG, OUT field to appear. You can add up to two additional REG, OUT fields for each sequence line.

NOTE

When entering REG and OUT instructions, position the screen cursor on any reverse-video field associated with the sequence line you wish to program.

NOTE

Before attempting to use the LOAD command, carefully read the paragraph titled Load *for instructions on loading the register(s) from the data field later in this section.*

To enter a REG or OUT instruction on a sequence line:

1. Move the screen cursor to any field on the line where the instruction is to be programmed.
2. Press the REG or OUT key until the desired instruction appears in the field.

The DAS will display the REG instructions in this order:

[LOAD RA]
[INCR RA]
[DECR RA]
[LOAD RB]
[INCR RB]
[DECR RB]

OR

[LOAD R]
[INCR R]
[DECR R]

If you have configured the 91S16 internal register to be two 8-bit registers, only RA and RB instructions will be displayed; if you have configured the register to be one 16-bit register, only R instructions will be displayed.

The DAS will display the OUT instructions in this order:

[OUT RA]
[OUT RB]

OR

[OUT R]

AND

[OUT REP]

To return REG and OUT instructions to their default values:

1. Move the screen cursor to the REG, OUT field you wish to default.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[OUT RA]

2. Press the DON'T CARE key.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[ ]

To add an additional REG or OUT field:

1. Move the screen cursor to a field on the line where the additional REG or OUT instruction needs to be added.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[INCR RA]

2. Press the ADD LINE key on the DAS keyboard up to two times.

   The DAS will create an additional reverse-video REG, OUT field each time you press the ADD LINE key; note that this does not create additional sequence lines, just extensions to the existing sequence line.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[ ]
						[ ]	[INCR RA]

REG and OUT Instructions

Read this section carefully; REG and OUT instructions depend on the configuration of the 91S16 internal register; most operations affect the output of Pod A only. Do not assume that a REG or OUT instruction also affects the data supplied to Pod B unless the following paragraphs specifically state that Pod B is affected.

Each REG (register control) and OUT (output register contents as data) instruction has individual performance characteristics. These characteristics are dependent on how you have configured the 91S16's internal register in the 91S16 Configuration sub-menu.

NOTE

You must select the configuration for the 91S16 internal register in the 91S16 Configuration sub-menu. You may select either two 8-bit registers named RB and RA, or one 16-bit register named R. The default configuration is RB and RA.

Keep in mind the following rules when using REG and OUT instructions:

1. When the 91S16's internal register is configured as two 8-bit registers called RA and RB, the initial value loaded into either register is loaded from the Pod A data field; the Pod B data field is not used to load either register. (Two sequence lines are required to load both registers.)

   The most significant bit for each data register corresponds to the most significant bit of the Pod A data field.

   When data is output from either RA or RB, it is delivered to the Pod A pattern generator probe; the Pod B probe receives its pattern (as usual) from the Pod B data column in the Run sub-menu. When either RA or RB is output, the data value specified for Pod A is ignored.

2. When the 91S16's internal register is configured as a single 16-bit register called R, the initial value is loaded from both the Pod B and the Pod A data fields.

   When data is output from 16-bit register R, it is delivered to both Pod B and Pod A probes. The most significant bit of the register is delivered to the most significant data channel of the pattern generator probe attached to Pod B, while the least significant bit of the register is delivered to the least significant channel of Pod A.

   When register R is output, the data values for Pod B and Pod A are ignored for that sequence line.

3. If you have programmed a SEQ FLOW or OUT instruction on the same line as a REG instruction, the SEQ FLOW or OUT instruction will be performed first. For example, if you program IF R = 0 JUMP <*label*> instruction on the same line as a LOAD R instruction, the pattern generator will test to see if R = 0 before loading R with some new value. Both instructions will be executed, but the conditional test will use the old value for R.

LOAD Instructions

The LOAD register commands are used to load the register with some initial value. LOAD uses either RA, RB, or R as an operand. The register names displayed will depend on whether you have selected two 8-bit registers or one 16-bit register.

LOAD RA, LOAD RB. Initial values for either RA or RB are loaded from the Pod A data field in the sequence line containing the LOAD instruction.

To load RA, move the screen cursor to the Pod A data field and use the data entry keys to specify the value you want loaded into the register. Move the screen cursor to the REG, OUT field and press SELECT until LOAD RA appears on the screen. LOAD RB works exactly the same way.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 01	0	0	0	[ ]	[LOAD RA]

After executing sequence line 100, register RA will contain the value 00000001_{bin}.

LOAD R. The initial value of register R is loaded from the Pod B and Pod A data fields. The most significant bit of register R is taken from the most significant bit of Pod B, and the least significant bit of R is taken from the least significant bit of Pod A.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	01 03	0	0	0	[ ]	[LOAD R]

After executing sequence line 100, register R contains the value 0000000100000010_{bin}.

INCR (Increment Register) Instructions

The INCR (Increment Register) instructions are used to increase the count of the specified register by one. There are INCR RA, INCR RB, and INCR R versions of this command. The options displayed depend on whether you have configured the internal register to be two 8-bit registers named RA and RB, or one 16-bit register named R.

INCR RA, INCR RB. These commands increment the values of their respective registers by 1 each time the sequence line containing the instruction is executed. The range of the counters is between 0 and FF. The next INCR command following FF resets the register to 0; no carry signal is generated.

INCR R. This command increments the value of register R each time the sequence line containing the instruction is executed. The range for the counter is between 0 and FFFF. The next INCR command following FFFF resets the register to 0; no carry signal is generated.

Here is an example of an INCR R instruction programmed into a sequence line; data fields are not affected by this command.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[INCR R]

DECR (Decrement Register) Instructions

The DECR (Decrement Register) instructions are used to decrease the value of the specified register by one. There are DECR RA, DECR RB, and DECR R versions of this command. The options displayed depend on whether you have configured the internal register to be two 8-bit registers named RA and RB, or one 16-bit register named R.

DECR RA, DECR RB. These commands decrement the values of their respective registers by 1 each time the sequence line containing the instruction is executed. The range of the counters is between FF and 0. The next DECR command following 0 sets the register to FF; no borrow signal is generated.

DECR R. This command decrements the value of register R each time the sequence line containing the instruction is executed. The range for the counter is between FFFF and 0. The next DECR command following 0 sets the register to FFFF; no borrow signal is generated.

Here is an example of a DECR R instruction programmed into a sequence line; data fields are not affected by this command.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[DECR R]

OUT (Output Register Contents) Instructions

The OUT (Output Register Contents) instruction allows you to output the contents of the 91S16's internal register as data in place of the value programmed in that sequence line's data field. There are OUT RA, OUT RB, and OUT R versions of this instruction. The options displayed depend on whether you have configured the internal register to be two 8-bit registers named RA and RB, or one 16-bit register named R. OUT instructions do not change the value in a register.

NOTE

OUT RA and OUT RB both provide data to the pattern generator probe attached to Pod A; neither outputs data to Pod B. OUT R outputs data to both Pod B and Pod A.

OUT RA, OUT RB. The value in the specified register is sent as data to the pattern generator probe connected to Pod A. Both register RA and register RB send data to the same pattern generator probe. You cannot have OUT RA and OUT RB instructions on the same sequence line.

OUT R. The value in register R is sent as data to the pattern generator probes connected to both Pod B and Pod A. The most significant register bit is sent to the Pod B channel 7 data line and the least significant register bit is sent to the Pod A channel 0 data line.

Here is an example of the OUT R instruction programmed into a sequence line. The data values programmed into the 4B and 4A fields for this line will not be sent to the pattern generator probe tips; these data values will be ignored by the pattern generator. (Note: the contents of data Pod B would be output if the instruction were OUT RB or OUT RA.)

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
100	[ ]	00 00	0	0	0	[ ]	[OUT R]

NOTE

STEP and TRACE modes allow you to see the data output as each sequence line is executed and view the contents of the 91S16's internal register for that sequence line. Read the section of this addendum titled 91S16 Step and Trace Mode Sub-Menus *for instructions on using these operating modes.*

OUT REP (Out Repeat) Instruction

The OUT REP (Out Repeat) instruction causes the pattern generator to ignore its current data source for Pod A and repeat whatever vector it output for Pod A in the previous sequence line. It does not matter if the previous sequence line's vector originated as data, a register value, or even another OUT REP instruction.

NOTE

OUT REP only repeats the output of Pod A; it does not repeat the previous vector supplied to Pod B. If the previous data vector was a 16-bit value from register R, OUT REP will only repeat the 8 least significant bits (those originally supplied to Pod A); Pod B data will be supplied by the Pod B data field.

Here is an example of the OUT REP instruction programmed into a sequence line.
When sequence line 101 is executed, it will output AA via the probe attached to Pod A, and 00 via the probe attached to Pod B.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
99	[ ]	AA AA	0	0	0	[ ]	
100	[ ]	00 00	0	0	0	[ ]	[OUT REP]

13 EDIT Fields

The 91S16 Module provides nine edit commands to manipulate labels, patterns, and instructions on program lines. These commands are designed to simplify programming.

To select an edit command:

1. Move the screen cursor to the edit field at the bottom of the screen:
2. Press the SELECT key until the desired command appears in the field. You can also use the INCR and DECR keys to select from the edit commands.

   The DAS displays the list of possible edit commands in this alphabetical sequence:

```
[CONVERSION]
[  COPY    ]
[ DELETE   ]
[ DISPLAY  ]
[  FILL    ]
[  INSERT  ]
[ MODIFY   ]
[  MOVE    ]
[  SEARCH  ]
```

Each edit command has a specialized function. The CONVERSION command has a sub-menu used to make and check a conversion table. Several commands have sub-fields you will use to specify starting and ending sequence lines, or to select among additional sub-commands. Some of the commands have fields that require you to enter setup and editing parameters.

3. After entering the changes you wish to make for any of the edit operations, press the EXECUTE key. Some of the fields, such as those pertaining to sequence numbers, will be blanked after the edit operation has been completed. This is to prevent you from accidentally pressing EXECUTE again and damaging your corrected program.

   The following paragraphs briefly describe each of the edit commands.

CONVERSION. The CONVERSION command allows you to search for and replace all pattern data values with corresponding different values in one operation. For instance, if you knew you wanted to replace all FFs *hex* in your program with AAs, and replace all 1Es *hex* with 00s, you could use the CONVERSION command to do that in one operation.

This feature is most commonly used when you are converting data from one coding system to another, such as from a normal binary counting method to that of the Gray code where only one bit changes as numbers are incremented.

The CONVERSION command has two sub-commands: CONVERT, which designates which pod's data is to be converted, and TABLE BUILD. The TABLE BUILD command displays a special menu called the TABLE BUILD sub-menu that allows you to specify which bit patterns to change. Instructions for using this menu are included in the following paragraphs.

CONVERT. This sub-command instructs the pattern generator to apply the conversion rules outlined in the TABLE BUILD sub-menu to the data in a particular pod. The way in which the TABLE BUILD sub-menu performs conversions will become clear as you read this section. If you had a 91S16 in DAS slot 1 and you wanted to modify the data programmed for Pod B according to the changes given in the TABLE BUILD sub-menu, you would type:

[CONVERSION] : [CONVERT] POD [1B]

Press the EXECUTE key to initiate the conversion.

The TABLE BUILD sub-menu only operates on one pod of data at a time. Therefore, if you wanted to convert all data patterns for a 91S16 in DAS slot 1 from one code to another, you would have to CONVERT POD 1A, and then CONVERT POD 1B. If you are using 91S32s along with your 91S16, you would have to run the conversion program four more times for each 91S32 to convert all the data from one code to another. However, you will often be using the different pods for different purposes, and you may only want to convert one pod's data and leave the rest of the data unchanged.

To specify which pod's data will be converted:

1. Move the screen cursor to the POD field.
   [CONVERSION] : [CONVERT] POD [ ]
2. Use the data entry keys to enter a pod I.D. For example, pod 4B. The DAS will display the pod I.D. in the POD field.
   [CONVERSION] : [CONVERT] POD [4B]
3. Press the EXECUTE key to start the conversion. The DAS will display "CONVERTED POD 4B" on the second line of the screen when the conversion has been completed. The DAS will also blank the POD field to prevent accidental conversions later.

TABLE BUILD. Use the TABLE BUILD sub-menu to convert an existing data pattern into some modified data pattern. The menu provides two columns of 8-digit binary numbers from 00000000 to 11111111. Modifying the bit pattern in the CODE column and executing the CONVERT command on some pod's data will cause all instances of the pattern in the right-hand DATA field to be converted to the pattern in the CODE field.

For example, moving the screen cursor to 00000000 in the left-hand column, typing in 00000001, and then executing CONVERT POD 1A, will cause all instances of 00000000 stored as data in POD-1A to be changed to 00000001.

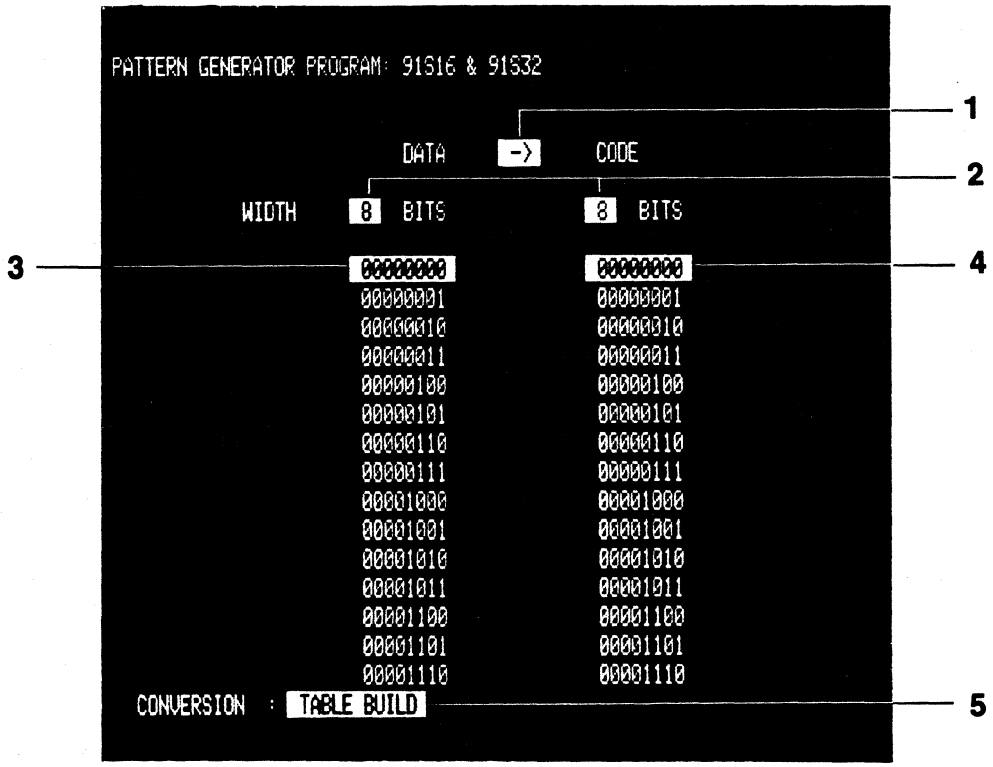
It may be useful for you to think of the bit-patterns in the left-hand column as sequence numbers. The bit-patterns in the left-hand DATA column represent all possible bit-patterns. Typing some pattern in a left-hand field is a way of moving your editing window from one bit-pattern to another; it will not change any data.

To invoke the TABLE BUILD sub-menu:

1. Move the screen cursor to the field containing CONVERT.

   [CONVERSION] : [CONVERT] POD [ ]

2. Press the SELECT key until TABLE BUILD appears in the field. The TABLE BUILD sub-menu will automatically appear on the screen.
   Refer to Figure 3-14.



5397-21

Figure 3-14. Table Build sub-menu.

1 → Field

The → field indicates the direction for converting data. If the arrow is pointing to the right, data in the right-hand column will replace the data pattern indicated in the left-hand column. If the arrow is pointing to the left, the pattern in the left-hand column will replace the pattern in the right hand column.

When the arrow is pointing to the right, you can enter the same bit pattern in the right column for any number of bit patterns in the left column. However, when the arrow is pointing to the left, each pattern in the left column must convert to a unique pattern in the right column.

As long as you are mapping a unique pattern in the right column to a unique pattern in the left column, this feature allows you to change the data pattern, and then change back easily if you don't like the results of your first conversion.

This field defaults with the arrow pointing to the right.

To change the direction of the conversion arrow:

1. Move the screen cursor to the arrow field.
   DATA [→] CODE
2. Press the SELECT key until the desired direction appears in the field.
   DATA [←] CODE

2 WIDTH Fields

Use the WIDTH fields to select the bit width of the data and code columns. For both columns, you can select bit widths ranging from 1 to 8 bits. The default field width is 4 bits for each column.

You will usually want to set both column widths to the same value. The bit width you select will determine the depth of the corresponding DATA and CODE fields. However, if you select a width of 4 bits for the DATA column and 5 bits for the CODE column, both selection fields will be 16 lines deep (16 possible patterns from 4 bits); the field depth always truncates to match the shorter column. Selecting 8-bit field widths for both columns will generate a TABLE BUILD sub-menu with 256 lines of bit patterns.

If you shorten the width CODE field after having entered some longer value into one of the fields, the display will change to show the shorter pattern, but the DAS will retain the longer value in memory until the DAS is turned off.

To enter the DATA and CODE fields column widths:

1. Move the screen cursor to the WIDTH field over the column you wish to change.

	DATA	CODE
WIDTH	[4] BITS	[4] BITS

2. Use the data entry keys to enter the desired column width. For example, 8.

	DATA	CODE
WIDTH	[8] BITS	[4] BITS

   Remember that no data conversion actually takes place until you EXECUTE the CONVERSION: CONVERT POD [##] command. Depending on how you configure your replacement

data patterns in the TABLE BUILD menu, it is possible that the CONVERT command will attempt to replace an 8-bit pattern with a smaller, say 4-bit, pattern. In this case, only the lowest 4 bits of the original pattern would be converted to the new pattern, and the data in the four most significant bits would not be changed. For example, if the original pattern was 11111111_{bin}, and the replacement pattern from the TABLE BUILD menu was 0000_{bin}, the resulting data would be 11110000_{bin}.

3 DATA Column

The DATA column automatically appears whenever the TABLE BUILD sub-menu is selected. The DATA column contains all possible bit patterns for data entered in the PROGRAM: Run sub-menu. Bit patterns in the DATA column represent existing data, while bit patterns in the CODE column represent planned changes to the data. (The only exception is when the direction field has the arrow pointing to the left.)

The depth of the DATA column is dependent on the value entered in the WIDTH field. Since all possible bit patterns for a particular width are shown, most TABLE BUILD sub-menus are too long to be displayed on one screen.

There are several ways of displaying different parts of the TABLE BUILD sub-menu. The first method is to use the scroll keys on the DAS keyboard.

To scroll through the DATA column sequences:

Press the ↑ or the ↓ key on the keyboard. The DAS will scroll the display up or down.

The second method used to display different DATA bit patterns is to enter the desired new pattern into a field within the DATA column. Just as in moving through sequence lines in the Program Run sub-menu, the DAS will display the DATA line you have entered and fill the rest of the page with DATA lines incrementing from that point.

To move forward to a larger block of DATA lines:

1. Move the screen cursor to the data field you wish to change. For example, line 1010.

DATA
00000101
00000110
00000111
00001000
00001001
[00001010]
00001011
00001100
00001101

2. Use the data entry keys to enter the first DATA line you wish to display. For example, 11001000.

```
   DATA
00000101
00000110
00000111
00001000
00001001
[11001000]  DATA pattern 00001010 is
 11001001    changed to 11001000 and
 11001010    the remaining DATA patterns
 11001011    increment from that line.
```

The DAS will display DATA line 11001000 in place of line 00001010, and then update the rest of the DATA lines following that position.

NOTE

Entering a value in one of the DATA column fields is a method of displaying different portions of this sub-menu; it will not change the data programmed for a pod in the Run sub-menu.

To display a block of DATA patterns with smaller values:

1. Move the screen cursor to the first DATA line displayed in the TABLE BUILD menu.
2. Use the data entry keys to enter the bit pattern you want to display. The display will fill with data lines starting with the pattern you have entered.

NOTE

Values in the DATA column are displayed in ascending order. If you wish to display a value smaller than any currently displayed, you must enter the new value in the topmost DATA column field.

4 CODE Column

Use the CODE column fields to enter the pattern you want to end up with after the conversion. Bit patterns in the CODE field will replace the bit patterns in the DATA field immediately to their left. More than one data pattern may be converted to the same CODE pattern. To do this, enter the same CODE pattern next to two or more DATA patterns.

To enter a pattern into the CODE field:

1. Move the screen cursor to the desired CODE field:

```
    DATA          CODE
[00000000]    [00000000]
```

2. Use the data entry keys to enter the desired pattern. The DAS will display the value you enter in the CODE field:

```
    DATA          CODE
[00000000]    [00001111]
```

3. Repeat this procedure for each line until all the desired patterns are entered in the CODE fields to the right of the existing patterns.

NOTE

If more than one DATA pattern is converted to the same CODE pattern, the conversion of DATA to CODE can not be reversed by switching the ~ field to ~.

5 CONVERSION Field

Use the CONVERSION field to exit the TABLE BUILD sub-menu.

To exit the TABLE BUILD sub-menu:

1. Move the screen cursor to the CONVERSION field:

   [CONVERSION] : [TABLE BUILD]

2. Press the SELECT key. The DAS will display the 91S16 Program Run sub-menu.

   [CONVERSION] : [CONVERT] POD [ ]

COPY Use the COPY command to duplicate sequence lines programmend in the 91S16 Run sub-menu, or to copy the data programmed for one pod to another. The command has a field that allows you to select either SEQ (sequences within the Run sub-menu) or POD (copy one pod's data to another pod).

To change the COPY command mode between SEQ and POD:

1. Move the screen cursor to the field next to COPY:

   [COPY] : [SEQ] [ ] THROUGH [ ] BEFORE SEQ [ ]

2. Press the SELECT key until the desired mode appears in the field.

   [COPY] : [POD] [ ] TO [ ]

SEQ Use the SEQ sub-command to duplicate sequence lines of program within the 91S16 Run sub-menu. When the COPY SEQ command is executed, all sequence lines specified are duplicated and placed immediately before the given destination. The sequence numbers for the menu are then updated; labels are retained in the duplicated lines.

NOTE

Using the COPY command when all 1024 sequence lines have been programmed may cause some high-numbered sequence lines to be lost from memory. (Only 1023 sequence lines are available when IRQ CALL is enabled.) The number of sequence lines lost will correspond to the number of new lines inserted. If you must add new sequence lines to a lengthy pattern, use the DELETE command first to remove unnecessary lines and make room for the additions.

To copy sequence lines:

1. Move the screen cursor to the SEQ/THROUGH fields.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0		FF FF	0	0	0		LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP END	
2		02 00	0	0	0	JUMP LOOP	DECR R
3		03 00	0	0	0		OUT R
4	END	04 00	0	0	0		OUT R
5		05 00	0	0	0		
6		06 00	0	0	0		
7		07 00	0	0	0		
8		08 00	0	0	0		
9		09 00	0	0	0		

[COPY] : SEQ [ ] THROUGH [ ] BEFORE SEQ [ ]

2. Use the data entry keys to enter the starting and ending sequences as well as a destination sequence. For example, to make a copy of sequence lines 0 through 4 and to place them before sequence line 5:

[COPY] : SEQ [0] THROUGH [4] BEFORE SEQ [5]

3. Press the EXECUTE key to initiate the COPY SEQ command.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0		FF FF	0	0	0		LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP END	
2		02 00	0	0	0	JUMP LOOP	DECR R
3		03 00	0	0	0		OUT R
4	END	04 00	0	0	0		OUT R
5		FF FF	0	0	0		LOAD R
6	LOOP	01 00	0	0	0	IF R=0 JUMP END	
7		02 00	0	0	0	JUMP LOOP	DECR R
8		03 00	0	0	0		OUT R
9	END	04 00	0	0	0		OUT R
10		05 00	0	0	0		
11		06 00	0	0	0		
12		07 00	0	0	0		
13		08 00	0	0	0		
14		09 00	0	0	0		

[COPY] : SEQ [ ] THROUGH [ ] BEFORE SEQ [ ]

The DAS will display the message "COPIED SEQ 0 THROUGH 4 BEFORE SEQ 5" in the message field at the top of the display when the operation is complete. The DAS will also blank the SEQ and THROUGH fields to prevent accidental operation.

NOTE

When sequence lines with labels are copied, these labels are duplicated in the new lines. Before you start the pattern generator, or exit the Pattern Generator menus, you must remove these duplicate labels.

POD Use the POD sub-command to duplicate a pattern entered into memory for one pod and put a copy of the same pattern into memory for another pod. If there is already data in the destination pod, it will be discarded when the new pattern is copied into that pod's memory.

To copy a data pattern from one pod to another:

1. Move the screen cursor to the COPY: POD field.

```
 SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

   0           FF FF   0   0   0                       LOAD R
   1   LOOP    01 00   0   0   0   IF R=0 JUMP   END
   2           02 00   0   0   0    JUMP         LOOP  DECR R
   3           03 00   0   0   0                       OUT R
   4   END     04 00   0   0   0                       OUT R
   5           05 00   0   0   0
   6           06 00   0   0   0
   7           07 00   0   0   0
   8           08 00   0   0   0
   9           09 00   0   0   0

[ COPY ] : POD   [  ] TO [  ]
```

2. Use the data entry keys to enter a pod I.D. For example, to make a copy of POD 4B and send it to POD 4A:

```
[ COPY ] : POD   [4B] TO [4A]
```

3. Press the EXECUTE key to start the COPY POD operation.

   The DAS will display the message "COPIED POD 4B to 4A" in the message field on the second line of the display when the COPY POD operation has been completed. The DAS will also blank the source and destination fields to prevent accidental operation.

```
 SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

   0           FF FF   0   0   0                       LOAD R
   1   LOOP    01 01   0   0   0   IF R=0 JUMP   END
   2           02 02   0   0   0    JUMP         LOOP  DECR R
   3           03 03   0   0   0                       OUT R
   4   END     04 04   0   0   0                       OUT R
   5           05 05   0   0   0
   6           06 06   0   0   0
   7           07 07   0   0   0
   8           08 08   0   0   0
   9           09 09   0   0   0

[ COPY ] : POD   [  ] TO [  ]
```

DELETE Use the DELETE command to erase sequence lines within the Program Run sub-menu. When the DELETE command is executed, all sequence lines between the given starting and ending sequence lines (inclusive) are deleted. The remaining sequence line numbers are automatically updated.

NOTE

When sequence lines are removed by the DELETE command, a corresponding number of new sequence lines containing default values are created at the end of the pattern generator's memory. These new sequence lines will be inserted after the last sequence line that contains programming data in order to maintain a total of 1023 sequence lines (IRQ CALL enabled) or 1024 lines (IRQ CALL disabled).

To delete one or more sequence lines:

1. Move the screen cursor to the edit command field at the bottom of the Run sub-menu screen. Press the SELECT key until DELETE appears in the field.
2. Move the screen cursor to the SEQ field.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0		FF FF	0	0	0		LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP END	
2		02 00	0	0	0	JUMP LOOP	DECR R
3		03 00	0	0	0		OUT R
4	END	04 00	0	0	0		OUT R
5		05 00	0	0	0		
6		06 00	0	0	0		
7		07 00	0	0	0		
8		08 00	0	0	0		
9		09 00	0	0	0		

[DELETE] : SEQ [ ] THROUGH [ ]

3. Use the data entry keys to enter the sequence numbers of the first and last lines you wish to delete. If you only wish to delete one line, enter that sequence number in both fields.

[DELETE] : SEQ [3] THROUGH [5]

4. Press the EXECUTE key to start the DELETE operation. The DAS will display the message "DELETED SEQ 3 THROUGH 5" when the DELETE operation has been completed. The DAS will also update the remaining sequence line numbers, and blank the SEQ and THROUGH fields to prevent accidental operation.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0		FF FF	0	0	0		LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP END	
2		02 00	0	0	0	JUMP LOOP	DECR R
3		06 00	0	0	0		
4		07 00	0	0	0		
5		08 00	0	0	0		
6		09 00	0	0	0		
7		10 00	0	0	0		
8		11 00	0	0	0		
9		12 00	0	0	0		

[DELETE] : SEQ [ ] THROUGH [ ]

DISPLAY Use the DISPLAY command to select the display radix for the pod data, S (Strobe), I (Internal Inhibit), and M (Interrupt Mask) fields. This command makes it easier for you to read the values programmed into these fields, or to remove them from the display if they are not being used.

To remove or change the radix of the pod data, S, I, and M, fields:

1. Move the screen cursor to the edit command field and press select until DISPLAY appears.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL		REG, OUT
0		FF FF	0	0	0			LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP	END	
2		02 00	0	0	0	JUMP	LOOP	DECR R
3		03 00	0	0	0			OUT R
4	END	04 00	0	0	0			OUT R
5		05 00	0	0	0			
6		06 00	0	0	0			
7		07 00	0	0	0			
8		08 00	0	0	0			
9		09 00	0	0	0			

[DISPLAY] : 4B [HEX] 4A [HEX] S [HEX] I [HEX] M [HEX]

2. Move the screen cursor to the DISPLAY command field you want to change and press the SELECT key to change the radix or to turn off the field. For example, to change the radix for the S and I fields to BIN (binary), and to turn off the M field:

   [DISPLAY] : 4B [HEX] 4A [HEX] S [BIN] I [BIN] M [OFF]

   The DAS will then change the display of the S, I, and M fields as follows:

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL		REG, OUT
0		FF FF	00	00				LOAD R
1	LOOP	01 00	00	00		IF R=0 JUMP	END	
2		02 00	00	00		JUMP	LOOP	DECR R
3		03 00	00	00				OUT R
4	END	04 00	00	00				OUT R
5		05 00	00	00				
6		06 00	00	00				
7		07 00	00	00				
8		08 00	00	00				
9		09 00	00	00				

[DISPLAY] : 4B [HEX] 4A [HEX] S [BIN] I [BIN] M [OFF]

FILL Use the FILL command to automatically fill in the values of the #B (POD-B data), #A (POD-A data), S (Strobe), I (Internal Inhibit), and M (Interrupt Mask) fields with some constant values. For instance, if you knew you wanted all the sequence lines from line 20 through line 30 to have the same data value for POD-A, you could use the FILL command to automatically enter that value in each data field instead of having to enter the value for each line individually.

You might use this command to change all the default values in the S (Strobe) field from 0s to 1s, or you might want to protect a block of sequence lines from external interrupts by programming a 1 into the M (Interrupt Mask) field for each line.

The FILL command displays its own fields which are used to modify each of the Run sub-menu's data, S, I, and M columns simultaneously. You can use this command to modify all of the columns in a single operation, or you can choose to modify just one or two columns at a time. Entering a DON'T CARE (X) into a FILL command field means that column's data will not be affected by the editing operation. For example, entering a DON'T CARE into the FILL command's S field means that values entered into the Run sub-menu's strobe column will not be affected by a FILL operation.

To use the FILL command:

1. Select the FILL command by pressing the SELECT key while the cursor is in the edit command field at the bottom of the DAS display.
2. Move the screen cursor to the SEQ field:

```
 SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

   0           FF FF   0   0   0                       LOAD R
   1   LOOP    01 00   0   0   0   IF R=0 JUMP   END
   2           02 00   0   0   0    JUMP        LOOP  DECR R
   3           03 00   0   0   0                       OUT R
   4   END     04 00   0   0   0                       OUT R
   5           05 00   0   0   0
   6           06 00   0   0   0
   7           07 00   0   0   0
   8           08 00   0   0   0
   9           09 00   0   0   0

[  FILL   ] : SEQ [     ] THROUGH [     ]
       ----   [XX XX] [X] [X] [X] ----------       --------
```

3. Use the data entry keys to enter the starting and ending sequence numbers. Then move the cursor to the appropriate field and enter the pattern you wish to place in all the corresponding fields within that sequence range. For example, to fill SEQ lines 1 through 4 with "XX AA X 0 1":

```
[  FILL   ] : SEQ [    1] THROUGH [    4]
       ----   [XX AA] [X] [0] [1] ----------       --------
```

4. Press the EXECUTE key to start the FILL operation. The DAS will display the message "FILLED SEQ 1 THROUGH 4" on the second line of the display when the FILL operation has been completed. The DAS will also blank the SEQ and THROUGH fields, but not the pattern fields.

```
 SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

   0           FF FF   0   0   0                       LOAD R
   1   LOOP    01 AA   0   0   1   IF R=0 JUMP   END
   2           02 AA   0   0   1    JUMP        LOOP  DECR R
   3           03 AA   0   0   1                       OUT R
   4   END     04 AA   0   0   1                       OUT R
   5           05 00   0   0   0
   6           06 00   0   0   0
   7           07 00   0   0   0
   8           08 00   0   0   0
   9           09 00   0   0   0

[  FILL   ] : SEQ [     ] THROUGH [     ]
       ----   [XX AA] [X] [0] [1] ----------       --------
```

INSERT Use the INSERT command to insert additional sequence lines into the Program Run sub-menu. The number of additional lines specified in the LINE(S) field are inserted just before the destination sequence line. The SEQ numbers for all the sequence lines are then updated. Newly inserted sequence lines always contain default values.

NOTE

If you are adding sequence lines to a program already containing 1023 lines (IRQ CALL enabled) or 1024 lines (IRQ CALL disabled), you will force the last lines in your program out of memory. The number of lines lost will correspond to the number of new lines inserted. If you must add new sequence lines to a lengthy pattern, use the DELETE command first to remove unnecessary lines and make room for the new lines.

To insert sequence lines:

1. Select the INSERT command by pressing the SELECT key while the cursor is in the edit command field at the bottom of the Program Run sub-menu.
2. Move the screen cursor to the LINE(S) field.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0		FF FF	0	0	0		LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP END	
2		02 00	0	0	0	JUMP LOOP	DECR R
3		03 00	0	0	0		OUT R
4	END	04 00	0	0	0		OUT R
5		05 00	0	0	0		
6		06 00	0	0	0		
7		07 00	0	0	0		
8		08 00	0	0	0		
9		09 00	0	0	0		

[INSERT] : [ ] LINE(S) BEFORE SEQ [ ]

3. Use the data entry keys to specify the number of lines you wish to add, and the sequence line where they are to be inserted. For example, to insert 3 lines before SEQ 2:

[INSERT] : [3] LINE(S) BEFORE SEQ [2]

3. Press the EXECUTE key to start the INSERT operation. The DAS will display the message "INSERTED 3 LINE(S) BEFORE SEQ 2" in the message field when the insert operation has been completed. The DAS will also update the remaining sequence numbers, and blank the LINE(S) and SEQ fields to prevent accidental insertions.

SEQ	LABEL	4B 4A	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0		FF FF	0	0	0		LOAD R
1	LOOP	01 00	0	0	0	IF R=0 JUMP END	
2		00 00	0	0	0		
3		00 00	0	0	0		
4		00 00	0	0	0		
5		02 00	0	0	0	JUMP LOOP	DECR R
6		03 00	0	0	0		OUT R
7	END	04 00	0	0	0		OUT R
8		05 00	0	0	0		
9		06 00	0	0	0		
10		07 00	0	0	0		
11		08 00	0	0	0		
12		09 00	0	0	0		

[INSERT] : [ ] LINE(S) BEFORE SEQ [ ]

MODIFY The MODIFY command uses logical operators to manipulate data already entered into the Program Run sub-menu. Three logical operators are available: AND, OR, and XOR (exclusive OR). Any programmable numeric column in the Run sub-menu can be modified by using these operators. For instance, you can modify one or both of the data fields, and the S (strobe), I (internal inhibit), and M (interrupt mask) fields, or any combination of the above. You can also limit the modification to a range of sequence numbers.

By ANDing a particular column with 0, you can modify all the data in that column to 0s. (Any number ANDed with 0 equals 0.) By ORing a column with a 1, you can set all the bits in that column to 1. (Any number ORed with a 1 equals 1.) By XORing any pattern with a 1, the bit pattern in that field is inverted. (In other words, all FFs $_{hex}$ would be changed to 00s, and all 11s $_{hex}$ become EEs.)

Here are reminder truth tables for the AND, OR, and XOR operations:

A AND B

A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

A OR B

A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

A XOR B

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

To MODIFY a column's data:

1. When the screen cursor is in the edit command field, press the SELECT key until the MODIFY command is displayed.

2. Move the screen cursor to the field immediately to the right of MODIFY and press the SELECT key until the desired logical operator is displayed. Logical operators are displayed in this order: AND, OR, XOR.

```
 SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

   0           FF FF   0   0   0                       LOAD R
   1   LOOP    01 00   0   0   0   IF R=0 JUMP   END
   2           02 00   0   0   0    JUMP         LOOP  DECR R
   3           03 00   0   0   0                       OUT R
   4   END     04 00   0   0   0                       OUT R
   5           05 00   0   0   0
   6           06 00   0   0   0
   7           07 00   0   0   0
   8           08 00   0   0   0
   9           09 00   0   0   0
[ MODIFY ] : LOGICAL [AND] SEQ [     ] THROUGH [     ]
      ----    [XX XX] [X] [X] [X] ---------- ---- ----------
```

3. Move the screen cursor to the SEQ and THROUGH fields. Use the data enty keys to enter the number of the first and last sequence line you want to modify. For example, to modify sequence lines 1 through 9, enter:

```
[ MODIFY ] : LOGICAL [XOR] SEQ [    1] THROUGH [    9]
      ----    [XX XX] [X] [X] [X] ---------- ---- ----------
```

4. Move the screen cursor down to the pattern line and enter the pattern you wish to use as a modifier. For example, to invert all the column B data pattern, select XOR as the logical operator and enter FF*hex* in the column B field. (Fields containing X are not affected by the MODIFY command.)

```
[ MODIFY ] : LOGICAL [XOR] SEQ [    1] THROUGH [    9]
      ----    [FF XX] [X] [X] [X] ---------- ---- ----------
```

5. Press the EXECUTE key to start the MODIFY operation. The DAS will display the message "MODIFIED SEQ 1 THROUGH 9" in the message field at the top left-hand corner of the display. The DAS will also blank the SEQ and THROUGH fields to prevent accidental operation.

```
 SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

   0           FF FF   0   0   0                       LOAD R
   1   LOOP    FE 00   0   0   0   IF R=0 JUMP   END
   2           FD 00   0   0   0    JUMP         LOOP  DECR R
   3           FC 00   0   0   0                       OUT R
   4   END     FB 00   0   0   0                       OUT R
   5           FA 00   0   0   0
   6           F9 00   0   0   0
   7           F8 00   0   0   0
   8           F7 00   0   0   0
   9           F6 00   0   0   0
```

```
[ MODIFY ] : LOGICAL [XOR] SEQ [     ] THROUGH [     ]
       ----   [FF XX] [X] [X] [X] ---------- ---- ----------
```

MOVE Use the MOVE command to move a block of sequence lines within a program to another location within that same program. When MOVE is executed, all the specified sequence lines are moved to a location just before the given destination sequence line. The sequence numbers are then automatically updated. Labels, data, and instructions are retained when sequence lines are moved.

Using the MOVE command will not destroy high-numbered program lines even if all 1024 lines have been programmed.

To MOVE a block of sequence lines from one location to another:

1. Select the MOVE command by pressing the SELECT key when the screen cursor is in the edit command field at the bottom of the 91S16 Program Run sub-menu.
2. Move the screen cursor to the SEQ field.

```
SEQ   LABEL   4B 4A   S  I  M   SEQ FLOW, CONTROL   REG, OUT
  0           FF FF   0  0  0                       LOAD R
  1   LOOP    01 00   0  0  0   IF R=0 JUMP   END
  2           02 00   0  0  0    JUMP         LOOP  DECR R
  3           03 00   0  0  0                       OUT R
  4   END     04 00   0  0  0                       OUT R
  5           05 00   0  0  0
  6           06 00   0  0  0
  7           07 00   0  0  0
  8           08 00   0  0  0
  9           09 00   0  0  0

[  MOVE  ] : [SEQ] [     ] THROUGH [     ] BEFORE SEQ [     ]
```

3. Use the data entry keys to enter the starting, ending, and destination sequence numbers. For example, to move sequence lines 1 through 3 and place them before sequence line 7:

```
[  MOVE  ] : [SEQ] [    1] THROUGH [    2] BEFORE SEQ [    7]
```

4. Press the EXECUTE key to start the MOVE operation. The DAS will display the message "MOVED SEQ 1 THROUGH 2 BEFORE SEQ 7" on the message line. The DAS will also update all the sequence lines and blank the SEQ, THROUGH, and BEFORE fields to prevent accidental move operations.

```
SEQ   LABEL   4B 4A   S  I  M   SEQ FLOW, CONTROL   REG, OUT
  0           FF FF   0  0  0                       LOAD R
  1           03 00   0  0  0                       OUT R
  2   END     04 00   0  0  0                       OUT R
  3           05 00   0  0  0
  4           06 00   0  0  0
  5   LOOP    01 00   0  0  0   IF R=0 JUMP   END
  6           02 00   0  0  0    JUMP         LOOP  DECR R
  7           07 00   0  0  0
  8           08 00   0  0  0
  9           09 00   0  0  0

[  MOVE  ] : [SEQ] [     ] THROUGH [     ] BEFORE SEQ [     ]
```

SEARCH Use the SEARCH command to locate some specific entry within the body of the Program Run sub-menu. The entry may be a label, a particular data pattern, or an instruction.

The SEARCH command allows you to specify the type of entry you are going to search for, and to specify a sequence range for the search. When executed, the SEARCH command compares all entries of the same type against the target string within the range of sequence lines you have specified. It will then place the screen cursor on the first sequence line containing that string, and display the total number of lines within the specified range that contain the target string. (The line total appears in the bottom right-hand corner of the display.)

The data entry keys can be used to select the second, or third, etc. sequence line containing the target string when the screen cursor is in the [ ] / # : SEARCHED field. (Instructions for using this field are included in the following paragraphs.)

To use the SEARCH command:

1. Select the SEARCH command by moving the screen cursor to the edit command field at the bottom of the Program Run sub-menu and pressing the SELECT key.
2. Select the type of pattern you are going to search for by moving the screen cursor to the field immediately to the right of the SEARCH: command.

```
[ SEARCH ] : [ LABEL   ] SEQ [      ] THROUGH [      ]
      [      ] -- --  -  -  -  ----------          --------
```

3. Press the SELECT key until the desired target group appears in the field.

   The DAS will display the target groups in this order:

```
[  LABEL    ]
[ PATTERN   ]
[SEQ FLOW   ]
[JUMP LABEL]
[ CONTROL   ]
[  REG      ]
[  OUT      ]
```

To SEARCH for a data pattern:

1. Move the screen cursor to the field immediately to the right of SEARCH:

```
 SEQ    LABEL    4B 4A    S    I    M    SEQ FLOW, CONTROL    REG, OUT

   0             FF FF    0    0    0                         LOAD R
   1    LOOP     01 00    0    0    0    IF R=0 JUMP    END
   2             02 00    0    0    0     JUMP          LOOP  DECR R
   3             03 00    0    0    0                         OUT R
   4    END      04 00    0    0    0                         OUT R
   5             05 00    0    0    0
   6             06 00    0    0    0
   7             07 00    0    0    0
   8             08 00    0    0    0
   9             09 00    0    0    0

[ SEARCH ] : [LABEL    ] SEQ [      ] THROUGH [      ]
      [      ] -- --  -  -  -  ----------          --------
```

2. Press the SELECT key until the target group PATTERN appears in the field.

```
[ SEARCH ] : [PATTERN ] SEQ [      ] THROUGH [      ]
      ----- [XX XX]  [X]  [X]  [X] ----------          --------
```

3. Move the screen cursor to the SEQ and THROUGH fields and enter the starting and ending sequence numbers for the block of program you wish to search. For example, enter SEQ 0 THROUGH 10 to search for a pattern programmed in lines 0 through 10 inclusive. Note: The larger the search range you specify, the longer it takes for the edit operation to be completed. This also increases the likelihood you will locate data you are not interested in.

4. Move the screen cursor to the PATTERN sub-fields and use the data entry keys to enter the pattern you wish to search for. For example, enter:

```
[ SEARCH ] : [PATTERN ] SEQ [   0 ] THROUGH [   10]
      ----- [10 00]  [X]  [X]  [X] ----------          --------
```

   DON'T CAREs (X's) will match any pattern.

5. Press the EXECUTE key to start the SEARCH operation. The DAS will display the message, "<[1] / 1 : SEARCHED>" in the bottom right-hand corner of the display. The first number in this message indicates that the screen cursor has been placed on the line containing the first occurrence of the target pattern. The number following the slash tells you how many lines contain the target pattern within the range you specified for the search.

   For example, if you had searched for 00 in a block of text where 15 lines contained the pattern 00, the message would read, "<[1]/ 15 : SEARCHED>". To see the 14th occurrence of the target pattern, you would move the screen cursor to the highlighted field in the first part of this message and type in 14. When you press the EXECUTE key, the screen cursor will be placed on the line containing the 14th occurrence of the target pattern, and the message field will read, "<[14] / 15 : SEARCHED>".

To SEARCH for an instruction:

1. To SEARCH for an instruction (for example: R OUT) move the screen cursor to the field immediately to the right of SEARCH: and press the SELECT key until the appropriate instruction type appears in the field. In the case of R OUT, we want the OUT (output register) instruction type to be displayed in this field.

```
[ SEARCH ] : [  OUT   ] SEQ [      ] THROUGH [      ]
      ------ -- --  -  -  -  ----------          [OUT R]
```

2. Move the screen cursor to the SEQ and THROUGH fields and use the data entry keys to enter the starting and ending sequence line numbers for the block of program you wish to search. For example, to search for some target pattern between sequence lines 3 and 10, enter SEQ 3 THROUGH 10.

3. Move the screen cursor to the OUT sub-field in the lower right-hand corner of the display. Press the SELECT key until the desired OUT instruction appears in the field. Note that in this case [OUT R] appears as the default choice. If you had configured the 91S16 register to be two 8-bit registers, you would have to move the screen cursor to this field and press the SELECT key until the desired instruction appeared. (OUT RA and OUT RB would be the choices in this case.)

```
[ SEARCH ] : [  OUT   ] SEQ [   3] THROUGH [   10]
      ----   -- --  -  -  -  ----------          [OUT R]
```

4. Press the EXECUTE key to start the SEARCH operation. The DAS will display the message "<[1]/ 2 : SEARCHED>" on the last line of the display to indicate that the SEARCH operation has been completed. The DAS will also blank the SEQ and THROUGH fields, and position the screen cursor on the first sequence line containing the target pattern.

```
SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

  0           FF FF   0   0   0                       LOAD R
  1   LOOP    01 00   0   0   0   IF R=0 JUMP   END
  2           02 00   0   0   0    JUMP        LOOP   DECR R
  3           03 00   0   0   0                       OUT R
  4   END     04 00   0   0   0                       OUT R
  5           05 00   0   0   0
  6           06 00   0   0   0
  7           07 00   0   0   0
  8           08 00   0   0   0
  9           09 00   0   0   0

[ SEARCH ] : [OUT      ] SEQ [   3] THROUGH [  10]
      ----   -- --  -  -  -  ----------          [OUT R]
```

NOTE

In the above display sample, the range specified for the SEARCH operation was from SEQ 3 through SEQ 10. That is why the first OUT R instruction found was on line 3, rather than on line 2.

5. Use the data entry keys to enter a value in the "<[1]/ 2 : SEARCHED>" message field if you wish to see a different sequence line containing the target pattern. For instance, if you wanted to see the second sequence line containing OUT R, you would move the screen cursor to the inverse-video field within the message and type a 2:

   <[2]/ 2 : SEARCHED>

   When you push the EXECUTE key the DAS will display:

```
SEQ   LABEL   4B 4A   S   I   M   SEQ FLOW, CONTROL   REG, OUT

  0           FF FF   0   0   0                       LOAD R
  1   LOOP    01 00   0   0   0   IF R=0 JUMP   END
  2           02 00   0   0   0    JUMP        LOOP   DECR R
  3           03 00   0   0   0                       OUT R
  4   END     04 00   0   0   0                       OUT R
  5           05 00   0   0   0
  6           06 00   0   0   0
  7           07 00   0   0   0
  8           08 00   0   0   0
  9           09 00   0   0   0

[ SEARCH ] : [OUT      ] SEQ [   3] THROUGH [  10]
      ----   -- --  -  -  -  ----------          [OUT R]
```

   The message would then display, "<[2]/ 2 : SEARCHED>". Of course, this feature is more dramatic when the sequence lines containing the target pattern are farther apart.

91S32 PROGRAM: RUN MODE SUB-MENU FIELDS AND VALUES

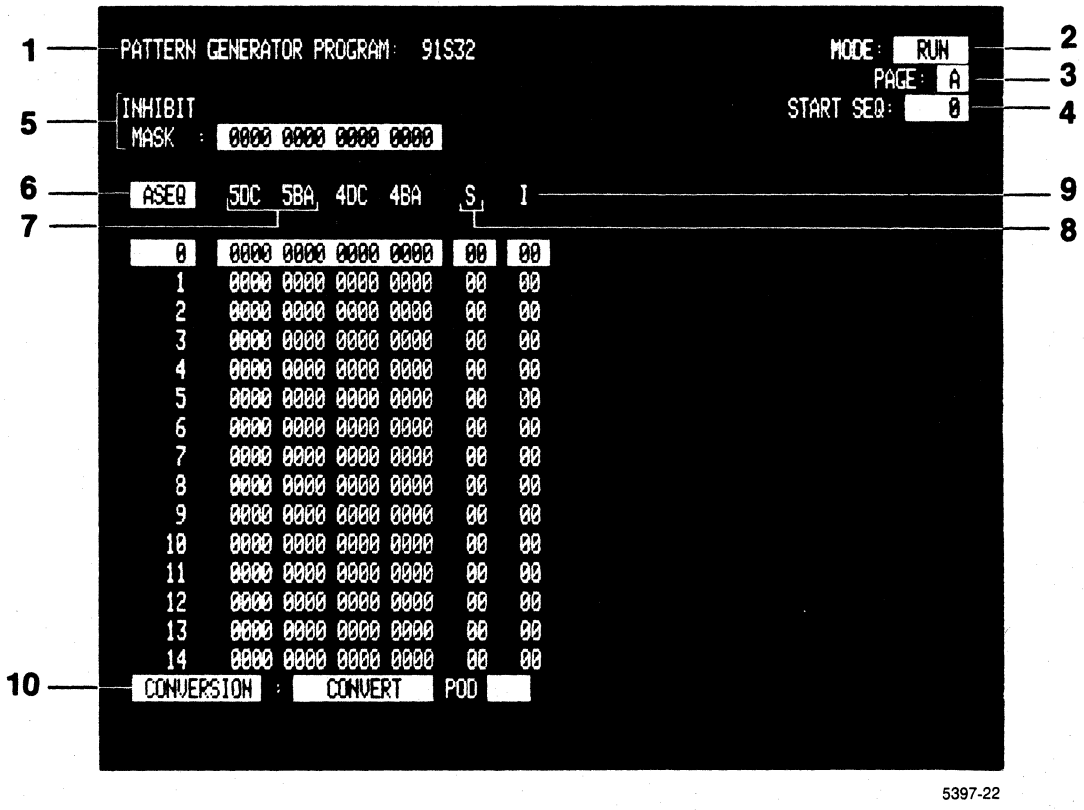
NOTE

The 91S32 Program Run Mode sub-menu appears only when the 91S32 Module is installed.

The following paragraphs describe how to use the 91S32 Program Run Mode sub-menu to enter patterns for the 91S32 Pattern Generator Module. They discuss each sub-menu field and list all optional values.

Figure 3-15 illustrates the 91S32 Pattern Generator Run Mode sub-menu and its fields. The fields, which appear in reverse video on the screen, are bracketed [ ] throughout the text. The four directional cursor keys and the NEXT key can be used to move the blinking screen cursor from one field to another.

Refer to the numbered callouts in Figure 3-15 when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.



5397-22

Figure 3-15. 91S32 Program: Run sub-menu.

NOTE

In the following discussion, the three 91S32 Modules are assumed to reside in DAS slots 3, 4, and 5.

1 PATTERN GENERATOR PROGRAM Field

Use this field (directly to the right of the menu title) to select either the 91S16 or the 91S32 sub-menu display. Refer to the description of the Sub-Menu Selections in the *Menu Overview* section of this addendum. If the 91S16 Module is installed, the 91S16 sub-menu is displayed as the default sub-menu. Otherwise, the 91S32 sub-menu is displayed.

To change the display to show the 91S32 sub-menu:

1. Move the screen cursor to the field directly to the right of the menu title.
   PATTERN GENERATOR PROGRAM: [91S16]
2. Press the SELECT key until 91S32 appears in the field.

   The DAS displays the sub-menu titles in this order:

   [91S16]
   [91S32]

2 MODE Field

Use the MODE field to select the Pattern Generator's operating mode.

The pattern generator normally outputs data in real-time fashion synchronously with the clock signal. This is called Run mode, hence the name of this sub-menu. The pattern generator can also output data at much slower rates, or even one step at a time, for debugging purposes. These modes of operation are called Trace and Step modes, and are described in the *Trace Mode and Step Mode* section of this manual.

Press the SELECT key when the screen cursor is in the MODE field to change between Run, Trace, and Step modes. The MODE field defaults to Run mode on power-up.

3 PAGE Field

The 91S16 sequential pattern generator can act as a controller for one or more 91S32s. However, the 91S16 has only 1024 lines of pattern memory, compared to the 91S32 which has 2048 lines of pattern memory. You can divide the 91S32's memory into two 1024-line pages and use the 91S16 INCR PAGE command to switch between the two pages. This approach has several programming advantages which are explained under the SEQUENTIAL and FOLLOWS modes descriptions in the *91S32 Configuration Menu* section. The PAGE field indicates which PAGE of memory (A or B) is being displayed.

Note that there are two possible sequence numbering schemes for the 91S32. The SEQ field has two possible values: ASEQ and RSEQ. Instructions for changing between these values are given later in this section, but the numbering scheme selected affects the PAGE field. When ASEQ (Absolute Sequence) is selected, the 91S32's program lines are numbered from 0 through 2047; page B will start with sequence 1024. RSEQ stands for Relative Sequence (relative to page A or page B). When RSEQ is selected, the 91S32's program lines are numbered from 0 through 1023 for page A, and from 0 through 1023 for page B. Use the numbering scheme that is most convenient to you.

If you are using the 91S32 with its memory divided into two pages, you can select which page of data appears on the display. The default value for the PAGE field is A.

To display the other memory page:

1. Move the screen cursor to the PAGE field.

   PAGE: [A]

2. Press the SELECT, INCR, or DECR key until the desired value appears in this field. For example, select page B:

   [B]

4 START SEQ Field

Use the START SEQ field to designate the first sequence line the pattern generator will execute when you press the START PAT GEN key or the START SYSTEM key.

If the 91S32 is being used without a 91S16, or if the 91S32 is being used with a 91S16 in the SEQUENTIAL mode, the number you enter in the START SEQ field will determine the first sequence line executed. If the 91S32 is being used with a 91S16 in the FOLLOWS mode, you cannot set a value in this field, since the starting sequence will be set by the 91S16. For an explanation of SEQUENTIAL and FOLLOWS modes, see the *91S32 Configuration Menu* section of this manual.

The START SEQ number you enter will depend on how you have configured your SEQ field: either ASEQ (absolute sequence numbers) or RSEQ (relative sequence numbers). If the sequence number field is set to ASEQ, you can enter a START SEQ value between 0 and 2047. (IRQ enabled CALL <*label*> mode reduces the number of availble sequence lines by one.) If you have set the sequence number field to RSEQ, you must set the memory page (A or B) and enter a sequence number between 0 and 1023. See the *SEQ Field* description later in this section for information on selecting ASEQ or RSEQ.

This field defaults to page A and sequence 0.

To specify the page and the sequence number for the START SEQ:

1. Move the screen cursor to the START SEQ field.

   START SEQ: [A] [0]

2. Press the SELECT, INCR, or DECR key to change the page. For example, to select page B:

   [B] [0]

3. Use the data entry keys to enter the starting sequence number. For example, to start the pattern generator at line 500:

   [B] [500]

5 INHIBIT MASK Field

Use the INHIBIT MASK field to specify whether or not the data output channels respond to the inhibit signal. If the inhibit mask for a given data channel is set to 0 (unmasked), then that data channel is tri-stated whenever the inhibit signal is asserted. If the inhibit mask is set to 1 (masked), then the inhibit signal is masked out and that data channel is not tri-stated, even though the inhibit signal has been asserted. You can set the inhibit mask for each individual data channel in a pod by specifying a hexadecimal value in the INHIBIT MASK field. The default value for this field is 0 (unmasked for all data channels).

To specify the inhibit mask for a data pod:

1. Move the screen cursor to the INHIBIT MASK field:

```
INHIBIT
  MASK : [0000 0000 0000 0000 0000 0000]
```

2. Use the data entry keys to specify (in hexadecimal) the inhibit mask for each data pod. The DAS will automatically move the screen cursor one space to the right after you have entered a value.

```
INHIBIT
  MASK : [F000 0E00 00D0 000C B000 0A00]
```

6 SEQ (Sequence) Field

The SEQ field consists of a column of numbers running down the left side of the display. Each number in this column corresponds to one sequence line. The program lines are displayed sequentially starting with page A, sequence 0. There are 2048 total sequence lines, but they can be numbered either of two ways. When the SEQ field is set to ASEQ (absolute sequence numbers), the sequence lines are numbered from 0 through 2047. When the SEQ field is set to RSEQ (relative sequence numbers), the sequence lines are divided into two pages of data, page A and page B. The sequence lines are numbered page A, 0 through 1023, and page B, 0 through 1023. Dividing the memory into two pages has certain programming advantages explained under the *91S32 Configuration Menu* description. The PAGE field description in this section explains how to switch from one page to the other. Only a portion of the sequence lines are displayed at any given time.

To select either ASEQ or RSEQ:

1. Move the screen cursor to the SEQ field.

```
[ASEQ]  5DC   5BA   4DC   4BA   3DC   3BA    S    I
```

2. Press the SELECT key until the desired value appears in this field. For example, RSEQ.

   The DAS displays optional values in this order.

```
[ASEQ]
[RSEQ]
```

You can display different sequence lines several different ways. The first method is to use the scroll keys. You can use these keys at any time and with the cursor in any field.

To scroll through the sequences:

1. Press the up (↑) or down (↓) scroll key. Additional sequence lines will scroll up from the bottom or down from the top of the display.

The second method for viewing more program lines requires you to enter a new number over an existing number displayed in the SEQ field. This method allows you to jump forward or backward and display specific blocks of sequence lines.

To move forward and display larger-numbered sequence lines:

1. Move the screen cursor to the sequence number you wish to change. For example, move the cursor to SEQ 11:

   [ASEQ]
   [11]

2. Use the data entry keys to enter the first sequence number you wish to have displayed. For example, SEQ 200. The DAS will display [200] in place of [11], and then update the rest of the sequence lines following that position.

   [ASEQ]
   0
   1
   2
   3
   4
   5
   6
   7
   8
   9
   10
   [200] SEQ 11 is changed to SEQ 200
   201 and the rest of the sequence
   202 numbers are updated from that
   203 position to the bottom of the display.

To move backward to a smaller-numbered block of program lines:

NOTE

The preceding sequence number on the display must always be smaller than the number you enter. If you want to display a number smaller than any currently displayed, you must enter that number in the top-most SEQ field on the display.

1. Move the screen cursor to the sequence number you wish to replace with a lower number. For example, SEQ 200.

   [ASEQ]
   [200]

2. Press the DON'T CARE key.

   The DAS enters a 0 at the cursor location.

3. Use the data entry keys to enter the sequence number to be displayed. For example, 15.

   The DAS displays SEQ 15 at the cursor location, then updates the rest of the sequences from that position.

```
[ASEQ]
   0
   1
   2
   3
   4
   5
   6
   7
   8
   9
  10
[ 15]      SEQ 200 is changed to SEQ 15,
  16         and the rest of the sequence
  17         numbers are updated from
  18         that position.
```

NOTE

When using the above procedures, observe the following two rules: 1), if the cursor is positioned below the top sequence number on the display, you cannot enter a number smaller than the number directly above the cursor location. 2) you cannot enter a number greater than 2047 for ASEQ and 1023 for RSEQ.

7 #DC and #BA Pattern Field

The pattern fields that appear on the sub-menu are used to specify the data pattern you wish to output through the P6464 probes. Data channels are grouped into pods of eight channels that correspond to a particular P6464 probe. A data pod is identified by a letter-number scheme called pod I.D. The pod I.D. number references the slot in the DAS where the 91S32 Module resides. The letters identify the connectors on the back of the 91S32 where the probes are attached. For example, a 91S32 installed in DAS slot 5 would have data column headings named 5DC and 5BA.

Data values are normally entered in hexadecimal, one pod at a time, card by card, and one line at a time. In other words, you would program the pattern for Pod D, and then Pod C, Pod B, and finally Pod A. If you had another 91S32, you would repeat this procedure until all pods had been programmed, and then move to the next sequence line. When the pattern generator is running, all pods output data synchronously with the output clock.

See the *DISPLAY Command* description later in this section for information about changing the display radix of the data columns. Data channels default to 0 for all cards and pods.

To enter data on any program line:

1. Move the screen cursor to the pattern field in the line you wish to program. Position the cursor over the pod to be programmed.

```
 6DC     6BA     5DC     5BA     4DC     4BA
[0000    0000    0000    0000    0000    0000]
```

2. Use the data entry keys to enter the pattern you desire. The DAS will display the data values you have entered in the field and then shift the cursor one space to the right. For example, enter the value 3*hex* for the 91S32 in DAS slot 6, pod D:

```
 6DC     6BA     5DC     5BA     4DC     4BA
[3000    0000    0000    0000    0000    0000]
```

3. Continue entering data values until all the pods have been programmed. Then press the NEXT key and the cursor will move to the first data field of the next line.

8 S (Strobe) Field

Use the S field to select whether or not the strobe lines associated with each pod will be output when this particular program line is executed. This field allows you to individually assert the strobe signals for pods D, C, B, and A. Data pods are grouped into pairs, and each pair is represented by a column in the Strobe field. Strobe values are entered according to the display radix.

When more than one 91S32 is installed, the Strobe field width will expand. Strobe field columns will correspond to the order of data-field columns. In other words, the data column displayed at the left of the screen will correspond to the two high-order bits in the strobe field.

Strobes function just like additional data lines. The strobe transitions are synchronous with the output clock. The strobes are asserted by entering a 1 *binary* into the sequence line's associated S bit. (Note: Pay attention to the display radix.) In default, the strobes are set to 0s. See the *DISPLAY Command* description later in this section for instructions on changing the strobe field display radix.

To assert a strobe:

1. Move the screen cursor to the S field on the line you wish to program.

```
  S
[000]
```

2. Use the data entry keys to enter the data value. For example, to assert the strobes of both pod 5A and 3D in hex, enter 108.

```
[108]
```

9 I (Inhibit) Field

Use the I (Inhibit) field to set the internal inhibit signal. The internal inhibit signal temporarily tri-states the output of one or all of the pods. Data pods are grouped into pairs, and each pair is represented by a column in the Inhibit field. Pods displayed on the left will be represented by the left-most column in the Inhibit field. Inhibit field values are entered for two pods at a time, usually in hexadecimal.

When more than one 91S32 is installed, the Inhibit field width will expand. Inhibit field columns will correspond to the order of the data-field columns. In other words, the data column displayed at the left of the screen will correspond to the two high-order bits in the Inhibit field.

The 91S32 provides two kinds of inhibit signals: Internal inhibits programmed in the 91S32 Program Run sub-menu, and External inhibits, delivered to the 91S32 via the P6452 External Clock (Data Acquisition)probe attached to the DAS Trigger/Time Base module. The 91S32 Configuration sub-menu allows you to select the polarity of each inhibit signal, and combine the two signals using logical operators.

For the following example, assume that the inhibit signals have been set to the following values: INHIBIT [INTERNAL 1] ONLY. (See the *91S32 Configuration Sub-Menu* description earlier in this addendum.)

Setting a 0*hex* in the I (Inhibit) field means that neither pod in the pair is tri-stated and both pods will continue to output data, clock, and strobe lines. Setting a 1*hex* in this field will tri-state the outputs of Pod A. Setting a 3*hex* in this field will cause pods A and B to be tri-stated.

Note that some data may still be output from a pod that has been tri-stated, because any value you set in the INHIBIT MASK field will cause certain data lines to ignore the inhibit signal. Inhibit mask fields for the strobe and clock lines appear in the Configuration sub-menu.

Values for the I (Inhibit) field must be set for every sequence line. The default value is 0 and the default radix is hexadecimal. See the DISPLAY command discription under the *91S32 RUN Sub-Menu* section for instructions on selecting a different display radix. The internal inhibit signal becomes effective in sync with the output clock.

If you are logically combining the internal and extenal inhibit signals in the Setup: Probe sub-menu, it is wise to check the inhibit interaction by viewing a portion of your program while in Step mode.

To assert an internal inhibit:

1. Move the screen cursor to the line you wish to program and position the cursor over the appopriate I field. In this example, there are 91S32s in DAS slots 6, 5, and 4.

   ```
        I
   [000]
   ```

2. Use the data entry keys to enter the data value. For example, to assert the internal inhibits for pods 5A, 4D and 4C in hex, enter 1CO.

   The DAS will display the value you enter in the I field.

   ```
   [1CO]
   ```

10 EDIT Fields

The 91S32 Module provides nine edit commands to manipulate data patterns on program lines. These commands are designed to simplify programming.

To select the edit command:

1. Move the screen cursor to the edit field at the bottom of the screen:

   [CONVERSION] : [CONVERT] POD [ ]

2. Press the SELECT key until the desired command appears in the field. In addition to the SELECT key, the INCR and DECR keys may also be used to select from the edit commands. The INCR key selects the next command given in the list below, and the DECR key selects the previous command. Pressing any one of these keys will cause the DAS to scroll through the list of options.

   The DAS will display the list of possible edit commands in this alphabetical sequence:

   [CONVERSION]
   [COPY]
   [DELETE]
   [DISPLAY]
   [FILL]
   [INSERT]
   [MODIFY]
   [MOVE]
   [SEARCH]

   Each edit command has a specialized function. The CONVERSION command has a sub-menu used to make and check a conversion table. Several commands have sub-fields you will use to specify starting and ending sequence lines, or select among additional sub-commands. Some of the commands will have fields that require you to enter setup and editing parameters.

3. After entering the changes you wish to make for any of the edit operations, press the EXECUTE key. Some of the fields, such as those pertaining to sequence numbers, will be blanked after the edit operation has been completed. This is to prevent you from accidentally pressing EXECUTE again and damaging your corrected program.

   The following paragraphs briefly describe what each of the edit commands does, and how to use them.

CONVERSION The CONVERSION command allows you to search for and replace all pattern data values with corresponding different values in one operation. For instance, if you knew you wanted to replace all FFs in your program with AAs, and replace all 1Es with 00s, you could use the CONVERSION command to do that in one operation.

This feature is most commonly used when you are converting data from one coding system to another, such as from a normal binary counting method to Gray code where only one bit changes as numbers are incremented.

The CONVERSION command has two sub-commands: CONVERT, which designates which pod's data is to be converted, and TABLE BUILD. The TABLE BUILD command displays a special sub-menu called the TABLE BUILD sub-menu that allows you to specify which bit patterns are to change. Instructions for using this sub-menu are included in the following paragraphs.

CONVERT This sub-command instructs the pattern generator to apply the conversion rules outlined in the TABLE BUILD sub-menu to the data in a particular pod. The way in which the TABLE BUILD sub-menu performs conversions will become clear as you read this section. If you had a 91S32 in DAS slot 1 and you wanted to modify the data programmed for Pod B according to the changes given in the TABLE BUILD sub-menu, you would type:

[CONVERSION] : [CONVERT] POD [1B]

Press the EXECUTE key to initiate the conversion.

The TABLE BUILD sub-menu only operates on one pod of data at a time, so if you wanted to convert all data patterns for a 91S32 in DAS slot 1 from one code to another, you would have to CONVERT POD 1A, and then CONVERT POD 1B, 1C and 1D. You will have to run the conversion program four more times for each additional 91S32 to convert all the data from one code to another. However, you will often use the different pods for different purposes, and you may only want to convert one pod's data and leave the rest unchanged.

To specify which pod's data will be converted:

1. Move the screen cursor to the POD field.

   [CONVERSION] : [CONVERT] POD [ ]

2. Use the data entry keys to enter a pod I.D. For example, pod 6B. The DAS will display the pod I.D. in the POD field.

   [CONVERSION] : [CONVERT] POD [6B]

3. Press the EXECUTE key to start the conversion. The DAS will display "CONVERTED POD 6B" on the second line of the screen when the conversion has been completed. The DAS will also blank the POD field to prevent accidental conversions later.

TABLE BUILD The TABLE BUILD sub-menu is used to convert an existing data pattern into some modified data pattern. The sub-menu provides two columns of 4-digit binary numbers from 0000 to 1111. However, you can set the column widths to be up to 8-digits wide. The following examples show 8-digit columns to demonstrate the TABLE BUILD's maximum capabilities.

Modifying the bit pattern in the CODE column and executing the CONVERT command on some pod's data will cause all occurrences of the pattern in the DATA field to be converted to the pattern in the CODE field.

For example: When you enter this sub-menu, both the DATA and CODE columns will contain the same bit pattern. Moving the screen cursor to 00000000 in the CODE column, typing in 00000001, and then executing CONVERT POD 1A will cause all occurrences of 00000000 stored as data in Pod-1A to be changed to 00000001.

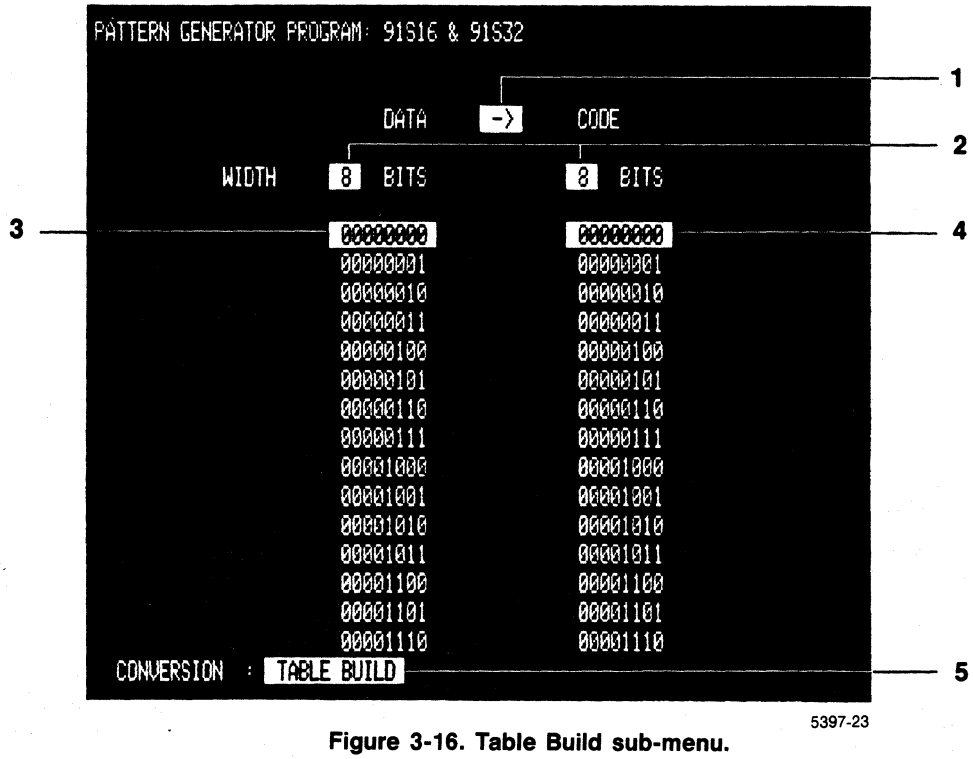
It may help you to think of the bit patterns in the DATA column as sequence numbers. The bit patterns in the DATA column represent all possible bit patterns. Typing some pattern in a DATA field is one way to move your editing window from one bit pattern to another; it will not change any data.

To invoke the TABLE BUILD sub-menu:

1. Move the screen cursor to the field containing CONVERT.

   [CONVERSION] : [CONVERT] POD [ ]

2. Press the SELECT key until TABLE BUILD appears in the field. The TABLE BUILD sub-menu will automatically appear on the screen. Refer to Figure 3-16.



5397-23

Figure 3-16. Table Build sub-menu.

1 → Field

The → field indicates the direction for converting data. If the arrow is pointing to the right, data in the right-hand column will replace the data pattern indicated in the left-hand column. If the arrow is pointing to the left, the pattern in the left-hand column will replace the pattern in the right hand column.

When the arrow is pointing to the right, you can enter the same bit pattern in the right column for any number of bit patterns in the left column. However, when the arrow is pointing to the left, each pattern in the left column must convert to a unique pattern in the right column.

As long as you are mapping a unique pattern in the right column to a unique pattern in the left column, this feature allows you to change the data pattern, and then change back easily if you don't like the results of your first conversion.

This field defaults with the arrow pointing to the right.

To change the direction of the conversion arrow:

1. Move the screen cursor to the arrow field.

   DATA [→] CODE

2. Press the SELECT key until the desired arrow appears in the field.

   DATA [-] CODE

2 WIDTH Fields

The WIDTH fields are used to select the bit width of the data and code columns. For both columns, you can select bit widths ranging from 1 to 8 bits.

Usually, you will want to set both column widths to the same value. The bit width you select will determine the depth of the corresponding DATA and CODE fields. However, if you select a width of 4-bits for the DATA column and 5-bits for the CODE column, both selection fields will be 16 lines deep (16 possible patterns from 4 bits); the field depth always truncates to match the shorter column. Selecting 8-bit field widths for both columns will generate a TABLE BUILD sub-menu with 256 lines of bit-patterns.

If you shorten the width of either the DATA or CODE fields after entering some longer value into one of the fields, the display will change to show the shorter pattern, but the DAS will retain the longer value in memory until it is turned off. The default width for both fields is 4 bits.

To enter the DATA and CODE fields column widths:

1. Move the screen cursor to the WIDTH field over the column you wish to change.

	DATA	CODE
WIDTH	[4] BITS	[4] BITS

2. Use the data entry keys to enter the desired column width. For example, 8.

	DATA	CODE
WIDTH	[8] BITS	[4] BITS

   Remember that no data conversion actually takes place until you EXECUTE the CONVERSION: CONVERT POD [##] command. Depending on how you configure your replacement data patterns in the TABLE BUILD sub-menu, it is possible that the CONVERT command will try to replace an 8-bit pattern with a smaller, say 4-bit, pattern. In this case, only the lowest four bits of the original pattern would be converted to the new pattern, and the data in the four most significant bits would not be changed. For example, if the original pattern was 11111111_{bin}, and the replacement pattern from the TABLE BUILD sub-menu was 0000_{bin}, the resulting data would be 11110000_{bin}.

3 DATA Column

The DATA column automatically appears whenever the TABLE BUILD sub-menu is selected. The DATA column contains all possible bit-patterns for data entered in the PROGRAM: Run sub-menu. Bit patterns in the DATA column represent existing data, where bit patterns in the CODE column represent planned changes to the data. (The only exception to this is when the direction field has the arrow pointing to the left.)

The depth of the DATA column is dependent on the value entered in the WIDTH field. Since all possible bit patterns for a particular width are shown, most TABLE BUILD sub-menus will be too long to be displayed on one screen.

There are several ways of displaying different parts of the TABLE BUILD sub-menu. The first method is to use the scroll keys on the DAS keyboard.

To scroll through the DATA column sequences:

Press the ↑ or the ↓ scroll key on the keyboard. The DAS will scroll the display up or down.

Another method more suited to big jumps is to enter the desired new pattern in a DATA column field. Just as in moving through sequence lines in the Program Run sub-menu, the DAS will display the DATA line you have entered and fill the rest of the page with DATA lines incrementing from that point.

To move forward through a large block of DATA lines:

1. Move the screen cursor to the data field you wish to change. For example, line 1010.

```
    DATA
[00000101]
[00000110]
[00000111]
[00001000]
[00001001]
[00001010]
[00001011]
[00001100]
[00001101]
```

2. Use the data entry keys to enter the first DATA line you wish to display. For example, 11001000.

```
    DATA
[00000101]
[00000110]
[00000111]
[00001000]
[00001001]
[11001000]  DATA pattern 00001010 is
[11001001]  changed to 11001000 and
[11001010]  the remaining DATA patterns
[11001011]  increase from that line.
```

The DAS will display DATA line 11001000 in place of line 00001010, and then update the rest of the DATA lines following that position.

NOTE

Entering a value in one of the DATA column fields is one way of displaying a different portion of this sub-menu; it will not change the data programmed for a pod in the Run sub-menu.

To display a block of DATA patterns with smaller values:

1. Move the screen cursor to the first DATA line displayed in the TABLE BUILD sub-menu.
2. Use the data entry keys to enter the bit pattern you want to display. The display will fill with data lines starting with the pattern you have entered.

NOTE

The DAS displays DATA patterns in ascending order. To display a DATA value smaller than any currently displayed, enter the new DATA value in the topmost DATA column field.

4 CODE Field

The CODE field is used to enter the pattern you want to end up with after the conversion; the DATA field is the pattern you start with. More than one data pattern may be converted to the same CODE pattern. To do this, enter the same CODE pattern next to two or more DATA patterns.

To enter a pattern into the CODE field:

1. Move the screen cursor to the desired CODE field:

DATA	CODE
[00000000]	[00000000]

2. Use the data entry keys to enter the desired pattern. The DAS will display the value you enter in the CODE field:

DATA	CODE
[00000000]	[00001111]

3. Repeat this procedure for each line until all the desired patterns are entered in the CODE fields to the right of the existing patterns.

NOTE

If more than one DATA pattern is converted to the same CODE pattern, the conversion from DATA to CODE can not be reversed by switching the [-] *field to* [-].

5 CONVERSION Field

The CONVERSION field is used to exit the TABLE BUILD sub-menu.

To exit the TABLE BUILD sub-menu:

1. Move the screen cursor to the CONVERSION field:

   CONVERSION : [TABLE BUILD]

2. Press the SELECT key. The DAS will display the Run sub-menu.

   [CONVERSION] : [CONVERT] POD [ ]

COPY The COPY command is used to duplicate sequence lines programmed in the 91S32 Run sub-menu, or to copy the data programmed for one pod to another. This instruction displays a field that allows you to select either SEQ (copy sequences within the Run sub-menu) or POD (copy one pod's data to another pod).

To change the COPY command mode between SEQ and POD:

1. Move the screen cursor to the field to the right of COPY:

   [COPY] : [SEQ] [ ] THROUGH [ ] BEFORE SEQ [ ]

2. Press the SELECT key until the desired mode appears in the field.

```
[  COPY  ] : [POD] [   ] TO [   ]
```

SEQ Use the SEQ sub-command to duplicate sequence lines of program within the 91S32 Run sub-menu. When the COPY SEQ command is executed, all sequence lines specified are duplicated and placed immediately before the given destination. The sequence numbers for the sub-menu are then updated; labels are retained in the duplicated lines.

NOTE

Using the COPY command when all 2047 ASEQ sequence lines, or all 1023 RSEQ (page A or B) sequence lines have been programmed may cause some high-numbered sequence lines to be lost from memory. The number of sequence lines lost will correspond to the number of new lines inserted. If you must add new sequence lines to a lengthy pattern, use the DELETE command first to remove unnecessary lines and make room for the additions.

To copy sequence lines:

1. Move the screen cursor to the SEQ and THROUGH fields.

```
[ASEQ] 5DC   5BA    4DC   4BA    3DC   3BA     S     I
   0   0123  4567   89AB  CDEF   0123  4567    89A   BCD
   1   1234  5678   9ABC  DEF0   1234  5678    9AB   CDE
   2   2345  6789   ABCD  EF01   2345  6789    ABC   DEF
   3   3456  789A   BCDE  F012   3456  789A    BCD   EF0
   4   4567  89AB   CDEF  0123   4567  89AB    CDE   F01
   5   5678  9ABC   DEF0  1234   5678  9ABC    DEF   012
   6   6789  ABCD   EF01  2345   6789  ABCD    EF0   123
   7   789A  BCDE   F012  3456   789A  BCDE    F01   234
   8   89AB  CDEF   0123  4567   89AB  CDEF    012   345
   9   9ABC  DEF0   1234  5678   9ABC  DEF0    123   456
  10   ABCD  EF01   2345  6789   ABCD  EF01    234   567
  11   BCDE  F012   3456  789A   BCDE  F012    345   678
  12   CDEF  0123   4567  89AB   CDEF  0123    456   789
  13   DEF0  1234   5678  9ABC   DEF0  1234    567   89A
  14   EF01  2345   6789  ABCD   EF01  2345    678   9AB
[COPY   ]:[SEQ][   ] THROUGH [    ] BEFORE SEQ [  ]
```

2. Use the data entry keys to enter the starting and ending sequences as well as a destination sequence. For example, to make a copy of sequence lines 0 through 4 and to place them before sequence line 5:

```
[COPY    ] : [SEQ] [   0] THROUGH [   4] BEFORE SEQ [   5]
```

3. Press the EXECUTE key to initiate the COPY SEQ command.

   The DAS will display the message "COPIED SEQ 0 THROUGH 4 BEFORE SEQ 5" in the message field at the top of the display when the operation is complete. The DAS will also blank the SEQ and THROUGH fields to prevent accidental operation.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	0123	4567	89AB	CDEF	0123	4567	89A	BCD
6	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
7	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
8	3456	789A	BCDE	F012	3456	789A	BCD	EF0
9	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
10	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
11	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
12	789A	BCDE	F012	3456	789A	BCDE	F01	234
13	89AB	CDEF	0123	4567	89AB	CDEF	012	345
14	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456

[COPY]:[SEQ] [ ] THROUGH [ ] BEFORE SEQ [ ]

POD The POD sub-command is used to duplicate a pattern entered into memory for one pod and put a copy of the same pattern into memory for another pod. If there is already data in the destination pod, it will be discarded when the new pattern is copied into that pod's memory.

To copy a data pattern from one pod to another:

1. Move the screen cursor to the COPY: POD field.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[COPY] :[POD] [ ] TO [ ]

2. Use the data entry keys to enter a pod I.D. For example, to make a copy of pod 5B and send it to pod 3D.

   [COPY]: [POD] [5B] TO [3D]

3. Press the EXECUTE key to start COPY POD operation.

   The DAS will display the message "COPIED POD 5B TO 3D" in the message field on the second line of the display when the COPY POD operation has been completed. The DAS will also blank the source and destination fields to prevent accidental operation.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	4523	4567	89A	BCD
1	1234	5678	9ABC	DEF0	5634	5678	9AB	CDE
2	2345	6789	ABCD	EF01	6745	6789	ABC	DEF
3	3456	789A	BCDE	F012	7856	789A	BCD	EF0
4	4567	89AB	CDEF	0123	8967	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	9A78	9ABC	DEF	012
6	6789	ABCD	EF01	2345	AB89	ABCD	EF0	123
7	789A	BCDE	F012	3456	BC9A	BCDE	F01	234
8	89AB	CDEF	0123	4567	CDAB	CDEF	012	345
9	9ABC	DEF0	1234	5678	DEBC	DEF0	123	456
10	ABCD	EF01	2345	6789	EFCD	EF01	234	567
11	BCDE	F012	3456	789A	F0DE	F012	345	678
12	CDEF	0123	4567	89AB	01EF	0123	456	789
13	DEF0	1234	5678	9ABC	12F0	1234	567	89A
14	EF01	2345	6789	ABCD	2301	2345	678	9AB

[COPY] : [POD] [ ] TO [ ]

DELETE Use the DELETE command to erase sequence lines within the Program Run sub-menu. When the DELETE command is executed, all sequence lines between the given starting and ending sequence lines (inclusive) are deleted. The remaining sequence line numbers are automatically updated.

NOTE

When sequence lines are removed by the DELETE command, a corresponding number of new sequence lines containing default values are created at the end of the pattern generator's memory. These new sequence lines will be inserted after the last sequence line that contains programming data in order to maintain a total of 2048 sequence lines (ASEQ) or 1023 lines (RSEQ) for both Page A and Page B.

NOTE

If you attempt to use the DELETE function across page boundries when the 91S32s are set to FOLLOWS 91S16 mode, only the lines within the current page will be deleted; you will have to change to the other page and repeat the DELETE operation to remove the rest of the sequence lines.

To delete one or more sequence lines:

1. Move the screen cursor to the edit command field at the bottom of the Run sub-menu screen. Press the SELECT key until DELETE appears in the field.

2. Move the screen cursor to the SEQ field.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[DELETE] : [SEQ] [ ] THROUGH [ ]

3. Use the data entry keys to enter the sequence numbers of the first and last lines you wish to delete. If you only wish to delete one line, enter that sequence number in both fields. For example, to erase sequence lines between SEQ 3 and 5.

   [DELETE]: SEQ [3] THROUGH [5]

4. Press the EXECUTE key to start the DELETE operation. The DAS will display the message "DELETED SEQ 3 THROUGH 5" when the DELETE operation has been completed. The DAS will also update the remaining sequence line numbers, and blank the SEQ and THROUGH fields to prevent accidental operations.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
4	789A	BCDE	F012	3456	789A	BCDE	F01	234
5	89AB	CDEF	0123	4567	89AB	CDEF	012	345
6	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
7	ABCD	EF01	2345	6789	ABCD	EF01	234	567
8	BCDE	F012	3456	789A	BCDE	F012	345	678
9	CDEF	0123	4567	89AB	CDEF	0123	456	789
10	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
11	EF01	2345	6789	ABCD	EF01	2345	678	9AB
12	F012	3456	789A	BCDE	F012	3456	789	ABC
13	0123	4567	89AB	CDEF	0123	4567	89A	BCD
14	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE

[DELETE] : [SEQ] [ ] THROUGH [ ]

DISPLAY Use the DISPLAY command to select the display radix for the vector data, S (Strobe), and I (Internal Inhibit) fields. This command is designed to make it easier for you to read the values programmed into these fields, or to remove them from the display if they are not being used.

NOTE

Changing the radix of several fields when there are several 91S32s installed may cause some data columns to disappear from the display. These data columns can still be viewed by using the right arrow (→) scroll key to shift the display to the right.

To remove or change the radix of the DATA, S, and I fields:

1. Move the screen cursor to the field you wish to change.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[DISPLAY] : 5DC [HEX] 5BA [HEX] 4DC [HEX] 4BA [HEX] 3DC [HEX] 3BA [HEX] S [HEX] I [HEX]

2. Press the SELECT key to change the radix or to turn off the field. For example, to change the radix for the 4DC column to OCT (Octal) and to change the I (Internal Inhibit) field to BIN (Binary) and to turn off the S (Strobe) field:

   [DISPLAY] : 5DC [HEX] 5BA [HEX] 4DC [OCT] 4BA [HEX] 3DC [HEX] 3BA [HEX] S [OFF] I [BIN]

   The DAS will then change the display of the 4DC, I, and S fields as follows:

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	I
0	0123	4567	89AB	CDEF	0123	4567	101111001101
1	1234	5678	9ABC	DEF0	1234	5678	110011011110
2	2345	6789	ABCD	EF01	2345	6789	110111101111
3	3456	789A	BCDE	F012	3456	789A	111011110000
4	4567	89AB	CDEF	0123	4567	89AB	111100000001
5	5678	9ABC	DEF0	1234	5678	9ABC	000000010010
6	6789	ABCD	EF01	2345	6789	ABCD	000100100011
7	789A	BCDE	F012	3456	789A	BCDE	001000110100
8	89AB	CDEF	0123	4567	89AB	CDEF	0011010000101
9	9ABC	DEF0	1234	5678	9ABC	DEF0	010001010110
10	ABCD	EF01	2345	6789	ABCD	EF01	010101100111
11	BCDE	F012	3456	789A	BCDE	F012	011001111000
12	CDEF	0123	4567	89AB	CDEF	0123	011110001001
13	DEF0	1234	5678	9ABC	DEF0	1234	100010011010
14	EF01	2345	6789	ABCD	EF01	2345	100110101011

[DISPLAY] : 5DC [HEX] 5BA [HEX] 4DC [OCT] 4BA [HEXC] 3DC [HEX] 3BA [HEX] S [OFF] I [BIN]

FILL The FILL command is used to automatically fill in the values of the #DC (PODs D and C data), #BA (PODs B and A data), S (Strobe), and I (Internal Inhibit) fields with some constant values. For instance, if you knew you wanted all the sequence lines from line 20 through line 30 to have the same data value for POD A, you could use the FILL command to automatically enter that value in each data field instead of having to enter the value for each line individually.

You might use this command to change all the default values in the S (Strobe) field from 0s to 1s. For large scale data value changes, see the CONVERSION: CONVERT Table Build sub-menu discription earlier in this section.

The FILL command provides editing fields to modify each of the data, S, and I columns in the Program: Run sub-menu. The replacement value for each column can be specified individually. You can choose to modify the value in all columns in one operation, or choose to modify just one or two columns at a time. Enter a DON'T CARE (X) into the FILL command fields for the columns you do not want to modify.

To use the FILL command:

1. Select the FILL command by pressing the SELECT key while the cursor is in the edit command field at the bottom of the DAS display.
2. Move the screen cursor to the SEQ field:

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[FILL] : SEQ [ ] THROUGH [ ]
[XXXX XXXX XXXX XXXX XXXX XXXX] [XXX] [XXX]

3. Use the data entry keys to enter the starting and ending sequence numbers. Then move the cursor to the appropriate field and enter the pattern you wish to place in all the corresponding fields within that sequence range. For example, to fill SEQ lines 1 through 4 with "XXXX 0A0A XXXX XXXX XXXX XXXX 0C0 111".

[FILL] : SEQ [1] THROUGH [4]
[XXXX 0A0A XXXX XXXX XXXX XXXX] [0C0] [111]

4. Press the EXECUTE key to start the FILL operation. The DAS will display the message "FILLED SEQ 1 THROUGH 4" on the second line of the display when the FILL operation has been completed. The DAS will also blank the SEQ and THROUGH fields, but not the pattern fields.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	0A0A	9ABC	DEF0	1234	5678	0C0	111
2	2345	0A0A	ABCD	EF01	2345	6789	0C0	111
3	3456	0A0A	BCDE	F012	3456	789A	0C0	111
4	4567	0A0A	CDEF	0123	4567	89AB	0C0	111
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[FILL] : SEQ [ ] THROUGH [ ]
[XXXX 0A0A XXXX XXXX XXXX XXXX] [0C0] [111]

INSERT Use the INSERT command to insert additional sequence lines into the Program: Run sub-menu. The number of additional lines specified in the LINE(S) field is inserted just before the destination sequence line. The SEQ numbers for all the sequence lines are then updated. Newly inserted sequence lines always contain default values.

NOTE

Adding sequence lines to a full memory page can cause existing sequence lines to be lost at the page boundries. If you add sequence lines between SEQ 0 and 1023, you may lose sequence lines at SEQ 1023. If you add sequence lines between SEQ 1024 and 2047, you may lose sequence lines at SEQ 2047. The number of sequence lines lost will correspond to the number of new lines inserted. If you must add new sequence lines to a lengthy pattern, use the DELETE command first to remove unnecessary lines and make room for the new lines.

To insert sequence lines:

1. Select the INSERT command by pressing the SELECT key while the cursor is in the edit command field at the bottom of the Program Run sub-menu.

2. Move the screen cursor to the LINE(S) field.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[INSERT] : [ ] LINE(S) BEFORE SEQ [ ]

Use the data entry keys to enter the number of lines you wish to add. Enter the sequence number where you want them to be inserted. For example, to insert 3 lines before SEQ 2:

[INSERT] : [3] LINE(S) BEFORE SEQ [2]

3. Press the EXECUTE key to start the INSERT operation.

The DAS will display the message "INSERTED 3 LINE(S) BEFORE SEQ 2" in the message field when the insert operation has been completed. The DAS will also update the remaining sequence numbers, and blank the LINE(S) and SEQ fields to prevent accidental insertions.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	0000	0000	0000	0000	0000	0000	000	000
3	0000	0000	0000	0000	0000	0000	000	000
4	0000	0000	0000	0000	0000	0000	000	000
5	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
6	3456	789A	BCDE	F012	3456	789A	BCD	EF0
7	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
8	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
9	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
10	789A	BCDE	F012	3456	789A	BCDE	F01	234
11	89AB	CDEF	0123	4567	89AB	CDEF	012	345
12	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
13	ABCD	EF01	2345	6789	ABCD	EF01	234	567
14	BCDE	F012	3456	789A	BCDE	F012	345	678

[INSERT] : [ ] LINE(S) BEFORE SEQ [ ]

MODIFY The MODIFY command uses logical operators to manipulate data already programmed in the Program Run sub-menu. Three logical operators are available: AND, OR, and XOR (exclusive OR). Any programmable numeric column in the Run sub-menu can be modified by using these operators. For example, you can modify one or both of the data fields, the S (Strobe), and the I (Internal Inhibit) field, or any combination of the above. You can also limit the modification to a range of sequence numbers.

By ANDing a particular column with 0, you can modify all the data in that column to 0's. (Any number ANDed with 0 equals 0.) By ORing a column with a 1, you can set all the bits in that column to 1. (Any number ORed with a 1 equals 1.) By XORing (exclusive OR) any pattern with a 1, the bit pattern in that field is inverted. (In other words, all FFs $_{hex}$ would be changed to 00s, and all 11s $_{hex}$ become EEs.)

Here are reminder truth tables for the AND, OR, and XOR operations:

A AND B

A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

A OR B

A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

A XOR B

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

To modify the pattern fields.

1. Press the SELECT key when the screen cursor is in the edit command field at the bottom of the Run sub-menu until the MODIFY command is displayed.
2. Move the screen cursor to the field immediately to the right of MODIFY and press the SELECT key until the desired logical operator is displayed. Logical operators are displayed in this order: AND, OR, XOR.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[MODIFY] : LOGICAL [AND] SEQ [ ] THROUGH [ ] BEFORE SEQ [ ]
[XXXX XXXX XXXX XXXX XXXX XXXX] [XXXX] [XXX]

3. Press the SELECT key until the desired operator appears in the field. For example, XOR.

   [MODIFY] : LOGICAL [XOR] SEQ [ ] THROUGH [ ]
   [XXXX XXXX XXXX XXXX XXXX XXXX] [XXX] [XXX]

4. Move the screen cursor to the SEQ and THROUGH fields. Use the data entry keys to enter the number of the first and last sequence lines you want to modify. For example, to modify sequence lines 1 through 9, enter:

   [MODIFY] : LOGICAL [XOR] SEQ [1] THROUGH [9]
   [XXXX XXXX XXXX XXXX XXXX XXXX] [XXX] [XXX]

5. Move the screen cursor down to the pattern line and enter the pattern you wish to use as a modifier. For example, to invert all the Pod 3B and 3A data patterns, select XOR as the logical operator and enter FFFF$_{hex}$ in the column A field. (Fields containing X are not affected by the MODIFY command.)

   [MODIFY] : LOGICAL [XOR] SEQ [1] THROUGH [9]
   [XXXX XXXX XXXX XXXX XXXX FFFF] [XXX] [XXX]

6. Press the EXECUTE key to start the MODIFY operation. The DAS will display the message "MODIFIED SEQ 1 THROUGH 9" in the message field at the top left-hand corner of the display. The DAS will also blank the SEQ and THROUGH fields to prevent accidental operation.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	A987	9AB	CDE
2	2345	6789	ABCD	EF01	2345	9876	ABC	DEF
3	3456	789A	BCDE	F012	3456	8765	BCD	EF0
4	4567	89AB	CDEF	0123	4567	7654	CDE	F01
5	5678	9ABC	DEF0	1234	5678	6543	DEF	012
6	6789	ABCD	EF01	2345	6789	5432	EF0	123
7	789A	BCDE	F012	3456	789A	4321	F01	234
8	89AB	CDEF	0123	4567	89AB	3210	012	345
9	9ABC	DEF0	1234	5678	9ABC	210F	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[MODIFY] : LOGICAL [XOR] SEQ [ ] THROUGH [ ]
[XXXX XXXX XXXX XXXX XXXX FFFF] [XXX] [XXX]

MOVE Use the MOVE command to move some block of sequence lines within a program to another location within that same program. When MOVE is executed, all the sequence lines specified are moved to a location just before the given destination sequence. The sequence numbers are then automatically updated. Labels, data, and instructions are retained when sequence lines are moved.

Using the MOVE command does not cause high-numbered program lines to be lost even if all 1022 sequence lines have been programmed.

NOTE

When 91S32 Modules are used in FOLLOWS 91S16 mode, you cannot move sequence lines from one page of memory to the other (e.g., Page A to Page B).

To MOVE a block of sequence lines from one location to another:

1. Select the MOVE command by pressing the SELECT key when the screen cursor is in the edit command field at the bottom of the 91S32 Program: Run sub-menu.
2. Move the screen cursor to the SEQ field.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[MOVE] : SEQ [ ] THROUGH [ ] BEFORE SEQ [ ]

3. Use the data entry keys to enter the starting, ending, and destination sequence numbers. For example, to move sequence lines 1 through 3 and place them before sequence line 7:

[MOVE] : SEQ [1] THROUGH [3] BEFORE SEQ [7]

4. Press the EXECUTE key to start the MOVE operation. The DAS will display the message "MOVED SEQ 1 THROUGH 3 BEFORE SEQ 7" on the message line. The DAS will also update all the sequence lines and blank the SEQ, THROUGH and, BEFORE fields to prevent accidental move operations.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
2	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
3	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
4	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
5	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
6	3456	789A	BCDE	F012	3456	789A	BCD	EF0
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[MOVE] : SEQ [ ] THROUGH [ ] BEFORE SEQ [ ]

Search. Use the SEARCH command to locate some specific entry within the body of the Program Run sub-menu. The entry may be a particular data pattern, a strobe value, or an internal inhibit value.

The SEARCH command allows you to specify the type of entry you are going to search for, and specify a sequence range for the search. When executed, the SEARCH command compares all entries of the same type against the target string within the range of sequence lines you have specified. It will then place the screen cursor on the first sequence line containing that string, and display the total number of lines within the specified range that contain the target string. (The number of occurrences appears in the bottom right-hand corner of the display.)

The data entry keys can be used to select the second, or third, etc. sequence line containing the target string when the screen cursor is in the [ ]/ # : SEARCHED field. (Instructions for using this field are included in the following paragraphs.)

The SEARCH command has a sub-field used to specify the pattern you want to search for. Fields containing X's (Don't Cares) match all data patterns.

To search a pattern:

1. Select the SEARCH command by moving the screen cursor to the edit command field at the bottom of the Program Run sub-menu and pressing the SELECT key.

2. Select the type of pattern you are going to search for by moving the screen cursor to the field immediately to the right of the SEARCH command.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
0	0123	4567	89AB	CDEF	0123	4567	89A	BCD
1	1234	5678	9ABC	DEF0	1234	5678	9AB	CDE
2	2345	6789	ABCD	EF01	2345	6789	ABC	DEF
3	3456	789A	BCDE	F012	3456	789A	BCD	EF0
4	4567	89AB	CDEF	0123	4567	89AB	CDE	F01
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
9	9ABC	DEF0	1234	5678	9ABC	DEF0	123	456
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[SEARCH] : SEQ [ ] THROUGH [ ]
[XXXX XXXX XXXX XXXX XXXX XXXX] [XXX] [XXX]

3. Move the screen cursor to the SEQ and THROUGH fields and enter the starting and ending sequence numbers for the block of program you wish to search. For example, enter SEQ 0 and THROUGH 10, to search for a pattern programmed in lines 0 through 10, inclusive. Note: the larger the search range you specify, the longer it takes for the edit operation to be completed, and the greater the likelihood you will locate data you are not interested in.

4. Move the screen cursor to the PATTERN sub-fields and use the data entry keys to enter the pattern you wish to find. For example, to search for a pattern between SEQ 0 and 10:

[SEARCH] : SEQ [0] THROUGH [10]

[XXXX XXXX 1234 XXXX XXXX XXXX] [123] [XXX]

5. Press the EXECUTE key to start the SEARCH operation. The DAS will display the message, "<[1]/ 1 : SEARCHED>" in the bottom right-hand corner of the display. The first number in this message indicates that the screen cursor has been placed on the line containing the first instance of the target pattern. The number following the slash tells you how many lines contain the target pattern within the range you specified for the search.

[ASEQ]	5DC	5BA	4DC	4BA	3DC	3BA	S	I
5	5678	9ABC	DEF0	1234	5678	9ABC	DEF	012
6	6789	ABCD	EF01	2345	6789	ABCD	EF0	123
7	789A	BCDE	F012	3456	789A	BCDE	F01	234
8	89AB	CDEF	0123	4567	89AB	CDEF	012	345
[9]	[9ABC	DEF0	1234	5678	9ABC	DEF0]	[123]	[456]
10	ABCD	EF01	2345	6789	ABCD	EF01	234	567
11	BCDE	F012	3456	789A	BCDE	F012	345	678
12	CDEF	0123	4567	89AB	CDEF	0123	456	789
13	DEF0	1234	5678	9ABC	DEF0	1234	567	89A
14	EF01	2345	6789	ABCD	EF01	2345	678	9AB

[SEARCH] : SEQ [0] THROUGH [10]
[XXXX XXXX 1234 XXXX XXXX XXXX] [123] [XXX]

For instance, if you had searched for 0000 in a block of text where 15 lines contained the pattern 0000, the message would read: "<[1]/ 15 : SEARCHED>". If you wanted to see the 14th occurrence of the target pattern, you could move the screen cursor to the highlighted field in the first part of this message and type in 14. When you pressed the EXECUTE key, the screen cursor would be placed on the line containing the 14th occurrence of the target pattern, and the message field would read: "<[14]/ 15 : SEARCHED>".

91S16 PROGRAM: TRACE AND STEP MODE SUB-MENUS

NOTE

The 91S16 Program Trace and Step sub-menus appear only when there is a 91S16 installed in the DAS.

The following paragraphs describe how you can use the 91S16 Trace and Step modes to monitor program execution and pattern output. Both Step and Trace modes cause the pattern generator to output data much more slowly than during normal operation. Trace mode causes the pattern generator to output data at a rate slow enough for you to monitor key parameters, while Step executes a single line of program each time you press the START PAT GEN key.

Both the Trace and Step sub-menus display CLOCK (the number of sequence lines executed since you pressed START), SEQ (the sequence line currently being executed), #B and #A (data output from pods B and A), S (strobe), register and control information.

Two features distinguish Trace mode from Step mode. Trace mode outputs the test vectors as fast as the DAS can but the corresponding data on the screen. Trace mode also allows you to set a breakpoint to automatically stop program execution after executing some specified program line. In Step mode, a test vector is output every time the START PAT GEN key is pressed; no breakpoint is needed since you control every output manually.

Figures 24 and 25 illustrate the 91S16 Pattern Generator Trace and Step Mode sub-menus. Refer to the numbered callouts when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.

NOTE

In the following discussion, the 91S16 is assumed to be installed in DAS slot 6.

1 PATTERN GENERATOR PROGRAM Field

Use this field (directly to the right of the menu title) to select either the 91S16 or the 91S32 sub-menu display. The 91S16 sub-menu is the default menu.

2 MODE Field

Use the MODE field to select the pattern generator's operating mode. The 91S16 has three modes of operation: Run, Trace, and Step. When operating in the Run mode, the pattern generator outputs data at the clock rate selected in the CONFIGURATION sub-menu. When in Trace mode, the pattern generator runs on a much slower clock of several hundred miliseconds, slow enough for you to see key trends in program execution. In Step mode, pattern execution is clocked each time you press the START PAT GEN key. Trace and Step modes assist you in debugging your pattern generation programs.

The MODE field defaults to Run mode.

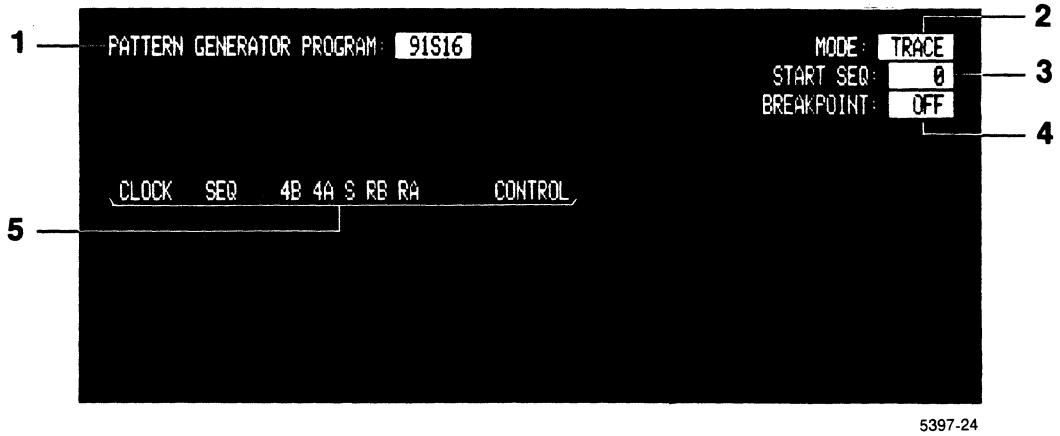


Figure 3-17. 91S16 Program: Trace sub-menu.

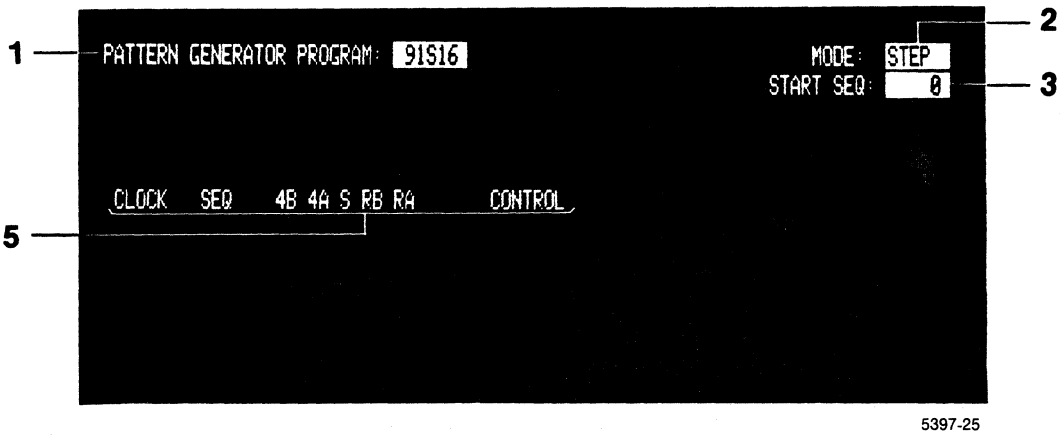


Figure 3-18. 91S16 Program: Step sub-menu.

Figures 3-17 and 3-18 illustrate the 91S16 Pattern Generator Trace and Step Mode sub-menus. Refer to the numbered callouts when reading the following paragraphs. These numbers serve as visual references and do not imply sequence of use.

TRACE The Trace mode allows continuous execution of the pattern generator program while allowing you to monitor the execution on the Trace sub-menu display. Program execution is monitored by a readback function in the 91S16. This function allows you to see how often interrupt servicing routines are called, how many times certain loops are executed, where interrupt routines are activated, and the general branching structure of your program.

Use the START PAT GEN key to start Trace mode pattern execution. Execution stops when any key other than the <SHIFT> START PAT GEN key is pressed, when the pattern generator encounters a HALT in a program sequence line, or when it reaches sequence line 1023. When the pattern generator has been stopped for any reason, the DAS will display "PATTERN GENERATOR STOPPED" in the message field at the top left-hand corner of the display. If you press the START PAT GEN key after execution has been stopped, execution will resume at the sequence line specified in the START SEQ field of the Trace sub-menu.

NOTE

If any key other than the <SHIFT> PAT GEN key is pressed during Trace operation, the normal function of that key will be ignored and the pattern generator will stop outputting data.

The pattern generator also stops execution when it encounters a breakpoint specified in the Trace sub-menu BREAKPOINT field. The breakpoint is specified as a sequence line number. The pattern generator will output data and perform any instruction listed in the breakpoint line before stopping.

This feature allows you to output only a narrow range of program lines by specifying the starting sequence in the START SEQ field, and specifying the ending sequence with the BREAKPOINT field. Following a breakpoint, you can resume pattern output on the next sequence line by pressing the START PAT GEN key. Detailed instructions for using this field are given later in this section.

STEP The Step mode sub-menu performs the same functions as the Trace mode sub-menu but it allows you to have more control over data execution. Program execution proceeds only as fast as you press the START PAT GEN key. There is no breakpoint field for the Step sub-menu because you control every step of program execution manually. When the pattern generator executes a line containing the HALT instruction, or when it reaches the end of the pattern generator memory, the DAS will display the message "PATTERN GENERATOR STOPPED" in the upper-left corner of the display. If you press the START PAT GEN key again, the pattern generator will start execution at the first sequence line listed in the START SEQ: field.

NOTE

Use the INCR and DECR keys instead of the SELECT key to change between Step and Trace modes; otherwise you will lose the current display.

To change the 91S16 MODE of operation:

1. Move the screen cursor to the MODE field in the upper right-hand corner of the display.

   MODE: [RUN]

2. Press the SELECT, INCR, or DECR key until the desired mode appears in this field. The DAS will the display the MODE field values in this order:

   [RUN]
   [TRACE]
   [STEP]

3 START SEQ Field

Use the START SEQ field to set the first sequence number to be executed when the pattern generator begins operation. (You can start the pattern generator by pressing either the START PAT GEN key or the START SYSTEM key.) The START SEQ value may be any number between 0 and 1023 if no service interrupt call has been programmed, and between 0 and 1022 if the service interrupt call has been programmed.

To enter a beginning sequence number in the START SEQ field:

1. Move the screen cursor to the START SEQ field.

   START SEQ: [0]

2. Use the data entry keys to enter the sequence number. For example:

   START SEQ: [500]

NOTE

If the IRQ CALL instruction has been selected in the CONFIGURATION sub-menu after you have programmed the START SEQ field to 1023, the START SEQ field will be reset to 0. (Valid SEQ numbers are 0-1022 when IRQ CALL is programmed.)

4 BREAKPOINT Field

NOTE

The BREAKPOINT field is only available in the Trace mode sub-menu. Step mode is always manually controlled and thus does not need a breakpoint.

Use this field to set a breakpoint at any sequence line where pattern generator execution needs to be suspended. You can only set one breakpoint at a time. When a breakpoint sequence number has been set in the BREAKPOINT field, the pattern generator will execute all preceding sequences, including the sequence line containing the breakpoint, and then stop. The BREAKPOINT field default value is OFF.

To set a BREAKPOINT:

1. Select the Trace Mode sub-menu. Move the screen cursor to the BREAKPOINT field in the upper right-hand corner of the display.

```
     MODE: [TRACE]
START SEQ: [ 0]
BREAKPOINT: [ OFF]
```

2. Press the SELECT key to turn on the BREAKPOINT function. The sequence number field will appear below the BREAKPOINT field.

```
     MODE: [TRACE]
START SEQ: [ 0]
BREAKPOINT: [ ON ]
            [1023]
```

3. Move the screen cursor to the sequence number field and use the data entry keys to enter the number of the sequence line where you want the breakpoint to occur. For example, enter sequence line 500:

```
      MODE: [TRACE]
 START SEQ: [    0]
BREAKPOINT: [ ON ]
            [ 500]
```

5 Program Display Column Headings

The Trace and Step mode sub-menus have six types of headings under which data is tabulated as program execution is being traced. The number of clocks (sequence lines executed since START was pressed), data patterns output, strobes, the contents of the pattern generator register(s), and instructions programmed for each sequence line are displayed below these headings as each program line is executed.

For example, if sequence line 100 was executed as the 115th sequence (some loop accounted for the other 15 clock cycles), the Trace sub-menu might show this display:

CLOCK	SEQ	6B	6A	S	RB	RA	CONTROL
115	100	FF	1A	1	00	04	INCR PAGE

Data is displayed line by line, and scrolls up from the bottom of the display when the screen is full.

CLOCK This heading shows the number of clocks generated since the pattern generator was started. The clock begins counting at 0 and is reset when it reaches 9999. Because of loops, jumps, and subroutine calls, the clock cycle does not necessarily correspond to the sequence line being executed.

SEQ This heading shows the sequence number of the program line that has just been executed. It is the same sequence number that appears in the Run sub-menu. By tracking this number, program flow can be thoroughly monitored.

#B and #A These headings display the pattern delivered to the P6464 probe tips. The number relates to the slot in the DAS where the 91S16 is installed, and the letter denotes the pod. A DON'T CARE (X) in this field indicates that at least one of the channels in that pod has been tri-stated (assuming display in Hex). The radix for this field can be changed by using the DISPLAY command in the 91S16 Run sub-menu.

S The S (strobe) heading displays the status of the strobe lines. A DON'T CARE (X) in this field indicates that at least one of the strobe lines has been tri-stated. The radix for this field can be changed by using the DISPLAY command in the 91S16 Run sub-menu.

RB, RA These headings display the contents of the 91S16 pattern generator's registers. RB displays the contents of 8-bit register RB. RA displays the contents of register RA. If you have selected just one 16-bit register instead of two 8-bit registers in the 91S16 Configuration sub-menu, the heading changes to R. The radices for these fields are set by the radices of the #B and #A data pattern fields. If the pattern generator register has been set to a single 16-bit register, the 8 most significant bits of this display column follow the radix set for #B, and the 8 least significant bits of this display column follow the radix set for #A.

CONTROL This heading covers the display of all CONTROL instructions when they are executed. The two CONTROL instructions are TRIGGER and INCR PAGE (increment page). See the explanation for these commands in the 91S16 Run Menu section of this manual. In brief, TRIGGER causes a TTL-level signal to be output via a phono jack on the back of the 91S16. This signal can be used to trigger an external test device, such as an oscilloscope. INCR PAGE is used by the 91S16 to control 91S32s when a long pattern is being downloaded from a host computer or mass storage device.

91S32 PROGRAM: TRACE AND STEP MODE SUB-MENUS

NOTE

The 91S32 Program Trace and Step sub-menus appear only when there is a 91S32 installed in the DAS.

The following paragraphs describe how you can use the 91S32 Trace and Step modes to monitor program execution and pattern output. Both Step and Trace modes cause the pattern generator to output data much more slowly than during normal operation. Trace mode causes the pattern generator to output data at a rate slow enough for you to monitor sequence flow, while Step executes only one line of program each time you press the START PAT GEN key.

Both the Trace and Step sub-menus display CLOCK (the number of sequence lines executed since you pressed START), SEQ (the sequence line currently being executed), #DC and #BA (data output from pods grouped in pairs), and S (strobe).

Figures 3-19 and 3-20 illustrate the 91S32 Pattern Generator Trace and Step Mode sub-menus. Refer to the numbered callouts when reading the following paragraphs. The numbers serve as visual references and do not imply sequence of use.

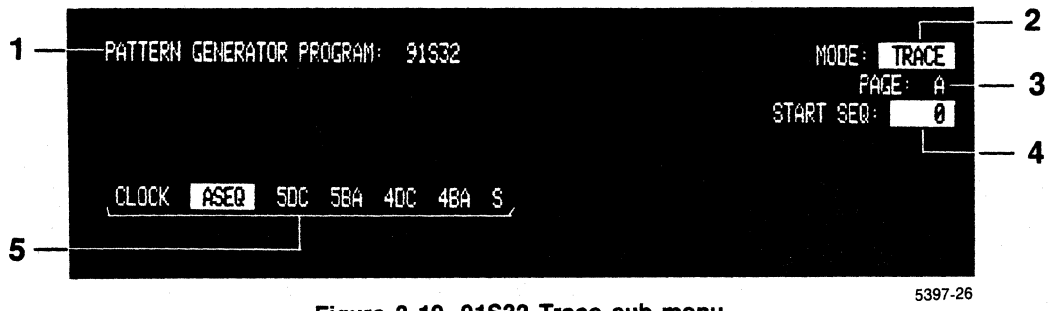


Figure 3-19. 91S32 Trace sub-menu.

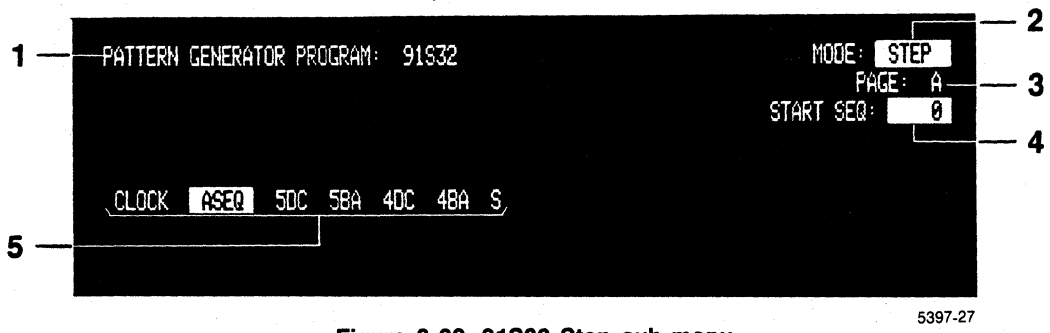


Figure 3-20. 91S32 Step sub-menu.

NOTE

In the following discussion, 91S32s are assumed to be installed in DAS slots 3, 4, and 5.

1 PATTERN GENERATOR PROGRAM Field

Use this field (directly to the right of the menu title) to select either the 91S16 or the 91S32 sub-menu display. The 91S16 sub-menu is the default menu.

To display the 91S32 Program sub-menus, position the screen cursor in this field and press the SELECT key. To change back to the 91S16 sub-menu, press the SELECT key again.

2 MODE Field

Use the MODE field to select the pattern generator's operating mode. The 91S32 has three modes of operation: Run, Trace, and Step. When operating in the Run mode, the pattern generator outputs data at the clock rate selected in the CONFIGURATION sub-menu. When in Trace mode, the pattern generator runs on a much slower clock of serveral hundred miliseconds, slow enough for you to see key trends in program execution. In Step mode, pattern execution is clocked each time you press the START PAT GEN key. Trace and Step modes are designed to assist you in debugging your pattern generation programs.

The MODE field defaults to Run mode.

TRACE The Trace mode allows continuous execution of the pattern generator program while allowing you to monitor the execution on the Trace sub-menu display. Program execution is monitored via a readback function in the 91S32. This will allow you to see how often subroutines are called, how many times certain loops are executed, where interrupt routines are activated, and the general branching structure of your program.

Use the START PAT GEN key to start Trace mode pattern execution. Execution will stop when any key is pressed, or when the pattern generator reaches sequence line 2047. When the pattern generator has been stopped for any reason, the DAS will display "PATTERN GENERATOR STOPPED" in the message field at the top left-hand corner of the display. If you press the START PAT GEN key after execution has been stopped, execution will resume at the sequence line specified in the START SEQ field of the Trace sub-menu.

STEP The Step mode sub-menu performs the same functions as Trace mode, except that only one program line is executed for each time you press the START PAT GEN key. When the pattern generator reaches the end of the pattern generator memory, the DAS will display the message "PATTERN GENERATOR STOPPED" in the upper-left corner of the display. Pressing the START PAT GEN key again will cause the pattern generator to start execution at the first sequence line listed in the START SEQ: field.

NOTE

When you change the mode field from Trace to Step, or to Run, the current display is lost. To change between Trace and Step mode without losing the current display, use the INCR and DECR keys instead of the SELECT key.

To change the 91S32 MODE of operation:

1. Move the screen cursor to the MODE field in the upper-right corner of the display.

   MODE: [RUN]

2. Press the SELECT, INCR, or DECR key until the desired mode appears in this field. The DAS will the display the MODE field values in this order:

   MODE: [RUN]
   MODE: [TRACE]
   MODE: [STEP]

3 PAGE: Heading

The page field indicates which page of the 91S32's memory is being executed. In this sub-menu the page value cannot be set; it is displayed here for reference purposes.

4 START SEQ Field

Use the START SEQ field to set the first sequence number to be executed when the pattern generator begins operation. (You can start the pattern generator by pressing either the START PAT GEN key or the START SYSTEM key.) The START SEQ value may be any number between 0 and 2047 if you are programming in absolute sequence numbers (ASEQ). If you are using relative sequence numbers (RSEQ), the range is Page A, 0 through 1023, or Page B, 0 through 1023. See the *91S32 Program: Run Sub-Menu* description for details concerning ASEQ and RSEQ numbers.

To enter a beginning sequence number in the START SEQ field:

1. Move the screen cursor to the START SEQ field.

   START SEQ: [0]

2. Use the data entry keys to enter the sequence number. For example:

   START SEQ: [500]

5 Program Display Column Headings

The Trace and Step mode sub-menus have four types of headings under which data is tabulated as program execution is being traced. The number of clocks (sequence lines executed since START was pressed), the number of the sequence line currently being executed, the data patterns being output via the P6464 probes, and the values programmed for each strobe are displayed below these headings as each program line is executed.

For example, if sequence line 100 was executed as the 115th sequence (some loop controlled by a 91S16 accounted for the other 15 clock cycles), the Trace sub-menu might show this display:

CLOCK	SEQ	6DC	6BA	S
115	100	01FF	1AEE	0

Data is shown line by line, and scrolls up from the bottom of the display when the screen is full.

CLOCK This heading shows the number of clocks generated since the pattern generator was started. The clock begins counting at 0 and is reset when it reaches 9999. If you are using a 91S16 with your 91S32s, the clock cycle will not necessarily correspond to the sequence line being executed because of loops, jumps, and subroutine calls. Starting the pattern generator at some mid-point in the pattern will also cause a discrepancy between the CLOCK count and the SEQ line being displayed.

SEQ This heading shows the sequence number of the program line that has just been executed. It is the same sequence number that appears in the Run sub-menu. The SEQ heading may be ASEQ or RSEQ depending on how you set the SEQ field in the 91S32 Run sub-menu. By tracking the SEQ numbers, you can thoroughly monitor program flow.

#DC and #BA These headings display the pattern delivered to the P6464 probe tips. The number relates to the slot in the DAS where the 91S16 is installed, and the letter denotes the pod. An X (DON'T CARE) in this field indicates that at least one of the channels in that pod has been tri-stated (assuming display in Hex). The radix for this field can be changed by using the DISPLAY command while in the 91S32 Run sub-menu.

S The S (strobe) heading displays the status of the strobe lines. An X (DON'T CARE) in this field indicates that at least one of the strobe lines has been tri-stated. The radix for this field can be changed by using the DISPLAY command in the 91S32 Run sub-menu.

GPIB PROGRAMMING

In this section you will find:

- general information on using the GPIB to remotely load and run the 91S16 and 91S32 pattern generator modules.
- a brief description of the capabilities and limitations of using GPIB commands with the Option 02 GPIB and RS-232 interfaces, and with the Option 06 GPIB interface.
- information on how to use the Option 06 GPIB interface to stimulate static devices (Pattern Download For Static Devices).
- information on how to use the Option 06 GPIB interface to stimulate dynamic devices (Pattern Download For Dynamic Devices {Keep-Alive}).

GENERAL INFORMATION

The General Purpose Interface Bus (GPIB) interface provided with DAS 9100 Series Options 02 and 06 conforms to the specifications contained in the IEEE 488-1978, *Standard Digital Interface for Programmable Instrumentation.* This section describes GPIB operational elements only in relation to 91S16 and 91S32 Pattern Generator modules installed in the DAS.

You can operate 91S16 and 91S32 pattern generator modules in the DAS from a remote controller by using the IEEE 488 General Purpose Interface Bus (GPIB) or the RS-232 master/slave interface (using GPIB commands).

Remote operation requires that you write a program for your controller to operate the DAS. To write such a program, you need to be familiar with your controller before you attempt to use the information in this section. The DAS can operate as a talker or a listener, but not as a controller in a GPIB system.

This section assumes that you are familiar with the GPIB as implemented in DAS 9100 Series Logic Analyzers. Refer to the *Option 06: I/O Communication Interface Operator's Manual Addendum* (part of the *DAS 9100 Series Operator's Manual package).* The following documents may also be useful to you:

- *GPIB Application Support* (Tektronix Part Number 070-2307-00)
- *Standard Digital Interface for Programmable Instrumentation* (IEEE 488-1978 standard). This document is published by The Institute of Electrical and Electronics Engineers, Inc. 345 East 47 Street, New York, New York 10017.

CAPABILITIES AND LIMITATIONS WHEN USING GPIB TO CONTROL THE 91S16 AND 91S32

There are three methods of implementing remote operation of the 91S16 and 91S32 pattern generator modules using GPIB commands. All three methods allow you to use a controller to load the pattern generator's memory and start operation. However, the method of implementing the Pattern Download From Host feature (described in the *91S32 Configuration Sub-Menu When Used With 91S16* section of this addendum) depends on whether you are using the Option 02 GPIB interface, the Option 06 GPIB interface, or the RS-232 interface.

All three methods use GPIB commands, but only Option 06 GPIB has the HSPAT (High-Speed PATtern download) command which allows you to use the Keep-Alive feature. Keep-Alive allows you to reload one page of the 91S32's memory while the 91S16 continues to output vectors; without this feature, the pattern generator briefly stops outputting vectors while the 91S32 completes its reload operation. (When the pattern generator stops, the last vectors are frozen at the probe tips.)

GPIB PROGRAMMING USING THE OPTION 02 GBIP AND RS-232 INTERFACES

Instructions for using the Option 02 GPIB and RS-232 interfaces are provided in the *DAS 9100 Series Operator's Manual.* Refer to that manual for more information.

GPIB PROGRAMMING USING THE OPTION 06 GPIB INTERFACE

This section only describes the Option 06 HSPAT command for the 91S16 and 91S32 pattern generator modules. Refer to the *Option 06 I/O Communication Interface Addendum* to the *DAS 9100 Series Operator's Manual* for an explanation of the GPIB system and description of other GPIB commands.

HSPAT (High-Speed Pattern Generator) Command
(Option 06 only, GPIB only)

The HSPAT command loads the pattern generator's program and pattern directly into the 91S16 and 91S32 memory. This command is supported only by the GPIB interface.

NOTE

The HSPAT command used with the 91S16 and 91S32 Pattern Generator modules is not the same HSPAT command used with the 91P16/32 Pattern Generator modules.

HSPAT Command Format

The HSPAT command has two parts. The first part consists of the command header (HSPAT) and its arguments. This part of the command is discussed under the paragraphs titled *Command Header Structure.*

The second part of the HSPAT command consists of the binary end block containing the data to be loaded into the pattern generator. This part of the command is discussed under the paragraphs titled *Data Block Stucture.*

The command format is:

HSPAT <slot>,<start seq>,<total lines>(EOM)
@<data bytes>BC_{16}

The DAS screen is turned off during data transfer. The pattern generator will stop when the HSPAT command is executed, unless the pattern generator is running in Keep-Alive mode.

Command Header Structure

The command header and its arguments tell the DAS which slot should receive the data, the sequence line where the data should start, and the total number of sequence lines in this transfer. The command header format is:

HSPAT <slot>,<start seq>,<total lines>(EOM)

<slot> is an ASCII integer representing the slot number of the pattern generator module you wish to reload.

<start> is an ASCII integer representing the hardware address where your program begins loading. For the 91S16, this number must be between 1 and 1024; for the 91S32, this number must be between 1 and 2048.

<total lines> is and ASCII integer representing the total number of lines being downloaded in this transfer. For the 91S16, this number must be between 0 and 1023; for the 91S32, this number must be between 0 and 2047.

(EOM) is the end of message indicator. (EOM) is the EOI line asserted on the last byte of the command header if the terminator switch is set to EOI. Otherwise, (EOM) is the LF (line feed) character if the terminator switch is set to LF/EOI.

Data Block Structure

The second part of the HSPAT command specifies the data you are downloading into the pattern generator. Data is transferred using the end block format:

@<data bytes>BC_{16}

<data bytes> are a continuous stream of bytes representing the pattern generator program microcode and patterns. The modules installed determine which data bytes are sent and their order. The byte order is described below:

For the 91S16:

1st byte	vector for Pod A
2nd byte	vector for Pod B
3rd byte	microcode (byte 0)
4th byte	microcode (byte 1)
5th byte	microcode (byte 2)
6th byte	microcode (byte 3)

For the 91S32:

1st byte	vector for Pod A
2nd byte	vector for Pod B
3rd byte	vector for Pod C
4th byte	vector for Pod D
5th byte	inhibit/strobe

The BC_{16} is always the last byte in the data byte sequence. The BC_{16} can be followed by a semicolon (;) and any formatting character (LF, CR, or SP).

Cautions and Restrictions when using the HSPAT command

When you view a program downloaded into your pattern generator, data vectors, instructions, strobes, and inhibit data will be properly displayed in the pattern generator Program: Run sub-menu, but labels will not be correctly displayed. HSPAT uses hardware addresses instead of labels.

Programming the Interrupt Mode. Absolute memory addresses used by the GPIB command are affected by the interrupt handling mode you have selected in the 91S16 Setup: Probe sub-menu. You must select the desired interrupt mode using the DAS keyboard before beginning GPIB operation.

If you select "IRQ enabled, CALL <*label*> mode," you must structure your controller program to enter the first line of the interrupt service routine in hardware location 0. (When an interrupt arrives, the DAS will automatically look in the first memory location for the address of the service routine.) This means that the first sequence line of your program (SEQ 0) should be addressed to memory location 1, and each subsequent program line is addressed to the memory location one greater than the SEQ number.

If you have selected "IRQ disabled," or "IRQ enabled, IF IRQ mode," you should address the first sequence line of your program (SEQ 0) to memory location 0; the memory location and the SEQ number should match. See the Tables 3-2 and 3-3 for assistance in determining the proper memory address for the interrupt mode you have selected.

Programming the 91S16 Register Configuration. Instructions that use the 91S16 internal register are dependant on how you have configured the register in the 91S16 Configutation sub-menu. You must select the 91S16 internal register to be either two 8-bit registers named RA and RB, or one 16-bit register named R, before beginning GPIB operation.

Do not program LOAD R, OUT R, INCR R, or DECR R instructions unless you have selected the 91S16 internal register to be one 16-bit register called R. Conversely, do not program RA and RB instructions if the 91S16 register is configured to be R.

Programming the RETURN Instruction. Do not program the RETURN instruction unless you have set the 91S16 Setup: Probe sub-menu's IRQ field to CALL <*label*> mode.

Since HSPAT uses hardware addresses as Jump destinations, you can program any number of Jump instructions (without HSPAT, you are limited to 15 labels).

Correlating Menu Sequences and Hardware Locations

Since the HSPAT command loads your program directly into the 91S16/32 memory, you must use hardware locations to program memory. Tables 3-2 and 3-3 show the relationship between menu sequence and hardware location.

Table 3-2
MENU SEQUENCE AND HARDWARE LOCATION FOR 91S16

Menu Sequence		Hardware Location
IRQ enabled CALL <label>	IRQ disabled or IF IRQ	
reserved	0	0
0	1	1
1	2	2
2	3	3
3	4	4
.	.	.
.	.	.
.	.	.
1022	1023	1023

91S32 Sequence Number to Hardware Location Adjustments

When designing the files your controller will use to download data into the 91S32, you must take two factors into account. First, the 91S32 loads its memory from the bottom up, and the last sequence line is loaded into the very first memory location used. This factor becomes important when you are designating the hardware location for 91S32 data; especially if you downloading files shorter than 2047 sequence lines to 91S32s operating in Sequential mode, or 91S32s operating without a 91S16. Second, in Sequential and 91S32 Stand-Alone modes, certain combinations of the internal and external inhibit signals (programmed in the 91S16 Probe sub-menu) require you to invert the inhibit bit value you download.

Table 16 shows the relationship between sequence line and hardware location for 91S32s in both versions of Follows 91S16 mode, and when you are downloading a full block of 2047 sequence lines to 91S32s in Stand-Alone or Sequential modes.

If you are downloading fewer than 2047 sequence lines to 91S32s in Stand-Alone or Sequential modes, designating the correct hardware location for each sequence line is less intuitive. See the following paragraph, titled *Partial 91S32 Memory Reloads*, and Table 17.

Table 3-3
MENU SEQUENCE AND HARDWARE LOCATION FOR EACH 91S32

	Menu Sequence			Hardware Location
	FOLLOWS 91S16 Mode		SEQUENTIAL	
	IRQ enabled CALL <label>	IRQ disabled or IF IRQ		
Page A	reserved	0	2047	0
	0	1	0	1
	1	2	1	2
	2	3	2	3
	3	4	3	4
	.	.	.	.
	.	.	.	.
	.	.	.	.
	1022	1023	1022	1023
Page B	reserved	1024 (0)	1023	1024
	1023 (0)	1025 (1)	1024	1025
	1024 (1)	1026 (2)	1025	1026
	1025 (2)	1027 (3)	1026	1027
	1026 (3)	1028 (4)	1027	1028
	.	.	.	.
	.	.	.	.
	.	.	.	.
	2045 (1022)	2047 (1023)	2046 (END SEQ −1)	2047

Note: This example shows SEQUENTIAL mode when the END SEQ field is set to 2047.

Partial 91S32 Memory Reloads. When 91S32s in Stand-Alone or Sequential mode are reloaded with fewer than 2047 sequence lines, the hardware address for each sequence line is dependent on the value entered into the END SEQ field. You will need to enter the END SEQ value either by using key codes via the GPIB, or else by using the DAS keyboard while in the Program: Run sub-menu prior to downloading the vectors.

The 91S32 loads its memory from the bottom up, starting with hardware location 2047. In other words, the highest-numbered memory locations are always filled, but the lowest-numbered memory locations will only be filled if you are reloading the entire memory. See Table 3-4 for examples of how the sequence numbers are loaded into hardware for various sizes of partial reloads. Notice that the sequence line specified in the END SEQ field is loaded into the first available memory location.

Table 3-4
91S32s in Sequential and Stand Alone Modes
Menu Sequence to Hardware Location Map

END SEQ 2047		END SEQ 1999		END SEQ 7	
ASEQ	Hardware Location	ASEQ	Hardware Location	ASEQ	Hardware Location
2047	0	1999	48	7	2040
0	1	0	49	0	2041
1	2	1	50	1	2042
2	3	2	51	2	2043
3	4	3	52	3	2044
.	.	.	.	4	2045
.	.	.	.	5	2046
.	.	.	.	6	2047
2045	2046	1997	2046		
2046	2047	1998	2047		

The following equation shows you how to determine the hardware location for most sequence lines relative to any given END SEQ value. The equation for finding the correct hardware location for the sequence line specified in the END SEQ field follows. Note: This equation only applies if you are using 91S32s in Stand-Alone or Sequential modes.

Absolute hardware address = 2048 − END SEQ value + ASEQ address.

For example, to find the hardware address for sequence line 25 when you are downloading 100 sequence lines, you would first set the END SEQ field to 99 (100 sequences). Then, using the formula:

X = 2048 − 99 + 25
X = 1974

To find the hardware location for the sequence line designated in the END SEQ field, use the following formula:

END SEQ line hardware address = 2047 − END SEQ field value.

Note: You cannot change the END SEQ field value after you have downloaded the HSPAT command.

91S32 Sequential and Stand-Alone Mode Inhibit Bit Inversion. Certain combinations of the internal and external Inhibit bits (selected in the Probe sub-menu) require you to invert the downloaded internal inhibit value (i.e., program a binary 0 where you would otherwise program a binary 1). The following combinations of internal and extenal inhibit bits do **not** require any change:

DISABLE
INT 1 ONLY
EXT 0 ONLY
EXT 1 ONLY
INT 1 OR EXT 0
INT 1 OR EXT 1
INT 0 AND EXT 0
INT 0 AND EXT 1

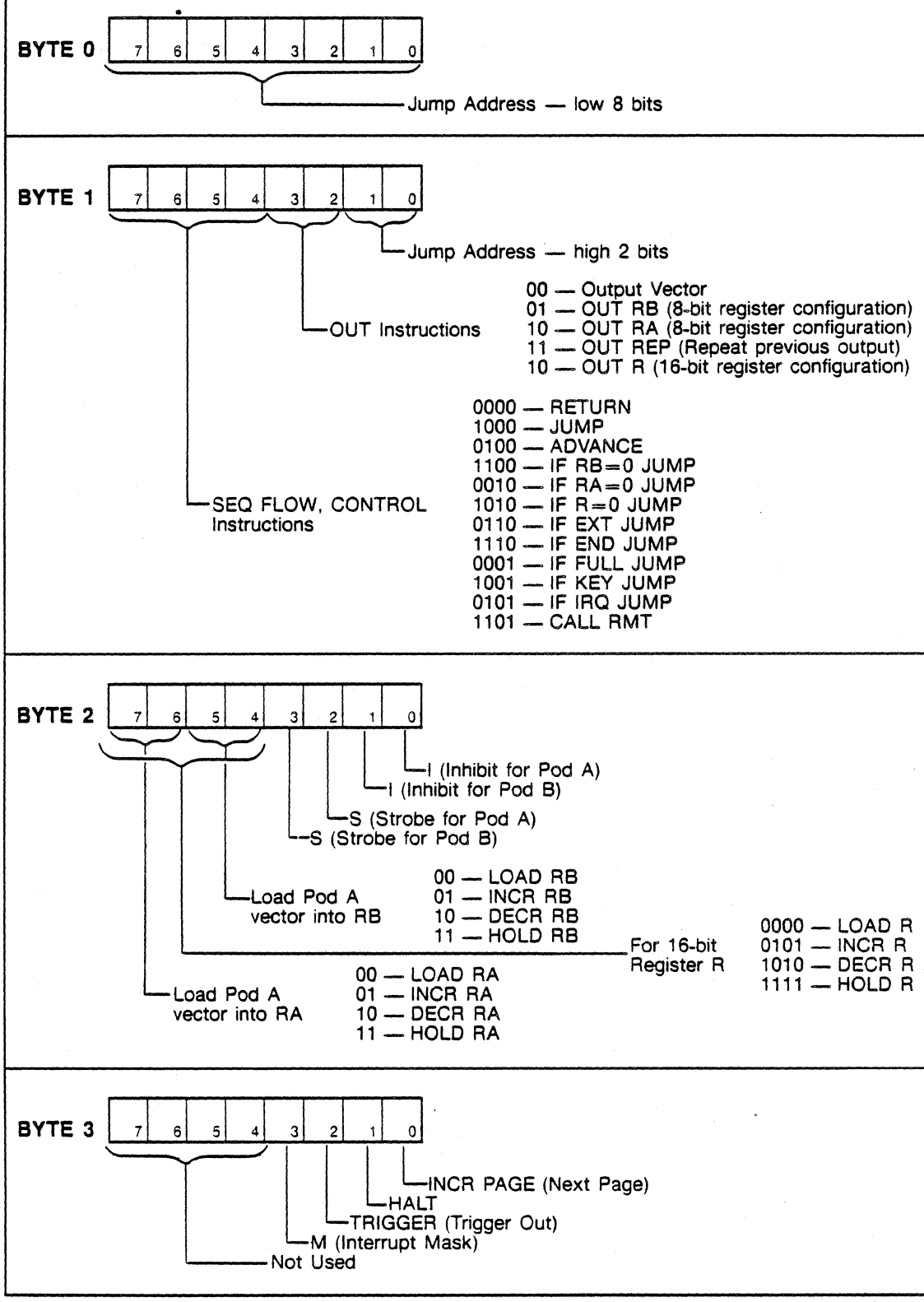
The following combinations of internal and external inhibits require you to invert the internal inhibit value inorder to obtain the expected results:

INT 0 ONLY
INT 0 OR EXT 0
INT 0 OR EXT 1
INT 1 AND EXT 0
INT 1 AND EXT 1

91S16 Microcode Bit Assignments. The 91S16 microcode bits are assigned as shown in Table 3-5.

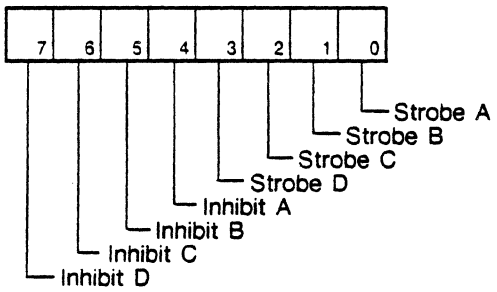
NOTE All bit values are given in binary.

Table 3-5: 91S16 Microcode Bit Assignment



91S32 Microcode Bit Assignments. Multiple 91S32s are addressed according to their bus slot location. Table 3-6 shows the 91S32 strobe and inhibit bit assignments.

Table 3-6: 91S32 Strobe/Inhibit Code Bit Assignment



Using the HSPAT Command

The HSPAT command loads the DAS hardware directly; it does not set up the Pattern Generator sub-menus. As a result, HSPAT does not show labels programmed in the 91S16 Program: Run sub-menu.

NOTE

Instructions containing labels in the 91S16 Program: Run sub-menu may contain invalid data after the HSPAT command has been executed.

You can use HSPAT when the 91S16 Setup: Probe sub-menu interrupt request (IRQ) field is set to either "CALL *<label>*" or "IF IRQ" mode, but you must remember that "CALL *<label>*" mode requires that you enter the first line of the interrupt service routine into the first hardware memory location.

PROGRAMMING THE PATTERN DOWNLOAD FROM HOST FEATURE

There are two versions of the Pattern Download From Host Feature: The version that stimulates static devices can be run with any standard combination of 91S16 and 91S32 modules. This version is called Pattern Download For Static Devices, and it does not support the Keep-Alive feature. Dynamic circuits that require constant clock and vector inputs even while the pattern generator module is being reloaded from the host computer require the Pattern Download For Dynamic Devices (Keep-Alive) version. A description of that version appears later in this section.

Pattern Download For Static Devices

When using Pattern Download For Static Devices, the pattern generator will alternately output a block of vectors, fix the last vector at the probe tips while it reloads the next block of vectors from the host computer, and then output the next block of vectors. No special fields need to be enabled in order to use Pattern Download For Static Devices.

If a 91S16 is used, you must program the HALT instruction on the last line of each 91S16 vector download.

HALT Instruction. When the 91S16 executes a HALT instruction, or the 91S32 completes its specified number of LOOPs, SRQ is asserted. The DAS then responds with status byte 66 (operation complete) when polled by the controller. Status byte 66 indicates that the pattern generator has halted with the last vector asserted at the probe tip. Execution may be resumed by downloading a new setup to the pattern generator and then sending a start command. New setups may be downlaoded by using either the PATGEN binary restore command or the HSPAT command.

NOTE

When using both acquisition and pattern generator modules, it is possible for status byte 66 to be generated twice (once for completion of acquisition and once for completion of pattern generation). If the controller polls the DAS after both of these operations have been completed, only one status byte 66 will be received.

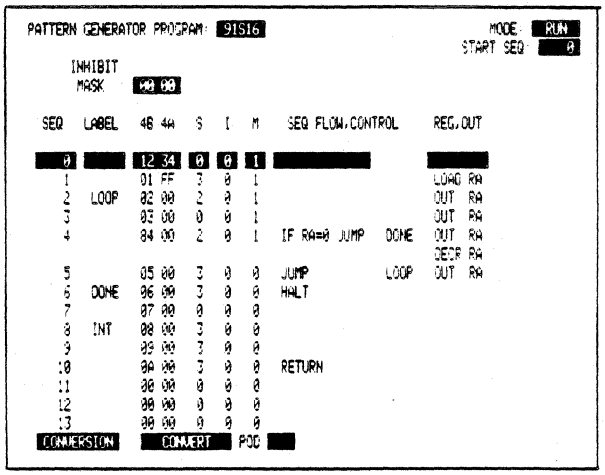
Example of Binary File that extablishes 91S16 Run sub-menu.

When downloaded, the following file (Table 3-7) results in the 91S16 Run sub-menu displayed at the right (Figure 3-21). The HSPAT command and its arguments are listed in the first line of the file. Note: The selected IRQ mode is CALL <*label*>; memory location 0 is loaded with the first line of the interrupt servicing routine.

Table 3-7. Binary file for Pattern Download For Static Devices.

SEQ	Hardware Location	Pattern Generator Program					
		HSPAT 4,0,12 (EOM)					
−1	0	@ 00	07	0A	80	F0	00
0	1	34	12	00	40	F0	08
1	2	FF	01	00	40	3C	08
2	3	00	02	00	48	F0	08
3	4	00	03	00	48	F0	08
4	5	00	84	07	28	B8	08
5	6	00	05	03	88	FC	00
6	7	00	06	00	40	FC	02
7	8	00	07	00	40	F0	00
8	9	00	08	00	40	FC	00
9	10	00	09	00	40	FC	00
10	11	00	0A	00	00	FC	00
		BC					

Begin, End Block	91S16 Data (Pod A)	91S16 Data (Pod B)	91S16 μCode (byte 0)	91S16 μCode (byte 1)	91S16 μCode (byte 2)	91S16 μCode (byte 3)



5397-28

Figure 3-21. 91S16 Program: Run sub-menu display after binary download.

Pattern Download For Dynamic Devices (Keep-Alive)

Pattern Download For Dynamic Devices (Keep-Alive) is only available if you are using DAS Option 06: I/O Interface (High Speed GPIB Programming). You must use a GPIB controller and the DAS GPIB interface. You must have a 91S16 and at least one 91S32 installed in the DAS.

When using Pattern Download For Dynamic Devices (Keep-Alive), the pattern generator outputs a page of vectors from both the 91S16 and the 91S32s. When the 91S16 reaches the bottom of its page, it enters a Keep-Alive subroutine that: 1) asserts the DAS SRQ line and informs the GPIB controller it is ready to receive a download (CALL RMT instruction), 2) executes the sequence lines contained within the Keep-Alive subroutine, thus continuing to output pattern to the circuit under test, and, 3) loops within the Keep-Alive subroutine until the controller sends a message that either the next page of vectors has been downloaded, or there are no more vectors to be downloaded. Upon receiving either of these instructions, the pattern generator exits the Keep-Alive routine and either instructs the 91S32s to begin executing the newly refilled memory page (implied INCR PAGE from IF FULL instruction), or else jumps to a specified shut-down routine (IF END instruction).

Description of Instructions:

CALL RMT When the CALL RMT (Call Remote device) instruction is executed, the DAS asserts the SRQ (service request) line and responds with status byte 197 when polled over the GPIB. Status byte 197 informs the controller that the pattern generator is ready for a download.

IF FULL JUMP When the 91S16 executes the IF FULL JUMP instruction it tests to see if the DAS has received KEY 46 from the controller. If KEY 46 has been received, the 91S16 instructs the 91S32s to change execution to the other memory page (implicit INCR PAGE), and begin execution on the sequence line containing the specified label. Initially, the pattern execution begins with Page A; the first successful IF FULL JUMP instruction transfers execution to Page B.

When constructing your controller program, you must send KEY 46 at the end of each complete download. If you are loading two 91S32 modules, the KEY 46 command should be sent only after both 91S32s have been loaded by HSPAT commands.

IF END JUMP When the 91S16 executes the IF END JUMP instruction it tests to see if the DAS has received KEY 47 from the controller. KEY 47 indicates that the controller has no more vectors to download to the 91S32s. Usually, the IF END JUMP instruction gives control to a routine that completes the pattern generation.

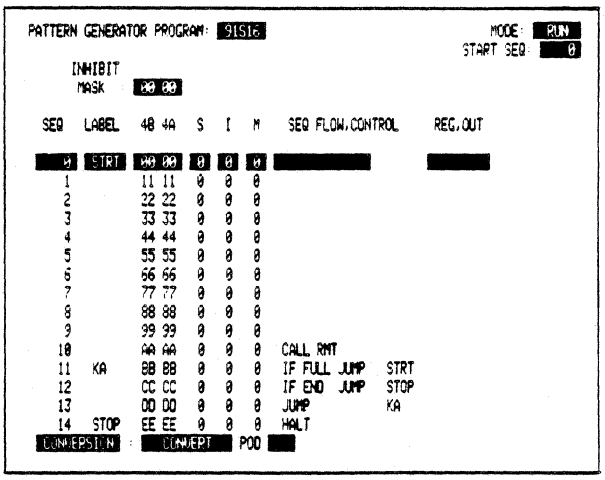
Example of a Binary File that establishes 91S16 Run sub-menu and Keep-Alive routine.

When downloaded, the following file results in the 91S16 Run sub-menu displayed at the right. Note: The selected IRQ mode is DISABLED so memory location 0 is loaded with SEQ 0 of the pattern generator program. Refer to Table 3-8 and Figure 3-22.

Table 3-8. Binary File for Pattern Download for Dynamic Devices.

SEQ	Hardware Location	Pattern Generator Program					
		HSPAT 4,0,15 (EOM)					
0	0	@ 00	00	00	40	F0	00
1	1	11	11	00	40	F0	00
2	2	22	22	00	40	F0	00
3	3	33	33	00	40	F0	00
4	4	44	44	00	40	F0	00
5	5	55	55	00	40	F0	00
6	6	66	66	00	40	F0	00
7	7	77	77	00	40	F0	00
8	8	88	88	00	40	F0	00
9	9	99	99	00	40	F0	00
10	10	AA	AA	00	D0	F0	00
11	11	BB	BB	00	10	F0	00
12	12	CC	CC	0E	E0	F0	00
13	13	DD	DD	0A	80	F0	00
14	14	EE	EE	00	40	F0	02
		BC					

Begin, End Block	91S16 Data (Pod A)	91S16 Data (Pod B)	91S16 µCode (byte 0)	91S16 µCode (byte 1)	91S16 µCode (byte 2)	91S16 µCode (byte 3)



5397-29

Figure 3-22. 91S16 Program: Run sub-menu display after binary download.

Debugging HSPAT Programs

There are two methods you can use to debug your HSPAT programs. The first is based on the Pattern Generator TRACE and STEP modes, and the second is based on acquiring the program into acquisition memory. TRACE mode is basically an automatic version of STEP mode, so the STEP mode description applys to both.

STEP Mode Method: The STEP mode method uses the Pattern Generator STEP mode to show you the vector sequences as they have been processed by your program. For example, if your program contains a loop, the STEP mode method allows you to single-step through the repeated sequences. To use the STEP mode method:

1. Press the PATTERN GENERATOR key to enter the Program: Run sub-menu. Move the screen cursor to the MODE field and press SELECT until STEP appears.
2. Download the HSPAT command and your program.
3. Press the START PAT GEN key to single-step through the vector sequences.

Acquisition Method: The acquisition method allows you to look at your vector data in the State Table display. As with STEP mode, the acquisition method shows you the vector data sequences as they have been processed by your program. Unlike STEP mode, the acquisition method allows you to see the vector data as a whole (not one sequence line at a time).

To use the acquisition method:

1. Connect your pattern generator module to an acquisition module with probes. Each pod used on the pattern generator must be connected to a pod on the acquisition module.
2. Download the HSPAT command and your progam.
3. Acquire the data with the acquisition module.
4. View the data in the State Table display.

SAMPLE GPIB CONTROLLER PROGRAMS

The following sample programs were written using a Tektronix 4050 Series graphic system as the GPIB system controller. Other controllers may require some program modification to work properly.

The sample programs use variable D1 as the talker/listener address for the DAS. You will need to enter this variable when you run the program. This variable needs to correspond to the setting you selected on the DAS address switch. The selected address is displayed at the top right corner of the Input Output menu.

Each program has a subroutine for handling Service Requests (SRQs). The program interrupts to this subroutine whenever SRQ is asserted.

NOTE

Some controllers can inadvertently Untalk the DAS by asynchronously responding to an SRQ from the DAS. For a discussion of this situation, see the Status Bytes, Error Codes, and Service Requests *section of the* Option 06 I/O Interface Operator's Addendum (Part of the DAS 9100 Series Operator's Manual package).

Modifying the Programs. If you need to modify these sample programs to run on your controller, not the following:

- The 4050 Series controller automatically asserts Remote Enable (REN) when these programs are run. You will need to include a statement that asserts REN in your program if your controller does not automatically do so.
- Table 12-42 of the Option 06 Operator's Addendum shows the traffic associated with the BASIC commands listed in the programming examples. This information may be useful to you if your controller functions differently from the 4050.

Sample Controller Program For Pattern Download For Static Devices

The example Pattern Download From Host for Static Devices program discussed in this section presupposes the following:

- A 91S16 (or 91S32) module is installed in slot 4.
- A properly formatted tape is currently mounted in the controller tape drive.
- If a 91S16 is used, the tape contains one or more files in binary end block format that specify vector data with a HALT instruction on the last sequence for the 91S16 module.
- If a 91S32 is used, the tape contains one or more files in binary end block format that specify vector data for a 91S32 module.

The following steps must be taken to program the example Pattern Download For Static Devices program:

1. Enter the 91S16 Setup: Probe sub-menu and set the IRQ field to IRQ enabled, CALL <1000>.
2. Enter the Setup: Timing sub-menu and set the clock rate.
3. Adapt the following controller program program to suit your needs. An example of a binary file that establishes the 91S16 Run sub-menu follows the program listing.

Overview of GPIB Controller Operation. The GPIB controller prompts the user for the DAS GPIB address, then waits for the DAS to assert an SRQ. When the proper SRQ is detected, the controller prompts the user for the number of the file containing data to be loaded into the first 91S32, issues the appropriate HSPAT command, and downloads that file. The controller continues to wait for SRQs (when the pattern generator executes a HALT instruction) and then performs file download routines until all files have been downloaded.

In order to use this feature, you must establish a GPIB controller program similar to that in Table 3-9. No special settings are required in the 91S16 or 91S32 sub-menus, but you must remember that hardware addresses are affected by the interrupt request mode selected. When using GPIB commands, the DAS cannot check for invalid entrys.

Table 3-9
Sample Pattern Download From Host Controller Program for Static Devices

Main Program

100 PRINT "Enter DAS address: "; 110 INPUT D1	1. Prompt the user for the DAS talker/listener address
120 ON SRQ THEN 2000	2. Establish the SRQ interrupt routine
130 GOSUB 1000	3. Load the pattern generator module
140 PRINT @D1:"START PGN"	4. Start the pattern generator
150 B1=0 160 IF B!<>66 AND B1<>82 THEN 160	5. Wait for the pattern generator to halt (operation complete: SRQ 66 or 82)
170 PRINT "Downlad more vectors? (Y or N): "; 180 INPUT Z$	6. Prompt the user for more vectors to download.
190 IF Z$<>"Y" THEN 220 200 GO TO 130	7. If the response is "Y," perform another download.
210 IF Z$<>N THEN 170 220 PRINT "DONE" 230 END	8. If the response is "N," report that the downloads are finished.

Table 3-9 (cont.)
Sample Pattern Download From Host Controller Program for Static Devices

Pattern Generator Load Routine

1000 PRINT "Loading vectors, enter file number: "; 1010 INPUT F1	1. Prompt use for tape file containing binary end block.
1020 FIND F1	2. Find file.
1030 PRINT @D1:"HSPAT 4,0,16"	3. Send HSPAT command header.
1040 WBYTE @D1+32:64	4. Designate the DAS as a listener.
1050 READ @33:B	5. Read binary data off tape byte-by-byte.
1060 WBYTE B	6. Relay it to the DAS.
1070 IF B=>0 THEN 1050	7. Final EOI sets 4050 Series sign bit negative.
1080 WBYTE @63:	8. Unlisten the DAS.
1090 RETURN	9. Return to load routine.

SRQ Handler Routine

2000 POLL A1,B1;D1	1. Poll the DAS
2010 IF B1=66 OR B1=82 THEN 2050	2. If the SRQ is an "operation complete" (a halt occurred), let it pass through and be handled by the main program.
2020 PRINT @D1:"ERRMSG?"	3. Otherwise, query the DAS for an error message.
2030 INPUT @D1:E$	4. Receive the error message from the DAS.
2040 PRINT "Status =",B1,E$	5. Print the status and error messages.
2050 RETURN	6. Return to main program.

Sample Controller Program for Pattern Download For Dynamic Devices (Keep-Alive)

The example Pattern Download For Dynamic Devices (Keep-Alive) program listed here presupposes the following:

- A 91S16 is installed in slot 4 and a 91S32 is installed in slot 5.
- A Properly formatted tape is currently mounted in the controller tape drive.
- The tape contains a file in binary end block format that specifies the vector data and Keep-Alive routine for the 91S16 module.
- The tape contains one or more files in binary end block format that specify vector data for a 91S32 module.

The following steps must be taken to enter the example Keep-Alive program listed below:

1. Enter the 91S32 Configuration sub-menu and select FOLLOW 91S16 mode. Set the MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) field to ON.
2. Enter the 91S16 Setup: Probe sub-menu and set the IRQ field to DISABLED.
3. Enter the Setup: Timing sub-menu and set to clock rate to 40 ns or greater.
4. Adapt the following controller program to suit your needs. A sample binary file that establishes the 91S16 Run sub-menu, including the Keep-Alive routine, follows the controller program.

Overview of GPIB Controller Operation. The GPIB controller prompts the user for the DAS GPIB address, then waits for the DAS to assert an SRQ. When the proper SRQ is detected, the controller prompts the user for the number of the file containing data to be loaded into the 91S16. The controller then issues the HSPAT command and downloads the contents of the file. It then prompts the user for the number of the file containing data for the first 91S32, issues the appropriate HSPAT command, and downloads that file. The controller continues to wait for SRQs and then perform file download routines until all files have been downloaded.

In order to use this feature you must establish a GPIB controller program similar to that in Table 3-10. No special settings are required in the 91S16 or 91S32 sub-menus, but you must remember that hardware addresses are affected by the interrupt request mode selected. When using GPIB commands, the DAS cannot check for invalid entrys; you must not program instructions that have been disabled.

Table 3-10
Sample Pattern Download For Dynamic Devices Controller Program (Keep-Alive)

Main Controller Program

100 PRINT "Enter DAS address: "; 110 INPUT D1	1. Prompt user for DAS talker/listener address
120 ON SRQ THEN 4000	2. Establishes SRQ interrupt routine
130 GOSUB 1000	3. Load 91S16
140 GOSUB 2000	4. Load 91S32
150 PRINT @D1:"START PGN" 160 B1=0	5. Start Pattern Generator
170 IF B1<>197 AND B1<>213 THEN 170	6. Wait for CALL RMT to occur
180 PRINT "Download more vectors? (Y or N): "; 190 INPUT Z$	7. Prompt the user for continuation of Keep-Alive
200 IF Z$<>"Y" THEN 270 210 GOSUB 2000 220 PRINT @D1:"KEY 46" 230 GO TO 160	8. If the response is "Y," send another page to the 91S32, issue "KEY 46" to indicate "FULL," wait for another "CALL RMT."
240 IF Z$<>"N" THEN 180 250 PRINT @D1:"KEY47"	9. If the response is "N," issue "KEY 47" to indicate "END."
260 PRINT "DONE" 270 END	10. Report when finished

91S16 Load Routine

1000 PRINT "Loading 91S16, enter file number: "; 1010 INPUT F1	1. Prompt user for tape file containing binary end block
1020 FIND F1	2. Find file
1030 PRINT @D1:"HSPAT 4,0,16"	3. Send HSPAT command header
1040 GOSUB 3000	4. Send binary end block to 91S16
1050 RETURN	5. Return to main program

Table 3-10 (cont.)
Sample Pattern Download For Dynamic Devices Controller Program (Keep-Alive)

91S32 Load Routine

2000 PRINT "Loading 91S32, enter file number: "; 2010 INPUT F1	1. Prompt for tape file containing binary end block
2020 FIND F1	2. Find file
2030 PRINT @D1:"HSPAT 5,0,16"	3. Send HSPAT command header
2040 GOSUB 3000	4. Send binary end block to 91S32
2050 RETURN	5. Return to either main program or to SRQ handler routine

Binary Transfer Routine

3000 WBYTE @D1+32:64	1. Designate the DAS as listener
3010 READ @33:B	2. Read binary data off tape byte-by-byte
3020 WBYTE B	3. Relay it to the DAS
3030 IF B=>0 THEN 3010	4. Final EOI sets 4050 Series' sign bit negative
3040 WBYTE @63:	5. "Unlisten" the DAS
3050 RETURN	6. Return to either 91S16 or 91S32 load routine

SRQ Handler Routine

4000 POLL A1,B1;D1	1. Poll the DAS for status
4010 IF B1=197 OR B1=213 THEN 4050	2. If the SRQ is a "CALL RMT," let it pass through and be handled by the main program.
4020 PRINT @D1:"ERMSG?"	3. Otherwise, query the DAS for the error message.
4030 INPUT @D1:E$	4. Receive error message from the DAS.
4040 PRINT "Status = ",B1,E$	5. Print status and error message
4050 RETURN	6. Return to main program.

ERROR AND PROMPTER MESSAGES:
Additions with the 91S16 and 91S32 Pattern Generator Modules

NOT A 91S16 POD	Appears in the 91S16 Program: Run sub-menu when you enter an invalid pod I.D. in the CONVERSION: CONVERT POD editing command. Check to see which DAS slot the 91S16 is installed in and enter the appropriate pod I.D.
NOT A 91S32 POD	Appears in the 91S32 Program: Run sub-menu when you enter an invalid pod I.D. in the CONVERSION: CONVERT POD editing command. Check to see which DAS slot the 91S16 is installed in and enter the appropriate pod I.D.
CALL UNAVAILABLE: **"IF IRQ" USED IN PROGRAM**	Appears in the 91S16 Setup: Probe sub-menu when you attempt to change the interrupt request (IRQ) mode. You must remove any IF IRQ JUMP *<label>* instructions from the Program: Run sub-menu before changing modes.
CALL UNAVAILABLE: **SEQ FLOW USED AT SEQ 1023**	Appears in the 91S16 Setup: Probe sub-menu when you attempt to change the interrupt request (IRQ) mode. CALL mode reserves the first memory location for the interrupt routine jump address; this reduces the number of available sequence lines from 1023 to 1022. You must remove any sequence flow (SEQ FLOW) instructions programmed in SEQ 1023 before selecting CALL mode.
"IF IRQ" UNAVAILABLE: **"RETURN" USED IN PROGRAM**	Appears in the 91S16 Setup: Probe sub-menu when you attempt to change the interrupt request (IRQ) mode. You must remove the RETURN instruction programmed in the 91S16 Program: Run sub-menu before selecting IF IRQ mode.
PROCESSING IRQ SETUP	Appears when you attempt to exit the Setup: Probe sub-menu after changing IRQ modes. This message will disappear when the processing is complete. No action is required.
"R" USED IN PROGRAM	Appears in the 91S16 Configuration sub-menu when you attempt to select two 8-bit internal registers named RA and RB. Remove any instructions pertaining to the 16-bit internal register named R from the Program: Run sub-menu before changing the configuration of the 91S16 internal register.

ERROR AND PROMPTER MESSAGES:
Additions with the 91S16 and 91S32 Pattern Generator Modules

"RA" OR "RB" USED IN PROGRAM	Appears in the 91S16 Configuration sub-menu when you attempt to select a single 16-bit internal register named R. Remove any instructions pertaining to the 8-bit registers named RA and RB from the Program: Run sub-menu before changing the configuration of the 91S16 internal register.
"IF FULL", "IF END", or "CALL RMT" USED IN PROGRAM	Appears in the 91S32 Configuration sub-menu when you select OFF in the MEMORY RELOAD FROM HOST (FOR KEEP-ALIVE) field. Remove any IF FULL, IF END, and CALL RMT instructions from the 91S16 Program: Run sub-menu before selecting OFF in this field.
PROCESSING END ASEQ SETUP	DAS is processing setup changes. No action required.
EDIT IN PROGRESS: <<<<<<<<	Appears in the Program: Run sub-menu whenever lengthy edit operations are in progress. Chevrons will disappear as the process continues. No action required.

Section 4
THEORY OF OPERATION

Section Organization

This section is designed to familiarize service personnel with the operation of the 91S16 and 91S32 circuitry. It is divided into five main subsections:

1. **91S16/91S32 System Architecture** describes how 91S16 and 91S32 modules fit into the DAS architecture.

2. **91S16 General Description** describes the 91S16 at the functional block level.

3. **91S32 General Description** describes the 91S32 at the functional block level.

4. **91S16 Detailed Circuit Description** describes 91S16 operation at the component level.

5. **91S32 Detailed Circuit Description** describes 91S32 operation at the component level.

Throughout this section, references are made to the 91S16 and 91S32 block diagrams and schematics located in the Diagrams section at the back of this addendum. The schematic and block diagram pages have tabs indicating the page title. Tabs on schematic pages include the numbered diamond assigned as the schematic number. Schematics are often referred to by the numbered diamond on the schematic tab.

For a more complete understanding of the 91S16 and 91S32 modules, you may also want to refer to the signal glossary in the Reference Information section and to the diagnostic information in the Maintenance: Troubleshooting section.

Logic Conventions

In this manual, digital logic is described using the positive convention. The more positive voltage indicates a true or 1 state; the more negative voltage indicates a false or 0 state. In logic descriptions, the more positive voltage is referred to as high, and the more negative voltage is referred to as low. The specific voltage that specifies a high or low state varies depending on the type of logic device. TTL, ECL, and CMOS devices all have different logic threshold levels.

Signal names on schematics are normally asserted high. Only signal names with overscores are asserted low. In this text, signals asserted high have the suffix (H); PAGA(H), for example. Those asserted low have the suffix (L), such as MWEM(L).

91S16/91S32 System Architecture

The 91S16 and 91S32 Pattern Generator Modules are designed to reside in any of the instrument bus slots (1 through 6) of any DAS 9100 mainframe. All 91S16 and 91S32 modules should be placed in adjacent bus slots. The mainframe must contain firmware version 1.11 or higher, along with the hardware changes associated with the firmware version. In particular, the 91S16 and 91S32 modules must be installed in DAS slots served by the new 22 amp 5 V power supply. More information on firmware version 1.11 is located in the Operating Instructions section of this addendum.

Both types of modules are initialized and read by the Controller board in the DAS mainframe. The firmware that allows the Controller board to operate is located on the 91S16 and 91S32 modules. The Trigger/Time Base board provides the clock to each module for synchronous operation. The only exception to this is when the 91S16 is operating as a controller for 91S32 modules, in which case the 91S16 supplies the clock to the 91S32s.

91S16 ALGORITHMIC PATTERN GENERATOR

The 91S16 is an algorithmic pattern generator providing 16 data output channels, two clock lines and two strobe lines. Strobes can be used as additional output channels. The master clock can be supplied either from the DAS internal clock or from an external device. Maximum clock rate is 50 MHz. Data output is normally synchronous with the master clock, but individual PODs (probes) can be programmed to output data ±5 ns relative to the master clock. Individual data and strobe lines within each POD can be programmed to output data an additional ±5 ns relative to their POD clock. Pattern memory is 1024 sequence lines (vectors) deep.

The 91S16 provides an internal 16-bit data register (or two 8-bit data registers) which can be used as counters or as an alternate source for pattern output. The 91S16 instruction set includes 9 instructions ranging from simple JUMP to label commands to IF Register = 0 JUMP to label. Fifteen different labels can be programmed, plus a special interrupt service routine.

Only one 91S16 can be installed in the DAS, however the 91S16 can be used as a controller for up to five 91S32s.

91S32 RAM-BASED PATTERN GENERATOR

The 91S32 is a RAM-based pattern generator providing 32 channels of data, four strobes, and four clock lines. In addition, the strobe lines can be used as extra data channels. Maximum clock speed is 50 MHz. Pattern depth for all channels is 2048 sequence lines (vectors). However, special features allow you to split

the memory into two 1024-line pages and reload alternate pages of memory while the pattern generator is outputting data (this requires a 91S16). The 91S32 can also be programmed to execute its program repeatedly.

The 91S32 usually executes its program in a sequential, beginning-to-end fashion. However, if you use the 91S32 in conjunction with a P6452 probe attached to the DAS Trigger/Time Base module, you can use inputs from that module to supply External Start, External Inhibit, and Pause signals. Data output is normally synchronous with the master clock's rising edge, but individual PODs can be adjusted ±10 ns relative to the master clock. Individual data and strobe lines can be adjusted an additional ±10 ns relative to their POD clock.

91S16 AS CONTROLLER FOR 91S32

One 91S16 can serve as a controller for up to five 91S32s. In this configuration, you can supply up to 16 data channels with a memory depth of 1024 lines, plus 160 data channels with a memory depth of 2048 lines. There are also 22 clock and 22 strobe lines available.

Also, this configuration provides all the branching instructions and interactive features available with the 91S16 in addition to the large number of data channels and pattern depth afforded by the 91S32s.

There are two different operating modes available when the 91S16 and 91S32 are used together. These modes are named Sequential mode and Follows mode.

Sequential Mode

This operating mode allows the 91S16 and 91S32 to operate simultaneously. The 91S16 will supply the clock signal to the 91S32. However, each card will execute its program independently. In other words, the 91S16 can be performing branching operations, but the 91S32s will continue to output their data in a straight sequential line-by-line manner. The 91S16 can be set to automatically restart from the beginning when it reaches the end of its memory. This will keep all data channels alive for as long as desired.

Follows Mode

This operating mode allows the 91S16 to have much more active control of the output of the 91S32s. The 91S32 will follow instructions programmed in the 91S16 that govern its sequence line execution.

In the Follows mode, the vector memory address register of the 91S16 acts as the vector memory address register for the 91S32s via an interconnect cable. This means that if the 91S16 executes a loop, the 91S32s will also loop.

The 91S16 also supplies the master clock to the 91S32 modules. Usually you would want the 91S16 and 91S32 to output data according to the same clock, but you can program the 91S32 to execute its program at one-half, or one-fourth the clock rate supplied by the 91S16 module.

In Follows mode, the memory of the 91S32 is divided into two 1024-line pages called Page A and Page B. The size of these pages matches the memory depth of the 91S16. The 91S16 has control over which memory page the 91S32 will execute. You can enter two different programs in the 91S32 (one in each page) and use the 91S16 to switch between the programs based on some signal sensed by the 91S16's P6460 External Control Probe.

One major feature provided by Follows mode is the automatic reload function. If your pattern generator program is very large, or if you have developed the program on a host computer, the entire program may be too large to fit into the 91S32's memory. Follows mode allows you to divide the 91S32's memory into two pages and reload one page while the other page is being executed. Instructions for communicating with the host computer or external storage device are programmed into the 91S16.

Keep-Alive

Down-loading a pattern from a host computer usually takes longer than executing the other memory page. This can cause a problem with dynamic circuit elements that require constant clock and vector inputs. The 91S16/32 combination provides a keep-alive function to supply the clock and a few vectors to keep the circuit under test active until the other memory page has been reloaded. Keep-alive is essentially a subroutine that you program into the 91S16. Static devices being tested so not require this feature.

91S16 General Description

In the following description, refer to the general block diagram for the 91S16 and the 91S32, located in the Diagrams section. The schematic numbers are included in the headings for your convenience.

The 91S16 circuitry is divided into the following functional blocks.

91S16 CONTROLLER INTERFACE AND ROMs <92>

The controller interface and ROMs block allows communication between the DAS Controller board and 91S16. Any block in the 91S16 general block diagram identified with an asterisk (*) uses the 91S16 controller interface.

The 91S16 contains three ROMs which are read by the DAS Controller board. Board identification, control codes, and pattern generator menu data are stored in these ROMs.

PATTERN GENERATION PROBES

There are two P6464 Pattern Generation probes used with the 91S16. They are attached at the back of the module to connectors labeled POD A and POD B. Each probe is capable of generating eight channels of data, one clock, and one strobe for either TTL or ECL logic systems. Programmable features include:

- o TTL or ECL output levels
- o output clock polarity
- o inhibit (respond to an internal or external inhibit signal)
- o data channel timing advance or delay relative to the POD clock

EXTERNAL CONTROL PROBE

The 91S16 can accept an optional P6460 Data Acquisition Probe used as an External Control Probe. This probe is attached at the back of the module to a connector labeled POD C. This probe accepts interrupt, inhibit, jump, and pause signals. This probe is an active device that converts unbalanced line signals into differential line signals for transmission to the 91S16 module.

PROBE INTERFACE <92> <94>

The probe interface establishes the serial probe communications link for the probes, the controller interface, and the status readback circuitry. This allows the DAS to read the vector being delivered by the pattern generator probe and also identifies which probe is attached to each connector (POD). The Probe interface also sets the proper threshold voltage for the probes.

PROBE RECEIVERS <93> <94> <99>

The probe receivers acquire differential ECL output from the acquisition and pattern generator probes and convert the signals to TTL levels.

START IN <93>

The external start signal enters the 91S16 via a phono jack on the back of the module. The 91S16 will start when:

- o the external trigger has been enabled in the 91S16 Setup Probe menu, and
- o a transition on the START IN line occurs while the STOP PG(H) signal is high.

CLOCK CONTROL <93>

Various pattern generator clock rates can be selected using either internal or external clock signals. The clock can be stopped by:

- o the PAUSE signal supplied by the P6460 probe,
- o the STOP PG(H) signal supplied by the DAS Trigger/Time Base module, and
- o the HALT(H) signal supplied by the microcode RAM

VECTOR AND MICROCODE MEMORY <96>

The vector memory is a 1K x 16 bit RAM. The microcode memory (micro-instruction memory) is a 1K x 28-bit RAM. Pattern generation is controlled by the output of the microcode memory.

Vector and Microcode Assignments

VB0 - VB15 vector
JA0 - JA9 jump address
MC0 output select
MC1 output select
MC2 inhibit A
MC3 inhibit B
MC4 strobe A
MC5 strobe B
MC6 PC control
MC7 PC control
MC8 PC control
MC9 PC control
MC10 RB control
MC11 RB control
MC12 RA control
MC13 RA control
MC14 next page (to the 91S32)
MC15 halt
MC16 trigger out
MC17 interrupt mask

PROGRAM COUNTER CONTROL MULTIPLEXER AND RESET <95>

The program counter control codes are interpreted by the multiplexer to determine the next address for the vector memory output and the microcode memory. The instruction decoder applies appropriate reset signals to the external signal latches and generates a signal used to control the 91S32.

START SETUP <94> <94>

The start setup circuitry establishes the initial signal conditions in preparation for the start procedure.

PROGRAM COUNTER AND STACK <95>

The program counter takes the output of the instruction multiplexer and applies the address to the vector memory and the microcode memory. The stack performs the same functions, except that after receiving an interrupt signal the stack stores a return address.

INTERRUPT LOGIC <94>

The interrupt logic circuit accepts the external interrupt signal, clocks it through a register, and applies the appropriate logic.

EXTERNAL SIGNAL LATCHES <94>

The external signal latches accept the external signals from the P6460 probe and hold them. After the appropriate instruction tests the appropriate bit in a latch, it is automatically reset by hardware.

91S32 TRANSCEIVER <93> <94> <96>

The 91S32 transceiver provides a clock and control logic for 91S32s operating in the Sequential or Follows mode with a 91S16 controller.

REGISTER CONTROL <97>

The 91S16 has two 8-bit internal registers (or one-16 bit register). The output of these registers is sent to the instruction multiplexer through the zero judging circuit and the pattern selector.

PATTERN SELECTOR <97>

The pattern selector determines the next output pattern. It selects the output pattern from any of three sources: the vector memory, the internal register, or the first latch before the clock (repeat previous vector).

FIRST LATCHES <97>

Values from the pattern selector and microcode RAM are clocked into the latches and held until the next value is clocked in.

CLOCK POSITIONING <98>

The POD clock may be delayed in 5 ns steps over a range of -5 to +5 ns. This provides the time difference between PODs.

OUTPUT LATCHES <98>

Values from the first latches are clocked into the output latches by the delayed POD clock and held until the next value is clocked in.

TRIGGER OUT <98>

The 91S16 can generate a TTL-level trigger signal supplied via a phono jack on the back of the instrument module.

CLOCK LINE <99>

Once the clock is selected, four distinct clock lines are provided for the system. Each clock line contains the appropriate delay lines to make the system work synchronously.

INHIBIT CONTROL <99>

The inhibit control circuitry selects either the programmed internal inhibit signal stored in the microcode memory or the external inhibit signal received from the P6460 probe. It can also perform appropriate logic operations between the internal inhibit and the external inhibit signals.

STATUS READBACK <100>

The status readback circuits take the data from the microcode memory, the program counter, and the first latches and performs appropriate logic operations. The information is divided into 8-bit words for transfer to the controller.

+3 VOLT POWER SUPPLY <98>

The +3 volt power supply is a switching current pump bootstrapped to +5 V. It powers the ECL terminating resistors.

91S32 System Synopsis

The 91S32 Pattern Generator Module resides in any of the instrument bus slots (slots 1 through 6) of a DAS 9100 Series Mainframe. The 91S32 module with its four pattern generator probes issues up to 2048 pattern vectors 32 bits wide, at sampling rates up to 50 MHz. In addition, each 91S32 provides four clock signals and four strobe signals. Strobe lines can be used as additional data lines.

The 91S32 has both a loop counter and a word depth counter (end sequence counter). You can use a single 91S32 Pattern Generator module, or combine up to six 91S32 modules for especially wide patterns. The 91S32 can also be controlled by a 91S16 pattern generator module.

A 91S16 used as a controller can accept up to five 91S32 expansion modules. Pattern generator modules must be in adjacent slots in the DAS with the 91S16 module on the end. Each additional 91S32 module supplies an additional 32 data channels, four clocks, and four strobes. When using the 91S16 as a controller, maximum clock speed is 25 MHz. Clock and Address signals are sent from the 91S16 to the 91S32s through a 40-wire flat cable attached to a card-edge connector on the top of each instrument module.

The 91S32 pattern output can be clocked in several different ways. When 91S32s are used without a 91S16 module, they can receive their master clock either from one of the DAS's internal clocks or from an external clock signal delivered through an external control probe attached to the DAS Trigger/Time Base module.

When a 91S16 is used to control the 91S32, the 91S32's clock is supplied by the 91S16 module. Usually, you will want the 91S32's clock to be the same as that for the 91S16, however you can also program the 91S32 to run at one-half or one-fourth the 91S16 clock rate.

A pattern is generated from the memory on each clock cycle. Pattern generation stops when the Trigger/Time Base module asserts the stop-pattern-generator signal.

91S32 General Description

The following description refers to the general block diagram located in the Diagrams section. Schematic numbers (<###>) where the functional blocks can be located are included.

91S32 CONTROLLER INTERFACE <101>

The controller interface provides a means of communication between the Controller Module and the 91S32. The interface stores information when written to and provides data for the Controller when called for. Any block in the 91S32 general block diagram identified with an asterisk (*) is used by the 91S32 controller Interface.

HIGH SPEED ADDRESS BUS BUFFER <103>

91S32 receives address, data, and clock signals from 91S16 Pattern Generator when the 91S32 Pattern Generator is in Follows mode. The 91S32 high-speed address bus buffer latches the address, data, and clock signals, and sends them to the address multiplexer block.

FREE-RUNNING ADDRESS COUNTER <103>

When no 91S16 is present, or when the 91S32 is operating in Sequential mode, the free-running address counter generates the internal vector address and increases the address each time the clock edge moves from low to high. This result is selected by the multiplexer and becomes the address for the pattern memory.

LOOP COUNTER <104>

The loop counter stops the free-running address counter if a loop value has been programmed.

PAGE CONTROLLER <103>

The page controller changes the page latch status between Page A and Page B.

CLOCK DISTRIBUTION <102>

The clock distribution circuit sends the clock to all other 91S32 functional blocks.

CLOCK DELAY <105>

The clock delay selects and adjusts the delayed clock timing value programmed in the Configuration menu or the Timing menu.

ADDRESS MULTIPLEXER <103>

The address multiplexer selects a buffered address from the 91S16 or from the internal address counter and sends the address to the vector memory.

RAM WRITE <104>

The RAM write circuitry determines which page of memory data is written to, and determines the ECL RAM write timing.

VECTOR RAM <107>

The vector RAM stores the data pattern. When the pattern generator is started, the vector RAM sends data to the output latches.

OUTPUT LATCHES AND DRIVER <107>

The output latches and driver circuit receives the data from the memory and sends it out to the P6464 probes.

DATA READBACK <106>

The data readback circuit receives the data pattern and sends it out to the microprocessor bus.

ADDRESS READBACK <103>

The address readback circuit receives the A-Page address and sends it out to the microprocessor bus.

PROBE INTERFACE <105>

The probe interface verifies probe attachments and sets the probe threshold voltages.

PATTERN GENERATION PROBES

There are four P6464 Pattern Generator probes used with the 91S32. These probes are attached to connectors labeled POD A through POD D on the back of the instrument module. Each probe is capable of generating eight data channels, one clock, and one strobe signal. The strobe channel can be used as an additional data channel. The probes can operate at TTL, ECL, or variable voltage levels.

+3 VOLT POWER SUPPLY <104>

The +3 volt power supply is a switching current pump bootstrapped to +5 V. It powers the ECL terminating resisters.

91S16 Detailed Circuit Description

OVERVIEW

Refer to the schematics in the Diagrams section of this manual while reading this detailed circuit description. The numbered diamonds on the schematic tabs in the Diagrams section are keyed to numbered diamonds in the detailed circuit descriptions.

Components are identified by a component designation preceded by an ECB assembly designation.

FUNCTIONAL BLOCKS

The 91S16 circuitry is divided into the following functional blocks:

91S16 Controller Interface and ROM---Schematic 92
Pattern Generator Probes
External Control Probe
Probe Interface----------Schematics 92 and 94
Probe Receivers---------- Schematics 93, 94, and 99
Start In----------Schematic 93
Clock Control----------Schematic 93
Vector and microcode Memory----------Schematic 96
PC Control Multiplexer and Reset-----Schematic 95
Program Counter and Stack----------Schematic 94
Start Setup----------Schematics 94 and 95
Interrupt Logic----------Schematic 94
External Signal latches----------Schematic 94
91S32 Transceiver----------Schematics 93, 94, and 96
Register Control----------Schematic 97
Pattern Selector----------Schematic 97
First Latches----------Schematic 97
Clock Positioning----------Schematic 98
Output Latches----------Schematic 98
Trigger Out----------Schematic 98
Clock Line----------Schematic 99
Inhibit Control----------Schematic 99
Status Readback----------Schematic 100
+3 Volt Power Supply----------Schematic 98

CIRCUIT DESCRIPTIONS

91S16 Controller Interface and ROM <92>

The 91S16 controller interface performs two major functions:

1. It takes data from the controller and sends it to appropriate registers by decoding the lowest four bits on the address bus and interpreting BWR(L), PORT(L), and BRD(L) from the controller.

2. It takes data from the module and writes it on the data bus.

Examples of read and write procedures follow.

READ PROCEDURE. The controller is reading the CARD ID. The address bus has 00H written in the three LSB positions. Simultaneously, PORT(L) and BRD(L) are asserted, which enables U112. U112 decodes the address, and U112-1 is asserted (L). U112-1 going low enables CARD ID register U132, putting data on the data bus.

WRITE PROCEDURE. The write procedure is similar, except that the BWR(L) and PORT(L) signals must be active to enable decoder U118.

See the following table for a listing of register links to the data bus through signal lines BWR(L), BRD(L), and PORT(L), and by hex address.

Hex Addr	BWR(L)	BRD(L)	PORT(L)	Control Line	Chip Affected	Schem. No.
XX00	H	L	L	CARD ID(L)	U132	92
XX00	L	H	L	MAP REG(L)	U116	92
XX01	H	L	L	RD ROM(L)	U108	92
XX01	L	H	L	THRESHOLD(L)	U320	94
XX02	H	L	L	DATA CLOCK	P6460,P6464	
XX02	L	H	L	PROBE R/W(L)	U130	92
XX03	H	L	L	STACK RESET(L)	U416-U420	95
XX03	L	H	L	PROBE DATA	U194	92
XX04	H	L	L	RDBACK GATE(L)	U960	100
XX04	L	H	L	RDBACK SEL(L)	U900	100
XX05	H	L	L	OUTPUT CLK	U134,U218	93
XX05	L	H	L	SEL RAM(L)	U502	96
XX06	H	L	L	RS CLK(L)	U134,U218	93
XX06	L	H	L	RAM WE(L)	U422	96
XX07	H	L	L	F-LATCH CLK(L)	U134,U302	99
XX08	L	H	L	SEL0(L)	U804	99
XX09	L	H	L	SEL1(L)	U806	99
XX0A	L	H	L	SEL2(L)	U808	99
XX0B	L	H	L	SEL3(L)	U810	99
XX0C	L	H	L	SEL4(L)	U812	99
XX0D	L	H	L	SEL5(L)	U814	99
XX0E	L	H	L	STEP CLK	U206	93
XX0F	L	H	L	PC RESET	U410-U414	95

The ROM resident on the 91S16 contains the Pattern Generator menu. There are three 256K-bit EPROMs on the 91S16. Register U116 selects which ROM is accessed by the Controller to control the Pattern Generator menu.

Probe Interface <92> <94>

The probe interface is functionally divided into two sections: probe-to-91S16 communication, and the probe threshold circuitry.

PROBE-TO-91S16 COMMUNICATION. The 91S16 can preset the status of a probe by sending data to the probe, and can detect it by reading data from the probe. To do this, the R/W bits in U130 are set low by writing to port PROBE R/W.

Write Mode. The lower three bits (bit 0-2) in U130 are sent low by writing to port PROBE R/W. This instructs the probe that the 91S16 is going to send the status. The 91S16 sends a status bit to the probe by writing to port PROBE W-DATA (U194). The 91S16 then reads to port DATA CLOCK. One bit of data is sent to the probe. This procedure is repeated as many times as required by the probes. U130 and U194 read/write status is as follows.

U130	POD	W or R	U194	POD
bit 0	A	W	bit 0	A
bit 1	B	W	bit 1	B
bit 2	C	W	bit 2	C
bit 4	A	R		
bit 5	B	R		
bit 6	C	R		

Read Mode. The upper three bits (bit 4-6) in U130 are sent low by writing to port PROBE R/W. This instructs the probe that the 91S16 is going to read the status. The 91S16 then reads to port DATA CLOCK. DATA CLOCK is repeated eight times. Each time, a new status bit is read from each of the three probes. This procedure is repeated each time the status of the probes is required.

PROBE THRESHOLD CIRCUITRY. Digital-to-analog converter (DAC) U320 has level-setting information written to it by the 91S16 controller interface. The threshold voltage required in the probe is selected by writing to port THRESHOLD(L). The selected voltage then appears at U320-18. The first stage of this circuit takes the error voltage generated by the user ground and adds it to the selected threshold voltage. The next stage of this circuit does two functions:

1. The error of the offset sense voltage is subtracted from the selected threshold voltage.

2. This stage also attenuates the threshold voltage by a feedback resistor located in the probe and connected between the threshold voltage line and the threshold sense line.

NOTE

This circuit cannot adjust unless DAC U320 (an NE5018) is lot date number 8335 or smaller.

Probe Receivers <93> <94> <99>

The probe receiver acquires the differential ECL output of the acquisition probe. The resistors attached to these lines are line terminators to match the impedance of the transmission line. Each line is run through a delay line and a polarity selector. The delay line allows the selected clock sufficient time to set up before clocking data into each latch. The polarity selector can select a high or low level, or a rising or falling edge for each line.

Start In <93>

The START IN signal, which is received via a phono connector, is converted from TTL level to ECL level through resistors R272, R274 and R276. U222A is a buffer. Trigger polarity to U704B determines whether the system start will occur on the rising or falling edge of the external start signal. When START IN is disabled, U212A-5 is usually low and U212A-4 is high. The start/stop of the 91S16 is controlled by the STOP PG(H) signal received through the DAS interconnect board.

When the 91S16 selects the SYSTEM START given by an external signal, U212A-2 is programmed high in the setup program before the system starts. Once the START SYSTEM key or START PAT GEN key is pressed, the STOP PG(L) signal goes low. Then the 91S16 can accept an external start signal. The 91S16 may start by the selected transition of this line. Resistors R282, R284, and R286 on the STOP PG line convert the signal from TTL level to ECL level. U302A is a buffer and U222D is a gate that controls the STOP PG(L) signal.

Clock Control <93>

The clocks selected by U206 are 91A32 INTL CLK(L), 91A08 INTL CLK(L), EXT CLK(H), EXT CLK(L), and STEP CLK(L). The output of U206-15 is sent to the pause circuit and the stop circuit through buffer U640C. The 91S16 may start when both the U212-2 (START IN) and the U302-3 (STOP PG) are low. The external PAUSE signal line is wire-ORed with the START IN and STOP PG line. When the PAUSE line becomes high, U208 stops supplying a clock to the stop circuit. U638B prevents extra clock pulses.

If the PAUSE signal is low, U208 clocks through it on the rising edge of the selected clock pulse. U216B generates a clock pulse the same pulse width as the selected clock. U208-3 makes a rising-edge clock pulse by setting U216B. The output of U208-14 is a reset pulse to make the duty cycle of the clock 50% by resetting U216B. U208-3 goes low whenever the PAUSE signal, the START IN signal, or the STOP PG signal is high. The output of U638B-3, which is wire ORed with the PAUSE signal, stops the clock to prevent extra clock pulses.

The output of register U216B is supplied to U214. Register U214 produces the halt state from the microcode instruction. Register U214 clocks the HALT(H) line on the rising edge of the selected clock. When the HALT(H) line is high, the output of U214-3 goes low and the selected clock is not transferred through register U214 to buffer U218. The output of U214-14 is a reset pulse which establishes the duty cycle of the clock pulse. Comparator U956B converts the HALT(H) signal from ECL to TTL and sends the status to the 91S16 controller interface. Clock lines are provided for the system by buffer U218 as follows.

U218-9	Reference clock (TP280)
U218-15	91S32 clock 0(L)
U218-11	Program Counter
U218-14	RESET CLK(L)
U218-6	Output clock path
U218-3	OUT CLK(L)
U218-5	R CLK
U218-2	Not Connected

Comparator U212B checks whether a clock is supplied to the system in the Trace mode.

Vector and Microcode Memory <96>

The output vector is loaded in vector RAM U504-U510. The vector is stored in a 16-by-1024 bit format. The microcode is loaded in the microcode RAM U512-U524, then recalled for decoding into instructions. The microcode is stored in a 28-by-1024 bit format. This memory is loaded from the data bus through buffer U500 with eight bits set. Resistor network R560, R562, R564, and R566 convert the data from TTL to ECL. The address being loaded is loaded directly or through buffers U530 and U532 by the program counter U410-U414. The memory being loaded is set by register U502. RAM content and microcode decoding are shown in the following tables.

Reg.(U502)	D7	D6	D5	D4	D3	D2	D1	D0
2#X1111110	VB7	VB6	VB5	VB4	VB3	VB2	VB1	VB0
2#X1111101	VB15	VB14	VB13	VB12	VB11	VB10	VB9	VB8
2#X1111011	JA7	JA6	JA5	JA4	JA3	JA2	JA1	JA0
2#X1110111	-	-	-	-	MC1	MC0	JA9	JA8
2#X1101111	MC9	MC8	MC7	MC6	-	-	-	-
2#X1011111	MC13	MC12	MC11	MC10	MC5	MC4	MC3	MC2
2#X0111111	-	-	-	-	MC17	MC16	MC15	MC14

MICROCODE DECODING

VMB Schematic 92
VB0 - VB15 VECTOR
JA0 - JA9 JUMP ADDRESS
JAB Schematic 92

MC0-MC1 Output selector

MC0	MC1	INSTRUCTION	
2 8 BIT	1 16 BIT		
0	0	OUT VECTOR	OUT VECTOR
1	0	OUT RA	OUT REGISTER
0	1	OUT RB	Prohibit
1	1	OUT REPEAT	OUT REPEAT & VECTOR

MC2	Inhibit A
MC3	Inhibit B
MC4	Strobe A
MC5	Strobe B

MC6-MC9 Program flow control

MC9	MC8	MC7	MC6	INSTRUCTION
0	0	0	0	RETURN
1	0	0	0	JUMP
0	1	0	0	ADVANCE
1	1	0	0	IF RB(L)=0
0	0	1	0	IF RA(L)=0
1	0	1	0	IF R(L)=0
0	1	1	0	IF EXT J(L)
1	1	1	0	IF END(L)
0	0	0	1	IF FULL(L)
1	0	0	1	IF KEY(L)
0	1	0	1	IF IRQ(L)
1	1	0	1	CALL REMOTE

MC10-MC11 Reg. B control

MC11	MC10	
0	0	LOAD VECTOR INTO RB
0	1	INCREMENT RB
1	0	DECREMENT RB
1	1	HOLD RB

MC12-MC13 Reg. A control

MC13	MC12	
0	0	LOAD VECTOR INTO RA
0	1	INCREMENT RA
1	0	DECREMENT RA
1	1	HOLD RA

MC14	Next Page
MC15	Halt
MC16	Trigger OUT
MC17	Interrupt mask

Program Counter (PC) Control Multiplexer and Reset <95>

Microcodes MC6-MC9 are interpreted by the multiplexer to determine the next address for the vector memory and the microcode memory. Instructions controlled by microcode MC6-MC9 are ADVANCE, JUMP, RETURN, IF R=0, IF RA=0, IF RB=0, IF IRQ, IF KEY, IF EXT J and IF LOAD.

If microcode MC6-MC9 are all zero, both U432-2 and U406-8 are low. This specifies that the PC may load the output of the stack (Return Address) through multiplexers U400, U402 and U404. Microcodes MC6, MC8, and MC9 also are interpreted by the decoder U408 to generate the reset signals FULL(L), KEY(L), IRQ(L), and the 91S32 control signal KA(L). The output (L) of U814 makes the external signal latches go to the initial state after these instructions are executed.

Program Counter and Stack <95>

The output of U406-8 controls the program counter U410-U414 and stack U416-U420. When U406-8 is high, the program counter and stack are counted up on the positive going edge of PC CLOCK(H). When it is low, they may load a 10-bit jump address from microcode memory on the positive-going edge of the clock.

When the 91S16 accepts the external interrupt signal in the IRQ CALL mode, the interrupt logic applies an interrupt pulse to the reset pin 12 of program counter (PC) U410, U412, and U414. The PC accepts an interrupt pulse on the positive going edge of a clock. The address of the PC output for the vector and microcode memory is 00H. Then, the first line of an interrupt subroutine is written at address 00H. U414-14 is usually high. But when the 91S16 receives an interrupt, U414-14 goes to LOW and sets the stack to a holding state through U316C (schematic 94).

When accepting an interrupt, the stack clocks according to the output of U406-6. After the interrupt is accepted, the stack goes to the holding state, and does not obey the output of U406, until the microcode memory provides a RETURN instruction . The RETURN instruction terminates the holding state, and U414-14 goes high.

Start Setup <94> <95>

U314A is used when the 91S16 starts from SEQUENCE 0. A clock is sent to all circuits, but the PC, stack, and internal registers A and B work from a second clock. Before the pattern generator starts, U314A is set by the controller not to send a first clock to those registers. U314A is reset by the clock and provides a half cycle delay after the 91S16 starts. An interrupt signal is disabled by U314B when the 91S16 is in a halt state. When the 91S16 stops, the HALT(H) signal is clocked through resister U314B and the QUALIFY(H) line is set low. This inhibits register U308 from again passing an interrupt signal.

Interrupt Logic <94>

The interrupt logic accepts the external interrupt signal, clocks it through a register, and applies a reset pulse to the program counter. The interrupt logic accepts two external signals, QUALIFY(H) and INTERRUPT(H). Receiver U300A and B acquires the differential ECL output of the acquisition probes. U200A establishes a logic level to qualify the acquisition of the interrupt signal. U200D determines the positive-going or negative-going edge of the interrupt signal to be accepted by the interrupt logic.

U820A is the gate of the QUALIFY(H) signal. When the 91S16 is in a halt state, U314-14 is low and the interrupt logic does not acquire an interrupt signal. U324A controls whether QUALIFY is enabled or disabled. The enabled QUALIFY means that an acceptance of the interrupt signal may be qualified by the external signal. The disabled QUALIFY means that the interrupt logic may usually acquire an interrupt signal. When a qualify line is programmed with an interrupt mask (MC17), gate U332C goes low.

U308 is the first latch for an interrupt. A qualify signal enters U308-7,10 and an interrupt signal enters U308-9. If U308 acquires an interrupt signal when the qualify line is high, both U308-2 and U308-15 may go high. U308-15 is the output for the IF IRQ instruction. The INT(H) signal is clocked through register U306A. The high output of U306A-2 resets program counter U410-U414 as an interrupt, and U414-15 goes low. The output of U414-14 resets latch U308A through buffers U316A and U316C.

The output of U414-14 is also sent to U306B as a clock through gate U316C and generates the STACK HOLD SIGNAL(H) signal. This also resets register U306A. The output at U306-2 goes low and produces an interrupt pulse. Latch U308 can receive the next interrupt signal. Register U306-14 goes low, allowing U310A to accept a RETURN signal. When a RETURN instruction is executed, the RETURN(H) signal is clocked through register U310A and resets register U306B. The output of U306-14 resets U310A. Then U310A-2 produces a reset pulse for the stack holding circuit. The stack

is released from the holding state and again works the same as the program counter. The MPU resets the PC athrough U802A.

External Signal Latches <94> <95>

IF EXT J. U200C (Schematic 93) selects a logic level for the IF EXTJ instruction. The EXT(H) signal is clocked through register U212B on the positive-going edge of the clock and is applied to instruction multiplexer U406.

INTERRUPT MASK(MC17). When the INT MSK(H) signal (an interrupt mask from microcode RAM) is clocked through register U330A and sent to gate U332C, latch U308A cannot accept an interrupt signal for the duration of one cycle.

IF IRQ. The IRQ(H) signal, which is acquired when the qualify signal is high, is clocked through register U310B. The output of U310-14 is sent to register U330B through buffer U302 and the multiplexer U406. Register U310B holds an IRQ signal until the IRQ instruction is performed. The IF IRQ(L) signal is wire ORed with IRQ RESET(L) (the output of U408-11). When both IF IRQ(L) and IRQ RESET(L) are low, the IF IRQ instruction is executed, U330B generates a reset pulse and sends it to registers U310B and U308. U310B and U308B are cleared via gate U332D by the controller when a START key is pressed.

IF KEY. The input of U312-10 is low and U312-15 is high. When U312-11 receives a key clock from the controller, the output of U312-15 goes low and is clocked to the multiplexer U406 via U232B. The IF KEY(L) signal through buffer U302 is wire-ORed with the KEY RESET(L) signal. When both IF KEY(L) and KEY RESET(L) are low (which mean this instruction is executed), U304A generates a reset pulse and both U312-15 and U232-15 go high.

IF FULL. The IF FULL logic is almost identical with the IF KEY procedure. But the signals which are wire-ORed are the IF FULL(L) and FULL RESET(L) signals, and are sent to the 91S32 module through driver U230A. U304BA produces a reset pulse and resets register U216A also. All registers used in IF KEY and IF FULL are reset by the controller through gates U332A and B.

CALL REMOTE. The KEEP-ALIVE(L) signal, which is given by decoder U408-10, is clocked through register U216A and is converted from ECL to TTL by U956A. This signal specifies that the 91S16 and 91S32 may enter into the keep alive mode.

IF END. This instruction is used in the keep-alive mode. When the controller receives the end-of-message terminator through GPIB or RS232C, the controller signals the 91S16 by way of U334A, and the 91S16 goes out of the keep-alive mode.

Register Control <97>

The 91S16 has two 8-bit counters or one 16-bit counter, either of which can count up, count down, hold, and preset. This is controlled by microcode. When the input of U638-5 is low, this circuit can operate as two 8-bit counters. When U638-5 is high, it can operate as one 16-bit counter. Register A consists of U600 and U602. Register B is U604 and U606. When the S1 and S2 of each counter are simultaneously low, these counters may load the vector. The following list shows the modes controlled by S1 and S2.

S1	S2	Operating mode
L	L	Load vector
L	H	Count up
H	L	Count down
H	H	Hold

When the 8-bit counter mode is selected, Both register A and register B may load VB0-VB7 on the positive-going edge of REG CLK(H). In the 16-bit counter mode, register A loads VB0-VB7 and register B loads VB8-VB15 through multiplexers U608 and U610. U640B is used as the start setup gate to start at an initial state. The output of registers A and B are sent to the zero-judging circuit. The zero-judging circuitry checks whether the outputs of the registers are all low. The zero-judging circuit consists of gates U626, U628, and U640A. The zero-judging outputs are sent to the instruction multiplexer.

91S32 Transceiver <93> <94> <96>

The controller can select the master-slave mode between the 91S16 and the 91S32. The outputs of PC are sent to the 91S32 through drivers U426, U428, and U430. The following signals are sent to the 91S32.

Signal Name	Driver	Schematic
91S32 Clock	U230C	93
Output of PC U426	U428 and U430	96
Next Page	U430A	96
FULL	U230A	94
EXT INHIBIT	U430C	99

The NEXT PAGE(H) signal, provided from microcode RAM U524-22, tells the 91S32 to change a page. The FULL(H) signal, from pin 2 of register U312, tells the 91S32 to exchange the memory bank. It is asserted when the controller sets the output of register U312B-15 low and the IF FULL instruction is executed. See the External Signal Latches description which appears earlier in this discussion.

The EXT INHIBIT(H) signal is sent as an external inhibit signal to the 91S32. The polarity of the external inhibit signal is selected by U800A. The 91S32 clock has three clock types which are divided by 1, 2, or 4 (Schematic 93). A reset pulse is sent to U250-4 and U250-12 to insure proper phase of clocks at U230C pins 14 and 15. U250A makes a 1/2 clock and U250B makes a 1/4 clock. Clock division coding is shown in the following table.

U218-13	U250-13	U422-13	Clock Division
L	H	H	1/1 clock
H	H	L	1/2 clock
H	L	H	1/4 clock

Pattern Selector <97>

The pattern selector determines which pattern is generated at POD A and POD B. The pattern output is selected from the vector memory, register, or the output of the first latch by microcode. U616 through U622 select the pattern generated at POD A. U612 and U614 select the pattern generated at POD B.

The pattern generated at POD A is selected by microcode. When the 91S16 selects two 8-bit registers, the pattern generated at POD B is VB8-VB15 because the output of U316-14 is high. When both MC0(H) and MC1(H) are high, the pattern generated at POD A is selected at the output of the first latches. See the following tables for microcode pattern selection.

8 bit register mode
Microcode Pattern Out

MC0(H)	MC1(H)	POD A	POD B
L	L	VB0-VB	VB8-VB15
L	H	Output of Reg. A	VB8-VB15
H	L	Output of Reg. B	VB8-VB15
H	H	Output of latch	VB8-VB15

When one 16-bit register is selected, the output of U316-14 goes low , and multiplexers U612 and U614 are controlled by the output of U224-12.

16 bit register mode, Microcode Pattern Out

MC0(H)	MC1(H)	POD A	POD B
L	L	VB0-VB7	VB8-VB15
L	H	Output of Reg. A	Output of Reg. B
H	L	Prohibit	Prohibit
H	H	Output of latch	VB8 - VB15

U532A and U532F are used when the controller reads the output of the register in the trace mode.

First Latches <97>

The first latches (U632, U634, and U636) act as registers, clocking through the value from the output selector. This adjusts the data channel skew for making POD clock edge positioning. While pins 4 and 13 of U630 are high, the internal INHIBIT instruction is disabled.

Clock Positioning <98>

Each POD clock may be positioned in a -5 ns to +5 ns range in 5 ns steps. Each delay line DL760, DL780, introduces 5 ns

delay, including the gate delay. The POD clock is sent to the probe through the drivers U714A and U714B, and is provided to the registers through buffer U700 or U702. Clock positioning is shown in the following table.

POD A DLA0(L), DLA1(L), DLA2(L) Delay Time

POD B	DLB0(L)	DLB1(L)	DLB2(L)
L	H	H	-5 ns
H	L	H	0 ns
H	H	L	+5 ns
H	H	H	No output

CLOCK SENSE. In the trace mode, the clock sense circuit checks whether a clock is provided to the last latch or the probes. The output of U702-15 is sent to flip-flop U716A-6 (Schematic 93). If U716A receives a clock, the level at U716-2 (Schematic 93) is changed. The controller reads it via comparator U954B.

Output Latches <98>

The output latches operate as a register, clocking through vectors from the first latch by each POD clock. The outputs of registers U706 through U712 are sent through connectors to the pattern generator probes with the differential ECL output while the OUT LATCH CLK line is low.

Trigger Out <98>

U716B clocks through microcode MC16(H) from the microcode RAM. The output of U716-15 is converted from ECL to TTL by transistors Q720 and Q722 and is sent to phono connector J180 through buffers U222B and C.

Clock Line <99>

Delays inserted into each line allow the selected clock sufficient time to be set up before clocking the vector and microcode into each register. DL820 is the delay line adjusting the delay time to the output system. The delay time to the first latch is adjusted by DL800. The F LATCH CLK(H) signal is a step clock from address decoder U112 (Schematic 92) to the first latch (U630A). This clock is used when the controller reads the contents of memory. The delay time to the output latch is adjusted by DL700 (Schematic 98).

Inhibit Control <99>

U820B and U820D turn the external inhibit on or off. The outputs of gates U820B and U820D are wire-ORed with the internal inhibit line. An internal inhibit accepts the logical AND/OR with the external inhibit line by setting the exclusive-OR gates U800A, U800D, U224B and U224C (Schematic 96). An inhibit signal is sent to the probe through the exclusive-OR gate. Each channel in the probe can be inhibited (tristate) by ANDing it with a probe inhibit control. An internal inhibit is disabled by U630 (Schematic 97). See the following list for inhibit function coding.

<96> U224-5,7	<99> U800-5,14	<99> U800-9	<99> U820-6,12	<97> U630-4,13	Inhibit Function
L	L	L	L	H	Disable
H	L	X	L	L	Internal 0 only
L	L	X	L	L	Internal 1 only
X	L	H	H	H	External 0 only
X	L	L	H	H	External 1 only
H	L	H	H	L	Int 0 or Ext 0
H	L	L	H	L	Int 0 or Ext 1
L	L	H	H	L	Int 1 or Ext 0
L	L	L	H	L	Int 1 or Ext 1
L	H	L	H	L	Int 0 and Ext 0
L	H	H	H	L	Int 0 and Ext 1
H	H	L	H	L	Int 1 and Ext 0
H	H	H	H	L	Int 1 and Ext 1

Status Readback <100>

This circuit divides the data from the system into 8-bit words for transfer to the controller. Comparators U902 through U958 convert data from ECL level to TTL level. Register U900 determines which 8-bit information is read. Resistor arrays R940 and R942 establish the ECL threshold level. The following tables show status readback position and readback information.

Readback Position

* Vector, Strobe, Inhibit

```
Vector          First Output
Memory  --->    Latch ---> Latch
   |
   --> Comparator --> Controller
```

* JA0-JA9, MC0-MC1, MC6-MC17

```
Microcode     Gates or
memory  --->  Latches
  |
  --> Comparator --> Controller
```

Readback Information <100>

PORT Content Read Infomation

READBACK SEL Bit (16#04)	7	6	5	4	3	2	1	0
01	VB7	VB6	VB5	VB4	VB3	VB2	VB1	VB0
02	VB15	VB14	VB13	VB12	VB11	VB10	VB9	VB8
04	JA7	JA6	JA5	JA4	JA3	JA2	JA1	JA0
08	MC9	MC8	MC7	MC6	MC1	MC0	JA9	JA8
10	MC13	MC12	MC11	MC10	MC5	MC4	MC3	MC2
20	-	-	IBO	IAO	MC17	MC16	MC15	MC14
40	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
80	-	-	-	-	-	A/J	PC9	PC8
When 16#05 = 2#1XXXXXXX								
00	-	-	-	-	C.O.	Halt	Clk	K.A.

IBO : Internal Inhibit Output at POD B
IAO : Internal Inhibit Output at POD A
C.O. : COUNT OVER (The PC out is out of range)
Clk : Check a clock
K.A. : go to a Keep Alive
A/J : Advance/Jump

+3 Volt Power Supply <98>

The +3 volt power supply generates the voltage for the ECL terminating resistors. It consists of a +3 V switching current pump. The +3 V power supply disposes of surplus current to keep the supply at 3 V. This supply disposes of the surplus current by bootstrapping it into the +5 volt supply. Resistors R958, R960, and R964 form a voltage divider to give a +3 V reference to comparator U980B. The non-inverting pin of the comparator is connected to the +3 V line through R954.

Whenever the +3 V line goes over-voltage, the output of comparator U980B goes high. This turns on Q950 and turns off Q952. This in turn raises the base voltage at Q954, the side of L952 tied to Q954 is pulled to ground, and current flows from the +3 V supply into L952.

Because of the inductance of L952, most of the current drawn is stored in the magnetic field of the inductor rather than going through Q954 to ground. When inductor L952 has drawn enough current, the +3 V line drops below the reference voltage. This reverses the above procedure, making Q954 not conduct. When Q954 stops conducting, L952 stops drawing current from the +3 V supply. However, there is still a magnetic field around L952 that stores the energy previously pulled out of the +3 V supply.

The magnetic field around L952 starts to collapse when Q954 stops conducting, so L952 is forced to dissipate as much power as it absorbed from the +3 V supply. L952 forces out a pulse of current at +5 V which goes through CR960 into the +5 V supply. L954 evens out the current spikes coming through CR960.

Comparator U980 works as an over-current sensor by monitoring the voltage across R952. If Q954 is conducting too much of the time, the current through L952 will become great enough to activate this comparator and shut down Q954.

91S32 Detailed Circuit Description

OVERVIEW

Refer to schematics in the Diagrams section of this addendum while reading this detailed circuit description.

FUNCTIONAL BLOCKS

The 91S32 circuitry is divided into the following functional blocks.

91S32 Controller Interface----------Schematic 101
High-Speed Address Bus Buffer---------Schematic 103
Free-Running address counter----------Schematic 103
Loop Counter----------Schematic 104
Page Controller----------Schematic 103
Clock Distribution----------Schematic 102
Clock Delay----------Schematic 105
Address Multiplexer----------Schematic 103
RAM Write----------Schematic 104
Vector RAM----------Schematic 107
Output Latches and Driver----------Schematic 107
Data Readback----------Schematic 106
Address Readback----------Schematic 103
Probe Interface----------Schematic 105
Pattern Generator Probes
+3 Volt Power Supply----------Schematic 104

CIRCUIT DESCRIPTIONS

91S32 Controller Interface <101>

The 91S32 controller interface performs two major functions.

1. It takes data from the Controller board and sends it to appropriate registers by decoding the lowest five bits on the address bus and interpreting BWR(L), BPORT(L), and BRD(L) signals issued by the Controller board.

2. It takes data from the module and writes it on the data bus at the command of the Controller board.

Examples of read and write procedures follow.

READ EXAMPLE. The DAS Controller Board is reading the card ID. The address bus has 0 (hex) written in the four least significant bit positions. Simultaneously, PORT(L) and BRD(L) are asserted, which enables U118. U118 decodes the address, and U118-4 is asserted (L). U118-4 going low enables the CARD ID register, U122, which put the card I.D. data on the data bus.

WRITE EXAMPLE. The write procedure is similar, except that the BWR(L) and PORT(L) signals must be active to enable decoders U106.

The following table is a list of register links to the data bus through signal lines BWR(L), BRD(L), and PORT(L), and by hexadecimal address.

91S32 CONTROLLER INTERFACE MAP

Hex Addr	BRW(L)	BRD(L)	PORT(L)	Control Line	ICs Affected	Schem
XX00	H	L	L	CARD ID(L)	U122	101
XX00	L	H	L	MAP REG(L)	U206	102
XX01	H	L	L	POD STATUS(L)	U120	101
XX01	L	H	L	SPARE		
XX02	H	L	L	DATA CLOCK	P6464	
XX02	L	H	L	PROBE R/W(L)	U516	105
XX03	H	L	L	RDB(L)	U650	106
XX03	L	H	L	PROBE DATA(L)	U520	105
XX04	L	H	L	MPUCLK	U216	102
XX05	L	H	L	MWEM(L)	U408	104
XX06	L	H	L	WP(L)	U400	104
XX07	L	H	L	PORT7(L)	U104	101
XX08	L	H	L	PORT8(L)	U112	101
XX09	L	H	L	PORT9(L)	U302	103
XX0A	L	H	L	PORTA(L)	U314	103
XX0B	L	H	L	PORTB(L)	U512	105
XX0C	L	H	L	PORTC(L)	U514	105
XX0D	L	H	L	PORTD(L)	U728	101
XX0E	L	H	L	PAGB(H)	U348	103
XX0F	L	H	L	PAGA(H)	U348	103

High Speed Address Bus Buffer <103>

U300, U308, and U312 receive the address and clock from the 91S16 Pattern Generator over the 40-wire flat cable. The high speed address bus buffer is only used when the 91S32 is in Follows mode with a 91S16 installed.

Free-Running Address Counter <103>

This circuit controls the vector address of the 91S32 except when the 91S32 is in Follows mode in conjunction with a 91S16. U304, U316, U330, and U340 generates the internal vector address. When the address comes to full value (7FF), the data stored in U302 and U314 is loaded into the loop counter. When the MPU writes the address to this counter, U314-15 should be low and U350 AND-GATEs are all off, and counter ICs parallel-load enables are all low. The MPU writes the address into the U302 & U314 and sends the load clock to these ICs. The following tables show how vector loop values are set.

VECTOR LOOP VALUE SET

Port no.	bit	vector address depth
09	0	0
09	1	1
09	2	2
09	3	3
09	4	4
09	5	5
09	6	6
09	7	7
0A	0	8
0A	1	9
0A	2	10

OTHER PORT 0A CONTROL BITS

Bit	Function	On or Off
3	Spare	
4	Spare	
5	Self Load	0:off 1:on
6	Internal Clock Output Control	0:on 1:off
7	SEQ/FOLLOW	0:follow 1:seq

Loop Counter <104>

U406, U412, U414, and U416 count the loop value. The 91S32 controller interface loads the loop value to these counters using WEA(L) and WEB(L). While the 91S32 is in the Run mode, LOOP COUNT(L) comes the vector address counter, the loop counter counts up, reaches terminal count, then U418-10 goes to high and latches the stop signal. The output U418B-15 stops the clock circuit U214 flip-flop.

Page Controller <103>

This circuit switches between Follows mode and Sequential mode. U328-A, U328-B, U328-C,U338-A, and U346-A become active in Follows mode. U352-C, U338-B, U338-C, and U338-D become active during the Page mode.

Page A locations: 0000-1023
Page B locations: 1024-2047

Clock Distribution <102>

U208 and U216B and C select one of three clocks 91A08 INTLCLK(L), PGEXTCLK(L), and MPUCLK(L). U216-A controls PGEXTPAUSE(H). U218A and B, U224A and B, and U210B distribute the clock to the address loop counter, page latch, delay lines, and output latches. There are several modes in which to send the clock to each block. When 91S32s are used with a 91S16, each 91S32 receives its clock from the 91S16.

In the Follows 91S16 mode, NOR gate U224B sends the clock signal to the output latches. NOR gate U210B sends the clock to the address counter. The page latch receives the clock directly from U220A.

In the Sequential mode, U218B sends the clock to the vector address counter, delay lines, and output latches.

When only 91S32s are installed, one of the 91S32s becomes the master and the others become slaves. The master 91S32's U210D, U228A, and U228B send the selected clock to the slave 91S32s. The slave 91S32's U220B and U224A receive the clock and send the clock to the vector address counter, delay lines, and output latches. In the setup mode, U218A sends the clock to the latches. P204 and P206 are the termination resistors for the clock from the master 91S32. P200 and P202 are the termination resistor straps for the clock from the 91S16. Straps to P200 and P202 are installed only on the 91S32 furthest from the 91S16.

Clock Delay <105>

This block consists of delay lines and gates. The output latches and buffer clock are delayed by the delay lines DL140, DL160, DL180, DL200, and DL220 and selected by the gate consisting of U500, U502, U504, and U506. Using this delayed clock, flip-flops U640, U642, U644, U646, U720, U722, U724, and U726 load the vector data. The following tables show delay timing control.

91S32 CLOCK LINE DELAY

Probe POD	Delay Value	Write#0B 01234567	Write#0C 01234567
A	5 n	011XXXXX	XXXXXXXX
A	0 n	101XXXXX	XXXXXXXX
A	-5 n	110XXXXX	XXXXXXXX
B	5 n	XXX011XX	XXXXXXXX
B	0 n	XXX101XX	XXXXXXXX
B	-5 n	XXX110XX	XXXXXXXX
C	5 n	XXXXXX01	1XXXXXXX
C	0 n	XXXXXX10	1XXXXXXX
C	-5 n	XXXXXX11	0XXXXXXX
D	5 n	XXXXXXXX	X011XXXX
D	0 n	XXXXXXXX	X101XXXX
D	-5 n	XXXXXXXX	X110XXXX

X: this bit not affected.

OTHER PORT 0C CONTROL BITS

Bit	Function	Stutus
4	Card Select	0:S16 1:S32
5	Stop pg line	0:on 1:off
6	SYSTEM CLOCK	0:on 1:off
7	Internal Clock Input Control	0:on 1:off

Address Multiplexer <103>

U306, U310, U318, U324, and U332 receive the address either from the 91S16 or from the internal address counter described earlier. These data are used to provide the A-block and B-block memory addresses.

RAM Write <104>

U402 and U410 select the vector memory address block; either chip can write to the memory block for Page A or Page B. U400 determines the write channel block. When one of U400's output channel changes low, MWRM(L) becomes effective. This signal, and MODEA(L) or MODEB(L), are ANDed in U402 or U100 to produce write enable.

Vector RAM 107>

U700 through U718 comprise a 1024 x 4-bit random access memory. When WE(L) input level is low, all data outputs are in a high-impedance state (tri-stated). When the outputs are tri-stated, the MPU writes the pattern data to the memory.

Output Latches and Driver <107>

The data from the memory is clocked into this block and the data is converted to differential data and sent out to the P6464 probe.

Data Read Back <106>

The data readback circuit receives the memory data; readback is determined by the value of U112 output data. Comparators U620, U622, U624, U626, U628, U630, U632, U634, U636, U638, U652, U654, U656, U658, U660, U662, U664, U666, U668, and U670 take data from the memory data output of channels 0 to 31, strobe and inhibit, convert it from ECL to TTL, and write it on the RDB0-RDB7 bus to the 91S32 controller interface. The output from the comparator is divided into five 8-bit bytes. Each corresponding bit in the five bytes is wire-ORed. Readback bytes are selected by RD0(H), RD1(H), RD2(H), RD3(H) and RD4(H), causing the selected byte to output data and the non-selected byte to output zeros (go to a high-impedance state).

Address Readback <103>

The address readback circuit receives A-block memory and status. Comparators U320, U326, U334, and U344 take data from the address output of RA0A to RA9A, SELINH(L), PAGE-A/B, HALFCK, START/STOP(H), and LSTOPM(L), convert it from ECL to TTL, and write it on the RDB0-RDB7 bus to the 91S32 controller interface. The readback port and the sequence is the same as the data read.

Probe Interface <105>

The 91S32 can detect the status of a probe by reading data from the probe. The 91S32 reads back one data line from each probe to determine the status. To do this, the four 91S32 read bits in U516 are sent low by writing low to PORT(L). The 91S32 then reads DATA CLOCK from the POD STATUS(L) port. When the 91S32 sends DATA CLOCK(H) to read the next probe status, a new status bit can be read from each of the four probes. This procedure is repeated each time the status of the 91S32 probes is required.

The 91S32 writes one bit to each probe to set up the pattern generator probe. To do this, the four 91S32 write bits in U516 are sent low by writing to PROBE WRITE. The 91S32 then writes to port PROBE DATA (port 03) and sends DATA CLOCK(H). This instructs the probe that the 91S32 is going to write the status. Each time, a new setting data bit can be written to the probe.

Pattern Generator Probes

The P6464 ECL/TTL Pattern Generator Probe is used by the 91S16 and the 91S32 Pattern Generator modules. The probe puts out 10 channels of data at ECL and TTL logic levels. The output levels of the probe (Vout) are set by the voltages present at the probe input's VH (high output level) and VL (low output level).

+3 Volt Power Supply <104>

The +3 volt power supply is used for biasing ECL circuits on the 91S32. Since +3 V is not supplied by the power supplies, it is created on the module by this +3 V switching current pump.

In ECL circuitry, the +3 V biasing supply tends to float up to +4 V. The +3 V supply must then dispose of surplus current to keep the supply at +3 V. This supply disposes of the surplus current by bootstrapping it into the +5 V supply. The +5 V Power Supply Module that is driving the 91S32 then adjusts for the extra current to maintain the +5 V regulation.

Resistors R216, R214, and R230 form a voltage divider to give a +3 V reference to comparator U222B. The noninverting pin of the comparator is connected to the +3 V line through R210. Whenever the +3 V line goes over-voltage, the output of comparator U222B goes high which turns on Q200 and turns off Q202. This, in turn, raises the base voltage at Q204, so the side of L202 tied to Q204 is pulled to ground.

When the side of L202 that is attached to Q204 is pulled to ground, current flows from the +3 V supply into L202. Because of the inductance of L202, most of the current drawn is stored in the magnetic field of the inductor rather than going through Q204 to ground.

When inductor L202 has drawn enough current, the +3 V line drops below the reference voltage. This reverses the above procedure, making Q204 not conduct. When Q204 stops conducting, L202 stops drawing current from the +3 V supply. However, there is still a magnetic field around L202 that stores the energy previously pulled out of the +3 V supply.

The magnetic field around L202 starts to collapse when Q204 stops conducting, so L202 is forced to dissipate as much power as it absorbed from the +3 V supply. The only place that the power can be dissipated is through CR200 into L204. The result is that L202 forces out a pulse of current at +5 V which goes through CR200 into the +5 V supply. L204 evens out the current spikes coming through CR200 to ease regulation of the +5 V supply.

Comparator U222A works as an over-current sensor by monitoring the voltage across R220. If Q204 is conducting too much of the time, the current through L202 will become great enough to activate this comparator and shut down Q204. The only place that the power can be dissipated is through CR200 into L204. The result is that L202 forces out a pulse of current at +5 V which goes through CR200 into the +5 V supply.

Section 5
VERIFICATION AND ADJUSTMENT PROCEDURES

Introduction

This section contains three main parts: functional check procedures, adjustment procedures, and probe check procedures. These procedures allow a qualified technician to verify the operation of a 91S16 or 91S32 Pattern Generator module, to adjust variables to achieve the proper performance.

A diagram showing the locations of components is located in the Diagrams section of this addendum.

FUNCTIONAL CHECK PROCEDURES

These tests verify that the device being tested is operational. The procedures exercise the main user interfaces of the device to verify their operation. They also verify that the main internal features are operating. These tests determine whether adjustment or repair is necessary.

ADJUSTMENT PROCEDURES

These adjustments bring the device being adjusted to meet, or exceed, product specifications. If the device cannot meet the specifications given in this addendum after adjustment, repair is necessary.

CAUTION

Verify installation of up-graded +5 V Power Supplies in your DAS mainframe before performing any of the procedures in this section. A verification procedure is provided at the end of this section.

Test Setup Information

SUGGESTED TEST INSTRUMENTS

The following test instruments and accessories are required for the functional checks and adjustment procedures provided in this section of the addendum. Unless otherwise specified, equivalent equipment may be substituted for the recommended type.

NOTE

Each procedure uses only some of the equipment given in these tables. Check the required equipment for each procedure before appropriating test equipment for that procedure.

Equipment Required for the Functional Checks

DAS Mainframe with V1.11 firmware and a 22 A +5 V Power Supply, no substitute

91A08 Data Acquisition Module, no substitute

P6452 Data Acquisition Probe, Tektronix P/N 010-6452-01, no substitute

P6454 100 MHz Clock Probe, Tektronix P/N 010-6454-01, no substitute

Service Maintenance Kit, Tektronix P/N 067-0980-00, no substitute

Oscilloscope, Dual Trace, 300 MHz, with probes, Tektronix 2465 or equivalent.

TM500 Series Mainframe (TM503 or higher)

Digital Multimeter, 0.05% dc V Accuracy, Tektronix DM501A or equivalent

Pulse Generator, 100 MHz, Tektronix PG502 or equivalent

BNC-PHONO Cable, 79 inches long, Tektronix P/N 176-8165-00 or equivalent

+5 V Power Supply, Tektronix PS503 or equivalent

Four flying lead sets p/n 131-2230-00 or equivalent

Two capacitors, 1 uF, p/n 290-0891-00 or equivalent

Equipment Required for the DAC Threshold Adjustment

TM500 Mainframe		TM503 or higher
Digital Multimeter	0.05% dc V Accuracy	DM501
*Threshold Fixture		

*This is the same fixture used as a service tool for the Tektronix 1240 Logic Analyzer. If you have the 1240 fixture, it is not necessary to build another one. If you do not have one, refer to the construction procedure at the beginning of the Adjustments subsection.

Equipment Required for Threshold Fixture Construction

Qty.	Description	Part Number
1	Terminal Connector Holder (2 holes-by-8 holes)	352-0484-00
5	Mini PV Female Connectors	131-0484-00
1	Resistor, 10.5 Kohm, 1%	321-0291-00
3	Wires, 26-guage, 1-inch long	

Equipment Required for the Delay Adjustments

DAS 9100 Series Mainframe

DAS Main Extender Board

350 MHz oscilloscope with two channels

Two P6230 probes for the oscilloscope

Probe Power Supply

Alignment tool, p/n 003-1134-00

Four flying lead sets p/n 131-2230-00 or equivalent

Two capacitors, 1 uF, p/n 290-0891-00 or equivalent

91S16, P6464, and P6460 Functional Check

This subsection contains functional check procedures for the 91S16 with P6464 and P6460 probes. This procedure allows a qualified technician to verify the operation of the 91S16 module and a P6464 or P6460 probe.

These instructions are limited to the procedures necessary to verify the modules. Detailed information about normal menu operation may be found in the first three sections of this addendum, and in the DAS 9100 Series Operator's Manual. Detailed information about diagnostic menu operation is located in the DAS 9100 Series Service Manual.

91S16 Functional Check

This procedure verifies the pattern generation capabilities of the 91S16.

You will need the following equipment to perform this procedure:

1 - DAS 9100 Mainframe with V1.11 firmware and:
  1 - 22 A, +5V Power Supply in a position to power slot 1
  1 - 91S16 Pattern Generator Module in slot 1
  2 - P6464 Pattern Generation Probe
  1 - P6460 Data Acquisition Probe
  1 - 91A08 Data Acquisition Module in slot 6
  2 - P6452 Data Acquisition Probe
  1 - P6454 100MHz Clock Probe kit
  1 - 300 MHz dual-trace oscilloscope with P6230 probes
  1 - TM500 mainframe
  1 - digital multimeter
  1 - variable power supply
  1 - 100 MHz pulse generator
  1 - +5 V external power supply

Refer to Section 3, Operating Instructions in this addendum for instructions on module installation.

Mainframe Setup for the Functional Check

The following steps configure the DAS for the functional check.

1. Turn off the mainframe.

2. Install the 91S16 in slot 1 and the 91A08 in slot 6. Ensure that slot 1 is powered by the 22 A, +5 V supply.

3. Turn on the mainframe.

(1) Executing the Diagnostic Self Test

Use the following procedure to enter the DAS Diagnostics menu and operate the ALL mode tests for each level.

1. Turn off the mainframe. Turn on the mainframe while holding down the STOP key on the keyboard. This causes the power-up self test to fail.

2. Press START SYSTEM to enter the Diagnostics menu.

3. Select SINGLE in the MODULE field.

4. Move the cursor to the SLOT field and enter 1 to test the 91S16 in slot 1.

5. Set the MODE field to SINGLE and run all functions.

The DAS diagnostics will perform all available tests on the slot. All Diagnostics tests should pass.

(2) Probe Connector Functional Tests

This test verifies:

- the operation of the probe R/W line and the POD R/W IC
- the runs from the POD R/W IC to the probe connectors
- the POD STATUS register and its selector.

For these tests, a P6460 probe is connected to POD C and a P6464 probe is connected to POD A, then to POD B.

CAUTION

A probe must not be connected or removed while a pattern is being generated. Doing so can damage the probe.

1. Press the POD ID button on the P6464 probe in POD A, and verify that the display shows POD 1A in the upper left corner.

2. Remove the probe and verify that POD 1A DISCONNECTED appears in the upper left corner of the DAS display.

3. Reconnect the P6464 probe to POD A and verify that the display shows POD 1A CONNECTED.

4. Repeat steps 1 through 3 for POD B on the 91S16 module. Using the P6460 probe, repeat steps 1 through 3 for POD C.

(3) POD A Data Output Test

Test Setup

The following procedure provides the initial setup for these tests. You will modify the probe setup as you perform the functional check.

1. Connect a P6464 Pattern Generator Probe A to POD connector A of the 91S16, a P6464 B to POD connector B, and the P6460 external control probe to POD connector C. When probes are installed, the mainframe should beep and show the message POD 1A (or 1B or 1C) CONNECTED.

2. Connect the data acquisition probe to the 91A08 Data Acquisition module in slot 6.

3. Connect the pattern generator probe podlets to the data acquisition probe using flying-lead sets and connector pins p/n 131-2230-00 connector pins or equivalent. Connect P6464 to POD A, and P6452 to the 91A08 in slot 6.

4. Connect the strobe line of the pattern generator probe to the qualifier line of the data acquisition probe.

5. Connect the ground lead of the data acquisition probe to an appropriate ground lead of the P6464 probe.

6. Connect the P6454 100 MHz Clock Probe to the coaxial connector on the 91A08 module in slot 6.

7. Connect the IN line of the 100 MHz Clock Probe to the clock output of the pattern generator probe.

8. Connect the REF line of the 100 MHz Clock Probe to the unused GND SENSE line of the data acquisition probe.

Pattern Generator Probe Setup

The following procedure connects the P6464 Pattern Generator Probes to the DAS and to an external +5 V power supply. The probes are also decoupled from variations in the supply with a 1 uf capacitor (p/n 290-0891-00 or equivalent).

NOTE

If a PS503A is used as the +5 V external power supply, install it in the high-power slot of your TM500 Series mainframe.

1. Connect P6464 Pattern Generator Probes to the POD connectors of the 91S16 in the DAS mainframe. If a label on a probe identifies it by POD number, it must be connected to that POD connector.

2. Connect a 2 foot (0.6m) wire to the +5 V output of the power supply. Connect a 2 foot wire to the ground of the power supply.

3. Connect the VL lines (black) and common lines (green) of all pattern generator probes to the 2 foot wire attached to the ground output of the +5 V, 2 A power supply.

4. Connect the VH lines (red) of all pattern generator probes to the 2 foot wire attached to the +5 V output of the +5 V, 2 A power supply.

5. Connect one 1 uF ceramic capacitor across the VH and VL inputs to each probe. The best and easiest way to connect these capacitors is to hook one end of each ceramic capacitor under the hook tip that connects the probe to the +5 V source. Place the other end of each ceramic capacitor under a hook tip that connects to the ground wire.

6. After connecting a ceramic capacitor, check to make sure that connections to the +5 V power supply and ground are secure.

(V-ref of podlets, VL and common of the P6464, DAS ground, PS501 ground, and P6452 ground are all common.)

7. Leave the Diagnostics menu by pressing the PATTERN GENERATOR key. In the Pattern Generator Timing sub-menu, verify that the pattern generator clock is set to 1 microsecond.

8. Enter SEQ 1000 after SEQ 0.

9. Enter the following program in the Pattern Generator Program menu.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	0	0	0		
1001		01	01	0	0	0		
1002		02	02	0	0	0		
1003		04	04	0	0	0		
1004		08	08	0	0	0		
1005		10	10	0	0	0		
1006		20	20	0	0	0		
1007		40	40	0	0	0		
1008		55	55	3	0	0		
1009		80	80	0	0	0		
1010		AA	AA	3	0	0		
1011		FF	FF	0	0	0	JUMP	1000

10. Enter the Trigger Specification menu and set the MODE field to 91A08 ONLY. See Figure 5-1.

11. In the Trigger Specification menu, set the acquisition clock to external falling edge.

12. Press the POD ID button on the back of the data acquisition probe. Read the POD number off the DAS screen. Set the qualifier of the acquisition module to 0.

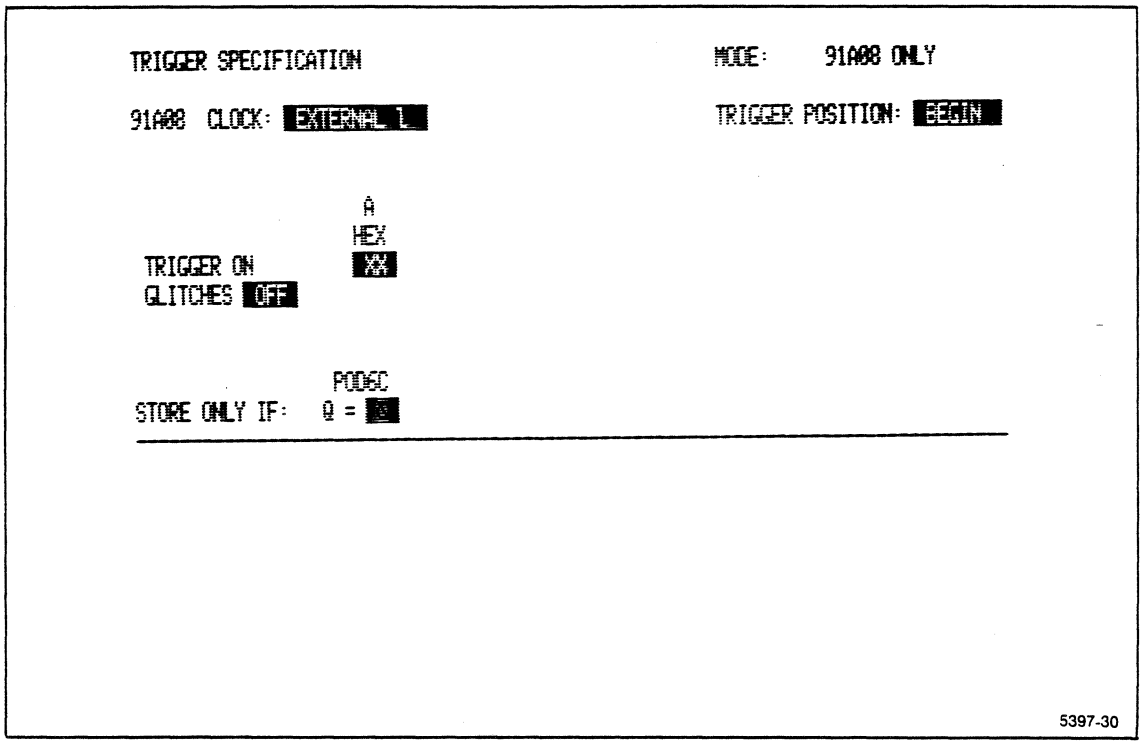


Figure 5-1. Trigger Specification menu organization.

The next steps verify that the 91S16 can transmit data, strobe, and clock signals through POD connector A.

13. Press the START SYSTEM key.

14. Enter the Timing Diagram menu.

15. Press and hold the POD ID button on the back of the Data Acquisition probe. Read the POD number off the DAS screen.

16. Set the magnification in the Timing Diagram menu to 10; this should show a display like Figure 5-2. The 91A08 should trigger on sequence 18.

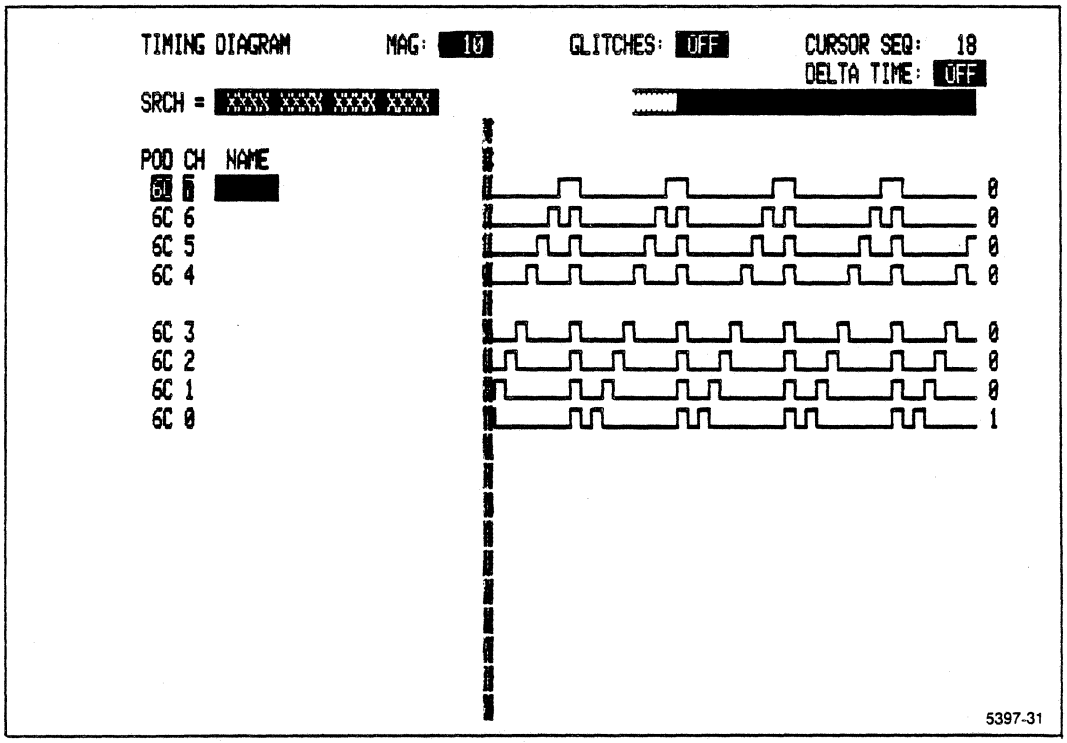


Figure 5-2. Timing Diagram menu, POD A transmission test.

(4) POD B Data Output Test

This test verifies that the 91S16 can transmit data, strobe and clock signals through POD connector B.

Connect the P6464 Pattern Generator Probe (B) to POD connector B, and to the data acquisition probe of the 91A08 in slot 6.

1. When the probe is installed in POD connector B, the DAS mainframe should beep and show the message "POD 1B CONNECTED".

2. Press the POD ID button on the back of the pattern generator probe housing. The DAS mainframe should beep and display the message "POD 1B".

3. Enter the Trigger Specification menu and set the qualifier for the data acquisition probe to 0 (active low).

4. Press the START SYSTEM key.

5. Enter the Timing Diagram menu.

6. Press the POD ID button on the back of the data acquisition probe. Read the POD number on the DAS screen. Adjust the Timing Diagram menu to show data from this POD.

7. Set the magnification of the Timing Diagram to 10; this should again show a display like Figure 5-2. The 91A08 should trigger on sequence 18.

(5) Inhibit Control Test

Test setup

1. Disconnect the P6452 qualifier lead from the P6464 and connect the strobe lead from the P6464 probe to the INHIBIT (red) lead of the P6460 input probe.

2. Enter the Pattern Generator menu. Verify the that INHIBIT MASK field in the Pattern Generator program is 0000, and that the INHIBIT MASK field in the Configuration sub-menu for clock and strobe inhibit masks is set to 1. Enter the Probe sub-menu and set the INHIBIT field to EXTERNAL 1 ONLY.

3. Enter the Timing menu and set the CLOCK field to 2 us.

4. Set the strobe to 3 on lines 1008 and 1009 lines of the pattern generator program. The program should now look like the following listing.

```
  INHIBIT
   MASK  :  00 00

SEQ     LABEL B  A     S I M   SEQ FLOW,  CONTROL REG, OUT

  0           00 00    0 0 0   JUMP        1000
1000 1000     00 00    0 0 0
1001          01 01    0 0 0
1002          02 02    0 0 0
1003          04 04    0 0 0
1004          08 08    0 0 0
1005          10 10    0 0 0
1006          20 20    0 0 0
1007          40 40    0 0 0
1008          80 80    3 0 0
1009          FF FF    3 0 0   JUMP        1000
```

Test Description

This test verifies that the 91S16 responds to an external inhibit signal through the P6460 probe.

Test sequence

5. Press the START SYSTEM key.

6. When data acquisition is complete, enter the Timing Diagram menu. The display should look like Figure 5-3.

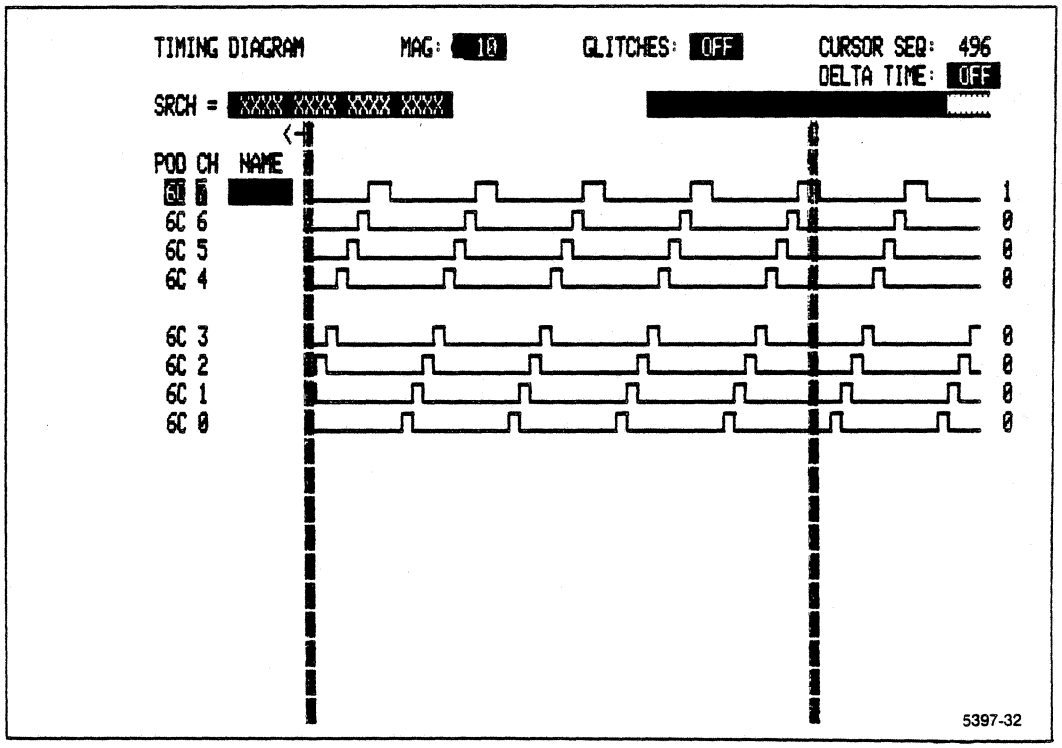


Figure 5-3. Test data, inhibit control test.

The next steps verify the operation of the internal inhibit.

7. Enter the Pattern Generator menu, and set the INHIBIT field to 1 as in the following display. Enter the Probe sub-menu and set the INHIBIT field to INTERNAL 1 ONLY.

```
  INHIBIT
   MASK  :  00 00

SEQ  LABEL   B  A    S I M   SEQ FLOW,  CONTROL REG, OUT

  0          00 00   0 0 0   JUMP        1000
1000 1000    00 00   0 0 0
1001         01 01   0 0 0
1002         02 02   0 0 0
1003         04 04   0 0 0
1004         08 08   0 0 0
1005         10 10   0 0 0
1006         20 20   0 0 0
1007         40 40   0 0 0
1008         80 80   0 0 0
1009         FF FF   0 3 0   JUMP       1000
```

8. Press START SYSTEM.

9. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-3.

(6) External Jump Line Test

Test Setup

1. Connect the strobe line to the EXT JUMP (orange) lead of the P6460 input probe.

2. Enter the SETUP PROBE sub-menu and set the EXT JUMP field to IF 1, and disable the INHIBIT field.

3. Enter the Pattern Generator Program menu and set the IF EXT JUMP instruction as shown in the following display.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	0	0	0		
1001		01	01	0	0	0		
1002		02	02	3	0	0		
1003		04	04	0	0	0	IF EXT JUMP	TEST
1004	1004	80	80	0	0	0		
1005		FF	FF	0	0	0	JUMP	1000
1006	TEST	08	08	0	0	0		
1007		10	10	0	0	0		
1008		20	20	0	0	0		
1009		40	40	0	3	0	JUMP	1004

This test verifies that the 91S16 responds to the IF EXT signal through the P6460 input probe.

4. Press the START SYSTEM key.

5. When displayed on the Timing Diagram menu, the data acquired from the pattern generator should look like the data shown in Figure 5-4.

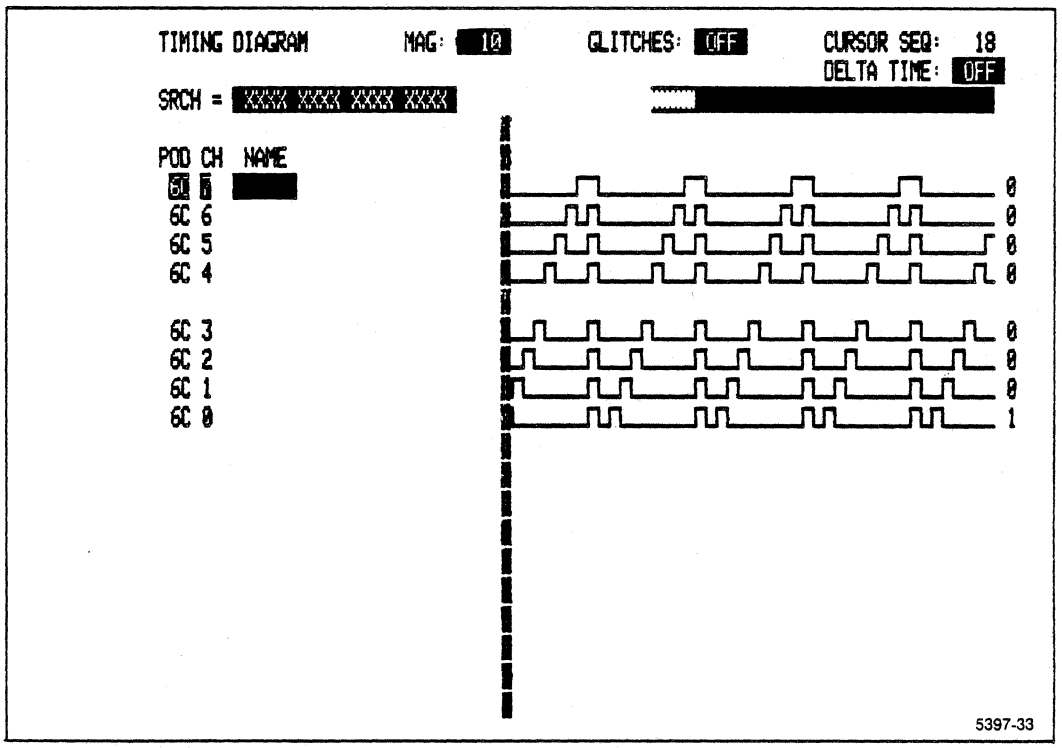


Figure 5-4. Test data, external jump line test.

(7) IRQ Test 1

Test Setup

1. Connect the strobe line of POD A to the interrupt line (yellow) of the P6460 input probe, and connect the strobe line of POD B to the qualify line (green) of the P6460 input probe.

2. Enter the Probe sub-menu and set the IRQ field to ON rising edge, CALL TEST, and Enter the Program sub-menu. Disable the EXT JUMP field, push DON'T CARE to eliminate sequence flow and control commands, then type in the program as follows.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	0	0	0		
1001		01	01	0	0	0		
1002		02	02	2	0	0		
1003		04	04	1	0	0		
1004		80	80	0	0	0		
1005		FF	FF	0	0	0	JUMP	1000
1006	TEST	08	08	0	0	0		
1007		10	10	0	0	0		
1008		20	20	0	0	0		
1009		40	40	0	0	0	RETURN	

Test Description

This test verifies that the 91S16 responds to an INTERRUPT signal through the P6460 input probe. It checks the qualifier line through the P6460 probe, and checks the interrupt mask instruction.

Test Sequence

3. Press the START SYSTEM key.

4. When IRQ test data is displayed on the Timing Diagram menu, the data acquired from the pattern generator should look like the data shown in Figure 5-5.

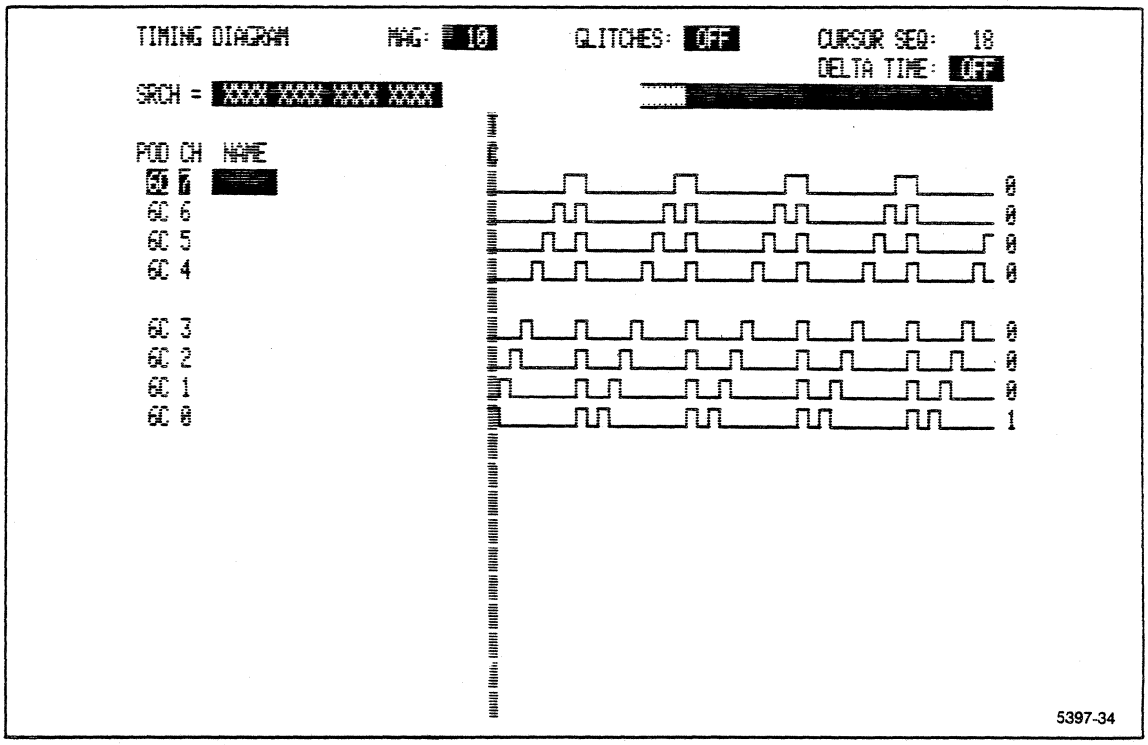


Figure 5-5. Test data, interrupt test 1.

The next steps verify the operation of the qualify line.

5. Enter the SETUP PROBE sub-menu and set the QUALIFIER field to 1.

6. Press the START SYSTEM key.

7. The Timing Diagram menu should again look like the data shown in Figure 5-5.

8. Enter the PROBE sub-menu and set the QUALIFIER field to 0.

9. Press the START SYSTEM key.

10. The Timing Diagram menu should look like the data shown in Figure 5-6.

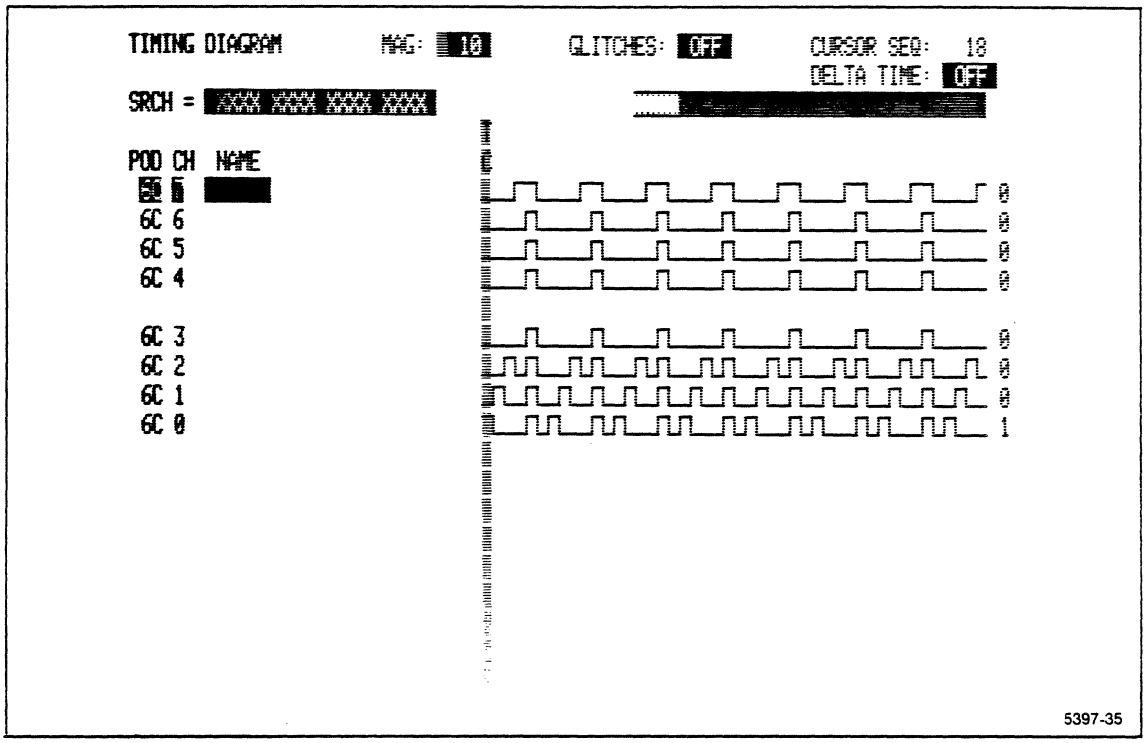


Figure 5-6. Test data, qualify line test.

The next steps verify the operation of the interrupt mask.

Test setup

11. Enter the Program sub-menu and set the M field as follows.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	0	0	0		
1001		01	01	0	0	0		
1002		02	02	2	0	1		
1003		04	04	1	0	0		
1004		80	80	0	0	0		
1005		FF	FF	0	0	0	JUMP	1000
1006	TEST	08	08	0	0	0		
1007		10	10	0	0	0		
1008		20	20	0	0	0		
1009		40	40	0	0	0	RETURN	

12. Enter the Probe sub-menu and set the qualifier field to X.

Test sequence

13. Press the START SYSTEM key.

14. The Timing Diagram menu should again look like the data in Figure 5-6.

(8) IRQ Test 2

1. Enter the Program sub-menu and remove the RETURN at sequence 1009.

2. Enter the Probe sub-menu and set the IRQ field to ON rising edge: IF IRQ ENABLED, and enter the Program sub-menu. Write the program as follows.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	0	0	0		
1001		01	01	0	0	0		
1002		02	02	1	0	0		
1003		04	04	0	0	0	IF IRQ JUMP	TEST
1004	1004	80	80	0	0	0		
1005		FF	FF	0	0	0	JUMP	1000
1006	TEST	08	08	0	0	0		
1007		10	10	0	0	0		
1008		20	20	0	0	0		
1009		40	40	0	0	0	JUMP	1004

Test Description

This test verifies that the 91S16 responds to the INTERRUPT signal through the P6460 input probe.

Test Sequence

3. Press the START SYSTEM key.

4. The Timing Diagram menu display shows the data acquired from the pattern generator. The display should again look like the data shown in Figure 5-5.

The next steps verify the operation of the qualify line.

5. Connect the strobe line of POD B to the qualifier line through the P6460 input probe.

6. Enter the Probe sub-menu and set the QUALIFIER field to 1.

7. Press the START SYSTEM key.

8. The Timing Diagram menu should again look like the data shown in Figure 5-5.

9. Enter the Probe sub-menu and set the QUALIFIER field to 0.

10. Press START SYSTEM.

11. The Timing Diagram menu should again look like the data shown in Figure 5-6.

(9) Transmission Test of the EXT CLK Signal

Test Setup

This test requires the use of an external clock source. The recommended clock source is a square wave or pulse generator with a 50 MHz output between ground and +5 V.

1. Connect the output of the signal generator to the EXT CLK line on the P6460 input Probe.

2. The signal generator must have a common ground with the probes. To accomplish this, connect the ground of the signal generator to the two clips that connect the data acquisition probe ground sense to the P6460 input Probe ground line.

3. Enter the Probe sub-menu and set the IRQ field to DISABLE, and enter the Timing sub-menu and set the CLOCK field to EXTERNAL rising edge.

4. Adjust the pattern generator program to match the following display.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	1	0	0		
1001		01	01	0	0	0		
1002		02	02	0	0	0		
1003		04	04	0	0	0		
1004		08	08	0	0	0		
1005		10	10	0	0	0		
1006		20	20	0	0	0		
1007		40	40	0	0	0		
1008		80	80	0	0	0		
1009		FF	FF	0	0	0	JUMP	1000

5. Enter the Trigger Specification menu and set the acquisition clock to External Falling edge.

Test Description

This test verifies the transmission of the EXT CLK signal through the P6460 Input Probe.

Test Sequence

6. Press START SYSTEM.

7. When acquisition is finished, examine the Timing Diagram menu. The data acquired from the pattern generator should look like the data shown in Figure 5-7.

A display like Figure 5-7 means the pattern generator external clock is being properly received and processed.

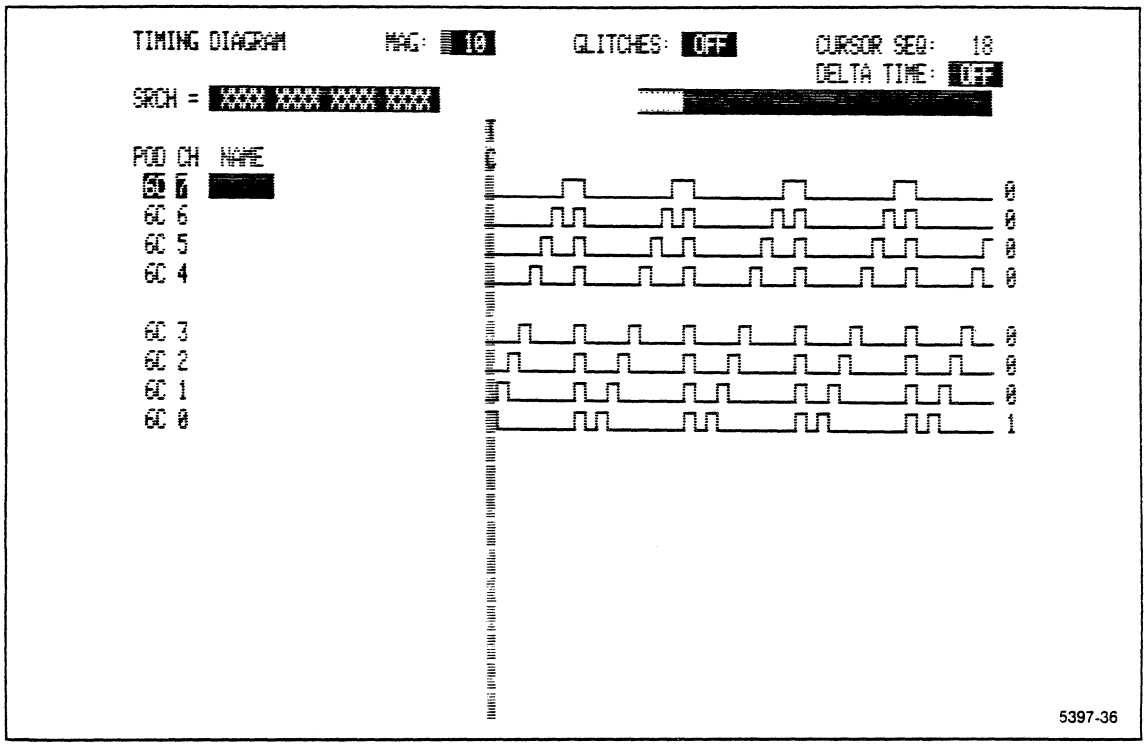


Figure 5-7. Test data, EXT CLK transmission test.

(10) TRIGGER OUT Signal Control Test

Test Setup

1. Enter the Timing sub-menu and set the CLOCK field to 200 ns.

2. Connect the phono connector TRIG OUT J180 (jack nearest POD C) to an oscilloscope with the BNC-phono cable, and set the oscilloscope as follows:

   TRIGGER --------- AUTO
   CH. 1 ----------- 2 V/div.
   TIME BASE -------500 ns/div.

3. Adjust the pattern generator program to match the following display.

SEQ	LABEL	B	A	S	I	M	SEQ FLOW,	CONTROL REG, OUT
0		00	00	0	0	0	JUMP	1000
1000	1000	00	00	1	0	0	TRIGGER	
1001		01	01	0	0	0		
1002		02	02	0	0	0		
1003		04	04	0	0	0		
1004		08	08	0	0	0		
1005		10	10	0	0	0		
1006		20	20	0	0	0		
1007		40	40	0	0	0		
1008		80	80	0	0	0		
1009		FF	FF	0	0	0	JUMP	1000

Test description

This test verifies the 91S16 can transmit the trigger out signal through the phono connector.

Test Sequence

4. Check that a square pulse is generated and looks like Figure 5-8.

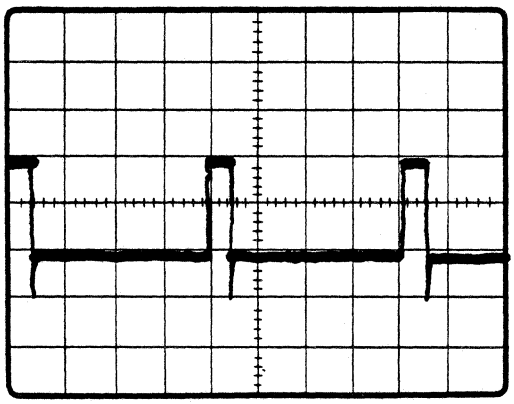


Figure 5-8. TRIGGER OUT pulse.

(11) External Pause Signal Control Test

Test Setup

These steps require the use of an oscilloscope and an external signal. The external signal required is a square wave with a 10 microsecond period and an output between ground and +5 V.

1. Enter the Probe sub-menu. Set the PAUSE field to ON 0.

2. Enter the Timing sub-menu. Set the CLOCK field to 200 ns by using the DECR key.

3. Attach the PAUSE input (brown lead) from P6460 to PG502 output. Attach the probe for channel 1 of the oscilloscope to the external signal. Attach the probe for channel 2 of the oscilloscope to the P6464 probe clock output. Set the oscilloscope to trigger on a rising edge in channel 1. Attach the ground leads of the probes to the ground of the P6460 and the P6464 probe.

   TRIGGER ------- NORM
   CH. 1 -------- 2 v/div.
   CH. 2 -------- 2 v/div.
   TIME BASE ----- 2 microseconds/div.

Test Description

The next steps verify that the 91S16 responds to the PAUSE signal through the P6464 External Probe.

Test Sequence

4. Press the START PAT GEN key.

5. The oscilloscope display should look like the one shown in Figure 5-9.

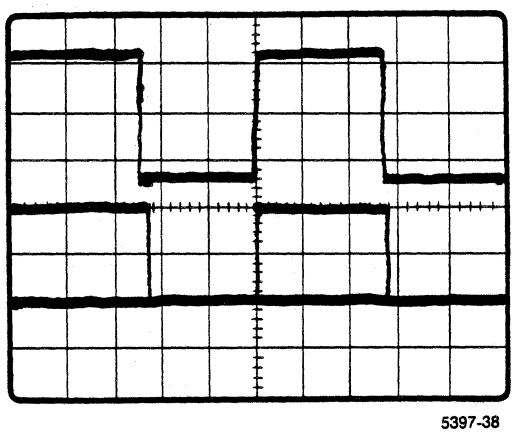


Figure 5-9. External pause pulse, PAUSE = 0.

6. Enter the Probe sub-menu. Set the PAUSE field to ON 1.

7. Press the START PAT GEN key.

8. The oscilloscope display should look like the one shown in Figure 5-10.

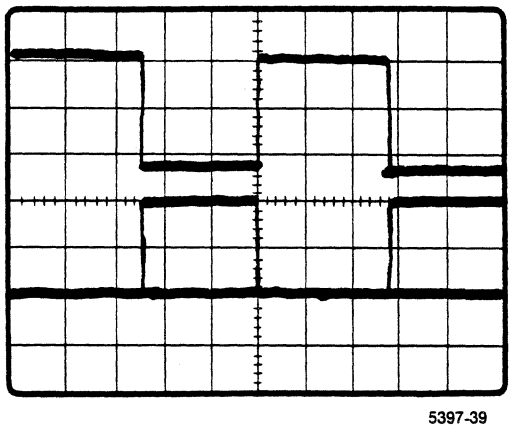


Figure 5-10. External pause pulse, PAUSE = 1.

(12) External Start Control Test

Test Setup

1. Connect the output of the pulse generator (PG502) to phono connector J160 with the BNC-PHONO cable, and set both TRIG and DURATION to EXTERNAL. Set the output level of the generator to TTL (0 V to +5 V).

2. Enter the Probe sub-menu. Set the PAUSE field to DISABLED.

3. Set the EXTERNAL START field to ON rising edge, and set the oscilloscope to trigger on channel 2.

Test Description

The following steps verify that the 91S16 responds to the START signal through the phono connector.

Test Sequence

4. Press the START PAT GEN key.

5. Check that the 91S16 starts generating a clock at the P6464 probe when you press the MANUAL TRIGGER button on the pulse generator.

6. Enter the Probe sub-menu. Set the EXTERNAL START field to falling edge.

7. Press START PAT GEN.

8. Check that the 91S16 starts generating a clock when you release the MANUAL TRIGGER button.

(13) POD Clock Delay Control Test

Test setup

1. Enter the Timing sub-menu and set the CLOCK field to 200 ns.

2. Connect the probe for channel 1 of the oscilloscope to the clock lead of the P6464 probe at POD A.

3. Connect the probe for channel 2 to the clock lead of POD B.

4. Remove the phono connector from J160.

Test description

This test verifies the POD clock delay.

Test sequence

5. Set the POD field to 1B (not the reference POD) and set the POD CLOCK field to 0 ns.

6. Check that the rising edge on channel 1 is overlapping the rising edge on channel 2. (The overlap should be ±500 ps if the tight tolerance adjustment was used to align the clock channels between POD A and POD B, or should be ±2.5 ns if clock alignment was done at the P6464 connector between POD A and POD B).

7. Set the 1B POD CLOCK field to +5 ns and check that the rising edge in channel 2 is 5 ns after the rising edge in channel 1. (The overlap should be ±1.5 ns if the tight tolerance adjustment was used to align the clock channels between POD A and POD B, and should be ±3.5 ns if the clock alignment was done at the P6464 connector between POD A and POD B.)

8. Set the 1B POD CLOCK field to -5 ns and check that the rising edge in channel 1 is 5 ns after the rising edge in channel 2.

9. Set the POD CLOCK field to 0 ns and set the POD field to 1A.

10. Verify that the POD CLOCK field is set to 0 ns and repeat steps 3 through 5 for POD A.

11. Set the POD CLOCK field to +5 ns and check that the rising edge in channel 2 is 5 ns after the rising edge in channel 1.

91S32 PATTERN GENERATOR MODULE FUNCTIONAL CHECK

You will need the following equipment to perform this procedure:

DAS 9100 mainframe with V1.11 firmware version and a 22 A, +5 V Power Supply

Four P6464 TTL/MOS Pattern Generator Probes

P6452 External Clock Probe

P6452 Data Acquisition Probe

91A08 Data Acquisition Module

P6454 100 MHz Clock Probe

350 MHz oscilloscope with two channels

Two probes for the above oscilloscope

100 MHz (or higher) pulse generator

Refer to the Operating Instructions section of this addendum for information on module installation and on the use of the Diagnostic menu. Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes together with the diagnostic lead set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe for use in this functional check. If, due to insufficient +5 V power supply modules or some other constraint, the mainframe is not configured in the recommended way, some functional check procedures will require modification. Configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so can damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the mainframe.

2. Remove the 91S16 from the mainframe.

3. Install a 91A08 in slot 6.

4. Install the 91S32 to be checked in slot 5 of the DAS mainframe that receives power from the 22 A, +5V supply. Install jumpers on J206 and J208. If there is another 91S32 module in the mainframe, remove it.

NOTE

The 91S32 module may be tested in any powered slot. However, this procedure will be easier to follow if the 91S32 module is installed in slot 5.

(2) Executing the Diagnostic Self-Test

The following procedure runs all available Self-test diagnostics on the 91S32 module.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostic menu. Run diagnostic tests on slot 5, the 91S32 module.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. All diagnostic VECTOR RAM tests should pass.

(3) Probe Setup for the Functional Check

The following procedure provides the initial probe setup for these tests.

1. Connect the P6464 pattern generator probe to POD connector D on the 91S32. When the probe is installed, the mainframe should beep and show the message POD 5D CONNECTED.

2. Press the POD ID button on the back of the probe housing. The mainframe should beep and display POD 5D.

3. Connect the P6452 data acquisition probe to the 91A08 acquisition module.

4. Connect the P6464 Pattern Generator Probe podlets to the P6452 data acquisition probe with the flying-lead set and connector pins p/n 131-2230-00 or equivalent. Use all the ground connections.

5. Connect the strobe line of the pattern generator probe to the qualifier line of the data acquisition probe (the white flying lead from the acquisition side of the Diagnostic Lead Set).

6. Connect the P6452 external clock probe to POD connector C of the Trigger/Time Base Module.

7. Install a flying lead set in the P6452 external clock Probe. Also install a ground lead in the GND DIAGNOSTIC connector on the clock probe.

8. Install a ground lead in one of the GND SENSE connectors of the P6452 Data Acquisition Probe. Connect the ground lead of the external clock Probe to one of the grounds on the P6464 pattern generator probe.

9. If a 91A08 module is being used as the acquisition module in the functional check, connect the 100 MHz Clock Probe to its connector on the 91A08 module in slot 6.

10. Connect the IN line of the 100 MHz Clock Probe to the clock output of the pattern generator probe.

11. Connect the REF line of the 100 MHz Clock Probe to the unused GND SENSE line on the pattern generator probe.

12. Set the external power supply output to +5 V.

13. Connect the red lead from the P6464 probe to the +5 V output of the external power supply.

14. Connect the power supply ground, V-ref on the podlets, and all probe grounds to the same ground point.

(4) Initial Menu Setup for the Functional Check

The procedure organizes the menus so that the remainder of the functional checks requires a minimal change to the menus.

1. Leave the Diagnostic menu by pressing the PATTERN GENERATOR key. Select the Timing sub-menu and verify that the pattern generator clock is at 1 microsecond (default).

2. Select the Pattern Generator Configuration sub-menu and enter END SEQ 11, FREE RUN; then select the 91S32 Program sub-menu.

3. Set the pattern generator program to match Figure 5-11.

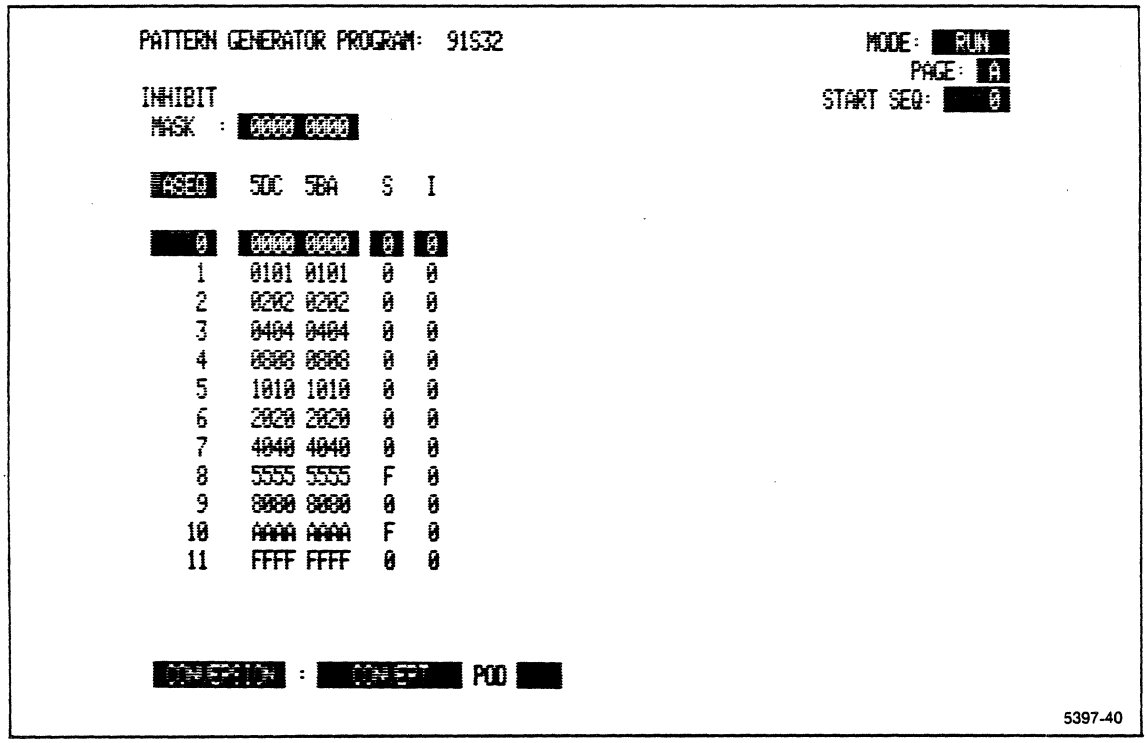


Figure 5-11. Pattern Generator Program sub-menu to start 91S32 functional test.

4. Enter the Trigger Specification menu. Set the MODE field to 91A08 only.

5. In the Trigger Specification menu, set the acquisition clock to external falling edge.

6. Press the POD ID button of the 91A08's P6452 data acquisition probe.

7. Read the POD number on the DAS screen. Set the qualifier corresponding to that POD to 0.

(5) Verifying POD Connector D

The following procedure verifies that the 91S32 can transmit data, strobes, and clock signals through POD connector D.

1. Press the START SYSTEM key.

2. Enter the Timing Diagram menu.

3. Press the POD ID button on the back of the acquisition probe. Read the POD number on the DAS screen. Adjust the Timing Diagram menu to show data from this POD.

4. Set the magnification of the Timing Diagram to 10; this should show a display like Figure 5-12. The actual position of the cursor and trigger will depend on the type of acquisition module used. A 91A08 should trigger on sequence 18.

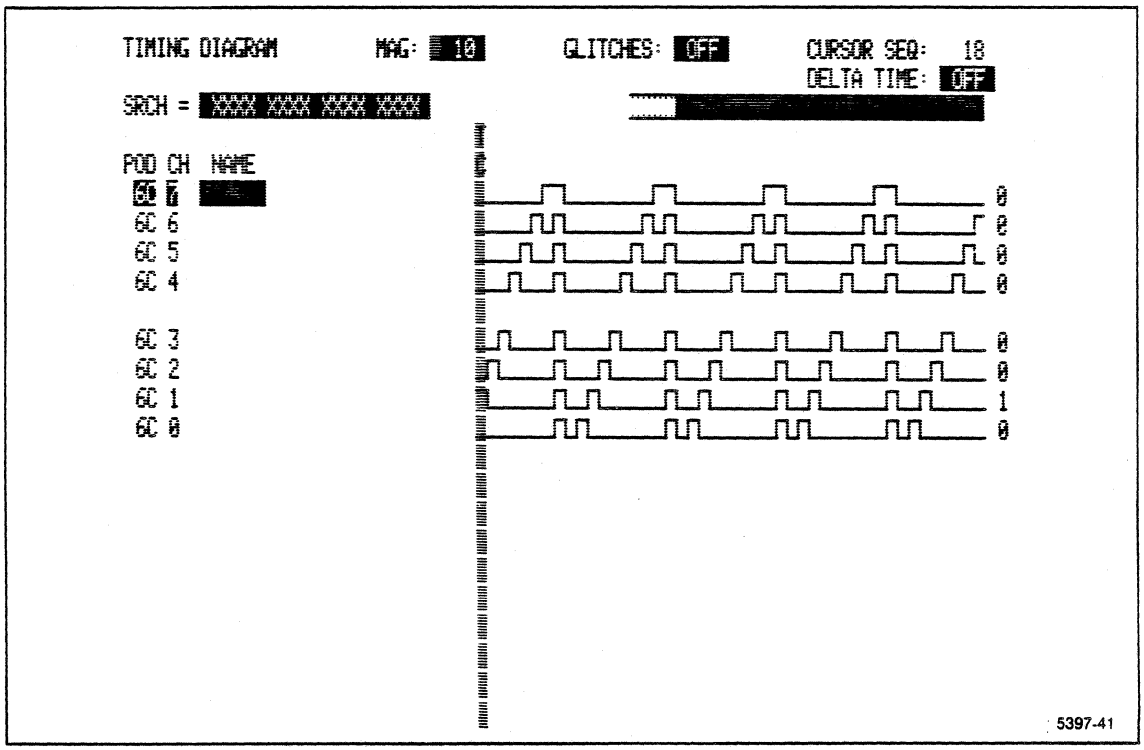


Figure 5-12. Timing Diagram menu for POD connector D.

5. Enter the Pattern Generator Program sub-menu. Set the lower-left corner sub-menu to MODIFY, and enter LOGICAL XOR SEQ 0 THROUGH 9 XXXX XXXX 8 X. Press the EXECUTE key. See Figure 5-13.

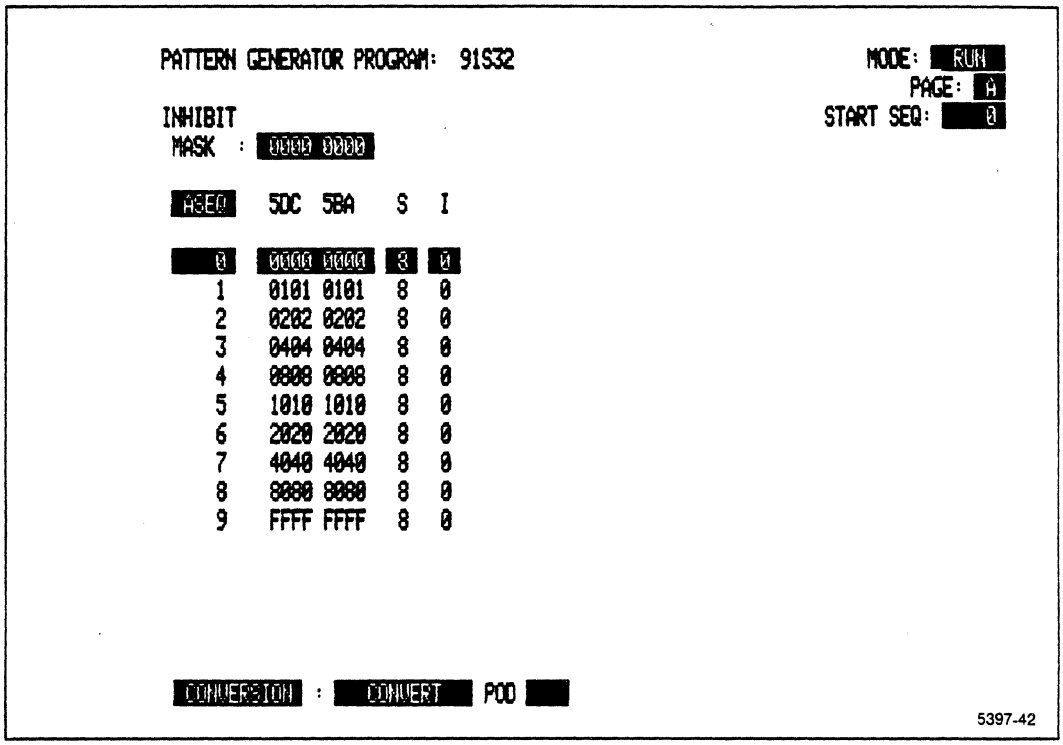


Figure 5-13. Pattern generator setup for POD D check.

6. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 1 (active low).

7. Press START SYSTEM.

8. The data acquired should again match Figure 5-12.

(6) Verifying POD Connector C

The following procedure verifies that the 91S32 can transmit data, strobes, and clock signals through POD connector C.

1. Remove the P6464 Pattern Generator Probe from POD connector D of the 91S32 module. Reconnect the probe to POD connector C of the 91S32 module.

2. When the probe is installed in POD connector C, the mainframe should beep and display the message POD 5C CONNECTED.

3. Press the POD ID button on the back of the pattern generator probe housing. The mainframe should beep again and display POD 5C.

4. Enter the Trigger Specification menu and set the qualifier for the acquisition probe to 0 (active low).

5. Press START SYSTEM.

6. Enter the Timing Diagram menu. The display should again look like Figure 5-12.

The previous steps have verified the operation of the clock, data, and strobe lines.

7. Enter the Pattern Generator Program sub-menu. Set the lower-left corner of the sub-menu to MODIFY, enter LOGICAL XOR SEQ 0 THROUGH 9 XXXX XXXX 4X, and press EXECUTE. See Figure 5-14

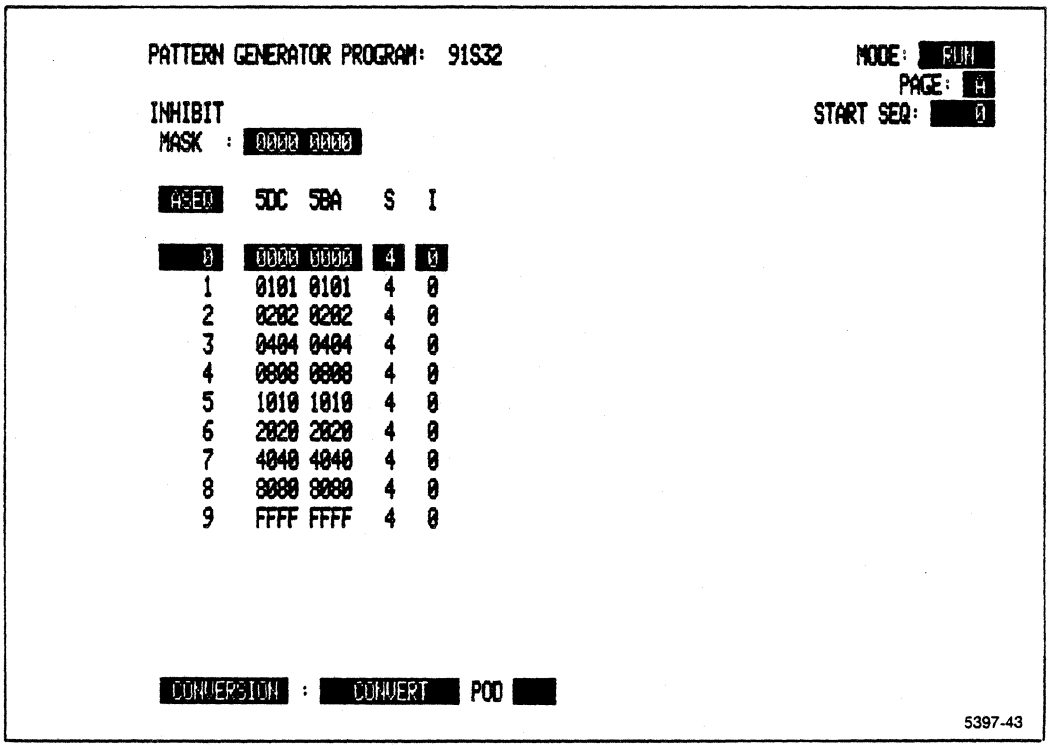


Figure 5-14. Pattern generator setup for POD C check

8. Enter the Timing Diagram menu. Set the qualifier for the data acquisition probe to 1 (active high).

9. Press START SYSTEM.

10. The data acquired should again match Figure 5-12.

(7) Verifying POD Connector B

The following procedure verifies that the 91S32 can transmit data, strobes, and clock signals through POD connector B.

1. Remove the P6464 Pattern Generator Probe from POD connector C of the 91S32 module. Reconnect the probe to POD connector B of the 91S32 module.

2. When the probe is installed in POD connector B, the mainframe should beep and display the message POD 5C CONNECTED.

3. Press the POD ID button on the back of the pattern generator probe housing. The mainframe should beep again and display POD 5B.

4. Enter the Trigger Specification menu and set the qualifier for the acquisition probe to 0 (active low).

5. Press START SYSTEM.

6. Enter the Timing Diagram menu. The display should again look like Figure 5-12.

The previous steps have verified the operation of the clock, data, and strobe lines.

7. Enter the Pattern Generator Program sub-menu. Set the lower-left corner of the sub-menu to MODIFY, and enter LOGICAL XOR SEQ 0 THROUGH 9 XXXX XXXX 2 X. Press the the EXECUTE key. See Figure 5-15.

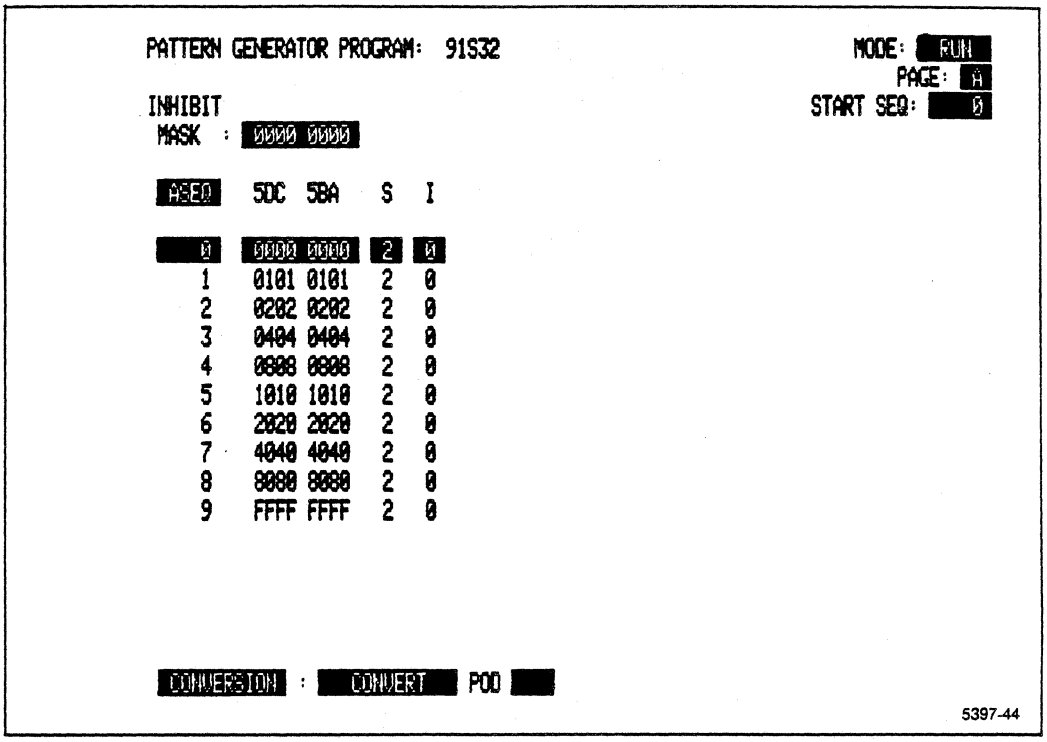


Figure 5-15. Pattern generator setup for POD B check

8. Enter the Timing Diagram menu. Set the qualifier for the data acquisition probe to 1 (active high).

9. Press START SYSTEM.

10. The data acquired should again match Figure 5-12.

(8) Verifying POD Connector A

The next steps verify that the 91S32 can transmit data, strobes, and clock signals through POD connector A.

1. Remove the P6464 Pattern Generator Probe from POD connector B of the 91S32 module. Reconnect the probe to POD connector A of the 91S32 module.

2. When the probe is installed in POD connector A, the mainframe should beep and display the message POD5A CONNECTED.

3. Press the POD ID button on the back of the pattern generator probe housing. The mainframe should beep again and display POD 5A.

4. Enter the Trigger Specification menu and set the qualifier for the acquisition probe to 0 (active low).

5. Press START SYSTEM.

6. Enter the Timing Diagram menu. The display should again look like Figure 5-12.

The previous steps verified the operation of the clock, data and the strobe.

7. Enter the Pattern Generator Program sub-menu. Set the lower-left corner of the sub-menu to MODIFY, and select LOGICAL XOR SEQ 0 THROUGH 9 XXXX XXXX 1 X. Press the EXECUTE key. See Figure 5-16.

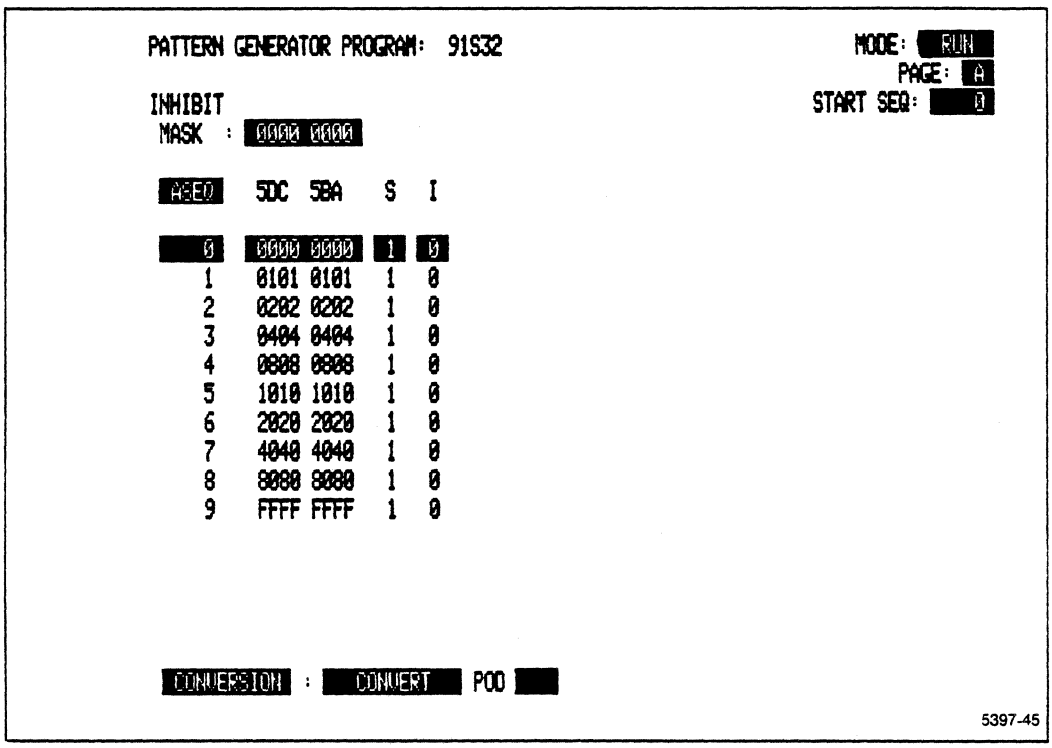


Figure 5-16. Pattern generator setup for POD A check.

8. Enter the Timing Diagram menu. Set the qualifier for the data acquisition probe to 1 (active high).

9. Press START SYSTEM.

10. The data acquired should again match Figure 5-12.

(9) Verifying the PG INHIBIT Line

The following procedure verifies that the 91S32 responds to the PG INHIBIT signal through the external clock probe.

1. Disconnect the strobe lead of the pattern generator probe from the qualifier lead of the data acquisition probe.

2. Connect probes and set up the Configuration sub-menu as follows:

   a. Connect the strobe lead from the pattern generator probe to the PG INHIBIT lead of the external clock probe (the red lead), and connect the P6452 probe to P7C on the Trigger/Time Base module.

   b. Connect the ground of the P6452 external clock probe to the P6454 ground.

   c. Enter the Configuration sub-menu and enter END SEQ 9, FREE RUN, set clock and strobe inhibit masks to 1, and press EXECUTE. See Figure 5-17.

3. Set the program to match Figure 5-18.

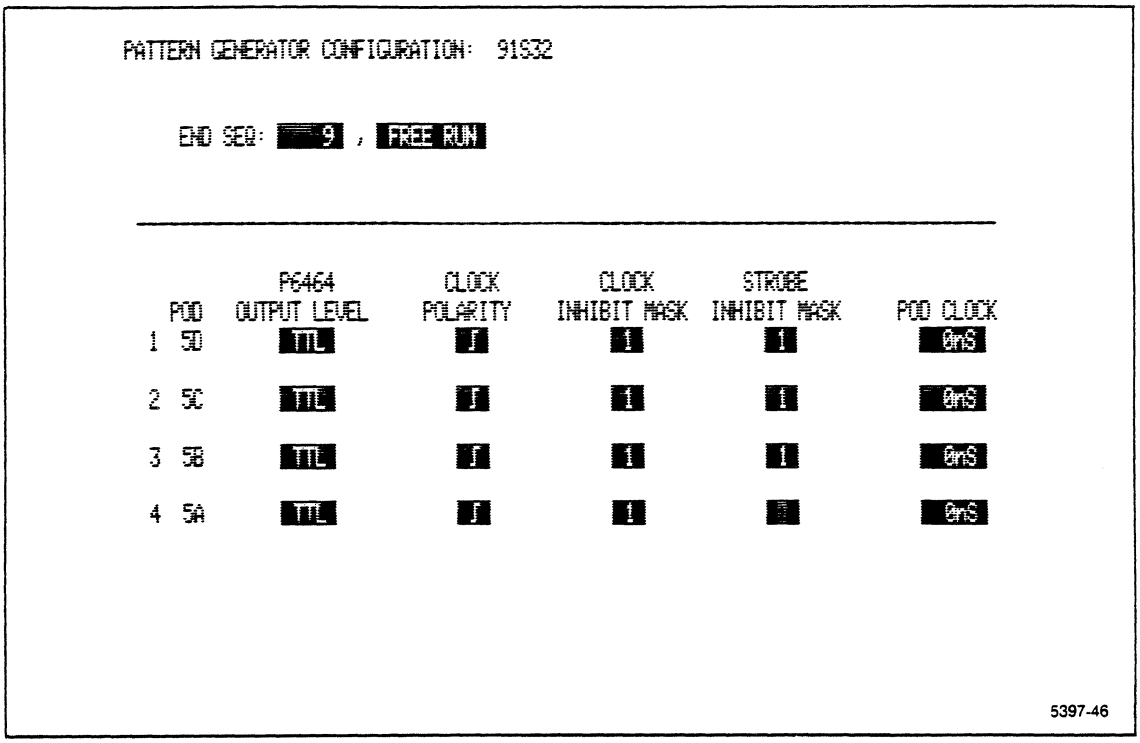


Figure 5-17. Pattern Generator Configuration sub-menu, PG inhibit line test.

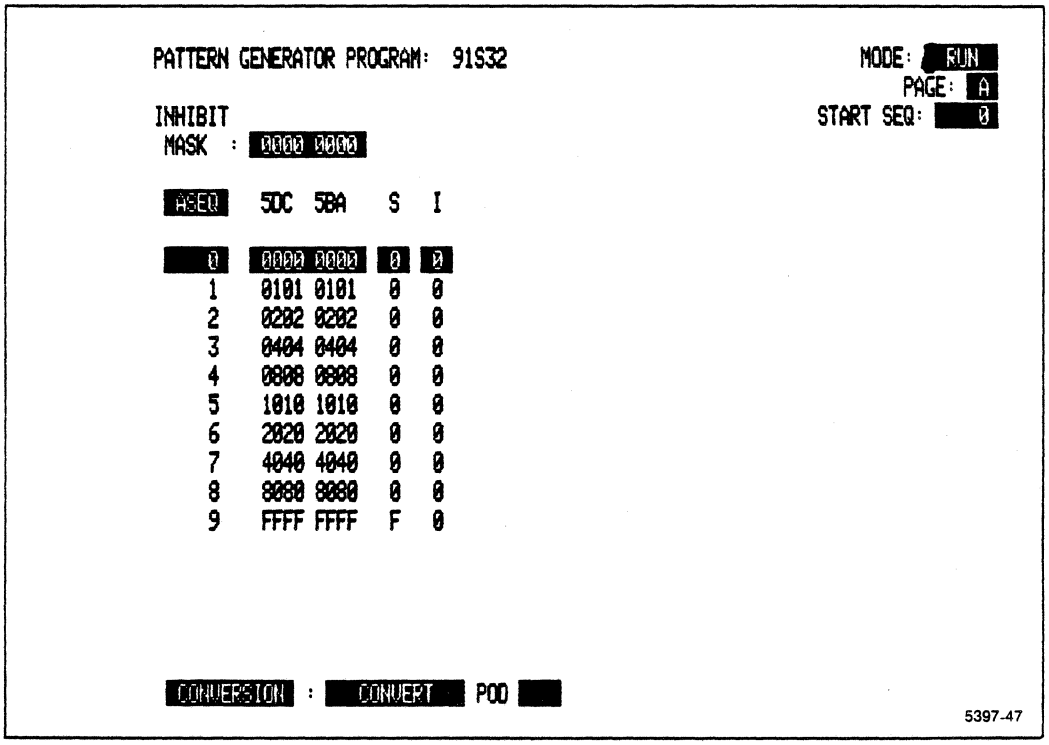


Figure 5-18. Pattern Generator Program menu for PG inhibit line test.

4. Enter the Pattern Generator Timing sub-menu. Set the CLOCK to 50 microseconds.

5. Press START SYSTEM.

6. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-12.

7. Enter the Pattern Generator Probe sub-menu. Set INHIBIT to EXTERNAL 1 ONLY.

8. Press START SYSTEM.

9. When data acquisition is finished, enter the Timing Diagram menu. The display should look like Figure 5-19.

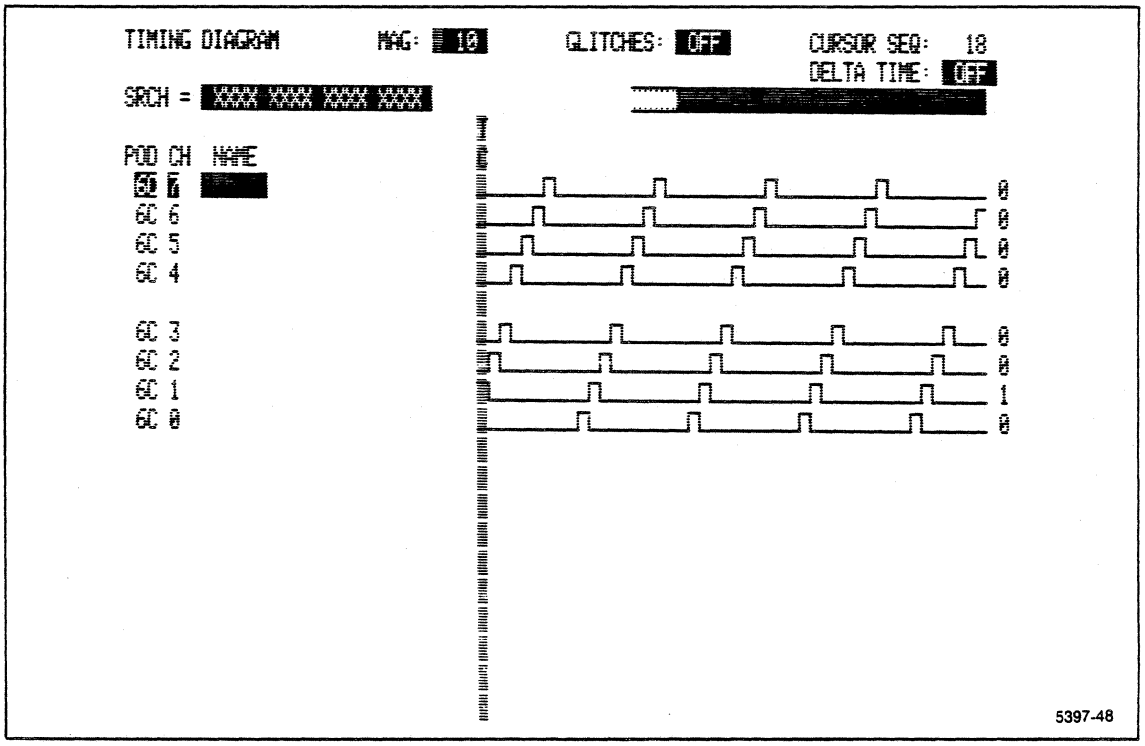


Figure 5-19. Timing Diagram menu, PG inhibit line test.

10. Enter the Pattern Generator Probe sub-menu. Set INHIBIT to INTERNAL 1 ONLY, and set SEQ 9 I column to F.

11. Press START SYSTEM.

12. When data acguisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-19.

13. Enter the Pattern Generator Probe sub-menu. Set the INHIBIT to EXTERNAL 1 AND INTERNAL 1.

14. Press START SYSTEM. Enter the Timing Diagram menu. The display should again look like Figure 5-19.

15. Enter the Pattern Generator Program sub-menu. Set the the lower-left corner of the sub-menu to MODIFY, and enter LOGICAL XOR SEQ 0 THROUGH 9 XXXX XXXX F F. Press EXECUTE. See Figure 5-20. (This step puts Fs in place of 0s in the S and I columns, and 0s in place of Fs from the previous test.)

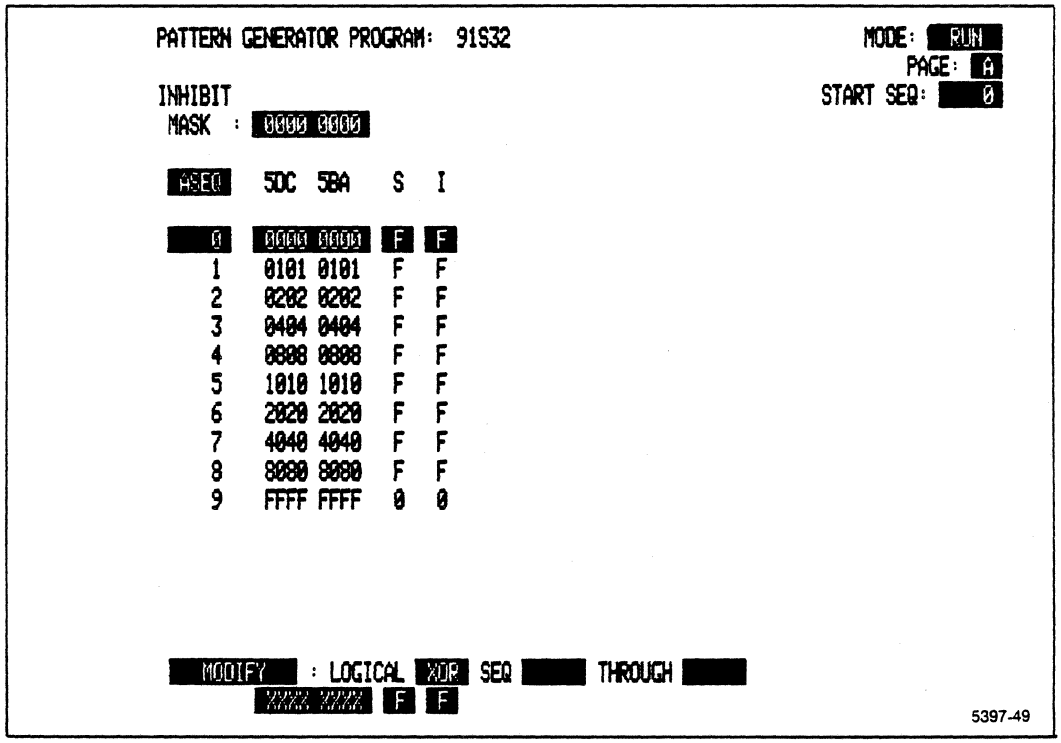


Figure 5-20. Pattern Generator Program Submenu modified, PG inhibit line test.

16. Enter the Pattern Generator Probe sub-menu. Set INHIBIT to EXTERNAL 0 ONLY.

17. Press START SYSTEM.

18. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-19.

19. Enter the Pattern Generator Probe sub-menu. Set INHIBIT to INTERNAL 0 ONLY.

20. Press START SYSTEM.

21. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-19.

22. Enter the Pattern Generator Probe sub-menu. Set the INHIBIT to EXTERNAL 0 OR INTERNAL 0.

23. Press START SYSTEM.

24. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-19.

(10) Verifying the EXTERNAL START Line

The following procedure verifies that the 91S32 responds to the PG START signal through the external clock Probe.

1. Connect the output of the pulse generator to the PG INTERRUPT line (the orange line) on the P6452 external clock probe. Set the signal generator for a 0 to +4 V signal, then set the pulse width and duration for manual trigger.

2. Connect EXT START (orange lead) to the output of the pulse generator.

3. Set the pattern generator program to again match Figure 5-18.

4. Enter the Pattern Generator Probe sub-menu. Select EXTERNAL START ON rising edge.

5. Press START SYSTEM, then manually trigger the pulse generator.

6. When displayed on the Timing Diagram menu, the data acquired from the pattern generator should again look like the data shown in Figure 5-12.

A display like Figure 5-12 means that the interrupt signal is being properly received and processed. The next steps verify the operation of the external start signal.

7. Enter the Pattern Generator Probe sub-menu. Select EXTERNAL START ON rising edge.

8. Press START SYSTEM, then manually trigger the pulse generator.

9. When displayed on the Timing Diagram menu, the data acquired from the pattern generator should again look like the data shown in figure 5-12.

10. Disconnect the PG INTERRUPT line from the signal source.

11. Press START SYSTEM.

12. The display should show WAITING FOR 91A08 TRIGGER.

13. Press STOP.

(11) Verifying the PG CLK Line

The following procedure verifies the transmission of the PG CLK signal through the external clock probe. These steps require the use of an external clock source. The recommended clock source is a square wave or pulse generator with an output that oscillates between ground and +5 V with an 8 ns pulse width and a frequency of 50 MHz.

1. Connect the output of the signal generator to the PG CLK line (brown) on the P6452 external clock Probe.

2. The signal generator must have a common ground with the probes. To accomplish this, connect the ground of the signal generator to the two clips that connect the data acquisition probe ground senses to the external clock probe ground line.

3. Enter the Pattern Generator Probe sub-menu. Select EXTERNAL START DISABLED.

The probes and the signal generator are now connected and the test can be performed.

4. Enter the Pattern Generator Timing sub-menu. Set the pattern generator clock to external rising edge.

5. Adjust the pattern generator program to again match Figure 5-18.

6. Enter the Trigger Specification menu and set the acquisition clock to external falling edge.

7. Press START SYSTEM.

8. When acquisition is complete, examine the Timing Diagram menu. The data acquired from the pattern generator should again look like the data shown in Figure 5-12.

A display such as Figure 5-12 indicates that the pattern generator external clock is being properly received and processed. The next steps verify the inversion operation of the external clock signal.

9. Enter the Pattern Generator Timing sub-menu. Set the pattern generator clock to external falling edge.

10. Press START SYSTEM.

11. When acquisition is complete, examine the Timing Diagram menu. The data acquired from the pattern generator should again look like the data shown in Figure 5-12.

(12) Verifying the PG PAUSE Line

The next steps verify that the 91S32 responds to the PG PAUSE signal through the external clock Probe. These steps require the use of an oscilloscope and an external signal. The recommended clock source is a square wave with a 10 microsecond period and an output between ground and +5 V.

1. Disconnect the strobe line from the inhibit line.

2. Enter the Pattern Generator Timing sub-menu. Set the CLOCK to 200 ns.

3. Enter the Pattern Generator Probe sub-menu. Set the INHIBIT to DISABLED. Set PAUSE to 0.

4. Connect the output of the pulse generator to the PG PAUSE line (yellow) of the P6452 probe.

5. Set up the oscilloscope as follows:

   a. Attach the probe for channel 1 of the oscilloscope to the external signal and set sensitivity for 2 V/div.

   b. Attach the probe for channel 2 of the oscilloscope to the P6464 probe clock podlet (podlet must also be grounded).

   c. Set the oscilloscope to trigger on a rising edge in channel 1.

   d. Attach the ground leads of the probes to the ground of the P6452 and the P6464 probe.

6. Press START PAT GEN.

7. The oscilloscope display should look like the one shown in Figure 5-21.

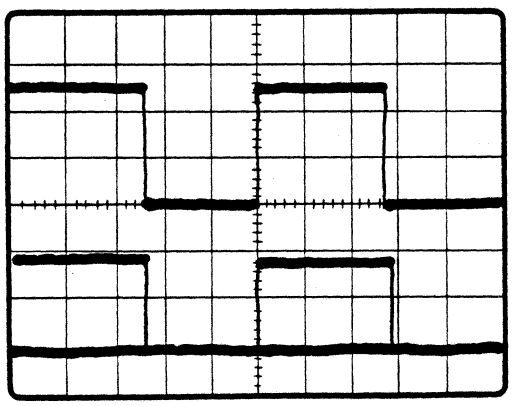


Figure 5-21. PG PAUSE line response, PAUSE = 0.

8. Enter the Pattern Generator Probe sub-menu. Select PAUSE ON 1.

9. Press START PAT GEN.

10. The oscilloscope display should look like Figure 5-22.

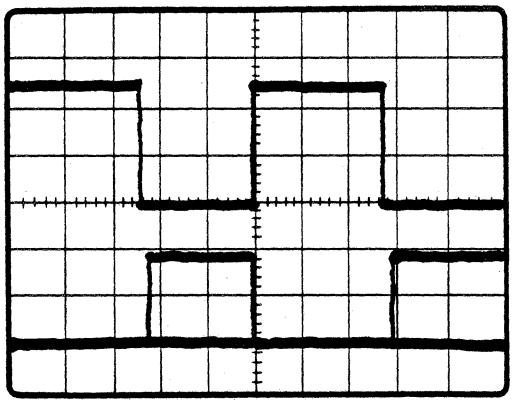


Figure 5-22. PG PAUSE line response, PAUSE = 1.

91S32 PATTERN GENERATOR FUNCTIONAL CHECK WITH 91S16

You will need the following equipment to perform this procedure:

DAS 9100 mainframe with V1.11 firmware and 22 A +5 V Power Supply

91S16 Pattern Generator Module

Two P6464 Pattern Generator Probes

P6460 External Clock Probe

P6452 Data Acquisition Probe

91A08 Data Acquisition Module and P6454 100 MHz Clock Probe

+5 V external power supply, Tektronix PS503A or equivalent

(13) Mainframe setup for the functional check of 91S32 with 91S16.

The following procedures verifies the operation of a 91S32 used with a 91S16.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so can damage the module or sub-assembly.

1. Turn off the mainframe.
2. Install a 91A08 Acquisition Module in slot 6.
3. Install the 91S16 in slot 4 of the mainframe.

NOTE

J402 must be in place on the 91A32, regardless of the configuration.

Also, the mainframe will not operate with more than one 91S16 Pattern Generator Module installed at the time of power-up. Make sure there are no 91S16 duplicates in the mainframe.

4. Install the 91S32 to be checked in slot 3 of the DAS mainframe. If there is another 91S32 module in the main frame, remove it.

5. Place jumpers on J302, J304, J306, J308, J310, J312, J314, J316, J318, J320, J322, J324, J202, J204, and J102 of the 91S32, then connect the flat cable from P2 of the 91S16 to P2 of the 91S32.

(14) Executing the Diagnostic Self-test

The following procedure runs all available self-test diagnostics on the 91S32 module.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select diagnostic tests for the 91S32 module in slot 3.

3. Select SINGLE mode, then run all functions.

4. Repeat steps 2 and 3 for slot 4.

(15) Probe Setup for the Functional Check

1. Connect a P6464 Pattern Generator Probe to POD connector A of the 91S32.

2. Connect a P6464 Pattern Generator Pprobe to POD connector A of the 91S16.

3. Connect the Data Acquisition Probe to the 91A08 Acquisition Module.

4. Connect the pattern generator probe from the 91S32 to the data acquisition probe with the diagnostic lead set.

5. Connect the P6460 external clock probe to POD connector C of the 91S16.

6. Install a flying lead set in the P6460 external clock probe. Connect the ground lead of the external clock probe to one of the grounds of the P6464 Pattern Generator Probe.

7. Connect the P6464 100 MHz clock probe to its connector on the 91A08 module in slot 6.

8. Connect the IN line of the P6464 100 MHz clock probe to the clock output of the 91S16's Pattern Generator Probe.

9. Connect the REF line of the P6464 100 MHz clock probe to the unused GND SENSE line on the pattern generator probe of the 91S16.

10. Adjust the external power supply for +5 V using a digital multimeter. Connect common and ground together if a Tektronix PS503A Power Supply is used. Turn off the power supply.

11. Connect one red lead from each P6464 probe to each +5 V source on the power supply. (The Tektronix PS503A can only drive two probes.)

12. Connect all black and green leads from the P6464s together, and connect them to the ground on the power supply.

13. Connect the power supply ground to all probe grounds and V-ref leads of the podlets.

(16) Initial Menu Setup for the Functional Check

The next steps organize the menus so that the remainder of the functional check will require a minimum of menu manipulation.

1. Leave the Diagnostics menu by pressing the PATTERN GENERATOR key. In the Pattern Generator Program sub-menu, verify that the pattern generator clock is set to 40 ns. Go to the Timing sub-menu and select the 40 ns clock.

2. Adjust the 91S16 program in the Program sub-menu to match Figure 5-23.

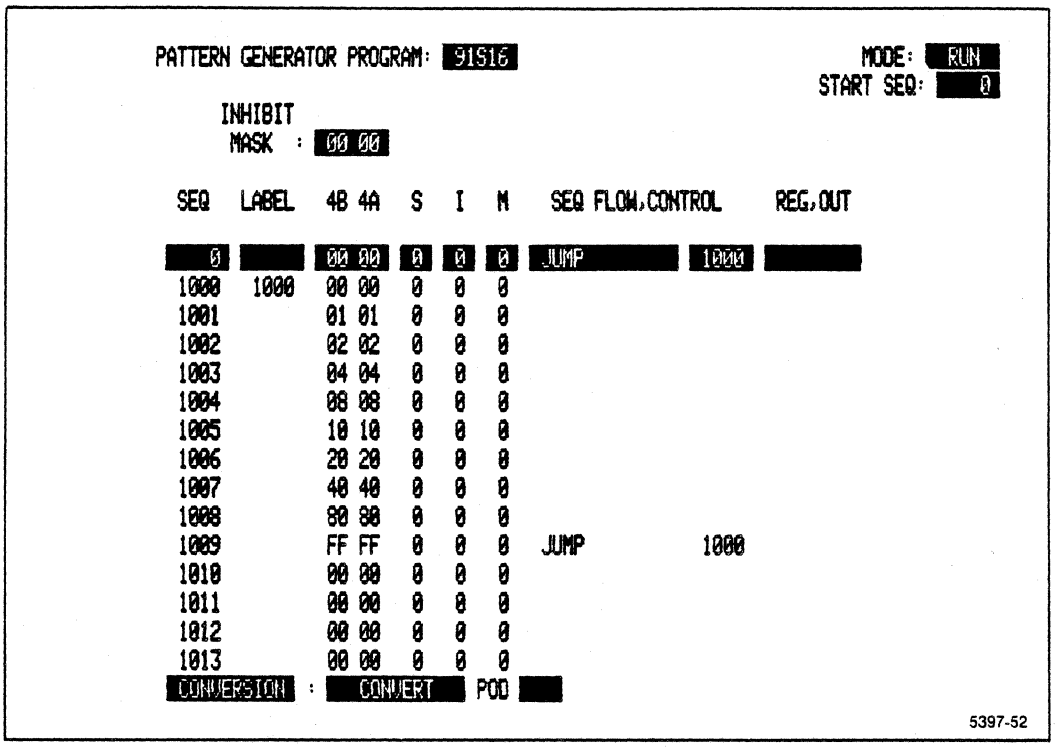


Figure 5-23. 91S16 Program sub-menu setup, 91S32 with 91S16.

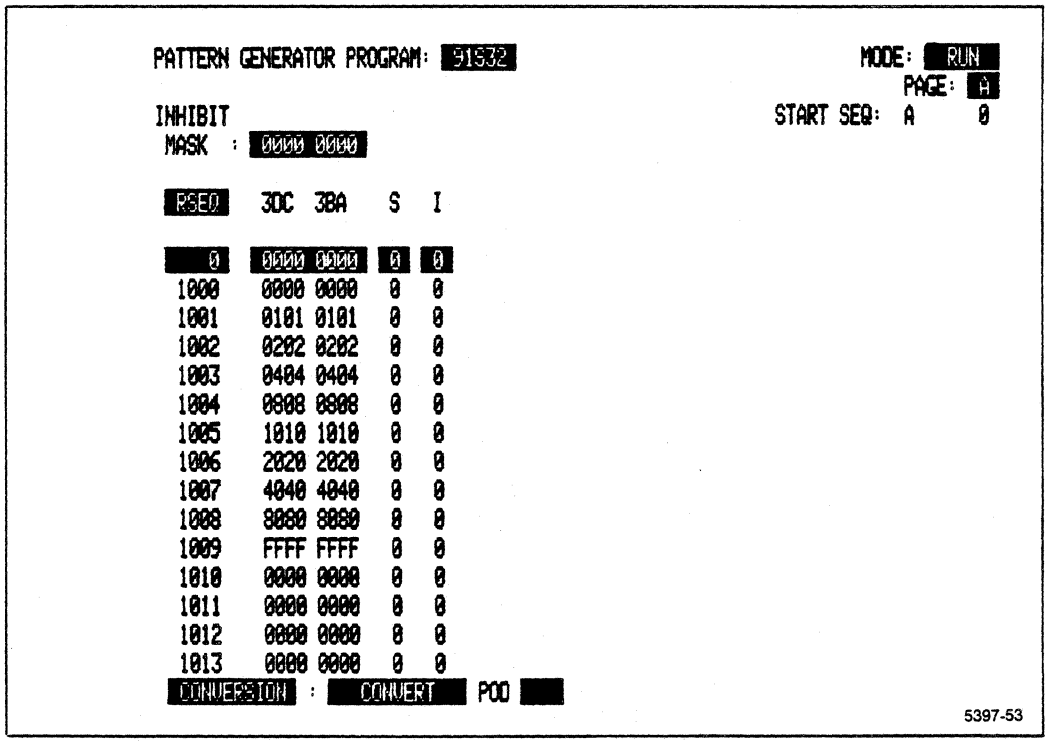


Figure 5-24. 91S32 Program sub-menu setup, 91S32 with 91S16.

3. Set the 91S32 pattern generator program to match Figure 5-24.

4. In the Trigger Specification menu, set the acquisition clock to external falling edge. The trigger word for the 91A08 can be left at DON'T CARE (X).

(17) Verifying POD Connector A of 91S32

The following procedure verifies that the 91S32 can transmit data through the POD connector A.

1. Press the START SYSTEM key.

2. Enter the Timing Diagram menu.

3. Press the POD ID button on the back of the acquisition probe. Read the POD number on the DAS screen. Adjust the Timing Diagram menu to show data from this POD.

4. Set the magnification of the Timing Diagram to 10. This should create a display like Figure 5-25. The actual position of the cursor and trigger will depend on the type of acquisition module used. The 91A08 should trigger on sequence 18.

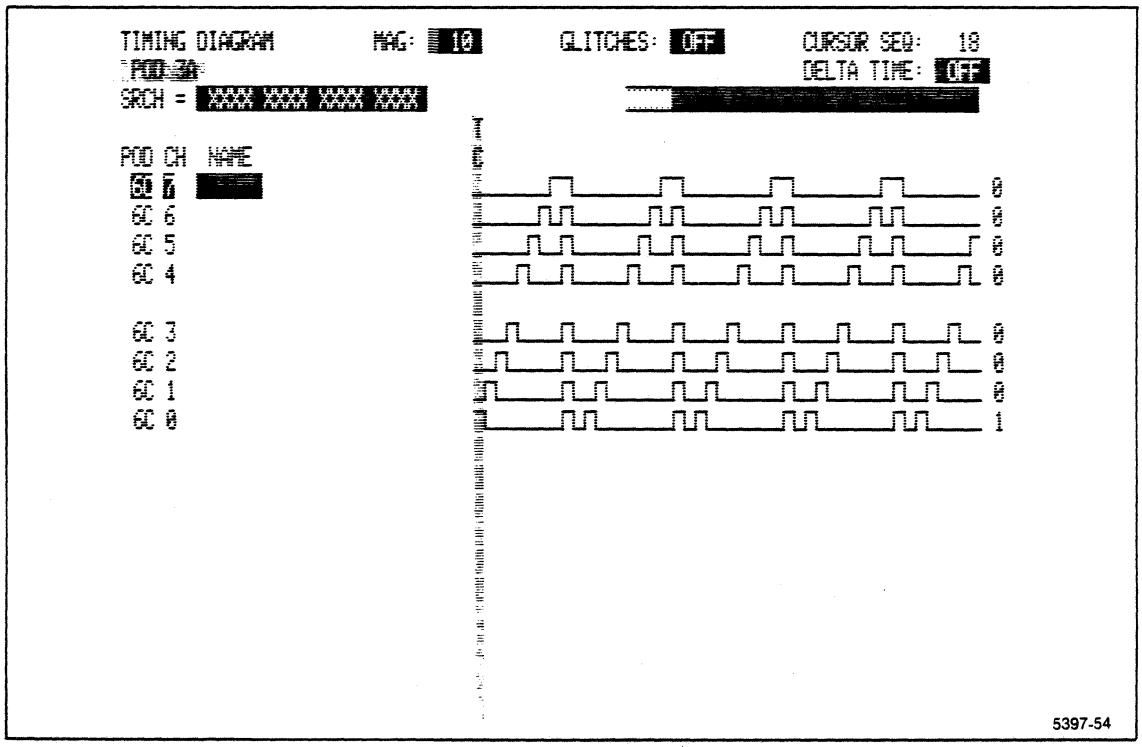


Figure 5-25. Timing Diagram menu, POD connector A.

(18) Verifying Clock Divider

The following procedure verifies that 91S16 can divide the clock and send it to the 91S32 pattern generator.

1. Enter the Pattern Generator CONFIGURATION 91S32 mode. Set the 91S32 MODE to SEQUENTIAL END SEQ A: 9.

2. Set the 91S32 pattern generator program to match Figure 5-26.

3. Select the Trigger menu and select 1 microsecond for the 91A08 clock.

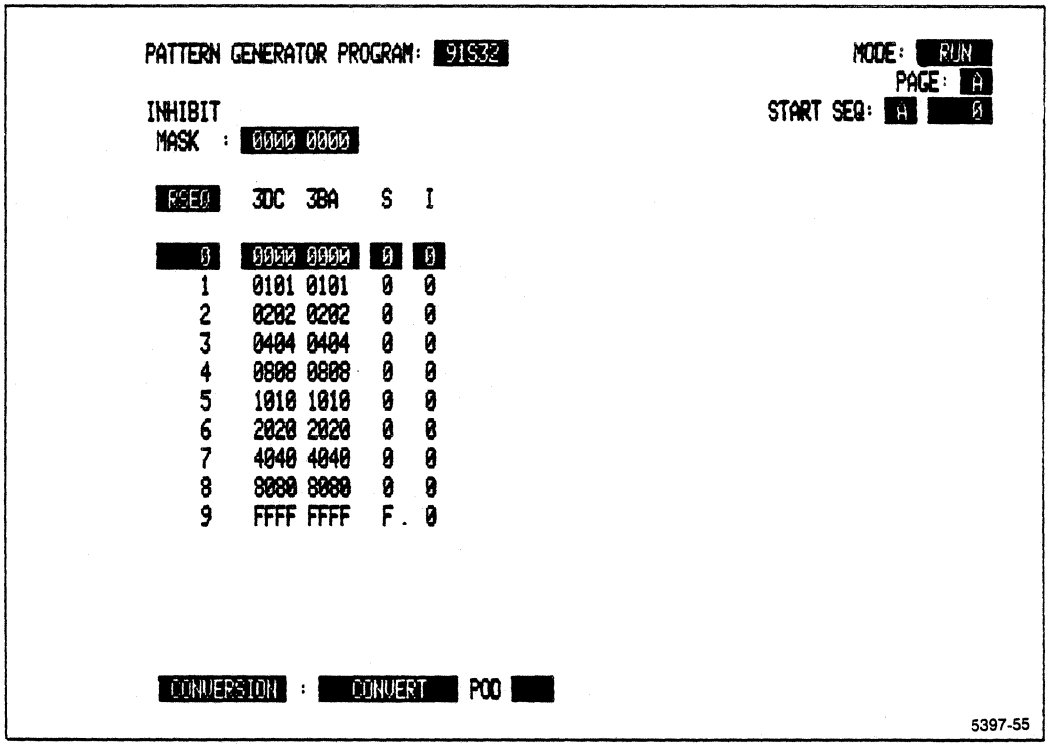


Figure 5-26. 91S32 Program sub-menu for clock divider test.

4. Press START SYSTEM.

5. When data acquisition is complete, enter the Timing Diagram menu.

6. Set the magnification of the Timing Diagram to 5. this should create a display like Figure 5-27.

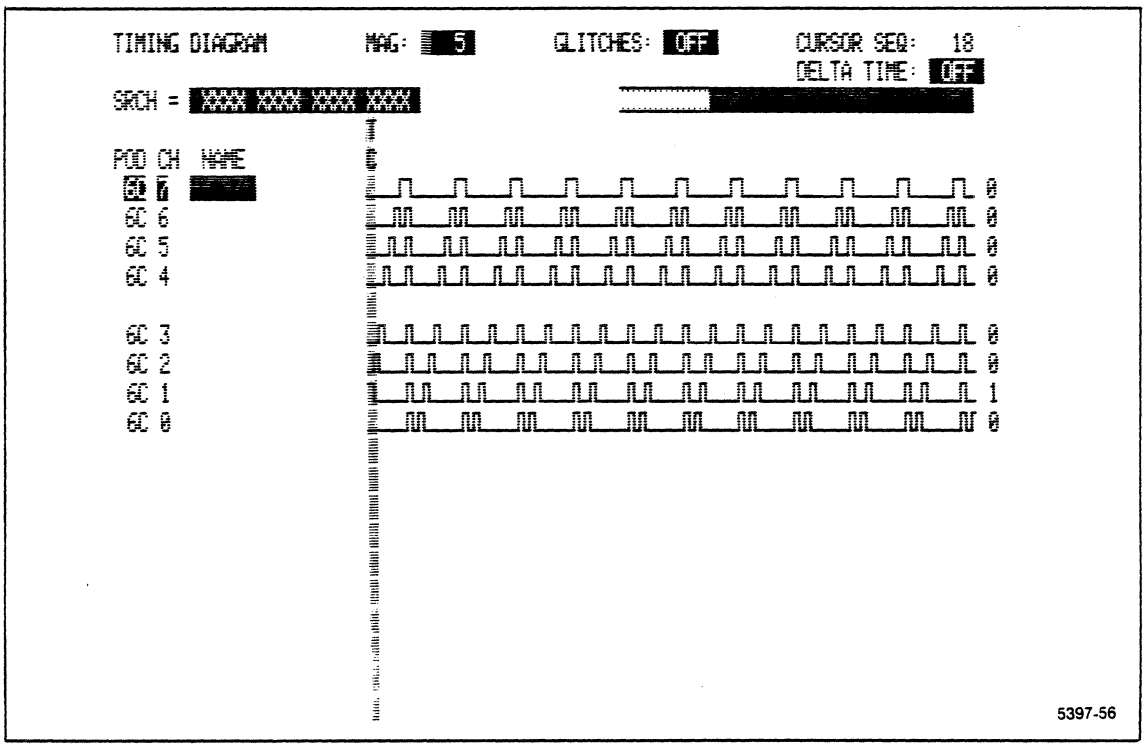


Figure 5-27. Timing Diagram menu for clock divided by 1.

7. Enter the Pattern Generator Configuration 91S32 sub-menu. Set the 91S32 CLOCK to 91S16 DIVIDED BY 2.

8. Press the START SYSTEM key.

9. When data acquisition is complete, enter the Timing Diagram menu. The display should look like Figure 5-28.

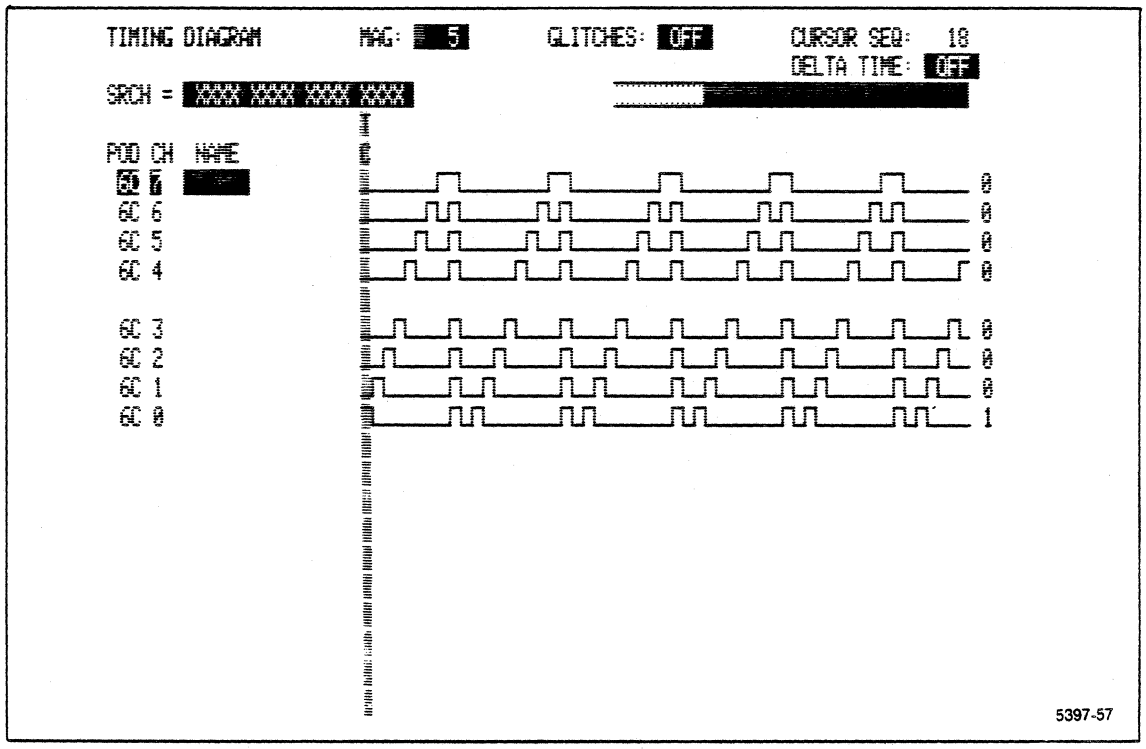


Figure 5-28. Timing Diagram menu with 91S16 clock divided by 2.

10. Enter the Pattern Generator Configuration 91S32 sub-menu. Set the 91S32 CLOCK to 91S16 DIVIDED BY 4.

11. Press the START SYSTEM key.

12. When data acquisition is complete, enter the Timing Diagram menu. The display should look like Figure 5-29.

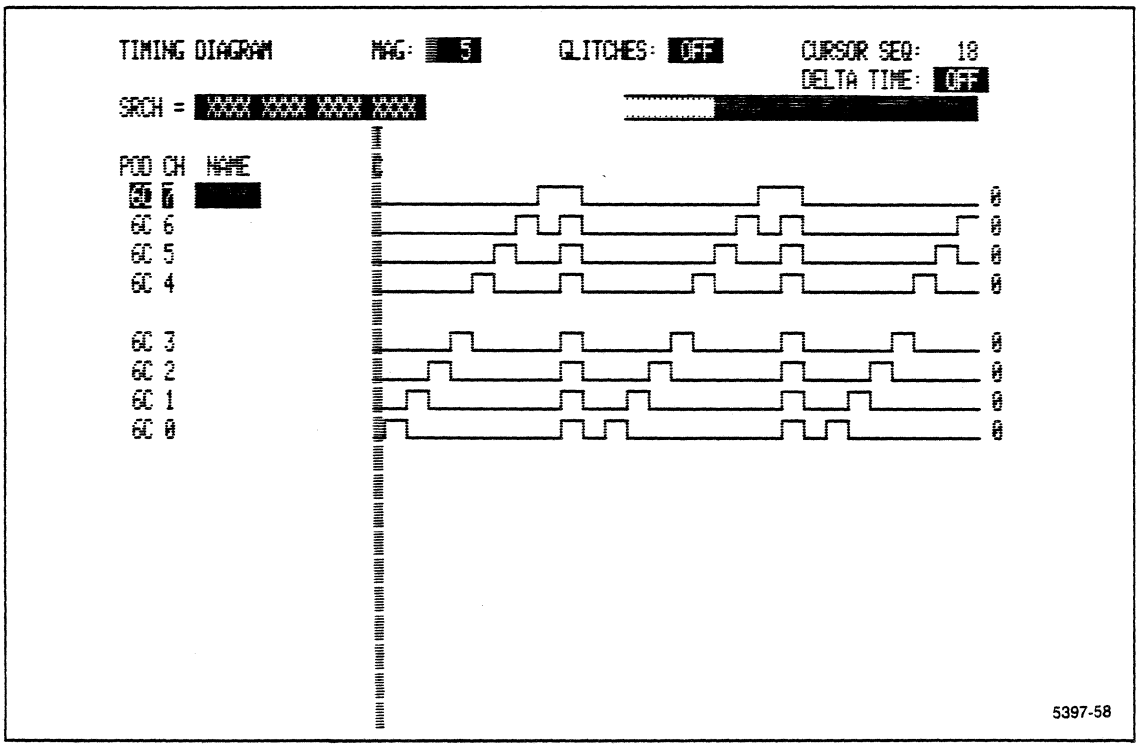


Figure 5-29. Timing Diagram menu with clock divided by 4.

(19) Verifying the PG INHIBIT Line from 91S16 to 91S32

The following procedure verifies that the 91S32 responds to the PG INHIBIT signal through the external clock probe connected to 91S16.

1. Connect the P6460 probe to the 91S16.

2. Connect the P6460 inhibit lead (red) to the P6464 strobe output of 91S32 POD A.

3. Enter the 91S32 Pattern Generator menu. Select PROGRAM: RUN, and set the INHIBIT MASK field in the Pattern Generator Program menu to 0000 0000 (default).

4. Enter the Pattern Generator Configuration: 91S32 sub-menu. Set 91S32 MODE to FOLLOWS 91S16. Set the 91S32 CLOCK to 91S16 DIVIDED BY 1. Set the configuration clock to match Figures 5-30 and 5-31.

5. Set the Program sub-menus to match Figures 5-32 and 5-33.

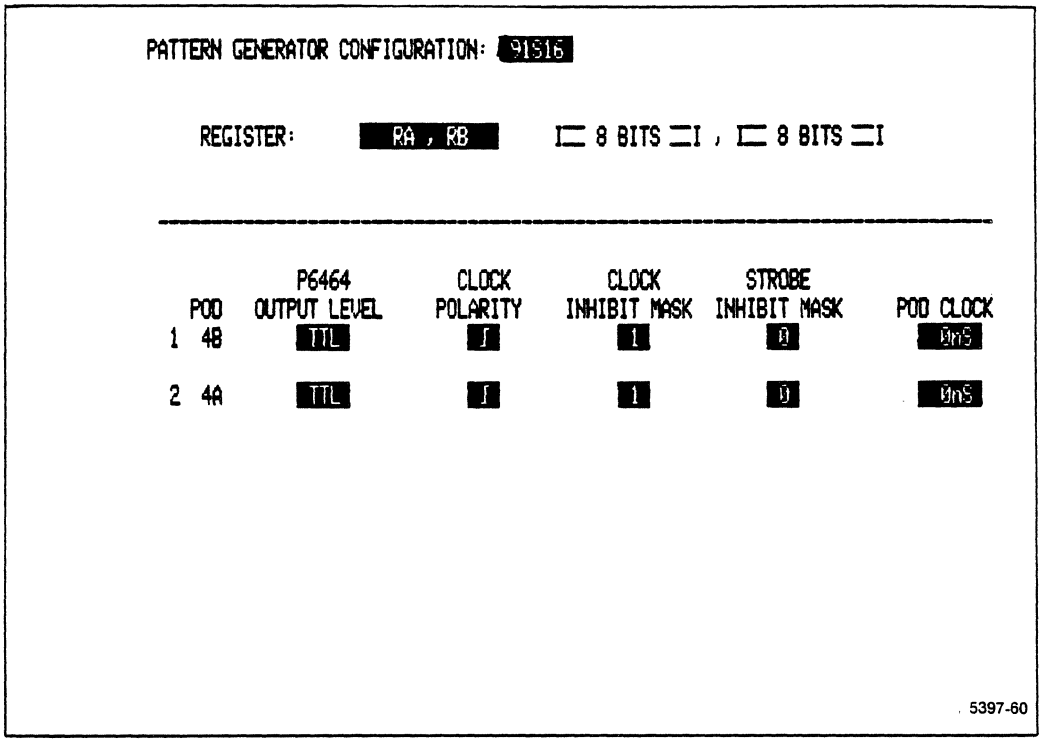


Figure 5-30. 91S16 configuration clock setup for PG inhibit test.

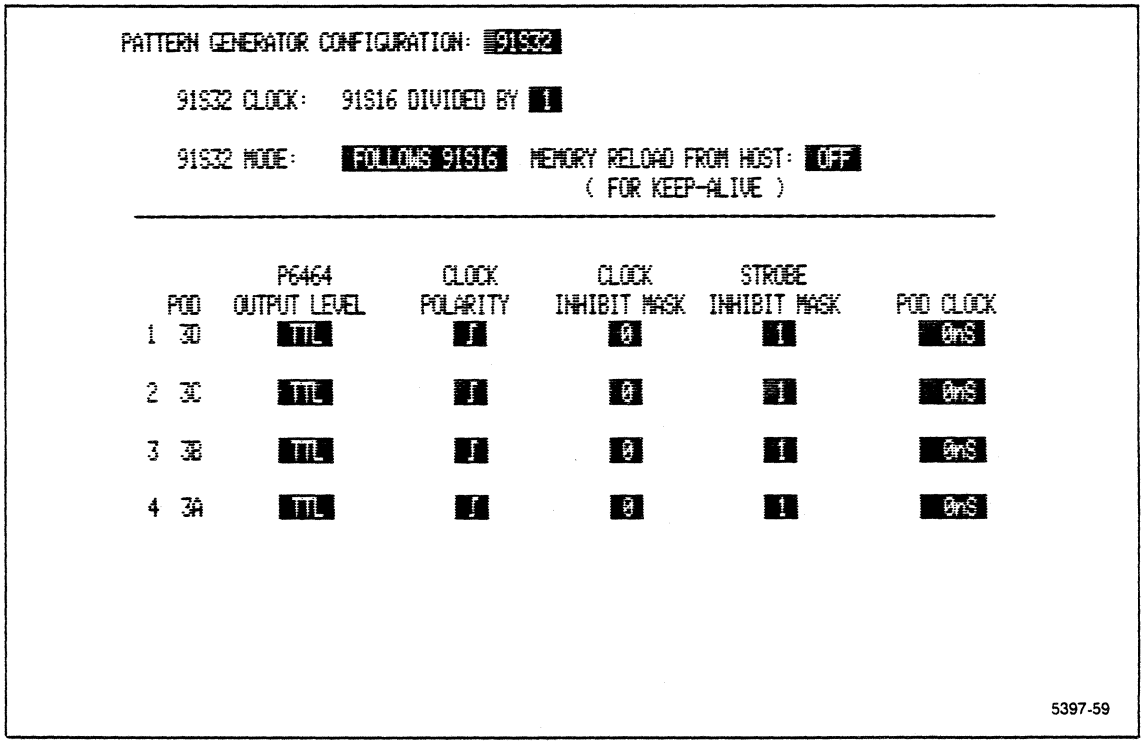


Figure 5-31. 91S32 configuration clock setup for PG inhibit test.

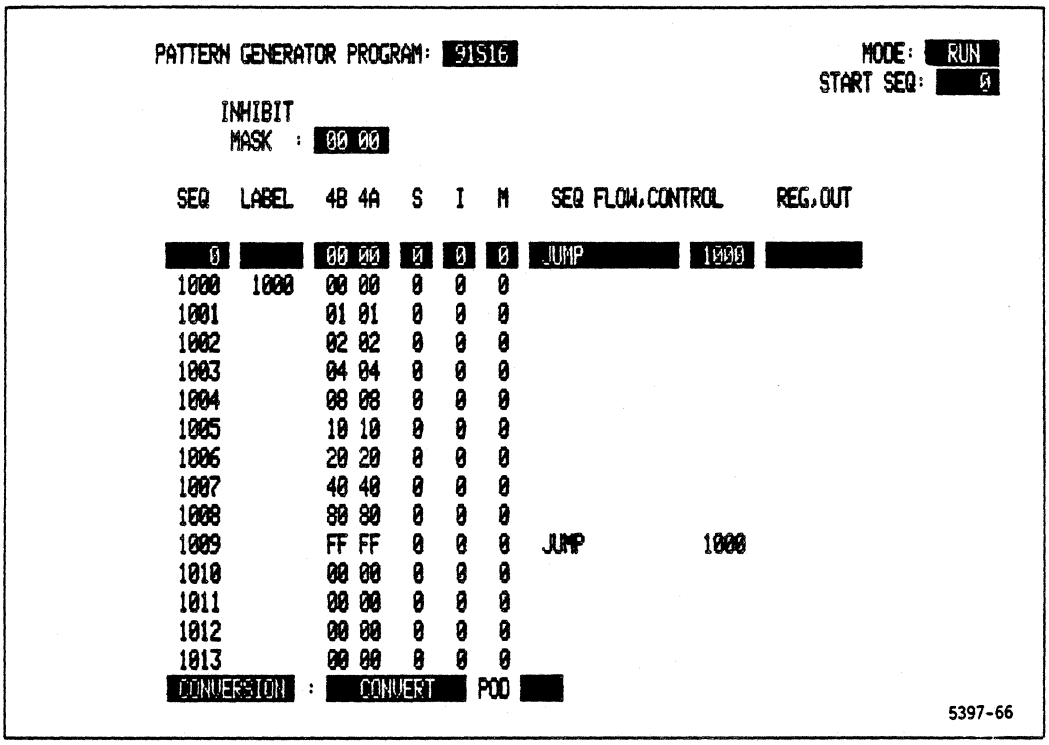


Figure 5-32. 91S16 Program sub-menu for PG inhibit test.

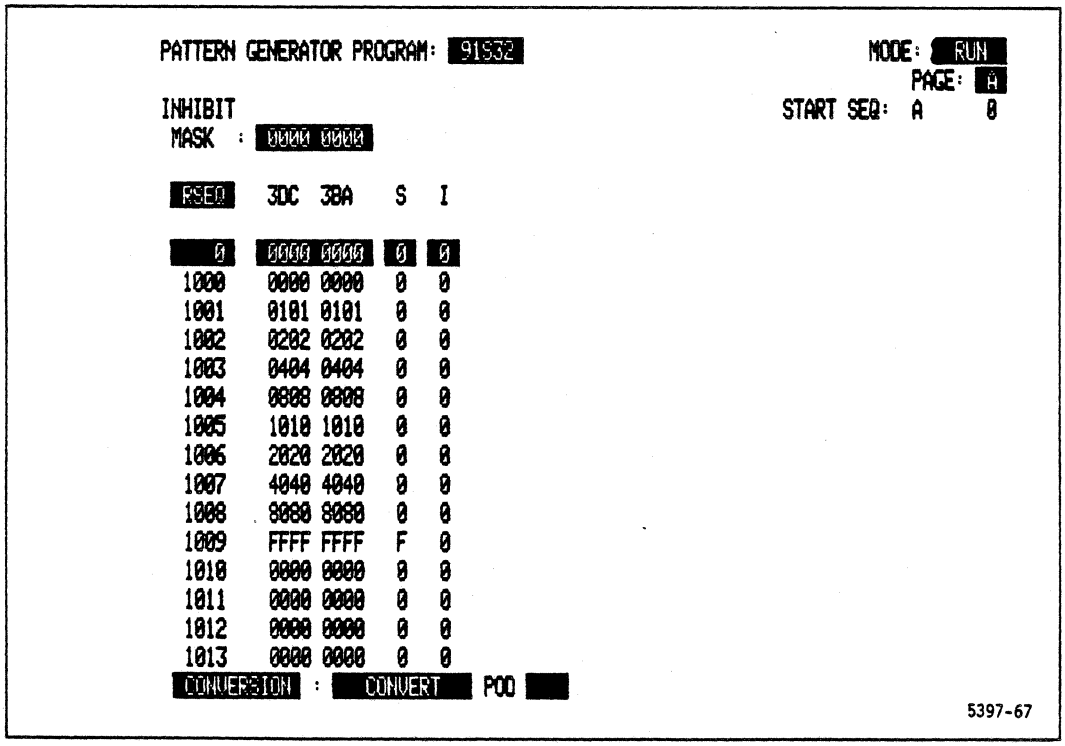


Figure 5-33. 91S32 Program sub-menu for PG inhibit test.

6. Enter the Pattern Generator Timing sub-menu. Set the CLOCK to 50 microseconds.

7. Enter the Pattern Generator Probe sub-menu. Set the INHIBIT to EXTERNAL 1 ONLY.

8. Enter the Trigger Specification menu and set the 91A08 clock to EXTERNAL falling edge.

9. Press START SYSTEM.

10. When data acquisition is finished, enter the Timing Diagram menu and set the magnification factor to 10. The display should look like Figure 5-34.

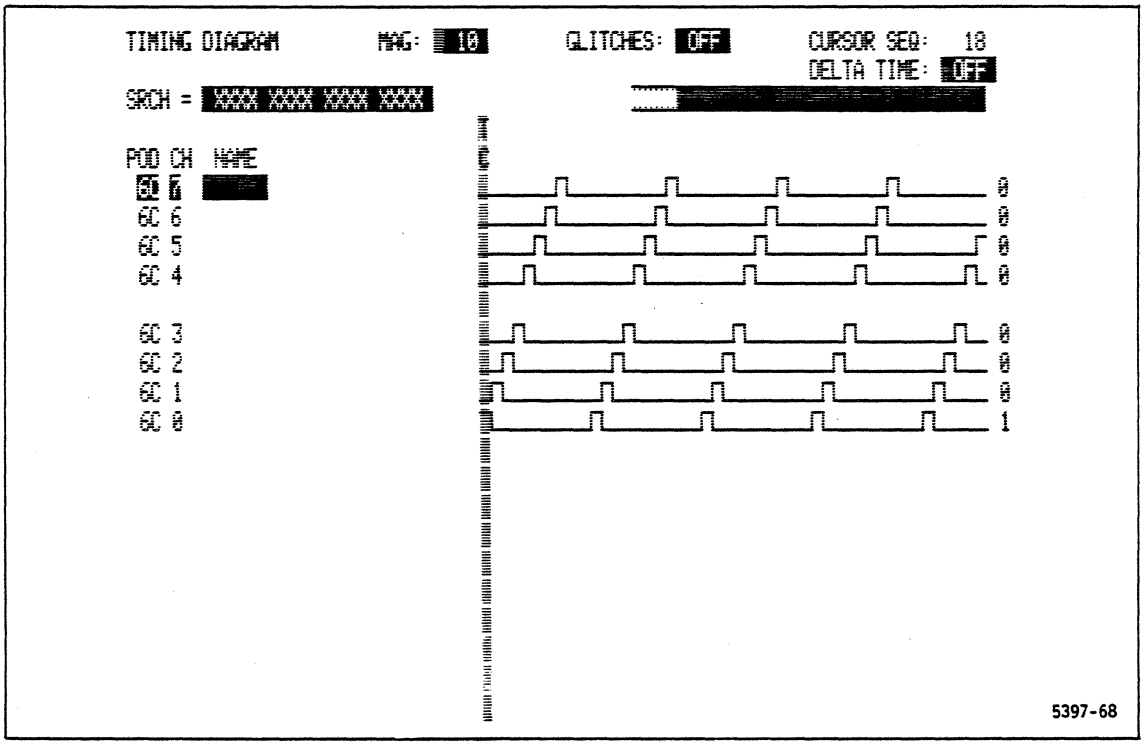


Figure 5-34. Timing Diagram menu for the PG inhibit test.

(20) Verifying the POD Delay

The following procedure verifies the POD to POD delay. These steps require the use of an oscilloscope.

1. Connect the P6464 Pattern Generator Probes to PODs A and B.

2. Enter the Pattern Generator Timing sub-menu. Set the pattern generator clock to 200 ns.

3. Enter the Pattern Generator Program sub-menu and program the following.

SEQ	0	0000	0000	0	0
	1	FFFF	FFFF	F	0

4. Enter the Configuration sub-menu and enter END SEQ 1 FREE RUN.

5. Set up the oscilloscope as follows:

   a. Attach the probe for channel 1 of the oscilloscope to the P6464 probe clock output of POD-A.

   b. Attach the probe for channel 2 of the oscilloscope to the P6464 probe clock output of POD-B.

   c. Provide power to probes A and B.

   d. Set the oscilloscope to trigger on a rising edge in channel 1 and set the sweep rate to 2 ns/div.

   e. Attach the ground leads of the probes to the V-ref of the P6464 probe clock outputs.

6. Press START PAT GEN.

7. The rising edge of channel 1 and channel 2 should be approximately the same.

8. Set the Pattern Generator Timing sub-menu POD CLOCK of 3A to +5 ns using the INCR key.

9. Press START PAT GEN.

10. The rising edge of channel 2 should occur 5 ns before the rising edge of channel 1. See Figure 5-35.

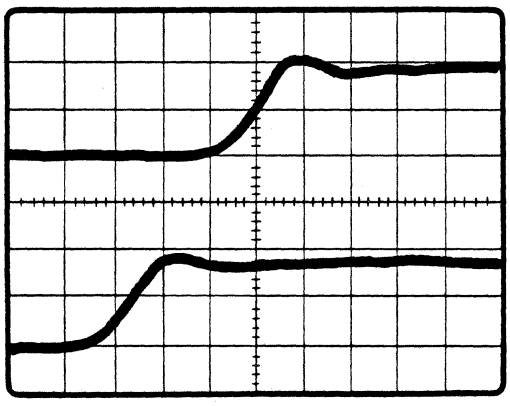
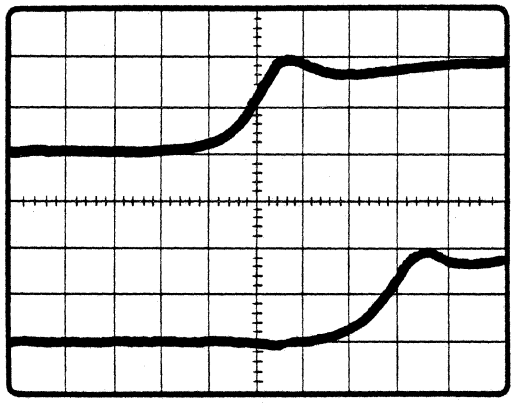


Figure 5-35. +5 ns POD delay.

11. Set the Pattern Generator Timing sub-menu POD CLOCK for POD 5A to -5 ns.

12. Press START PAT GEN.

13. The rising edge of channel 2 should occur 5 ns after the rising edge of channel 1. See Figure 5-36.



5397-70

Figure 5-36. -5 ns POD delay.

14. Set the Pattern Generator Timing sub-menu POD CLOCK for 5A to 0 ns. Change the selected POD field from 5A to 5B.

15. Set the Pattern Generator Timing sub-menu POD CLOCK for 5B to -5 ns.

16. Press START PAT GEN.

17. The rising edge of channel 2 should occur 5 ns before the rising edge of Channel 1.

18. Set the Pattern Generator Timing sub-menu POD CLOCK for 5B to +5 ns.

19. Press START PAT GEN.

20. The rising edge of channel 2 should occur 5 ns after the rising edge of channel 1.

CAUTION

Do not move probes from pod to pod with the pattern generator started. Doing so can damage the pattern generator module.

21. Set the Pattern Generator Timing sub-menu POD CLOCK for 5B to 0 ns.

22. Move the P6464 pattern generator probe to POD connector C.

23. Set the Pattern Generator Timing sub-menu POD CLOCK for 5C to -5 ns.

24. Press START PAT GEN.

25. The rising edge of channel 2 should occur 5 ns before the rising edge of channel 1.

26. Set the Pattern Generator Timing sub-menu POD CLOCK for 5C to +5 ns

27. Press START PAT GEN.

28. The rising edge of channel 2 should occur 5 ns after the rising edge of channel 1.

29. Set the Pattern Generator Timing sub-menu POD CLOCK for 5C to 0 ns.

30. Press START PAT GEN.

31. The rising edge of channel 2 and Channel 1 should approximately coincide.

32. Make sure the pattern generator is stopped, then move the P6464 Pattern Generator Probe to POD connector D.

33. Set the Pattern Generator Timing sub-menu POD CLOCK for 5D to -5 ns.

34. Press START PAT GEN.

35. The rising edge of channel 2 should occur 5 ns before the rising edge of channel 1.

36. Set the Pattern Generator Timing sub-menu POD CLOCK for 5D to +5 ns.

37. Press START PAT GEN.

38. The rising edge of channel 2 should occur 5 ns after the rising edge of channel 1.

39. Set the Pattern Generator Timing sub-menu POD CLOCK for 5C to 0 ns.

40. Press START PAT GEN.

41. The rising edge of channel 2 and channel 1 should approximately coincide.

(21) Verifying the data delay

The following procedure verifies the clock-to-data delay. These steps require the use of an oscilloscope.

1. Enter the Pattern Generator Program sub-menu and enter the following program.

```
SEQ    0    0000    0000    0  0
       1    FFFF    FFFF    F  0
```

2. Enter the Configuration sub-menu and enter END SEQ 1 FREE RUN.

3. Connect as many P6464 probes as can be powered by the +5 V external power supply to the 91S32, starting at POD 5A. (The Tektronix PS503A can power only two P6464s.)

4. Set all clock delays in the Pattern Generator Configuration sub-menu to 0 ns.

5. Enter the Pattern Generator Timing sub-menu. Set the POD field to 5A. Set each data and strobe delay to +5 ns.

6. Set up the oscilloscope as follows:

   a. Attach the probe for channel 1 of the oscilloscope to the P6464 probe clock output of POD 5A.

   b. Attach the probe for channel 2 of the oscilloscope to the P6464 probe DATA 0 output of POD 5A.

   c. Set the oscilloscope to trigger on a rising edge in channel 2.

   d. Attach the ground leads of the oscilloscope probes to the ground leads of the pattern generator probes.

7. Press START PAT GEN.

8. The rising edge of channel 1 should occur 5 ns before the rising edge of channel 2.

9. Move the probe for channel 2 sequentially from DATA 0 through DATA 1, 2, 3, 4, 5, 6, 7, and Strobe of POD 5A. Each channel waveform should be the same as the signal at DATA 0 output.

10. Repeat steps 4 through 8 for PODs 5B, 5C, and 5D.

This completes the functional check procedure for the 91S32 Pattern Generator Module using a 91S32-only configuration.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so can damage the module or sub-assembly.

ADJUSTMENT PROCEDURES

91S16 ADJUSTMENT PROCEDURE

Test point and adjustment locations for this procedure can be found in the 91S16 Parts Location drawing in the Diagrams section of this addendum.

DAC Adjustment for the P6460 Input Probe

The 91S16 Pattern Generator uses one P6460 Probe. The threshold level for the P6460 is adjusted on the 91S16 module. The following instruments are required for this adjustment. Equivalent test instruments may be substituted.

NOTE

This adjustment cannot be performed unless DAC U320 (an NE5018) is lot date number 8335 or smaller.

Equipment Required for Threshold Test

Equipment	Specification	Recommended Type
DAS Mainframe		DAS 9100 Series with V1.11 firmware and 22 A, +5 V power supply
TM500 Mainframe		TM503 or higher
Digital Multimeter	0.05% dc V accuracy	DM501
Module Extender		Main Extender Board from DAS Service Maintenance Kit
*Threshold Fixture		Local manufacture, see following procedure. See also Figure 5-37.

*This is the same fixture used as a service tool for the Tektronix 1240 Logic Analyzer. If you have the 1240 fixture, it is not necessary to build another one.

Equipment Required for Threshold Fixture Construction

Qty.	Description	Part Number
1	Terminal Connector Holder (2 holes by 8 holes)	352-0484-00
5	Mini PV Female Connectors	131-0484-00
1	Resistor, 10.5 K, 1%	321-0291-00
3	Wires, 26-gauge, 1-inch long	

Construction Procedure. Assemble the Threshold Fixture as follows:

1. Connect three of the Mini-PV connectors to three lengths of wire.
2. Connect the remaining two Mini-PV connectors to the resistor, one at each end.
3. Install the three wire/Mini PV connector combinations into holes 1, 4, and 7 of the Terminal Holder Connector.
4. Solder the three free ends of the wires together.
5. Install the two ends of the resistor/Mini-PV connector combinations in holes 13 and 16 of the Terminal Holder Connector.

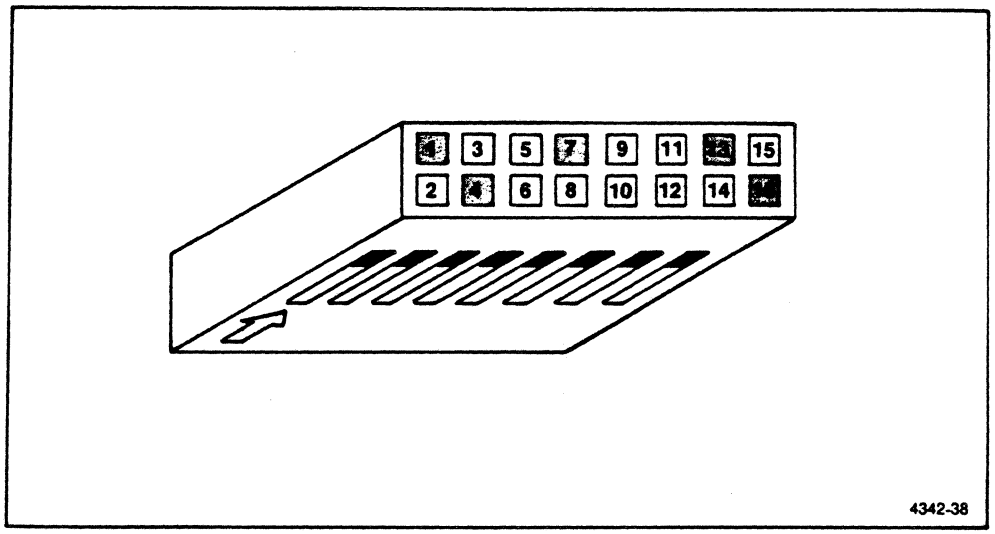


Figure 5-37. Threshold Fixture. (The arrow on the fixture indicates the pin-1 end.)

DAC Threshold Adjustment. Adjust the 91S16 DAC threshold according to the following procedure. This procedure assumes that the 91S16 is installed on the DAS Main Extender Board, and that the DAS is powered up.

CAUTION

Do not install or remove a module from the DAS mainframe with the power turned on. Doing so can damage the module.

1. Install the threshold fixture into POD C (J140) of the 91S16.

NOTE

As a substitute for steps 2 through 5, use the DAS Diagnostics. Select SINGLE mode and test function 6 in the Diagnostics menu, then press START SYSTEM.

2. Enter the sub-menu by pressing the START PAT GEN key and the SETUP key.
3. Select the VAR mode in the P6460 INPUT THRESHOLD field.
4. Move the cursor to the voltage field to the right of VAR.
5. Keep pressing the DECR key until you select becomes 0.00V.
6. Press START PAT GEN.
7. Connect the DMM high lead to test pin THRES, and connect the low lead to GND.
8. Adjust R390 for a DMM reading of 0.00 V $\pm$2 mV.
9. Change the VAR value to +6.35 V (maximum value) with the INCR key.
10. Press START PAT GEN.
11. Adjust R392 for -1.587 V $\pm$2 mV.
12. Set the VAR to -6.40 V (minimum value) with the DECR key.
13. Press START PAT GEN.

14. Check for +1.600 V ±6 mV by switching between the two range extremes. Readjust R390, if necessary, to equalize the difference in voltage between the two settings within the specified 6 mV.

15. Disconnect the DMM leads and remove the Threshold Fixture.

Adjusting Delay Lines in Clock Control

The 91S16 has a total of six different variable delay lines in three different circuitry areas. There is one adjustment in the register timing circuitry, three in the POD clock positioning circuitry, and two in the deskew circuitry between the POD clocks.

The following equipment is necessary to perform this adjustment procedure.

DAS 9100 Series Mainframe with V1.11 firmware and 22A +5 V power supply

DAS Main Extender Board

350 MHz oscilloscope with two channels

Two P6230 probes for the oscilloscope

+5 V Probe Power Supply, Tektronix PS503A or equivalent

Alignment tool, p/n 003-1134-00

91S16/32 overlay for the DAS keyboard

NOTE

The same menu setup and equipment used to adjust these delay lines is used for subsequent procedures.

CAUTION

Use only the alignment tool p/n 003-1134-00 or damage to components may result.

This procedure assumes that the 91S16 is installed on the DAS Main Extender Board, and that the DAS is powered up and has passed all diagnostics.

CAUTION

Do not install or remove a module from the DAS mainframe with the power turned on. Doing so can damage the module.

1. Ensure power is off, then remove covers from all delay lines on the extended 91S16.
2. Connect one P6464 probe to POD connector A and another P6464 to POD connector B.
3. Power up the DAS.
4. Enter the Pattern Generator menu by pressing the PATTERN GENERATOR key.
5. Select the Pattern Generator Program sub-menu and write the following program.

SEQ	LABEL	A	B	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0	A	FF	FF	0	0	0		
1		00	00	0	0	0	JUMP	A

6. Enter the sub-menu by pressing the SETUP key, then press SELECT to enter the Timing sub-menu.
7. Set the pattern generator clock to 200 ns.

Delay Line Adjustment for the First Latch's Clock in the Clock Line

1. Attach the probe for channel 1 of the oscilloscope to TP280-2, and connect probe ground leads to convenient GND test points. (TP280 is the reference point for the system clock.)
2. Attach the probe for channel 2 of the oscilloscope to TP610-2, and connect probe ground leads to convenient GND test points.

3. Set the oscilloscope to trigger on channel 1.

4. Press START PAT GEN. Adjust the oscilloscope for a display like Figure 5-38.

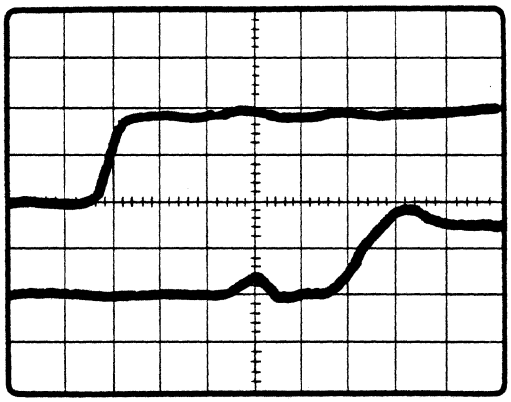


Figure 5-38. First-latch clock line delay.

5. Adjust delay line DL800 so that the rising edge on channel 2 is 25.5 ns ±1.0 ns after the rising edge on channel 1.

6. Move the position of all remaining variable delay lines except DL800 to approximate center.

Adjusting Delay Lines for the Clock Line in the P6464 Probe

1. Attach the probe for channel 1 of the oscilloscope to TP720-2, and attach the probe for channel 2 to TP780-2. Connect probe grounds to GND test points.

2. Press START PAT GEN. Adjust delay line DL720 so that the rising edge of channel 1 is 3 ns ±0.5 ns after the rising edge of channel 2. (Channel 1 is clock, channel 2 is data.) See Figure 5-39. Replace cover on DL720.

3. Move the probe for channel 2 to TP760-2. Adjust delay line DL740 so that the rising edge in channel 2 is 0 ns ±0.5 ns after the rising edge in channel 1. Replace cover on DL740.

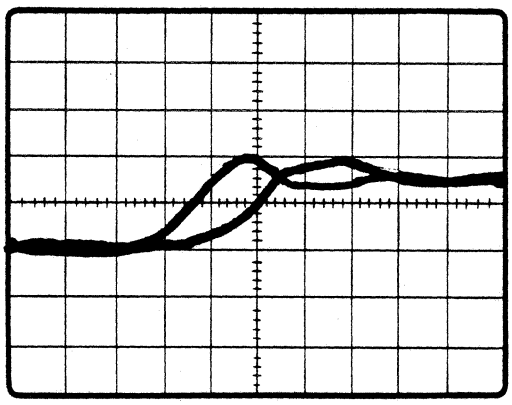


Figure 5-39. P6464 clock line delay.

Adjusting Delay Lines for the POD clock in Clock Positioning

1. Enter the Timing sub-menu, then set the POD B clock delay to -5 ns. Set POD A clock delay to 0 ns (default for POD A). See Figure 5-40.

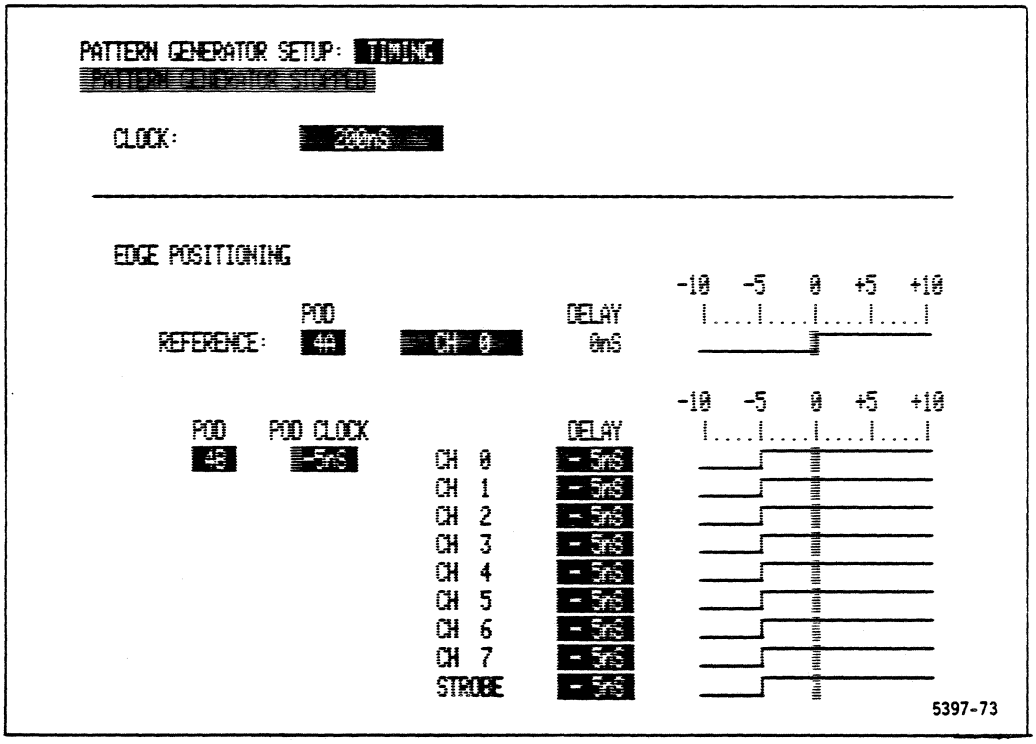


Figure 5-40. POD clock line delay line setup.

2. Press START PAT GEN.

3. Adjust delay line DL760 so that the rising edge in channel 1 is 5.0 ns ±0.25 ns after the rising edge in channel 2. See Figure 5-41. Reinstall cover on DL760.

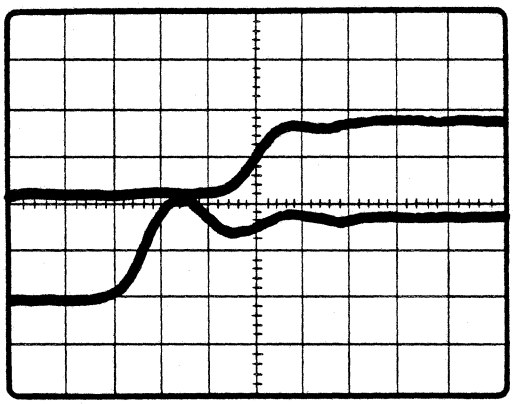


Figure 5-41. Clock line delay for delay line DL760.

4. Set POD B clock delay to +5 ns in the sub-menu and press START PAT GEN. Adjust delay line DL780 so that the rising edge of channel 1 occurs 5.0 ns ±0.25 ns before the rising edge of channel 2. See Figure 5-42.

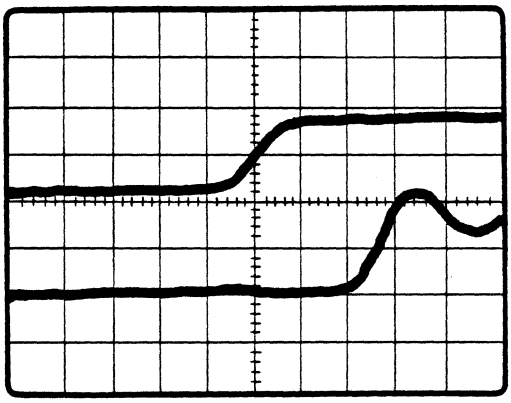


Figure 5-42. Clock line delay for delay line DL780.

Delay Line Adjustment for the Last Latch Clock

1. Move the oscilloscope channel 1 probe to test point TP280-2, and the probe for channel 2 to test point TP700-2.

2. Select the Timing sub-menu, then set the POD A clock delay to -5 ns. Press START PAT GEN. (Leave the POD B clock delay as it is.)

3. Adjust delay line DL700 so that the rising edge of channel 2 occurs 35.0 ±0.25 ns after the rising edge of channel 1. See Figure 5-43.

4. Reinstall the cover on DL700.

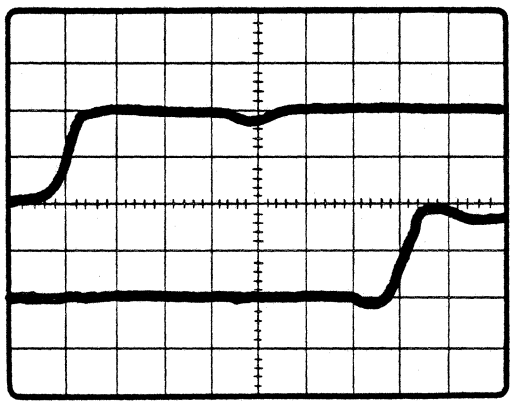


Figure 5-43. Clock line delay for DL700.

91S32 ADJUSTMENT PROCEDURE

Test point and adjustment locations for these procedures can be found in the Parts Location drawing in the Diagrams section of this addendum.

Delay Timing Adjustment

You will need the following equipment to perform this procedure.

DAS 9100 Series Mainframe with V1.11 firmware and 22 A +5 V power supply

DAS Main Extender Extender Board

350 MHz oscilloscope with two channels

Two P6230 oscilloscope probes

Delay line alignment tool, p/n 003-1134-00

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while power is on. Doing so can damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove all 91S32 or 91S16 Pattern Generator Modules from the mainframe.
3. Adjust the square-pin shorting jumpers on the Main Extender Board to accept a 91S32 module (slots 1 through 6).
4. Insert the Main Extender Board in the slot where the 91S32 was removed. Install the 91S32 to be tested on the extender. Remove the covers from all delay lines on the 91S32.
5. Attach square-pin shorting jumpers J206 and J208 of the 91S32.

6. Connect the four P6464 Pattern Generator Probes to the 91S32.

7. Turn on the DAS. After the power-up sequence is successfully completed, enter the 91S32 Pattern Generator menu.

8. Enter the Pattern Generator Timing sub-menu and set the clock to 200 ns.

9. Enter the Configuration sub-menu and select END SEQUENCE 2047, FREE RUN.

10. Check PODs A through D to ensure delays are 0 ns (default).

11. Connect oscilloscope probes and set up the oscilloscope as follows:

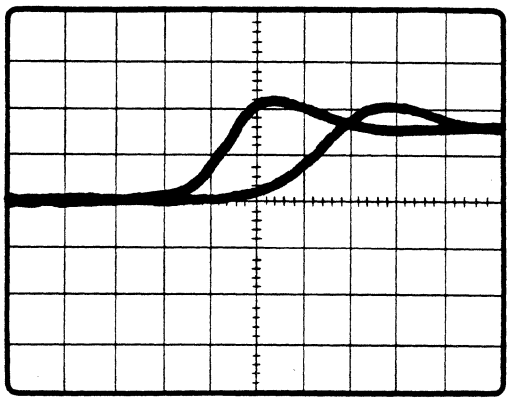
    a. Channel 1 to TP500.

    b. Channel 2 to TP580.

    c. Connect probe grounds to GND test points near TP500 and TP580.

    d. Trigger on a rising edge in channel 1.

12. Press START PAT GEN and adjust the oscilloscope to show a display like Figure 5-44.



5397-77

Figure 5-44. 91S32 pre-adjustment setup.

13. Adjust DL240 so that the pulse delay between channel 1 and channel 2 is 4 ns (±0.25 ns). Reinstall the cover on DL240.

14. Connect the channel 1 probe to TP580 and the channel 2 probe to TP600. Set the oscilloscope to trigger on a rising edge in channel 1.

(14) (Tight specification): Connect the channel 1 probe to the P6464 probe clock output of POD A. Connect the channel 2 probe to the P6464 clock output of POD B. Attach the ground leads of the oscilloscope probes to the grounds of the P6464s. Trigger the oscilloscope on the rising edge of channel 1.

15. Adjust DL260 so the pulse delay between channel 1 and channel 2 is 0 ns (±0.25 ns) see Figure 5-45. Reinstall the cover on DL260.

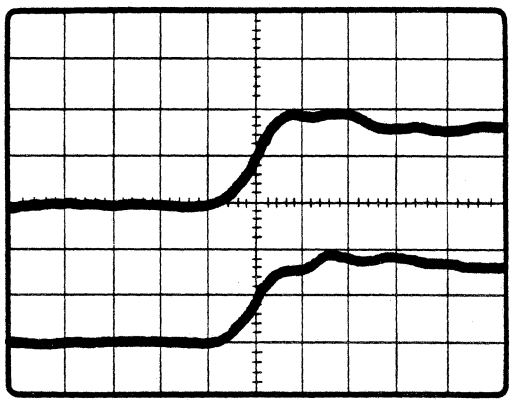


Figure 5-45. 91S32 timing delay for DL260.

16. Move the channel 2 probe to TP620.

(16) (Tight Specification): Move the channel 2 probe to the P6464 clock output of POD C. Attach the ground lead of the channel 2 probe to the ground of the P6464 clock probe.

17. Adjust DL280 so that the pulse delay between channel 1 and channel 2 is 0 ns (±0.25 ns). Reinstall the cover on DL280.

18. Move the channel 2 probe to TP640.

(18) (Tight Specification): Move the channel 2 probe to the P6464 probe clock output of POD D. Attach channel 2 probe ground to the ground of the P6464 clock probe.

19. Adjust DL300 so that the pulse delay between channel 1 and channel 2 is 0 ns (±0.25 ns). Reinstall the cover on DL300.

Adjusting 5 ns POD-to-POD Delay

20. Connect the channel 1 oscilloscope probe to TP580 and the channel 2 probe to TP600. Connect the probe ground leads to the grounds associated with those test points. Set the oscilloscope to trigger on a rising edge in channel 2.

(20) (Tight Specification): Attach the channel 1 oscilloscope probe to the P6464 probe clock output of POD A. Attach the channel 2 probe to the P6464 probe clock output of POD B. Attach the ground leads of the oscilloscope probes to the grounds of the P6464 clock probes. Trigger the oscilloscope on a rising edge in channel 2.

21. Select the Timing sub-menu and set POD A delay value to 0 ns, and set POD B delay value to -5 ns.

22. Press START PAT GEN, then adjust the oscilloscope for a display like Figure 5-46.

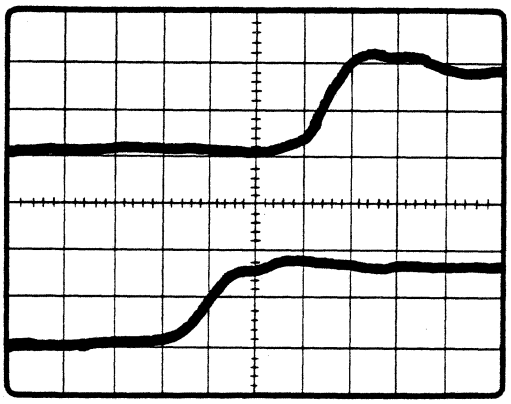


Figure 5-46. Setup for -5 ns POD-to-POD delay adjustment.

23. Adjust DL200 so that the pulse delay between channel 1 and channel 2 is 5 ns (±0.25 ns). Reinstall the cover on DL200.

24. Set the POD A delay to 0 ns and POD B delay to +5 ns. Trigger the oscilloscope on a rising edge in channel 1.

25. Press START PAT GEN and adjust the oscilloscope for a display like Figure 5-47.

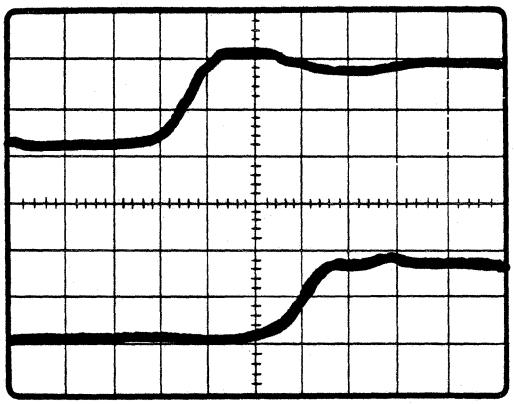


Figure 5-47. Setup for +5 ns POD to POD delay.

26. Adjust DL220 so that the pulse delay between channel 1 and channel 2 is 5 ns (±0.25 ns). Resinstall the cover on DL220.

27. Connect the channel 1 oscilloscope probe to TP200 and the channel 2 probe to TP500.

28. Adjust DL140 so that the pulse delay between rising edges of channel 1 and channel 2 is 33 ns (±0.5 ns). See Figure 5-48. Reinstall the cover on DL140.

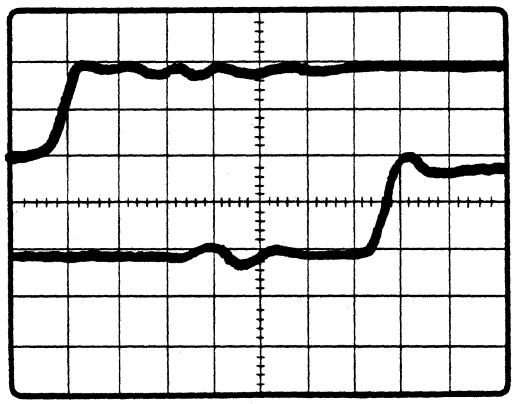


Figure 5-48. Oscilloscope display for DL140 adjustment.

29. Set the clock in the Timing sub-menu to 20 ns and press START PAT GEN.

30. Adjust DL160 so that the pulse delay between the rising edge of channel 1 and the second rising edge of channel 2 is 31 ns (±0.5 ns). See Figure 5-49. Reinstall the cover on DL160.

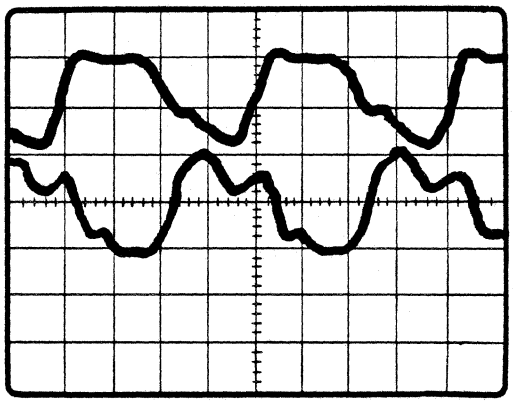


Figure 5-49. Oscilloscope display for DL160 adjustment.

31. Repeat the procedure for each 91S32 in your system.

32. Disconnect the oscilloscope. Turn off the DAS mainframe, remove the 91S32 from the Main Extender Board, then remove the Main Extender Board. Finally, reinstall the 91S32 in its slot.

This completes the 91S32 delay timing adjustment procedure.

91S32 Board Skew Adjustment Without a 91S16

The same equipment used to adjust the 91S32 clock delay is used in this procedure. This procedure assumes the clock delay adjustment has been performed.

1. Install jumpers on J206 and J208 of the first and last 91S32 in the system. (This is the standard jumper configuration when no 91S16 is present.)

2. Remove covers from DL140 and DL160 on a 91S32.

3. Remove the Main Extender board and install two 91S32s in slots powered by a 22 A +5 V power supply.

4. Connect P6464 probes to the 91S32 POD A connectors.

5. Connect the channel 1 oscilloscope probe to TP580 of the 91S32 in the slot closest to slot 7. Connect the channel 2 probe to TP580 of the 91S32 to be adjusted.

(5) (Tight specification): Connect the channel 1 oscilloscope probe to the P6464 POD A clock output of the 91S32 in the maximum slot. Connect the channel 2 probe to the P6464 POD A clock output of the 91S32 to be adjusted. Ground the oscilloscope probes to the V-ref of the P6464 clock podlets.

6. Select the Timing sub-menu and set the clock to 200 ns.

7. Enter the Configuration sub-menu and select END SEQUENCE 2047, FREE RUN.

8. Press START PAT GEN, then adjust the oscilloscope for a display like Figure 5-45.

9. Adjust DL140 so that the pulse delay between channel 1 and channel 2 is 0 ns (±0.5 ns). Reinstall the cover on DL140.

10. Select the Timing sub-menu, set the clock to 20 ns, and press START PAT GEN.

11. Adjust DL160 so that the pulse delay between channel 1 and channel 2 is 0 ns (±0.5 ns). Reinstall the cover on DL160.

12. If another 91S32 is present, repeat the procedure for that module. (Work from first to third, first to fourth, etc.)

13. Turn off DAS power and remove the 91S32 modules.

91S32 Board Skew Adjustment With a 91S16

Equipment required for this procedure is the same as for previous procedures. This procedure assumes the clock delay adjustment has been performed on the 91S16 and 91S32 modules.

1. Install square-pin shorting jumpers on J102, J302, J304, J308, J310, J312, J314, J316, J318, J320, J322, J324, J202, J204, J206, and J208 of the 91S32.

NOTE
If multiple 91S32s are installed, position the 91S32 with the jumpers furthest from the 91S16.

2. Connect the channel 1 oscilloscope probe to test point TP720 on the 91S16. Connect the channel 2 probe to TP580 on the 91S32 to be adjusted.

(2) (Tight specification): Connect the oscilloscope channel 1 probe to the P6464 POD A probe clock output of the 91S16. Attach the channel 2 probe to the P6464 POD A probe clock output of the 91S32 to be adjusted. Connect oscilloscope probe grounds to the P6464 grounds and podlet V-refs.

3. Set the 91S16 Pattern Generator menu to the Program sub-menu and enter the following program.

SEQ	Label	A	B	S	I	M	SEQ FLOW, CONTROL	REG, OUT
0	A	00	00	0	0	0		
1		00	00	0	0	0	JUMP	

4. Select the Timing sub-menu and set the clock to 200 ns.

5. Press START PAT GEN and adjust the oscilloscope for a display like Figure 5-45.

6. Adjust DL140 on the 91S32 so that the pulse delay between channel 1 and channel 2 is 0 ns (+0.5 ns).

This completes all 91S16 and 91S32 adjustment procedures. Disconnect the test equipment and restore the DAS to the standard operating configuration.

P6464 TTL/ECL PATTERN GENERATOR PROBE CHECK

You will need the equipment specified in Table 5-1 (or equivalent) to complete this check procedure.

Table 5-1
EQUIPMENT NEEDED FOR THE P6464 PERFORMANCE CHECK

Equipment	Specifications	Equivalent Tektronix Instrument
DAS 9100 Mainframe with firmware version 1.11 and upgraded +5 V module for 91S16/S32 slots	No substitute allowed	Tektronix part number 020-0707-01
91S16 or 91S32 Pattern Generator Module	No substitute allowed	
Pulse or square wave generator	100 MHz pulse rate, min. Output swing between +5 V and ground.	PG 502
Power Supply	Min output ± 5 V @ 1 A	PS 503A
Programmable Universal Counter/Timer	Capable of measuring 125 MHz	DC 5010 or DC 503A
P6460 Data Acquistion Probe with flying lead set	No substitute allowed	
P6462 Clock Probe with flying lead set	No substitute allowed	
Oscilloscope	Min. 350 MHz bandwidth	485
82 Ω resistor	0.25W,5%	Tektronix part number 315-0820-00
51 Ω resistor	0.25W,5%	Tektronix part number 315-0510-00
BNC T		Tektronix part number 103-0030-00
Probe Tip to BNC Adapter		Tektronix part number 013-0084-01

For instructions on use of the various menus, refer to the Operating information section of this manual.

(1) Mainframe Setup using the 91S16

Use the following procedure to setup the DAS mainframe for this performance check procedure using the 91S16.

WARNING

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Install the 91S16 module in any slot powered with the upgraded +5 V module.
3. Connect the P6464 TTL/ECL Pattern Generator Probe to pod connector A on the rear edge of the 91S16 module.
4. Connect the P6460 Data Acquisition Probe to pod connector C on the rear edge of the 91S16 module.
5. Turn on the DAS mainframe.
6. Enter the Setup:timing menu and set the clock to External ⌐.
7. Enter the Setup:probe menu and set the P6460 Input Threshold to ECL.
8. Enter the Configuration menu and set the P6464 for ECL.

(2) Maximum Frequency Verification using the 91S16

The following procedure verifies the operation of the probe at 50 MHz, using the 91S16 card.

1. Connect a scope to the output of the pulse generator using a BNC-T to BNC-probe adapter.
2. Connect the P6460 external clock (black lead) to the unused side of the BNC T.
3. Set the pulse generator as follows:

   PERIOD to 10 ns
   PULSE DURATION to 5 ns
   BACK TERM out
   LEVEL OUTPUT (VOLTS) to −3
   HIGH LEVEL OUTPUT (VOLTS) to 2
   NORM/COMP switches set to NORM

4. Using the multimeter, set the power supply for outputs of +2 V and −3 V. Ground the common terminal.
5. Set the programmable counter/timer as follows:

   CHANNEL A TERM switch to 50 Ω
   CHANNEL A COUPL switch to DC
   CHANNEL A SLOPE switch to +
   AVGS to 2

6. Connect CHANNEL A of the counter/timer to the output of the pulse generator.

7. Push the AUTOTRIGGER switch of the pulse generator. Adjust the frequency of the pulse generator to 50+ MHz, and observing the scope, adjust the pulse width to 7 ns.

8. Connect the P6464 VH (red) to +2 V, VL (black)to −3 V, and GND (green) to common on the power supply.

9. Connect the P6464 clock channel podlet to the counter/timer CHANNEL A.

10. Press the counter/timer PERIOD A and AUTO TRIG switches.

11. Press START PAT GEN on the DAS.

12. The counter/timer should read ≤ 20 ns or ≥ 50 MHz.

(3) ECL Mode Verification using the 91S16

The following procedure verifies each channel for ECL mode.

1. Program the 91S16 card for ECL mode.

2. Adjust the power supply for V+ = 2 and V− = −3.

3. Connect the 51 Ω resistor in parallel with the scope probe.

4. Connect the scope probe to the SIGNAL OUT of the channel 0 podlet. Connect REF of the podlet to the power supply common.

5. Press the START PAT GEN key on the DAS mainframe.

6. Measure the high and low voltage levels of the signal.

7. The low level should be below .35 V and the high level should be above 1 V.

8. Measure each of the remaining channels

(4) TTL Mode Verification using the 91S16

The following procedure verifies each channel for TTL mode.

1. Program the 91S16 card for TTL mode.

2. Adjust the power supply for V+ = 2.6 and V− = −2.4.

3. Connect the 82 Ω resistor in parallel with the scope probe.

4. Connect the scope probe to the SIGNAL OUT of the channel 0 podlet. Connect REF of the podlet to common.

5. Press the START PAT GEN key on the DAS mainframe.

6. Measure the high and low voltage levels of the signal.

7. The low level should be below −1.65 V and the high level should be above 1.1 V.

8. Measure each of the remaining channels.

(1) Mainframe Setup using the 91S32

Use the following procedure to setup the DAS mainframe for this performance check using the 91S32.

1. Turn off the DAS mainframe.
2. Install the 91S32 module in any slot powered with the upgraded +5 V module.
3. Connect the P6464 TTL/ECL Pattern Generator Probe to pod connector A on the rear edge of the 91S32 module.
4. Connect the P6452 to the rear edge of the Trigger/Timebase card.
5. Turn on the DAS mainframe.
6. Enter the Setup:timing menu and set the clock to External ⌐.
7. Enter the Setup:probe menu and set the P6452 Input Threshold to ECL.
8. Enter the Configuration menu and set the P6464 for ECL. Set END SEQ to 1 and FREE RUN.
9. Enter the Program:run menu set a 0-F-0-F pattern for the pod by setting SEC 0 to all 0s and 1 to all Fs.

(2) Maximum Frequency Verification using the 91S32

The following procedure verifies the operation of the probe at 50 MHz, using the 91S32 card.

1. Connect a scope to the output of the pulse generator using a BNC-T to BNC-probe adapter
2. Connect the P6452 PG CLK (brown lead) to the unused side of the BNC T.
3. Set the pulse generator as follows:

   PERIOD to 10 ns
   PULSE DURATION to 5 ns
   BACK TERM out
   LOW LEVEL OUTPUT (VOLTS) to −3
   HIGH LEVEL OUTPUT (VOLTS) to 2
   NORM/COMP switches set to NORM
   Add a 50 Ω terminator to the OUTPUT

4. Using the multimeter, set the power supply for outputs of +2 V and −3 V. Ground the common terminal.
5. Set the programmable counter/timer as follows:

   CHANNEL A TERM switch to 50 Ω
   CHANNEL A COUPL switch to DC
   CHANNEL A SLOPE switch to +
   AVGS to 2

6. Connect CHANNEL A of the counter/timer to the output of the pulse generator.

7. Push the AUTOTRIGGER switch of the pulse generator. Adjust the frequency of the pulse generator to 50+ MHz and, observing the scope, adjust the pulse width to 7 ns.
8. Connect the P6464 VH (red) to +2 V, and VL (black) to −3V, and connect the GND (green) lead to common on the power supply.
9. Connect the P6464 clock channel podlet to the counter/timer CHANNEL A.
10. Press the counter/timer PERIOD A and AUTO TRIG switches.
11. Press START PAT GEN on the DAS.
12. The counter/timer should read ≤ 20 ns or ≥ 50 Mhz.

(3) ECL Mode Verification using the 91S32

The following procedure verifies each channel for ECL mode.

1. Program the 91S32 card for ECL mode.
2. Adjust the power supply for V+ = 2 and V− = −3.
3. Connect the 51 Ω resistor in parallel with the scope probe.
4. Connect the scope probe to the SIGNAL OUT of the channel 0 podlet. Connect REF of the podlet to the power supply common.
5. Press the START PAT GEN key on the DAS mainframe.
6. Measure the high and low voltage levels of the signal.
7. The low level should be below .35 V and the high level should be above 1 V.
8. Measure each of the remaining channels.

(4) TTL Mode Verification using the 91S32

The following procedure verifies each channel for TTL mode.

1. Program the 91S32 card for TTL mode.
2. Adjust the power supply for V+ = 2.6 and V− = −2.4.
3. Connect the 82 Ω resistor in parallel with the scope probe.
4. Connect the scope probe to the SIGNAL OUT of the podlet of channel 0.
5. Press the START PAT GEN key on the DAS mainframe.
6. Measure the high and low voltage levels of the signal.
7. The low level should be below −1.65 V and the high level should be above 1.1 V.
8. Measure each of the remaining channels.

SERVICE INFORMATION

VERIFYING INSTALLATION OF THE UPGRADED + 5 V POWER SUPPLY

DAS 9100 mainframes can be configured using either an upgraded or an original-design + 5 V power supply. The original + 5 V power supplies provide up to 18 amps current, while the upgraded + 5 V power supplies provide up to 22 amps. 91S16 and 91S32 Pattern Generator modules require power from the upgraded + 5 V power supply. Therefore, it may be necessary to determine which + 5 V supplies are installed in your DAS.

A fully configured DAS contains three + 5 V power supplies; each supply provides power to two module slots. 91S16 and 91S32 Pattern Generator modules must be installed in slots supplied by the upgraded high-current +5 V power supply. Other DAS modules may not require this supply. You may want to install only enough upgraded + 5 V power supplies to satisfy your 91S16 and 91S32 modules, and then restrict module placement accordingly.

DAS 9100 instruments with the following serial numbers and greater will automatically have the upgraded power supply installed:

- Monochrome DAS 9109, serial numbers B050326 and higher
- Color DAS 9129, serial numbers B060100 and higher
- DAS 9119, serial numbers B010102 and higher

To identify the + 5 V power supply models in your mainframe, proceed as follows:

Remove Top Panel and Covers

Figure 5-50 illustrates how to remove the top panel and the module compartment cover.

1. Loosen the two large slotted screws in the upper corners of the back panel. Rotate the brackets behind these screws until they no longer block the edge of the top panel.
2. Press backward on the ridges at the front of the top panel. Simultaneously, pull on the rear edge until the front disengages.
3. Lift the panel up and off the mainframe.

NOTE

Step 4 is not necessary if you do not need to determine the position of the 91S16 and 91S32 modules.

4. Loosen the slotted-head screws that secure the module compartment cover until approximately 1/4 inch of each screw is exposed. Grasp the front edge of the cover and lift it off the mainframe.

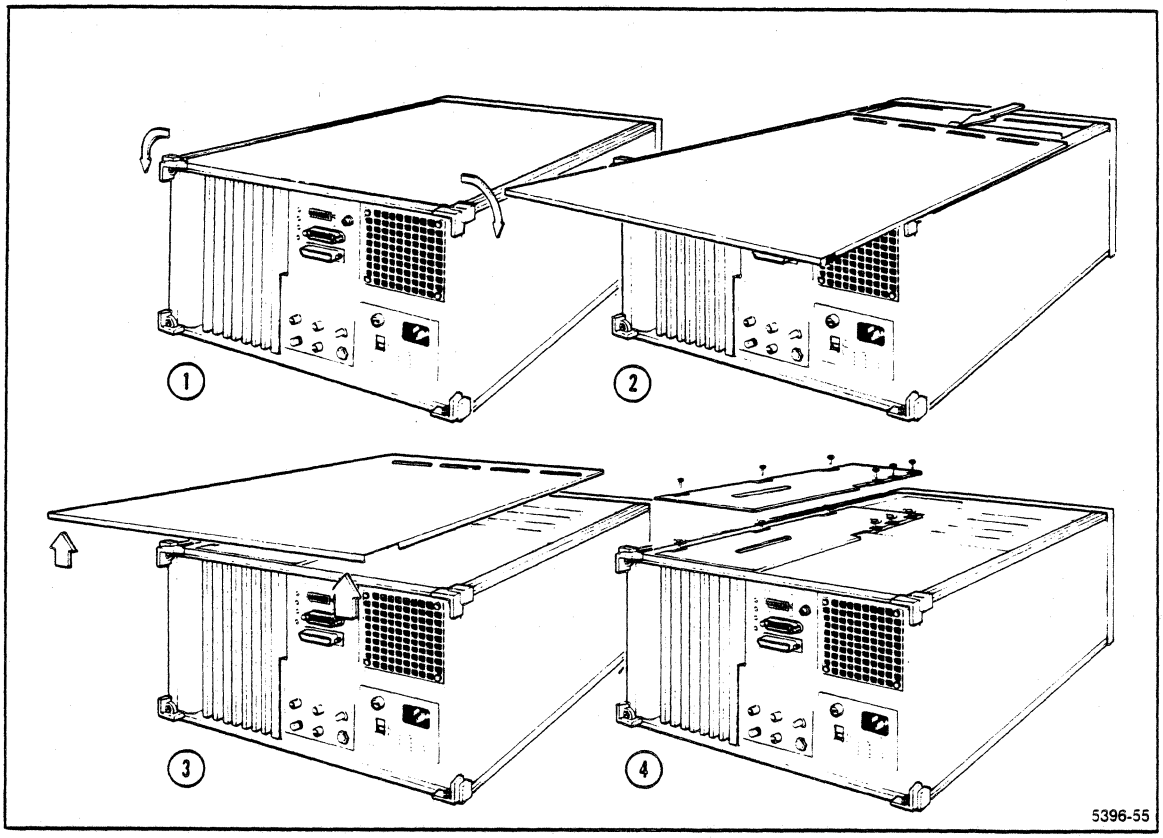


Figure 5-50. Removing the top panel and the module compartment cover

WARNING

The power supply cover should be removed only by qualified service personnel. Hazardous voltages may be present; use extreme caution. Be sure power is off and the power cord is disconnected before removing the cover.

There are three holes located in the power supply cover. Chrome pins show through these holes to indicate the position of the + 5 V power supplies already installed. Locate these pins without removing the power supply cover; if all three pins are present, the DAS contains three + 5 V power supplies; this does not necessarily mean that upgraded + 5 V power supplies are installed.

- The + 5 V power supply module in the left position (adjacent to the main power supply) provides power to bus slots 1 and 2; this power supply is provided as a part of the basic DAS mainframe.
- The + 5 V power supply module in the center position provides power to bus slots 5 and 6.
- The + 5 V power supply in the right position (closest to the instrument modules) provides power to bus slots 3 and 4.

Remove Power Supply Cover

WARNING

DANGEROUS VOLTAGES ARE PRESENT ON THE CAPACITOR BRACKET BOARD DURING OPERATION AND FOR FIVE MINUTES AFTER POWER-DOWN. Each filtering capacitor can hold a 160 V charge. Wait at least five minutes for the capacitors to discharge before accessing the power supplies or related assemblies.

1. Remove the flat-head, POZIDRIVE screws that secure the power supply cover.
2. Lift the cover up and off.

Identify Power Supply Models

Refer to Figure 5-51 and identify the + 5 V power supplies that serve the DAS bus slots where 91S16 and 91S32 modules reside. If original 18 amp + 5 V power supplies are installed, contact your Tektronix sales representitive to obtain an upgraded 22 amp + 5 V power supply.

NOTE

If you have a color DAS, and you need to obtain upgraded 22-amp +5 V power supplies, you must also obtain the accompanying EMI kit. The EMI kit contains a shield that is placed between the color CRT gun and the +5 V module compartment. The EMI kit is not necessary for monochrome DAS's.

Part-number tags are fastened to the back of the chassis on each + 5 V power supply. Part numbers 620-0296-00 are for the original-design 18 amp models. Part numbers 620-0296-01 and up are for the upgraded 22 amp models.

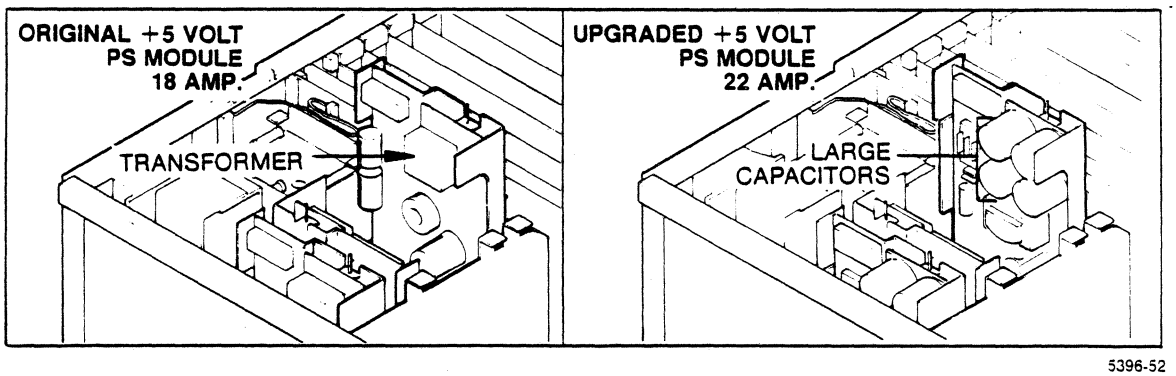


Figure 5-51. Identifying the + 5 V power supply.

Section 6
MAINTENANCE: GENERAL INFORMATION

Tektronix maintains repair and recalibration facilities at its local Field Service Centers and at the Factory Service Center. For further information or assistance, contact your local Tektronix Field Office or representative.

NOTE

Refer to the DAS 9100 Series Service Manual for general maintenance procedures and precautions. Only new or changed maintenance information is included in this addendum.

Maintenance Precautions

The general maintenance precautions for 91S16 and 91S32 Pattern Generator modules are nearly identical to those of other DAS instrument modules. Observe the following special precautionary measures while performing maintenance on the 91S16 or 91S32.

CAUTION

Do not ground signal test points; this will damage ECL outputs.

Do not connect the P2 ribbon cable while DAS power is on; this action will damage the line drivers in the 91S16 (or in the master 91S32 if a 91S16 is not used).

Do not connect P6464 probes while the pattern generator is running; this will damage probe circuits.

Podlets are extremely static-sensitive. Handle them only in a static-free environment, and make sure you are grounded while handling them.

Do not operate a 91S16 or 91S32 on an extender without an external fan blowing air on the component side of the board. Heat will build up and damage the boards.

Do not subject variable delay lines to cleaning solutions. Doing so will degrade delay-line performance.

Installing and Removing Instrument Modules

CAUTION

The 91S16 and 91S32 modules are fragile. Be very careful when removing or installing these modules. Be especially careful not to exert excessive pressure, or to flex the modules when they are extended for maintenance. Pressure or flexing will cause broken board runs and separated component connections.

The procedure for installing or removing 91S16 and 91S32 modules in a DAS mainframe is nearly identical to that of any other DAS instrument module. For specific information on module installation or removal, see the Operating Instructions section of this addendum.

INSTALLATION SLOT RESTRICTIONS

Power to the DAS mainframe slots in which a 91S16 or 91S32 resides must be provided by a DAS 22 A, +5 V Power Supply. Earlier DAS power supplies with less current capability cannot supply these modules.

Preventive and Corrective Maintenance

Preventive maintenance procedures for 91S16 and 91S32 modules and probes are the same as preventive maintenance procedures for other modules and probes in the DAS system. Refer to the DAS 9100 Series Service Manual for this information.

CAUTION

Do not brush the module while rinsing with isopropyl alcohol. Brushing causes the solder residue to adhere to the board where it remains after the alcohol evaporates. This can degrade operation by causing leakage between the board runs. While rinsing the module with isopropyl alcohol, be especially careful to avoid getting the solution on or near the variable delay lines.

When cleaning a 91S16 or 91S32 module after soldering, perform the following steps.

1. Flush the module repeatedly with isopropyl alcohol (do not brush). **DO NOT ALLOW THE SOLUTION TO GET ON, OR NEAR, THE VARIABLE DELAY LINES.**

2. Wait 60 seconds after flushing, then blow-dry with low-velocity air.

REPAIRING 91S16 AND 91S32 MODULES

Repair procedures for 91S16 and 91S32 modules are generally the same as those for the other DAS modules. Refer to your DAS 9100 Series Service Manual for these procedures. However, observe the precautionary measures stated in the Maintenance Precautions provided earlier in this section.

EXTENDING THE MODULES FOR MAINTENANCE

When extending a 91S16 or 91S32, use extender ribbon cable p/n 175-9782-00 instead of the standard ribbon cable.

CAUTION

When operating a 91S16 or 91S32 on an extender, blow air onto the component side of the board with an external fan. Without the external fan, excissive heat will build up and damage the board.

Repackaging Information

All DAS 9100 Series products are shipped in specially designed transportation packaging. If you need to ship a product, use its original packaging. If the original packaging is no longer fit for use, contact your nearest Tektronix Field Office and obtain new DAS packaging.

If you need to ship any part of your 91S16/91S32 Pattern Generator system, include all components of the system: all 91S16 and 91S32 modules, and their probes, podlets, and leads.

When you ship a product to a Tektronix Service Center, be sure to attach an identifying tag to the product (inside the packaging). On this tag include:

your name,

the name of your company,

the name and serial numbers of the enclosed products,

a detailed description of all failure indications,

and a description of the service requested.

DISASSEMBLY OF THE P6464 PROBE

The following steps are used to disassemble the P6464.

1. With a small flat-blade screwdriver, unlatch the latches located on the side of the P6464.

2. Grasp the top and bottom halves of the probe and pull.

The inside is now exposed for troubleshooting. The heat sink and plate must stay in place if you need to troubleshoot the probe. If desired, the boards can be pulled from the case.

CAUTION

The hybrid and podlets are static sensitive. Full static precautions should be used when handling the probe.

3. Using a small pozidrive screwdriver, unscrew the four screws holding the heatsink to the hybrid.

4. Pull up the heatsink and the plate underneath to expose the hybrid. The hybrid can now be replaced.

Assembly of the P6464 Probe is in the reverse order.

Section 7
MAINTENANCE: TROUBLESHOOTING

Refer to Section 8, Maintenance: Diagnostic Test Descriptions. Use the description of the failed function and test, along with the schematics, to analyze the failure.

Section 8
MAINTENANCE: DIAGNOSTIC TEST DESCRIPTIONS

This section contains information on troubleshooting the 91S16 and 91S32 Pattern Generator modules using the DAS diagnostics.

91S16 PATTERN GENERATOR DIAGNOSTICS

THE DIAGNOSTICS MENU

The DAS diagnostics present information in two menus: the power-up display and the Diagnostics menu.

The DAS self-diagnostics are only accessible when the power-up display shows that one of the modules has failed the power-up diagnostics. The power-up diagnostics are a limited number of brief functional tests that are run whenever the DAS is turned on. These tests verify the basic functions of the DAS, but should not be considered comprehensive.

It is possible for a module in the DAS to fail in such a way that the power-up diagnostics do not detect the failure. To access the self-diagnostics in this situation, the operator can induce a diagnostic failure from the keyboard (except the shift key) from the time the DAS is turned on to the time the power-up diagnostics are finished.

NOTE

Do not press any key other than the START SYSTEM key. If you do, you may leave the power-up display and lose access to the Diagnostics menu. The only time the diagnostics are accessible is when the power-up display shows a failure.

The Diagnostics menu is controlled in the same way as the standard menus. All changeable fields are shown in reverse video. Fields are changed by moving the blinking screen cursor to the field to be altered. Cursor movement is controlled by the up, down, right and left cursor arrows, and the NEXT key. The value in the field is changed either by using the SELECT key, or by entering a hexadecimal value from the data entry keys.

After the various fields have been changed to run the desired test, the test can be started by pressing the START SYSTEM key. A test can be stopped at any time by pressing the STOP key.

The Diagnostics menu may be exited by pressing any menu selection key while no tests are running. This will display the selected menu on the screen. The diagnostics cannot be re-entered from the standard menu displays.

DIAGNOSTICS CONTROL SUMMARY

In summary, the diagnostics are controlled in the following way.

1. A power-up diagnostics failure is forced by pressing and holding down a keyboard key immediately after the DAS is turned on.

2. The START SYSTEM key is pressed to enter the Diagnostics menu.

3. The reverse video fields on the display are changed to the desired values using the cursor control keys and the data entry keys.

4. The START SYSTEM key is pressed to start the diagnostic test or function.

5. The function will either stop by itself, or the STOP key may be pressed to stop the function at any time.

6. The Diagnostics menu may be exited at any time by pressing a menu selection key while no tests are running. The DAS must be turned off or reset to re-enter the Diagnostics menu.

ORGANIZATION OF DIAGNOSTIC FUNCTION AND SUBTEST DESCRIPTIONS

Information on the diagnostic functions is organized as follows:

1. A listing of quick reference diagnostic function descriptions is given for the 91S16.

2. Each diagnostic function and its subtests are described in detail.

There are six diagnostic function descriptions. They are as follows:

FUNCTION 0 CLK PATH (Clock Path)
FUNCTION 1 MEM ADDR (Memory Address)
FUNCTION 2 VECTOR RAM
FUNCTION 3 REGISTER
FUNCTION 4 INSTR (Instructions)
FUNCTION 5 INTERRUPT
FUNCTION 6 DAC THRESH (Threshold)

Each of the above functions contains one to seven subtests. All of the functions above and their subsets are run on the 91S16.

QUICK REFERENCE FUNCTION DESCRIPTIONS

The following list briefly describes the diagnostic functions for the 91S16 Pattern Generator module. If functions are run individually, they should be run in the listed order under the module type. Only the functions for the module in question need be run.

The tests in each function can be selected individually only when the diagnostics are in a looping mode using the SELECT key.

CLK PATH

This function verifies that a clock is given to the last latches from the input clock selector through the main clock line. Most of the circuitry tested by this function is shown on schematics 93, 98 and 99.

MEM ADDR

This function verifies the operation of the program counter and the register for selecting a memory. This test checks the circuitry that addresses the vector and micro-code RAMs. Most of the circuitry tested is shown on schematics 95, 96 and 100.

VECTOR RAM

This function verifies the vector and micro-code memory and checks associated write and readback circuits. The VECTOR RAM function tests all RAMs that are used by the 91S16 to generate any pattern. Most of the circuitry tested by the VECTOR RAM function is shown on schematics 96, 97 and 100.

REGISTER

This function verifies the operation of the two registers. Most of the circuitry tested by the REGISTER function is shown on schematic 96, 97 and 100.

INSTR

This function verifies the instructions controlling a program flow and checks associated circuitry. Most of the circuitry tested by the INSTR function is shown on schematic 94, 95, 96 and 97.

INTERRUPT

This function verifies the operation of the stack and the CALL IRQ and RETURN instruction. Most of the circuitry tested by the INTERRUPT function is shown on schematic 94, 95, 96 and 100.

THRESH

This function tests the DAC that specifies threshold levels on the data acquisition probes. This function exercises the DAC to verify the voltage accuracy, and to make sure all voltages may be selected. The circuitry exercised by this function is on schematic 94. Since there is no readback in the DAC THRESH circuitry, a diagnostic routine is provided to aid in adjustment. This test requires the technician to monitor specified test points while the test is running.

91S16 FUNCTION 0 CLK PATH

Circuit Overview

A clock is sent to the last latches through the clock selector, PAUSE circuitry, HALT circuitry, some gates and some delay lines. The controller gives a step clock, and a clock is received at flip-flop after the last gate.

Function Description

A clock is controlled by such signals as PAUSE, HALT, etc. This function verifies that a clock is transferred to the last latch by using a step clock.

Tested circuitry includes

U206, U640C, U208, U216B, U214, U218 (Schematic 93)
U502 (Schematic 96)
DL820, U802B, DL800, U802D (Schematic 99)
DL700, U700B, DL760, U702B (Schematic 98)
U716A, U954, U960 (Schematic 93 & 100)

Readback Ports

The 91S16 reads the level of U716-2, before and after a step clock is generated. A status is read from U952 and U960. When U900-12 (read8(H)) is asserted, U952 is enabled, and the status is read from U960 on the data bus (BD0-BD7).

Test Run Sequence

1. Disables PAUSE line and HALT line.
2. Select the step clock mode.
3. Read a status from port hex04 after U952 is enabled.
4. Send a clock by writing to port hex0E.
5. Read the status.

Reading the Error Code

Both expected and actual value should be 00 or 02.

Error Indication

If this function has failed, set the LOOPING field to ON, and check for a clock signal along the path with an oscilloscope. While the test is running, the controller sets a level at each point as follows:

CKT #	pin #	level (ECL)
U206	7	L
	9	H
	10	H
U208	7	L
U214	7	L
U218	7	L
U954	7	3.7V

For setting U208-7 to a low level:

CKT #	pin #	level (ECL)
U820	10	L
U222	11	H (TTL)
U212	4	H
	5	L
U638	7	L

For setting U954-7:

CKT #	pin #	level (TTL)
U502	12	H
U900	2	L
	19	L
	5	L
	16	L
	6	L
	15	L
	9	L
	12	L

91S16 FUNCTION 1 MEM ADDR

Circuit Overview

The program counter consists of a 10 bit up-counter (composed of three individual counters) which supplies the address for all memory. When the counter exceeds the maximum count(3FF), a status bit (COUNT OVER) is set. As the DAS has an 8 bit bus line, the micro-code and vector memories are shared every 8 bits for read/write. Then the 91S16 has selection lines for setting which memory is read or written.

Function Description

The MEM ADDR function consists of three tests.

Test 0 writes a value to the program counter (U410, U412, U414) and resets it. The PC count is then read back.

Test 1 exercises the PC to count from 000 to 3FF, and reads back the result every clock. This test also runs on power-up and verifies the count from hex2AA to hex3FF.

Test 2 writes a value to a memory, and checks each address line and memory selection line.

Readback Ports

The output of the program counter is read through U934-U942 and U960. When U900-9 (read7(H)) is asserted, U936-U942 are enabled, and PC0-PC7 are read from U960 on the data bus (BD0-BD7) . When U900-12 (read8(H)) is asserted, U934 is enable, and PC8-PC9 are read from U960 on the data bus (BD0-BD1).

Test 0 General Description

This test checks the clear, load, and readback of the program counter.

Clearing the counter. A reset pulse to the counter is generated by writing data to port hex0F (U118-17).

Setting the counter to a load mode. A jump instruction is clocked into memory.

Clocking the counter. A clocking pulse is generated by writing data to port hex0D(U118-15).

Reading the output of the counter. U900-9(H) enables the output PC0-PC7 of the counter to the data bus(SRD0-SRD7) through U936-U942. U900-12(H) enables the output PC8-PC9 of the counter to the data bus (SRD0-SRD1) through U934.

Tested circuitry includes

U118, U134, U218 (Schematic 93)
U424C, U410, U412, U414 (Schematic 95)
U500, U502, U422B, U512, U514, U516 (Schematic 96)
U812 (Schematic 99)
U900, U934, U936, U938, U940, U942, U960 (Schematic 100)

Test 0 Readback Port

Comparators U934, U936, U938, U940 and U942 are enabled and Test 0 results are read back through port hex04 (U960).

Test 0 Run Sequence

Test 0 includes:

1. Writing hex2AA to the memories U512, U514 and U516.
2. Writing hex8X to the memory U520.
3. Loading hex2AA to the PC.
4. Reading back the PC.
5. Clearing the PC by writing to port hex0F.
6. Reading back the PC.
7. Writing hex155 to the memories.
8. Loading hex155 to the PC.
9. Reading back the PC.

10. Clearing the PC.

11. Reading back the PC.

Test 0 Error Code

	Address	Expect	Actual
Step 1.	hex0D	hexAA	hexAA (PC0-PC7)
	hex1D	hex02	hex02 (PC8-PC9)
Step 2.	hex0D	hex00	hex00 (PC0-PC7)
	hex1D	hex00	hex00 (PC8-PC9)
Step 3.	hex0D	hex55	hex55 (PC0-PC7)
	hex1D	hex01	hex01 (PC8-PC9)
Step 4.	hex0D	hex00	hex00 (PC0-PC7)
	hex1D	hex00	hex00 (PC8-PC9)

Error Indication

Possible Cause 0. Check that there are many pulses when the LOOPING field is ON.

Check Item	Check point
A clock for the PC	Pin 13 of U410
A resetting pulse for the PC	TP440

Possible Cause 1. If the test fails, check the following: In the following table, X, which is in the Actual, specifies the position where the actual data does not match the expected data. N is a hexadecimal value.

Address	Actual	Memory	PC	Readback
hex0D	hexNX	U512	U410	U936 & U938
	hexXN	U514	U412	U940 & U942
hex1D	hex0X	U516	U414	U934

If ACTUAL data is hexXX, check U520 which is written with the JUMP instruction.

Possible Cause 2. Check the logic level at each point.

While the test is running, the circuitry has the following condition.

Loading a data to the PC:

CKT #	pin #	level (ECL)
U218	12	L
TP400	2	L
U406	17	H
	19	L
	20	L
	21	L
U502	2	H (TTL)
	19	H (TTL)
	5	L (TTL)
	16	L (TTL)
	6	L (TTL)
	15	H (TTL)
	9	H (TTL)
	12	H (TTL)

Setting TP400 to a low level :

CKT #	pin #	level (ECL)
U314	2	L
	5	L
U424	10	L

Reading the output of PC:

CKT #	pin #	level (TTL) PC0-PC7	PC8-PC9
U502	12	L	L
U900	2	L	L
	19	L	L
	5	L	L
	16	L	L
	6	L	L
	15	L	L
	9	H	L
	12	L	H

Test 1 General Description

This test checks the clear, count-up and readback of the program counter. The test contains the steps which include clearing, setting an incremental mode and reading the counter.

Setting an incremental mode. For setting an incremental mode, pin 5 of U410-U414 are set to a high level by writing 1 to bit 2 at port hex0B (U812).

Reading the counter. (The same as Test 0)

Test 1 Readback Port

Test 1 results are read back through port hex04 (U960) .

Test 1 Run Sequence. Test 1 includes the following:

1. Clearing the PC by writing to port hex0F.
2. Setting an incremental mode by writing XXXXXX1X to port hex0B.
3. Counting up to 1023.
4. Reading back the PC at every clock.

Test 1 Error Code

Address : hex0D

Expect : hex3FF (a number of clocks)

Actual : output of the PC

Error Indication

Possible Cause 0. Check that there are many pulses when the LOOPING field is ON.

Check Item	Check Point
A clock for the PC	Pin 13 of U410
A resetting pulse for the PC	TP440

Possible Cause 1

A checked device follows. (X is missing data and N is correct data).

Address	ACTUAL	PC	Readback
hex0D	hexNNX	U410	U936 & U938
	hexNXN	U412	U940 & U942
	hexXNN	U414	U934

Possible Cause 2

Check a logic level at each point.

For an incremental mode:

CKT #	pin #	level (ECL)
TP400	2	H
U424	10	H
TP440	2	L (while the PC is receiving a clock)

For reading the PC:

CKT #	pin #	level (TTL) PC0-PC7	PC8-PC9
U502	12	L	L
U900	2	L	L
	19	L	L
	5	L	L
	16	L	L
	6	L	L
	15	L	L
	9	H	L
	12	L	H

Test 2 General Description

This test checks the connection between the program counter and memories, and between the RAM selector and memories. This test contains the steps which include counting up the PC, writing to memory and reading from memory.

Writing to Memory. The data, which is a two raised to the Nth power, is written to all memory.

Readback the Content of Memory. Vectors and two strobes are loaded to the latches (U630, U632, U634, U636) by addressing port hex07. After loading, they are read via comparators. Other content of memory are read directly through comparators.

Test 2 Readback Port

Test 2 results are read back through port hex04 (U960) .

Test 2 Run Sequence

1. Clearing the PC and setting an incremental mode.
2. Incrementing the PC until a two raised to the Nth power.
3. Writing the incremented value to each memory
4. Clearing the PC.
5. Readback the written data from each memory at the address which is two to the Nth power, and comparing the readback data with the written data.
6. If the read data matches the write data, the RAM is cleared.

Test 2 Error Code

The high 4 bits of the ADDR field specifies an address line's number. The low 4 bit of the ADDR field specifies the memory. The EXPECTED is write data and the ACTUAL is read data.

Error Indication

If the test fails, loop on FUNCTION 2 VECTOR RAM.

Possible Cause 0

Check that there are pulses when the LOOPING field is ON.

Check Item	Check Point
A clock for the PC	Pin 13 of U410
A clock for latch	TP610

Possible cause 1

As the bus line is an 8-bit line, micro-code and vector RAM are shared. The low 4 bits of the ADDR specifies RAM. The high 4 bits specifies an address line's number. When a FAIL message appears, the ADDR specifies a bad address line, a bad RAM selections line or bad RAM.

ADDR	Memory	Buffer
X1	U504,U506	U502-3
X2	U508,U510	U502-19
X3	U512,U514	U502-5
X4	U516,U520	U502-16,6
X5	U518,U522	U502-15
X6	U524	U502-9

ADDR	Address line	PC	Buffer
0X	PC0 or SPC0	U410-3	U530-15
1X	PC1 or SPC1	U410-2	U530-2
2X	PC2 or SPC2	U410-15	U530-14
3X	PC3 or SPC3	U410-14	U530-3
4X	PC4 or SPC4	U412-3	U530-13
5X	PC5 or SPC5	U412-2	U530-4
6X	PC6 or SPC6	U412-15	U532-4
7X	PC7 or SPC7	U412-14	U532-13
8X	PC8 or SPC8	U414-3	U532-3
9X	PC9 or SPC9	U414-2	U532-14

Expect(ACTUAL) (Address for write)	Output of PC
00000001	0000000001
00000010	0000000010
00000100	0000000100
00001000	0000001000
00010000	0000010000
00100000	0000100000
01000000	0001000000
10000000	0010000000
10000001	0100000000
10000010	1000000000

DATA line	Buffer (TTL -> ECL)
TD0	U500-9
TD1	U500-8
TD2	U500-7
TD3	U500-6
TD4	U500-5
TD5	U500-4
TD6	U500-3
TD7	U500-2

91S16 FUNCTION 2 VECTOR RAM

Circuit Overview

The vector and micro-code memory of the 91S16 consists of eleven 4 X 1024 bit RAMs for a total of 1024 words by 44 bits.

Function Description

The data to RAM is read/written to/from the MPU bus with one byte at a time. To write to the memory, two memories (one byte) are assigned by writing the appropriate data to port hex05 and a write pulse is generated by writing to port hex06.

The VECTOR RAM function consists of six separate tests. All tests are basically identical, and will be described in detail once. Memory is selected by writing to port hex05 (U502). Once the memory is selected, data is written to port hex06 to be loaded to the selected memory. Test 0, test 1, and test 4 require a clock to load the memory output to a latch. The data is read back from the latches by the comparators.

To read results, comparators U902-U958 must be selected by writing to port hex04 (U900). A content of memory is read from port hex04 (U960).

Test 0 General Description

This test checks the memories U504, U506. These memories are used for vector VB0-VB7.

This test contains the steps which include clocking the PC, writing and reading a memory, selecting an output multiplexer, loading first latches, and reading the memory.

Tested circuitry includes:

U118, U134, U218 (Schematic 92 & 93)
U410, U412, U414, U422, U424 (Schematic 94)
U500, U502, U504, U506, U530, U532 (Schematic 96)
U616, U618, U620, U622, U634, U636 (Schematic 97)
U900, U908, U910, U912, U914, U960 (Schematic 100)

Test 0 Readback Port

Comparators U908, U910, U912 and U914 are enabled. Test 0 results are read back through port hex04 (U960).

Test 0 Run sequence

1. Selecting the memories U504 and U506 by writing hex7E to port hex05 (U502) .
2. Set the PC to an incremental mode by writing 1 to bit 2 of port hex0B (U812) and clearing the PC by addressing port hex0F (U118) .
3. Writing hexAA to the memories with a write pulse which is generated from port hex06 (U118).
4. Giving a clock to the first latches (U632-U636) by reading the port hex07. The output of the memories are loaded to the first latches.

5. Selecting the comparators (U908, U910, U912 and U914) by writing hex01 to port hex04 (U900) and reading the output of first latches from port hex04 (U960).

6. Comparing the data and writing hex55 to the memories via port hex06.

7. Reading the data by the same method

8. Giving a clock to the PC for incrementing up the address to memory.

9. Repeating the sequences from 2 to 6 until the PC is 1023.

Test 0 Error Code

The ADDR specifies a value of the program counter. The EXPECT specifies a written data and the ACTUAL is a read data.

Error Indication

Possible Error 0

Check Item	Check Point
write pulse	U504-16, U506-16
load pulse	TP610

Levels

CKT #	pin #	Level (TTL)
U502	2	L
	19	H
	5	H
	16	H
	6	H
	15	H
	9	H
	12	L
U900	2	H
	19	L
	5	L
	16	L
	6	L
	15	L
	9	L
	12	L

CKT #	pin #	Level (ECL)
U616	7,9	L
U618	7,9	L
U620	7,9	L
U622	7,9	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to the following table:

Bit	Memory	Mux	Latch	Comparator
0	U504-22	U616-2	U634-14	U908-8
1	U504-3	U616-15	U634-2	U908-2
2	U504-23	U618-2	U634-15	U910-8
3	U504-2	U618-15	U636-4	U910-2
4	U506-22	U620-2	U636-13	U912-8
5	U506-3	U620-15	U636-3	U912-2
6	U506-23	U622-2	U636-14	U914-8
7	U506-2	U622-15	U636-2	U914-2

Test 1 General Description

Test 1 checks the memories U508, U510. These memories is used for VECTOR VB8 - VB15. The steps are the same as Test 0.

New tested circuitry includes:

U508, U510 (Schematic 96)
U612, U614, U224C, U316D, U632, U634 (Schematic 97)
U916, U918, U920, U922 (Schematic 100)

Test 1 Readback Port

Comparators U916, U918, U920 and U922 are enabled. Test 1 results are readback through port hex04 (U960) .

Test 1 Run Sequence

The following steps differ from test 0. All other steps in this test are the same as test 0.

1. Selecting the memories U508, U510 by writing the data hex7D to port hex05 (U502) .

5. Selecting the comparators (U916, U918, U920 and U922) by writing hex02 to port hex04 (U900) and reading the output of the first latches from port hex04 (U960).

Test 1 Error Code

(The same as Test 0).

Error Indication

Possible Error 0

Check Item	Check Point
write pulse	U508-16, U510-16
load pulse	TP610

Levels

CKT #	pin #	Level (TTL)
U502	2	H
	19	L
	5	H
	16	H
	6	H
	15	H
	9	H
	12	L
U900	2	L
	19	H
	5	L
	16	L
	6	L
	15	L
	9	L
	12	L

CKT #	pin #	Level (ECL)
U616	7,9	L
U618	7,9	L
U620	7,9	L
U622	7,9	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to the following table:

Bit	Memory	Mux	Latch	Comparator
0	U508-22	U612-14	U632-4	U916-8
1	U508-3	U612-1	U632-13	U916-2
2	U508-23	U612-15	U632-3	U918-8
3	U508-2	U612-2	U632-14	U918-2
4	U510-22	U614-14	U632-2	U920-8
5	U510-3	U614-1	U632-15	U920-2
6	U510-23	U614-15	U634-4	U922-8
7	U510-2	U614-2	U634-13	U922-2

Test 2 General Description

This Test checks the memories U512 and U514. These memories are used for the destination (JA0-JA7) of the JUMP instruction.

The steps are the same as Test 0.

New tested circuitry includes:

U512, U514 (Schematic 96)
U924, U926, U928, U930 (Schematic 100)

Test 2 Readback Port

Comparators U924, U926, U928 and U930 are enabled. Test 2 results are readback through port hex04 (U960).

Test 2 Run Sequence

The following steps differ from test 0. All other steps in this test are the same as test 0.

1. Selecting the memories U512 and U514 by writing hex7B to port hex05 (U502) .

4. This sequence is not needed.

5. Selecting the comparators (U924, U926, U928 and U930) by writing the data hex04 to port hex04 (U900) and reading the content of the memories from port hex04 (U960) .

Test 2 Error Code

(The same as Test 0).

Error Indication

Possible Error 0

Check Item	Check Point
write pulse	U512-16, U514-16
load pulse	TP610

Levels

CKT #	pin #	Level (TTL)
U502	2	H
	19	H
	5	L
	16	H
	6	H
	15	H
	9	H
	12	L
U900	2	L
	19	L
	5	H
	16	L
	6	L
	15	L
	9	L
	12	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to next table.

Bit	Memory	Comparator
0	U512-22	U924-8
1	U512-3	U924-2
2	U512-23	U926-8
3	U512-2	U926-2
4	U514-22	U928-8
5	U514-3	U928-2
6	U514-23	U930-8
7	U514-2	U930-2

Test 3 General Description

This test checks the memories U516 and U520. These memories are used for the destination (JA8 and JA9) of the JUMP instruction, the OUT instruction, and the instructions for controlling the program flow. The steps are the same as Test 0.

New tested circuitry includes

U516, U520 (Schematic 96)
U958, U902, U906 (Schematic 100)

Test 3 Readback Port

Comparators U958, U902 and U906 are enabled (same as Test 0).

Test 3 Run Sequence

The following steps differ from test 0. All other steps in this test are the same as test 0.

1. Selecting the memories U516 and U520 by writing hex67 to port hex05 (U502) .

4. This sequence is not needed.

5. Selecting the comparators (U902, U946 and U958) by writing the data hex08 to port hex04 (U900) and reading the content of the memories from port hex04 (U960).

Test 3 Error Code

(The same as Test 0).

Error Indication

Possible Error 0

Check Item	Check Point
write pulse	U516-16, U520-16

Levels

CKT #	pin #	Level (TTL)
U502	2	H
	19	H
	5	L
	16	L
	6	H
	15	H
	9	H
	12	L
U900	2	L
	19	L
	5	L
	16	H
	6	L
	15	L
	9	L
	12	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to next table.

Bit	Memory	Comparator
0	U516-22	U958-2
1	U516-3	U958-13
2	U516-23	U906-2
3	U516-2	U906-13
4	U520-22	U904-2
5	U520-3	U904-13
6	U520-23	U904-1
7	U520-2	U904-14

Test 4 General Description

This test checks the memories U518 and U522. These memories are used for the INHIBIT and STROBE instructions, and the instruction for the register control. The steps are the same as Test 0.

New tested circuitry includes

U518, U522 (Schematic 96)
U630, U634, U636 (Schematic 97)
U946, U948, U904 (Schematic 100)

Test 4 Readback Port

Comparators U946, U948 and U904 are enabled (same as Test 0).

Test 4 Run Sequence

The following steps differ from test 0. All other steps in this test are the same as test 0.

1. Selecting the memories U518 and U522 by writing hex5F to port hex05 (U502) .

5. Selecting the comparators (U904, U946 and U948) by writing the data hex10 to port hex04 (U900) and reading the content of the memories from port hex04 (U960).

Test 4 Error Code

(The same as Test 0).

Error Indication

Possible Error 0

Check Item	Check Point
write pulse	U518-16, U522-16
load pulse to latch	TP610

Levels

CKT #	pin #	Level (TTL)
U502	2	H
	19	H
	5	H
	16	H
	6	L
	15	H
	9	H
	12	L
U900	2	L
	19	L
	5	L
	16	L
	6	H
	15	L
	9	L
	12	L

CKT #	pin #	Level (ECL)
U616	7,9	L
U618	7,9	L
U620	7,9	L
U622	7,9	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to the following table.

Bit	Memory	Gate	Latch	Comparator
0	U516-22	U224-10	U630-15	U946-8
1	U516-3	U224-3	U630-2	U946-2
2	U516-23	-	U636-15	U948-8
3	U516-2	-	U634-3	U948-2
4	U522-22	-	-	U904-2
5	U522-3	-	-	U904-13
6	U522-23	-	-	U904-1
7	U522-2	-	-	U904-14

Test 5 General Description

This test checks memory U524. This memory is used for the NEXT PAGE, HALT, TRIGGER OUT, and INTERRUPT MASK instruction. The steps are the same as Test 0.

New tested circuitry mainly includes

U524 (Schematic 96)
U906, U958 (Schematic 100)

Test 5 Readback Port

Comparators U906 and U958 are enabled (the same as Test 0).

Test 5 Run Sequence

The following steps differ from test 0. All other steps in this test are the same as test 0.

1. Selecting the memory U524 by writing hex3F to port hex05 (U502) .

4. This sequence is not needed.

5. Selecting the comparators (U906 and U958) by writing the data hex20 to port hex04 (U900) and reading the content of the memories from port hex04 (U960).

Test 5 Error Code

(The same as Test 0).

Error Indication

Possible Error 0

Check Item	Check Point
write pulse	U524-16

Levels

CKT #	pin #	Level (TTL)
U502	2	H
	19	H
	5	H
	16	H
	6	H
	15	H
	9	L
	12	L
U900	2	L
	19	L
	5	L
	16	L
	6	L
	15	H
	9	L
	12	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to the following table.

Bit	Memory	Comparator
0	U524-22	U958-1
1	U524-3	U958-14
2	U524-23	U906-1
3	U524-2	U906-14
4	-	-
5	-	-
6	-	-
7	-	-

91S16 FUNCTION 3 REGISTER

Circuit Overview

The 91S16 has two 8 bit registers (or one 16bit register). These registers can load, hold, count up or down by micro-code instruction. The program flow is controlled by these registers. And the output of these register is transferred to probes via the OUTPUT selector and two latches.

Functional Description

Test 0 checks the load, count up, and count down functions of register A (U600 and U602); and readback the value of the registers.

Test 1 checks the load, count up, and count down functions of register B (U604 and U606); and readback the value of the registers.

Test 2 checks the load and increment functions.

91S16 FUNCTION 3 REGISTER

Circuit Overview

The 91S16 has two 8-bit registers (or one 16-bit register). These registers can load, hold, count up or down by micro-code instruction. The program flow is controlled by the result of these registers, and the output is transferred to probes via the output selector and two latches.

Functional Description

The REGISTER function consists of four tests.

Test 0 checks register A's function (U600 and U602) which are the load, count up, and count down; and reads back the value of the registers.

Test 1 checks register B's function (U604 and U606) which are the load, count up, and count down; and reads back the value of the registers.

Test 2 checks the load and increment functions as a 16 bit register. This test does not run at power-up.

Test 3 checks the load and increment functions as a 16 bit register. This test does not run at power-up.

Writing a value to a register

A desired value are written to the memories (U504, U506, U508 and U510). And the control bits for register are written to the memory U522. Registers RA and RB are controlled by giving a clock, according to the output of the memory (U522).

Reading a value from a register

A output of a register is passed to the first latches (U632-U636)by selecting the multiplexer(U612-U622), and is clocked to the first latches by reading from port hex07 (U112). After they are clocked in, the output of the first latch is read via comparators.

Test 0 General Description

This test checks register A's function which are the LOAD, HOLD, INCRE, and DECRE modes. The results are read via selector, latches, and comparators.

Setting the mode

The memory U522 is selected by writing hex5F to port hex05 (U502) and the following data is loaded in memory U522 by writing to port hex06 (U118).

bit 7	bit 6	
0	0	load vector to register A
0	1	Increment
1	0	Decrement
1	1	Hold

Setting the OUTPUT SELECTOR

The OUTPUT SELECTOR is selected by OUT RA. The data hex20 is written to port hex0C (U814) via the disabled RAM (U516).

Loading to the first latches

The output of register A is loaded into the first registers by reading from port hex07.

Reading the data loaded to the first latches

The same as the steps which read vector VB0-VB7.

Tested circuitry includes

U422, U500, U502, U504, U506, U522 (Schematic 96)
U600, U602, U616, U618, U620, U622, U634, U636 (Schematic 97)
U900, U908, U910, U912, U914, U960 (Schematic 100)

Test 0 readback port

Comparators U908, U910, U912 and U914 are enabled. The output of the register A can be read via the OUTPUT SELECTOR and the first latches.

Test 0 Run Sequence

1. Sets the output selector to OUT RA.

2. Selects the memories U504 and U506 by writing hex7E to port hex05 (U502).

3. Loads the vector hex55 to the memories by writing to port hex06.

4. The initial data (hex55) is loaded to register A.

5. Selects the memory U522 for loading MC12 and MC13 by writing hex5F to port hex05.

6. To set register A to an incremental mode, selects the memory U522 and writes the data hex7F to port hex06 (write pulse).

7. Clocks register A until the output of register A is hexFF.

8. The value of register A is read back after being loaded to the first latches after every clock.

9. Selects the memories U504 and U506 by writing hex7E to port hex05 (U502).

10. Loads the vector hexAA to the memories by writing to port hex06.

11. The initial data (hexAA) is loaded to register A.

12. Selects the memory U522 for loading MC12 and MC13.

13. To set register A to a decremental mode, writes the data hexBF to port hex06 (write pulse).

14. Clocks register A until the output of register A is hex00.

15. The value of register A is read back after being loaded to the first latches after every clock.

Test 0 Error Code

The ADDR specifies the incremental or decremental mode. EXPECT is a number of clocks which are given to register A and ACTUAL is the output of the register A.

Error Indication

Possible Cause

Check that there are many pulses at test point:

Check Item	**Check Point**
Clock for register	TP600
Clock for latch	TP610

For an incremental mode:

ADDR = hex70

CKT #	**pin #**	**Level (ECL)**
U600	7	H
	9	L
U602	7	H
	9	L

For a decremental mode:

ADDR = hexB0

CKT #	**pin #**	**Level (ECL)**
U600	7	L
	9	H
U602	7	L
	9	H

Output Selector selects the output of register A.

CKT #	**pin #**	**Level (ECL)**
U616	7	L
	9	H
U618	7	L
	9	H
U620	7	L
	9	H
U622	7	L
	9	H

Readback port :

CKT #	pin #	Level (TTL)
U502	12	L
U900	2	H
	19	L
	5	L
	16	L
	6	L
	15	L
	9	L
	12	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to following table:

Bit	register A	Mux	Latch	Comparator
0	U600-14	U616-2	U634-14	U908-8
1	U600-15	U616-15	U634-2	U908-2
2	U600-2	U618-2	U634-15	U910-8
3	U600-3	U618-15	U636-4	U910-2
4	U602-14	U620-2	U636-13	U912-8
5	U602-15	U620-15	U636-3	U912-2
6	U602-2	U622-2	U636-14	U914-8
7	U602-3	U622-15	U636-2	U914-2

Test 1 General Description

This test checks register B's function which are the LOAD, HOLD, INCRE, and DECRE modes. The results are read via OUTPUT selector, latches, and comparators.

Setting the mode

The memory U522 is selected by writing hex5F to port hex05 (U502) and the following data is loaded to the memory U522 by writing to port hex06 (U118).

bit 5	bit 4
0	0 load vector to register B
0	1 Increment
1	0 Decrement
1	1 Hold

Setting the OUTPUT SELECTOR

The OUTPUT SELECTOR is selected by OUT RB. The hex10 data is written to port hex0C (U814) with the disabled RAM (U516).

Loading to the first latches

The output of register B is loaded to the first registers by reading from port hex07.

Reading the data loaded to the first latches

The same as Test 0 sequence.

New tested circuitry includes:

U608, U610, U604, U606 (Schematic 97)

Test 1 readback port

The output of the register A is read via the OUTPUT SELECTOR and the first latches.

Test 1 Run Sequence

1. Sets the output selector to OUT RB.
2. Selects the memories U508 and U510 by writing hex7D to port hex05 (U502).
3. Loads the vector hex55 to the memories by writing to port hex06.
4. The initial data (hex55) is loaded to register A.
5. Selects the memory U522 for loading MC10 and MC11 by writing hex5F to port hex05.
6. To setting register B to an incremental mode, selects the memory U522 and write the data hexDF to port hex06 (write pulse).
7. Clocks to register B until the output of register B is hexFF.
8. The value of register B is read back after being loaded to the first latches after every clock.
9. Selects the memories U508 and U510 by writing hex7D to port hex05 (U502).
10. Loads the vector hexAA to the memories by writing to port hex06.
11. The initial data (hexAA) is loaded to register B.
12. Selects the memory U522 for loading MC10 and MC11.
13. To set register B to a decremental mode, write the data hexEF to port hex06 (write pulse).
14. Clocks to register B until the output of register B is hex00.
15. The value of register B is read back after being loaded to the first latches after every clock.

Test 1 Error Code

The ADDR specifies the incremental or decremental mode. EXPECT is a number of clocks which are given to register B and ACTUAL is the output of the register B.

Error Indication

Possible Cause

Check that there are many pulses at the test points:

Check Item	Check Point
Clock for register	TP600
Clock for latch	TP610

For an incremental mode:

ADDR = hexD0

CKT #	pin #	Level (ECL)
U604	7	H
	9	L
U606	7	H
	9	L

For a decremental mode:

ADDR = hexE0

CKT #	pin #	Level (ECL)
U604	7	L
	9	H
U606	7	L
	9	H

For loading data to register B:

CKT #	pin #	Level (ECL)
U608	9	H
U610	9	H

Output Selector selects the output from the register B.

CKT #	pin #	Level (ECL)
U616	7	H
	9	L
U618	7	H
	9	L
U620	7	H
	9	L
U622	7	H
	9	L

Readback port:

CKT #	pin #	Level (TTL)
U502	12	L
U900	2	H
	19	L
	5	L
	16	L
	6	L
	15	L
	9	L
	12	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to next table.

Bit	register B	Mux	Latch	Comparator
0	U604-14	U616-2	U634-14	U908-8
1	U604-15	U616-15	U634-2	U908-2
2	U604-2	U618-2	U634-15	U910-8
3	U604-3	U618-15	U636-4	U910-2
4	U606-14	U620-2	U636-13	U912-8
5	U606-15	U620-15	U636-3	U912-2
6	U606-2	U622-2	U636-14	U914-8
7	U606-3	U622-15	U636-2	U914-2

Test 2 General Description

This test checks a 16 bit register's function which are the LOAD and INCRE mode. The results are read via OUTPUT selector, latches and comparators.

Setting the mode

The 16 bit register mode is selected by setting bit 6 of U808 to 1. The memory U522 is selected by writing hex5F to port hex05 (U502) and the following data is loaded to the memory U522 by writing to port hex06 (U118).

bit 5 & 7	bit 4 & 6	
0	0	load vector to register
0	1	Increment

Setting the OUTPUT SELECTOR

The OUTPUT SELECTOR is set to select OUT RA. Hex20 is written to port hex0C (U814) with the disabled RAM (U516).

Loading to the first latches

The output of the registers are loaded to the first latches by reading (clocking) from port hex07.

Reading the data loaded to the first latches

The lower 8 bits are read by the same steps as vector VB0-VB7. The higher 8 bits are read by the same steps as vector VB8-VB15.

New tested circuitry includes:

U508, U510 (Schematic 96)
U638, U612, U614, U632 (Schematic 97)
U916, U918, U920, U922 (Schematic 100)

Test 2 readback port

The output of the register is read via the OUTPUT SELECTOR and the first latches.

Test 2 Run Sequence

1. Sets the output selector to OUT RA.
2. Selects the memories U504, U506, U508 and U510 by writing hex7C to port hex05 (U502).
3. Loads the vector hex55 to the memories by writing to port hex06.
4. The initial data (hex5555) is loaded to register.
5. Selects the memory U522 for loading MC10 - MC13 by writing hex5F to port hex05.
6. To setting the register to an incremental mode, selects the memory U522 and write the data hex5F to port hex06 (write pulse).
7. Clocks to register until the output of Register is hex6000.
8. The value of the register is read back after being loaded to the first latches after every clock.

Test 2 Error Code

The ADDR specifies the incremental or decremental mode. EXPECT is a number of clocks which are given to Register and ACTUAL is the output of the Register.

Error Indication

Possible Cause 0

Check that there are pulses at the test point

Check Item	Check Point
Clock for register	TP600
Clock for latch	TP610

For an incremental mode:

ADDR = hex50

CKT #	pin #	Level (ECL)
U600	7	H
	9	L
U602	7	H
	9	L
U604	7	H
	9	L
U606	7	H
	9	L

Output Selector selects the output from register A.

CKT #	pin #	Level (ECL)
U616	7	L
	9	H
U618	7	L
	9	H
U620	7	L
	9	H
U622	7	L
	9	H

For a 16 bit register:

CKT #	pin #	Level (ECL)
U638	5	H
U612	9	L
U614	9	L

Readback port:

		Low 8 bit	High 8 bit
CKT #	**pin #**	**Level (TTL)**	**Level (TTL)**
U502	12	L	L
U900	2	H	L
	19	L	H
	5	L	L
	16	L	L
	6	L	L
	15	L	L
	9	L	L
	12	L	L

Possible Cause 1

When an EXPECTED value does not match an ACTUAL value, check ICs according to the following table.

Bit	register A	Mux	Latch	Comparator
0	U600-14	U616-2	U634-14	U908-8
1	U600-15	U616-15	U634-2	U908-2
2	U600-2	U618-2	U634-15	U910-8
3	U600-3	U618-15	U636-4	U910-2
4	U602-14	U620-2	U636-13	U912-8
5	U602-15	U620-15	U636-3	U912-2
6	U602-2	U622-2	U636-14	U914-8
7	U602-3	U622-15	U636-2	U914-2
8	U604-14	U612-14	U632-4	U916-8
9	U604-15	U612-1	U632-13	U916-2
10	U604-2	U612-15	U632-3	U918-8
11	U604-3	U612-2	U632-14	U918-2
12	U606-14	U614-14	U632-2	U920-8
13	U606-15	U614-1	U632-15	U920-2
14	U606-2	U614-15	U634-4	U922-8
15	U606-3	U614-2	U634-13	U922-2

Test 3 General Description

This test checks the 16 bit register's LOAD and DECRE modes. The results are read via OUTPUT selector, latches and comparators.

Setting the mode:

The 16 bit register mode is selected by setting bit 6 of U808 to 1. Memory U522 is selected by writing hex5F to port hex05 (U502) and the following data is loaded in the memory U522 by writing to port hex06 (U118).

bit 5 & 7	bit 4 & 6	
0	0	load vector to register
1	0	Decrement

Setting the OUTPUT SELECTOR:

The OUTPUT SELECTOR is set to select OUT RA. Hex20 is written to port hex0C (U814) with the disabled RAM (U516).

Loading to the first latches:

The output of the registers is loaded to the first latches by reading from port hex07.

Reading the data loaded to the first latches:

The lower 8 bits are read by the same steps as vector VB0-VB7. The high 8 bit are read by the same steps as vector VB8-VB15.

Test 3 readback port:

The output of the register is read via the OUTPUT SELECTOR and the first latches.

Test 3 Run Sequence

1. Sets the output selector to OUT RA.
2. Selects the memories U504, U506, U508 and U510 by writing hex7C to port hex05 (U502).

3. Loads the vector hexAA to the memories by writing to port hex06.

4. The initial data (hexAAAA) is loaded to Register.

5. Selects the memory U522 for loading MC10 - MC13.

6. To set the register to a decremental mode, writes the data hexAF to port hex06 (write pulse).

7. Clocks to Register until the output of Register is hex9FFF.

8. The value of the register is read back after being loaded to the first latches after every clock.

Test 3 Error Code

The ADDR specifies the incremental or decremental mode. EXPECT is a number of clocks which are given to Register and ACTUAL is the output of the Register.

Error Indication

The same as the Test 2, excluding the following:

For a decremental mode:

ADDR = hexA0

CKT #	pin #	Level (ECL)
U600	7	L
	9	H
U602	7	L
	9	H
U604	7	L
	9	H
U606	7	L
	9	H

91S16 FUNCTION 4 INSTR

Circuit Overview

This test checks some of the sequence flow instructions. The multiplexer (U406)is controlled by micro-code MC6-MC9 which selects the sequence flow instruction. If the output (U406-8) of the multiplexer is low, it means that the PC should be loaded with a new 10 bit value at the next rising edge of the clock. If it is high, the PC is incremented by one.

Functional Description

This functional test includes the following:

Test 0 checks the ADVANCE and JUMP instruction.

Test 1 checks the IF RA=0 JUMP, IF RB=0 JUMP, and IF R=0 JUMP instruction.

Test 2 checks the IF KEY JUMP, IF END JUMP, and CALL RMT instruction.

Writing an instruction :

Memory U520 is selected, and a bit pattern which specifies an instruction is written to U520.

Readback a status

The output of the multiplexer U406-8 is passed to comparator U952 via U432B. The read status value is inverted by U432B. The output of U952 is transferred to the CPU bus via U960 by writing hex80 to port hex04.

Test 0 General Description

Test 0 checks that a correct control signal is given to the program counter from the multiplexer according to the ADVANCE/JUMP instruction. Test 0 contains the steps which include loading micro-code to memory, and reading the status.

When the ADVANCE instruction is written to memory U520, the /PE pin of the PC (U410-U414) should receive a high level signal from multiplexer U406.

When the JUMP instruction is written to the memory, the /PE pin of the PC should receive a low level signal from the multiplexer (U406).

Tested circuitry includes:

U118, U134, U218 (Schematic 92 & 93)
U406, U432 (Schematic 95)
U500, U502, U530, U532, U520, U422 (Schematic 96)
U900, U952, U960 (Schematic 100)

Test 0 Readback Port

A signal to the PC is passed to comparator U952 via NOR gate U432B. Then the comparator receives an inverted level of the multiplexer. The result is transferred to the BD2 bus through U960.

Test 0 Run Sequence

1. Clears the PC
2. Selects comparator U952 for reading the status by writing hex80 to port hex04.
3. Selects the memory U520 to write the micro-code MC6-MC9.
4. Writes the micro-code to U520.

Instruction	Write Data (micro-code)
ADVANCE	0100XXXX
JUMP	1000XXXX

5. Read the status (output of the multiplexer U406) for each case.

Test 0 Error Code

ADDR specifies the micro-code. EXPECT is the desired status and ACTUAL is the read value. The read status is inverted because it is read back through the NOR gate.

Error Indication

If the test fails, set the LOOPING field to ON.

Possible Cause 0

The ADDR specifies the executing instruction.

Instruction	ADDR
ADVANCE	hex40
JUMP	hex80

While these instructions execute, the following levels are maintained:

Levels

CKT #	pin #	Level (ECL)
U432	12	L
U424	11	L
U424	10	L
U406	24	H
U406	23	L
U520	17	L

If U432-12 is a high level, examine TEST 2 in FUNCTION 4 INTERRUPT.

For readback

CKT #	pin #	Level (TTL)
U502	12	L
U900	2	L
	19	L
	5	L
	16	L
	6	L
	15	L
	9	L
	12	H

For ADVANCE instruction

CKT #	pin #	Level (ECL)
U406	17	L
	19	H
	20	L
	21	L
	8	H

For JUMP instruction

CKT #	pin #	Level (ECL)
U406	17	H
	19	L
	20	L
	21	L
	8	H

Test 1 General Description

Test 1 checks the flow control instructions sent to the RA and RB registers. This test contains the steps which include writing the data to registers, writing the micro-code memory, and reading the status at the /PE pin of the program counter.

Writing the data to the RA and RB registers

Data to load to a register is written to the memory for vector and A clock is given to the RA and RB registers.

Writing an instruction

An instruction is written to the memory U520. The multiplexer selects a status line for each instruction according to the written pattern. A pattern for instruction is as follows.

Instruction	Write Data (micro-code)
IF RA=0 JUMP	0010XXXX
IF RB=0 JUMP	1100XXXX
IF R=0 JUMP	1010XXXX

New tested circuitry includes:

U406, U432 (Schematic 95)
U504, U506, U508, U510, U520 (Schematic 96)
U608, U610, U600, U602, U604, U606, U626, U628, U638, U640 (Schematic 97)

Test 1 Readback Port

The same as Test 0.

Test 1 Run Sequence

1. Disables all memories and sends a clock to RA and RB registers by reading from port hex05. Registers are cleared.
2. Selects the memory U520 and writes the micro-code for the IF RA=0 JUMP instruction to the memory by writing to port hex06.
3. Selects the comparator U952 for reading the status by writing hex80 to port hex04.
4. Reads the status at the output of multiplexer U406-8 from port hex04.
5. Writes the data hexFF to the vector RAM and produces a clock. A register loads data hexFF.
6. Repeats sequence 2, 3 and 4.
7. Repeats the sequence 1 to 6 for each instruction.

Test 1 Error Code

ADDR specifies the instruction. EXPECT is the desired status and ACTUAL is the read status. The read status data is the inverse of what was actually read back because of the NOR gate.

Error Indicator

Possible Error

If the test fails, execute the diagnostics FUNCTION 3 REGISTER. Verify that FUNCTION 3 REGISTER passes. ADDR specifies the executing instruction.

Instruction	ADDR
IF RA=0 JUMP	hex20
IF RB=0 JUMP	hexC0
IF R=0 JUMP	hexA0

Levels

CKT #	pin #	Level (ECL)
U432	12	L
U424	11	L
U424	10	L
U520	17	L

If U432-12 is a high level, examine TEST 2 in FUNCTION 4 INTERRUPT.

For readback

CKT #	pin #	Level (TTL)
U502	12	L
U900	2	L
	19	L
	5	L
	16	L
	6	L
	15	L
	9	L
	12	H

For IF RA=0 JUMP instruction

CKT #	pin #	Level (ECL)
U406	17	L
	19	L
	20	H
	21	L
	8	L or H (They are the same logic level as U626-2,15 minus a little delay time).

If U626-2,15 do not go to a low level or a high level, examine TEST 0 in FUNCTION 3 REGISTER.

For IF RB=0 JUMP instruction :

CKT #	pin #	Level (ECL)
U406	17	H
	19	H
	20	L
	21	L
	8	L or H (They are the same logic level as U628-2,15 minus a little delay time).

If U628-2,15 do not go to a low level or a high level, examine TEST 1 in FUNCTION 3 REGISTER.

For IF R=0 JUMP instruction

CKT #	pin #	Level (ECL)
U406	17	H
	19	L
	20	H
	21	L
	8	L or H (When both U626-2,15 and U628-2,15 U640-2 are low, U640-2, U406-8, and U626-2,15 go to the low level with little U628-2,15 delay time).

Test 2 General Description

Test 2 checks the IF KEY JUMP, IF END JUMP, CALL RMT and IF FULL JUMP instruction. Test 2 contains the steps which include clearing the latch, writing the instruction to the memory, and reading the status.

NOTE

The IF FULL JUMP instruction is also checked in the 91S32 Diagnostic Routine if the 91S32 exists.

Writing the instruction :

The same as Test 0 and Test instructions.

Clearing the latch :

The latches for the IF KEY JUMP instruction are U312B and U232B. They are cleared by setting a high level to bit 7 of U810 (port hex0A). At the same time, the latch for CALL RMT instruction is cleared by executing the IF FULL JUMP instruction.

Readback the status:

The same as Test 0.

Latch for the IF END JUMP instruction

Bit 7 of port hex07 (U804) is for the IF END THEN instruction. If data from a host computer is ended, the controller writes 1 to bit 7 of port hex07. Its signal is passed to the PC via multiplexer U406.

Latch for the CALL RMT instruction:

The micro-code for the CALL RMT instruction is written to memory U520. It is decoded at U408, sent to U216A, and loaded by a clock.

New tested circuitry includes

U216A, U316B, U956A (Schematic 93)
U312B, U232B, U304A, U332, U302, U334 (Schematic 94)
U408 (Schematic 95)

Test 2 Readback

The same as the status.

Test 2 Run Sequence

1. Clears latches U232B and U312B by writing 1 to bit 7 of port hex0A (U810).

2. To provide a KEY, writes 0 and 1 to bit 2 of the port hex0C (U814).

3. Selects the memory for the flow control instruction and writes it with the pattern 0001XXXX for the IF KEY JUMP instruction.

4. Reads back a status.

5. Clears the latches and reads back a status.

The following verify the IF END JUMP instruction.

6. Writes 1 to bit 7 of port hex07 (U804) and clocks latch U334A.

7. Selects memory U520 for the flow control instruction and writes it with the pattern 1110XXXX.

8. Reads back the status.

9. Writes 0 to bit 7 of port hex07 (U804) clocks latch U334A.

10. Reads back the status.

11. Clears latch U216A for CALL RMT instruction.

12. Writes the micro-code to memory U520 and clocks the memory.

13. Reads back the status.

14. Produces a clock for a LOAD END by writing 1 and 0 to bit 19 of U814.

15. Clocks the LOAD signal through U232B.

16. Writes pattern 0001XXXX to memory U520. The pattern specifies the IF FULL JUMP instruction.

17. Reads back the status at TP400 via gate U432.

18. Executes the IF FULL JUMP instruction, and clears latch U216A. U216A is used for holding CALL RMT bit.

19. Reads back a status.

Test 2 Error Code

ADDR specifies an instruction. EXPECT is a desired status and ACTUAL is the inverse of what was read back because of the NOR gate.

Error Indication

Possible Cause 0

The ADDR specifies the executing instruction.

Instruction	ADDR
IF KEY JUMP	hex90
IF END JUMP	hexE0
CALL RMT	hexD0
IF FULL JUMP	hex11
Reset CALL RMT	hex10

Verify that there are many pulses

Check Item	Check point
write pulse	U422-3
latch clock	U304-9
	U232-9
	U334-6

Levels

CKT #	pin #	Level (ECL)
U432	12	L
U424	10	L
U424	11	L

If U432-12 is a high level, examine TEST 2 in FUNCTION 5 INTERRUPT.

Possible Cause 1

IF KEY JUMP Instruction

Levels

CKT #	pin #	Level (ECL)
U406	17	H
	19	L
	20	L
	21	H

If they are an incorrect level, check FUNCTION VECTOR RAM.

When EXPECTED = hex04 and ACTUAL = hex00, check the logic level at each point.

CKT #	pin #	Level (ECL)
U312	11	L to H
U312	15	L
U232	15	L
U304	7	L
U332	7	L
U304	7	L

When EXPECTED = hex00 and ACTUAL = hex04, check the logic level at each point.

CKT #	pin #	Level (ECL)
U408	12	H to L
U302	11	L

Possible Cause 2

IF END JUMP Instruction

Levels

CKT #	pin #	Level (ECL)
U406	17	H
	19	H
	20	H
	21	L

When EXPECTED = hex04 and ACTUAL = hex00, check the logic level at each point.

CKT #	pin #	Level (ECL)
U334	7	L
	2	L

When EXPECTED = hex00 and ACTUAL = hex04, check the logic level at each point.

CKT #	pin #	Level (ECL)
U334	7	H
	2	H

Possible Cause 3

CALL RMT Instruction

When ADDR = hexD0, EXPECTED = hex01 and ACTUAL = hex00, check the logic level at each point.

CKT #	pin #	Level (ECL)
U406	17	H
	19	H
	20	L
	21	H
	8	H
U408	10	L

When ADDR := hex11, EXPECTED := hex04, ACTUAL := hex00 For latch U232A for load end is not set.

Check the logic level at each point.

CKT #	pin #	Level (ECL)
U406	17	L
	19	L
	20	L
	21	H
	8	L
U312	5	L
	2	L
U232	2	L

When ADDR := hex10, EXPECTED := hex00 and ACTUAL := hex04 Latch U216 for CALL RMT is not cleared by executing the IF FULL JUMP instruction.

Check the logic level at each point. If next setting is satisfied, a pulse appears at U216-5.

CKT #	pin #	Level (ECL)
U406	17	L
	19	L
	20	L
	21	H
	8	L
U232	2	L
U302	15	L
U304	12	L

91S16 FUNCTION 5 INTERRUPT

FUNCTION 5 General Description

This FUNCTION Test checks the stack and the interrupt circuitry. The operation of the stack is the same as the program counter, excluding after receiving an interrupt signal.

Test 0 writes a value to the stack (U416, U418 and U420) and resets it. The output of the stack is readback via the PC.

Test 1 exercises the PC to count from hex000 to hex3FF, and reads back the result every clock. This test also runs on power-up and verifies the count from hex2AA to hex3FF.

Test 2 checks a logic operation in the interrupt circuitry.

Test 0 General Description

This test checks the operation of the stack. The test contains the steps which include clearing and loading the stack.

Clearing the stack :

A reset pulse to the stack is generated by reading from port hex03.

Setting a mode and clocking the stack:

The operation of the stack is basically the same as the PC.

Tested circuitry includes:

U112, U118 (Schematic 92)
U134, U218 (Schematic 93)
U400, U402, U404, U406, U410, U412, U414, U416, U418, U420
U422, U424, U432 (Schematic 95)
U900, U934, U936, U938, U940, U942, U960 (Schematic 100)

Test 0 Readback Port

There is no readback port for the stack. The output of the stack has to be loaded to the program counter and is read as the output of the PC. The output of the stack is passed to the PC via Selector U400, U402 and U404 by disabling the memory U520. The PC is loaded from the stack with a clock pulse. The loaded data to the PC is read with the same method as Test 0 in FUNCTION 1 MEM ADDR.

Test 0 Run Sequence

Test 0 includes:

1. Clearing the stack by reading from port hex03 (U112).
2. Writing the data hex2AA to the memories U512, U514 and U516.
3. Writing hex8X, which specifies the JUMP instruction, to the memory U520.
4. Loading it to the stack by writing to port hex0D.
5. Loading the output of the stack to the PC by disabling RAM and writing to port hex0D.
6. Readback the PC.
7. Repeating the sequence from 1 to 6 with data hex155.

Test 0 Error Code

Step	Address	Expected	Actual
Step 0	hex0D	hexAA	hexAA (RAB0-RAB7)
	hex1D	hex02	hex02 (RAB8-RAB9)
Step 1	hex0D	hex00	hex00 (RAB0-RAB7)
	hex1D	hex00	hex00 (RAB8-RAB9)
Step 2	hex0D	hex55	hex55 (RAB0-RAB7)
	hex1D	hex01	hex01 (RAB8-RAB9)
Step 3	hex0D	hex00	hex00 (RAB0-RAB7)
	hex1D	hex00	hex00 (RAB8-RAB9)

Error Indication

Before this test is executed, it is a necessary that FUNCTION 1 MEM ADDR passes.

Possible Cause 0

Check that there are pulses when the LOOPING field is ON.

Check Item Check point

A clock for the PC at Pin 13 of U416

A reset pulse for the PC at Pin 12 of U416

Possible Cause 1

If the test fails, refer to the following table for devices checked. In the table, X in the Actual column specifies the position where the actual data does not match the expected data. N is a Hexadecimal value.

Address	Actual	Memory	Stack	MUX	PC	Readback
hex0D	hexNX	U512	U416	U400	U410	U936 & U938
	hexXN	U514	U418	U402	U412	U940 & U942
hex1D	hex0X	U516	U420	U404	U414	U934

If ACTUAL data is hexXX, check U520.

Possible Cause 2

Check for a logic level at each point.

While the test is running, the circuitry has the following condition.

Loading data to the stack

CKT #	pin #	level (ECL)
U218	12	L
TP400	2	L
U406	17	H
	19	L
	20	L
	21	L
U424	12	L
	13	L
U400	9	L
U402	9	L
U404	9	L

If U424-13 is a high level, execute test 2 in this function.

Test 1 General Description

This test checks the clear, count-up and readback of the program counter. The test contains the steps which include clearing, setting an incremental mode, and reading the counter.

Setting an incremental mode

For setting an incremental mode, pins 5 of U416-U420 are set to a high level by writing 1 to bit 2 at port hex0B (U812).

New tested circuitry includes

none.

Test 1 Readback Port

The same as Test 0. The results are read back through port hex04 (U960).

Test 1 Run Sequence

Test 1 includes:

1. Clearing the stack by reading from port hex03.

2. Setting an incremental mode by writing XXXXXX1X to port hex0B.
3. Counting up to 1023.
4. Readback the stack via the PC at every clock.

Test 1 Error Code

ADDR specifies hex0D. EXPECTED specifies a number of given clocks. ACTUAL is the output of the stack.

Error Indication

Possible Cause 0

Check a logic level at each point.

For an incremental mode :

CKT #	pin #	level (ECL)
U432	15	H
U424	10	H
	15	L

Possible Cause 1

If test fails while counting up, examine a bit according the table at Possible Cause 1 in Test 0 as a reference. Remember the ADDR is hex0D.

Test 2 General Description

Test 2 checks the interrupt circuitry. The test contains the steps which include making a stack hold state when an interrupt signal is received, and clearing the hold state when the RETURN instruction is executed. When a qualify signal is high, an interrupt signal is received to U308. The output of U308 is clocked in U306A which is treated by the PC as a clearing signal. An output of the PC, which is generated only when the PC is cleared, becomes a clock to U306B through U316C and clears U308. After the interrupt circuit receives an interrupt signal, the

output of U306B becomes a high level and the stack cannot accept a clock. This test checks the output of U306B. The output of U306B is cleared when the RETURN instruction is executed. The RETURN instruction is written to the memory as micro-code and a clock pulse is given. U306B becomes a low level. This level is verified again.

New tested circuitry includes:

U308, U306, U310, U316C (Schematic 94)
U406, U414, U432 (Schematic 95)
U900, U952, U960 (Schematic 100)

Readback Port

The same as the FUNCTION Test 4.

Test Run Sequence

1. Resets latch U306B.
2. Makes an interrupt signal by controlling U308.
3. Clocks an interrupt signal in U306A. The stack hold signal is then sent to the stack.
4. Reads back the level.
5. Writes the RETURN instruction to memory U520.
6. Provides a clock pulse and executes the RETURN instruction.
7. Reads back the status.

Read Error Code

ADDR specifies the checked circuitry, EXPECTED is the desired status, and ACTUAL is the readback status.

Error Indication

The ADDR value meanings are as follows:

ADDR	Checked function
hex01	Clears the hold signal for the stack.
hex02	A hold signal is set at U306-15 by an interrupt signal.
hex03	A hold signal is cleared by executing the RETURN instruction.

Possible Cause 0

If test fails, set the LOOPING field to ON, and check that there are signals at the following points:

Check Item	Test point
Reset pulse for the PC	TP440
Clock for a reset pulse	TP360
Clock for RETURN	U310-9

Possible Cause 1

When ADDR = hex01

Check for a pulse at U306-13, and check that U306-15 goes to a low level.

Possible Cause 2

When ADDR = hex02

Check circuit operation with an interrupt signal. Check the level at each of the following points.

CKT #	pin #	Level (ECL)
U308	2	H
	4	L
	5	H
U414	11	H
U316	9	L to H
U306	10	H

When ADDR = hex03

When checking a circuit operation by the RETURN instruction, it is necessary to know what the next condition is.

CKT #	pin #	Level (ECL)
U310	7	H
	4	L

91S16 FUNCTION 6 THRSH

NOTE

The DAC threshold fixture must be inserted before this test is run in order for the output voltages to be accurate. Refer to the Test and Verification section of this addendum for test fixture construction and installation details.

Circuit Overview

The DAC THRESHOLD circuitry controls the threshold for the P6460 data acquisition probe.

Functional Description

There is no readback in the DAC circuitry, therefore it cannot be tested. However, as an aid in calibration, an exercise routine is provided to facilitate adjustment and verification of the DAC.

DAC Threshold General Description

The THRSH function tests the DAC that specifies threshold levels on the external signal acquisition probe. Most of the circuitry being tested can be seen on schematic 94.

This function has no readback capability, so the output of the DAC must be monitored by connecting a digital multimeter between test point THRES and test point PGND. THRES and PGND can be found right behind the P6460 connector. The indications should

be 0.00 V, +1.60 V, -1.587 V and a ramp. The voltage between the two points is chosen using the SELECT key in the special DAC THRESHOLD SET field. This field only appears when the test has been individually selected and START SYSTEM has been pressed.

The DAC threshold test writes data corresponding to the voltage to be produced. This data is latched to DAC U320 as follows.

DATA (Hexadecimal	**OUTPUT**
00	-1.587 V
80	0.00 V
FF	+1.60 V

A ramp is generated by incrementing from 00 to FF with a delay to settle the DAC.

The steady voltages in the DAC threshold function can be used to determine the accuracy and correct operation of the DAC circuitry. The ramp can be used to determine whether all selectable voltages are available.

91S32 PATTERN GENERATOR DIAGNOSTICS

Organization of Diagnostic Function and Subset Description.

Information on the diagnostic function is organized as follows:

1. A listing of quick reference diagnostic function descriptions are given for the 91S32.

2. Each diagnostic function and its subtests are described in detail. Troubleshooting information is included.

There are eight diagnostic function descriptions. They are as follows:

Function 0	VECTOR GEN	(Vector Generator)
Function 1	LOOP COUNT	(Loop Counter)
Function 2	VECTOR RAM	(Vector Ram)
Function 3	CLK SEL	(Clock Selector)
Function 4	START FF	(Start Flip Flop)
Function 5	INHIBIT	(Inhibit from TRIG/TIMEBASE board)
Function 6	PROBE IF	(Probe Interface)
Function 7	BUFFER	(Input Buffer from 91S16 or 91S32 Clock Buffer)

Each of the above functions contains one to seven subtests. All of the functions above and their subtests are run on the 91S32.

The 91S32 runs all of the above functions except:

FUNCTION 3	CLK SEL	(Clock from TRIG/TIMEBASE board)
FUNCTION 4	START FF	(Start from TRIG/TIMEBASE board)
FUNCTION 5	INHIBIT	(Inhibit from TRIG/TIMEBASE board)
FUNCTION 7	BUFFER	(Input Buffer from 91S16)

Each function subsection (for example, Function 0 VECTOR GEN) details function and subtest operation as follows:

1. There is a theory overview of the circuitry exercised by the diagnostic function.

2. There is a brief description of the diagnostic routine within the function; This specifies how data is loaded and readback on the function level.

3. There is a description of the first subset (TEST X) within the function. This description includes:

   - o a diagram showing circuitry blocks of the 91S32 exercised by TEST X
   - o a detailed description of the subtest diagnostic routine including readback ports
   - o a detailed description of the TEST X pass sequence as the TEST X diagnostic routine is run.

QUICK REFERENCE FUNCTION DESCRIPTIONS

The following list briefly describes the diagnostic functions for the 91S32 Pattern Generator modules. If Functions are run individually, they should be run in the listed order under the module type. Only the functions for the module in question need be run.

The tests in each function can be selected individually only when the diagnostics are in a looping mode. For more information, refer to the description of LOOPING provided earlier in this section.

VECTOR GEN This function verifies that the vector generate counters can be loaded, incremented, and read. Most of the circuitry tested by the VECTOR GEN function is on schematic <103>.

LOOP COUNT This function verifies that the loop counters can be loaded, incremented, and read. Most of the circuitry tested by the LOOP COUNT function is on schematic <104>.

VECTOR RAM This function verifies that the operation of the vector RAM and the write enable registers. Most of the circuitry tested by the VECTOR RAM function is on schematics <104>, <106>, and <107>.

CLK SEL This function checks the operation of the clock selector gates and latches. Most of the circuitry tested by the CLK SEL function is on schematic <102>.

START FF This function tests the operation of the start flip flop set/reset circuit and trigger start line. Most of the circuitry tested by the START FF function is on schematic <104>.

INHIBIT This function tests the operation of the probe inhibit signal line. Most of the circuitry tested by the INHIBIT function is on schematics <101>, and <103>.

PROBE IF This function checks the operation of the probe interface latches, receivers, and buffers. Most of the circuitry tested by the PROBE IF function is on schematics <101>, and <105>.

BUFFER This function checks the operation of the clock buffer and receiver of 91S32 or address receiver and clock receiver of the signals from 91S16. Most of the circuitry tested by the BUFFER function is on schematics <102>, and <103>.

91S32 FUNCTION 0 VECTOR GEN

CIRCUIT OVERVIEW

The Vector Generator circuit consists of a 11-bit counter (composed of four individual counters) which supplies the address for the vector RAM. When these counters reach their maximum count (7FF) a load pulse for these counters counts up the loop counter.

FUNCTION DESCRIPTION

The VECTOR GEN function consists of eight separate tests.

Test 0 sets the page flip-flop to B.

Test 1 sets the page flip-flop to A.

Test 2 writes hex55 to each of the 4-bit counter U304 and U316 then reads the counter.

Test 3 writes hex05 to each of the 4-bit counter U330 and U340 then reads the counter.

Test 4 writes hexAA to each of the 4-bit counter U304 and U316 then reads the counter.

Test 5 writes hex04 to each of the 4-bit counter U330 and U340 then reads the counter.

Test 6 loads the vector generator with 0's and counts up to 555 then reads the count.

Test 7 loads the vector generator with 555 and counts up to 7FF then reads the count.

Readback ports

Test data is read from U650 <106> through U320, U326,U334, and U344 <103>. When U112-15 (RD5(H)) is asserted, U320 and U326 is enabled, and data is sent from the RA0A-RA7A bus to the RDB0-RDB7 bus. When U112-9 (RD6(H)) is asserted, U334 and U344 are enabled, and data is sent from RA8A-RA9A and PAGE SELECT to RDB0-RDB7.

Test 0 General Description

This test sets the U348A flip-flop to PAGE-B mode using port #0F from U106 -15.

Test 0 Readback Port

Test 0 result is read back from port 03 (U650 on schematic <106>) through U344-7 on schematic <103>.

Test 0 Run Sequence

1. Hex00 is written to port 0A (U314) <103>.
2. A pulse is sent to the port 0E. This sets the page to B.
3. Hex40 is written to port 08 (U112) <101> so that the address data can be read.
4. The test passes if hex10 is read at port 03.

Test 1 General Description

This test sets the U348A flip-flop to PAGE-A mode using port #0E from U106 -14.

Test 1 Readback Port

Test 1 result is read back from port 03 (U650 on schematic <106>) through U344-7 on schematic <103>.

Test 1 Run Sequence

1. Hex00 is written to port 0A (U314) <103>.
2. A pulse is sent to port 0F. This sets the page to A.
3. Hex40 is written to port 08 (U112) <101> so that the address data can be read.
4. The test passes if hex 00 can be read at port 03.

Test 2 General Description

This test loads U302 hex55 and sends it to U304 and U316 using the MPU clock, then U306 and U316 select the data for page-A memory address bus RA0A-RA7A.

Test 2 Readback Port

Test 2 result are read back from port 03 (U650 on schematic <106>) through U320 and U326.

Test 2 Run Sequence

1. A MPU clock path is selected.
2. Hex55 is written to port 09 (U302) <103>.
3. Hex00 is written to port 0A (U314) <103>.
4. A clock is sent from port 04 to load the data from U302 to U304 and U316.
5. The test passes if hex55 can be read at port 03.

Test 3 General Description

This test loads U314 hex05 and sends it to U330 and U340 using the MPU clock then U332 select the data for page-A memory address bus RA8A-RA9A.

Test 3 Readback Port

Test 3 results are read back from port 03 (U650 on schematic <106>) through U334-6,7 and U344-7.

Test 3 Run Sequence

1. An MPU clock path is selected.
2. Hex05 is written to port 0A (U314) <103>.
3. A clock is sent from port 04 to load the data from U314 to U330 and U340.
4. The test passes if hex05 is read at port 03.

Test 4 General Description

This test loads U302 with hexAA and sends it to U304 and U316 using the MPU clock, then U306 and U316 select the data for page-A memory address bus RA0A-RA7A.

Test 4 Readback Port

Test 4 results are read back from port 03 (U650 on schematic <106>) through U320 and U326.

Test 4 Run Sequence

1. An MPU clock path is selected.
2. HexAA is written to port 0 (U304) <103>.
3. A clock is sent from port 04 to load the data from U302 to U304 and U316.
4. The test passes if hexAA is read at port 03.

Test 5 General Description

This test loads U314 hex04 and sends it to U330 and U340 using the MPU clock then U332 selects the data for page-A memory address bus RA8A-RA9A.

Test 5 Readback Port

Test 5 results are read back from port 03 (U650 on schematic <106>) through U334-6,7 and U344-7.

Test 5 Run Sequence

1. An MPU clock path is selected.
2. Hex04 is written to port 0A (U314) <103>.
3. A clock is sent from port 04 to load the data from U314 to U330 and U340.
4. The test passes if hex04 is read at port 03.

Test 6 General Description

This test loads U302 and U314 with 0s and sends it to U304, U316, U330, and U340 using the MPU clock then single steps it to 555. After each step, the vector generator is read through RA0A-RA9A to verify that it contains the correct count.

Test 6 Readback Port

Test 6 result are read back from port 03 (U650 on schematic <106>) through U330, U340, U334, and U344.

Test 6 Run Sequence

1. An MPU clock path is selected.
2. Hex00 is written to port 09 (U304) <103>.
3. Hex00 is written to port 0A (U314) <103>.
4. A clock is sent from port 04 to load the data from U304 and U314 to U304, U316, U330, and U340.
5. Hex25 is written to port 0A (U314) <103> and the vector counter is set to the count mode.
6. 681 clock is sent from port 04.

7. The test passes if hex555 is read at port 03.

Test 7 General Description

This test loads U302 and U314 with 555 and sends it to U304, U316, U330, and U340 using the MPU clock then single steps it to 7FF. After each step, the vector generator is read through RA0A-RA9A to verify that it contains the correct count.

Test 7 Readback Port

Test 7 results are read back from port 03 (U650 on schematic <106>) through U330, U340, U334, and U344.

Test 7 Run Sequence

1. A MPU clock path is selected.
2. Hex55 is written to port 09 (U304) <103>.
3. Hex05 is written to port 0A (U314) <103>.
4. A clock is sent from port 04 to load the data from U304 and U314 to U304, U316, U330, and U340.
5. Hex25 is written to port 0A (U314) <103> and set the vector counter to the count mode.
6. 1366 clock is sent from port 04.
7. The test passes if hex7FF is read at port 03.

91S32 FUNCTION 1 LOOP COUNT

CIRCUIT OVERVIEW

The loop counter consists of a 16-bit up-counter (Us 404, 406, 412, 414, and 416) which generates the stop signal for the loop count function. When these counters reach their maximum count (FFFF) stop latch U418 is set.

FUNCTION DESCRIPTION

The LOOP COUNT function consists of five separate tests.

Test 0 loads the loop counter with FFFD, counts up to FFFE, and reads back the carry.

Test 1 loads the loop counter with FFFE, counts up to FFFF, and reads back the carry.

Test 2 loads the loop counter with EEE0, counts up to FFFE, and reads back the carry.

Test 3 loads the loop counter with EEE0, counts up to FFFF, and reads back the carry.

Test 4 loads the loop counter with 0000, counts up to FFFF, and reads back the carry.

Readback Ports

Test data is read from U650 <106> through U344 <103>. When U112-9 (RD6(H)) is asserted, U334 and U344 is enabled, then STOP/START data is sent through the RDB6 to the BD6.

Test 0 General Description

This test loads the loop counter with FFFD and then single steps it to FFFE. After a step, The stop latch U418B <104> is read to verify that it is not in the stop mode.

Test 0 Readback Port

Test 0 result is read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 0 Run Sequence

1. An MPU clock path is selected.
2. A pulse is sent to port 0F and PAGE is set to A.
3. HexFF is written to port 09 (U302) <103>.

4. Hex87 is written to port 0A (U314) <103>.
5. A clock is sent to port 04.
6. Hex07 is written to port 0A (U314) <103>.
7. A pulse is sent to port 0E and PAGE is set to B.
8. HexAE is written to port 07 (U104) <101>.
9. HexFD is written to port 04 (U406 and U412) <104>.
10. HexEE is written to port 07.
11. A pulse is sent to port 0F and PAGE is set to A.
12. Hex6E is written to port 07.
13. HexFF is written to port 04 (U414 and U416) <104>.
14. HexEE is written to port 07.
15. HexFF is written to port 09.
16. HexA7 is written to port 0A.
17. HexE8 is written to port 07.
18. A clock is sent to port 04.
19. Hex40 is written to port 08.
20. The test passes if hex80 is read at port 03.

Test 1 General Description

This test loads the loop counter with FFFE, then single steps it to FFFF. After a step, the stop latch U418 <104> is read to verify that it is in the stop mode.

Test 1 Readback Port

Test 1 results is read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 1 Run Sequence

1. An MPU clock path is selected.
2. A pulse is sent to port 0F and PAGE is set to A.
3. HexFF is written to port 09 (U302) <103>.
4. Hex87 is written to port 0A (U314) <103>.
5. A clock is sent to port 04.
6. Hex07 is written to port 0A (U314) <103>.
7. A pulse is sent to port 0E and PAGE is set to B.
8. HexAE is written to port 07 (U104) <101>.
9. HexFE is written to port 04 (U406 and U412) <104>.
10. HexEE is written to port 07.
11. A pulse is sent to port 0F and PAGE is set to A.
12. Hex6E is written to port 07.
13. HexFF is written to port 04 (U414 and U416) <104>.
14. HexEE is written to port 07.
15. HexFF is written to port 09.
16. HexA7 is written to port 0A.
17. HexE8 is written to port 07.
18. A clock is sent to port 04.
19. Hex40 is written to port 08.
20. The test passes if hex00 is read at port 03.

Test 2 General Description

This test loads the loop counter with EEE0, then single steps it to FFFE. After a step, the stop latch U418 <104> is read to verify that it is not in the stop mode.

Test 2 Readback Port

Test 2 Results is read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 2 Run Sequence

1. An MPU clock path is selected.
2. A pulse is sent to port 0F and PAGE is set to A.
3. HexFF is written to port 09 (U302) <103>.
4. Hex87 is written to port 0A (U314) <103>.
5. A clock is sent to port 04.
6. Hex07 is written to port 0A (U314) <103>.
7. A pulse is sent to port 0E and PAGE is set to B.
8. HexAE is written to port 07 (U104) <101>.
9. HexE0 is written to port 04 (U406 and U412) <104>.
10. HexEE is written to port 07.
11. A pulse is sent to port 0F and PAGE is set to A.
12. Hex6E is written to port 07.
13. HexEE is written to port 04 (U414 and U416) <104>.
14. HexEE is written to port 07.
15. HexFF is written to port 09.
16. HexA7 is written to port 0A.
17. HexE8 is written to port 07.
18. 4382 clock is sent to port 04.
19. Hex40 is written to port 08.
20. The test passes if hex00 is read at port 03.

Test 3 General Description

This test loads the loop counter with EEE0, then single steps it to FFFF. After a step, the stop latch U418 <104> is read to verify that it is in the stop mode.

Test 3 Readback Port

Test 3 result is read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 3 Run Sequence

1. A MPU clock path is selected.
2. A pulse is sent to port 0F and PAGE is set to A.
3. HexFF is written to port 09 (U302) <103>.
4. Hex87 is written to port 0A (U314) <103>.
5. A clock is sent to port 04.
6. Hex07 is written to port 0A (U314) <103>.
7. A pulse is sent to port 0E and PAGE is set to B.
8. HexAE is written to port 07 (U104) <101>.
9. HexE0 is written to port 04 (U406 and U412) <104>.
10. HexEE is written to port 07.
11. A pulse is sent to port 0F and PAGE is set to A.
12. Hex6E is written to port 07.
13. HexEE is written to port 04 (U414 and U416) <104>.
14. HexEE is written to port 07.
15. HexFF is written to port 09.
16. HexA7 is written to port 0A.
17. HexE8 is written to port 07.

18. 4383 clock is sent to port 04.

19. Hex40 is written to port 08.

20. The test passes of hex00 is read at port 03.

Test 4 General Description

This test loads the loop counter with 0000, then single steps it to FFFF. After a step, the stop latch U418 <104> is read to verify that it is in the stop mode.

Test 4 Readback port

Test 3 results is read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

1. An MPU clock path is selected.

2. A pulse is sent to port 0F and PAGE is set to A.

3. HexFF is written to port 09 (U302) <103>.

4. Hex87 is written to port 0A (U314) <103>.

5. A clock is sent to port 04.

6. Hex07 is written to port 0A (U314) <103>.

7. A pulse is sent to port 0E and PAGE is set to B.

8. HexAE is written to port 07 (U104) <101>.

9. Hex00 is written to port 04 (U406 and U412) <104>.

10. HexEE is written to port 07.

11. A pulse is sent to port 0F and PAGE is set to A.

12. Hex6E is written to port 07.

13. Hex00 is written to port 04 (U414 and U416) <104>.

14. HexEE is written to port 07.

15. HexFF is written to port 09.

16. HexA7 is written to port 0A.
17. HexE8 is written to port 07.
18. 65535 clock is sent to port 04.
19. Hex40 is written to port 08.
20. Data is read from port 03 and it is checked for hex80.

91S32 FUNCTION 2 VECTOR RAM

CIRCUIT OVERVIEW

The vector memory of the 91S32 consists of twenty 1024 X 4 bit RAMs for a total of 2048 words by 40 bits.

FUNCTION DESCRIPTION

TEST 0 checks the write enable, chip select and the read/write logic on the 91S32 memory.

Test 1 checks U600, U602, U700, and U702 memory.
Test 2 checks U604, U606, U704, and U706 memory.
Test 3 checks U610, U612, U708, and U710 memory.
Test 4 checks U614, U616, U712, and U714 memory.
Test 5 checks U608, U618, U716, and U718 memory.

Readback Ports

Test data is read from U650 <106> through U620, U622, U624, U626, U628, U630, U632, U634, U636, U638, U652, U654, U656, U658, U660, U662, U664, 666, U668, and U670.

Test 0 General Description

This test checks the write enable and the read/write logic on the 91S32 memory.

Test 0 Readback Port

Test 0 results are read back from port 03 (U650 on schematic <106>) through 620 to U670.

The 91S32 VECTOR RAM TEST 0 provides test results like the following:

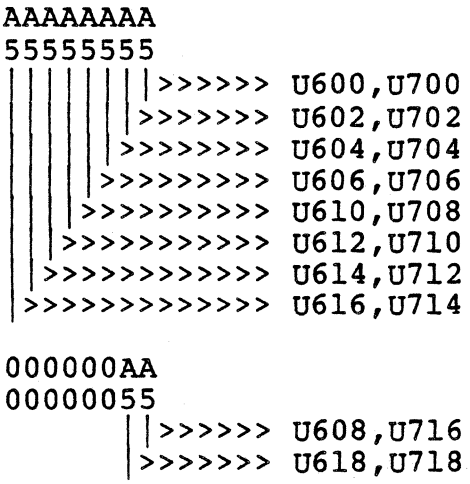
```
                          ADDR      EXPECTED      ACTUAL
2 VECTOR RAM  TEST 0   53EF A   000000AA      00000000        PASS
                         |  |       |             |             |
                         a  b       c             d             e
```

a. This indicates memory address error bit position plus one. If this value is 5 then address 4 line (pin 8) is bad.

b. This indicates test address pattern.

c. This indicates the error page, page-A or page-B.

d. This indicates expected data. This always shows AAAAAAAA, 55555555, 000000AA, or 00000055. The 000000AA and 00000055 pattern is used for U608, U618, U716, and U718. The AAAAAAAA and 55555555 pattern is used for another 10422 memory. This means the following.



e. This is the data pattern which is actually read from memory.

Test 0 Run Sequence

1. Hex00 is written to entire memory.
2. Hex55 is written to memory address hex001.
3. HexAA is written to memory address hex000.
4. Data is read from memory address hex001 and is expected to compare with hex55.
5. Hex00 is written to memory address hex001.
6. Hex55 is written to memory address hex002.
7. HexAA is written to memory address hex000.
8. Data is read from memory address hex002 and is expected to compare with hex55.
9. Hex00 is written to memory address hex002.
10. Hex55 is written to memory address hex004.
11. HexAA is written to memory address hex000.
12. Data is read from memory address hex004 and is expected to compare with hex55.

13. Hex00 is written to memory address hex004.
14. Hex55 is written to memory address hex008.
15. HexAA is written to memory address hex000.
16. Data is read from memory address hex008 and is expected to compare with hex55.
17. Hex00 is written to memory address hex008.
18. Hex55 is written to memory address hex010.
19. HexAA is written to memory address hex000.
20. Data is read from memory address hex010 and is expected to compare with hex55.
21. Hex00 is written to memory address hex010.
22. Hex55 is written to memory address hex020.
23. HexAA is written to memory address hex000.
24. Data is read from memory address hex020 and is expected to compare with hex55.
25. Hex00 is written to memory address hex020.
26. Hex55 is written to memory address hex040.
27. HexAA is written to memory address hex000.
28. Data is read from memory address hex040 and is expected to compare with hex55.
29. Hex00 is written to memory address hex040.
30. Hex55 is written to memory address hex080.
31. HexAA is written to memory address hex000.
32. Data is read from memory address hex080 and is expected to compare with hex55.
33. Hex00 is written to memory address hex080.
34. Hex55 is written to memory address hex100.
35. HexAA is written to memory address hex000.
36. Data is read from memory address hex100 and is expected to compare with hex55.
37. Hex00 is written to memory address hex100.
38. Hex00 is written to entire memory.
39. HexAA is written to memory address hex7FE.
40. Hex55 is written to menory address hex7FF.
41. Data is read from memory address hex7FE and is expected to compare with hexAA.
42. Hex00 is written to memory address hex7FE.
43. HexAA is written to memory address hex7FD.
44. Hex55 is written to memory address hex7FF.
45. Data is read from memory address hex7FD and is expected to compare with hexAA.
46. Hex00 is written to memory address hex7FD.
47. HexAA is written to memory address hex7FB.
48. Hex55 is written to memory address hex7FF/
49. Data is read from memory address hex7FB and is expected to compare with hexAA.
50. Hex00 is written to memory address hex7FB.
51. HexAA is written to memory address hex7F7.
52. Hex55 is written to memory address hex7EF.

53. Data is read from memory address hex7F7 and is expected to compare with hexAA.
54. Hex00 is written to memory address hex7F7.
55. HexAA is written to memory address hex7EF.
56. Hex55 is written to memory address hex7FF.
57. Data is read from memory address hex7DF and is expected to compare with hexAA.
58. Hex00 is written to memory address hex7EF.
59. HexAA is written to memory address hex7DF.
60. Hex55 is written to memory address hex7FF.
61. Data is read from memory address hex7DF and is expected to compare with hexAA.
62. Hex00 is written to memory address hex7DF.
63. HexAA is written to memory address hex7BF.
64. Hex55 is written to memory address hex7FF.
65. Data is read from memory address hex7BF and is expected to compare with hexAA.
66. Hex00 is written to memory address hex7BF.
67. HexAA is written to memory address hex77F.
68. Hex55 is written to memory address hex7FF.
69. Data is read from memory address hex77F and is expected to compare with hexAA.
70. Hex00 is written to memory address hex77F.
71. HexAA is written to memory address hex6FF.
72. Hex55 is written to memory address hex7FF.
73. Data is read from memory address hex6FF and is expected to compare with hexAA.
74. Hex00 is written to memory address hex6FF.
75. HexAA is written to memory address hex5FF.
76. Hex55 is written to memory address hex7FF.
77. Data is read from memory address hex5FF and is expected to compare with hexAA.
78. Hex00 is written to memory address hex5FF.
79. HexAA is written to memory address hex3FF.
80. Hex55 is written to memory address hex7FF.
81. DAta is read from memory address hex3FF and is expected to compare with hexAA.
82. Hex00 is written to memory address hex3FF.

The DAS should display EXPECT 0000 and ACTUAL 0000.

Test 1 General Description

This test loads U600, U602, U700, and U702 with 55 and is read through the memory readback ports (U's 620, 622, 624, 626, and 650 <106>). It is checked for hex55 then loaded with hexAA and verified as hexAA.

Test 1 Readback Port

Test 1 results are read back from port 03 (U650 on schematic <106>) through U620, U622, U624, and U626.

Test 1 Run Sequence

1. Hex00 is written to U600, U602, U700, and U702.
2. Hex55 is written to the same memory and the data is read back.
3. Hex00 is written to the tested address memory.
4. These data are checked one by one when the address is counted up.
5. HexAA is written to these memory and the data is read from these memory.
6. Hex00 is written to the tested address memory.
7. These data are checked one by one when the address is counted up.

Test 2 General Description

This test loads U604, U606, U704, and U706 with 55 and is read through the memory readback ports (U's 628, 630, 632, 634, and 650 <106>) and checked for accuracy. It then loads the memory with AA and checks for accuracy.

Test 2 Readback Port

Test 2 results are read back from port 03 (U650 on schematic <106>) through U628, U630, U632, and U634.

Test 2 Run Sequence

1. Hex00 is written to whole address of U604, U606, U704, and U702.
2. Hex55 is written to the memory and the data is read from these memory.
3. Hex00 is written to the tested address memory.
4. These data are checked one by one when the address is counted up.
5. HexAA is written to the memory and the data is read from these memory.
6. Hex00 is written to the tested address memory.
7. These data are checked one by one when the address is counted up.

Test 3 General Description

This test loads U610, U612, U708, and U710 with 55 and is read through the memory readback ports (U's 652, 654, 656, 658, and 650 <106>) and checked for accuracy. It then loads the memory with AA and checks for accuracy.

Test 3 Readback Port

Test 3 results are read back from port 03 (U650 on schematic <106>) through U652, U654, U656, and U658.

Test 3 Run Sequence

1. Hex00 is written to entire address of U610, U612, U708, and U710.
2. Hex55 is written to these memory and the data is read from the memory.
3. Hex00 is written to the tested address memory.
4. These data are checked one by one when the address is counted up.
5. HexAA is written to these memory and the data is read from the memory.
6. Hex00 is written to the tested address memory.
7. These data are checked one by one when the address is counted up.

Test 4 General Description

This test loads U614, U616, U712, and U714 with 55 and is read through the memory readback ports (U's 660, 662, 664, 666, and 650 <106>) and checked for accuracy. It then loads these memory with AA and checks for accuracy.

Test 4 Readback Port

Test 4 results are read back from port 03 (U650 on schematic <106>) through U660, U662, U664, and U666.

Test 4 Run Sequence

1. Hex00 is written to entire address of U614, U616, U712, and U714.
2. Hex55 is written to the memory and the data is read from the memory.

3. Hex00 is written to the tested address memory.
4. These data are checked one by one when the address is counted up.
5. HexAA is written to these memory and the data is read from the memory.
6. Hex00 is written to the tested address memory.
7. These data are checked one by one when the address is counted up.

Test 5 General Description

This test loads U608, U618, U716, and U718 with 55 and is read through the memory readback ports (U's 636, 638, 668, 670, and 650 <106>) and checked for accuracy. It then loads these memory with AA and checks for accuracy.

Test 5 Readback Port

Test 5 results are read back from port 03 (U650 on schematic <106>) through U636, U638, U668, and U670.

Test 5 Run Sequence

1. Hex00 is written to whole address of U608, U618, U716, and U718.
2. Hex55 is written to these memory and the data is read from the memory.
3. Hex00 is written to the tested address memory.
4. These data are checked one by one when the address is counted up.
5. HexAA is written to these memory and the data is read from the memory.
6. Hex00 is written to the tested address memory.
7. The data is checked one by one when the address is counted up.

91S32 FUNCTION 3 CLK SEL

CIRCUIT OVERVIEW

The clock selector is made up of NOR gates U208 and U216.

FUNCTION DESCRIPTION

The CLK SEL function consists of six separate tests.

Test 0 checks the step or trace mode clock.
Test 1 checks the pause line low state.
Test 2 checks the pause line high state.
Test 3 checks the MPU load clock.
Test 4 checks the 91A08 clock.
Test 5 checks the 91A32 clock.
Test 6 checks the EXT clock.

Readback Ports

Test data is read from U650 <106> through U344 <103>. When U112-0 (RD6 H)) is asserted, U334 and U344 is enabled, and then STOP/START signal line data is sent through the RDB6 to the BD6.

Test 0 General Description

This test checks the step or trace mode clock. The step clock gate U216-7 <102> is set low and sends a clock from hex04 port, then reads the state of flip-flop U418B <104>.

Test 0 Readback Port

Test 0 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

1. The loop counter is loaded with hexFFFD.
2. HexF0 is written to port 07 (U104) <101>.
3. A clock is sent from port 04.
4. Hex40 is written to port 08 (U112) <101>.
5. The test passes if hex00 is read at port 03.

Test 1 General Description

This test sets the pause line low. The pause line gate U208-13, the stop gate U216-5 and MPU clock gate U216-11 <102> are set low and send a clock from port hex04, then reads the state of stop flip-flop U418B <104>.

Test 1 Readback Port

Test 1 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 1 Run Sequence

1. The loop counter is loaded with hexFFFD.
2. HexF0 is written to port 07 (U104) <101>.
3. A clock is sent twice from port 04.
4. Hex40 is written to port 08 (U112) <101>.
5. Test passes if hex00 is read at port 03.

Test 2 General Description

This test sets the pause line high state. The pause line gate U208-13, the stop gate U216-5 and MPU clock gate U216-11 <102> are set low and send a clock from port hex04. It then reads 91S32 stop flip-flop U418B <104> state.

Test 2 Readback Port

Test 2 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 2 Run Sequence

1. Hex00 is written to the Trigger/Time Base port 02.
2. Hex07 is written to the Trigger/Time Base port 0D.
3. The loop counter is loaded with hexFFFD.
4. HexE8 is written to port 07 (U104) <101>.
5. HexCF is written to port 0C (U514) <105>.
6. HexF0 is written to port 0D (U728) <107>.
7. A clock is sent twice from port 04.
8. Hex40 is written to port 08 (U112) <101>.
9. Test passes if hex00 is read at port 03.
10. Hex08 is written to the Trigger/Time Base port 02.

Test 3 General Description

This test checks the MPU load clock. MPU clock gate U216-11 is<102> set low and receives a clock from hex04 port. It then reads the state of stop flip-flop U418B <104>.

Test 3 Readback Port

Test 3 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 3 Run Sequence

1. Hex00 is written to the Trigger/Time Base port 02.
2. Hex27 is written to the Trigger/Time Base port 0D.
3. The loop counter is loaded with hexFFFD.
4. HexE8 is written to port 07 (U104) <101>.
5. HexCF is written to port 0C (U514) <105>.
6. HexF0 is written to port 0D (U728) <107>.
7. A clock is sent twice from port 04.
8. Hex40 is written to port 08 (U112) <101>.
9. Test passes if hex08 is read at port 03.
10. Hex08 is written to the Trigger/Time Base port 02.

Test 4 General Description

This test checks the Trigger/Time Base 91A08 CLK line. The 91A08CLKCTRL line U208-5 <102> is set low and receives a 91A08 clock from Trigger/Time Base board. It then reads the state of stop flip-flop U418B <104>.

Test 4 Readback Port

Test 4 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 4 Run Sequence

1. The loop counter is loaded with hexFFFD.
2. HexE8 is written to Trigger/Time Base port 04.
3. HexF8 is written to port 07 (U104) <101>.
4. HexD4 is written to port 0D (U728) <107>.
5. A clock is sent twice from Trigger/Time Base port 09.
6. Hex40 is written to port 08.
7. Test passes if hex00 is read at port 03.

Test 5 General Description

This test checks the Trigger/Time Base 91A32 CLK line. The 91A32CLKCTRL line U208-7 <102> is set low and receives a 91A32 clock from Trigger/Time Base board. It then reads the state of stop flip-flop U418B <104>.

Test 5 Readback Port

Test 5 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 5 Run Sequence

1. The loop counter is loaded with hexFFFD.
2. HexE8 is written to Trigger/Time Base port 0D.
3. HexF8 is written to port 07 (U104) <101>.
4. HexB4 is written to port 0D (U728) <107>.
5. A clock is sent twice from Trigger/Time Base port 09.
6. Hex40 is written to port 08.
7. Test passes if hex00 is read at port 03.

Test 6 General Description

This test checks the Trigger/Time Base EXT CLK line. The PG EXT CLK CTRL line U208-11 <102> is set low and receives a PG EXT CLK from Trigger/Time Base board. It then reads the state of stop flip-flop U418B <104>.

Test 6 Readback Port

Test 6 results are read back from port 03 (U650 on schematic <106>) through U344-11 <103>.

Test 6 Run Sequence

1. The loop counter is loaded with hexFFFD.
2. Hex07 is written to Trigger/Time Base port 0D.
3. HexF8 is written to port 07 (U104) <101>.
4. Hex74 is written to port 0D (U728) <107>.
5. Hex17 is written to Trigger/Time Base port 0D.
6. Hex07 is written to Trigger/Time Base port 0D.
7. Hex17 is written to Trigger/Time Base port 0D.
8. Hex40 is written to port 08.
9. Test passes if hex00 is read at port 03.

91S32 FUNCTION 4 START FF

CIRCUIT OVERVIEW

The start flip>flop is made up of NOR gate and flip-flop U100 amd U418 <104>

FUNCTION DESCRIPTION

The START FF function consists of three separate tests.

Test 0 verifies the start flip-flop reset line.
Test 1 verifies the start flip-flop set line.
Test 2 verifies the start 91S32 line from Trigger/Time Base board.

Test 0 General Description

This test verifies the START flip-flop U418 <104> RESET line.

Test 0 Readback Port

Test 0 results are read back from port 03 (U650 on schematic <106>) through U344-9 <103>.

Test 0 Run Sequence

1. HexF9 is written to port 07.
2. HexF8 is written to port 07.
3. Hex40 is written to port 08.
4. Test passes if hex00 is read at port 03.

Test 1 General Description

This test verifies the START flip-flop U418 <104> SET line.

Test 1 Readback Port

Test 1 results are read back from port 03 (U650 on schematic <106>) through U344-9 <103>.

Test 1 Run Sequence

1. HexFA is written to port 07.
2. HexF8 is written to port 07.
3. Hex40 is written to port 08.
4. Test passes if hex40 is read at port 03.

Test 2 General Description

This test verifies the START flip-flop U418 <104> START line from Trigger/Time Base board.

Test 2 Readback Port

Test 2 result are read back from port 03 (U650 on schematic <106>) through U344-9 <103>.

Test 2 Run Sequence

1. Hex07 is written to Trigger/Time Base port 0D.
2. HexE4 is written to 91S32 port 0D.
3. HexF9 is written to port 07.
4. HexF8 is written to port 07.
5. Hex47 is written to Trigger/Time Base port 0D.
6. Hex40 is written to port 08.
7. Test passes if hex40 is read at port 03.

91S32 FUNCTION 5 INHIBIT

CIRCUIT OVERVIEW

The inhibit circuit is made up of OR, NOR, and EXCLUSIVE OR GATES as follows: U100 <104>, U228 <102>, U648 <106>, and U730 <107>.

FUNCTION DESCRIPTION

The INHIBIT function consists of two separate tests.

Test 0 checks the inhibit line high state.
Test 1 checks the inhibit line low state.

Readback Ports

Test data is read from U650 <106> through U344 <103>. When U112-9 (RD6 (H)) is asserted, U334 and U344 are enabled. INHIBIT signal line data is selected by U228-7 <102> and is sent through the RDB2 to BD2.

Test 0 General Description

This test checks for a high on the INHIBIT line from the Trigger/Time Base.

Test 0 Readback Port

Test 0 results are read back from port 03 (U650 on schematic <106>) through U334-9 <103>.

Test 0 Run Sequence

1. Hex07 is written to Trigger/Time Base port 0D.
2. HexF5 is written to port 0D.
3. Hex40 is written to port 08.
4. Test passes if hex00 is read at port 03.

Test 1 General Description

This test checks for a low on the INHIBIT line from the Trigger/Time Base.

Test 1 Readback Port

Test 1 results are read back from port 03 (U650 on schematic <106>) through U334-9 <103>.

Test 1 Run Sequence

1. Hex87 is written to Trigger/Time Base port 0D.
2. HexF5 is written to port 0D.
3. Hex40 is written to port 08.
4. Test passes if hex04 is read at port 03.

91S32 FUNCTION 6 PROBE IF

CIRCUIT OVERVIEW

The probe interface consists of U120 receiver, U516 latch, and U522 buffer.

FUNCTION DESCRIPTION

The PROBE IF function consists of two separate tests.

Test 0 writes hex05 to U520 and reads it from U120.
Test 1 writes hex0A to U520 and reads it from U120.

Readback Ports

Test data is read from U120 <101>. When U118-5 (PODSTATUS (L)) is asserted, U120 is enabled, and data is read from the data bus (BD0-BD3).

Test 0 General Description

This test writes hex05 to U520 port #03 and reads it from U120.

Test 0 Readback Port

Test 0 result are read back through port 01 (U120 on schematic <101>).

Test 0 Run Sequence

1. Data is read from port 02.
2. Hex05 is written to port 03.
3. Hex01 is written to port 02.
4. Test passes if hex05 is read at port 03.
5. Hex00 is written to port 02.
6. Hex0F is written to port 03.

Test 1 General Description

This test writes hex0A to U520 (port #03) and reads it from U120.

Test 1 Readback Port

Test 1 results are read back through port 01 (U120 on schematic <101>).

Test 1 Run Sequence

1. Data is read from port 02.
2. Hex0A is written to port 03.
3. Hex01 is written to port 02.
4. Test passes if hex0A is read at port 03.
5. Hex00 is written to port 02.
6. Hex0F is written to port 03.

91S32 FUNCTION 7 BUFFER

CIRCUIT OVERVIEW

The buffer circuit consists of three 10115 (U's 300, 308, and 312) and a 10116 (U220), and a 10H102 (U228).

FUNCTION DESCRIPTION

The BUFFER function consists of two blocks. The first block, which tests the 91S32 clock circuit, consists of three tests.

Test 0 checks the internal clock buffer and receiver.

Test 1 checks the master clock buffer and slave clock receiver.

Test 2 checks the slave clock receiver.

The second block tests the signal from the 91S16, and consists of seven separate tests.

Test 0 receives address data hex155 from the 91S16.

Test 1 receives address data hex2AA from the 91S16.

Test 2 checks the 91S16 clock for the 91S32.

Test 3 checks the 91S16 divided clock for the 91S32.

Test 4 verifies 91S16 PAGE, FULL line LOW state.

Test 5 verifies the 91S16 PAGE signal line.

Test 6 verifies the 91S16 FULL signal line.

Readback Ports

Test data is read from U650 <106> through U320, U326, U334, and U344 <103>. When U112-15 (RD5(H) is asserted, U320 and U326 are enabled and data is sent from RA0A-RA7A to RDB0-RDB7. When U112-9 (RD6(H)) is asserted, U334 and U344 are enabled and data is sent from RA8A-RA9A and PAGE SELECT signal to RDB0-RDB7.

This test changes according to the 91S16 configuration. If a 91S16 is installed, the buffer test runs from 0 to 6. If there is no 91S16 installed, only one test is run.

91S32 Only

Test 0 General Description

Test 0 results are read back from port 03 (U650 on schematic <106>) through U344-5 (schematic <103>).

Test 0 Run Sequence

1. Hex40 is written to port 0A on each 91S32 installed.
2. HexF4 is written to port 0D.
3. Hex3F is written to port 06.
4. HexEE is written to port 07
5. HexEC is written to port 07.
6. Hex00 is written to port 0A.
7. HexFF is written to port 0B.
8. Hex6F is written to port 00.
9. Hex40 is written to port 08.
10. Port 03 is set to hex00.
11. A clock is sent to port 04.
12. Data is read from port 03, and verifies that the data has changed to hex20.

Test 1 General Description

This test sends out an MPU clock from the master board to the slaved 91S32. It then verifies that the clock has been received.

Test 1 Readpack Port

Test results are read back from port 03 (U650 on schematic <106> through U344-5 <103>.

Test 1 Run Sequence

1. Hex40 is written to port 0A on all 91S32s installed.
2. Hex00 is written to port 0A on the master board.
3. Port 03 is set to hex20.
4. A clock is sent from the master board.
5. Data is read from port 03, and it is verified that the data has changed to hex00.

Test 2 General Description

This test sends no MPU clock from the master board, and the slaved 91S32 is checked for non-receipt of clock.

Test 2 Readback Port

Test results are read back from port 03 (U650 on schematic <106> through U344-5 <103>.

Test 2 Run Sequence

1. Hex40 is written to port 0A of all 91S32s installed.
2. Hex00 is written to port 0A of the master board.
3. Port 03 is set to hex20.
4. Data is read from port 03, and data is verified to be hex20.

91S32 with 91S16

Test 0 General Description

This test checks the address receiver, multiplexer, and readback comparator. The 91S16 sends address hex155 to P2, and:

U300, U308, and U312 <103> receive it,

U306, U318, and U332 select it,

U320, U326, U334 <103> and U650 <106> reads it.

This verifies the address to be hex155.

Test 0 Readback Port

Test 0 results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 0 Run Sequence

1. Address hex155 is sent from the 91S16.
2. Hex00 is written to port 0A.
3. A pulse is sent to port 0F.
4. Hex40 is written to port 08.
5. Data is read from port 03, and is memorized.
6. Hex00 is written to port 0A.
7. A pulse is sent to port 0F.
8. Hex20 is written to port 08.
9. Data is read from port 03 and added to the memorized data.
10. The data in step 9 is verified to be hex155.

Test 1 General Description

This test checks the address receiver, multiplexer, and readback comparator. The 91S16 sends address hex2AA to P2. U300, U308, and U312 <103> and U650 <106> read the address to verify that it is hex2AA.

Test 1 Readback Port

Test results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 1 Run Sequence

1. Address hex2AA is sent from the 91S16.
2. Hex00 is written to port 0A.
3. A pulse is sent to port 0F.
4. Hex40 is written to port 0A.
5. Data is read from port 03 and memorized.
6. Hex00 is written to port 0A.
7. A pulse is sent to port 0F.
8. Hex20 is written to port 08.
9. Data is read from port 03, and is added to the memorized data.
10. The data in step 9 is verified to be hex2AA.

Test 2 General Description

This test verifies the 91S16 clock to the 91S32.

Test 2 Readback Port

Test results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 2 Run Sequence

1. The 91S16 generates a clock for the 91S32.
2. The loop counter is loaded with hexFFFD.
3. HexF8 is written to port 07.
4. HexAF is written to port 0C.
5. The 91S16 sends a clock twice to the 91S32.
6. Hex40 is written to port 08.
7. Data is read from port 03, and verified to be Hex00.

Test 3 General Description

This test verifies the 91S16 divided clock to the 91S32.

Test 3 Readback Port

Test results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 3 Run Sequence

1. The 91S16 generates a divided clock for the 91S32.
2. The loop counter is loaded with hexFFFD.
3. HexF8 is written to port 07.
4. HexAF is written to port 0C.

5. The 91S16 sends a divided clock twice to the 91S32.
6. Hex40 is written to port 08.
7. Data is read from port 03, and verified to be Hex00.

Test 4 General Description

This test sets the 91S16 PAGE FULL line low, reads the PAGE signal level, sends a clock from the 91S16, reads the PAGE signal line again, and checks the difference.

Test 4 Readback Port

Test results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 4 Run Sequence

1. Hex00 is written to port 0A.
2. HexD8 is written to port 07.
3. The 91S16 sets PAGE and FULL lines low.
4. Hex40 is written to port 08.
5. Data is read from port 03, and is memorized.
6. A clock is sent from the 91S16.
7. Data is read from port 03, and compared with the memorized data.

Test 5 General Description

This test sets the 91S16 FULL signal line high, reads the PAGE signal level, sends a clock from the 91S16, reads the PAGE line again, and checks the difference.

Test 5 Readback Port

Test results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 5 Run Sequence

1. Hex00 is written to port 0A.
2. HexD8 is written to port 07.
3. Hex40 is written to port 08.
4. Data is read from port 03, and is memorized.
5. The 91S16 sets the PAGE line low.
6. The 91S16 sends a clock to the 91S32.
7. Data is read from port 03 and compared with the memorized data.

Test 6 General Description

This test sets the 91S16 FULL line high, reads the PAGE signal level, sends a clock from the 91S16, reads the PAGE line again, and checks the difference.

Test 6 Readback Port

Test results are read back from port 03 (U650 on schematic <106>) through U320, U326, and U334 <103>.

Test 6 Run Sequence

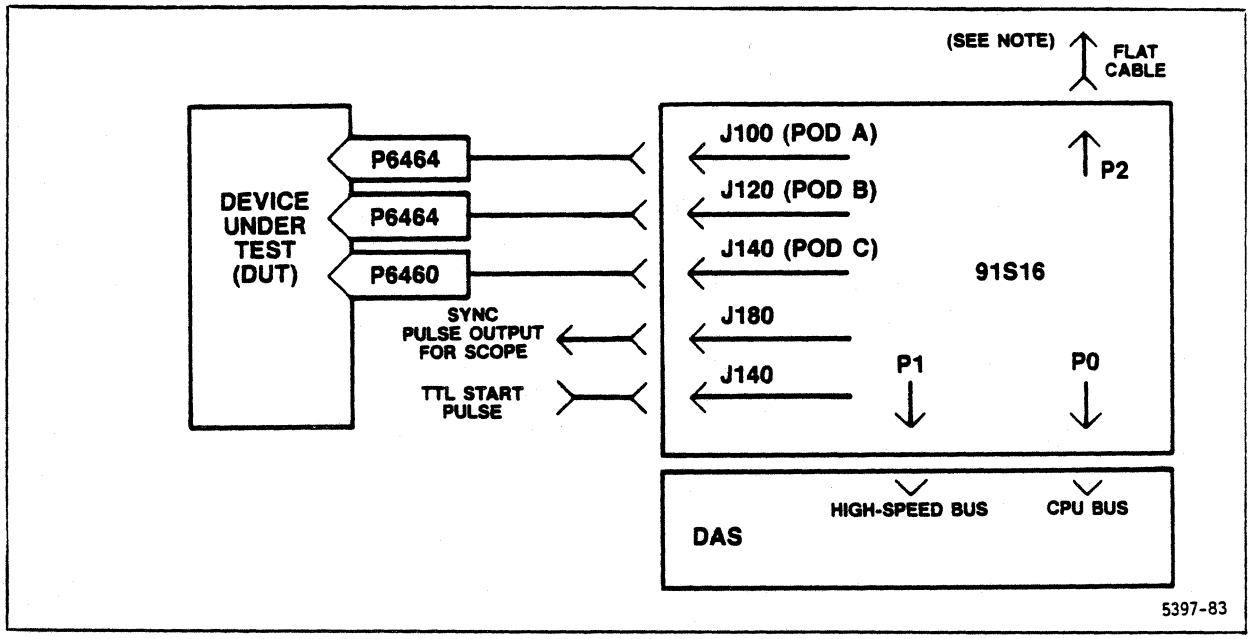
1. Hex00 is written to port 0A.
2. HexD8 is written to port 07.
3. The 91S16 generates a FULL signal low sequence.
4. Hex40 is written to port 08.
5. Data is read from port 03 and memorized.
6. The 91S16 sets FULL to a low level.
7. The 91S16 sends a clock to the 91S32.
8. Data is read from port 03 and compared with the memorized data.

Section 9
REFERENCE INFORMATION

This section contains diagrams and look-up tables to assist service personnel in identifying cable connections; locating test points, adjustments, and jumpers; and identifying signal functions.

System Connections

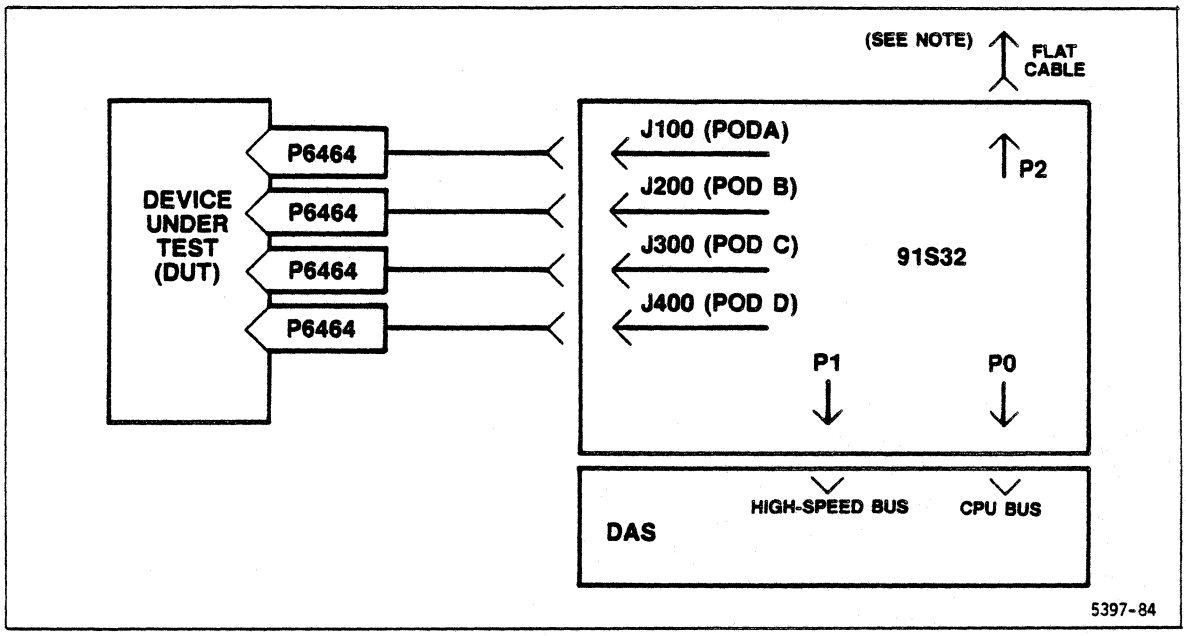
Figures 9-1 and 9-2 show how the 91S16 and 91S32 are connected to each other, to the DAS, and to the device under test. Table 9-1 identifies the signals passed between the 91S16 and the 91S32 in a master-slave configuration.



NOTE

This is an output to the slaved 91S32(s), and is not used in the 91S16-only configuration. See Table 9-1 for signal details.

Figure 9-1. 91S16 cable connections.



NOTES

1. Not used in the single-91S32 configuration.
2. This is an output to the slave 91S32(s) if this 91S32 is the master.
3. This is the input from the master 91S16 or 91S32 if this 91S32 is the slave.
4. See Table 9-1 for signal details.

Figure 9-2. 91S32 cable connections.

Table 9-1

91S16/91S32 P2 SIGNAL DETAIL

Signal	Pin	91S32 Jumper Connector
GND	B1 to B20	none
GND	A1	none
EXA0	A2	P302
EXA1	A3	P304
EXA2	A4	P306
EXA3	A5	P308
EXA4	A6	P310
EXA5	A7	P312
EXA6	A8	P314
EXA7	A9	P316
EXA8	A10	P318
EXA9	A11	P320
PAGE	A12	P322
FULL	A13	P324
S16INHIBIT(L)	A14	P102
GND	A15	none
S16CLK(H)	A16	P202
S16CLK(L)	A17	P204
GND	A18	none
ICLK(H)	A19	P206
ICLK(L)	A20	P208

Test Point, Jumper, and Adjustment Locations

Test points, jumpers, and adjustments are listed in Tables 9-2 and 9-3 (91S16) and Tables 9-4 and 9-5 (91S32). The tables are arranged in pairs. Test points, jumpers and adjustments are first listed alpha-numerically by component designation number; then the list is repeated alpha-numerically by the signal description. Schematic and board location zones are provided in each table. Refer to the Diagrams section of this addendum for parts-location drawings and schematics.

Table 9-2
91S16 TEST POINTS, JUMPERS, AND ADJUSTMENTS (COMPONENT LISTING)

Component	Location Zone Board	Location Zone Schematic	Description
DL700	B1	<98> C3	Last-latch clock line delay adjustment
DL720	B1	<98> E1	P6464 clock-line delay adjustment (with DL740)
DL740	B1	<98> E5	Part of P6464 clock-line delay adjustment (with DL720)
DL760	B1	<98> D3	POD-clock delay adjustment (with DL780)
DL780	B1	<98> D3	POD-clock delay adjustment (with DL760)
DL800	C2	<99> C1	First-latch clock line delay adjustment
DL820	C2	<99> C1	OUT CLOCK delay adjustment
R390	C4	<94> D5	Threshold adjustment, 0.00 V ±2 mV
R392	C4	<94> D5	Threshold adjustment, -1.587 V ±2 mV
TP200	A4	<93> A4	External clock input from P6460

Table 9-2 (cont.)
91S16 TEST POINTS, JUMPERS, AND ADJUSTMENTS (COMPONENT LISTING)

Component	Location Zone Board	Schematic	Description
TP240	D3	<93> C1	TTL START input circuit, output signal
TP280	E4	<93> F4	Clock reference for system clock
TP400	E2	<95> B5	Program counter output
TP440	E2	<95> D5	Address register reset
TP600	C2	<97> A1	Register clock
TP610	C2	<97> F1	First-latch clock line delay
TP700	B1	<98> E2	Last-latch clock delay
TP720	A1	<98> E1	P6464 clock-line delay
TP760	A2	<98> E5	Threshold, 0.00 V $\pm$2 mV
TP780	A1	<98> F1	P6464 clock-line reference
TP800	B3	<99> B2	Inhibit input
TP860	G2	<98> A4	Ground reference to DAS
TP910	F4	<98> A4	Ground reference to DAS
TP930	E3	<98> A3	Ground reference to DAS
TP940	F3	<98> A3	Ground reference to DAS
TP950	C2	<98> A3	Ground reference to DAS
TP960	B1	<98> A3	Ground reference to DAS
TP970	A3	<98> A3	Ground reference to DAS
TP980	F2	<93> F4	SIG CLOCK output to 91S32
TP990	G2	<98> A1	+3 V power supply

Table 9-3
91S16 TEST POINTS, JUMPERS, AND ADJUSTMENTS (SIGNAL LISTING)

Description	Location Zone Board	Schematic
Address register reset, TP440	E2	<95> D5
CLOCK output to 91S32, TP980	F2	<93> F4
Clock reference for system clock, TP280	E4	<93> F4
Clock from P6460, TP200	A4	<93> A4
First-latch clock line delay adjustment, DL800	C3	<99> D1
First-latch clock line delay, TP610	C2	<97> F1
Ground reference to DAS, TP860	G2	<98> A4
Ground reference to DAS, TP910	F4	<98> A4
Ground reference to DAS, TP930	E3	<98> A3
Ground reference to DAS, TP940	F3	<98> A3
Ground reference to DAS, TP950	C2	<98> A3
Ground reference to DAS, TP960	B1	<98> A3
Ground reference to DAS, TP970	A3	<98> A3
Inhibit input, TP800	B3	<99> B2
Last-latch clock line delay adjustment, DL700	B1	<98> C3
Last-latch clock delay, TP700	B1	<98> E2
OUT CLOCK delay adjustment, DL820	C2	<99> C1
P6464 clock-line delay adjustment, DL720 (with DL740)	B1	<98> E1
P6464 clock-line delay adjustment, DL740 (with DL720)	B1	<98> E5
P6464 clock-line delay, TP720	A1	<98> E1

Table 9-3 (Cont.)
91S16 TEST POINTS, JUMPERS, AND ADJUSTMENTS (SIGNAL LISTING)

Description	Location Zone Board	Schematic
P6464 clock-line reference, TP780	A1	<98> F1
POD-clock delay adjustment, DL760 (with DL780)	B1	<98> D3
POD-clock delay adjustment, DL780 (with DL760)	B1	<98> D3
Program counter output, TP400	E2	<95> B5
Register clock, TP600	C2	<97> A1
Threshold adjustment, 0.00 V ±2 mV, R390	C4	<94> D5
Threshold adjustment, 1.587 V ±2 mV, R392	C4	<94> D5
Threshold, 0.00 V ±2 mV, TP760	A2	<98> E5
TTL START input circuit, output of, TP240	D3	<93> C1
+3 V power supply, TP990	G2	<98> A1

Table 9-4
91S32 TEST POINTS, JUMPERS, AND ADJUSTMENTS (COMPONENT LISTING)

Component	Location Zone Board	Schematic	Description
DL140	D2	<105> B1	BCLK delay adjustment (with DL160)
DL160	D2	<105> B1	BCLK delay adjustment (with DL140)
DL200	D2	<105> C1	BCLK delay adjustment (with DL220)
DL220	D2	<105> C1	BCLK delay adjustment (with DL200)
DL240	B1	<105> E2	ACLOCKIN delay adjustment
DL260	B1	<105> E2	BCLOCKIN delay adjustment
DL280	C1	<105> E3	CCLOCKIN delay adjustment
DL300	C1	<105> E3	DCLOCKIN delay adjustment
J102	F2	<107> C5	Configuration jumper
J202	F1	<102> B5	Configuration jumper
J204	F1	<102> B5	Configuration jumper
J206	F1	<102> E2	Configuration jumper
J208	F1	<102> F2	Configuration jumper
J302	F1	<103> B3	Configuration jumper
J304	F1	<103> B3	Configuration jumper
J306	F1	<103> B3	Configuration jumper
J308	F1	<103> B3	Configuration jumper
J310	F1	<103> B3	Configuration jumper
J312	F1	<103> B3	Configuration jumper
J314	F1	<103> B3	Configuration jumper
J316	F1	<103> B3	Configuration jumper

Table 9-4 (cont.)
91S32 TEST POINTS, JUMPERS, AND ADJUSTMENTS (COMPONENT LISTING)

Component	Location Zone Board	Location Zone Schematic	Description
J318	F1	<103> B3	Configuration jumper
J320	F1	<103> B3	Configuration jumper
J322	F1	<103> B3	Configuration jumper
J324	F1	<103> B3	Configuration jumper
TP200	E1	<102> F3	ACLK to address multiplexer
TP300	A1	<104> F4	Ground reference to DAS
TP320	A3	<104> F4	Ground reference to DAS
TP340	D3	<104> F4	Ground reference to DAS
TP360	E1	<104> F4	Ground reference to DAS
TP380	E3	<104> F4	Ground reference to DAS
TP400	G1	<104> F4	Ground reference to DAS
TP420	G2	<104> F4	Ground reference to DAS
TP500	B2	<105> F2	LCLK0 to output latches
TP520	B2	<105> F3	LCLK1 to output latches
TP540	B3	<105> F3	LCLK2 to output latches
TP560	B4	<105> F4	LCLK3 to output latches
TP580	A1	<105> F2	ACLKIN probe clock to POD A
TP600	A2	<105> F2	BCLKIN probe clock to POD B
TP620	A3	<105> F3	CCLKIN probe clock to POD C
TP640	A4	<105> F3	DCLKIN probe clock to POD D
TP660	F2	<104> E3	+3 V power supply
TP680	E1	<104> E5	+5 V from DAS

Table 9-5
91S32 TEST POINTS, JUMPERS, AND ADJUSTMENTS (SIGNAL LISTING)

Description	Location Zone Board	Schematic
ACLK to address multiplexer, TP200	E1	<102> F3
ACLKIN probe clock to POD A, TP580	A1	<105> F2
ACLOCKIN delay adjustment, DL240	B1	<105> E2
BCLK delay adjustment, DL140 (with DL160)	D2	<105> B1
BCLK delay adjustment, DL160 (with DL140)	D2	<105> B1
BCLK delay adjustment, DL200 (with DL220)	D2	<105> C1
BCLK delay adjustment, DL220 (with DL200)	D2	<105> C1
BCLKIN probe clock to POD B, TP600	A2	<105> F2
BCLOCKIN delay adjustment, DL260	B1	<105> E2
CCLKIN probe clock to POD C, TP620	A3	<105> F3
CCLOCKIN delay adjustment, DL280	C1	<105> E3
Configuration jumper, J102	F2	<107> C5
Configuration jumper, J202	F1	<102> B5
Configuration jumper, J204	F1	<102> B5
Configuration jumper, J206	F1	<102> E2
Configuration jumper, J208	F1	<102> F2
Configuration jumper, J302	F1	<103> B3
Configuration jumper, J304	F1	<103> B3
Configuration jumper, J306	F1	<103> B3
Configuration jumper, J308	F1	<103> B3
Configuration jumper, J310	F1	<103> B3

Table 9-5 (Cont.)
91S32 TEST POINTS, JUMPERS, AND ADJUSTMENTS (SIGNAL LISTING)

Description	Location Zone Board	Schematic
Configuration jumper, J312	F1	<103> B3
Configuration jumper, J314	F1	<103> B3
Configuration jumper, J316	F1	<103> B3
Configuration jumper, J318	F1	<103> B3
Configuration jumper, J320	F1	<103> B3
Configuration jumper, J322	F1	<103> B3
Configuration jumper, J324	F1	<103> B3
DCLKIN probe clock to POD D, TP640	A4	<105> F3
DCLOCKIN delay adjustment, DL300	C1	<105> E3
Ground reference to DAS, TP300	A1	<104> F4
Ground reference to DAS, TP320	A3	<104> F4
Ground reference to DAS, TP340	D3	<104> F4
Ground reference to DAS, TP360	E1	<104> F4
Ground reference to DAS, TP380	E3	<104> F4
Ground reference to DAS, TP400	G1	<104> F4
Ground reference to DAS, TP420	G2	<104> F4
LCLK0 to output latches, TP500	B2	<105> F2
LCLK1 to output latches, TP520	B2	<105> F3
LCLK2 to output latches, TP540	B3	<105> F3
LCLK3 to output latches, TP560	B4	<105> F4
+3 V power supply, TP660	F2	<104> E3
+5 V from DAS, TP680	E1	<104> E5

Signal Glossary

The following signal glossaries are arranged in alphanumeric order. Each entry contains the signal mnemonic, the number of the schematic(s) where it can be found, and a description of the signal function. Table 9-6 lists 91S16 signals and Table 9-7 lists 91S32 signals.

Table 9-6
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
A0-A12	92	Address from the controller on the 91S16
ADDR REG RESET(H)	94, 95	Reset for the program counter
BA0-BA12	92	Address bus from the DAS Controller
BD0-BD7	92	Data bus to/from the DAS Controller
BRD(L)	92	Buffered read request from the DAS
BWR(L)	92	Buffered write request from the DAS
CHA0-CHA15	98	Positive pattern output to the P6464 probe at POD A
CHA0-CHA15(L)	98	Negative pattern output to the P6464 probe at POD A
CHB0-CHB15	98	Positive pattern output to the P6464 probe at POD B
CHB0-CHB15(L)	98	Negative pattern output to the P6464 probe at POD B
CLK A(H)	98	Positive clock line to the P6464 probe at POD A
CLK A(L)	98	Negative clock line to the P6464 probe at POD A
CLK B(H)	98	Positive clock line to the P6464 probe at POD B

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
CLK B(L)	98	Negative clock line to the P6464 probe at POD B
CLK SENSE(H)	93, 98	Detects a generated clock
CNTL LINE(H)	95	Checks the output of instruction multiplexer U406
COUNT OVER(H)	93, 95	Indicates the program counter has gone to overrun
CS0-CS5(L)	96	Code to select the enabled memory
DLA0-DLA2	98, 99	Clock delay control for POD A
DLB0-DLB2	98, 99	Clock delay control for POD B
ED0-ED7	96	Data line to the memory
EXA0-EXA9	96	Address lines to the 91S32
EXT CLK(H)	93	External positive clock from the P6460 probe
EXT CLOCK(L)	93	External negative clock from the P6460 probe
EXT JUMP POL(H)	93, 99	External signal polarity for the IF EXT JUMP instruction
EXT JUMP SET(H)	93, 99	Sets the IF EXT JUMP instruction to false
EXT JUMP(H)	93	External signal for IF EXT JUMP instruction from the P6460 probe
EXT JUMP(L)	93	External negative signal for IF EXT JUMP instruction from the P6460 probe
F INH A,B(H)	96, 97	Internal inhibit signal to the first latch

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
F LATCH CLK(H)	93, 99	Clock to the first latch
F LATCH STEP CLOCK(H)	92, 99	Clock for loading the pattern to the first latch
FULL RESET(L)	94	Indicates that the IF FULL JUMP instruction has been executed
FULL(H)	94	Page change request signal to the 91S32
HOLD/COUNT(H)	94, 95	Hold signal for the stack
IBA, IBB(H)	98	Internal inhibit signals to the last latch
IF END0(L)	94, 99	Indicates that KEY 47 has been received through GPIB
IF END1(L)	94, 95	Status for the IF END JUMP INSTRUCTION
IF EXT(L)	93, 95	Latched status for the IF EXT JUMP instruction
IF FULL(L)	94 95	Status for the IF FULL JUMP instruction
IF IRQ(L)	94, 95	Latched status for the IF IRQ JUMP instruction
IF KEY(L)	94, 95	Status for the IF KEY JUMP instruction
IF R=0(L)	95, 97	Checks whether the output of the 16-bit register is 0
IF RA=0(L)	95, 97	Checks whether the output of 8-bit register RA is 0
IF RB=0(L)	95, 97	Checks whether the output of 8-bit register RB is 0
IF RESET(L)	95, 97	Disable reset signal for several instructions
INH 2 OR/AND(H)	96, 99	Inhibit control

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
INHIBIT A, B(H)	98, 99	Internal inhibit signal to POD A or B
INHIBIT(H)	99	Positive external inhibit signal from the P6460 probe
INHIBIT(L)	99	Negative external inhibit signal line from the P6460 probe
INT INHIBIT DIS(H)	99	Internal inhibit disable
INT POL(H)	94, 99	Polarity for an interrupt signal
INT RESET(H)	94, 99	Resets the latch for an interrupt signal
INT RESET(L)	94, 95	Stack hold signal given by receiving an interrupt signal
INT SET(H)	94, 99	Sets the latch for an interrupt signal
INTERRUPT(L)	94	Negative interrupt signal line from the P6460 probe
INTERRUPT:(H)	94	Positive interrupt signal line from the P6460 probe
IRQ RESET(L)	94, 99	Indicates that the IF IRQ JUMP instruction has been executed
JA0-JA9	95	Address loaded to the program counter
JAB0-JAB9	95, 96, 100	Destination for the JUMP instruction
KA RESET(H)	93, 94	Resets the latch for CALL RMT instruction
KA(L)	93, 95	Indicates that the CALL RMT instruction has been executed

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
KEY CLK(H)	94, 99	Generated if a key is pressed while the program is running, used as a latch clock
KEY RESET(L)	95	Indicates that the IF KEY JUMP instruction has been executed
L & K RESET(H)	94	Resets the latch for the IF FULL JUMP and the IF KEY JUMP instruction
LOAD CLOCK(H)	94, 99	Used as the page-change signal to the 91S32, generated when the command KEY 46 is received from the GPIB
MAIN CLOCK	93	Clock source for the 91S32
MC0-MC1	100	Selects either the pattern or the output of a register as the output to the probe
MC10-MC11	97	Control for register RB
MC12-MC13	97	Control for register RA
MC16(H)	96, 98	Triggers data from the microcode memory
MC17(H)	94	Mask signal for an interrupt
MC2-MC3	100	Strobe signal line
MC4-MC5	96, 97	Internal inhibit signal line
MC6-MC9	95	Flow control instruction
OUT CLK	93, 99	Main clock to the output system
OUT CLK(L)	93, 97, 99	Clock to the register

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
OUT CLOCK 0(L)	92, 93	Clock to the output system
OUT LATCH CLK	98, 99	Clock line to the last latches
P CLK A(L)	92	Clock to the P6464 probe at POD A
P CLK B(L)	92	Clock to the P6464 probe at POD B
P CLK C(L)	92	Clock to the P6464 probe at POD C
P INHIBIT A, B(H)	99	Inhibit signal to the P6464 probe
PAGE(H)	96	Page change request signal to the 91S32
PAUSE ON/OFF(H)	93, 99	Turns the PAUSE signal on or off
PAUSE POL(H)	93	Selects the PAUSE polarity
PAUSE(H)	93	Pause line from the P6460 probe
PAUSE(L)	93	Inverse pause line from the P6460 probe
PC CLK 0(L)	92	Clock for incrementing the program counter
PC CLK	93, 95	Clock to the program counter
PC INCR(H)	95, 99	Sets the program counter to an incremental mode
PC RESET(L)	92, 94	Reset pulse for the program counter
PC SET(H)	95, 99	Clock hold signal for starting the pattern generator
PC0-PC9	95, 96, 100	Output of the program counter

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
PERSONALITY(H)	92	A memory map output from the DAS Controller that selects the personality ROMs
PGND SENSE(H)	94	The ground level fed back from an input probe
POD A, B, C DATA	92	Data line to the P6464 probe at POD A, B, or C
POD A, B, C READ(H)	92	Set the P6464 at POD A, B, or C to the read mode
POD A, B, C WRITE(H)	92	Set the P6464 at POD A, B, or C to the write mode
POFFSET SENSE(H)	94	Feeds back the offset level from an input probe
PORT(L)	92	Indicates when the slot-select logic is to write data to the selected module
PROBE DATA CLOCK(L)	92	Clock for loading the data into the probe
PROBE R/W(L)	92	Sets probes to the read/write mode
PROBE W DATA(L)	92	Loads the latch with the probe data
QUAL OFF/ON(H)	99	Turns the qualify signal line off or on
QUAL POL(H)	94, 99	Polarity for the qualify signal
QUALIFY(H)	94	Positive qualify signal line from the P6460 probe

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
QUALIFY(L)	94	Negative qualify signal line from the P6460 probe
R CLK	93, 94	Main clock to the external signal input system
RA0-RA7	97	The output of register A
RAB0-RAB9	95	Return address from the stack
RAM WE(L)	92, 96	Generates a write pulse for the RAM
RB0-RB7	97	The output of register B
READ 0(H)	93, 95	Selects the readback gate for the current status
READ 1-READ 8	100	Selects the desired read status
READ SEL(L)	92, 100	Selects a port for reading the status
READ STATUS GATE(L)	92	Enables a gate for reading the status
REG CLK OFF/ON	97, 99	Turns the clock gate to the registers off or on
RESET CLK(H)	93, 95	Clock for resetting the latch which is used as the start setup
RESET CLK(L)	92	Resets the latch for the start setup
RETURN(H)	94, 95	Indicates that the RETURN instruction has been executed
RS CLK 0	93	Clock pulse for the external signal latch

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
S16 CLK	93	Positive clock line to the 91S32
S16 CLK(L)	93	Negative clock line to the 91S32
S16 INHIBIT(L)	99	Inhibits the signal line to the 91S32
SCLK	93, 94	Clock source for the system
SEL 0(L)	92, 99	Loads data to latch U804
SEL 1(L)	92, 99	Loads data to latch U806
SEL 2(L)	92, 99	Loads data to latch U808
SEL 3(L)	92, 99	Loads data to latch U810
SEL 4(L)	92, 99	Loads data to latch U812
SEL 5(L)	92, 99	Loads data to latch U814
SEL 8/16 E(H)	99	Selects two 8-bit registers or one 16-bit register
SEL RAM(L)	92, 96	Selects the RAM to be read from or written to
SEL SLOT(L)	92	Indication from the DAS Controller slot-select logic as to which personality ROM is being read
SET OUT 0, 1(H)	97	Selects the output latch to the probe
SPC0-SPC9	96	Address to the pattern and microcode memory
SRD0-SRD7	93, 95, 100	Reads back the selected status signal

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
STACK RESET(H)	92, 95	Clears the content of the stack
START CONTROL 1(H)	93, 95	Setup signal used at pattern-generator start
START CONTROL 2(H)	95, 97	Controls a clock for the register at startup
START IN(H)	93	External trigger signal for starting the pattern generator
START SET(H)	94, 99	Setup signal for starting the system
STB A, B	98, 99	Strobe A or B
STEP CLK(L)	92, 93	A step clock for the system
STOP PG(H)	93	Start/stop control signal from the controller
STOP/START	93, 99	Controls the start/stop control signal
TD0-TD7	92, 94, 96, 99, 100	Data on the 91S16 data bus
THRESHOLD(L)	92	Threshold voltage control for the P6460 external signal probe
TRIG IN RESET(H)	99	Resets the stop/start control latch
TRIG IN SET(H)	99	Sets the stop/start control latch
TRIGGER CLK	98, 99	Clock line for the trigger output
TRIGGER POL(H)	93, 99	Sets polarity of the external start signal

Table 9-6 (Cont.)
91S16 SIGNAL GLOSSARY

Signal	Schematic	Description
TRIGGER(H)	98	Trigger signal output
V0-V15	97	Pattern output from the pattern selector to the first latch
VB0-VB15	97, 98, 100	Pattern from the first latches to the last latches
VMB0-VMB15	96, 97	Pattern generated from the memory
VTHRESH SENSE(H)	94	Feeds back the threshold level from an input source
VTHRESHOLD	94	Threshold for an input probe
91A08 INTL(H)	92	91A08 clock from the Trigger/Time Base
91A08 INTL(L)	93	91A08 negative clock from the Trigger/Time Base
91A32 INTL(L)	93	91A32 clock
91S32 CLK 0, 1, 2(H)	93, 99	Control clocks to the 91S32
91S32 CLK RESET(H)	93, 99	Sets the polarity of the S16 clock signal

Table 9-7
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
A0-A12	101, 102	Internal address bus
ACLK(H)	101, 102	Clocks the vector generation counter to count up or load the address data
ACLOCKIN(H)	105	High-speed clock output for POD A P6464 probe
ADATACLK	105	The clock for the POD A P6464 probe setup data
AIC(L)	101, 102	Trace/step clock control, controls the clock from the MPU when the trace/step mode is selected
BA0-BA12	101	Buffered address from the DAS Controller
BCLK(H)	102, 105	Clocks the last data latch
BCLOCKIN(H)	105	High-speed clock output for POD B P6464 probe
BD0-BD7	101, 102, 106	Buffered address from DAS Controller
BDATACLK	105	The clock for the POD B P6464 probe setup data
BRD(L)	101	Buffered read request from the DAS Controller
BRW(L)	101	Buffered write request from the DAS Controller

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
CARD ID(L)	102	Card identification signal which enables card ID buffer U122
CCLK(H) and	102, 103,	Clocks the loop counter
	104	the page latch
CCLOCKIN(H)	105	High-speed clock output for POD C P6464 probe
CCLOCKIN(L)	105	Inverse line for CCLOCKIN(H)
CDATACLK	105	The clock for the POD C P6464 probe setup data
CH0-CH8	106, 107	Two-line, high-speed data for the P6464 probe
DASINHC(L)	101, 107	DAS inhibit control which enables the inhibit signal from the DAS Controller
DATA CLK	101, 105	Clock for the P6464 probe setup data
DATA OUTA	101	Setup data input/output line for the POD A P6464 probe
DATA OUTB	101	Setup data input/output line for the POD B P6464 probe
DATA OUTC	101	Setup data input/output line for the POD C P6464 probe
DATA OUTD	101	Setup data input/output line for the POD D P6464 probe
DATA	101, 105	Probe data A (same as DATA OUTA)

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
DATB	101, 105	Probe data B (same as DATA OUTB)
DATC	101, 105	Probe data C (same as DATA OUTC)
DATD	101, 105	Probe data D (same as DATA OUTD)
DCLK	102, 103	Clock for the page flip-flop
DCLOCKIN(H)	105	High-speed clock output for POD D P6464 probe
DCLOCKIN(L)	105	Inverse line for DCLOCKIN(H)
DDATACLK	101, 105	The clock for the POD D P6464 probe setup data
EXA0-EXA9	103	Address from the 91S16
EXT GATE	101, 107	Controls external inhibit signal from 91S16 or DAS Controller
EXT INH(H)	101, 106, 107	External inhibit control from DAS data word, USED when internal inhibit is not used
FREE/PAGE	103	Selects the sequential mode or follows the 91S16 mode
FULL(H)	103	Page-full signal from the 91S16 when the 91S16 is in the CALL REMOTE mode and the 91S32 vector memory is reloaded
HALFCK	102, 103	Main clock divided by two

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
ICIC(L)	102, 105	Internal clock input control which enables the internal clock input gate
ICLK(H)	102	Internal clock used between multiple 91S32s
ICLK(L)	102	Inverse line for ICLK(H)
ICOC(L)	102, 103	Internal clock output control which enables the internal clock output
ID0-ID7	101, 104, 106, 107	Internal data bus 0-7 which supplies ECL-level MPU bus
INHIBIT(H)	106, 107	Inhibits P6464 probe output
INHIBIT(L)	106, 107	Inverse line for INHIBIT(H)
INPOL(H)	101, 106, 107	Same as EXTINH(H)
INTGATE(H)	107	Internal inhibit gate which disables the internal inhibit signal
KEEP(L)	101, 102	Keep-alive signal which enables the keep-alive-mode clock when the 91S32 follows the 91S16
LCLK0	105, 106	Last clock 0, clocks the POD A last latch

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
LCLK1	105, 106	Last clock 1, clocks the POD B last latch
LCLK2	105, 106	Last clock 2, clocks the POD C last latch
LCLK3	105, 106	Last clock 3, clocks the POD D last latch
LOOP COUNT(L)	103, 104	Enables the loop counter to count up
LSTOPM(L)	103, 104	Loop-stop monitor, goes low when the loop counter stops
MASKT(L)	101, 104	Mask trigger, enables the trigger-start signal
MODEA(L)	103, 104	Selects the A-page memory
MODEB(L)	103, 104	Selects the B-page memory
MPUCLK	101, 102	Clock line from the processor
MPUCLKCTRL(L)	101, 102	Enables the MPU clock line
MRD(L)	101, 102	Memory read, instructs the controller microprocessor to read the data bus
MWRM(L)	101, 104	Memory write mode, enables data to be written to the vector memory
PA 0	105	Probe A delay 0, sets probe A POD delay to 0 ns
PA 5	105	Probe A delay 5, sets probe A POD delay to +5 ns
PA-5	105	Probe A delay -5, sets probe A POD delay to -5 ns
PAGA	101, 103	Sets the page latch to page A

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
PAGB	101, 103	Sets the page latch to page B
PAGE(H)	103	Page change signal from the 91S16, changes the page-latch output
PAUSE(H)	101, 102	Enables the external pause signal
PB 0	105	Probe B delay 0, sets probe B POD delay to 0 ns
PB 5	105	Probe B delay 5, sets probe B POD delay to +5 ns
PB-5	105	Probe B delay -5, sets probe B POD delay to -5 ns
PC 0	105	Probe C delay 0, sets probe C POD delay to 0 ns
PC 5	105	Probe C delay 5, sets probe C POD delay to +5 ns
PC-5	105	Probe C delay -5, sets probe C POD delay to -5 ns
PD 0	105	Probe D delay 0, sets probe D POD delay to 0 ns
PD 5	105	Probe D delay 5, sets probe D POD delay to +5 ns
PD-5	105	Probe D delay -5, sets probe D POD delay to -5 ns
PERSONALITY(L)	101	Memory map from the DAS that selects the personality ROMs
PG EXT CLK CTRL(H)	101, 102	Enables the PG EXT CLK(L) input

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
PG EXT CLK(L)	102	External clock input from the DAS
PG EXT INT(H)	104	External interrupt from the DAS
PG EXT PAUSE(H)	102	External pause input from the DAS
PGND	106, 107	Ground for the P6464 probes
PODA INH	106, 107	Inhibit signal for POD A
PODB INH	106, 107	Inhibit signal for POD B
PORT 0(L)	101, 102	Port 0 write, writes to U206
PORT 2(L)	101, 105	Port 2 write, writes to U516
PORT 3(L)	101, 105	Port 3 write, writes to U520
PORT 9(L)	101, 103	Port 9 write, writes to U302
PORT10(L)	101, 103	Port 10 write, writes to U314
PORT11(L)	101, 105	Port 11 write, writes to U512
PORT12(L)	101, 105	Port 12 write, writes to U514
PORT13(L)	101	Port 13 write, writes to U728
PS0-PS9	103	Programmed start, start address data of the vector counter

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
PSTART(H)	101, 104	Pre-start, sets the loop counter start latch
RA0-RA9	103	Buffered address data from the 91S16
RA0A-RA9A	103, 106	Memory address for A-page memory
RA0B-RA9B	103, 107	Memory address for B-page memory
RB0-RB9	106	Extender address from 91S16
RD0-RD6	101, 103, 106	Enables one of the read-back blocks
RDB(L)	101, 106	Readback, enables data on the bus to be read
S16 CLK(H)	102	Clock from the 91S16
S16 CLK(L)	102	Inverse line for S16 CLK(H)
S16INHC	101, 107	Inhibit control, disables the inhibit signal from the 91S16
S16INHIBIT(L)	107	Inhibit input from the 91S16
SELINH	102, 103	The selected inhibit signal
SR4-SR10	103	Start register data, the original address of the vector counter

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
START(H)	101, 104	Sets the 91S32 start flip-flop
START/STOP	103, 104	Goes high when the 91S32 starts
STOP(H)	101, 104	Resets the 91S32 start flip-flop
STOP/START	103, 104	Inverse line for START/STOP
STOPGATE(L)	102, 105	Enables the 91S32 clock path
SYSCLK(L)	102, 105	System clock, enables the 91S16 clock gate when the 91S32 runs in the sequential mode
T/B OFF/ON	102, 104	Time base off/on control, controls the selected clock from the DAS Trigger/Time Base
VMB0-VMB39	106, 107	Vector memory bus, data from the memory to the output latch
WA0-WA4	104, 106	Write enable for the A-page 0-4 block memory
WB0-WB4	104, 107	Write enable for the B-page 0-4 block memory

Table 9-7 (Cont.)
91S32 SIGNAL GLOSSARY

Signal	Schematic	Description
WEA(L)	101, 104, 106	Write enable for the A-page memory
WEB(L)	101, 104, 107	Write enable for the B-page memory
WP(L)	101, 104	Write port, loads memory write block data
91A08 INTL CLK(L)	102	91A08 negative clock from the DAS Trigger/Time Base
91A08 CLK CTRL(L)	101, 102	91A08 clock control, enables the 91A08 clock
91A32 INTL CLK(L)	102	91A32 negative clock from the DAS Trigger/Time Base
91A32 CLK CTRL(L)	101, 102	91A32 clock control, enables the 91A32 clock

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

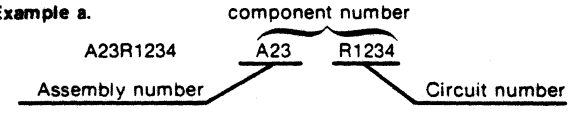
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

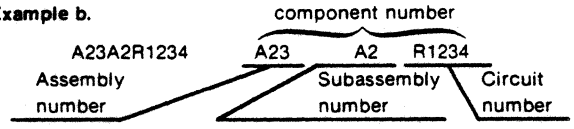
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE WI 53204
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPRESSWAY P O BOX 225012 M/S 49	DALLAS TX 75265
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR GROUP	5005 E MCDOWELL RD	PHOENIX AZ 85008
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
05828	GENERAL INSTRUMENT CORP GOVERNMENT SYSTEMS DIV	600 W JOHN ST	HICKSVILLE NY 11802
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV	464 ELLIS ST	MOUNTAIN VIEW CA 94042
07716	TRW INC TRW ELECTRONICS COMPONENTS TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
11236	CTS OF BERNE INC	406 PARR ROAD	BERNE IN 46711
13454	CRYSTEK CRYSTALS CORP	1000 CRYSTAL DR	FT MYERS FL 33901
18324	SIGNETICS CORP	811 E ARQUES	SUNNYVALE CA 94086
19701	MEPCO/ELECTRA INC A NORTH AMERICAN PHILIPS CO	P O BOX 760	MINERAL WELLS TX 76067
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
31433	UNION CARBIDE CORP ELECTRONICS DIV	PO BOX 5928	GREENVILLE SC 29606
52648	PLESSEY INC PLESSEY OPTOELECTRONICS AND MICROWAVE	1641 KAISER AVE	IRVINE CA 92714
54583	TDK ELECTRONICS CORP	755 EASTGATE BLVD	GARDEN CITY NY 11530
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195
57668	ROHM CORP	16931 MILLIKEN AVE	IRVINE CA 92713
71744	GENERAL INSTRUMENT CORP LAMP DIV	4433 N RAVENSWOOD AVE	CHICAGO IL 60640
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES IL 60016
76493	BELL INDUSTRIES INC MILLER J W DIV	19070 REYES AVE P O BOX 5825	COMPTON CA 90224
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
82389	SWITCHCRAFT INC SUB OF RAYTHEON CO	5555 N ELSTRON AVE	CHICAGO IL 60630
91637	DALE ELECTRONICS INC	P O BOX 609	COLUMBUS NE 68601

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34	670-8810-00			CIRCUIT BD ASSY:PATT GEN MODULE (91S16 ONLY)	80009	670-8810-00
A35	670-8811-00			CIRCUIT BD ASSY:PATT GEN MODULE (91S32 ONLY)	80009	670-8811-00
A36	670-8742-00	B010100	B010673	CIRCUIT BD ASSY:MAIN (P6464 ONLY)	80009	670-8742-00
A36	670-8742-01	B010674		CIRCUIT BD ASSY:MAIN (P6464 ONLY)	80009	670-8742-01
A37	670-8808-00			CIRCUIT BD ASSY:3V PWR SPLY (P6464 ONLY)	80009	670-8808-00
A34	670-8810-00			CIRCUIT BD ASSY:PATT GEN MODULE (91S16 ONLY)	80009	670-8810-00
A34C106	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C108	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C112	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C114	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C116	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C118	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C122	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C124	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C126	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C128	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C200	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C204	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C208	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C212	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C216	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C220	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C222	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C228	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C258	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C264	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C322	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C330	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C342	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C346	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C360	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C370	281-0792-00			CAP,FXD,CER DI:82PF,10%,100V	04222	MA101A820KAA
A34C372	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C374	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C376	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C378	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A34C380	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A34C382	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A34C384	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A34C386	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A34C388	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A34C390	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A34C394	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C396	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C398	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C500	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C502	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C504	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C506	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C508	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C510	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34C512	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C514	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C516	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C518	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C520	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C522	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C524	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C526	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C570	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C574	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C578	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C602	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C606	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C610	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C614	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C618	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C622	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C626	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C630	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C634	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C638	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C662	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C666	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C670	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C676	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C680	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C702	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C706	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C710	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C714	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C720	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C760	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C762	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C764	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C782	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C786	290-1014-00			CAP,FXD,ELCTLT:1UF,35V	80009	290-1014-00
A34C788	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C790	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C800	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C802	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C804	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C806	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C808	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C810	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C828	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C840	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C900	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C902	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C904	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C906	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C910	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C912	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C916	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C960	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C964	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A34C966	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C968	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A34C970	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C976	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34C986	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A34C988	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A34C990	290-1083-00			CAP,FXD,ELCTLT:220UF,20%,16V	80009	290-1083-00
A34C992	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A34C996	283-0833-00			CAP,FXD,CER DI:100UF,+80-20%,25V	80009	283-0833-00
A34CR240	152-0882-00			SEMICOND DVC,DI:SI,100MA,80V	80009	152-0882-00
A34CR320	152-0882-00			SEMICOND DVC,DI:SI,100MA,80V	80009	152-0882-00
A34CR340	152-0882-00			SEMICOND DVC,DI:SI,100MA,80V	80009	152-0882-00
A34CR700	152-0882-00			SEMICOND DVC,DI:SI,100MA,80V	80009	152-0882-00
A34CR720	152-0882-00			SEMICOND DVC,DI:SI,100MA,80V	80009	152-0882-00
A34CR960	152-0881-00			SEMICOND DVC,DI:SI,4A,30V	80009	152-0881-00
A34DL240	119-1891-00			DELAY LINE,ELEC:5NS,1000HM,3 SIP	80009	119-1891-00
A34DL280	119-1893-00			DELAY LINE,ELEC:3NS,1000HM,3 SIP	80009	119-1893-00
A34DL290	119-1891-00			DELAY LINE,ELEC:5NS,1000HM,3 SIP	80009	119-1891-00
A34DL310	119-1893-00			DELAY LINE,ELEC:3NS,1000HM,3 SIP	80009	119-1893-00
A34DL320	119-1891-00			DELAY LINE,ELEC:5NS,1000HM,3 SIP	80009	119-1891-00
A34DL400	119-1893-00			DELAY LINE,ELEC:3NS,1000HM,3 SIP	80009	119-1893-00
A34DL420	119-1893-00			DELAY LINE,ELEC:3NS,1000HM,3 SIP	80009	119-1893-00
A34DL600	119-1894-00			DELAY LINE,ELEC:2NS,1000HM,3 SIP	80009	119-1894-00
A34DL700	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A34DL720	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A34DL740	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A34DL760	119-1890-00			DELAY LINE,ELEC:5NS,INPUT 50/OUTPUT	80009	119-1890-00
A34DL780	119-1890-00			DELAY LINE,ELEC:5NS,INPUT 50/OUTPUT	80009	119-1890-00
A34DL800	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A34DL820	119-1922-00			DELAY LINE:13NS,1000HM,16 DIP	80009	119-1922-00
A34J100	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A34J120	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A34J140	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A34J160	131-3068-00			JACK,TELEPHONE:SUBMINIATURE,CKT BD MT	82389	MDPC-2A-RA
A34J180	131-3068-00			JACK,TELEPHONE:SUBMINIATURE,CKT BD MT	82389	MDPC-2A-RA
A34L952	108-1248-00			COIL,RF:FXD,80UH	80009	108-1248-00
A34L954	108-1248-00			COIL,RF:FXD,80UH	80009	108-1248-00
A34Q720	151-0221-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS246
A34Q722	151-0221-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS246
A34Q950	151-0809-00			TRANSISTOR:NPN,SI	80009	151-0809-00
A34Q952	151-0808-00			TRANSISTOR:PNP,SI	80009	151-0808-00
A34Q954	151-0807-00			TRANSISTOR:NPN,SI	80009	151-0807-00
A34R160	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A34R162	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A34R164	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A34R180	307-0904-00			RES NTWK,FXD,FI:(4)10K OHM,5%,0.125W EACH	80009	307-0904-00
A34R258	307-1183-00			RES NTWK,FXD,FI:(6),75-360,5%,0.125W	80009	307-1183-00
A34R260	307-1182-00			RES NTWK,FXD,FI:(6),620HM,5%,0.125W	80009	307-1182-00
A34R264	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R266	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R268	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R270	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A34R272	313-0331-00			RES,FXD,FILM:330 OHM,5%,0.166W	80009	313-0331-00
A34R274	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A34R276	313-0202-00			RES,FXD,FILM:2K OHM,5%,0.166W	80009	313-0202-00
A34R282	313-0331-00			RES,FXD,FILM:330 OHM,5%,0.166W	80009	313-0331-00
A34R284	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A34R286	313-0202-00			RES,FXD,FILM:2K OHM,5%,0.166W	80009	313-0202-00
A34R350	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R352	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R360	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R362	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R364	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34R366	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R368	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R370	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A34R372	321-0248-00			RES,FXD,FILM:3.74K OHM,1%,0.125W,TC=T0	19701	5043ED3K740F
A34R374	321-0142-00			RES,FXD,FILM:294 OHM,1%,0.125W,TC=T0	07716	CEA0294R0F
A34R376	321-0289-07			RES,FXD,FILM:10.0K OHM,0.1%,0.125W,TC=T9	19701	5033RE10K008
A34R378	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A34R380	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A34R382	321-0289-07			RES,FXD,FILM:10.0K OHM,0.1%,0.125W,TC=T9	19701	5033RE10K008
A34R384	321-0924-07			RES,FXD,FILM:40K OHM,0.1%,0.125W,TC=T9	07716	CEAE400018
A34R386	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A34R388	321-0414-04			RES,FXD,FILM:200K OHM,0.1%,0.125W,TC=T2	19701	5033RC200K0B
A34R390	311-2041-00			RES,VAR,NONWW:CKT BD,10K OHM,10%,0.5W	80009	311-2041-00
A34R392	311-0634-04			RES,VAR,NONWW:TRMR,500 OHM,20%,0.5W	80009	311-0634-04
A34R450	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R452	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R454	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R460	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R462	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R464	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R466	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R468	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R470	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R472	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R474	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R476	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R480	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R482	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R560	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A34R562	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A34R564	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R566	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R568	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R570	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R572	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R574	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R576	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R578	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R580	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R590	313-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.166W	80009	313-0272-00
A34R592	313-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.166W	80009	313-0822-00
A34R658	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R658	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R660	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R660	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R662	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R662	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R664	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R666	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R668	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R670	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R672	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R676	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R678	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R680	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R684	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R694	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R760	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R762	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34R764	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A34R766	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A34R770	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A34R818	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A34R850	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R852	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R854	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R856	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R858	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R860	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R862	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R864	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R866	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R868	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R870	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R872	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R874	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R876	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A34R940	307-1184-00			RES NTWK,FXD,FI:(4),8.2K-2.7K,5%,0.125W	80009	307-1184-00
A34R942	307-1184-00			RES NTWK,FXD,FI:(4),8.2K-2.7K,5%,0.125W	80009	307-1184-00
A34R944	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A34R950	308-0849-00			RES,FXD,WW:30W OHM,10%,2W	80009	308-0849-00
A34R952	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A34R954	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A34R956	313-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.166W	80009	313-0122-00
A34R958	321-0235-00			RES,FXD,FILM:2.74K OHM,1%,0.125W,TC=TO	07716	CEAD27400F
A34R960	321-0121-00			RES,FXD,FILM:178 OHM,1%,0.125W,TC=TO	07716	CEAD178R0F
A34R962	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A34R964	321-0221-00			RES,FXD,FILM:1.96K OHM,1%,0.125W,TC=TO	19701	5043ED1K960F
A34R966	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A34TP200	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP240	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP280	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP300	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP320	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP360	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP400	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP440	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP600	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP610	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP700	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP720	131-0589-00			TERM,PIN:0.46L X 0.025 SQ BRZ GLD PL	22526	48283-029
A34TP740	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP760	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP780	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP800	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP860	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP910	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP930	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP940	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP950	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP960	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP970	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34TP980	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A34TP990	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A34U100	156-1111-02			MICROCKT,DGTL:OCT BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A34U102	156-1111-02			MICROCKT,DGTL:OCT BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A34U106	156-1111-02			MICROCKT,DGTL:OCT BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A34U108	156-1111-02			MICROCKT,DGTL:OCT BUS XCVRS W/3 ST OUT	01295	SN74LS245N3

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34U112	156-2316-00			MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2316-00
A34U114	156-0541-02			MICROCKT,DGTL:DUAL 2-TO 4-LINE DCDR/DEMUX	04713	SN74LS139NDS
A34U116	156-0392-03			MICROCKT,DGTL:QUAD LATCH W/CLEAR,SCRN,	07263	74LS175PCQR
A34U118	156-2302-00			MICROCKT,DGTL:4/16 LINE DECODER	80009	156-2302-00
A34U120	160-3134-01			MICROCKT,DGTL:32768 X 8 EPROM,PRGM	80009	160-3134-01
A34U122	160-3133-00			MICROCKT,DGTL:32768 X 8 EPROM,PRGM	80009	160-3133-00
A34U124	160-3132-02			MICROCKT,DGTL:32768 X 8 EPROM,PRGM	80009	160-3132-02
A34U130	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U132	156-2300-00			MICROCKT,DGTL:OCTAL BUFFER W/3 STATE OUT	80009	156-2300-00
A34U134	156-2309-00			MICROCKT,DGTL:HEX INVERTER	80009	156-2309-00
A34U180	156-2301-00			MICROCKT,DGTL:QUAD BUFFER W/3 STATE	80009	156-2301-00
A34U182	156-2301-00			MICROCKT,DGTL:QUAD BUFFER W/3 STATE	80009	156-2301-00
A34U194	156-2310-00			MICROCKT,DGTL:HEX D TYPE FF	80009	156-2310-00
A34U200	156-2314-00			MICROCKT,DGTL:QUAD EXCL OR	80009	156-2314-00
A34U206	156-1667-01			MICROCKT,DGTL:8 LINE MUX	80009	156-1667-01
A34U208	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U210	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A34U212	156-0230-00			MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U214	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U216	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U218	156-1668-01			MICROCKT,DGTL:QUAD 2 INPUT OR/NOR	80009	156-1668-01
A34U222	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 N8 OR FB
A34U224	156-1676-01			MICROCKT,DGTL:TRIPLE 2 INPUT EXCL	80009	156-1676-01
A34U230	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A34U232	156-0230-00			MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U250	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U300	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05
A34U302	156-0543-02			MICROCKT,DGTL:HEX BUFFER	80009	156-0543-02
A34U304	156-0880-04			MICROCKT,DGTL:DUAL D-TYPE MASTER SLAVE FLIP FLOP	80009	156-0880-04
A34U306	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U308	156-0880-04			MICROCKT,DGTL:DUAL D-TYPE MASTER SLAVE FLIP FLOP	80009	156-0880-04
A34U310	156-0230-00			MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U312	156-0230-00			MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U314	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U316	156-0759-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR GATE	04713	MC10103 L OR P
A34U320	156-1311-01			MICROCKT,LINEAR:D/A CONVERTER	18324	NE5018N8
A34U322	156-1699-00			MICROCKT,LINEAR:DUAL BI-FET,OPNL AMPL	01295	TL288CP
A34U324	156-1020-01			MICROCKT,DGTL:DUAL MUX W/LATCH	80009	156-1020-01
A34U330	156-0880-04			MICROCKT,DGTL:DUAL D-TYPE MASTER SLAVE FLIP FLOP	80009	156-0880-04
A34U332	156-0759-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR GATE	04713	MC10103 L OR P
A34U334	156-0230-00			MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U400	156-1891-01			MICROCKT,DGTL:QUAD 2 LINE MUX	80009	156-1891-01
A34U402	156-1891-01			MICROCKT,DGTL:QUAD 2 LINE MUX	80009	156-1891-01
A34U404	156-1891-01			MICROCKT,DGTL:QUAD 2 LINE MUX	80009	156-1891-01
A34U406	156-1085-02			MICROCKT,DGTL:ECL,16 INP MULTIPLEXER	07263	F1001640C
A34U408	156-2313-00			MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2313-00
A34U410	156-2313-00			MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2313-00
A34U412	156-2313-00			MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2313-00
A34U414	156-2313-00			MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2313-00
A34U416	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A34U418	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A34U420	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A34U422	156-0759-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR GATE	04713	MC10103 L OR P
A34U424	156-0759-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR GATE	04713	MC10103 L OR P
A34U426	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05
A34U428	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34U430	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05
A34U432	156-2308-00			MICROCKT,DGTL:DUAL 4-5 INPUT OR/NOR	80009	156-2308-00
A34U500	156-1111-02			MICROCKT,DGTL:OCT BUS XCVRS W/3 ST OUT	01295	SN74LS245N3
A34U502	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U504	156-2307-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U504	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U506	156-2307-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U506	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U508	156-2307-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U508	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U510	156-2307-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U510	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U512	156-2307-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U514	156-2307-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U516	156-2307-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U518	156-2288-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A34U518	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U520	156-2307-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U520	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U522	156-2307-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U524	156-2307-00	300101	300235	MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2307-00
A34U524	156-2557-00	300236		MICROCKT,DGTL:1024 X 4,ECL,RAM	80009	156-2557-00
A34U530	156-0543-02			MICROCKT,DGTL:HEX BUFFER	80009	156-0543-02
A34U532	156-0543-02			MICROCKT,DGTL:HEX BUFFER	80009	156-0543-02
A34U600	156-1889-01			MICROCKT,DGTL:UNIVERSAL HEX COUNTER	80009	156-1889-01
A34U602	156-1889-01			MICROCKT,DGTL:UNIVERSAL HEX COUNTER	80009	156-1889-01
A34U604	156-1889-01			MICROCKT,DGTL:UNIVERSAL HEX COUNTER	80009	156-1889-01
A34U606	156-0641-00			MICROCKT,DGTL:UNIVERSAL HEXIDECIMAL CNTR	04713	MC10136L
A34U608	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A34U610	156-0746-02	300101	300235	MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A34U610	156-1891-01	300236		MICROCKT,DGTL:QUAD 2 LINE MUX	80009	156-1891-01
A34U612	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A34U614	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A34U616	156-0637-02			MICROCKT,DGTL:DUAL 4 TO 2 MUX	80009	156-0637-02
A34U618	156-0637-02			MICROCKT,DGTL:DUAL 4 TO 2 MUX	80009	156-0637-02
A34U620	156-0637-02			MICROCKT,DGTL:DUAL 4 TO 2 MUX	80009	156-0637-02
A34U622	156-0637-02			MICROCKT,DGTL:DUAL 4 TO 2 MUX	80009	156-0637-02
A34U626	156-2308-00			MICROCKT,DGTL:DUAL 4-5 INPUT OR/NOR	80009	156-2308-00
A34U628	156-2308-00			MICROCKT,DGTL:DUAL 4-5 INPUT OR/NOR	80009	156-2308-00
A34U630	156-0230-00			MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U632	156-0633-00			MICROCKT,DGTL:ECL,HEX D MASTER-SLAVE FF	04713	MC10176L
A34U634	156-0633-00			MICROCKT,DGTL:ECL,HEX D MASTER-SLAVE FF	04713	MC10176L
A34U636	156-0633-00			MICROCKT,DGTL:ECL,HEX D MASTER-SLAVE FF	04713	MC10176L
A34U638	156-1674-01			MICROCKT,DGTL:QUAD 2 INPUT AND GATE	80009	156-1674-01
A34U640	156-1642-02			MICROCKT,DGTL:TRIPLE 2-3-2 IN OR/NOR GATE	80009	156-1642-02
A34U700	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A34U702	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A34U704	156-1676-01			MICROCKT,DGTL:TRIPLE 2 INPUT EXCL	80009	156-1676-01
A34U706	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A34U708	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A34U710	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A34U712	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A34U714	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A34U716	156-0230-00	300101	300235	MICROCKT,DGTL:ECL,DUAL D MASTER-SLAVE FF	04713	MC10131(L OR P)
A34U716	156-1639-02	300236		MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A34U800	156-1676-01			MICROCKT,DGTL:TRIPLE 2 INPUT EXCL	80009	156-1676-01
A34U802	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A34U804	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U806	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A34U808	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U810	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U812	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U814	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U820	156-1674-01			MICROCKT,DGTL:QUAD 2 INPUT AND GATE	80009	156-1674-01
A34U900	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A34U902	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A34U904	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A34U906	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A34U908	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U910	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U912	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U914	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U916	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U918	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U920	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U922	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U924	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U926	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U928	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U930	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U934	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U936	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U938	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U940	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U942	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U946	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U948	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U950	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U952	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U954	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U956	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A34U958	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A34U960	156-2300-00			MICROCKT,DGTL:OCTAL BUFFER W/3 STATE OUT	80009	156-2300-00
A34U980	156-1778-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-1778-00
A35	670-8811-00			CIRCUIT BD ASSY:PATT GEN MODULE (91S32 ONLY)	80009	670-8811-00
A35C200	290-1083-00			CAP,FXD,ELCTLT:220UF,20%,16V	80009	290-1083-00
A35C202	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A35C204	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A35C206	283-0833-00			CAP,FXD,CER DI:100UF,+80-20%,25V	80009	283-0833-00
A35C400	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A35C402	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C404	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C406	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C408	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C410	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C412	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C414	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C416	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C418	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C420	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C422	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C424	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C426	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C428	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C430	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C432	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C434	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35C436	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C438	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C440	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C442	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C444	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C446	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C448	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C450	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C452	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C454	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C456	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C458	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C460	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C462	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C464	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C466	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C468	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C470	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C472	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C474	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C476	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C478	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C480	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C482	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C484	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C486	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C488	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C490	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C492	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C494	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C496	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C498	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C500	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C502	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C504	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C506	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C508	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C510	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C512	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C514	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C516	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C518	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A35C520	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A35C522	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A35C524	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A35C526	119-1762-00			FILTER,RFI:22000PF,50V WITH FERRITE BEAD	80009	119-1762-00
A35C600	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C602	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C604	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C606	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C608	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C610	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C612	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C614	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C616	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C618	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C620	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C622	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C624	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35C626	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C628	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C700	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A35C702	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C704	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C706	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C708	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C710	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A35C712	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A35C800	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C802	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C804	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35C806	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A35CR200	152-0881-00			SEMICOND DVC,DI:SI,4A,30V	80009	152-0881-00
A35DL120	119-1891-00			DELAY LINE,ELEC:5NS,1000HM,3 SIP	80009	119-1891-00
A35DL140	119-1892-00			DELAY LINE,ELEC:20NS,INPUT 50/OUTPUT	80009	119-1892-00
A35DL160	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A35DL180	119-1891-00			DELAY LINE,ELEC:5NS,1000HM,3 SIP	80009	119-1891-00
A35DL200	119-1890-00			DELAY LINE,ELEC:5NS,INPUT 50/OUTPUT	80009	119-1890-00
A35DL220	119-1890-00			DELAY LINE,ELEC:5NS,INPUT 50/OUTPUT	80009	119-1890-00
A35DL240	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A35DL260	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A35DL280	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A35DL300	119-1889-00			DELAY LINE,ELEC:10NS,INPUT 50/OUTPUT	80009	119-1889-00
A35DL320	119-1891-00			DELAY LINE,ELEC:5NS,1000HM,3 SIP	80009	119-1891-00
A35J100	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A35J102	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J200	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A35J202	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J204	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J206	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J208	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J300	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A35J302	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J304	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J306	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J308	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J310	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J312	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J314	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J316	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J318	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J320	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J322	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J324	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35J400	131-3087-00			CONN,RCPT,ELEC:HEADER,RIGHT ANGLE,2 X 17	22526	67950-001
A35J402	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35L202	108-1248-00			COIL,RF:FXD,80UH	80009	108-1248-00
A35L204	108-1248-00			COIL,RF:FXD,80UH	80009	108-1248-00
A35P102	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P202	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P204	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P206	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P208	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P302	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P304	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P306	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P308	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P310	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35P312	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P314	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P316	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P318	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P320	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P322	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P324	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35P402	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A35Q200	151-0809-00			TRANSISTOR:NPN,SI	80009	151-0809-00
A35Q202	151-0808-00			TRANSISTOR:PNP,SI	80009	151-0808-00
A35Q204	151-0807-00			TRANSISTOR:NPN,SI	80009	151-0807-00
A35R100	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A35R102	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R104	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R106	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R108	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R110	307-1184-00			RES NTWK,FXD,FI:(4),8.2K-2.7K,5%,0.125W	80009	307-1184-00
A35R112	307-1184-00			RES NTWK,FXD,FI:(4),8.2K-2.7K,5%,0.125W	80009	307-1184-00
A35R126	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R128	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R130	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R138	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A35R140	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A35R142	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A35R200	307-0493-00			RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125W RES	11236	750-81-R50 OHM
A35R202	307-0493-00			RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125W RES	11236	750-81-R50 OHM
A35R204	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R208	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R210	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R212	313-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.166W	80009	313-0122-00
A35R214	321-0235-00			RES,FXD,FILM:2.74K OHM,1%,0.125W,TC=T0	07716	CEAD27400F
A35R216	321-0121-00			RES,FXD,FILM:178 OHM,1%,0.125W,TC=T0	07716	CEAD178R0F
A35R218	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A35R220	308-0849-00			RES,FXD,WW:30W OHM,10%,2W	80009	308-0849-00
A35R230	321-0221-00			RES,FXD,FILM:1.96K OHM,1%,0.125W,TC=T0	19701	5043ED1K960F
A35R232	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A35R234	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R236	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R238	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R240	131-3411-00			CONN,RCPT,ELEC:LYES,FXD,0H0 DUMMY	80009	131-3411-00
A35R300	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R302	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R304	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R306	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R308	307-0866-00			RES NTWK,FXD,FI:8,100 OHM,5%,0.1W	80009	307-0866-00
A35R310	307-0866-00			RES NTWK,FXD,FI:8,100 OHM,5%,0.1W	80009	307-0866-00
A35R312	307-0866-00			RES NTWK,FXD,FI:8,100 OHM,5%,0.1W	80009	307-0866-00
A35R316	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R316	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R318	307-0866-00			RES NTWK,FXD,FI:8,100 OHM,5%,0.1W	80009	307-0866-00
A35R320	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R320	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R322	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A35R324	307-0866-00			RES NTWK,FXD,FI:8,100 OHM,5%,0.1W	80009	307-0866-00
A35R326	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R326	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R328	307-0913-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W EACH	80009	307-0913-00
A35R332	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R332	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35R334	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R334	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R336	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R336	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R338	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R338	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R400	307-0539-00			RES NTWK,FXD,FI:(7)510 OHM,10%,1W	11236	750-81-R510 OHM
A35R402	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R402	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R404	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R408	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R410	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R410	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R500	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R500	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R502	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R502	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R504	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R506	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R508	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R510	307-1185-00			RES NTWK,FXD,FI:(4),2.7K,1.3K,5%,0.125W	80009	307-1185-00
A35R516	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A35R600	307-0488-00	300101	300216	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A35R600	307-0488-01	300217		RES NTWK,FXD,FI:5,100 OHM,10%,0.125W	80009	307-0488-01
A35R602	307-0488-00	300101	300216	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A35R602	307-0488-01	300217		RES NTWK,FXD,FI:5,100 OHM,10%,0.125W	80009	307-0488-01
A35R604	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R604	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R606	307-0488-00	300101	300216	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A35R606	307-0488-01	300217		RES NTWK,FXD,FI:5,100 OHM,10%,0.125W	80009	307-0488-01
A35R608	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R608	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R700	307-0488-00	300101	300216	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A35R700	307-0488-01	300217		RES NTWK,FXD,FI:5,100 OHM,10%,0.125W	80009	307-0488-01
A35R702	307-0488-00	300101	300216	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A35R702	307-0488-01	300217		RES NTWK,FXD,FI:5,100 OHM,10%,0.125W	80009	307-0488-01
A35R704	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R704	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R706	307-0488-00	300101	300216	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A35R706	307-0488-01	300217		RES NTWK,FXD,FI:5,100 OHM,10%,0.125W	80009	307-0488-01
A35R708	307-0489-00	300101	300216	RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A35R708	307-0489-01	300217		RES NTWK,FXD,FI:7,100 OHM,10%,0.125W	80009	307-0489-01
A35R714	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35R716	307-1186-00			RES NTWK,FXD,FI:(4),2K,5%,0.125W	80009	307-1186-00
A35TP200	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP300	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP320	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP340	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP360	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP380	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP400	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP420	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP500	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP520	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP540	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP560	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP580	131-0589-00			TERM,PIN:0.46L X 0.025 SQ BRZ GLD PL	22526	48283-029
A35TP600	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35TP620	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP640	131-0590-03			TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131-0590-03
A35TP660	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35TP680	214-0579-00			TERM,TEST POINT:	80009	214-0579-00
A35U100	156-0205-00			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	04713	MC10102(P OR L)
A35U102	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U104	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A35U106	156-2302-00			MICROCKT,DGTL:4/16 LINE DECODER	80009	156-2302-00
A35U108	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U110	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U112	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U114	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U116	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U118	156-0541-02			MICROCKT,DGTL:DUAL 2-TO 4-LINE DCDR/DEMUX	04713	SN74LS139NDS
A35U120	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U122	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U124	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN	01295	SN74LS32NP3
A35U200	160-3134-01			MICROCKT,DGTL:32768 X 8 EPROM,PRGM	80009	160-3134-01
A35U202	160-3133-00			MICROCKT,DGTL:32768 X 8 EPROM,PRGM	80009	160-3133-00
A35U203	160-3132-02			MICROCKT,DGTL:32768 X 8 EPROM,PRGM	80009	160-3132-02
A35U204	156-0385-02			MICROCKT,DGTL:HEX INVERTER,SCRN	07263	74LS04PCQR
A35U206	156-1221-00			MICROCKT,DGTL:LSTTL,HEX D-TYPE FF,SCRN	01295	SN74LS378N3
A35U208	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U210	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U212	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A35U214	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A35U216	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U218	156-0636-00			MICROCKT,DGTL:ECL,DUAL 3-INP,3-OUT NOR GATE	04713	MC10111(L OR P)
A35U220	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A35U222	156-1778-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-1778-00
A35U224	156-0636-00			MICROCKT,DGTL:ECL,DUAL 3-INP,3-OUT NOR GATE	04713	MC10111(L OR P)
A35U226	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A35U228	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U300	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05
A35U302	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U304	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U306	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A35U308	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05
A35U310	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A35U312	156-0308-05			MICROCKT,DGTL:ECL,RECEIVER QUAD DIFF LINE	80009	156-0308-05
A35U314	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U316	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U318	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A35U320	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A35U324	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A35U326	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A35U328	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U330	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U332	156-0746-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NON-INV MUX	80009	156-0746-02
A35U334	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A35U338	156-0205-00			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	04713	MC10102(P OR L)
A35U340	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U344	156-1783-00			MICROCKT,LINEAR:QUAD COMPARATOR	80009	156-1783-00
A35U346	156-1674-01			MICROCKT,DGTL:QUAD 2 INPUT AND GATE	80009	156-1674-01
A35U348	156-0688-00			MICROCKT,DGTL:ECL,DUAL J-K MASTER-SLAVE FF	04713	MC10135L
A35U350	156-1674-01			MICROCKT,DGTL:QUAD 2 INPUT AND GATE	80009	156-1674-01
A35U352	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U400	156-0633-00			MICROCKT,DGTL:ECL,HEX D MASTER-SLAVE FF	04713	MC10176L
A35U402	156-1021-02			MICROCKT,DGTL:ECL,HEX & GATE MC10197L	80009	156-1021-02

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35U404	156-2303-00			MICROCKT,DGTL:QUAD 2 INPUT	80009	156-2303-00
A35U406	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U408	156-0639-00			MICROCKT,DGTL:ECL,DUAL 3-INP,3-OUT OR GATE	04713	MC10110P
A35U410	156-1021-02			MICROCKT,DGTL:ECL,HEX & GATE MC10197L	80009	156-1021-02
A35U412	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U414	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U416	156-1038-00			MICROCKT,DGTL:ECL,4 BIT BINARY COUNTER	07263	F100160C
A35U418	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A35U500	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U502	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U504	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U506	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A35U508	156-1668-01			MICROCKT,DGTL:QUAD 2 INPUT OR/NOR	80009	156-1668-01
A35U510	156-2311-00			MICROCKT,DGTL:QUAD LINE DRIVER	80009	156-2311-00
A35U512	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U514	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U516	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U518	156-1668-01			MICROCKT,DGTL:QUAD 2 INPUT OR/NOR	80009	156-1668-01
A35U520	156-2315-00			MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A35U522	156-2301-00			MICROCKT,DGTL:QUAD BUFFER W/3 STATE	80009	156-2301-00
A35U600	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U602	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U604	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U606	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U608	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U610	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U612	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U614	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U616	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U618	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U620	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U622	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U624	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U626	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U628	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U630	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U632	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U634	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U636	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U638	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U640	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U642	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U644	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U646	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U648	156-1518-00			MICROCKT,DGTL:ECL,QUINT EXCLUSIVE	07263	F100107DC
A35U650	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A35U652	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U654	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U656	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U658	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U660	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U662	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U664	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U666	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U668	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U670	156-2305-00			MICROCKT,LINEAR:DUAL COMPARATOR	80009	156-2305-00
A35U700	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U702	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U704	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A35U706	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U708	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U710	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U712	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U714	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U716	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U718	156-2288-00			MICROCKT,DGTL:1024 X 4 STATIC RAM	80009	156-2288-00
A35U720	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U722	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U724	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U726	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A35U728	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A35U730	156-1668-01			MICROCKT,DGTL:QUAD 2 INPUT OR/NOR	80009	156-1668-01
A36	670-8742-00	B010100	B010673	CIRCUIT BD ASSY:MAIN (P6464 ONLY)	80009	670-8742-00
A36	670-8742-01	B010674		CIRCUIT BD ASSY:MAIN (P6464 ONLY)	80009	670-8742-01
A36C143	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C145	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C150	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C151	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-10%,10V	55680	ULB1A221TEAANA
A36C250	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C350	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-10%,10V	55680	ULB1A221TEAANA
A36C355	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C455	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C463	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C464	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C470	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C475	283-5003-00			CAP,FXD,CER DI:0.01UF,10%,50V	54583	C3216X7R1H103K
A36C578	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	54583	C3216X7R1E104K
A36C579	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-10%,10V	55680	ULB1A221TEAANA
A36CR141	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A36CR142	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A36CR143	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A36CR165	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR265	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR266	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR466	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR560	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR562	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR564	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR570	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36CR576	152-0766-00			SEMICOND DVC,DI:SHOTTKY,SI,50V,SOT-23	04713	SMBD1082T1
A36DS125	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,AGED & SEL	71744	7153 AS 15
A36F120	159-0124-00			FUSE,WIRE LEAD:3A,125V,0.05SEC	75915	272003
A36F170	159-0124-00			FUSE,WIRE LEAD:3A,125V,0.05SEC	75915	272003
A36J160	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A36J360	131-2615-00			CONN,RCPT,ELEC:CKT BD,RTANG,17/34 CONT,MALE	22526	65820-005
A36Q100	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q101	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q102	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q103	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q104	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q160	151-0515-01			SCR:SI,MU-10	04713	SCR1256K
A36Q200	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q201	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q202	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q203	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q204	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36Q205	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q206	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q207	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q208	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q209	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q225	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q300	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q301	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q302	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q303	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q304	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q305	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q306	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q307	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q308	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q309	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q324	151-0730-01			TRANSISTOR:NPN,SI,TO-236	04713	MMBTH24T1
A36Q329	151-0730-01			TRANSISTOR:NPN,SI,TO-236	04713	MMBTH24T1
A36Q400	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q401	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q402	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q403	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q404	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q405	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q406	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q407	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q408	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q409	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q424	151-0730-01			TRANSISTOR:NPN,SI,TO-236	04713	MMBTH24T1
A36Q429	151-0730-01			TRANSISTOR:NPN,SI,TO-236	04713	MMBTH24T1
A36Q500	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q501	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q502	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q503	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q504	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q505	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q506	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q507	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q508	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q509	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q600	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q601	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q602	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q603	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q604	151-0663-01			TRANSISTOR:PNP,SI,TO-236	04713	MMBTH81T1
A36Q623	151-0730-01			TRANSISTOR:NPN,SI,TO-236	04713	MMBTH24T1
A36Q624	151-0730-01			TRANSISTOR:NPN,SI,TO-236	04713	MMBTH24T1
A36R110	307-1162-00			RES,FXD,FILM:150 OHM,5%,0.062W	91637	CRCW-0805-151JT
A36R112	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R113	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R114	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R115	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R120	307-1162-00			RES,FXD,FILM:150 OHM,5%,0.062W	91637	CRCW-0805-151JT
A36R121	307-1166-00			RES,FXD,FILM:3K OHM,5%,0.062W	91637	CRCW-0805-302JT
A36R122	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062W	91637	CRCW-0805-822JT
A36R123	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R124	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R125	307-1166-00			RES,FXD,FILM:3K OHM,5%,0.062W	91637	CRCW-0805-302JT
A36R145	307-1171-00			RES,FXD,FILM:510 OHM,5%,0.062W	91637	CRCW-0805-511JT

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36R151	307-1159-00			RES,FXD,FILM:1K OHM,5%,0.062W	91637	CRCW-0805-102JT
A36R161	307-1159-00			RES,FXD,FILM:1K OHM,5%,0.062W	91637	CRCW-0805-102JT
A36R212	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R213	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R214	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R215	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R216	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R217	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R218	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R219	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R220	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062W	91637	CRCW-0805-822JT
A36R221	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R222	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R223	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R224	307-1162-00			RES,FXD,FILM:150 OHM,5%,0.062W	91637	CRCW-0805-151JT
A36R225	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062W	91637	CRCW-0805-822JT
A36R226	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R227	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R228	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062W	91637	CRCW-0805-822JT
A36R229	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R252	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R254	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R256	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R258	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R260	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R265	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R312	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R313	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R314	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R315	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R316	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R317	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R318	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R319	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R320	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062W	91637	CRCW-0805-822JT
A36R321	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R322	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R323	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R325	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062W	91637	CRCW-0805-822JT
A36R326	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R327	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R328	307-1163-00			RES,FXD,FILM:200 OHM,5%,0.062W	91637	CRCW-0805-210JT
A36R352	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R354	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R355	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R356	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R358	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R360	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R361	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R362	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R363	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R364	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R365	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R366	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R367	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062W	91637	CRCW-0805-620JT
A36R370	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062W	91637	CRCW-0805-103JT
A36R412	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062W	91637	CRCW-0805-331JT
A36R413	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT
A36R414	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062W	91637	CRCW-0805-910JT

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36R415	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R416	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R417	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R418	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R419	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R420	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062M	91637	CRCM-0805-822JT
A36R421	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R422	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R423	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R425	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062M	91637	CRCM-0805-822JT
A36R426	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R427	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R428	307-1163-00			RES,FXD,FILM:200 OHM,5%,0.062M	91637	CRCM-0805-210JT
A36R452	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R454	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R456	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R458	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R460	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R465	307-1169-00			RES,FXD,FILM:62 OHM,5%,0.062M	91637	CRCM-0805-620JT
A36R472	307-1168-00			RES,FXD,FILM:47K OHM,5%,0.062M	91637	CRCM-0805-473JT
A36R512	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R513	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R514	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R515	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R516	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R517	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R518	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R519	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R520	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062M	91637	CRCM-0805-822JT
A36R521	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R522	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R523	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R524	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062M	91637	CRCM-0805-822JT
A36R525	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062M	91637	CRCM-0805-822JT
A36R526	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R527	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R528	307-1162-00			RES,FXD,FILM:150 OHM,5%,0.062M	91637	CRCM-0805-151JT
A36R560	307-1161-00			RES,FXD,FILM:1M OHM,5%,0.062M	91637	CRCM-0805-105JT
A36R561	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R562	307-1168-00			RES,FXD,FILM:47K OHM,5%,0.062M	91637	CRCM-0805-473JT
A36R564	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R565	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R567	307-1168-00			RES,FXD,FILM:47K OHM,5%,0.062M	91637	CRCM-0805-473JT
A36R572	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R574	307-1171-00			RES,FXD,FILM:510 OHM,5%,0.062M	91637	CRCM-0805-511JT
A36R576	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R612	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R613	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R614	307-1173-00			RES,FXD,FILM:91 OHM,5%,0.062M	91637	CRCM-0805-910JT
A36R615	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R620	307-1170-00			RES,FXD,FILM:8.2K OHM,5%,0.062M	91637	CRCM-0805-822JT
A36R621	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R622	307-1167-00			RES,FXD,FILM:330 OHM,5%,0.062M	91637	CRCM-0805-331JT
A36R625	307-1162-00			RES,FXD,FILM:150 OHM,5%,0.062M	91637	CRCM-0805-151JT
A36R662	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R672	307-1160-00			RES,FXD,FILM:10K OHM,5%,0.062M	91637	CRCM-0805-103JT
A36R674	307-1159-00			RES,FXD,FILM:1K OHM,5%,0.062M	91637	CRCM-0805-102JT
A36R676	307-1161-00			RES,FXD,FILM:1M OHM,5%,0.062M	91637	CRCM-0805-105JT
A36S550	175-9699-00			CA ASSY,SP,ELEC:2,26 AWG,6.0 L	80009	175-9699-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36U135	156-5021-00			MICROCKT,DGTL:CMOS,8 STATE SHIFT AND STORE	18324	HEF4094BTD
A36U150	156-1248-00			MICROCKT,DGTL:ECL,PRESCALER/DIVIDE BY 100	52648	SP8629
A36U535	156-5021-00			MICROCKT,DGTL:CMOS,8 STATE SHIFT AND STORE	18324	HEF4094BTD
A36U540	156-2127-00			MICROCKT,DGTL:DUAL 4 BIT STATIC SHIFT	18324	HEF4015BTD
A36U545	156-2127-00			MICROCKT,DGTL:DUAL 4 BIT STATIC SHIFT	18324	HEF4015BTD
A36U550	156-5020-00			MICROCKT,DGTL:CMOS,HEX INVERTER	18324	HEF4069UBTD
A36U555	156-2132-00			MICROCKT,DGTL:HEX NON-INVERTING BUFFER	18324	HEF40097BTD
A36U565	156-2298-00			MICROCKT,LINEAR:OPERATIONAL AMPLIFIER,DUAL	04713	LM358D
A36U635	156-2129-00			MICROCKT,DGTL:QUAD 2 INPUT AND GATE	18324	HEF4081BTD
A36U640	156-2131-00			MICROCKT,DGTL:QUAD 2 INPUT NAND	18324	HEF4093BTD
A36U645	156-2126-00			MICROCKT,DGTL:DUAL D-TYPE FLIP-FLOP	18324	HEF4013BTD
A36U650	156-5022-00			MICROCKT,DGTL:CMOS,TRIPLE 3 INPUT AND GATE	18324	HEF4073BTD
A36U655	156-2128-00			MICROCKT,DGTL:8 BIT STATIC SHIFT REGISTER	18324	HEF4021BTD
A36U660	156-2126-00			MICROCKT,DGTL:DUAL D-TYPE FLIP-FLOP	18324	HEF4013BTD
A36VR140	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A36Y670	158-0014-00			XTAL UNIT,QTZ:1MHZ,+/-0.005%	13454	158-0014-00
A37	670-8808-00			CIRCUIT BD ASSY:3V PWR SPLY (P6464 ONLY)	80009	670-8808-00
A37C100	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A37C110	290-0135-00			CAP,FXD,ELCTLT:15UF,20%,20V	05397	T110B156M020AS
A37C112	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A37C114	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A37C116	290-0135-00			CAP,FXD,ELCTLT:15UF,20%,20V	05397	T110B156M020AS
A37CR200	152-0581-00			SEMICOND DVC,DI:RECT,SI,20V,1A,A59	04713	1N5817
A37J210	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A37L100	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A37L200	108-0109-00			COIL,RF:FIXED,63UH	80009	108-0109-00
A37Q200	151-0736-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0736-00
A37R210	315-0910-00			RES,FXD,FILM:91 OHM,5%,0.25W	19701	5043CX91R00J
A37R212	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W	19701	5043CX200K0J
A37R214	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A37R216	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A37R218	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A37U210	156-1126-01			MICROCKT,LINEAR:VOLTAGE COMPARATOR,SELECTED	01295	LM311JG4
H340	165-2051-00			MICROCKT,DGTL:DESKEW IC HYBRID (P6464 ONLY)	80009	165-2051-00
J100	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J200	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J206	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J300	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J306	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J400	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J406	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J500	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J506	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10
J600	165-2048-10			MICROCKT,LINEAR:LET 2048 W/INSUL SLVG (P6464 ONLY)	80009	165-2048-10

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.

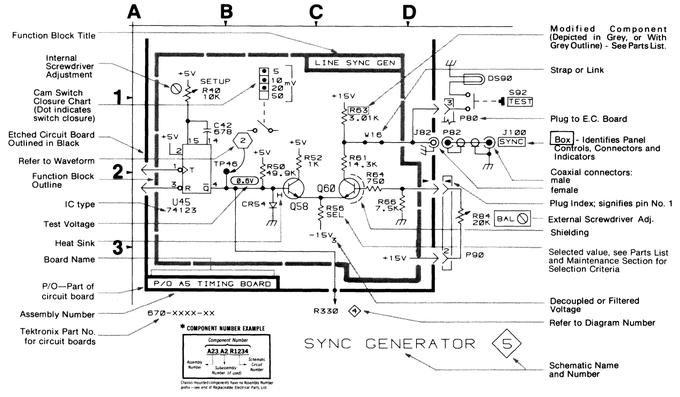


Table 11-1

IC PIN INFORMATION

Device Type	V_{CC} or V_{DD}	GND
10H101	1,16	8
10H102	1,16	8
10103	1,16	8
10104(H)	1,16	8
10H105	1,16	8
10H107	1,16	8
10113	1,16	8
10H116	1,16	8
10115	1,16	8
10131(H)	1,16	8
10134	1,16	8
10136	1,16	8
10158(H)	16	8
10H161	1,16	8
10H164	1,16	8
10174	1,16	8
10176	1,16	8
10188	1,16	8
10209	1,16	8
10231	1,16	8
10474-8	1,24	12
10474-15	1,24	12
100151	6,7	18
100164	6,7	18
74F02	14	7
74HC04	14	7
74HC125	14	7
74HC138	16	8
74LS139	16	8
74HC154	24	12
74HC174	16	8
74LS175	16	8
74HC245(LS)	20	10
74HC374	20	10
AN6913	+6V 1,9	5
F10016	1,16	8
LF412	+12V 8	-12V 4
MBM27C256-30	28	14
MC10H016L	1,16	8
NE5018	+12V 19	-12V 17
uPC339C	+6V 3	12
uPC393	8	4

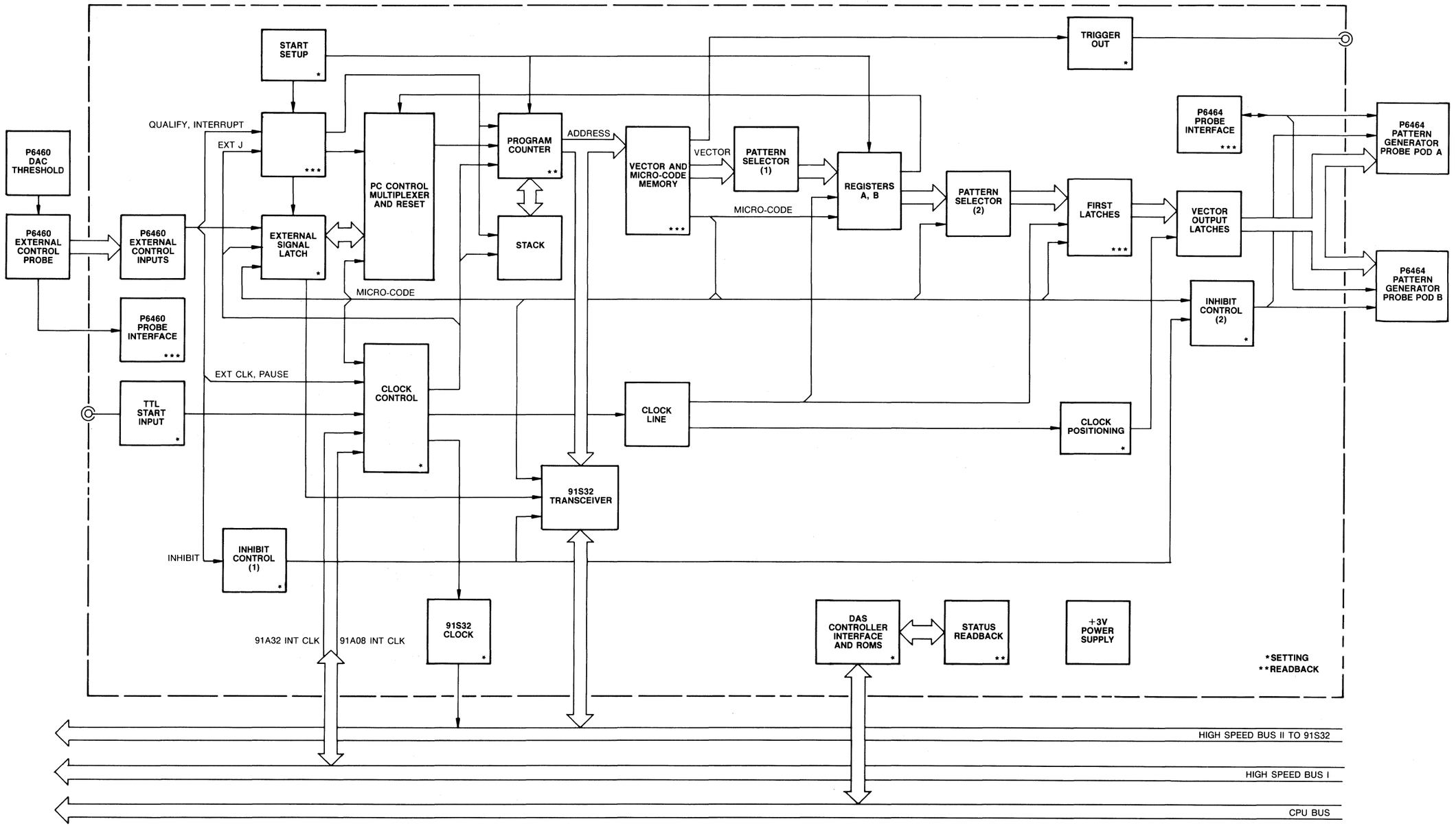


Figure 11-1. 91S16 Block Diagram.

5397-62

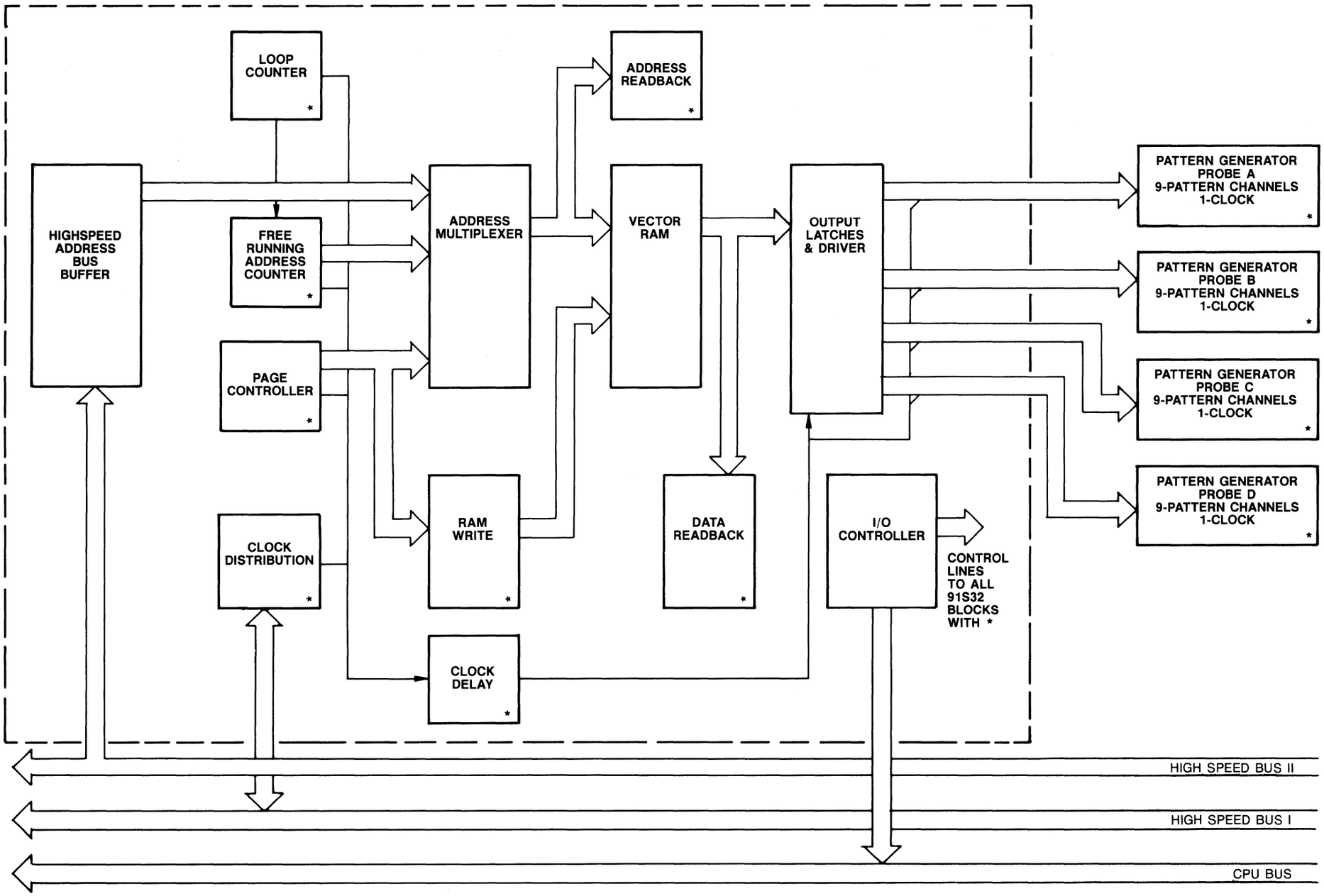


Figure 11-2. 91S32 Block Diagram.

5397-63

A34 91S16 PAT. GEN. BD.
& COMPONENT LOCATIONS

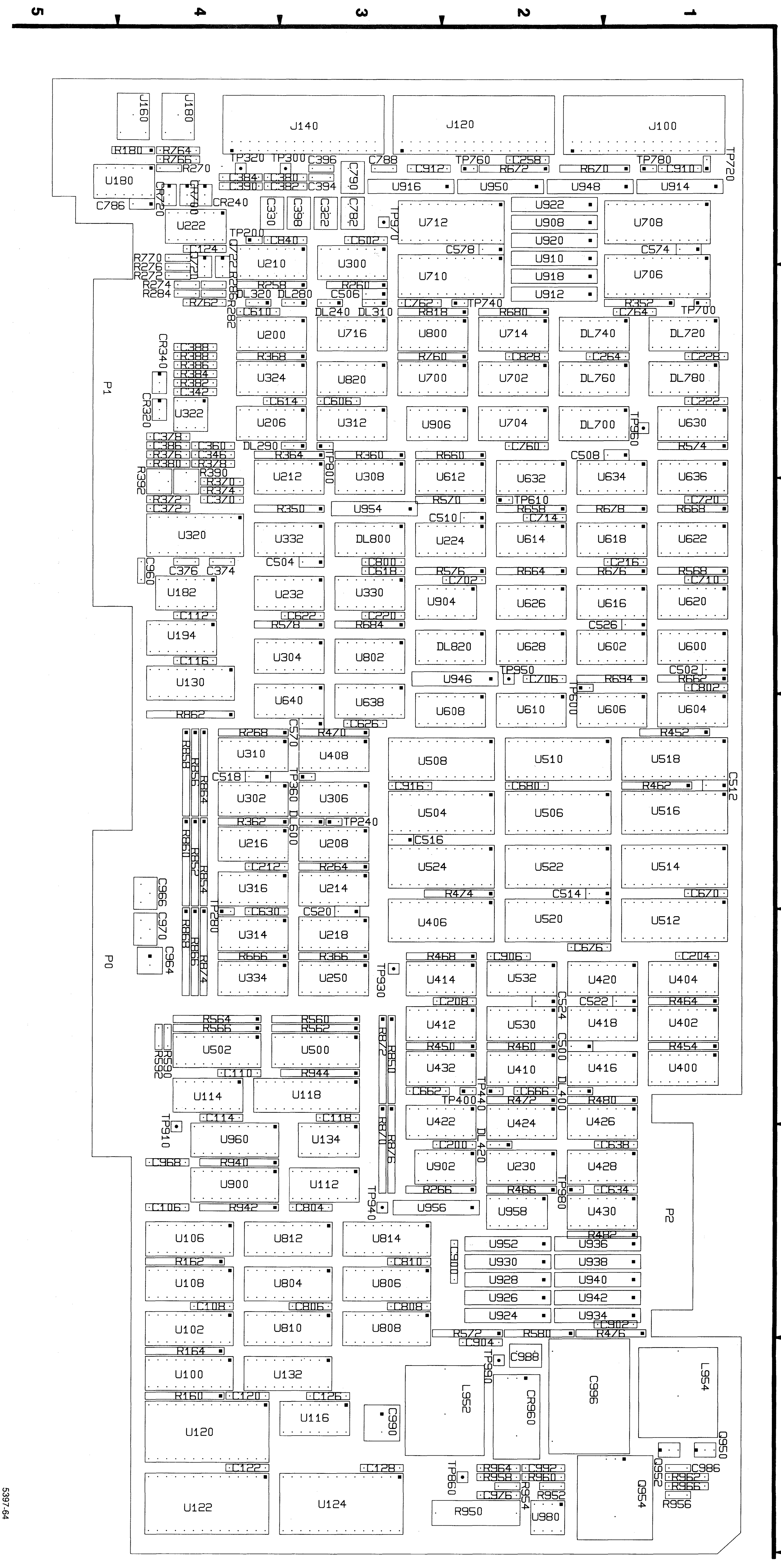


Figure 11-3. A34 91S16 Pattern Generator Board & Component Locations.

5397-64

Table 11-2

PROCESSOR INTERFACE & PROBE INTERFACE CKT. (92) — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J100	D1	A1	R850B	C1	E3
J100	A5	A1	R850C	C1	E3
J100	F5	A1	R852A	E4	D4
J120	A5	A2	R852B	E4	D4
J120	D2	A2	U100	A1	G4
J120	F5	A2	U102	A2	F4
J140	A5	A3	U106	A4	F4
J140	D2	A3	U108	C3	F4
J140	F5	A3	U112	B1	F3
R160	B1	G4	U114	B3	E4
R162	B4	F4	U116	F1	G3
R164A	B2	G4	U118	E3	E3
R164B	B2	G4	U120	F1	G4
R164C	B2	G4	U122	F2	G4
R164D	B2	G4	U124	F2	G3
R164E	B2	G4	U130	E5	C4
R164F	B2	G4	U132	C5	G3
R164G	B2	G4	U134A	C1	F3
R164H	B2	G4	U180A	C2	A4
R180B	A5	A4	U180B	C5	A4
R180C	A5	A4	U182	C5	C4
R180D	A5	A4	U194	B5	C4
R850A	C1	E3			

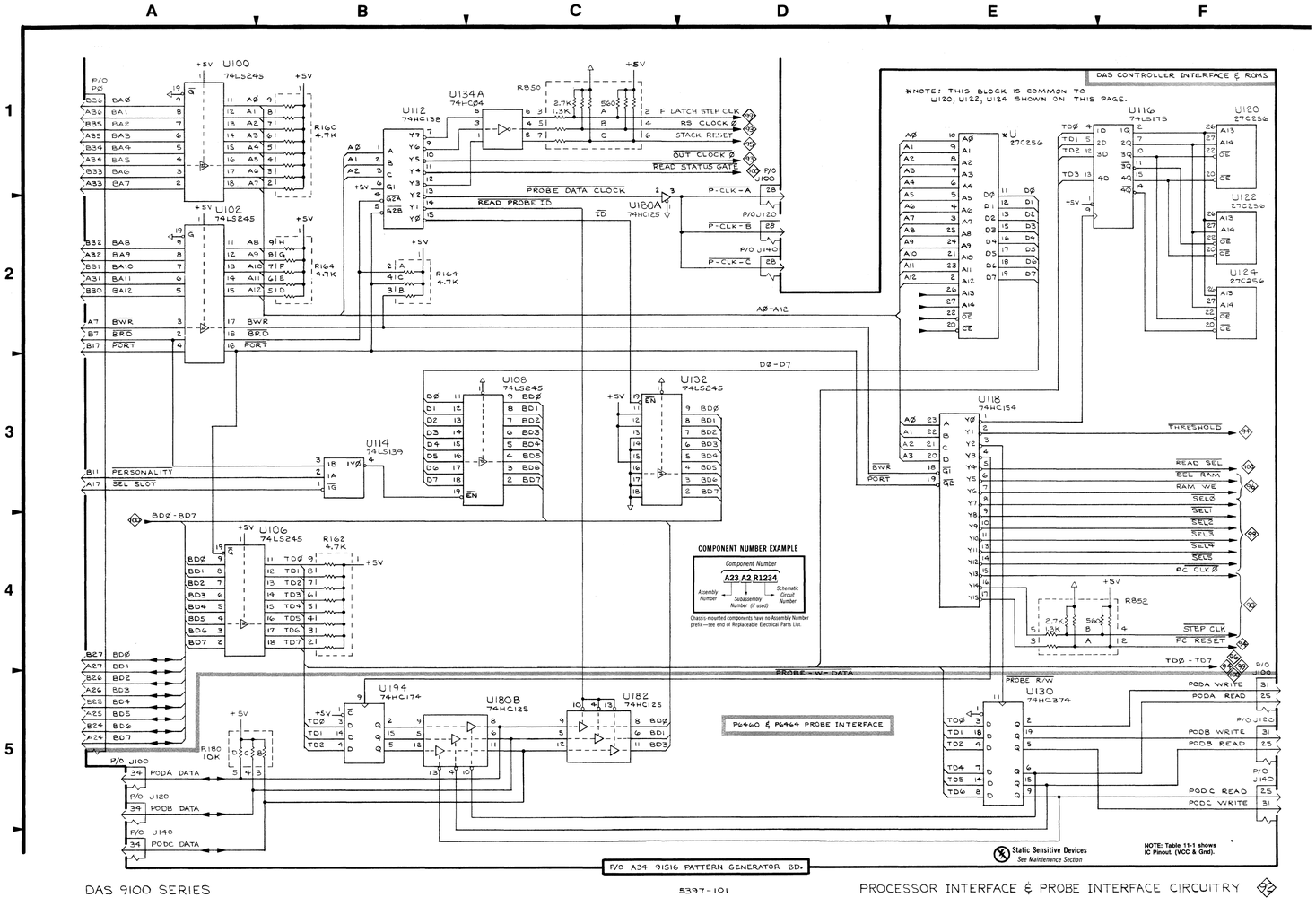


Table 11-3

CLOCK CONTROL CIRCUITRY (93) — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
CR240	B1	A4	R470D	D3	D3
DL240	E5	B3	R470E	B3	D3
DL280	B2	B3	R472B	F4	E2
DL290	E5	B3	R474D	F5	D2
J140	A4	A3	R572F	E2	F2
J140	A2	A3	R666A	D3	E4
J160	A1	A4	R666B	E3	E4
P1	A3	B4	R666D	E4	E4
P1	A4	B4	R818D	D1	B2
P1	A2	B4	R850D	E5	E3
P2	F4	F1	R852C	E5	D4
R180A	B1	A4	TP200	A4	A4
R258A	A3	B3	TP240	C1	D3
R258D	A4	B3	TP280	F4	E4
R258E	D5	B3	TP980	F4	F2
R260B	D5	B3	U134E	D5	F3
R260C	A2	B3	U134F	D5	F3
R260F	A3	B3	U200B	B2	B3
R264A	C3	D3	U200C	E5	B3
R264B	D4	D3	U206	B3	B3
R264C	C3	D3	U208A	C3	D3
R264D	C4	D3	U208B	C4	D3
R264E	C4	D3	U210A	A4	B3
R264F	D4	D3	U210B	A3	B3
R264G	F4	D3	U212A	C1	C3
R266A	F1	F2	U212B	F5	C3
R270	A1	A4	U214A	D3	D3
R272	B1	B4	U214B	D4	D3
R274	B1	B4	U216A	F1	D4
R276	B1	B4	U216B	C3	D4
R282	B2	B4	U218	E4	E3
R284	B2	B4	U222A	B1	A4
R286	B2	B4	U222D	B2	A4
R350E	F5	C3	U230B	F4	F2
R350F	E5	C3	U230C	F4	F2
R360D	D1	B3	U250A	E3	E3
R360E	B2	B3	U250B	E3	E3
R362C	E1	D4	U300C	D5	B3
R364A	C2	B3	U300D	A2	B3
R364B	B4	B3	U302A	C2	D4
R364C	B4	B3	U302B	C2	D4
R364D	B3	B3	U316B	E1	D4
R364E	D2	B3	U422D	E4	E2
R364F	C1	B3	U638B	C2	D3
R366A	D3	E3	U640C	C3	D3
R366B	C3	E3	U704B	C1	B2
R366D	D3	E3	U716A	D1	B3
R368E	B2	B4	U820C	C3	B3
R368F	E5	B4	U954B	E1	C3
R450C	E3	E2	U956A	F2	F2
R460C	F4	E2	U956B	E2	F2
R460D	F4	E2			

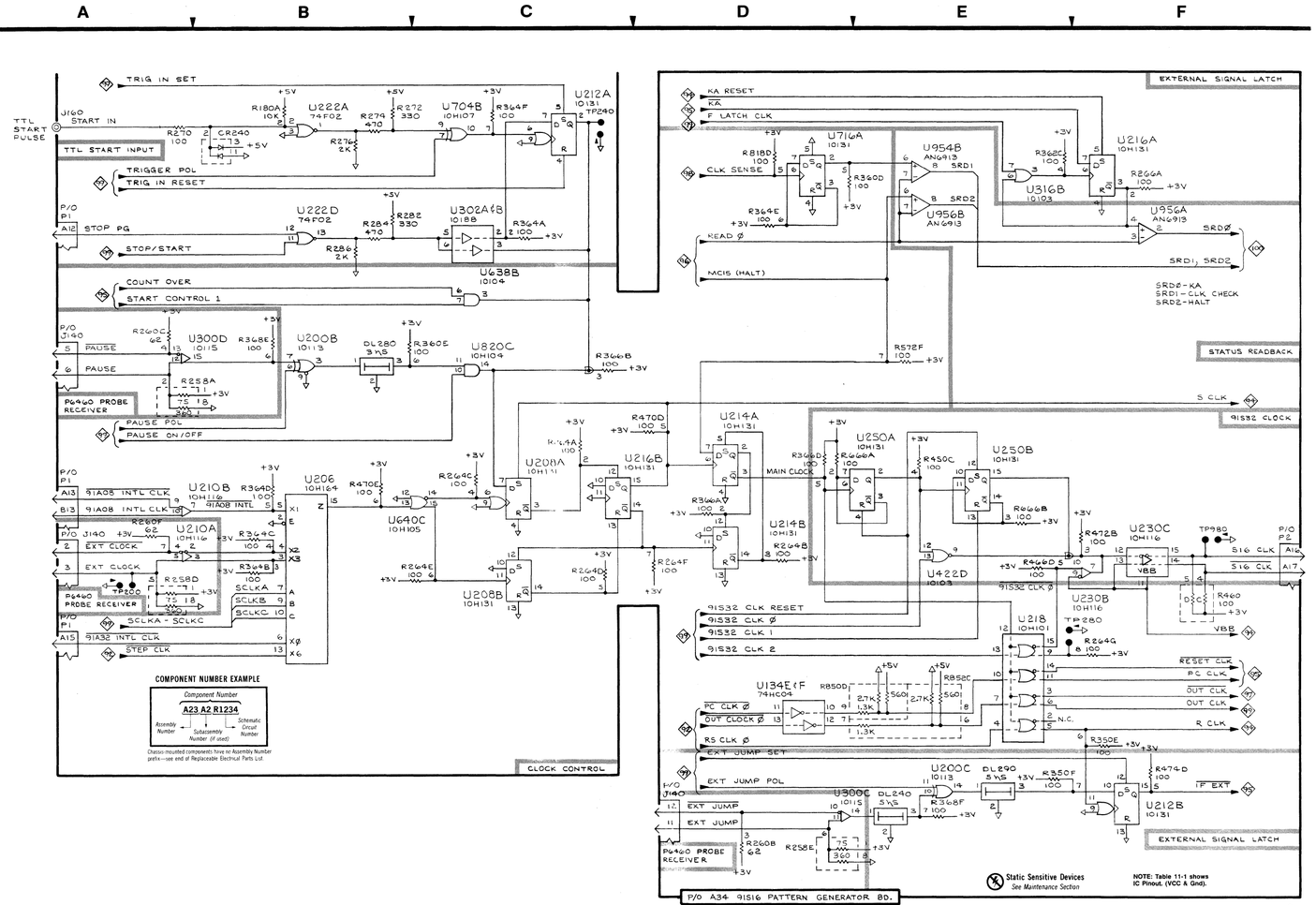
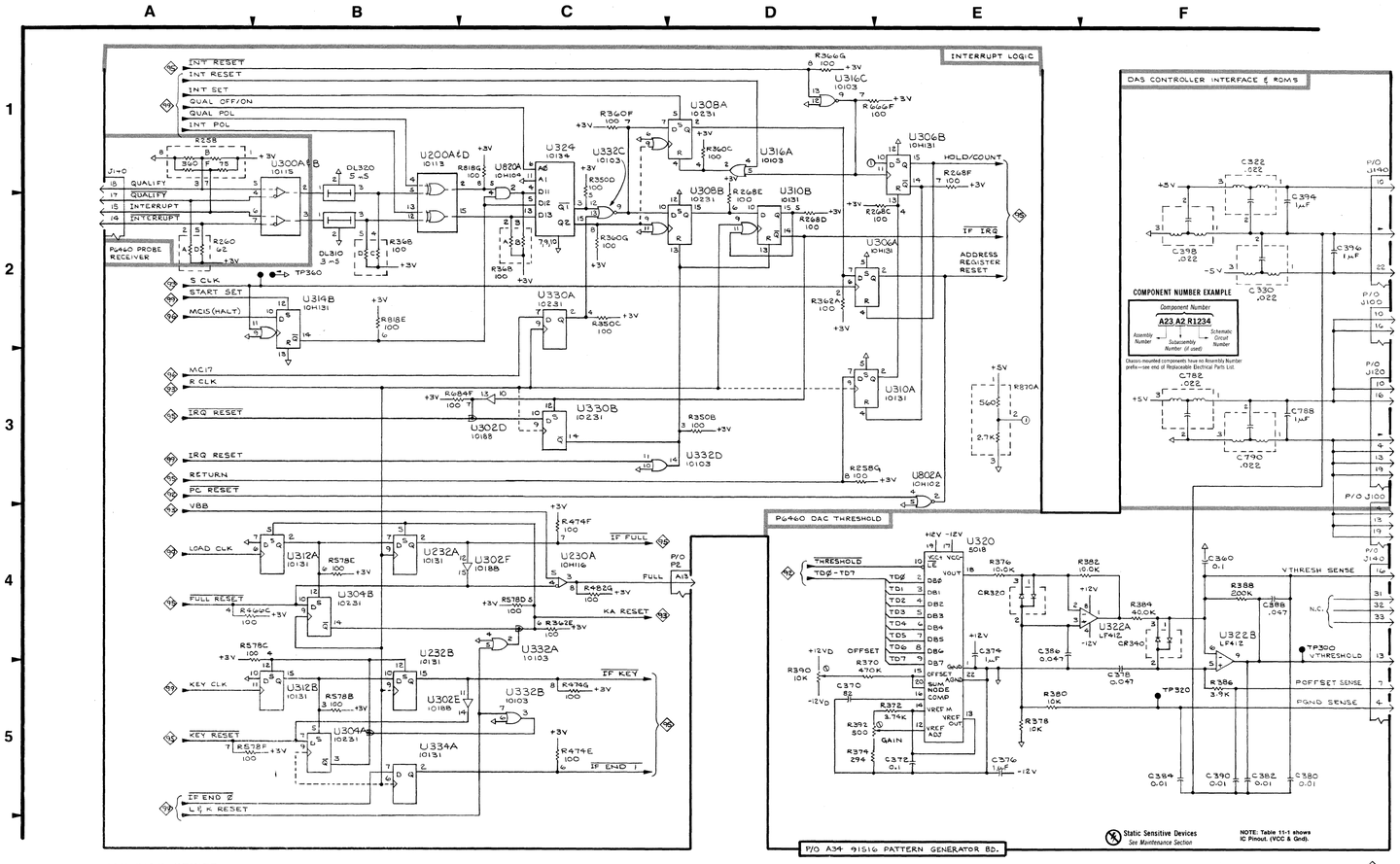


Table 11-4

EXTERNAL SIGNAL CNTL. AND DAC THRESHOLD 94 — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C322	F2	A3	R384	F4	B4
C330	F2	A3	R386	F5	B4
C360	F4	B4	R388	F4	B4
C370	D5	C4	R390	D5	C4
C372	E5	C4	R392	D5	C4
C374	E4	C4	R466C	B4	F2
C376	E5	C4	R474E	C5	D2
C378	F5	B4	R474F	C4	D2
C380	F5	A3	R474G	C5	D2
C382	F5	A3	R482G	C4	F1
C384	F5	A4	R578B	B5	C3
C386	E4	B4	R578C	B4	C3
C388	F4	B4	R578D	C4	C3
C390	F5	A4	R578E	B4	C3
C394	F2	A3	R666F	D1	E4
C396	F2	A3	R684F	C3	C3
C398	F2	A3	R818E	B2	B2
C782	F3	A3	R818G	C1	B2
C788	F3	A3	R870A	E3	F3
C790	F3	A3	TP300	F4	A3
CR320	E4	B4	TP320	F5	A4
CR340	F4	B4	TP360	B2	D3
DL310	B2	B3	U200A	B1	B3
DL320	B1	B4	U200D	B1	B3
J100	F3	A1	U230A	C4	F2
J120	F3	A2	U232A	B4	C3
J140	F2	A3	U232B	B5	C3
J140	A1	A3	U300A	B1	B3
J140	F4	A3	U300B	B1	B3
R258B	A1	B3	U302D	C3	D4
R258F	A1	B3	U302E	C5	D4
R258G	D3	B3	U302F	C4	D4
R260A	A2	B3	U304A	B5	C3
R260D	A2	B3	U304B	B4	C3
R268C	E2	D4	U306A	D2	D3
R268D	D2	D4	U306B	E1	D3
R268E	D2	D4	U308A	D1	C3
R268F	E1	D4	U308B	D2	C3
R350B	D3	C3	U310A	D3	D4
R350C	C2	C3	U310B	D2	D4
R350D	C1	C3	U312A	B4	B3
R360C	D1	B3	U312B	B5	B3
R360F	C1	B3	U314B	B2	E4
R360G	C2	B3	U316A	D1	D4
R362A	D2	D4	U316C	D1	D4
R362E	C4	D4	U320	E4	C4
R366G	D1	E3	U322A	F4	B4
R368A	C2	B4	U322B	F4	B4
R368B	C2	B4	U324	C1	B3
R368C	B2	B4	U330A	C2	C3
R368D	B2	B4	U330B	C3	C3
R370	D5	C4	U332A	C4	C3
R372	E5	C4	U332B	C5	C3
R374	D5	C4	U332C	C2	C3
R376	E4	B4	U332D	C3	C3
R378	E5	B4	U334A	B5	E4
R380	E5	B4	U802A	E3	C3
R382	F4	B4	U820A	C1	B3



DAS 9100 SERIES

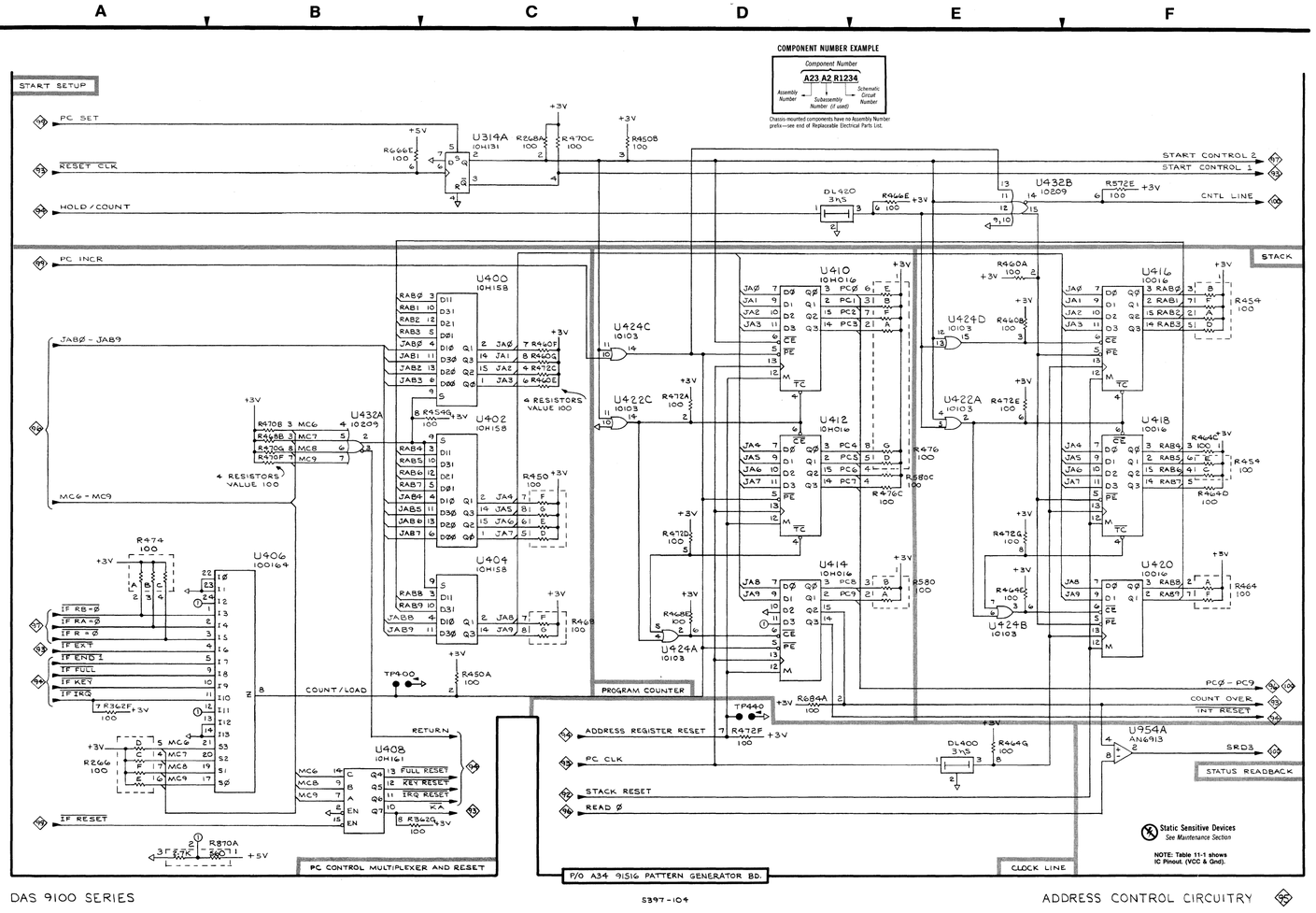
8397-103

EXTERNAL SIGNAL CONTROL & DAC THRESHOLD 94

Table 11-5

ADDESS CONTROL CIRCUITRY (95) — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL400	E5	E2	R472D	D4	E2
DL420	D2	F2	R472E	E3	E2
R266C	A5	F2	R472F	D5	E2
R266D	A5	F2	R472G	E4	E2
R266E	A5	F2	R474A	A4	D2
R266F	A5	F2	R474B	A4	D2
R288A	C1	D4	R474C	A4	D2
R362F	A5	D4	R476A	E2	F1
R362G	B5	D4	R476B	E2	F1
R366G	D5	E3	R476C	E3	F1
R450A	C4	E2	R476D	E3	F1
R450B	C1	E2	R476E	E2	F1
R450D	C3	E2	R476F	E2	F1
R450E	C3	E2	R476G	E3	F1
R450F	C3	E2	R572E	F1	F2
R450G	C3	E2	R580A	E4	F2
R454A	F2	E1	R580B	E4	F2
R454B	F2	E1	R580C	E3	F2
R454C	F3	E1	R666E	B1	E4
R454D	F2	E1	R684A	D1	C3
R454E	F3	E1	R870A	A5	F3
R454F	F2	E1	TP400	B5	E2
R454G	C3	E1	TP440	D5	E2
R460A	E2	E2	U314A	C1	E4
R460B	E2	E2	U400	C2	E1
R460E	C3	E2	U402	C3	E1
R460F	C2	E2	U404	C4	E1
R460G	C2	E2	U406	B4	E2
R464A	F4	E1	U408	B5	D3
R464C	F3	E1	U410	D2	E2
R464D	F3	E1	U412	D3	E2
R464E	E4	E1	U414	D4	E2
R464F	F4	E1	U416	F2	E1
R464G	E5	E1	U418	F3	E1
R466E	E2	F2	U420	F4	E1
R468B	B3	E2	U422A	E3	E2
R468E	D4	E2	U422C	C3	E2
R468F	C4	E2	U424A	D4	E2
R468G	C4	E2	U424B	E4	E2
R470B	B3	D3	U424C	C2	E2
R470C	C1	D3	U424D	E2	E2
R470F	B3	D3	U432A	B3	E2
R470G	B3	D3	U432B	E2	E2
R472A	D3	E2	U954A	F5	C3
R472C	C3	E2			



DAS 9100 SERIES

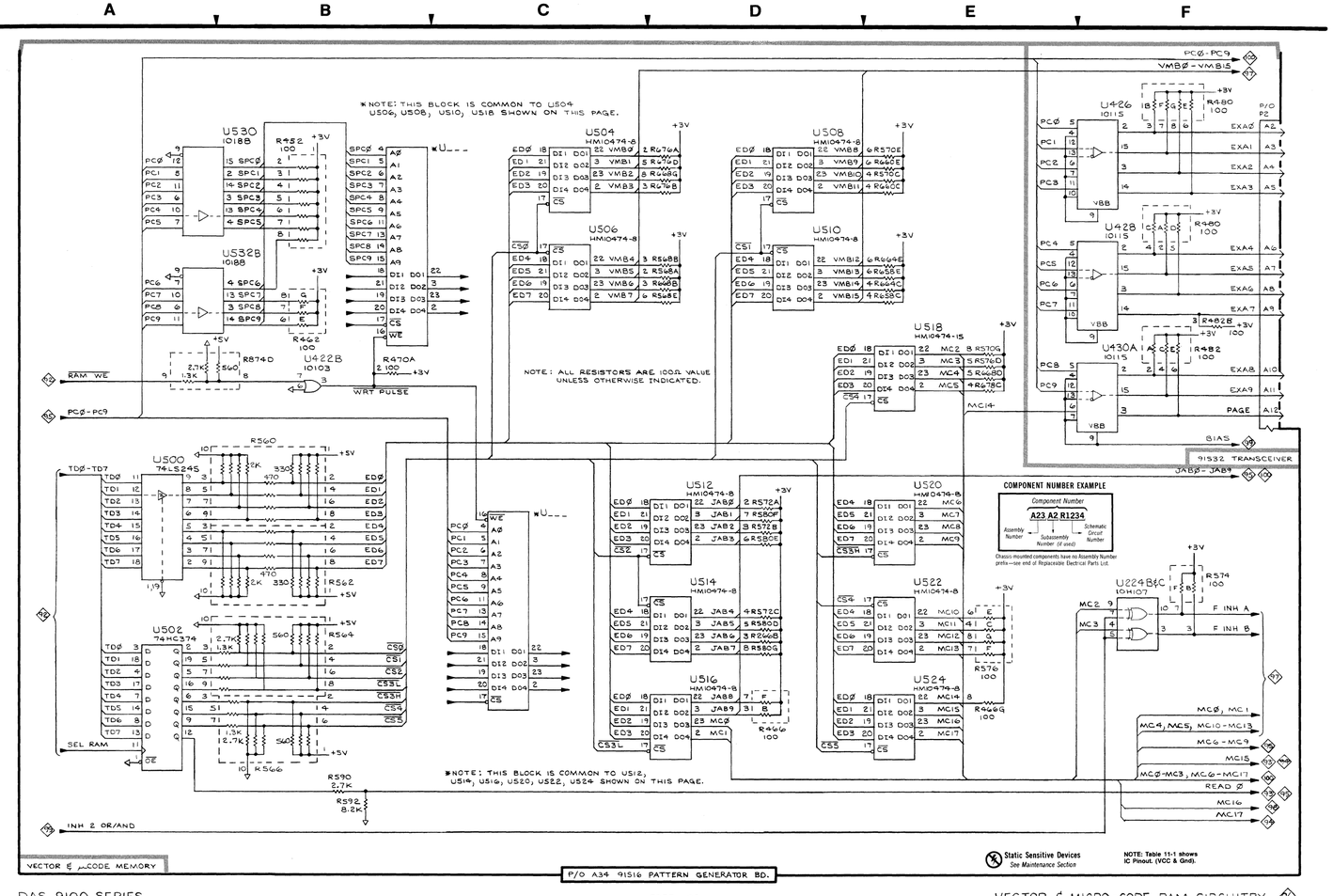
5397-104

ADDRESS CONTROL CIRCUITRY (95)

Table 11-6

VECTOR & MICRO-CODE RAM CKT. (96) — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
P2	F1	F1	R580D	D4	F2
R266B	D4	F2	R580E	D4	F2
R452	B1	D1	R580F	D3	F2
R462E	B2	D1	R580G	D4	F2
R462F	B2	D1	R590	B5	E4
R462G	B2	D1	R592	B5	E4
R466B	D5	F2	R658C	E2	C2
R466F	D5	F2	R658E	E2	C2
R466G	E5	F2	R660C	E1	B2
R470A	B3	D3	R660E	E1	B2
R480A	F2	E1	R664C	E2	C2
R480B	F1	E1	R664E	E2	C2
R480C	F2	E1	R668B	D2	C1
R480D	F2	E1	R668D	E3	C1
R480E	F1	E1	R668G	D1	C1
R480F	F1	E1	R676A	D1	C1
R480G	F1	E1	R676B	D1	C1
R482A	F2	F1	R676D	D1	C1
R482B	F2	F1	R678C	E3	C1
R482C	F2	F1	R874D	A3	E4
R482E	F2	F1	U224B	F4	C2
R560	B3	E3	U224C	F4	C2
R562	B4	E3	U422B	B3	E2
R564	B4	E4	U426	F1	E1
R566	B5	E4	U428	F2	F1
R568A	D2	C1	U430	F3	F1
R568B	D2	C1	U500	A3	E3
R568E	D2	C1	U502	A4	E4
R570C	E1	C2	U504	C1	D2
R570E	E1	C2	U506	C2	D2
R570G	E3	C2	U508	D1	D2
R572A	D3	F2	U510	D2	D2
R572B	D4	F2	U512	D3	E1
R572C	D4	F2	U514	D4	D1
R574B	F4	B1	U516	D5	D1
R574F	F4	B1	U518	E3	D1
R576C	E4	C2	U520	E3	E2
R576D	E3	C2	U522	E4	D2
R576E	E4	C2	U524	E5	D2
R576F	E4	C2	U530	A1	E2
R576G	E4	C2	U532B	A2	E2



DAS 9100 SERIES

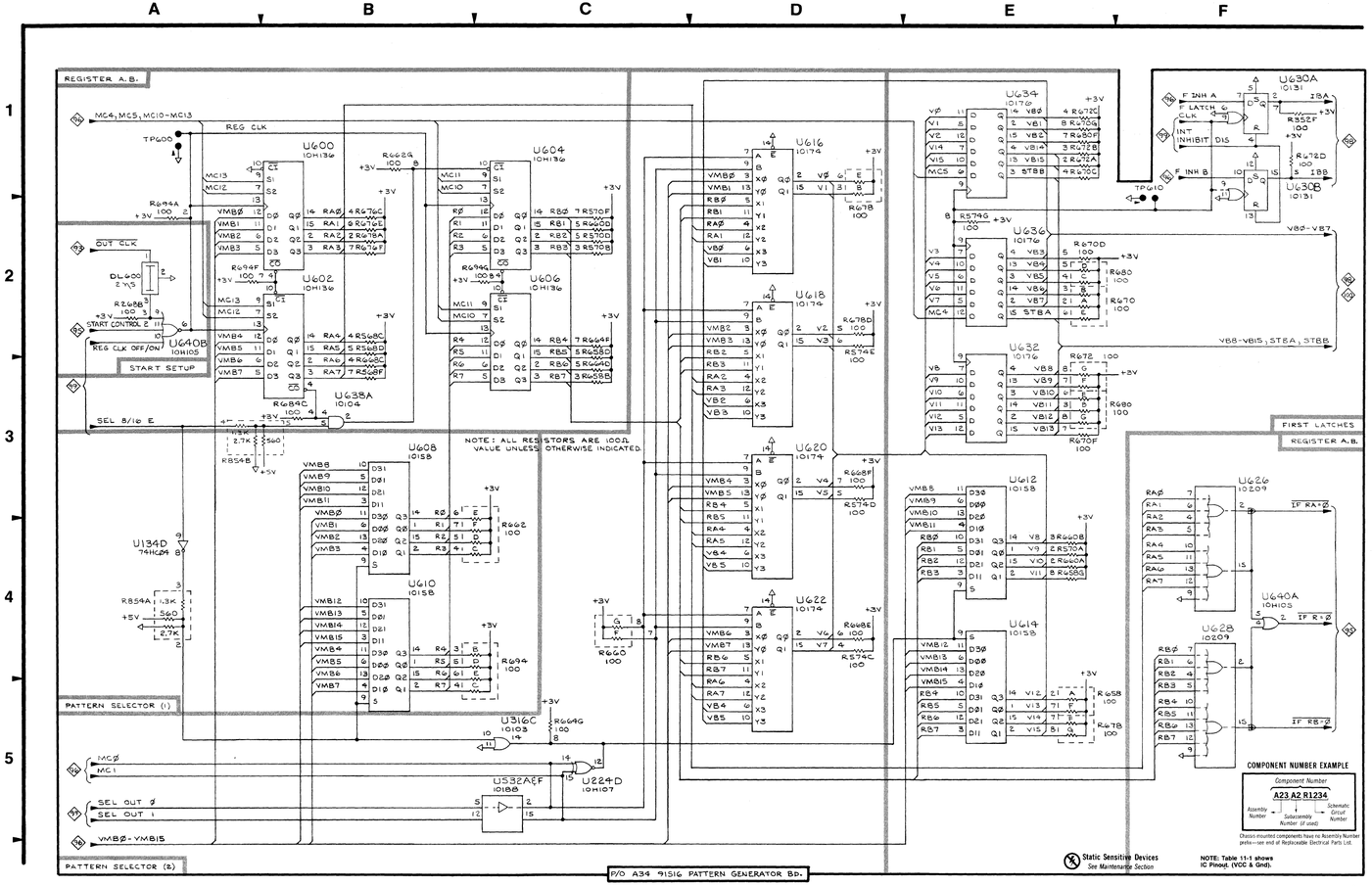
5397-105

VECTOR & MICRO-CODE RAM CIRCUITRY (96)

Table 11-7

REGISTER & OUTPUT CNTL. CKT. (97) — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL600	A2	D3	R678A	B2	C1
R268B	A2	D4	R678B	D1	C1
R352F	F1	B1	R678D	D2	C1
R568C	B2	C1	R678E	D1	C1
R568D	B2	C1	R678F	E5	C1
R568F	B3	C1	R678G	E5	C1
R570A	E4	C2	R680B	E3	B2
R570B	C2	C2	R680C	E2	B2
R570D	C2	C2	R680D	E2	B2
R570F	C2	C2	R680E	E3	B2
R574C	D5	B1	R680F	E1	B2
R574D	D3	B1	R680G	E3	B2
R574E	D2	B1	R684C	B3	C3
R574G	E2	B1	R694A	A2	C1
R658A	E5	C2	R694B	C4	C1
R658B	C3	C2	R694C	C4	C1
R658D	C2	C2	R694D	C4	C1
R658F	E5	C2	R694E	C4	C1
R658G	E4	C2	R694F	A2	C1
R660A	E4	B2	R694G	C2	C1
R660B	E4	B2	R854A	A4	D4
R660D	C2	B2	R854B	A3	D4
R660F	C4	B2	TP600	A1	C2
R660G	C4	B2	TP610	F1	C2
R662C	C4	C1	U134D	A4	F3
R662D	C4	C1	U224D	C5	C2
R662E	C4	C1	U316C	C5	D4
R662F	C4	C1	U532A	C5	E2
R662G	B1	C1	U532H	C5	E2
R664D	C3	C2	U600	B1	C1
R664F	C2	C2	U602	B2	C1
R664G	C5	C2	U604	C1	D1
R668C	B3	C1	U606	C2	D1
R668E	D5	C1	U608	B3	D2
R668F	D3	C1	U610	B4	D2
R670A	E2	A2	U612	E3	C2
R670B	E2	A2	U614	E4	C2
R670C	E1	A2	U616	D2	C1
R670D	E2	A2	U618	D1	C1
R670E	E2	A2	U620	D3	C1
R670F	E3	A2	U622	D5	C1
R670G	E1	A2	U626	F3	C2
R672A	E1	A2	U628	F4	C2
R672B	E1	A2	U630A	F1	B1
R672C	E1	A2	U630B	F1	B1
R672D	F1	A2	U632	E3	C2
R672F	E3	A2	U634	E1	B1
R672G	E3	A2	U636	E2	B1
R676C	B2	C1	U638A	B3	D3
R676E	B2	C1	U640A	F4	D3
R676F	B2	C1	U640B	A2	D3



DAS 9100 SERIES

5397-106

REGISTER & OUTPUT CONTROL CIRCUITRY (97)

Table 11-8

+3V POWER SUPPLY, OUTPUT DATA & CLOCK CONTROL (98) — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C106	B3	F4	C680	B3	D2	Q952	A2	G1
C108	B3	F4	C702	B3	C2	Q954	B2	G1
C110	B3	E4	C706	B3	C2	R352A	E2	B1
C112	B3	C4	C710	B3	C1	R360B	B5	B3
C114	B3	E4	C714	B3	C2	R368G	B5	B4
C116	B3	C4	C720	B3	C1	R760C	C2	B2
C118	B3	E3	C760	B3	B2	R760D	E1	B2
C120	B3	G4	C762	B3	B3	R760E	D2	B2
C122	B3	G4	C764	B3	B1	R760F	D2	B2
C124	B3	A4	C786	B4	A4	R760G	E5	B2
C126	B3	G3	C800	A2	C3	R762	B5	B4
C128	B3	G3	C802	B3	C1	R764	C5	A4
C200	B1	F2	C804	B3	F3	R766	C5	A4
C204	B1	E1	C806	B3	F3	R770	B5	B4
C208	B1	E2	C808	B3	F3	R818B	E4	B2
C212	B1	D4	C810	B3	F3	R950	B2	G2
C216	B1	C1	C828	B3	B2	R952	A1	G2
C220	B1	C3	C840	B3	A3	R954	A2	G2
C222	B1	B1	C900	A2	F2	R956	A2	G1
C228	B1	B1	C902	A2	F1	R958	A2	G2
C258	A1	A2	C904	B3	G2	R960	A2	G2
C264	B1	B1	C906	B3	E2	R962	B2	G1
C342	A4	B4	C910	A2	A1	R964	A2	G2
C346	A4	B4	C912	A2	A3	R966	B2	G1
C500	A1	E2	C916	B3	D3	TP700	E2	B1
C502	A1	C1	C960	A3	C4	TP720	E1	A1
C504	A1	C3	C964	B4	E4	TP740	E4	B2
C506	A1	B3	C966	A4	D4	TP760	E5	A2
C508	A1	B1	C968	B3	F4	TP780	F1	A1
C510	B3	C2	C970	A4	E4	TP860	A4	G2
C512	B4	D1	C976	A2	G2	TP910	A4	F4
C514	B4	D2	C986	B2	G1	TP930	A3	E3
C516	B4	D3	C988	A1	G2	TP940	A3	F3
C518	B4	D4	C990	A1	G3	TP950	A3	C2
C520	B4	E3	C992	A1	G2	TP960	A3	B1
C522	B4	E1	C996	B1	G2	TP970	A3	A3
C524	B4	E2	CR700	C5	A4	TP990	A1	G2
C526	B4	C1	CR720	C5	A4	U222B	C5	A4
C570	A1	D3	CR960	B1	G2	U222C	C5	A4
C574	B4	A1	DL700	C3	B1	U700A	D2	B2
C578	B4	A2	DL720	E1	B1	U700C	C3	B2
C602	B3	A3	DL740	E5	B1	U702A	D4	B2
C606	B3	B3	DL760	D3	B1	U702C	D3	B2
C610	B3	B4	DL780	D3	B1	U704A	E2	B2
C614	B3	B3	J100	F1	A1	U704D	E4	B2
C618	B3	C3	J120	F4	A2	U706	F1	B1
C622	B3	C3	J180	F4	A4	U708	F2	A1
C626	B3	D3	L952	B1	G2	U710	F3	B2
C630	B3	E4	L954	B1	G1	U712	F4	A2
C634	B3	F1	P0	A4	E4	U714A	E1	B2
C638	B3	F1	P1	A3	B4	U714B	E5	B2
C662	B3	E4	P2	A5	F1	U714C	E5	B2
C666	B3	E2	Q720	B5	B4	U716B	B5	B3
C670	B3	D1	Q722	B5	B4	U980A	A2	G2
C676	B3	E2	Q950	A2	G1	U980B	A2	G2

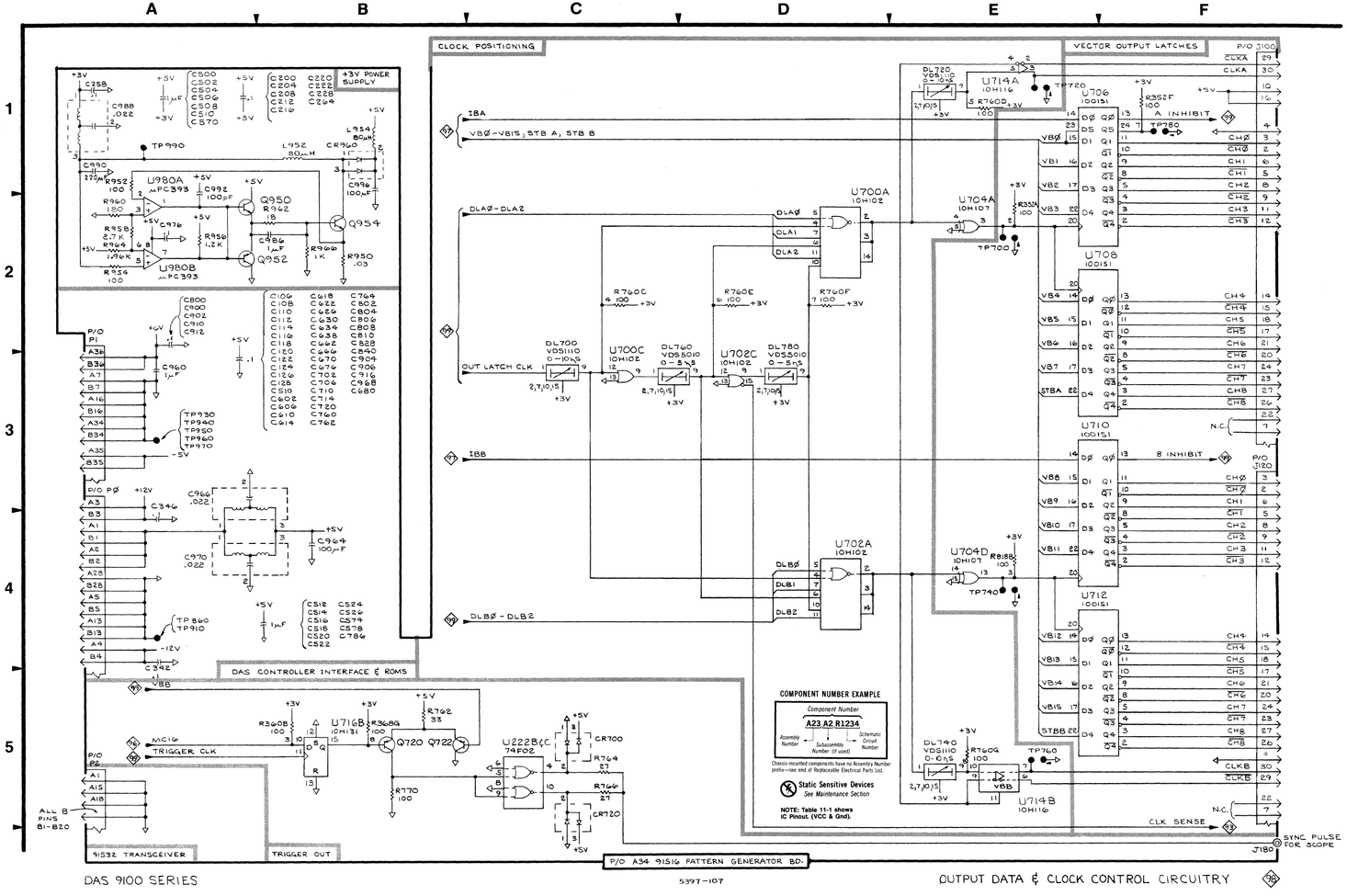


Table 11-9

CLOCK & SETTING CONTROL 99 — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL800	D1	C3	R868	D5	E4
DL820	C1	C2	R870	F3	F3
J100	F2	A1	R872	F4	E3
J120	F2	A2	R874	F4	E4
J140	A2	A3	R876	F5	F3
P2	F2	F1	TP800	B2	B3
R258C	A2	B3	U210C	B2	B3
R260E	A2	B3	U302C	D1	D4
R364G	B2	B3	U430C	C2	F1
R466A	C2	F2	U800A	C2	B2
R666G	D1	E4	U800B	B2	B2
R672E	C2	A2	U800D	C2	B2
R684D	D1	C3	U802B	C1	C3
R684E	C1	C3	U802C	D1	C3
R760B	E1	B2	U802D	D1	C3
R818C	C2	B2	U804	A3	F3
R818F	B2	B2	U806	A5	F3
R854	D4	D4	U808	C3	F3
R856	B3	D4	U810	C5	F3
R858	B4	D4	U812	E3	F3
R860	B4	D4	U814	E5	F3
R862	B5	D4	U820B	B2	B3
R864	D3	D4	U820D	B2	B3
R866	D4	E4			

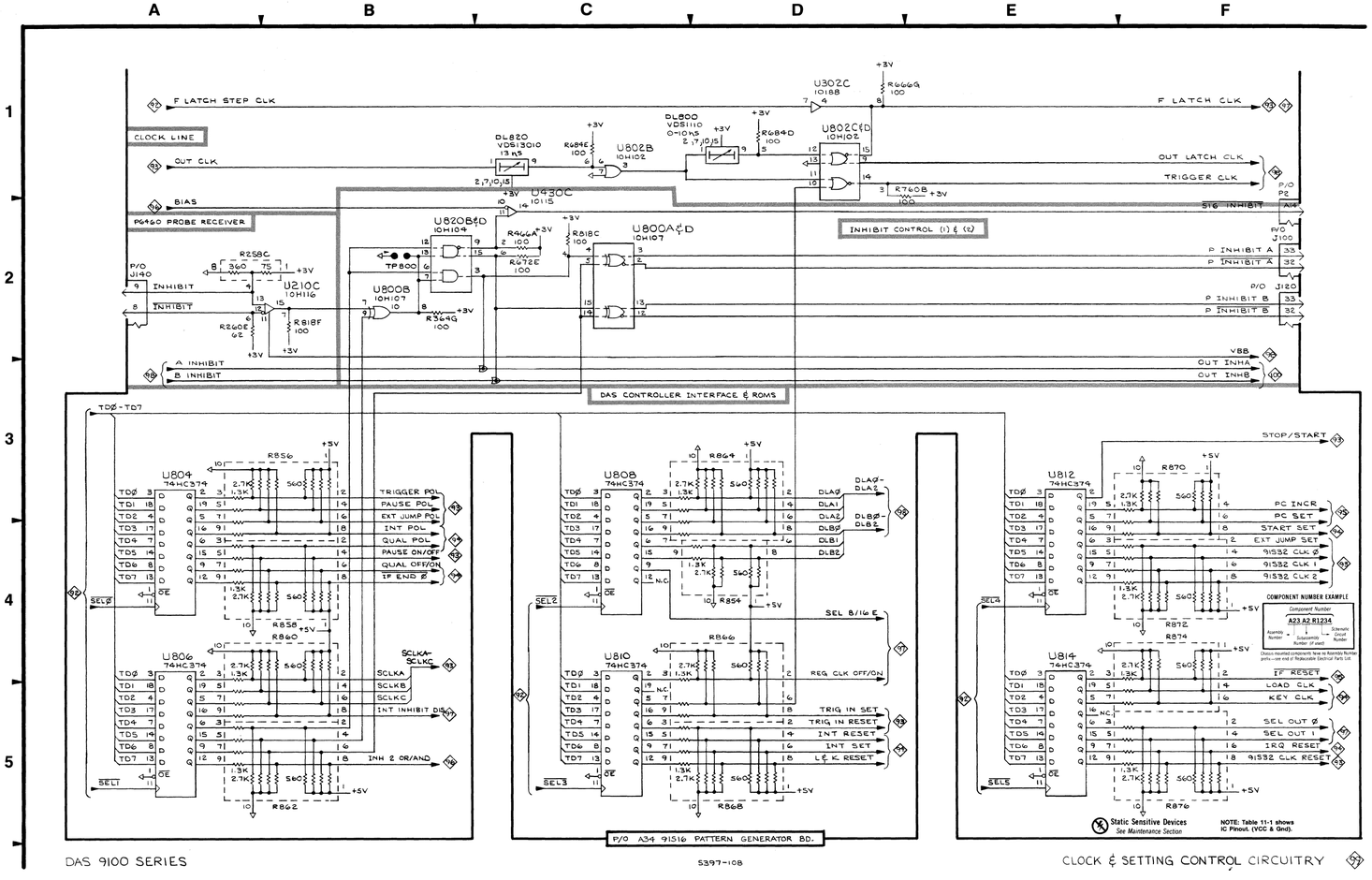
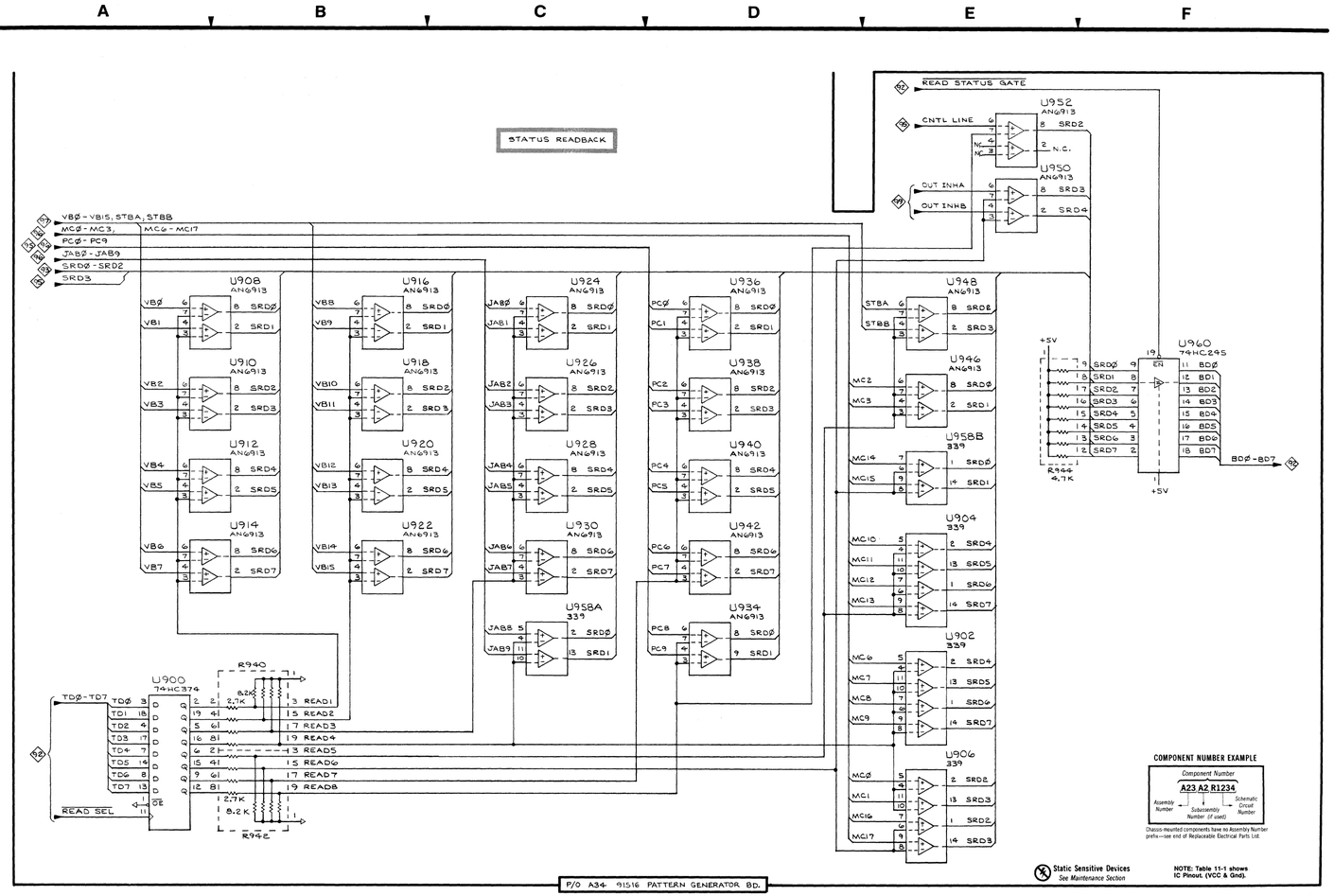


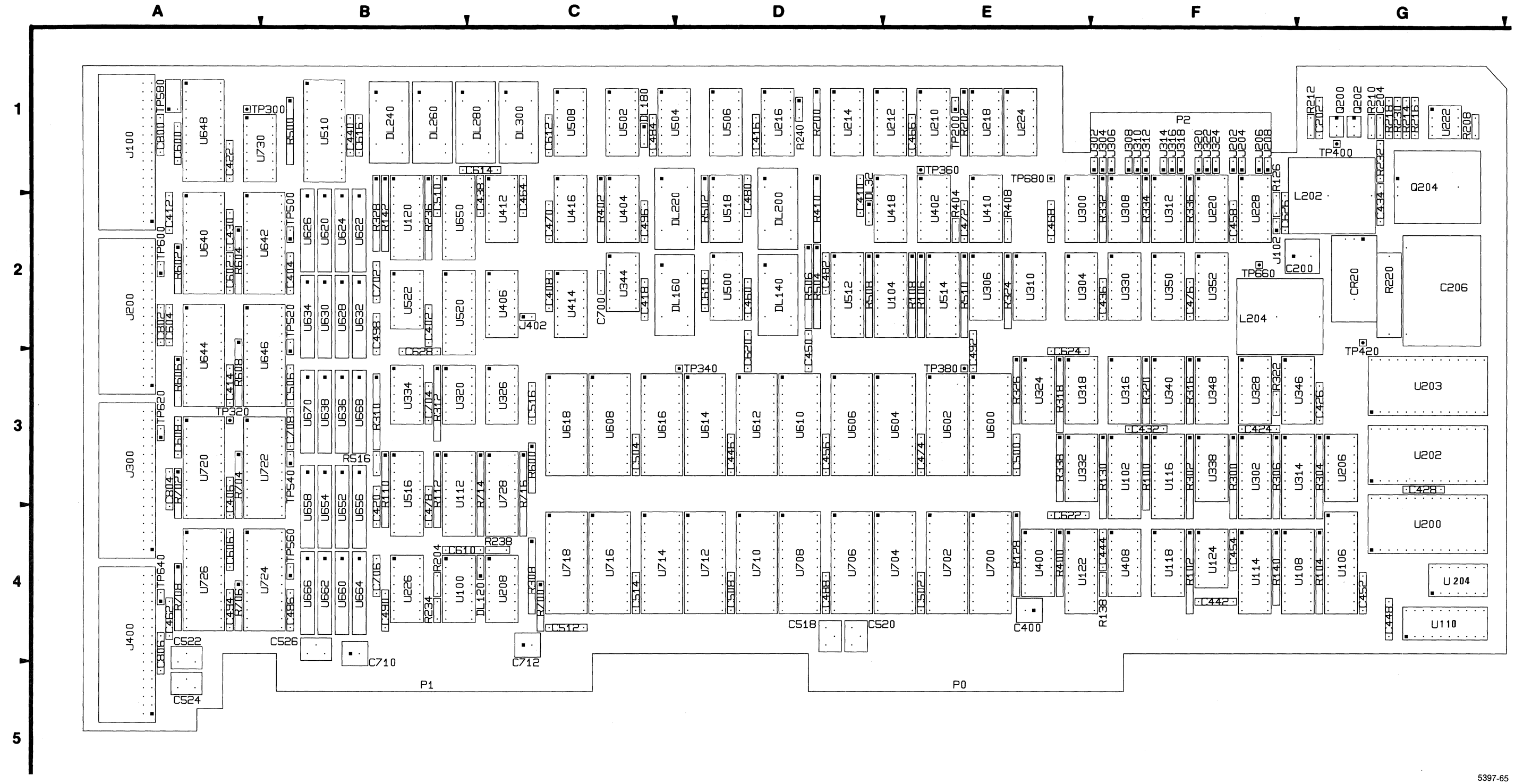
Table 11-10

READ STATUS CIRCUITRY ◇100◇ — 91S16 PAT. GEN. BD., ASSY. A34

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R940	B5	F4	U926	C3	F2
R942	B5	F4	U928	C3	F2
R944	F3	E3	U930	C4	F2
U900	A5	F4	U934	D4	F1
U902	E4	F2	U936	D2	F1
U904	E4	C2	U938	D3	F1
U906	E5	B2	U940	D3	F1
U908	B2	A2	U942	D4	F1
U910	B3	A2	U946	E3	C2
U912	B3	B2	U948	E2	A2
U914	B4	A1	U950	E1	A2
U916	B2	A3	U952	E1	F2
U918	B3	B2	U958A	C4	F2
U920	B3	A2	U958B	E3	F2
U922	B4	A2	U960	F3	F4
U924	C2	F2			



P/O A34 PAT. GEN. BD.
READ STATUS CIRC. ◇100◇



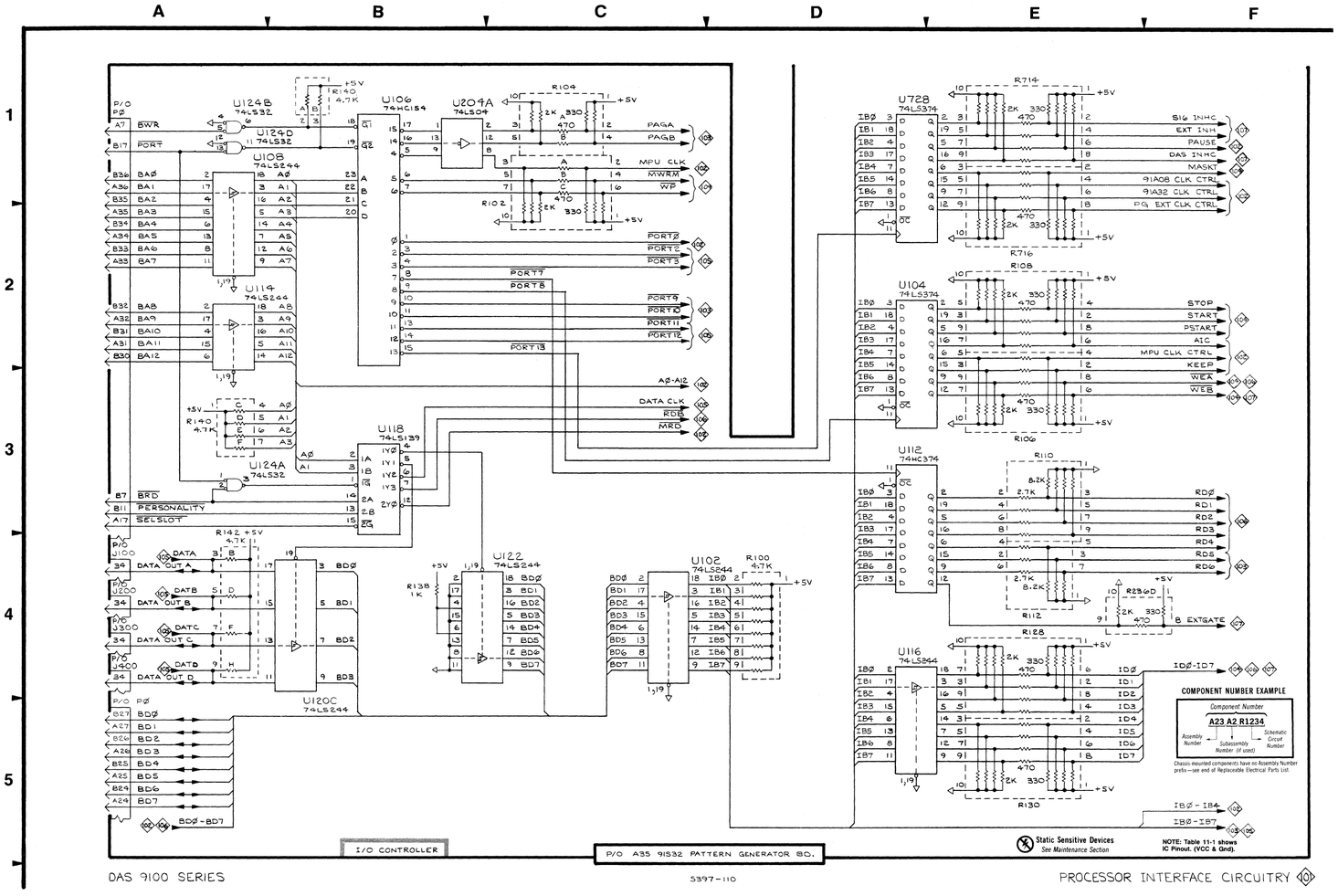
5397-65

Figure 11-4. A35 91S32 Pattern Generator Board & Component Locations.

Table 11-11

PROCESSOR INTERFACE (101) — 91S32 PATTERN GENERATOR BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J100	A4	A1	R140F	A3	F4
J200	A4	A2	R142B	A4	B2
J300	A4	A3	R142D	A4	B2
J400	A4	A4	R142F	A4	B2
P0	A1	E4	R142H	A4	B2
P0	A5	E4	R236D	E4	B2
R100	D4	F3	R714	E1	C3
R102A	C1	F4	R716	E2	C3
R102B	C1	F4	U102	C4	F3
R102C	C1	F4	U104	D2	E2
R104A	C1	G4	U106	B1	G4
R104B	C1	G4	U108	A1	G4
R106	E3	E2	U112	D3	B3
R108	E2	E2	U114	A2	F4
R110	E3	B3	U116	D4	F3
R112	E4	B3	U118	B3	F4
R128	E4	E4	U120C	B4	B2
R130	E5	F3	U122	C4	E4
R138	B4	F4	U124A	A3	F4
R140A	B1	F4	U124B	A1	F4
R140B	B1	F4	U124D	A1	F4
R140C	A3	F4	U204A	B1	G4
R140D	A3	F4	U728	D1	C3
R140E	A3	F4			



DAS 9100 SERIES

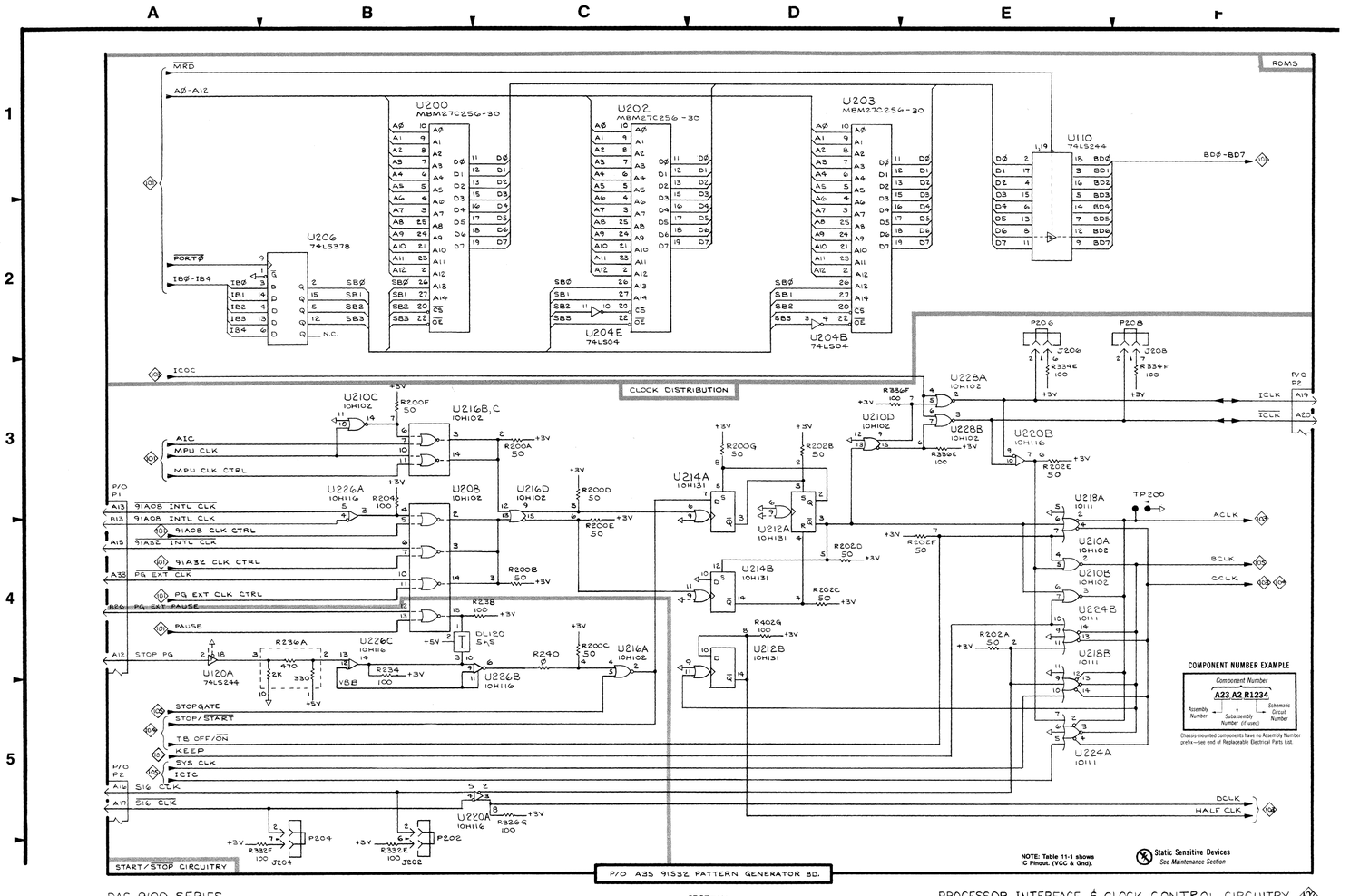
5397-110

PROCESSOR INTERFACE CIRCUITRY (101)

Table 11-12

PROCESSOR INTFC. & CLK. CNTL. 102 — 91S32 PAT. GEN. BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL120	B4	C4	R336F	E3	F2
J202	B5	F1	R402G	D4	C2
J204	B5	F1	TP200	F3	E1
J206	E2	F1	U110	E1	G4
J208	F2	F1	U120A	A4	B2
P1	A3	B4	U200	B1	G4
P2	F3	F1	U202	C1	G3
P2	A5	F1	U203	D1	G3
P202	B5	harmonica	U204B	D2	G4
P204	B5	harmonica	U204E	C2	G4
P206	E2	harmonica	U206	B2	G3
P208	F2	harmonica	U208	B4	C4
R200A	C3	D1	U210A	E4	E1
R200B	C4	D1	U210B	E4	E1
R200C	C4	D1	U210C	B3	E1
R200D	C3	D1	U210D	D3	E1
R200E	C4	D1	U212A	D3	E1
R200F	B3	D1	U212B	D4	E1
R200G	D3	D1	U214A	D3	D1
R202A	E4	E1	U214B	D4	D1
R202B	D3	E1	U216A	C4	D1
R202C	D4	E1	U216B	B3	D1
R202D	D4	E1	U216C	B3	D1
R202E	E3	E1	U216D	C3	D1
R202F	E4	E1	U218A	E4	E1
R204	B3	B4	U218B	E4	E1
R234	B4	B4	U220A	C5	F2
R236A	B4	B2	U220B	E3	F2
R238	C4	C4	U224A	E5	E1
R240	C4	D1	U224B	E4	E1
R326G	C5	E3	U226A	B3	B4
R332E	B5	F2	U226B	C4	B4
R332F	B5	F2	U226C	B4	B4
R334E	E3	F2	U228A	E3	F2
R334F	F3	F2	U228B	E3	F2
R336E	E3	F2			



DAS 9100 SERIES

5397-111

PROCESSOR INTERFACE & CLOCK CONTROL CIRCUITRY 102

Table 11-13

ADDRESS CONTROL CIRCUITRY ◇103◇ — 91S32 PAT. GEN. BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J302	B3	F1	R322	B5	F3
J304	B3	F1	R324A	D2	E2
J306	B3	F1	R324B	D2	E2
J308	B3	F1	R324C	D2	E2
J310	B3	F1	R324D	D2	E2
J312	B3	F1	R324E	D3	E2
J314	B3	F1	R324F	D3	E2
J316	B3	F1	R324G	D3	E2
J318	B3	F1	R324H	D3	E2
J320	B3	F1	R326A	D5	E3
J322	B3	F1	R326B	B2	E3
J324	B3	F1	R328	F5	B2
P2	A1	F1	R332A	B3	F2
P302	B3	harmonica	R332B	B3	F2
P304	B3	harmonica	R332C	B3	F2
P306	B3	harmonica	R332D	B3	F2
P308	B3	harmonica	R334A	B3	F2
P310	B3	harmonica	R334B	B3	F2
P312	B3	harmonica	R334C	B3	F2
P314	B3	harmonica	R334D	B3	F2
P316	B3	harmonica	R336A	B3	F2
P318	B3	harmonica	R336B	B3	F2
P320	B3	harmonica	R336C	B3	F2
P322	B3	harmonica	R336D	B3	F2
P324	B3	harmonica	R338A	B4	E3
R300	C1	F3	R338B	A4	E3
R302	C2	F3	R338C	B3	E3
R304	C3	G3	R338D	B3	E3
R306	C2	F3	R338E	B4	E3
R308A	E2	C4	R338F	D1	E3
R308B	E2	C4	R338G	B4	E3
R308C	E4	C4	U300	A1	E2
R308D	E4	C4	U302	B1	F3
R308E	E4	C4	U304	D1	E2
R308F	E4	C4	U306	E1	E2
R308G	E2	C4	U308	A2	F2
R308H	E2	C4	U310	E2	E2
R310A	E4	B3	U312	A3	F2
R310B	E4	B3	U314	B2	G3
R310C	E4	B3	U316	D2	F3
R310E	E4	B3	U318	E3	E3
R312A	E1	B3	U320	F3	B3
R312B	E1	B3	U324	E3	E3
R312C	E1	B3	U326	F4	C3
R312D	E3	B3	U328A	C4	F3
R312E	E3	B3	U328D	D3	F3
R312F	E3	B3	U330	D4	F2
R312G	E3	B3	U332	E4	E3
R312H	E1	B3	U334	F4	B3
R316A	D5	F3	U338	C5	F3
R316A	B5	F3	U340	D5	F3
R316C	C1	F3	U344	F5	C2
R316D	B5	F3	U346A	C5	G3
R316E	B4	F3	U346B	B4	G3
R316F	A4	F3	U346C	D5	G3
R316G	B5	F3	U346D	B5	G3
R318	B1	E3	U348A	B5	F3
R320A	D3	F3	U348B	B5	F3
R320B	D2	F3	U350	C4	F2
R320C	C3	F3	U352A	B5	F2
R320D	C4	F3	U352B	C5	F2
R320E	D5	F3	U352C	C4	F2
R320F	C5	F3	U352D	B5	F2
R320G	D5	F3			

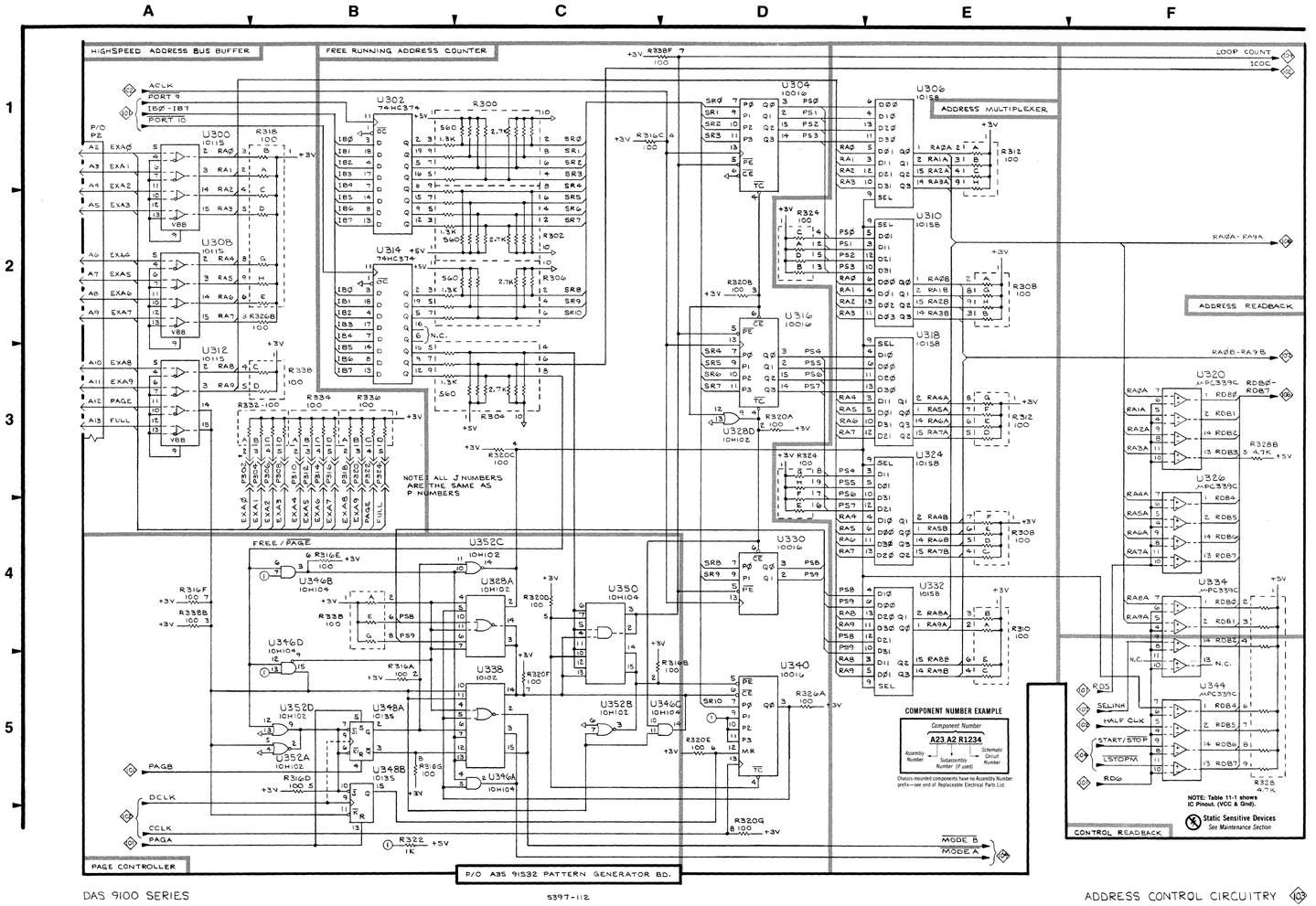
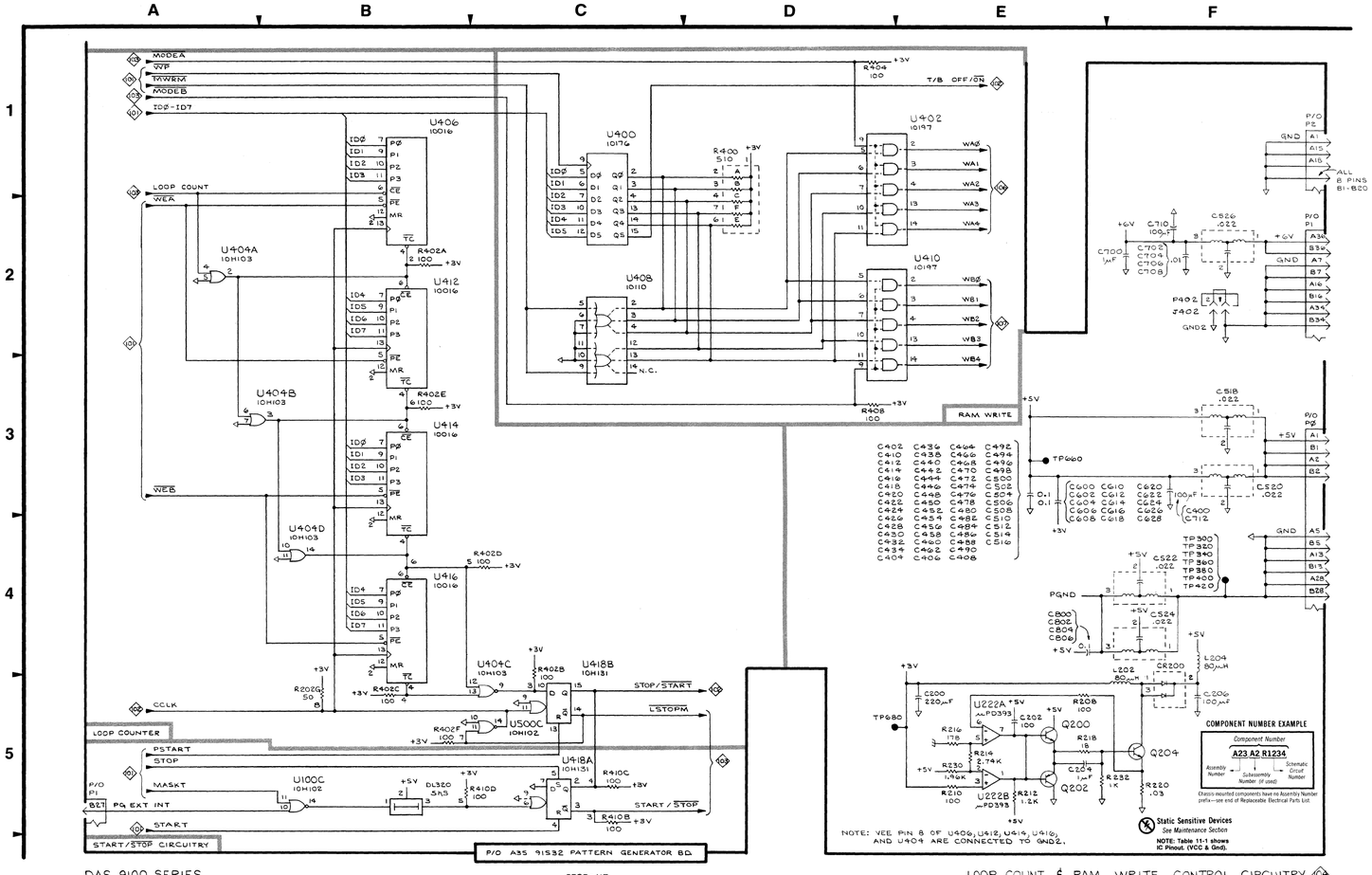


Table 11-14

LOOP COUNT & RAM WRITE CONTROL (104) — 91S32 PAT. GEN. BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C200	E5	G2	C500	E3	E3	R202G	B5	E1
C202	E5	G1	C502	E3	E4	R208	E5	G1
C204	E5	G1	C504	E3	C3	R210	E5	G1
C206	F5	G2	C506	E3	B3	R212	E5	G1
C400	F3	E4	C508	E3	D4	R214	E5	G1
C402	E3	B2	C510	E3	B2	R216	E5	G1
C404	E3	B2	C512	E3	C4	R218	E5	G1
C406	E3	A3	C514	E3	C4	R220	F5	G2
C408	E3	C2	C516	E3	C3	R230	E5	G1
C410	E3	D2	C518	F3	D4	R232	F5	G1
C412	E3	A2	C520	F3	D4	R400A	D1	E4
C414	E3	A3	C522	F4	A4	R400B	D1	E4
C416	E3	D1	C524	F4	A4	R400C	D1	E4
C418	E3	C2	C526	F2	B4	R400E	D1	E4
C420	E3	B3	C600	E3	A1	R400F	D1	E4
C422	E3	A1	C602	E3	A2	R402A	B2	C2
C424	E3	F3	C604	E3	A2	R402B	C5	C2
C426	E3	G3	C606	E3	A4	R402C	B5	C2
C428	E3	G3	C608	E3	A3	R402D	B4	C2
C430	E3	A2	C610	E3	B4	R402E	B3	C2
C432	E3	F3	C612	E3	C1	R402F	B5	C2
C434	E3	G2	C614	E3	C1	R404	D1	E2
C436	E3	F2	C616	E3	B1	R408	D3	E2
C438	E3	C2	C618	E3	D2	R410B	C5	D2
C440	E3	B1	C620	E3	D3	R410C	C5	D2
C442	E3	F4	C622	E3	E4	R410D	C5	D2
C444	E3	F4	C624	E3	E3	TP300	F4	A1
C446	E3	D3	C626	E3	F2	TP320	F4	A3
C448	E3	G4	C628	E3	B2	TP340	F4	D3
C450	E3	D3	C700	F2	C2	TP360	F4	E1
C452	E3	G4	C702	F2	B2	TP380	F4	E3
C454	E3	F4	C704	F2	B3	TP400	F4	G1
C456	E3	D3	C706	F2	B4	TP420	F4	G2
C458	E3	F2	C708	F2	B3	TP660	E3	F2
C460	E3	D2	C710	F2	B4	TP680	E5	E1
C462	E3	A4	C712	F3	C4	U100C	B5	B4
C464	E3	C2	C800	E4	A1	U222A	E5	G1
C466	E3	E1	C802	E4	A2	U222B	E5	G1
C468	E3	E2	C804	E4	A3	U400	C1	E4
C470	E3	C2	C806	E4	A4	U402	E1	E2
C472	E3	E2	CR200	F5	G2	U404A	A2	C2
C474	E3	E3	DL320	B5	D2	U404B	B3	C2
C476	E3	F2	J402	F2	C2	U404C	C5	C2
C478	E3	B3	L202	F5	G2	U404D	B4	C2
C480	E3	D2	L204	F4	F2	U406	B1	C2
C482	E3	D2	P0	F3	E4	U408	C2	F4
C484	E3	C1	P1	A5	B4	U410	E2	E2
C486	E3	B4	P1	F2	B4	U412	B2	C2
C488	E3	D4	P2	F1	F1	U414	B3	C2
C490	E3	B4	P402	F2	harmonica	U416	B4	C2
C492	E3	E3	200	E5	G1	U418A	C5	E2
C494	E3	A4	Q202	E5	G1	U418B	C5	E2
C496	E3	C2	Q204	F5	G2	U500C	C5	D2
C498	E3	B2						

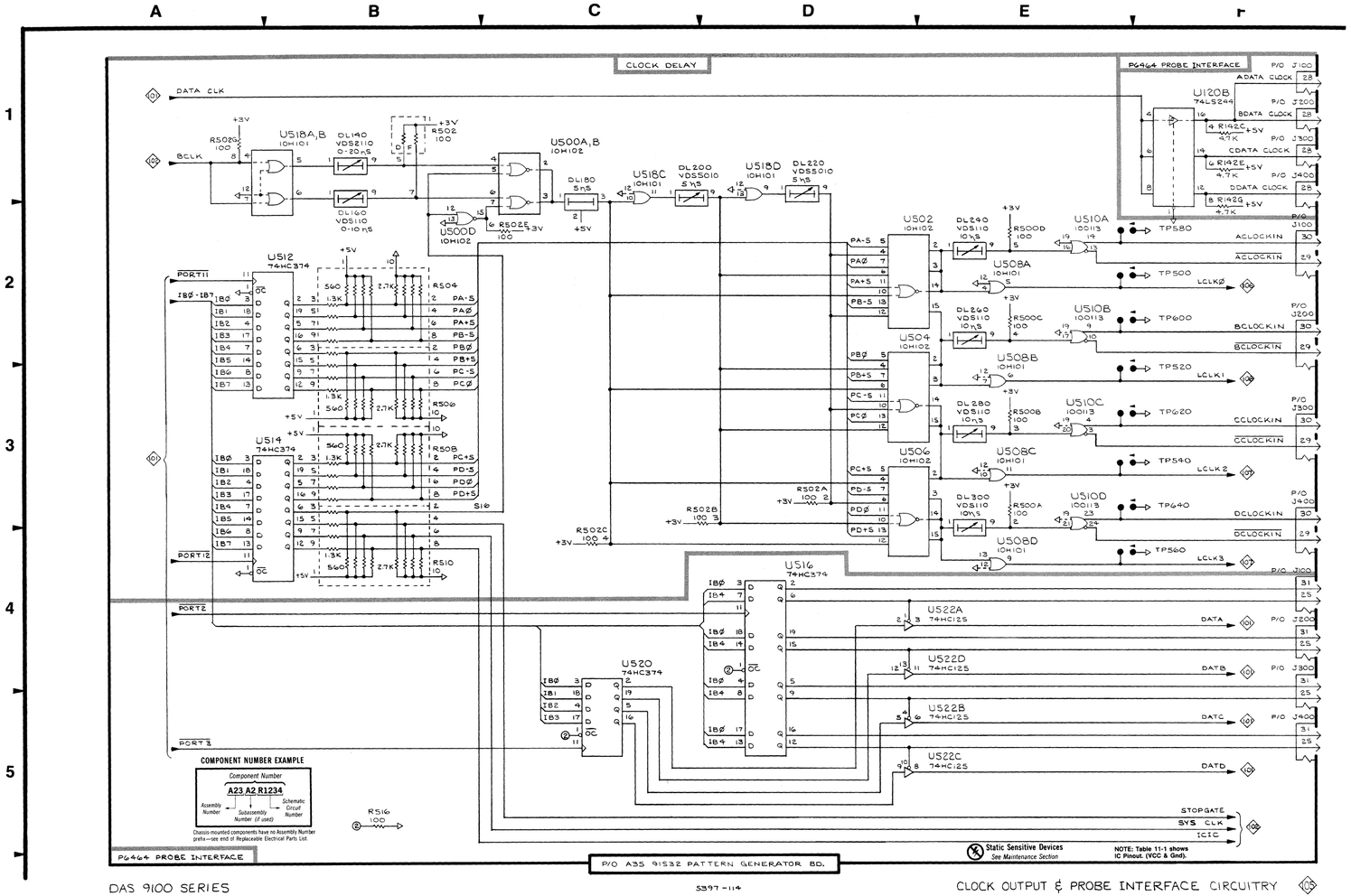


P/O A35 PAT. GEN. BD. LOOP CNT. & RAM WR. CONT. CIRCUITRY (104)

Table 11-15

CLOCK OUTPUT & PROBE INTFC. (105) — 91S32 PAT. GEN. BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
DL140	B1	D2	R510	B4	E2
DL160	B1	D2	R516	B5	B3
DL180	C1	C1	TP500	F2	B2
DL200	C1	D2	TP520	F3	B2
DL220	D1	D2	TP540	F3	B3
DL240	E2	B1	TP560	F4	B4
DL260	E2	B1	TP580	F2	A1
DL280	E3	C1	TP600	F2	A2
DL300	E3	C1	TP620	F3	A3
J100	F4	A1	TP640	F3	A4
J100	F2	A1	U120B	F1	B2
J100	F1	A1	U500A	C1	D2
J200	F4	A2	U500B	C1	D2
J200	F2	A2	U500D	B2	D2
J200	F1	A2	U502	D2	C1
J300	F3	A3	U504	D3	D1
J300	F1	A3	U506	D3	D1
J300	F4	A3	U508A	E2	C1
J400	F4	A4	U508B	E3	C1
J400	F1	A4	U508C	E3	C1
J400	F3	A4	U508D	E4	C1
R142C	F1	B2	U510A	E2	B1
R142E	F1	B2	U510B	E2	B1
R142G	F1	B2	U510C	E3	B1
R500A	E3	B1	U510D	E3	B1
R500B	E3	B1	U512	A2	D2
R500C	E2	B1	U514	B3	E2
R500D	E2	B1	U516	D4	B3
R502A	D3	D2	U518A	B1	D2
R502B	D3	D2	U518B	B1	D2
R502C	C4	D2	U518C	C1	D2
R502D	B1	D2	U518D	D1	D2
R502E	C2	D2	U520	C4	B2
R502F	B1	D2	U522A	E4	B2
R502G	A1	D2	U522B	E5	B2
R504	B2	D2	U522C	E5	B2
R506	B3	D2	U522D	E4	B2
R508	B3	D2			



DAS 9100 SERIES

5397-114

CLOCK OUTPUT & PROBE INTERFACE CIRCUITRY (105)

P/O A35 PAT. GEN. BD. CLK OUT. & PROBE INTER. CIRC. (105)

Table 11-16

VECTOR RAM, READ STATUS, & DATA OUTPUT (106) — 91S32 PAT. GEN. BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J100	F1	A1	U606	A3	D3
J200	F3	A2	U608	B3	C3
R600A	B1	C3	U610	B1	D3
R600B	B1	C3	U612	B2	D3
R600C	B1	C3	U614	B2	D3
R600D	A3	C3	U616	B3	C3
R600E	A2	C3	U618	B4	C3
R602A	E1	A2	U620	C1	B2
R602B	E1	A2	U622	C1	B2
R602C	E1	A2	U624	C2	B2
R602D	E1	A2	U626	C2	B2
R602E	E1	A2	U628	C3	B2
R604A	E2	A2	U630	C3	B2
R604B	E2	A2	U632	C3	B2
R604C	E2	A2	U634	C4	B2
R604D	E2	A2	U636	C4	B3
R604E	E2	A2	U638	C5	B3
R604F	E2	A2	U640	F1	A2
R604G	E3	A2	U642	F2	B2
R606A	E3	A3	U644	F3	A2
R606B	E3	A3	U646	F4	B2
R606C	E3	A3	U648A	F3	A1
R606D	E3	A3	U648B	F5	A1
R606E	E3	A3	U650	E5	B2
R608A	E4	A3	U652	D1	B3
R608B	E4	A3	U654	D1	B3
R608C	E4	A3	U656	D2	B3
R608D	E4	A3	U658	D2	B3
R608E	E4	A3	U660	D3	B4
R608F	E4	A3	U662	D3	B4
R608G	F5	A3	U664	D3	B4
U600	A1	E3	U666	D4	B4
U602	A2	E3	U668	D4	B3
U604	A2	E3	U670	D5	B3

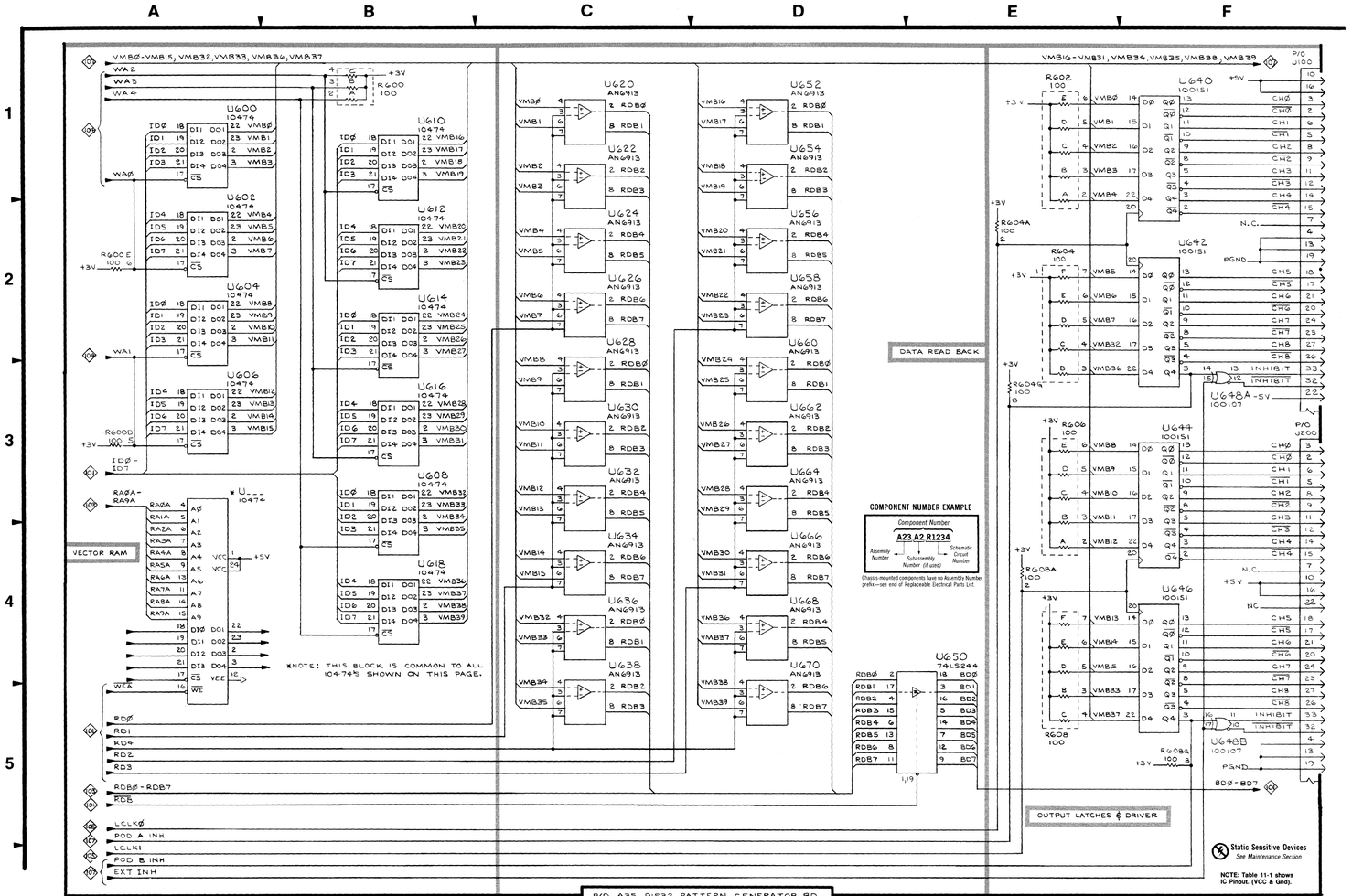
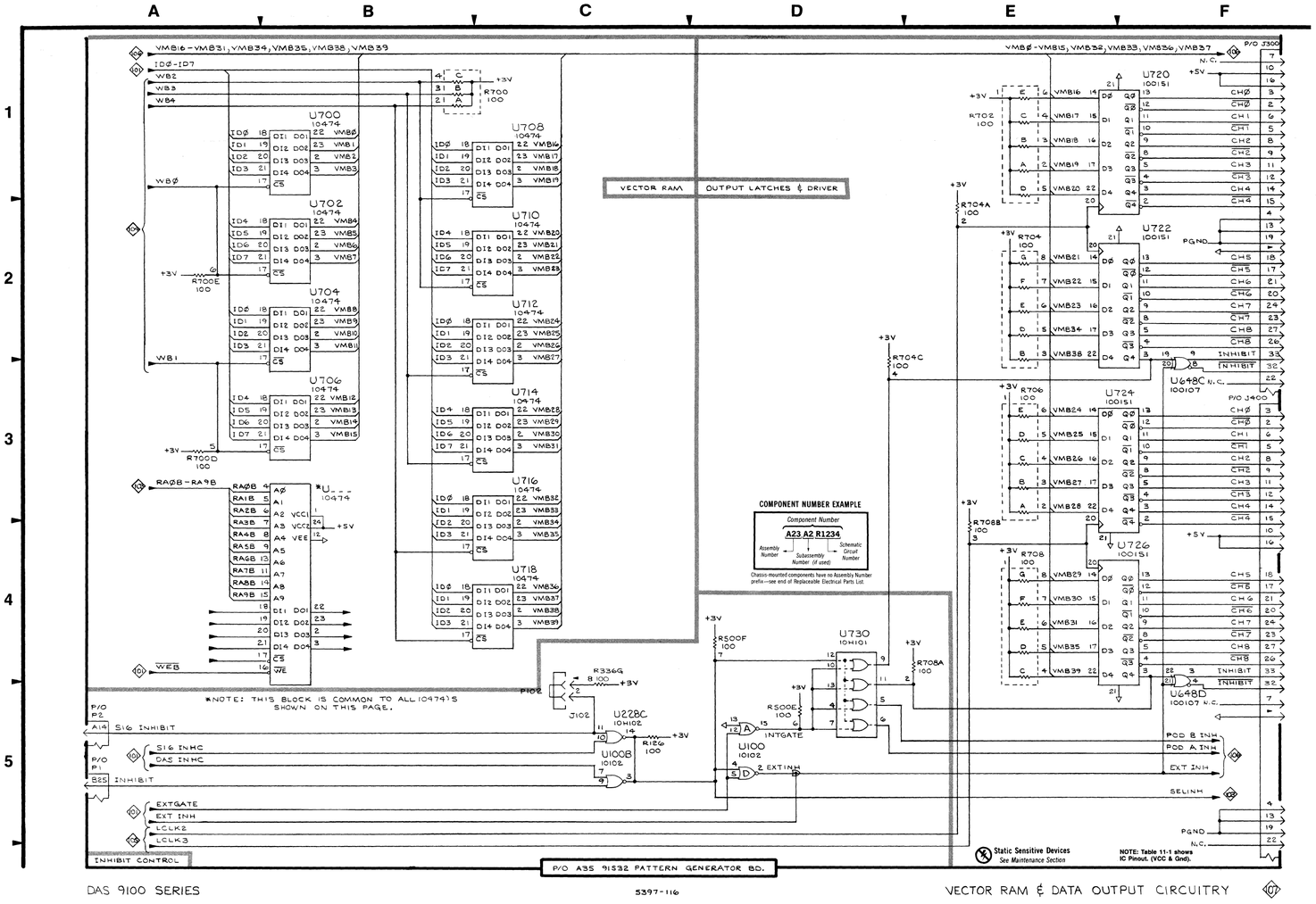


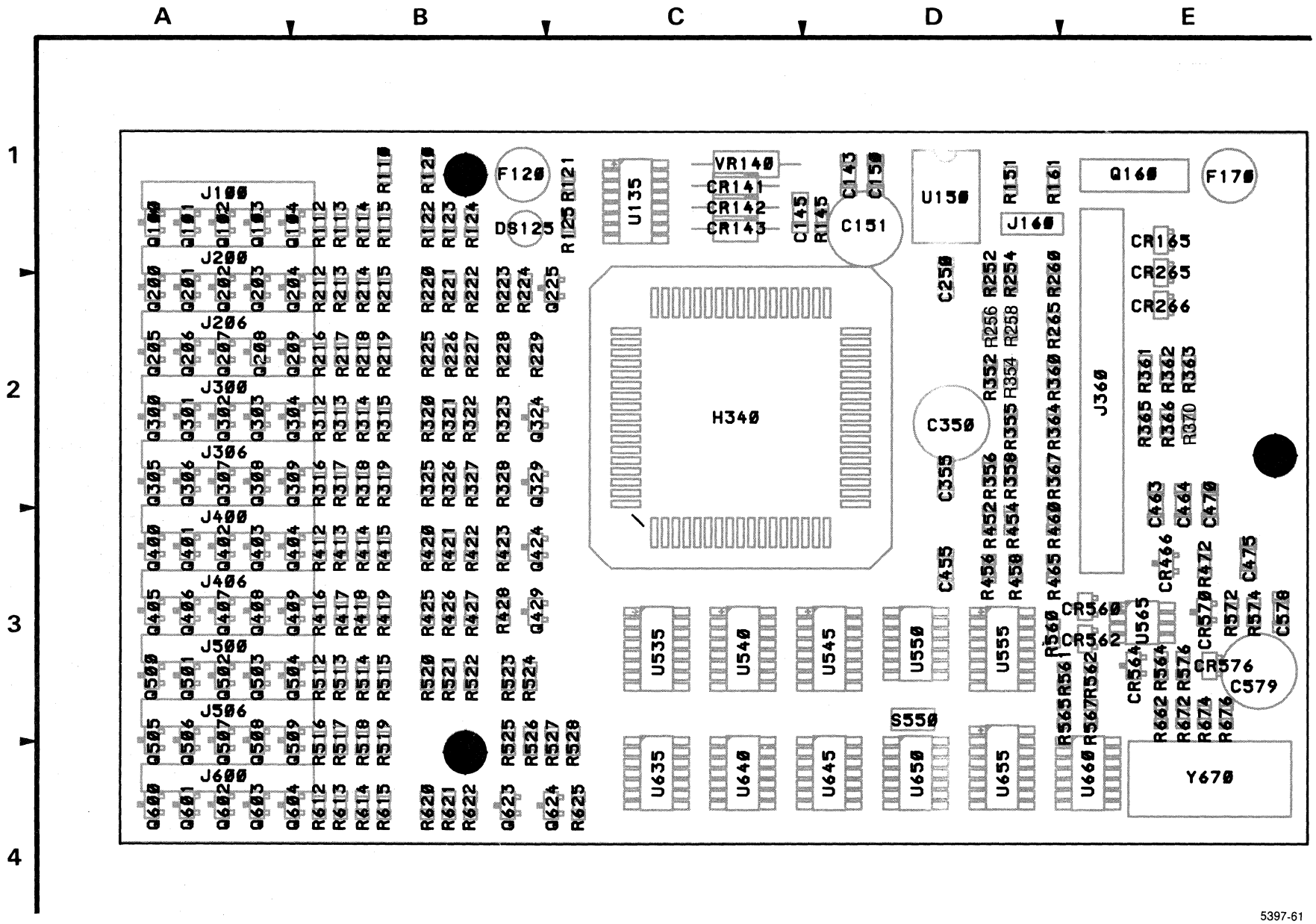
Table 11-17

VECTOR RAM & DATA OUTPUT (107) — 91S32 PAT. GEN. BD., ASSY. A35

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J102	C5	F2	R706E	E3	A4
J300	F1	A3	R708A	E4	A4
J400	F3	A4	R708B	E4	A4
P1	A5	B4	R708C	E4	A4
P2	A5	F1	R708D	E4	A4
R126	C5	F2	R708E	E4	A4
R336G	C5	F2	R708F	E4	A4
R500E	D5	B1	R708G	E4	A4
R500F	D4	B1	U100A	D5	B4
R700A	B1	C4	U100B	C5	B4
R700B	B1	C4	U100C	C5	B4
R700C	B1	C4	U100D	D5	B4
R700D	A3	C4	U648C	F3	A1
R700E	A2	C4	U648D	F4	A1
R702A	E1	A3	U700	B1	E4
R702B	E1	A3	U702	B2	E4
R702C	E1	A3	U704	B2	E4
R702D	E1	A3	U706	B3	D4
R702E	E1	A3	U708	C1	D4
R704A	E2	A3	U710	C2	D4
R704B	E2	A3	U712	C2	D4
R704C	D3	A3	U714	C3	C4
R704D	E2	A3	U716	C3	C4
R704E	E2	A3	U718	C4	C4
R704F	E2	A3	U720	F1	A3
R704G	E2	A3	U722	F2	B3
R706A	E3	A4	U724	F3	B4
R706B	E3	A4	U726	F4	A4
R706C	E3	A4	U730	D4	B1
R706D	E3	A4			



A36 P6464 BOARD



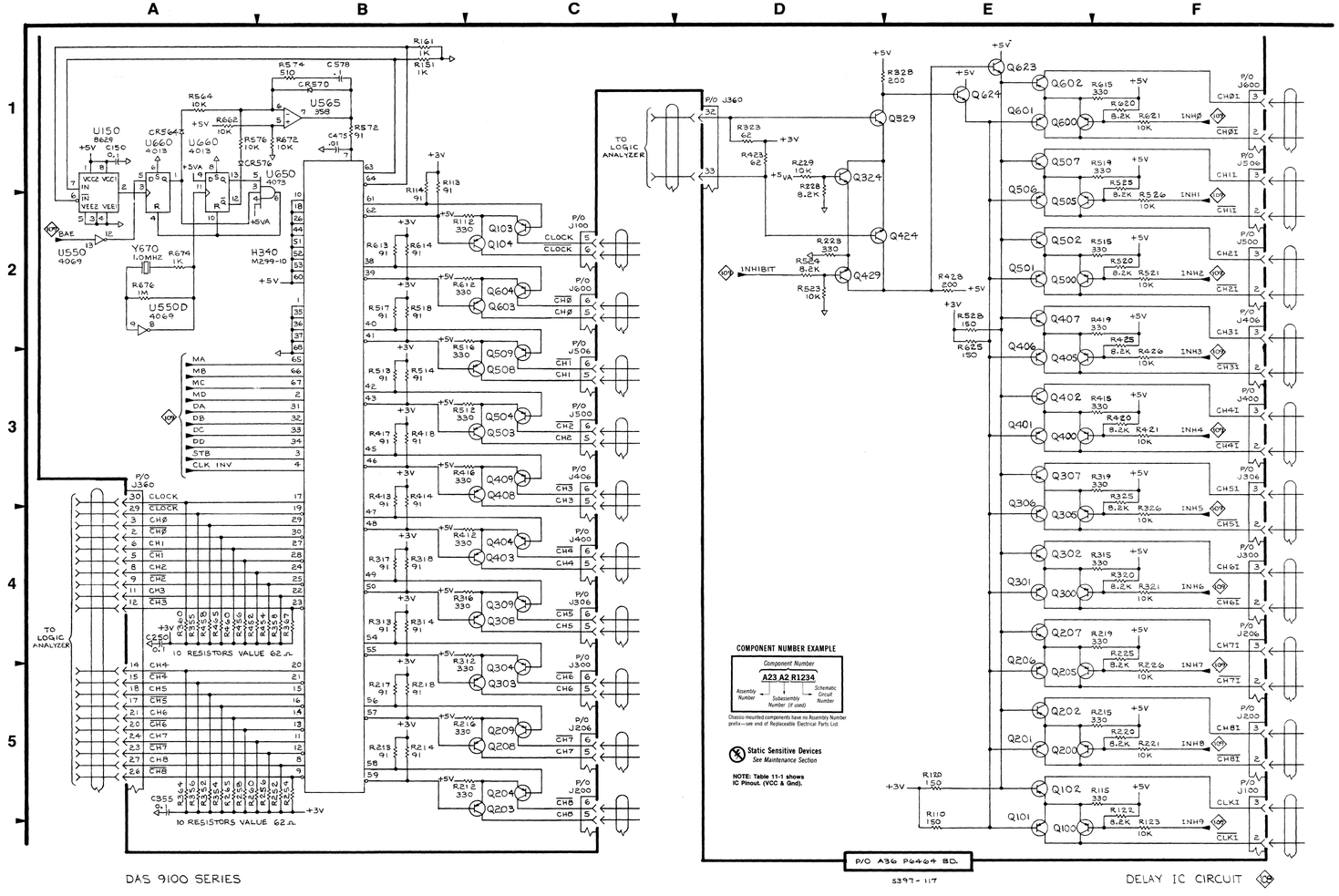
5397-61

Figure 11-5. A36 P6464 Board.

Table 11-18

DELAY IC CIRCUIT (108) — P6464 BOARD,ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C150	A1	D1	Q409	C3	A3	R354	A5	D2
C250	A4	D2	Q424	D2	B3	R355	A4	D2
C355	A5	D2	Q429	D2	B3	R356	A5	D2
C475	B1	E3	Q500	E2	A3	R358	B4	D2
C578	B1	E3	Q501	E2	A3	R360	A4	D2
CR564	A1	E3	Q502	E2	A3	R364	A5	D2
CR570	B1	E3	Q503	C3	A3	R367	B4	D2
CR576	A1	E3	Q504	C3	A3	R412	C4	B3
H340	B2	C2	Q505	E2	A4	R413	B3	B3
J100	F5	A1	Q506	E2	A4	R414	B3	B3
J100	C2	A1	Q507	E1	A4	R415	F3	B3
J200	F5	A1	Q508	C3	A4	R416	C3	B3
J200	C5	A1	Q509	C3	A4	R417	B3	B3
J206	F4	A2	Q600	E1	A4	R418	B3	B3
J206	C5	A2	Q601	E1	A4	R419	F2	B3
J300	C5	A2	Q602	E1	A4	R420	F3	B3
J306	F3	A2	Q603	C2	A4	R421	F3	B3
J306	C4	A2	Q604	C2	A4	R423	D1	B3
J360	A4	E2	Q623	E1	B4	R425	F2	B3
J360	D1	E2	Q624	E1	C4	R426	F3	B3
J400	C4	A3	R110	E5	B1	R428	E2	B3
J400	F3	A3	R112	C2	B1	R452	B4	D3
J406	F2	A3	R113	B1	B1	R454	B4	D3
J406	C3	A3	R114	B1	B1	R456	A4	D3
J500	C3	A3	R115	F5	B1	R458	A4	D3
J500	F2	A3	R120	E5	B1	R460	A4	D3
J506	C3	A3	R122	F5	B1	R465	A4	D3
J506	F1	A3	R123	F5	B1	R512	C3	B3
J600	C2	A4	R151	B1	D1	R513	B3	B3
J600	F1	A4	R161	B1	D1	R514	B3	B3
Q100	E5	A1	R212	C5	B2	R515	F2	B3
Q101	E5	A1	R213	B5	B2	R516	C2	B4
Q102	E5	A1	R214	B5	B2	R517	B2	B4
Q103	C2	A1	R215	F5	B2	R518	B2	B4
Q104	C2	A1	R216	C5	B2	R519	F1	B4
Q200	E5	A2	R217	B5	B2	R520	F2	B3
Q201	E5	A2	R218	B5	B2	R521	F2	B3
Q202	E5	A2	R219	F4	B2	R523	D2	B3
Q203	C5	A2	R220	F5	B2	R524	D2	B3
Q204	C5	A2	R221	F5	B2	R525	F1	B4
Q205	E5	A2	R223	D2	B2	R526	F2	B4
Q206	E5	A2	R225	F4	B2	R528	E2	C4
Q207	E4	A2	R226	F5	B2	R564	A1	E3
Q208	C5	A2	R228	D1	B2	R572	B1	E3
Q209	C5	A2	R229	D1	B2	R574	B1	E3
Q300	E4	A2	R252	B5	D2	R576	A1	E3
Q301	E4	A2	R254	B5	D2	R612	C2	B4
Q302	E4	A2	R256	B5	D2	R613	B2	B4
Q303	C5	A2	R258	A5	D2	R614	B2	B4
Q304	C5	A2	R260	B5	D2	R615	F1	B4
Q305	E4	A2	R265	A5	D2	R620	F1	B4
Q306	E4	A2	R312	C4	B2	R621	F1	B4
Q307	E3	A2	R313	B4	B2	R625	E2	C4
Q308	C4	A2	R314	B4	B2	R662	A1	E3
Q309	C4	A2	R315	F4	B2	R672	B1	E3
Q324	D1	B2	R316	C4	B2	R674	A2	E3
Q329	D1	B2	R317	B4	B2	R676	A2	E3
Q400	E3	A3	R318	B4	B2	U150	A1	D1
Q401	E3	A3	R319	F3	B2	U550D	A2	D3
Q402	E3	A3	R320	F4	B2	U550F	A2	D3
Q403	C4	A3	R321	F4	B2	U565	B1	E3
Q404	C4	A3	R323	D1	B2	U650B	B1	D4
Q405	E3	A3	R325	F3	B2	U660A	A1	E3
Q406	E3	A3	R326	F4	B2	U660B	A1	E3
Q407	E2	A3	R328	E1	B2	Y670	A2	E4
Q408	C3	A3	R352	A5	D2			

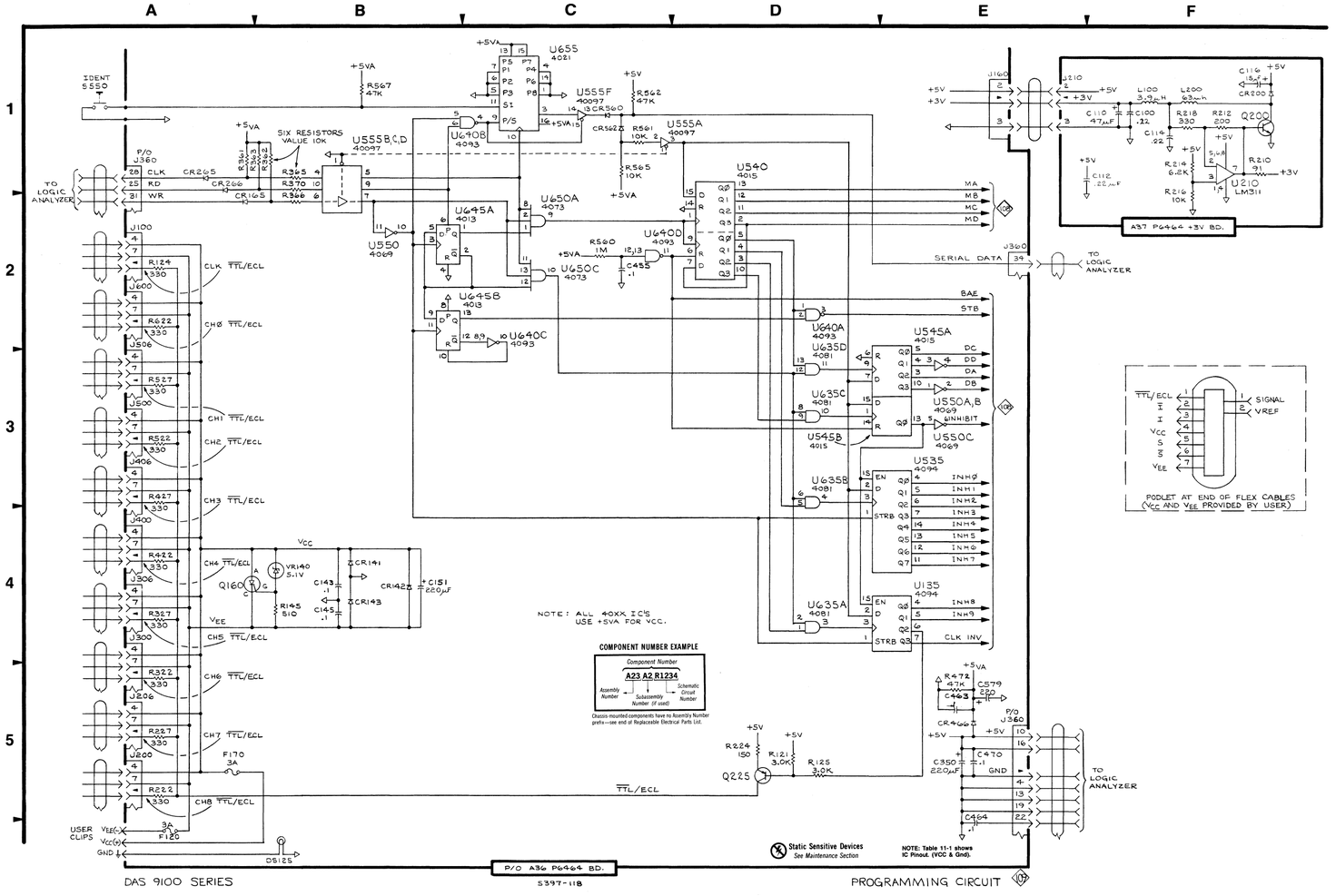


P/O A36 P6464 BD.
DELAY IC CIRCUIT (108)

Table 11-19

PROGRAMMING CIRCUIT 109 — P6464 BOARD,ASSEMBLY A36

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C143	B4	D1	R361	A1	E2
C145	B4	C1	R362	B1	E2
C151	B4	D1	R363	B1	E2
C350	E5	D2	R365	B1	E2
C455	C2	D3	R366	B2	E2
C463	E5	E3	R370	B1	E2
C464	E5	E3	R422	A4	B3
C470	E5	E3	R427	A3	B3
C579	E5	E3	R472	E5	E3
CR141	B4	C1	R522	A3	B3
CR142	B4	C1	R527	A3	C4
CR143	B4	C1	R560	C2	D3
CR165	A2	E1	R561	C1	E3
CR265	A1	E1	R562	C1	E3
CR266	A1	E2	R565	C1	E3
CR466	E5	E3	R567	B1	E3
CR560	C1	E3	R622	A2	B4
CR562	C1	E3	S550	A1	D3
DS125	B5	B1	U135	E4	C1
F120	A5	B1	U535	E3	C3
F170	A5	E1	U540	D2	C3
J100	A2	A1	U545A	E3	D3
J160	E1	D1	U545B	E3	D3
J200	A5	A1	U550A	E3	D3
J206	A5	A2	U550B	E3	D3
J300	A4	A2	U550C	E3	D3
J306	A4	A2	U550E	B2	D3
J360	A1	E2	U555A	C1	D3
J360	E5	E2	U555B	B1	D3
J360	E2	E2	U555C	B1	D3
J400	A4	A3	U555D	B1	D3
J406	A3	A3	U555F	C1	D3
J500	A3	A3	U635A	D4	C4
J506	A3	A3	U635B	D3	C4
J600	A2	A4	U635C	D3	C4
Q160	A4	E1	U635D	D3	C4
Q225	D5	C2	U640A	D2	C4
R121	D5	C1	U640B	C1	C4
R124	A2	B1	U640C	C2	C4
R125	D5	C1	U640D	C2	C4
R145	B4	D1	U645A	B2	D4
R222	A5	B2	U645B	B2	D4
R224	D5	B2	U650A	C2	D4
R227	A5	B2	U650C	C2	D4
R327	A4	B2	U655	C1	D4
R322	A5	B2	VR140	B4	C1



REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

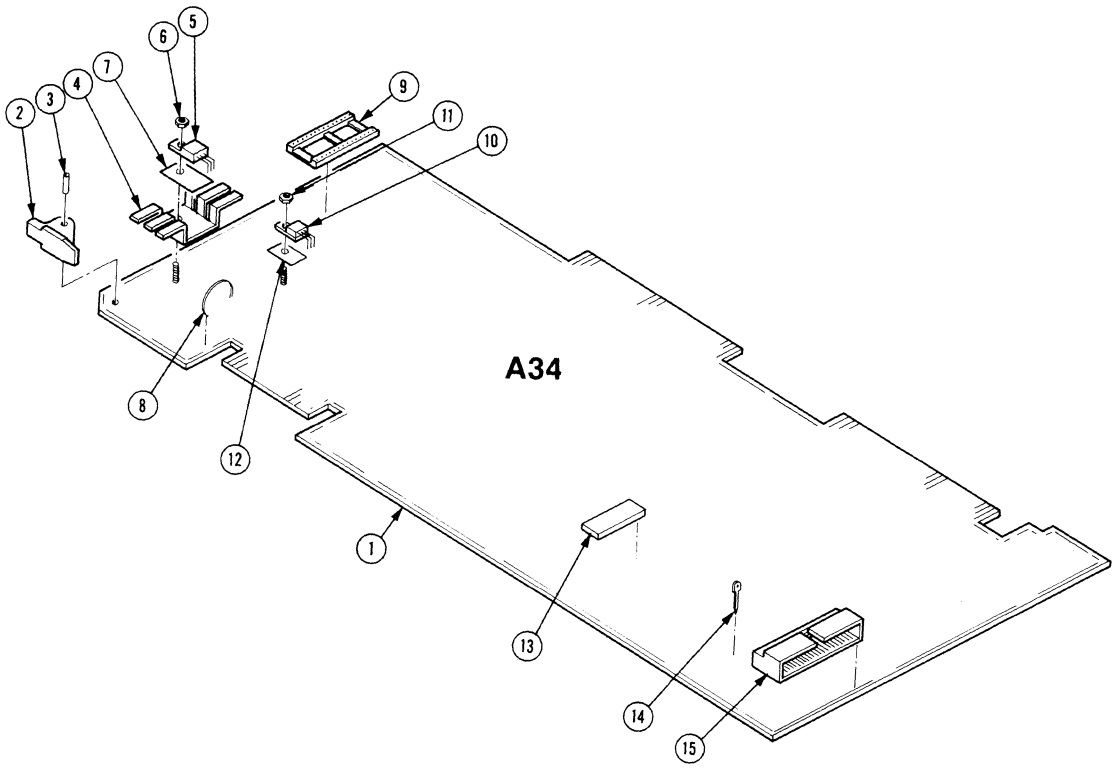
CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
73743	FISCHER SPECIAL MFG CO	446 MORGAN ST	CINCINNATI OH 45206
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
83385	MICRODOT MANUFACTURING INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
98159	RUBBER TECK, INC.	19115 HAMILTON AVE., P O BOX 389	GARDENA, CA 90247
TK1374	TRI-TEC ENGINEERING CORP	13130 S NORMANDIE AVE	GARDENA CA 90249
TK1473	RICHARD HIRSCHMANN OF AMERICA	PO BOX 229/INDUSTRIAL ROW	RIVERDALE NJ 07457

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	----- -----			1	CKT BOARD ASSY:PATT.GEN.(SEE A34 REPL)		
-2	105-0160-04			1	.EJECTOR,CKT BD:YELLOW PLASTIC	80009	105-0160-04
-3	214-1337-00			1	.PIN,SPRING:0.25 L X 0.103 OD,STL CD PL	80009	214-1337-00
-4	214-3729-00			1	.HEAT SINK:	80009	214-3729-00
-5	----- -----			1	.TRANSISTOR:(SEE A34Q954 REPL) .(ATTACHING PARTS)		
-6	210-0406-00			1	.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL .(END ATTACHING PARTS)	73743	12161-50
-7	342-0163-01			1	.INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	80009	342-0163-01
-8	346-0032-00			5	.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829-75-4
-9	136-0755-00			3	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-10	----- -----			1	.SEMICOND DVC:(SEE A34CR960 REPL) .(ATTACHING PARTS)		
-11	210-0406-00			1	.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL .(END ATTACHING PARTS)	73743	12161-50
-12	342-0163-01			1	.INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	80009	342-0163-01
-13	200-3070-00			6	.COVER,DLY LINE:	80009	200-3070-00
-14	----- -----			10	.TERM,TEST POINT:(SEE A34TP300,TP320, .TP860,TP910,TP930,TP940,TP950,TP960, .TP970,TP990 REPL)		
-15	----- -----			3	.CONN,RCPT,ELEC:(SEE A34J100,J120,J140 .REPL)		
	334-6230-00			1	.MARKER,IDENT:MKD 91S16 CHANNEL SELECTOR	80009	334-6230-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	----- -----			1	CKT BOARD ASSY:PATT.GEN.(SEE A35 REPL)		
-2	105-0160-04			1	.EJECTOR,CKT BD:YELLOW PLASTIC	80009	105-0160-04
-3	214-1337-00			1	.PIN,SPRING:0.25 L X 0.103 OD,STL CD PL	80009	214-1337-00
-4	214-3729-00			1	.HEAT SINK:	80009	214-3729-00
-5	----- -----			1	.TRANSISTOR:(SEE A35Q204 REPL)		
					.(ATTACHING PARTS)		
-6	210-0406-00			1	.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
					.(END ATTACHING PARTS)		
-7	342-0163-01			1	.INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	80009	342-0163-01
-8	346-0032-00			5	.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829-75-4
-9	----- -----			1	.SEMICOND DVC:(SEE A35CR200 REPL)		
					.(ATTACHING PARTS)		
-10	210-0406-00			1	.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
					.(END ATTACHING PARTS)		
-11	342-0163-01			1	.INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	80009	342-0163-01
-12	136-0755-00			3	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-13	----- -----			8	.TERM,PIN:(SEE A35TP200,TP500,TP520,		
					.TP540,TP560,TP600,TP620,TP640 REPL)		
-14	----- -----	300101	300115	18	.BUS,COND:(SEE A35P102,P202,P204,P206,		
					.P208,P302,P304,P306,P308,P310,P312,		
					.P314,P316,P318,P320,P322,P324,P402 REPL)		
-15	----- -----			1	.TERM,PIN:(SEE A35TP580 REPL)		
-16	200-3070-00	300101	300115	8	.COVER,DLY LINE:	80009	200-3070-00
-17	----- -----			9	.TERM,TEST POINT:(SEE A35TP300,TP320,		
					.TP340,TP360,TP380,TP400,TP420,TP660,		
					.TP680 REPL)		
-18	----- -----			4	.CONN,RCPT,ELEC:(SEE A35J100,J200,J300,		
					.J400 REPL)		
	200-3070-00	300116		8	COVER,DLY LINE:	80009	200-3070-00
	----- -----			18	BUS,COND:(SEE A35P102,P202,P204,P206,P208,		
					P302,P304,P306,P308,P310,P312,P314,P316,		
					P318,P320,P322,P324,P402 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
3-1	013-0217-00			23	GRABBER,IC LEAD:BLACK,2.047 L X 0.137 DIA (P6464 ONLY)	TK1473	973 592 500
	070-5167-00			1	MANUAL,TECH:OPERATORS	80009	070-5167-00
-2	175-9700-00			1	CA ASSY,SP,ELEC:40,28 AWG (91S32 ONLY)	80009	175-9700-00
-3	196-2963-00			10	LEAD SET,ELEC:(2) 23 AWG,3.156 L (P6464 ONLY)	80009	196-2963-00
-4	334-6094-00			1	OVERLAY,KYBD:MKD SONY/TEKTRONIX	80009	334-6094-00
	010-6464-00			2	PROBE,PATT GEN:50MHZ (91S16 ONLY)	80009	010-6464-00
	010-6464-00			4	PROBE,PATT GEN:50MHZ (91S32 ONLY)	80009	010-6464-00
-5	334-5957-00			2	.MARKER,IDENT:	80009	334-5957-00
-6	334-5987-00			1	.LABEL:MKD CLK STB	80009	334-5987-00
-7	380-0735-00			1	.HOUSING HALF:UPPER	80009	380-0735-00
-8	214-3672-00			1	.HEAT SINK,ELEC:68 PIN HYBRID,ALUMINUM .(ATTACHING PARTS)	80009	214-3672-00
-9	211-0001-00	8010100	8010673	4	.SCREW,MACHINE:2-56 X 0.25,PNH,STL	83385	ORDER BY DESCR
	211-0374-00	8010674		4	.SCREW,MACHINE:2-56 X 0.219 L,PNH,STL .(END ATTACHING PARTS)	80009	211-0374-00
-10	----- -----			1	.CKT BOARD ASSY:3V PWR SPLY(SEE A37 REPL) .(ATTACHING PARTS)		
-11	211-0007-00			2	.SCREW,MACHINE:4-40 X 0.188,PNH,STL .(END ATTACHING PARTS)	83385	ORDER BY DESCR
					CKT BOARD ASSY INCLUDES:		
-12	----- -----			3	..TERMINAL PIN:(SEE A37J210 REPL)		
-13	175-2911-00			1	.CA ASSY,SP,ELEC:3,26 AWG,3.5 L,RIBBON .(FROM A36J160 TO A37J210)	80009	175-2911-00
-14	175-9677-00			1	.CA ASSY,SP,ELEC:8,28 AWG,80.0 L,RIBBON	TK1374	ORDER BY DESCR
-15	----- -----			10	.MICROCIRCUIT,DI:(SEE J100,J200,J206, .J300,J306,J400,J406,J500,J506,J600 .REPL)		
-16	----- -----			1	.CKT BOARD ASSY:MAIN(SEE A36 REPL)		
-17	136-0252-07			70	..SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-18	136-0840-00	8010100	8010673	1	..SKT,PL-IN ELEK:CHIP CARRIER,HIGH SPEED	00779	821516-5
	136-0840-01	8010674		1	..SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACT	80009	136-0840-01
-19	----- -----			3	..TERMINAL PIN:(SEE A36J160 REPL)		
-20	----- -----			1	..CONN,RCPT,ELEC:(SEE A36J360 REPL)		
-21	----- -----			1	..CA ASSY,SP,ELEC:(SEE A36S550 REPL)		
-22	361-1323-00			1	.SPACER,PLATE:0.01 X 0.945 X 0.945,BRS,NP	80009	361-1323-00
-23	380-0736-00			1	.HOUSING HALF:LOWER	80009	380-0736-00
	346-0032-00			1	.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829-75-4
					OPTIONAL ACCESSORIES		
	003-1134-00			1	ALIGN TOOL,ELEC:	80009	003-1134-00
	010-6460-01			1	PROBE,DATA ACQ:	80009	010-6460-01
	070-5397-00			1	MANUAL,TECH:SERVICE	80009	070-5397-00
	175-8165-00			1	CABLE ASSY,RF:50 OHM COAX,79.0 L,8-N	80009	175-8165-00
	175-9676-00			1	CABLE ASSY,RF:50 OHM COAX,6.0 L	80009	175-9676-00
	175-9782-00			1	CA ASSY,SP,ELEC:INTERCONNECT EXTENSION	80009	175-9782-00
	346-0032-00			1	.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829-75-4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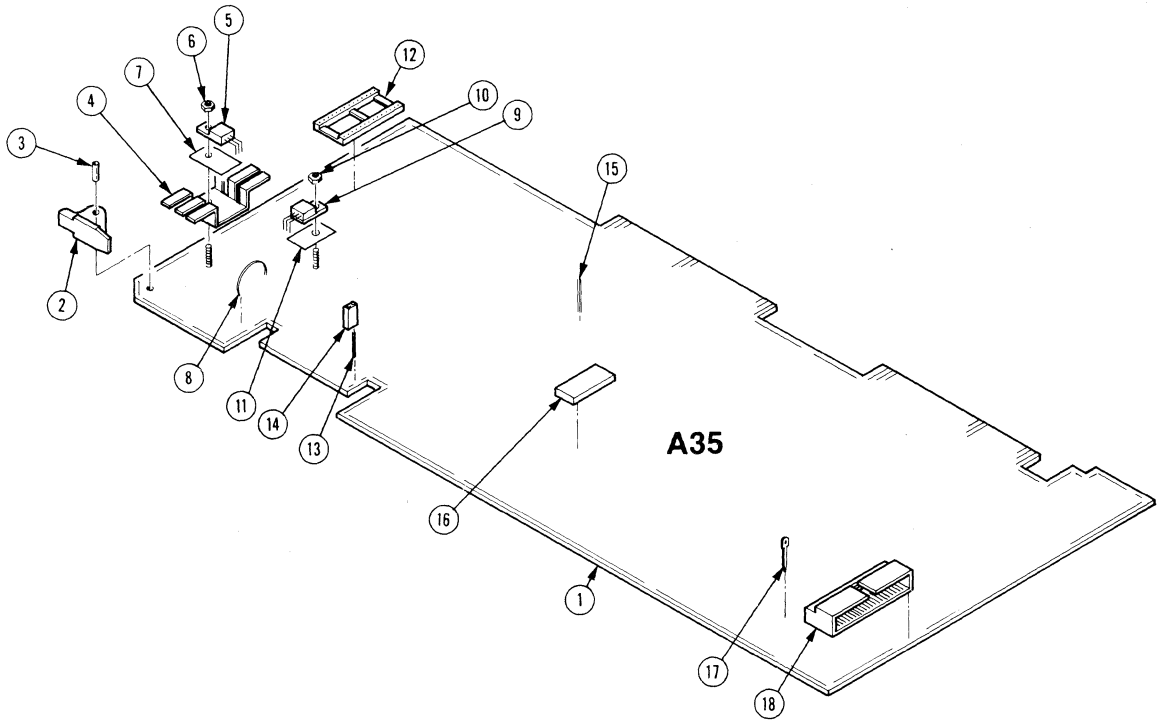
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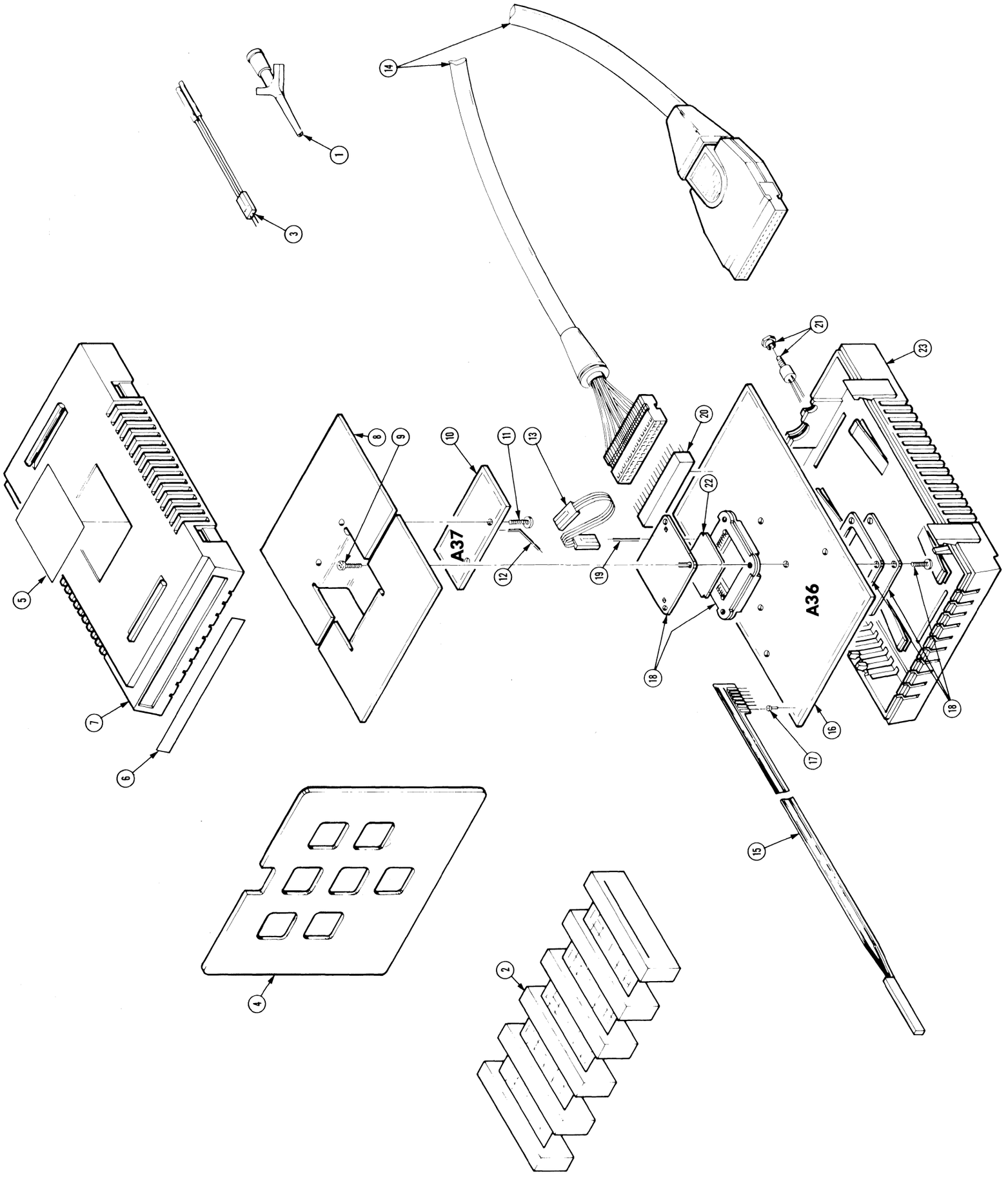
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MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: January 28, 1986 Change Reference: C1/186

Product: 91S16/91S32 Service Manual Addendum Manual Part No.: 070-5397-00

DESCRIPTION

THIS IS A PAGE PULL AND REPLACE PACKAGE

1. Remove the designated pages from your manual and insert the following pages 1-31 and 1-32.
2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.

000-2775-00D

Table 1-9 (cont.)
ELECTRICAL SPECIFICATION: 91S32 EXTERNAL CONTROL SIGNALS

Characteristic	Performance Requirement	Supplemental Information
Pause Input		1 pause line (level selectable) Freezes the current data outputs while pause line remains true.
Pause Input Minimum Pulse Width		19 ns
Pause Input Setup Time Relative to External Clock Input		19 ns minimum Assert the pause request 19 ns prior to the selected edge of the external clock.
Pause Input Hold Time Relative to External Clock Input		0 ns max Assert the pause request 0 ns after the selected edge of the external clock.
Pause Input Setup Time Relative to Pod Clock Output		120 ns minimum 108 ns typical Assert the pause request 120 ns prior to Pod Clock selected edge output.
External Start Input		The pattern generator automatically starts when the external start signal is asserted after once pressing the START PAT GEN or START SYSTEM key on the keyboard.
External Start Input Minimum Pulse Width		19 ns minimum
External Start Input Setup Time Relative to External Clock Input		14 ns minimum 5 ns typical
External Start Input Hold Time Relative to External Clock Input		5 ns minimum 0 ns typical

Table 1-10
P6464 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
Clock In, Maximum Frequency	50 MHz (20 ns)	
Power Required		Power required per channel from user's circuit. Voltages referenced to instrument ground.
V_H		−.5 V to +5.5 V at 85 mA + I load (user's more positive supply voltage)
V_L		+.3 V to −5.5 V at 88 mA + I load (user's more negative supply voltage)
$V_H - V_L$		4.8 V to 5.2 V (within individual probes)
Pin Driver Outputs: Data, Clock, Strobe		
TTL Mode	$V_{L\,OUT} = V_L + .80$ V $V_{H\,OUT} = V_H - 1$ V	
Drive Capability	sink or source > 20 mA	
Transition Time		3.5 ns maximum (20% to 80% of logic level), resistive load
ECL Mode	$V_{L\,OUT} = V_H - 1.65$ V $V_{H\,OUT} = V_H - 1$ V	Nominal open emitters
Drive Capability	20 mA (50Ω to V_H −2 V)	50 pF maximum
Transition Time		2.5 ns maximum (20% to 80% of logic level), resistive load