Tektronix®
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DAS 9100 SERIES

SERVICE MANUAL WITH OPTIONS
VOL. I

This Tektronix manual supports all products listed below. It revises the original manual (issued October 1982, part numbers 070-3625-00 and 070-3836-00) by incorporating service information for the DAS9129 Color Mainframe throughout all sections.

MAINFRAMES

DAS9129 - Color
DAS9109 - Basic
DAS9119 - ATE

INSTRUMENT MODULES

91A32 - Data Acquisition
91A08 - Data Acquisition
91P16 - Pattern Generator
91P32 - Pattern Generator

OPTIONS

Option 01 - Tapedrive
Option 02 - I/O Interface
Option 03, 04 - +5 V Power Supply
Option 05 - Rackmount

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

Tektronix, Inc.
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Serial Number _____

070-3625-01
Product Group 57

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

MANUAL REVISION STATUS

PRODUCT: DAS 9100 SERIES SERVICE MANUAL VOL. I

This manual supports the following versions of this product: All

REV DATE	DESCRIPTION
AUG 1982	Original Issue
APRIL 1983	Revised Printing
MAY 1983	Revised Printing
OCT 1983	Revised Printing: Sections; 1, 4 and 5 Pages; iii and Tab 1, INTRODUCTION & SPECIFICATIONS
JAN 1984	Revised Printing: Pages; i and 1-11

PREFACE

The DAS 9100 Series Service Manual is organized in two volumes. The first volume contains the specifications, the theory of operation, and other instrument familiarization information. The second volume contains the information most likely to be used directly while repairing or maintaining a DAS module or system. Note, however, that both of the volumes are required to complete a repair because the Verification and Adjustment Procedures are contained in the first volume.

This manual is designed for use by a qualified service technician with moderate experience with high-speed digital circuitry. Familiarity with both the TTL and ECL logic families is assumed. Familiarity with, and the ability to operate, standard test instruments used on digital circuitry, like high-speed oscilloscopes and logic analyzers, is also assumed.

The DAS 9100 Series contains some complicated and/or non-standard circuits. For most effective use of repair time, it is wise to become familiar with the operation of the instrument, both the hardware and the firmware. The Theory of Operation is organized as a learning guide to the structure and function of the instrument.

Since in many cases familiarity with the instrument is not feasible, the Maintenance: General Information and the Maintenance: Troubleshooting sections in volume two give the required information to complete most repairs in a short time. This will prove useful to the technician who does not often have occasion to repair a DAS 9100 Series instrument.

WHAT THIS MANUAL CONTAINS

The Service Manual is divided into twelve sections that are located in two binders. The third binder is available for Addenda to the Service Manual.

VOLUME 1

Section 1 - Introduction and Specifications. This section describes the DAS 9100, its modes of operation, products and options, standard and optional accessories, and electrical and physical specifications.

Section 2 - Options. This section lists the options that are available with the DAS 9100 Series of instruments.

Section 3 - Operating Instructions. This section describes the DAS 9100 power requirements, module installation procedures, probe connections, and the keyboard. There is also an overview of the menus used by the operator to control the system. Refer to the DAS 9100 Series Operator's Manual for complete operating instructions.

Section 4 - Theory of Operation. This section contains a discussion of the basic operation of the DAS 9100 Series instruments, a block diagram description of the DAS, and detailed circuit descriptions of all parts of the mainframe, modules, probes, and options.

Section 5 - Verification and Adjustment Procedures. This section contains the functional check procedures, the adjustment procedures and the performance check procedures for all parts of the DAS.

VOLUME 2

Section 6 - Maintenance: General Information. This section of the manual contains information necessary to maintain the DAS. General precautions, disassembly procedures, and general maintenance information is included in this section.

Section 7 - Maintenance: Troubleshooting. This section contains troubleshooting trees and information.

Section 8 - Maintenance: Diagnostic Test Descriptions. This section gives detailed instructions for using the Diagnostics menu. It also provides detailed descriptions of the operation of each test used by the diagnostics.

Section 9 - Reference Material. This section provides quick reference material for use while troubleshooting or adjusting any part of the DAS.

Section 10 - Replaceable Electrical Parts. This section contains a list (including Tektronix part numbers) of all replaceable electrical parts in the DAS.

Section 11 - Diagrams. This section contains all schematics for the DAS as well as board and component locator diagrams and tables.

Section 12 - Replaceable Mechanical Parts. This section contains lists (including part numbers) of all replaceable mechanical parts in the DAS and provides illustration to show the location of each of these parts.

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OPERATOR'S SAFETY SUMMARY

The general safety information in this summary is for both operator and service personnel. Specific cautions and warnings are placed throughout the manual where they apply but may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS AS MARKED ON EQUIPMENT


DANGER—high voltage


Protective ground (earth) terminal.


ATTENTION—refer to manual.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting it to the product. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including keys and controls that may appear to be insulating) can render an electrical shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for this product, and be sure it is in good condition.

Refer to the Operating Instructions section of this manual for information on power cords and connectors.

USE THE PROPER FUSE

To avoid fire hazard, use only a fuse of the correct type, voltage rating, and current rating as specified in the parts list for this product.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operator's Safety Summary.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on. Do not wear metal neck chains, wrist-bands or other metal jewelry while power is on and connections and components are exposed.

Disconnect power before removing protective panels, soldering, or replacing components.

USE CAUTION WHEN SERVICING THE CRT

The CRT should be serviced only by qualified personnel familiar with CRT servicing procedures and precautions.

CRTs retain hazardous voltages for long periods of time after power-down. Before attempting any work inside the monitor, discharge the CRT by shorting the anode connection to chassis ground. When discharging, connect to ground, then to anode.

Use extreme caution when handling the CRT. Rough handling may cause it to implode. Do not nick or scratch the glass or subject it to undue pressure during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the primary power supply, do not power up the instrument until such objects have been removed.

INTRODUCTION AND SPECIFICATIONS 1

INTRODUCTION AND SPECIFICATIONS

DESCRIPTION

The Digital Analysis System (DAS) 9100 Series is a family of programmable logic analysis instruments useful in the design, manufacture, and service of digital products. The series features a modular system architecture that allows various instrument configurations, each tailored to meet specific testing requirements. A DAS may be configured as a logic analyzer, as a pattern generator, or as a combination of the two. Option selections for adding an I/O interface (GPIB, RS-232, hard copy), a tape drive, supplemental dc power, and rackmount hardware are also available.

DAS modularity is built around the 9100 Series of microprocessor-controlled mainframes (see Figure 1-1). These units house all modular components and options and provide the circuitry and firmware necessary to integrate their functions.

Instrument functions and additional power supplies are added to the mainframe in modules. Up to six data acquisition and pattern generator modules may be installed, as long as they do not exceed the maximum of 104 acquisition or 80 stimulus channels.

Choose between:

- **91A32 Data Acquisition Module,** 32 channels at 25 MHz, (three maximum).
- **91A08 Data Acquisition Module,** 8 data/glitch channels at 100 MHz, (four maximum).
- **91P16 Pattern Generator Module,** 16 channels at 25 MHz, (one maximum).
- **91P32 Pattern Generator Expander Module,** 32 channels at 25 MHz, (two maximum).

MODES OF OPERATION

DATA ACQUISITION

Operating as a logic analyzer, the DAS can acquire up to 104 channels of parallel data. The number of acquisition channels, along with clock and trigger functions, is a direct result of the number and type of data acquisition modules installed in the mainframe.

Using one to three 91A32 modules, the DAS acquires and stores from 32 to 96 input channels with 2 to 6 clock qualifiers. In this mode, all modules may be run from the same internal clock (set at intervals ranging from 5 ms to 40 ns), or from the same external clock's rising or falling edge (set to 40 ns maximum). A special split-clock feature is also provided for setting each 91A32 module to a different external clock, such as those belonging to multiplexed bus structures. Three word recognizers may be specified on all channels and used in several different triggering sequences.

Using one to four 91A08 modules, the DAS acquires and stores from 8 to 32 input channels with 1 to 4 clock qualifiers. All modules may run at a 100 MHz maximum clock rate using the DAS internal clock or an external clock's rising or falling edge. The 91A08 modules also acquire and store glitches on all data channels. Word recognition can be set to trigger on data or glitches.

Two modes are provided for using the 91A32 and 91A08 modules together. The AND mode runs the modules simultaneously using the clock and word recognizer functions of the 91A32 module(s). The ARMS mode runs the two modules simultaneously, but at different clock rates. In this mode, the 91A32 trigger enables the 91A08 trigger to produce a display effect similar to an oscilloscope's delayed sweep.

In all acquisition modes, triggering may be positioned at the beginning, center, or end of the acquisition memory; or it may be delayed for up to 32,767 clock cycles. BNC connectors on the mainframe's back panel also provide a trigger output and a trigger enable signal.

ACQUISITION AND REFERENCE MEMORY DISPLAY

Once in memory, acquired data is displayed in either Timing Diagram or State Table format.

In the Timing Diagram format, the DAS displays data in logic waveforms representing the high and low states of each clock cycle. Up to 16 of these waveforms are displayed at one time. Screen editing functions are available for viewing different portions of memory, for labeling and rearranging channel orders, and for altering display magnification. The Timing Diagram also displays 91A08 glitch information.

In the State Table format, data is displayed in hexadecimal, octal, or binary radices. Up to 16 data words appear on the screen at one time, with channel widths as wide as 104 bits. Up to 256 mnemonic definitions can be specified and incorporated into the display. As with the Timing Diagram, screen editing functions are provided for moving, modifying, or reformatting the display.

DAS reference memory is also displayed in hexadecimal, octal, or binary radices. Data may be loaded into reference memory from acquisition memory. Reference memory and newly acquired data appear on the screen as two adjacent tables. Any difference in bit values is highlighted on the acquisition memory portion of the display. Bit masking and editing functions are provided for altering reference memory to represent any desired bit values.

PATTERN GENERATION

When used as a pattern generator, the DAS outputs clock, data, and strobe signals to a system under test. The 91P16 module provides 2 clock output lines, 16 data output lines, and 2 strobe lines. The addition of one or two 91P32 expander modules increases the output to 6 clock lines, 48 data output lines, and 6 strobe lines; or to 10 clock lines, 80 data output lines, and 10 strobe lines.

The output clocks and data signals run from the master pattern generator clock (25 MHz maximum). The master clock can be supplied by the DAS internal clock or by an external clock source.

Data output is synchronous to the clock edge. The data program may be entered in hexadecimal, octal, or binary radices. Special commands are available for compressing this direct in-line code through the use of call, return, goto, repeat, hold, and count functions.

Strobes are programmed asychronously, on a cycle-by-cycle basis, and may be asserted in positive- or negative-true formats. Their leading and trailing edges may be positioned independently.

The pattern generator also responds to external input signals. It accepts external interrupt, pause, or inhibit signals. This allows interactive communication with the system under test.

GPIB, RS-232, AND HARD COPY INTERFACES

All DAS test operations may be extended through the use of the GPIB, RS-232, and hard copy interfaces included in the I/O Interface assembly (mainframe Option 02).

The GPIB interface allows parallel data transmission between the DAS and any compatible host controller. The DAS can function as a talker and listener in a GPIB network; the host controller controls all menu setup and test functions.

The RS-232 interface allows two DAS systems to be linked together for master/slave transmission. The master DAS serves as the controller for setting up and operating another DAS in a remote location. The RS-232 interface can also be used for transmitting GPIB commands.

A composite video output for hard copy units or video terminals is the third interface provided by Option 02. This feature allows documentation of test results and operating parameters.

TAPE DRIVE

The tape drive (mainframe Option 01) may be used to store specific DAS setups on a magnetic tape. You can store the entire instrument status or selected portions of the instrument status, and then restore that information to the DAS at any time.

MAINFRAME STANDARD COMPONENTS

Refer to Figure 1-1 for the position of mainframe components, available modules, and options. All probes connect through back-panel openings.

Keyboard — a functionally encoded keyboard located on the front of the mainframe. When lowered, this unit serves as the operator's interface. Keystrokes are provided for calling up the menus, for entering operating parameters, and for starting or stopping the test functions.

When folded, the keyboard serves as a protective front cover.

Display Monitor — a 9-inch raster scan CRT with 24, 80-character lines of display. The monitor displays the various DAS menus and provides highlighted, reverse video, and blinking screen prompters. The DAS9129 color monitor also features a color-coded display using green, yellow, and red.

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Interconnect Board — an etched circuit board fixed at the bottom of the mainframe. This board provides the module bus slots used for installing data acquisition and pattern generator modules. The board holds the Controller Module, the Trigger/Time Base Module, and up to six data acquisition or pattern generator modules.

Main Power Supply — an etched circuit board providing the power needed for all mainframe components except module bus slots 1-6. The Main Power Supply provides all operating power for the module bus slots occupied by the Controller and Trigger/Time Base Modules (slots 0 and 7). Operating power for the other six slots is provided by additonal +5 V Power Supply modules.

+5 V Power Supply — a plug-in circuit module providing all operating power for two contiguous module bus slots. If more than two modules are to be used, more power must be added as specified under mainframe Options 03 and 04.

Controller — a plug-in circuit module containing the system's Z80 microprocessor, firmware, and memory. It communicates over a 72-pin CPU bus on the interconnect board and controls all system modules including the keyboard and monitor interfaces and the tape drive unit.

Trigger/Time Base — a plug-in circuit module with one P6452 Data Acquisition Probe used as an external clock probe. This module performs two basic functions: it determines the occurrence of a specified trigger sequence and then generates an acquisition stop/store signal. It also provides the intrnal or external clock sources required by any installed data acquisition or pattern generator modules.

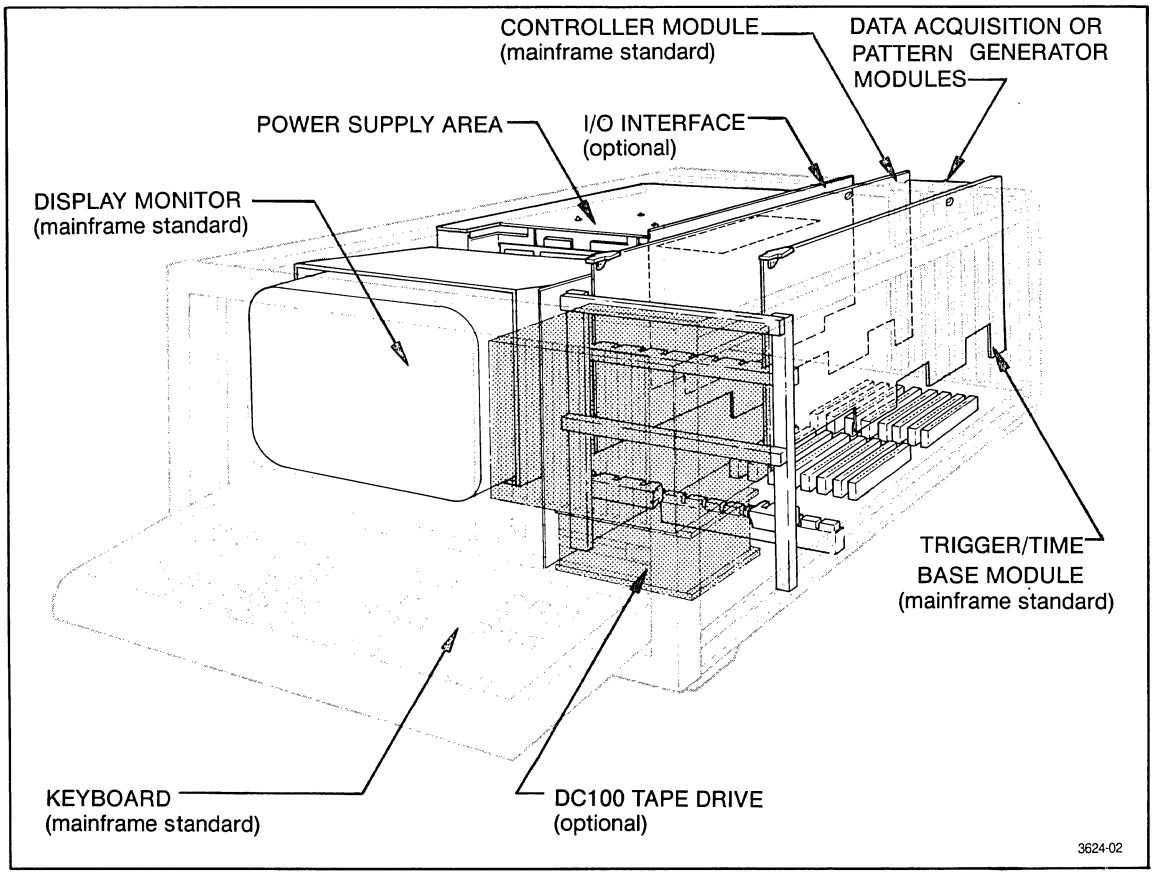

Figure 1-1. DAS9109 Mainframe configuration.

INSTRUMENT MODULES

Module installation procedures are provided in Disassembly/Installation Procedures in the Maintenance: General Information section.

91A32 Data Acquisition Module — The 91A32 features acquisition rates up to 25 MHz with 32 data input lines and two clock qualifiers. It has a 32-channel memory width and a 512-word depth (three 91A32 modules maximum).

91A08 Data Acquisition Module — The 91A08 features acquisition rates up to 100 MHz with 8 data/glitch channels and one clock qualifier. It has separate data and glitch memories, both of which have an 8-channel memory width and 512-word depth (four 91A08 modules maximum).

91P16 Pattern Generator Module — The 91P16 features 16 data output lines, 2 clock output lines, and 2 strobe lines. It outputs at rates up to 25 MHz and has the capability to respond to external interrupt, inhibit, and pause lines (one 91P16 module maximum).

91P32 Pattern Generator Expander Module — The 91P32 works in conjunction with the 91P16 to provide 32 additional data output lines, four clock output lines, and four strobe lines (two 91P32 modules maximum).

NOTE

The 91P32 modules are operable only if a 91P16 module is installed in the mainframe.

MAINFRAME OPTIONS

All of the following options, except the tape drive, may be installed by qualified service personnel in accordance with the instructions contained in the Disassembly/Installation Procedures.

OPTION 01, Tape Drive for DC100-type Cartridges — resides in a reserved space in the right-front of the mainframe. Its recording medium is a DC100-type tape cartridge inserted into the driver through a slot on the mainframe's front panel. This unit will store and recall DAS status, menu parameters, and reference memories.

DAS91F1 is the field-installable version of Option 01. DAS91F1 must be installed at a Tektronix Field Service Center.

OPTION 02, I/O Interface — a plug-in circuit module providing GPIB, RS-232, and hard copy interfaces. Included with this option is a back panel insert with appropriate connectors for each interface.

DAS92F2 is the field-installed version of Option 02 for the DAS9129 (color) Mainframe. DAS91F2 is the field-installable version of Option 02 for the DAS9109 (monochrome) Mainframe. DAS92F2 and DAS91F2 may be installed by any qualified service technician.

OPTION 03, One +5 V Power Supply — a plug-in circuit module providing operating power for two contiguous module bus slots. By combining this module with the power supplies provided with the mainframe, six of the eight bus slots receive operating power.

OPTION 04, Two +5 V Power Supplies — two plug-in circuit modules providing operating power to four module bus slots. By combining these modules with the power supplies provided with the mainframe, all eight of the bus slots receive power.

OPTION 05, Rackmount Hardware

OPTION A1, European Plug, 220 V/16A

OPTION A2, United Kingdom Plug, 240 V/13A

OPTION A3, Australian Plug, 240 V/10A

OPTION A4, North American Plug, 240 V/15A

STANDARD AND OPTIONAL ACCESSORIES

MAINFRAME

Standard Accessories

The following items are provided with any DAS mainframe, whether ordered separately or as part of a preconfigured system.

1	062-5847-01	DAS 9100 Series Operator's Manual
1	010-6452-01	P6452 Data Acquisition Probe (with clock cable attached)
1	012-1000-00	Diagnostic lead set (10 in.)
1	214-3154-00	Ejector, circuit board

Optional Accessories

062-5848-01	DAS 9100 Series Service Manual, Vol. I, II, and III.
119-1350-01	Tape Cartridges, DC100-Type; package of 5
012-0630-01	Interconnect Cable (2-meter GPIB cable)
012-0630-02	Interconnect Cable (4-meter GPIB cable)
012-0815-00	Interconnect Cable (2-meter RS-232 cable)
012-0820-00	Interconnect Cable (null modem)
012-0074-00	Cable Assembly (75 Ω coaxial, 42 in., for hard copy unit)
175-2753-00	Cable Assembly (75 Ω coaxial, 120 in., for hard copy unit)
067-0980-00	DAS Service Maintenance Kit
067-1037-00	Setup/Hold Time Test Fixture

91A32 DATA ACQUISITION MODULE

Standard Accessories

1	070-3627-00	91A32 Instructions

Optional Accessories

There are no optional accessories to the 91A32 module.

91A08 DATA ACQUISITION MODULE

Standard Accessories

1	070-3612-00	91A08 Instructions
1	012-0987-00	Flying lead set (5 in.)
1	012-0989-00	Ground (or V_L) sense lead (5 in. with Pomona hook tip)

Optional Accessories

There are no optional accessories to the 91A08 module.

91P16 PATTERN GENERATOR MODULE

Standard Accessories

1	070-3613-00	91P16 Instructions
2	010-6455-01	P6455 TTL/MOS Pattern Generator Probes with tips and leads

Optional Accessories

There are no optional accessories to the 91A08 module.

91P32 PATTERN GENERATOR EXPANDER MODULE

Standard Accessories

1	070-3614-00	91P32 Instructions

Optional Accessories

There are no optional accessories to the 91A08 module.

P6452 DATA ACQUISITION PROBE

Standard Accessories

1	070-3615-00	P6452 Instructions
1	012-0747-00	Flying lead set (10 wide, 10 in.)
1	020-0720-00	Grabber tips; package of 12
1	012-0989-00	Ground (of V_L) sense lead (5 in. with Pomona hook tip)
1	334-4174-00	External Clock Probe label
1	343-1048-00	Flat cable mounts

Optional Accessories

012-0987-00	Flying lead set (10 wide, 5 in.)
012-0800-00	Harmonica lead set (10 wide, 10 in.)
012-0968-00	Harmonica lead set (10 wide, 5 in.)
012-1000-00	Diagnostic lead set (10 in.)
012-0989-01	Ground (or V_L) sense leads (5 in. with Pomona hook tips); package of 10
103-0209-00	GPIB adapter
003-0709-00	DIP clip, IC (16-pin test clip)
015-0330-00	Test clip adapter (16 DIP, 30 cm, low profile)
015-0339-02	Test clip adapter (40 DIP, 10 cm, low profile)
015-0339-00	Test clip adapter (40 DIP, 30 cm, low profile)
012-1012-00	Probe extender cable (2 meters)

P6454 100 MHz CLOCK PROBE

Standard Accessories

1	070-3837-00	P6454 Instructions
1	195-3659-00	Lead with grabber tip; package of 2

Optional Accessories

195-2234-06	High-speed hook tips (DIP); package of 10
195-1943-06	High-speed hook tips (flat pack); package of 10

P6455 TTL/MOS PATTERN GENERATOR PROBE

Standard Accessories

1	070-3616-00	P6455 Instructions
1	012-1053-00	Patttern generator lead set
1	020-0720-00	Grabber tips; package of 12
1	012-0989-00	Ground (or V_L) sense lead (5 in., black, with Pomona hook tip)
1	012-0990-00	Ground (or V_H) sense lead (5 in., green with Pomona hook tip)
1	343-1048-00	Flat cable mounts

Optional Accessories

012-0747-00	Flying lead set (10 wide, 10 in.)
012-1000-00	Diagnostic lead set (10 in.)
012-0989-01	Ground (or V_L) sense leads (5 in., black, with Pomona hook tips); package of 10
012-0990-01	Ground (or V_H) sense leads (5 in., green, with Pomona hook tips); package of 10
012-1012-00	Probe extender cable (2 meters)

P6456 ECL PATTERN GENERATOR PROBE

Standard Accessories

1	070-3753-00	P6456 Instructions
1	012-0926-00	Pattern generator lead set (9 in.)
1	012-1001-00	High-speed pattern generator lead set (10 wide, 5 in., harmonica)
1	020-0720-00	Grabber tips; package of 12
1	012-0989-00	Ground (or V_L) sense lead (5 in., black, with Pomona hook tip)
1	012-0990-00	Ground (or V_H) sense lead (5 in., green with Pomona hook tip)
1	343-1048-00	Flat cable mounts

Optional Accessories

012-1000-00	Diagnostic lead set (10 in.)
012-0989-01	Ground (or V_L) sense leads (5 in., black, with Pomona hook tips); package of 10
012-0990-01	Ground (or V_H) sense leads (5 in., green, with Pomona hook tips); package of 10
012-1012-00	Probe extender cable (2 meters)

SPECIFICATIONS

MAINFRAMES

Table 1-1
DAS9129 and DAS9109 Electrical Specifications: Mainframe Power

Characteristic	Performance Requirements	Supplemental Information
MAIN POWER SUPPLY BOARD		
Primary Power Input		90 V to 132 V (Low) or 180 V to 250 V (High), 48 to 63 Hz, Single Phase 1000 VA max, 10 A max.
Power Supply Clock		Typically 4 μs high, 25 μs low. Period approximately 29 μs.
V_H levels		From 0 to 3.25 V
V_L levels		From 3.25 V below 11.3 V supply up to the 113.5 V supply.
Internal Power		
+12 V Supply		
Voltage	+12 V, ±1.5%	
Ripple	120 mV, max., p-p	
Current		0.85 A min., 6.0 A max.
Overload Protection		Current limited above 6 A and below 12 A
Over-voltage Protection		Above 14 V, below 18 V
+5 V Supply		
Voltage	+5 V, ±3.0%	
Ripple	50 mV, max., p-p	
Current		8.0 A
Overload Protection		Current limited above 8 A and below 14 A
Over-voltage Protection		Above 5.4 V, below 6.6 V
+6 V Supply		
Voltage	+6 V, ±3.0%	
Ripple	60 mV, max., p-p	

Table 1-1 (cont)

Characteristic	Performance Requirements	Supplemental Information
MAIN POWER SUPPLY BOARD		
Current		2 A
Overload Protection		Current limited above 2 A and below 4 A
Over-voltage Protection		Above 6.3 V, below 7.7 V
−5 V Supply		
Voltage	−5 V, ±3.0%	
Ripple	50 mV, max., p-p	
Current		4.0 A
Overload Protection		Current limited above 4 A and below 8 A
Over-voltage Protection		Above −5.4 V, below −6.6 V
−12 V Supply		
Voltage	−12 V, ±10.0%	
Ripple	120 mV, max., p-p	
Current		0.75 A
Overload Protection		1.5 A fuse
−12 V Supply		
Voltage	−12 V, ±5.0%	
Ripple	120 mV, max., p-p	
Current		0.035 A
Overload Protection		Internal shutdown
Over-voltage Protection		79L12AC – three terminal regulator
+11.3 V Supply		
Voltage		+11.3, +15%, −0%
Ripple		250 mV, max., p-p
Current		0.5 A
Overload Protection		None
Over-voltage Protection		For +5 V Power Supply Modules only

Table 1-1 (cont)

Characteristic	Performance Requirements	Supplemental Information
+5 V POWER SUPPLY MODULE		
Input Power		±160 V unregulated @ 0.8 A +5.0 V ref @ <2 mA +11.3 V unregulated @ 50 mA
Output Power		
Voltage	+5.0 V, ±3%	
Ripple	50 V, max., p-p	
Current		18 A, max., cont. 1.0 A, min.
Overload Protection		Current limited above 18 A and below 25 A
Over-voltage Protection		Above 5.2 V, below 6.3 V

Table 1-2
DAS9129 ELECTRICAL SPECIFICATIONS: COLOR DISPLAY MONITOR

Characteristic	Performance Requirements	Supplemental Information
Power Requirement		20 W; +12 V @ ≤1.8 A +5 V @ ≤0.2 A
Monitor Internal Supply Voltages		+110 V nominal (+104 V to +116 V) +24 V nominal (+22.6 V to +25.4 V) −10 V nominal (−9.6 V to −10.4 V0
Screen Area		44 sq. in. (9 in. diagonal)
Phosphor	Red, Green, Yellow	
Signal Inputs	MPSCK, CSUNC, VSYNC video: RED, GREEN, YELLOW	MPSCK: Monitor Power Supply Clock CSYNCL: Horizontal sync for color monitor only

Table 1-2 (cont)

Characteristic	Performance Requirements	Supplemental Information
Input Levels		LSTTL, High True except MPSC which is Low True
Input Impedance		CSYNC: LSTTL, 2 loads VSYNC: >1.5 kΩ MPSCK: LSTTL, 2 loads RED, GREEN, YELLOW: 1 TTL load each
Pulse Rise Time	35 ns max	
Color Balance		Yellow-on-red matches the color of the yellow phosphor.
		Green brightness matches the yellow brightness on reverse video areas.
Characters		Characters shall be readable and located within the uniform area of the raster.
Resolution		.30 mm phosphor-dot, triad spacing
Geometric Distortion		Vertical or Horizontal Edge Bowing ≤0.03 inches.
High Voltage		21 kV nominal
Horiz Blanking Interval		12 μs nominal
Scanning Frequency		Horiz, 15,750 hz, ±500 Hz; Vert, 60 Hz, ±3.2%
Internal Adjuistments		Red, yellow, green brightness; intensity range; vertical position; horizontal, vertical size; focus
External Adjustments		Intensity

Table 1-3
DAS9109 Electrical Specifications: CRT Monochrome Display Monitor

Characteristic	Performance Requirements	Supplemental Information
Power Requirement		+12 V dc @900 mA
Screen Area		44 sq. in. (9 in. diagonal) 24 x 80 characters
Phosphor		P4
Signal Inputs		Separate video, horizontal and vertical sync
Input Levels		TTL (2.5 to 5.0 V p-p), sync positive at input
Input Impedance		75 Ω video; >2 kΩ sync
Video Response		Within 3 dB, 10 Hz to 12 MHz
Pulse Rise Time		20 V rise in 40 ns
Resolution		650 lines center, 500 lines corners
Geometric Distortion		<2%, measured with std. EIA ball chart and dot pattern
High Voltage		9.5 kV @ 50 μA beam current, nominal
Horiz Blanking Interval		11.0 μs min. (includes retrace and delay)
Scanning Frequency		Horiz, 15,750 Hz, ±500 Hz; Vert, 50/60 Hz
Internal Adjustments		Brightness, vertical size, vertical linearity, horizontal hold, vertical hold, contrast, focus, horizontal width, S-shaping, video bias
External Adjustments		Brightness control and Degauss switch

Table 1-4
DAS9129 and DAS9109 Electrical Specifications: Keyboard

Characteristic	Performance Requirements	Supplemental Information
Mainframe-to-Keyboard Signals		
Operating Power		+12 V, ±5% @ 110 mA, max. −12.0 V, ±8% @ ≤10 mA, max.
Keyboard-to-Mainframe Signals		
Data Bus		7-bit TTL, high-true
Keydown Signal		TTL Level, low-true
Key-Down Sense Delay		800 ms

Table 1-5
DAS9109 Electrical Specifications: Controller Module

Characteristic	Performance Requirements	Supplemental Information
Operating Power Required		+12 V, ±5% @ 100 mA Max. +5 V, ±3% @ 2.0 A Max. −5 V, ±3% @ 10 mA Max. −12 V, ±10% @ 10 mA Max.
DAS9129 Output Drive Signals (exclusive of bus signals)		Separate red, green, yellow video; horizontal Sync; Vertical Sync; CSYNC; MPSCK
Internal Adjustments		Horiz position (affects CSYNC only)
DAS9109 Output Drive Signals (exclusive of bus signals)		Separate video, horizontal sync, and vertical sync
Bus Signal Levels		TTL (2.5 V to 5.0 V, p-p), positive logic
Output Impedance of Video Output		75 Ω
Refresh Rate		60 (±2) frames per Second
Screen Buffer memory Size		1920 x 8 bits

Table 1-5 (cont)

Characteristic	Performance Requirements	Supplemental Information
Character Generation		
Character Matrix		5 x 7 character, 6 x 10 block
Characters per Line		80
Lines per Screen		24
Character and Waveform Sets		(See Figure 1-2)
Attributes		Highlight, blink and reverse video
Cursor		Blinking reverse-video block
Color Attributes (DAS9129 Only)		Yellow on red background; green, inverse green; yellow, inverse yellow, blink any color

Table 1-6
DAS9129 DAS9109 Electrical Specifications: Trigger/Time Base Module

Characteristic	Performance Requirements	Supplemental Information
Operating Power Required		+12 V, ±5% @ 50 mA Max. +6 V, ±5% @ 75 mA Max. +5 V, ±3% @ 3.5 A Max. −5 V, ±5% @ 170 mA Max. −12 V, ±10% @ 50 mA Max.
Power (from Mainframe) Output to External Clock Probe		+5 V, ±5% @ 700 mA −5 V, +5% @ 100 mA
Word Recognizer Output		
Output level		TTL
Propagation delay		53 ns, ±10 ns
Cycle delay		Output signal occurs 3 clock cycles after word is clocked in at probes
Trigger Enable Input		
Triggering level		TTL
Setup time		50 ns min.

DAS 9100 CHARACTER SET CONVERSION

Hexadecimal	ASCII	Character Set	Waveform	Hexadecimal	ASCII	Character Set	Waveform	Hexadecimal	ASCII	Character Set	Waveform	Hexadecimal	ASCII	Character Set	Waveform
20				30	0	0		40	@	@		50	P	P	
21	!	!		31	1	1		41	A	A		51	Q	Q	
22	"	"		32	2	2		42	B	B		52	R	R	
23	#	#		33	3	3		43	C	C		53	S	S	
24	$	$		34	4	4		44	D	D		54	T	T	
25	%	%		35	5	5		45	E	E		55	U	U	
26	&	&		36	6	6		46	F	F		56	V	V	
27	'	'		37	7	7		47	G	G		57	W	W	
28	(	(		38	8	8		48	H	H		58	X	X	
29	)	)		39	9	9		49	I	I		59	Y	Y	
2A	*	*		3A	:	:		4A	J	J		5A	Z	Z	
2B	+	+		3B	;	;		4B	K	K		5B	[	[	
2C	,	,		3C	<	<		4C	L	L		5C	\	\	
2D	–	–		3D	=	=		4D	M	M		5D	]	]	
2E	.	.		3E	>	>		4E	N	N		5E	^	^	
2F	/	/		3F	?	?		4F	O	O		5F	-	_	

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Figure 1-2. Character and Waveform Sets.

Table 1-6 (cont)

Characteristic	Performance Requirements	Supplemental Information
Cycle Offset		This trigger is enabled from the fifth data word preceding this clock cycle that the Trigger Enable Input is received.
Trigger "Event 1" Occurrence Counter		1 Count, min.; 32,767 Counts, min.;
Delay Counter		1 Count, min.; 32,767 Counts, max.
91A32 Internal Clock	5 ms to 40 ns, ±1%, ±1 ns	
91A08 Internal Clock	5 ms to 10 ns, ±1%, ±1 ns	
External clock Inputs:		
Pulse Period	40 ns, min.	
Pulse High	19 ns, min.	
Pulse Low	19 ns, min.	
Probe-to-module Signals		9 channels, identify, pod presence, and MOS status
Channel Signal Characteristics		Differential ECL V_{cc} = +5 V, V_{ee} = Gnd
Channel Rise/Fall Time		<3 ns 20% to 80%
Identify Pod Precence, and MOS Status		Ground-true, normally open
Module-to-Probe Signals		
Threshold Reference Voltage (VTHLD)		For clocks and control signals
Fixed (TTL)		+1.4 V
Variable (VAR)		−2.5 V to +5.0 V in 50 mV steps
Auxiliary (MOS)		−10 V to +20 V in 200 mV steps Selected by slide switch on probe in AUX position
TTL and VAR Threshold Accuracy (at Module Output)	(Menu-selected value) (−0.25) ±1%, ±5 mV	
MOS Threshold Accuracy (at Module Output)	(Menu-selected value) (−1) ±3%, ±20 mV	

Table 1-6 (cont)

Characteristic	Performance Requirements	Supplemental Information
TTL and VAR Threshold Accuracy (to input of attached probe		Menu-selected Value ±(2% ±100 mV)
MOS Threshold Accuracy (to input of attached probe)		Menu-selected Value ±(4% ±160 mV)

Table 1-7
DAS9129 and DAS9109 Environmental Specifications

Characteristic	Description
Temperature	
Operating	0°C to +50°C
Storage	−40°C to +65°C
Humidity	Class 5 with the following exception: before applying power, the mainframe must reside in ≤70% RH for two hours.
Altitude	
Operating	4.06 km max. (15,000 ft.) – DAS9129; 3.07 km max. (10,000 ft.) – DAS9109
Storage	15 km max. (50,000 ft.)
Vibration	0.37 mm (.015 in.) @ 10 to 45 Hz
Shock	30 g.

Table 1-8
DAS9129 and DAS9109 Physical Specifications

Characteristic	Description
Weight (w/o Accessories)	230.13 kg (51 lbs.) – DAS9129; 21/77 kg (48 lbs.) – DAS9109.
Finish	Earth brown and ivory gray
Overall Dimensions	See Figure 1-3
Instrument Module Compartment (bus slots)	Must accommodate 8 modules of size shown in Figure 1-4
Power Module Compartment	Must accommodate 3 modules of size shown in Figure 1-5

91A32 DATA ACQUISITION MODULE

Table 1-9
91A32 Electrical Specifications: Power

Characteristic	Performance Requirements	Supplemental Information
Operating Power Required		+12 V, +1.5% @ 700 mA max. +5 V, ±3% @ 6.5 A max. −12 V, ±10% @ 50 mA max.
Power (from mainframe) Output To Each Of Four Probes		+5 V, ±5% @ 700 mA −5 V, ±5% @ 100 mA

Table 1-10
91A32 Electrical Specifications: Data Acquisition and Storage

Characteristic	Performance Requirements	Supplemental Information
Maximum Sampling Rate	25 MHz with internal or external clock (40 ns cycle time)	20 Mhz with Qualifiers enabled
Acquisition Memory		
Memory Depth		512 words
Memory Width		32 channels data (1 module, 4 probes); expandable to 96 channels data (3 modules, 12 probes)
Data Set-up (period data valid prior to external clock edge)	29 ns, min. with data acquisition probe attached	
Data Hold (period data valid beyond external clock edge)	0 ns, min. with data acquisition probe attached	
Storage Qualifiers		2 per module (6 max. with 3 modules)
Qualifier Polarity		Selectable: pos or neg
Qualifier Set-up Time	29 ns, min. with data acquisition probe attached	
Qualifier Hold Time	0 ns, max. with data acquisition probe atached	
Clock		Clock is actually a function of the mainframe Trigger/Time Base Module
Source		Selectable from one internal and three external sources through the Trigger/Time Base. With external clock selected, at least one 91A32 module must be using CLK1. CLK1 is acquired through the External Clock Probe.
Clock Polarity (external)		Selectable: rising or falling edge
Clock Period (internal)		Selectable: 40 ns, or 50 ns through 5 ms in 16 steps (1-2-5 sequence) or off
Minimum External Clock Pulse Inputs:		
Pulse Period	40 ns, min.	
Pulse High	19 ns, min.	
Pulse Low	19 ns, min.	

Table 1-11
91A32 Electrical Specifications: Clock and Trigger

Characteristic	Performance Requirements	Supplemental Information
Trigger		
Trigger Types		Trigger is actually a function of the mainframe's Trigger/Time Base Module. 1, 2, and 3-level word recognition and pattern-sequence comparison
Word Recognizers		Three: "Event 1", "Event 2", and "Event 3"
Recognizer Word Width		Same as memory width
Recognizer Bit Condition Selection		Logic 1, logic 0, or X (don't care)
Trigger Position		BEGIN, CENTER, END, and DELAY. In DELAY mode the 91A32 trigger sequence number is assigned as follows: Trigger sequence = 504-DELAY value. P/O Trigger/Time Base Module
Stop-store Delay		Selectable from 1 to 32,767 sample periods after trigger
Pattern Sequence Comparison		Compare until equal or until not equal
Pattern Sequence Length		From 1 to 512 words
Trigger Modes		
91A32 and 91A08		Must have both 91A32 and 91A08 modules in the system. The 91A08 Qualifier is disabled. "Event 2" and "Event 3" trigger words are not supported on the 91A08 module. The 91A08 is restricted to the specifications of the 91A32, with the following exception: in AND mode the 91A08 module has a hold time of 20 ns. In the AND mode, the 91A08 modules always use the master CLK1 from the External Clock Probe. 91A08 pods cannot be in the same group(s) as 91A32 pods.

Table 1-11 (cont)

Characteristic	Performance Requirements	Supplemental Information
91A32 ARMS 91A08		After 91A32 completes trigger sequence, 91A08 is enabled. 91A32 and 91A08 have no special setup or hold restrictions in this mode. If any qualifiers are enabled in this mode, you will get a separation fence display.
91A32 EXT-SPLIT Clocks		In order for the split clock display to make sense, all clocks used in split mode must run at the same frequency and be phase related. CLK1 defines the cycle boundary. Clocks CLK2 and CLK3 must fall within the cycle times of CLK1. Clocks CLK2 and CLK3 must occur 40 ns prior to the next CLK1 boundary. Each 91A32 module must meet set-up and hold specifications individually. The rightmost 91A32 module in the Trigger specification menu that uses CLK1 is the master 91A32 module. Only 91A32 modules using CLK1 in the same polarity as the master 91A32 may have qualifiers.

Table 1-12
91A32 Electrical Specifications: Probe Interface and Support

Characteristic	Performance Requirements	Supplemental Information
Probe-to-Module Signals		9 channels, identify, pod presence, and MOS status
Channel Signal Characteristics		Differential ECL V_{cc} = +5 V, V_{ee} = gnd
Channel Rise/Fall Time		<3 ns 20% to 80%
Identify, Pod Presence, and MOS Status		Ground-true, normally open
Module-to-Probe Signals		
Threshold Reference Voltage (VTHLD)		For data and qualifiers
Fixed (TTL)		+1.4 V
Variable (VAR)		−2.5 V to +5.0 V in 50 mV steps.
Auxiliary (MOS)		−10 V to +20 V in 200 mV steps. Selected by putting the slide switch on the probe in AUX position
TTL and VAR Threshold Accuracy (at Module Output)	(Menu-selected value) times (−0.25) ±1%, ±5 mV	
MOS Threshold Accuracy (at Module Output)	(Menu-selected value) times (−1) ±3%, ±20 mV	
TTL and VAR Threshold Accuracy (to input of attached probe)		Menu-selected value (±2%, ±100 mV)
MOS Threshold Accuracy (to input of attached probe)		Menu-selected value (±4%, ±160 mV)

91A32 Environmental Specifications

The environmental specifications for this instrument (operating) meet or exceed those specified for the operation of the DAS9129 and DAS9109 Mainframes.

The environmental specifications for this instrument non-operation shall be in accordance with those stated for a Class V instrument in the Tektronix Standard 062-2853-00, including the specifications pertaining to the transportation of the packaged instrument.

91A32 Physical Specifications

The 91A32 Data Acquisition Module consists of components mounted on an etched circuit board. See Table 1-7 and Figure 1-4 for physical specifications.

91A08 DATA ACQUISITION MODULE

Table 1-13
91A08 Electrical Specifications: Power

Characteristic	Performance Requirements	Supplemental Information
Input Power Used by 91A08 Module		+12 V, ±1.5% @ 100 mA max. +6 V, ±3% @ 100 mA max. +5 V, ±3% @ 8 A max. −12 V, ±10% @ 100 mA max.
Input Power (from mainframe) Output To Probe		+5 V, ±5% @ 700 mA, −12V, ±5% @ 100 mA

Table 1-14
91A08 Electrical Specifications: Data Acquisition and Storage

Characteristic	Performance Requirements	Supplemental Information
Maximum Sampling Rate	100 MHz with internal or external clock	66 MHz with qualifiers enabled; 66 MHz with glitch acquisition. Valid from 0°C to 40°C
Acquisition Memory		
Memory Depth		512 words
Memory Width		8 channels data, 8 channels glitch (1 module, 1 probe); expandable to 32 channels glitch (4 modules and 4 probes)

Table 1-14 (cont)

Characteristic	Performance Requirements	Supplemental Information
Data Set-up (period data valid prior to external clock edge)	≤9 ns	Valid from 0°C to 40°C
Data Hold (period data valid beyond external clock edge)	0 ns, max.	
Minimum Glitch Width	7 ns	At threshold
Glitch Set-up (duration glitch trailing edge must occur prior to external clock edge for detection)		11 ns
Storage Qualifiers		1 per module (4 max. with 4 modules)
Qualifier Polarity		Selectable: pos or neg
Qualifier Set-up Time	≤15 ns using one to four 91A08 modules	Valid from 0°C to 40°C
Qualifier Hold Time	0 ns, max, with data acquisition probe attached	

Table 1-15
91A08 Electrical Specifications: Clock and Trigger

Characteristic	Performance Requirements	Supplemental Information
Clock		Clock is actually a function of the Trigger/Time Base Module
Source		Selectable from two internal and 2 external sources (91A32 CLK1 from the Trigger/Time Base module or the 100 MHz Probe)
Clock Polarity (external)		Selectable: rising or falling edge
Clock Period (internal)		Selectable: 10 ns, 20 ns, 40 ns or 50 ns through 5 ms in 16 steps (1-2-5 sequence) or off
Accuracy (internal clock)		Specified rate ±1% ±1 ns

Table 1-15 (cont)

Characteristic	Performance Requirements	Supplemental Information
Trigger		
Trigger Types		Single-level word recognition
Word Recognition		Single-level data-word or glitch-word, externally armable (from 91A32 trigger)
Word Width		Same as memory width
Bit Specification		
Word Recognition		Logic 1 or logic 0, or X (don't care)
Glitch Recognition		Logic 1 or X (don't care)
Trigger Position		BEGIN, CENTER, END, and DELAY. In DELAY mode, the 91A08 trigger sequence number is assigned by the user as follows: trigger sequence = 508 – DELAY value
Stop-store Delay		Selectable from 1 to 32,767 sample periods after trigger
Pattern-sequence Comparison		Compare until equal or until not equal
Pattern Length		From 1 to 512 words
External Clock		Valid for 0°C to 40°C
Pulse Period	10 ns min.	
Pulse High	5 ns min.	
Pulse Low	5 ns min.	
AND Mode Characteristics		
Setup Time		29 ns
Hold Time		20 n
Maximum Clock Rate (Internal or External)		20 MHz (50 ns)
ARMs Mode Characteristics		The 91A08 trigger will be armed within 10 91A32 clock cycles after the occurrence of the 91A32 trigger

Table 1-16
91A08 Electrical Specifications: Probe Interface and Support

Characteristic	Performance Requirements	Supplemental Information
Data Probe-to-Module Signals		9 Channels, identify, pod presence, and MOS status
Channels		8 data/glitch and 1 qualifier
Channel signal Characteristic		Differential ECL $V_{cc} = +5$ v, V_{ee} = gnd
Channel Rise/Fall Time		<3 ns 20% to 80%
Identify Pod Presence, and MOS Status		Ground-true, normally open
Data Module-to-Probe Signals		
Threshold Reference Voltage (VTHLD)		
Fixed (TTL)		+1.4 V
Variable (VAR)		−2.5 V to +5.0 V in 50 mV steps
Auxiliary (MOS)		−10 V to +20 V in 200 mV steps. Selected by slide switch on probe in AUX position.
TTL and VAR Threshold times Accuracy (at module output)	(Menu-selected value) (−0.25) ±1%, ±5 mV	
MOS Accuracy (at module output)	(Menu-selected value) times (−1) ±3%, ±20 mV	
TTL and VAR Threshold Accuracy (to input of attached probe)		Menu-selected value (±2%, ±100 mV)
MOS Threshold Accuracy (to input of attached probe)		Menu-selected value (±4%, ±160 mV)
Clock Signal Characteristic (function of the P6454 100 MHz Clock Probe)		Coaxial shield at +12 V. Center conductor at: $0.75\ V + \frac{\text{input signal}}{10}$

91A08 Environmental Specifications

The environmental specifications for this instrument (operating) meet or exceed those specified for the operation of the DAS9129 and DAS9109 Mainframes.

The environmental specifications for this instrument (non-operation) shall be in accordance with those stated for a Class V instrument in the Tektronix Standard 062-2853-00, including the specifications pertaining to the transportation of the packaged instrument.

91A08 Physical Specifications

The 91A08 Data Acquisition Module consists of components mounted on an etched circuit board. See Table 1-7 and Figure 1-4 for physical specifications.

PATTERN GENERATOR MODULES

Table 1-17
91P16 and 91P32 Electrical Specifications: Power

Characteristic	Performance Requirements	Supplemental Information
Input Power Used by 91P16		+12 V, ±1.5% @ 1.5 A max. +5 V, ±3% @ 9 A max.
Input Power Used by 91P32		+5 V, ±3% @ 9 A max.
Output Power (from mainframe) Output To Each PG Probe		+6 V, ±5% @ 160 mA, max. +5 V, ±5% @ 120 mA, max. −5 V, ±5% @ 230 mA, max.

Table 1-18
91P16 and 91P32 Electrical Specifications: Pattern Data

Characteristic	Performance Requirements	Supplemental Information
Pattern Data Width		16 parallel channels (1 91P16, 2 probes); expandable to 80 channels (1 91P16, 2 91P32's and 10 probes)
Data Channel Skew	⩽10 ns at Probe Output	All data channels will be valid at the probe outputs within 10 ns of each other.
Pattern Compression Techniques		The following instructions are available to specify the sequence of data output: COUNT, REPEAT, HOLD, GOTO, CALL, RETURN, HALT, and ADVANCE

Table 1-18 (cont)

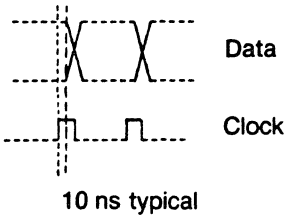
Characteristic	Performance Requirements	Supplemental Information
REPEAT, HOLD, and Data-Increment COUNT		Programmable from 2 to 255 clock cycles
Data-Clock Timing	Data changes a minimum of 2 ns and a maximum of 15 ns after the transition of the selected clock edge	
Maximum Number of Unique COUNT, HOLD, and REPEAT Values		6 total
Maximum Number of nested Subroutines and Interrupts		16
Maximum Number of Labels		32

Table 1-19
91P16 and 91P32 Electrical Specifications: Strobe and Clock Outputs

Characteristic	Performance Requirements	Supplemental Information
Number of Strobes		2 individual strobes (1 module, 2 probes); expandable to 10 strobes (3 modules, 10 probes)
Strobe Start Time		Selectable from 70 ns to 40.910 μs in 40 ns steps
Maximum Pulse Width plus Strobe Delay		40.950 μs
Strobe Pulse Width		Selectable from 40 ns to 40.880 μs in 40 ns steps
Probe Pulse Polarity		Selectable: pos or neg
Strobe Enable Time		First strobe edge must be programmed 70 ns or greater after the beginning of the cycle boundary
Strobe Delay Accuracy	Menu-selected value $\pm$10%, $\pm$6 ns	
Strobe Width	Menu-selected value $\pm$10%, $\pm$6 ns	

Table 1-19 (cont)

Characteristic	Performance Requirements	Supplemental Information
Strobe Trailing Edge Restrictions		The trailing edge of a strobe may not occur any closer to the rising edge of the output clock than: 50 ns ± 10% of the total strobe cycle time
Clock Output		One clock line (rising edge signifies beginning of each cycle)
Clock Output Pulse Width (using internal clock)		⩾14 ns, min.
Clock Output Pulse Width (using external clock)		Input clock pulse width ±6 ns (clock pulse comes from External Clock Probe)
Clock Skew Between Output Clocks of Different Probe Pods Interrupt Minimum Pulse Width		±5 ns

Table 1-20
91P16 and 91P32 Electrical Specifications: Timing

Characteristic	Performance Requirements	Supplemental Information
Operating Rate, RUN Mode		Up to 25 MHz (40 ns cycle time), determined by selected clock
Clock Source		External or internal, menu-selectable
Polarity		Rising or falling edge, menu-selectable
External Clock		
Pulse Period	40 ns, min.	
Pulse High	19 ns, min.	
Pulse Low	19 ns, min.	
Internal Clock		Obtained from Trigger/Time Base Module of the mainframe

Table 1-21
91P16 and 91P32 Electrical Specifications: Input control Signals

Characteristic	Performance Requirements	Supplemental Information
External Clock Input		1 external clock line (edge selectable) 19 ns min. pulse width
Pause Input		1 pause line, selectable high- or low-true (pattern generator maintains current output conditions while pause line remains true). 19 ns minimum pulse width.
Pause Input Hold Time		14 ns. If pause line is held true for 14 ns after the pattern generator External Clock transition, then the next cycle's output data will pause. That is, output data will be held constant and output clocks will stop until the pause line goes false. Typical hold time is 7 ns.
Pause Input Set-up Time Relative to the Pattern Generator External Clock Input		7 ns min. Assert the pause request 7 ns prior to the pattern generator external clock. Typical Value = 0 ns.
Pause Input Set-up Time Relative to the Pattern Generator Clock Output		72 ns min. Assert the pause request 72 ns prior to clock rising edge output. Typical Value = 60 ns.
Pause Input Minimum Pulse Width		19 ns
Interrupt Input		1 interrupt line from External Clock Probe selectable for rising or falling edge assertion.
Interrupt Processing Cycle Delay		4 cycles. When a valid interrupt request is logged in, the first interrupt vector appears at the probe tip in the fourth following cycle unless the instruction on that cycle is a GOTO, CALL, or RETURN. If so, the first interupt vector will not appear until these instructions have been executed.
Interrupt Minimum Pulse Width		19 ns

Table 1-21 (cont)

Characteristic	Performance Requirements	Supplemental Information
Interrupt Input Set-up Time Relative to the Pattern Generator External Clock Input		7 ns min. Assert the interrupt request 7 ns prior to the selected edge of the pattern generator external clock. Typical value = 0 ns.
Interrupt Input Set-up Time Relative to the Pattern Generator Clock		72 ns min. Assert interrupt request 72 ns prior to clock rising edge output. Typical value = 60 ns.
Interrupt latency		4 cycle times. After an interrupt, the pattern generator must begin to execute the interrupt routine without receiving another interrupt. After the interrupt has begun, it is valid to interrupt again. Interrupts sent at an invalid time are ignored.
	NOTE *Inhibit capability may only be used with the P6455 TTL/MOS Pattern Generator Probe.*	
Inhibit Delay Time		70 ns. When the pattern generator external inhibit line is asserted, the pattern generator data outputs will be inhibited or tri-stated a maximum of 70 ns later.
Inhibit Input Minimum Pulse Width		19 ns

Table 1-22
91P16 and91P32 Electrical Specifications: Probe Interface and Support

Characteristic	Performance Requirements	Supplemental Information
Module-to-Probe Signals		10 Channels plus INHIBIT
Signal Characteristic		Differential ECL, V_{cc} = +5 V, V_{ee} = gnd
Probe-to-Module Signals		
Identify Signal and Pod Presence		Ground-true, normally open

91P16 and 91P32 Environmental Specifications

The environmental specifications for this instrument (operating) meet or exceed those specified for the operation of the DAS9129 and DAS9109 Mainframes.

The environmental specifications for this instrument (non-operating) shall be in accordance with those stated for a Class V instrument in the Tektronix Standard 062-2853-00, including the specifications pertaining to the transportation of the packaged instrument.

91P16 and 91P32 Physical Specifications

The 91P16 and 91P32 Pattern Generator Modules consist of components on an etched circuit board. See Table 1-7 and Figure 1-4 for physical specifications.

P6452 DATA ACQUISITION PROBE

Table 1-23
P6452 Electrical Specifications

Characteristic	Performance Requirements	Supplemental Information
Module-to-Probe Signals		
Operating Power Requirement		+5 V, ±5% @ 400 mA, max. (outputs not loaded)
Maximum Input Threshold Control Voltage		±10 V
Probe-to-Module Signals		
Data Channel Signal		Differential ECL, V_{cc} = +5 V, V_{ee} = gnd
Rise/Fall Time	<3 ns, 20% to 80% excursion	
MOS,L		Ground-true, open circuit-false
PODSNS,L		Grounded at probe
IDENT,L		Ground-true, normally open
Input Resistance		1 MΩ, ±1%
Input Capacitance		5 pF nominal, Lead set adds ≈5 to 10 pF
Maximum Non-destructive Input Voltage Range		±40 V peak
Operating Input Voltage Range		From −40 V to input threshold voltage +10 V (+30 V for RS-232 only)

Table 1-23 (cont)

Characteristic	Performance Requirements	Supplemental Information
Small Signal Gain		100 mV input around programmed input threshold yields a minimum gain of 5 (across differential outputs)
Ratio of Input Voltage to Threshold Control Voltage	4:1, ±1%	
Threshold Offset	±80 mV (±40 mV 20°C to 30°C)	
Transit Time of Probe (one channel)		19.5 ns, ±2 ns
Transit Time of Probes (all channels and patterns)		19.5 ns, ±3 ns
Output Impedance		120 Ω nominal (transmission line)

Table 1-24
P6452 Environmental Specifications

Characteristics	Description
Temperature	
Operating	0°C to +50°C
Storage	−55°C to +75°C
Humidity	90% to 95% relative humidity for 5 days cycled from 30°C to 50°C
Altitude	
Operating	4.60 km (15,000 ft)
Non-operating	15 km (50,000 ft)
Vibration	0.64 mm (0.0252 in.) 10 Hz to 55 Hz, 75 minutes
Shock	500 g. (1/2 sine), 1 ms, 18 shocks

Table 1-24 (cont)

Characteristic	Description
Transportation	
Vibration	25 mm (1 in.) at 270 rpm for 1 hour
Package Drop	10 drops from 91 cm (3 ft)
Bench Handling	45° or 4 in. or equilibrium, whichever occurs first
Cables	
Flex Life	1000 cycles at 120° flex with 0.68 kg (1.5 lb) weight
Pull Test	15.88 kg (36 lbs) axial pull at 1 minute duration
Electrical Discharge	10 kV max. from 200 pF with 2 kΩ series resistance

Table 1-25
P6452 Physical Specifications

Characteristics	Description
Finish	Slate Grey
Dimensions (approx):	
POD	See Figure 1-6.
Cable (Flat Ribbon)	2 ms (78.75 in.)
Weight	340 gm (12 oz)

P6454 100 MHz CLOCK PROBE

Table 1-26
P6454 Electrical Specifications
(Includes Circuitry on 91A08 Module)

Characteristic	Performance Requirements	Supplemental Information
Hybrid-to-Module Signals		
Number of Channels	One	
Power Requirements		
Voltage		+12 V, ±5%
Current		≤30 mA
Transconductance		2 mA/V nominal
Bandwidth	150 MHz, min. to -3 dB point	
Propagation Delay		9.2 ns, ±150 ps
Probe Input Impedance		
Input Resistance at Tip of Probe Lead		1 MΩ, ±5%
Input Capacitance		5 pF, ±1 pF
Reference Input Characteristic at Tip		Floating reference input
Maximum Non-destructive Voltage to Either Input		±25 V (dc + peak ac)
Maximum Non-destructive Voltage to V_{ref}		±25 V (dc + peak ac)
Voltage Range		
Operating Input		−4 V to +7 V (dc + peak ac)
Common Mode		−4 V to +7 V (dc + peak ac)
Input Sensitivity	700 mV p-p	700 mV p-p, centered on threshold will provide full ECL swing at output of receiver
Threshold Accuracy	±50 mV, ±3% of threshold setting	
Clock Rise Time/Fall Time (Terminated in 50 Ω to +3 V).		1.0 ns max 20-80% in response to a 700 mV p-p square wave centered about V_{ref} at the output of the comparator
Minimum Input Signal Slew-rate		50 V/μs

Table 1-27
P6454 Environmental Specifications

Characteristic	Description
Temperature	
Operating	0°C to +50°C
Storage	−55°C to +75°C
Humidity	≤95% Relative Humidity
Altitude	
Operating	4.6 km (15,000 ft.)
Non-operating	15 km (50,000 ft.)
Vibration	0.64 mm (0.0252 in.), 10 Hz to 55 Hz, 75 minutes
Shock	500 g. (1/2 sine), 11 ms, 18 Shocks
Bench Handling	45° or 4 in., or equilibrium, whichever comes first
Electrical Discharge	12 kV, max.; 1 kΩ series resistance +500 pF
Transportation	
Vibration	25 mm (1 in.) at 270 rpm for 1 hour
Package Drop	10 drops from 91 cm (3 ft.)
Cables	
Flex Life	10,000 cycles at 120° flex with 0.40 kg (0.882 lb.) weight
Pull Test, Hybrid Pod	4.54 kg (10 lbs.)
Pull Test Connector	4.54 kg (10 lbs.)

Table 1-28
P6454 Physical Specifications

Characteristic	Description
Length	
Probe Tip to Connector	Electrically cut to length
Input Leads	38 mm (1.5 in)
Weight	
Probe Assembly	23 gm (0.81 oz)

P6455 TTL/MOS PATTERN GENERATOR PROBE

Table 1-29
P6455 Electrical Specifications

Characteristic	Performance Requirements	Supplemental Information
Module-to-Probe Signals		
Operating Power Requirement		+6 V, ±5% @ 160 mA, max. −5 V, ±5% @ 200 mA, max. +5 V, ±5% @ 120 mA, max. max. when in AUX mode
Number of Channels		10
Channel Characteristic		Diffenential ECL, V_{cc} = +5 V, V_{ee} = gnd
INHIBIT (tri-state control)		Differential ECL, V_{cc} = +5 V, V_{ee} = gnd
Max Frequency	25 MHz at V_L = 0, V_H = 5 V	
Min Pulse Width		15 ns
Signal Transit Time		21.5 ns, ±5 ns measured with V_H = 5 V, V_L = 0 V with load 1 MΩ, 15 pF
Inhibit, Uninhibit Delay Time		≤10 ns (after transit Time) measured with V_H = 5 V, V_L = 0 V Load: 100 Ω to +2.5 V C ≤15 pF
Probe-to-Module Signals		
INDENT L (identify)		Ground-true, normally open
PODSNS (pod Presence)		Grounded at pod

Table 1-29 (cont)

Characteristic	Performance Requirements	Supplemental Information
User Logic Supply Power to POD		
Logic high (V_H) Range	0 V to +15 V	
Logic low (V_L) Range	−15 V to 0 V	
V_{DIF} (V_H − V_L) Range	3 V to 25 V	
Current Drain	User load current +120 mA, max.	
Maximum Non-destructive Voltages		V_H: ±20 V V_{DIF}: ±25 V V_L: −20 to +5 V
Drive Configurations		
TTL or MOS		Active pull-up and pull-down
Tri-state		High impedance (>100 kΩ)
Output Drive Current		
(for V_{DIF} range)		(3 to 5 V) (>5 to 25 V)
Maximum Source of Sink Current for probe output		20 mA 10 mA
Output Levels		
Logic Low (V_{OL})	<V_L +0.5 with current load of 10 mA, V_L +0.6 V @ 20 mA	
Logic High (V_{OH})	>V_H − 1.6 V with current load of 20 mA	
Short Circuit Protection		Between (V_L +5 V) and V_L −0.5 V) in low state. Between (V_H −5 V) and (V_H +0.5 V) in high state
Output Rise/Fall Time		
TTL and MOS (V_{diff} 5 V to 15 V)		Slew rate >0.5 V per ns, 15 pF load. Measured from 10% – 90% of steady state voltage.
Inhibited Output		
Leakage		<100 μA
Capacitance		10 pF, nominal without lead set. Lead set adds ≈10 pF.

Table 1-30
P6455 Environmental Specifications

Characteristic	Description
Temperature	
Operating	0°C to +50°C
Storage	−55°C to +75°C
Humidity	95% relative humidity for 5 days to 50°C
Altitude	
Operating	4.6 km (15,000 ft.)
Non-operating	15 km (50,000 ft)
Vibration	0.64 mm (0.0252 in.) 10 Hz to 55 Hz, 75 minutes
Shock	500 g. (1/2 sine), 1 ms, 18 shocks
Bench Handling	45° or 4 in. or equilibrium, whichever occurs first
Electrical Discharge	12 kV max. from 500 pF with 1 kΩ resistance
Transportation	
Vibration	25 mm (1 in.) at 270 rpm for 1 hour
Package Drop	10 drops from 91 cm (3 ft.)
Cables	
Flex Life	1000 cycles at 120° flex with 0.68 kg (1.5 lb) weight
Pull Test	15.88 kg (35 lbs) axial pull at one minute duration

Table 1-31
P6455 Physical Specifications

Characteristic	Description
Finish	Slate grey
Dimensions (approx)	
POD	See Figure 1-6
Cable (Flat Ribbon)	2 ms (78.75 in.)
Weight	
Probe	340 gm (12 oz)

P6456 ECL PATTERN GENERATOR PROBE

Table 1-32
P6456 Electrical Specifications

Characteristic	Performance Requirements	Supplemental Information
Module-to-Probe Signals		
Operating Power Requirement		+6 V, +5% @ 100 mA, max. −5 V, ±5% @ 230 mA, max.
Number of Channels		10
Channel Characteristic		Differential ECL, V_{cc} = +5 V, V_{ee} = gnd
Maximum Frequency	25 MHz	
Minimum Pulse Width		15 ns
Signal Transit Time		18.2 ns, ±5 ns measured with V_H = 0 V, V_L = 5 V with load 50 Ω to −2 V, ≤15 pF
Probe-to-Module Signals		
IDENT L (identify)		Ground-true, normally open
PODSNS (pod presence)		Grounded at pod

Table 1-32 (cont)

Characteristic	Performance Requirements	Supplemental Information
User Logic Supply Power to Probe.		
V_H		0 V to 5.5 V
V_L		−5.5 V to 0 V
Maximum Non-Destructive Input		V_H ±15 V V_L ±15 V V_{DIFF} ±10 V
Output Levels		
Logic High (V_{OH})	V_H −0.60 V to V_H −1.00 V	With 50 Ω load to V_H −2 V)
Logic Low (V_{OL})	V_H −1.65 V to V_H −2.00 V	With 50 Ω load to (V_H −2 V)
Current Drain		
V_H		User load +130 mA, max. with V_{DIFF} = 5.2 V, ±5%
V_L		230 mA, max. with V_{DIFF} = 5.2 V ±5%
Protection (output short circuit)		To between (V_H +0.5 V and V_{LH} −0.5 V)

Table 1-33
P6456 Environmental Specifications

Characteristic	Description
Temperature	
Operating	0°C to +50°C
Storage	−55°C to +75°C
Humidity	90% to 95% relative humidity for 5 days to 50°C
Altitude	
Operating	4.6 km (15,000 ft)
Non-operating	15 km (50,000 ft)

Table 1-33 (cont)

Characteristic	Description
Vibration	0.64 mm (0.0252 in.) 10 Hz to 55 Hz, 75 minutes
Shock	500 g. (1/2 sine), 1 ms, 18 shocks
Bench Handling	45° or 4 in. or equilibrium, whichever occurs first
Electrical Discharge	12 kV max. from 500 pF with 1 kΩ series resistance
Transportation	
Vibration	25 mm (1 in.) at 270 rpm for 1 hour
Package Drop	10 drops from 91 cm (3 ft)
Cables	
Flex Life	1000 cycles at 120° flex with 0.68 kg (1.5 lb) weight
Pull Test	15.88 kg (35 lbs) axial pull at one minute duration

Table 1-34
P6456 Physical Specifications

Characteristic	Description
Finish	Slate grey
Dimensions (approx)	
POD	See Figure 1-6
Cable (Flat Ribbon)	2 m (78.75 in.)
Weight	
Probe	340 gm (12 oz)

OPTION 01, TAPE DRIVE ASSEMBLY

Table 1-35
Tape Drive Electrical Specifications

Characteristic	Performance Requirements	Supplemental Information
Power Requirements		
+5 V		Regulated +5 V ±5% @ 660 mA, ripple 10 mV max.
+12 V		Regulated ±3% @18 mA
20 V — 28 V		Unregulated 300 mA avg, 2 A peak (60 ms). This voltage may be offset with respect to gnd if the following conditions are met: V+ must be greater than or equal to +11 V; V− must be less than or equal to 0 V.
Power Dissipation		
Read/Write Speed (25 IPS)		<7
Search Speed (60 IPS)		<11
Standby		<4.25
Cartridge Capacity		160 K bytes
Data Cartridge Data Format		
Characters Per Record		256 8-bit bytes
Recording Method		Duty cycle modulation
Recording Density		
2F		1600 flux reversals/in.
1F		800 flux reversals/in/
1F/2F Ratio	0.75 min.	
Write Current Amplitude		11 mA p-p
Write Current Rise Time	12 μs max.	
Read Output (2F)	18 mV p-p min.	Output into 10 kΩ in parallel with 200 pF
Crosstalk (read to read)		1% max.
Overwrite		<−30 dB

Table 1-35 (cont)

Characteristic	Performance Requirements	Supplemental Information
2 V Reference Supply Gap Detect	2 V, ±7%	
One shot Delay	125 ms, ±12%	
Delay Time At Start of Data	870 ms, ±10%	
Hold Time After Loss Of Data	1.12 ms, ±10%	
Read/Write Characteristics		
Bit Density		533 bpi (1600 flux reversals/in.)
Data Transfer Rate		13.324K bits/sec (tape to electronics)
Effective Data Transfer Rate		1280 bytes/sec assuming no stopping at gaps
Soft Error Rate (recoverable)	<1 error in 10E6 bits read at interface level	
Hard Error Rate (unrecoverable)	<1 error in 10E8 bits read	Combined write/reads
Gap Detect	<1 error in 10E8 bits read	
Error Verification Methods		
Header		Checksum complement
Data		CRC-16 algorithm
Tape Transport		
Drive Type		Digitally controlled servo motor
Drive Method		Single capstan drive on cartridge drive roller
Drive Speed		
Read/Write	25 IPS, ±5% (motor speed 1948 rpm)	Tach freq.: 1.623 kHz, ±0.5%
Search	60 IPS, ±8% (motor speed 4830 rpm)	Tach freq.: 4.025 kHz, ±2%
Start/Stop Time		
Read/Write		30 ms at 25 ips, typical
Fast Fwd/Rev		50 ms at 60 ips, typical

Table 1-35 (cont)

Characteristic	Performance Requirements	Supplemental Information
Start/Stop Distance		
Read/Write		Start: 17, ±2-tach pulses (0.255, ±0.030 in.) Stop: 20, ±5-tach pulses (0.30, ±0.075 in.)
Fast Fwd/Rev		Start: approx. 100 tach pulses or 1.5 in. Stop: approx. 100 tach pulses or 1.5 in.

Table 1-36
Tape Drive Environmental Specifications

Characteristic	Description
Temperature	
Operating	0° to +50°C max. ambient
Storage	−40° to +65°C (without tape)
Vibration	Vibration swept from 10 Hz to 55 Hz to 10 Hz at 1 minute per sweep Vibration 15 minutes in each of three major axes at 0.025 total displacement, holding 10 minutes at major resonance (if none, at 55 Hz). Time is 75 minutes.
Shock	Shock to frame of 50 g. 11 ms duration, 1/2 sine shock pulse.
Altitude	
Operating	Up to 4.60 km (15,000 ft)
Storage	Up to 15 km (50,000 ft)
Humidity (relative)	
Operating	20% to 80% non-condensing
Storage	95% max., without data cartridge
Package Transportation Vibration	39 cm (1 in) at approximately 270 rpm
Package Drop	0.91 m (3 ft)

Table 1-37
Tape Drive Physical Specifications

Characteristic	Description
Dimensions	
Drive Unit	11.5 cm (4.38 in.) wide 8.9 cm (3.5 in.) deep 6.4 cm (2.5 in.) high
Tape Drive Data Board	15.6 cm (6.10 in.) wide 8.3 cm (3.25 in.) deep 1.8 cm (0.7 in.) high
Servo Board	14.1 cm (5.5 in.) wide 7.9 cm (3.1 in.) deep 1.8 cm (0.7 in.) high
Weight	0.68 kg (24 oz) including electronics
Cartridge Insertion Force	0.5 kg to 2.3 kg (1 to 5 lbs.)
Eject Button Activation Force	0.5 kg to 1.4 kg (1 to 3 lbs.)
Capstan Force	400 gm, ±60 gm (14, ±2 oz) (measured between drive motor capstan and cartridge drive wheel)
Read/Write Head	
Type	2 track, single gap per track
Mounting	Perpendicular to tape path within 6 minutes of arc (Alignment is present using optical instruments). Read/Write Head is permanently bonded to tape transport, realignment is not possible.

Table 1-37 (cont)

Characteristic	Description
Status Board	
Hole Detect	1 V min. at TP29 with tape stopped at a hole
TPL Sensor Pulse	2 V p-p min. signal, with 2.5 V dc mean value measured at TP9 and motor running
Cartridge Mounting	Cartridge mounts so it is in contact with the 2 reference points nearest the head and either one of the two points nearest the cartridge entrance of the drive. Proper cartridge location is ensured by latching mechanism that presses cartridge against the four tape transport reference points. The cartridge is also pushed against the two forward reference surfaces.
Cartridge Latching	As cartridge is inserted into tape transport, a pawl is engaged that pulls the latching mechanism into place. When the latching cam goes over the center, a spring forces the mechanism against the cartridge that located it against the mounting surface.
Cartridge Ejection	When the eject button is pushed, latching spring force is removed and the spring on the pawl pushes the cartridge out and resets the mechanism.

OPTION 02, I/O INTERFACE ASSEMBLY

Table 1-38
I/O Interface Electrical Specifications: Power

Characteristic	Performance Requirements	Supplemental Information
Inputs (from mainframe)		
With RS-232 Connected		+5 V, ±5% @ 560 mA +12 V, ±10% @ 16 mA −12 V, ±10% @ 23 mA
Without RS-232		+5 V, ±5% @ 560 mA +12 V, ±10% @ 16 mA −12 V, ±10% @ 15 mA

Table 1-39
I/O Interface Electrical Specifications: RS-232 Lines

Characteristic	Performance Requirements	Supplemental Information
Baud Rates (keyboard select)		300, 600, 1200, 2400, 4800, and 9600 baud
Inputs Pin 3 Received Data		Input impedance; 3 kΩ, $\leq Z_{in}$, $\leq$7 kΩ
Pin 5 Clear To Send		MARK or OFF: -25 V, $\leq V_{in}$, ≤ -3 V
Pin 6 Data Set Ready		SPACE or ON: $+3$ V, $\leq V_{in}$, $\leq +25$ V
Pin 8 Data Carrier Detect		
Outputs Pin 2 Transmitted Data		With load impedance: $R_{load} \geq 3$ kΩ
Pin 4 Request To Send		MARK or OFF: $V_{out} \leq -6$ V
Pin 20 Data Terminal Ready		SPACE or ON: $V_{out} \geq +6$ V
Other Pin 1 Ground		Case ground
Pin 7 Signal Ground		Instrument ground

Table 1-40
I/O Interface Electrical Specifications: GPIB Signals

NOTE

The electrical specifications of this interface conform to the electrical specifications contained in the IEEE 488-1978, "Standard Digital Interface for Programmable Instrumentation."

Table 1-41
I/O Interface Electrical Specifications: Composite Video

Characteristic	Performance Requirements	Supplemental Information
V_{on}		1.4 V to 1.6 V, nominal 1.5 V
V_{off}		0.3 V to 0.7 V, nominal 0.5 V
V_{sync}		0 V to 0.1 V, nominal 0 V
T_{hsync}		63.5 μs, $\pm$0.1 μs
T_{vsync}		16.5 ms, $\pm$0.1 ms

I/O Interface Environmental Specifications

The environmental specifications for this instrument (operating) meet or exceed those specified for the operation of the DAS9129 and DAS9109 Mainframes.

The environmental specifications for this instrument (non-operating) shall be in accordance with those stated for a Class V instrument in Tektronix Standard 062-2853-00, including the specifications pertaining to the transportation of the packaged instrument.

I/O Interface Physical Specifications

The DAS Option 02 I/O Interface Assembly is made up of two etched circuit boards and cabling. One board plugs into the DAS Interconnect board and the other mounts on the DAS rear panel. See Figure 1-7 for physical dimensions.

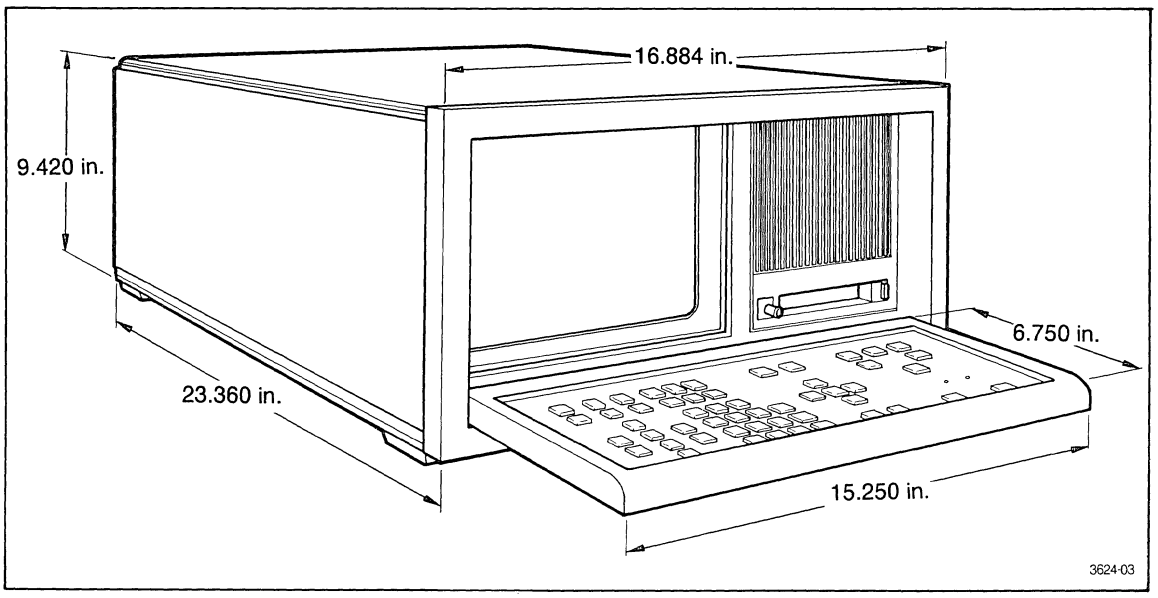


Figure 1-3. Overall dimensions of the DAS9129 and DAS9109 Mainframes.

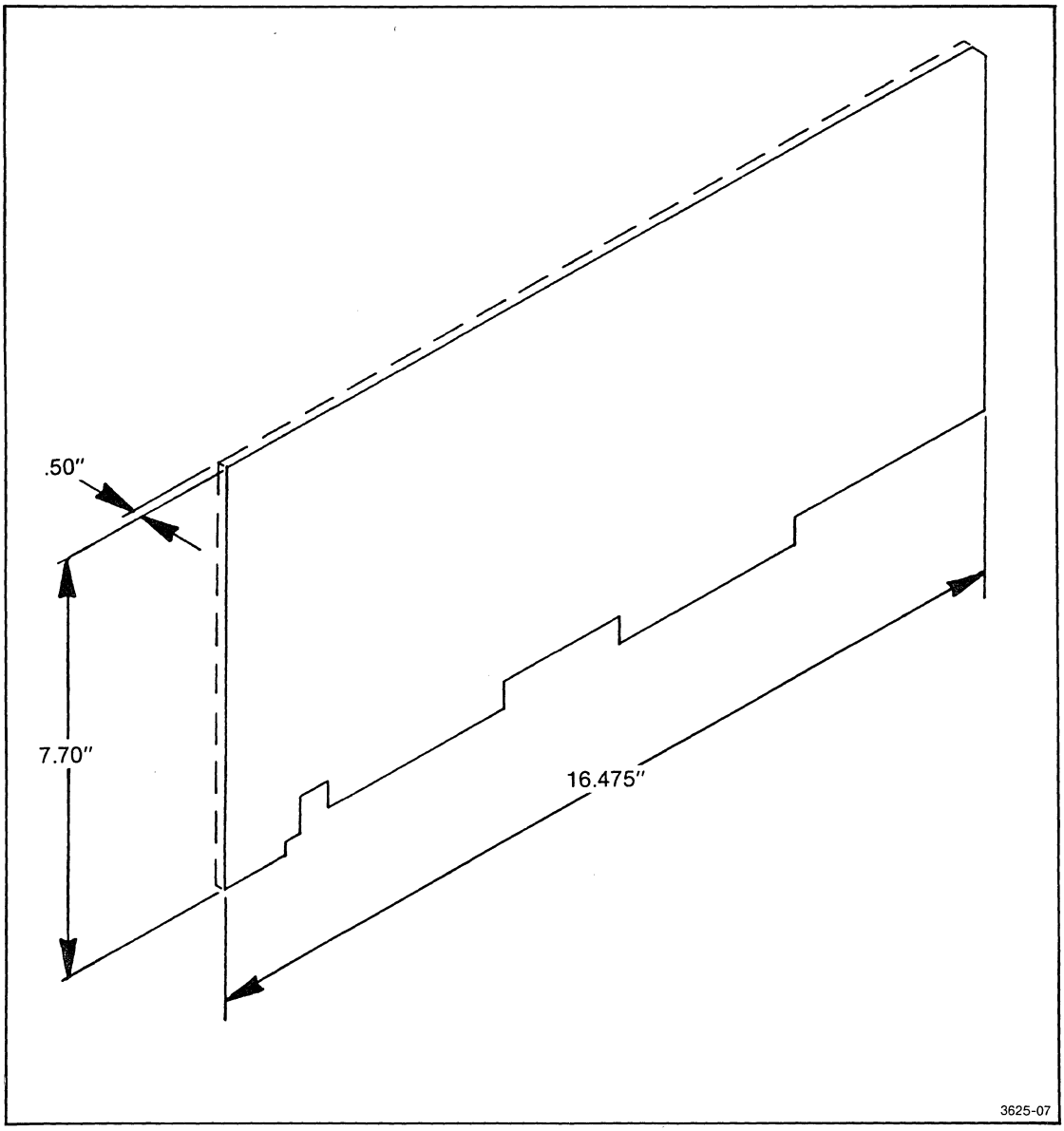


Figure 1-4. Instrument module dimensions.

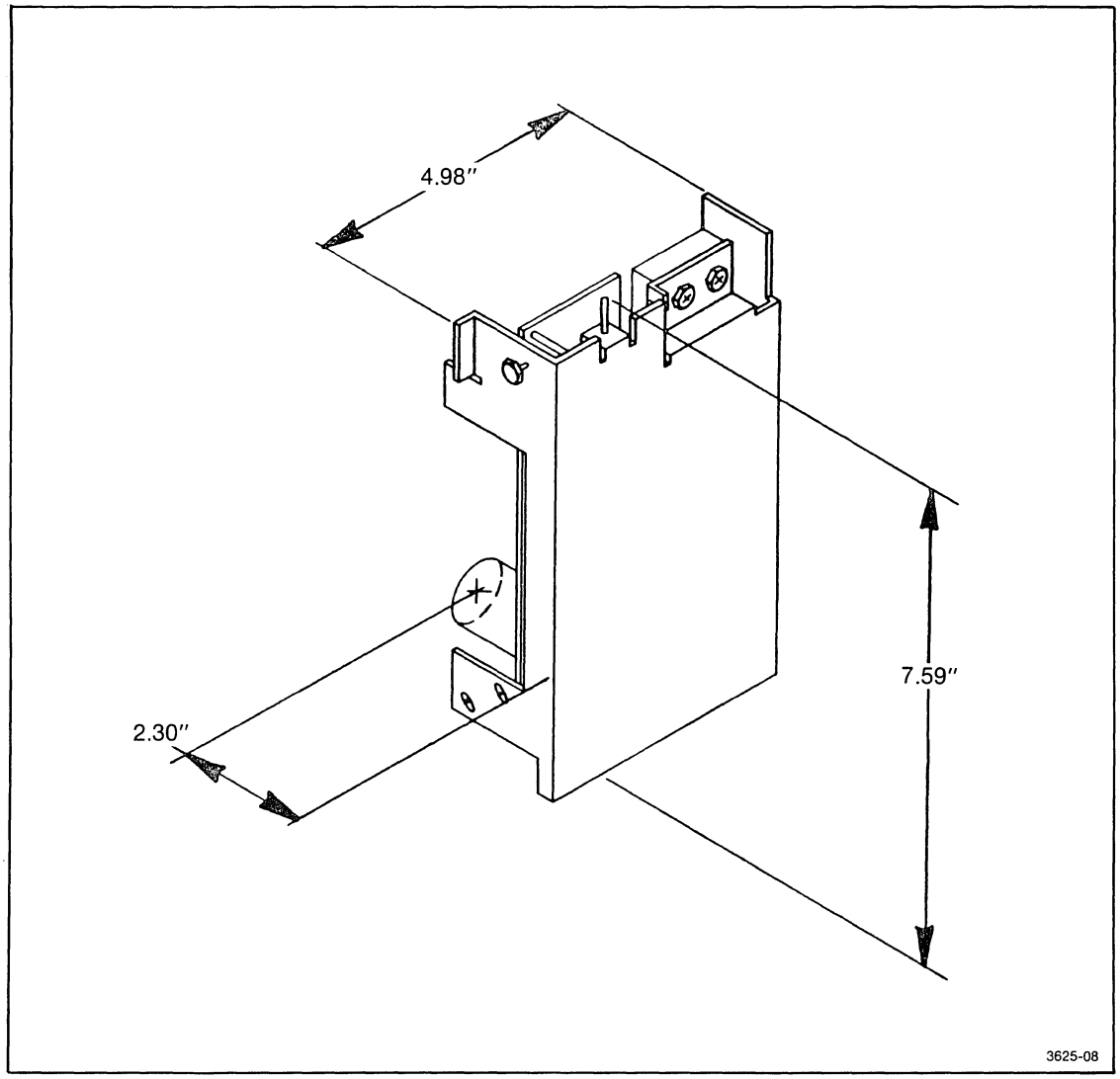


Figure 1-5. +5 V power supply module dimensions.

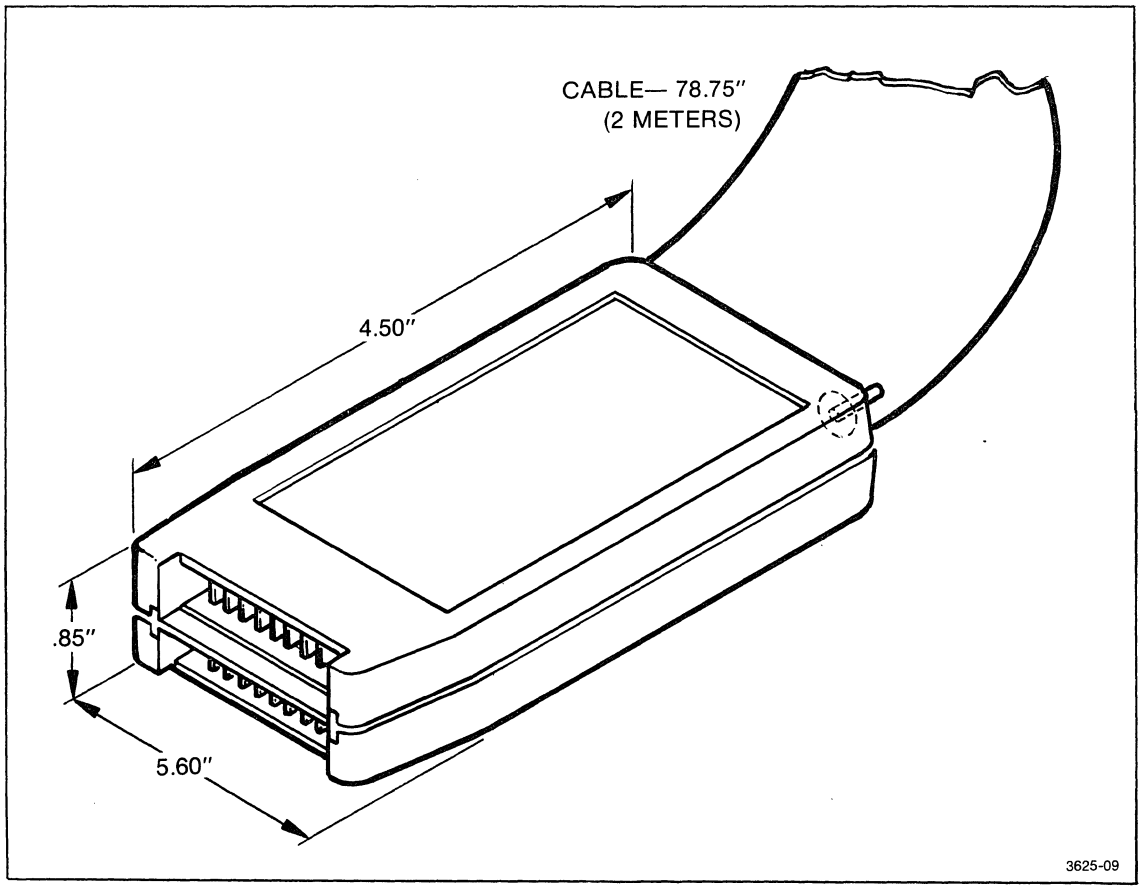


Figure 1-6. P6452, P6455, P6456 dimensions.

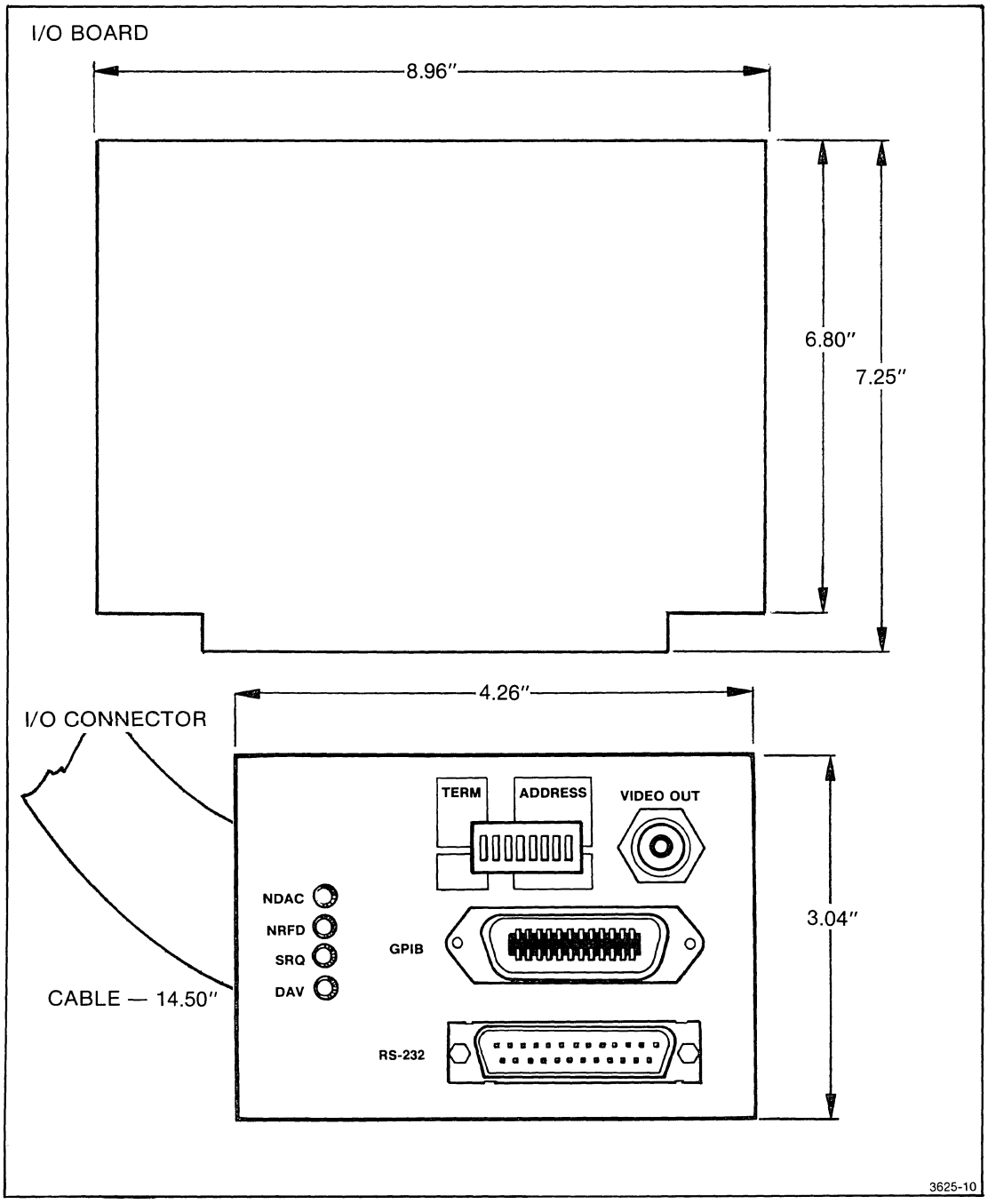


Figure 1-7. Dimensions of the I/O Interface assembly.

OPTIONS 2

OPTIONS

This section contains a brief description of the options available for purchase for a DAS 9100 Series instrument. Further information regarding any option can be found in the manual section containing the type of information desired. For instance, to find the theory of operation for Option 02 (the I/O Interface), refer to the Theory of Operations section.

The following paragraphs briefly describe the options available for the DAS 9100 Series. For more specific information regarding the servicing or operation of any of the listed options, refer to the appropriate part of this manual or to the DAS 9100 Series Operator's Manual.

OPTION 01, TAPE DRIVE

The tape drive is a mass storage device for saving DAS menu setups and reference memory. The tape drive is controlled through the Input Output menu.

DAS91F1 is the field-installable version of Option 01. DAS91F1 must be installed at a Tektronix Field Service Center; installation costs are included in the purchase price.

OPTION 02, I/O INTERFACE

The I/O Interface allows the DAS to use RS-232 and IEEE 488 (GPIB) data transmission techniques. RS-232 can be used in establishing a master/slave mode between two DAS instruments; or it can be used for transmitting GPIB commands between the DAS and a host controller.

The GPIB interface allows the DAS to be controlled remotely by an intelligent device. The DAS acts as a talker/listener on the GPIB.

The I/O Interface also has composite video output for use with hard copy units and video monitors.

DAS91F2 is the field-installable version of Option 02 for the DAS9109 Mainframe. DAS91F2 may be installed by any qualified service technician.

DAS92F2 is the field-installable version of Option 02 for the DAS9129 Mainframe. DAS92F2 may be installed by any qualified service technician.

OPTION 03, ONE +5 V POWER SUPPLY

The +5 V Power Supply Module provides power for two additional instrument bus slots. By combining this module with the power supplies standard to the mainframe, six of the eight bus slots receive power.

OPTION 04, TWO +5 V POWER SUPPLIES

Two +5 V Power Supply Modules, when used in combination with the power supplies standard to the mainframe, are sufficient to power all eight bus slots in the mainframe.

OPTION 05, RACKMOUNT HARDWARE

The rackmount hardware allows a DAS mainframe to be installed in a standard 19 inch rack. Installation instructions are provided in an instruction sheet accompanying the hardware. This option is operator installable.

OPERATING INSTRUCTIONS 3

OPERATING INSTRUCTIONS

MAINFRAME CONFIGURATION

POWER REQUIREMENTS

All DAS mainframes operate from a nominal 115 or 230 V, 50 to 60 Hz, single-phase power source. Before connecting the mainframe to a power source, verify that the line-voltage indicator on the mainframe's back panel is showing the correct nominal voltage for the power source you are using. Figure 3-1 shows the back-panel location of the line-voltage indicator.

If the line voltage indicator shows the wrong voltage for the power source to be used, push the indicator switch to the other position. The line-voltage fuse must also be changed. This fuse is located immediately above the line-voltage indicator; twist the spring-loaded fuse holder counter-clockwise to access the fuse.

A label listing fuse requirements is located to the right of the line-voltage indicator. Use a 250 V, 10 A, slow-blow fuse for 115 V power sources. Use a 250 V, 5 A, 3 AG fuse for 230 V sources.

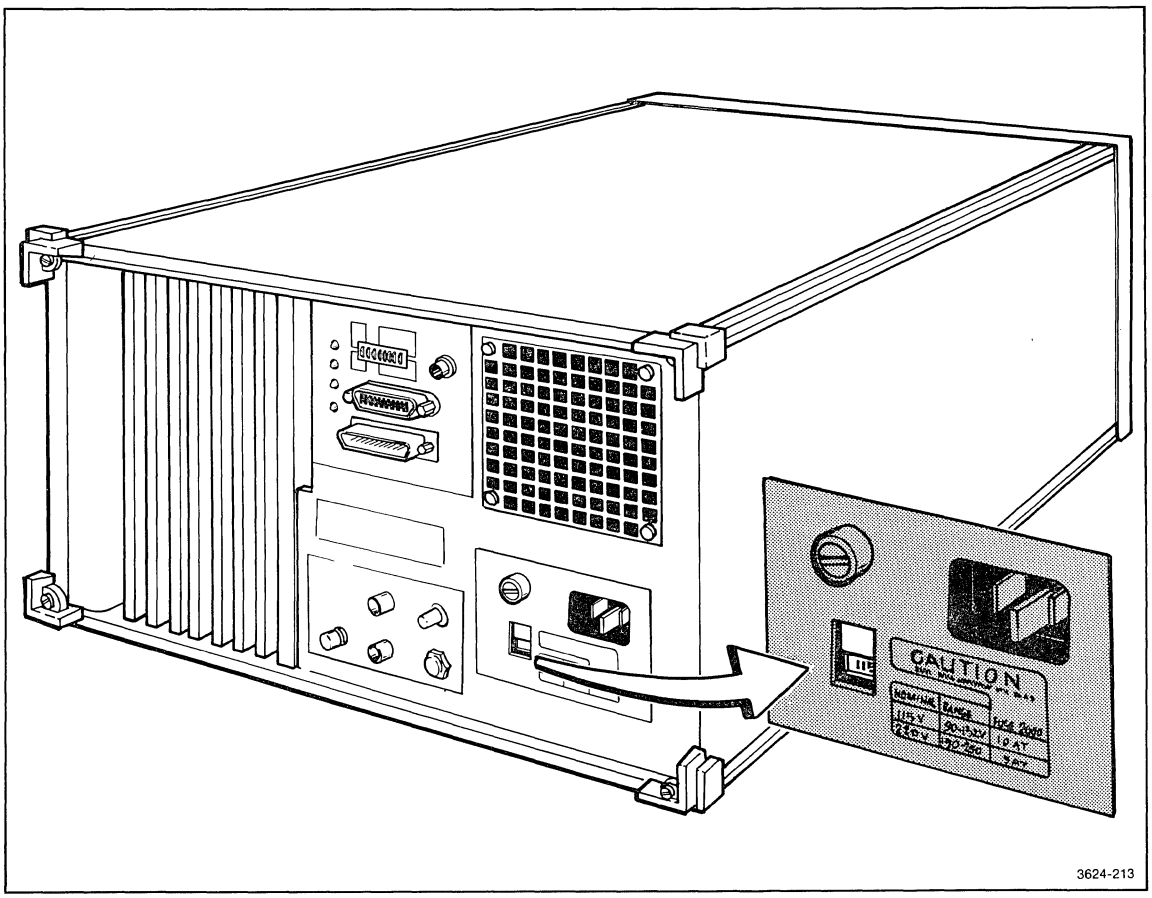


Figure 3-1. Location of the line-voltage indicator.

CAUTION

Before applying power to the mainframe, verify that the line-voltage indicator, the line voltage fuse, and the power cord are compatible with the power source to be used.

POWER CORDS

All DAS mainframes come with a 3-wire power cord with a 3-contact plug for connection to the power source and to protective ground. The plug protective-ground contact connects to the accessible metal parts of the instrument through the power cord protective grounding conductor. For protection against electrical shock, insert this plug into a power source socket that has a securely grounded protective-ground contact.

WARNING

Hazardous voltages may be present on the exposed metal surfaces of the mainframe if the power source socket's protective ground connection is not securely grounded.

DAS mainframes are usually shipped with a 115 V power cord unless otherwise ordered. Other power cords that can be used with the mainframe are shown in Figure 3-2. For information on these power cords, contact your Tektronix representative or the nearest Field Office.

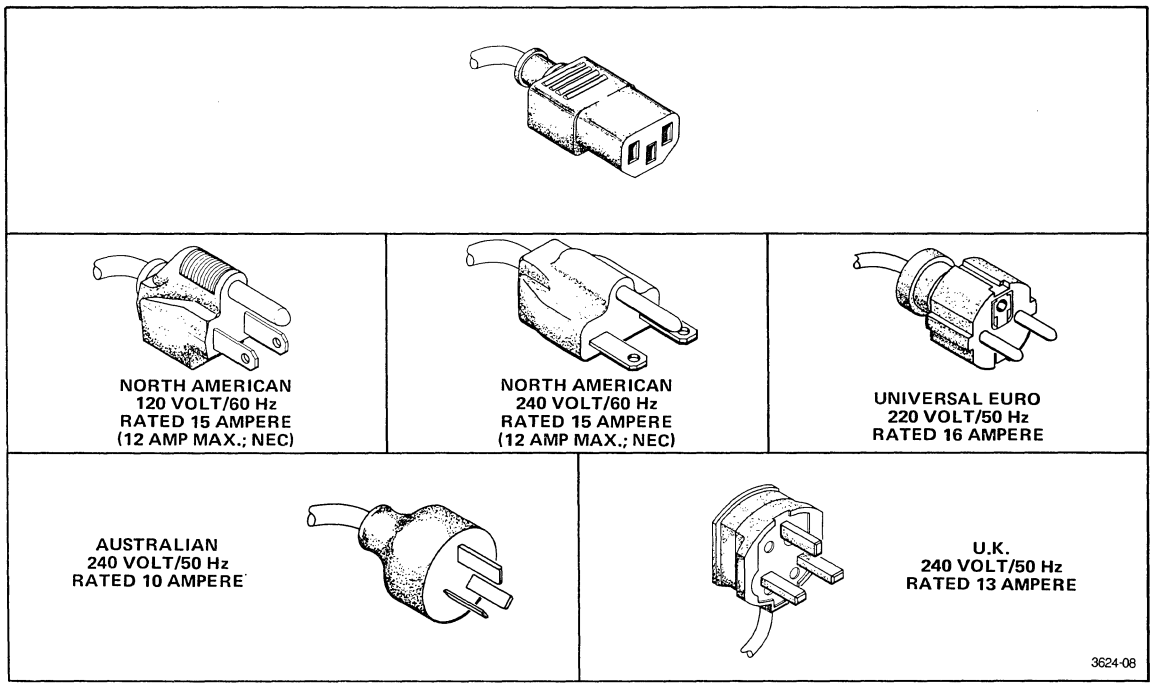


Figure 3-2. Optional DAS 9100 power cords.

MAINFRAME GROUND

As shown in Figure 3-3, the mainframe provides a back-panel ground post. This post can be used to establish a common ground between the mainframe and other instrumentation. Use the post connector to avoid ground-loop problems.

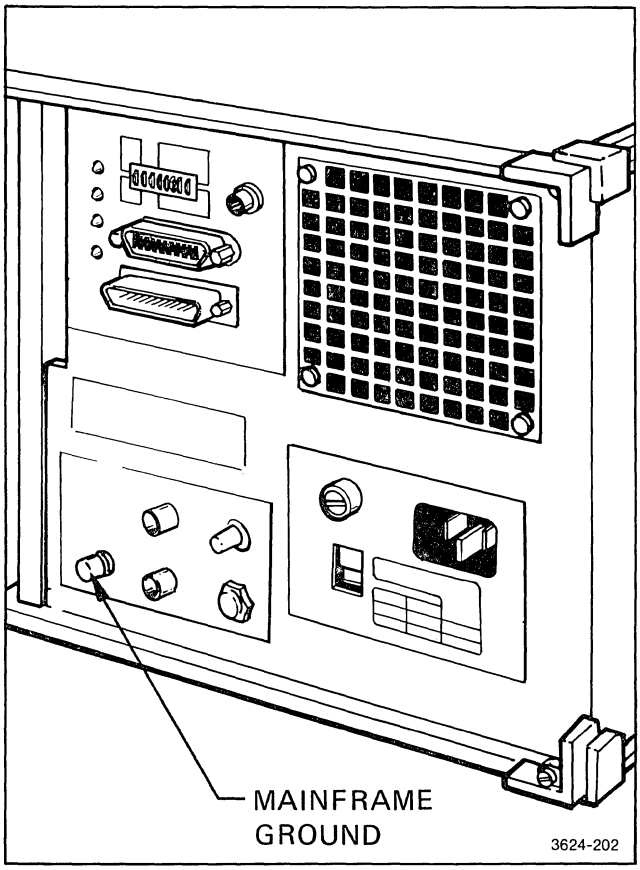


Figure 3-3. Location of the mainframe ground connector.

CONFIGURATION GUIDELINES

Figure 3-4 shows the inside of the mainframe from the front view. For information on accessing the module compartment and installing instrument modules, refer to the Disassembly/Installation Procedures in the Maintenance: General Information section of this manual.

The module compartment contains eight bus slots labeled 0—7. These bus slots may be identified by the white numbers on the fan housing in front of the module compartment. Each bus slot consists of two parallel connectors located on the DAS Interconnect board.

Bus slot 0 is dedicated to the Controller Module; slot 7 is dedicated to the Trigger/Time Base Module. These two modules are standard with the mainframe and must always be installed in their dedicated slots.

Bus slots 1—6 are reserved for data acquisition and pattern generator modules. Table 3-1 provides guidelines for positioning the modules within the six bus slots. These guidelines match factory configurations and, therefore, other DAS instruments. The configuration compatibility between two instruments is especially useful when transferring magnetic tape files from one instrument to another. (Refer to the discussion of the Input Output menu in the DAS 9100 Series Operator's Manual.)

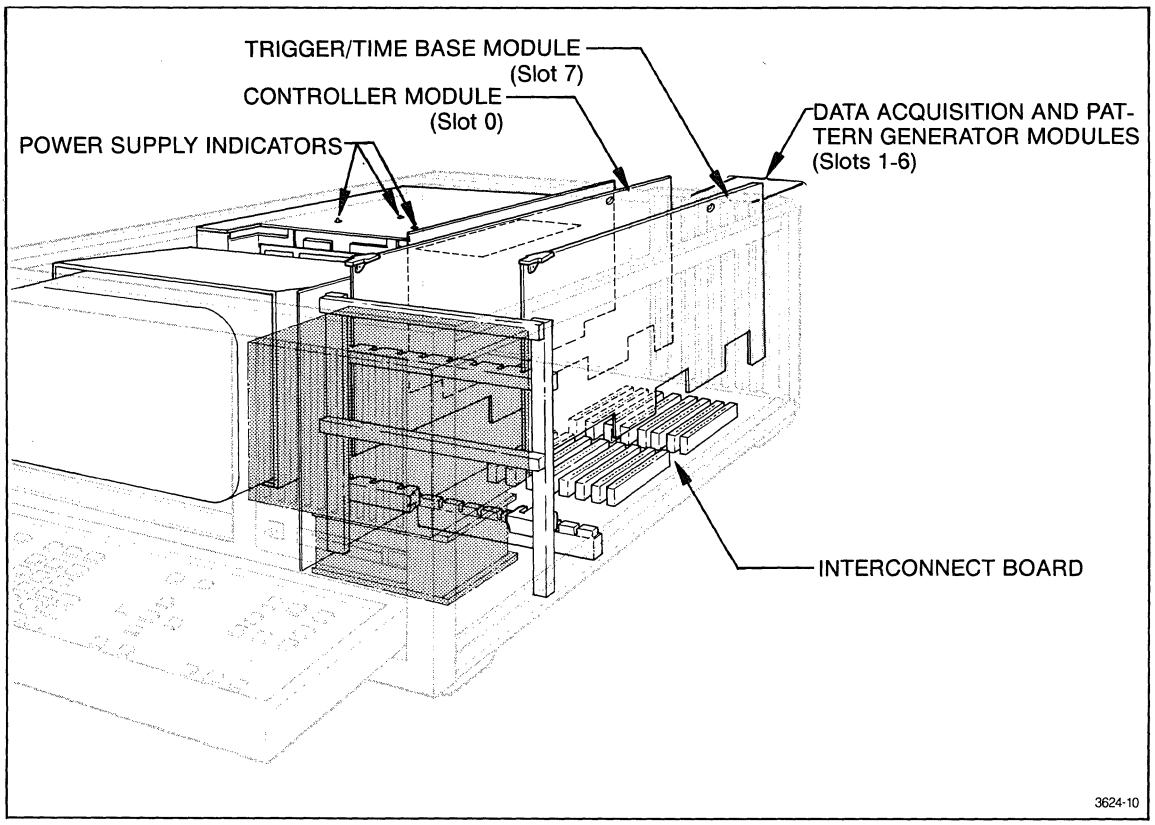


Figure 3-4. Internal structure of the DAS mainframe.

Table 3-1
Configuration Guidelines

Module	Max. per Mainframe	Recommended Bus Slot(s)	Functional in Bus Slot(s)	Comments
Controller	1	0	0	Required
Trigger/ Time Base	1	7	7	Required
91A08	4	6 (5,4,3)	6 (5,4,3)	Required: first 91A08 in slot 6, additional 91A08s in descending slots (5,4,3).
91A32	3	2—6	1—6	
91P16	1	1	1—6	
91P32	2	2—6	1—6	Will not function without a 91P16 installed.

Remember, power to bus slots is modular. Verify that the selected slot has power before installing the module.

For a module to work, it must be installed in a bus slot that is powered. The power for bus slots 1—6 is modular, so you should always check to make sure which bus slots are powered before you install a module.

You can see which bus slots are being powered by looking at the three power supply holes located on the black covering over the power supply area. A +5 V power supply is present if a chrome stem is visible in the hole. Each modular power supply supports two bus slots. The label next to each power supply indicator tells you which bus slots that power supply supports.

MODULE CONFIGURATION LABEL

As shown in Figure 3-5, a module configuration label is provided on the mainframe's back panel. This label is used to specify the mainframe's module configuration, options, and serial numbers. Any changes made to the mainframe should be written on this label.

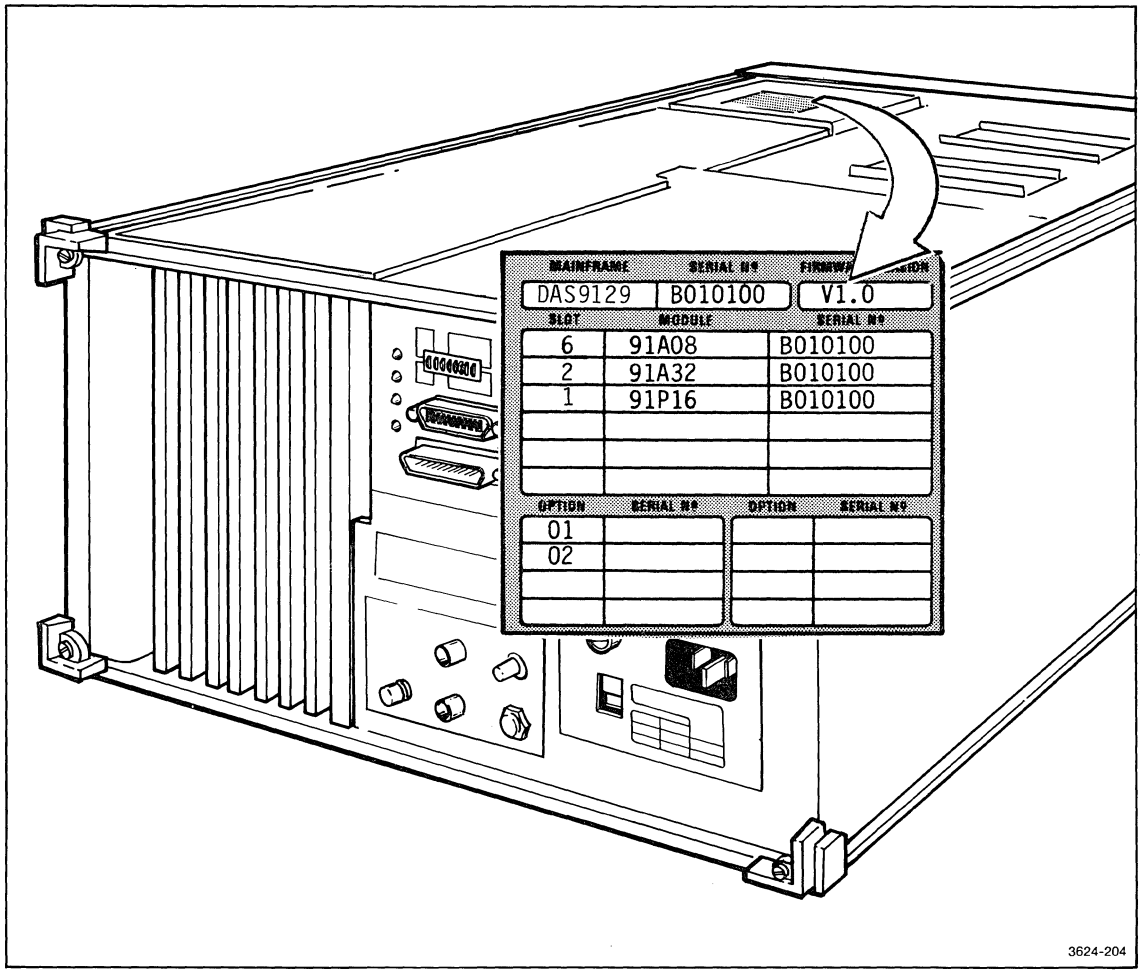


Figure 3-5. Location of the module configuration label.

PROBE CONNECTIONS

CONNECTING A PROBE TO THE DAS

The DAS probes are attached to their respective modules via the mainframe's back panel. Openings in the back panel allow access to the square-pin pod connectors located on the back edge of each module.

Each back-panel opening provides room for up to four pod connector locations, labeled A—D. Depending on the module installed in the bus slot, one or all of these pod connector locations may be used.

Table 3-2 lists the various probe types, which modules they support, and where they are connected.

Table 3-2
DAS Probes and Their Pod Connections

Probe Type	Module	POD Connectors
P6452 External Clock Probe	Trigger/Time Base Module	C
P6452 Data Acquisition Probe	91A32 Data Acquisition Module	A B C D
	91A08 Data Acquisition Module	C
P6455 TTL/MOS Pattern Generator Probe	91P16 Pattern Generator Module	B C
Generator Probe (Available as an option)	91P32 Pattern Generator Module	A B C D
P6454 100 MHz Clock Probe	91A08 Data Acquisition Module	[a]

[a] **Does not use a pod connector. Attach to the coaxial connector located on the 91A08 module installed in bus slot 6.**

If the DAS is turned on when you are connecting the probes, the mainframe will beep when a new probe is connected and the monitor will display that probe's POD ID (see following description of POD ID) on the second line of the screen. If an acquisition probe is connected to a pattern generator module (or vice versa) the mainframe will beep continuously until the probe is disconnected.

NOTE

Do not bind or tape together more than four probes of any one type.

To disconnect a probe from a pod connector, simply grasp the probe by its cable holder, and gently pull it off the pod connector.

CAUTION

Damage may occur to the probe cable if you try to disconnect the probe by pulling the cable rather than the cable holder.

To avoid frequent connecting and disconnecting of probes and lead sets, you may use the Channel Specification menu to rearrange the display order of data acquisition channels without reconnecting probe leads. (For more information, refer to the discussion of the Channel Specification menu in the DAS 9100 Series Operator's Manual.)

When connecting a probe to a module, first find the bus slot where that module is installed. This information should be written on the module configuration label.

Once you have the bus slot, look through the back-panel opening and locate the pod connectors.

NOTE

When connecting probes to a module with more than one pod connector, it is easiest to connect the first probe to the bottom connector and then work up.

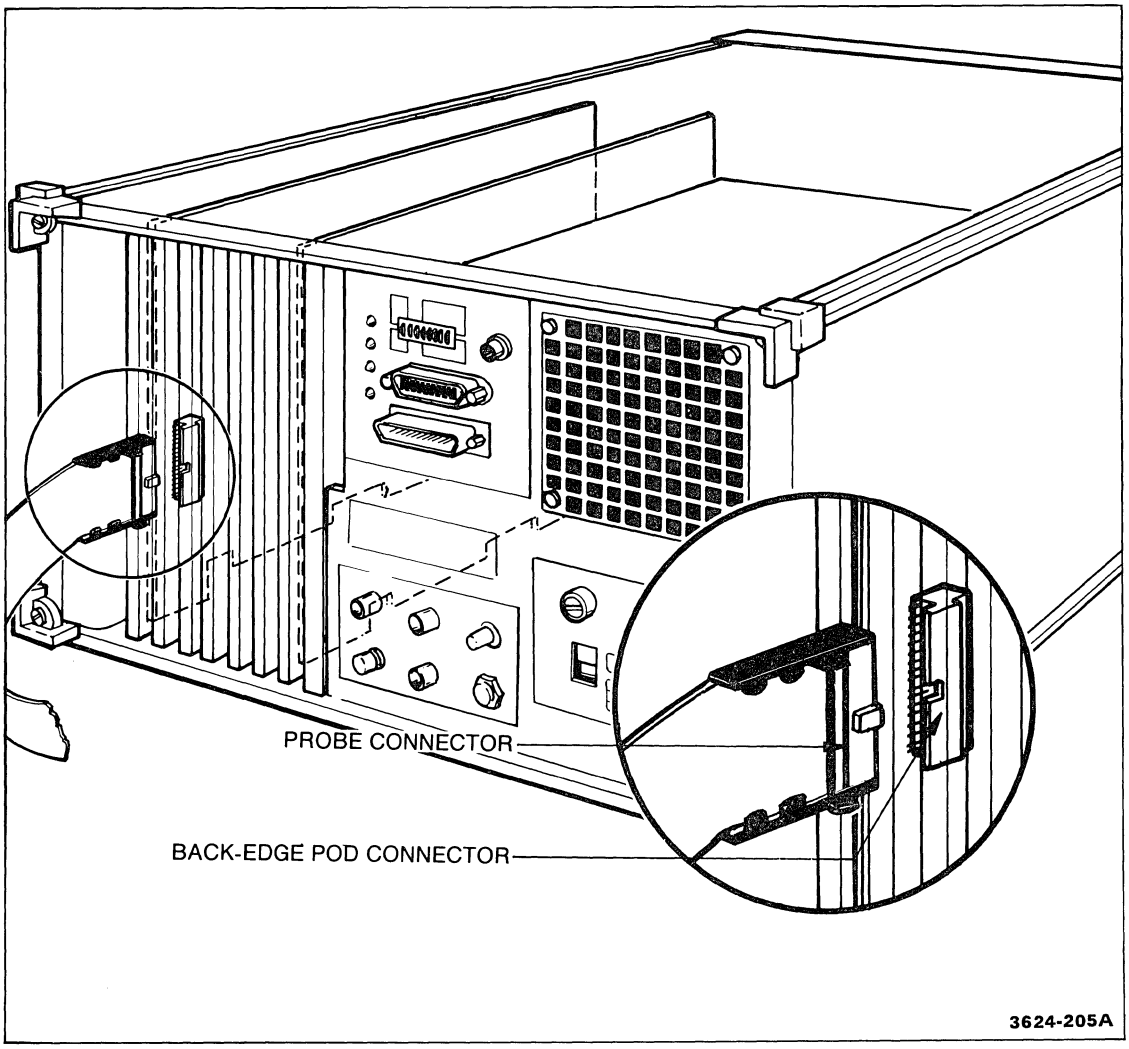


Figure 3-6. Connecting a probe to a pod connector.

To connect a probe:

1. Grasp the probe's cable holder.

2. Align the cable connector with a square-pin pod connector. Be sure the raised tab on the cable holder is facing towards bus slot 0, and is aligned with the opening on the pod connector.

3 Gently push the cable connector onto the pod connector. Do not force the connection.

Connecting the 100 MHz Clock Probe

The P6454 100 MHz Clock Probe is not attached to a square-pin pod connector. This probe is attached to a special coaxial connector located on the back edge of the 91A08 module installed in bus slot 6. One 100 MHz Clock Probe supports all installed 91A08 modules.

POD ID

Each connected probe (except for the 100 MHz Clock Probe) has a POD ID. The ID consists of a bus slot number and a pod connector letter.

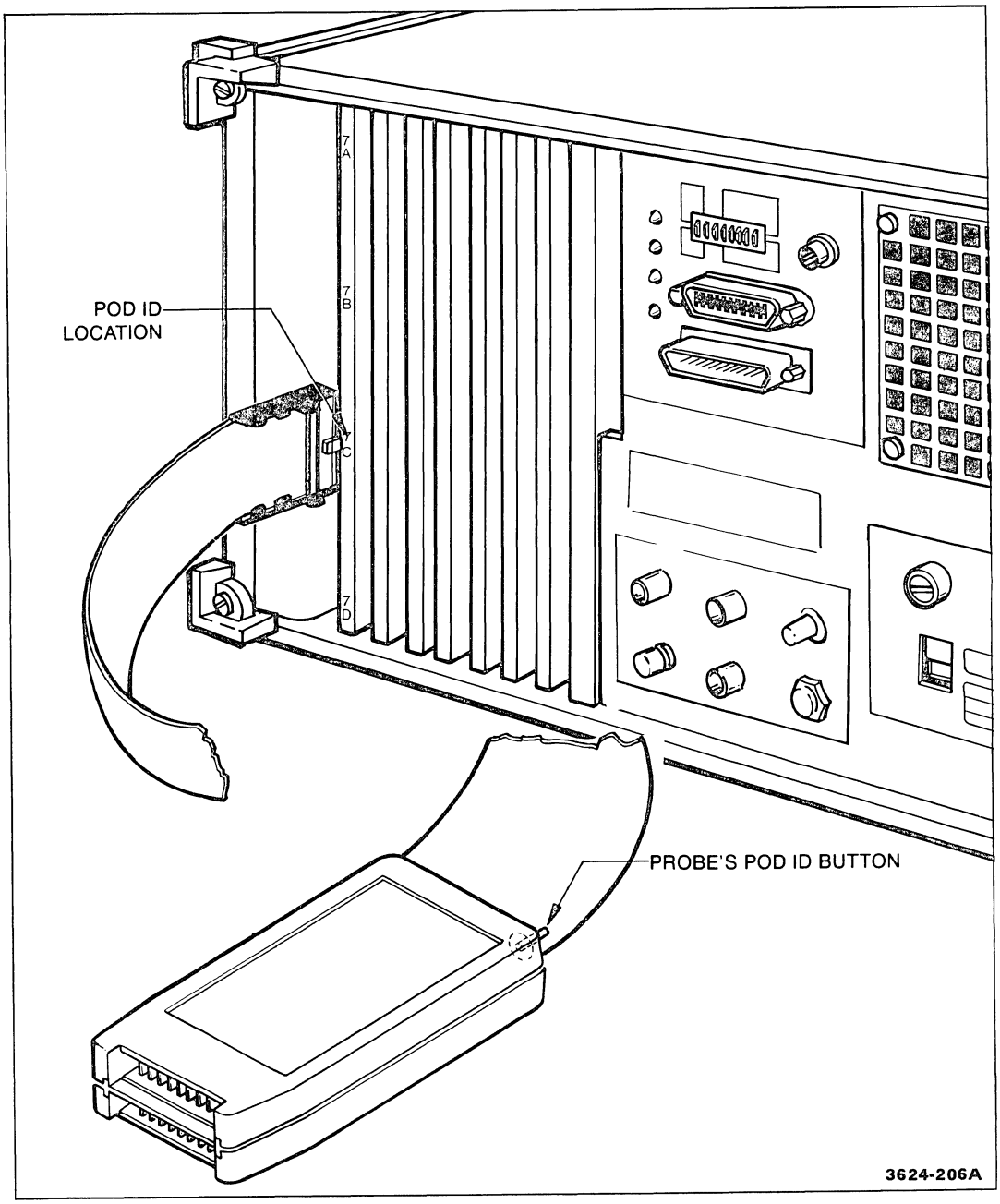


Figure 3-7. POD ID location and button.

The POD IDs for each possible probe location are written on the mainframe's back panel next to each bus slot opening.

A POD ID button is provided on the back edge of each probe (except the 100 MHz Clock Probe). When the DAS is turned on, you may press this button to obtain a screen readout of a specific probe's POD ID.

NOTE

Any time the DAS refers to a probe in a menu or a screen message, it uses the probe's POD ID.

P6452 EXTERNAL CLOCK PROBE

The Trigger/Time Base Module comes with one P6452 Data Acquisition Probe. Any P6452 probe may serve as either a data acquisition probe or an external clock probe. If used as the external clock probe, the appropriate label should be attached.

The probe comes with a 10 inch flying lead set, 12 grabber tips, and one 5 inch ground lead with a Pomona hook tip.

NOTE

Do not bind or tape the External Clock Probe to any other probe.

Signal Lines

The External Clock Probe acquires seven control signals. Three of these signals are used by the 91A32 Data Acquisition Modules, and four are used by the pattern generator modules.

Table 3-3 describes the seven signal lines and their pulse characteristics.

Table 3-3
External Clock Probe Signal Lines

Input Signals	Description	Pulse Characteristics
CLK1	Master external clock line for 91A32 Data Acquisition.	19 ns minimum external pulse width. 25 MHz maximum clock rate.
CLK2	Additional external clock for 91A32 modules. May only be used for EXT SPLIT clock (see Trigger Specification Menu section.)	19 ns minimuim external pulse width. Maximum clock rate is dependent on CLK1 signal.
CLK3	Additional external clock for 91A32 modules. May only be used for EXT SPLIT clock (see Trigger Specification Menu section.)	19 ns minimum external pulse width. Maximum clock rate is dependent on CLK1 signal.

Table 3-3 (cont.)

Input Signals	Description	Pulse Characteristics
PG CLK	Master external clock for pattern generator modules.	19 ns minimum external pulse width. 25 MHz maximum clock rate.
PG PAUSE	Pause (hold) request to pattern generator modules.	19 ns minimum external pulse width. 7 ns minimum set-up time relative to pattern generator clock.
PG INTERRUPT	Interrupt request to pattern generator modules.	19 ns minimum external pulse width. 7 ns minimum set-up time and 14 ns minimum hold time relative to pattern generator clock.
PG INHIBIT	Inhibit (tri-state) request to pattern generator modules.	19 ns minimum external pulse width.

The External Clock Probe requires one connected ground lead. This lead may be attached to the probe at either of the two GND SENSE locations. The GND DIAGNOSTIC location should only be used when the probe is connected to the diagnostic lead set. Information on the diagnostic lead set is provided later in this section under the Operator's Checkout Procedure.

The External Clock Probe has the same threshold range, maximum non-destructive input voltage, and impedance as the P6452 Data Acquisition Probe. Refer to the following description of the P6452 for these values.

P6452 DATA ACQUISITION PROBE

The P6452 Data Acquisition Probe may be used with either a 91A32 or 91A08 Data Acquisition Module. Four of these probes are provided as standard with every 91A32 module, while one is provided with every 91A08 module.

Figure 3-8 illustrates how this probe and its accessories are put together. The probe comes with a 10 inch flying lead set, 12 grabber tips, and one 5 inch ground lead with a Pomona hook tip.

Each 91A08 module also provides an extra 5 inch ground lead and a 5 inch flying lead set. For acquisition rates $>$50 MHz, substitute the 5 inch lead set for the 10 inch lead set and connect the extra ground lead.

Signal Lines

The P6452 Data Acquisition Probe uses nine input lines. Eight of these lines are used for acquiring data, while one serves as a clock qualifier line (if attached to 91A32 Pods A and B, or 91A08 Pod C).

All input signals to this probe must meet setup and hold requirements. The setup requirement refers to the duration for which data must have a constant assigned value before the clock transition. The hold requirement refers to the time that the assigned value must remain after the clock transition.

Table 3-4 describes the eight input lines of this probe and the setup and hold requirements.

When the probe is attached to a 91A08 module, glitches are acquired on all data channels (7—0). A glitch is defined as two or more transitions between a given clock cycle. To be recognized, the glitch must be >5 ns in width, and it must overdrive the threshold by at least 350 mV.

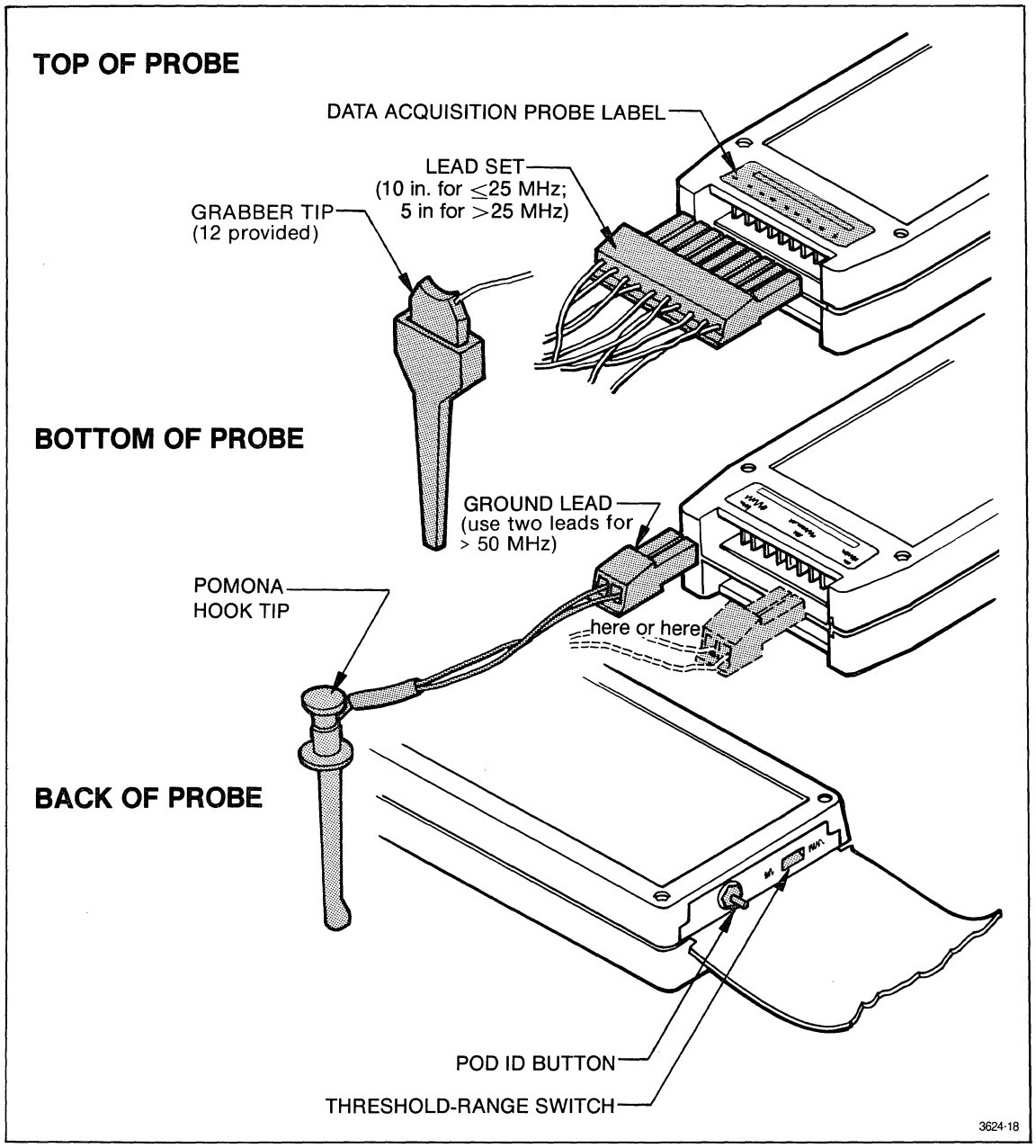


Figure 3-8. P6452 Data Acquisition Probe.

Table 3-4
P6452 Data Acquisition Probe Lines

Input Signals	Description	Pulse Characteristics
7-0	Data channels.	Data Setup Time: 29 ns minimum (91A32) 9 ns minimum (91A08) Data Hold Time: 0 ns maximum (91A32) 0 ns maximum (91A08)
Q	Clock qualifier line when attached to pods A and B of 91A32 module, or pod C of 91A08 module.	Same as above.

Ground

If used for acquisition <50 MHz, the probe requires one ground lead connected at either GND SENSE location. If used for acquisition rates >50 MHz, the probe requires two ground leads—one for each GND SENSE location.

The GND DIAGNOSTIC location should only be used when the probe is connected to the diagnostic lead set. Information on the diagnostic lead set is provided later in this section under the Operator's Checkout Procedure.

Threshold Range

The threshold range switch on the back of the P6452 is used for selecting between a NORM (TTL/VAR) and AUX (MOS) threshold. The maximum threshold control voltage is −2.50 V to +5.00 V in the NORM position or −10 V to +20 V in the AUX position.

This switch only selects the general threshold range. The actual threshold voltage selections are made in the Channel Specification menu.

Maximum Non-Destructive Input Voltage

The maximum input voltage that may be used with the P6452 Data Acquisition Probe is a +40 V peak.

CAUTION

Probe circuitry may be damaged if the P6452 Data Acquisition Probe is connected to a voltage greater than a +40 V peak.

Impedance

The input impedance of the P6452 Data Acquisition Probe is a 1 MΩ input resistance with a 5 pF nominal input capacitance. The lead set adds approximately 5 pF additional input capacitance.

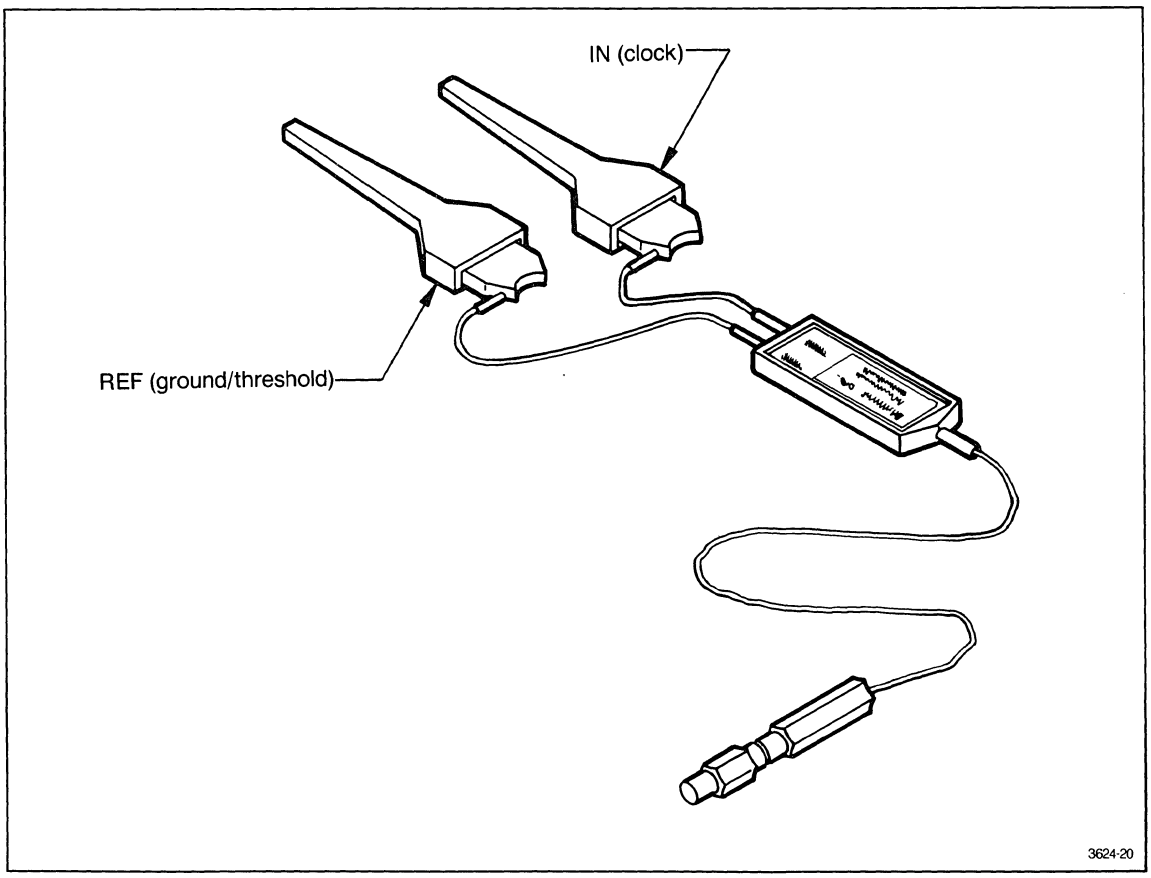


Figure 3-9. P6454 100 MHz Clock Probe.

P6454 100 MHz CLOCK PROBE

The 100 MHz Clock Probe provides the external clock signal for all installed 91A08 modules. It should be attached to the 91A08 module installed in bus slot 6.

Figure 3-9 shows the various elements and features of the probe. The probe comes with two leads with Pomona hook tips. One lead serves as the clock input (labeled IN), and the other serves as the ground (labeled REF).

IN (Clock)

The 100 MHz Clock probe provides one input clock signal. This signal serves as the external clock line for all 91A08 modules.

The maximum clock rate of this probe is 100 MHz (10 ns). The signal must be at least 700 mV peak-to-peak, centered around the threshold.

REF (Threshold Ground)

The reference lead establishes the probe threshold. This lead is connected to ground, the clock probe has the same threshold voltage as the 91A08 module to which it is connected. If the lead is connected to a voltage source (25 V maximum), the clock probe has a threshold equal to the 91A08 threshold plus the selected voltage.

Maximum Non-Destructive Voltage

The maximum input voltage that may be used with the 100 MHz Probe is a +25 V peak.

CAUTION

Probe circuitry may be damaged if the 100 MHz Probe is connected to a voltage greater than a +25 V peak.

Impedance

The input impedance of the 100 MHz Probe is 1 MΩ with a 5 pF nominal input capacitance. The probe lead adds approximately 5 pF additional input capacitance.

P6455 TTL/MOS PATTERN GENERATOR PROBE

The P6455 TTL/MOS Pattern Generator Probe may be used with either a 91P16 Pattern Generator Module or a 91P32 Pattern Generator Expander Module. Two of these probes are provided as standard with a 91P16 module, while four are provided with a 91P32 module.

Figure 3-10 shows how the P6455 and its accessories are put together. The probe comes with one 9 inch twisted signal/ground lead set, 12 grabber tips, one 5 inch black V_L (voltage low) ground sense lead with Pomona hook tip, and one green V_H (voltage high) ground sense lead with Pomona hook tip.

Signal Lines

The P6455 is an active 10-channel probe used with the pattern generator modules. The stimulus output of the probe consists of 8 data channels, one clock line, and one strobe line.

Lead Sets and Ground

The CLK and STRB signal leads are combined with a black ground lead. For most applications using an output clock rate slower than 500 ns, these two ground leads do not need to be connected. For faster clock rates, however, you should connect both of these leads to ensure adequate clock fidelity.

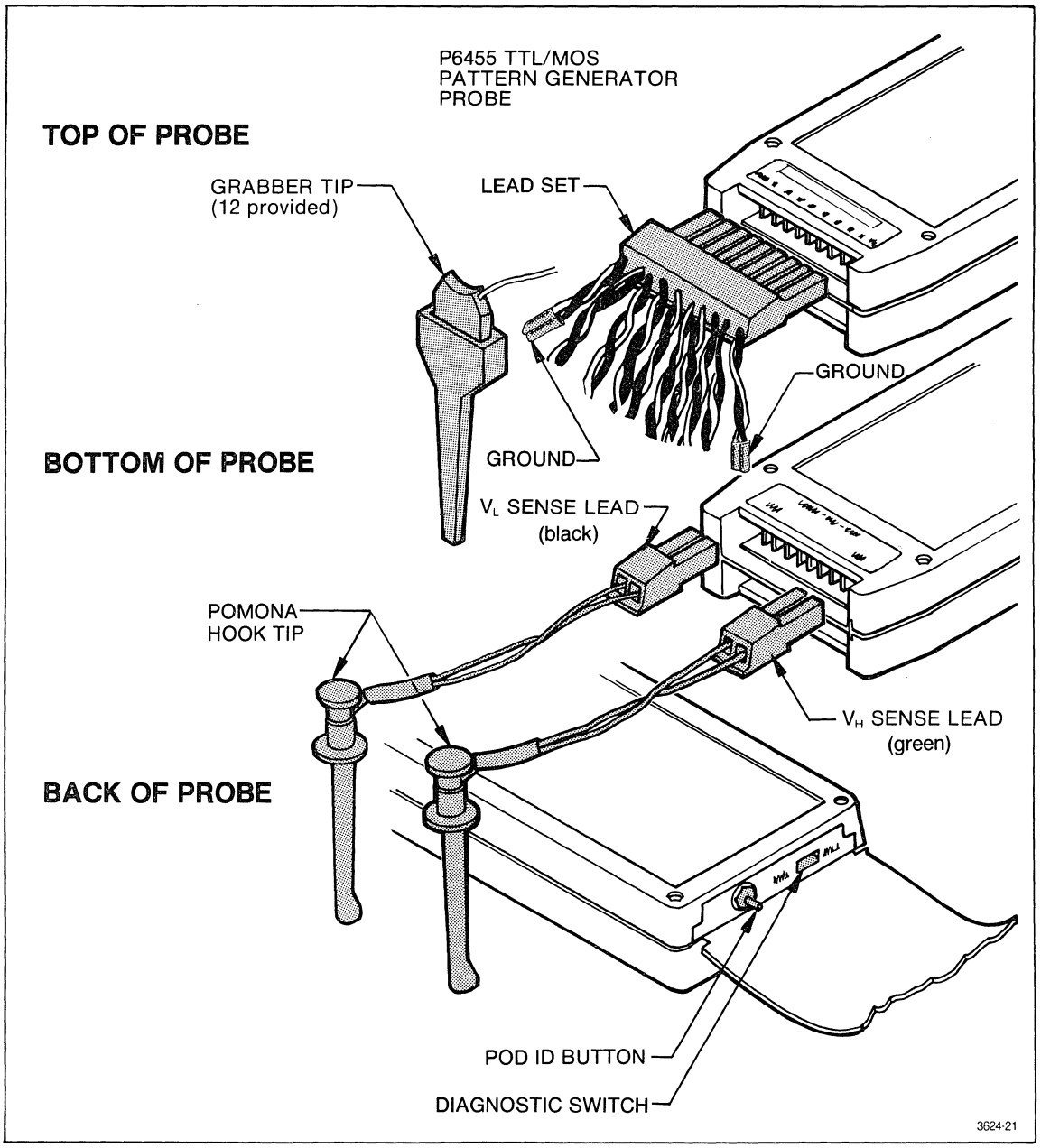


Figure 3-10. P6455 TTL/MOS Pattern Generator Probe.

NOTE

Some combinations of active and capacitive loads at clock rates greater than 100 ns require use of the high-speed harmonica lead set to maintain adequate clock fidelity. This can be determined by examination with an oscilloscope.

V_L/V_H Sense Leads

The black V_L and green V_H sense leads must be used to provide power and threshold sensitivity to the probe. The V_L lead serves as voltage low and may be connected to a voltage range of −15 V to 0 V. The V_H lead serves as voltage high and may be connected to a voltage range of 0 V to +15 V. The maximum operating range is 25 V.

Diagnostic Switch

A diagnostic switch is located at the back of the probe. This switch should always be set to NORM, unless you are using the diagnostic lead set. Procedures on how to use the diagnostic lead set are contained later in this section under the Operator's Checkout Procedure.

P6456 ECL PATTERN GENERATOR PROBE

The P6456 ECL Pattern Generator Probe is available as a mainframe optional accessory. It may be used with either a 91P16 Pattern Generator Module or a 91P32 Pattern Generator Expander Module.

A combination of P6455 TTL/MOS and P6456 ECL probes may be used on the same pattern generator module.

Figure 3-11 shows how the P6456 probe and its accessories are put together. The probe comes with one 9 inch twisted signal/ground lead set, 12 grabber tips, one high-speed harmonica lead set, one 5 inch black V_L (voltage low) ground sense lead with Pomona hook tip, and one 5 inch green V_H (voltage high) ground sense lead with Pomona hook tip.

Signal Lines

The signal lines of the P6456 probe are identical to those of the P6455 TTL/MOS pattern generator probe.

Lead Sets and Ground

The 9 inch lead set may be used for most applications with 100 Ω loads or more. The two ground leads provided with the CLK and STRB signal leads should be connected.

The high-speed lead set should be used with clock rates greater than 200 ns with 50 Ω loads. This high-speed lead set provides ground with every signal lead, and ensures adequate clock fidelity. The necessity of using the high-speed lead set is best determined by inspecting the clock fidelity with an oscilloscope.

V_L/V_H Sense Leads

The black V_L and green V_H sense leads must be used to provide power and reference voltage levels for the probe. The V_L lead serves as voltage low and may be connected to a voltage range of −5.50 V to 0 V. The V_H lead serves as voltage high and may be connected to a voltage range of 0 V to +5.50 V. The maximum voltage difference between V_L and V_H is 5.50 V.

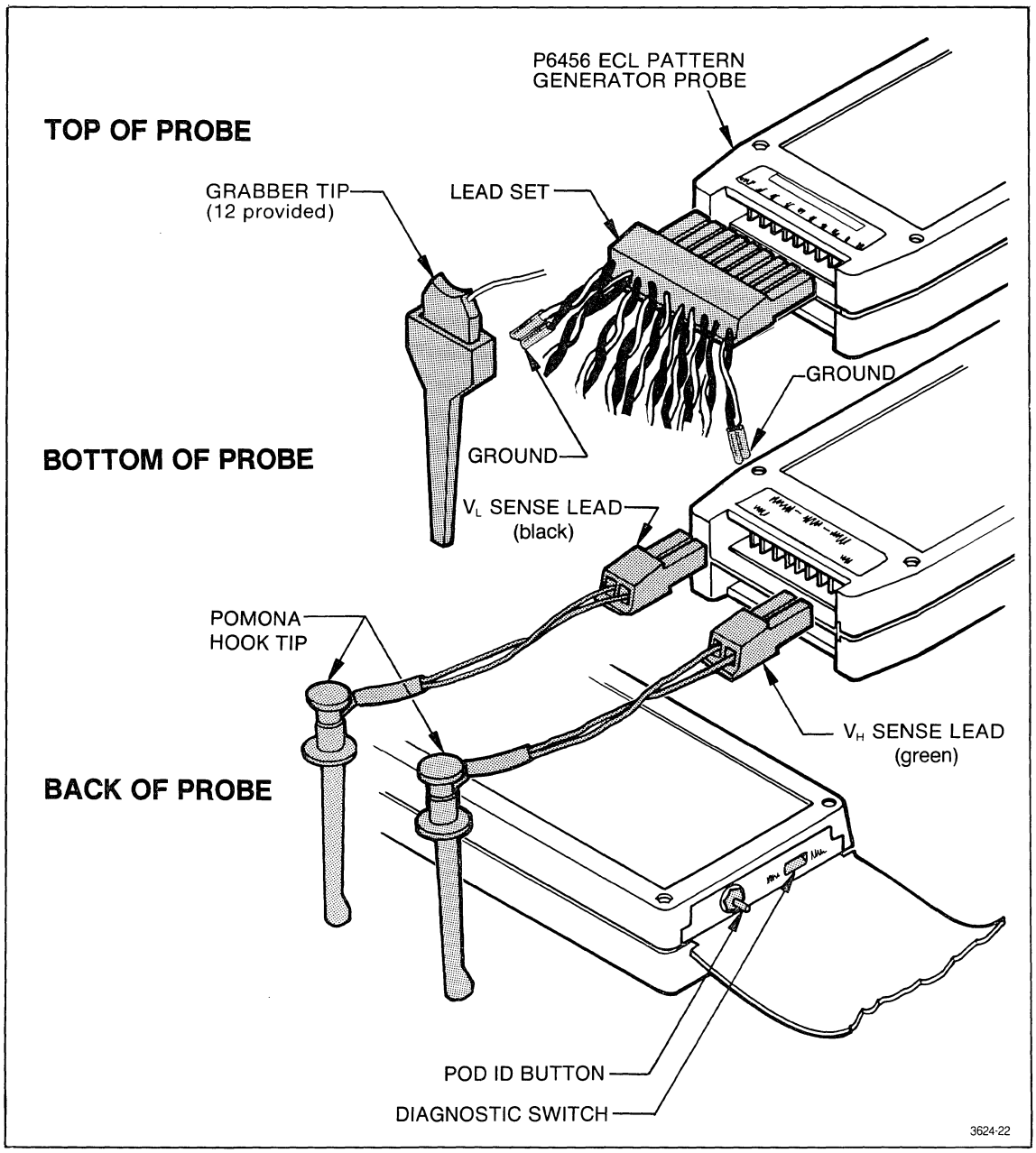


Figure 3-11. P6456 ECL Pattern Generator Probe.

STANDARD AND OPTIONAL I/O CONNECTORS

WORD RECOGNIZER OUTPUT AND TRIGGER INPUT CONNECTORS

Figure 3-12 shows the back panel location of the Word Recognizer Output and the Trigger Input connectors.

The Word Recognizer Output connector (BNC) outputs a rising edge whenever Event 1 is recognized during acquisition. Event 1 is produced whenever a 91A32 module is used during acquisition. For more information on Event 1, refer to the Trigger Specification Menu section of the DAS 9100 Series Operator's Manual.

The Trigger Input connector (BNC) may be used to enable the trigger on 91A32 modules during acquisition. A high-level signal enables the trigger.

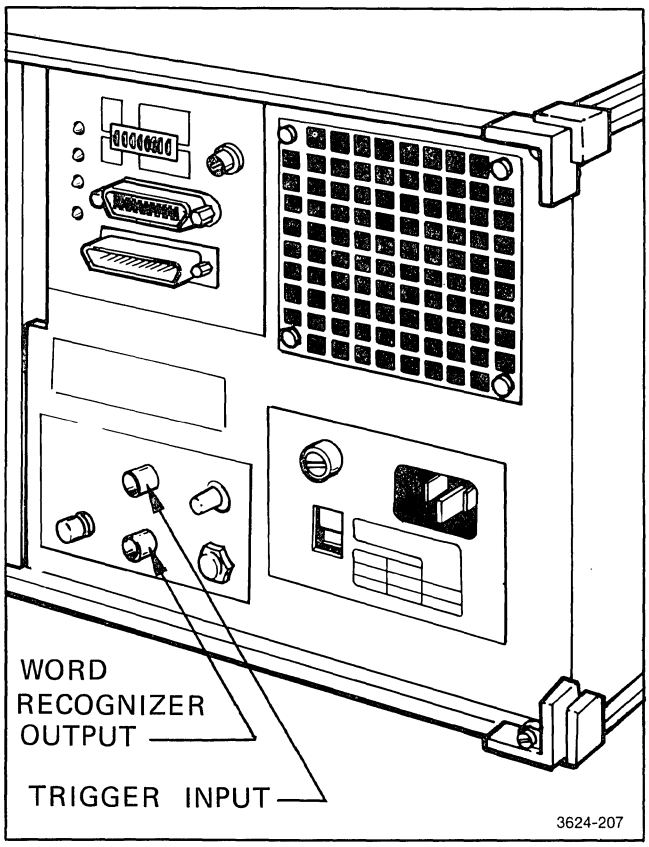


Figure 3-12. Location of the Word Recognizer Output and Trigger Input Connectors.

TAPE DRIVE CONTROLS

The tape drive controls are present if your DAS contains an Option 01, Tape Drive for DC100-type Cartridges.

As shown in Figure 3-13, the tape drive has two front-panel controls: a tape slot and a tape eject button. These two controls allow the insertion and removal of a tape cartridge.

Tape Slot

The tape slot is used for inserting any DC100-type cartridge tapes. The tape is simply pushed through the slot. The design of the tape drive ensures that a tape cannot be inserted upside down.

Tape Eject Button

The tape eject button is used when removing the tape cartridge. When this button is pressed, the tape is ejected. Tapes should be ejected before the keyboard is folded up.

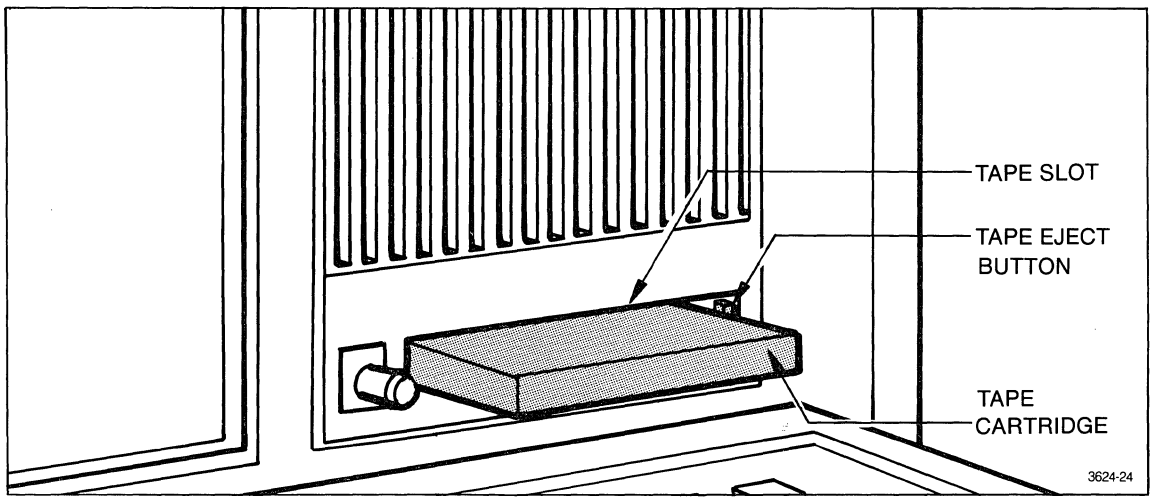


Figure 3-13. Tape Drive controls.

Cleaning the Tape Drive

In order to minimize oxide and foreign matter accumulation, the tape head should be cleaned regularly. Cleaning instructions are discussed in the Maintenance: General Information section of this manual.

RS-232 INTERFACE

The RS-232 connector is provided as part of Option 02. This connector provides a serial data interface for use with the DAS. It may be used to establish master/slave transmission between two DAS systems, or it may be used for transmitting GPIB instructions between a DAS and a host controller.

For information on how to establish DAS master/slave transmission, refer to the Input Output menu information in the DAS 9100 Series Operator's Manual.

The RS-232 connector is located on a back panel insert that is installed in the mainframe as a part of Option 02.

Only eight pins of the RS-232 connector are used:

Pin 1 – Case Ground
Pin 2 – Transmitted Data
Pin 3 – Received Data
Pin 4 – Request to Send
Pin 5 – Clear to Send
Pin 7 – Signal Ground
Pin 8 – Carrier Detect
Pin 20 – Data Terminal Ready

NOTE

The modem should be configured for No Auto Disconnect, No Loss of Carrier Detect, and No Abort Time Disconnect.

The RS-232 connector may also be used in a null-modem mode, where the lines are connected without use of a modem. For this purpose, you can use the null-modem optional accessory or you can wire the interface as follows:

RS-232 Connector	RS-232 Connector
Case Ground Pin 1	Pin 1 Case Ground
Transmitted Data Pin 2	Pin 3 Received Data
Received Data Pin 3	Pin 2 Transmitted Data
Request to Send Pin 4	Pin 8 Carrier Detect
Clear to Send Pin 5	Pin 20 Data Terminal Ready
Signal Ground Pin 7	Pin 7 Signal Ground
Carrier Detect Pin 8	Pin 4 Request to Send
Data Terminal Ready Pin 20	Pin 5 Clear to Send

When the RS-232 interface is used for GPIB transmission, only pins 2, 3, and 7 need to be connected. If a null modem is used, it must cross pins 2 and 3. Pin 20 can be toggled by the host controller to inhibit DAS character transmission.

GENERAL PURPOSE INTERFACE BUS (GPIB)

A General Purpose Interface Bus (GPIB) is provided as part of Option 02. With this bus, the DAS can communicate with any GPIB-compatible controller. The DAS operates as a talker and listener, but not as a controller.

For detailed GPIB information, refer to the GPIB Programming section in the DAS 9100 Series Operator's Manual.

GPIB Switches

Eight DIP switches are used for setting the DAS talker/listener address on the bus.

They are also used for specifying the end-of-message terminator character.

Switches 4—8 – Select the DAS talker/listener address.
Switch 1 – Selects the end of message terminator.

GPIB LEDs

The four LEDs indicate the current handshaking protocol in use between the DAS and the GPIB bus. They also indicate if a Service Request (SRQ) is present.

- SRQ — Service Request
- NDAC
- NRFD — Handshaking Protocol
- DAV

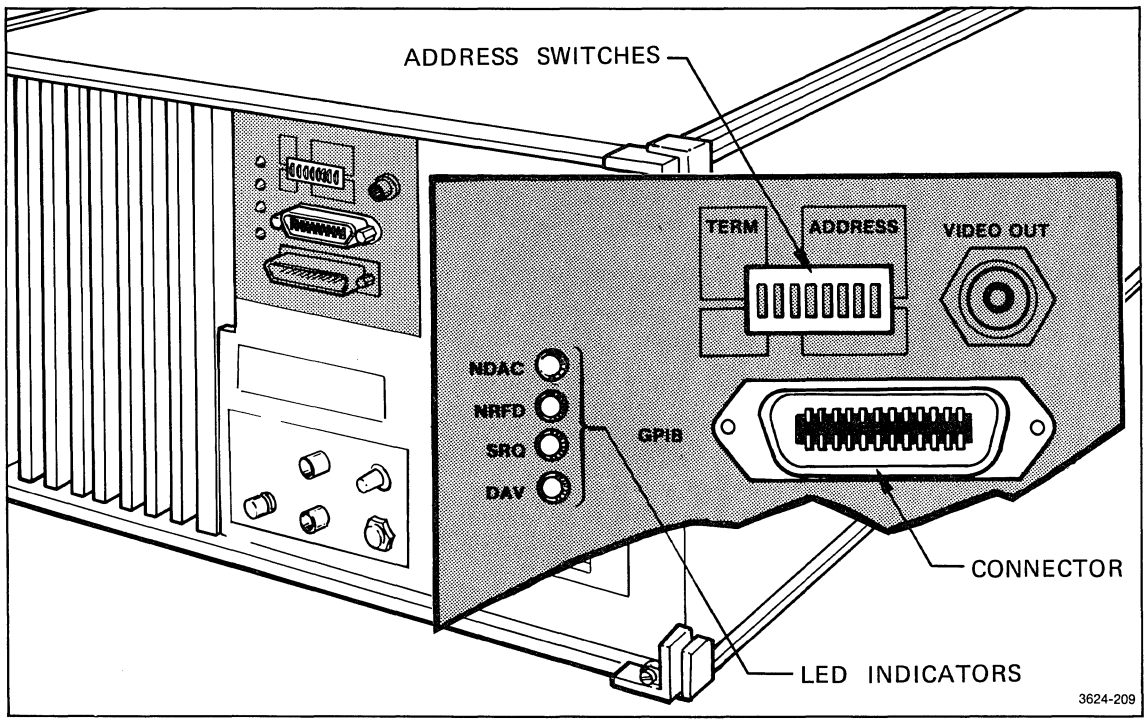


Figure 3-14. GPIB connectors and indicators.

GPIB Connector

The contact assignments for the GPIB connector are as follows:

Contact	Signal Line	Contact	Signal Line
1	DI01	13	DI05
2	DI02	14	DI06
3	DI03	15	DI07
4	DI04	16	DI08
5	EOI	17	REN
6	DAV	18	GROUND (6)
7	NRFD	19	GROUND (7)
8	NDAC	20	GROUND (8)
9	IFC	21	GROUND (9)
10	SRQ	22	GROUND (10)
11	ATN	23	GROUND (11)
12	SHIELD	24	GROUND, LOGIC

VIDEO COMPOSITE OUTPUT

The video composite BNC connector provided with Option 02 may be used with any compatible hard copy or monitor unit. This connector is located on the mainframe's back panel above the GPIB connector. Control of this interface is handled via the connected hard copy or monitor instrument.

NOTE

Be sure to read the video composite specifications carefully to ensure compatibility between the DAS video composite signal and a hard copy or monitor unit. These specifications are located in Section 1 of this manual under Specifications.

COLOR MONITOR CONTROLS (DAS9129 COLOR MAINFRAME ONLY)

DEGAUSS CONTROL

If the DAS9129 Mainframe is exposed to a magnetic field (or is moved to a different orientation in the earth's magnetic field), the purity of the color display may be affected. The colors may appear to bleed or shift out of alignment. If so, the degauss button located on the mainframe's back panel (see Figure 3-15) can be used to neutralize the residual magnetism on the components, and therefore, adjust the display. The degauss button should be depressed for at least five seconds.

BRIGHTNESS CONTROL

The DAS9129 Mainframe provides a brightness control (see Figure 3-15) that can be used to adjust the intensity of the color display. The recommended brightness setting under normal ambient conditions is mid-scale. Prolonged operation of the instrument set to maximum brightness should be avoided.

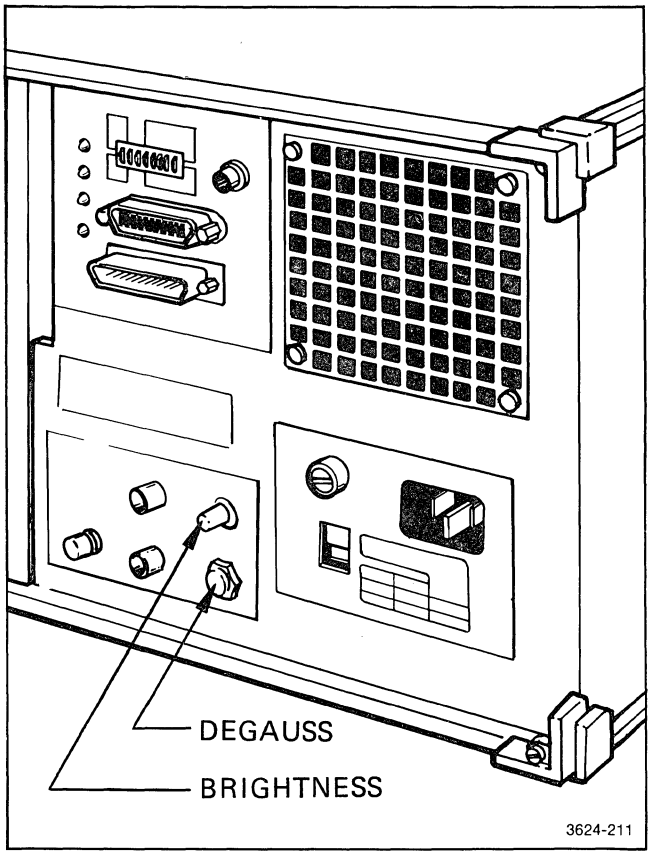


Fig. 3-15. Location of the degauss and brightness controls for the color monitor. (Applies to the DAS9129 Color Mainframe only.)

KEYBOARD CONTROLS AND INDICATORS

The DAS keyboard folds up and latches to the mainframe's front panel to serve as a protective cover. To access the keyboard, simply press down on the front-panel latch and gently lower the keyboard.

Figure 3-16 illustrates the keyboard layout. The keyboard is divided into seven functional areas: Menu Selection; Pattern Generator Instructions; Data Entry; Editing, Cursor, Scroll; and System Control. Each of these functional keyboard areas and their associated keys are described in the following paragraphs.

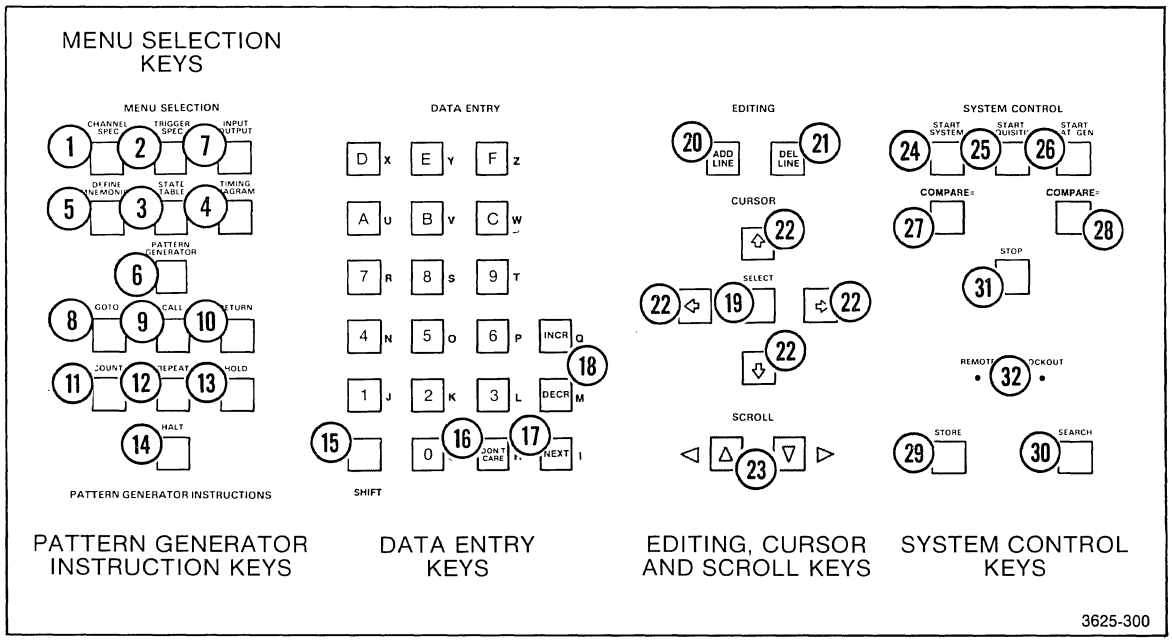


Figure 3-16. DAS keyboard functional layout.

MENU SELECTION

All DAS operations, except for GPIB, are menu driven. You may set up operating parameters by displaying the various menus on the DAS screen and making field alterations. Fields are alterable menu elements that appear in inverse video.

More menu information is provided later in this section under Menu Familiarization. For specific information on how to use the various menus, refer to the DAS 9100 Series Operator's Manual.

Refer to the numbered callouts in Figure 3-16 while reading the following descriptions of keys on the DAS keyboard.

Five DAS menus support the data acquisition operation. The functions of these menus only apply if at least one data acquisition module is installed in the mainframe.

(1) **CHANNEL SPEC** – This key accesses the Channel Specification menu and displays it on the DAS screen.

The Channel Specification menu provides fields for organizing the data acquisition channels into logic groups and establishing their display radix and polarity. This organization is reflected in the State Table, Trigger Specification, and Define Mnemonics menus.

The Channel Specification menu also provides fields for setting up the data acquisition probe thresholds.

(2) **TRIGGER SPEC** – This key accesses the Trigger Specification menu and displays it on the DAS screen.

The Trigger Specification menu provides fields for selecting the acquisition mode, clock rate, trigger, and qualifier parameters. This menu determines which data is stored in acquisition memory, and thus available for display.

(3) **STATE TABLE** – This key accesses the State Table menu and displays it on the DAS screen.

The State Table menu displays the data stored in acquisition and reference memory. It displays each memory separately, or in comparison. The display is in a tabular format.

(4) **TIMING DIAGRAM** – This key accesses the Timing Diagram menu and displays it on the DAS screen.

The Timing Diagram menu provides a logic-waveform display of data stored in acquisition memory. It also displays any glitch information acquired via 91A08 modules.

(5) **DEFINE MNEMONICS** – This key accesses the Define Mnemonics menu and displays it on the DAS screen.

The Define Mnemonics menu provides tables for entering up to 256 mnemonic definitions. The mnemonics are shown on the State Table menu display.

One DAS menu supports the pattern generator operations. The functions of this menu apply only if a 91P16 Pattern Generator Module is installed in the mainframe.

(6) **PATTERN GENERATOR** – This key accesses the Pattern Generator menu and displays it on the DAS screen.

The Pattern Generator menu is used for entering an output program. Fields are provided for selecting the output clock rate, data values, program instructions, and strobe characteristics. Fields are also provided for enabling the external input signals: interrupt, pause, and inhibit.

The Input Output menu is used for controlling tape drive operations which include tape formatting, instrument setup saves and restores, and file deletions. The menu is also used for setting up and controlling RS-232 master/slave transmissions.

(7) **INPUT OUTPUT** – This key accesses the Input Output Specification menu and displays it on the DAS screen. The functions of this menu only apply if the appropriate options (tape drive —Option 01, RS-232 —Option 02) are installed in the mainframe.

PATTERN GENERATOR INSTRUCTIONS

The pattern generator instruction keys are only usable when the Pattern Generator menu is displayed on the DAS screen. These keys enter specific instruction values into the menu's program.

(8) **GOTO** – This key enters a GOTO instruction into the pattern generator program. GOTO tells the pattern generator to jump from one program line to another, then continue program execution from that point.

(9) **CALL** – This key enters a subroutine CALL instruction into the pattern generator program. CALL tells the pattern generator to jump to the first program line of a subroutine, then continue program execution from that point until a RETURN instruction is encountered.

(10) **RETURN** – This key enters a RETURN instruction into the pattern generator program. RETURN tells the pattern generator to return to the next sequential line from which it was CALLed. RETURN should only be used in conjunction with a CALL (or an interrupt CALL).

(11) **COUNT** – This key enters a COUNT instruction into the pattern generator program. COUNT provides a program compression function which tells the pattern generator to stay on the same program line and output incrementing values for up to 255 clock cycles.

(12) **REPEAT** – This key enters a REPEAT instruction into the pattern generator program. REPEAT provides a program compression function which tells the pattern generator to stay on the same program line and output its data value for up to 255 clock cycles.

(13) **HOLD** – This key enters a HOLD instruction into the pattern generator program. HOLD tells the pattern generator to stay on the same program line and hold its value for up to 255 clock cycles. The output clock signals from the 91P16 Pattern Generator Module are also held. The clock signals from the expander modules continue.

(14) **HALT** – This key enters a HALT instruction into the pattern generator program. HALT tells the pattern generator to stop data and clock output.

DATA ENTRY

The Data Entry keys are only usable if a menu is displayed on the DAS screen.

Keys 0—9, A—F, and all 20 shiftable keys are used for entering values into certain menu fields. Entries may take the form of hexadecimal, octal, binary, decimal, or alphanumeric values.

(15) **SHIFT** — This key is used with any of the other 20 data entry keys to obtain the shiftable values G—Z.

(16) **DON'T CARE** — This key is used for entering don't care status in place of digits when specifying data for word recognition and display.

In the Pattern Generator menu, don't care is used to enter tri-state into the pattern generator program. In other data entry fields, don't care is used to delete field values.

(17) **NEXT** — This key advances the screen cursor to the next menu field to the right. If the next field is on a lower line, the cursor will move to that line. In some cases, the NEXT key skips over fields that are not often used. Use the cursor keys to reach these fields.

(18) **INCR and DECR** — These two keys are used in certain menu fields to step through predetermined numerical values.

EDITING, CURSOR, AND SCROLL

The Editing, Cursor, and Scroll keys are only usable if a menu is displayed on the DAS screen. These keys are used for manipulating certain menu fields.

(19) **SELECT** — This key is used in some menu fields to select between predetermined field values.

(20) **ADD LINE** — This key is used to insert lines or spaces in some menu fields.

(21) **DEL LINE** — This key is used to delete lines and values from some menu fields.

(22) ↓ ↑ ← → — The four directional keys are used for moving the screen cursor from one menu field to another. The screen cursor must be residing in a field before changes to that field may be made.

(23) Δ ∇ — These two keys are used to vertically scroll through the table portions of the Channel Specification, State Table, Define Mnemonics, Pattern Generator, and Input Output menus.

In the Timing Diagram menu, the two keys are used to horizontally scroll through displayed data.

SYSTEM CONTROL

The System Control keys are used to initiate DAS operations. Except for the START PAT GEN and STOP keys, the functions of this group all require that at least one data acquisition module be installed in the mainframe.

(24) **START SYSTEM** — This key starts data acquisition and pattern generator operations simultaneously. If no pattern generator modules are installed, the key starts data acquisition. The key will not start the pattern generator if no data acquisition modules are installed.

(25) **START ACQUISITION** — This key starts data acquisition only. If the pattern generator modules are running, the key will not affect their operation.

(26) **START PAT GEN** — This key starts pattern generation only. The key will not start the pattern generator if the data acquisition modules are running.

(27) **COMPARE** = — This key starts data acquisition comparisons. When the key is pressed, an acquisition occurs and is compared to reference memory. If the memories are equal, the comparisons stop. If they are unequal, a new acquisition occurs. The acquisitions continue until the two memories are equal.

The start function for this key is either START SYSTEM or START ACQUISITION, whichever was last used.

If the start function is START SYSTEM, the key will restart the pattern generator with every acquisition.

If the start function is START ACQUISITION, the key will only restart acquisition and will not affect the pattern generator.

(28) **COMPARE** ≠ — This key works like the COMPARE = key, except that new acquisitions are taken until the two memories are unequal.

(29) **STORE** — This key transfers the contents of acquisition memory into reference memory. Any data previously stored in reference memory is lost.

(30) **SEARCH** — This key is used to start memory search functions in the State Table or Timing Diagram menus.

(31) **STOP** — This key stops data acquisition or pattern generator operations. It also stops the SEARCH key function.

The SHIFT/STOP key function displays the power-up configuration on the screen.

(32) **LOCKOUT and REMOTE** — These two indicators specify whether the DAS is in a local, remote, or lockout mode.

When the DAS is in a local mode, both lights are off. This means the DAS is being operated from the keyboard.

The REMOTE light comes on when:

a. The RS-232 port is transmitting or receiving data.

b. The DAS is remote-addressed by the GPIB.

c. The tape drive is formatting a tape (the REMOTE light blinks).

d. The DAS is in a self-test mode.

The LOCKOUT light comes on when:

a. The Lockout command is sent over the RS-232 port.

b. The Universal Address Command Local Lockout is sent over the GPIB.

c. The DAS is in a self-test mode.

When the REMOTE and LOCKOUT lights are both on, the DAS does not respond to the keyboard.

MENU FAMILIARIZATION

The DAS is a menu-driven system. This means that all operations are set up via menus which are displayed on the monitor screen. There are five menus for setting up the data acquisition operation, one menu for setting up the pattern generator, and one menu for controlling I/O functions.

The following paragraphs briefly describe these menus and how they affect the overall operation of the DAS.

DATA ACQUISITION

The block diagram in Figure 3-17 illustrates the five menus controlling data acquisition. Refer to this diagram when reading the following paragraphs.

Channel Specification Menu

The Channel Specification menu serves two basic functions.

First, the menu determines the way in which acquisition channels are organized for display. It organizes the channels into logical groups, and sets display radices and polarity. This information is then used by the Trigger Specification menu for organizing the data display and the Define Mnemonics menu for organizing the mnemonic tables.

This channel organization in the menu is independent of the order in which channels are connected to the system under test. The organization only affects display, not the actual acquisition. Changes can be made to the data display after the data has been acquired.

The second major function of the Channel Specification menu is to determine probe input thresholds.

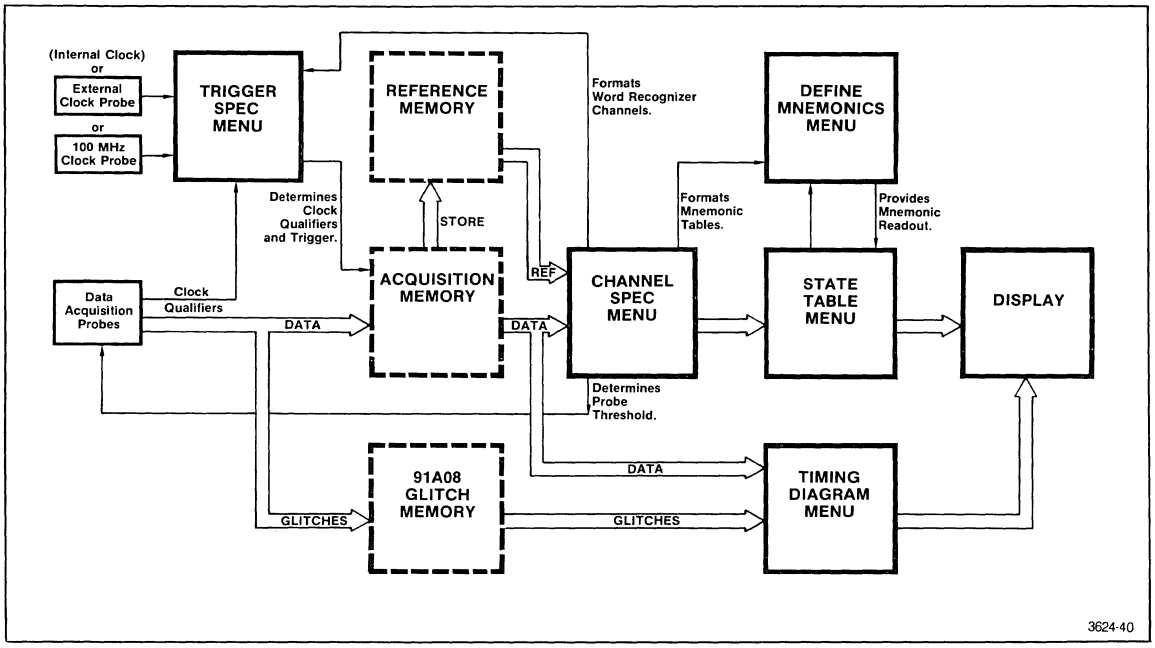


Figure 3-17. Functional overview of the DAS acquisition menus.

Trigger Specification Menu

The Trigger Specification menu sets up the major acquisition parameters. First, it specifies which modules will be used during acquisition. Then, it specifies the acquisition clock (external or internal), and enables clock qualifier lines.

The Trigger Specification menu also controls all word recognition and triggering parameters.

State Table Menu

The State Table menu provides access to acquisition memory and reference memory. It allows three display formats: acquisition memory, reference memory, or acquisition and reference memory comparison.

The channel organization of the state table display is controlled by the Channel Specification menu.

If the Define Mnemonics menu is used, the State Table sends the data through the mnemonics tables for appropriate disassembly on the display.

Timing Diagram Menu

The Timing Diagram menu provides access to acquisition memory and 91A08 glitch memory. The data is presented in a logic-waveform format.

NOTE

The 91A08 glitch memory is only available if 91A08 modules were used during the acquisition. 91A08 modules always acquire glitches when they are used.

Define Mnemonics Menu

The Define Mnemonics menu is used to build mnemonic tables for the State Table menu. The tables are organized by the Channel Specification menu to match the channel group organization. Up to 256 mnemonics may be assigned, under one group table or divided between several.

PATTERN GENERATOR

The pattern generator is used to exercise a system under test. For this purpose, it outputs data, clock, and strobe signals which may be used to stimulate circuit elements. It also responds to three external signals supplied via the External Clock Probe: interrupt, pause, and inhibit.

The pattern generator may run from the DAS internal clock or an external clock supplied via the External Clock Probe. This input clock is then used by the pattern generator as an output clock signal. The data output is synchronous to this clock output.

Output strobe signals are programmable within the clock-cycle boundaries. Their leading and trailing edges may be programmed from the rising edge of the output clock. Plus, they may be inserted as a positive-true or negative-true signal.

Three external signals (interrupt, pause, and inhibit) are supplied via the External Clock Probe. These signals may be enabled and used to interrupt the pattern generator's program.

I/O FUNCTIONS

The tape drive operations and the RS-232 master/slave transmission are controlled via the INPUT OUTPUT menu. GPIB transmission, over the GPIB or RS-232 interface, is controlled via the connected controller unit.

MENU CHARACTERISTICS

There are certain characteristics and terms common to all menus. The following paragraphs discuss these common characteristics and their meaning.

Power-Up Configuration Display

When the DAS is first powered up, it lists the mainframe bus slots and identifies all installed modules. When setting up the various menus, you may often want to refer back to this power-up display. This is accomplished by pressing the SHIFT and STOP keys simultaneously.

Menus and Sub-Menus

Each DAS menu is displayed on the monitor screen by pressing its associated menu key on the keyboard.

Some of the menus are comprised of several parts called sub-menus. These sub-menus are individual screen displays which may be selected only after the menu is entered. For example, the Input Output menu has two sub-menus: one for controlling the tape drive and one for controlling RS-232 master/slave transmission. To display either of these sub-menus, you must first enter the Input Output menu.

Menu Default Displays

On system power up, the DAS assigns each menu with default operating parameters. When you enter the menu, the menu and its default parameters appears on the DAS screen. This inintial menu display is called the menu's default display.

If no changes are made to the menu's default display, the DAS will use the default parameters during the various operations.

Menu Fields and the Screen Cursor

When a menu is displayed on the DAS screen, the menu's changeable parameters appear as reverse-video fields. Before making any changes in a specific field, you must first move the blinking screen cursor to that field.

The screen cursor moves from field to field, in any direction. It is controlled via these keys:

- ↑, ↓, ←, or → **keys** — move the cursor one space up, down, left, or right.
- **NEXT key** — moves the cursor one field to the right.

Once the screen cursor is located in a specific field, you may change the field value. The common usage of keys in making field changes are:

- **Data Entry keys** — used in fields that have a string of numeric or alphanumeric values.
- **SELECT key** — used in fields with predetermined values.
- **INCR and DECR keys** — used in fields that have specific incrementing or decrementing numerical values.

Error Message Readout

The DAS has a comprehensive set of error and prompter messages. These messages appear on the second line of the screen and are displayed in highlighted video. The messages are also accompanied by a beeping sound from the mainframe.

POD Messages

There are three pod messages that may appear on the second line of the screen. They are:

- **POD ID** — appears when a probe's POD ID button is pressed.
- **POD DISCONNECTED** — appears when a probe is disconnected from the back panel of the DAS.
- **POD CONNECTED** — appears when a probe is connected to the back panel of the DAS.

In these messages, the probes are always identified by their POD ID (bus slot number, pod connector letter). The messages appear in highlighted video and are accompanied by a beeping sound from the mainframe.

OPERATOR'S CHECKOUT PROCEDURE

The DAS power switch is located on the mainframe's front panel as shown in Figure 3-18. To power up the DAS, simply pull out the switch.

POWER-UP SELF TEST

The DAS has internal diagnostic tests that run automatically every time the mainframe is powered up. These tests check out the major mainframe components and operating firmware.

During the first phase of self test, the DAS tests the major blocks of system RAM and ROM and initializes I/O ports. The LOCKOUT indicator on the keyboard is illuminated while the RAMs are being tested, and the REMOTE indicator is illuminated while the ROMs are being tested. After the RAM/ROM tests, both indicators are illuminated while the DAS finishes system initialization.

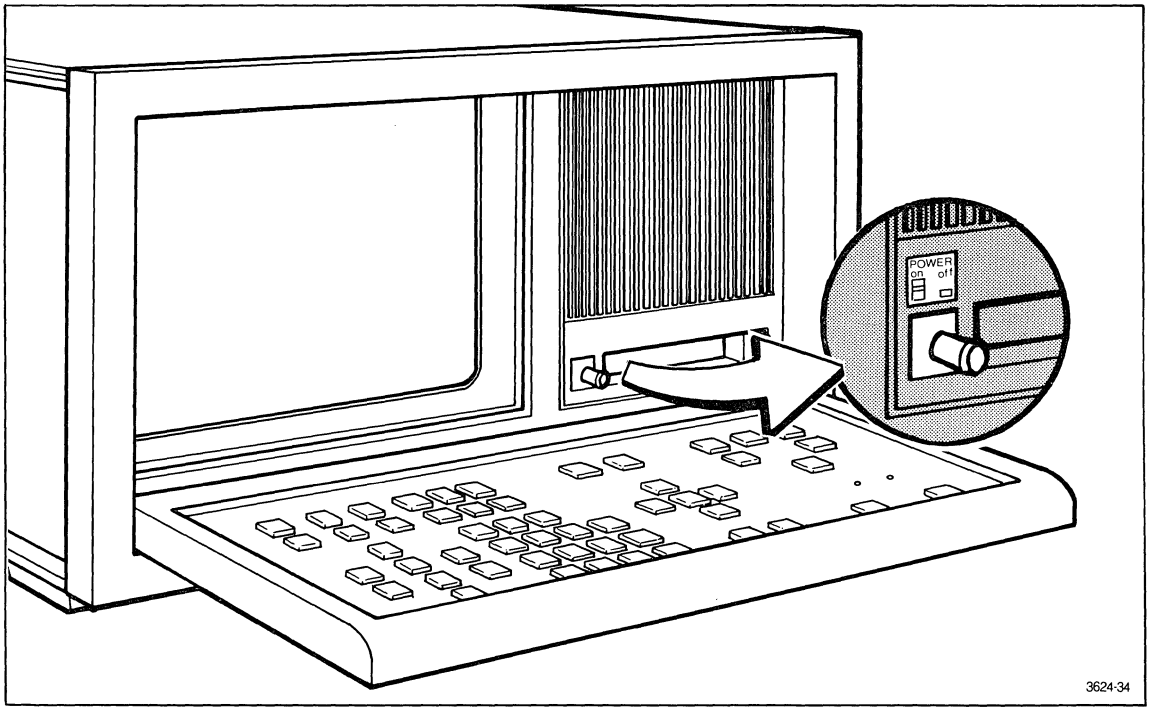


Figure 3-18. Location of the power switch.

The screen display does not appear until both indicators are off and the initialization is complete (approximately 20 seconds). The display shows a configuration listing. Each installed module is listed on the screen along with its bus slot number. At the top of the screen, a message appears reading DAS 9100 SERIES SELF TEST IN PROGRESS.

Each listed module (except the I/O board) is tested and given a PASS or FAIL notation. A PASS means that the module test was successful, while FAIL means that the test was unsuccessful.

If a ROM checksum test failed during initialization, an error message will appear in the upper-right portion of the screen reading ROM CHECKSUM ERROR.

When the tests are finished, the DAS screen displays a message reading DAS 9100 SERIES SELF TEST COMPLETE.

Table 3-5 lists and defines the possible power-up errors. Some of these errors only inhibit a portion of the DAS functions.

Table 3-5
Power-Up Error Conditions

ERROR CONDITION	DEFINITION
A display does not appear on the screen (and the REMOTE and/or LOCKOUT indicator is on).	An error occurred on the Controller board. Power down the DAS, then turn it back on.
ROM CHECKSUM ERROR	
0,...	An error occurred on the Controller board, and the instrument will not operate properly.
1-6,...	An error occurred on the module installed in the specified slot (1—6). The module will not operate properly. (See descriptions of failures listed below.)
7,...	An error occurred on the Trigger/Time Base Module, and the instrument will not operate properly.
RAM ERROR	The lower 16K of RAM did not pass the RAM power-up test. The instrument will not operate properly.
ROM ADDRESS ERROR	The Trigger, Channel, or Start ROMs cannot be addressed or are missing. The instrument will not operate properly.
Controller FAIL	The keyboard has failed the power-up test. Turn the DAS off and on again, making sure no key is pressed on the keyboard.
Trigger/Time Base Module FAIL	The Trigger/Time Base Module has failed the power-up test. The instrument will not operate properly.
91A32 Data Acquisition Module FAIL	The 91A32 module has failed the power-up test. The module will not operate properly, but the rest of the instrument is not affected.
91A08 Data Acquisition Module FAIL	The 91A08 module has failed the power-up test. The module will not operate properly, but the rest of the instrument is not affected.
	If the 91A08 module that failed is in slot 6, remove the module and place the functioning 91A08 modules in descending slot order 6 through 3.
91P16 Pattern Generator Module FAIL	The 91P16 module has failed the power-up test. The module will not operate properly. This does not affect data acquisition modules, but it does affect the operation of 91P32 modules. 91P32 modules cannot be operated without a 91P16.
91P32 Pattern Generator Expander Module FAIL	The 91P32 module has failed the power-up test. The module will not operate properly, but the rest of the instrument is not affected.

Figure 3-19 illustrates how the DAS screen appears when no errors are found during the self test. You may now enter any menu and begin operation.

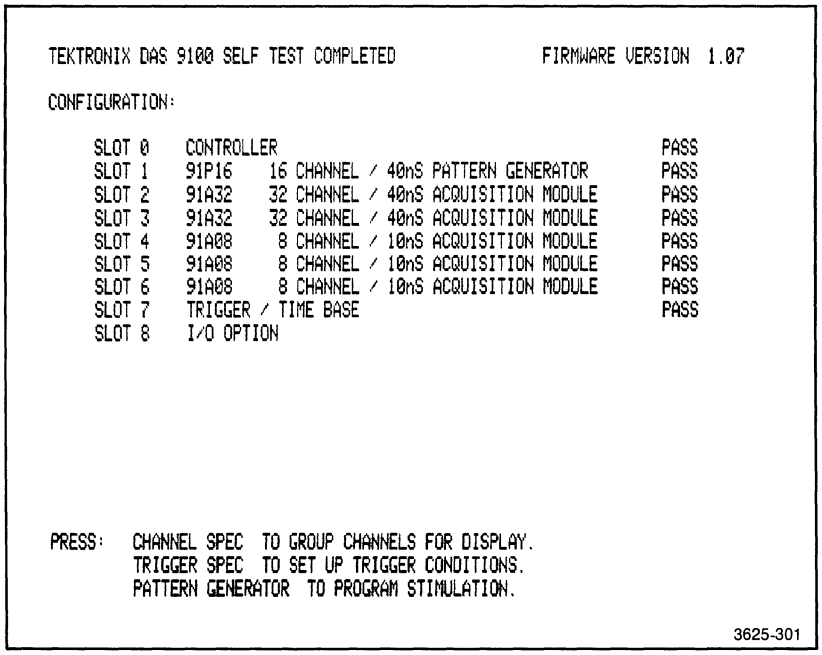


Figure 3-19. Successful completion of the Power-Up Self Test.

Figure 3-20 illustrates how the DAS screen appears when an error occurs during self test. If the error that occurred does not affect the DAS operations you wish to perform, press the DON'T CARE key. A prompt message will be displayed on the bottom of the screen describing the available menus.

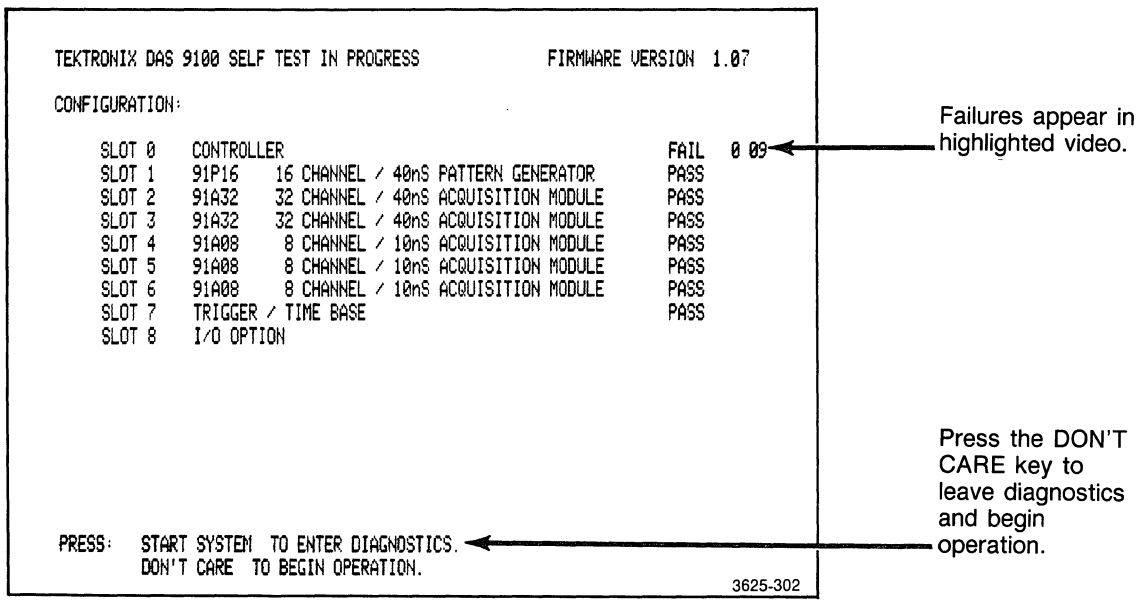


Figure 3-20. Failure in the Power-Up Self Test.

DIAGNOSTICS MENU

The power-up self tests consist of a limited number of fast functional tests that are run whenever the DAS is powered up. These tests verify the basic functionality of the DAS, but are not considered comprehensive.

The Diagnostics menu offers more levels of diagnostics. The Diagnostic menu is only accessible when the power-up tests show that one of the modules has failed. To enter the Diagnostics menu, press the START SYSTEM key.

NOTE

Do not press any key other than START SYSTEM. If you do, you may leave the power-up self test display and lose access to the Diagnostics menu.

It is possible for a module to fail in such a way that the power-up tests do not detect the failure. To access the Diagnostics menu in this situation, the operator can induce a power-up failure from the keyboard by holding down any key on the keyboard from the time the DAS is turned on to the time the power-up self tests are complete.

When first entered, the Diagnostics menu looks similar to the display in Figure 3-21.

The Diagnostics menu is controlled in the same way as the other DAS menus. All changeable fields are shown in reverse video. Fields are changed by moving the blinking screen cursor into the field to be altered. Cursor movement is controlled by the four cursor keys and the NEXT key. The value in the field is changed either by using the SELECT key, or by entering a hexadecimal value from the data entry keys.

If any menu selection key is pressed at this point, the diagnostics will be exited and the selected menu will be displayed. The Diagnostics menu cannot be re-entered from the standard menu displays.

Press the START SYSTEM key to start a diagnostic test or function. The function will either stop by itself, or the STOP key can be pressed to stop the function at any time. The Diagnostics menu may be exited by pressing any menu selection key while no tests are running.

Diagnostics Menu User-Changeable Fields

Six user-changeable fields are used in the Diagnostics menu. All of these fields can apply to any diagnostic test.

The following four fields select which modules will be tested and which functional tests will be run. Refer to the numbered callouts in Figure 3-21 while reading the following paragraphs.

(1) **MODULE** — This field can be set to ALL or SINGLE. ALL causes all modules in the system to be tested. SINGLE allows modules to be tested individually.

(2) **SLOT** — This field only appears when the MODULE field is set to SINGLE. Use the data entry keys to enter the slot number of the module to be tested.

When the cursor enters this field, the DAS displays the slot locations of the modules installed in the mainframe. The failed module is highlighted in the display.

(3) **MODE** — This field only appears when a slot number has been entered in the SLOT field. MODE can be set to ALL or SINGLE. ALL causes most of the functions for the selected module to be executed in sequence. SINGLE allows individual functions to be selected.

When the cursor enters this field, the DAS displays a list of the test functions available for the selected slot.

(4) **FUNCTION** — This field appears when the MODE field is set to SINGLE. Use the data entry keys to enter the number of the diagnostic function to be run.

The following two fields influence the way the selected functional tests are run by the DAS.

(5) **LOOPING** — This field is always present and may be set to either ON or OFF using the SELECT key. When the field is set to ON, the looping feature allows one test or sequence of tests to be run continuously. Use this feature to catch intermittent faults or for circuit tracing with an oscilloscope.

(6) **DISPLAY** — This field only appears when the LOOPING field is set to ON. The DISPLAY field can be set to ON or OFF. When it is set to OFF, the Controller board stops allowing direct memory access for the display monitor whenever a test is running. This allows the diagnostic test that is looping to run continuously without interruptions. Use this mode to perform circuit tracing with an oscilloscope.

NOTE

If an error occurs while a diagnostic test is running and the display is turned off, the LOCKOUT and REMOTE lights are turned on.

For more detailed information regarding the Diagnostics menu or the functional tests, refer to the Maintenance: Diagnostic Test Descriptions section of this manual.

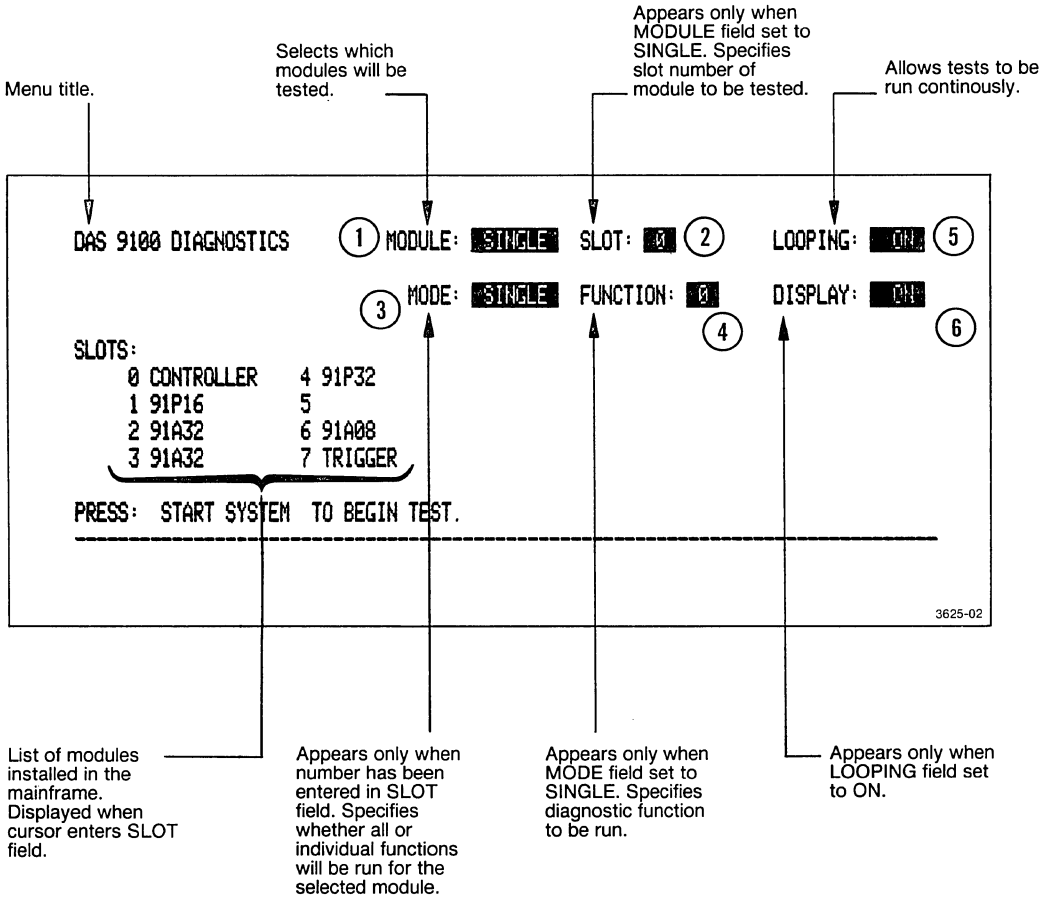


Figure 3-21. Display of the Diagnostics menu.

PROBE SELF-TEST

The DAS provides a special probe self-test capability. The test requires that your DAS contain a 91P16 Pattern Generator Module, a data acquisition module, and a diagnostic lead set. (The diagnostic lead set is standard with every mainframe.)

The probe self test operates in the following way. One pattern generator probe and one data acquisition probe are connected together via the diagnostic lead set. The DAS is started. A special power-up program is sent out from the pattern generator and acquired by the data acquisition probe. This program creates a specific display pattern. If the pattern is correct, then the two probes are functional.

The following paragraphs describe the various steps to this test. Read these paragraphs carefully before attempting to test a probe.

Connecting the Probes to the DAS

The pattern generator probe to be tested must always be connected to the 91P16 module's pod connector B.

The data acquisition probe should be connected to pod A of the 91A32 module installed closest to the Trigger/Time Base Module. If no 91A32 modules are installed in the mainframe, then the data acquisition probe should be connected to pod C of the 91A08 module installed in bus slot 6.

NOTE

If you use other data acquisition probe locations, make sure that the Trigger Specification menu is set in the appropriate operating mode for the module being used.

Connecting the Diagnostic Lead Set

Figure 3-22 illustrates how the pattern generator and data acquisition probes are connected to the diagnostic lead set. Make sure all of the following conditions are true:

1. The data acquisition ground lead from the diagnostic lead set is connected to the GND DIAGNOSTIC location.
2. The pattern generator ground lead from the diagnostic lead set is connected to the V_L location if using a P6455 TTL/MOS probe, or to the V_H location if using a P6456 ECL probe.
3. The threshold range switch on the data acquisition probe is set to NORM.
4. The diagnostic switch on the pattern generator probe is set to AUX.

NOTE

If you are using a P6456 ECL Pattern Generator probe, you must enter the Channel Specification menu and set the data acquisition probe's threshold to variable (VAR).

Starting the Probe Test

Once the probes have been connected, press the START SYSTEM key. This key starts the data acquisition and pattern generator functions simultaneously. At the top of the screen a message appears reading ACQUISITION AND PATTERN GENERATOR STARTED.

Displaying the Test Pattern

When the operation is completed, the DAS automatically displays the State Table menu. Figure 3-23 illustrates how this menu should appear. The data from the data acquisition probe being tested should show the repeating pattern: 00, 01, 02 ,04, 08, 10, 20, 40, 80, FF, 00, and so on.

To view the pattern in the Timing Diagram menu, press the TIMING DIAGRAM menu key. Figure 3-24 illustrates a display of this pattern. To achieve a similar display, you must increase the waveform magnification of the menu to 10. This is accomplished by positioning the cursor in the menu's MAG field and pressing the INCR key.

NOTE

When using the Timing Diagram menu display, you may need to enter the active data acquisition channels into the menu's POD and CH fields.

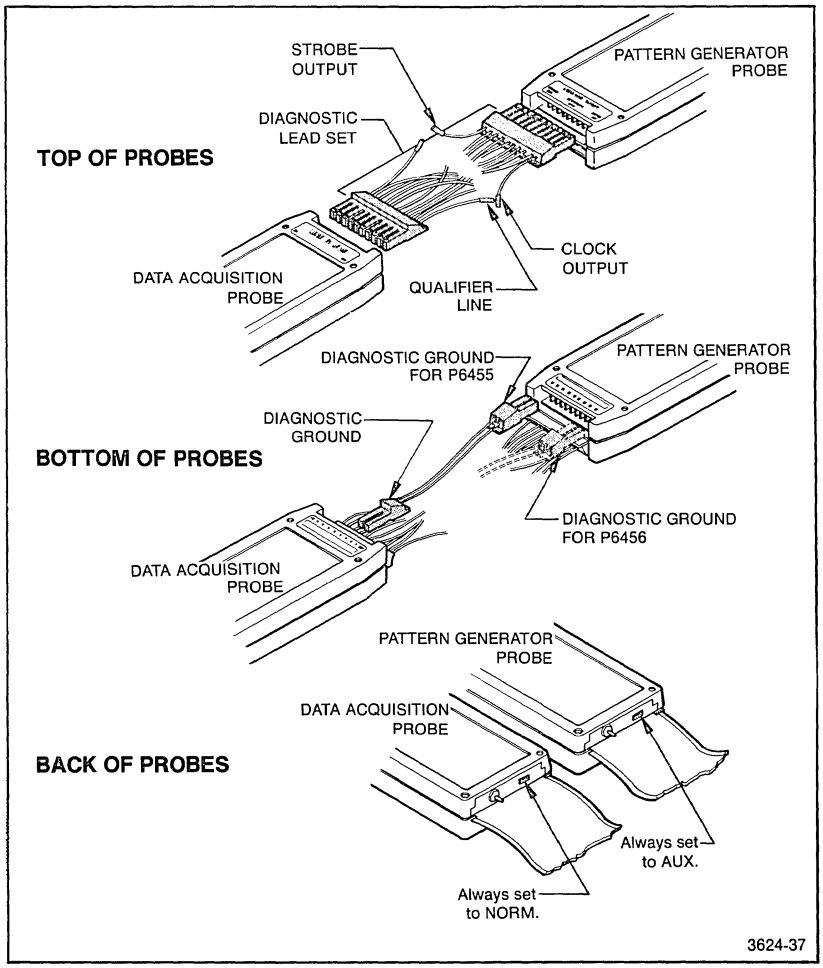


Figure 3-22. Connecting the Diagnostic Lead Set.

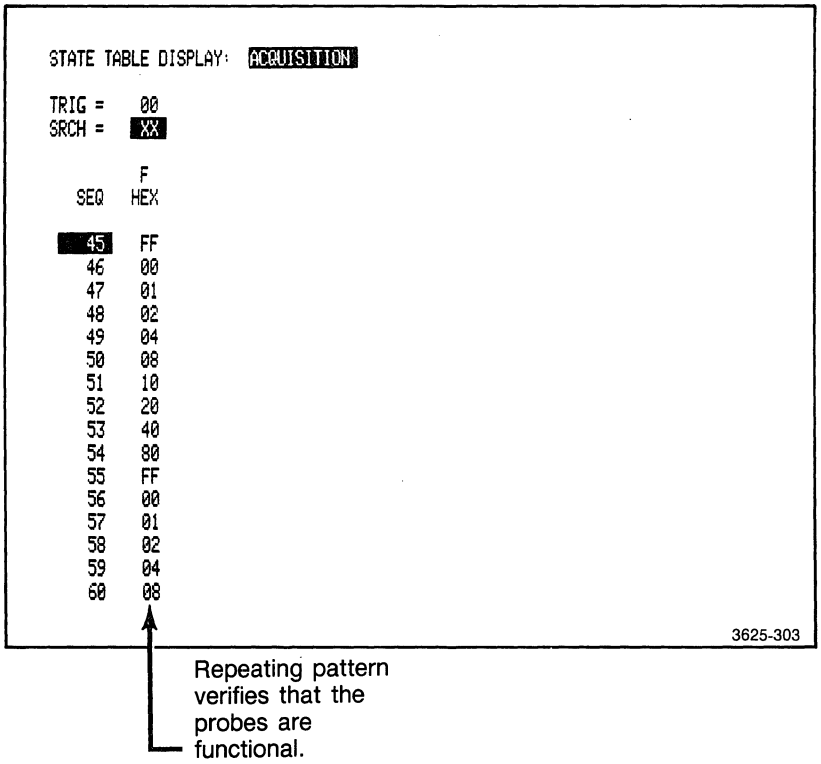


Figure 3-23. State Table display of probe self test.

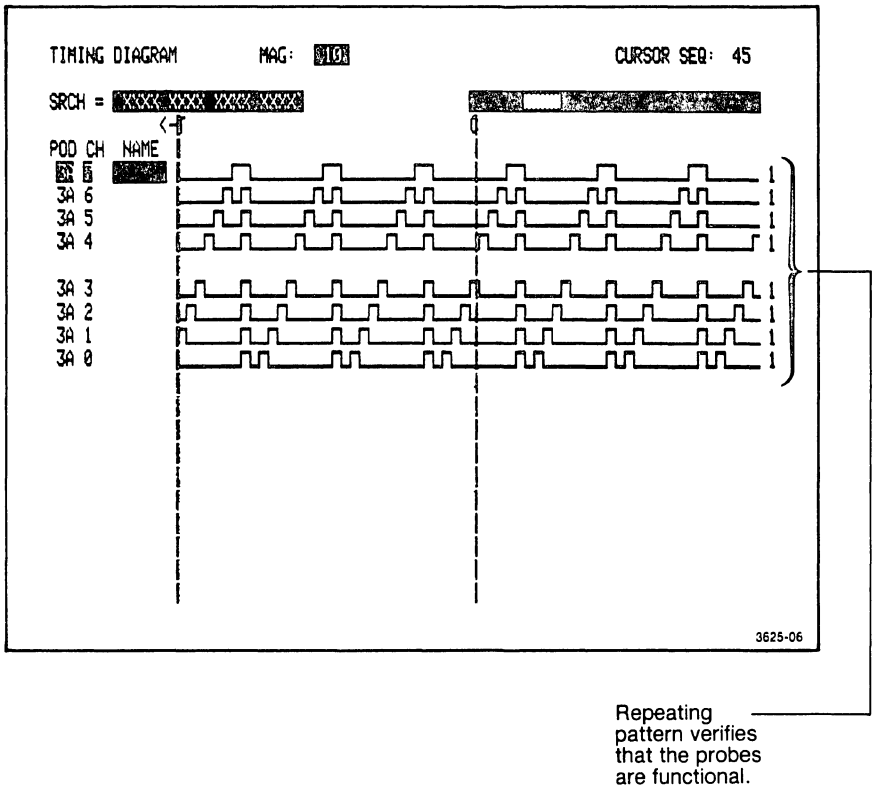


Figure 3-24 Timing Diagram display of probe self test.

COLOR DISPLAY (DAS9129 COLOR MAINFRAME ONLY)

The DAS9129 Mainframe features a color-coded display. All menu displays appear on a black background, and their information is catagorized by a three color code. The DAS Operator's Manual contains complete descriptions (with color pictures) of these displays.

THEORY OF OPERATION 4

THEORY OF OPERATION

SECTION ORGANIZATION

This Theory of Operation section is offered to familiarize service personnel with both general and specific system circuitry functions. The section is divided into three main parts. Part one consists of the System Architecture, which explains circuit board and module functions and positioning. Part two is a General System Description. Part three is a Detailed Circuit Description.

When using any section part, reference may be made to the system schematics as well as to the System Block Diagram and to all system schematics as well as to figures and tables within the text. The System Block Diagram and schematics for all DAS circuitry are located and tabbed in the Diagrams section.

Use the System Block Diagram especially in conjunction with the General System Description part of this section. Blocks on the System Block Diagram correspond to subheadings in the General System Description.

Use the system schematics especially in conjunction with the Detailed Circuit Description. Schematics are referenced to section headings and subheadings by corresponding numbers in diamonds.

Diagrams and schematics in the Diagrams section as well as this Theory of Operation section may also be valuable as a reference when troubleshooting system circuitry. Specific troubleshooting information is presented in the Maintenance sections of this manual, found in volume 2.

NOTE

Unless otherwise specified, the text, tables and figures in this section refer to both the Monochrome DAS (9109). and the Color DAS (9129). Differences are called out as they occur.

LOGIC CONVENTIONS

Digital logic techniques are used to perform most functions within this instrument. Function and operation of the logic circuits are represented by standard logic symbols and terms. All logic functions are described using the positive logic convention. Positive logic is a system of notation whereby the more positive of two levels is the true, or 1 state; and the more negative level is the false, or 0 state.

In logic descriptions, the more positive of the two logic voltages is referred to as high, and the more negative state as low. The specific voltages which constitute a high or low state vary between different electronic devices.

Whenever a line name on a schematic is referred to within the text, that line name may be followed by either (H) or (L). If the schematic line name has an overscore (is asserted low), that line name will be followed by (L) within the text. If the schematic line name does not have an overscore, that line name may be followed by (H) within the text to indicate that the line is asserted high.

SYSTEM ARCHITECTURE

DAS MAINFRAME

The DAS mainframe is supplied from the factory with a keyboard, a display monitor unit, a Main Power Supply board, an Interconnect board, a Controller Module, a Trigger/Time Base Module, and a +5 V Power Supply Module. A probe for external clock inputs is also supplied with the Trigger/Time Base Module. The display monitor is mounted at the front of the mainframe and the keyboard is attached in front, below the CRT. See Figure 4-1 for board and module positioning.

WARNING

The installation, removal, or repositioning of any DAS module requires the removal of the mainframe top cover and the module compartment cover. Only these two covers may be removed by the user. Removal of other covers exposes potentially dangerous voltages. Only qualified personnel may remove covers other than the mainframe top cover or the module compartment cover.

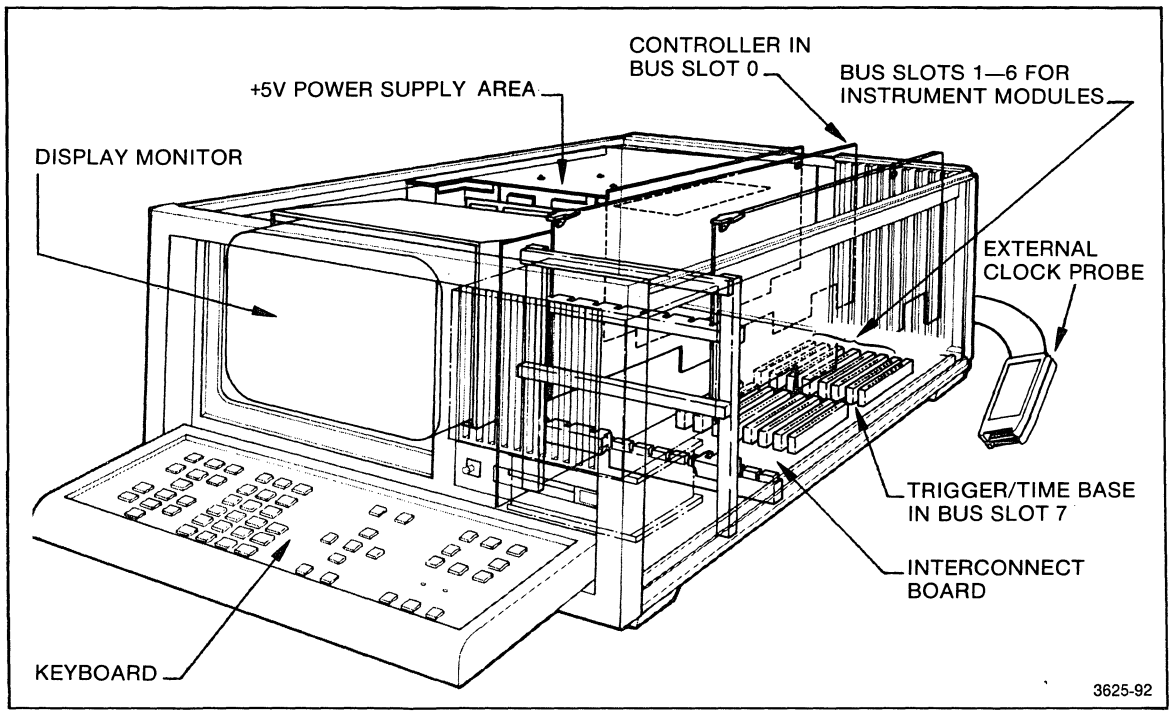


Figure 4-1. DAS Mainframe parts. This figure shows the Monochrome DAS (9109). The Color DAS (9129) is similar.

Instrument modules for test operations such as data acquisition or pattern generation are mounted in bus slots 1 through 6 between the original Controller and Trigger/Time Base Modules. Optional hardware and modules may be placed in the mainframe when ordered, or may be field installed.

KEYBOARD

The keyboard serves as the operator's interface. When the keyboard is folded into the mainframe, it holds the power switch in the off position, which disables the DAS power.

Refer to the Operating Information section of this manual or to the DAS 9100 Series Operator's Manual for user information.

DISPLAY MONITOR

The display monitor is a 9 inch CRT with etched circuit boards, mounted on a chassis. The chassis is fixed to the DAS mainframe. Any display on the CRT is arranged by the Controller with system firmware and controlled by the operator through the keyboard (see Figure 4-1).

NOTE

Some of the technical data in this manual that pertains to the Motorola Display Monitor used in the Monochrome DAS (9109) has been taken verbatim from corresponding Motorola (©) instruction manuals. Permission for using that material has been granted by Motorola Corp. and credit in general is hereby documented.

The display monitor in the Color DAS (9129) is a product of Tektronix, Inc.

MAIN POWER SUPPLY

The Main Power Supply provides +12 Vdc, −12 Vdc, +6 Vdc and −5 Vdc to all system circuitry. These voltages are carried through a bus on the Interconnect board. The Main Power Supply also supplies the +5 Vdc to slots 0 and 7 on the Interconnect board and, therefore, to the Controller and Trigger/Time Base Modules.

NOTE

Only bus slots 0 and 7 are supplied with +5 Vdc from the Main Power Supply board. Other slots must be powered by +5 V Power Supply Modules as explained in the +5 V Power Supply description following.

The Main Power Supply board is positioned in the DAS Mainframe as illustrated in Figure 4-1.

+5 V POWER SUPPLIES

At least one +5 V Power Supply Module must be installed in a DAS mainframe. Each supply provides +5 Vdc for two instrument modules. A maximum of three of the +5 V modules may be installed on the mainframe; in this case, all of the bus slots on the mainframe receive power. See Table 4-1 for +5 V Power Supply positioning information.

NOTE

The presence of +5 V Power Supplies in a mainframe is indicated by the presence of a metal button in the cover over the power supplies. The power supply cover also indicates which bus slots are receiving +5 V power.

Table 4-1
+5 V Power Supply Positioning

Module Position	Bus Slots Powered
[a] Left (standard module)	1 and 2
Center	5 and 6
Right	3 and 4

[a] The left side is the operator's left as he faces the front of the mainframe.

INTERCONNECT

The Interconnect etched circuit board is fixed at the bottom of the DAS mainframe. It provides the means of connecting and powering modules to create a system (see Figure 4-1).

The plugs for the Controller, Trigger/Time Base, and instrument modules are in tandem pairs and are referred to as bus slots 0 through 7. These eight slots are numbered from 0 to 7 (left to right viewed from the front of the DAS mainframe). Instrument modules are installed in slots 1 through 6. The bus slot numbers may be found on the black fan housing in front of the module compartment.

Connectors are provided for the positioning of three +5 V Power Supply Modules (see Figure 4-1). Each of these power supplies provide +5 Vdc to two module bus slots. Not all DAS models have all bus slots powered. If needed, additional +5 V Power Supplies are available as options. Refer to the previous +5 V Power Supply discussion for details.

Connectors and plugs are also provided for installation of options. Optional hardware is explained later and illustrated in Figure 4-5, DAS options hardware.

The Interconnect board also contains a ±160 V power supply. This power supply provides power for the Main Power Supply and any +5 V Power Supplies. The Interconnect also has a +11.3 V power supply to provide start-up power to the switching power supplies, as well as a +3 V supply to bias the ECL bus lines.

CONTROLLER

The Controller Module contains the microprocessor, system RAM, and other components necessary for controlling all functions of the DAS system.

The Controller Module is an etched circuit board with connector pins on its bottom edge that plug into slot connectors on the Interconnect board. Slot 0 on the Interconnect board is dedicated to the Controller Module. Physically, the Controller Module will fit into any slot on the Interconnect board; however, circuitry prevents proper operation from any but slot 0 (the left-most bus space as viewed from the front of the mainframe). Refer to Figure 4-1 for proper Controller Module positioning.

NOTE

The Controller board will operate only in Interconnect bus slot 0. In any other position, neither the module nor the system will function properly.

TRIGGER/TIME BASE

The Trigger/Time Base Module provides all internal clocks for DAS instrument modules and holds some of the Controller's ROM. The Trigger/Time Base must be installed in bus slot 7 for the DAS to operate. The Trigger/Time Base receives all of its power from the Main Power Supply.

The Trigger/Time Base Module provides the internal clock circuitry for the system, and provides the controls for complex triggering based on word recognition.

Three possible external clocks for acquisition (CLK1, CLK2, and CLK3) and four signals to control pattern generator modules (PG CLK, PG INHIBIT, PG INTERRUPT, and PG PAUSE) are channeled through the Trigger/Time Base. They are input through the External Clock Probe and are menu controllable.

P6452 External Clock Probe

The Trigger/Time Base Module is supplied with a P6452 External Clock Probe. The probe supplies three external clock lines and four pattern generator control lines to the system. These signals are controlled by the DAS menus. The probe plugs into the Pod C connector on the rear edge of the Trigger/Time Base etched circuit board (see Figure 4-2).

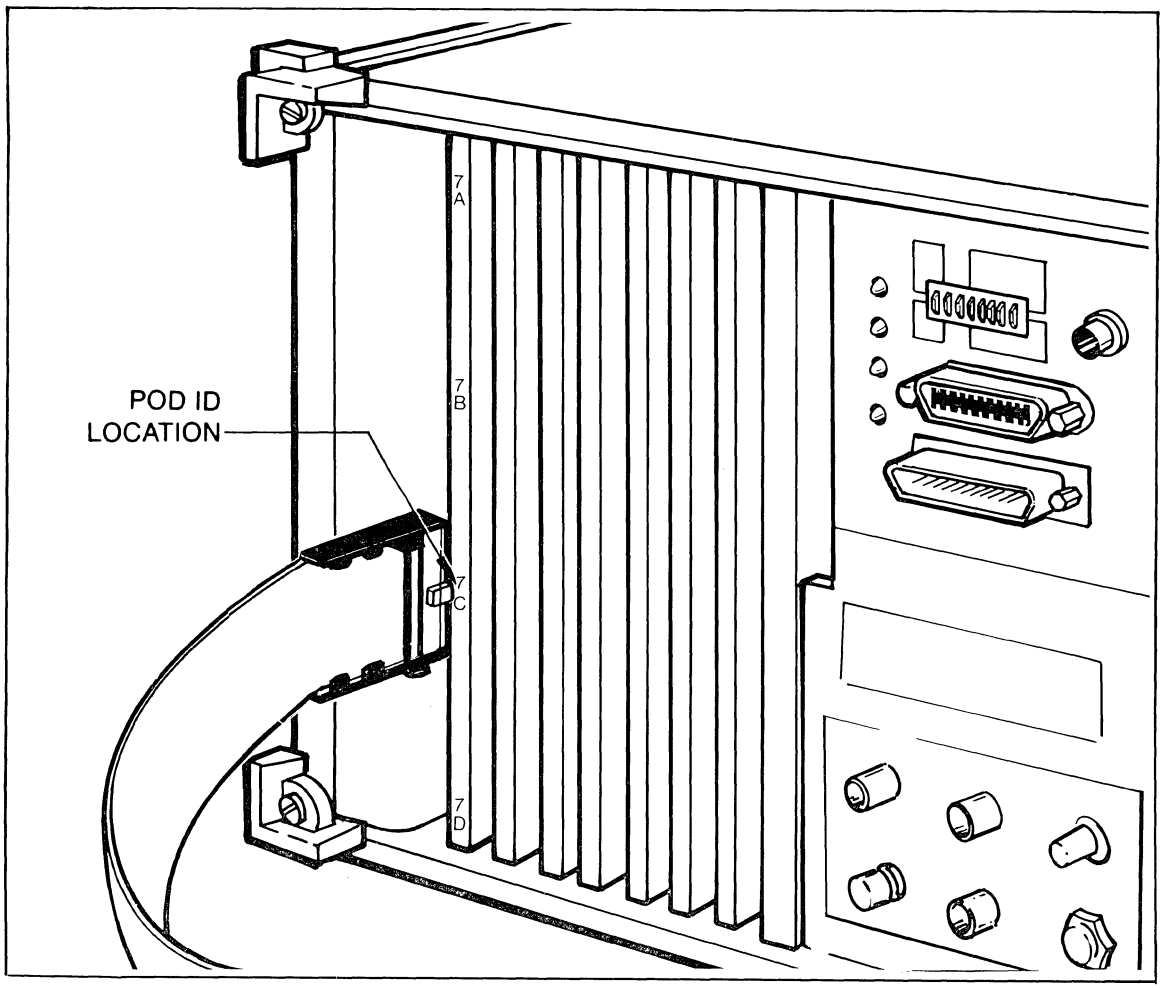


Figure 4-2. Location of the P6452 External Clock Probe.

DATA ACQUISITION MODULES (WITH PROBES)

91A32 DATA ACQUISITION MODULE

The 91A32 Data Acquisition Module plugs into a bus slot (any of 1 through 6) on the Interconnect board. It is a 32-channel, recirculating data acquisition module with a maximum clocking speed of 25 MHz. Trigger events are set using menu presentations on the CRT. Control is then given to the system from the keyboard and data acquisition begins. When a word is recognized, a signal alerts trigger circuitry on the Trigger/Time Base module and the acquisition stopping sequence is initiated. When the trigger conditions are satisfied, the 91A32 stops acquiring data and the acquired data is displayed on the video screen.

Refer to Figure 4-3 for physical relationships between the modules and probes.

P6452 Data Acquisition Probe

Four P6452 Data Acquisition Probes are supplied with each 91A32 Data Acquisition Module. They plug into pod connectors A, B, C and D at the rear of the module's etched circuit board through a mainframe opening. System circuitry recognizes which probes are connected and menus display their positions.

Refer to the Operating Information section of this manual and to the DAS 9100 Series Operator's Manual for connecting probe leads and for data acquisition operating procedures.

A maximum of three 91A32 Data Acquisition Modules may be operated in one DAS. These modules may be installed in any of slots 1 through 6; however, it is recommended they be placed in ascending order with the first 91A32 in slot 2, the next going in slot 3, and the last in slot 4. This order of installation ensures interchangeability of DAS setups stored on tape.

91A08 DATA ACQUISITION MODULE

The 91A08 Data Acquisiton Module is an 8-channel recirculating data acquisition module with a maximum clocking speed of 100 MHz. Events to be recognized are selected from the displayed menu using the keyboard. With an additional keystroke, control is given to the system and data acquisition starts. When a trigger event is recognized, the acquisition stopping sequence is initiated. When the stopping sequence is finished, the stored data is displayed on the screen.

The 91A08 Acquisition Modules should only be installed in bus slots 6, 5, 4, and 3. The first 91A08 module must be installed in slot 6 in order for clocks to be received by any of the 91A08 modules. Additional 91A08 modules must reside first in slot 5, then 4, then 3 in that order; 91A08 clocks are not available in other slots. A maximum of four 91A08 modules may be operated in one DAS mainframe.

Refer to Figure 4-3 for physical relationships between the modules and probes.

P6452 Data Acquisition Probe

Each 91A08 Data Acquisition Module is supplied with a P6452 Data Acquisition Probe. The probe is plugged into connector C at the rear of the module's etched circuit board.

P6454 100 MHz Clock Probe

The external clock for 91A08 modules is usually acquired by the P6454 100 MHz Clock Probe. This probe is plugged into a coaxial connector on the rear edge of the 91A08 module installed in slot 6. The clock probe connector is located above the acquisition probe connector.

NOTE

The P6454 100 MHz Clock Probe will only operate while connected to a 91A08 module that is installed in slot 6. Do not connect the probe to modules in other slots.

Refer to the Operating Information section of this manual and to the DAS 9100 Series Operator's Manual for information on connecting probes and for data acquisition operating procedures.

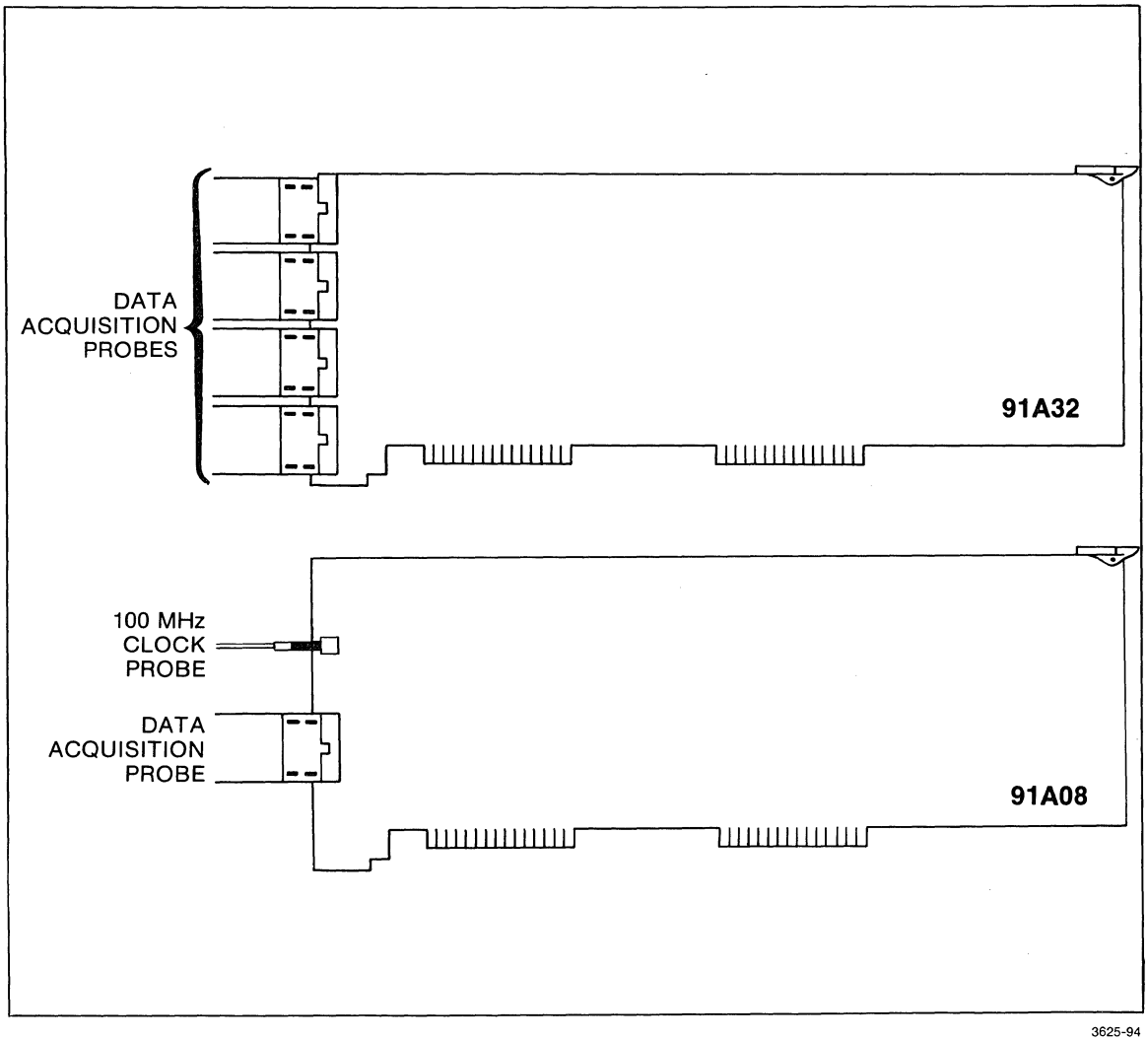


Figure 4-3. Relationship of DAS acquisition modules to probes.

PATTERN GENERATOR MODULES (WITH PROBES)

91P16 PATTERN GENERATOR MODULE

The 91P16 Pattern Generator Module will output word sequences as programmed on the Pattern Generator menu and keyed by the operator. The pattern may be generated at various speeds by internal or external clocks. Internal clocks are selectable from 5 ms to 40 ns. External clock speeds will operate pattern generation at speeds up to 25 MHz. The output is provided through two 10-channel probes (refer to Figure 4-4 for probe connector locations).

P6455 TTL/MOS Pattern Generator Probe

Two 10-channel TTL/MOS probes are supplied with each 91P16 Pattern Generator Module to output words generated. They plug into connectors B and C at the rear of the 91P16 Pattern Generator Module circuit board. This probe outputs TTL or MOS output levels depending on the V_H and V_L voltages supplied by the user.

P6456 ECL Pattern Generator Probe

The ECL pattern generator probe may be used with 91P16 Pattern Generator Modules. With the ECL probe, the pattern generator modules can output ECL data levels.

Refer to the Operating Information section of this manual and to the DAS 9100 Series Operator's Manual for probe installation and pattern generator operating procedures.

91P32 PATTERN GENERATOR EXPANDER MODULE

The 91P32 Pattern Generator Expander Module can be used only in conjunction with a 91P16 Pattern Generator Module. Together, the 91P16 and 91P32 modules can provide a maximum of 80 channels of pattern generation. Pattern selection is made from the keyboard with reference to the Pattern Generator Menu. Output from the 91P32 Pattern Generator Expander is through four 10-channel probes (probe connections explained below).

P6455 TTL/MOS Pattern Generator Probe

The four 10-channel probes plug into pod connectors A, B, C and D at the rear of the 91P32 Pattern Generator Expander Module circuit board (see Figure 4-4). The probe outputs TTL or MOS level data depending on the V_H and V_L voltages supplied by the user.

P6456 ECL Pattern Generator Probe

This probe, which puts out ECL-level data, may be used with the 91P32 Pattern Generator Expander Module.

Refer to the Operating Information section of this manual and to the DAS 9100 Series Operator's Manual for probe installation and pattern generator operating procedures.

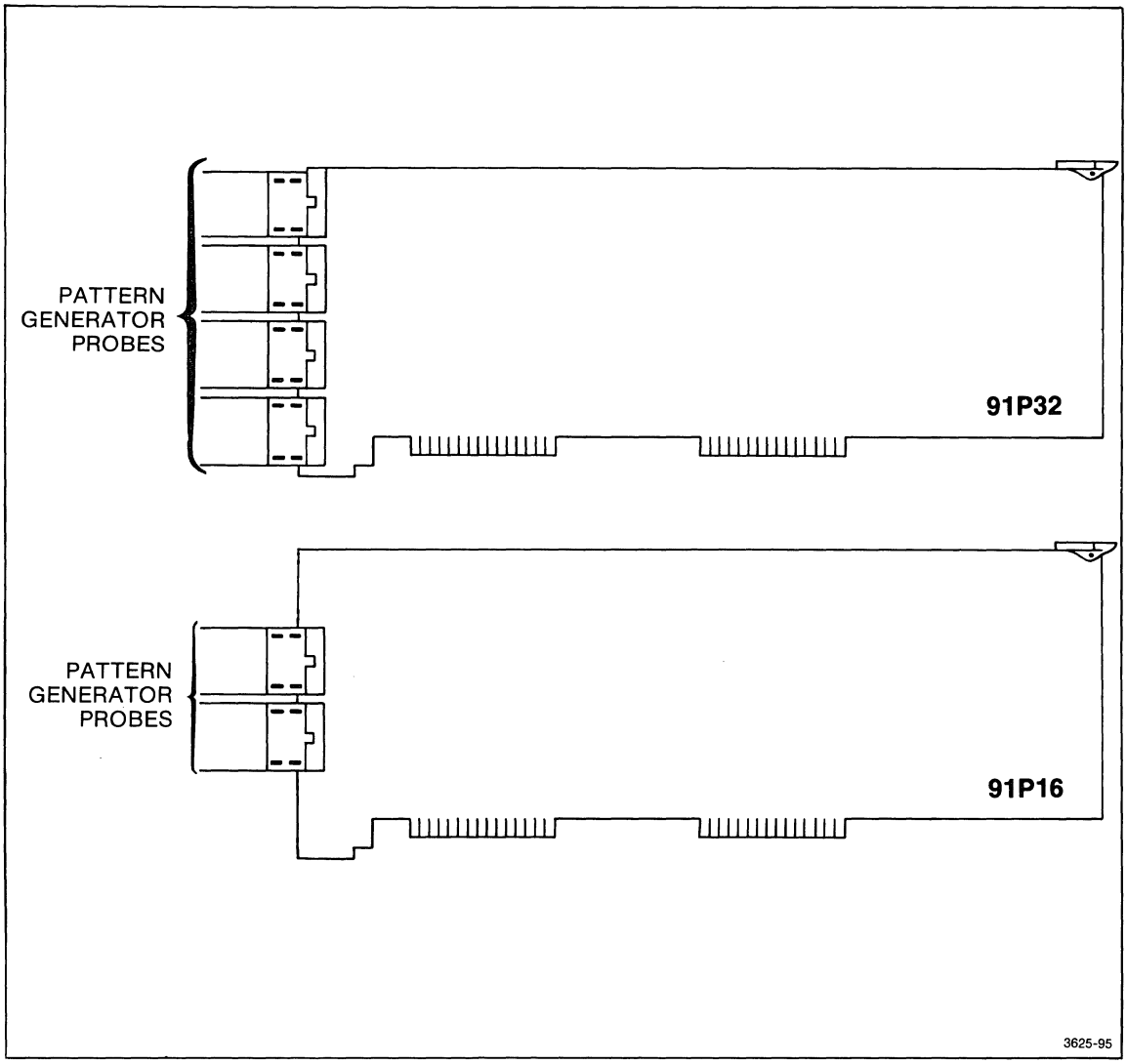


Figure 4-4. Relationship of DAS pattern generation modules to probes.

OPTIONS

OPTION 01 (TAPE DRIVE FOR DC100-TYPE CARTRIDGES)

When the DAS Option 01 is ordered, a tape drive for DC100-type cartridges is installed in the mainframe. The drive's components and etched circuit boards are located under the mainframe's front fan. The tape cassette is inserted in a covered slot located above the keyboard, adjacent to the power on/off switch. The tape unit is operated through the Input/Output menu. Figure 4-5 shows the location of the tape drive.

Refer to the Operating Information section of this manual and to the DAS 9100 Series Operator's Manual for tape drive operating procedures.

OPTION 02 (I/O INTERFACE)

Option 02 may be ordered with a DAS mainframe or added to the system. It provides interfaces for GPIB, RS-232, and Composite Video. An etched circuit board is plugged into a space on the Interconnect board and interface connectors are mounted on a board that is fixed in back of the mainframe. The Input/Output menu controls the I/O Interface. Figure 4-5 shows the location of the I/O Interface in a DAS mainframe.

Refer to the Operating Information section of this manual and to the DAS 9100 Series Operator's Manual for I/O Interface operating procedures.

NOTE

The I/O Interface Board is in the same area in the Color DAS (9129) as it is in the Monochrome DAS (9109), but is on the opposite side of the mainframe center divider panel.

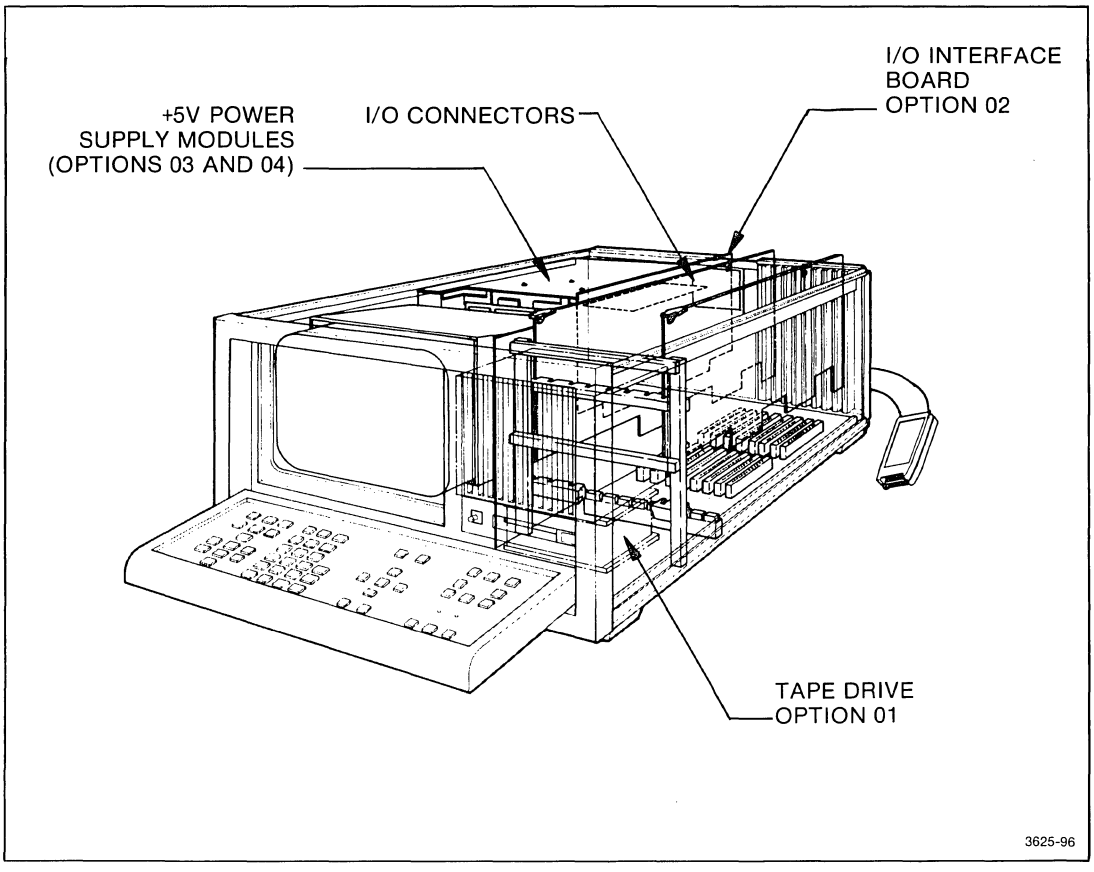


Figure 4-5. DAS option locations.

OPTION 03 (+5 V POWER SUPPLY MODULE)

One additional +5 V Power Supply module is supplied with an order that includes Option 3. This supply powers an additional two bus slots of the mainframe so that a total of four bus slots are powered.

OPTION 04 (TWO +5 V POWER SUPPLY MODULES)

Two +5 V Power Supply modules (in addition to the one supplied originally with the Mainframe) will be supplied with an order that includes Option 04. These power supplies are sufficient to power all of the bus slots on the mainframe Interconnect Module.

OPTION 05 (RACKMOUNT HARDWARE)

Option 05 provides all the hardware necessary to rackmount the DAS mainframe.

OPTIONAL ACCESSORIES

The two optional accessories particularly applicable to servicing the instrument are listed below. Refer to the Introduction and Specifications Section in this manual for a complete list of optional accessories.

SERVICE MAINTENANCE KIT (067-0980-00)

This kit contains all the extender boards and cables necessary to gain service access to all parts of any DAS configuration.

SETUP/HOLD TEST FIXTURE (067-1037-00)

This fixture provides the fastest and easiest way to verify setup and hold times met by the 91A32 and 91A08 acquisition modules. The fixture requires a single width in a Tektronix TM 500 Oscilloscope mainframe.

GENERAL SYSTEM DESCRIPTION

The DAS (Digital Analysis System) 9100 Series may be configured to accomplish the following basic operations:

1. Data acquisition of up to 104 channels at speeds up to 25 MHz (up to 32 channels can acquire at speeds up to 100 MHz).

2. Pattern generation at speeds up to 25 MHz.

3. Combined data acquisition and pattern generation.

4. Tape drive control and I/O interface control of the above operations.

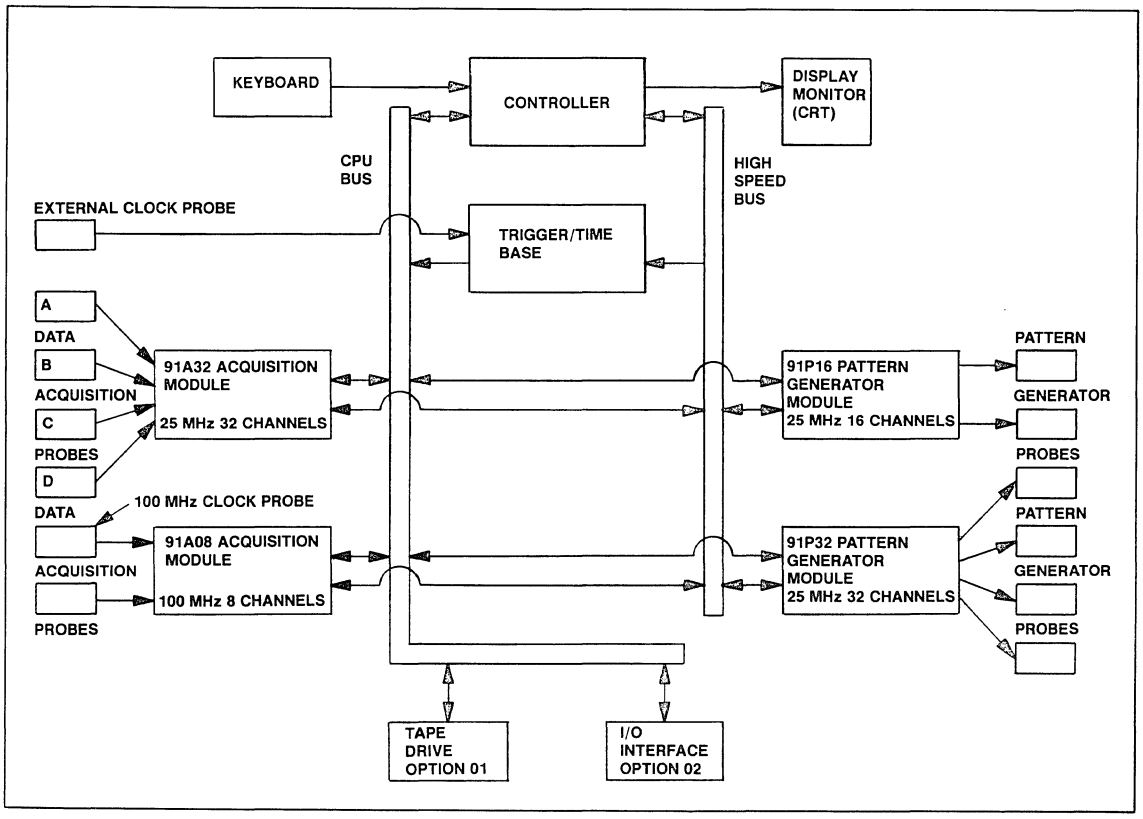
The DAS can be operated as a simple eight-channel acquisition system, as an interactive system consisting of multiple 32 and 8 channel modules, or as two independent logic analyzers. Also, a BNC connector on the rear panel provides a trigger output for use with an oscilloscope or other user equipment. In total, there are at least nine different modes in which the DAS can be used to acquire data.

Refer to the Detailed Circuit Description (later in this section) for power supply and Interconnect information.

Refer to Figure 4-6, DAS Instrument System, and the DAS System Block Diagram, in the Diagrams section of this manual (volume 2), for a block diagram presentation of a DAS system with one of each module and option (excluding power supplies). Block titles in the System Block Diagram are keyed to headings in the text of the General System Description.

NOTE

For text describing the schematics, refer to the Detailed Circuit Description that follows this General System Description.



3625-305

Figure 4-6. DAS instrument system.

DAS MAINFRAME

The following description is supported by the DAS System Block Diagram in the Diagrams section of this manual (volume 2).

KEYBOARD

The operator uses the keyboard to program module operation and select menus. Pressing any key will cause that key's seven bit code to be presented to the Controller's data bus. See Tables 4-2a and 4-2b for a listing of the key codes used by the keyboard. Refer to the DAS 9100 Series Operator's Manual or to the Operating Information section of this manual for procedures.

Table 4-2a
Shiftable Characters

Unshifted	Hex Value	Shifted	Hex Value
0	0	G	40
X (don't care)	13	H	52
NEXT	14	I	53
DECR	17	J	56
1	1	K	41
2	2	L	42
3	3	M	43
INCR	16	N	55
4	4	O	44
5	5	P	45
6	6	Q	46
7	7	R	47
8	8	S	48
9	9	T	49
A	A	U	4A
B	B	V	4B
C	C	W	4C
D	D	X	4D
E	E	Y	4E
F	F	Z	4F

Table 4-2b
Unshiftable Characters

Character	Hex	Character	Hex	Character	Hex
GOTO	1F	DEFINE TABLES	34	SCROLL ▽	1D
REPEAT	1D	TIMING DIAGRAM	37	SYSTEM START	26
HOLD	20	STATE TABLE	38	START ACQUISITION	28
HALT	24	DEL LINE	10	START PAT GEN	29
COUNT	1E	ADD LINE	11	COMPARE =	2A
CALL	21	SELECT	14	COMPARE ≠	2B
RETURN	22	↑	17	STORE ACQUISITION	2C
PATTERN GENERATOR	30	←	1A	FIND WORD	2D
CHANNEL SPEC	31	→	18	STOP	2E
TRIGGER SPEC	32	↓	19		
INPUT-OUTPUT	33	SCROLL △	1C		

CONTROLLER

The Controller board sets up the system configurations, performs system diagnostics, and performs all user interface functions.

Keyboard Interface and Control Circuitry

The keyboard interface buffers the data from the keyboard for inclusion on the microprocessor's data bus. The control circuitry supplies a clock for the keyboard encoder, and a clock for signaling interrupt logic that the keyboard should be read. The control circuitry also handles other interrupts, the LOCKOUT and REMOTE lights, the beeper, and the baud rates.

Interrupt Logic

The interrupt logic scans the interrupt lines (int0 — int7) at 3.68 MHz with a data multiplexer. When an interrupt is present, the microprocessor's interrupt line goes active, and stops the multiplexer from scanning. The interrupt method allows each interrupt (0 through 7) to call different subroutines. If the interrupt is not masked out, the IORQ and M1 lines of the microprocessor go active, and the bit pattern corresponding to the interrupt line is loaded on the data bus. This data is then used as part of the next address referenced by the microprocessor.

Microprocessor

A Z80A microprocessor is the controlling element for the Controller Module. The microprocessor's main functions are interpreting instructions stored in RAM or ROM, and routing of data from one place to another (from an instrument module to a system RAM, for example).

ROM and System RAM

The ROM contains the necessary instructions for powering up the DAS mainframe and interpreting the code in the system ROMs located on the Trigger/Time Base as well as ROMs that may be located on other boards (like the 91P16 or I/O Interface option). The system RAM, used for any volatile information storage, is a set of sixteen 16K x 1-bit blocks that provides 32K bytes of read-write memory.

Table 4-3
DAS Memory Map

Address	Memory
FFFF	
	Patch ROM
E000	
	Personality ROM for modules
C000	
A000	
8000	32K RAM
6000	
4000	
	Runtime ROM
2000	
	Interp ROM
0000	

Address Buffer

The address buffer isolates the microprocessor's address bus to prevent loading of the microprocessor and to isolate DMA (direct memory access) activity for the display monitor from the rest of the bus.

Data Buffer

The data buffer isolates the microprocessor's data bus to prevent loading of the microprocessor.

DMA (Direct Memory Access)

The DMA provides direct memory access for the CRT controller without the direct intervention of the microprocessor. This reduces the access time for the CRT controller and decreases the time sharing load on the microprocessor. The DMA consists of a single 8257 integrated circuit under the direction of the microprocessor and the CRT controller.

CRT Controller

The CRT controller consists of an 8275 Programmable CRT Controller. The 8275 Programable CRT Controller receives data from the DMA, stores it in a row-by-row format, and then outputs it at a rate consistent with the display monitor. The data from the 8275 includes which character should be displayed, as well as character attributes like inverse video and highlighting. The CRT Controller also provides horizontal and vertical scan timing signals for the display monitor.

Display Generator

The display generator consists primarily of a 1024 x 8 bit ROM, an eight bit shift register, and a data selector. The CRT controller writes its data to the character ROM address, which selects a line of a specific character. The bits output by the ROM correspond to the light and dark pattern of a line of the selected character. The bits from the ROM go to the eight bit shift register, which shifts the data out serially. The data selector controls which display attributes are selected.

Timing Diagram Decoding

When the timing waveform decoder is selected by the microprocessor — through the CRT controller — the General Purpose Attribute 0 (GPA0) line of the 8275 Programmable CRT Controller goes high. This line selects a special portion of the character ROM that displays digital timing waveforms instead of alphanumeric characters. The timing waveform decoder changes the way the character ROM is addressed whenever a waveform display is selected.

DISPLAY MONITOR

The display monitor is a 9 inch video monitor that shows DAS menus for control purposes. The DAS9109 presents a monochrome display. The DAS9129 presents a three-color display in red, yellow and green. Refer to the Operating Information Section of this manual, or to the DAS 9100 Series Operators Manual for details of color presentations.

HIGH SPEED BUS (P1)

The high speed bus is a seventy-two line bus with seven two-sided seventy-two pin connectors. There is one connector for each instrument module position in the DAS mainframe except for the Controller slot.

NOTE

The Controller Module has a connector in the same position as the instrument modules, but it is not part of the high-speed bus.

The high speed bus is designed for rapid information transfer between the Trigger/Time Base, acquisition modules, and pattern generation modules. Note that most, but not all, lines of the high speed bus are common to all connectors. This presents restrictions in positioning certain modules (such as the 91A08 Data Acquisition Module, for example).

CPU BUS (P0)

The CPU Bus has seventy two lines with eight two-sided seventy-two-pin connectors (36 pins each side). There is one connector for each module position if the DAS mainframe. The CPU bus provides the means by which the Controller Module gets information to and from the other modules.

TRIGGER/TIME BASE AND PROBE

The Trigger/Time Base serves two functions:

1. It can provide clock signals for all of the instrument modules of the DAS.

2. It provides complex triggering for the acquisition modules.

TRIGGER/TIME BASE CONTROLLER INTERFACE AND SYSTEM ROM

The controller interface provides for communications between the Controller Module and the Trigger/Time Base. Registers store information from the Controller when written to and also access data for the Controller Module when it is called for. Any blocks in the Trigger/Time Base Block Diagram that are identified with an asterisk (*) use data stored in the registers and/or pass information to the Controller Module via the interface.

The system ROM resides on the Trigger/Time Base where it can be accessed by the Controller. The system ROM contains the diagnostic test routines and the data-acquisition-related menus. Code required to operate the tape drive (Option 01) and the I/O Interface (Option 02) is also located on the Trigger/Time Base.

EXTERNAL CLOCK PROBE

The probe used by the Trigger/Time Base is identical to the Data Acquisition Probe used by the acquisition modules. It serves as an interface to the circuitry under test. The External Clock Probe can be used to obtain as many as three different acquisition clock lines from external circuitry. These clocks are labeled CLK1, CLK2, and CLK3. This probe also acquires four lines to control the pattern generation function; these lines are the PG PAUSE, PG INTERRUPT, PG INHIBIT, and PG CLK lines.

FREQUENCY DIVIDER

The frequency divider contains a 10 ns clock, and from that clock, provides the following clock rates: 10 ns, 20 ns, 40 ns, 50 ns, 100 ns, 1 μs, 10 μs, 100 μs, and 1 ms. Additional subdivisions of these clock rates are provided by the 91A08 and 91A32 clock select circuits.

91A08 CLOCK SELECT

One of the clocks provided by the frequency divider is chosen by a data selector and a register in the 91A32 Clock Select Circuit. The selected clock is then divided further by a programmable counter that is also controlled by a register. This clock is then applied to the 91A08 internal clock line on the high speed bus.

91A32 CLOCK SELECT

One of the clocks provided by the frequency divider is chosen by a data selector and a register. The selected clock is then divided further by a programmable counter that is also controlled by a register. This clock is then applied to the 91A32 internal clock line on the high speed bus.

PIPELINED INTERNAL TIMING SEQUENCER

The pipelined internal timing sequencer uses the clock select line from the Trigger/Time Base Controller Interface and System ROM block to choose between CLK 1 and the 91A32 internal clock. The selected clock line is then shifted through registers so that each clock pulse lines up with the proper triggering data.

The pipelined internal timing sequencer can also stop the selected clock when signaled by the 91A32 qualifier bus or the CLEAR line from the Controller.

Any block in the Trigger/Time Base identified with an A on the DAS System Block Diagram uses a clock provided by the timing sequencer.

EVENT CONDITIONER

This block accepts the EVENT 1, EVENT 2, and EVENT 3 signals from acquisition modules, and then conditions them according to the instructions from the controller interface. Conditioning may include such things as trigger on EVENT 1 OR EVENT 2, invert EVENT 2, or invert EVENT 3. The conditioned event outputs are called AAA, BBB, and CCC (not shown on the block diagram).

ARM TRIGGER

The circuitry in the arm trigger block accepts signals from the control registers and event conditioner to determine when data can get through to the A counter and the trigger. The circuit conditions signals to the A counter and may cause the A counter to be reset (depending on programming). When the A counter is finished, it signals the arm trigger circuit. The arm trigger then waits for conditions to be finished (with a BBB signal). When a BBB signal is received, the trigger is activated.

A COUNTER

The A counter increments each time an "AAA" word gets past the arm trigger block. When the number of counts equals the one's complement of the number loaded in the A counter register, an A done signal is sent to the arm trigger circuit. Satisfying the A counter is the first step in triggering the 91A32 acquisition modules.

TRIGGER

When the arm trigger circuit is done, the trigger sequence is started. This makes the 91A32 trigger delay (TRIGRD) lines active and starts the delay counter. The delay counter being done is the last triggering condition that must be satisfied, so the STOP-STORE signal occurs and the 91A32 QUAL line is pulled low. This stops the 91A32 modules.

DELAY COUNTER

The delay counter is loaded by the Controller with the one's complement of the number of clock cycles the delay counter must cycle. A signal from the trigger circuit then causes the counter to run for this predetermined number of cycles. When finished, the counter notifies the trigger circuit that the delay is finished.

DATA ACQUISITION

In the following description, refer to the DAS System Block Diagram in the diagrams section of this manual.

91A32 DATA ACQUISITION MODULE AND PROBES

91A32 Controller Interface

The controller interface provides a means of communications between the Controller Module and the 91A32. The interface stores information when written to and provides data for the Controller when called for. Any block in the 91A32 on the DAS System Block Diagram identified with an asterisk (*) uses the 91A32 controller interface.

Data Aquisition Probes

There are four data acquisition probes used with the 91A32, labeled A through D. Each probe is capable of acquiring eight lines of data. Probes A and B are also capable of receiving one qualifier line each. The probes can acquire TTL, MOS, and ECL levels. Each probe is an active device that converts unbalanced signals to balanced line signals for transmission to the acquisition module.

Probe Receivers

Each incoming line from the acquisition probes is converted from differential ECL to TTL for use by the 91A32 Data Acquisition Module.

Clock and Clock Edge Select

The clock select circuitry uses lines from the controller interface to select between the 91A32 internal clock and three possible external clocks. If an external clock is selected, its polarity is then adjusted for triggering on the rising or falling edge. The selected clock and edge are then used in the clocked portions of the 91A32. Any block in the 91A32 on the DAS System Block Diagram identified with an A uses the selected clock.

Qualifier Logic

The qualifier logic circuits receive the qualifier lines from probes A and B. The controller interface determines the functional polarity of the qualifier lines, and whether they will be used to enable data acquisition.

Login Register

The buffered data lines from the probes are clocked through registers so that data transitions occur at the same time. The output from these registers is then alternately clocked into the even and odd sides of the acquisition memory.

Memory Address Register

The memory address register (MAR) is an 8-bit counter that is clocked at the same rate as the even acquisition memory. The output of the counter is used to set the address where data is stored in both sides of the acquisition memory.

Acquisition Memory

This memory stores the data acquired by the probes in an alternating fashion. One set of 32 bits goes to the even side, the next set goes to the odd side, and the following set goes to the even side, etc. This method provides room for 512 sets of acquired data. The address of the acquisition memory is set by the memory address register.

Memory Readback

The memory readback circuits take the data from the acquisition memory and divide it into 8 bit words for transfer over the CPU bus to the Controller Module.

Word Recognizers

The word recognition block is designed to recognize three different binary words, up to 32 bits wide. The three words to be recognized are loaded into the word recognition RAM by the controller interface and labeled EVENT 1, EVENT 2, and EVENT 3. If any of these words is recognized, signals are sent on the high speed bus to the Trigger/Time Base.

91A08 DATA ACQUISITION MODULE AND PROBES

91A08 Controller Interface

The controller interface is the means of communication between the Controller Module and the 91A08. The interface accepts and stores information that is written from the Controller and also accesses data to the Controller when called for. Any block in the 91A08 diagram identified with an asterisk (*) on the DAS System Block Diagram is connected to the interface.

Data Acquisition Probe

The 91A08 uses one data acquisition probe capable of acquiring eight lines of data and one qualifier. The probe is identical to the probes for the Trigger/Time Base and the 91A32.

100 MHz Clock Probe

The 91A08 usually acquires external clock signals through the 100 MHz clock probe, not through the external clock probe of the Trigger/Time Base.

Probe Receivers

Each incoming line from the data acquisition probe is converted from differential ECL to single-ended ECL for use by the glitch and word recognizers.

Glitch and Word Recognizers

This block performs four functions. The first function is glitch identification. Glitches are identified in each data line by watching for more than one logic transition during any one clock cycle. The second function is data transmission; this allows the glitch recognition bus to output glitch data in sync with the probe data, rather than one cycle behind. Functions three and four are for triggering. The glitch data and the data word to be recognized are loaded into registers by the controller interface. If these words are recognized, signals are sent to the trigger recognizer block.

Clock and Clock Edge Select

The clock and clock edge select uses lines from the controller interface to select between the 91A08 internal clock, the 91A32 internal clock (supplied by the Trigger/Time Base), CLK1 from the External Clock probe, or the clock from the 100 MHz Clock probe. The selected clock is then used to clock the 91A08 module. The rising or falling edge of either CLK 1 or the clock line from the 100 MHz Clock Probe can also be specified. Any block in the 91A08 diagram identified with an A on the DAS System Block Diagram uses the selected clock.

Trigger Recognizer

Through signals from the controller interface, the trigger recognition circuits control whether the trigger will happen on the data word, the glitch word, or the glitch word ORd with the data word. It also determines whether the 91A08 trigger will appear on the EVENT 1 line of the high speed bus.

Arm 91A08 Trigger

The arming block determines if the 91A08 trigger needs to be armed by the 91A32 trigger words in order to complete a trigger. The arming is specified by the controller interface.

Delay Counter

The delay counter, once set by the controller interface, determines the number of clock cycles the stop acquisition signal will be delayed from the time the trigger is satisfied. The counter is loaded with the one's complement of the delay count and counts up to all ones to stop acquisition.

Qualifier Logic

The qualifier logic controls which, if any, of the following lines are used as qualifiers: the 91A32 qualifier line, and the 91A08 qualifier line. The qualifier line stops data acquisition.

Memory Address Register

The memory address register (MAR) is an eight bit counter that is clocked at the same rate as the even acquisition memory. The output of the counter is used to set the address where both sides of the acquisition memory store data.

Acquisition Memory

This memory stores the data and glitches acquired by the 91A08 for future readback by the Controller. The memory has two sides (odd and even) that are written to alternately. The address of the acquisition memory is determined by the memory address register.

Memory Readback

The memory readback circuit takes the data stored in the acquisition memory and divides it into 8 bit words to be put on the CPU bus for the Controller Module.

Difference Counter

The difference counter counts the number of 91A32 or CLK1 clock cycles between the 91A32 trigger and the 91A08 trigger. This information is then made accessible to the controller interface. The Controller Module uses this information to ensure correct timing allignment when displaying data acquired from different modules at different rates.

PATTERN GENERATION

In the following description, refer to the DAS System Block Diagram in the diagrams section of this manual.

91P16 PATTERN GENERATOR MODULE AND PROBES

91P16 Controller Interface and ROM

The controller interface block allows the Controller Module to write to and receive data from the 91P16 through the CPU bus. Any block in the 91P16 Block Diagram identified with an asterisk (*) is connected to the controller interface.

The ROM resident on the 91P16 contains the Pattern Generator menu. This ROM is accessed by the Controller to control the pattern generator portion of the DAS.

μCode Memory

The μCode memory is 256 x 16 bit RAM, only 13 bits of which are used. The μCode memory is addressed by the instruction multiplexer during pattern generation. It stores strobe initiating and tristate information as well as instruction control data. This information is loaded by the controller interface. The individual bits of the μCode memory are used as shown in Table 4-4.

Table 4-4
Pattern Generator μCode Assignments

bit 12	11	10	9	8	7	6	5	4	3	2	1	bit 0
					goto field							
1 cntl	2 field	tri-state	strb 1 sel	strb 0 sel	7	6	5	4	3	2	1	0
0	0 ← advance			←	HALT	—	HOLD	REPEAT	COUNT			
0	1 ← GOTO											
1	0 ← CALL											
1	1 ← RETURN											

The μCode memory is central to the operation of the addressing portion of the 91P16. See Figure 4-7 to see the relationship between the μCode memory and other portions of the 91P16 Pattern Generator Module.

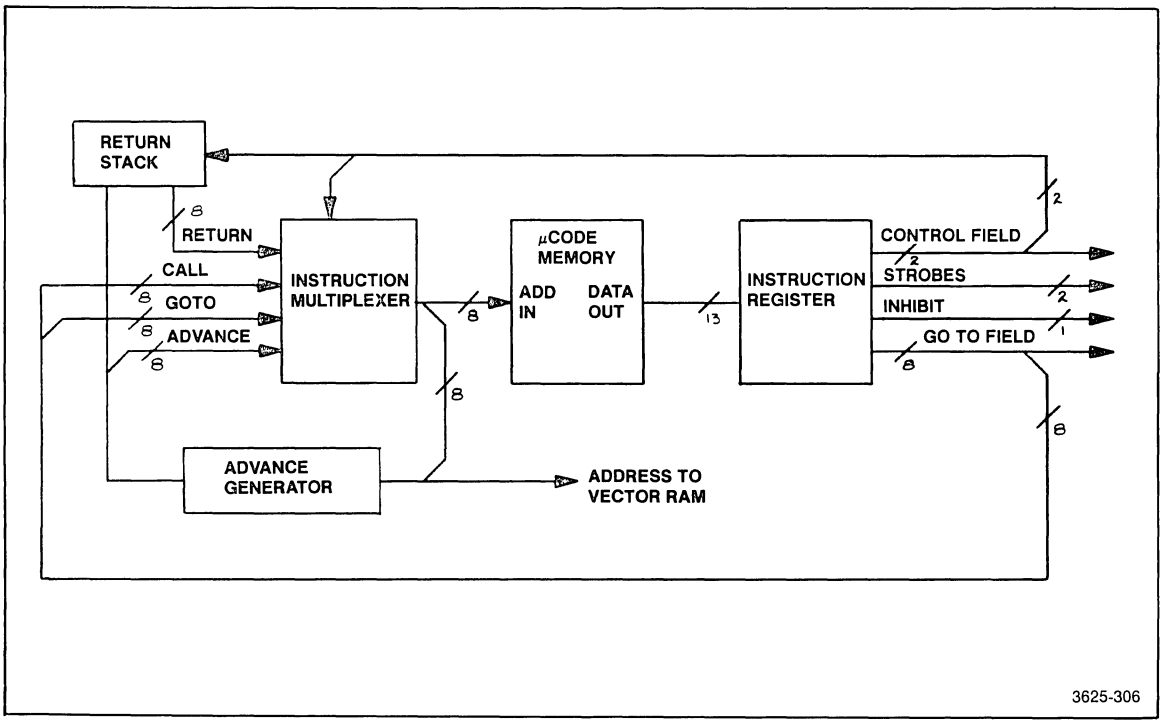


Figure 4-7. 91P16 address processor.

Instruction Register

The instruction register temporarily stores the data from the μCode memory for processing by the other blocks.

Instruction Multiplexer

The goto field and the control field from the μCode memory are interpreted by the instruction multiplexer to determine the next address for the vector memory output and the μCode memory. The instruction multiplexer can select the address from the goto field, the return stack, or the advance generator.

Advance Generator

The advance generator adds one to the address output from the instruction multiplexer. The address-plus-one is then sent to the return stack and the instruction multiplexer. The instruction multiplexer then uses the address-plus-one as the new address output if ADVANCE is the next instruction received from the control field.

Return Stack

The return stack is a push-pop memory stack that will store up to sixteen return addresses. When a GOTO instruction is received from the instruction register (or if the PG INTERRUPT line from

the External Clock probe goes active), the return stack pushes the present address-plus-one from the advance generator, into the return stack.

If a RETURN instruction is in the control field, the most recent addition to the Return Stack is used as the next address from the instruction multiplexer. The next value down is then pulled to the top of the return stack.

Vector RAM 0 and 1

This memory contains the data that is to be presented to the output latch. The data is loaded into the vector RAM through the controller interface. During operation the vector RAM is addressed by the instruction multiplexer.

Clock Control RAM

This block implements the COUNT, REPEAT, and HOLD functions. The clock control RAM is loaded with the number of clock cycles any of these functions will require. This stack is capable of storing REPEAT/COUNT/HOLD durations of up to 255 clock cycles, and up to 6 different function durations that are separately addressed. The address for the clock control RAM comes from the three least significant bits of the goto field.

When a COUNT, REPEAT, or HOLD instruction is encountered in the goto field, the clock control RAM either causes the output latches to hold on to their current data (for a HOLD or REPEAT instruction) or makes the output latches count up from the original output vector (for COUNT instructions). These actions continue for the duration of the instruction (held in the RAM).

Output Latches

This block is an output buffer for the vector memories. Values from the vector memories are clocked into the latches and held until the next value is clocked in. Under special circumstances the output latch can be caused to count up from a latched-in value (during a COUNT instruction).

Clock Control

The Pattern Generator can be run by the 91A32 internal clock, the 91A08 internal clock, or the PG CLK from the External Clock probe (of the Trigger/Time Base). The clock control block determines which clock is used. This block also selects the rising or falling edge of the PG CLK.

Once the clock is selected, three distinct clock lines are provided for the Pattern Generator. The first clock, $\underline{A}$ on the System Block Diagram, goes through the high speed bus to run any Pattern Generator Expanders in the system. The $\underline{A}$ clock runs all the time. The next clock, $\underline{B}$ on the System Block Diagram, runs the instruction register, the return stack, and the advance generator. The $\underline{B}$ clock runs all the time except when a COUNT, PAUSE, or HOLD instruction is happening. The last clock, $\underline{C}$ on the System Block Diagram, is provided through the probes to the circuit under test. The $\underline{C}$ clock runs all the time except when a HOLD instruction is being executed.

Strobe Counter

The strobe counter, when signaled by a strobe select signal from the instruction register, counts from 0 up to 1,023, unless it is reset. A reset occurs whenever the end of a strobe is detected. The counter has its own internal clock that has a 40 ns cycle time. There is only one counter for both strobes.

Strobes 0 and 1

Each strobe circuit consists of a 1024 x 1 bit RAM, a strobe done detector, and a polarity selector. The RAM is loaded with 0s and 1s by the controller interface. A low indicates a 40 ns false output and a high indicates a 40 ns true output.

When a strobe is selected by the μCode memory, the strobe counter starts counting up from zero, incrementing every 40 ns. The selected strobe has its output enabled as the counter addresses the RAM.

When the output of the RAM makes a transition from high to low, the end detect circuit is triggered, the counter is reset to zero, and the strobe output is disabled. The polarity selector controls whether the strobe outputs will be active high or active low.

Pattern Generator Probes

Two P6455 TTL/MOS Pattern Generator Probes are used by the Pattern Generator. Each probe outputs 8 bits of parallel data, a strobe line, and a clock line. The probe is an active device capable of interfacing with TTL or MOS logic.

P6456 ECL Pattern Generator Probes may be used with the Pattern Generator that allows the Pattern Generator to interface with ECL circuitry.

91P32 PATTERN GENERATOR EXPANDER MODULE AND PROBES

91P32 Controller Interface

The controller interface block allows the Controller to write to and receive data from the 91P32 Pattern Generator Expander. Any block in the 91P32 on the DAS System Block Diagram identified with an asterisk (*) is connected to the controller interface.

Program Counter

The program counter addresses both the vector memory and the μCode memory to determine what data will be output. The program counter is an 8 bit bus that is taken from the output of the instruction multiplexer of the 91P16 Pattern Generator and put on the high speed bus for use by 91P32 modules.

Clock Line

The clock used by the 91P32 Pattern Generator Expander is the A clock from the 91P16 Pattern Generator. That clock line is put on the high speed bus by the 91P16. Any block in the 91P32 on the DAS System Block Diagram identified with an A uses this clock line.

Vector RAM 2 through 5

This memory contains the data that is presented through the probe to the circuit under test. The vector RAM are loaded by the controller interface. During operation the memories are addressed by the program counter from the 91P16.

μCode Memory

The μCode memory in the 91P32 module runs parallel to the μCode memory in the 91P16. Before the module begins operation, the μCode memory is loaded with the starting positions for each strobe on the module. During operation the μCode memory is addressed by the program counter from the 91P16.

Strobe Counter

The strobe counter, when signaled by a strobe select from the μCode memory, counts from 0 up to 1023, unless it is reset. A reset occurs whenever the end of a strobe is detected. The counter has its own internal clock that has a 40 ns cycle time. There is only one counter for all four strobes.

Strobes 2 through 5

Each strobe circuit consists of a 1024 x 1 bit RAM, an end of strobe detect, and a polarity selector. The RAM is loaded with 0s and 1s by the controller interface. A 0 indicates a 40 ns duration false output, and a 1 indicates a 40 ns true output. When a strobe is selected by the μCode memory, the strobe counter starts running – counting up from 0. The selected strobe has its output enabled as the counter addresses the RAM at 40 ns increments. If the output of the RAM makes a transition from true to false, the end detect circuit is triggered, the counter is reset to zero, and the strobe output is disabled. The polarity selector controls whether the strobe outputs will be high true or low true.

Pattern Generator Probes 2 through 5

Four P6455 TTL/MOS Pattern Generator Probes are used by the 91P32 Pattern Generator Expander. Each probe outputs 8 parallel bits of data, a strobe line, and a clock line. The probe is an active device capable of interfacing with TTL- or MOS-level logic.

P6456 ECL Pattern Generator Probes may be used by the Pattern Generator Expander. This allows the module to interface with ECL level logic.

OPTIONS

OPTION 01, TAPE DRIVE

The tape drive option allows mass storage of most DAS variables; these include trigger setups, reference memory, pattern generator setups, and mnemonics tables.

The tape drive has three basic parts. These parts are data control, tape motion control, and status sensors. The data control is done through a Tektronix integrated circuit that performs parallel to serial data conversion during writes, and serial to parallel conversion during reads. The IC also does CRC calculations.

Tape motion control is performed by a custom-programmed 6500/1 microcomputer. The microcomputer sets the speed of the drive motor according to data received from the data control

board. The 6500 regulates the speed of the motor through the use of a tachometer wheel driven by the motor.

The sensor circuits include the tachometer wheel for tape speed regulation, an LED and optical sensor that detect the end and beginning of a tape, and two switches that detect whether a tape is installed and whether the tape is write-protected.

OPTION 02, I/O INTERFACE

The I/O Interface has three functions: the RS-232 interface, the general purpose interface bus (GPIB), and the composite video output. The RS-232 allows two DAS systems to be linked in a master/slave mode or allows the DAS to be controlled remotely using GPIB commands transmitted in ASCII over the RS-232. The RS-232 is implemented by an 8251A Programmable Communications Interface integrated circuit.

The GPIB on the I/O Interface is managed by a TMS 9914 integrated circuit and several buffers. The GPIB interface allows the DAS to act as a talker/listener on a GPIB controlled system.

The composite video output takes the signals going to the display monitor from the Controller and forms a composite signal for use with a hard copy unit or a video monitor.

Refer to the Detailed Circuit Description, which follows, for details about Interconnect board and power supplies, and for a detailed description of the schematics.

MAINFRAME DETAILED CIRCUIT DESCRIPTION

Refer to schematics in the Diagrams section of this manual while reading this detailed circuit description. Diagram numbers in the diamonds on page tabs in the Diagrams section are keyed to the numbers in diamonds at the relevant headings and subheadings of the circuit descriptions.

In text, signal mnemonics may be followed by (H) or (L). If the schematic signal name has an overscore (is asserted low), that signal name will be followed by (L) within this text. If the schematic signal name does not have an overscore, that signal name may be followed by (H) to indicate that the signal is asserted high.

The assembly numbers (A numbers) in Table 4-5 have been assigned to all etched circuit boards used in the DAS. When necessary, A numbers are assigned to assemblies around the ECBs. For example, the P6455 Pattern Generator Probe assembly is A15. The boards in that assembly are assigned an A number, also. The P6455 TTL/MOS Pattern Generator Probe ECB number is A15A1. Circuit boards that are fixed in the mainframe (the A2 Main Power Supply board, for example) and modules that are made up of only an etched circuit board (such as the 91A32 Data Acquisition Module) have only an assembly number — A12, A13, etc. Assemblies that do not have etched circuit boards do not have assembly numbers.

Assembly numbers are used to identify components to the board on which they are mounted. R100 could be a resistor on any board, but A1R100 identifies the resistor and the ECB.

NOTE

A numbers will be etched on circuit boards if possible. Boards that are supplied by a vendor or special Tektronix boards may not have A numbers etched on, but they are assigned and explained in the text.

Table 4-5
Assembly Numbers for DAS Assemblies and Circuit Boards

A1			DAS9109 Interconnect ECB
A2			Main Power Supply ECB
A3			+5 V Power Supply Module
	A3A1		+5 V Power Supply ECB
A4			DAS9109 Display Monitor
	A4A1		Deflection ECB
	A4A2		Signal ECB
A5			Keyboard
	A5A1		Keyboard ECB
A6			DAS9109 Monochrome Controller ECB
A7			P6452 Data Acquisition Probe
	A7A1		P6452 Data Acquisition Probe ECB
A9			P6454 100 MHz Clock Probe
A10			Trigger/Time Base ECB
A12			91A32 Data Acquisition Module ECB
A13			91A08 Data Acquisition Module ECB
A14			91P16 Pattern Generator Module ECB
A15			P6455 TTL/MOS Pattern Generator Probe
	A15A1		P6455 TTL/MOS Pattern Generator Probe ECB
A16			P6456 ECL Pattern Generator Probe
	A15A1		P6456 ECL Pattern Generator Probe ECB
A17			91P32 Pattern Generator Expander Module ECB
A18			Option 01, Tape Drive for DC100-type Cartridges
	A18A1		Tape Drive Data ECB
	A18A2		Tape Drive Servo ECB
	A18A3		Tape Drive Transport Assembly
		A18A3A1	Tape Drive Transport Assembly Sensor ECB
		A18A3A2	Tape Drive Transport Assembly Status ECB
A19			Option 02, I/O Interface
	A19A1		I/O Interface Option ECB
	A19A2		I/O Interface Connector ECB
A25			DAS9109 Capacitor Bracket
	A25A1		DAS9109 Capacitor Bracket ECB
A30			DAS9129 Color Display Monitor
	A30A1		Deflection ECB
	A30A2		Z-axis ECB
	A30A3		CRT ECB
A31			DAS9129 Interconnect ECB
A32			DAS9129 Capacitor Bracket
	A32A2		DAS9129 Capacitor Bracket ECB
A33			DAS9129 Color Controller ECB

INTERCONNECT BOARD

The Interconnect board serves two purposes. It has the bus lines and connectors that connect all of the modules and sub-assemblies of the DAS 9100 Mainframe. It also holds the ±160 V supply and the +11.3 V supply for the Main Power Supply, and any +5 V Power Supply modules.

INTERCONNECT +5 V CONNECTORS AND CPU BUS ◇1◇ AND ◇2◇

Schematics M1 and M2 (monochrome) or C1 and C2 (color) in the Diagrams section, show all connections between the Controller and every other circuit board on the DAS. Schematic 1 also shows power supply plugs. Table 4-6 shows what board or module each connector should be attached to.

Table 4-6
MAIN INTERCONNECT CONNECTORS

DAS 9109 (Monochrome)		DAS 9129 (Color)	
J100	Controller	J100	Controller
J101	Controller	J101	Controller
J10		J10	
J20		J20	
J30		J30	
J40	Instrument modules	J30	Instrument modules
J50		J50	
J60		J60	
J70	Trigger/Time Base	J70	Trigger/Time Base
J80	Test Fixture	J80	Test Fixture
J101	Main Power Supply	J101	Main Power Supply
J131	I/O Interface	J131	I/O Interface
J212		J212	
J311	5 V Power Supplies	J311	5 V Power Supplies
J321		J321	
J421	Display Monitor		
J422	Tape Drive	J422	Display Monitor
J423	Keyboard		
		J425	Tape Drive
		J427	Tape Drive
		J429	Keyboard
J431	Tape Drive		
J432	Future Use	J432	Future Use

DAS 9100 SERIES INTERCONNECT HIGH SPEED BUS AND SHIELDS ◇3◇ AND ◇4◇

The schematics M3 and M4 (monochrome) or C3 and C4 (color) show the connections between the various high speed modules in the DAS, the instrument modules and the Trigger/Time Base.

Note that the bus and shields are not the same at all connectors on the Interconnect board. This places certain restrictions on module location (discussed in the Operating Information section of this manual).

The resistors on the lines create a specific line impedance. This reduces ringing and glitches on the bus lines.

DAS 9100 SERIES INTERCONNECT ±160 V SUPPLY ◇5◇

AC Input Power

The turn-on procedure for the ac input power starts with pulling on the DAS main power switch, S100. This switch turns on the fans and the 11.3 V supply (in the other power block). When the 11.3 V supply is stabilized, relay K101 is turned on. Relay K101 supplies power to the ±160 V power supply.

The ac input power block also performs supply voltage selection. When S103 is in the 230 V position, the ±160 V power supply works as a standard bridge rectifier circuit, as shown in Figure 4-8a. With S103 in the 115 V position, the supply acts as a voltage doubler, as shown in Figure 4-8b. Switch S103 also causes the secondaries of T101 to be driven in parallel in the 115 V position, and in series in the 230 V position.

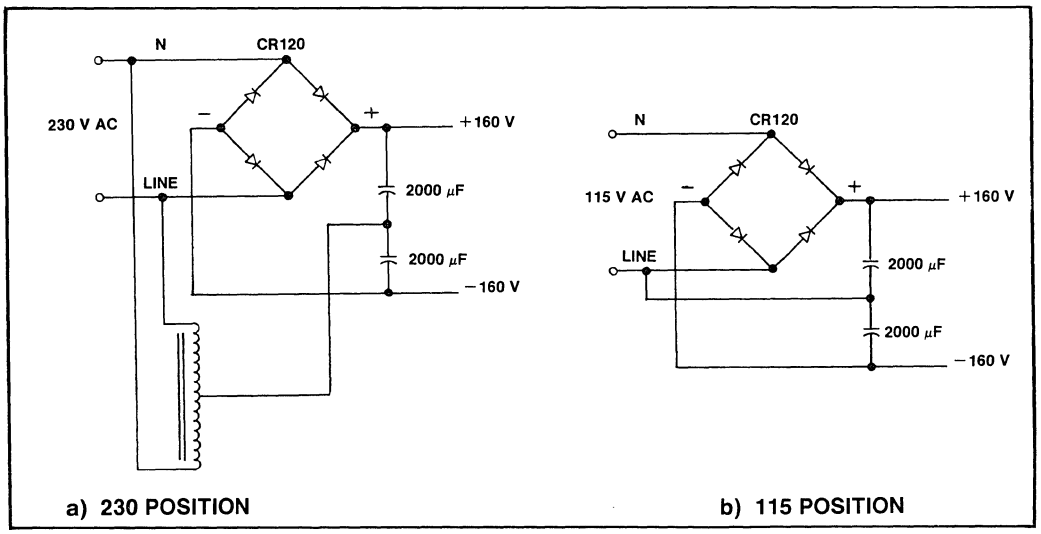


Figure 4-8. ±160 V power supply.

±160 Volt Power Supply M ◇5◇ or C ◇5◇

The ±160 V power supply receives power through relay K101, which charges ±160 V supply capacitor. The spark gaps (E124 and E125 for the monochrome DAS and E115 and E119 for the color DAS) repress line surges and spikes.

Capacitor Bracket Board M ◇5◇ or C ◇5◇

The Capacitor Bracket Board is separate from the main interconnect board. It contains the following circuitry: the main filter capacitors for the ±160 V supply, resistors to bleed off the voltage across the filter capacitors after the power is turned off, and a neon light that blinks when excessive voltage is present across the filter.

DAS 9109 Interconnect +11.3 V and +3 V supplies M ◇5◇

+11.3 V Supply. The +11.3 V start-up power supply is derived from T101 and a full-wave rectifier CR109. The supply is filtered by C102 and regulated by VR111 and Q112. As soon as the +12 V supply in the Main Power Supply is operating, the +11.3 V line is raised to +11.6 V. Q112 no longer conducts, shutting off the +11.3 V supply. The LOW LINE SENSE(H) line is used by the Main Power Supply.

+3 V Supply. The +3 V supply is controlled by the +5 V supply in the Main Power Supply. R108 and R109 provide a +3 voltage reference to the non-inverting input of op amp U110. The output of the op amp drives the base of transistor Q11 to maintain the potential on the ECL line of the high speed bus. A transistor in the feedback loop of the op amp maintains voltage accuracy.

DAS 9129 Interconnect +11.3 V and +3 V supplies C ◇5◇

+11.3 V Supply. The +11.3 V start-up power supply is derived from T101 and a full-wave rectifier CR202. The supply is filtered by C101 and regulated by VR203 and Q202. As soon as the +12 V supply in the Main Power Supply is operating, the +11.3 V line is raised to +11.6 V. Q202 no longer conducts, shutting off the +11.3 V supply. The LOW LINE SENSE(H) is used by the Main Power Supply.

+3 V Supply. The +3 V supply is controlled by the +5 V supply in the Main Power Supply. R205 and R305 provide a +3 voltage reference to the non-inverting input of op amp U207. The output of the op amp drives the base of transistor Q205 to maintain the potential on the ECL line of the high speed bus. A transistor inside the feedback loop of the op amp maintains voltage accuracy.

MAIN POWER SUPPLY

The Main Power Supply (assembly number A2) is a switching power supply with outputs of +12 V, +6 V, ±5 V, and two −12 V supplies. There is also a power supply clock and +5 V

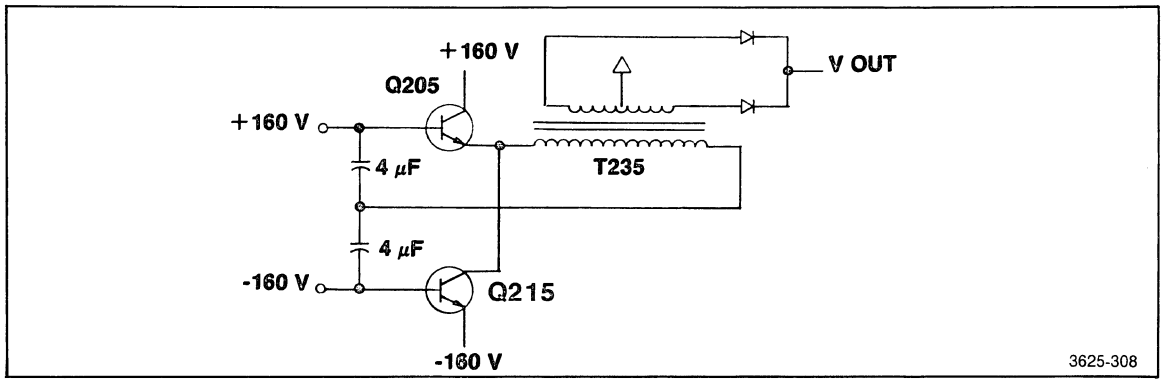


Figure 4-9. Concept of the switching power supply.

reference output. The inputs required are a ±160 V nonregulated supply, and a +11.3 V start-up supply. All component numbers in the Main Power Supply description are assumed to have A2 as a preface unless otherwise stated.

Pin 2 of U875 monitors both the +6 V SENSE and +5 V SENSE lines through a resistor network consisting of R770, R771, and R772. Diode CR783 prevents an overvoltage condition on the +6 V line from influencing the +5 V line. Capacitor C875 allows a short over-voltage condition (less than 1 ms) to occur without triggering the circuit.

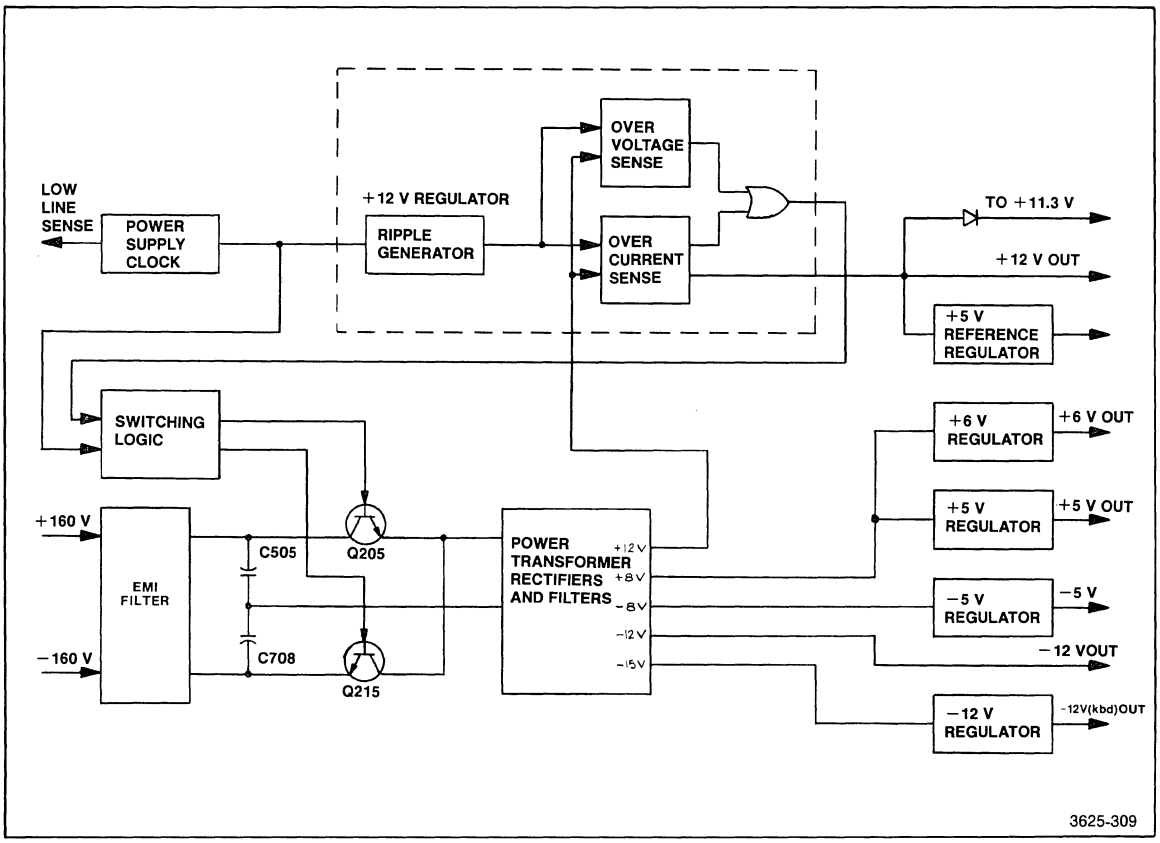


Figure 4-10. DAS Main Power Supply block diagram.

MAIN POWER SUPPLY BOARD ◇6

Power Supply Clock

The clock is built around comparator U820D. When the comparator output is high, the non-inverting input is raised to 7.5 V and C923 is charged through R921 and R819. This state continues until the voltage at the inverting input exceeds the voltage at the non-inverting input and causes the output to go to ground. Pin 13 going to ground pulls the non-inverting pin to 3.7 V and causes C923 to discharge through R819 — instead of R921 because of diode CR921.

The comparator output, pin13of U820, goes high when the charge on capacitor C923 falls below the voltage of the non-inverting input of the comparator. This ends the clock cycle.

The output of the comparator drives transistor Q916, which provides the current necessary to drive all clocked sources. The clock output looks like Figure 4-11.

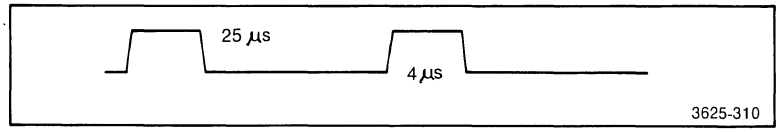


Figure 4-11. Power supply clock output.

The clock line on the Main Power Supply board clocks the +5 V Power Supply modules to make all supplies switch in phase.

The LOW LINE SENSE(H) shuts down the clock if the incoming line voltage drops below 90 V ac. The nonregulated side of the 11.3 V supply is voltage divided by R835, R836, and R942, and is compared to the +5 V reference by comparator U830A. If the non-regulated side of the 11.3 V supply goes too low, the output of U830A goes to ground, so diode CR922 conducts. Because of this path to ground, capacitor C923 cannot charge, and the clock stops. Resistor R836 provides some hysteresis so the low line sensor does not start a free-running oscillation.

Switching Logic

The switching logic drives switches Q205 and Q215 to provide pulsed dc to transformer T235. The switching is designed to provide pulse width modulation for the switches as a means of voltage regulation. U720B is a divide-by-two clocked flip-flop that writes alternate 1s and 0s to triple-input NOR gate U715B, and the inverse to triple-input NOR gate U715C. Flip-flop U720A is set by a rising edge from the over-voltage or over-current sensors, and is reset by a rising edge from the clock. The output of RS flip-flop U720A is sent to inputs of all the triple-input NOR gates in package U715. The clock is also sent to all three NOR gates. A timing diagram showing the relationships between the clock signal, the over-voltage or over-current signal, and the three NOR gate outputs is shown in Figure 4-12.

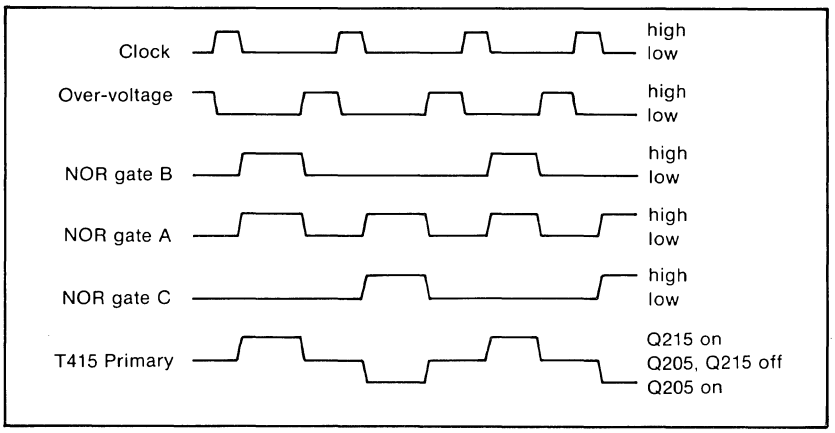


Figure 4-12. Main Power Supply switching logic.

Each of the NOR gates in U715 drives a switching transistor. If NOR gate B is high, current flows from tap 2 to tap 3 of T415, through Q518 to ground. Likewise, if NOR gate C is high, current flows from tap 2 to tap 1 and through Q514 to ground. When the over-voltage or over-current line is set, all of the NOR gates outputs are low. This situation makes Q518 and Q514 non-conducting and Q617 conducting, which shorts out transformer T415 across diodes CR513 and CR519. The short means no current will flow through T415, as can be seen in Figure 4-12.

Switches

The secondaries of transformer T415 drive the bases of switching transistors Q205 and Q215. When current flows from tap 2 to tap 3 of the base drive transformer T415, Q205 is turned on and Q215 is left off. Q205 then conducts current from the +160 V supply through the primary of T235 to charge capacitors C505 and C708. When the current to the base drive transformer is turned off, both drive transistors are turned off. As a result, no current flows through the primary of the power transformer. When transistor Q215 is turned on, capacitors C505 and C708 are discharged to −160 V through the primary of transformer T235. Then both drive transistors are turned off and the cycle repeats.

The support components for the switches include resistors R600 and R606, which bleed off capacitors C505 and C708. R224 and C223 damp ringing from the inductance of the primary of T235 when both drive transistors turn off. Diodes CR312 and CR318 limit the back EMF from the primary's inductance to the supply voltages (±160 V) to protect the driving transistors. Diodes CR306, CR308, CR315, and CR317 keep the driving transistors from saturating, so they turn off fast. Capacitors C307 and C316 bypass diodes CR306 and CR317 during turn-off.

EMI Filter

When driving transistors Q205 and Q215 switch at high frequencies, they will force high frequency interference into the supplying lines. Since this interference can disrupt other devices connected to the same line supply, it must be filtered out. T905, L701, C812, C912, and C811 are an EMI filter to block this interference before it gets to the supply line.

+12 Volt Supply

Diodes CR268 and CR258 form a full-wave rectifier off the secondary of T235, which provides the +12 outputs. Inductor L645 and capacitors C653, C845, and C745 provide filtering for the +12 V supply.

+12 Volt Sense

The outputs of comparators U830C, U830D, and U820B form an OR gate. If the +12 V line goes over-voltage or draws too much current, this OR gate output goes high; otherwise the output, pin 1 of U820B, will be low. U820B is an inverting buffer with its non-inverting terminal tied to the +5 V reference. The output is used to set flip-flop U720A.

A ripple generator is tied to the non-inverting pins of the over-voltage and over-current sensors, U830C and U830D. The ripple generator consists of comparator U820C, inverting buffer Q834 (which is controlled by comparator Q832, a constant current source), and capacitor C939. When Q834 is turned on by the clock being high, C939 is charged high. When Q834 is turned off by the

clock, the charge on C939 is drained through Q832. This causes a downward voltage ramp. The ramp wave across C939 is put through voltage divider R937 and R931 to produce a 200 mV peak to peak waveform. The ripple waveform is attached to the non-inverting side of both the over-voltage and over-current sensors to prevent the comparators from free-running, to provide for a small amount of ripple at the output, and to keep over-voltage and/or over-current control in sync with the clock rate.

The over-voltage sensor built around U830C has a line (pin 5 of P940) that ties to the +12 V supply bus to sense if the voltage gets too high. If this line should get disconnected, R944 prevents the output from going totally out of regulation. R837 and R935 divide the sensed voltage to +5 V. C725 provides loop compensation. The non-inverting input of U830C goes to the +5V reference and is coupled through a capacitor to the ripple generator.

Over-current sensor U830D looks at the voltage drop across resistor R730 through resistors R734 and R726 to the non-inverting input, and through R737 and R736 to the inverting input. These resitors form a voltage divider between the collector of Q832 and ground.

Comparator U830B can be used to force the +12 V regulator's wired OR gate to trigger at the inverse of the power supply clock for power-up testing and troubleshooting. See the Maintenance: Troubleshooting section of this manual for more information.

Over-Voltage Protection (OVP)

The over-voltage protection circuit consists of 2 special-purpose ICs (U875 and U885) and a means of pulling the power supply clock high. The +12 V supply has its own OVP in the +12 V sense circuitry. The +6 V and +5 V supplies are monitored by U875, and the +5 V supply is monitored by U885.

Pin 2 of U875 monitors both the +6 V SENSE and +5 V SENSE lines through a resistor network consisting of R770, R771, and R772. Diode CR783 prevents an overvoltage condition on the +6 line from influencing the +5 V line. Capacitor C875 allows a short over-voltage condition (less than 1 ms) to occur without triggering the circuit.

Pin 2 of U885 monitors the −5 V SENSE line through resistor network R888 and R887. Capacitor C887 allows a short over-voltage condition (less than 1 ms) to occur without triggering the circuit.

If either U875 or U885 detects an over-voltage condition, SCR Q985 is turned on through diode CR980 or CR981. These diodes act as an OR gate for the over-voltage condition. When the SCR is turned on, the base of transistor Q918 is pulled low. This brings the collector of the transistor close to 11.3 V (supplied by the emitter). The high voltage from the collector supplies enough current to pull the output of the power supply clock high; so the clock line no longer pulses. This turns off all power supplies that use the power supply clock (this includes the entire Main Power Supply and all +5 V Power Supplies in the mainframe).

+5 Volt Reference

The +5 V reference derives power from the 11.3 V power-up supply on the Interconnect board until the +12 V supply is operating. Then diode CR738 conducts and allows the +12 V supply to take over. The +5 V reference is Zener diode VR931 between the ground sense line and the non-

inverting side of comparator U820A. The comparator is wired as an op amp. The +5 volt reference can be adjusted through the use of variable resistor R936. The reference voltage is used on the Main Power Supply board as well as by the +5 V modules as their +5 V reference.

−12 Volt Supply

Diodes CR356 and CR359, in the preregulated supplies block, form a full-wave rectifier for the −12 V supply and L850 and C665 provide filtering. Fuse F150 provides over-current protection.

−12 Volt Keyboard Supply

Since the keyboard requires a more tightly regulated supply than the regular −12 V supply, a seperate keyboard supply is used. Diodes CR357 and CR358, in the preregulated supplies block, form a full-wave rectifier. R572 and C570 form a simple RC filter to remove ripple. U975 is a standard 3-terminal, −12 V regulator. Diodes CR976 and CR977 provide protection from positive voltages and spikes. Capacitors C976 and C977 remove noise from the line.

Preregulated Supplies

The preregulated supplies output recified and filtered voltages from the main power transformer, T235. Most of these supplies have already been discussed. The last of these supplies to cover is the ±8 V supply, which supplies power to the +6 V, +5 V, and −5 V regulators.

Taps 8 and 10 of T235 provide current to a bridge rectifier consisting of CR430A, CR430B, CR355, and CR255. From the rectifiers, the current goes through filters made of L448, L425, C458, and C456. The rectifier diodes are Schottky, and because of their turn-off speed, may produce ringing that is snubbed by R532, R536, C532, and C536. This supply is used as a source for the regulated +6 V, +5 V, and −5 V supplies.

+6 Volt Supply

The +8 V supply provides a current source for series pass transistor Q170, which has its base controlled by Q172. The base of Q172 is in turn controlled by op amp U280B. U280A senses the voltage drop across current-limiting resistor R275, causing pin 1 go low if too much current is drawn. If pin 1 goes low, the non-inverting input of U280B goes to ground, which drives its output low, decreasing the current through Q170. The +6 V sense line is voltage-divided through R277 and R278 and compared to the +5 V reference by op amp U280B to control the output voltage. C275 provides compensation for the feedback loop. Zener diode VR376 provides reverse-voltage protection.

+5 Volt Supply

The +5 V regulator works in exactly the same way as the +6 regulator except two series pass transistors are connected in parallel for greater current-handling capabilities.

−5 Volt Supply

The output of the −8 V supply passes through a −5 V regulator similar to the +6 V regulator. The +5 V reference is applied across voltage divider R688 and R781. The divider provides 0 V, which the over-voltage detector then compares to ground.

+5 VOLT POWER SUPPLY MODULE

The +5 V module (assembly number A3) supplies +5 V at 18 A, which is sufficient to drive two instrument modules. The module cannot be operated without a Main Power Supply board since the Main Power Supply provides both the clock and the +5 V reference for the +5 V module. Any component numbers in the +5 V power supply circuit description are assumed to have A3 as a preface unless otherwise stated.

The +5 V module operates like the +12 V side of the Main Power Supply. Figure 4-13 is a block diagram of the +5 Volt Power Supply.

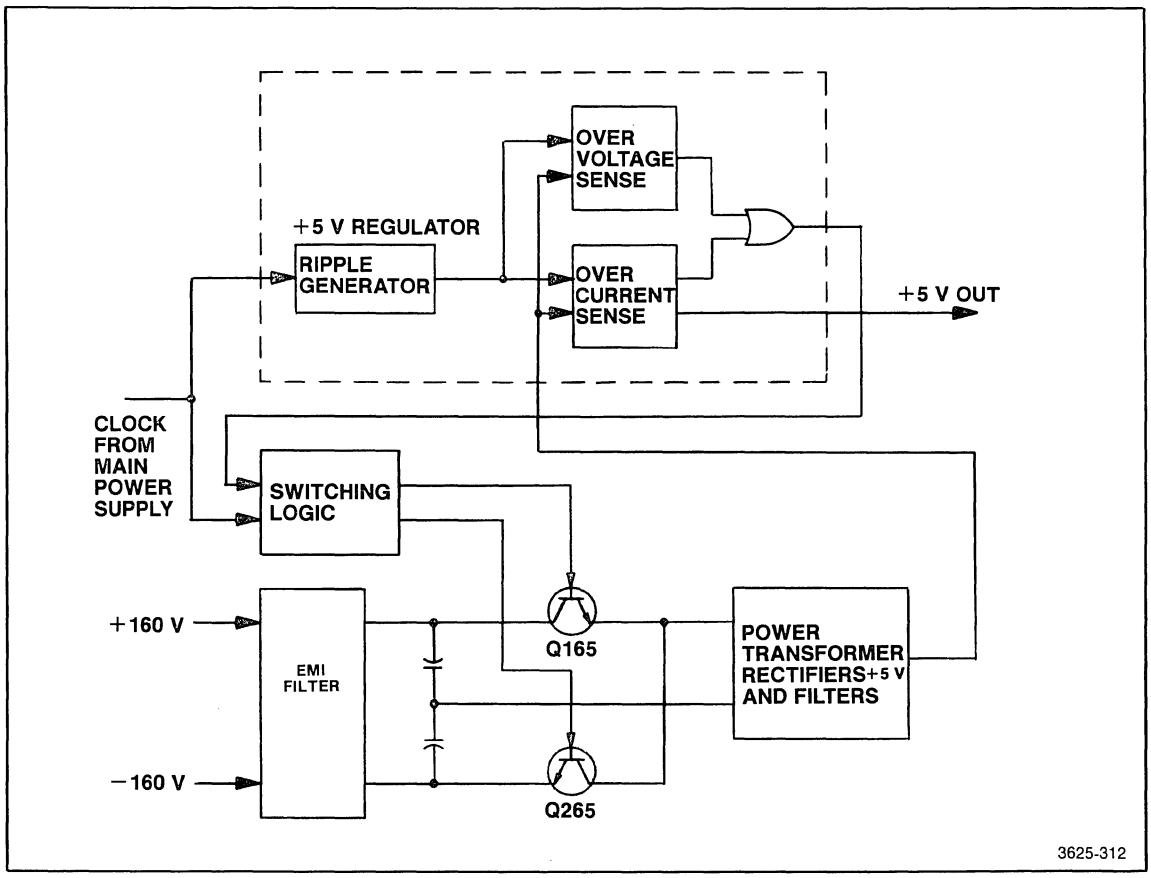


Figure 4-13. +5 Volt Power Supply block diagram.

+5 VOLT POWER SUPPLY ◇7

Power Supply Clock

The clock is provided by the Main Power Supply and is used to control the switching logic and the +5 V regulators.

Switching Logic

The switching logic drives switches Q165 and Q265 to provide pulsed dc to transformer T565. The switching is designed to provide pulse width modulation for the switches as a means of voltage regulation. The clocked flip-flop U315B is a divide-by-two that writes alternate 1s and 0s to triple-input NOR gate U215B and the inverse to triple-input NOR gate U215C. Flip-flop U315A is set by a rising edge from the over-voltage or over-current sensors in the +5 V sense circuit, and is reset by a rising edge from the clock. The output of the RS flip-flop is sent to inputs of all the triple-input NOR gates in package U215. The clock is also sent to all three NOR gates. A timing diagram showing the relationships between the clock line, the over-voltage or over-current line, and the three NOR gates is shown in Figure 4-14.

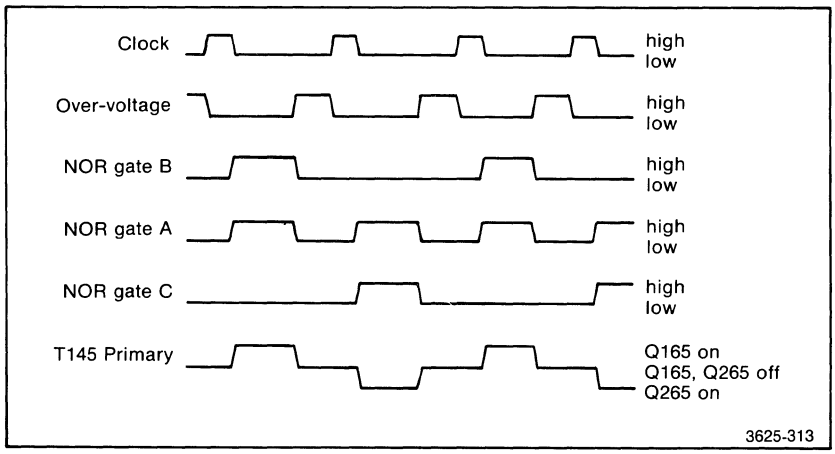


Figure 4-14. +5 Volt Power Supply switching logic.

Each of the NOR gates in U246 drives a switching transistor. If NOR gate B is high, current flows from tap 2 to tap 3 of T255, through Q248 to ground. Likewise, if NOR gate C is high, current flows from tap 2 to tap 1 and through Q244 to ground. When the over-voltage or over-current line is set, all of the NOR gates outputs are low. This situation makes Q248 and Q244 non-conducting and Q246 conducting, which shorts the transformer out across diodes CR148 and CR342. The short means no current will flow through T255, as can be seen in Figure 4-14.

Switches

The secondaries of transformer T255 drive the bases of switching transistors Q165 and Q265. When current flows from tap 2 to tap 3 of the base drive transformer T255, Q165 is turned on and Q265 is left off. Q165 then conducts current from the +160 V supply through the primary of T565 to charge capacitors C135 and C155. When the current to the base drive transformer is turned off, both drive transistors are turned off so no current flows through the primary of the power transformer. When transistor Q265 is turned on, capacitors C135 and C155 are discharged to −160 V through the primary of transformer T565. Then both drive transistors are again turned off and the cycle repeats.

The support components for the switches include the following:

- Resistors R145 and R354, which bleed off capacitors C135 and C155.
- Resistor R546 and capacitor C468, which damp any ringing from the inductance of the primary of transformer T565 when both drive transistors turn off.
- Diodes CR254 and CR356, which limit the back EMF from the transformer primary inductance to the supply voltages (±160 V) to protect the driving transistors.
- Diodes CR158, CR252, CR354, and CR355, which keep the driving transistors from saturating, allowing them to turn off fast.
- Capacitors C252 and C350, which bypass diodes CR158 and CR354 during turn-off.

EMI Filter

When driving transistors Q165 and Q265 switch at high frequencies, they force high frequency interference into the supplying lines. Since this interference can disrupt other devices connected to the same line supply, it must be filtered out. T114, L116, C118, C121, and R112 are an EMI filter to block this interference before it gets to the supply line.

+5 Volt Supply

This block is a standard full-wave rectifier with the exception of resistors R635 and R756 and capacitors C646 and C756. These components act as snubbers to restrict ringing when the diodes switch. L435, L620, C625, and C615 act as a standard LC filter. Diode CR508 prevents the output from being reversed.

+5 V Sense

The outputs of comparators U415A and D and U415B form an OR gate. If the +5 V line goes over-voltage or draws too much current, this OR gate goes high; otherwise the output, pin 1 of U415B, will be low. U415B is an inverting buffer with its non-inverting terminal tied to the +5 V reference. The output is used to set flip-flop U315A.

A ripple generator is tied to the non-inverting pins of the over-voltage and over-current sensors. The ripple generator consists of comparator U415C, an inverting buffer; Q318, which is controlled by the comparator; Q319, a constant current source; and capacitor C425. When Q318 is turned on by the clock being high, C425 is charged high. When Q318 is turned off by the clock, the charge on C425 is drained through Q319. This causes a downward voltage ramp. The ramp wave across C425 is voltage divided by R525 and R429 to produce a 200 mV peak to peak waveform. The ripple waveform is applied to the non-inverting side of both the over-voltage and over-current sensors to prevent the comparators from free-running, and to provide for a small amount of ripple at the output. It also keeps the over-voltage and/or over-current control in sync with the clock rate.

The over-voltage sensor built around U415D has an input from pin 5 of P400. This input ties to the +5 V supply bus to sense if the voltage gets too high. If this line should be disconnected,

R506 prevents the output from going totally out of regulation. R514 matches impedance to the comparator. C515 provides loop compensation. The non-inverting input of U415D goes to the +5 V reference and is coupled through a capacitor to the ripple generator.

The over-current sensor, U415A, looks at the voltage drop across resistor R720 through resistors R516, R517, and R518, which form a voltage divider. The non-inverting input of the comparator is biased by the ripple generator. C519 removes noise.

Transistor Q317 can be used to force the +5 V regulator's wired OR gate to trigger at the inverse of the power supply clock for power-up testing and troubleshooting. See the Maintenance: Troubleshooting section of this manual for more information.

Over-Voltage Protection (OVP)

The over-voltage protection circuit consists of special purpose IC U225 and a means of pulling the power supply clock high.

Pin 2 of U225 monitors the +5 V SENSE line through resistor network R226, and R227. Capacitor C255 allows a short over-voltage condition (less than 1 ms) to occur without triggering the circuit.

If U255 detects an over-voltage condition, SCR Q235 is turned on. When the SCR is turned on, the base of transistor Q335 is pulled low. This brings the collector of the transistor close to 11.3 V (supplied to the emitter). The high voltage from the collector supplies enough current to pull the output of the power supply clock high so the clock line no longer pulses. This turns off the +5 V supply. The clock stoppage is blocked from affecting other power supplies by diode CR217.

DAS 9129 COLOR DISPLAY MONITOR

The DAS 9129 Color Display Monitor displays red, green, and yellow information from the controller on a 9 inch CRT. Each color represents a level of importance.

- Red indicates the highest level of importance.
- Yellow indicates foreground information.
- Green indicates background information.
- Reverse video indicates user changeable areas.

All component numbers in the DAS 9129 color monitor description are assumed to have an A30 preface. This number is etched on all of the color monitor circuit boards.

DEFLECTION BOARD C 8A

Vertical Deflection

The vertical deflection circuit creates a current ramp in the vertical deflection yoke.

The VERT SYNC(H) line from the controller turns Q232 on and off. When Q232 is turned off, C238 is charged by the constant current source from Q134. This creates a linear voltage ramp into Q132.

When Q232 is turned on, C238 is discharged very rapidly through Q232 to ground. C238 remains low until Q232 is turned off by VERT SYNC(H), at which point the voltage ramp will begin again.

The emitter follower, Q132, provides a low impedance output for the voltage ramp. The output of Q132 is applied to U116A.

U116A, Q330, and Q235 make up a current amplifier that translates the voltage ramp, at the emitter of Q132, to a current ramp in the deflection yoke. The output of the amplifier at TP270 forces a current through the deflection yoke and R310. The current in the deflection yoke produces a voltage ramp on R310 that is fed back through R211, which nulls the input at TP175.

CR211 and CR212 provide a linearity correction at the screen edge.

The vertical positioning circuitry, which includes R170, governs the vertical position by varying the current through R122 to the summing node at TP175.

Horizontal Deflection

Clock line CSYNC(H) is the horizontal sync for the color monitor. CSYNC(H) is used in place of HORZ SYNC(H) because the color monitor has a different drive requirement than the monochrome monitor.

U508A, U508B, and Q517 together make up an inverter with high sourcing and sinking capabilities. This inverter goes into a Baker circuit (CR435 through CR438) to prevent transistor Q443 from saturating.

Q443 is the switch that controls a current ramp for the yoke and fly-back transformer T460. When Q443 is on, the 110 Vdc begins to supply a current through the fly-back transformer and the yoke. The deflection yoke current, which is flowing in the reverse direction, begins to ramp up linearly (see Figure 4-15).

When CSYNC is high, the base of Q443 is pulled negative about 4 V, turning it off. The current, which is from the parallel combination of the horizontal deflection yoke and the fly-back transformer primary winding, flows into C534 and C530. This produces a half sine wave with 900 V peak at TP259 (Q433 collector). When the voltage returns to zero, the deflection yoke current has changed direction and flows through CR334. The current will continue to flow through CR334 until the deflection yoke current passes through 0, at which point Q443 begins to conduct. (See Figure 4-15.)

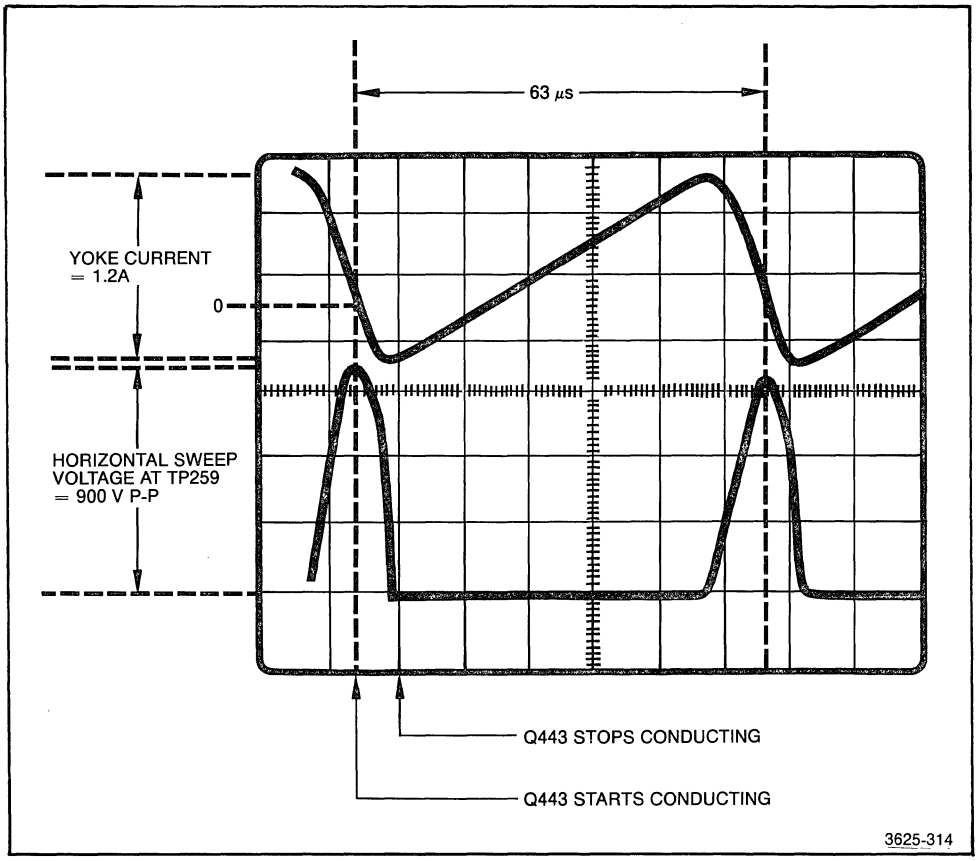


Figure 4-15. Horizontal deflection circuit, current vs. voltage.

Horizontal Size Control

L255 is a variable inductor that increases or decreases the current in the yoke. This increase or decrease controls the horizontal size.

High Voltage Section

The high voltage section rectifies the fly-back pulse to create the 21 kV potential and the high voltage focus potential.

The horizontal circuitry needs a geometric correction, because the CRT face is flat. The correction voltage circuit corrects the horizontal deflection by modulating the 110 V applied to the fly-back transformer. This will produce a slightly larger horizontal size at the vertical center of the screen, compensating for the shorter beam length at that position. (See Figure 4-16.)

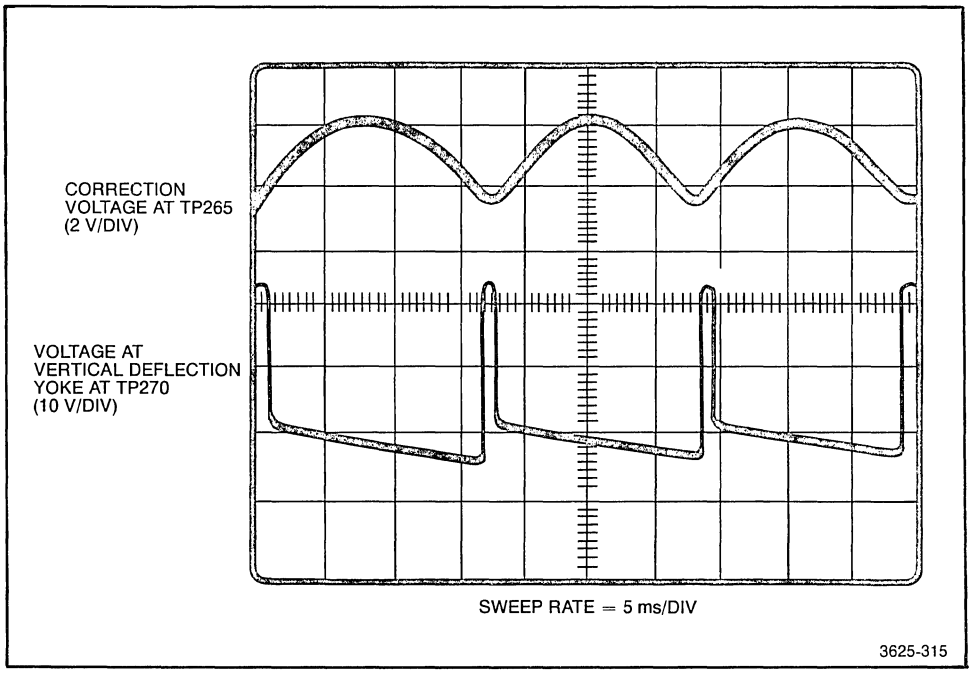


Figure 4-16. Modulation of the 110 V vs. vertical deflection.

Z AXIS BOARD C 8B

Z Axis Amplifier

There are three lines that make up the video data: RED(H), GREEN(H), and YELLOW(H). These three lines go into separate NAND gates that act as inverters: U635B for red, U635A for green, and U645B for yellow.

The output of each NAND gate drives the Z-axis output transistors (Q440, Q530, and Q540), which provide the voltage gain for the Z-axis outputs. If one or more of the three color video lines is high, the Z-axis output associated with that line goes low, allowing that color to write to the screen.

The potentiometers R140, R130, and R150 control the dc level of the Z-axis signal to set the relative brightness of the three colors.

The yellow characters that are in a red background are created by turning on the green color gun at the same time that the red background is on. When the RED(H) and GREEN(H) signals, which come from the controller, are high at the same time, the red intensity is slightly brighter than normal, because U645A bypasses R642. The red background is slightly dimmer than the other colors to increase the readability of the yellow-on-red.

Color Monitor Power Supply

The color monitor has a switching supply that creates +110 V, +24 V, and −10 V.

At power-up, the monitor power supply remains off for six seconds until the controller is ready. The 555 timer, U410, prevents it from turning on by disabling the shift register, U520. After six seconds, U520 counts 5 MPSCLK(H) pulses before allowing U510 to start. U510 is a regulating pulse width modulator which governs the switching supply. The internal timing of U510 is controlled by MPSCLK(H), (pin 12). It has automatic soft start and current limit capabilities. Pins 1 and 2 are used for beam current sensing, and pins 6 and 7 are used for the +12 V current sensing. If the monitor draws too much current from the +12 V supply the SH(L) output resets U520, and the supply will remain off for 5 MPSCLK(H) pulses. This allows C619 to discharge more completely before attempting to start again. C619 provides the automatic soft start.

The outputs of U510, pins 13 and 16, drive transistors Q410 and Q420. These push-pull transistors are the current drivers for the main power supply transformer, T300. The on-times of these transistors do not overlap.

The output of T300 is rectified by the following diode pairs: CR427 and CR426 produce +110 V, CR424 and CR325 +24 V, and CR423 and CR421 −10 V.

Inductors L100, L111, and L121 prevent the current from decaying to 0 A during the off portion of the power supply cycle. Capacitors C200, C210, and C220, filter out the ripple for each of the lines.

DAS 9109 MOTOROLA DISPLAY MONITOR

NOTE

Material used in the Motorola Display Monitor circuit description and associated schematics and component placement diagrams are taken from the "M1000 and M2000 Series Service Manual" © 1979 Motorola, Inc., by permission of Motorola, Inc.

The Motorola Display Monitor is the main user output interface of the DAS9109 mainframe. Unless otherwise noted, all component numbers in the Motorola Display Monitor circuit description are assumed to have an A4 preface. The Motorola Display Monitor does not have its A numbers etched on its circuit boards.

MOTOROLA DISPLAY MONITOR M 8

Video Amplifier

The video amplifier circuit consists of four stages that include Q1, Q2, Q3, and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of this first stage permits use of a low resistance CONTRAST control, R6, which furnishes a flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator, Q5. Capacitor C2 provides high frequency roll-off to limit the collector output to the bandwidth required to pass synchronization signals.

Transistors Q2 and Q3 form a direct-coupled amplifier with frequency compensation provided by C40 and C41. The output from Q3 is capacitively coupled (C5) to the base of Q4, the video output stage. The VIDEO BIAS control, R14, is used to set the quiescent collector current of Q4. Fre-

quency compensation is provided by R17 and C6. The combined action of clamping diode D1 and capacitor C5 provides dc restoration for the video signal.

Components C7, D2, and R19 provide CRT beam current limiting. Diode D2 is normally forward-biased; therefore, as Q4 conducts, its collector voltage drops. This causes a larger beam current to flow through R19, which in turn causes the voltage drop across it to rise. If excessive beam current flows, the voltage across R19 becomes greater than the collector voltage of Q4. This action reverse-biases D2, which prevents further increase in beam current. Capacitor C7 helps couple video to the CRT cathode, pin 2, through R20. Resistor R20 is used to isolate Q4 from transients that may occur as a result of CRT arcing.

Sync Separator

The sync separator employs two stages. Transistor Q5 is the sync separator and Q6 is the sync amplifier. The video input to the the sync separator is black positive. Capacitor C3 is charged by the peak bias current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak-to-peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R23 sets the clipping level.

Phase Detector

The phase detector control consists of two diodes (D3 and D13) in a keyed clamp circuit. Two inputs are required to generate the required output: one from the sync amplifier, Q6, and one from the horizontal output circuit, Q8. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output (Q8) collector pulse is integrated into a sawtooth by R28, C13, and R29. During horizontal sync time, both diodes conduct, which shorts C13 to ground. This effectively clamps the sawtooth on C13 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A in Figure 4-17), the sync pulse will occur when the sawtooth is passing through its ac axis and the net charge on C13 will be zero (waveform B in Figure 4-17). If the horizontal time base is lagging the sync, the sawtooth on C13 will be clamped to ground at a point negative from the ac axis. This will result in a positive dc charge on C13 (waveform C in Figure 4-17). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C13 will be clamped at a point positive from its ac axis. This results in a net negative charge on C13, which is the required polarity to slow the horizontal oscillator (waveform D in Figure 4-17).

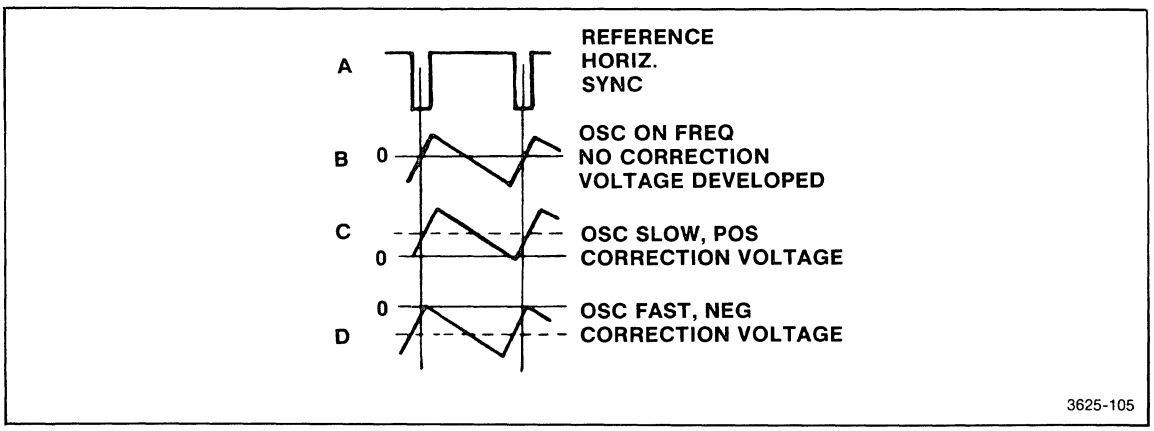


Figure 4-17. Phase detector waveforms.

Passive components R30, R31, and C16 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. When present, optional capacitor C14 times the phase detector for correct centering of the picture on the raster.

Horizontal Oscillator and Driver

The horizontal oscillator consists of integrated circuit IC1, which is essentially a voltage-controlled oscillator with variable mark-space ratio (duty cycle) and internal voltage reference. The reference voltage is present at pin 6, while resistors R37 and R38 determine the mark-space ratio. The main oscillator timing capacitor is C17, with its charging current derived from three sources: (a) a fixed current from R33, (b) a variable current from R34 and HORZ HOLD control R35, and (c) a correcting current from the phase detector network through R32. The combination of these three charging currents and C17 determines the horizontal frequency. The output from IC1 (pin 1) is a square wave of proper frequency and duration that is applied to the base of horizontal driver Q7. The output from Q7 is coupled via the horizontal driver transformer T1 (current step-up) to the base of horizontal output device Q8. Components R41 and C19 provide current limiting, while components R40 and C18 provide transformer damping to suppress ringing in the primary of T2 when Q7 goes into cutoff.

Horizontal Output

The secondary of T1 provides the required low drive impedance for Q8. Once during each horizontal period Q8 operates as a switch that connects the supply voltage ocross the parallel combination of the horizontal deflection yoke (L3-A) and the primary of the high voltage transformer, T2. The required deflection current (through the horizontal yoke) is formed by the L-R time constant of the yoke and primary winding of the transformer, T2. An S-shaping transformer, T3, and capacitor C44 provide additional shaping of the horizontal deflection yoke current for proper linearity. The horizontal retrace pulse charges C33 through D7 to provide +87 V.

Momentary transients at the collector of Q8, should they occur, are limited to the voltage on C33 since D7 will conduct if the collector voltage exceeds this value.

The damper diode, D10, conducts during the period between retrace and turn-on of Q8. Capacitor C20 is the retrace tuning capacitor. Coil L1 is a series HORIZ WIDTH control. Components C32 and D8 generate a negative voltage necessary to properly bias the CRT. A copper sleeve on the neck of the CRT shapes the horizontal magnetic field for proper linearity.

Pin 4 of the high voltage transformer, T2, is a boost winding, which together with components D11 and C34, develops a +400 V for G2 of the CRT. This same +400 V is also present on the high side of FOCUS control R61.

Dynamic Focus

Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to the corner as compared to the distance traveled to the center of the CRT screen. As a result of the distance change, optimum focus can be obtained only at one point. One method to resolve this difficulty is to modulate the focus voltage at the horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam

travel along the axis. The secondary of transformer T3 generates a parabolic voltage, which together with a fixed voltage from the FOCUS control, R61, is applied to the focus grid, pin 6 of the CRT. This system dynamically changes the value of the focus voltage from the CRT screen center to the screen edge, which will provide an optimum amount of voltage for best overall focus.

Vertical Oscillator, Driver, and Output

Composite sync pulses from the collector of sync amplifier Q6 are applied to the double-integrating network of R45, C23, R46, and C24. The horizontal component of the sync signal is removed, leaving only the sync pulses. The vertical sync pulses are coupled to the free-running vertical oscillator stage, Q10, by C45 and R47. Transistors Q10 and Q12 are connected as a multivibrator. Transistor Q11 is used as an emitter follower that provides a low impedance drive for the vertical output stage, Q12. The series combination of capacitors C27 and C28 is initially charged to the supply voltage through R53 and the VERT SIZE control, R52, which generates an exponential voltage ramp.

When a positive vertical sync pulse is applied to the base of Q10, it begins conducting, which discharges C27 and C28. This action turns off Q11 and causes a decrease in the collector current of Q12, which also decreases the vertical deflection current through the vertical deflection yoke (Y3-B) and the vertical choke (L2). The resulting rapidly collapsing field in L2 generates a large voltage spike that is used for vertical retrace. Components R58, C29, R51, and C26 shape this spike to ensure that Q10 remains conducting until retrace is carried to completion. Diode D4 couples the shaped spike to the base of Q10. At this point Q10 reverts to its non-conducting state and the cycle repeats. The VERT HOLD control, R49 and R48, provides a feedback signal to Q10 to maintain oscillation in the event vertical sync pulses are not present. Diodes D5 and D6 provide the proper voltage drops to run Q12 class A.

Vertical linearity is maintained by applying the ramp voltage generated across R59, through R57 (VERT LIN control) and R54, to the junction of C27 and C28. Since this path is resistive, the waveform will be integrated into a parabola by C27 (waveform A in Figure 4-18). This results in predistortion of the ramp waveform (waveform C in Figure 4-18). Waveform B in Figure 4-16 illustrates what the drive sawtooth would look like without parabola shaping. Parabolic shaping is necessary to compensate for the non-linear charging of C27 and C28, and the impedance change occurring in L2 with current. Capacitor C31 serves to remove the dc component of the vertical deflection yoke current. Diode D9 clamps the collector voltage of Q12 to a safe level.

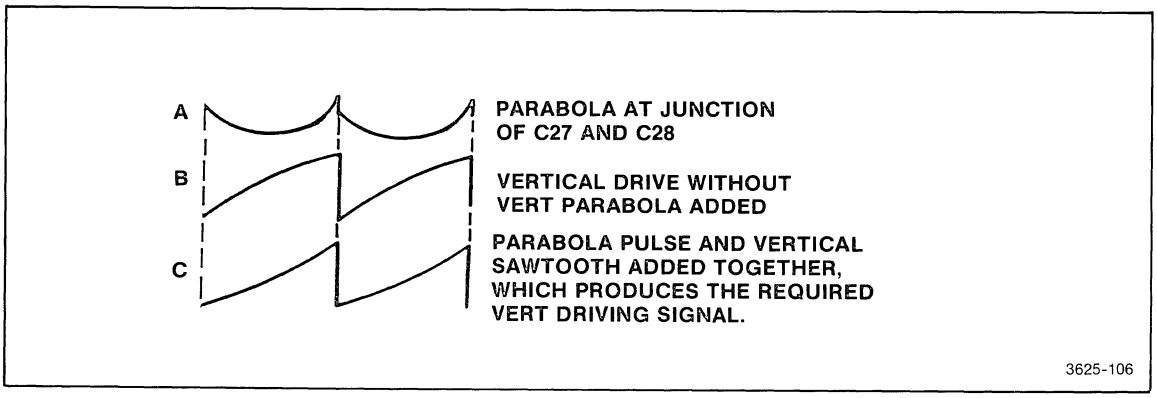


Figure 4-18. Vertical-drive waveforms.

Retrace Blanking

Retrace blanking is provided by negative-going horizontal and vertical rate pulses applied to G1 of the CRT. The collector pulse from the vertical output stage, Q8, is developed across R43 through R42 and C22. The collector pulse from the vertical output stage, Q12, is differentiated by C21 to remove the sawtooth portion of the waveform. The remaining pulse appears across R43. The mixed vertical and horizontal pulses on R43 are amplified and inverted by the blanking amplifier, Q9, and applied to G1 of the CRT.

KEYBOARD

The keyboard (assembly number A5) is the main user input interface to the DAS. All component numbers in the keyboard circuit description are assumed to have A5 as a preface unless otherwise noted.

KEYBOARD ◇9

An etched circuit board has key switches set in a matrix to provide X and Y inputs to an encoder, U157. The encoder supplies 7-bit parallel code words, KBIT0 through KBIT6, to the Controller module through connectors onto the system's data bus. The scanning rate of the encoder is determined by C147 and R149.

Tri-state transceiver U141 is used to buffer the code words from the encoder to the data bus.

The STROBE(H) output from the encoder is inverted and used as the KEY DOWN(L) signal for the Controller. STROBE(H) is set with any key stroke and stays high (low to the Controller) as long as the key is depressed or for a duration determined by C167 and R168. The keyboard encoder stops scanning for as long as the strobe is set.

Refer to schematic 9, the DAS keyboard, in the Diagrams section, and to Figure 4-19 for key designations and matrix assignments.

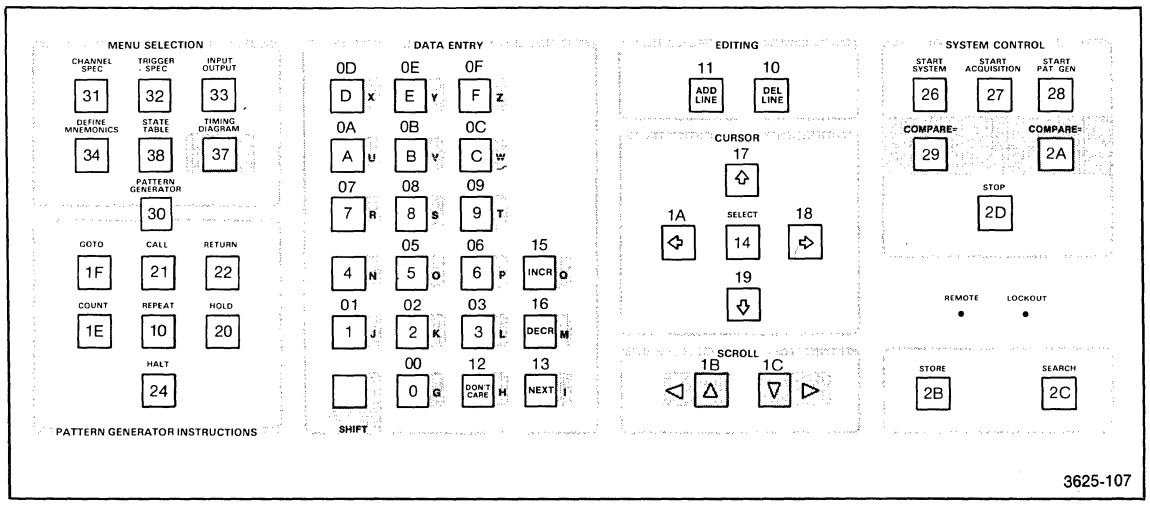


Figure 4-19. DAS keyboard hexadecimal codes.

REMOTE and LOCKOUT for the GPIB and RS-232 functions are read on the keyboard with an LED for each. They are lit when the controller supplies a low at pins 15 and 16, respectively, at J400. Control is from the control circuitry on the Controller board (see the Controller circuit description, following).

FIRMWARE

The acquistion, pattern generation, and I/O capabilities of the DAS are all provided by firmware. For a thorough understanding of the system, therefore, the firmware must be taken into account. The firmware comes into its own in three particular areas.

- During power-up the firmware sets up the DAS for operation and verifies the operation of most of the hardware.
- When the START SYSTEM key is pressed, the firmware loads user-programmed values into the hardware ports so that the system operates in the desired way.
- The firmware also manages all menus for programming operation of the DAS and displaying acquired data.

POWER-UP SEQUENCE

Upon power-up the DAS firmware executes code out of the Interp ROM that tests the system RAM (resident on the Controller board) and the system ROM (which resides mostly on the Trigger/Time Base, but may reside on other boards as well). The power-up routine then organizes the system ROM code into a useable system.

The portion of the power-up procedure being executed is indicated by the status of the LOCKOUT and REMOTE lights on the DAS keyboard. A step-by-step procedure for the power-up sequence follows.

NOTE

If the DAS cannot complete the power-up procedure, pressing any key on the keyboard will cause the DAS to re-attempt power-up. This may be useful in troubleshooting an intermittent Controller problem.

1. The DAS turns on the LOCKOUT light.
2. If Option 02, the I/O Interface, is installed in the DAS, the baud rate for the RS-232 port is set to the default value (4800 baud).
3. The firmware now determines how much RAM is available. All DAS Controller boards come with 32K of RAM. If less than 32K of RAM is detected, the power-up sequence continues, but an error message appears on the screen after power-up.

4. All of the system RAM on the Controller board is tested now. First the data lines for the RAM are checked by a walking-1 sequence at address 4000. If one of the values read back does not match the expected value, the value that was read is stored in register HL of the Z80A. Otherwise, the RAM test continues with step 5.

5. All locations in RAM are loaded with 55 hexadecimal.

6. All addresses in RAM are examined and compared to 55 hexadecimal. If a match occurs, then AA is loaded into the address and the next address is compared to 55. If a value found in the RAM does not match 55, the RAM test stops and loads the address of the failure into register HL of the Z80A. The test may be re-started from step 1 by pressing any key on the DAS.

7. After every address in RAM has been examined for 55 and loaded with AA hexadecimal, the Z80A examines all RAM addresses again for AA. If AA is found in all cases, then step 8 is initiated. If a value found in the RAM does not match AA, the test reacts the same as for a failure in step 6.

8. The RAM test has been passed. The LOCKOUT light on the keyboard turns off and the REMOTE light is turned on. The REMOTE light indicates that the ROMs resident on the Controller board are being checked.

9. Both the Interp and Runtime ROMs on the Controller are checksummed. If the checksum is passed, the test proceeds to the next step. If the Interp ROM fails, register HL of the Z80A is loaded with 1FFF and the test stops. If Runtime fails the checksum, then register HL is loaded with 3FFF.

10. Both Controller ROMs have now passed the checksum. Both the REMOTE and LOCKOUT lights are turned on for the duration of the power-up routine.

11. The Z80A searches the Trigger/Time Base and all instrument cards in the DAS for ROMs. When a ROM is found a checksum is performed. If a checksum error is found, the test continues, but an error message is displayed when the display monitor is started.

12. A list is now created by the firmware that indicates the location of all I/O drivers in the firmware. As each driver is located, it initializes the hardware it controls.

NOTE

If an I/O driver contains a checksum error, the driver will still attempt to initialize the hardware. The system may fail if a faulty I/O driver is executed with an incorrect instruction. If the DAS fails with both the LOCKOUT and REMOTE lights on, try running the DAS after removing all ROMs that contain I/O drivers.

13. Now a list is created by the firmware that indicates the location of all units. (A unit is a self-contained set of Pascal instructions. A unit roughly corresponds to a menu.) The variables that set the menu status (like internal clock rates or trigger values) are loaded into their own table so they are accessible to all of the units.

14. The DAS now locates all patches in the firmware. A patch list table is created that contains the locations of all valid patches.

15. The Pascal interpreter starts operating at this point. The interpreter takes Pascal codes stored in units and executes the codes through the Z80A.

16. Up to this point, all instructions that were executed are found in the Interp ROM. The Run-time ROM now starts executing its instructions.

17. When the Interp ROM starts operating, both the LOCKOUT and REMOTE lights turn off. This indicates that the system is initialized and ready to operate.

18. The DMA and CRT Controller ICs on the Controller board are now initialized so messages can be shown on the display monitor. Note, however, that no data has yet been loaded into the RAM locations that hold video screen information.

19. The keyboard and the interrupts to the Z80A are now enabled.

NOTE

If the interrupt circuits are malfunctioning the Z80A will not have the opportunity to show information on the screen.

20. SELF TEST IN PROGRESS appears on the screen. From this point on, the screen provides a good indication of the operations being performed by the microprocessor.

OPERATION OF THE START SYSTEM KEY

The START SYSTEM key informs the Controller board that the instrument modules in the DAS must now be programmed and start acquiring data and/or generating patterns. There are seven major steps the Controller performs in the following sequence when the START SYSTEM key is pressed.

1. Display the start message at the top of the screen of the display monitor.

2. Program the data acquisition and pattern generation modules with the information contained in the Channel Specification, Trigger Specification, and Pattern Generator menus.

3. Start the pattern generator and data acquisition modules.

4. Monitor the data acquisition modules while they are operating.

5. After data acquisition is finished, complete shutting down the acquisition modules.

6. Process the data acquired by the DAS for display on the State Table and Timing Diagram menus.

7. Finally, give control to the State Table or Timing Diagram menu; whichever was displayed last.

Each step in the above sequence consists of one or several procedures. The procedures involved in each of the above steps are given next.

NOTE

After the START SYSTEM key is pressed, the Controller takes over operation of the DAS. No further actions of the operator are needed. Thus, the processes described next are performed entirely by the Controller board, with no operator intervention.

The Processes for Step 1

There is only one procedure for initiating the START SYSTEM process. The message ACQUISITION AND PATTERN GENERATOR STARTED is shown at the top of the video display. If the DAS only contains acquisition modules, the display will refer only to acquisition.

The Processes for Step 2

The acquisition and pattern generator modules are programmed at this point.

a. Clear the Trigger/Time Base Module and stop the pattern generator. This is done by loading the Trigger/Time Base A10U275 with 0000 1010 binary. Clearing the Trigger/Time Base initializes the trigger and initializes the pipelined internal timing sequencer.

b. If an acquisition is to be performed then:

   1. Set the 91A32 to single-step and initialize the MAR and qualifier pipeline.

   2. Turn off the 91A08 clock (set clock selector to 00 hexadecimal) and clear the 91A08.

   3. If 91A32 modules are being used, then load the A counter and delay counter on the Trigger/Time Base. All the values loaded into the counters are the one's complement of the values specified in the Trigger Specification menu. The values are loaded in the following sequence. The A count lsb then the A count msb are loaded. Then the delay count lsb and finally the delay msb are loaded.

   4. If 91A08 modules are being used, then load the 91A08 delay counter. First the EN LD DELAY 0(H) line is made active. Next the delay counter is loaded with the one's complement of the programmed delay. The counter is loaded in the following sequence: msb of the delay counter is loaded with 00 hexadecimal. The lsb of the of the counter is now loaded, and finally the msb is loaded with the desired value. Finally, the EN LD DELAY 0(H) line is brought back low.

   5. Load the word recognizers on the 91A32 modules. This requires loading both the 91A32 modules and the Trigger/Time Base. First the START ALL(L) signal is generated on the Trigger/Time Base. Then the word recognizers in each 91A32 are loaded. The word recognizers are loaded by hitting the SINGLE STEP line of the selected 91A32 once and then loading all of the word recognizer RAMs from the least significant to the most significant.

6. When all 91A32 word recognizers have been loaded, the Trigger/Time Base is cleared again. Then each 91A32 has both the even MAR and odd MAR loaded with 00 hexadecimal. After the MARs are loaded, the 91A32 has INIT(L) pulsed low to clear the qualifiers again.

7. If 91A08 modules are being used, then each 91A08 has the following steps performed. Both the even and odd MARs are loaded with 00. Then the three control registers that regulate the M218 trigger recognizers are programmed. Finally the trigger control register is loaded with a value depending on whether the 91A08 is used in AND mode (16 hexadecimal), ARMS mode (3E hexadecimal), or ONLY mode (0E hexadecimal).

c. Program all acquisition and external clock probe thresholds.

d. Program the data acquisition and pattern generator clocks. First the two internal clock rates on the Trigger/Time Base are programmed. Then the 91A32 modules are programmed to the clock and clock edge that each one will use. Next, all 91A08 modules are programmed to select the clock to be used for the acquisition memory, as well as the clock for the difference counter.

e. Program the Trigger/Time Base to pass the proper polarity of pattern generator control signals (the external clock, inhibit, pause, interrupt lines).

f. Program the data acquisition probe qualifiers; first 91A32 qualifiers, then 91A08 qualifiers.

g. If the pattern generator is to be run, then program the pattern generator modules in the following sequence:

1. If 31P32 modules are used, then their strobe shapes are programmed.

2. The 91P16 is set to single-step. The interrupts and the instruction multiplexer are disabled.

3. The program counter loading register is set to 01 hexadecimal and the single-step clock is pulsed. This sets the pattern generator so it will start executing instructions at μCode address 01.

4. The program counter loading register is set to 00 hexadecimal. This is done because the outputs of the instruction multiplexer and the program counter loading register are wire ORed. If the loading register had a value other than 00, the program counter would not work.

5. The interrupt signal is now enabled or disabled, according to the way the Pattern Generator menu is programmed. The single-step clock is then pulsed again to initialize the interrupt signal pipeline.

6. Next, the PROBE CLK EN(H) line is programmed high and the instruction multiplexer is enabled.

7. The strobe shapes for the 91P16 are now programmed.

8. Finally, the clock that will run the 91P16 is programmed into the CLK CNTL BUS.

The Processes for Step 3

Start the data acquisiton and pattern generator modules. Everything is now set to go. The START ALL signal is made active to let all modules run.

The Processes for Step 4

Monitor the data acquisition modules while they are operating. This consists entirely of seeing whether the acquisition modules have triggered, and whether the acquisition memories have been filled. This information is available through control registers on both 91A32 and 91A08 modules. Finally, the 91A08 and the 91A32 STOP STORE signals are monitored. When STOP STORE is true, then the next step can occur.

The Processes for Steps 5 through 7

The procedures for reading back and formatting data from the acquisition modules are very dependent on the specific module being read. Refer to the detailed circuit descriptions of the memory readback circuits of the relevent modules for more information.

THE ROMs

There are three types of firmware in the DAS ROMs. There are units, which roughly correspond to menus. There are drivers, which control I/O devices (like the tape drive or RS-232 port). There are also patches, which are corrections or up-grades to firmware in a ROM that has already been masked. All three of these types of firmware will be referred to as items for the purposes of this discussion.

Each item (a unit, a driver, or a patch) contained in a ROM has a number associated with it. All firmware has a unique number. At power-up, if two pieces of firmware are found with the same item number, the one with the highest version number ("V" number) is used. Item numbers are assigned in the following way:

DECIMAL	HEX	FUNCTION
00 — 63	00 — 3F	Pascal units (menus)
64 — 127	40 — 7F	Patches for units
128 — 255	80 — FF	I/O drivers

Following is a description of the contents of the standard ROMs that are found in a DAS. Because the ROMs were released over a period of time, some of the later ones contain patches for ROMs that had already been masked.

NOTE

The Interp, Runtime, and Patch ROMs must be located in the proper sockets on the Controller board. The Pat Gen ROM must be located on a 91P16 module. Any other ROM in the system will be functional when plugged into any ROM socket on the Trigger/Time Base or I/O Interface boards.

Interp ROM

Located on the Controller board, this ROM contains the Pascal interpreter as well as the Z80 assembly code required to power-up the DAS and the initial RAM test and ROM checksum routines.

Runtime ROM

This ROM, located on the Controller board, contains one unit: unit 0 (V0). Unit 0 contains the DAS power-up display and support menu routines.

Channel ROM

This ROM, located on the Trigger/Time Base, contains two units: unit 3 (V22) and unit 12 (V10). Unit 3 controls the Channel Specification menu. Unit 12 contains the Pattern Generator Timing menu.

Define ROM

This ROM, located on the Trigger/Time Base, contains one driver and one unit: driver 128 (V1) and unit 8 (V0). Unit 8 contains the Define Mnemonics menu. Driver 128 is an old driver for the tape drive (Option 01). Driver 128 is not currently used for the tape drive, the driver actually used is in the I/O ROM.

Diag 1 ROM

This ROM, located on the Trigger/Time Base, contains one unit and one patch: unit 14 (V1) and patch 71 (V1). Unit 14 contains the diagnostic tests for the Trigger/Time Base, 91A32, 91A08, 91P16 and 91P32 boards. Patch 71 is a patch to the State Table (affects unit 11, V23) to allow for the creation of microprocessor disassembly tapes.

Diag 2 ROM

This ROM, located on the Trigger/Time Base, contains one unit: unit 2 (V1). Unit 2 contains the diagnostic menu and the diagnostic tests for the Controller board.

I/O ROM

Located on the Trigger/Time Base, this ROM contains a unit, a driver, and a patch: unit 7 (V1), driver 129 (V2), and patch 65 (V1). Unit 7 contains the Input Output menu. Driver 129 is the actual driver for the tape drive (Option 01). Patch 65 (affects unit 3, V22) fixes a scrolling problem in the Channel Specification menu when there are multiple 91A32 modules.

Start ROM

Located on the Trigger/Time Base, this ROM contains one unit and one patch: unit 9 (V26) and patch 67 (V1). Unit 9 operates the system control keys. Patch 67 actually contains three patches. These patches are patch 62, patch 51, and patch 14. Patch 62 (affects unit 0, V0) makes the Pod ID buttons and the connect/disconnect signals operate for pods A, B, and D of the 91P32 module.

Patch 51 (affects unit 11, V23) stops an infinite loop that could occur in the State Table menu when the STORE key was pressed. Patch 14 (affects unit 5, V8) makes add line and delete line work properly for 91P32 modules in the Pattern Generator menu.

State ROM

This ROM, located on the Trigger/Time Base, contains one unit and one patch: unit 11 (V23) and patch 66 (V1). Unit 11 is the State Table menu. Patch 66 (affects unit 6, V12) corrects an error in the Trigger Specification menu.

Timing ROM

Located on the Trigger/Time Base, this ROM contains one unit, one patch, and one driver: unit 4 (V10), patch 64 (V1), and driver 130 (V1). Unit 4 contains the Timing Diagram menu.

Patch 64 actually contains three patches. These patches are patch 40 (V1), patch 41 (V1), and patch 55 (V1). Patch 40 (affects unit 5, V8) corrects a difficulty with labels in the Pattern Generator menu that were referenced before they were defined. Patch 41 (affects unit 5, V8) fixes a problem with single-stepping the pattern generator while the cursor was in the INTERRUPT ON field. Patch 55 (affects unit 5, V8) allows the use of strobes on the first instruction of an interrupt routine.

Driver 130 contains two driver patches. These patches are Csp 19 and Csp 4. Csp 19 fixes the patch procedures so variables other than local or global can be referred to in a patch. Csp 4 adjusts the switch mapping registers when a procedure is exited. This patch is necessary for the GPIB driver and for procedures that have been patched and are exited from.

Trigger ROM

Located on the Trigger/Time Base, this ROM contains one unit: unit 6 (V12). Unit 6 contains the Trigger Specification menu.

Pat Gen ROM

Located on the 91P16 Pattern Generator, this ROM contains one unit: unit 5 (V8). Unit 5 contains the Pattern Generator menu.

GPIB1 ROM

Located on the I/O Interface, Option 02, this ROM contains one unit and one patch: unit 15 (V5) and patch 70 (V1). Unit 15 contains the message processor for the GPIB. Patch 70 is a modification to the Runtime firmware to support the GPIB.

GPIB2 ROM

Located on the I/O Interface, Option 02, this ROM contains one unit and two drivers: unit 13 (V0), driver 133 (V1), and driver 134 (V2). Unit 13 contains more firmware for the message processor for the GPIB (see GPIB1). Driver 133 runs the input and output of the GPIB. Driver 134 is the RS-232 driver, which allows GPIB commands to be accepted over RS-232.

Patch ROM (Version 1.05)

The patch ROM contains an assortment of patches that are included as they become necessary. The information given here may not contain the most recent patches. Be sure to refer to the Change Information section at the back of this manual to find the most recent patches.

This ROM contains patch 69 (V1), which is a reference to 26 different patch procedures. The individual patch procedures are listed below. The ROM also contains two drivers (actually, driver patches): driver 135 and driver 136. Finally, there is a special purpose assembly language patch, which patches the interpreter. This patch is called the Boot Patch.

Patch 53 (V1) for unit 11, V23 (the State Table menu). It fixes the menu so the acquisition memory continues to be displayed after a new reference memory is loaded from the tape or GPIB.

Patch 2 (V1) for unit 11, V23 (the State Table menu). It changes the way reference memory space is allocated.

Patch 1 (V1) for unit 11, V23 (the State Table menu). If the tape drive restores the system with a configuration change, the restored reference memory may not be used. This prevents exposing reference memory that has not been programmed.

Patch 44 (V1) for unit 11, V23 (the State Table menu). This patch fixes the COMPARE= routine, which on certain occasions would compare one extra value, and therefore could fail.

Patch 35 (V1) for unit 11, V23 (the State Table menu). This patch fixes the ARMS mode display so when no fast data is displayed the slow data is compressed to normal size.

Patch 24 (V1) for unit 5, V8 (the Pattern Generator menu). This patch displays 91P32 modules from the high numbered slot to the low slot (instead of low to high).

Patch 34 (V1) for unit 5, V8 (the Pattern Generator menu). This patch prevents definition of more than 6 duration values for COUNT, REPEAT, and HOLD instructions in the Pattern Generator menu.

Patch 2 (V1) for unit 12, V10 (the Pattern Generator Timing menu). This patch adds 30 ns to all strobe delays. Default value was 40 ns, now it is 70 ns.

Patch 18 (V1) for unit 8, V0 (the Define Mnemonics menu). This patch fixes a bug in the use of the INCR and DECR keys with define values greater than 16 bits. It also corrects a problem in the use of INCR and DECR on X (don't care) values.

Patch 21 (V1) for unit 8, V0 (the Define Mnemonics menu). This patch has influence on later DAS versions, and is not presently applicable.

Patch 35 (V1) for unit 8, V0 (the Define Mnemonics menu). This patch repairs a difficulty with the Define Mnemonics menu, which caused mnemonics defined for group B to appear in group C under certain conditions.

Patch 36 (V1) for unit 6, V12 (the Trigger Specification menu). This patch restricts the allowable qualifiers in split clock mode to the slots that match the master CLK1's slope.

Patch 63 (V1) for unit 6, V1 (the Trigger Specification menu). When in split clock mode, this patch removes the programmability of qualifiers when a slot set to CLK1 has its slope changed from that of the master CLK1.

Patch 12 (V1) for unit 3, V22 (the Channel Specification menu). This patch changes the power-up default pod sequence assignment. It was ABCD. It is now DCBA, which makes pod A the least significant.

Patch 15 (V1) for unit 7, V1 (the Input Output menu). This patch initializes the counter, which watches the number of retries when a soft error is found.

Patch 37 (V1) for unit 7, V1 (the Input Output menu). This patch causes configuration changes in the state table menu to occur only when the reference memory is restored.

Patch 42 (V1) for unit 7, V1 (the Input Output menu). The DC100 tape manufacturers recommend that the tape be wound to the end and then rewound before writing to it if the tape has been stored (or shipped) at a higher-than-usual temperature. This patch winds the tape to the hole at the end of the tape before a format operation is performed.

Patch 1 (V1) for unit 2, V1 (the diagnostics). This patch allows the diagnostic ROMs to be patched from the Patch ROM.

Patch 16 (V1) for unit 14, V1 (the diagnostics). This patch turns off the DAS display monitor during ramping of the DAC circuitry. This eliminates variations in step width during these tests caused by DMAs.

Patch 79 (V1) for unit 14, V1 (the diagnostics). This patch clears the high byte of the integer where the MAR is stored.

Patch 81 (V1) for unit 14, V1 (the diagnostics). This patch fixes the 91A08 difference counter test so both the high and the low byte are read by the test, rather than only reading the low byte.

Patch 33 (V1) for unit 4, V10 (the Timing Diagram menu). When all fast clocks took place inside 8 slow clock periods, there was a 45 second delay the first time the timing diagram was entered. This delay was caused by an algorithm that calculated the optimum magnification. This patch replaces this calculation with an assumption that a magnification of 3 is good enough.

Patch 56 (V1) for unit 4, V10 (the Timing Diagram menu). This patch corrects an infinite loop that occurred sometimes when a fence was used and the fast module triggered before the slow module.

Patch 17 (V1) for unit 15, V1 (the GPIB message processor). This patch accepts all ASCII characters so they can be mapped into the DAS special character set.

Patch 62 (V1) for unit 13, V1 (the GPIB message processor). This patch causes configuration changes in the state table menu to occur only when the reference memory is restored.

Patch 1 (V1). This patch is not applicable to current firmware.

Driver 135 (V1) fixes driver 129, V2 (the tape drive driver). This patch corrects a difficulty that occurs when the tape drive is operated over RS-232 in master/slave mode. If the RS-232 baud rate was set to either 300 or 600, the tape drive would kick the baud rate up to 1200, thus terminating communications. This patch prevents the baud rate from changing at inappropriate times.

Driver 136 (V3) fixes driver 133, V1 (the GPIB driver). This patch prevents the input buffer of the GPIB chip on the I/O Interface board from over-running.

Boot Patch (V1). This patch alters the power-up sequence in the Interp ROM. With this patch, drivers found in the Patch ROM are brought into operation last. This is required for driver 135 and driver 136 to work properly.

CONTROLLER

The Controller board in the DAS mainframe provides most logic functions, drives all interfaces, and provides the intelligence for the DAS. For an overview of the Controller's circuits refer to the Controller in the General System Description.

CONTROLLER MICROPROCESSOR 10

Controller Clock

Crystal Y432 and inverter 431D form a 29.4912 MHz ECL level clock. The crystal is kept centered around the ECL threshold level by inverter U431C. Normally U431C would oscillate, but this is an unstable condition because of low pass filter C330. So U431C stays centered at the threshold voltage, V_{bb}. The crystal's oscillations would upset the stability of the V_{bb} source, so a notch filter consisting of L435 and C431 isolates the ac from the V_{bb} source but passes V_{bb}. Transistors Q435 and Q438 convert the clock from ECL to TTL levels.

U337C buffers the 29.4912 MHz clock signal. This signal is divided-by-two by register U535B. Registers U331A and B divide the signal by four and give two identical signals 90° out of phase with each other. These signals are 3.6864 MHz clocks. One of the 3.6864 MHz clocks is converted to MOS levels by U337A and Q335, so it can be used to clock the microprocessor. The two 3.6864 MHz clocks are inverted by U337C and D, and sent to the CPU bus as PHASE(L) and 2PHASE(L).

Microprocessor

The CPU of the Controller is a Z80A microprocessor, U351. The data bus, address bus, and those control lines that are outputs, are all buffered because the microprocessor must drive large numbers of circuits. The functions of the various pins of the microprocessor are listed below.

Data Bus. The data bus is a bidirectional bus used for data transfers with memory and other modules. It also receives firmware instructions that are interpreted by the microprocessor.

Address Bus. The address bus provides the addresses for memory and I/O data exchanges. The 16-bit bus provides direct access to 64K addresses.

RFSH(L). Goes active to indicate the lower 7 bits of the address bus contain a refresh address for dynamic RAMs. It is used in conjunction with the MREQ(L) signal to do a refresh read to all dynamic RAMs.

M1(L). Goes active when the microprocessor is in the op code fetch cycle of an instruction execution.

RD(L). Goes active when the microprocessor is ready to receive data on the data bus from the currently addressed device.

WR(L). Goes active when the microprocessor is writing data on the data bus to the currently addressed device.

MREQ(L). Goes active to indicate that the address bus holds a valid address for a memory-read or memory-write operation.

IORQ(L). Goes active to indicate that the lower half of the address bus holds a valid I/O address for a read or write operation. An IORQ(L) signal is also generated with an M1(L) signal to acknowledge an interrupt and indicate the interrupt vector can be placed on the data bus. Interrupt acknowledge operations occur during M1(L) cycles, but I/O operations never occur while M1(L) is active.

INT(L). This input is made active to request an interrupt. A request is honored at the end of the current instruction if the internal interrupt enable flip-flop is in the enable position, and the BUSRQ(L) signal is not active. There are three different software-controllable modes for the microprocessor to react to the interrupt signal.

NMI(L). This input is made active to request a non-maskable interrupt. A request is honored at the end of the current instruction if the BUSRQ(L) signal is not active. A non-maskable interrupt causes the microprocessor to store all contents of its registers in external stack and start executing instructions at address 0066.

RESET(L). This input is made active to force the program counter to 0000 and initialize the microprocessor. Initialization includes:

1. Disable maskable interupts.
2. Set Register I to 00.
3. Set Register R to 00.
4. Set Interrupt mode to 0.

While the RESET(L) is active, the address and data buses go to a high impedance state and all output control signals go to the inactive state.

BUSREQ(L). This input is made active to request use of the data, address, and control buses by some device other than the microprocessor. In response to this signal the microprocessor sets its inputs to these buses to a high impedance state as soon as the current machine cycle is finished.

BUSAK(L). This output goes active to indicate that the data, address, and control buses can be used by devices other than the microprocessor. The microprocessor's inputs to these buses are set to a high impedance state when BUSAK(L) is active.

There is also a delay circuit built around U537D and Q539 which prevents the microprocessor from being initiated (RESET(L)) until the power supplies have stabilized. This is done by sensing when the Main Power Supply has been stable long enough to charge C538 through R539 high enough to flip inverter U537D. When the inverter's output flips low, the transistor pulls the RESET(L) line low to initiate the microprocessor's start-up sequence.

Interrupt Logic

The interrupt logic polls the eight interrupt request lines to signal the microprocessor when an

interrupt request is occurring. Counter U137A is clocked at the same rate as the microprocessor. The counter increments and causes data selector U141 to scan the eight interrupt lines. If one of the eight interrupt lines is active (low), the data selector will produce a signal which: 1) signals the interrupt line of the microprocessor, and 2) stops the counter from scanning. When the interrupt signal is acknowledged, the BM1(L) and BIORQ(L) lines go active. This causes inverting-input NAND gate U138D to output a low signal, which enables tri-state buffer U237. This tri-state buffer then passes the value held in counter U137A on to the data bus so the microprocessor can go to the proper interrupt routine.

The microprocessor is programmed to react to any maskable interrupt in mode 3. This mode of interrupt has a different starting address for each interrupt routine. When an interrupt is accepted, a 16 bit pointer is formed from the lowest eight bits of the pointer (the value on the data bus), and the highest eight bits of the pointer (the contents of internal register I). The pointer is then used to address 16 bits of memory, which in turn are used as the starting address of the routine. The address bus then jumps to the new starting address and starts to execute the routine. The contents of all internal registers are dumped to the external stack before the interrupt is processed, so when the interrupt routine is finished the microprocessor can return to the original place in its program.

Wait Generator

These gates regulate the insertion of wait states in microprocessor routines to keep pace with slower speed peripherals. The wait control works in two ways. Any WAIT(L) signal from the Interconnect board activates wait states for as long as the signal is active. All other wait-producing signals go through registers U168A and B. These registers have the effect of producing a one-clock-cycle wait state, regardless of the duration of the wait-producing signals. See Figure 4-20 for a timing diagram of the one cycle wait producing circuit.

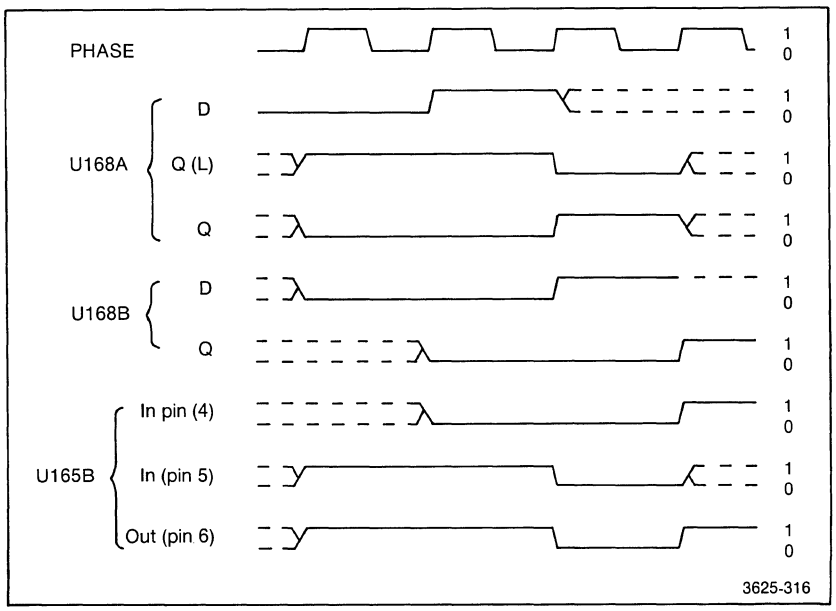


Figure 4-20. One-cycle wait circuit timing diagram.

Several different combinations of signals will produce a one-cycle wait. Presently, one-cycle waits are caused by all op code fetches, any time ROM is read, and any I/O execution. Reading from RAM does not cause a one-cycle wait. Table 4-7 shows all of the different signal combinations that will produce a one-cycle wait and those that will cancel one-cycle waits.

Table 4-7
One Cycle Wait Triggering Signals

BA15	BA14	BMI	BIOREQ	BMREQ	State
0	0	X	X	L	Wait 1 clock
1	1	X	X	L	Wait 1 clock
X	X	L	X	X	Wait 1 clock
X	X	X	L	H	Wait 1 clock
X	X	X	L	L	Cancels Wait 1

External Bus Request Logic

The data, address, and control bus on the interconnect board, is normally under control of the controller board. It can be relinquished at the request of another card by driving the BREQ(L) line low. This causes pin 11 of U151 to activate the BUSRQ(L) line of the Z80. The Z80 will stop executing at the first avialable cycle and tristate it's busses. The Z80 then asserts BUSAK(L). BUSAK(L) is anded with BREQ(L) by U338B. The output of of U338B tristates address buffers U475 and U478, control bus buffer U438, and data bus buffer U555. Pin 1 of U555 is driven low through U138B and U537C making it an input on the bus side. The output of U338B is also inverted and returned to the interconnect bus on the BACK(L) line.

Data Bus Access Logic

The direction of the data bus buffer, U555, is determined by gates U297D, U295C, U295A, and U537C. Table 4-8 shows what combinations of active signals influence the direction of the data bus buffer. Note that the combination of the DMARD(L) and DMA IN PROGRESS(L) lines being active causes the buffer to present a high impedance in both directions.

Table 4-8
Data Bus Buffer Direction Signals

BREQ(L)&BUSAK(L)	BIORQ(L)	BA7	BA6	BRD(L)	Buffer U555
L	X	X	X	H	microprocessor output
L	H	H	H	L	microprocessor input
L	L	H	H	L	microprocessor input
L	H	H	H	L	microprocessor input
L	L	L	H	L	microprocessor input
L	L	H	L	L	microprocessor output
L	L	H	L	L	microprocessor input
L	H	H	L	L	microprocessor input
L	L	L	L	L	microprocessor input
H	X	X	X	X	microprocessor input

CONTROLLER DMA AND SLOT SELECT 

Direct Memory Access Controller (DMA)

The direct memory access (DMA) controller, U251, provides data to the programmable CRT controller (schematic 12) to determine what is presented on the display monitor. The DMA acquires control of the data and address buses from the microprocessor when the programmable CRT controller requests data. Data is then transferred from memory to the CRT controller. At the

end of the DMA cycle, control of the buses is returned to the microprocessor so it can continue operations. The DMA controls the buses for about 15% of the operating time.

The handshaking procedure for a DMA request proceeds as follows:

- The CRT controller (schematic 12) makes DRQ2(H) active.
- The DMA (schematic 11) responds by making HRQ(H) active. This in turn makes BUSRQ(L) active through NOR gate U338D.
- The microprocessor (schematic 10) receives the BUSRQ(L) signal and, at the end of the current instruction cycle, sets all of its inputs to the buses at a high impedance and sets BUSAK(L) active.
- BUSAK(L) is inverted through inverting-input AND gate U338C to give BUSAK(H). BUSAK(H) is applied to the HLDA(H) input of the DMA to inform it that the bus can be used for direct memory transfer.
- The 8257 sends out the address, and the data gets on the bus.
- Finally, the DACK2(L) line goes active to signal the CRT controller that the data is now ready to be transferred.

When the DMA has control of the buses, it creates an address or the data being read in accordance with how it was programmed. The lowest 8 bits of the address bus come from 0 through A7 on the DMA. The D0 through D7 bits from the DMA replaced on the highest eight lines of the address bus through atch U461 when the AEN(H) line goes active. For more nformation regarding how the DMA is used, see the CRT Cntroller detailed circuit description that appears later in this section.

Control Circuitry

The control circuitry provides decoding of the data and address buses for various internal and external signals.

Registers U305A and U305B service the keyboard interrupt signal. The 60 Hz signal from the CRT controller is divided by two by U305B. When this signal has a falling edge, capacitor C300 applies a negative-going spike to U305A, pin 1. This spike resets register U305A so the Q(H) output is low. The Q(H) output is the 30 Hz signal that goes active to signal the Controller that the keyboard should be read. When the interrupt is acknowledged the INTERRUPT VECTOR(L) goes active which clocks register U305A and sets its Q(H) output high. This sequence is repeated every 33 milliseconds.

The I/O Register, U345, decodes four address lines (BA4 through BA7) from the Controller address bus to control some system I/O selection. It outputs enable signals as follows:

Y0(L). A low signal (DMA CS(L)), which selects the DMA Controller for initial programming (see the DMA on schematic 11).

Y1(L). A low signal (CRT CS(L)), which enables the programmable CRT controller (see the CRT Controller on schematic 12).

Y2(L). A low signal (BEEPER CS(L)) to inverting-input NAND gate U127C, which clocks the beeper register, U227, in this circuitry block.

Y3(L). A low signal (MAP REG CS(L)) to inverting-input NAND gate U138C, which clocks the I/O mapping register, U541 (refer to the Slot-Select Logic circuit description).

Y4(L). A low signal (GLITCH DISPLAY(L)), which either enables the keyboard interface to be read (see the Keyboard Read circuitry block on schematic 13), or allows glitches to be shown or suppressed in the timing display (see the CRT Controller on schematic 12).

Y5(L). Used for test only.

Y6(L). A low signal (TAPE DRIVE CS(L)), which enables Option 01, the tape drive. Refer to the tape drive circuit description.

Y7(L). A low signal (I/O INTERFACE OPTION CS(L)), which enables Option 02, the I/O Interface. Refer to the I/O Interface circuit description.

The beeper register, U227, provides various I/O and interfacing signals. It is clocked by a chip-select bit from the I/O register, and by BWR(L) from the microprocessor through inverting-input NAND gate U127C. Clocking is determined by the firmware. The register's outputs control the following parameters:

Q0. A high bit allows current to flow through the magnet of the beeper. Sounds are determined by the on-off rate of this bit.

Q1. When this bit is low, current flows through the LOCKOUT LED on the keyboard.

Q2. When this bit is low, current flows through the REMOTE LED on the keyboard.

Q3 and Q4. These bits are wired to data selector U131B to provide selection bits A and B. These bits determine the BAUD CLOCK rate (see the Baud Clocks circuit description).

Q5. After passing through buffer U127D, this bit provides the TAPE RESET signal to Option 01, the tape drive.

Q6. This bit provides the DRQ1(H) signal to the DMA controller (see the DMA on schematic 11)

Q7. This bit provides the INT 7(L) signal to the interrupt logic through inverter U337B (see the Microprocessor block on schematic 10).

Transistor Q110 provides the power handling capabilities needed to drive the beeper, LS100. The beeper makes audible signals whenever required by the firmware.

Baud Clocks

The 14.7456 MHz clock from the microprocessor's clock is divided by three by registers U131C and D, and NAND gate U531B. This 4.9152 MHz clock is divided again by counter U231A to

produce 2.44576 MHz (called 2PHASE/3(H)), 614.4 kHz, and 307.2 kHz. Both 2PHASE/3(H) and the 614.4 kHz clock are inverted by U537A and U325A, respectively, and then pass through P1. The 307.2 kHz clock is further divided by counter U231B. The output of U231B is applied to data selector U131B and selected by a code from the beeper register, U227. The baud clock selection code is shown in Table 4-9. The selected clock is output as BAUD CLOCK(H) on P1.

Table 4-9
Baud Rate Selection Codes

Beeper Register Data								
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Clock Output
X	X	X	0	0	X	X	X	153.6 kHz
X	X	X	1	0	X	X	X	76.8 kHz
X	X	X	0	1	X	X	X	38.4 kHz
X	X	X	1	1	X	X	X	19.2 kHz

Slot-Select Logic

The slot-select logic controls which modules are being written to or read by the microprocessor. The selection is done by specifing the bus slot the desired module resides in. Slot selection is initiated by the MAP REG CS(L), Y3, signal from the I/O register, U345, and a BWR(L) signal from the microprocessor. These signals cause inverting-input NAND gate U138C to generate a falling edge followed by a rising edge when BWR(L) is deactivated. On the rising edge from U138C, BD0 through BD3 (from the microprocessor) are clocked into the I/O mapping register, U541. The data from the I/O mapping register, the I/O SEL(L) signal, and BA7 are all decoded by the slot select decoders, U605, U511, U563, and U565. Table 4-10 shows how these signals are decoded.

Table 4-10
Slot And Port Decoding

BD3	BD2	BD1	BD0	Slot	Port[a]
0	0	0	0	SEL SLOT 0(L)	-------
0	0	0	1	SEL SLOT 1(L)	PORT 1(L)
0	0	1	0	SEL SLOT 2(L)	PORT 2(L)
0	0	1	1	SEL SLOT 3(L)	PORT 3(L)
0	1	0	0	SEL SLOT 4(L)	PORT 4(L)
0	1	0	1	SEL SLOT 5(L)	PORT 5(L)
0	1	1	0	SEL SLOT 6(L)	PORT 6(L)
0	1	1	1	SEL SLOT 7(L)	PORT 7(L)
1	0	0	0	SEL SLOT 8(L)	PORT 8(L)
1	0	0	1	SEL SLOT 9(L)	PORT 9(L)
1	0	1	0	SEL SLOT 10(L)	PORT 10(L)
1	0	1	1	SEL SLOT 11(L)	PORT 11(L)
1	1	0	0	SEL SLOT 12(L)	PORT 12(L)
1	1	0	1	SEL SLOT 13(L)	PORT 13(L)
1	1	1	0	SEL SLOT 14(L)	PORT 14(L)
1	1	1	1	SEL SLOT 15(L)	PORT 15(L)

[a] Ports are selected only when both I/O SEL(L) and BA7 are low.

CONTROLLER DISPLAY MONITOR INTERFACE 

CRT Controller

The 8275 Programmable CRT Controller, U121, has as its primary functions refreshing the display monitor (by buffering the information from memory) and keeping track of the electron gun position on the CRT. When the Controller board is powered up, the CRT controller is programmed to request DMA bursts that are eight cycles long and fifteen cycles apart. The fifteen cycles allow time for the microprocessor to perform its tasks. The CRT controller is also programmed so that the character blocks are ten dots high, with 80 characters horizontally across the screen and 24 lines of characters vertically down the screen.

When the display is in operation, the programmable CRT controller partially loads one of the two character buffers (part of U121) during each DMA burst. One character buffer is loaded by the DMA while the other buffer outputs character codes. When one 80 character buffer is emptied completely, the other buffer is used for output and the emptied buffer is filled by DMA bursts. The programmable CRT controller also indicates when the presently displayed character has any special attributes, like inverse video, highlighting, or video suppression. In addition, there is a General Purpose Attribute line, GPA0(H), which specifies whether standard characters or timing waveforms are displayed.

Display Clocks

The 29.4912 MHz clock is divided by three by registers U535C and U535D and NAND gate U531C. This results in a 9.8304 MHz clock called DOT CLOCK(H). DOT CLOCK(H) is divided by six by counter U425 and NAND gate U531A. The divide-by-six circuit has two out-of-phase outputs, both of which run at 1.6384 MHz. One of the 1.6384 MHz clocks is called CHAR CLOCK(L). These three clocks are related as shown in Figure 4-21.

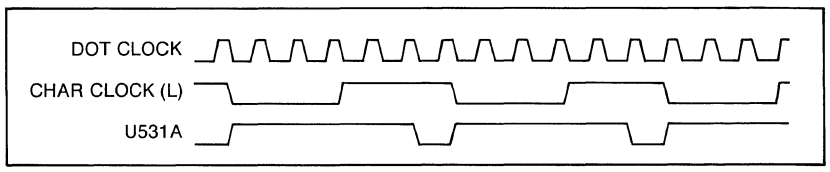


Figure 4-21. Display clock timing.

CHAR CLOCK(L) clocks the programmable CRT controller to regulate how often character codes are advanced. The clock from NAND gate U531A clocks visual attribute data through register U321. The clock from U531A passes through U405C and is used for logging new data into shift register U315. DOT CLOCK(H) clocks shift register U315. PHASED DOT CLOCK(L) passes through OR gate U205A and is used in video highlighting.

Display Generator

The heart of the display generator is a 1K x 8 bit ROM (U215) that decodes the data from the programmable CRT controller into bits that will make sense when shown on the display monitor. The display generator has two modes of operation: the character generator and the timing display

generator. All display characters consist of dots filling in a rectangular matrix (six dots across and ten dots high) as shown in Figure 4-22.

Alphanumeric characters are addressed in character ROM U215 by CC0 through CC5, used to address A3 through A8, and GPA0(H) from the programmable CRT controller, used for A9. The ROM produces one 6-dot line at a time, as specified by the line counter (address lines A0, A1, and A2). For standard alphanumerics, GPA0 line is low. When GPA0 is low, character selection lines CC1 and CC4 pass through AND gates U105A and D unaltered, because the GPA0(H) is low and inverting-input OR gate U197C produces a high.

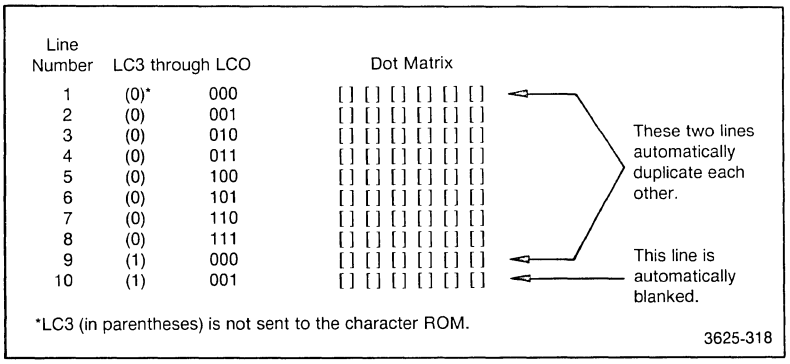


Figure 4-22. Display character format.

The tenth line of all characters is automatically blanked because AND gate U105C activates the VSPB(H) signal. See Table 4-11 and Figure 4-22 for more details. The first and ninth lines in a character automatically duplicate each other because they both write to low order address 000, so these lines are usually programmed blank in the character ROM.

The character ROM, U215, generates all six dots in one line of a character simultaneously. This data is serialized by shift register U315. New data is logged into the shift register just before the new character is to be displayed. The data is then shifted out through Q(H) by DOT CLOCK(H). The shifted out data is then decoded by U200.

Data selector U200 takes data from shift register U315 and the visual attribute signals from register U321. With this information, U200 creates video information for the display monitor. See Table 4-11 for an explanation of how the data is decoded.

Transistor Q425, with its associated circuitry, is an intensity control to regulate the voltages going to the display monitor.

Register U400B, exclusive-OR gate U115A, and inverting-input NOR gate U300D ordinarily pass exactly the same data that comes out of shift register U315. Whenever the RVVB(H) signal is active, however, the register and two gates stretch the length of the low signals from the shift register. This slightly enlarges the dark character against the light background shown on the video screen.

The RVVB(H) line only goes active when the CRT screen shows inverse video. When reverse video is not occurring, register U400B is held reset, so U300B outputs the same data that U315 outputs.

Table 4-11
Visual Attribute Decoding

Attributes					Origin of Output Signals				
		Output Muxes							
VSPB	RVBB	SelB HGLTB	SelA EXPB	Selected Input	Video	Red	Green	Yellow	Visual Display
0	0	0	0	0	U315	0	U315	0	Normal Text—Green
0	0	0	1	1	U315	0	U421	U315	Yellow Text[a]
0	0	1	0	2	U315 + Φ DOT CLK	1	U315 + U421	0	Highlighted Text—Green on Red[a]
0	0	1	0	3	U315 + Φ DOT CLK	1	U315 + U421	0	Highlighted Text—Green on Red[a]
0	1	0	0	0	$\overline{\text{U315}}$	0	$\overline{\text{U315}}$	0	Reverse Video—Green
0	1	0	1	1	$\overline{\text{U315}}$	0	$\overline{\text{U421}}$	$\overline{\text{U315}}$	Reverse Video—Yellow[a]
0	1	1	0	2	U315 + Φ DOT CLK	1	U315 + U421	0	Highlighted Text—Green on Red[a]
0	1	1	1	3	U315 + Φ DOT CLK	1	U315 + U421	0	Highlighted Text—Green on Red[a]
1	X	X	X		0	0	0	0	Suppressed Video—Blank

[a]Highlighted text is perceived as yellow on red. Can have green glitches.

When RVVB(H) is active (inverse video is occurring), high outputs from inverting-input NOR gate U300D have the same rising and falling edges as the output of U315. Low outputs from U300D, however, have their rising edge delayed by 1/2 of a DOT CLK(H) clock cycle. This is a result of clocking register U400B with the PHASED DOT CLK(H) signal.

Timing Diagram Decoding

The timing display generator is enabled by GPA0(H). When this line from the CRT controller goes high, the most significant bit of the character ROM, U215, goes high. This selects the half of the ROM that is used for waveform display. The timing display has a different data decoding format from the standard alphanumeric characters because there are more than 64 timing display characters.

Figure 4-23 shows a standard timing display character. The first and ninth lines are programmed blank in the ROM and the tenth line is automatically blanked. The middle five lines are identical.

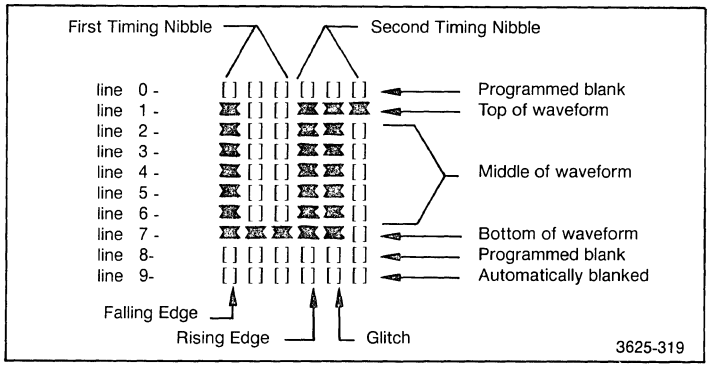


Figure 4-23. Timing display character.

This means there are, ROM-addressing-wise, only four different lines for each waveform: the top line (identical to the bottom line), the top of the waveform, the middle of the waveform (five identical lines), and the bottom of the waveform. Since the waveform only requires four different lines, the line selection address for the character ROM need only be two bits instead of the three adddress lines used for alphanumeric characters.

Since the line selecting requirements are reduced from 3 to 2 address lines, the left-over address line (A2) is used to select the waveform to be displayed. This allows the use of seven address lines to specify the type of waveform, instead of the six used for alphanumerics.

There are two timing nibbles in the character selection word. The nibbles divide the displayed character in half. Each nibble displays information regarding one acquired bit. The necessary data to define one nibble is 1) what was the data stored, 2) was there a glitch with the data, and 3) was there a transition immediately before this data was stored. The format bit allows the use of special characters in the timing display. Table 4-12 shows how the nibbles are decoded. Each nibble occupies three vertical lines (half of a standard character).

Table 4-12
First/Second Timing Display Nibble Decoding

Previous Bit	Format	Glitch	Data	Display
A2/A6	A8/A5	A7/A4	A6/A3	
X	1	X	0	"space"
X	1	X	1	
1	0	0	1	
0	0	0	1	
1	0	0	0	
0	0	0	0	
1	0	1	1	
0	0	1	1	
1	0	1	0	
0	0	1	0	

The data specifying a new waveform must contain the data bit prior to the first nibble of the new waveform. This bit determines if there should be a rising or falling edge, or a high or low display of the first nibble of the new character. The previous bit is supplied to the ROM address by hardware.

The previous data bit is recognized and stored by registers U415B, C, and D, and the associated gates. Registers U415C and D detect when GPA0(H) goes high by turning NAND gate U311C low. This is important because data written before GPA0(H) goes active is not waveform display data, therefore does not contain valid previous-bit information.

Register U415B shifts through data from CC0, which is the value of the previous data bit. If this is valid waveform data (determined by NAND gate U311C) it passes through NAND gate U311D and inverting-input OR gate U311A. If GPA0(H) just made the upward transition, the value of the previous bit is indeterminate. To fix the value, the previous bit is assumed to be the same as the

first bit of the displayed character. The first data bit of the new waveform is given in address bit CC3. When GPA0(H) has a rising edge, bit CC3 is passed through NAND gate U311B and inverting input OR gate U311A, and is used as the previous data bit.

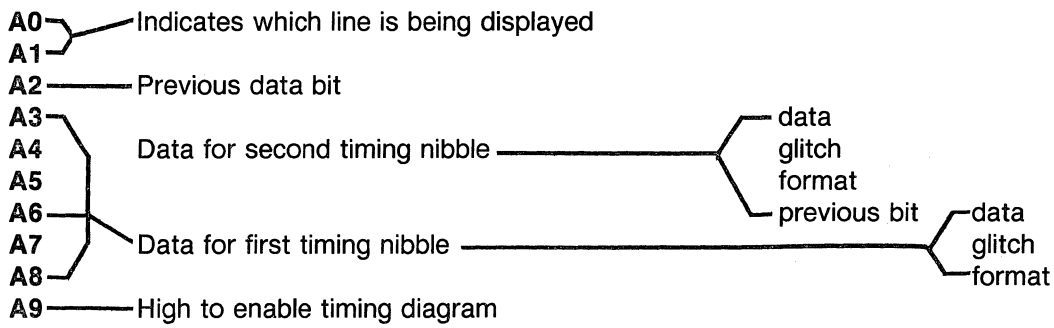
Data selector U211 and its associated logic convert the character ROM line selection code from three bits to two bits. When GPA0(H) is low, the line count outputs (LC0 through LC2) are passed through by the data selector. When GPA0(H) is high, the three bits are decoded into two bits by exclusive-OR gate U115D, inverter U115B, AND gate U105C, and inverting-input OR gate U205D. A logic chart of how the decoding works is shown in Table 4-13.

Table 4-13
Waveform Display Line Count Decoding

In			Out	
LC2	LC1	LC0	2B	3B
0	0	0	0	0 — Programmed blank
0	0	1	0	1 — Top of waveform
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0 — Middle of waveform (identical)
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1 — Bottom of waveform
0	0	0	0	0 — Programmed blank
0	0	1	0	1 — Automatically blanked

All of the above information leads to selecting characters in the character ROM. When the character ROM is in the timing display format, the addresses are assigned as shown in Table 4-14.

Table 4-14
ROM Addressing For Timing Characters



In the timing display decoding, the format bit (A8/A5) specifies whether the displayed nibble is a special character (1) or a standard timing waveform (0). The special characters are the fuzz

character and the space. The fuzz shows an over-density of data and the space shows a lack of data. If the format bit is 0, standard timing waveforms are generated. The waveforms are designed so that if the previous bit is different from the data bit a vertical line is the first part of the nibble.

If the glitch bit is a 1, a vertical line is in the middle part of the nibble. The data bit determines whether the horizontal bar in the character is at the top (1) or the bottom (0) of the nibble.

Glitch displays are determined by bits A7 and A4. There are some cases where glitch displays are not wanted, so there is hardware to allow glitch suppression. Register U185A is clocked by both BWR(L) and GLITCH SUPPRESS(H) being active. If BD7 is low when this happens, glitches are displayed; if BD7 is high, glitches are suppressed. If the GLITCH SUPPRESS(H) line and GPA0 are both high, inverting-input OR gate U197 writes out a low. That low will mask out the CC1 and CC4 data from the programmable CRT controller through AND gates U105A and D. This turns all glitch addresses to the character ROM to 0s so glitches are not displayed.

Display Monitor Timing

Counters U515 and U521 act as pulse stretchers. The Horizontal Retrace signal, HRTC(H), from the programmable CRT controller (U121) is normally low. The low from HRTC(H) holds counter U515 in the load mode, so the counter is loaded with 0011 binary.

HRTC(H) goes high to indicate the end of a line. When HRTC(H) goes high, counter U515 goes into count mode. U515 increments from 0011 binary to 0000 (wrap around), when the counter is disabled by inverting-input AND gate U517B. At this time HORIZ SYNC(H), from U300A, returns low. The end result is that the HRTC(H) signal lasts for 13 CHAR CLK pulses. Counter U521 operates similarly, except it is triggered by the VRTC(H) signal from the programmable CRT controller to create the VERT SYNC(H) signal.

MPSCLK C ⟨12⟩

The color monitor's low voltage switching power supply is synchronized so that the display will not jitter. The MPSCLK clock line governs the supply's switching time. MPSCLK is in phase with horizontal sync, and is twice as fast.

HRTC(H) creates the first MPSCLK through inverters U603A and U603C, and AND gate U300A. At the same time, HORZ SYNC(H) loads counters U500 and U600. When the count reaches 10 0000 binary, pin 2 of U405 goes high, allowing U515 to clock out a MPSCLK in between the clock pulses of either HORZ SYNC(H) or CSYNC(H) (see Figure 4-24).

CSYNC(H) C ⟨12⟩

CSYNC(H) is the color monitor's horizontal sync. It is created by a set of counters initialized by HORZ SYNC(H). The counters (U500 and U600) clock out CSYNC(H) just before, or just after the next HORZ SYNC(H).

When U500 and U600 reaches 1010000 binary, pin 3 of the NAND gate U603B goes low and enables counter U521.

The S100 switches (1,2, and 3) determine the number of counts U521 will count before CSYNC(H) is clocked out. (see Figure 4-24)

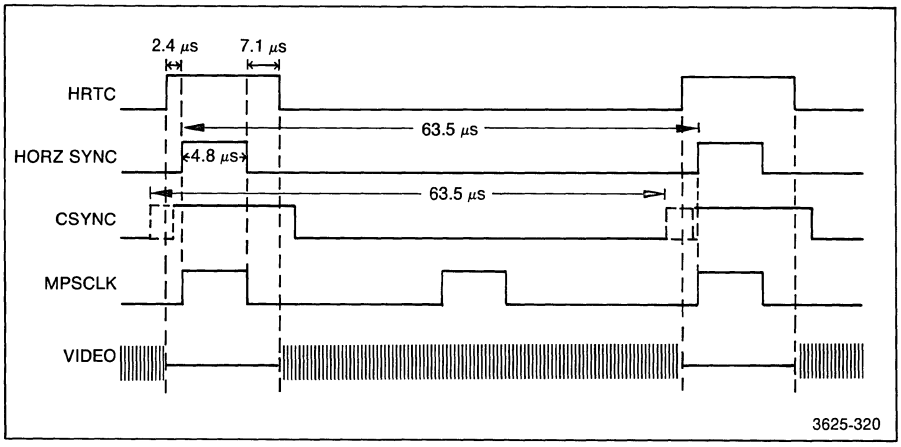


Figure 4-24. Horizontal sync timing for the color monitor.

CONTROLLER SYSTEM MEMORY CONTROL 13

Memory Map

The Controller-tied memory in the DAS is divided into six different sections by the Memory Map. This is accomplished by the three highest-order bits on the address bus, BA13, BA14, and BA15. The mapping is selected by the BMREQ(L) signal from the microprocessor's control bus. The memory map register, U195, decodes the addresses as is shown in Table 4-15.

Table 4-15
Memory Decoding

BA13	BA14	BA15	Signal	Selected Memory
0	0	0	SYS 0(L)	Interp ROM, U591
1	0	0	SYS 1(L)	Runtime ROM, U585
0	1	0	UPPER RAM SEL(L)	Upper RAM, schematic 14
1	1	0		
0	0	1	LOWER RAM SEL(L)	Lower RAM, schematic 14
1	0	1		
0	1	1	PERSONALITY(L)	Personality ROMs
1	1	1	PATCH(L)	Patch ROM, U597

If either of the system ROMs or the Patch ROM are selected by the memory map register, U195, when the BRD(L) line goes active, inverting-input NAND gate U165C produces a low (active) signal. This enables tri-state buffer U571.

System ROM

The address bus lines, BA0 through BA12, are buffered by U488 and U495A-E. These address lines are then bused to ROMs U585, U591, and U597. These ROMs output data when one receives a chip-select signal (CS(L)) from the memory map, discussed previously. The selected

ROM then writes its data through buffer U571 when the buffer is enabled by a signal from the memory map.

ROMs U585 and U591 contain the information required to power up the system and display the power-up menu. ROM U597 is a Patch ROM that contains corrections to firmware bugs. U597 may be either an EPROM or a masked ROM. One EPROM type has 2K x 8 bits of storage. The masked ROM and another type of EPROM have 8K x 8 bits of storage. The pins of J498 are strapped to correctly address the type of ROM installed.

RAM Addressing Logic

The system RAM (schematic 14) in the Controller has multiplexed addressing. The RAM ICs have only seven pins to accept addresses, but they require fourteen bits for a full address. The full address is input by means of the RAS(L) (Row Address Strobe) and CAS(L) (Column Address Strobe) lines. The RAM addressing logic creates the RAS(L) and CAS(L) signals and multiplexes the address bus, as well as determining the direction of the RAM read/write buffer, U581. There are three situations the RAM addressing logic has to handle: instruction fetch and refresh, data read, and data write. In addition, the circuits have to differentiate between the two sets of system RAM: the lower RAM and the upper RAM.

The instruction fetch and refresh cycle consists of two seperate processes, the fetch and the refresh. However, since both processes occur every time the microprocessor goes through an M1 cycle (op code fetch), both processes may be looked at as one whole. Refer to Figure 4-25 while reading about the instruction fetch and refresh cycle.

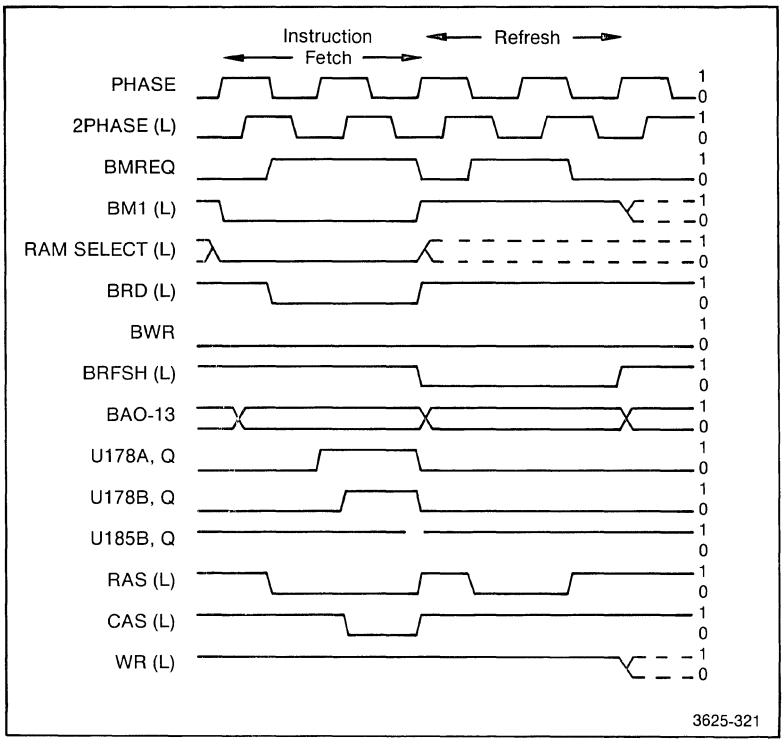


Figure 4-25. RAM addressing logic: timing diagram for instruction fetch in RAM and refresh cycle.

To perform an instruction fetch the BM1(L) line goes low. This signal cannot be clocked through register U185B because it is being held set. Next, the address bus changes to hold the address of the instruction being fetched. At this point only the lower half of the address bus (BA0 through BA6) will go through data selectors U485 and U481 to be written to the system RAM on RA0 —RA7. If the address on the address bus is mapped to the lower RAM, the LOWER RAM SELECT(L) signal goes active. If the address is mapped to the upper RAM, the UPPER RAM SELECT(L) signal goes active. If the address is not mapped to either RAM, neither signal goes active and the RAM addressing logic is not used. For this discussion it is assumed that the address is mapped to the upper RAM. The UPPER RAM SELECT(L) enables the RAM data bus buffer, U581.

Next, both BMREQ(L) and BRD(L) go active. BMREQ(L) is inverted to BMREQ(H). BMREQ(H) is the last high signal necessary to make three input NAND gate U188B output a low signal, which is UPPER RAS(L). BRD(L) sets the direction for buffer U581. At the next falling edge from PHASE(L), a high gets clocked through U178A, which puts the upper half of the address bus on RA0 — RA7. At the next rising edge of 2PHASE(L), register U178B clocks out a high. This makes NAND gate U188A go low so UPPER CAS(L) is active. At the next falling edge from PHASE(L), all registers get set back to their initial conditions by BMREQ(L) going high. The RAM addressing logic is now ready to refresh the system RAM.

The read, write, and refresh cycles exercise the RAM addressing logic in ways similar to the instruction fetch cycle. For signal timing diagrams of these different ways the RAM addressing logic is used, refer to Figures 4-25, 4-26, and 4-27.

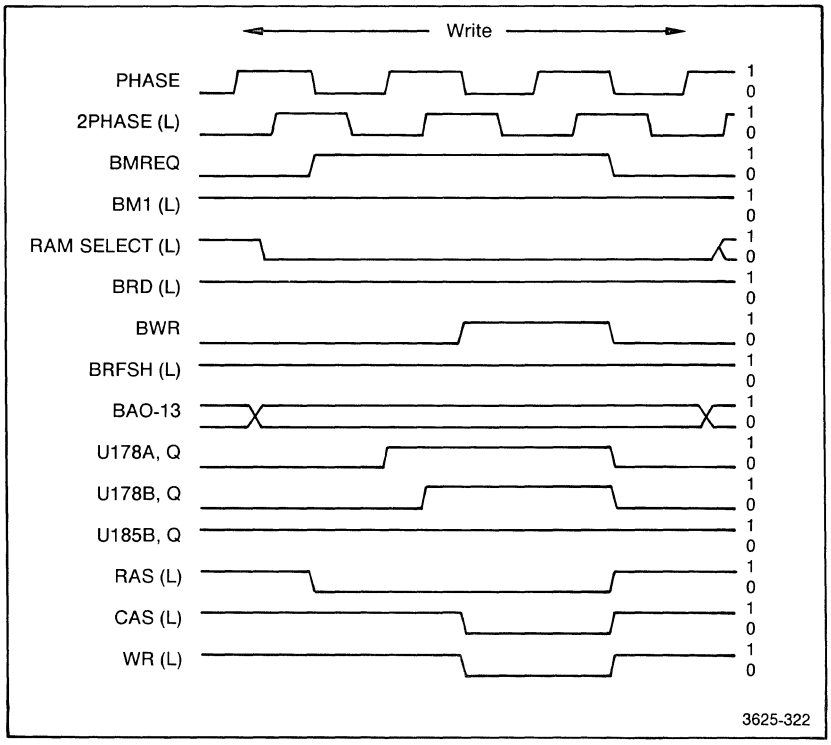


Figure 4-26. RAM addressing logic: timing diagram for data write in RAM.

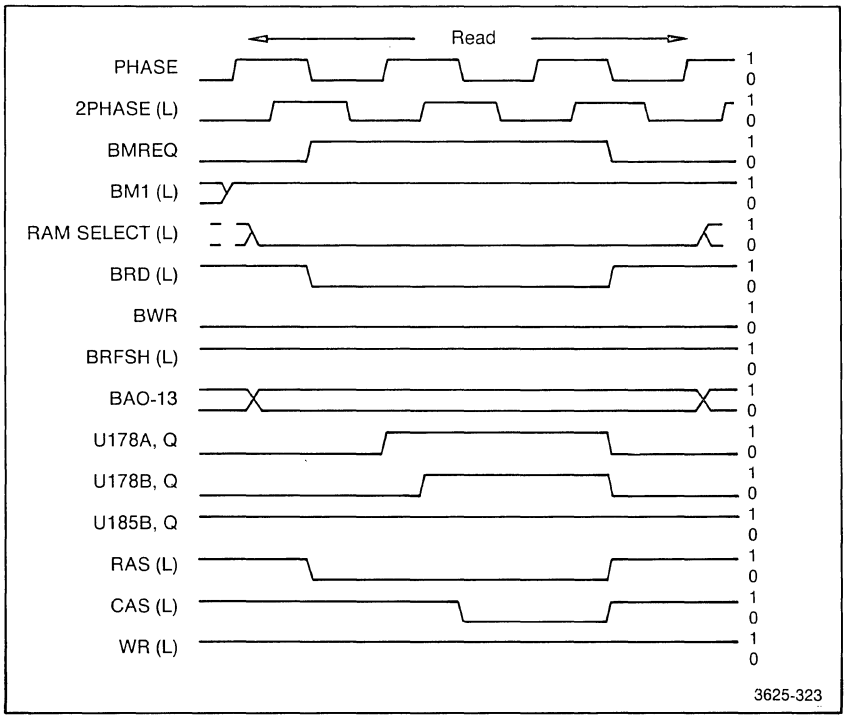


Figure 4-27. RAM addressing logic: timing diagram for data read in RAM.

CONTROLLER SYSTEM RAM 14

Lower RAM

The lower RAM consists of eight 4116 type 16K x 1 bit RAMs. All signals to the lower RAM come from the RAM addressing logic, schematic 13. For information on how the RAM is written to and read, see the RAM addressing logic circuit description.

Upper RAM

The upper RAM consists of eight 4116 type 16K x 1 bit RAMs. The upper RAM is identical to the lower RAM except for the addressing lines. Refer to the RAM addressing logic, schematic 13, for information of how the RAM is written to and read.

P6452 EXTERNAL CLOCK PROBE

The Trigger/Time Base uses a data acquisition probe to acquire three external clocks for data acquisition and four control lines for the pattern generation modules. This probe is identical to the probes used by the 91A32 and 91A08 acquisition modules. For more details, read the probe circuit description immediately following the circuit descriptions of the instrument modules.

TRIGGER/TIME BASE

The Trigger/Time Base Module performs two basic funtions in the DAS instrument configurations. It provides internal clocks for all of the instrument modules, and contains most of the triggering logic for the 91A32 Data Acquisition Module. The 91A32 trigger can also be influenced by, and be made to influence, the 91A08 triggering. All of the component numbers in the Trigger/Time Base description are assumed to have an A10 preface unless otherwise noted.

This description is divided into several levels. The level divisions are by schematic and then by functional block on the schematic. Numbers in diamonds refer to the numbers on schematic tabs in the Diagrams section. Those schematics should be referred to while reading the circuit description. For an overview of the Trigger/Time Base circuits, refer to the Trigger/Time Base in the previous General System Description.

TRIGGER/TIME BASE CONTROLLER INTERFACE 

The Controller Interface takes data from the Controller board and sends it to the appropriate registers in the Trigger/Time Base. This is performed by decoding the lowest four bits on the address bus and interpreting RESET(L), BWR(L), BRD(L), and PORT(L) from the Controller.

For example, suppose 02 is present on the address bus at the same time the Controller is writing PORT(L) and BWR(L). PORT(L) and BWR(L) enable decoder U491. An 02 on the address bus puts Y2(L) low on the enabled decoder U491 and clocks register U275. Any data on the data bus at that moment is then held by U275 until the same process happens again or the RESET(L) line from the Controller becomes active.

Table 4-16 shows which signals can be written from the Controller to reconfigure the Trigger/Time Base and which ICs each set of signals affects.

TRIGGER/TIME BASE ROM

All of the menus and interpretive information for the 91A32, 91A08, and Trigger/Time Base are stored in ROM. These ROMs are all addressed by the address bus of the Controller and are mapped in from C000 to DFFF. At power up, the Controller reads each ROM to see what is stored in it. The Controller then sets up a table in RAM to select the ROM to be read for each selected menu.

Memory Map

To select the desired ROM, the MAP1(L) line from the Controller Interface must be active. The active MAP1(L) clocks bits D0 through D3 on the data bus into register U495. Bit 3 selects either decoder U595 (if low) or decoder U596 (if high). The selected decoder then enables the appropriate ROM. If the PERSONALITY(L), SELECT SLOT(L), and BBRD(L) lines (all from the Controller) are active, decoder U471B will allow the selected ROM to be read on the data bus through U381. Table 4-17 shows a hexadecimal listing of how each ROM gets enabled.

Table 4-16
Trigger/Time Base—Controller Interface Map

Hex Addr	RESET	BWR	BRD	PORT	Line Name	ICs Affected U#	ICs Affected Schem.#
[a]XXX0	H	L	X	L	MAP1(L)	U495	16
[a]XXX1	H	L	X	L	THRESHOLD(L)	U131	17
XXX1	H	X	L	L	POD STATUS(L)	1/2 U177	15
[a]XXX2	H	L	X	L	CNTL0(H)	U275	15
XXX2	H	X	L	L	MOS STATUS(L)	U375	15
[a]XXX3	H	L	X	L	CLK 91A32(H)	U135	19
[a]XXX4	H	L	X	L	CLK 91A08(H)	U141	19
XXX5	X	L	X	L	DELAY0(L)	U351 & U361	18
XXX5	X	X	L	L	STATUS 0(L)	1/2 U17	15
XXX6	X	L	X	L	DELAY1(L)	U345 & U36	18
[a]XXX7	H	L	X	L	ACNTR0(L)	U271	18
[a]XXX8	H	L	X	L	ACNTR1(L)	U274	18
XXX9	X	L	X	L	SINGLE STEP (L)	U221 & U321	19
XXXA	X	L	X	L	DIAG B DONE(L)	U245B	18
XXXB	X	L	X	L	DIAG 91A32 TRIG(L)	U145A	18
XXXC	X	L	X	L	DIAG DELAY EN(H)	U461B	18
XXXD	X	L	X	L	TRIG CLK SEL(H)	U128	17

[a] These lines have their registers reset to 0 by a RESET(L) signal.

Table 4-17
MENU ROM SELECTION

Hex Code	ROM	Hex Code	ROM
1	U391	6	U283
2	U291	7	U287
3	U385	8	U181
4	U395	9	U183
5	U281	A	U295

ROM

There are sockets for 9 MK36000-type ROMs on the Trigger/Time Base board. The ROMs in these sockets are selected by the memory map. There is one socket (for U295) that is suitable for either an MK36000-type ROM or a 2716-type ROM. The type of ROM to be used dictates the configuration of jumper J195.

TRIGGER/TIME BASE EXTERNAL CLOCK PROBE INTERFACE 

Probe Threshold DAC

Register U131 has level-setting information written to it by the controller interface. This level-setting data in U131 controls digital-to-analog converter (DAC) U121. This DAC has a current output that is converted to a voltage output by op amp U109.

VREF– is supplied to the DAC by op amp U206. U206 compensates for differences between the DAS ground and the ground of the circuit under test. VREF+ is set with variable resistor R110 by adjusting the potential difference between TP105 and TP110 to 1.60 V with the greatest possible accuracy. This voltage sets the current output by the DAC when the most significant bit is set. Less significant bits are controlled by an internal current divider.

IO(H) and IO(L) are the DAC outputs. IO(H) is a current sink that is proportional to the 8-bit input. IO(L) sinks a current proportional to the one's complement of the 8-bit input. The sum of these current sinks is always a constant current. The constant current is set by zener diode VR112 and variable resistor R110.

The current out of the IO(H) pin of the DAC is converted to a voltage by op amp U109. The offset voltage of U109 is controlled by variable resistor R106. Solid state switch U108 sets whether the op amp acts as a voltage follower (switch open) or as a voltage multiplier (switch closed). When the switch is closed, the inverting input of the op amp is controlled by voltage divider R210 and R117. This means the inverting input reads a voltage that is 1/4 the voltage at the output. If the switch is open, R210 and the ground reference are disconnected. R117 then matches R118 and op amp U109 acts as a voltage follower.

Probe Receivers

The acquisition clock lines from the External Clock Probe are buffered and retained in their complementary ECL form. The acquired clocks are then supplied to the high speed bus through P1; acquired clock CK1 is also retained for use in trigger generation.

Signal Control

The trigger portion of the Trigger/Time Base is designed to provide complex triggering for 91A32 acquisition modules. Since 91A32s are usually clocked by either 91A32 INT CLK(L) or CLK1, the triggering section of the Trigger/Time Base must have a means of selecting between these two clocks. Register U128 selects one of these two clocks by writing to NOR gates U421 A, B, and D. Two of the three clocks — CK1(H), CK1(L), and 91A32 INT CLK(L) — are masked out by the signals from U128. The clock that passes through these NOR gates is inverted by the NOR gate, and written to transistor Q431. Q431 and Q432 convert the ECL clock signal to TTL levels.

The pattern generator external control lines are buffered and passed through programmable inverters (U309). All four control lines are then put on the high speed bus for use by a pattern generator module.

Pipelined Internal Timing Sequencer

This section controls the clocks to various parts of the trigger, and creates DQUAL(H). Refer to Figure 4-28, which shows how the pipelined internal timing sequencer relates to the rest of the trigger. The pipeline exists because the qualifier and word recognition signals caused by an

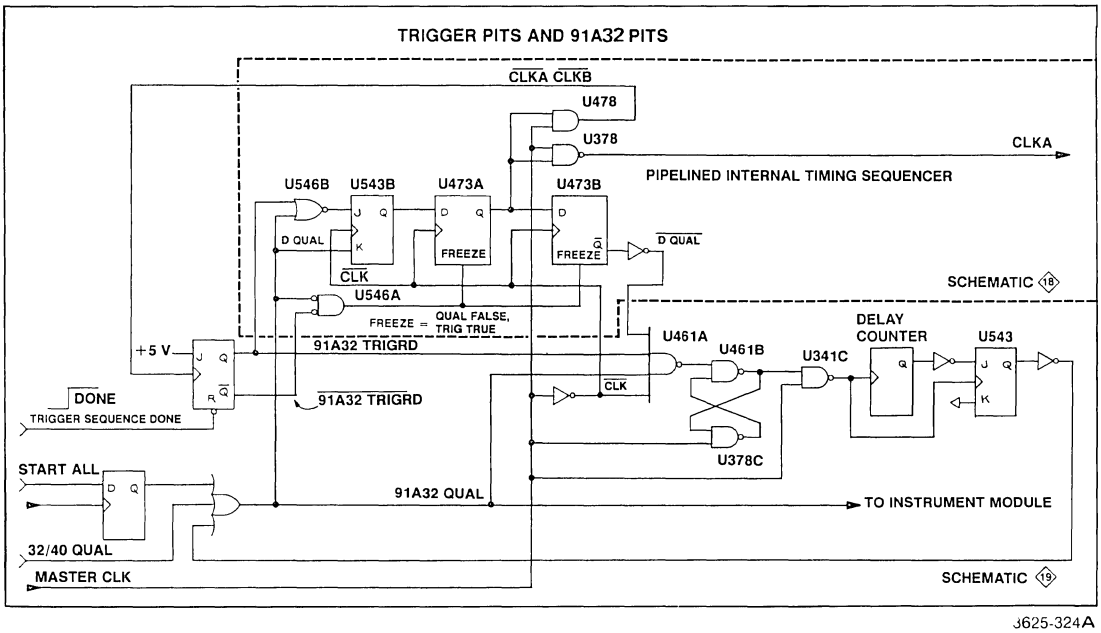


Figure 4-28. Simplified trigger shutdown circuit diagram.

acquired word are not processed on the same clock cycles. The pipeline is initiated at start-up time as shown in Figure 4-29. The pipeline is preset by the CLEAR(L) line.

If the qualifier goes low (stops storage) before the trigger occurs, the pipeline performs the action diagramed in Figure 4-30. This action:

1. stops CLKA(H), CLKA(L), and CLKB(L) one cycle after the qualifier signal goes low, and

2. makes the DQUAL(H) go low two cycles after the qualifier signal goes low.

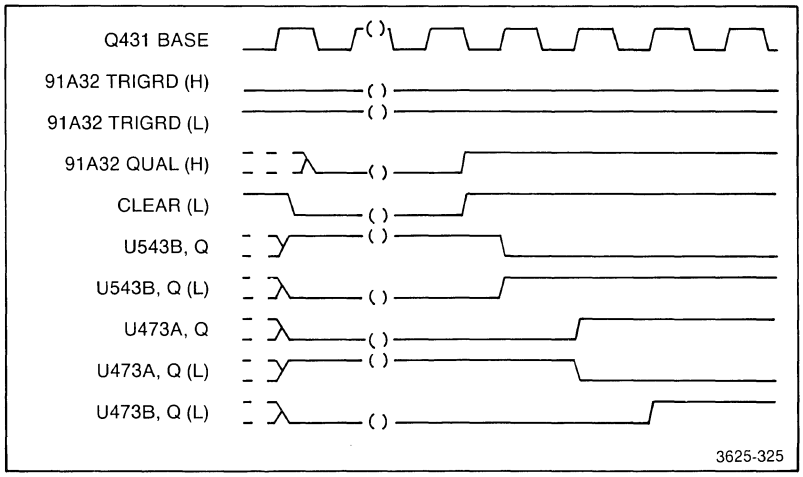


Figure 4-29. Initiating the pipelined internal timing sequencer.

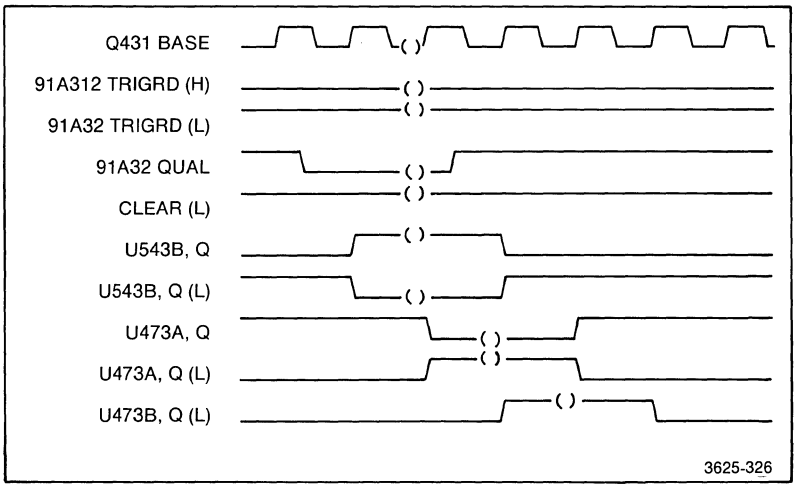


Figure 4-30. Qualifying before triggering the pipelined internal timing sequencer.

When the qualifier line returns high, the clocks and the DQUAL return to their normal states after one and two clock cycles, respectively.

After trigger conditions have been fulfilled, the 91A32 TRIGGERED(H) and 91A32 TRIGGERED(L) signals go active. If the 91A32 QUALIFIER(H) line is high, the output of the pipeline does not change from its previous output. The inputs to NOR gate U546B and inverting input AND gate U546A change, but the outputs do not change.

After the trigger occurs, if the qualifier line goes low, the J and K inputs to all three registers in the pipeline are driven low by the gates in front of the inputs to the registers. Writing low to both the J and K inputs of a register locks up the register so it will continue to output the previously logged-in data. This action prevents the low state of the qualifier from passing through the pipeline and stopping CLK1(H), CLK1(L), and CLK2(L) or changing the DQUAL(H) state.

TRIGGER/TIME BASE TRIGGER CIRCUITS 

Event Conditioner

The trigger receives EVENT 1, 2, and 3 recognition signals from the high speed bus. The event conditioner controls how the trigger will react to these signals.

The EVENT 1, 2, and 3 signals are clocked in from the high speed bus through registers U446A and B, and U445A. The EVENT 2 and 3 signals may be inverted by exclusive-OR gates U443D and C, respectively, depending on the INV2 and INV3 signals. The 1OR2 line influences the state of pins 4, 10, and 11 in U451, and thus changes the way events 1 and 2 are decoded. The EVENT 1 and (possibly inverted) EVENT 2 signals are then decoded by U451 and the 1OR2 line. Table 4-18 lists the outputs of the decoder for each circumstance. Table 4-19 shows how the INV2, INV3, and 1OR2 lines are set for each triggering mode.

Table 4-18
A, B Decoding

EVENT 1	EVENT 2	1OR2	AAA	BBB
0	0	0	0	0
1	0	0	1	0
0	1	0	0	1
1	1	0	1	1
0	0	1	0	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

Table 4-19
Trigger Mode Setting

Inputs				Menu Setting		
1OR2	INV2	INV3	TRIGGER ON	[	]	RESET ON
1	0	0	[1]			[3]
0	0	0	[1]	Followed By	[2]	*[3]
0	0	1	[1]	Followed By	[2]	[XXX]
1	0	0	[1]	Or	[2]	[3]
0	1	0	[1]	Then Not	[2]	[3]

Note: Events 1, 2, and 3 may be any combination of data and don't cares except at *. At * Event 3 may be anything except all don't cares.

Arm Trigger

The arm trigger circuits determine what signals go to the A counter. The AAA(H) line gets clocked through U155B by CLKB(L). The Q(L) goes low, passes through U151C, and resets flip-flop U155B. This results in a negative-going spike from Q(L) of U155B, which is sent to A counter U255. This flip-flop can be reset by holding any of the lines to OR gate U151C low. The signals that reset the flip-flop are ARM(H), A DONE(L), and Q(L) from pin 7 of the same flip-flop.

BBB(H) and CCC(H) are controlled in the same way as AAA(H). The BBB flip-flop, U155A, is reset by ARM(H), by pin 9 of U245B, and by its own Q(L). The CCC flip-flop, U145B, is reset by ARM, by pin 9 of U245B, and by its own Q(L). The output of the BBB flip-flop is used in the trigger circuits. The output of CCC flip-flop U145B reloads the A counter.

A Counter

The one's complement of the TRIGGER ON OCCURRENCE number in the Trigger Specification menu is loaded into registers U271 and U274 by the Trigger/Time Base controller interface, schematic 15. Before the DAS starts to acquire data, the data in these registers is loaded into presettable counters U255, U261, U161, and U165 by the CLEAR(L) signal. The counters can also be reloaded by the CCC flip-flop, U145B.

After loading, the counters are advanced one count by a negative-going spike from AAA flip-flop. When all the A counter's outputs are high, A DONE(L) is generated by AND gates U265A, B, and D, and 13-input NAND gate U248. A DONE(L) resets the AAA flip-flop so that the A counter cannot be advanced further, and writes a low signal to the D input of flip-flop U245B.

Trigger

When A DONE(L) is low, the first BBB signal through U155A clocks a low into U245B. A low from U245B means that the trigger conditions have been met. This low resets flip-flops U155A and U145B. The low in U245B also releases the reset state that was holding U145A low.

When U145A is released from the reset, Q(L) goes low at the next falling edge from CLKA(L). The low from the Q(L) output of U145A is the 91A32 TRIGRD(L) signal and drives inverter U435E to produce the 91A32 TRIG 0(H) signal. The Q(H) output of U145A goes high–which produces the 91A32 TRIGRD(H) signal, and provides a high to the input of NAND gate U461A.

If all the inputs to NAND gate U461A are high, the output goes low. This allows CLK(H) pulses from NAND gate U378C to pass through NAND gate U461B, so that CLK(H) is output by NAND gate U341C. These pulses clock the delay counter.

Delay Counter

The delay counter is loaded with the delay count by the Trigger/Time Base controller interface. Presettable counters U351, U361, U345, and U365 are preset to the one's complement of the value in the DELAY field of the Trigger Specification menu.

Whenever the output of U341C presents a negative going edge to CLK1 of U351, the counters increment. When every output of the delay counters is high, AND gates U371A, U371B, U371D, and 13-input NAND gate U355 generate a signal through inverter U341A. This signal goes high when the counters read FFFF hexadecimal, and returns low on the next clock, when the counters wrap around to 0000 hexadecimal. Flip-flop U543A is clocked on that falling edge.

CLK(H) from U341C to U543A sets its Q(H) line high. This turns on transistor Q538 so that 91A32 QUALIFIER BUS(L) goes active. This inputs a low signal to NAND gate U461A, inhibiting the clock to the delay counter.

It is also possible to make the 91A32 QUALIFIER BUS(L) active by writing a START ALL(L). This turns on Q539, bypassing the rest of the triggering circuits. START ALL(L) is the signal that allows all 91A32 modules to start acquiring data by releasing the 91A32 QUALIFIER BUS(L) signal.

TRIGGER/TIME BASE INTERNAL CLOCKS 

Time Base Clock

The components around U100D and crystal Y100 form a high stability 100 MHz clock. Inverter U100C is set up as an oscillator by connecting its output to its input. Capacitor C202, however, is set up as a low-pass filter so oscillating is an unstable condition. The inverter is then forced into

"dc oscillation", at a stable value intermediate to the two ECL threshold levels. This intermediate value is called V_{bb}.

Since the stability of U100C would be upset by the oscillation of the crystal, a notch filter is used to provide isolation. L101 and C201 form a notch filter centered at 92 MHz, which stops the crystal from unsettling U100C, but allows V_{bb} to pass. The steady intermediate voltage, V_{bb}, keeps U100D triggering regularly. U100B is a buffer to keep the oscillator stable.

Frequency Divider

The 100 MHz clock output from U100B is fed to counter U215. The Q1 output of U215 is a divide by two, which gives a 20 ns clock output. The Q2 output of U215 divides by five to provide a 50 ns clock. These outputs again are divided by two, by U315B and U315A, respectively, to yield a 40 ns clock and a 100 ns clock.

The associated transistor pairs (Q212, Q211, Q311, and Q312) are ECL to TTL converters. Inverter U100A and capacitor C214 provide an ECL triggering threshold, V_{bb}, for the ECL to TTL converters.

There is also a decade divider consisting of U235A and B, and U241A and B. Each of the counters in the decade divider divides an input signal by ten, starting from a 100 ns input. The decade divider provides clock periods of 1 μs, 10 μs, 100 μs, and 1 ms.

91A08 Clock Selector

The Trigger/Time Base controller interface writes the rate for the 91A08 INT CLK into register U141. If bits D0 or D1 are high, then data selector U471A will choose either the 10 ns, the 20 ns, or the 40 ns clocks as output through the AND gates in U415. If any of bits D2 through D5 are high in U141, a decoding action occurs. Bits D4, D5, and D6 are used to select a 100 ns, 1 μs, 10 μs, 100 μs, or 1 ms clock through data selector U325.

The selected clock from the frequency divider goes to bi-quinary divider U325. The outputs of this divider, as well as the 50 ns clock, go to U335 where one clock is selected by bits D2, D3, and D4. The selected clock is then output from U335 and converted to ECL to be transmitted on the 91A08 INT CLK(L) line of the high speed bus. Table 4-20 lists the hexadecimal code that is written to U141 to define which clock is used.

Table 4-20
91A08 Internal Clock Selection Code

Hex Code	Clock Rate	Hex Code	Clock Rate	Hex Code	Clock Rate
00	Off	30	500 ns	88	100 μs
01	10 ns	48	1 μs	8C	200 μs
02	20 ns	4C	2 μs	90	500 μs
03	40 ns	50	5 μs	A8	1 ms
04	50 ns	68	10 μs	AC	2 ms
28	100 ns	6C	20 μs	B0	5 ms
2C	200 ns	70	50 μs	E8	Single Step

91A32 Internal Clock Selector

The Trigger/Time Base controller interface writes the rate for the 91A32 INT CLK into register U135. If bit D0 is high, the 40 ns clock will be the output through buffer U425A. Otherwise, the selector is similar to the clock selector in the 91A08 time base. Refer to the 91A08 time base circuit description for more details. The hexadecimal code that is written to U135 to define the rate for the 91A32 internal clock is listed in Table 4-21.

Table 4-21
91A32 Internal Clock Selection Code

Hex Code	Clock Rate	Hex Code	Clock Rate	Hex Code	Clock Rate
00	Off	4C	2 μs	90	500 μs
03	40 ns	50	5 μs	A8	1 ms
04	50 ns	68	10 μs	AC	2 ms
28	100 ns	6C	20 μs	B0	5 ms
2C	200 ns	70	50 μs	E8	Single Step
30	500 ns	88	100 μs		
48	1 μs	8C	200 μs		

DATA ACQUISITION DETAILED CIRCUIT DESCRIPTIONS

P6452 DATA ACQUISITION PROBE

The Data Acquisition Probe is used by the 91A32 and 91A08 acquisition modules as well as by the Trigger/Time Base. The probe is used to acquire qualifier signals and data to be stored. Refer to the probe circuit description immediately following the circuit descriptions of the instrument modules for more details.

91A32 DATA ACQUISITION MODULE

The 91A32 Data Acquisition Module can acquire 32 independent channels of information at speeds up to 25 MHz. The module also has a three-word event recognizer that works with the Trigger/Time Base for triggering. Data can be stored up to 512 sets deep. All component numbers in the 91A32 module circuit description are assumed to have an A12 preface unless otherwise noted.

This description will be divided into several sections. The section divisions will be by schematic and then by functional blocks on the schematic. Numbers in diamonds refer to the numbers on schematic tabs in the Diagrams section of this manual. Those schematics should be referred to while reading the circuit description. For an overview of the 91A32 acquisition module's circits, refer to the 91A32 in the General System Description, earlier in this section.

91A32 CONTROLLER INTERFACE 

The 91A32 controller interface takes data from the Controller board and sends it to appropriate registers by decoding the lowest four bits on the address bus and interpreting BWR(L), PORT(L), and BRD(L) from the Controller board. The interface also takes data from the module and writes it on the data bus at the command of the Controller board.

For example, suppose the Controller board is reading the MOS switch status. The address bus has 2 hexadecimal written on the least significant four bits. Simultaneously, PORT(L) and BRD(L) go active. This action enables decoder U341, which decodes the address; pin 3 goes active (low). The MOS status register, U241, is then enabled and puts data on the data bus.

The writing procedure is similar, except the BWR(L) and PORT(L) signals must be active to enable decoders U441 and U451. Bit 3 of the address bus selects between these two decoders while a write procedure is occurring. Table 4-22 shows which registers are connected to the data bus by each hexadecimal address and the BWR(L), BRD(L), and PORT(L) lines.

Table 4-22
91A32 — Controller Interface Map

Addr	BWR	BRD	PORT	Line Name	ICs Affected	
					U#	Schem.#
XXX0	X	L	L	CARD ID STRB(L)	U245	20
XXX1	X	L	L	POD DETECT RD(L)	U335	20
XXX1	L	X	L	DAC DATA REG(L)	U661	20
XXX2	X	L	L	MOS RD(L)	U241	20
XXX2	L	X	L	CNTL REG(L)	U665	20
XXX3	X	L	L	MAR RDBK(L)	U251	24
XXX3	L	X	L	CHIP SEL REG(L)	U658	20
XXX4	X	L	L	EBR0(L)	U165 & U168	23
XXX4	L	X	L	MAR CLK(L)	U655A & B	24
XXX5	X	L	L	EBR1(L)	U171 & U175	23
XXX5	L	X	L	WD REC WE 0(L)	U465 & U468	25
XXX6	X	L	L	EBR2(L)	U178 & U181	23
XXX6	L	X	L	WD REC WE 1(L)	U471 & U475	25
XXX7	X	L	L	EBR3(L)	U185 & U188	23
XXX7	L	X	L	WD REC WE 2(L)	U478 & U481	25
XXX8	X	L	L	OBR0(L)	U265 & U268	23
XXX8	L	X	L	WD REC WE 3(L)	U485 & U488	25
XXX9	X	L	L	OBR1(L)	U271 & U275	23
XXX9	L	X	L	SINGLE STEP	U638	24
XXXA	X	L	L	OBR2(L)	U278 & U281	23
XXXA	L	X	L	O-MAR LD(L)	U655A & B	24
XXXB	X	L	L	OBR3(L)	U285 & U288	23
XXXB	L	X	L	Q0 SET(L)	U233A	24
XXXC	L	X	L	Q1 SET(L)	U233B	24
XXXF	L	X	L	INIT(L)	U233A & B & U153A	24

Probe Threshold

The 91A32 controller interface writes level-setting information to register U661. This level-setting data in U661 controls digital-to-analog converter (DAC) U152. This DAC has a current output that is converted to voltages by op amps U122, U133, U140, and U142.

The VREF– input to the DAC is supplied by op amp U105. U105 compensates for differences between the DAS ground and the ground of the circuit under test. VREF+ is set by variable resistor R147. The voltage at VREF+ is set by adjusting the potential between TP147 and TP148 to 1.60 V with the greatest possible accuracy. This voltage sets the current supplied if the most significant bit is set. Less significant bits are controlled by an internal current divider.

IO(H) and IO(L) are the DAC outputs. IO(H) is a current sink that is proportional to the 8-bit input. IO(L) sinks a current proportional to the one's complement of the 8-bit input. The sum of these current sinks is a constant current. The constant current is set by Zener diode VR148 and variable resistor R147.

The current out of the IO(H) pin of the DAC is converted to threshold voltages by op amps U122, U133, U140, and U146. The offset voltage of each of these op amps is individually set with trimmer potentiometers.

The solid state switches in U134 control whether the op amp acts as a voltage follower (switch open) or as a voltage multiplier (switch closed). When a switch is closed, the inverting input of the associated op amp is controlled by a voltage divider that sets the inverting input to 1/4 of the output voltage of the op amp. If a switch is open, the voltage divider is disconnected from the ground reference and the op amp acts as a voltage follower (because the feedback resistance matches the input resistance).

91A32 POD A AND B RECEIVERS 

Pod A Receivers

Each probe receiver is identical, so only one receiver will be described. Refer to Figure 4-31 while reading this circuit description.

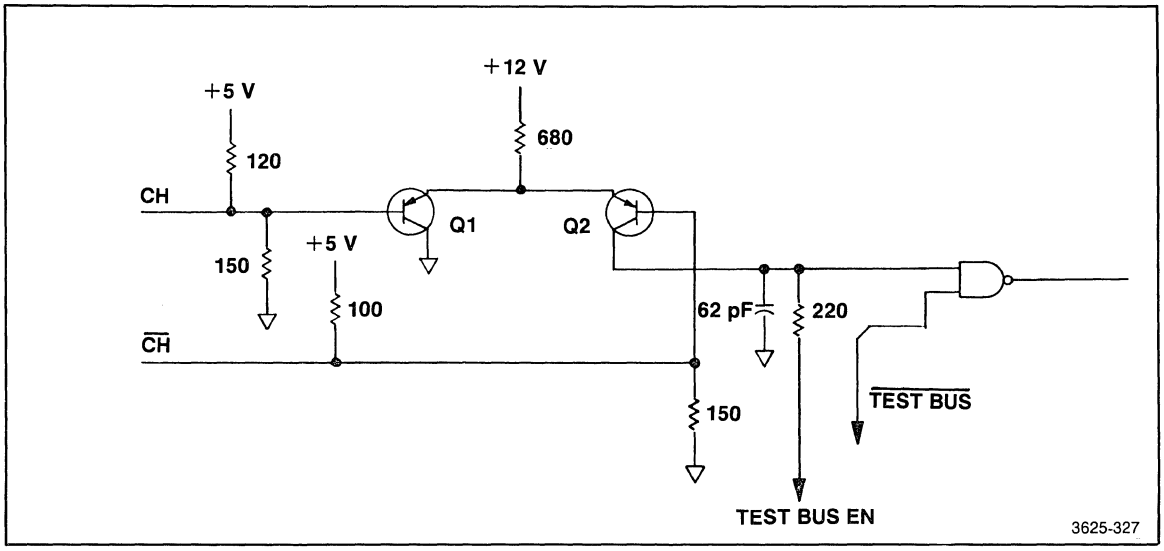


Figure 4-31. 91A32 probe receiver.

TEST BUS EN(L) is inverted and allows the TBD0—TBD7 bus to write data into the acquisition memory as though it were coming from a probe. This is done by pulling the probe input to the NAND gate high. The 220 Ω resistor is usually a pull down resistor, but when the test bus is enabled, it pulls up to +5 V. This pulls the probe input to the NAND gate high, so TBD0—TBD7 can write data through the NAND gates. When the test bus is not in use, all of its lines are programmed high, otherwise they would mask out data from the probe.

Pod B Receivers

The receivers for pod B are identical to the receivers for pod A, discussed previously. Refer to the pod A receiver discussion for more information.

Transistors Q1 and Q2 and the 680 Ω resistor are a differential ECL to TTL translator. The resistors attached to the bases of these transistors are line terminators to match impedance of the transmission line. The 220 Ω resistor and the 62 pF capacitor are a time delay. The delay allows the selected clock sufficient time to be set up before clocking through data.

91A32 POD C AND D RECEIVERS 

The receivers for pods C and D are identical to the receivers for pod A, discussed previously. Refer to the pod A receiver discussion for more information.

91A32 ACQUISITION MEMORY 

Log-in Registers

Data from the probe receivers is clocked through registers, U121, U221, U321 U421, U521, and U621 and inverted by buffers U125, U225, U325, U425, U525, and U625. This deskews the data and corrects the polarity.

Even Acquisition Memory

The even register (U131, U231, U331, U431, U531, and U631) is clocked at one half the selected clock rate, so only every other set of data from the probes gets clocked through. The data out of this register goes to both the even acquisition memory and the even word recognition RAM (schematic 25).

The even acquisition memory, U165, U168, U171, U175, U178, U181, U185, and U188, stores alternate sets of data from the probes. The other sets of data are stored by the odd acquisition memory. The memory is loaded from the even register with all 32 bits from the probes. While acquiring data, the WE(L) lines are all enabled by the even write-enable generator (schematic 24). The memory can store 256 sets of data for future readback. Before acquisition starts, the CS0—CS3(L) bus must have all low voltages written on it.

The Controller board can only read data 8 bits at a time. The acquisition memory is divided into four 8-bit bytes for readback purposes. Each 8-bit section can be read back by writing a low on both the EBR0—EBR3(L) bus and the CS0—CS3(L) bus to the memories to be read.

Even Acquisition Readback

When the Controller board is reading back data from even acquisition memory, one line on the EBR0—EBR3(L) bus must go low. That selects which 8-bit byte of memory will be read. The EBR0—EBR3(L) bus has all of its lines NORed by U345B to enable buffer U351. The output of the buffer is connected to the data bus, so the memory byte can be read by the Controller board.

Odd Acquisition Memory

The odd acquisition memory stores the alternate sets of data that are not stored by the even acquisition memory. The odd acquisition memory is functionally identical to the even acquisition memory, except for being clocked by the ODD REG CLK(H) rather than the EVEN REG CLK(H). For further details refer to the even acquisition memory circuit description.

Odd Acquisition Readback

The odd readback is functionally identical to the even readback. When the Controller board is reading back data from odd acquisition memory, one line on the ORB0—ORB3(L) bus must go low. That selects which 8-bit byte of memory will be read.

The ORB0—ORB3(L) bus has all of its lines NORed by U345A to enable buffer U361. The output of the buffer is connected to the data bus, so the memory byte can be read by the Controller board.

91A32 TIMING CIRCUITS 

Clock Select

CLK1, CLK2, and CLK3, from the External Clock Probe; the 91A32 INT CLK(L); and the SINGLE STEP(H) signal are inputs to data selector U638. The external clock lines are deskewed by comparators U635A, B, and C. Data selector U638 then outputs the clock line selected by the CLK SEL 0 - CLK SEL 2(H) bus. An octal listing of the clock select code written on the select bus is shown in Table 4-23. The clock output from the data selector is converted to TTL levels by transistors Q533 and Q534.

Table 4-23
91A32 Clock Select Code

Hex Code	Selected Clock	Hex Code	Selected Clock
0	SINGLE STEP(H)	4	CLK2(L)
1	91A32 INT CLK(L)	5	CLK2(H)
2	CLK3(L)	6	CLK1(L)
3	CLK3(H)	7	CLK1(H)

Qualifier Logic

Qualifiers from the probes are clocked through flip-flops U233A and B by the selected clock. If INIT(L) goes active, both of these flip-flops are reset until INIT(L) goes inactive. The outputs of the

flip-flops are sent to inputs of the NAND gates in U641. These NAND gates allow the 91A32 controller interface to select which qualifier is enabled, and what polarity it is, through the QEN0—QEN3(H) bus. Any disabled qualifier has 0 written to its NAND gate by the QEN0—QEN3(H) bus, masking the qualifier signal.

The outputs of these open collector NAND gates are wire-ANDed and used as an input to NAND gate U646A and to register U651A. These two inputs provide two different paths for the signal to follow. One or the other of the paths is selected by the Q+1 EN(H) signal from the 91A32 controller interface.

In SPLIT CLOCK mode, when the 91A32 module is being clocked by anything other than the master clock, the qualifier signal must have an extra clock cycle added before it is used by the 91A32.

Register U651A adds that extra cycle through the use of the Q+1 EN(H). In any other clocking mode, the extra clock cycle must not be present.

If Q+1 EN(H) is low, register U651A is held reset and NAND gate U646A inverts the qualifier signal from U641. If Q+1 EN(H) is high, register U651A clocks through the qualifier signal from U641; however, NAND gate U646A has its output held low by the signal from inverter U646B.

If the qualifier is not passing through register U651A, then whenever the the qualifier signal from U641 is high (that is, no qualifiers are in their inactive state) register U655B and exclusive-OR gates U645C and U645D oscillate at one half the clock frequency. If the qualifier line goes active (low) the oscillations stop at the next clock edge.

If the qualifier signal is being passed through register U651A, there is a one clock cycle delay before the oscillation of U655B is shut down by the qualifier.

The output of oscillator U655B is duplicated by register U655A to provide sufficient fan-out.

EVEN WORD(H) is used by the Controller board to find out where the last data was stored in acquisition memory. If EVEN WORD(H) is high, the last word written was in the even side memory at the OMAR address plus one. If EVEN WORD(H) is low, the last acquired data was written to the odd side memory at the OMAR address. See the following description of the memory address registers.

Memory Address Registers

The memory address registers control the address where data in the acquisition memory is read or written.

When the Controller board loads an address into the address counter, EMAR LD(L) goes active. The EMAR (even memory address register, U158 and U161) is then loaded with the contents of the D0-D7 bus. This value is then output by the EMAR. The EMAR counts up from this value each time it is clocked by the EVEN WORD(H) signal.

The output of the EMAR then addresses the even acquisition memory. The output from the EMAR is also clocked into the OMAR (odd memory address register, U261 and U255C and D) by the WRD REC MUX CONT(H) clock; the complement of EVEN WORD(H). The OMAR output is used to address the odd acquisition memory. The OMAR output can also be read back by the Controller board through tri-state buffer U251.

All Valid Register

The most significant bit of the OMAR (pin 7 of U255) clocks register U153A. INIT(L) resets register U153A, so it initially has a low output. If the register gets clocked, the output goes high and does not change with subsequent clocks. The msb from the OMAR has a falling edge when the OMAR has incremented past 256 decimal. The ALL VALID(H) line, from register U153A, is then used by the Controller as an indication that all the addresses in the acquisition memory contain valid data.

Even Write-Enable Generator

Data must be clocked into the even acquisition memory at the same rate it is clocked out of the even register. However, because of propagation delays and set up times, the same clock cannot be used for both purposes. The even write-enable generator generates a new clock from the EVEN REG CLK(H) to be used by the even acquisition memory. The EVEN WE(L) output of the write-enable generator has two special characteristics: its rising edge is delayed for a specified time after the rising edge of the EVEN REG CLK(H), and the pulse is high for a specified period of time independent of the EVEN REG CLK(H). Figure 4-32 shows a timing diagram for one cycle of the write-enable generator.

Inverter U435A inverts the EVEN REG CLK(H) so the rising edge of the clock becomes a falling edge. The falling edge is integrated by RC network R325, C351, C352, and C345. When the integrated signal goes below the TTL threshold level, inverter U346A outputs a high. When the EVEN REG CLK(H) goes low, inverter U435A outputs a high that is passed through diode CR352 to charge the capacitors. This section of circuitry is now ready to receive another EVEN REG CLK(H) rising edge.

The output of inverter U346A clocks register U155A. If RAM DIS(H) is low (which means acquisition is enabled), the Q(L) output of U155A goes high when it is clocked. The Q(L) output is inverted by U346F, which outputs a falling edge. The falling edge is integrated by R156, C156, C158, and C243. When the integrated signal falls below the TTL threshold level, buffer U151A outputs a low, which sets register U155A. Setting the register forces Q(L) low so inverter U346F outputs a high. This high output charges C156, C158, and C243 through diode CR156. As the capacitors charge, the output of buffer U151A goes high, so the register is no longer set. The register is now ready to receive another clock pulse from inverter U346A.

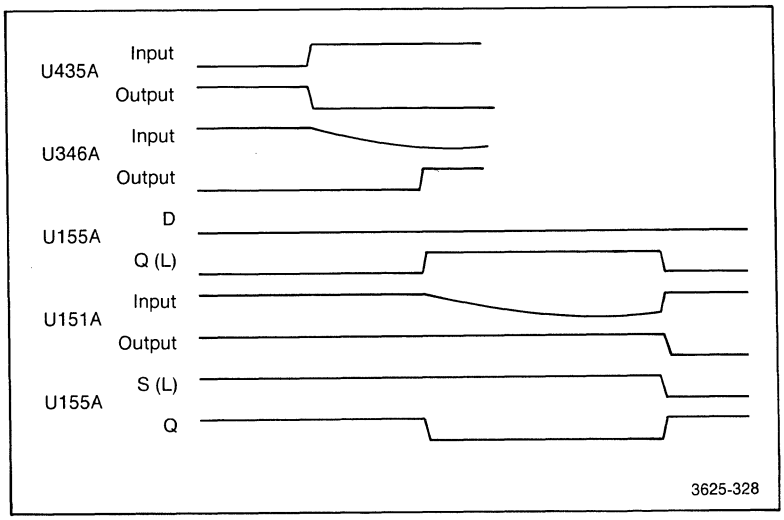


Figure 4-32. 91A32 even write-enable generator timing diagram.

Jumpers W245 and W445 give the write-enable generator a broader adjustment range. If the pulse delay or duration is too short, a jumper may be placed to disable capacitors C345 and/or C243. If the delay or duration is too short, the straps may be placed to enable these capacitors.

Odd Write-Enable Generator

The odd write-enable generator provides write-enable pulses for the odd acquisition memory. The odd write-enable generator is functionally identical to the even write-enable generator. Refer to the even write-enable generator circuit description for more information.

91A32 WORD RECOGNIZER 

Even Word Recognizer RAM

The even word recognizer RAM (U465, U471, U478, and U485) is designed to look for specific words that are output on the EW0—EW31 bus.

To understand how the RAM is used for word recognition, consider the memory as an addressable register. The memory is programmed by writing 1s in all the addresses that correspond to the words to be recognized, and 0s in all other addresses. After programming, the stream of data containing the word to be recognized is used to address the RAM. When the RAM outputs a 1, the word is recognized.

Since the words to be recognized may have X (don't care) as an element, programming becomes slightly more complicated. If the word to be recognized is 10100110, a single 1 must be written into memory. If X0100110 is to be recognized, 1s must be loaded at both addresses 00100110 and 10100110. If XX100110 is to be recognized, 1s must be loaded at four different addresses. So, if XXXXXXXX is to be recognized, all 256 addresses must have 1s written in them.

Since 32 bits have to be recognized, four 8-bit RAMs are used. Each RAM recognizes eight of the 32 bits involved. All four of the RAMs must recognize their words at the same time for triggering to occur.

Each RAM is used to recognize three different words: Event 1, through the D1 lines; Event 2, through the D2 lines; and Event 3, through the D3 lines. The D4 lines are for future expansion.

Odd Word Recognizer RAM

The odd word recognizer RAM (U468, U475, U481, U488) is functionally identical to the even word recognizer RAM. For further details, read the even word recognizer RAM circuit description.

Word Recognizer Multiplexer

Since all four word recognition RAMs must output high signals at the same time for a word to be recognized, the outputs of the RAMs are NANDed by U675, U681, U685, and U688. The output of a NAND gate goes low to signal word recognition.

The data from the probes was divided into two alternating sides—even and odd. These two sides are clocked 180° out of phase with each other. Since word recognition from either the even or

odd side is valid, the word recognition signals from the two sides are multiplexed so there are only three word recognition signals, not six. (The fourth word recognition signal, through NAND gates U688A and B, is not used.) The word recognition signals are multiplexed by U671. The output of the multiplexer is clocked through register U545A.

The signals from register U545 will be masked out by NAND gates U541A, B, C, and D if WD REC EN(H) is low. If WD REC EN(H) is high, the signals are inverted by these NAND gates and passed onto the high speed bus on the Interconnect board.

Exclusive-OR gate U645A has EVENT2(H) and EVENT3(H) as inputs. The output of U645A can be read by the Controller board. This is used during diagnostic exercises to see if the EVENT2(H) and EVENT3(H) lines are acting properly.

P6452 DATA ACQUISITION PROBE

The data acquisition probe is used by the 91A32 and 91A08 acquisition modules as well as the Trigger/Time Base. The probe is used to acquire qualifier signals and data to be stored. Refer to the probe circuit description immediately following the circuit descriptions of the instrument modules for more details.

91A08 DATA ACQUISITION MODULE

The 91A08 Data Acquisition Module can acquire eight independent channels of information at speeds up to 100 MHz. The module has a single-word event recognizer for triggering, stores up to 512 data words, and recognizes and stores glitches. All of the component numbers used in the 91A08 module circuit description are assumed to have an A13 preface.

This circuit description will be divided into several sections. The section divisions are by schematic and then by functional blocks on the schematic. Numbers in diamonds refer to the numbers on schematics tabs in the diagrams section. Those schematics should be referred to while reading the circuit description. For an overview of the 91A08 acquisition module's circuits, refer to the 91A08 in the General System Description earlier in this manual.

91A08 CONTROLLER INTERFACE 

The 91A08 controller interface takes data from the Controller board and sends it to appropriate registers by decoding the lowest four bits on the address bus and interpreting BWR(L), PORT(L), and BRD(L) from the Controller board. The interface also takes data from the module and writes it on the data bus at the command of the Controller board.

For example, suppose the Controller board is reading the probe status. The address bus has 9 hexadecimal written on the least significant four bits. This address is inverted to 6 hexadecimal by U671A—C, and H. Simultaneously, PORT(L) and BRD(L) go active. This action enables decoder U675, which decodes the address bus so that Y6(L) (pin 9) goes active. Pod status register U678 is then enabled and lets data onto the data bus. The writing procedure is similar, except the BWR(L) and PORT(L)signals must be active to enable U171. Table 4-24 shows which registers are connected to the data bus by each hexadecimal address and the BWR(L), BRD(L), and PORT(L) lines.

Table 4-24
91A08 Controller Interface Map

Hex Addr	RESET	BWR	BRD	Port	Line Name	ICs Affected U#	ICs Affected Schem.#
XXX0	X	X	L	L	CARD ID(L)	U695	26
XXX1	X	X	L	L	POD STATUS(L)	U678	26
XXX1	H	L	X	L	THRESHOLD(L)	U118	26
XXX2	X	X	L	L	MOS STATUS(L)	U681	26
XXX2	H	L	X	L	CLK SEL(L)	U131	30
XXX3	X	X	L	L	MAR RD(L)	U175D	26
XXX3	X	L	X	L	MAR LD(L)	U255 & U258	29
XXX4	X	X	L	L	MEM RD(L)	U175D & B	26 & 29
XXX4	X	L	X	L	MEM LD(L)	U175B	29
XXX5	X	X	L	L	DIFF0(L)	U688	30
XXX5	X	L	X	L	DELAY0(L)	U155	31
XXX6	X	X	L	L	DIFF1(L)	U691	30
XXX6	X	L	X	L	DELAY1(L)	U151 & U145	31
XXX7	H	L	X	L	WD REC DATA(L)	U125	27
XXX8	H	L	X	L	WD REC CONT(L)	U128	27
XXXA	H	L	X	L	GLITCH CONT(L)	U121	27
XXXB	H	L	X	L	TRIG CONT(L)	U135	31
XXXC	H	L	X	L	QUAL MEM CONT(L)	U141	29

+3 V Power Supply

The +3 V power supply is used for biasing ECL circuits on the 91A08. Since +3 V is not supplied by the power supplies, it is created on the module by this +3 V switching current pump.

In ECL circuitry, the +3 V biasing supply tends to float up to +4 V. The +3 V supply must then dispose of surplus current to keep the supply at 3 V. This supply disposes of the surplus current by bootstrapping it into the +5 V supply. The +5 V Power Supply Module that is driving the 91A08 then adjusts for the extra current to maintain the +5 V regulation.

Resistors R399, R397, and R398 form a voltage divider to give a +3 V reference to comparator U298A. The non-inverting pin of the comparator is connected to the +3 V line through R392.

Whenever the +3 V goes over-voltage, the output of comparator U298A goes high, which turns on Q298 and turns off Q297. This raises the base voltage at Q295, and the side of L290 tied to Q295 is pulled to ground.

When the side of L290 that is attached to Q295 is pulled to ground, current flows from the +3 V supply into L290. Because of the inductance of L290, most of the current drawn is stored in the magnetic field of the inductor rather than going through Q295 to ground.

When inductor L290 has drawn enough current, the +3 V line drops below the reference voltage. This reverses the above procedure, halting conduction by Q295. (Resistors R392 and R396 provide hysteresis so the regulator does not oscillate.) When Q295 stops conducting, L290 stops drawing current from the +3 V supply. However, there is still a magnetic field around L290 that stores the energy previously pulled out of the +3 V supply.

The magnetic field around L290 starts to collapse when Q295 stops conducting, so L290 is forced to dissipate as much power as it absorbed from the +3 V supply. The only place that the power can be dissipated is through CR291 into L292. The result is that L290 forces out a pulse of current at +5 V, which goes through CR291 into the +5 V supply. L292 evens out the current spikes coming through CR291 to ease regulation of the +5 V supply.

Comparator U298B works as an over-current sensor by monitoring the voltage across R191. If Q295 is conducting too much of the time, the current through L290 will become great enough to activate this comparator and shut down Q295.

Probe Threshold

The 91A08 controller interface writes level-setting information to digital-to-analog converter (DAC) U118. THRESHOLD(L) clocks the level-setting information into the DAC. The DAC outputs current that is converted to voltage by op amps U101 and U201.

The VREF– input of the DAC is supplied by op amp U211. U211 compensates for differences between the DAS ground and the ground of the circuit under test. VREF+ is set by variable resistor R110. The voltage at VREF+ is set by adjusting the potential between TP106 and TP111 to 1.60 V with the greatest possible accuracy. This voltage sets the current supplied if the most significant bit is set. Less significant bits are controlled by an internal current divider.

IO(H) and IO(L) are the DAC outputs. IO(H) is a current sink that is proportional to the 8-bit input. IO(L) sinks a current proportional to the one's complement of the 8-bit input. The sum of these currents is constant. The constant current is set by Zener diode VR106 and variable resistor R110.

The current out of the IO(H) pin of the DAC is converted to a voltage by each of op amps U101 and U201. The offset voltage of each op amp is set with trimmer potentiometers.

Solid state switch U115 controls whether op amp U201 acts as a voltage follower (switch open) or as a voltage multiplier (switch closed). When a switch is closed, the inverting input of U201 is controlled by a voltage divider (R202 and R203) that sets the inverting input to 1/4 of the output voltage of the op amp. If a switch is open, the voltage divider is disconnected from the ground reference so the op amp acts as a voltage follower (because the feedback resistance matches the input resistance).

The output of U201 controls the threshold voltage of the data acquisition probe. The output of U101 controls the threshold voltage of the 100 MHz Clock Probe.

91A08 DATA RECEIVERS 

Data Probe Receiver

Each of the inputs from the data acquisition probe is level converted by a differential amplifier. All of the data inputs and the qualifier are then run through delay lines. This allows the clock to be set up by the clock selector and used when the corresponding data arrives at the glitch detect circuits.

Glitch and Word Recognizers

All glitch recognition and word recognition is performed by M218 integrated circuits U228, U325, U225, U328, U321, U221, U318, and U218. All the one-bit channels are identical, so only one channel will be described. Each M218 has several control lines. These control lines come from the word/glitch trigger control block. The pin numbers in the following list refer to the M218 ICs in the glitch and word recognizer block.

- **GRFIN** (pin 15) is held high if glitch triggering is set on this probe bit; otherwise it is held low.
- **WRFIN** (pin 7) is held high if this probe bit is part of a data word to be recognized.
- **PH/L** (pin 6) is high if this probe bit must be high for word recognition. If this probe bit must be low, the PH/L bit is low.
- **CLOCK** (pin 1) is used to clock out data and to reset the glitch sensor.
- **DIN** (pin 12) is for the data bit coming from the probe.
- **DOUT** (pin 3) shifts out the data that was present at DIN. GOUT (pin 2) goes high if there was a glitch in the DIN line inside the previous clock cycle.
- **WR(L)** (pin 8) is active if the previous probe data was the proper polarity for word recognition and the WRFIN line is high. Each WR(L) line is wire-ORed with three other WR(L) bits.
- **GR** bit (pin 14) becomes active if a glitch is detected and the GRFIN bit is high. Each GR line is wire-ORed with three other GR bits.

Word/Glitch Trigger Control

Three data registers in this block control the triggering for the 91A08. Registers U128 and U125 control triggering on data words. U121 controls triggering on glitch detection. (Also refer to the glitch and word recognizers circuitry.)

91A08 data word triggering consists of two parts:

- whether a bit is watched or ignored (care or don't care)
- whether a bit must be high or low to cause triggering.

U128 controls whether a bit is watched or ignored. If a bit is to be ignored, the corresponding line out of U128 writes out a low voltage. If a bit is watched, the corresponding line is high.

U125 controls the state each bit must be in (high or low) to cause a trigger.

U121 controls whether or not detecting a glitch on a line is a triggering condition.

91A08 ACQUISITION MEMORY 28

Even Acquisition Memory

The even register (U241, U238, U235, and U231) is clocked at one half the selected clock rate, clocking every other set of data from the probes through the even register.

AND/NAND gates U355, 251, 248, and 245 usually mask out the data on the ECLD0—ECLD7(H) bus because the ECL MEM ACC EN(L) line is high. However, whenever the Controller board needs to write data into the acquisition memory, it can do so through these AND/NAND gates.

For the Controller board to write data into the even acquisition memory, the ECL MEM ACC EN(L) line is pulled low. The data to be loaded into the memory must now be placed on the ECLD0—ECLD7(H) bus. The Controller also sets the address to be loaded and, finally, pulses the EVEN WE(L) line. For more information, refer to the memory read and load circuit description (schematic 29).

The even acquisition memory (U285, U281, U278, U271, and U268) stores alternate sets of data from the probes. The other sets of data are stored by the odd acquisition memory. This format of data storage is illustrated in Figure 4-33.

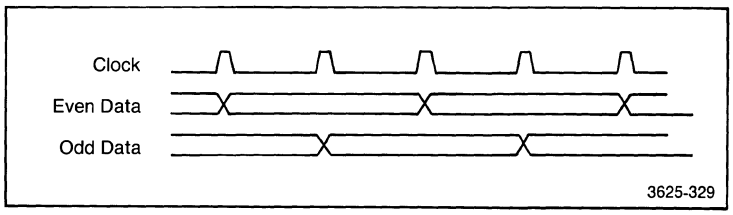


Figure 4-33. Data demultiplexing timing diagram.

The acquisition memory is loaded from the even register with 8 data bits, 8 glitch recognition bits, and 4 miscellaneous bits. While acquiring data, the WE(L) lines are all enabled by the even write-enable generator (schematic 29). The memory can store 256 sets of data for future readback.

The Controller board can only read data 8 bits at a time. The acquisition memory is divided into 3 bytes for readback purposes. Each byte can be read back by writing a low on the BS0—BS2(L) bus to the byte to be read.

Odd Acquisition Memory

The odd acquisition memory stores the alternate sets of data that are not stored by the even acquisition memory. The odd acquisition memory is functionally identical to the even acquisition memory, except for being clocked by ODD WE(L) rather than EVEN WE(L). For further details, refer to the even acquisition memory circuit description.

91A08 MEMORY AND QUALIFIER CONTROLS 29

Qualifier and Memory Control Register

This register is loaded with data from the 91A08 controller interface. The outputs of this register control the behavior of many of the qualifier and storage circuits.

Memory Read and Load Circuitry

These circuits allow the Controller board to read from or write to the acquisition memory. To do this, MEM ACC EN(H) goes active and MEM RD(L) (to read memory) or the MEM LD(L) (to write into memory) go active.

Every time MEM RD(L) or MEM LD(L) go active, counter U578 increments by one. When the counter hits 1000 binary, it gets loaded with all zeros so it can start counting up again.

The counting is decoded by U581 and then buffered by U585 to provide the BS0—BS6(H) bus. The end result is, every time a MEM RD(L) or MEM LD(L) is selected, while MEM ACC EN(H) is active, the BS0—BS6(H) bus gets advanced one position until all six bus lines have been enabled. Then the first bus line is enabled again.

In the event that the Controller board needs to load an address into the address counter, the MAR LD(L) line goes active. This starts the astable multivibrator built around Schmitt trigger U181B. The multivibrator will run for seven cycles and then be stopped by the QD output of counter U591B. The QA and QB outputs from counter U591B drive EVEN CLK(H) and ODD CLK(H) through flip-flop U528B. While the astable multivibrator is running, memory address registers U255, U258, U265, and U465E—F are loaded with whatever data is present on the ECLD0—ECLD7(H) bus.

Memory Address

The memory address registers control the address where data in the acquisition memory is read or written.

The output of even memory address register (EMAR) U258 and U255 is used to address the even acquisition memory. The output from the EMAR is also clocked into odd memory address register (OMAR) U261 and U255C and D by the ODD CLK(H) (the complement of EVEN CLK(H)). The OMAR output is used to address the odd acquisition memory. The OMAR output can also be read back by the Controller board through comparators and a tri-state buffer (these are seen on schematic 26).

The initial value in the EMAR is loaded by the memory read and load circuitry, discussed previously.

The most significant bit of the OMAR (pin 7 of U465) clocks MAR overflow register U655B. The CLR TRIG ECL(H) signal sets register U655B, so it initially has a high output. If the register gets clocked, the output goes low and does not change with future clock inputs.

The msb from the OMAR has a falling edge when the OMAR has incremented past 256 decimal. MAR OVERFLOW(H) from register U655B is then used by the Controller as an indication that all the addresses in the acquisition memory have valid data written in them.

Qualifier Logic

PRB QUAL HI/LO determines the active state of QUALIFIER(H) by either setting register U518A or resetting U518B. The active state of INH PRB QUAL(H) disables QUALIFIER(H) entirely by causing both registers U518A and B to always write low signals.

QUALIFIER(H) is applied to the inputs of registers U581A and B, and possibly gets clocked through. When QUALIFIER(H) is at the selected state, the enabled register clocks out a high. This stops register U528B from transmitting the EVEN CLK(H) and ODD CLK(H) signals (through exclusive-OR U525C). The 91A08 QUAL BUS(L) signal can also stop the even and odd clocks in the same way. The even and odd clocks drive the acquisition memory, so stopping them stops data acquisition.

Even-Odd Clock Generator

Register U528B is a divide by two. It drives the EVEN CLK(H) and ODD CLK(H) signals alternately at half the speed of CLK B(H). These clocks allow data to be written to the two acquisition memory sides alternately.

Even Write-Enable Generator

Data must be clocked into the even acquisition memory at the same rate it is clocked out of the even register. However, because of propagation delays and set up times, the same clock cannot be used for both purposes. The even write-enable generator generates a new clock from EVEN CLK(H) to be used by the even acquisition memory. The output of the write-enable generator has two special characteristics: its rising edge is delayed for a specified time after the rising edge of the EVEN CLK(H), and the pulse is high for a specified period of time independent of EVEN CLK(H). Figure 4-34 shows a timing diagram for one cycle of the write-enable generator.

If the data from inverting-input OR gate U551C is low and register U561A is being clocked, the register and two comparators works as a single-shot multivibrator. Keep in mind that ECL logic can source current but cannot sink it, and the inputs are high impedance.

The EVEN WE(L) signal is generated whenever a low is clocked into the D input of U561A. The Q(H) output then goes low. Previously, the Q(H) output was high, which charged up C656. When the Q(H) output goes low, C656 starts to discharge through R661, which controls the pulse delay. When C656 discharges to V_{bb}, comparator U558A has a rising edge on its inverting output. This edge does three things: it charges C657 high; it is inverted by U558C to provide a low output on EVEN WE(L); and it is written, through U558C, to the set pin of register U561A.

A set-active signal forces the Q(H) output of U561A high, which charges C656 high and is inverted by U558A. The low output from U558A causes C671 to discharge through R658, which determines the pulse width. After C658 discharges to V_{bb}, U558C puts a high on its inverting output.

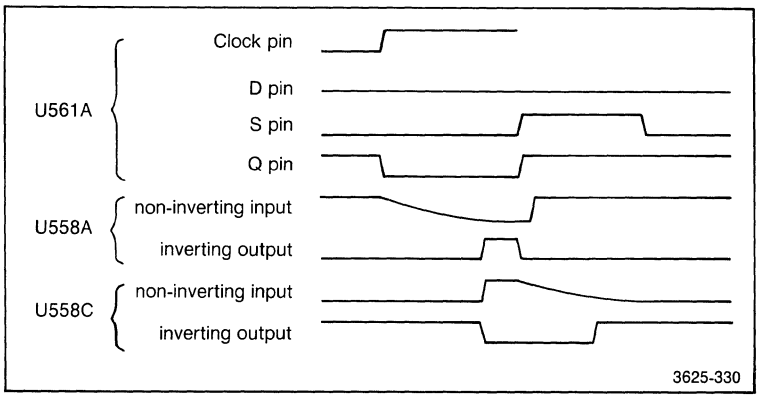


Figure 4-34. 91A08 even write-enable timing diagram.

This ends the EVEN WE(L) pulse, and writes a low to the set pin of U561A, so the next clock pulse can be excepted. Refer to Figure 4-34 for a timing diagram of the generation of a WE(L) pulse.

If ENABLE LOAD(H) is active and neither MEM RD(L) nor MEM LD(L) is active, a high is written out of AND gate U455C. This high line disables the clock on register U561A. Otherwise, register U561A is clocked by EVEN CLK(H). If either MAR LD(L) or INH WR EN(H) are active, inverting-input OR gate U551C will output a high and the write-enable generators will be disabled.

Odd Write-Enable Generator

The odd write-enable generator provides write-enable pulses for the odd acquisition memory. The odd write-enable generator is functionally identical to the even write-enable generator. Refer to the even write-enable generator circuit description for more information.

91A08 CLOCKS AND DIFFERENCE COUNTER 

Clock Select Control Register

This register selects the clock used to clock the 91A08 module, and the clock used by the difference counter. The register is loaded with data from the TTLD0—TTLD7 bus by the 91A08 controller interface.

100 MHz Clock Probe Receiver

Signals from the 100 MHz Clock Probe enter the 91A08 module through J300 and are passed through an adjustable delay line. This delay line is a coax cable that is connected between J302 and J705. The length of the coax is adjusted so the acquired data has the proper setup time before being clocked in. U701, Q601, and Q602 then adjust the threshold of the single-ended signal from the clock probe, and convert it to differential ECL.

Clock Selectors

The clock selector circuits select the clock to be used for acquiring data, and select the triggering functions in the 91A08. CLKSEL0(H), CLKSEL1(H), and CLKSEL2(H) are coded in octal to enable the appropriate clock. See Table 4-25 for a code listing. These signals are decoded by U605 which then passes the selected clock.

Table 4-25
91A08 Clock Selection Code

Octal Code	Selected Clock	Octal Code	Selected Clock
1	91A32 INTL CLK(L)	4	91A08 INTL CLK(L)
2	CKL1(H)	5	PRB CLK(L)
3	CKL1(L)	6	PRB CLK(H)

If there are both 91A32 and 91A08 type modules in the same DAS configuration, they may be made to trigger at different times. The difference counter counts how many clock cycles there are between the two trigger times. The time difference is measured in terms of the clock that drives the master 91A32 module(s) (either the 91A32 internal clock or either edge of external CKL1). The 91A32 INTL CLK SEL(L), SEL CLK1 NOT(L), and SEL CLK1(L) signals control which clock is used for the difference counter. The selected clock then passes through one of the inverting-input NAND gates in U435.

Start-Up Circuit

The selected clock has a three cycle wait/start up control circuit consisting of AND gate U455B and three registers, U441B, U415C, and U415D. All three registers are held set by AND gate U455B until the START ACQ(H) signal goes high, or the PUT 91A08 TRIG ON EVENT 1(L) signal goes low. The three registers then start clocking through the inverted (by U541B) START ACQ(H) signal.

When START ACQ(H) goes high, these registers start clocking through a low. When the low is clocked out of the last register (U415D), the low enables the NOR gates in U615, which then transmit the selected clock.

91A08 Clock Drivers

The selected clock is sent to the rest of the 91A08 module through the gates in U615 and U511.

Start Delay Flip-Flop

Start delay flip-flop (U415A) prevents data acquisition for one clock cycle after the clocks are enabled. This syncs the 91A08 module to the 91A32 modules, and prevents an off-by-one error by the MAR overflow flip-flop (U655B on schematic 29).

Before the 91A08 clock starts to run, the CLR TRIG ECL(H) line sets U415A so the Q(H) output is high. When the first clock comes out of U511, it clocks a low out of U415A so the 91A08 can start acquiring data. The start delay flip-flop can be over-ridden by the 91A32 ECL QUAL EN(H) signal, because the 91A32 QUAL bus will then give the 91A08 the proper starting time.

Difference Counter

If there are both 91A32 and 91A08 modules in the same DAS configuration, they may be made to trigger at different times. The difference counter counts how many clock cycles there are between the two trigger times. The time difference is measured in terms of the clock that drives the master 91A32 module(s) (either the 91A32 internal clock or either edge of external CLK1). The selected clock comes from one of the inverting-input NAND gates in U435 and is translated to TTL by Q644 and Q645, which drive counter U588.

The counter is enabled through OR gate U431B, which is inverted and translated to TTL by Q571 and Q572. The 91A32 TRIG 0(L) and the 91A08 TRIGRD(H) signals are inputs to the OR gate. Before the difference counter starts, the 91A32 TRIG 0(L) signal is high, which prevents the counter from starting. After the 91A32 modules finish the trigger sequence, the 91A32 TRIG 0(L) line goes low and the difference counter starts. When the 91A08 module finishes its trigger

sequence, 91A08 TRIGRD(H) goes high. This stops the difference counter through the ENP pin of U588. Also, if the most significant bit of counter U595A goes high (the difference counter hits 8000 hexadecimal), the counter is stopped by inverter U185D.

The state of the counters can be read on the data bus through buffers U688 and U691.

Miscellaneous Input

The miscellaneous data stored in the 91A08 acquisition memory is used to decode how data acquired by the 91A08 corresponds to data acquired by 91A32 modules. This information is used particularly when the DAS is in 91A32 ARMS 91A08 mode. 91A32 QUAL(H) is clocked through register U445B to be stored in the acquisition memory.

The clock used by the master 91A32 module (91A32 internal clock, CLK1 rising edge, or CLK1 falling edge) is also stored in the 91A08 acquisition memory so 91A08 data can be synchronized with 91A32 data when the boards are running at different rates.

91A08 TRIGGER 

Trigger Control Register

This register selects the triggering mode of the 91A08 module. The register is loaded with data from the TTLD0—TTLD7 bus by the 91A08 controller interface.

91A08 Trigger

The word recognition (WR0(L) and WR1(L)) and glitch recognition (GR0(H) and GR1(H)) signals come from the glitch and word recognizers section of schematic 27. These signals are pipelined for one clock pulse by registers U425A and U421A, and then the similar lines are wire-ORed before being delayed one or more clock pulses by register U528A and C.

The resultant glitch trigger signal from U528A is placed on the 91A08 GLITCH BUS(H). If DELAYED QUAL(L) is low, the glitch trigger signal will be inverted by NOR gate U625F; otherwise, the glitch trigger signal is masked out. The output of U625F is passed to the input of U625A where it may be masked out by either EN GLITCH OR(L) or DELAYED QUAL(L). If the glitch trigger signal makes it this far, it is wire-ORed with the word recognizer signal from U625C and passed on to register U521B.

The outputs of U625A and C go to the D input of register U521B. If this register is allowed to clock through the signal (controlled by the arm 91A08 trigger section and the pipelined internal timing sequencer), it outputs the 91A08 TRIGRD(H) signal. If a low (active) signal is clocked out of the Q(L) output of register U521B, inverter U525A re-inverts the signal and places it on the D input. This latches-up the register so it stays triggered until it is reset.

Table 4-26 shows how the triggering control lines are set for the different triggering modes.

Table 4-26
91A08 Triggering Modes

Mode	EN GLITCH OR(L)	IGNORE GLITCHES
Glitches Off	L	H
Glitches On	L	L

Arm Trigger

The arm trigger circuits determine whether a trigger signal can pass through U521B and whether the 91A08 trigger is used by the Trigger/Time Base. The circuit is controlled by ARM 91A08 TRIG(L), ARM 91AO8 ON 91A32 TRIG(H), and 91A32 TRIG 0(H). Table 4-27 shows how the arming control signals are set for various arming modes.

Table 4-27
91A08 Arming Modes

Mode	ARM 91A08 TRIG(L)	PUT 91A08 TRIG ON EVENT 1(L)	ARM 91A08 ON 91A32 TRIG(H)
91A32 ONLY	H	L	H
91A32 AND 91A08	L	H	L
91A32 ARMS 91A08	L	L	L
91A08 ONLY	L	L	L

The ARM 91A08 TRIG(L) and ARM 91A08 ON 91A32 TRIG(H) signals control whether register U521B is held reset, or may not be reset, or is held reset until 91A32 TRIG 0(H) goes high. This is done through gates U431C and D, U438B and C, and U451C and E.

Put 91A08 Trigger on Event 1

The word recognizer signal from U528C is placed on the 91A08 DATA WR BUS(H) where it will be clocked through U251A unless the PUT 91A08 TRIG ON EVENT 1(L) signal holds the register reset. The output of the register is then put on the EVENT 1(H) bus of the Interconnect to be used by the Trigger/Time Base board.

Pipelined Internal Timing Sequencer

This section of circuitry controls the qualifier lines to various parts of the 91A08 and creates DELAYED QUAL(L). The pipeline is necessary because the qualifier and word recognition signals caused by acquired data and glitches are not processed on the same clock cycles.

Refer to Figure 4-35, which shows how the pipelined internal timing sequencer relates to the rest of the 91A08 module.

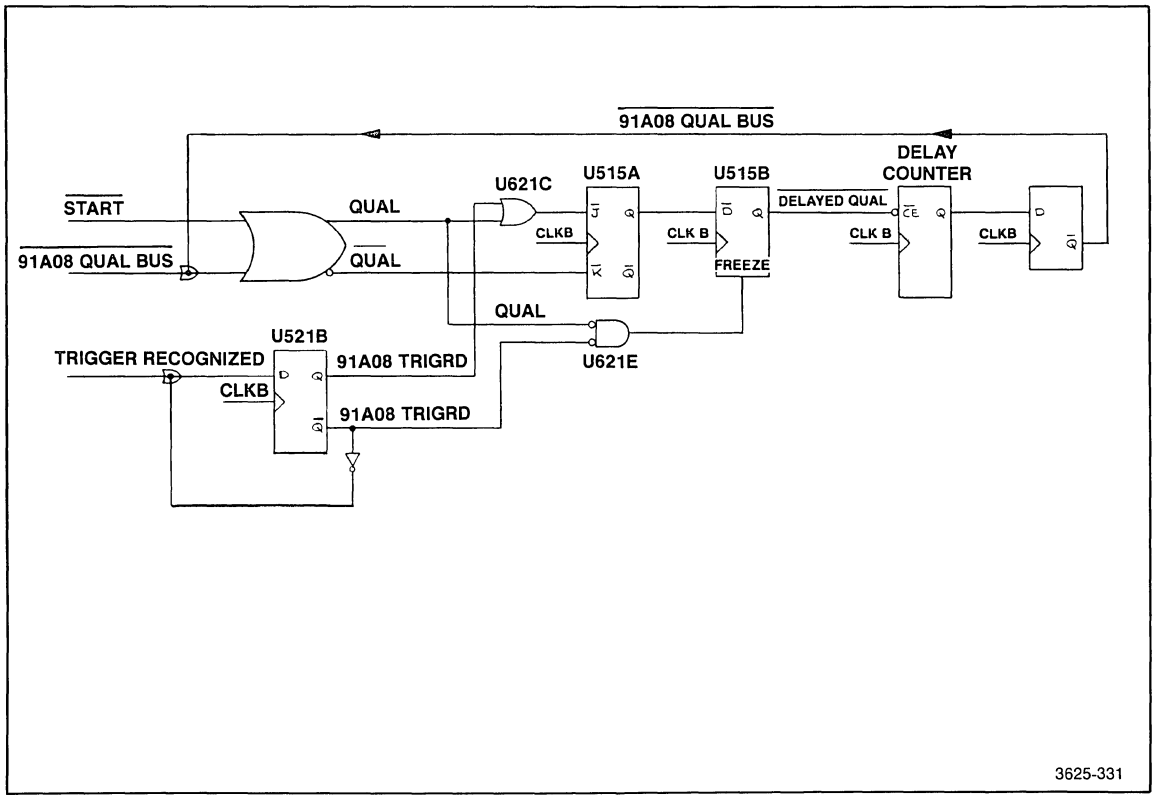


Figure 4-35. Simplified trigger shutdown circuit diagram.

The pipelined internal timing sequencer is initiated at start-up time as shown in Figure 4-36. The presetting of the pipeline is done by the CLR TRIG ECL(H) line.

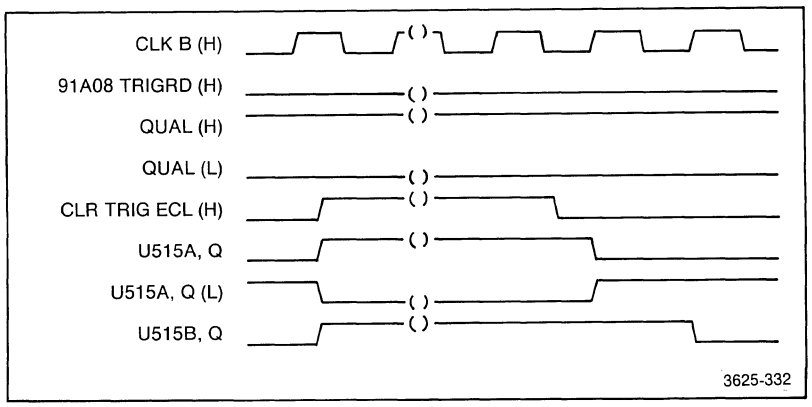


Figure 4-36. Initiating the pipelined internal timing sequencer.

If the qualifier goes low (stops storage) before the trigger occurs, the pipeline performs the actions diagramed in Figure 4-37. This causes the DELAYED QUAL(L) line to go high two clock cycles after the qualifier signal goes low. When the qualifier line returns high, the DELAYED QUAL(L) signal returns low after one clock cycle.

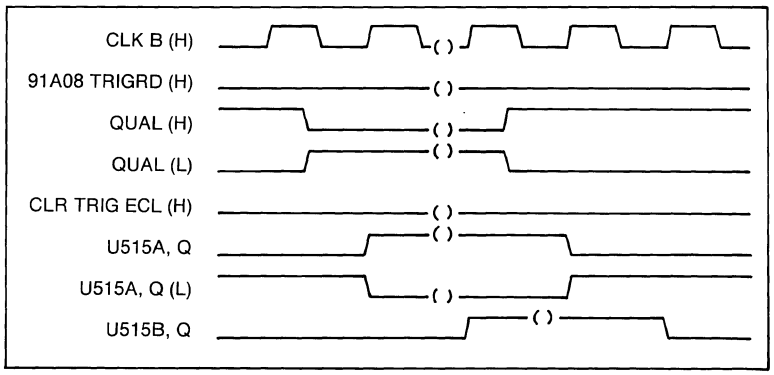


Figure 4-37. Qualifying before triggering the pipelined internal timing sequencer.

After trigger conditions have been fulfilled, the 91A08 TRIGRD(H) and 91A08 TRIGRD(L) signals go active. If QUAL(H) and QUAL(L) are active, the output of the pipeline does not change from its previous output. The inputs to OR gate U621C and inverting- input AND gate U621E change, but the outputs do not change.

After the trigger occurs, if QUAL(H) goes low, both the J(L) and the K(L) inputs to both registers in the pipeline go high. This is caused by the gates in front of the inputs to the registers. Writing high to both the J(L) and K(L) inputs of a register locks up the register so it will continue to output the previously logged-in data. This action prevents the low condition of QUAL(H) from passing through the pipeline and changing the DELAYED QUAL(L) state.

Lower 1/4 Delay Counter

The delay counter allows the 91A08 to delay the time when acquisition is stopped by a preset number of clock periods. The delay counter is divided into two portions, the lower 1/4 and the top 3/4, because the lower section must operate faster than the top part. The lower 1/4 is therefore designed with ECL, while the top portion is TTL.

The lower 1/4 of the counter, U428, is loaded with a delay value by the 91A08 controller interface. When the EN LD DELAY 0(H) is high, U428 is loaded with the lowest four bits on the ECLD0—ECLD7 bus.

Once loaded, the counter increments once with every rising edge from CLK B(H) unless it is disabled through pin 6. The counter is disabled by the 91A08 TRIGRD(L) signal OR the QUAL(L) signal OR the DELAYED QUAL(L) signal. This means the counter cannot increment until the 91A08 has triggered, and then it cannot increment unless the data being acquired is qualified.

The Q3(H) output of the lower 1/4 counter clocks the UP(H) line of the top 3/4 of the delay counter.

The end of the delay count is also detected in this circuit block. When the top 3/4 of the delay counter outputs all high values, a high is written to inverter U541C. The low out of U541C is translated to ECL levels and ORed with QUAL(L) by U431A. The output of U431A is wire-ORed with the terminal count pin of U428 and set to the D input of register U518B. So when the count is not yet completed, register U518B clocks through high values. When the terminal count is reached, the D input of register U518B drops low, clocking through a low, causing the 91A08 STOP STORE(L) signal to go active. Simultaneously, U518B pulls up on the 91A08 QUAL BUS(L) line so all 91A08 modules in the system are stopped from acquiring data.

Top 3/4 Delay Counter

The delay counter allows the 91A08 to delay the time when acquisition is stopped by a preset number of clock periods. The delay counter is divided into two portions, the lower 1/4 and the top 3/4, because the lower section must operate faster than the top part. The top 3/4 is therefore designed with TTL, while the lower 1/4 is designed with ECL.

The top 3/4 of the delay counter (U155, U145, and U151) is loaded with a delay value by the 91A08 Controller interface. When DELAY 0(L) is active, U155 is loaded with the highest four bits on the TTLD0—TTLD7 bus. When DELAY 1(L) is active, U145 and U151 are loaded with the value on the TTLD0—TTLD7 bus.

The Q3 output of U428 supplies the up count clock for the top 3/4 delay counter. The signal from U428 is converted from ECL to TTL by transistors Q151 and Q152.

The outputs of the top 3/4 delay counter pass through open collector buffers. The outputs of these buffers are wire-ANDed and sent back to the lower 1/4 delay counter, where the end of the delay count is detected.

PATTERN GENERATION DETAILED CIRCUIT DESCRIPTIONS

P6455 TTL/MOS PATTERN GENERATOR PROBE

The pattern generator probe uses data from a pattern generator or a pattern generator expander to create 8 bits of data, a clock, and a strobe that can be used to stimulate external circuits. The probe output has variable high and low levels and can also go to a high impedance state. See the detailed circuit description following the descriptions of the instrument modules for more details.

91P16 PATTERN GENERATOR

The 91P16 Pattern Generator can stimulate sixteen different logic lines at rates up to 25 MHz. Patterns are specified by means of a special purpose programming code and can contain a non-repeating pattern of 256 words, or repeating patterns of much greater duration. For an overview of the circuits in the pattern generator, refer to the 91P16 Pattern Generator in the General System Description.

This description is divided into several sections. The section divisions are by schematic and then by functional blocks on the schematic. Numbers in diamonds refer to the numbers on schematics tabs in the Diagrams section. Refer to those schematics while reading the circuit descriptions. All of the component numbers in the 91P16 module's circuit description are assumed to have an A14 preface unless otherwise noted.

91P16 CONTROLLER INTERFACE 

Controller Interface

The 91P16 controller interface takes data from the Controller board and sends it to appropriate registers and RAMs by decoding the lowest 4 bits on the address bus and interpreting BWR(L), PORT(L), and BRD(L) from the Controller board. The interface also takes data from the module and writes it on the data bus at the command of the Controller board.

For example, suppose the Controller board is reading the pod IDs.The address bus has 1 octal written on the least significant three bits. Simultaneously the BRD(L) and PORT(L) signals go active. This action enables decoder U495, which decodes the address so pin 14 goes active (low). The pod status register, U661, is then enabled and puts data on the data bus. The writing procedure is similar, except the BWR(L) and PORT(L) signals must go active to enable U685. Table 4-28 shows which registers are connected to the data bus by each hexadecimal address and the BWR(L), BRD(L), and PORT(L) lines.

Table 4-28
91P16 — Controller Interface Map

Hex Addr	BWR	BRD	PORT	Line Name	ICs Affected U#	Schem#
XXX1	X	L	L	POD READ(L)	U661	32
XXX2	L	X	L	CNTL 0(L)	U585	32
XXX3	L	X	L	CNTL 1(L)	U581	32
XXX4	X	L	L	VCTR MEM RD(L)	U371	32
XXX4	L	X	L	STB LD(L)	U153 & U165	33
XXX5	L	X	L	μC 0(L)	U435 & U441	33
XXX6	L	X	L	μC 1(L)	U427 & U431	33
XXX7	L	X	L	VCTR 0(L)	U421 & U425	36
XXX8	L	X	L	VCTR 1(L)	U521 & U525	36
XXX9	L	X	L	SINGLE STEP(L)	U617	35
XXXA	L	X	L	VCTR PC LD(L)	U367 & U471	34
XXXB	L	X	L	μC PC LD(L)	U445 & U541	33
XXXC	L	X	L	IR LD 0(L)	U365C	35
XXXD	L	X	L	STACK LD(L)	U145 & U151	35

The 91P16 controller interface also holds ROM U481, which contains menus, instructions for programing the 91P16 and 91P32 modules, and a record of the read back data at each address. This ROM is selected to be read when the BRD(L), PERSONALITY(L), and SEL SLOT(L) signals are all active. The ROM's data is then put on the data bus through buffer U485 when addressed by BA0-BA12 (the address bus lines).

The resistor packs, R595, R571, R695, and R597 are TTL-to-ECL converters.

2 A Current Source

The 2 A current source converts 1 A at +12 V to 2 A at +5 V. This is needed because the 91P16 module draws more current from the +5 V supplies in the mainframe than they can supply.

The current from the +12 V supply that is converted to +5 V passes through fuse F696. If the fuse blows, the voltage drop across the fuse will turn on LED DS198 as a warning light. The current drain from the supply is isolated from the +12 V supply by LC network L695 and C498.

Q398 is the power transistor that switches pulses of +12 V current into inductor L494. Switching is controlled by current-sensing comparator U198A through transistors Q196 and Q197.

Comparator U198A monitors for 2 A through R394 (a voltage drop of 0.2 V). When the comparator senses that less than 2 A is flowing through R394, it outputs a high voltage. This high voltage turns on switch transistors Q196, Q197, and Q398. The switch loads current into inductor L494. The reactance of L494 stores the initial turn-on current and integrates the voltage pulse from the +12 V supply. After the initial turn-on of the switch, L494 starts passing more current until finally 2 A are flowing through R394. The current is sensed by the comparator, which turns off the switch.

When the switch transistor Q398 is turned off, the current stored in inductor L494 is discharged through R394. When the current coming from the inductor drops below 2 A, the comparator turns on again, repeating the cycle.

The current through R394 follows a triangle wave. Notice that inductor L494, by integrating the current, provides the hysteresis needed by the circuit. LC network L294 and C382 flatten out the 2 A supply further.

The circuit has no voltage regulation. The load provided by the 91P16 for the 2 A current source guarantees that more than 2 A is needed to maintain the +5 V supply at +5 V. The remainder of the necessary current is provided by the +5 V Power Supplies in the mainframe, which regulate the voltage.

91P16 μCODE MEMORY AND STROBES 

μCode Memory

The μCode memory, U427, U431, U435, and U441, is where the μCode is loaded into memory and then recalled for decoding into instructions. The μCode is stored in a 13 x 256 bit format. The memory is loaded from the data bus into two different sets of RAM, the first eight bits by μC0(L) and the last five bits by μC1(L). The address being loaded is set by registers U445 and U541.

While the pattern generator is running, registers U541 and U445 are loaded with 00; so the μCode memory is addressed through ECL program counter bus ECLP0—ECLP7(H) which comes from the instruction multiplexer (schematic 34). The data in the μCode memory then goes to the instruction register. Table 4-29 shows how the μCode is decoded. (In Table 4-29 stb = strobe, sel = select, and int = interrupt.)

For the COUNT, REPEAT, and HOLD instructions, the lowest three bits of the GOTO FIELD(H) specify an address in the clock control RAM (see the clock control RAM circuit description).

If the Cntl Field contains 11 binary, the GOTO FIELD(H) is ignored. If the Cntl Field contains 01 or 10 binary, the value in the GOTO FIELD(H) is used as the new position for the program counter.

Instruction Register

The data in the μCode memory goes to registers U451, U453, and U467A. All these registers are clocked by the IR CLK(H) and write their data to the appropriate circuits for decoding.

Table 4-29
Pattern Generator μCode Decoding

bit 12	11	10	9	8	7	6	5	4	3	2	1	bit 0
1	0	tri-	stb	stb	7	6	5	4	3	2	1	0
Cntl Field		state	1 sel	0 sel	GOTO FIELD							

Bits 12 and 11 — The Cntl Field, C0(H) and C1(H), regulate what action is performed by the pattern generator. The decoding is as follows:

00 — ADVANCE, COUNT, REPEAT, HOLD, or HALT (determined by the contents of the GOTO FIELD).

01 — GOTO
10 — CALL
The GOTO FIELD(H) contains the the value that the program counter is adjusted to.

11 — RETURN adjusts the program counter to the value at the top of the stack.

Bit 10 — The INT TRI ST(H) bit goes high to indicate that all of the pattern generator's probe outputs should present a high impedance to the circuit being stimulated.

Bit 9 — The STB1 SEL(L) bit signals the pattern generator that strobe 1 should start.

Bit 8 — The STB0 SEL(L) bit signals the pattern generator that strobe 0 should start.

Bits 7 through 0 — The GOTO FIELD(H) is decoded according to the contents of the Cntl Field, C0(H) and C1(H). If the Cntl Field is 00 the GOTO FIELD is decoded as follows.

GOTO FIELD Bits								Instruction
7	6	5	4	3	2	1	0	
0	X	0	0	0	X	X	X	ADVANCE
0	X	0	0	1	X	X	X	COUNT
0	X	0	1	0	X	X	X	REPEAT
0	X	1	0	0	0	0	0	HOLD
1	X	0	0	0	0	0	0	HALT

Strobe Control

The strobe control registers turn the strobe clock on and off, control which strobe is enabled, and prevent the strobes from being interrupted in the middle of their cycles.

The STB1 SEL(L) and the STB0 SEL(L) signals are clocked through registers U285A and B, respectively. If either of these signals goes active (low), the corresponding register clocks out a low from its Q(H) output and a high from its Q(L) output. The low from the Q(H) output un-asserts the reset on the end-detect register (either U267A or U265A). This allows the selected strobe to pass through the register and prevents the un-selected strobe from getting through.

The high from the Q(L) output of one of the strobe control registers does the following things:

- masks the STB T0(H) signal from clocking either of the strobe control registers, effectively latching up the registers.
- starts the strobe clock circuit.

The strobe control remains in this state until the end of the strobe is detected. The end of strobe detector sets the corresponding strobe control register, which reverses the state of its outputs. This stops the strobe clock circuit and allows STB T0(H) entry into the strobe control registers. The registers are now ready to receive another strobe signal.

Strobe Clock

The strobe clock drives both strobes. The clock is turned on by either of the Q(L) outputs of the strobe control registers, U285A and B. When a strobe is selected, one of the Q(L) outputs of registers U285A and B presents a high to the D input of register U281B and to pins 4 and 13 of U185.

The high to all these inputs causes the following events:

- OR gate U185A (output pin 2) outputs a high that causes the strobe counter to go into the count mode.
- the output of NOR gate U185C (output pin 14) goes low, allowing OR/NOR U185B to start oscillating.
- U281B clocks through a high with the first rising edge from U185B.

The period of oscillation of U185B is determined by the amount of time necessary to charge and discharge capacitors C196 and C197 through R193. As soon as the oscillation starts, the high at the D input of U281B gets clocked through. As long as one of the strobe control registers outputs a high on its Q(L) pin, the clock will continue to oscillate.

The strobe clock is shut down by the end-detect circuitry. When the active strobe has an end-detect, the corresponding strobe control register, U285A or B, is set. Setting the register causes the Q(H) output to go high and the Q(L) output to go low. This causes register U281B to have a low logged in at the next falling edge of the strobe clock.

Once the data is logged in, the outputs of register U281B stop the clock (through NOR gate U185C) and load the strobe counter with all zeros (through OR gate U185A). The clock now waits to be reactivated by a strobe-select signal.

Strobe Counter

The strobe counter addresses both strobe RAMs in an incrementing fashion whenever a strobe is running. The counter is initially loaded with all zeros. This value is output on the Q0(H) through Q3(H) pins of all three counters, U167, U171, and U175. When started by OR gate U185A, the counters increment in sync with the strobe clock. The output of the counters then addresses the strobe RAM, U153, and U165.

Strobe RAM

The strobe RAM is programmed before run time by the Controller board. While programming, the counters are advanced in a single-step fashion by the STB LD(L) and the STB LDEN(H) through AND gate U271C. After each counter advance, values are loaded into the strobe RAMs from D0(H) and D1(H) of the pattern generator data bus, D0-D7.

When the pattern generator is running, the strobe counter addresses both RAMs simultaneously, incrementing every 40 ns. The RAMs are loaded with zeros for the strobe delay period, and then with ones for the active period of the strobe. Both strobe RAMs output the strobe data even when only one strobe has been selected. The data from the strobe RAMs is also used by the end-detect and polarity-select circuits.

End-Detect and Polarity Select

There are two identical end-detect and demultiplexer circuits: one for strobe 0 and one for strobe 1. Since the circuits are identical, only the circuit for strobe 0 is described.

The data from strobe RAM U153 is written to register U267A. If the strobe is not selected, U267A is held reset by strobe control register U285B, so the strobe data does not pass through. If strobe 0 is selected, the data is clocked through register U267A at 40 ns intervals. The data from U267A is then clocked through U267B into exclusive-OR gate U261A. This gate makes the strobe low active if STB0 POL(H) is high, otherwise leaving the strobe high active.

AND gate U271A detects the end of the strobe by going high when both U267A's Q(L) and U267B's Q(H) outputs are high. This only occurs when the RAM output data makes a transition from high to low. The high from AND gate U271A sets strobe control register U285B to stop the clock and set the strobe counter back to all zeros.

91P16 STACK AND INSTRUCTION MULTIPLEXER 

Call Stack

The call stack stores the program counter + 1 (PC + 1) value any time a CALL instruction is encountered. If a RETURN instruction is encountered, the value at the top of the call stack is put on the program counter. The call stack then decrements and puts the next-most-recently-loaded value at the top of the stack. The call stack can store 16 different PC + 1 values in a push-pop format.

First, μCode bits MC11(H) and MC12(H) and the INT(H) signal must be decoded by OR gates U465B and C, inverter U461C, and NOR gate U461D. The results of the decoding are shown in Table 4-30.

Table 4-30
Stack μCode Decoding

INSTRUCTION	INT	MC12	MC11	S2	S1	U353's Action
ADVANCE	0	0	0	1	1	Hold
GO TO	0	0	1	1	1	Hold
CALL	0	1	0	1	0	Increment
RETURN	0	1	1	0	1	Decrement
ADVANCE	1	0	0	1	0	Increment
GO TO	1	0	1	0	1	Decrement
CALL	1	1	0	1	0	Increment
RETURN	1	1	1	0	1	Decrement

The write-enable pulses generated by register U565B and its associated circuitry make allowances for setup and hold times of the RAM. Pulses are generated whenever counter U353 increments; that is, whenever S1 is low. The time constant of R663 and C562 determines the total length of the write-enable sequence. R360 and C362 control how long after the write-enable sequence begins the write-enable line goes active (low).

RAMs U251 and U351 are identically addressed to provide 16 x 8 bits of storage. The RAM's outputs are buffered and synchronized by registers U345 and U245. The data through the registers is sent to the instruction multiplexer to be used when returning from sub-routines.

Interrupt Logic

The interrupt logic accepts the PG EXT INT(H) signal, clocks it through a register, and applies conditioning logic.

Before an interrupt can be received, register U131A must be set. Also, the interrupt may only occur during an ADVANCE, COUNT, REPEAT, or HOLD instruction. The interrupt(L) signal from Q(L) of register U131B is wire ORed with the two Cntl Field bits, MC11(H) and MC12(H). If the Cntl Field bits and the interrupt(L) signals are all low, the INT(H) signal goes high.

The INT(H) signal is clocked through register U535 and sets flip-flop U131A, which on the next rising edge from the clock passes through U131B and turns off the INT(H) signal. Each INT(H) signal lasts for two clock periods.

Advance Generator

The value on the program counter bus, EPC0—EPC7, is incremented by one by AND gates U545 and U551, and exclusive OR gates U645 and U651. The output of these gates is clocked through registers U367 and U471. The register's output, ADV0—ADV7, is used by the ADVANCE instruction to increase the program counter value by one.

Instruction Multiplexer

The instruction multiplexer controls the program counter value, EPC0—EPC7, by selecting the ADV0—ADV7 bus (ADVANCE), the GOTO0—GOTO7 bus (GOTO and CALL), or the R0—R7(H)

bus (RETURN). The data selection is regulated by the Cntl Field, MC11(H) and MC12(H), as shown in Table 4-31. Each of the four data selectors, U337, U335, U331, and U327, selects data for two of the bits in the program counter.

Table 4-31
Instruction Multiplexer Decoding

CNTL FIELD		Selected Data
MC11 C0	MC12 C1	
0	0	ADVANCE (ADV0 — 7)
1	0	GOTO (GOTO FIELD)
0	1	CALL (GOTO FIELD)
1	1	RETURN (RETURN ADDRESS BUS)

The program count, EPC0—EPC7, is then sent to address the μCode memory and is also clocked through the program counter buffer.

Program Counter Buffer

The program counter, EPC0—EPC7, is clocked through the program counter buffer, U535 and U531. The data from these registers is sent on the PC0—PC7 bus to the vector memory. The output of the registers is also buffered and sent through the Interconnect board on the PC0—PC7 bus to any 91P32 Pattern Generator Expanders in the DAS.

91P16 TIMING CIRCUITS 

Clock Selector

The CLK CONT(H) bus goes from the 91P16 controller interface to data selector U617. The clock choices are 91A32 INTL CLK(L), 91A08 INTL CLK(L), PG EXT CLK(L), and SINGLE STEP(L). The Z output pin of data selector U617 is buffered by NOR gates U115B,C,D and used for on board clocking. The W output pin is buffered by NOR gate U121B and used to clock 91P32 Pattern Generator Expander modules.

μCode Clock Decoder

Gates U341B, C and D, U241C and D, and U237B and C decode Cntl Field bits C0(H) and C1(H) and bits 3-7 of the GOTO FIELD(H) to provide clock control signals. The μCode fields are decoded as shown in Table 4-32.

Table 4-32
μCODE FIELD CLOCK STOPPING LOGIC

Inputs						Outputs		
CNTL	FIELD	GOTO FIELD				HOLD	HALT	IR CLK EN
C1	C0	7	5	4	3			
1	0	X	X	X	X	0	0	1
0	1	X	X	X	X	0	0	1
1	1	X	X	X	X	0	0	1
0	0	0	0	0	1	0	0	0
0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	1	1

The HOLD(H) output of U237 pin 14 is used by the probe clock and inhibit circuitry. IR CLK EN(H), the output of U241 pin 9, is used in the clock control circuitry. The wire ORed HALT(H) outputs of U241 pin 14 and U237 pin 3, control registers U125A and B, which stop the clock line through NOR gates U121B, and U115.

When HALT(H) is low, register U125A clocks through lows on the falling edge of the selected 91P16 clock. The Q output of register U125A is clocked through register U125B on the rising edge of the selected 91P16 clock. Both registers may be reset by the μC PC EN(L) signal (μCode program counter enable).

The PG EXT PAUSE(H) signal from the Interconnect can also make HALT(H) active through buffer U237B (output pin 3). PRB CLK EN(H) can mask out the STB T0(H) and INT CLK(H) signals through NOR gates U115B and D.

Comparator U215D converts the signal out of register U125B from ECL to TTL and writes it, as HALT RD(H), to the 91P16 controller interface.

Clock Control RAM

The clock control RAM stores six different durations for COUNT, REPEAT, and HOLD instructions. When one of these instructions is programmed into the Pattern Generator menu, a field appears for specifing the number of clock periods the instruction should be executed. The one's complement of that number is loaded into RAMs U145 and U151 by the D0—D7 bus and STACK LD(L). The RAMs are addressed by the lowest three bits of the GOTO FIELD(H).

During run time, the RAMs are continually addressed by the lowest three bits of the GOTO FIELD(H). As long as the Q(L) output of register U235B (in the clock control portion of the schematic) is low, counters U137 and U141 are loaded with the contents of the RAMs, and the CO(L) signal from U141 stays low. When the Q(L) output of register U235B goes high, the counters no longer are loaded from the RAMs and increment with each clock cycle. The CO(L) signal of U141 goes high when the counters start to increment. When the counters wrap around to 00 hexadecimal, the CO(L) signal returns low. The CO(L) signal is part of the clock control circuit.

Clock Control

The clock control circuit regulates the turning on and off of clocks to the call stack, and controls the instruction register (IR CLK(H)) and the program counter (IR CLK EN(H)). The clock control circuit also controls the output latch (OUT CNTR LD(L)) and indicates whether the count register, U137 and U141, should increment or load new values.

Ordinarily, IR CLK EN(H) at U241 pin 9 is high. If either a COUNT, REPEAT, or HOLD instruction is encountered, IR CLK EN(H) goes low. As long as IR CLK EN(L) is high, the CNT REG CLK(H) can pass through AND gates U135C and U237D.

Register U235B outputs a low on its Q(L) output. The low on Q(L) holds the counters in count register U137 and U141 in the load mode so the counter's CO(L) outputs are low. The clock control circuit is stable in this condition. Figure 4-38 shows what the logic levels are in this state.

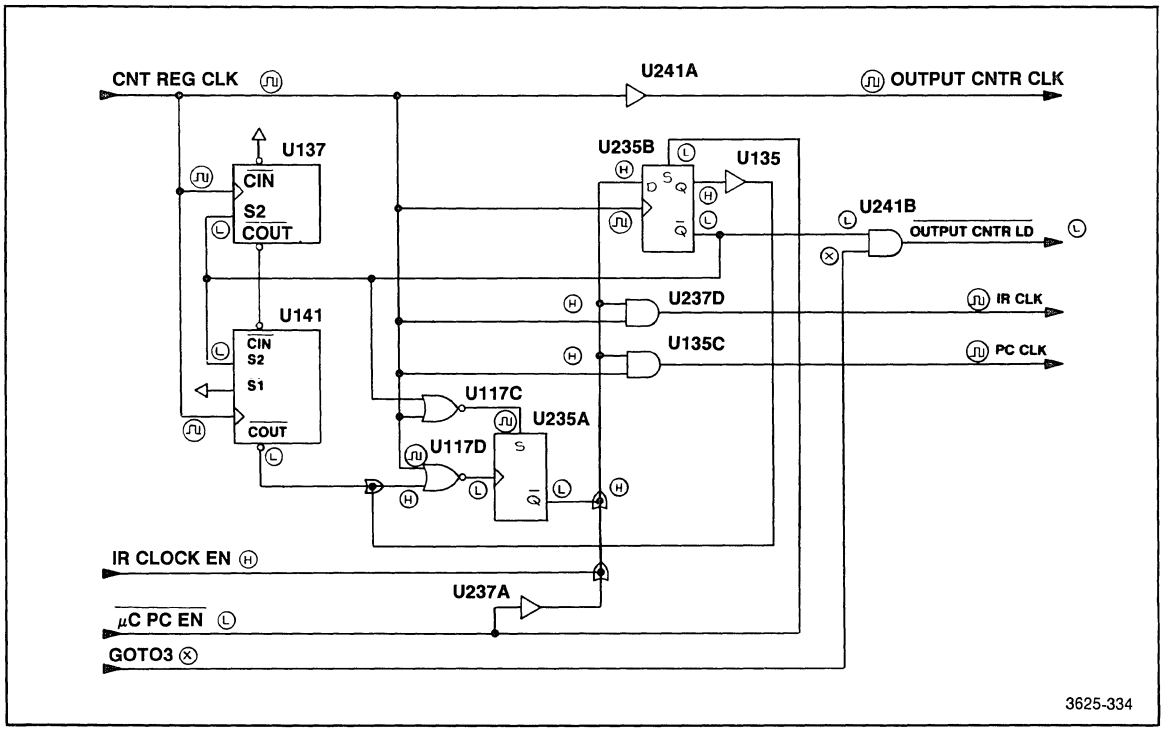


Figure 4-38. Clock control: non-count logic state.

If IR CLK EN(H) goes low, the following events occur:

- AND gates U135C and U237D stop transmitting the clock, because their formerly high inputs go low.
- The D input to register U235B goes low.

At the next rising edge from the clock, register U235B logs through a low on the Q(H) output and a high on the Q(L) output. The Q(L) output changes the inputs of counters U137 and U141 so the CO(L) pins go high. The Q(L) output of U235B also stops the clock from passing through NOR gate U177C, so register U235A is no longer set at the beginning of each clock cycle. The high on the Q(L) pin of U235B also allows the value present on the GOTO 3 line to pass through AND gate U241B.

The Q(H) output of register U235B goes low, but the clock input to register U235A remains low because of the CO(L) pin of U141. Figure 4-39 shows the status of the circuitry at this point.

The situation shown in Figure 4-39 stays stable until the counters in the count register (U137 and U141) wrap around, causing the CO(L) (or COUT(L)) pin of U141 to go low. That low causes NOR gate U117D to start transmitting the inverse of the clock to register U235A.

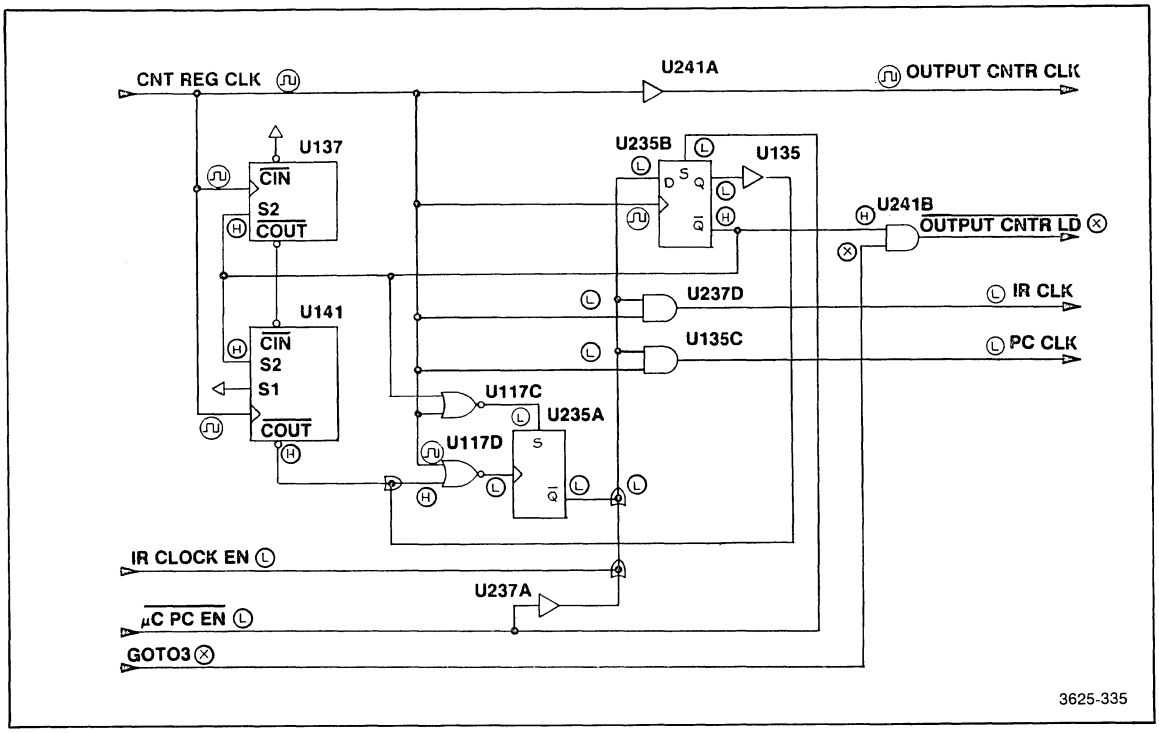


Figure 4-39. Clock control: start-count logic state.

Nothing else changes until the next falling edge from the clock. At this point a low gets clocked through register U235A, causing a high on the Q(L) output. A high on the Q(L) output of U235A lets the clock pass through AND gates U135C and U237D.

At the next rising edge from the clock, a high is logged into U235B. The high from the Q(H) output of U235B stops the clock from passing through NOR gate U177D. The low on the Q(L) pin of U235B allows the inverted clock to reach the set pin of U235A. The Q(L) pin of U235B also sets counters U137 and U141 to load data rather than increment, and forces the output of AND gate U241B low. The logic levels at this point are those shown in Figure 4-40.

The situation shown in Figure 4-40 remains until the clock falls low. When this happens, NOR gate U125D outputs a high. This sets register U235A so Q(L) goes low. When Q(L) goes low, it returns to the state it was in initially, as shown in Figure 4-38. Another low IR CLK EN(L) can be accepted at any time. Figure 4-41 is a timing diagram for the clock control circuit.

Probe Clock and Inhibit

The probe clock and inhibit section controls and buffers the clock and the tri-state signals that

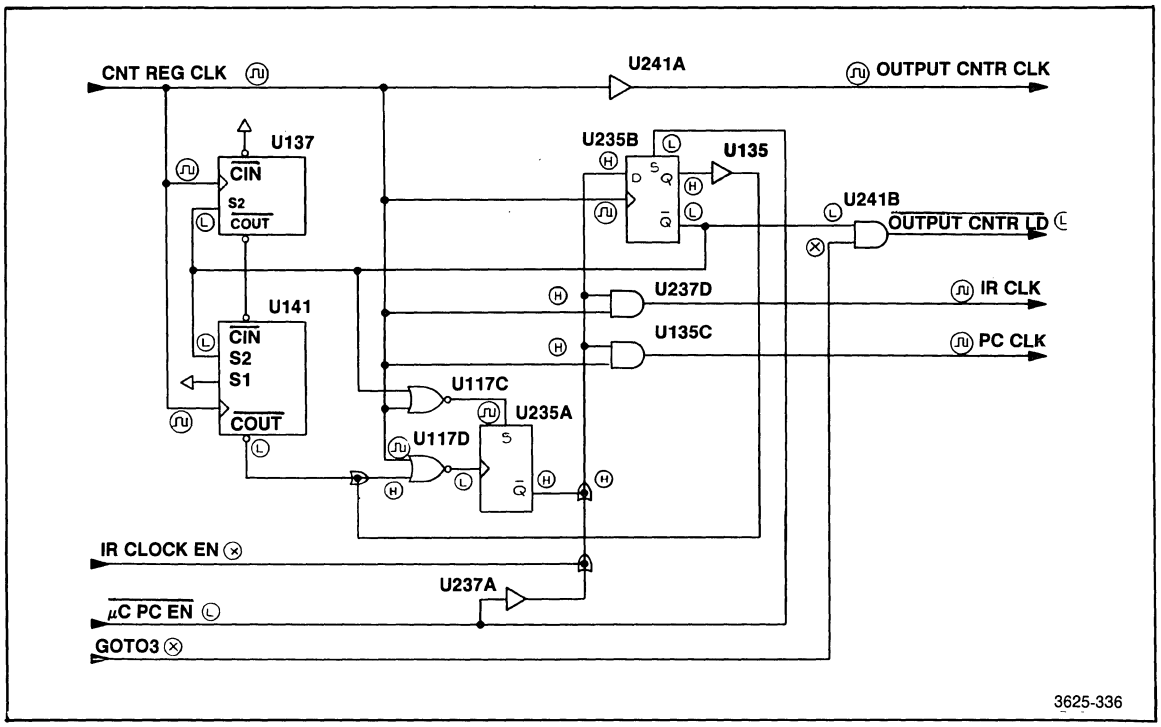


Figure 4-40. Clock control: end-count logic state.

control the probe. INT CLK(H) is usually transmitted through OR gates U110A and C. This clock may be masked out by INT HOLD(H).

The INHIBIT signal is created by the PG EXT TRI-ST(H) or INT TRI-ST(H) signals through OR gate U207A, B, and C. The level on the interrupt line can be read by the 91P16 controller interface through comparator U221A. The comparator acts as an ECL to TTL converter.

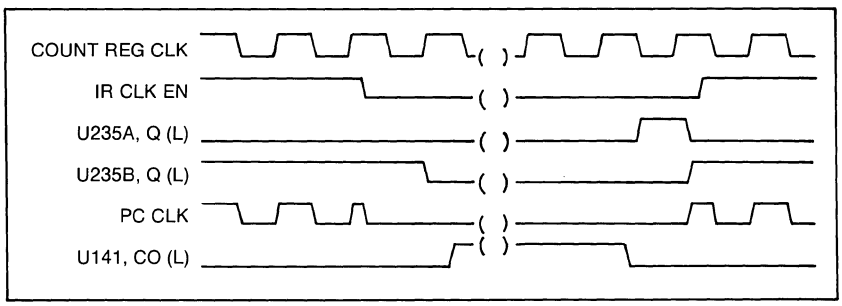


Figure 4-41. Pattern generator clock control timing diagram.

91P16 VECTOR MEMORY AND PROBE INTERFACE

Vector RAM

For each value of the program counter there is: 1) a µCode instruction, and 2) an output value. The vector memory (U421, U425, U521, and U525) is loaded with the values to be output by the

probes for each program counter value when the pattern generator is programmed. While the pattern generator is running, the vector memory is addressed by the program counter. The data from the vector memory goes to the output latches.

Output Latches

Output latches U315, U415, U515, and U615 have two functions.

- In most situations the latches act as registers, clocking through data from the vector memory. This occurs as long as pin 7 of the counters is held low; that is, while OUT CNTR LD(L) is active.

- OUT CNTR LD(L) goes high when a COUNT instruction is encountered. This causes the output latches to stop clocking-through data and start incrementing by one with each clock period. The count continues until OUT CNTR LD(L) returns low. All data out of the output latch is sent to the probe interface and readback circuits.

Probe Interface

The data from the output latches is buffered by U305, U405, U505, and U605. The output of these buffers is sent through the connectors to the probes.

Readback Select, PC Readback, and Vector Readback

The readback function allows the Controller board to read the vector output and the program counter. Since all this data takes up 24 bits, it is divided into three 8-bit bytes. The VM0(H) and VM1(H) signals on the VCTR MSEL(H) bus come from the Controller interface and determine which of the three 8-bit bytes will be read. This bus is decoded by U225B, which then turns on one of three comparators, U221B, C, and D. The outputs of these comparators drive the inverting inputs of the readback comparators, U310, U321, U325, U410, U510, and U610.

The output of the readback comparators is wire ORed into buffer U371 (on schematic 32). The comparators that are not enabled output low levels. The enabled comparators act as ECL to TTL converters. Tri-state buffer U371 (on schematic 32) is enabled by VECT MEM RD(L).

P6455 TTL/MOS PATTERN GENERATOR PROBE

The P6455 TTL/MOS Pattern Generator Probe takes data from a 91P16 Pattern Generator or a 91P32 Pattern Generator Expander, and creates ten output lines that can be used to stimulate external circuits. The output has variable high and low levels, and can also go to a high impedance state. See the detailed circuit description following the descriptions of the instrument modules for more details.

91P32 PATTERN GENERATOR EXPANDER

The 91P32 Pattern Generator Expander module can stimulate thirty-two independent channels at rates up to 25 MHz. The module can output a non-repeating sequence up to 512 words deep, or a repeating sequence much deeper. The 91P32 can only work in combination with a 91P16 module (pattern generator). All of the component numbers in the 91P32 module circuit description are assumed to have an A17 preface unless otherwise noted.

This description is divided into several sections. The section divisions are by schematic and then by functional blocks on the schematic. Numbers in diamonds refer to the numbers on schematic tabs in the Diagrams section of this manual. Refer to those schematics while reading the circuit descriptions.

91P32 CONTROLLER INTERFACE 

The 91P32 controller interface takes data from the Controller board and sends it to appropriate registers and RAMs by decoding the lowest four bits of the address bus and interpreting BWR(L), PORT(L), and BRD(L) from the Controller. The interface also takes data from the module and writes it on the data bus at the command of the Controller board.

For example, suppose the Controller board is reading the pod IDs. The Controller writes 1 octal, written on the least significant three bits of the address bus. Simultaneously, BRD(L) and PORT(L) go active, enabling decoder U445, which decodes the address so pin 14 goes active (low). The pod status register, U638, is then enabled and puts data on the data bus. The writing procedure is similar, except the BWR(L) and PORT(L) signals must be active to enable U441 and U448. Table 4-33 shows which registers are connected to the data bus by each hexadecimal address and the BWR(L), BRD(L) and PORT(L) signals.

Table 4-33
91P32 — Controller Interface Map

Hex Addr	BWR	BRD	PORT	Line Name	ICs Affected U#	Schem#
XXX0	X	L	L	CARD ID(L)	U641	37
XXX1	X	L	L	POD READ(L)	U638	37
XXX2	L	X	L	CNTL 0(L)	U538	37
XXX3	L	X	L	CNTL 1(L)	U545	37
XXX4	X	L	L	VCTR MEM RD(L)	U635	37
XXX4	L	X	L	STB LD(L)	U358 U361 U365 U368	40
XXX5	L	X	L	μC 0(L)	U135	40
XXX9	L	X	L	VCTR2(L)	U125 U131	38
XXXA	L	X	L	VCTR3(L)	U325 U331	38
XXXB	L	X	L	VCTR4(L)	U425 U431	39
XXXC	L	X	L	VCTR5(L)	U525 U531	39

91P32 VECTOR MEMORY 2 AND 3 

PC Buffer

The 91P32 Pattern Generator Expander is driven by the program counter from the 91P16. The PC0—PC7 bus comes off the Interconnect board through P1 and is buffered by U621, and U628. The program count then is sent to address all vector memories on the 91P32 as well as the μCode RAM for the 91P32 strobes.

Vector RAM 2 and 3

Before operation, vector RAM 2 and 3 (U125 and U131) is loaded with the values to be output by the probes for each program count (PC) value. Vector RAM 2 is loaded by the VCTR2(L) line and D0—D7. Vector RAM 3 is loaded by the VCTR3(L) line. During run time, the vector memory is addressed by the program counter and outputs the previously programmed data.

The data from vector RAM 2 and 3 goes to registers U115, U318, and U318A—D. These registers clock out the data simultaneously so it is transmitted to the probes with as little skew as possible.

A and B Probe Interface

Differential output buffers U101, U105, U301, and U305 transmit data from the output latches of vector RAM 2 and 3 to the associated probes.

Readback Vector 2 and 3

Comparators U108, U111, U308, and U311 take data from the data output registers of vector memories 2 and 3, convert it from ECL to TTL, and write it on the RVB0—RVB7 bus to the 91P32 controller interface.

The output from the comparators is divided into two 8-bit bytes. Each corresponding bit in the two bytes is wire ORed (RVB0 from byte 2 with RVB0 from byte 3, etc.). Readback bytes are selected by BYTE 2 SEL(H) and BYTE 3 SEL(H), causing the selected byte to output data and the non-selected byte to output zeros (go to a high impedance state).

91P32 VECTOR MEMORY 4 AND 5 

Vector RAM 4 and 5

Vector RAM 4 and 5 (U425, U431, U525, and U531) works identically to vector RAM 2 and 3 (schematic 38), with the exception that vector RAM 4 and 5 are loaded by the VCTR 4(L) and VCTR5(L) signals.

Before operation, the vector RAM is loaded with the values to be output by the probes for each program counter (PC) value. During run time, the vector memory is addressed by the PC0—PC7 bus and outputs the previously programmed data. The data from the vector memory goes to the probe interface and readback circuits.

The data from vector RAM 4 and 5 goes to registers U415, U615, and U515A, C, D, and E. These registers clock out the data simultaneously so it is transmitted to the probes with as little skew as possible.

Readback Vector 4 and 5

Comparators U508, U511, U608, and U611 take data from the data output registers of vector memories 4 and 5, convert it from ECL to TTL, and write it to the 91P32 controller interface on the RVB0—RVB7 bus.

The output from the comparators is divided into two 8-bit bytes. Each corresponding bit in the two bytes is wire ORed (RVB0 from byte 4 with RVB0 from byte 5, etc). Readback bytes are selected by BYTE 4 SEL(H) and BYTE 5 SEL(H), causing the selected byte to output data and the non-selected byte to output zeros (i.e., go to a high impedance state).

Data from the comparators for vector bytes 2 and 3 is wire ORed with the corresponding bits from the comparators for vector bytes 4 and 5. The data from all these comparators goes to tri-state buffer U635, on schematic 37. The Controller board can read selected output data bytes through this buffer by making VCTR MEM RD(L) active.

91P32 STROBES 

Strobe μCode RAM

The strobes in the 91P32 require a signal to trigger. The 91P32 μCode RAM, U135, provides this trigger by writing a zero whenever a strobe is to start, and ones at all other times. The PC0—PC7 bus from the 91P16 addresses this RAM. A strobe is triggered whenever the program counter contains the proper value. The RAM is organized so that DO0 starts strobe 2, DO1 starts strobe 3, DO2 starts strobe 4, and DO3 starts strobe 5.

Strobe Control

Strobe control registers U141 and U341 turn the strobe clock on and off, control which strobe is enabled, and prevent the strobes from being interrupted in the middle of their cycles.

The STB2 SEL(L), STB3 SEL(L), STB4 SEL(L), and STB5 SEL(L) signals are clocked through registers U141 and U341. If any of these signals goes active (low) the corresponding register clocks out a low from its Q(H) output and a high from its Q(L) output. The low from the Q(H) output releases the reset on the corresponding end-detect register (U155B, U151B, U348B, or U351B). This allows the selected strobe to pass through the register and prevents any unselected strobe from getting through.

The high from the Q(L) output of one of the strobe control registers does the following things.

- Masks the EXPANSION CLK(H) signal from clocking any of the strobe control registers, effectively latching up the registers.
- Starts the strobe clock circuit.

The strobe control registers remain in this state until the end of the strobe is detected. The end-of-strobe detector sets the corresponding strobe control register, which reverses the state of its outputs. This stops the strobe clock circuit and allows STB T0(H) entry into the strobe control registers. The registers are now ready to receive another strobe signal.

Strobe Clock

The strobe clock drives all four strobes on the 91P32. The clock is turned on by the Q(L) outputs of the strobe control registers, U141 and U341. When a strobe is selected, the Q(L) outputs of these registers present a high to the D input of register U161A and to pins 11 and 12 of U158.

The high to all these inputs causes the following events:

- OR gate U158C outputs a high, which causes the strobe counter to start counting.
- the output of NOR gate U158B goes low, allowing OR/NOR U158A to start oscillating.
- U161A clocks through a high with the first rising edge from U158A.

The period of oscillation of U158A is determined by the amount of time necessary to charge and discharge capacitors C158 and C160 through R153. As soon as the oscillation starts, the high at the D input of U161A is clocked through. As long as one of the strobe control registers outputs a high on its Q(L) pin, the clock will continue to oscillate.

The strobe clock is shut down by the end-detect circuitry. When the active strobe has an end-detect, the corresponding strobe control register, U141 or U341, is set. Setting the register causes the Q(H) output to go high and the Q(L) output to go low. This causes register U161A to have a low logged in at the next falling edge of the strobe clock.

Once the data is logged in, the outputs of register U161A stop the clock through NOR gate U158B, and load the strobe counter with all zeros through OR gate U158C. The clock now waits to be reactivated by a strobe-select signal.

Strobe Counter

The expansion strobe counter is initially loaded with all zeros. This value is output on the Q0 — Q3 pins of all three counters, U355, U455, and U458. Once started, the counters increment in sync with the strobe clock. The output of the counters then addresses the strobe RAM, U358, U361, U365, and U368.

Strobe RAM

The strobe RAMs (U358, U361, U365, and U368) are programmed before run-time by the Controller board. While programming, the counters are advanced in a single-step fashion by STB LD(L) and STB LDEN(H) through AND gate U148A. After each counter advance, values are loaded into the strobe RAMs by D0(H), D1(H), D2(H), and D3(H) of the pattern generator expander data bus, D0—D7.

When the pattern generator is running, the strobe counter addresses all RAMs simultaneously, incrementing every 40 ns. The RAMs are loaded with zeros for the delay period of the strobe, and then ones for active strobe duration. All strobe RAMs output the strobe data even when only one strobe has been selected. The data from the RAMs is used by the end-detect and polarity-select circuits.

End-Detect and Polarity Select

There are four identical end-detect and demultiplexer circuits; one each for strobes 2, 3, 4, and 5. Since the circuits are identical, only the circuit for strobe 2 is described.

The data from strobe RAM U358 is written to register U155B. If the strobe is not selected, U155B is held reset by strobe control register U141B, so that the strobe data does not pass through. If

strobe 2 is selected, the data is clocked through register U155B at 40 ns intervals. The data from U155B is then clocked through U155A into exclusive-OR gate U451C. This gate makes the strobe active low if STB2 POL(H) is high, otherwise leaving the strobe active high.

AND gate U145C detects the end of the strobe by going high when the Q(L) output of U155B and the Q(H) output of U155A are high. This only occurs when the RAM output data makes a transition from high to low. The high from AND gate U145C sets strobe control register U141B to stop the clock and set the strobe counter back to all zeros.

Probe Clock and Inhibit

Differential buffer U401 transmits the EXPANSION CLK(H) to the probes to be output from the probes. Differential buffer U405 transmits the INH PG signal to the probes, so the probes receive signals to enter a high impedance state.

PROBE DETAILED CIRCUIT DESCRIPTIONS

P6452 DATA ACQUISITION AND EXTERNAL CLOCK PROBE

P6452 DATA ACQUISITION PROBE 

The P6452 Acquisition Probe is used by the Trigger/Time Base board, the 91A32 module, and the 91A08 module. When used with the Trigger/Time Base, the probe is used to acquire external clock signals for acquisition modules and external control signals for pattern generator modules. When used with either a 91A32 or 91A08 module, the probe acquires eight channels of data and may also acquire a clock qualifier signal. All of the component numbers in the P6452 probe circuit description are assumed to have an A7 or A7A1 preface unless otherwise noted.

Refer to the P6452 schematic (schematic 41) and Figure 4-42 while reading this circuit description.

The P6452 acquisition probe is a 10 channel amplifier. Each channel has a minimum small signal gain of 5. The voltage divider and amplifier at the input are hybridized. There are two hybrids for each probe, and each hybrid contains 5 channels. Each channel of the hybrid goes to an ECL line driver. The outputs of the probe are differential ECL.

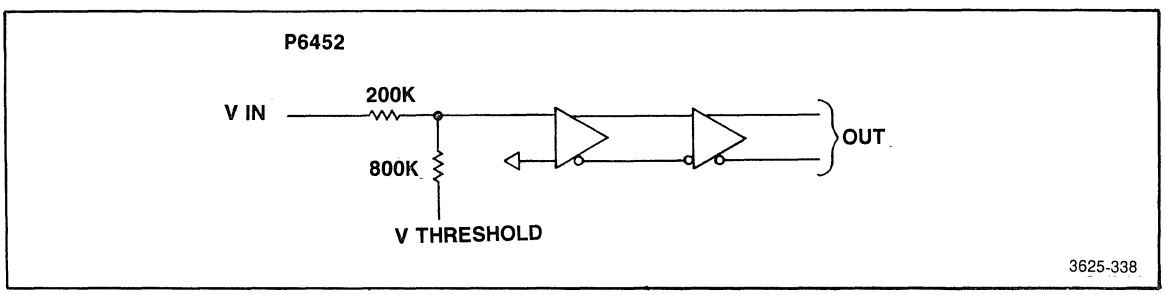


Figure 4-42. One channel of a P6452.

For the probe to respond to an input signal, the signal must be centered around the probe's ground. This is accomplished by applying a threshold (offset) voltage to the shunt leg of the input voltage divider. The voltage divider gives the threshold voltage an effective gain of −4. For example, to set the probe to accept data centered around +1 V, the V threshold input to the voltage divider must be −0.25 V.

P6454 100 MHz CLOCK PROBE

The P6454 100 MHz Clock Probe is used by a 91A08 module installed in slot 6 of a DAS mainframe. The probe acquires external clock signals for 91A08 modules at rates up to 100 MHz. The P6454 probe will only operate when connected to a 91A08 module in slot 6. All of the component numbers in the P6454 probe circuit description are assumed to have an A9 preface unless otherwise noted. The package of the P6454 100 MHz Clock Probe is simple enough that no schematic is provided in the manual. Refer to Figure 4-43 while reading this circuit description.

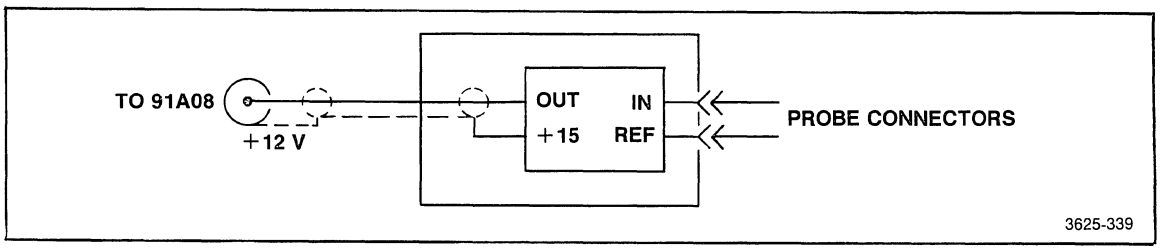


Figure 4-43. P6454 100 MHz Clock Probe.

A hybrid at the probe tip acts as a 1 MΩ input, 50 Ω output, 10X FET probe. The two inputs to the probes, V_{in} and V_{ref}, perform the same function as the signal and ground inputs on standard probes. The only exception is that V_{ref} may be referenced to a dc voltage other than ground. The hybrid output will track V_{in} with respect to this reference level.

The cable of the P6454 probe is cut to electrical length at the factory. This cable length is critical since it controls the setup time of all 91A08 modules in the DAS when the external clock is used. The cable is a 50 Ω coaxial cable. The shield carries +12 V for use by the hybrid. The center conductor carries the clock signal, which rides above the probe ground.

P6455 TTL/MOS PATTERN GENERATOR PROBE

P6455 TTL/MOS PATTERN GENERATOR PROBE 

The P6455 TTL/MOS Pattern Generator Probe is used by 91P16 and 91P32 pattern generator modules. The probe outputs ten channels of data at TTL and MOS logic levels. The output levels of the probe (V_{out}) are set by the voltages present at the probe inputs V_H (high output level) and V_L (low output level). Channels 0 through 7 are defined as data channels and have inhibit (tri-state) capabilities. Channels 8 and 9 output clock and strobe signals and do not inhibit. All of the component numbers in the P6455 circuit description are assumed to have an A15 or A15A1 preface unless otherwise noted.

Refer to the P6455 schematic (schematic 42) and Figure 4-44 while reading this circuit description.

A hybrid data driver circuit drives each output channel of the probe. These hybrids cannot be serviced. The hybrids require the two user-defined voltages (V_H and V_L), +6 V, and −5 V to operate. The INHIBIT(L) input operates around ECL levels, but the high state (not inhibit) must be high impedance (no current flow out of the node).

Diode CR114, which is common to all channels, prevents current flow if V_H and V_L are reversed. The diodes from the output of each hybrid to V_H and V_L are also for circuit protection.

The circuitry around Q316, Q318, Q114, and Q214 receives the INHIBIT(L) signal. Transistors Q316 and Q318 form a current switch. In the non-inhibit mode, Q318 is turned on, putting approximately 3.1 V on the bases of Q114 and Q214. The emitters of Q114 and Q214 are at approximately 3.8 V. Since the nominal voltage at the inhibit pin of the hybrid (pin 5) is approximately +4 V, diodes CR110, CR111, CR112, CR210, CR211, CR212, CR213, and CR310 cannot conduct. This turns off the INHIBIT(L) signal.

When inhibit is enabled, Q318 turns off. Voltage divider R215 and R216 biases the bases of Q114 and Q214 to about 1.6 V. This turns on Q114 and Q214, putting their emitters at approximately 2.3 V. This allows the diodes to conduct, so the inhibit pin of the hybrid drops to about +3 V causing the hybrids to tri-state.

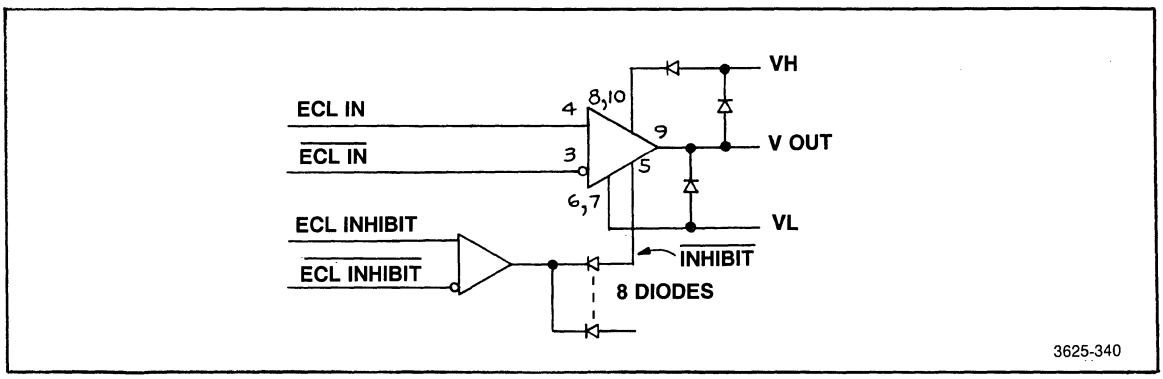


Figure 4-44. One channel of a P6455.

P6456 ECL PATTERN GENERATOR PROBE

P6456 ECL PATTERN GENERATOR PROBE 

The P6456 ECL Pattern Generator Probe is used by 91P16 and 91P32 pattern generator modules. The probe outputs ten channels of data at ECL logic levels. The output levels of the probe (V_{out}) are set by the voltages present at the probe inputs V_H (high output level) and V_L (low output level). Channels 0 through 7 are defined as data channels. Channels 8 and 9 output clock and

strobe signals. The P6456 ECL probe does not have inhibit capabilities and does not respond to an INHIBIT(L) signal from a pattern generator module. All of the component numbers in the P6456 circuit description are assumed to have an A16 or A16A1 preface unless otherwise noted.

Refer to the P6456 schematic (schematic 43) and Figure 4-45 while reading this circuit description.

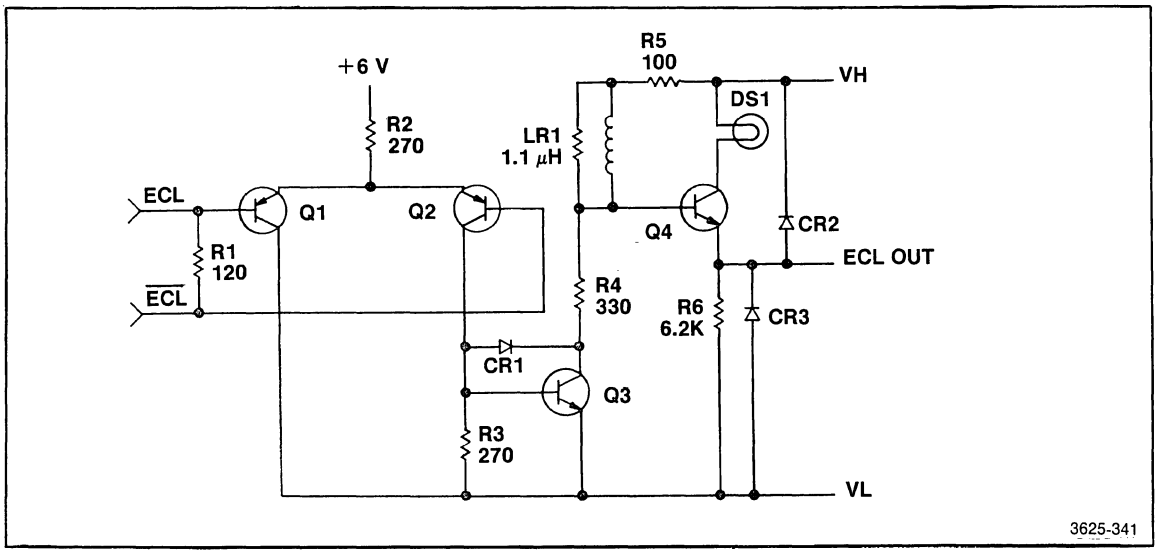


Figure 4-45. One channel of a P6456.

Transistors Q1 and Q2 form a differential-pair current switch. They turn Q3 on and off. When Q3 is off, R5 and LR1 pull up on the base of Q4. Resistor R6 is a pull-down resistor that pulls a nominal amount of sink current. This allows the probe to run at slow speeds (for instance, with the diagnostic lead set) without an external pull-down resistor.

When Q3 is on, the base of Q4 is pulled low so the ECL OUT node goes to an ECL low.

Diode CR1 serves as a Baker clamp which speeds up the turn-on of Q3. LR1 provides some peaking to the output of Q4 to compensate for the effect of the lead set. Lamp DS1 at the collector of Q4 provides current limiting. The bulb usually has a low resistance, but if too much current flows (if the emitter of Q4 is shorted to ground) the filament heats up and increases its resistance.

The outputs of the probe are static-protected by diodes CR2 and CR3 and by spark gaps designed into the printed circuit board.

OPTION DETAILED CIRCUIT DESCRIPTIONS

OPTION 01 - TAPE DRIVE

The optional tape drive provides a mass storage device for the DAS. Tapes may be loaded with data stored in reference memory, mnemonic disassembly tables, acquisition setups, pattern gen-

erator programs, or all of the above. The tape drive uses DC100-type data cartridges. Each cartridge can hold several different setups, lists, and programs. All of the component numbers in the tape drive circuit description are assumed to have A18 as a preface unless otherwise noted.

This description is divided into several sections. The section divisions are by schematic, and then by functional blocks on the schematics. Numbers in diamonds refer to numbers on schematic tabs in the Diagrams section of this manual. Refer to those schematics while reading this circuit description.

TAPE FORMAT

The data stored on the tape by the tape drive is encoded by duty cycle modulation. The tape drive indicates the beginning of one clock period on the tape by writing a rising edge. The presence of a 1 or a 0 on the tape is determined by the location of the falling edge between two rising edges. A falling edge that is 1/3 into the clock period indicates a 0. A falling edge that is 2/3 into the clock period indicates a 1. Figure 4-46 illustrates the format.

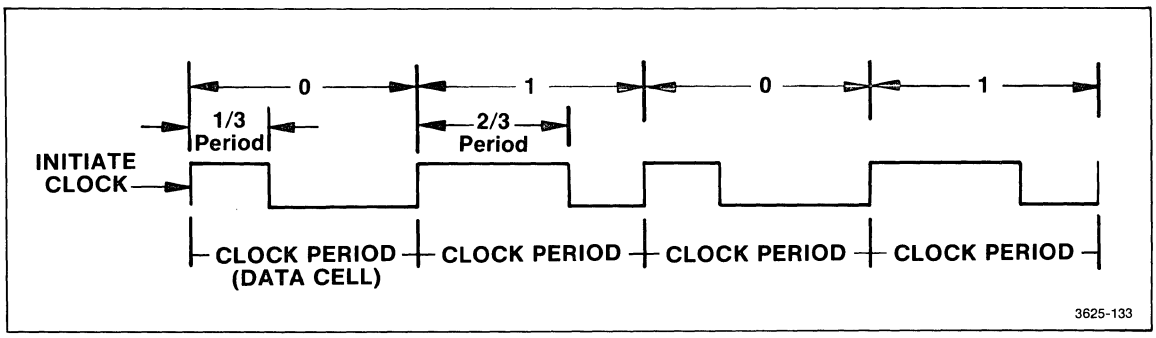


Figure 4-46. Tape bit storage format.

The stored data is divided into bytes by an internal counter in the tape controller IC. The data stored by the tape drive is divided into manageable sections called records. Each record contains 256 eight-bit bytes. These records include a preamble, a header, the data, and a postamble. The data in the header, preamble, and postamble includes the number assigned to the record, record format information, and a Cyclic Redundancy Check (CRC) value. The CRC is an error detection code that indicates whether the data read from the record is the same as the data originally written into the record.

Each record occupies approximately 4.85 inches of the tape. The records on the tape are separated from one another by a 0.9 inch section of tape that contains no data. The format of a single record is shown in the Figure 4-47.

The magnetic tape in the data tape cartridge contains holes at the beginning and the end of the tape. These holes are light-sensed. The tape drive detects the presence of the holes and performs the steps necessary to avoid running the tape off the end of the spool.

At the beginning of a tape there are three sets of two holes each. Each set is placed 12 inches apart and the two holes in each set are 0.218 inches apart. Twenty-four inches after these paired holes there is a single hole. This single hole marks the beginning of useable tape space.

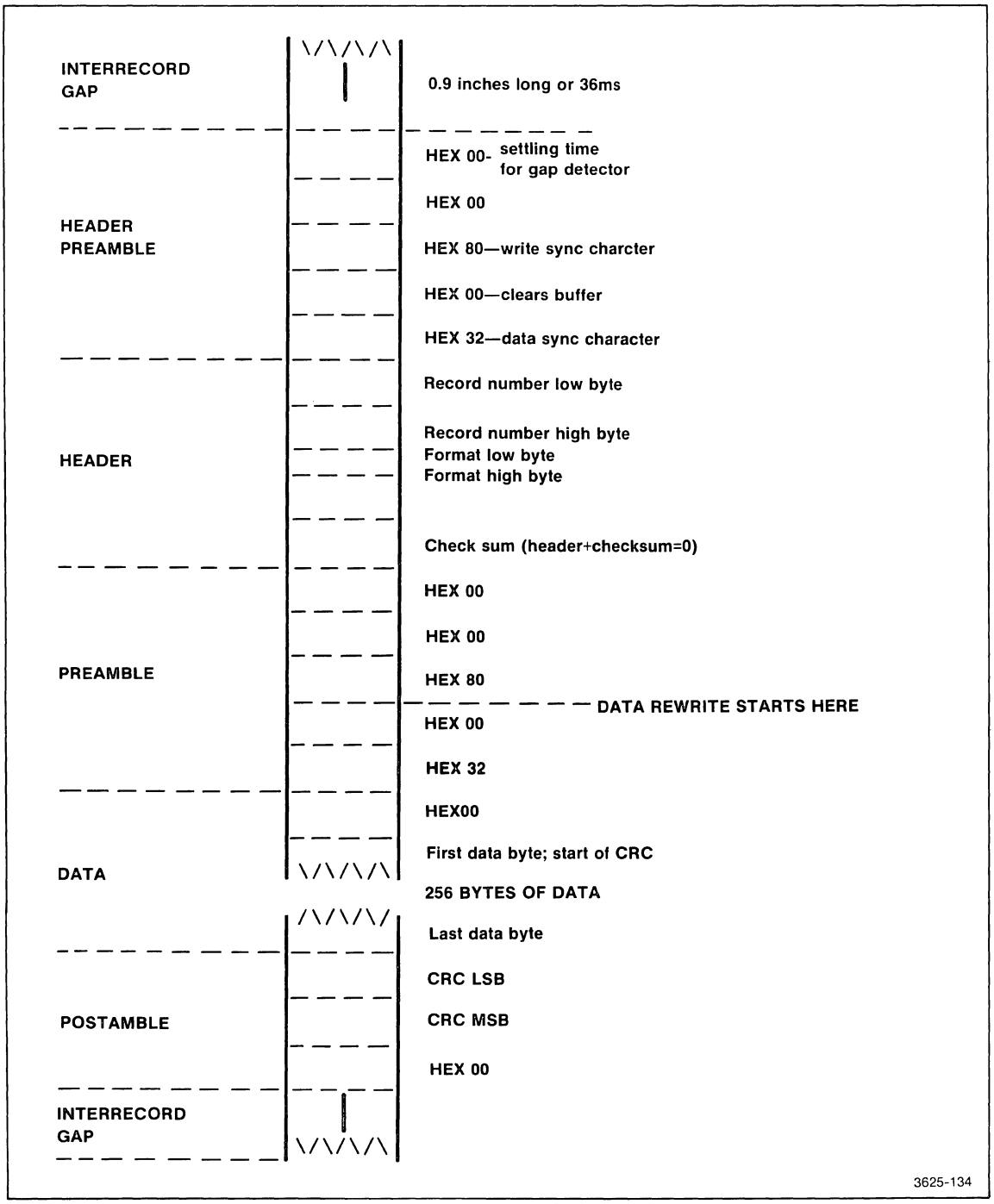


Figure 4-47. Tape record format.

At the end of a tape there is a single light-sensed hole to warn that the end of usable tape area is approaching. Twenty-four inches after this single hole, there are three individual holes spaced 12 inches apart. These holes mark the end of usable tape.

TAPE DRIVE DATA BOARD 

This board provides the interface between the tape drive and the DAS mainframe. It converts parallel data to serial data as well as performing serial-to-parallel data conversions and reading from and writing to the tape head. All circuitry on the data board has an A18A1 preface.

Tape Controller

The tape controller, U661, is a Tektronix-made M233 Tape Controller that provides both data and tape drive motion commands. The data control consists of read and write operations under the supervision of the mainframe Controller board. The tape controller also performs CRC calculations using the CRC-16 algorithm.

The tape controller also senses write-protect, and cartridge-in-place signals.

The tape controller IC has 40 pins that are identified as follows:

Table 4-34
Tape Controller Pin-Outs

Pin #	Signal Name	I/O	Description
1	RESET	I	Resets all tape controller functions.
2	INT	O	Interrupt. Current limited to drive transistor base. Does not provide TTL levels.
3	READ(L)	I	Microprocessor read request.
4	SEL(L)	I	Tape controller select
5	WRITE(L)	I	Microprocessor write.
6	A1	I	Register address line 1
7	A2	I	Register address line 0
8	D7	I/O	Data line 7 (msb)
9	D6	I/O	Data line 6
10	D5	I/O	Data line 5
11	D4	I/O	Data line 4
12	D3	I/O	Data line 3
13	D2	I/O	Data line 2
14	D1	I/O	Data line 1
15	D0	I/O	Data line 0 (lsb)
16	SC1(L)	O	Tape drive servo control bit 1
17	SC2(L)	O	Tape drive servo control bit 2
18	SC3(L)	O	Tape drive servo control bit 3
19	Digital ground	--	
20	CNIP	I	Cartridge not in place
21	HOL(L)	I	Hole detected
22	SFF(L)	I	Servo fail flag
23	RDATA	O	Read data from decoder
24	PDATA	O	Peak detected but still encoded
25	EDI	I	External data input
26	Not used	--	
27	Write V	--	4.75 V to 5.25 V supply for write buffer

Table 4-34 (cont)
Tape Controller Pin-Outs

Pin #	Signal Name	I/O	Description
28	Write A+	O	These four lines determine the direction of the write current in the selected tape head
29	Write A−	O	
30	Write B+	O	
31	Write B+	O	
31	Write B−	O	
32	WINH	I	Write-inhibit signal: status set by data cartridge
33	IT	O	Increase threshold: decreases output from read amplifier
34	T B/A(L)	O	Selects data track A or B
35	Pdata In	I	Peak data from read amplifier
36	Not used	--	
37	GDET	I	Inter-record gap detected
38	Clock	--	75 times the write bit rate
39	+5 V digital	--	4.75 V to 5.25 V
40	Bit clock	--	Clocks valid data. Used with EDI

The tape controller IC have five internal eight bit registers; two command registers, a status register, and one bidirectional data register. Selecting registers is controlled by the A0 and A1 address lines and the read/write select line. The command registers can only be written to, and the status register can only be read from. Register addresses are shown in Table 4-35.

Table 4-35
Tape Controller Register Addresses

	Address			
Register	A1	A0	READ(L)	WRITE(L)
Data	X	L	X	X
Command 1	L	H	X	L
Command 2	H	H	L	X
Status	X	H	L	X

The Data register contains two bidirectional data buffers that receive data to be stored on the tape, or program the tape controller IC, or hold data that has been read from the tape.

The Command 1 register is an 8-bit register that holds control bits that regulate the operation of the tape heads and the servo control bits.

The Command 2 register is an 8-bit register that controls the CRC calculations, the write current, the gap-detect interrupt, and data logging procedures.

The Status register holds eight status bits that must periodically be read by the host microprocessor. The status bits contain information regarding what sort of service is required by the tape controller from the host microprocessor, whether the tape is write-inhibited, whether an inter-record gap is detected, if a tape cartridge is in place, if a hole in the tape is detected, or if the tape servo has failed.

The bus read/write mode for the tape drive is selected at tape controller U661 pins 3 and 5, respectively. Pin 4 is the tape controller SEL(L) signal. When the SEL(L) signal is low, the tape controller is enabled. SEL(L) must be held low during the entire read/write operation. When write mode is selected, data flows from the DAS Controller board to the tape controller through pins 8 through 15 of U661. When read mode is selected, data flows the other direction. The READ(L) and SEL(L) signals also control the direction bidirectional buffer U651.

Tape controller U661 synchronizes and prepares data for reading or writing on either track A or B of the tape drive.

Write Circuitry

Data to be written to the tape is applied to the tape head through buffers, U851 and U841C and D, and a diode-resistor network using the diodes contained in CR361. The network is enabled by a positive voltage applied through diode CR631 from transistor Q666 (in the write-inhibit block). Transistor Q666 is turned on whenever a tape cartridge is in place that is not write-protected (detected by the status board, A18A3A2). Depending on the status of the bit being written, write current flows either up or down through the tape head. The diodes provide isolation when the tape head is reading and steer the current flow when the head is writing.

Write-Inhibit

Write-inhibit circuitry is enabled when the status board does not detect a write-enabled tape cartridge in place. When writing is enabled, +12 V is applied to transistors Q666 and Q765. Q666 applies a positive voltage to CR361, which allows write current to flow through the tape head. Applying +12 V to the base of Q765 turns it off, which causes a high to pin 32 of tape controller U661. This high signals the tape controller that writing is allowed.

If the cartridge is not write-enabled, the status board supplies no current to transistors Q666 and Q765. This prevents current from flowing through the tape head and signals tape controller U661 that writing is not permitted.

Read Amplifier and Track Select

When tape controller U661 is reading data from the tape head, the diodes in the write circuitry disable all inputs to the tape head. The head then generates current due to changes in the magnetic flux from the tape. This current due to flux changes is applied to the read preamplifier, U721A and D, and then to the track select circuit, U615A and B. The track-select circuitry selects which track will be read and sends data from the selected track to the programmable gain circuit.

Programmable Gain

The programmable gain circuit receives the output of the track-select circuit and the INCRTH (increase threshold) signal from the tape controller IC. The INCRTH signal halves the gain of U721. This has the same effect as the magnetic tape losing half of its magnetism. The signal may be used to verify data that has been written on the tape.

Peak and Threshold Detectors

Both the peak and threshold detectors receive data out of the programmable gain circuit. The peak and threshold detectors operate together to decode the data stored on the tape, and differentiate between good and bad data.

Peak detector U611A switches state whenever a peak of the opposite polarity from the previous peak is detected. The period of time between peaks is decoded by tape controller U661 into a logic 1 or 0. The output of the peak detector goes directly to tape controller U661 to be decoded into 8-bit bytes.

The threshold detector, U611B, switches states whenever the output of the programmable gain circuit passes a certain threshold. The threshold detector separates valid data on the tape from back-ground noise. The following conditions define the logic states of the threshold detector (ADATA is the output of the programable gain circuit):

Threshold detector output = 1, when ADATA $> V_{gnd} + 0.287\ V \pm 30\ mV$
Threshold detector output = 0, when ADATA $< V_{gnd} - 0.198\ V \pm 20\ mV$

The output of the threshold detector also controls the operation of the peak detector through R813.

Gap Detector

Gap detector U805, and U611C and D signals tape controller U661 when it has detected an inter-record gap. The gap-detect circuit is slow actuating and deactuating so that noise in a gap does not cause false beginning-of-gap or end-of-gap detections.

2 V Reference

This reference, generated by U721B, provides a common reference for the read amplifier, programable gain threshold and peak detector, and gap detectors.

TAPE DRIVE SERVO BOARD 

Control of the tape drive motor is accomplished with the Servo board. The Servo board is comparable to the summing point in a traditional servo loop because it receives both motion commands and feedback signals, and from these signals generates its own drive commands. Motion commands come from the the tape controller IC located on the Data board (A18A1).

The feedback from the motor consists of tachometer pulses from the timing disk attached to the tape drive motor shaft. The tachometer pulses are generated by an infrared LED/light detector pair located on the Sensor board (A18A3A1).

The drive command generated by the Servo board is a dc voltage that drives the tape drive motor. Functionally, the Servo board may be divided into four areas: the clock circuit, the microcomputer, the modulator circuit, and the bridge circuit. All circuit numbers refered to in the Servo board circuit descriptions are assumed to have an A18A2 preface unless otherwise noted.

Clock

The clock is a crystal-controlled oscillator that consists of crystal Y333 and four inverters in U321. The clock output is 4 MHz which is used by the modulator. A tap off of the modulator divider provides a 2 MHz clock for the microprocessor.

Microprocessor

This description is confined to microcomputer operation as it applies to the operation of the tape drive. For a detailed description of the 6500/1, refer to Rockwell literature.

Microcomputer U211 is the Rockwell 6500/1. It is a single chip microcomputer that has been custom-programmed for use in the tape drive servo circuit. Standard features of the 6500/1 include four bidirectional input/output ports of eight bits each, 64 bytes of RAM, and 2048 bytes of ROM. It receives motion commands from the tape controller IC. By using firmware algorithms, feedback information, and housekeeping information, it outputs digital words that control the speed and direction of the tape drive.

Motion commands from tape controller U651 (schematic 45) to the microcomputer are input at pins 22, 23, and 24. These three bits provide eight tape motion possibilities. The possibilities are shown in Table 4-36.

Table 4-36
Tape Motion Commands

Motion Command	SC3(L)	SC2(L)	SC1(L)
Stop	0	0	0
Find beginning of tape	0	0	1
Reset servo fail	0	1	0
Acknowledge power up	0	1	1
Forward at 25 ips	1	0	0
Reverse at 25 ips	1	0	1
Forward at 60 ips	1	1	0
Reverse at 60 ips	1	1	1

In addition to motion commands, U221 receives a system reset signal at pin 39. When this signal is low, the 6500/1 is prevented from operating. When this signal goes high, the 6500/1 begins executing its program. The cartridge in place (CIP) signal at pin 31 is a status signal informing the 6500/1 that a tape cartridge is in place, and that it is safe to operate the servo.

There are two types of feedback to the 6500/1: cartridge status feedback and tape motion feedback. Cartridge status feedback results from the housekeeping information (beginning and end of tape and cartridge in place). The main source of housekeeping information is the hole-detect (HDT) signal applied at pin 32. By counting the number of holes and knowing the current direction and speed of tape motion, the internal firmware can determine the initial tape position. The 6500/1 also outputs a hole-detect signal at pin 14 for use by tape controller U651 (schematic 45).

Tape motion feedback is in the form of chopped light pulses that originate at the timing disk attached to the drive motor shaft. The light pulses are converted to electrical pulses by the sensor

board (A18A3A1) and then are referred to as tachometer pulses. Tachometer pulses are received by the 6500/1 at pin 38 and are used to measure the distance traveled by the tape. Tachometer pulses do not correspond to bit position on the tape.

Tape motion commands are two digital words. One word controls the tape drive motor speed. This word controls the modulator. The second word controls the direction of the drive and is applied to the bridge circuit. Drive motor speed control commands come from pins 2 through 9 of the 6500/1. The commands are eight bits in length and provide quasi-linear drive motor speed control.

Drive motor direction commands are output at pins 25 through 28 of the 6500/1. The Table 4-37 gives the bit values for the direction commands.

Table 4-37
Drive Motor direction Commands

Command	DR3	DR2	DR1	DR0
Forward	0	1	1	0
Reverse	1	0	0	1
Off	1	0	1	0

An additional output at pin 29 is motor off (MOF(H)). This signal is applied to the modulator and when active (high) holds the modulator output off by holding D flip-flop U221B cleared.

Pin 21 is the input line for the internal counter. It is used in conjunction with pin 33 to perform a power-up test of the modulator and internal timing chains.

Pin 33 is an input for port A and is to detect edges on the modulator during testing. See the pin 21 description.

Pins 35 and 40 are used in conjunction with the check port (pins 16 through 20). Pin 35 is used to measure the time that the NMI signal is low.

Pin 40 is the non-maskable interrupt to the 6500/1. The length of time that this signal is held low determines the test that will be run.

Pin 15 is the at-speed signal. It is output by the 6500/1 when the drive motor is at drive speed.

Pins 34 and 36 are used to select various operating modes. Pin 36 allows for selection of a 1 MHz or 2 MHz microprocessor. This output must agree with the frequency of the clock supplied to the 6500/1. Pin 35 is a logic 0.

The servo fail flag is output at pin 13.

Pins 16 (msb) through 20 (lsb) are check ports that indicate which firmware subroutine is being executed. Table 4-38 shows the correspondence between firmware subroutines and the value put out by pins 16 through 20.

When the 6500/1 is reset, a test sequence is started. The test sequence starts with an internal check of the 6500/1, then checks the modulator circuit. After the self-test, the 6500/1 is ready to run.

Table 4-38
6500/1 Check Port Values

Port Value	Meaning
1F	Hardware reset
1E	Internal ROM check in progress, ports set up.
1D	RAM check in progress, ROM OK.
1C	Modulator check in progress, RAM OK.
1B	Modulator OK, signal host microprocessor that everything works.
1A	Acknowledge received from host. Start tape operation.
19	The sequence hangs here if the drive does not detect a cartridge in place.
18	Fault 1 error.
17	Waiting for cartridge removal.
16	Hole detected error (not fatal)
15	Waiting for fault acknowledge, hole too long. May indicate that the tape ran off the end.
14	BRK error
13	Waiting for hole acknowledge
12	Waiting for fault acknowledge
11	Slow clock error
10	Fast clock error
0F	Waiting for BOT acknowledge
0E	Double hole found (located at beginning of tape).
0D	Start BOT (find beginning of tape) sequence.
0C	Executing HARDRAMP sequence.
0B	Executing SLOWDN25 sequence. This sequence slows the drive from 60 ips to 25 ips.
0A	Executing STOP60. Brings tape drive to a stop.
09	Executing REG60. Brings the tape drive up to 60 ips and regulates the speed.
08	RAMPC subroutine entered. Brings the tape drive from 0 ips up to 25 ips.
07	Executing HARDSTOP routine.
06	6500/1 sets up the pointers for the SLOWDN25 routine and turns off the tape drive motor.
05	Executing COAST subroutine which sets up pointers for STOP60 and turns off the drive motor.
04	Setting up pointers for ramping the tape drive motor to 60 ips.
03	Setting up pointers for ramping the tape drive up to 25 ips.
02	Executing the DLY100 command. This subroutine delays 100 counts. It is used for final tape positioning at the end of a BOT (find beginning of tape) command.
01	Executing the tape hole checking subroutine.
00	Executing SCAN. This subroutine ensures that tape motion commands are valid and executed in a manner that is safe for the magnetic tape.

Modulator

The modulator consists of two 4-bit adders, a counter, and a latch. It receives inputs from the clock circuit and the microcomputer, and its output is a logic signal to the bridge circuit that controls the amount of voltage applied to the tape drive motor.

The output of the 4 MHzclock circuit clocks counter U301. The counter is free-running as long as register U221A is held clear. The counter output is one of the two inputs to adders U201 and U115. The other input to these adders is a digital word from the microcomputer (6500/1) that is proportional to the voltage to be applied to the tape drive motor.

For the purposes of this explanation, assume that the counters begin counting at zero. Also assume that the digital word from the 6500/1 is 0F hexadecimal. With these conditions, one input to the adders is 00 (from the counter) and the other input is 0F (from the 6500/1). The counter begins to increment. As soon as the counter reaches F0 hexadecimal, a carry signal goes to flip-flop U221B. The output of U221B goes to the bridge circuit where it controls the bridge drive voltage.

As long as flip-flop U221B is set, transistor Q161 is turned on. With Q161 on, +V1 is applied through Darlington amplifier Q165 to the tape drive motor to turn it. Drive direction is controlled by the bridge circuit which is explained later.

If the digital word from the 6500/1 had been a hexadecimal 00, a carry signal would never occur. Therefore, a hexadecimal 00 results in a drive voltage off and a hexadecimal FF results in the drive voltage always on.

Bridge Circuit

The bridge circuit applies the drive voltage to the tape drive motor. It also controls the direction of current flow to the motor, and thus its drive direction.

The drive direction word from the 6500/1 is applied to comparators U325A and B. If the motor is to turn in the forward direction, the output of U325A is high. This high turns on transistor Q354, which turns on Darlington amplifiers Q265 and Q365. Current then flows through the motor in the direction necessary for forward tape motion.

When the motor is to drive in the reverse direction, the output of U325B is high to turn on transistor Q352. The output of Q352 turns on Q260 and Q360, so current flows in the opposite direction. This reverses the direction of the motor.

Transistor Q165, which is turned on by transistor Q161, controls the value of V+ to the bridge circuit. Q161 is turned on whenever flip-flop U221B is set. The length of time Q165 is on is determined by the length of time flip-flop U221B is set.

When Q165 is on, inductor L150 and capacitor C255 are charged up. The time constant of this filter is much longer than the charging pulses, so the filter rises or falls to a constant voltage, depending on the action of the modulator circuit.

Servo Board Test Routine

The ROM in the 6500/1 provides an open loop test of the Servo board. This test is entered through the NMI interrupt pin. The duration that the NMI pin is held low determines the test that

will be performed. During these tests, caused by the NMI pin, the values output by pins 16 (msb) through pin 20 (lsb) take on new meanings. Table 4-39 lists the tests available, how long NMI must be held to activate them, and the new port meanings.

Table 4-39
Servo Board Test Routine

Port Value	Test	Time NMI held low
00	Drive forward with modulator value of 00	64.77 ms
01	Drive forward with modulator value of 20	63.03 ms
02	Drive forward with modulator value of 40	60.70 ms
03	Drive forward with modulator value of 60	58.63 ms
04	Drive forward with modulator value of 80	56.57 ms
05	Drive forward with modulator value of A0	54.53 ms
06	Drive forward with modulator value of C0	52.44 ms
07	Drive forward with modulator value of E0	50.42 ms
08	Drive reverse with modulator value of 00	48.22 ms
09	Drive reverse with modulator value of 20	46.18 ms
0A	Drive reverse with modulator value of 40	44.14 ms
0B	Drive reverse with modulator value of 60	42.03 ms
0C	Drive reverse with modulator value of 80	40.01 ms
0D	Drive reverse with modulator value of A0	37.95 ms
0E	Drive reverse with modulator value of C0	36.01 ms
0F	Drive reverse with modulator value of E0	33.77 ms
10	Modulator output (bridge off) 00	31.78 ms
11	Modulator output (bridge off) 20	29.75 ms
12	Modulator output (bridge off) 40	27.68 ms
13	Modulator output (bridge off) 60	25.61 ms
14	Modulator output (bridge off) 80	23.59 ms
15	Modulator output (bridge off) A0	21.54 ms
16	Modulator output (bridge off) C0	19.50 ms
17	Modulator output (bridge off) E0	17.59 ms

TAPE DRIVE SENSOR AND STATUS BOARDS 

Sensor Board

The Sensor board is mounted on the tape drive housing. The board has assembly number A18A3A1.

The Sensor board holds an infrared LED and photo-transistor pair. These components are used by the Servo board (A18A2) to monitor the rotation of the tachometer wheel attached to the drive motor. As the tachometer wheel rotates, it alternately transmits and obstructs light from the LED. The transistor then turns on and off according to how fast the tachometer wheel rotates.

Status Board

The Status board is mounted on the tape drive housing. The board has assembly number A18A3A2.

The Status board monitors the current status of the tape cartridge installed in the tape drive. Switch S2 turns on whenever a cartridge is in place. Switch S1 turns on only when a write-enabled cartridge is in place. The signals from these switches are used by the Servo board (A18A2) and the Data board (A18A1).

The Status board also has an infrared LED and a photo-transistor to detect holes in the magnetic tape. When a hole is detected by transistor Q1, the output of the transistor goes to a high-pass filter consisting of the U1B and C circuitry. The high-pass filter allows the sudden burst of light through a hole in the tape to pass, but will not allow signals due to ambient light to trigger the hole detect circuit.

OPTION 02 – I/O INTERFACE

The I/O interface provides a means for the DAS to communicate with another DAS or other intelligent devices. The I/O interface provides GPIB and RS-232 interface capabilities. The I/O interface also has a composite video output. All of the component numbers in the I/O interface circuit description are assumed to have A19A1 as a preface unless otherwise noted.

This description is divided into several sections. The section divisions are by schematic, and then by functional blocks on the schematic. Numbers in diamonds refer to numbers on schematic tabs in the Diagrams section of this manual. Refer to those schematics while reading this circuit description.

I/O INTERFACE GPIB AND RS-232 

I/O Board Controller Interface

The I/O board Controller interface takes data and control signals from the DAS Controller board and uses them to control the GPIB and RS-232, interfaces and to retrieve instructions from the firmware. U246 buffers the DAS data bus and is enabled through inverting input NOR gate U347B by PORT 8(L), COM CS(L), or ROM SEL(L). Table 4-40 shows which integrated circuit is connected to the data bus by each hexadecimal address and the BRD(L), RESET(L), and PORT 8(L) signals.

Table 4-40
I/O Controller Interface Map

Hex Addr	PORT 8(L)	BRD(L)	U#
XXX0 to XXX3	L	X	U135
XXX4 to XXX7	L	H	U251
XXX8 to XXXF	L	X	U242

Buffer U135 transmits the GPIB address of the DAS when it is enabled. U251 is the RS-232 interface controller, and U242 is the GPIB interface controller.

ROM

There are four ROMs in the I/O Interface that hold firmware to control the GPIB and RS-232; U455, U451, U445, and U440. U440 may be a programmable read-only memory used to fix errors in the firmware. U551 and U545 buffer the address bus coming from the interconnect to address the ROMs. One of the four ROMs is selected by the data held by register U331. U331's data is then decoded by U335 to enable the selected ROM.

NAND gate U335A detects when the ROMs are to be read. The ROMs are read when BRD(L), SEL SLOT(L), and PERSONALITY(L) are all active. This condition makes NAND gate U335A output a low to enable decoder U335B. U335B then selects the ROM to be read. The ROM is selected by the two lowest data bits in conjunction with BWR(L) and PORT 8(L) being active. Table 4-41 shows the ROM select code.

Table 4-41
I/O ROM Select Codes

BWR(L)	PORT 8(L)	D1	D0	Selected ROM
L	L	0	0	U455
L	L	0	1	U451
L	L	1	0	U445
L	L	1	1	U440

GPIB Control Buffer

Buffer U135 transmits the GPIB address to which the DAS is set when it is enabled by the controller interface. The address is set with the DIP switch on the back panel of the DAS mainframe. The switch also has a place to specify the line terminator for RS-232 and GPIB transmissions.

GPIB

U242 is the integrated circuit that controls the GPIB interface for the DAS. U242, a TMS9914 GPIB Controller chip, performs the interface function between an IEEE 488-1975/78 General Purpose Interface Bus (GPIB) and a microprocessor. It communicates with the microprocessor via a memory-mapped 8-bit data bus and provides a 16-bit bus to interface with the GPIB through buffers. IEEE 488-1975/78 standard protocol is handled automatically in Talker or Listener operational modes.

The IEEE 488 standard uses the negative logic convention for the GPIB lines. The FALSE state is represented by a high voltage ($>$2.0 V); the TRUE state is represented by a low voltage ($<$0.8 V). The GPIB terminations of the TMS9914 are in agreement with this convention. For example, if Data Valid is true, the DAV line is pulled low by the device. These terminations are connected to the bus through non-inverting buffers to obtain the correct signal polarity.

Note that the terminations on the microprocessor side of the device are in positive logic. This is in agreement with the logic used by the DAS microprocessor. Table 4-42 is a list of the pins of U242 and their functions.

Buffers U227, U231, U127, and U131 are line drivers to isolate the GPIB chip from the bus.

Table 4-42
TMS9914 Pin Functions

Name	Pin	Function
ACCRQ(L)	1	ACCESS REQUEST: this pin becomes low to request a direct memory access.
ACCGR(L)	2	ACCESS GRANTED: when received from the direct memory access controller, this enables the byte onto the data bus.
CE(L)	3	CHIP ENABLE: the chip is active when the CE(L) line is pulled low.
WE(L)	4	WRITE ENABLE: when low this line indicates to the TMS9914 that data is being written to one of its registers.
DBIN	5	DATA BUS IN: a high state indicates to the TMS9914 that a read is about to be carried out by the MPU.
RS0 RS1 RS2	6 7 8	REGISTER SELECT LINES: determine which register is addressed by the MPU during a read or write operation.
INT(L)	9	INTERRUPT: sent to the MPU to cause a branch to a service routine.
D7 (lsb) D6 D5 D4 D3 D2 D1 D0 (msb)	10 11 12 13 14 15 16 17	Data transfer bits on the MPU side of the device.
CLOCK(L)	18	CLOCK: up to 5 MHz maximum input. Need not be the system clock.
RESET(L)	19	RESET: initializes the TMS9914 at power-up.
V_{ss}	20	Ground reference voltage.
TE	21	TALK ENABLE: controls the direction of transfer of the line transceivers.
REN	22	REMOTE ENABLE: sent by the system controller to select control either from the front panel or from the GPIB.
IFC	23	INTERFACE CLEAR: sent by the bus system controller to set the interface system to a known quiescent state. The bus system controller becomes the bus controller in charge.
NDAC	24	NOT DATA ACCEPTED: handshake signal. Acceptor sets this high when it has latched the data from the I/O lines.

Table 4-42 (cont)
TMS9914 Pin Functions

Name	Pin	Function
NRFD	25	NOT READY FOR DATA: handshake signal. Sent by acceptor to indicate readiness for the next byte.
DAV	26	DATA VALID: handshake signal controlled by source to show acceptors when valid data is present on the bus.
EOI	27	END OR IDENTIFY: if ATN is high this indicates the end of a message block. If ATN is low, the bus controller is requesting a parallel poll.
ATN	28	ATTENTION: sent by bus controller in charge when LOW interface commands are being sent over the DIO lines. When this signal is high, the DIO lines carry data.
SRQ	29	SERVICE REQUEST: set low by a device to indicate a need for service.
CONT(L)	30	CONTROLLER: controls the direction of the transfer of the bus transcievers for the bus management lines (ATN, and SRQ). When high, the device is the bus controller in charge.
DIO8 (msb)	31	DIO8 through DIO1 are the data input/output lines on the GPIB side. These pins connect to the IEEE 488 bus via non-inverting transceivers.
DI07	32	
DI06	33	
DIO5	34	
DIO4	35	
DIO3	36	
DIO2	37	
DIO1 (lsb)	38	
TR	39	TRIGGER: activated when the GET command is received over the interface or the FGET command is given by the MPU.
V_{cc}	40	Supply voltage (+5 V nominal).

RS-232

U251 is the integrated circuit that controls the RS-232 interface for the DAS. U251, an 8251A chip, is a Universal Synchronous/Asynchronous Receiver/Transmitter. Table 4-43 is a list of the pins in U251 and their functions.

Buffers U155A and B, U145C and D, and U151A, B, and C are line drivers to isolate the RS-232 chip from the outside world.

Table 4-43
8251A Pin Functions

Name	Pin	Function
D0 D1 D2 D3 D5 D6 D7	27 28 1 2 6 7 8	D0 through D7 are tri-state bidirectional data bits that interface between the data bus and the 8251A. Data, control words, command words, and status information is transmitted by these bits.
RxD	3	RECEIVE DATA: this pin receives the serial data input that the rest of the receiving converts to parallel data.
GND	4	GROUND: the ground reference voltage for the IC.
TxC(L)	9	TRANSMITTER CLOCK: controls the rate at which characters are transmitted.
WR(L)	10	WRITE: when LOW informs the 8251A that the CPU is writing data or control words to the 8251A.
CS(L)	11	CHIP SELECT: when LOW the IC becomes active.
C/[D(L)]	12	CONTROL/DATA: in conjunction with the WR(L) and RD(L) inputs, informs the 8251A whether the word on the data bus is a data character (low) or a control word or status information (high).
RD(L)	13	READ: when low this input informs the 8251A that the CPU is reading data or status information from the integrated circuit.
RxRDY	14	RECEIVER READY: this output indicates that the IC contains a character that is ready to be sent to the CPU.
TxRDY	15	TRANSMITTER READY: indicates to the CPU that the transmitter is ready to accept a data character.
SYNDET/BD	16	SYNC DETECT/BREAK DETECT: acts as either an input or an output. When used as an output, the pin goes high to indicate that the SYNC character has been located and identified. When used as an input, a positive-going signal causes the IC to start assembling data characters on the rising edge of the next RxC(L) signal.
CTS(L)	17	CLEAR TO SEND: a low to this input enables transmission of serial data if the TxEnable bit in the command byte is set to a logic 1.
TxEMPTY	18	TRANSMITTER EMPTY: when the IC has no characters to transmit, this output goes high.
TxD	19	TRANSMITTER DATA: this pin outputs the serial data and control words from the IC.
CLK	20	CLOCK: this input is used to generate internal timing. No external inputs or outputs are referenced to CLK.

Table 4-43 (cont)
8251A Pin Functions

Name	Pin	Function
RESET	21	RESET: a high on this input forces the IC into an idle mode.
DSR(L)	22	DATA SET READY: this is a general-purpose one-bit inverting input port.
RTS(L)	23	REQUEST TO SEND: this is a general-purpose one-bit inverting output port.
DTR(L)	24	DATA TERMINAL READY: this is a general-purpose one-bit inverting output port.
RxC(L)	25	RECEIVER CLOCK: this input controls the rate at which the serial data is to be received.
V_{cc}	26	Supply voltage (+5 volts nominal).

I/O INTERFACE VIDEO DRIVER 

NOR gates U145A and B form a composite video signal from the HORZ SYNC, VERT SYNC, and VIDEO(L) signals. Transistor Q139 is the final driver for the COMPOSITE VIDEO output.

I/O INTERFACE CONNECTOR 

The I/O Connector is a sub-assembly of Option 02, the I/O Interface. The assembly number of the I/O connector is A19A2. This sub-assembly is attached to the back panel of the DAS mainframe. It holds the GPIB connector, the RS-232 connector, and the composite video connector for the I/O Interface.

The I/O connector also holds four LEDs that indicate the GPIB status and a set of DIP switches to select the DAS's Talker/Listener address on the GPIB and to select the type of terminal the DAS is communicating with.

OPTION 03

Option 03 is a single +5 Volt Power Supply for use in the DAS Mainframe. Refer to the +5 Volt Power Supply circuit description for more detailed information about Option 03.

OPTION 04

Option 04 consists of two +5 Volt Power Supplies for use in the DAS Mainframe. Refer to the +5 Volt Power Supply circuit description for more information about Option 04.

OPTION 05

Option 05 consists of the hardware necessary to rackmount a DAS.

VERIFICATION & ADJUSTMENT PROCEDURES 5

VERIFICATION & ADJUSTMENT PROCEDURES

INTRODUCTION

NOTE

Unless otherwise specified, the material in this section applies to all DAS 9100 Series instruments. Material applicable only to the monochrome (DAS9109) or color (DAS9129) mainframes is identified.

This section of the manual contains three main parts: the functional check procedures, the adjustment procedures, and the performance check procedures. These parts, along with the test setup information at the beginning of this section, should allow a qualified technician to bring into adjustment and verify the operation of any DAS 9100 mainframe, mainframe sub-assembly, instrument module, probe, or option to the DAS 9100 Series.

NOTE

Throughout this manual the term verification is used to mean either a functional check or a performance check.

Functional Check Procedures. These tests verify that the device being functionally tested is basically operational. The procedure exercises the main user interfaces of the device to verify their operation and checks the main internal features. These tests can be used to determine whether adjustment and/or repair is necessary.

Adjustment Procedures. These instructions for setting variables should bring the device being adjusted to or within product specifications. If the instrument module, mainframe sub-assembly, probe, or option cannot meet the specifications given in this manual after adjustment, repair is necessary.

Performance Check Procedures. These tests provide a detailed check of internal and external product characteristics. All specifications listed in the performance requirement column of the specifications are verified. These checks can be extensive and time consuming. Under normal circumstances the functional check procedures provide an adequate test of product performance in a less costly or time consuming manner.

TEST SETUP INFORMATION

The procedures in this Verification and Adjustment Procedures section require some test setups and general information relevant only to the DAS 9100 Series. This information is presented here at the front of the section to prevent duplication throughout the following procedures.

NOTE

Due to space limitations, not all DAS test setup information can be presented here. For questions regarding operation or disassembly that are outside the scope of this section, refer to the Operating Information or the Maintenance: General Information sections of this manual.

SUGGESTED TEST INSTRUMENTS

There are three different sets of procedures in this section: the functional check, the adjustments, and the perfomance check. Below are lists of instruments that are used at some point in each of these procedures, along with their Tektronix equivalents.

NOTE

Each separate procedure will only use some of the instruments given in these tables. Check the procedure in question before appropriating test instruments.

Table 5-1
Equipment Needed For The Functional Check Procedures

Equipment	Specifications	Equivalent Tektronix Instrument
DAS 9100 mainframe	No substitute allowed	
DAS 9100 Service Maintenance Kit	No substitute allowed	
Digital multimeter	3.5 digits, 0.1% dc volts accuracy	DM 502A
Oscilloscope with probe	50 kHz bandpass	2213
Pulse or square wave generator	1 MHz pulse rate, min. Output swing between +5 V and ground.	PG 502
91A32 Data Acquisition Module	No substitute allowed	
91A08 Data Acquisition Module	No substitute allowed	
91P16 Pattern Generator Module	No substitute allowed	
Diagnostic Lead Set	No substitute allowed	Tektronix Part number 012-1000-00
P6452 External Clock Probe	No substitute allowed	
P6452 Data Acquisition Probe	No substitute allowed	
P6454 100 MHz Clock Probe	No substitute allowed	

Table 5-1 (cont)
Equipment Needed For The Functional Check Procedures

Equipment	Specifications	Equivalent Tektronix Instrument
P6455 TTL/MOS Pattern Generator Probe	No substitute allowed	
Formatted DC100-type tape cartridge with no data stored	No substitute allowed	Tektronix part number 119-1350-00 (unformatted)
TEKTRONIX 4051 Desktop Computer with Option 01 Installed	No substitute allowed	
RS-232 cable		Tektronix part number 012-0815-00
GPIB cable	IEEE 488-1978	Tektronix part number 012-0630-03
Special purpose null modem	Hand constructed, schematic included.	None

Table 5-2
EQUIPMENT NEEDED FOR THE ADJUSTMENT PROCEDURES

Equipment	Specifications	Equivalent Tektronix Instrument
DAS 9100 mainframe	No substitute allowed	
DAS 9100 Service Maintenance Kit	No substitute allowed	
DAS formatted DC 100-type data cartridge	No substitute allowed	Tektronix part number 119-1350-00 (unformatted)
Two-channel oscilloscope with probes	350 MHz	485
Digital multimeter	3.5 digits, 0.1% dc volts accuracy	DM 502A
Pulse generator	250 MHz pulse rate, variable output levels	PG 502
50 Ω termination for the above pulse generator		
Standard slotted screwdriver		
Small slotted screwdriver		
Long Shank (9 inch min.) POZIDRIVE type magnetic screwdriver		
Small-plastic bladed, slotted screwdriver		
Plastic alignment tool		
Ruler or tape measure		
Wire strippers		
Soldering iron		
Solder		

Table 5-3
EQUIPMENT NEEDED FOR THE PERFORMANCE CHECK PROCEDURES

Equipment	Specifications	Equivalent Tektronix Instrument
DAS 9100 mainframe	No substitute allowed	
DAS 9100 Service Maintenance Kit		
DAS Setup/Hold Time Test Fixture		Tektronix part number 067-1037-00

Table 5-3 (cont)
EQUIPMENT NEEDED FOR THE PERFORMANCE CHECK PROCEDURES

Equipment	Specifications	Equivalent Tektronix Instrument
TM 500 Mainframe		
Two-channel oscilloscope with probes	350 MHz	485
Digital multimeter	3.5 digits, 0.1% dc volts accuracy, 1% ac volts accuracy	DM 502A
Pulse generator	250 MHz pulse rate, variable output levels	PG 502
Sine wave generator	Variable frequency up to 200 MHz with variable output	SG 503
5 V Power Supply	2 A output	
Dual Variable DC Power Supply	300 mA output from both outputs	PS 503A
91A32 Data Acquisition Module	No substitute allowed	
91A08 Data Acquisition Module	No substitute allowed	
91P16 Pattern Generator Module	No substitute allowed	
Diagnostic Lead Set	No substitute allowed	Tektronix part number 012-1000-00
P6452 External Clock Probe	No substitute allowed	
P6452 Data Acquisition Probe	No substitute allowed	
P6454 100 MHz Clock Probe	No substitute	
P6455 TTL/MOS Pattern Generator Probe	No substitute allowed	
50 Ω coaxial cable with male BNC connectors on the ends		
BNC female to BNC female adapter		Tektronix part number 103-0028-00
BNC male to dual binding post		Tektronix part number 103-0033-00
BNC T		Tektronix part number 103-0030-00
Bayonet ground assembly		Tektronix part number 013-0085-00
Termination, 50 Ω		Tektronix part number 011-0049-01
50 Ω 5X attenuator		Tektronix part number 011-0060-02
Ten 1.5 kΩ resistors	5% accuracy, 1/4 W	
Ten 50 Ω resistors	5% accuracy, 1/4 W	
2.2 pF	200 V	
Graph paper Straight edge		

USING THE DIAGNOSTIC LEAD SET

Included in the DAS Service Maintenance Kit is a special lead set called the Diagnostic Lead Set. This lead set can be used to connect any pattern generator probe to a data acquisiton probe to acquire pattern generator data. This lead set is often used in verification procedures to simplify the task of connecting a pattern generator probe to a data acquisition probe.

Connecting the Probes

Figure 5-1 illustrates how pattern generator and acquisition probes are connected using the Diagnostic Lead Set. Make sure all the following conditions are true.

- The data acquisition ground lead from the diagnostic lead set is connected to the GND DIAGNOSTIC location.
- The pattern generator ground lead from the diagnostic lead set is connected to the V_L location if using a P6455 TTL/MOS probe, or to the V_H location if using a P6456 ECL probe.

NOTE

If you are using a P6456 ECL Pattern Generator probe, you must enter the Channel specification menu and set the data acquisition probe's threshold to variable (– 1.30 V).

- The recessed threshold range switch on the data acquisiton probe is set to NORM.
- The recessed diagnostic switch on the pattern generator probe is set to AUX.

Connecting the Strobe to the Qualifier

With some tests, the strobe line of the Diagnostic Lead Set (the white flying lead on the pattern generator side) must be connected to the qualifier line (the white flying lead on the acquisition side). These two leads are best connected by square pins. The leads may also be connected using any appropriate piece of conductive wire, like a piece of transistor lead, or by putting gripper tips on the ends and hooking the gripper tips together.

Special Rules

If you modify any of the functional tests that use the Diagnostic Lead Set, be aware of the following restrictions:

- The Diagnostic Lead Set cannot operate at clock rates less than 1 μs. Be sure to set both the acquisition and pattern generator clock rates accordingly.
- Acquisition modules using the Diagnostic Lead Set will not recognize a tri-state condition (from the pattern generator) because there are no pull-up or pull-down resistors. Data read during a tri-state condition depends entirely upon the previous data.

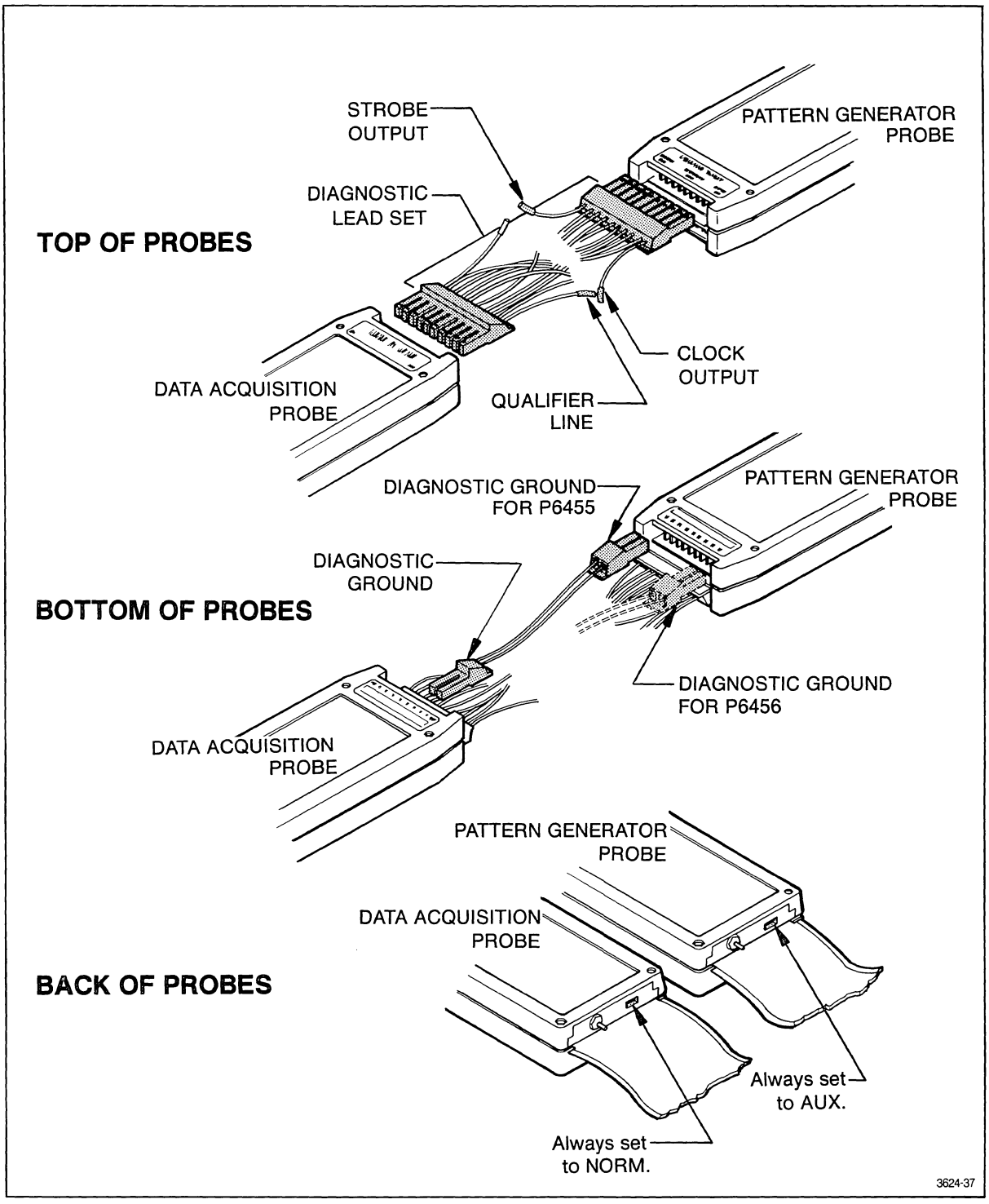


Figure 5-1. Connecting the Diagnostic Lead Set.

CONNECTING CLOCK PROBES TO THE DIAGNOSTIC LEAD SET

At many times in the functional check procedures, a clock or strobe from the pattern generator must be connected to a line on the External Clock Probe of the Trigger/Time Base or to the 100 MHz Clock Probe of a 91A08 module. For example, the pattern generator strobe could control the pattern generator interrupt, or the pattern generator clock output could be used to perform synchronous acquisition.

Connecting the External Clock Probe to the Diagnostic Lead Set

Figure 5-2 illustrates how to connect lines between the pattern generator side of the diagnostic lead set and the External Clock Probe. The pattern generator's output clock lead (gray flying lead from the pattern generator side of the Diagnostic Lead Set) or the pattern generator's strobe lead (the white flying lead from the pattern generator side of the lead set) may be connected to any of the External Clock Probe leads.

The two flying leads are best connected by square pins. Otherwise, these leads may also be connected using any appropriate piece of conductive wire, like a piece of transistor lead, or by putting gripper tips on the ends and hooking the gripper tips together.

NOTE

It is very important to connect the grounds between all three probes in order to acquire accurate data and control signals.

The ground connection between the data acquisition probe and the pattern generator probe is already made by the Diagnostic Lead Set. The external clock probe, however, must have special connections made for a solid ground. Procedures for grounding the External Clock Probe are given below.

1. Insert a Pomona-type grounding clip in the GND DIAGNOSTIC position of the External Clock Probe.

2. Insert a Pomona-type grounding clip in one of the GND SENSE positions of the data acquisition probe.

3. Connect these two Pomona clips.

The External Clock Probe is now grounded properly.

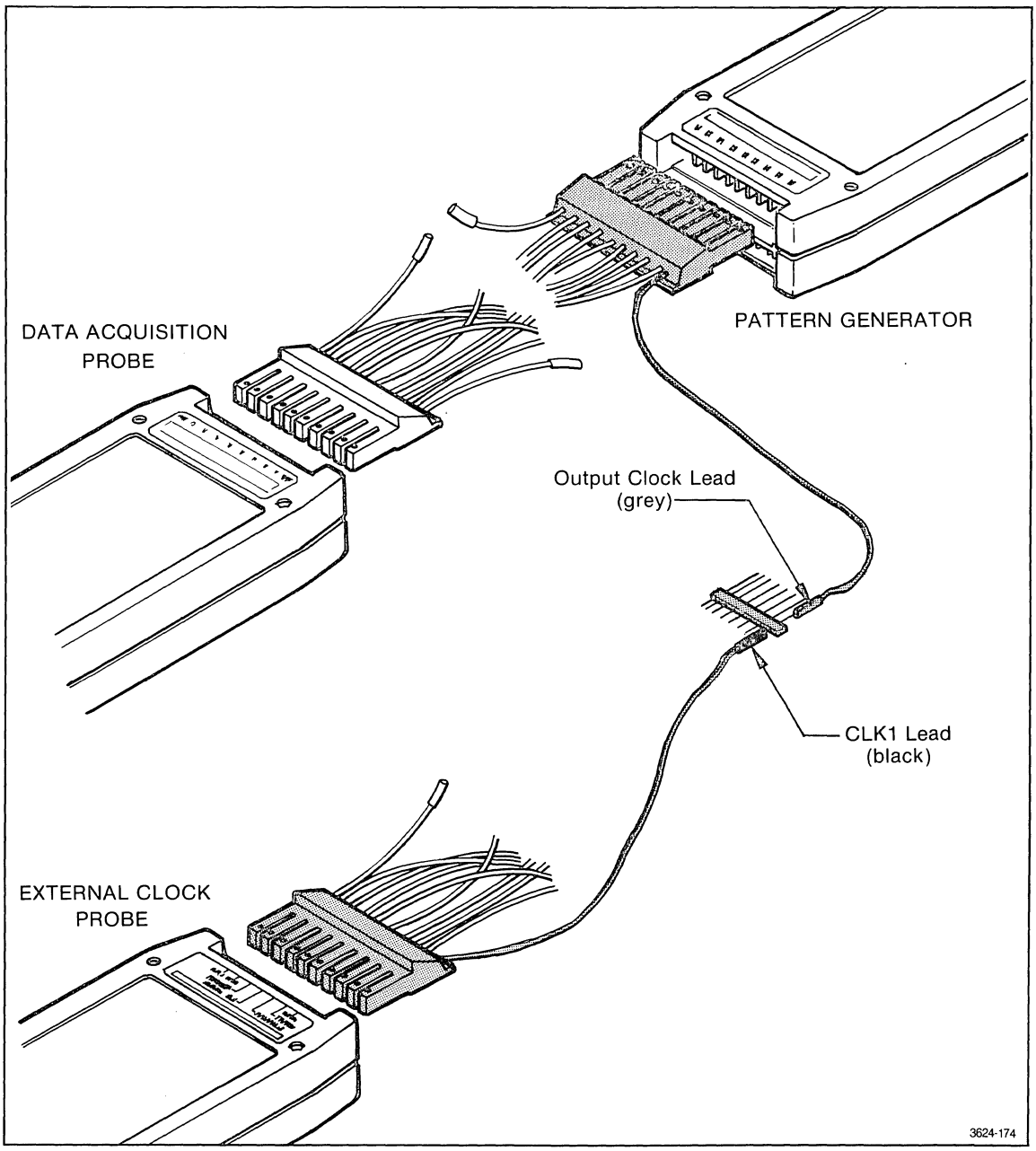


Figure 5-2. Connecting the External Clock Probe to the Diagnostic Lead Set.

Connecting the 100 MHz Clock Probe to the Diagnostic Lead Set

The 100 MHz Clock Probe has two inputs, a clock input and a ground sense input. These inputs are labeled on the probe housing. During some procedures involving the 91A08, the pattern generator's output clock lead (gray flying lead from the pattern generator side of the Diagnostic Lead Set) or the pattern generator's strobe lead (the white flying lead from the pattern generator side of the lead set) may be connected to the clock input of the 100 MHz Clock Probe.

Two flying leads are best connected with square pins. These leads may also be connected using any appropriate piece of conductive wire (like a piece of transistor lead) or by putting gripper tips on the ends and hooking the gripper tips together.

NOTE

It is very important to connect the grounds between all three probes to acquire accurate data and control signals.

The ground connection between the data acquisition probe and the pattern generator probe is already made by the Diagnostic Lead Set. The 100 MHz Clock Probe, however, must have special connections made for a solid ground. Procedures for grounding the 100 MHz Clock Probe are given below.

1. Connect a gripper tip to the REF location of the P6454 100 MHz Clock Probe.
2. Insert a Pomona-type grounding clip in one of the GND SENSE positions of the data acquisition probe.
3. Connect these two clips.

The 100 MHz Clock Probe is now grounded properly.

USING THE DAS MAIN EXTENDER

The main extender board in the DAS 9100 Service Maintenance Kit is used in some of the adjustment and performance check procedures. The board elevates the module being tested or adjusted to a convienient level above the mainframe, so test points and components are accessible.

Signal Test Points and Jumpers

Each instrument module has an A side and a B side. The B side of a module holds all of the components on the board, while the A side is the solder side. The main extender board has an A side and a B side also. Each side is labeled at the top and bottom of the board. The extender pulls A-side signals through to the B side, so all signals on the board are accessible in the same area. Each signal (on both the A side and B side) is passed through a two-pin terminal connector and a test point, then A side signals are routed back to the A side of the board.

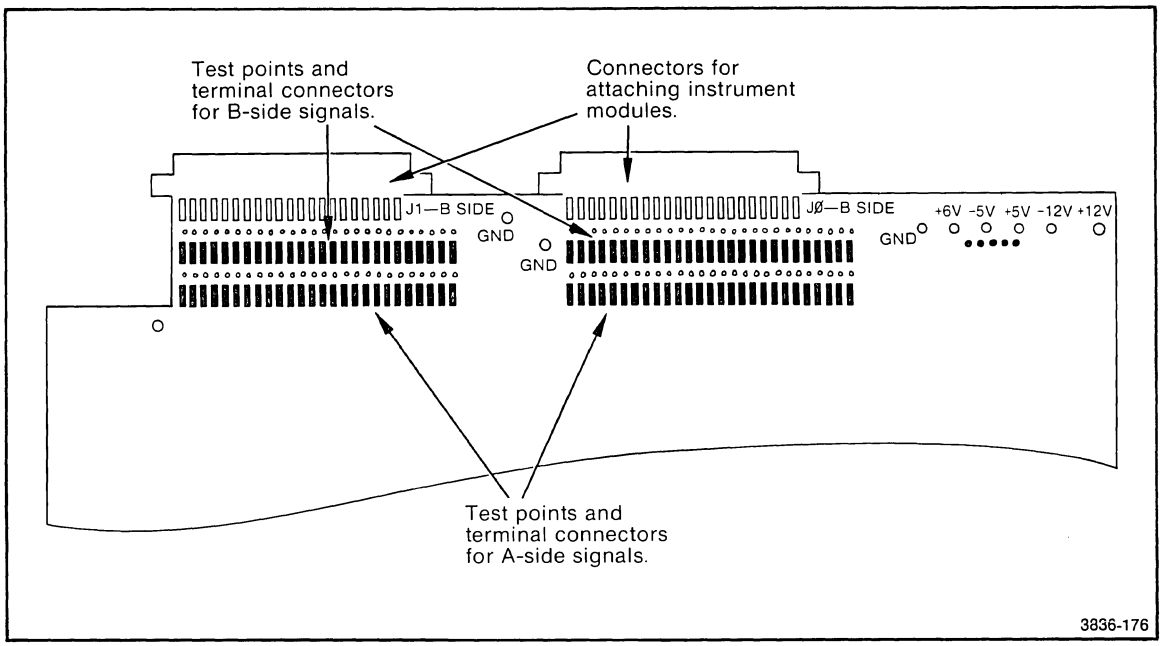


Figure 5-3. Main extender A-side and B-side terminal connectors and test points.

Signals can be prevented from leaving or entering the module being tested by removing the appropriate terminal connector. The signal lines are numbered beneath the row of A-side terminal connectors.

Figure 5-3 shows the rows of A-side and B-side terminal connectors and test points. Note the four ground connections.

Power Indicator Lights

Five red LEDs in the upper right corner of the extender board indicate the presence of +6 V, −5 V, +5 V, −12 V, and +12 V (left to right).

High-Speed Bus Buffers

High-speed instrument modules can operate while connected to the main extender board. Buffers located on the lower left side of the extender help isolate the extender stub from the high-speed bus lines. The termination of signals is changed, but not the signals themselves.

When testing or adjusting modules in mainframe bus slots 1 through 6, activate the buffers by placing the ten terminal connectors (located on the lower left side of the extender board) over the upper two pins. When adjusting or testing the Controller board or the Trigger/Time Base board (slots 0 and 7), place the terminal connectors on the lower two pins, since the bus is already terminated on the Interconnect at these two slots.

USING THE MAIN POWER SUPPLY EXTENDER

WARNING

Hazardous voltages are exposed during troubleshooting procedures involving this board. Use extreme caution.

Use the main power supply extender (in the DAS 9100 Series Service Maintenance Kit) when adjusting or testing the DAS Main Power Supply. The extender board elevates the board out of the mainframe to make test points and components accessible.

To adjust or test the DAS Main Power Supply, the supply must be removed from the mainframe, the extender for the supply must be installed, and the supply must be connected to the top of the extender.

For detailed instructions for removing the Main Power Supply, refer to the dissassembly procedures in the Maintenance: General Information section of this manual. While reading this procedure, refer to Figure 5-4, which illustrates the proper connection of the extender and supply.

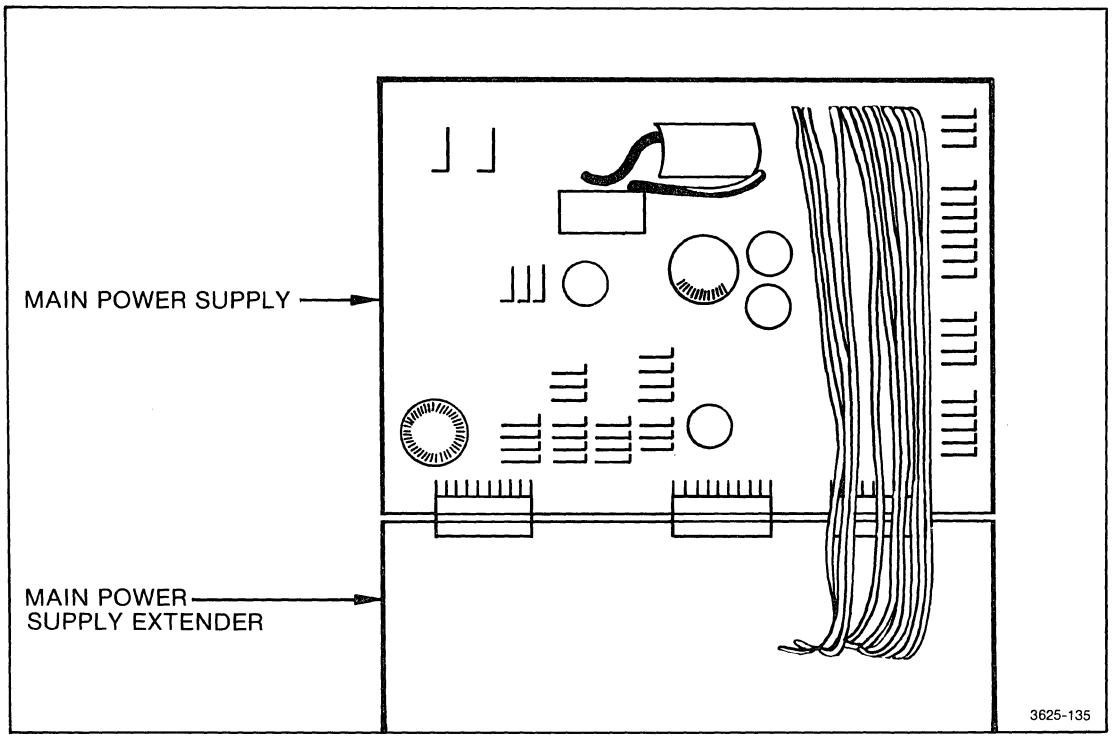


Figure 5-4. Connecting the Main Power Supply to the extender board.

The power supply is held in place in the mainframe with three screws underneath the left side-panel of the mainframe. This side panel (on the same side as the display monitor) must be slid off the mainframe to access these three screws.

The series pass sections of the DAS Main Power Supply have transistors mounted on a heat sink near the rear fan. These transistors are attached to the supply by cables. Remove the two connectors that attach these cables to the supply. It should now be possible to remove the supply entirely from the mainframe.

Insert the extender board in the mainframe in the same position the Main Power Supply occupied.

CAUTION

Make sure the connectors at the bottom of the extender mate properly with the pins protruding from the mainframe. If the extender is connected to either side of the proper position (one or more of the pins is not connected) the Main Power Supply may be damaged upon power-up.

The series pass transistors must now be connected to the extender board. There are two rows of pins on the upper right side of the main power supply extender board. Use the lower set of pins to connect the series pass transistors to the extender in the same way they were connected to the main power supply. (See Figure 5-4.)

Attach the DAS Main Power Supply to the top of the extender. Verify that the connectors and pins mate properly. Locate the pins on the Main Power Supply that were attached to the series pass transistors. Connect these pins to the pins on the main extender that are immediately above the transistor connectors. Perform the connection with the cables found in the DAS Service Maintenance Kit.

CAUTION

Do not twist the cables used to connect the DAS Main Power Supply to the extender board. Twisting the cables may destroy the transistors or other components of the power supply.

The extender and supply combination should now look identical to Figure 5-4. The DAS may now be powered up for adjustment or testing.

FUNCTIONAL CHECK PROCEDURES

The Functional Check Procedure verifies that all major sections of the product being checked are operational. These tests can be used to determine whether adjustment and/or repair is necessary.

The Functional Check Procedure is organized into sets of tests for each sub-system of the mainframe, each type of module, each type of probe, and finally a procedure for each option.

Refer to the beginning of this Verification and Adjustment Procedures section and to the Operating Information section of this manual for instructions on module installation, probe connections, use of menus, and use of the Diagnostic Lead Set.

NOTE

These procedures assume that the user has a moderate understanding of operation of the DAS menus and hardware.

MAIN POWER SUPPLY FUNCTIONAL CHECK

The functional check for the DAS Main Power Supply verifies the presence and accuracy of all voltages provided by the supply.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe (containing the Main Power Supply being tested)
- Main Extender Board (in the DAS Service Maintenance Kit)
- Digital multimeter (or any dc volt measuring device)
- Oscilloscope with probe

Refer to the Operating Information section of this manual for procedures covering installation of instrument modules. Refer to the beginning of this Verification and Adjustment Procedures section for instructions for installing the Main Extender Board.

(1) Setup for the Functional Check

The following procedures bring most of the voltages supplied by the Main Power Supply out of the mainframe so they can be measured. The procedure is designed so access to the power supply compartment of the mainframe is unnecessary.

1. Turn off the mainframe. Remove the Trigger/Time Base board from the mainframe.
2. Set the Main Extender Board to accept a Trigger/Time Base board. Install the extender in slot 7 of the mainframe.
3. Install the Trigger/Time Base on top of the extender.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so could cause damage to the module or sub-assembly.

(2) Verifying Voltage Accuracy

The following procedures check the accuracy of the power supply voltages.

1. Turn on the mainframe. The power-up self-test should pass. Examine the LEDs at the top foremost corner of the extender board. All LEDs should be lit; these indicate the presence of +12 V, +6 V, +5 V, −5 V, and −12 V.

2. Using the digital multimeter, verify the accuracy of the voltages present on the main extender board. The voltages on the main extender can be measured at the pins on the upper right-hand corner. The voltages should be within the following tolerances.

Supply Voltage	Tolerances
+12 V	+11.82 V to +12.18 V
+6 V	+5.82 V to +6.18 V
+5 V	+4.85 V to +5.15 V
−5 V	−5.15 V to −4.85 V
−12 V	−10.80 V to −13.20 V

3. Press the CHANNEL SPEC key. If the display changes to the Channel Specification menu, then the −12 V supply for the keyboard is present and sufficiently accurate to drive the keyboard.

(3) Verifying Maximum Voltage Ripple

The next steps verify that the voltage ripple on the various supplies are within the maximum ripple specification. The steps assume the voltage accuracy has just been verified, so the Trigger/Time Base is on an extender.

1. Disconnect the digital multimeter from the extender board.

2. AC couple the oscilloscope. Set the oscilloscope to a convenient scale for measuring 120 mV peak to peak.

3. Using the oscilloscope, verify that the ripple on any of the supply voltages does not exceed specifications. These voltages can be measured at the pins on the upper right-hand corner of the main extender board. The ripple should be less than or equal to the following tolerances.

Supply Voltage	Maximum Ripple
+12 V	120 mV p-p
+6 V	60 mV p-p
+5 V	50 mV p-p
−5 V	50 mV p-p
−12 V	120 mV p-p

This completes the Main Power Supply functional check. Turn off the DAS mainframe before removing the Trigger/Time Base or the Main Extender Board.

+5 V POWER SUPPLY FUNCTIONAL CHECK

The functional check for the +5 V Power Supply verifies the presence and accuracy of the voltage provided by the supply.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe (containing the +5 V supply to be tested)
- Main Extender Board (in the DAS Service Maintenance Kit)
- Digital multimeter (or any dc volt measuring device)
- Oscilloscope with probe
- Two DAS instrument modules

Refer to the Operating Information section of this manual for procedures covering installation of instrument modules. Refer to the beginning of this Verification and Adjustment Procedures section for instructions for installing the Main Extender Board.

(1) Setup for the Functional Check

The following procedures bring the voltage supplied by the +5 V Power Supply module out of the mainframe so they can be measured. The procedure is designed so that access to the power supply compartment of the mainframe is unnecessary.

1. Turn off the mainframe.
2. Set the Main Extender Board to accept a standard instrument module. Install the extender board in one of the slots powered by the +5 V supply being tested (see Figure 5-5).
3. Install one of the DAS instrument modules on top of the extender board. Install the other instrument module in the other slot powered by the +5 V supply (see Figure 5-5).

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

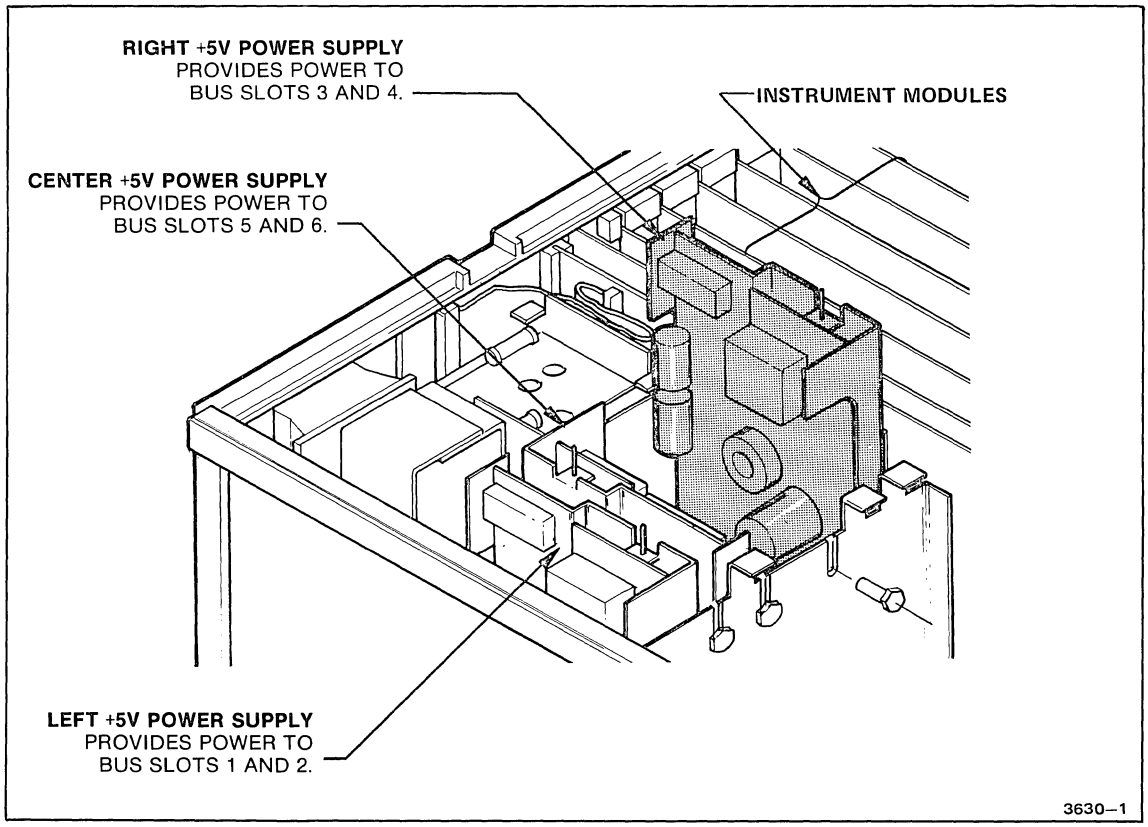


Figure 5-5. Bus slots powered by each +5 V Power Supply Module.

(2) Verifying Voltage Accuracy

The following procedures check the accuracy of the +5 V supply voltage.

1. Turn on the mainframe. The power-up self-test should pass. examine the LEDs at the top foremost corner of the extender board. All LEDs should be lit; these indicate the presence of +12 V, +6 V, −5 V, and −12 V (from the main power supply) and +5 V (from the supply being tested).

2. Using the digital multimeter, verify the accuracy of the +5 V supply. The voltage can be measured on the main extender board on the +5 V pin in the upper right-hand corner. The voltage should be between +4.85 V and +5.15 V.

(3) Verifying Maximum Voltage Ripple

The next steps verify that the voltage ripple on the supply is within the maximum ripple specification. These steps assume the voltage accuracy has just been verified, so the +5 V supply can be measured on the extender board.

1. Disconnect the digital mutimeter from the extender board.
2. AC couple the oscilloscope. Set the oscilloscope to a convenient scale for measuring 50 mV peak to peak.
3. Using the oscilloscope, verify that the ripple on the supply voltage does not exceed specifications. The voltage can be measured at the +5 V pin on the upper right-hand corner of the main extender board. The ripple should be less than or equal to 50 mV peak to peak.

This completes the +5 V Power Supply functional check. Turn off the mainframe before removing the Main Extender Board or any instrument modules.

KEYBOARD FUNCTIONAL CHECK

The functional check for the keyboard verifies the ability of the Controller board to detect each key properly.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe with the keyboard under test installed

Refer to the Operating Information section of this manual for instructions on use of the Diagnostics menu.

(1) Setup for the Functional Check

The following procedures get the user into the Diagnostics menu and then into the keyboard function in the Diagnostics. This diagnostic function will be used to verify the operation of the keyboard.

1. Turn off the mainframe. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.
2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 0, the Controller.
3. Select SINGLE mode and set the LOOPING field to ON. Then select to run function 0, the keyboard function, and start the test by pressing START SYSTEM.

(2) Verifying the Keys and LEDs

The following procedures verify the operation of the keys and LEDs on the keyboard.

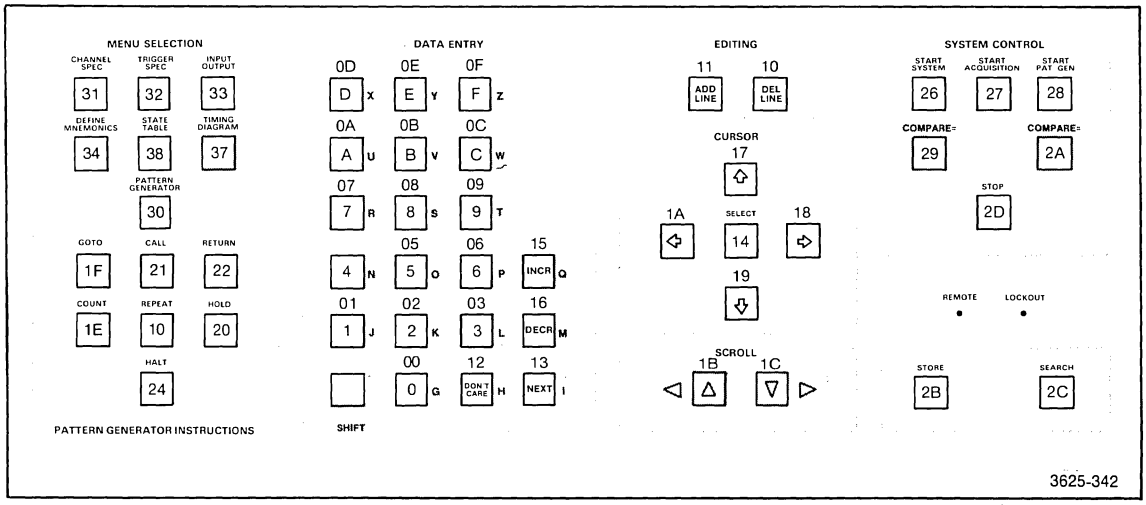


Figure 5-6. DAS keyboard hexadecimal codes.

1. There are two parts to the Keyboard function, test 0 and test 1. Press the SELECT key so test 1 is running (indicated in the blinking field).

2. Press all the keys on the keyboard except SHIFT, STOP, SELECT, and up-cursor. The Diagnostics menu should show FAIL for as long as each key is pressed. The display should also show the number that corresponds to the key being pressed (see Figure 5-6).

3. Note that whenever a key is pressed during this test, both LEDs on the keyboard light up. This verifies the operation of the LEDs.

4. Press the SHIFT key at the same time the 0 key is pressed. The display should show 40 in the key code field. This verifies the action of the SHIFT key.

5. Press the up-cursor key. The cursor should move to the FUNCTION select field. This verifies the up-cursor key.

The keyboard has now been verified. The STOP key was verified while causing the power-up self-test failure. The SELECT key was verified while altering the test selection fields. All other keys were verified in the Diagnostics menu.

MOTOROLA DISPLAY MONITOR FUNCTIONAL CHECK

The functional check for the Motorola Display Monitor checks the monitor for defects in the phosphor and verifies that the display is centered properly.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe with the Motorola Display Monitor under test installed

Refer to the Operating Information section of this manual for instructions in the use of the Diagnostics menu.

(1) Setup for the Functional Check

The following procedures get the user into the Display function in the Diagnostics menu. This diagnostic function will be used to verify the operation of the Motorola Display Monitor.

1. Turn off the mainframe. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 0, the Controller.

3. Select SINGLE mode, then select to run function 1; the Display function. Start the test by pressing START SYSTEM.

(2) Verifying the Display Centering

The following procedures check the screen display area for centering and possible rotation.

1. The screen should now show a border and cross hairs using the number 8. Verify that the border and cross hairs are centered on the CRT screen.

2. Still observing the display area, verify that the cross hairs are not tilted with respect to the physical mainframe.

(3) Checking for Phosphor Defects

The next steps check the CRT screen for burned-out or defective areas.

1. Press the SELECT key. The display should show a green area everywhere a character might appear.

2. Examine the screen for dark spots in the green fields. A dark spot indicates a flaw in the screen phosphor.

Press STOP to exit the test. This completes the functional check for the Motorola Display Monitor.

COLOR DISPLAY MONITOR FUNCTIONAL CHECK

The functional check for the color display monitor verifies that the display is properly centered, and that all combinations of characters and colors are legible.

You will need the following equipment to perform this procedure:

- DAS9129 Mainframe with the color monitor under test installed.

Refer to the Operating Information section of this manual for instructions on the use of the Diagnostics menu.

(1) Setup for the Functional Check

The following procedures get the user into the DISPLAYS function of the Diagnostics menu. This diagnostic function will be used to verify the operation of the color display monitor.

1. Turn off the mainframe. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 0, the Controller.

3. Select SINGLE mode, then select to run function 1; the DISPLAYS function. Start this test by pressing START SYSTEM.

(2) Verifying the Display Centering

The following procedures check the screen display area for centering and possible rotation.

1. The screen should now show a border and cross hairs using the number 8. Verify that the border and cross hairs are centered on the CRT screen within 3.2 mm (1/8 inch).

2. Still observing the display area, verify that the cross hairs are not tilted with respect to the physical mainframe. The maximum allowable tilt should be about 1/2 character from one side of the screen to the next.

(3) Checking Red Phosphor Defects

The DAS self-diagnostics verify the red phosphor. Yellow and green are not checked.

1. Press the SELECT key. The display should show a red area everywhere a character might appear.

2. Examine the screen for unusually dark or bright spots in the red fields. These spots indicate flaws in the screen phosphor.

(4) Checking Legibility

The last part of the functional check verifies the legibility of all characters in all the available colors and attributes.

1. Press the SELECT key. The display should now show all possible display characters in all available colors.

2. Compare the intensity of some green characters to the intensity of some yellow characters. This is easiest on the reverse video characters. The intensity of the yellow and the green characters should be about the same.

3. Compare a yellow character on a red background to a yellow character with no background. The color of both characters should be the same.

4. Turn the rear panel intensity control up to maximum. The background raster should not become visible and the display should remain stable (not dim and flickering).

5. Turn the intensity control down to minimum. The characters on the screen should remain visible.

6. Return the rear panel intensity control to a comfortable intermediate setting. Press STOP to exit the test.

This completes the functional check of the color display monitor.

CONTROLLER FUNCTIONAL CHECK

The functional check for the Controller board verifies that the Controller can bring a DAS 9100 system up to operation and can generate all possible characters for the display monitor.

You will need the following equipment to perform this procedure:
- DAS 9100 Mainframe with the Controller board to be tested installed in slot 0.

Refer to the Operating Information section of this manual for instructions on module installation and on use of the Diagnostics menu.

(1) Setup for the Functional Test

The following procedures get the user into the DISPLAYS function in the Diagnostics menu. This diagnostic function will be used to verify the operation of the Controller interface to the display monitor.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the mainframe. If the Controller to be tested is not currently installed in the mainframe, install it now.

2. Turn on the mainframe while holding the 0 key down. This will cause the power-up self-test to fail.

3. When all the modules in the mainframe have finished their power-up self-test, verify that the module vs slot readout on the screen reflects the actual order of the modules in the mainframe.

NOTE

At this point, the Controller board has passed its power-up self-test (except for the keyboard). This self-test verifies that the system RAM and ROM are operating and that the modules can be written to and read from.

4. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 0, the Controller.

5. Select SINGLE mode, then select to run function 1; the DISPLAYS function. Start the test by pressing START SYSTEM.

(2) Checking the User Interface

The next steps check the ability of the Controller to generate each possible character and display attribute and operate the beeper.

1. Press the SELECT key twice. The video screen should show a display of all possible characters and attributes. The display should be like Figure 5-7.

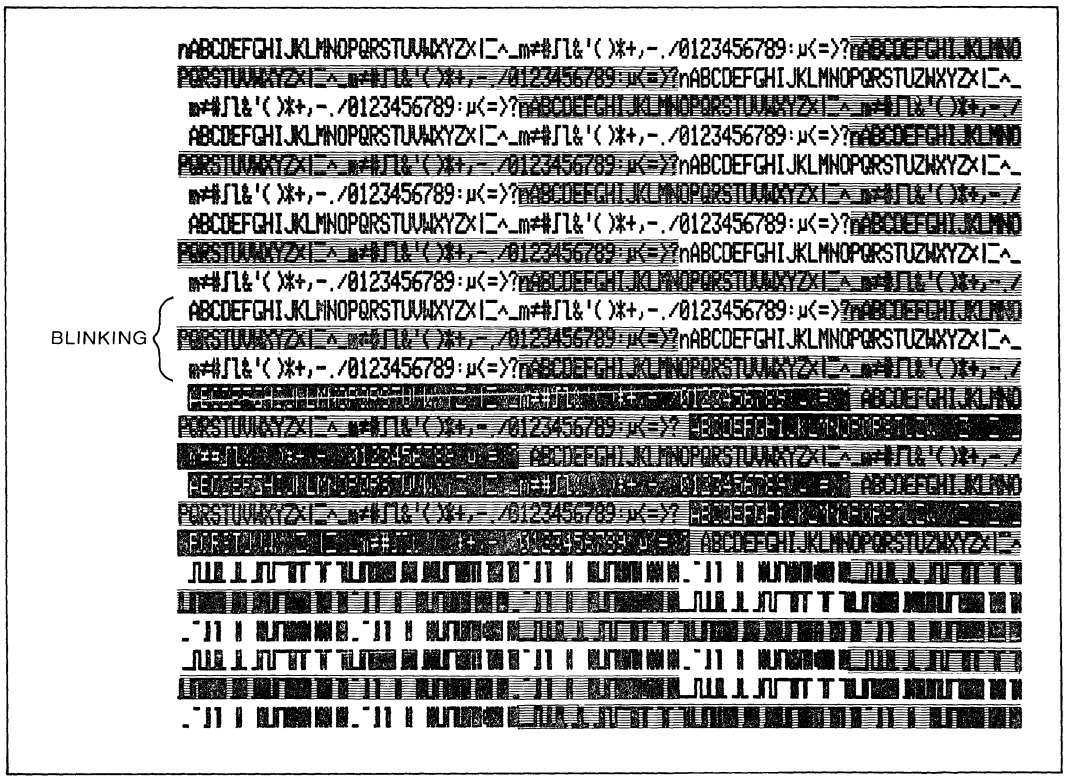


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Figure 5-7. Result of the DISPLAY function.

NOTE

If you have a color display monitor in your DAS mainframe (DAS9129 configuration), also verify that all possible character/color combinations are displayed. The display should include:

- Yellow characters, normal and reverse video
- Green characters, normal and reverse video
- Yellow characters on a red background
- Yellow waveforms with green glitches

2. Press STOP to exit the diagnostic function.
3. Press the INCR key. The beeper should sound. This verifies the operation of the beeper on the Controller board.
4. Pressing the INCR key should cause the message ENTER IN HEX to appear on the screen. Verify that the letters of the message are legible against the background field, but that the background is still bright enough to draw attention.

This completes the functional check procedure for the Controller board.

TRIGGER/TIME BASE FUNCTIONAL CHECK

NOTE

If you have a system to check that contains a 91P16 and/or a 91A32, use it/them in this functional check procedure. Parts of the 91P16 and 91A32 functional tests are duplicated in the tests for the Trigger/Time Base. Using them now will shorten the time required to check the functionality of these modules.

The functional check verifies the operation of the internal clocks, the various triggering modes, and the control lines from the External Clock probe.

The Trigger/Time Base module's function is to control instrument modules while they are operating at speed. Because of this, the Trigger/Time Base must be tested in conjunction with at least one acquisition module and a pattern generation module.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe with the Trigger/Time Base board to be tested installed in slot 7.
- P6452 External Clock Probe with acquisition lead set
- 91P16 Pattern Generator Module
- P6455 TTL/MOS Pattern Generator Probe
- 91A32 Data Acquisition Module
- P6452 Data Acquisition Probe
- Diagnostic Lead Set
- Pulse or square-wave generator

If available, add the following:

- 91A32 Data Acquisition Module (used to check split clock acquisition).

Refer to the Operating Information section of this manual for instructions on module installation and on use of the Diagnostics menu. Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes using the Diagnostic Lead Set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe for this functional check. If, due to insufficient +5 V power supply modules or some other constraint, the mainframe is not configured in the recommended way, then steps later in the functional check will need modification. For the greatest ease in following the functional check procedure, configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the DAS mainframe.

1. Turn off the mainframe. If the Trigger/Time Base board is not yet in the mainframe, install it in slot 7 at this point.

2. Install the 91P16 Pattern Generator module in slot 1 of the mainframe.

NOTE

The mainframe will not operate if there is more than one Trigger/Time Base or more than one 91P16 Pattern Generator module installed at the time of power-up. Before power-up, make sure there are no duplicates in the mainframe.

3. Install the 91A32 Data Acquisition module in slot 2. (If your system contains a 91A32 module to be functionally checked, install it in this slot. This will save time on the 91A32 functional check later on.)

4. If a second 91A32 module is available, install the second module in slot 3.

(2) Executing the Diagnostic Self-Test

The next steps run all available self-test diagnostics on the Trigger/Time Base board.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 7, the Trigger/Time Base.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. The diagnostic tests WR&SEQ, A COUNTER, DELAY, 91A32 GEN, 91A32 SEL, and 91A08 GEN, should all pass. (The DAC THRSH test does not have internal read back, so it can neither pass nor fail.)

(3) Setup of the Probes for the Functional Check

These steps provide the initial probe setup for these tests. This probe organization will go through a series of permutations as the functional check continues.

As a side effect of connecting the probes, the interface between the Trigger/Time Base and the P6452 External Clock probe is verified.

NOTE

For further details on connecting probes with the Diagnostic Lead Set, refer to the beginning of this Verification and Adjustment Procedures section.

1. Connect the TTL/MOS pattern generator probe to pod connector B of the 91P16. Set the diagnostic slide switch on the back of the probe to AUX.

2. Connect the data acquisition probe to pod connector A of the 91A32 in slot 2. Connect these two probes (currently connected to the back of the DAS) using the Diagnostic Lead Set.

3. Connect the P6452 External Clock probe to pod connector C of the Trigger/Time Base. When this probe is installed, the mainframe should beep and the message POD 7C CONNECTED should show on the screen.

4. Press the Pod ID button on the back of the P6452 External Clock probe housing. The mainframe should beep again and the message POD 7C should appear on the screen.

5. Install a flying lead set in the P6452 External Clock probe. Also install a ground lead in the diagnostic ground connector on the probe.

6. Install a ground lead in one of the GND SENSE connectors of the P6452 Data Acquisition probe. Connect the ground lead of the clock probe to the ground lead of the data acquisition probe.

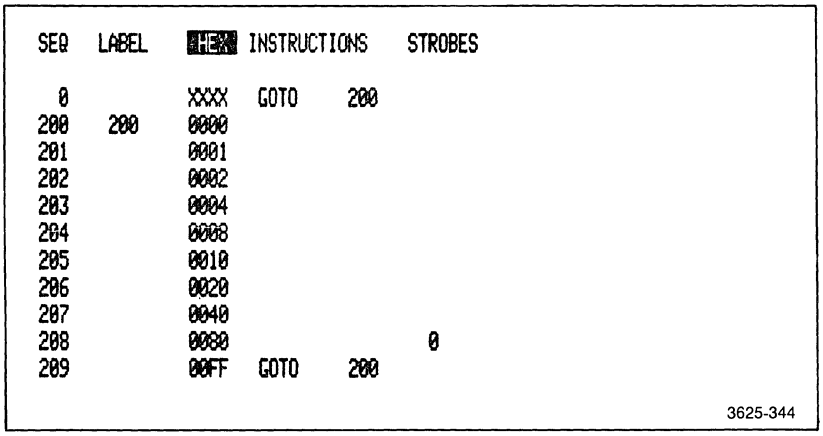
The above steps provide the basic connections for the three probes being used. The next step sets up the probes to perform the next set of tests.

7. Connect the strobe lead from the pattern generator probe (the white flying lead) to the PG INHIBIT lead from the P6452 External Clock probe (the red lead).

(4) Verifying the PG INHIBIT Line

The next steps verify the transmission of the PG INHIBIT signal through the External Clock probe.

1. Leave the Diagnostics menu by pressing the PATTERN GENERATOR key. Set the INHIBIT field in the Pattern Generator Program menu to 0. Adjust the program that is already present to match the following display.



2. Enter the Pattern Generator Timing menu and set strobe 0 to the following state:

3. Press START SYSTEM to start data acquisition.

4. When data acquisition is finished, enter the Timing Diagram menu. Adjust the Timing Diagram display to show the data acquired through pod 2A and set the magnification to 10. The display should look like Figure 5-8.

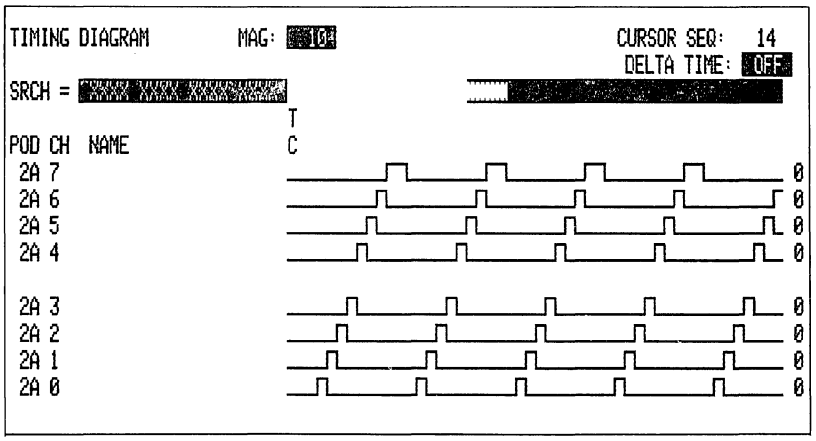
A display like Figure 5-8 indicates that the inhibit signal is being received by the Trigger/Time Base. The next steps verify the operation of the inversion of the inhibit signal.

5. Enter the Pattern Generator Program menu and set the INHIBIT field to 1.

6. Enter the Pattern Generator Timing menu and set the SHAPE field of strobe 0 to high true.

7. Press START SYSTEM.

8. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-8.



3625-137

Figure 5-8. Trigger/Time Base inhibit test results.

(5) Verifying the PG PAUSE Line

The next steps verify the transmission of the PG PAUSE signal through the External Clock probe.

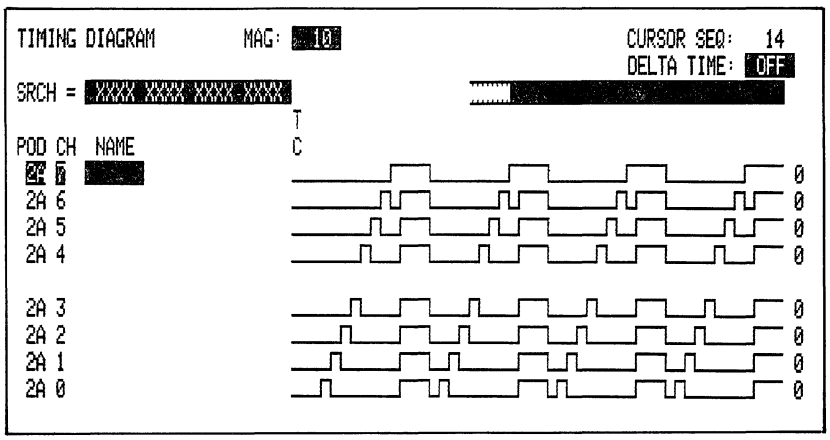
1. Disconnect the strobe line from the inhibit line. Reconnect the strobe line to the PG PAUSE line of the External Clock probe. This is done by reconnecting the white strobe line to the yellow PG PAUSE line.

2. Enter the Pattern Generator Program menu and set the PAUSE field to 0.

3. Enter the Pattern Generator Timing menu and set the SHAPE of strobe 0 to low true.

4. Press START SYSTEM.

5. The data acquired from the pattern generator, when displayed on the Timing Diagram menu, should look like the data shown in Figure 5-9.



3625-138

Figure 5-9. Trigger/Time Base pause test results.

A display like Figure 5-9 means the pause signal is being properly received and reacted to. Note in particular that the FF value is three times the width of the other data.

The next steps verify the operation of the inversion of the pause signal.

6. Enter the Pattern Generator Program menu and set the PAUSE field to 1.

7. Enter the Pattern Generator Timing menu and set the SHAPE of strobe 0 to high true.

8. Press START SYSTEM.

9. Enter the Timing Diagram menu when acquisition is finished. The display should again match Figure 5-9.

(6) Verifying the PG INTERRUPT Line

The next steps verify the transmission of the PG INTERRUPT signal through the External Clock probe.

1. Disconnect the strobe line from the pause line. Reconnect the strobe line to the PG INTERRUPT line of the External Clock probe. This is done by reconnecting the white strobe line to the orange PG INTERRUPT line.

2. Enter the Pattern Generator Program menu. Set the CALL field in the Pattern Generator menu to call TEST on a falling edge.

3. Set the pattern generator program to match the following display.

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0		XXXX	GOTO	200	
200	200	0000			0
201		0001			
202		0002			
203		0004			
204		0080			
205		00FF	GOTO	200	
206	TEST	0008			
207		0010			
208		0020			
209		0040	RETURN		

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4. Enter the Pattern Generator Timing menu. Set the shape of strobe 0 to low true.

5. Press START SYSTEM.

6. The data acquired from the pattern generator, when displayed on the Timing Diagram menu, should look like the data shown in Figure 5-10.

A display like Figure 5-10 means the interrupt signal is being properly received and processed. The next steps verify the operation of the inversion of the interrupt signal.

7. Enter the Pattern Generator Program menu and set the CALL field to call TEST on a rising edge.
8. Enter the Pattern Generator Timing menu and set the SHAPE of strobe 0 to high true.
9. Press START SYSTEM.
10. When acquisition is finished, again enter the Timing Diagram menu. The data acquired should look like Figure 5-10.

(7) Verifying the PG CLK Line

The next steps verify the transmission of the PG CLK signal through the External Clock probe. These steps require the use of an external clock source. The recommended clock source is a square wave or pulse generator with an output that swings between ground and +5 V.

1. Disconnect the strobe line from the interrupt line.
2. Connect the clock output from the pattern generator probe (the gray lead on the pattern generator side of the Diagnostic Lead Set) to the CLK1 line on the External Clock probe (the black lead).
3. Connect the output of the signal generator to the PG CLK line (brown) on the P6452 External Clock probe.
4. The signal generator must have a common ground with the probes. To accomplish this, connect the ground of the signal generator to the two clips that connect the data acquisition probe ground sense to the External Clock probe ground line.

The probes and the signal generator are now connected so the test can be performed.

5. Enter the Pattern Generator Program menu. Set the pattern generator clock to external rising edge. Set the CALL field to X (don't care).
6. Adjust the pattern generator program to match the following display.

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0		XXXX	GOTO	200	
200	200	0000			0
201		0001			
202		0002			0
203		0004			
204		0008			0
205		0010			
206		0020			0
207		0040			
208		0080			0
209		00FF	GOTO	200	

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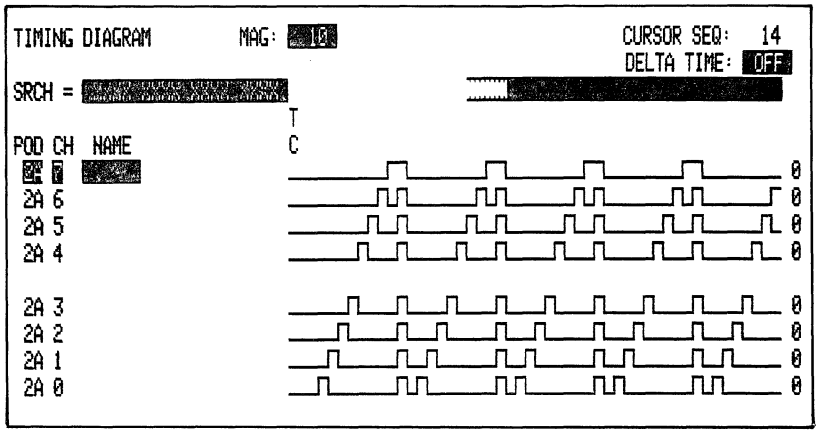


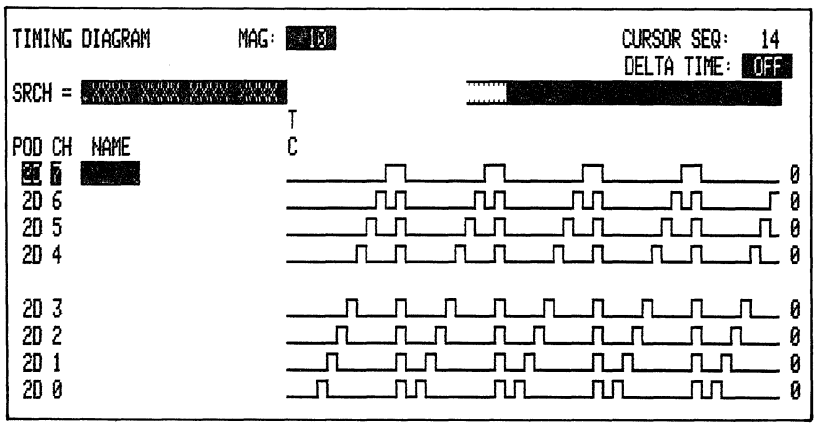
3625-139

Figure 5-10. Trigger/Time Base interrupt test results.

7. Enter the Trigger Specification menu and set the acquisition clock to external rising edge.

8. Press START SYSTEM.

9. When acquisition is finished, examine the Timing Diagram menu. The data acquired from the Pattern Generator should look like the data shown in Figure 5-11.



3625-140

Figure 5-11. Pattern generator external clock line test results.

A display like Figure 5-11 means the pattern generator external clock is being properly received and processed. The next steps verify the operation of the inversion of the external clock signal.

10. Enter the Pattern Generator Program menu and set the pattern generator clock to external falling edge.

11. Press START SYSTEM.

12. When acquisition is finished, examine the Timing Diagram menu. The data acquired from the Pattern Generator should again look like the data shown in Figure 5-11.

This finishes the tests of the external pattern generator control signals and their inversions. The external clocks for acquisition (CLK1, CLK2, and CLK3) will be tested at the end of the procedures for the Trigger/Time Base. The separation is due to the requirement for an extra 91A32 for the acquisition clock tests.

The next set of test procedures verify the word recognizers and triggering modes in the Trigger/Time Base.

(8) Menu Setup for Testing the Triggering Modes

These steps provide the initial menu setup for the triggering mode tests. This initial setup will be modified slightly as the functional check continues.

NOTE

This setup assumes that the Pattern Generator menu and the probe connections are as they were left at the conclusion of the previous steps (for the PG CLK line).

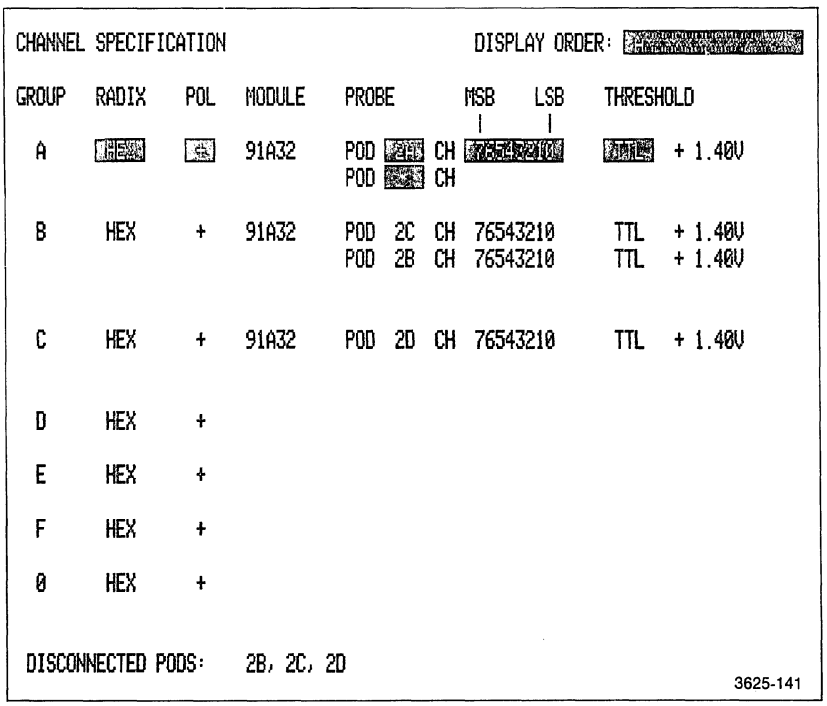


Figure 5-12. Channel Specification menu for the triggering mode functional tests.

1. Enter the Pattern Generator Program menu. Change the pattern generator clock to 1 μs.

2. Enter the Channel Specification menu. Adjust the channels so pod 2A is in group A and remove all other pods from this group.

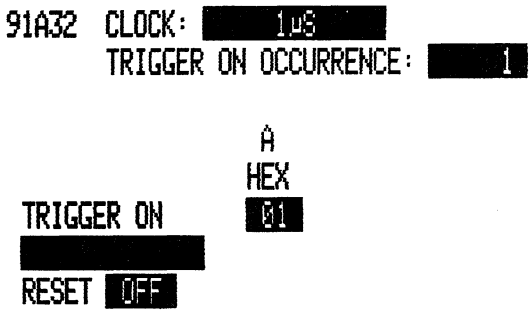
3. Enter the DISPLAY ORDER field of the Channel Specification menu. Adjust the field to show only A. All the other positions in the field should be changed to X (don't care). The final display should look like Figure 5-12.

(9) Verifying Single Word Triggering

The next steps verify the operation of the single word triggering capability of the Trigger/Time Base board.

1. Enter the Trigger Specification menu. Change the 91A32 clock to 1 μs (it was external rising edge).

2. Set the Trigger Specification menu to match the following display.



3. Press START SYSTEM

4. Enter the State Table menu. The trigger, shown by the highlighted data, should have occurred at sequence 14 and the data should match Figure 5-13.

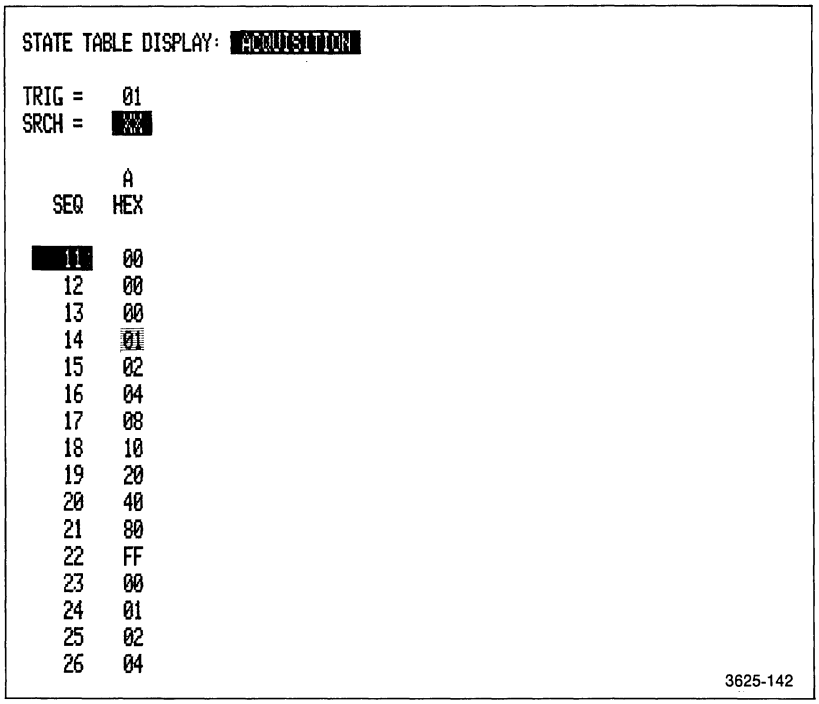
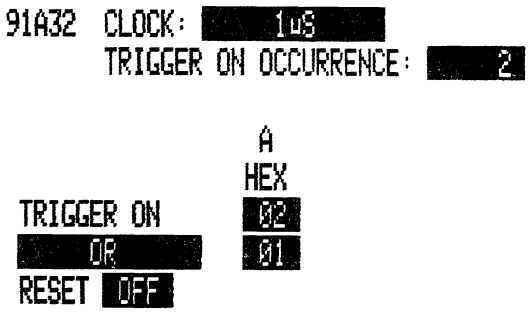


Figure 5-13. State Table display to verify single word triggering.

(10) Verifying OR Mode Triggering

The following steps verify the operation of OR mode triggering.

1. Enter the Trigger Specification menu. Set the menu to match the following display.



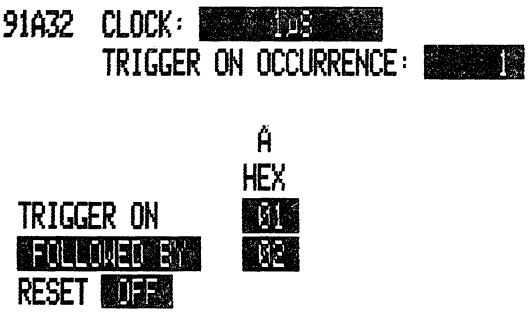
2. Press START SYSTEM.

3. Enter the State Table menu. The trigger should be on 02 data and should have occurred at sequence 14.

(11) Verifying FOLLOWED BY Triggering

The following steps verify the FOLLOWED BY triggering mode.

1. Enter the Trigger Specification menu. Set the menu to match the following display.



2. Press START SYSTEM.

3. Enter the State Table menu. The trigger should have occurred at sequence 15 and the data should match data shown in Figure 5-14.

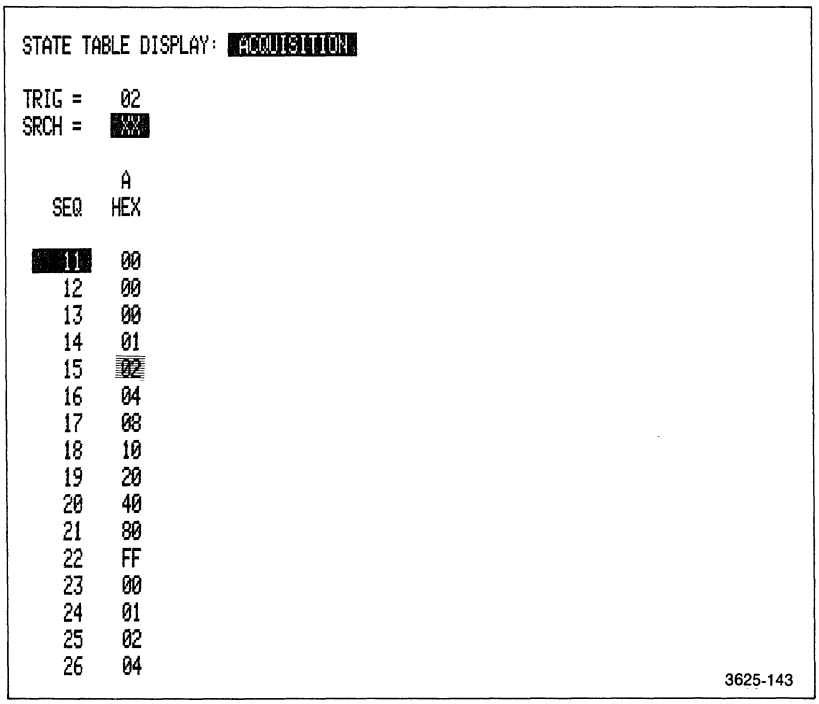
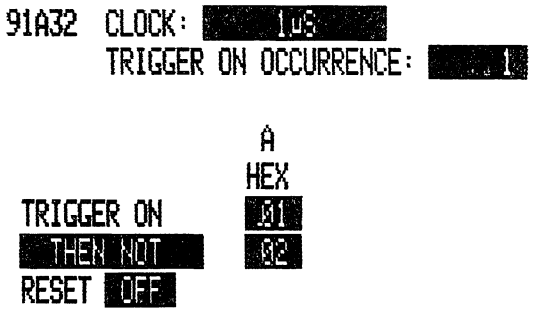


Figure 5-14. State Table display to verify followed by triggering.

(12) Verifying THEN NOT Triggering

1. Enter the Trigger Specification menu. Set the menu to match the following display.



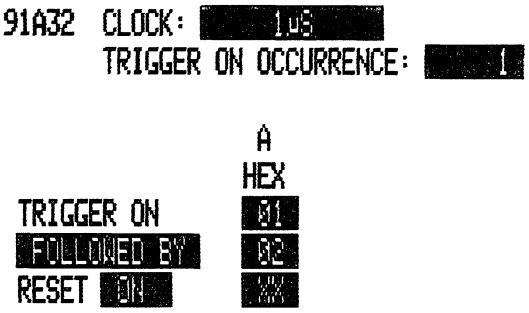
2. Press START SYSTEM.

3. Enter the State Table menu. The trigger should be on 04 data and should have occurred at sequence 15.

(13) Verifying RESET Triggering

The following steps verify the RESET capability of the trigger. Two test procedures are required to test RESET thoroughly.

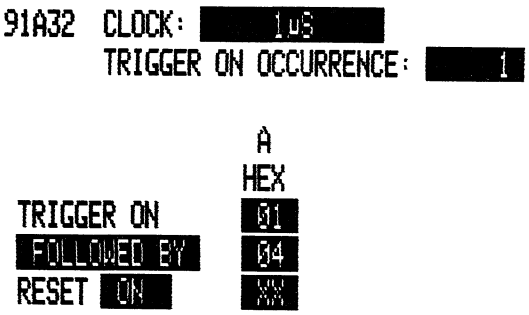
1. Enter the Trigger Specification menu. Set the menu to match the following display.



2. Press START SYSTEM.

3. Enter the State Table menu. The trigger should have occurred at sequence 15 and the data should match data shown in Figure 5-14.

4. Enter the Trigger Specification menu. Set the menu to match the following display.



5. Press START SYSTEM.

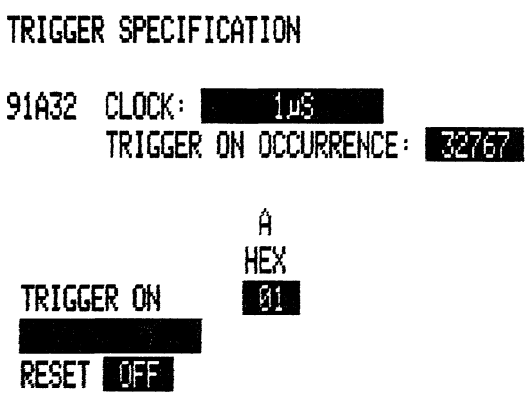
6. The WAITING FOR 91A32 TRIGGER signal should show on the screen. This verifies the RESET ON triggering capability.

(14) Verifying the Trigger Occurrence Counter

The following steps verify the operation of the occurrence counter.

1. Press STOP to stop the 91A32 from trying to trigger.

2. Enter the Trigger Specification menu. Set the menu to match the following display.



3. Press START SYSTEM.

4. The WAITING FOR 91A32 TRIGGER message should appear very briefly and then the acquired data should be shown on the screen. This verifies the action of the occurrence counter.

(15) Verifying the Trigger Delay Counter

The next steps verify the operation of the delay counter.

1. Enter the Trigger Specification menu. Set the menu to match the following display.

2. Press START SYSTEM.

3. The WAITING FOR STOP STORE message should appear very briefly and then the acquired data should be shown on the screen. The actual data acquired is not important, although the screen should say TRIGGER NOT IN MEMORY. This verifies the action of the delay counter.

This finishes the tests of the Trigger/Time Base triggering modes.

The next set of test procedures verify the circuitry for the internal clocks and the qualifier circuitry on the Trigger/Time Base board.

(16) Verifying Internal Clock Independence

The next steps verify the independence of the two internal clocks provided by the Trigger/Time Base board.

1. Enter the Trigger menu. Set the TRIGGER POSITION field to BEGIN.

2. Enter the Pattern Generator Program menu. Adjust the pattern generator clock to 5 μs. The 91A32 clock will remain at 1 μs.

3. Press START SYSTEM.

4. When acquisition is finished, enter the Timing Diagram menu. The data displayed should be like Figure 5-15.

(17) Verifying Qualifier and Trigger Interaction

The next steps verify that the qualifier line of the 91A32 module interacts properly with the trigger.

1. Connect the strobe output from the pattern generator probe (the white lead on the pattern generator side of the Diagnostic Lead Set) to the qualifier input of the data acquisition probe (the white lead on the data acquisition side of the Diagnostic Lead Set).

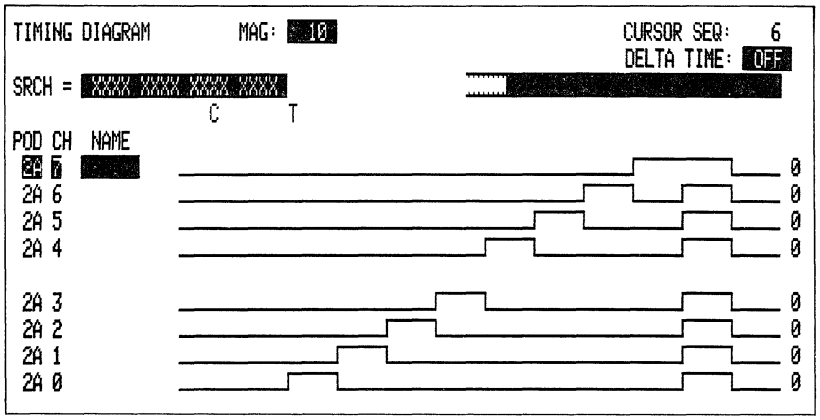
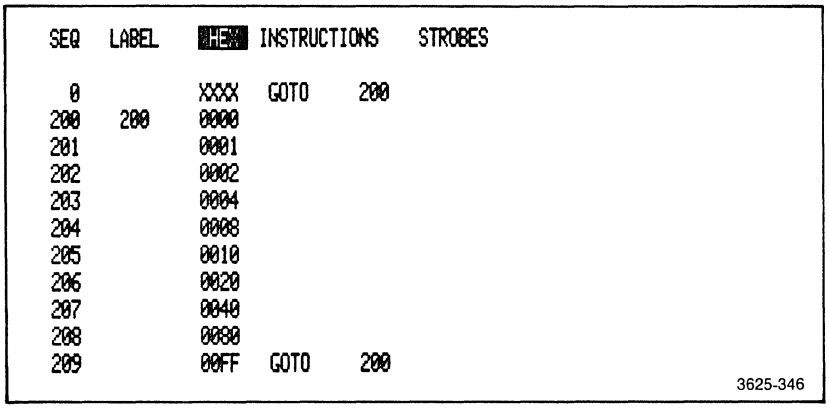


Figure 5-15. 5 μs pattern generator data acquired at 1 μs.

2. Enter the Pattern Generator Program menu. Set the pattern generator clock back to 1 μs.

3. Adjust the strobe field in the Pattern Generator Program menu to match the following display.



4. Enter the Pattern Generator Timing menu. Adjust strobe 0 to the following state.

5. Enter the Trigger Specification menu. Set the qualifier for pod 2A to 0.

6. Press START SYSTEM.

7. When acquisition is finished, enter the State Table menu. The data stored should match the data shown in Figure 5-16. Note in particular the position of the trigger, indicated by the highlighted data. If the trigger is in the right position, the qualifier and the trigger are correlating properly.

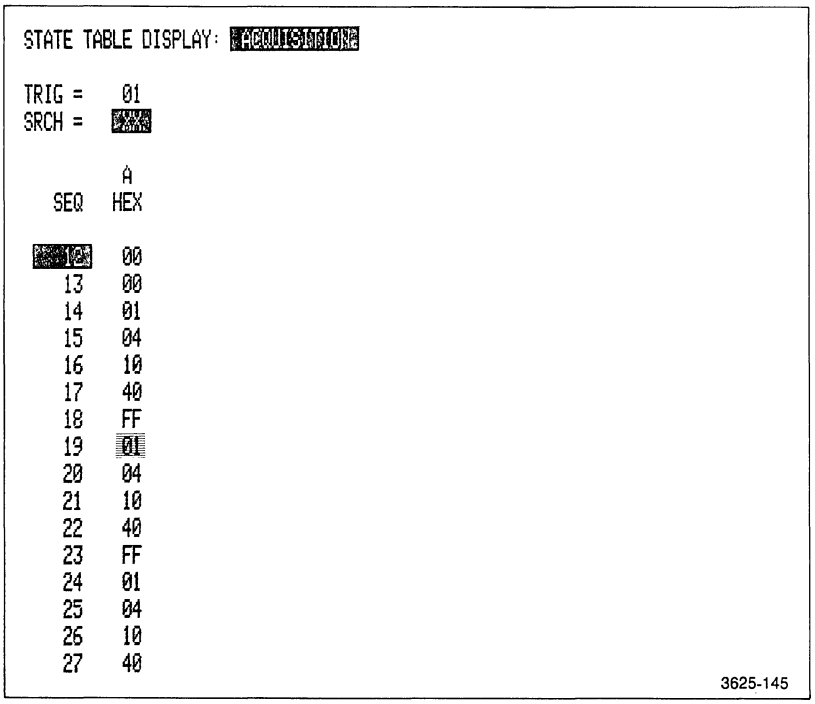


Figure 5-16. Acquisition of qualified data.

(18) Verification of the 91A08 Internal Clock

The internal diagnostics verify the operation of all the 91A32 clock rates. The 91A08 internal clock rates, however, are not checked. The next steps verify the availability of all 91A08 internal clock rates of 40 ns and over.

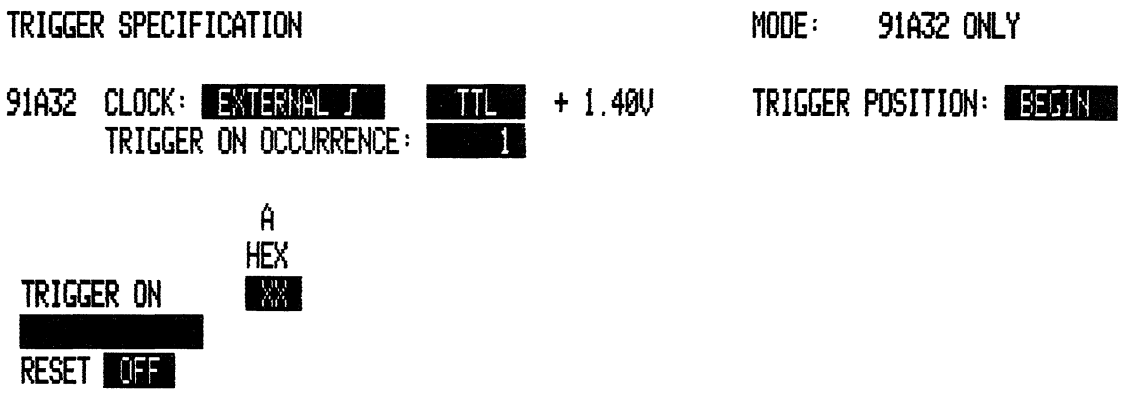
The next steps assume that the probes are still connected as they were for the previous steps (see the setup for the pattern generator external clock verification).

This test has the 91P16 module use the 91A08 internal clock, so the Trigger Specification menu must still be set in 91A32 ONLY mode.

1. Verify that the pattern generator clock output (the gray flying lead on the pattern generator side of the Diagnostic Lead Set) is still connected to the CLK1 line (black) of the External Clock probe.

2. Enter the Trigger Specification menu. Verify that the DAS is set to 91A32 ONLY mode. Set all qualifiers to the X (don't care) state.

3. In the Trigger Specification menu, set the 91A32 clock to external rising edge. Also set the trigger to the following state.



4. Enter the Pattern Generator Program menu. Set the pattern generator clock to internal 40 ns.

5. Press START SYSTEM.

6. The actual data acquired is not vital, but data should be acquired, and the SLOW CLOCK signal should not appear.

7. Enter the Pattern Generator Program menu again. Set the pattern generator clock to 50 ns. Press START SYSTEM. Again, the SLOW CLOCK message should not appear. Perform the same test for each of the other available pattern generator internal clock rates; 100 ns, 200 ns, 500 ns, 1 μs, 2 μs, 5 μs, 10 μs, 20 μs, 50 μs, 100 μs, 200 μs, 500 μs, 1 ms, 2 ms, and finally, 5 ms. The SLOW CLOCK signal should not appear on the screen during any of these tests.

NOTE

The remainder of the functional tests of the Trigger/Time Base board are optional. They verify the multi-phase clocking capability of the Trigger/Time Base. To perform the following tests the mainframe must contain two 91A32 modules.

If your test setup does not include two 91A32 modules, the functional check is complete. The test setup may be dismantled. To prevent damage to the DAS modules used for the test, be sure to turn off power to the mainframe before removing any modules.

(19) Setup for CLK2 and CLK3 Testing

The remaining steps in the Trigger/Time Base functional tests are optional, depending upon the availability of two 91A32 modules. At the initial mainframe setup for all the Trigger/Time Base tests, if two 91A32 modules were available, the 91A32 modules were installed in slots 2 and 3. These procedures assume that both of the 91A32 modules are present and located in those slots. Additionally, it is assumed that the probe setup has not been disturbed since the last tests.

1. Leave the clock output of the pattern generator probe (the gray flying lead on the pattern generator side of the Diagnostic Lead Set) connected to the CLK1 input of the External Clock probe (the black lead).

2. Disconnect the strobe from the qualifier line. Connect the strobe line (the white flying lead on the pattern generator side of the Diagnostic Lead Set) to the CLK2 line of the External Clock probe (the green lead).

3. Enter the Pattern Generator Program menu. Adjust the pattern generator clock to 1 μs (internal).

4. In the Pattern Generator Program menu, adjust the strobe field so the program matches the following display.

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0	CLR	0000			0
1		0000	GOTO	CLR	0
200	200	0000			0
201		0001			0
202		0002			0
203		0004			0
204		0008			0
205		0010			0
206		0020			0
207		0040			0
208		0080			0
209		00FF	GOTO	200	0

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5. Enter the Pattern Generator Timing menu. Adjust strobe 0 to the following state.

DELAY	WIDTH	SHAPE
110nS	40nS	⊓⊔

6. Enter the Channel Specification menu. Pod 2A should be the only occupant of group A. Put pod 3A in group B. Remove all other pods from group B.

7. Enter the DISPLAY ORDER field of the Channel Specification menu. Adjust the field so only A and B are showing. All other positions in the field should be set to X (don't care). The Channel Specification menu should now look like Figure 5-17.

8. Enter the Trigger Specification menu. Reset the trigger words in the Trigger Specification menu to all X (don't care).

9. Set the TRIGGER ON OCCURRENCE field in the Trigger Specification menu to 1 and set the RESET field off.

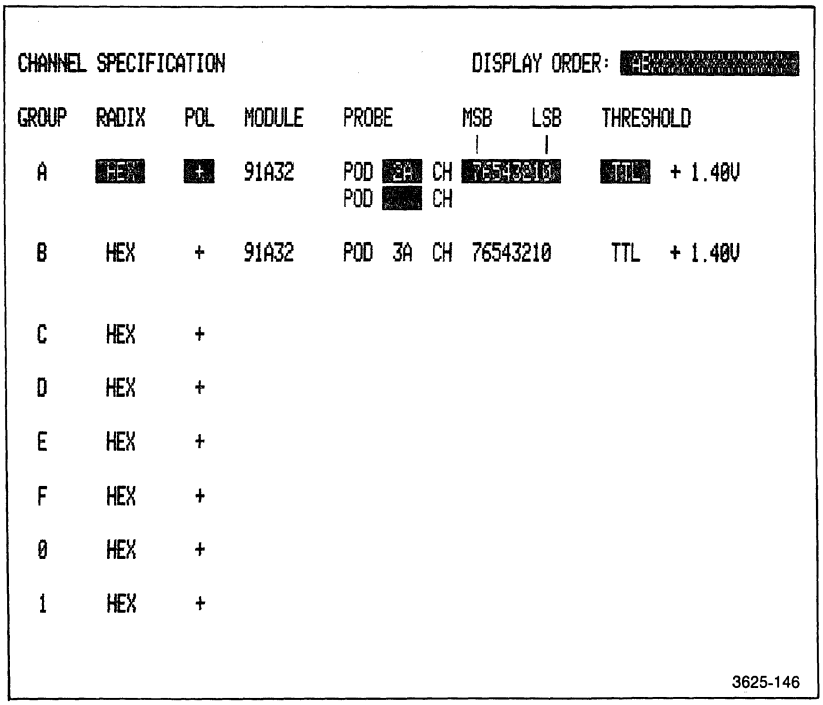

Figure 5-17. Channel Specification menu for acquisition clock testing.

(20) Verifying Operation of CLK2

The next steps check the operation of CLK2 and the ability of the Trigger/Time Base to clock in split mode.

1. Set the 91A32 clock in the Trigger Specification menu to external split mode.

2. Select CLK2 rising edge for the 91A32 in slot 2. Select CLK1 rising edge for the 91A32 in slot 3. The menu should now look like Figure 5-18.

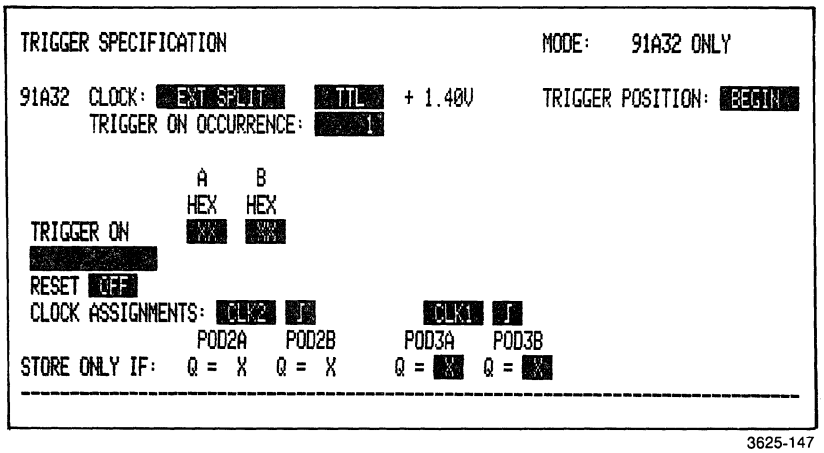

Figure 5-18. Trigger Specification menu setup for CLK2 verification.

3. Press START SYSTEM.

4. Enter the Timing Diagram menu. Adjust the menu so the data acquired by pods 2A and 3A is displayed. Pod 2A should show all zeros acquired.

The previous steps verified the operation of CLK2. The next few steps verify the operation of the inversion of CLK2.

5. Enter the Pattern Generator Program menu. Set the instruction field of sequence 0 to GOTO 200.

6. Enter the Trigger Specification menu. Change the clock for the 91A32 in slot 2 to CLK2 falling edge.

7. Press START SYSTEM.

8. Enter the Timing Diagram menu. Pod 2A should show data like the data in Figure 5-19. This verifies the operation of the inversion of CLK2.

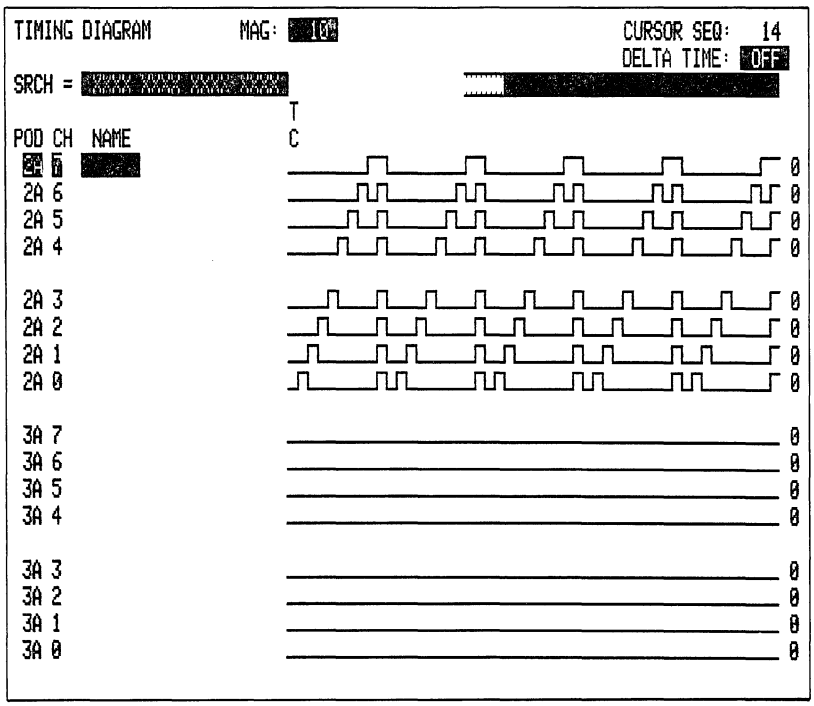

Figure 5-19. Inversion of CLK2 and CLK3 verification display.

(21) Verifying Operation of CLK3

The next steps check the operation of CLK3 and the ability of the Trigger/Time Base to clock in split mode.

1. Disconnect the CLK2 line (green) from the strobe line of the pattern generator probe. In place of CLK2, connect the CLK3 line (blue) to the strobe line.

2. Enter the Pattern Generator Program menu. Change the instruction field of sequence 0 from GOTO 200 to empty (don't care).

3. Enter the Trigger Specification menu. Change the clock for the 91A32 in slot 2 to CLK3 rising edge.

4. Press START SYSTEM.

5. Enter the Timing Diagram menu. The data acquired by pod 2A should be all LOW. This verifies the operation of CLK3.

6. Enter the Pattern Generator Program menu. Change the instruction field of sequence 0 from empty (don't care) to GOTO 200.

7. Enter the Trigger Specification menu. Change the clock for the 91A32 in slot 2 to CLK3 falling edge.

8. Press START SYSTEM.

9. Enter the Timing Diagram menu. Pod 2A should show data like that in Figure 5-19. This verifies the operation of the inversion of CLK3.

This completes the Trigger/Time Base functional check. The test setup may now be dismantled. Turn off the mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

91A32 DATA ACQUISITION MODULE FUNCTIONAL CHECK

The functional check verifies the operation of the acquisition and word recognition capabilities of the module.

NOTE

If the 91A32 module under test was used in slot 2 in the Trigger/Time Base functional check, some of the tests in this procedure have already been performed. Steps already performed in the Trigger/Time Base functional check are indicated with an asterisk (*) after the step number. These steps need not be duplicated.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe
- 91P16 Pattern Generator Module
- P6455 TTL/MOS Pattern Generator Probe
- P6452 Data Acquisition Probe
- P6452 External Clock Probe
- Diagnostic Lead Set

If available, add the following:

- 91A32 Data Acquisition module (used to check split clock acquisition)

Refer to the Operating Information section of this manual for instructions on module installation and on the use of the Diagnostics menu. Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes together using the diagnostic lead set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe in the way used on this functional check. If, due to insufficient +5 V Power Supply modules or some other constraint, the mainframe is not configured in the recommended way, then steps later in the functional check will need modification. For the greatest ease in following the functional check procedure, configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the DAS mainframe.
2. Install the 91A32 under test in slot 2 of the mainframe (if it is not already there).
3. Install the 91P16 in the mainframe slot 1.

NOTE

The mainframe will not operate if there is more than one 91P16 Pattern Generator module installed at the time of power-up. Before power-up, make sure there are no duplicates of this board in the mainframe.

4. If a second 91A32 module is available, install it in slot 3 (used to check split clock mode).

(2) Executing the Diagnostic Self-Test

The next steps run all available self-test diagnostics on the 91A32 module.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 2, the 91A32 module.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. The diagnostic tests MEM ADDR, ACQ MEM, and WRD REC should all pass. (The DAC THRSH test does not have internal read back, so it can neither pass nor fail.)

(3) Probe Setup for the Functional Test

These steps provide the initial setup for these tests. This probe organization will go through a series of permutations as the functional check continues.

NOTE

For further details on connecting probes together with the Diagnostic Lead Set, refer to the beginning of this Verification and Adjustment Procedures section.

1. Connect the TTL/MOS pattern generator probe to pod connector B of the 91P16. Set the diagnostic slide switch on the back of the probe to AUX.

2. Connect the data acquisition probe to pod connector D of the 91A32 module in slot 2. When this probe is installed, the mainframe should beep and the message POD 2D CONNECTED should show on the screen.

3. Press the Pod ID button on the back of the data acquisition probe housing. The mainframe should beep again and the message POD 2D should appear on the screen.

4. Connect these two probes (pod 1B and pod 2D) with the Diagnostic Lead Set.

5. Connect the External Clock probe to pod connector C of the Trigger/Time Base.

6. Install a flying lead set in the External Clock probe. Also install a ground lead in the diagnostic ground connector on the probe.

7. Install a ground lead in one of the GND SENSE connectors of the Data Acquisition Probe. Connect the ground lead of the clock probe to the ground lead of the acquisition probe.

(4) Verifying Pod Connector D

The next steps verify the operation of all data lines of pod connector D.

1. Leave the Diagnostics by pressing the PATTERN GENERATOR key. Verify that the pattern generator clock is set to 1 μs.

2. Verify that the following pattern generator program is already present.

SEQ	LABEL	HEX	INSTRUCTIONS	STROBES
0		XXXX	GOTO 200	
200	200	0000		
201		0001		
202		0002		
203		0004		
204		0008		
205		0010		
206		0020		
207		0040		
208		0080		
209		00FF	GOTO 200	

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3. Enter the Trigger Specification menu. Verify that the 91A32 clock is set to 1 μs.

4. Press START SYSTEM.

5. Examine the Timing Diagram menu. If pod D of the 91A32 being checked is not shown on the display, adjust the menu to show the data acquired by this pod. Set the magnification of the Timing Diagram to 10; this should result in a display like Figure 5-20.

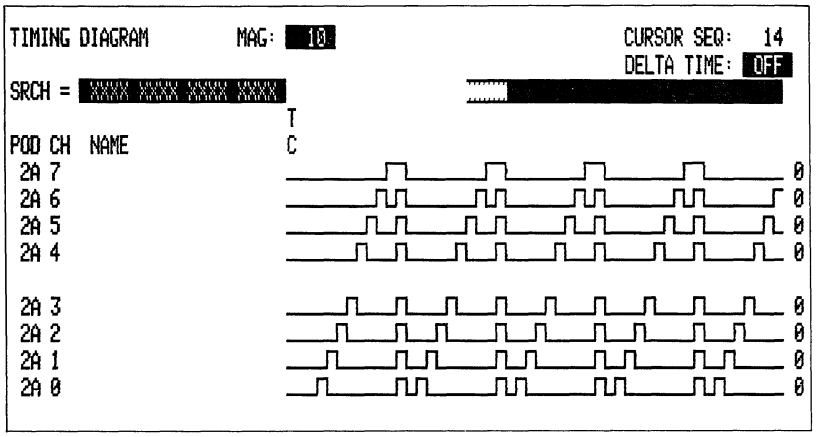


Figure 5-20. Initial test data acquired by the 91A32.

(5) Verifying Pod Connector C

The next steps verify the operation of all data lines of pod connector C.

1. Remove the acquisition probe connector from pod connector D and insert it in pod connector 2C. When the connector is inserted, the mainframe should beep and the screen should show POD 2C CONNECTED.

2. Press the Pod ID button on the back of the acquisition probe housing. The mainframe should beep again and POD 2C should show on the screen.

3. Press START SYSTEM.

4. Enter the Timing Diagram menu and adjust the display to show pod 2C's data. The display should again look like Figure 5-20.

(6) Verifying Pod Connector B

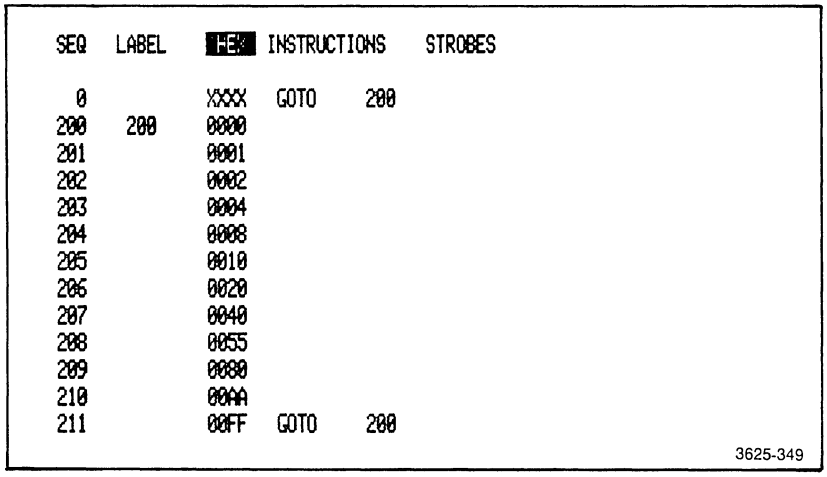
The next steps verify the operation of all data lines of pod connector B.

1. Connect the strobe line of the pattern generator probe (the white flying lead from the pattern generator probe) to the qualifier line of the data acquisition probe (the white flying lead from the data acquisition probe).

2. Remove the acquisition probe from pod connector C and insert it into pod connector B of the 91A32. When the connector is inserted, the mainframe should beep and the screen should show POD 2B CONNECTED.

3. Press the Pod ID button on the back of the acquisition probe housing. The mainframe should beep again and POD 2B should show on the screen.

4. Enter the Pattern Generator Program menu. Use the ADD LINE key to insert two lines immediately above sequence 209 (00FF data). Then adjust the pattern generator program to match the following display.



5. Enter the Pattern Generator Timing menu and set strobe 0 to the following state.

6. Enter the Trigger Specification menu and set the qualifier of pod 2B to 0.

7. Press START SYSTEM.

8. Enter the Timing Diagram menu and adjust the menu to show data acquired by pod 2B. The data acquired through pod B should look like Figure 5-20. Proper data verifies that pod B acquires data and that qualifier B operates.

The previous steps verified the operation of the data and qualifier lines. The next few steps verify the operation of the inversion of the qualifier.

9. Enter the Pattern Generator Timing menu and set strobe 0 to active low.

10. Enter the Trigger Specification menu and set the qualifier of pod 2B to 1.

11. Press START SYSTEM.

12. The data acquired through pod B should look like Figure 5-20 when viewed on the Timing Diagram menu. Proper data verifies that the inversion of qualifier B operates.

(7) Verifying Pod Connector A

The next steps verify the operation of all data lines of pod connector A.

1. Remove the acquisition probe from pod connector B and insert it into pod connector A of the 91A32. When the connector is inserted, the mainframe should beep and the screen should show POD 2A CONNECTED.

2. Press the Pod ID button on the back of the acquisition probe housing. The mainframe should beep again and POD 2A should show on the screen.

3. Enter the Trigger Specification menu. Set the qualifier of pod 2A to 1 and set the qualifier of pod 2B to X (don't care).

4. Press START SYSTEM.

5. The data acquired through pod A should look like Figure 5-20 when viewed on the Timing Diagram. Proper data verifies that pod A acquires data and that the inversion of qualifier A operates.

The previous steps verified the operation of the data and qualifier lines. The next few steps complete the verification of the qualifier line.

6. Enter the Pattern Generator Timing menu and set strobe 0 to active high.

7. Enter the Trigger Specification menu and set the qualifier of pod 2A to 0.

8. Press START SYSTEM.

9. The data acquired through pod A should look like Figure 5-20 when viewed on the Timing Diagram menu. Proper data verifies that qualifier A operates.

(8) Verifying the All-Valid Flip-Flop

The next steps verify the operation of the All-Valid flip-flop. This flip-flop indicates whether or not the entire acquisition memory is filled.

1. Examine the data acquired in the previous test. There should be no data stored at sequence 0.

2. Enter the Trigger Specification menu. Change the trigger position from BEGIN to DELAY with a delay value of 1000.

3. Press START SYSTEM.

4. Enter the Timing Diagram menu and look at sequence 0. Sequence 0 should contain data, although the actual value of the data is not important. The presence of data in sequence 0 indicates that the All-Valid flip-flop toggled at the appropriate time.

NOTE

If the 91A32 module being tested was used in slot 2 during the Trigger/Time Base functional test, the functional test is finished. All steps after this note have already been performed while testing the Trigger/Time Base.

If you are finished, you may dismantle the test setup. Turn off the DAS mainframe before removing any modules to prevent damage to the modules or the mainframe.

(9)* Verifying the CLK1 Line

The next steps verify that the 91A32 module is receiving the CLK1 signal properly through the interconnect.

1. Connect the external clock line of the Diagnostic Lead Set (the gray flying lead on the pattern generator side) to the CLK1 lead (black) of the External Clock probe.

2. Enter the Trigger Specification menu and set the acquisition clock to external rising edge. Also set the trigger position field from DELAY to BEGIN.

3. Press START SYSTEM.

4. Look at the data acquired through pod 2A on the Timing Diagram. The data should look like Figure 5-20.

The previous four steps verified that the 91A32 module could receive CLK1 signals. The next few steps verify that the inversion of CLK1 can also be received.

5. Enter the Trigger Specification menu and set the acquisition clock to external falling edge.

6. Press START SYSTEM.

7. Look at the data acquired through pod 2A on the Timing Diagram. The data should look like Figure 5-20. Proper data verifies the operation of the inversion of the 91A32 module's external clock.

NOTE

The remainder of the functional tests of the 91A32 module are optional. They verify the multi-phase clocking capability of the 91A32. To perform the following tests the mainframe must contain two 91A32 modules.

If your test setup does not include two 91A32 modules, the functional check is complete. The test setup may be dismantled. To prevent damage to the DAS modules used for the test, be sure to turn off power to the mainframe before removing any modules.

***If the 91A32 module under test was used in slot 2 in the Trigger/Time Base functional check, some of the tests in this procedure have already been performed. Steps already performed in the Trigger/Time Base functional check are indicated with an asterisk (*) after the step number. These steps need not be duplicated.**

(10)* Setup for Optional CLK2 and CLK3 Testing

The remaining steps in the 91A32 module functional tests are optional, and require two 91A32 modules. At the initial mainframe setup for all the 91A32 tests, if two 91A32 modules were available, the 91A32 modules were installed in slots 2 and 3. These procedures assume that both of the 91A32 modules are present and located in those slots. Additionally, it is assumed that the probe setup has not been disturbed since the last tests.

1. Leave the clock output of the pattern generator probe (the gray flying lead on the pattern generator side of the Diagnostic Lead Set) connected to the CLK1 input of the External Clock probe (the black lead).

2. Disconnect the strobe from the qualifier line. Connect the strobe line (the white flying lead on the pattern generator side of the Diagnostic Lead Set) to the CLK2 line of the External Clock probe (the green lead).

3. Enter the Pattern Generator Program menu. Delete sequences 210 and 208 and adjust the strobe field so the program matches the following display.

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0	CLR	0000			0
1		0000	GOTO	CLR	0
200	200	0000			0
201		0001			0
202		0002			0
203		0004			0
204		0008			0
205		0010			0
206		0020			0
207		0040			0
208		0080			0
209		00FF	GOTO	200	0

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4. Enter the Pattern Generator Timing menu. Adjust strobe 0 to the following state.

DELAY	WIDTH	SHAPE
110nS	40nS	⊓

5. Enter the Channel Specification menu. Make pod 2A the only occupant of group A. Put pod 3A in group B. Remove any other pods from groups A and B.

6. Enter the DISPLAY ORDER field of the Channel Specification menu. Adjust the field so only A and B are showing. All other positions in the field should be set to X (don't care). The Channel Specification menu should now look like Figure 5-21.

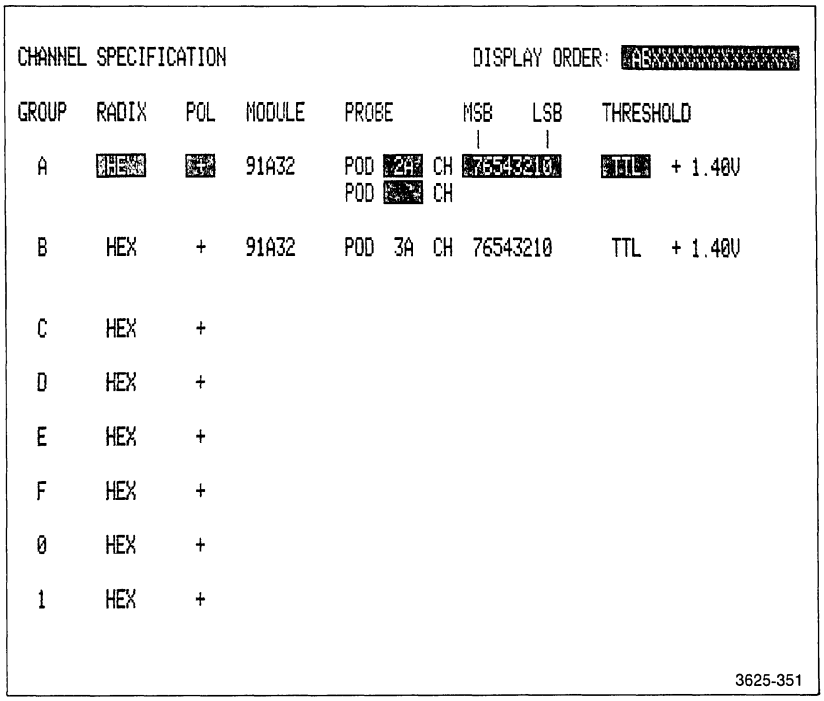

Figure 5-21. Channel Specification menu for acquisition clock testing.

(11)* Optional Verification of CLK2

The next steps check the ability of the 91A32 module to receive CLK2.

1. Enter the Trigger Specification menu. Set the 91A32 clock in the Trigger Specification menu to external split mode.

2. Select CLK2 rising edge for the 91A32 in slot 2. Select CLK1 rising edge for the 91A32 in slot 3. The menu should now look like Figure 5-22.

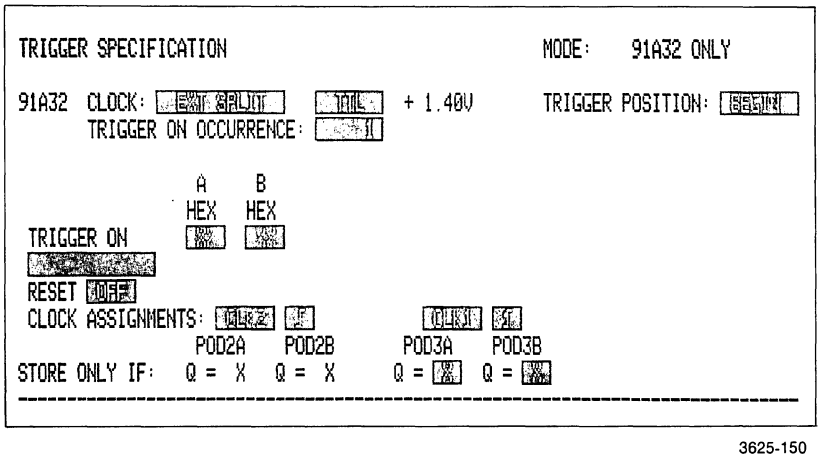

Figure 5-22. Trigger menu setup for CLK2 verification.

3. Press START SYSTEM.

4. Enter the Timing Diagram menu. Adjust the menu so the data acquired by pod 2A is displayed. Pod 2A should show all zeros acquired.

The previous steps verified the reception of CLK2. The next few steps verify that the 91A32 receives the inversion of CLK2.

5. Enter the Pattern Generator Program menu. Set the instruction field of sequence 0 to GOTO 200.

6. Enter the Trigger Specification menu. Change the clock for the 91A32 in slot 2 to CLK2 falling edge.

7. Press START SYSTEM.

8. Enter the Timing Diagram menu. Pod 2A should show data like the data in Figure 5-23. This verifies the operation of the inversion of CLK2.

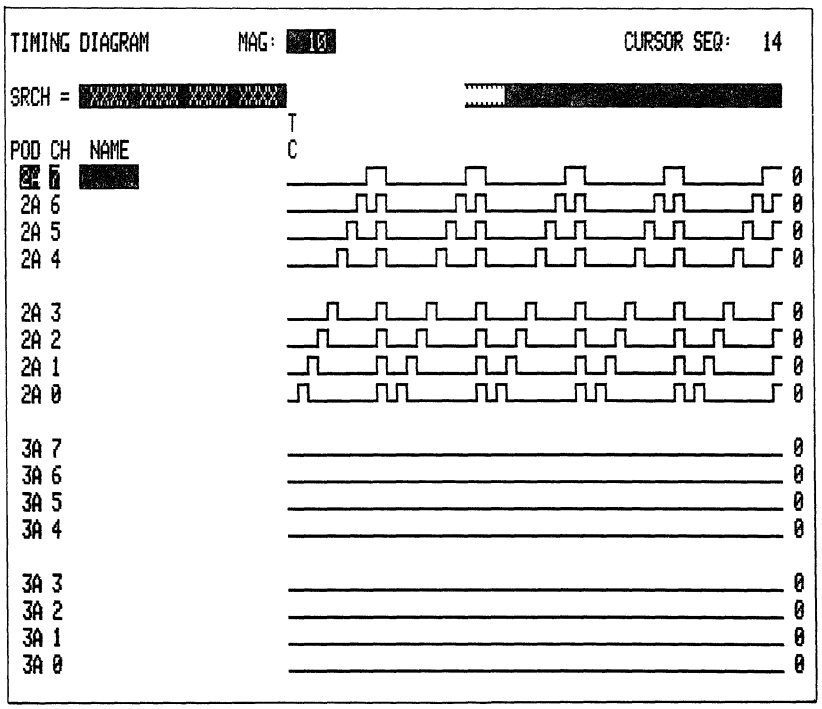

Figure 5-23. Inversion of CLK2 and CLK3 verification display.

(12)* Optional Verification of CLK3

The next steps check ability of the 91A32 module to receive CLK3.

1. Disconnect the CLK2 line (green) from the strobe line of the pattern generator probe. In place of CLK2, connect the CLK3 line (blue) to the strobe line.
2. Enter the Pattern Generator Program menu. Change the instruction field of sequence 0 from GOTO 200 to don't care (empty).
3. Enter the Trigger Specification menu. Change the clock for the 91A32 in slot 2 to CLK3 rising edge.
4. Press START SYSTEM.
5. Enter the Timing Diagram menu. The data acquired by pod 2A should be all LOW. This verifies the operation of CLK3.
6. Enter the Pattern Generator Program menu. Enter GOTO 200 into the instruction field of sequence 0.
7. Enter the Trigger Specification menu. Change the clock for the 91A32 in slot 2 to CLK3 falling edge.
8. Press START SYSTEM.
9. Enter the Timing Diagram menu. Pod 2A should show data like Figure 5-23. This verifies the operation of the inversion of CLK3.

This completes the 91A32 Functional Check. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

91A08 DATA ACQUISITION MODULE FUNCTIONAL CHECK

The 91A08 functional check verifies the operation of the acquisition and word recognition capabilities of the module.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe
- 91P16 Pattern Generator Module
- P6455 TTL/MOS Pattern Generator Probe
- P6452 Data Acquisition Probe
- P6454 100 MHz Clock Probe

If available, add the following:

- 91A32 Data Acquisition Module (used to check 91A32 ARMS 91A08 mode and 91A32 AND 91A08 mode)
- P6452 External Clock Probe

Refer to the Operating Information section of this manual for instructions on module installation and on the use of the Diagnostic menu. Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes together using the Diagnostic Lead Set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe in the way used for this functional check. If, due to insufficient +5 V power supply modules or some other constraint, the mainframe is not configured in the recommended way, then steps later in the functional check will need modification. For the greatest ease in following the functional check procedure, configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the DAS mainframe.
2. Install the 91A08 module to be checked in slot 6 of the mainframe.
3. Install the 91P16 module in slot 1.

NOTE

The mainframe will not operate if there is more than one 91P16 Pattern Generator module installed at the time of power-up. After inserting the modules used for this test, make sure there are no duplicates of this board in the mainframe.

4. If a 91A32 is available, it should be installed in slot 2 (used to check 91A32 ARMS 91A08 mode and 91A32 AND 91A08 mode).

(2) Executing the Diagnostic Self-Test

The next steps run all available self-test diagnostics on the 91A08 module.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run the tests on slot 6, the 91A08 module.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. The diagnostic tests MEM ADDR, DIF CNTR, DEL CNTR, WRD REC, and ACQ MEM, should all pass. (The DAC THRSH test has no internal read back, so it can neither pass nor fail.)

(3) Probe Setup for the Functional Test

These steps provide the initial test setup for these tests. This probe organization will go through several modifications as the functional test continues.

1. Connect the TTL/MOS pattern generator probe to pod connector B of the 91P16. Set the diagnostic slide switch on the back of the probe to AUX.

2. Connect the data acquisition probe to pod connector C of the 91A08 module in slot 6. When the probe is connected to the 91A08, the mainframe should beep and the message POD 6C CONNECTED should show on the screen.

3. Press the Pod ID button on the back of the acquisition probe housing. The mainframe should beep again and the message POD 6C should appear on the screen.

4. Connect these two probes (pod 1B and pod 6C) together using the Diagnostic Lead Set.

5. Connect the data acquisition probe diagonstic ground to the pattern generator VL sense lead. Connect the 100 MHz Clock Probe REF lead to this junction also.

6. Connect the strobe line of the pattern generator probe (the white flying lead from the pattern generator probe) to the qualifier line of the data acquisition probe (the white flying lead from the data acquisition probe).

7. Connect the P6454 100 MHz Clock Probe to the coaxial connector on the back of the 91A08 module in slot 6. This coaxial connector is located immediately above pod connector C.

8. Connect the IN lead of the 100 MHz Clock Probe to the clock output of the pattern generator probe (the gray flying lead on the pattern generator side of the Diagnostic Lead Set).

9. Press CHAN SPEC and select +2.50 VAR threshold.

(4) Verifying Pod Connector C

The next steps verify the operation of all data lines of pod connector C. The operation of the external clock is verified at the same time.

1. Leave the diagnostics by pressing the PATTERN GENERATOR key. This displays the Pattern Generator Program menu. Verify that the pattern generator clock is set to 1 μs.

2. Use the ADD LINE key to insert two lines immediately above sequence 209 (00FF data). Then adjust the pattern generator program to look like:

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0		XXXX	GOTO	200	
200	200	0000			
201		0001			
202		0002			
203		0004			
204		0008			
205		0010			
206		0020			
207		0040			
208		0055			0
209		0080			
210		00AA			0
211		00FF	GOTO	200	

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3. Enter the Pattern Generator Timing menu and set strobe 0 to the following state.

DELAY	WIDTH	SHAPE
70nS	1.000uS	⎍

4. Enter the Trigger Specification menu. Adjust the mode to 91A08 ONLY if the DAS is not already set to this mode.

5. While in the Trigger Specification menu, set the qualifier of pod 6C to 0. Also set the 91A08 CLOCK field to external rising edge.

6. Press START SYSTEM.

7. Examine the Timing Diagram menu. If pod C of the 91A08 is not shown on the display, adjust the menu to show pod C's data.

8. Set the magnification of the Timing Diagram to 10; this should show a display like Figure 5-24. Proper data verifies that pod C acquires data and that the 91A08 qualifier operates. The trigger word is not critical.

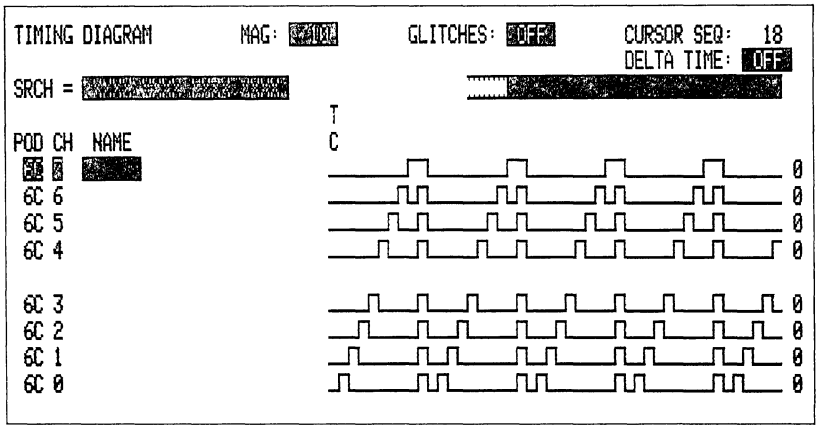


Figure 5-24. Initial test data acquired by the 91A08.

The previous steps verified the operation of the data and qualifier lines of the 91A08. The next steps verify the operation of the inversion of the qualifier.

9. Enter the Pattern Generator Timing menu and set the shape of strobe 0 to active low.

10. Enter the Trigger Specification menu and set the qualifier for pod 6C to 1.

11. Press START SYSTEM.

12. The data acquired through pod C should look like Figure 5-24 when viewed on the Timing Diagram menu. Proper data verifies that qualifier C operates.

(5) Verifying the Inversion of the External Clock

Since the previous steps verified the operation of the external clock, this is a good opportunity to verify the inversion of the clock.

1. Enter the Trigger Specification menu. Set the 91A08 clock to external falling edge.

2. Press START SYSTEM.

3. Check the Timing Diagram menu to verify that the 91A08 module acquired data (any data is acceptable). This verifies the operation of the inversion of the external clock.

(6) Verifying Triggering on Data

The next steps verify that the single level data trigger contained on the 91A08 board is functional.

1. Enter the Trigger Specification menu. Set the TRIGGER ON field to 00.

2. Press START SYSTEM.

3. Enter the State Table menu. Note the data highlighted as the trigger word. This data should be 00. This verifies the word recognizer on the 91A08 module.

(7) Verifying the Trigger/Qualifier Interaction

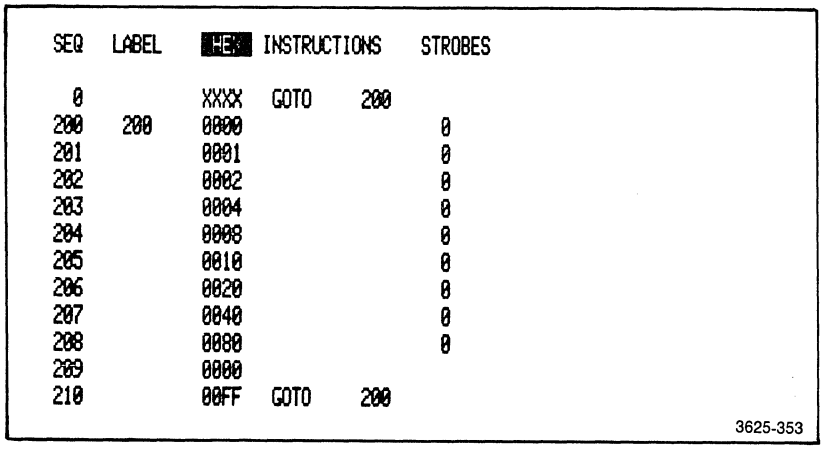
The next steps check that the trigger is reacting properly to qualifier signals.

1. Enter the Trigger Specification menu. Set the TRIGGER ON field to AA. Leave the qualifiers set as they are.
2. Press START SYSTEM.
3. The DAS should display the WAITING FOR 91A08 TRIGGER message. This verifies that the 91A08 will not trigger on unqualified data.
4. Press STOP.
5. Enter the Trigger Specification menu. Set the TRIGGER ON field to 80.
6. Press START SYSTEM.
7. Enter the State Table menu. Notice that the highlighted word is 80. This verifies that the trigger and qualifier on the 91A08 are interacting properly.

(8) Verifying Glitch Acquisition

The following steps verify the operation of the glitch detectors and the glitch portion of the acquisition memory.

1. Disconnect the qualifier line from the strobe line on the Diagnostic Lead Set. Also disconnect the pattern generator output clock from the 100 MHz Clock Probe.
2. Reconnect the 100 MHz Clock Probe IN line to the strobe output of the pattern generator probe (the white flying lead on the pattern generator side of the Diagnostic Lead Set).
3. Enter the Pattern Generator menu. Delete sequence 208 and set the data of sequence 209 to all zeros. Then adjust the STROBE field so the pattern generator program looks like the following:



4. Enter the Pattern Generator Timing menu and set strobe 0 to the following state.

5. Enter the Trigger Specification menu and set all qualifiers to X (don't care).

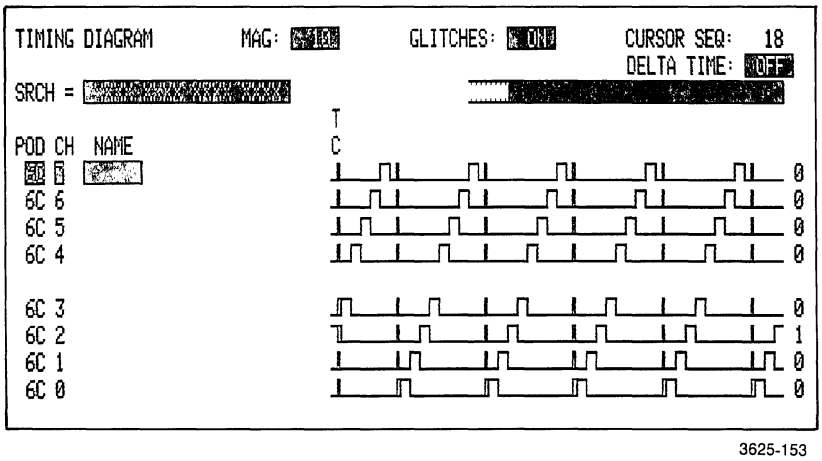


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Figure 5-25. 91A08 glitch detector test

6. While in the Trigger Specification menu, also set the 91A08 clock to external rising edge.

7. Press START SYSTEM.

8. Enter the Timing Diagram menu and set the GLITCH field to ON. The data acquired by the 91A08 module should look like Figure 5-25. This verifies the operation of the glitch detectors and glitch memory.

(9) Verifying Triggering on Glitches

The next steps verify the trigger on glitches feature of the 91A08.

1. Enter the Trigger Specification menu. Set the GLITCHES field ON. Fill the field adjacent to the GLITCHES ON field with ones (1). This sets the 91A08 to trigger on the first glitch it sees.

2. Set the TRIGGER ON field, in the Trigger Specification menu, to AA. This prevents the 91A08 from triggering on data words provided by the Pattern Generator.

3. Press START SYSTEM.

4. The WAITING FOR 91A08 TRIGGER message should not appear on the screen. The actual data acquired is not important as long as the trigger occurs promptly. This verifies the trigger on glitches capability.

(10) Verifying the Trigger Delay Counter

The following steps verify that the delay counter for the 91A08 module is operational.

1. Enter the Trigger Specification menu. Set the GLITCHES field OFF. Set the TRIGGER ON field to XX (don't care).

2. In the Trigger Specification menu, change the TRIGGER POSITION field to DELAY and set the delay value to 32767.

3. Press the START SYSTEM key.

4. The WAITING FOR 91A08 TRIGGER message may flash on the screen, but the acquisition should be finished shortly afterwards. The screen should show the TRIGGER NOT IN MEMORY message along with the acquired data. This verifies the operation of the delay counter in the 91A08 module.

(11) Verifying the High Speed Internal Clocks

The following steps verify that the 10 ns and 20 ns internal clocks are present. These clocks are a function of the Trigger/Time Base board, but they aren't verified in the Trigger/Time Base functional check procedure.

1. Enter the Trigger Specification menu. Set the 91A08 clock to internal 10 ns.

2. Press START SYSTEM.

3. Data should be acquired. The actual data acquired is not important, because a 10 ns clock exceeds the capabilities of the Diagnostic Lead Set. This verifies the operation of the 10 ns clock.

4. Enter the Trigger Specification menu. Set the 91A08 clock to 20 ns.

5. Press START SYSTEM.

6. Data should be acquired. The actual data acquired is not important, because a 20 ns clock exceeds the capabilities of the Diagnostic Lead Set. This verifies the operation of the 20 ns clock.

NOTE

The remainder of the functional tests of the 91A08 module are optional. They verify the operation of the 91A08 in 91A32 ARMS 91A08 mode and in 91A32 AND 91A08 mode. To perform the following tests the mainframe must contain a 91A32 module.

If your test setup does not include a 91A32 module, the functional check is complete. The test setup may be dismantled. To prevent damage to the DAS modules used in the test, be sure to turn off power to the mainframe before removing any modules.

(12) Verifying 91A32 ARMS 91A08 Mode

The next tests verify operation of the 91A08 in ARMS mode. To perform the following tests, the mainframe must contain a 91A32 module as well as the 91A08 module under test. Only the 91A08 module installed in slot 6 will be tested. The 91A32 module should have already been installed in slot 2.

1. Enter the Trigger Specification menu. Set the MODE field to 91A32 ARMS 91A08.

2. In the Trigger Specification menu change the 91A32 clock rate to 2 μs. Change the 91A08 clock rate to 1 μs. The 91A08 module now cannot trigger until it is armed by the 91A32 module. The menu should match the display shown in Figure 5-26.

3. Press START SYSTEM.

4. Enter the State Table menu. The first data acquired by the 91A08 may have either two or three data words to the 91A32 module's one data word. After the initial synchronization, there should be exactly two 91A08 data words for every 91A32 data word. Note that the actual data acquired is not important. This verifies the operation of the difference counter and the miscellaneous input storage on the 91A08.

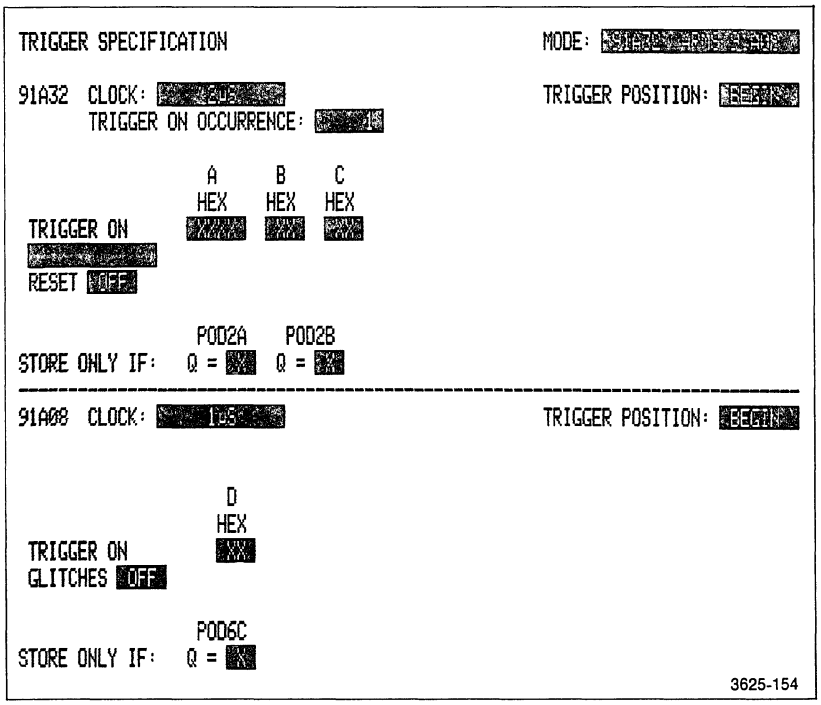


Figure 5-26. Setup for 91A32 ARMS 91A08 functional test.

(13) Verifying 91A24 ARMS 91A08 Mode

To perform the following tests, the mainframe must contain a 91A24 module as well as the 91A08 module under test.

1. Enter the Trigger Specification menu. Set the MODE field to 91A24 ARMS 91A08.

2. Select the Clock Specification menu and set the clock rate to 2 μs.

3. Press START ACQUISITION.

4. The DAS should acquire and display time-aligned data (all zeros) with 2 fast data samples (91A08) per 1 slow data sample (91A24).

(14) Probe Setup for Verifying 91A32 AND 91A08 Mode

The following steps reorganize the probe connections so that the 91A08 module can operate from the 91A32 external clock (CLK1).

1. Disconnect the IN lead of the 100 MHz Clock Probe from the strobe line of the pattern generator.

2. Connect the External Clock Probe to the Trigger/Time Base Module (pod connector 7C).

3. Connect the CLK1 line of the External Clock Probe (the black lead) to the clock output of the pattern generator probe (the gray flying lead on the pattern generator side of the diagnostic lead set).

4. Disconnect the REF lead of the 100 MHz Clock Probe from the GND SENSE lead of the data acquisition probe.

5. Connect the GND DIAGNOSTIC lead of the External Clock Probe to the GND SENSE lead of the data acquisition probe. This gives all three probes a common ground connection.

(15) Verifying 91A32 AND 91A08 Mode

The next steps verify that the 91A08 module can use all of the clocks necessary to operate in the 91A32 AND 91A08 mode.

1. Enter the Trigger Specification menu. Set the MODE field to 91A32 AND 91A08. Change the 91A32 clock rate to 1 μs.

2. Press START SYSTEM.

3. Enter the Timing Diagram menu and examine the data acquired by pod 6C. The data should look like Figure 5-27.

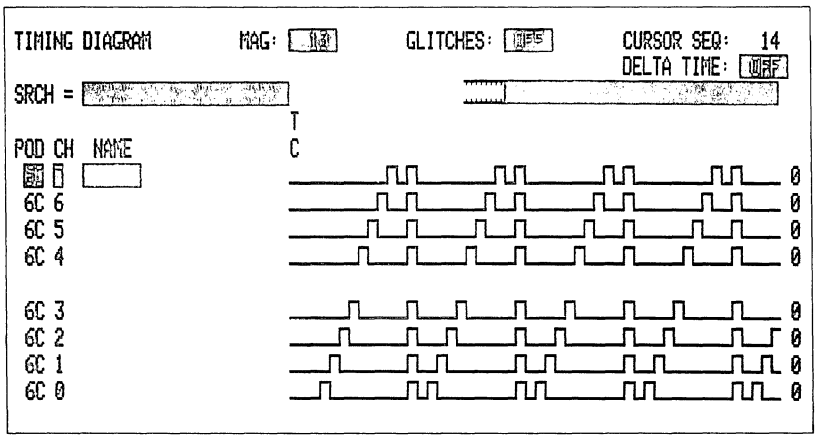


Figure 5-27. AND mode verification data. 3625-155

The previous steps verified that the 91A08 module receives the 91A32 internal clock. The next steps verify that the 91A08 can operate with CLK1, the 91A32 master internal clock.

4. Enter the Trigger Specification menu. Set the 91A32 clock to external rising edge.
5. Press START SYSTEM.
6. Look at the data acquired by pod 6C on the Timing Diagram menu. The data should look like Figure 5-27. Proper data verifies the operation of the 91A08 using CLK1.
7. Enter the Trigger Specification menu. Set the 91A32 clock to external falling edge.
8. Press START SYSTEM.
9. Look at the data acquired by pod 6C on the Timing Diagram menu. The data should look like Figure 5-27. Proper data verifies the operation of the 91A08 using the inversion of CLK1.

This completes the functional check procedure for the 91A08 Data Acquisition Module. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

91P16 PATTERN GENERATOR MODULE FUNCTIONAL CHECK

NOTE

If the 91P16 module to be functionally tested was used in the Trigger/Time Base functional check procedure, some of the tests in this procedure will already have been performed. These steps are indicated by an asterisk after the step number; they need not be duplicated.

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe
- Diagnostic Lead Set
- P6455 TTL/MOS Pattern Generator Probe
- P6452 Data Acquisition Probe
- Pulse or square wave generator

and either of the following:

- 91A32 Data Acquisition Module; or
- 91A08 Data Acquisition Module and
- P6454 100 MHz Clock Probe

Refer to the Operating Instructions of this manual for instructions on module installation and on the use of the Diagnostics menu. Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes together with the Diagnostic Lead Set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe in the way used for this functional check. If, due to insufficient +5 V power supply modules or some other constraint, the mainframe is not configured in the recommended way, then steps later in the functional check will need modification. For the greatest ease in the functional check procedure, configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the mainframe.
2. Install the 91P16 to be checked in slot 1 of the mainframe.

NOTE

The mainframe will not operate with more than one 91P16 Pattern Generator Module installed at the time of power-up. After inserting the modules used for this test, make sure there are no duplicates of this board in the mainframe.

3. Install the acquisition module to be used for testing. If a 91A08 module is used, install it in slot 6. If a 91A32 module is used, install it in slot 2.

(2) Executing the Diagnostic Self-Test

The next steps run all available self-test diagnostics on the 91P16 module.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.
2. Press START SYSTEM to enter the Diagnostics menu. Select to run diagnostic tests on slot 1, the 91P16 module.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. The diagnostic tests PC, VECTOR RAM, MICRO RAM, ADVANCE, GOTO, CALL, RETURN, STACK RAM, and CLOCK, should all pass.

(3) Probe Setup for the Functional Test

These steps provide the initial test setup for these tests. This probe organization will go through several modifications as the functional check continues.

NOTE

For further details on connecting probes together with the Diagnostic Lead Set, refer to the beginning of this Verification and Adjustment Procedures section.

1. Connect the TTL/MOS pattern generator probe to pod connector C of the 91P16. When the probe is installed, the mainframe should beep and show the message POD 1C CONNECTED.

2. Press the Pod ID button on the back of the probe housing. The mainframe should beep and display POD 1C.

3. Set the diagnostic slide switch on the back of the TTL/MOS pattern generator probe to AUX.

4. Connect the data acquisition probe to the acquisition module (either a 91A08 module or a 91A32 module). If a 91A32 module is used, install its data acquisition probe in pod connector A.

5. Connect the pattern generator probe to the data acquisition probe with the diagnostic lead set.

6. Connect the strobe line of the pattern generator probe (the white flying lead from the pattern generator side of the Diagnostic Lead Set) to the qualifier line of the data acquisition probe (the white flying lead from the acquisition side of the diagnostic lead set).

7. Connect the External Clock Probe to pod connector C of the Trigger/Time Base Module.

8. Install a flying lead set in the External Clock Probe. Also a ground lead in the GND DIAGNOSTIC connector on the clock probe.

9. Install a ground lead in one of the GND SENSE connectors of the data acquisition probe. Connect the ground lead of the External Clock Probe to the ground lead of the data acquisition probe.

10. If a 91A32 module is being used for the test, connect the CLK1 line of the External Clock Probe (the black lead) to the clock line of the pattern generator probe (the gray flying lead on the pattern generator side of the Diagnostic Lead Set).

NOTE

If a 91A32 is being used for this procedure, then the probe setup is complete.

11. If a 91A08 module is being used as the acquisition module in the functional check, connect the 100 MHz Clock Probe to the coaxial connector on the 91A08 module in slot 6.

12. Connect the IN line of the 100 MHz Clock Probe to the clock output of the pattern generator probe (the gray flying lead from the pattern generator side of the Diagnostic Lead Set).

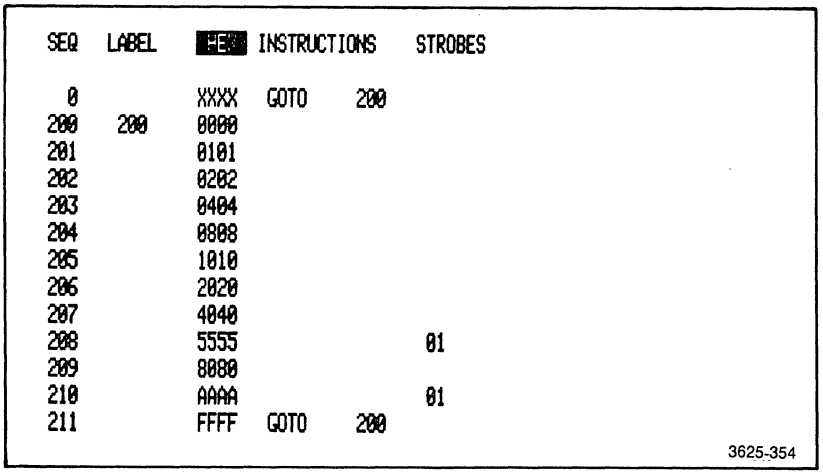
13. Connect the REF line of the 100 MHz Clock Probe to the unused GND SENSE line of the data acquisition probe.

(4) Initial Menu Setup for the Functional Check

The next steps organize the menus so the remainder of the functional check will require an minimum of menu manipulation.

1. Leave the Diagnostics menu by pressing the PATTERN GENERATOR key. In the Pattern Generator Program menu, verify that the pattern generator clock is set to 1 μs.

2. Adjust the program already present in the Pattern Generator Program menu to match the following display:



3. Enter the Pattern Generator Timing menu and set both strobes 0 and 1 to the following state:

4. Enter the Trigger Specification menu. If the functional check is being performed with a 91A32 module, leave the MODE field set to 91A32 ONLY. If the functional check is being performed with a 91A08 module, set the MODE field to 91A08 ONLY.

5. In the Trigger Specification menu, set the acquisition clock to external rising edge.

6. Press the Pod ID button on the back of the data acquisition probe.

7. Read the pod number off the DAS screen. Then set the qualifier for that pod to 1.

(5) Verifying Pod Connector C

The next steps verify that the 91P16 can transmit data, strobes, and clock signals through pod connector C.

1. Press the START SYSTEM key.

2. Enter the Timing Diagram menu.

3. Press the Pod ID button on the back of the Data Acquisition probe. Read the pod number off the DAS screen. Adjust the Timing Diagram menu to show data from this pod.

4. Set the magnification of the Timing Diagram to 10; this should show a display like Figure 5-28. The actual position of the cursor and trigger will depend on the type of acquisition module used. A 91A08 should trigger on sequence 18 and a 91A32 should trigger on sequence 14.

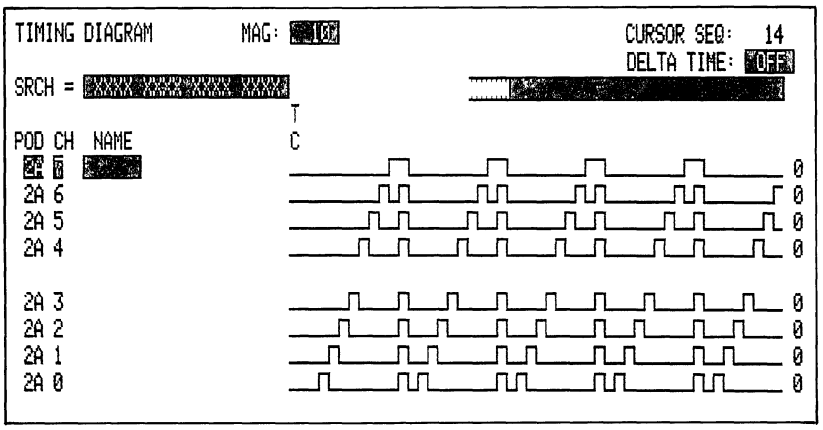


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Figure 5-28. 91P16 data output test.

The previous steps verified the operation of the clock, data and the inversion of the strobe. The next few steps verify the operation of the non-inverted strobe.

5. Enter the Pattern Generator Timing menu. Set the shape of strobe 1 to active high.

6. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 0 (active low).

7. Press START SYSTEM.

8. The data acquired should match Figure 5-28.

(6) Verifying Pod Connector B

The next steps verify that the 91P16 can transmit data, strobes, and clock signals through pod connector B.

1. Remove the TTL/MOS pattern generator probe from pod connector C of the pattern generator. Reconnect the probe to pod connector B of the 91P16.

2. When the probe is installed in pod connector B, the mainframe should beep and show the message POD 1B CONNECTED.

3. Press the Pod ID button on the back of the pattern generator probe housing. The mainframe should beep and display the message POD 1B.

4. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 1 (active high).

5. Press the START SYSTEM key.

6. Enter the Timing Diagram menu.

7. Press the Pod ID button on the back of the data acquisition probe. Read the pod number off the DAS screen. Adjust the Timing Diagram menu to show data from this pod.

8. Set the magnification of the Timing Diagram to 10; this should again show a display like Figure 5-28. The actual position of the cursor and trigger will depend on the type of acquisition module used. A 91A08 should trigger on sequence 18 and a 91A32 should trigger on sequence 14.

The previous steps verified the operation of the clock, data and the inversion of the strobe. The next few steps verify the operation of the non-inverted strobe.

9. Enter the Pattern Generator Timing menu. Set the shape of strobe 0 to active high.

10. Enter the Trigger Specification menu. Set the qualifier for the Data Acquisition probe to 0 (active low).

11. Press START SYSTEM.

12. The data acquired should match Figure 5-28.

NOTE

If the 91P16 module under test was used in slot 1 in the Trigger/Time Base functional check, some of the tests in this procedure have already been performed. Steps already performed in the Trigger/Time Base functional check are indicated with an asterisk (*) after the step number. These steps need not be duplicated.

If you are finished, you may dismantle the test setup. Turn off the DAS mainframe before removing any modules to prevent damage to the modules or the mainframe.

(7)* Verifying the PG INHIBIT Line

The next steps verify that the 91P16 responds to the PG INHIBIT signal through the External Clock Probe.

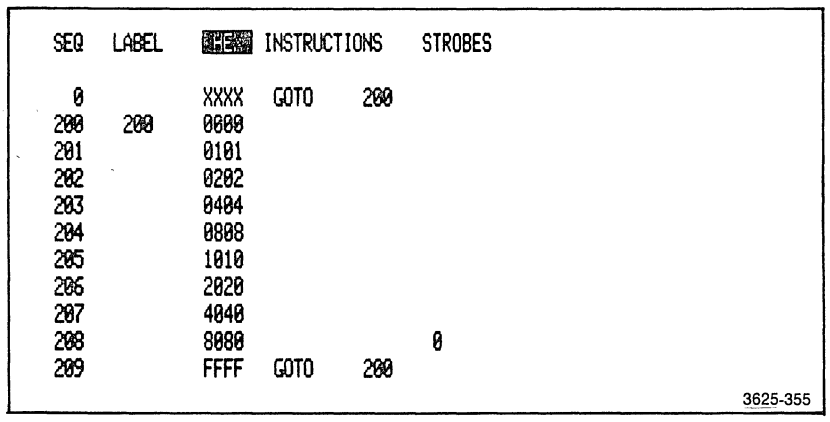
1. Disconnect the strobe lead of the pattern generator probe from the qualifier lead of the data acquisition probe.

2. Connect the strobe lead from the pattern generator probe (the white flying lead) to the PG INHIBIT lead from the External Clock Probe (the red lead).

3. Enter the Pattern Generator menu. Set the INHIBIT field in the Pattern Generator Program menu to 0.

4. Use the DEL LINE key to remove lines 210 and 208 (data AAAA and 5555).

5. Call strobe 0 on the new 208 line of the pattern generator program. The program should now look like the listing below.



6. Enter the Pattern Generator Timing menu and set strobe 0 to the following state:

7. Press START SYSTEM to start the DAS.

8. When data acquisition is finished, enter the Timing Diagram menu. The display should look like Figure 5-29.

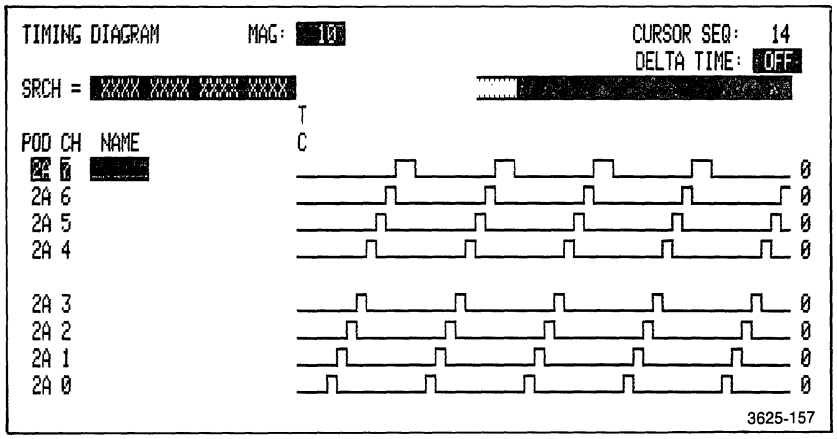


Figure 5-29. 91P16 inhibit test results.

A display like Figure 5-29 indicates that the inhibit signal is being properly processed by the 91P16. The next steps verify the operation of the inversion of the inhibit signal.

9. Enter the Pattern Generator Program menu and set the INHIBIT field to 1.

10. Enter the Pattern Generator Timing menu and set the SHAPE field of strobe 0 to high true.

11. Press START SYSTEM.

12. When data acquisition is finished, enter the Timing Diagram menu. The display should again look like Figure 5-29.

(8)* Verifying the PG PAUSE Line

The next steps verify that the 91P16 responds to the PG PAUSE signal through the External Clock Probe.

1. Disconnect the strobe line from the inhibit line. Reconnect the strobe line (the white flying lead from the pattern generator probe) to the PG PAUSE line of the External Clock Probe (the yellow lead).

2. Enter the Pattern Generator Program menu and set the PAUSE field to 0.

3. Enter the Pattern Generator Timing menu and set the SHAPE of strobe 0 to low true.

4. Press START SYSTEM.

5. When displayed on the Timing Diagram menu, the data acquired from the pattern generator should look like the data shown in Figure 5-30.

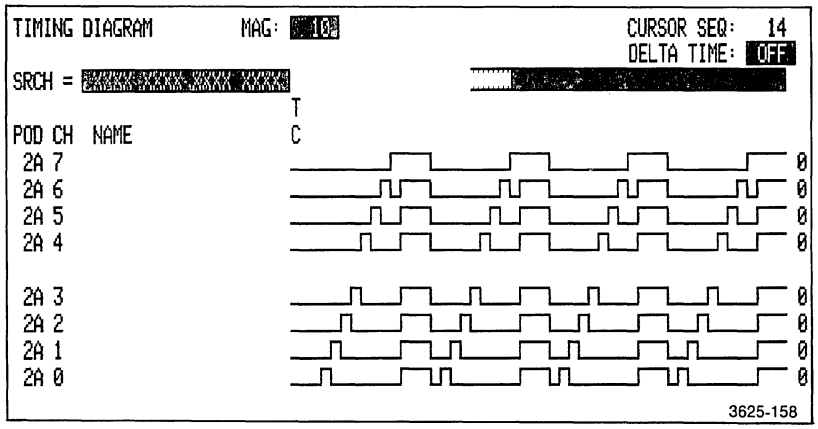


Figure 5-30. 91P16 pause test results.

A display like Figure 5-30 means the pause signal is being properly received and reacted to. Note in particular that the FF value is twice the width of the other data.

The next steps verify the operation of the inversion of the pause signal.

6. Enter the Pattern Generator Program menu and set the PAUSE field to 1.

7. Enter the Pattern Generator Timing menu and set the SHAPE of strobe 0 to high true.

8. Press START SYSTEM.

9. Enter the Timing Diagram menu when acquisition is finished. The display should match Figure 5-30.

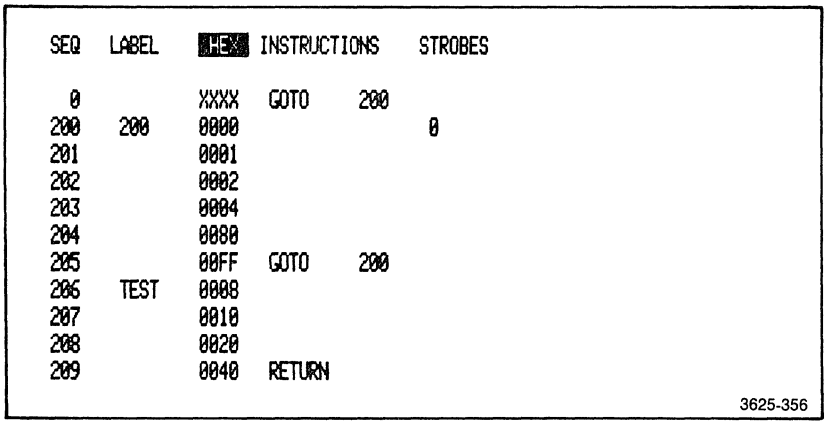
(9)* Verifying the PG INTERRUPT Line

The next steps verify that the 91P16 responds to the PG INTERRUPT signal through the External Clock Probe.

1. Disconnect the strobe line from the pause line. Reconnect the strobe line (the white flying lead from the Pattern Generator probe) to the PG INTERRUPT line of the External Clock Probe (the orange line).

2. Enter the Pattern Generator Program menu. Set the CALL field in the Pattern Generator menu to call TEST on a falling edge.

3. Set the pattern generator program to match the following display.



4. Enter the Pattern Generator Timing menu. Set the shape of strobe 0 to low true.

5. Press START SYSTEM.

6. When displayed on the Timing Diagram menu, the data acquired from the pattern generator should look like the data shown in Figure 5-31.

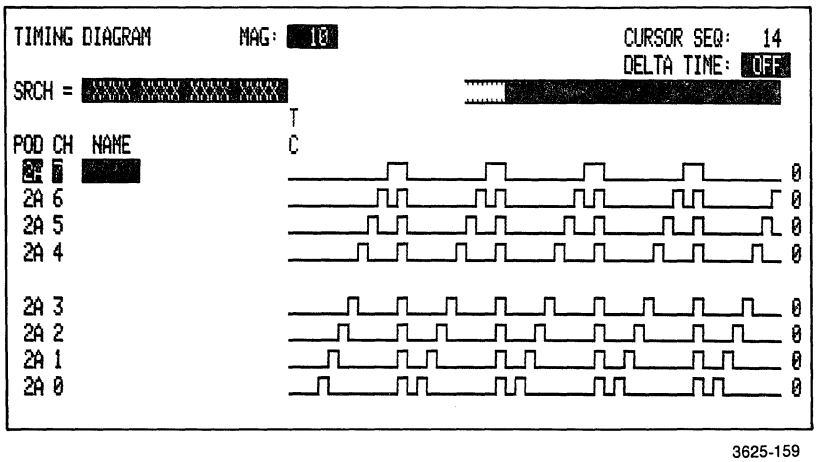


Figure 5-31. 91P16 interrupt test results.

A display like Figure 5-31 means the interrupt signal is being properly received and processed. The next steps verify the operation of the inversion of the interrupt signal.

7. Enter the Pattern Generator Program menu and set the CALL field to call TEST on a rising edge.

8. Enter the Pattern Generator Timing menu and set the SHAPE of strobe 0 to high true.

9. Press START SYSTEM.

10. When acquisition is finished, enter the Timing Diagram menu. The data acquired should look like Figure 5-31.

(10)* Verifying the PG CLK Line

The next steps verify the transmission of the PG CLK signal through the External Clock Probe. These steps require the use of an external clock source. The recommended clock source is a square wave or pulse generator with an output that oscillates between ground and +5 V.

1. Disconnect the strobe line from the interrupt line.

2. Connect the output of the signal generator to the PG CLK line (brown) on the P6452 External Clock Probe.

3. The signal generator must have a common ground with the probes. To accomplish this, connect the ground of the signal generator to the two clips that connect the data acquisition probe ground sense to the External Clock Probe ground line.

The probes and the signal generator are now connected so the test can be performed.

4. Enter the Pattern Generator Program menu. Set the pattern generator clock to external rising edge. Set the CALL field to X (don't care).

5. Adjust the pattern generator program to match the following display:

SEQ	LABEL	[redacted]	INSTRUCTIONS		STROBES
0		XXXX	GOTO	200	
200	200	0000			
201		0001			
202		0002			
203		0004			
204		0008			
205		0010			
206		0020			
207		0040			
208		0080			
209		00FF	GOTO	200	

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6. Enter the Trigger Specification menu and set the acquisition clock to external rising edge.

7. Press START SYSTEM.

8. When acquisition is finished, examine the Timing Diagram menu. The data acquired from the Pattern Generator should look like the data shown in Figure 5-32.

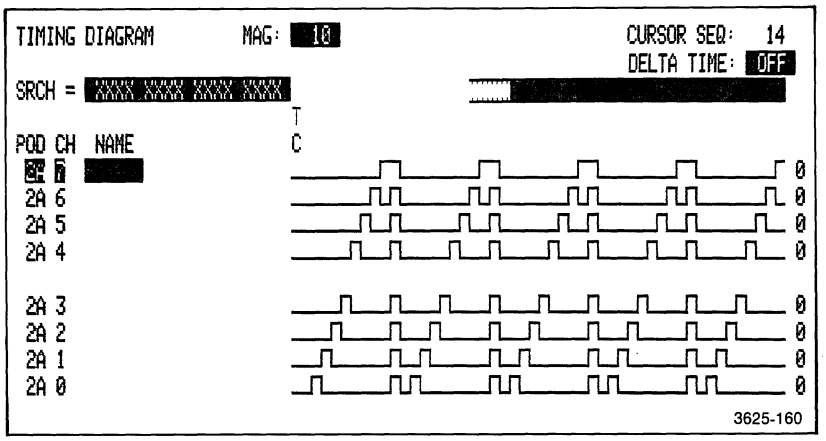

Figure 5-32. Pattern generator external clock line test results.

A display like Figure 5-32 means the pattern generator external clock is being properly received and processed. The next steps verify the operation of the inversion of the external clock signal.

9. Enter the Pattern Generator Program menu and set the pattern generator clock to external falling edge.

10. Press START SYSTEM.

11. When acquisition is finished, examine the Timing Diagram menu. The data acquired from the Pattern Generator should again look like the data shown in Figure 5-32.

This completes the functional check procedure for the 91P16 Pattern Generator Module. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

91P32 PATTERN GENERATOR EXPANDER MODULE FUNCTIONAL CHECK

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe
- 91P16 Pattern Generator Module
- Diagnostic Lead Set
- P6455 TTL/MOS Pattern Generator Probe
- P6452 External Clock Probe
- P6452 Data Acquisition Probe

and either of the following

- 91A32 Data Acquisition Module; or
- 91A08 Data Acquisition Module and P6454 100 MHz Clock Probe

Refer to the Operating Instructions section of this manual for instructions on module installation and on the use of the Diagnostics menu. Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes together with the diagnostic lead set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe in the way used for this functional check. If, due to insufficient +5 V power supply modules or some other constraint, the mainframe is not configured in the recommended way, then steps later in the functional check will need modification. For the greatest ease in the functional check procedure, configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the mainframe.
2. Install the 91P16 in slot 1 of the mainframe.

NOTE

The mainframe will not operate with more than one 91P16 Pattern Generator Module installed at the time of power-up. After inserting the modules used for this test, make sure there are no duplicates of this board in the mainframe.

3. Install the acquisition module to be used for testing. If a 91A08 module is used, install it in slot 6. If a 91A32 module is used, install it in slot 2.
4. Install the 91P32 to be checked in any empty slot of the DAS mainframe that receives +5 V power. If there is another 91P32 module in the mainframe, remove it.

NOTE

For the purposes of this procedure, it is assumed that the 91P32 module is in slot 3. However, the 91P32 module may be tested in any other powered slot. This procedure will be easier to follow if the 91P32 module is installed in slot 3.

(2) Executing the Diagnostic Self-Test

The next steps run all available self-test diagnostics on the 91P32 module.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run diagnostic tests on slot 3, the 91P32 module.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. The diagnostic test, VECTOR RAM, should pass.

(3) Probe Setup for the Functional Check

These steps provide the initial probe setup for these tests.

NOTE

For further details on connecting probes together with the Diagnostic Lead Set, refer to the beginning of this Verification and Adjustment Procedures section.

1. Connect the TTL/MOS pattern generator probe to pod connector D of the 91P32. When the probe is installed, the mainframe should beep and show the message POD 3D CONNECTED.

2. Press the Pod ID button on the back of the probe housing. The mainframe should beep and display POD 3D.

3. Set the diagnostic slide switch on the back of the TTL/MOS pattern generator probe to AUX.

4. Connect the data acquisition probe to the acquisiton module (either a 91A08 module or a 91A32 module). If a 91A32 module is used, install the data acquisition probe in pod connector A.

5. Connect the pattern generator probe to the data acquisition probe with the diagnostic lead set.

6. Connect the strobe line of the pattern generator probe (the white flying lead from the pattern generator side of the Diagnostic Lead Set) to the qualifier line of the data acquisition probe (the white flying lead from the acquisition side of the Diagnostic Lead Set).

7. Connect the External Clock Probe to pod connector C of the Trigger/Time Base Module.

8. Install a flying lead set in the External Clock Probe. Also install a ground lead in the GND DIAGNOSTIC connector on the clock probe.

9. Install a ground lead in one of the GND SENSE connectors of the data acquisition probe. Connect the ground lead of the External Clock Probe to the ground lead of the data acquisition probe.

NOTE

If a 91A32 module is being used for the test, perform only step 10, then proceed to the initial menu setup. If a 91A08 module is being used for the test, skip step 10 and perform steps 11 through 13.

10. If a 91A32 module is being used for the test, connect the CLK1 line of the External Clock Probe (the black lead) to the clock line of the pattern generator probe (the gray flying lead on the pattern generator side of the Diagnostic Lead Set).

NOTE

If a 91A32 is being used for this procedure, then the probe setup is complete.

11. If a 91A08 module is being used as the acquisition module in the functional check, connect the 100 MHz Clock Probe to its connector on the 91A08 module in slot 6.

12. Connect the IN line of the 100 MHz Clock Probe to the clock output of the pattern generator probe (the gray flying lead from the pattern generator side of the Diagnostic Lead Set).

13. Connect the REF line of the 100 MHz Clock Probe to the unused GND SENSE line of the data acquisition probe.

(4) Initial Menu Setup for the Functional Check

The next steps organize the menus so the remainder of the functional check will require a minimum of menu manipulation.

1. Leave the Diagnostics menu by pressing the PATTERN GENERATOR key. In the Pattern Generator Program menu, verify that the pattern generator clock is set to 1 μs.

2. Adjust the program already present in the Pattern Generator Program menu to match the following display.

SEQ	LABEL	HEX	HEX	HEX	INSTRUCTIONS		STROBES
0		XXXX	XXXX	XXXX	GOTO	200	
200	200	0000	0000	0000			
201		0101	0101	0001			
202		0202	0202	0002			
203		0404	0404	0004			
204		0808	0808	0008			
205		1010	1010	0010			
206		2020	2020	0020			
207		4040	4040	0040			
208		5555	5555	0000			2345
209		8080	8080	0080			
210		AAAA	AAAA	0000			2345
211		FFFF	FFFF	00FF	GOTO	200	

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3. Enter the Pattern Generator Timing menu and set strobes 2, 3, 4, and 5 to the following state.

DELAY	WIDTH	SHAPE
70nS	1.000µS	LJ

4. Enter the Trigger Specification menu. If the functional check is performed with a 91A32 module, leave the MODE field set to 91A32 ONLY. If the functional check is being performed with a 91A08 module, set the MODE field to 91A08 ONLY.

5. In the Trigger Specification menu, set the acquisition clock to external rising edge.

6. Press the Pod ID button on the back of the data acquisition probe.

7. Read the pod number off the DAS screen. Set the qualifier corresponding to that pod to 1.

(5) Verifying Pod Connector D

The next steps verify that the 91P32 can transmit data, strobes, and clock signals through pod connector D.

1. Press the START SYSTEM key.

2. Enter the Timing Diagram menu.

3. Press the Pod ID button on the back of the Data Acquisition probe. Read the pod number off the DAS screen. Adjust the Timing Diagram menu to show data from this pod.

4. Set the magnification of the Timing Diagram to 10; this should show a display like Figure 5-33. The actual position of the cursor and trigger will depend on the type of acquisition module used. A 91A08 should trigger on sequence 18, and a 91A32 should trigger on sequence 14.

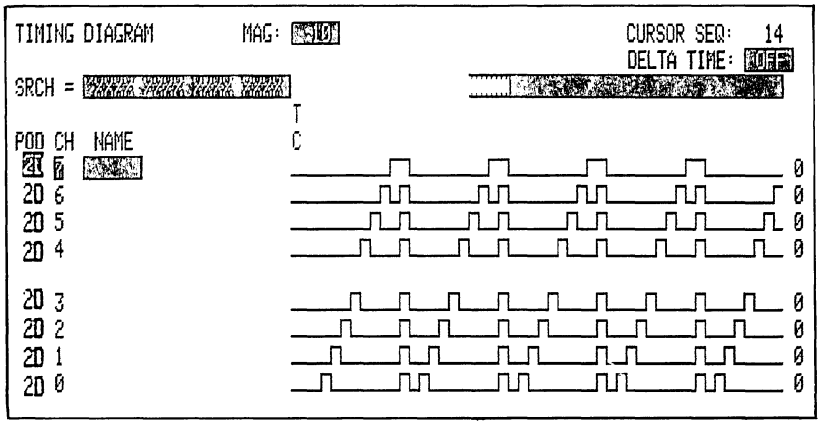


Figure 5-33. 91P32 data output test.

The previous steps verified the operation of the clock, data, and inversion of the strobe. The next few steps verify the operation of the non-inverted strobe.

5. Enter the Pattern Generator Timing menu. Set the shape of strobe 5 to active high.

6. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 0 (active low).

7. Press START SYSTEM.

8. The data acquired should match Figure 5-33.

(6) Verifying Pod Connector C

The next steps verify that the 91P16 can transmit data, strobes, and clock signals through pod connector C.

1. Remove the TTL/MOS Pattern Generator probe from pod connector D of the 91P32 module. Reconnect the probe to pod connector C of the 91P32 module.

2. When the probe is installed in pod connector C, the mainframe should beep and display the message POD 3C CONNECTED.

3. Press the Pod ID button on the back of the pattern generator probe housing. The mainframe should beep again and display POD 3C.

4. Enter the Trigger Specification menu and set the qualifier for the acquisition probe to 1 (active high).

5. Press START SYSTEM.

6. Enter the Timing Diagram menu. The display should again look like Figure 5-33.

The previous steps verified the operation of the clock, data, and the inversion of the strobe. The next few steps verify the operation of the non-inverted strobe.

7. Enter the Pattern Generator Timing menu. Set the shape of strobe 4 to active high.

8. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 0 (active low).

9. Press START SYSTEM.

10. The data acquired should match Figure 5-33 again.

(7) Verifying Pod Connector B

The next steps verify that the 91P16 can transmit data, strobes, and clock signals through pod connector B.

1. Remove the TTL/MOS pattern generator probe from pod connector C of the 91P32 module. Reconnect the probe to pod connector B of the 91P32 module.

2. When the probe is installed in pod connector B, the mainframe should beep and display the message POD 3B CONNECTED.

3. Press the Pod ID button on the back of the pattern generator probe housing. The mainframe should beep again and display POD 3B.

4. Enter the Trigger Specification menu and set the qualifier for the acquisition probe to 1 (active high).

5. Press START SYSTEM.

6. Enter the Timing Diagram menu. The display should again look like Figure 5-33.

The previous steps verified the operation of the clock, data, and the inversion of the strobe. The next few steps verify the operation of the non-inverted strobe.

7. Enter the Pattern Generator Timing menu. Set the shape of strobe 3 to active high.

8. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 0 (active low).

9. Press START SYSTEM.

10. The data acquired should match Figure 5-33 again.

(8) Verifying Pod Connector A

The next steps verify that the 91P32 can transmit data, strobes, and clock signals through pod connector A.

1. Remove the TTL/MOS pattern generator probe from pod connector B of the 91P32 module. Reconnect the probe to pod connector A of the 91P32 module.

2. When the probe is installed in pod connector A, the mainframe should beep and display the message POD 3A CONNECTED.

3. Press the Pod ID button on the back of the pattern generator probe housing. The mainframe should beep again and display POD 3A.

4. Enter the Trigger Specification menu and set the qualifier for the acquisition probe to 1 (active high).

5. Press START SYSTEM.

6. Enter the Timing Diagram menu. The display should again look like Figure 5-33.

The previous steps verified the operation of the clock, data, and the inversion of the strobe. The next few steps verify the operation of the non-inverted strobe.

7. Enter the Pattern Generator Timing menu. Set the shape of strobe 2 to active high.

8. Enter the Trigger Specification menu. Set the qualifier for the data acquisition probe to 0 (active low).

9. Press START SYSTEM.

10. The data acquired should match Figure 5-33.

This completes the functional check procedure for the 91P32 Pattern Generator Expander Module. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

DAS PROBE FUNCTIONAL CHECK

NOTE

If any of the probes to be functionally checked were used to verify a Trigger/Time Base, an acquisition module, or a pattern generator module, then those probes are assured to be functional. In that case, this procedure need not be performed for those probes.

Due to the large quantity of different types of probes that may be found in any DAS 9100 system, this functional check procedure is designed to test any of the following probe types.

- P6452 External Clock Probe
- P6452 Data Acquisition Probe
- P6454 100 MHz Clock Probe
- P6455 TTL/MOS Pattern Generator Probe
- P6456 ECL Pattern Generator Probe

You will need the following equipment to perform this procedure:

- DAS 9100 mainframe
- 91P16 Pattern Generator Module
- 91A08 Data Acquisition Module
- Diagnostic Lead Set

NOTE

If necessary, a 91A32 module and an External Clock Probe can be substituted for the 91A08. However, if a 91A08 module is not used in the test setup, P6454 100 MHz Clock Probes cannot be checked.

At least one acquisition probe or External Clock Probe and one pattern generator probe are required for this procedure. These probes may include the probes to be functionally checked.

NOTE

The procedure checks all of the connected probes simultaneously.

The pattern generator probe outputs data that is acquired by the data acquisition probe. The 100 MHz Clock Probe acquires its clock from the pattern generator probe as well. A failure in this functional check may indicate a failure in any of the probes under test.

Refer to the beginning of this Verification and Adjustment Procedures section for information on connecting probes together with the Diagnostic Lead Set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe in the way used for this functional check. If, due to insufficient +5 V power supply modules or some other constraint, the mainframe is not configured in the recommended way, then steps later in the functional check will need modification. For the greatest ease in the functional check procedure, configure the mainframe according to the following steps.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the mainframe.
2. Install the 91P16 module in slot 1 of the mainframe.

NOTE

The mainframe will not operate with more than one 91P16 Pattern Generator Module installed at the time of power-up. After inserting the modules used for this test, make sure there are no duplicates of this board in the mainframe.

3. Install the 91A08 module in slot 6 of the mainframe. If a 91A08 is not available, install the 91A32 module in slot 2 of the mainframe.

(2) Installing the Pattern Generator Probe

NOTE

For further details on connecting probes with the Diagnostic Lead Set, refer to the beginning of this Verification and Adjustment Procedures section.

1. Turn on the mainframe. All modules should pass the power-up self-test.
2. Connect a pattern generator probe (either P6455 or P6456) to pod connector B of the 91P16 module.
3. When the pattern generator probe is connected, the mainframe should beep and display the message POD 1B CONNECTED.
4. Press the Pod ID button on the back of the probe housing. The mainframe should beep again and display the message POD 1B.
5. Set the diagnostic slide switch on the back of the pattern generator probe housing to AUX.

(3) Installing the P6452 Probe

1. Connect a P6452 probe (either data or external clock) to pod connector C of the 91A08. If a 91A32 is used in place of the 91A08, connect the P6452 probe to pod connector A of the 91A32.

2. When the P6452 probe is connected, the mainframe should beep and display the message POD XX CONNECTED, where XX stands for the slot and pod connector the probe was installed in.

3. Press the Pod ID button on the back of the P6452 probe housing. The mainframe should beep again and display the message POD XX.

(4) Installing the Clock Probe

1. Install the P6454 100 MHz Clock Probe in the coaxial connector of the 91A08 module in slot 6.

2. If a 91A08 module is not available for this test, install a P6452 External Clock Probe in the Trigger/Time Base Module (slot 7, connector C).

(5) Connecting the Probes

These steps connect all of the probes together in the proper configuration for this test.

1. Using the Diagnostic Lead Set, connect the pattern generator probe being tested to the P6452 probe being tested. Do not connect the grounds of the diagnostic lead set to the probes.

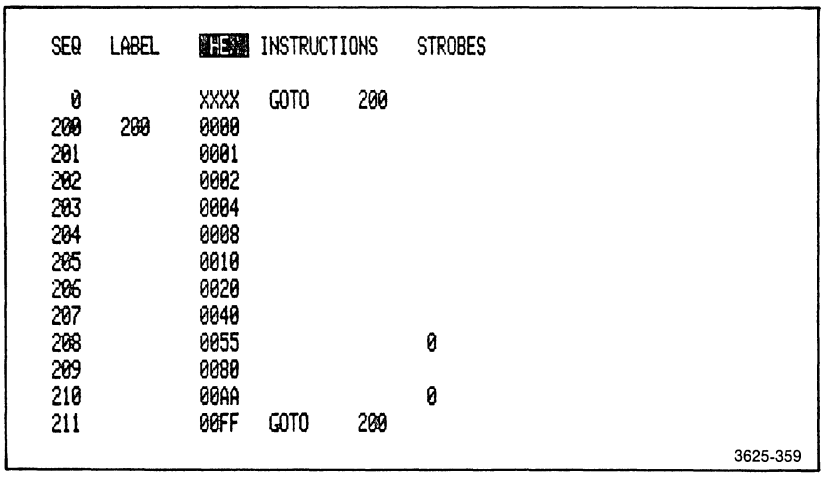
2. Connect the strobe line of the pattern generator probe (the white flying lead from the pattern generator side of the Diagnostic Lead Set) to the white flying lead on the acquisition side of the diagnostic lead set (the qualifier line).

3a. If a 91A08 module is being used for this test, connect the IN line of the P6454 100 MHz Clock Probe to the clock output of the pattern generator probe (the gray flying lead). Connect the reference lead of the P6454 100 MHz Clock Probe, the ground sense input of the P6452 probe, and the VL sense lead of the pattern generator probe together.

3b. If a 91A32 is being used for this test, connect the CLK1 lead of the External Clock Probe of the Trigger/Time Base (the black lead) to the clock output of the pattern generator probe (the gray flying lead). Connect the ground sense lead of the External Clock Probe, the ground sense lead of the P6452 probe, and the VL sense lead of the pattern generator probe to this same ground.

(6) Menu Setup for the Functional Test

1. Enter the Pattern Generator Program menu and adjust the program already present to match the following display.If an ECL pattern generator probe and a 91A32 are being used set PAUSE ON: and INHIBIT ON: fields to 0.



2. Enter the Pattern Generator Timing menu. Adjust strobe 0 to the following state.

3. Enter the Trigger Specification menu. Adjust the mode to 91A08 ONLY if a 91A08 module is used, or adjust the mode to 91A32 ONLY if a 91A32 module is used.

4. In the Trigger Specification menu change the acquisition clock to external rising edge.

5. You should still be in the Trigger Specification menu. If a TTL pattern generator probe is being used, leave the field adjacent to the external clock field set to TTL. If an ECL pattern generator probe is being used, change the this field to VAR −1.30 V.

6. Press the Pod ID button on the back of the P6452 probe being tested. Set the qualifier field corresponding to that probe to 0 (active low). Leave all other qualifiers set to X (don't care).

7. If a P6455 TTL/MOS Pattern Generator Probe is being tested, skip this step. If a P6456 ECL Pattern Generator Probe is being tested, enter the Channel Specification menu. Find the group that contains the P6452 probe being checked. Change the threshold of that group to VAR −1.30 V.

(7) Performing the Test

1. Press START SYSTEM.

2. Enter the Timing Diagram menu and adjust the magnification to 10.

3. Adjust the timing diagram display to show data acquired from the pattern generator by the 91A08 (or 91A32). The display should look like Figure 5-34.

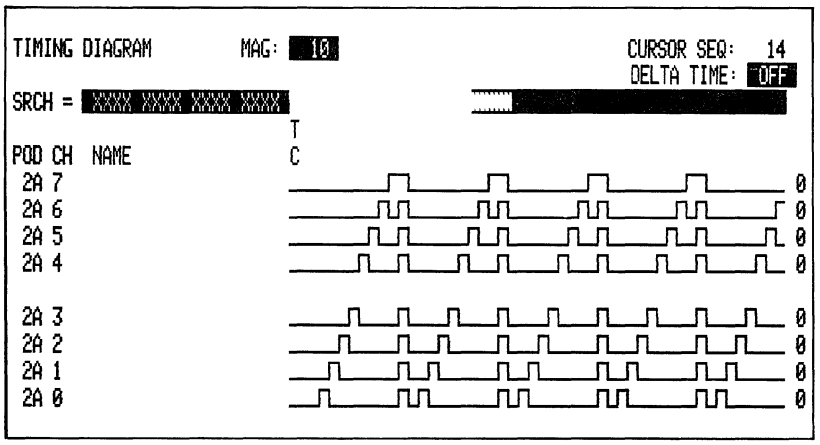


Figure 5-34. Probe verification display.

4. A display like Figure 5-34 means that the acquisition probe, the pattern generator probe, and (if used) the P6454 100 MHz Clock Probe are all functional.

NOTE

To perform tests on multiple probes, remove a probe from its module connector and its lead set connector(s) and replace it with the next probe to be tested. Do not change the lead set configuration. This reduces the time required to remake connections.

This completes the functional check procedure for the probes. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules to prevent damage to the modules or the mainframe.

TAPE DRIVE (OPTION 01) FUNCTIONAL CHECK

You will need the following equipment to perform this procedure:

- DAS mainframe with the tape drive installed.

- Formatted DC100 type tape cartridge with no data stored.

For instructions on use of the Diagnostics menu, refer to the Operating Information section of this manual.

(1) Menu Setup for the Functional Test

1. Turn on the DAS mainframe containing the tape drive while holding down the STOP key. This causes the power-up self-test to fail.
2. After the self-test is finished, press START SYSTEM to enter the Diagnostics menu.
3. Select to run diagnostic tests on slot 0 (the Controller).
4. Set the MODE field to SINGLE and run function 3, the TAPE WRITE test.

(2) Performing the Functional Test

1. Set the sliding tab on the tape cartridge in the record position. Insert the cartridge in the drive.
2. Press START SYSTEM.
3. The test should run approximately 4 minutes. After this time, the screen message changes from TAPE OPERATION IN PROGRESS to WAITING. There should be no hard or soft errors shown.
4. Press STOP. The tape drive has now been verified.

This completes the functional check procedure for the tape drive.

I/O INTERFACE (OPTION 02) FUNCTIONAL CHECK

This functional check procedure has two parts. The first part requires only the equipment listed below:

- DAS mainframe with the I/O Interface installed

The second part of the functional check is optional, since it requires some specialized equipment. The equipment required for the second part of the test is given in the following list.

- TEKTRONIX 4051 Desktop Computer with Option 01 (Data Communications Interface)
- RS-232 cable
- GPIB cable
- null modem (constructed according to Figures 5-37 and 5-38).

NOTE

All Basic programs found in this text must be run on a Tektronix computer, to avoid incompatabilities with other versions of Basic.

The 4051 stimulates and reads the RS-232 and GPIB ports of the DAS I/O Interface. The null modem allows the 4051 and the DAS to communicate without a modem.

For instructions on use of the DAS menus, refer to the Operating Information section of this manual.

(1) Part 1 of the Functional Check

1. On the back of the DAS mainframe, set the address switches to address 01. This is done by setting the DIP switch on the back of the DAS to the following state. (Switches 1, 2, and 3 can be left in an indeterminate state.)

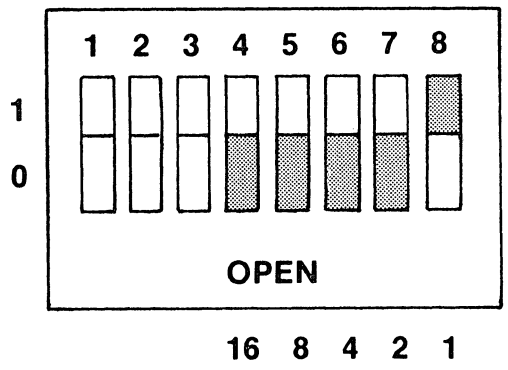


Figure 5-35. Setting GPIB address 01.

2. Remove any connectors attached to the GPIB or RS-232 ports on the back panel of the mainframe.

3. Turn on the mainframe.

4. Shortly after the power-up sequence is finished, the SRQ light on the back panel should turn on.

5. Press the INPUT OUTPUT key to enter the Input Output menu.

6. The Input Output menu should show a message at the top that says GPIB TALK/LISTEN ADDRESS: 1.

7. On the back panel of the DAS mainframe, change the setting of the DIP switch to the following state.

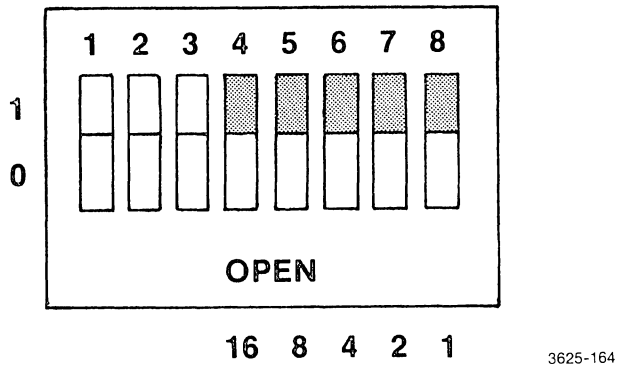


Figure 5-36. Setting GPIB off line.

8. The message on the Input Output menu should change to say GPIB OFFLINE and the SRQ light should go off.

NOTE

The next part of the I/O Interface functional check is optional. To perform the following tests a TEKTRONIX 4051 Desktop Computer with the Data Communications Interface (Option 01) must be used.

If your test setup does not include a 4051, the functional check is complete.

(2) Part 2 of the Functional Check

1. Turn off the DAS. Do not turn on any of the other instruments yet.

2. The 4051 Option 01 has two possible output configurations; that of a terminal, or that of a modem. The standard output of the communications option is like a modem. If you are using the standard output of the 4051, then construct the null modem shown in Figure 5-37.

   The 4051 Option 01 has an interconnect cable as a standard accessory. The connector at the end of this cable makes the output of the 4051 look like a terminal. If this cable is used in the test set up, then construct the null modem shown in Figure 5-38.

3. Attach the null modem to one end of the RS-232 cable. Connect the RS-232 cable with the null modem between the DAS RS-232 port and the 4051 RS-232 port.

4. Connect the GPIB cable between the DAS GPIB port and the 4051 GPIB port.

5. Turn on the 4051.

6. Load the program given in Table 5-4 into the 4051.

7. Run the program just loaded into the 4051.

8. Enter 1 followed by a carriage return in the 4051 for the address of the DAS.

9. Set the GPIB address on the back of the DAS to 01, as shown in Figure 5-35.
10. Turn on the DAS and wait for the 4051 to indicate POWER ON.

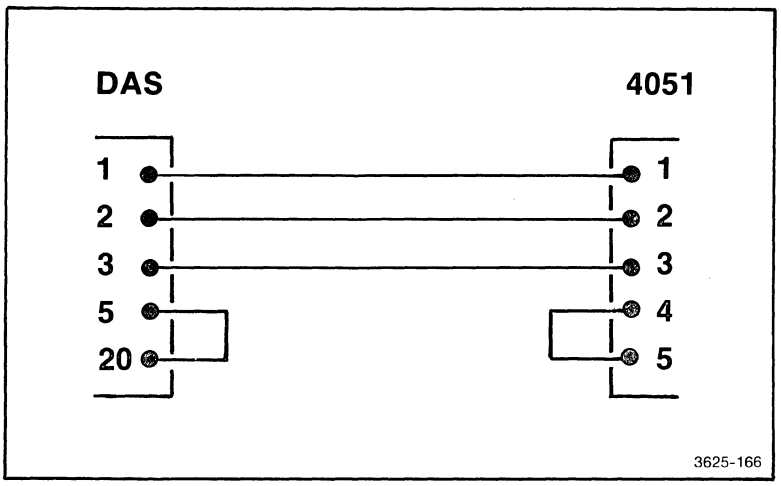


Figure 5-37. Connector between the DAS and the modem output of the 4051.

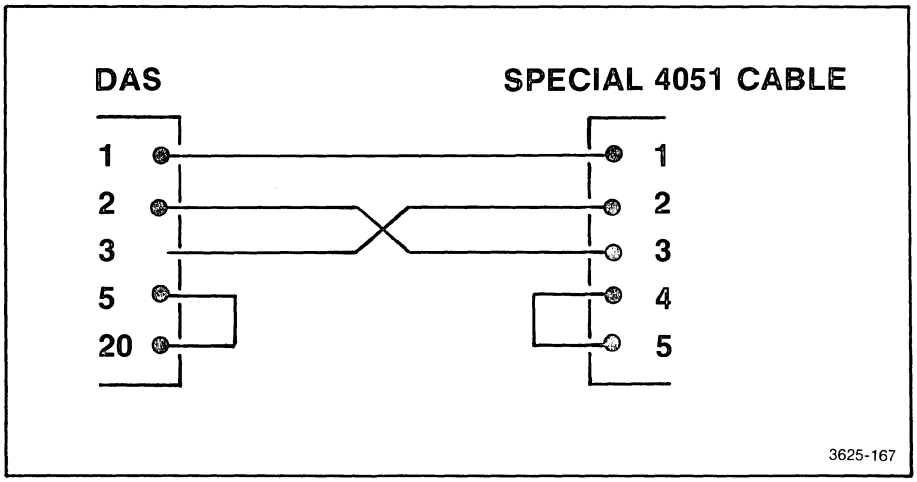


Figure 5-38. Connector between the DAS and the terminal output of the 4051 interconnect cable.

11. On the 4051, press user defined key #1. This initiates the GPIB test.

12. While the test is running, examine the 4 LEDs on the back of the DAS. All of the LEDs should flash independently. Some of the LEDs are brighter than others, but all should light to some degree.

    The GPIB test may be restarted as desired by pressing user defined key #1 again.

The GPIB port on the DAS has now been verified as operational. The next steps verify the operation of the RS-232 port.

13. On the 4051, press user defined key #2. This initiates the RS-232 test.

14. Set the GPIB address on the back of the DAS to 31 (off line), as shown in Figure 5-36.

15. Press the INPUT OUTPUT key on the DAS to enter the Input Output menu. The message at the top of the menu shold read GPIB OFFLINE.

16. Set the DEVICE field to RS-232. Set the BAUD RATE field to 2400.

17. The DAS is now ready for the test. Press carriage return on the 4051.

18. Watch the DAS screen carefully. The screen should change to the power-up display. Then the screen should become blank and flash the message RS-232 IS ON THE AIR. The message has a very short duration. The DAS screen should then return to its original state.

19. If the DAS screen is not watched carefully, the message may be missed. The RS-232 test can be performed again by pressing the user defined key #1 followed by a carriage return on the 4051.

This completes the functional test of the DAS I/O Interface, Option 02. The test setup may now be dismantled.

(3) I/O Interface Test Program

This is a listing of the program used to test the GPIB and RS-232 interfaces of Option 02.

NOTE

This Basic program is written for Tektronix 4050-series graphic computing systems only. The program must be run on a Tektronix computer, to avoid incompatabilities with other versions of Basic.

After loading the test program into the 4051, it is highly recommended that the program be saved on a 4051 tape. This eliminates the need of entering the program a second time should this test need to be performed again.

Table 5-4
GPIB and RS-232 Test Program

```
1       ON SRQ THEN 3000
2       GO TO 99
4       GO TO 1000
8       GO TO 2000
12      GO TO 1000
99      PAGE
100     PRINT "DAS9100 RS-232/GPIB CHECKOUT PROGRAM V1.0"
110     PRINT " ************************************************************ "
120     PRINT
130     PRINT "USE USER DEFINED KEYS TO INITIATE TESTS"
140     PRINT " ------------------------------------------------------------ "
150     PRINT
160     PRINT "UDK #1 - GPIB/LED CHECKOUT SEQUENCE"
170     PRINT "UDK #2 - RS-232 CHECKOUT SEQUENCE"
190     PRINT
210     PRINT
220     PRINT "ENTER ADDRESS FOR DAS: ";
230     INPUT D1
240     PRINT
250     PRINT "PLEASE TURN ON DAS"
260     WAIT
270     END
990     REM ***** CHECKOUT IEEE 488 INTERFACE *****
1000    ON SRQ THEN 2280
1005    PAGE
1010    PRINT "DAS GPIB LIGHT TEST"
1011    PRINT "** IF BUS HANGS, THEN FAILURE SHOULD BE ASSUMED **"
1020    WBYTE @17:
1030    FOR I=1 TO 72
1040    WBYTE @D1+32:-255
1050    WBYTE @D1+64:
1060    RBYTE X
1062    X=ABS(X)
1065    IF X<>255 THEN 1140
1070    PRINT ". ";
1080    FOR J=1 TO 50
1090    NEXT J
1100    NEXT I
1110    PRINT
1120    PRINT "TEST COMPLETED"
1130    END
1140    PRINT
1150    PRINT "FAILURE - DATA LINES NOT CORRECT"
1160    PRINT "DATA BUS SHOULD BE: 255 INSTEAD OF: ";X
1990    REM ***** CHECKOUT THE RS-232 INTERFACE *****
2000    PAGE
2005    PRINT "RS-232 CHECKOUT SEQUENCE"
```

Table 5-4 (cont)
GPIB and RS232 Test Program

```
2010    PRINT
2020    PRINT "MAKE SURE ADDRESS SWITCHES ON BACK OF THE DAS ARE"
2030    PRINT "SET TO ADDRESS 31 (GPIB OFFLINE) AND THE BAUD RATE"
2040    PRINT "OF THE DAS IS SET TO 2400"
2050    PRINT
2060    PRINT "PRESS <CR> WHEN READY"
2070    INPUT A$
2080    PRINT
2090    CALL "RATE",2400,5,2
2100    CALL "PRLIST"
2110    PRINT @40:"LOCKOUT ON"
2120    PRINT @40:"DEFAULT;ERASE 0,24"
2130    PRINT @40:"MESSAGE 2,20,20,'RS-232 IS ON THE AIR'"
2140    PRINT @40:"SCREEN?"
2150    INPUT @40:A$
2160    A$=SEG(A$,POS(A$,"S",1),10)
2170    IF A$<>"SCREEN ON;" THEN 2260
2180    PRINT @40:"LOCKOUT?"
2190    INPUT @40:A$
2195    A$=SEG(A$,POS(A$,"L",1),11)
2200    IF A$<>"LOCKOUT ON;"THEN 2260
2210    PRINT @40:"LOCKOUT OFF;DEFAULT"
2220    PRINT
2230    PRINT "TEST COMPLETE"
2250    END
2260    PRINT "COMMUNICATIONS ERROR"
2270    END
2280    POLL A,B;D1
2290    RETURN
3000    POLL A,B;D1
3010    POLL A1,B1;D1
3020    IF B1=B THEN 3240
3030    IF B<>65 THEN 3060
3040    PRINT "POWER ON"
3050    GO TO 3220
3060    IF B<>97 THEN 3090
3070    PRINT "COMMAND ERROR"
3080    GO TO 3190
3090    IF B<>98 THEN 3120
3100    PRINT "EXECUTION ERROR"
3110    GO TO 3190
3120    IF B<>99 THEN 3150
3130    PRINT "SYSTEMS ERROR"
3140    GO TO 3190
3150    IF B<>101 THEN 3180
3160    PRINT "POD CHECK"
3170    GO TO 3220
```

Table 5-4 (cont)
GPIB and RS232 Test Program

```
3180    PRINT "SRQ: ";B;
3190    RETURN
3200    INPUT @D1:E$
3210    PRINT " ";A$
3220    ON SRQ THEN 3000
3230    RETURN
3240    PRINT "INTERRUPT FAILURE"
3250    PRINT "CHECK GPIB INTERRUPT PATH"
3260    PRINT "CHECK INTERRUPT MUX PIN #4"
```

ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains procedures for adjusting instrument variables so that the instrument meets or exceeds performance specifications. If the product cannot be made to meet or exceed specifications by following these procedures, repair is necessary.

IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

Purpose

The Adjustment Procedure provides a sequence for adjustments. It is not a troubleshooting guide or a verification procedure. The Adjustment Procedure is divided into sub-sections that describe adjustments for one particular board or set of boards in the DAS. Each sub-section is divided into two parts. The first part of the subsection gives a test or tests that indicate whether an adjustment needs to be made. The second part gives procedures for making the actual adjustment.

Limits and Tolerances

All limits and tolerances given in this procedure are adjustment guides. They should not be interpreted as instrument specifications unless they are also found in the Specification part of this manual.

Tolerances given are for the instrument under test and do not include test equipment error.

Equipment Required

The equipment listed at the very beginning of this Adjustment and Verification Procedures section in Table 5-2, or equivalent, is necessary to complete all the adjustment procedures. A partial list of equipment needed for each individual check and adjustment is also shown at the beginning of each procedure's major step.

The specifications given in Table 5-2 are the minimum necessary to produce accurate results. Therefore, related equipment must meet or exceed the listed specifications. Detailed instructions for operating the test equipment are not offered in this manual. Refer to the manual for the specific test equipment if more information is required.

Equipment Alternatives and Partial Procedures

When equipment other than recommended test equipment is substituted, control settings or adjustment setups may need to be altered. If the exact equipment listed in Table 5-2 is not available, check the Minimum Specification column carefully to see if any other equipment will suffice.

NOTE

With the exception of the Main Power Supply, each DAS module that requires adjustment may be brought within specifications without affecting the adjustment of other modules in the system. The Main Power Supply is the only exception and must have its +12 V supply within specifications before proceeding to adjust the instrument modules in the system.

Adjustment Interval

To ensure correct instrument operation, adjustment should be checked every 1,000 hours of operation or every six months if used infrequently. Before performing the adjustment procedures, perform preventive maintenance as outlined in the Maintenance: General Information section.

Test Sequence

NOTE

These adjustment procedures assume prior knowledge of some aspects of disassembly of the DAS. If further information is required, refer to the disassembly procedures in the Maintenance: General Information section.

The Main Power Supply should be checked prior to performing any of the other adjustments. Other circuit adjustments in the system may then be performed in any order. If any Main Power Supply +12 V adjustment is made, any or all of any DAS module's circuitry may be affected, and the entire Adjustment Procedure for instrument modules in the system should be performed. Again, once the +12 V supply is adjusted, only the module of immediate concern must be adjusted to insure that module's correct operation.

MAIN POWER SUPPLY ADJUSTMENT

Pre-adjustment Test

This test checks whether the Main Power Supply needs to be adjusted. You will need the following equipment to perform this procedure:

- DAS mainframe with Main Power Supply
- Module Extender board
- Digital multimeter (DMM) with leads

The test checks the accuracy of the +12 V supply from the Main Power Supply. The supply must be tested under load conditions, so any modules installed in the system may be left installed. The minimum required load comes from having the Controller and the Trigger/Time Base installed in the system. The test procedure follows.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the Trigger/Time Base Module.
3. Set the jumpers on the Main Extender board to accept a Trigger/Time Base module. Install the Main Extender board in slot 7 of the mainframe.
4. Install the Trigger/Time Base on the top of the extender board.
5. Set the digital multimeter to a range that will read 12 V comfortably and with at least ±0.1% accuracy.
6. Attach the positive lead of the DMM to the +12 V test point on the Main Extender board.
7. Attach the ground lead of the DMM to a GND test point on the extender board.
8. Turn on the DMM and the DAS mainframe. The +12 V supply should be at +12 V, ±1.5%. If the DMM reads in this range, no adjustment of the Main Power Supply is required. If the DMM does not read in this range, the Main Power Supply needs to be adjusted in the manner indicated in the following procedure.

Adjustment

If the previous tests indicate that the Main Power Supply needs adjustment, follow the procedures below. The adjustment of the +12 V Supply may cause voltage spikes on the supply lines, so all voltage sensitive modules are removed during this procedure. You will need the following equipment addition to the equipment required for pre-adjustment test to perform this procedure:

- Main Power Supply Extender board
- 12 Ω, 12 W resistor
- Medium POZIDRIV-type screwdriver
- Small slotted screwdriver

CAUTION

If the +12 V supply is out of tolerance, any or all of the DAS module's operating circuitry may be affected. After correction of the power supply adjustment, the entire Adjustment Procedure for all the instrument modules to be used in the system should be performed.

1. Turn off the DAS mainframe.

2. Remove all instrument modules from the mainframe slots 0 through 7. This includes removing the Controller and Trigger/Time Base Modules.

3. Remove the protective plate over the power supply section of the mainframe by removing five flat-head POZIDRIV screws.

WARNING

Removing the power supply cover will expose the technician to high voltages and currents.

4. If the system contains Option 01, the tape drive, the drive should have its power disconnected. This can be done by locating J422 and J431 (monochrome) or J425 and J427 (color) on the Interconnect (see Figure 5-39) and removing the connectors attached to these jacks.

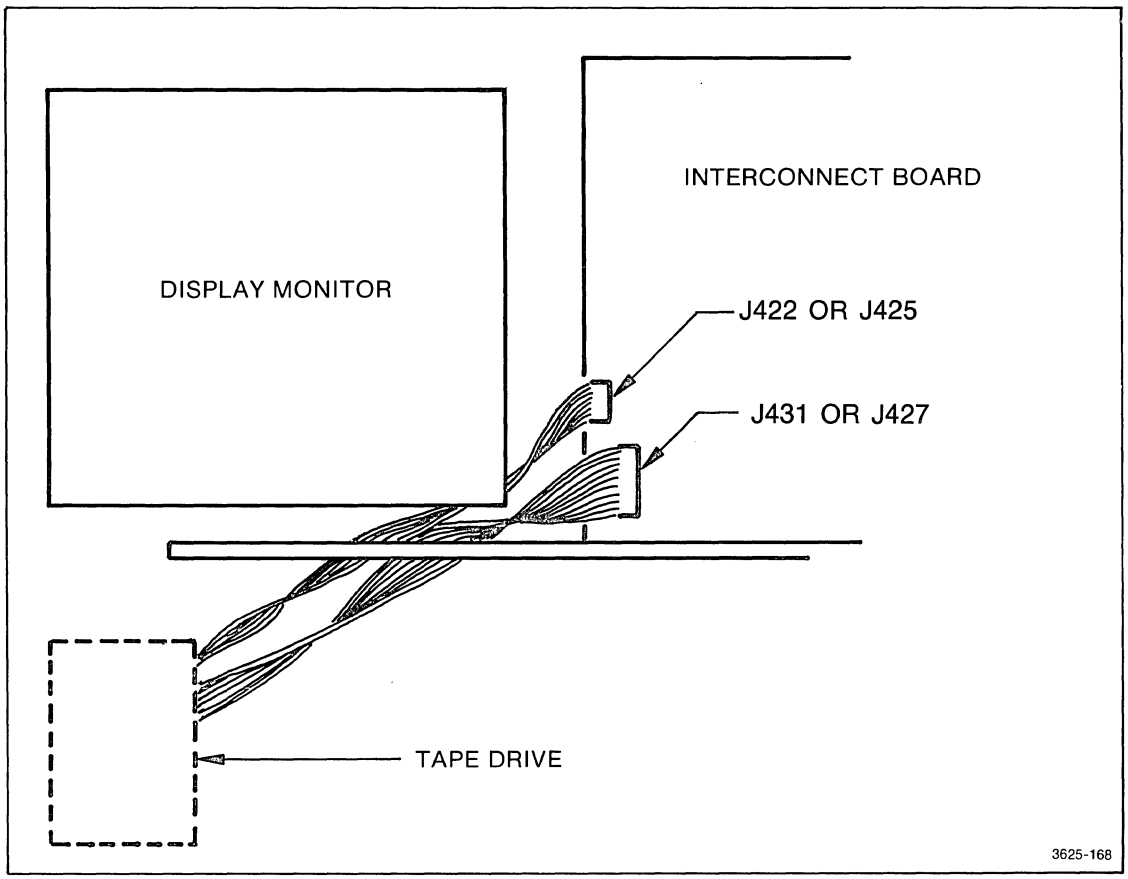


Figure 5-39. Tape drive interconnect connectors.

5. If the system being adjusted contains Option 02, the I/O Interface, this board should also be removed from the Interconnect (see Figure 5-40). The I/O Option board should be pulled straight up, out of the Interconnect's socket.

6. When the board is disconnected, hang the main Option 02 board by its cable over the back of the DAS mainframe. This disconnects the I/O Interface from the power supplies.

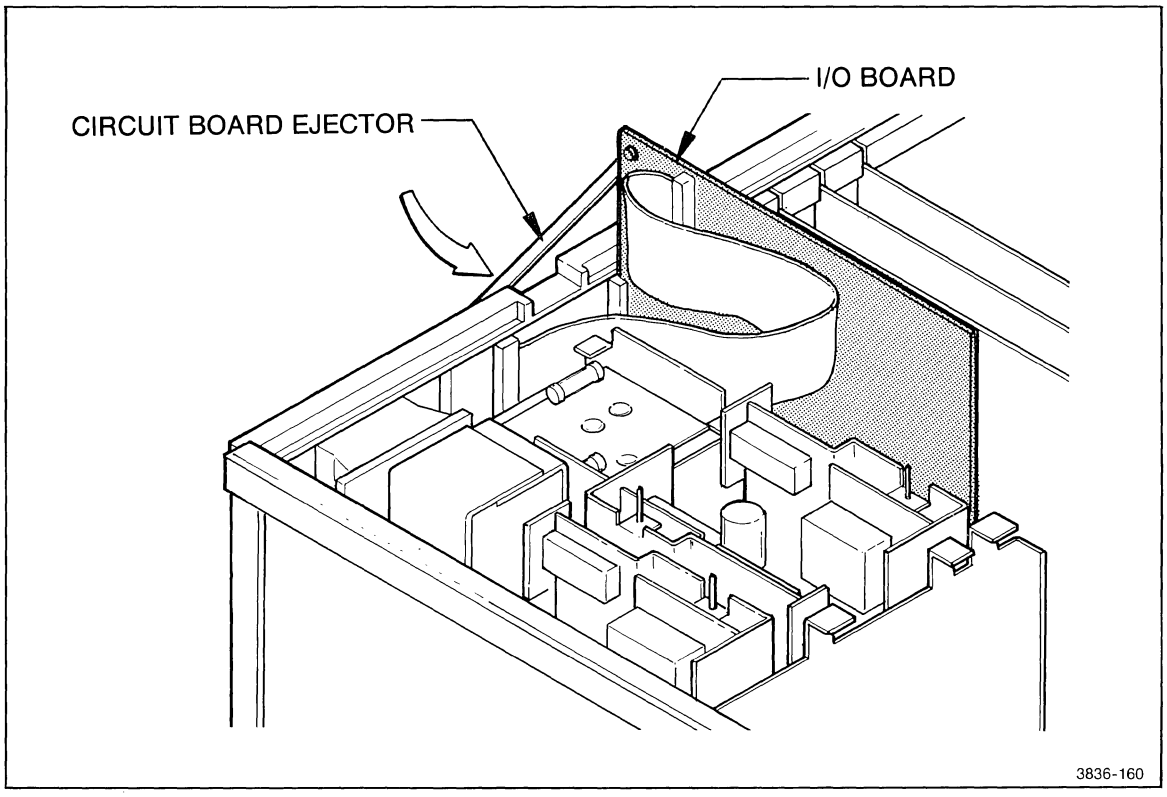


Figure 5-40. Disconnecting the I/O Interface.

7. Wait until 5 minutes have passed from the time the mainframe was turned off. This allows the main power capacitors to drain to safe levels.

WARNING

Not allowing the main power capacitors 5 minutes to drain will expose dangerous voltage and current levels during the following procedures.

8. Remove the Main Power Supply from the mainframe. To allow this, remove the side panel of the mainframe that is adjacent to the Main Power Supply.

9. Once this side panel is removed, remove the three screws shown in Figure 5-41.

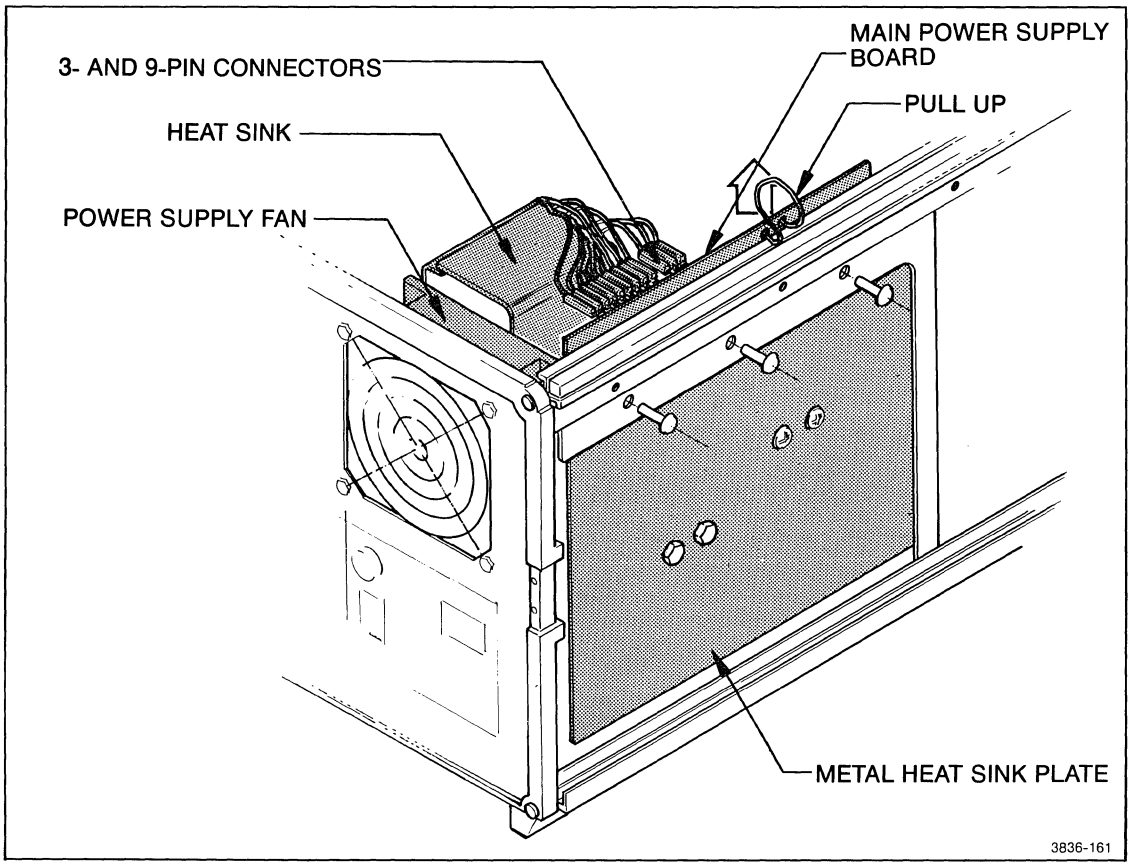


Figure 5-41. Main Power Supply removal.

10. After these screws are removed, the Main Power Supply can be lifted straight-up off of the connecting pins on the Interconnect.

11. Now that the Main Power Supply board has been pulled out of the mainframe, insert the Main Power Extender board into the Interconnect. Use the same connectors that were used by the Main Power Supply.

CAUTION

When inserting the Main Power Extender board, verify that the extender's connectors and the Interconnect connectors are accurately joined. If the extender is connected backwards or is shifted to the right or left of the appropriate position, the Main Power Supply may be severely damaged.

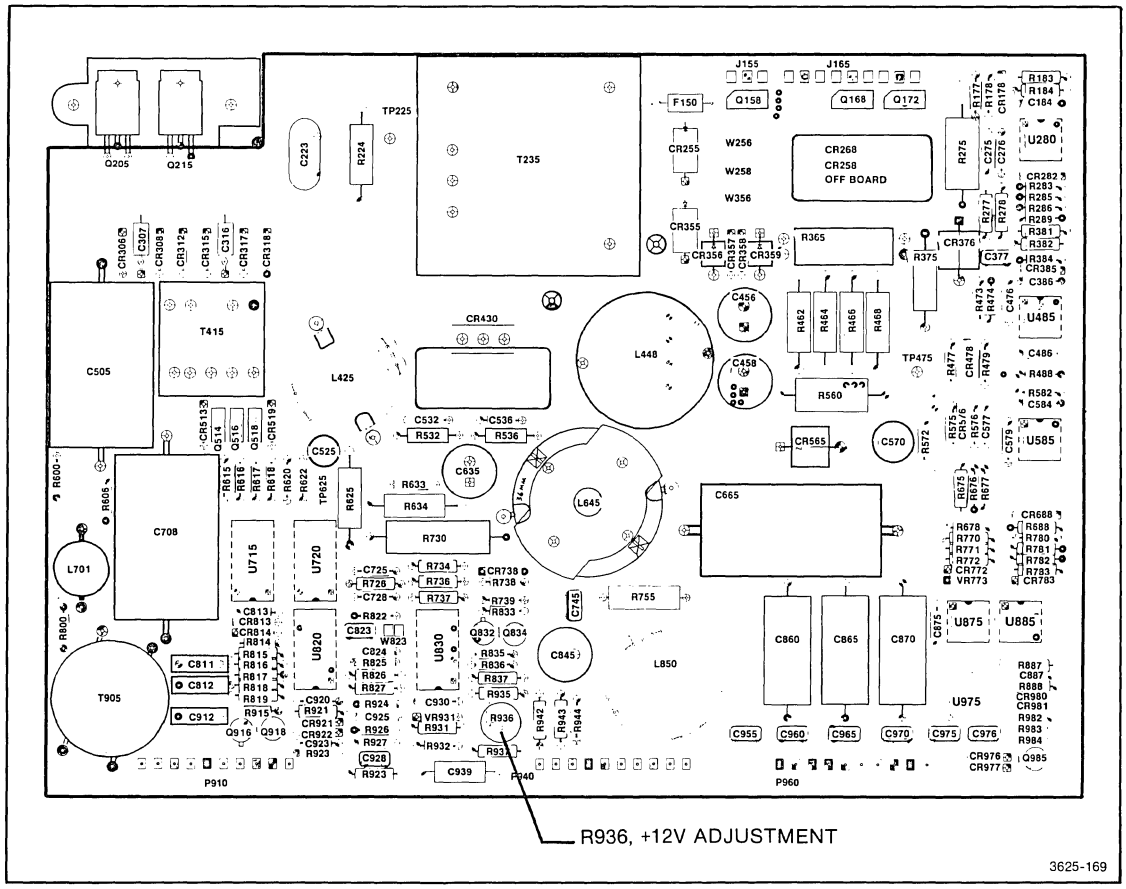


Figure 5-42. Main Power Supply adjustment locations.

12. Install the Main Power Supply on the Main Power Extender board according to the instructions found at the beginning of this Verification and Adjustment Procedures section.

13. Insert the Main Extender board (the module extender) into slot 3 of the DAS mainframe.

14. Connect one end of the 12 Ω, 12 W resistor to a GND test point on the Main Extender board. Connect the other end of the resistor to the +12 V test point on the Module Extender board. This resistor will draw 1 A, so these connections must be secure.

WARNING

The 12 Ω resistor may become quite hot during the following steps. Avoid touching the resistor while the DAS power is on.

15. Connect the DMM leads across the resistor, the ground lead to GND, and the positive lead to +12 V.

16. Set the DMM to a range that will comfortably read +12 V with at least ±0.1% accuracy.

17. Turn on the DMM and the DAS mainframe.

18. Adjust R936 on the Main Power Supply (see Figure 5-42) with the small slotted screwdriver until the DMM reads +12 V within a ±1% test boundary.

19. Turn off power to the DAS mainframe and allow it to sit for at least five minutes before reassembling the mainframe.

While reassembling the mainframe, do not forget to reconnect the tape drive and the I/O Interface if present. There are no further adjustments to be made in the power supplies section of the mainframe.

NOTE

All units in the DAS mainframe are affected by the accuracy of the +12 V supply from the Main Power Supply. If this adjustment has been made, all of the modules in the mainframe should have their adjustment procedures performed.

CONTROLLER ADJUSTMENT

Pre-adjustment Test

The Controller has two adjustments. Only one of the two needs to be performed, depending on whether the Controller is used with a monochrome or a color display monitor. Perform only those adjustments applicable to your situation. See Figure 5-43 for adjustment locations.

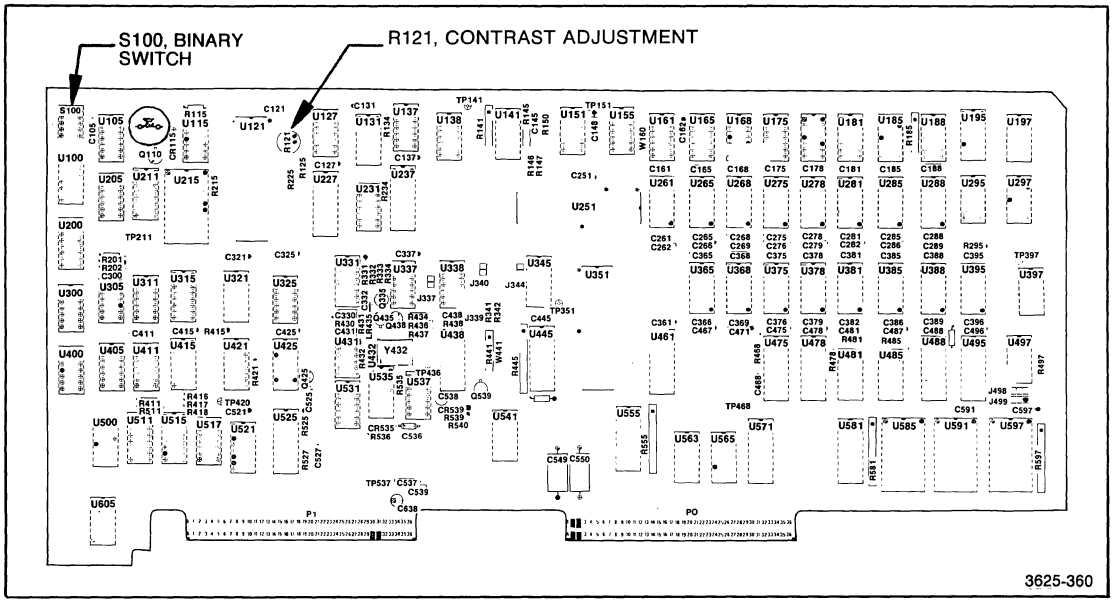


Figure 5-43. Controller adjustment locations.

Monochrome Contrast Adjustment

You will need the following equipment to perform the monochrome contrast adjustment for the Controller board:

- DAS Mainframe with a Monochrome Display Monitor
- Main Extender board
- Small plastic-bladed screwdriver

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the Controller Module.
3. Set the square pin jumpers on the Main Extender board so the extender will accept a Controller board. Install the Main Extender board in the mainframe slot 0.
4. Connect the Controller to be adjusted to the Main Extender board.
5. Turn on the mainframe.
6. Rotate the contrast control, R121 on the Controller, until a pleasing display is shown by the display monitor. When adjusting contrast, one good procedure is to watch a highlighted field for maximum readability combined with the brightest possible highlight field. See Figure 5-43 for the location of this control on the Controller board.

CAUTION

Unusually high luminesence levels from the screen of the display monitor may shorten the life of the phosphors in the CRT. Therefore, use discretion when setting the contrast control.

This completes the Controller adjustment for monochrome mainframes. Turn off the DAS mainframe before removing the Controller board or the Main Extender board.

Color Horizontal Position Adjustment

You will need the following equipment to perform the color horizontal position adjustment for the Controller board:

- DAS Mainframe with a Color Display Monitor
- Main Extender board
- Small plastic screwdriver

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the Controller module.
3. Set the square pin jumpers on the Main Extender board so the extender will accept a Controller board. Install the Main Extender board in the mainframe slot 0.
4. Connect the Controller to be adjusted to the Main Extender board.
5. Turn on the mainframe.
6. Set switches 1, 2, and 3 of S100 on the Controller board so the display is centered on the display area. The switches are organized in binary, where a closed switch represents a 1 and an open switch is a 0. As the binary number specified on S100 gets larger, the center of the display is shifted more to the right. As the binary number decreases, the display shifts to the left. The location of S100 on the Controller board is shown in Figure 5-43.

This completes the Controller adjustment for color mainframes. Turn off the DAS mainframe before removing the Controller board or the Main Extender board.

MOTOROLA DISPLAY MONITOR ADJUSTMENT

Pre-adjustment Test

The Motorola Display Monitor does not, under normal circumstances, require adjustment. Do not adjust this monitor unless the screen has become difficult to read and the contrast control on the Controller does not increase legibility to an acceptable level.

Adjustment Setup Procedure

You will need the following equipment to perform the next adjustment procedures:

- DAS mainframe

- Long shank (9 inch minimum) POZIDRIVE-type magnetic screwdriver
- Display Monitor Extender cable
- Small plastic-bladed, slotted screwdriver
- 60 MHz oscilloscope with 10X probe
- Digital multimeter (DMM)
- A plastic alignment tool for tuning inductors

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the DAS mainframe side panel that is adjacent to the Motorola Display Monitor.
3. Unplug the display monitor from the Interconnect board by removing the plug from socket J421 on the Interconnect.
4. Remove the monitor from the mainframe according to the Disassembly procedures given in the Maintenance: General Information section of this manual.
5. Remove the most exterior of the protective shields around the monitor. Remove the back panel of the display monitor. Instructions for these procedures are given in the disassembly procedures, in the Maintenance: General Information section of this manual.

WARNING

The display monitor contains very high voltages. Do not use metal bladed tools when making the following adjustments. Do not touch any circuitry other than adjustment points. In particular, be careful of the CRT; it may have over 21 kV on the anode.

6. Reconnect the Motorola Display Monitor to the DAS mainframe using the Display Monitor Extender cable.
7. Remove the Controller module from slot 0 of the mainframe.
8. Install the Main Extender board in slot 0 of the mainframe. Connect the Controller to the top of the extender board.

There are five separate adjustments to be made in the Motorola Display Monitor. The procedures to perform each of these adjustments are listed separately, below. The following procedures assume that the monitor has been removed from the mainframe and reconnected and that the protective covers have been removed as indicated previously. The locations of the monitor adjustments are shown in Figures 5-44 and 5-45.

NOTE

The following material regarding the Motorola Display Monitor was taken from the "M100 and M200 Series Service Manual" 1979 Motorola, Inc., by permission of Motorola, Inc.

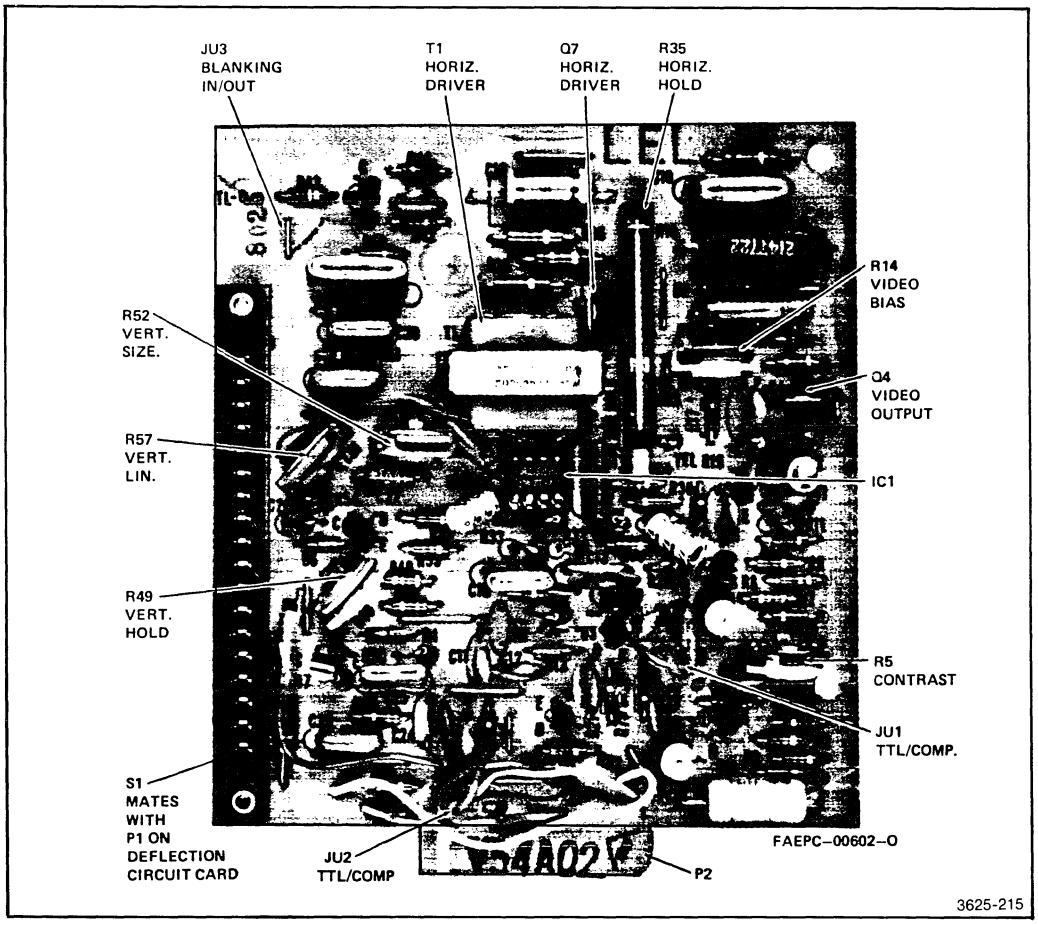


Figure 5-44. Motorola Display Monitor signal circuit board (A4A2) test point and adjustment locations.

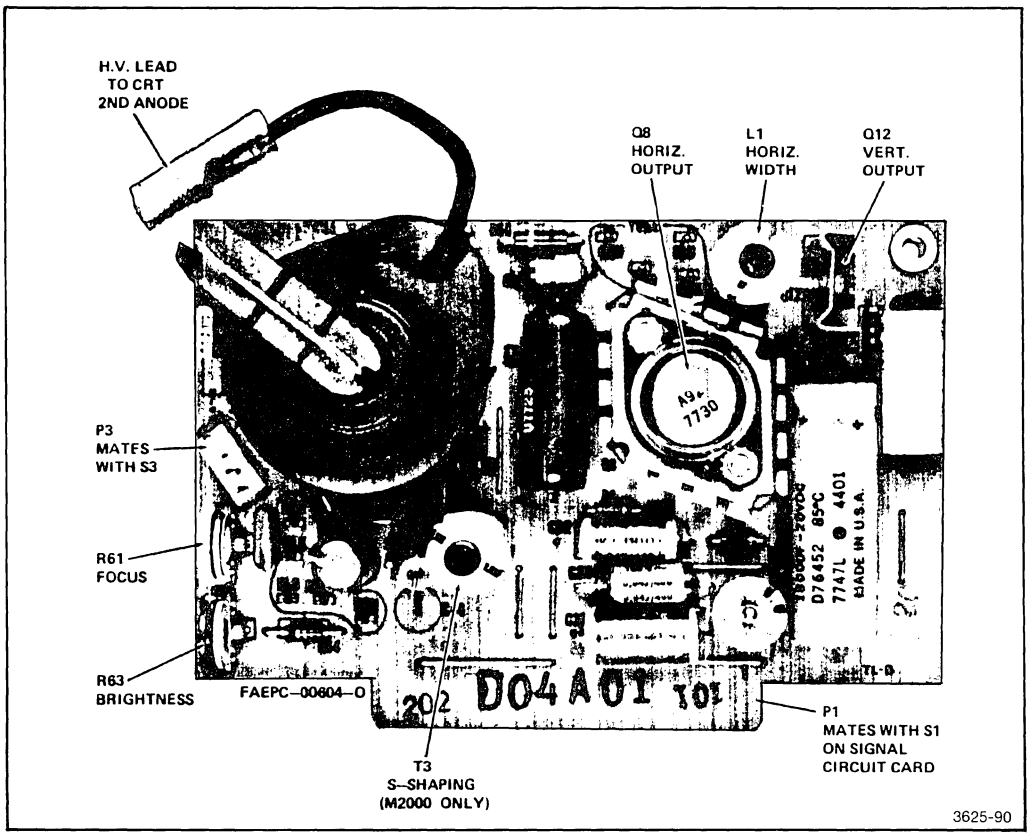


Figure 5-45. Motorola Display Monitor deflection circuit board. (A4A1) test point and adjustment locations.

9. After the monitor is fully adjusted (see following procedures), turn off the DAS mainframe.
10. Re-install the protective shields around the monitor.
11. Detach the extender cable from the monitor, and re-install the monitor in the DAS mainframe.
12. After the monitor is re-installed, reconnect the monitor to the Interconnect, J421.
13. Remove the Controller module from the Main Extender board.
14. Remove the Main Extender board from the mainframe and re-insert the Controller in slot 0 of the DAS mainframe.
15. Put the removed side panel back on the DAS mainframe.

WARNING

Use extreme care in handling the CRT during adjustment procedures. Rough handling may cause the tube to implode due to the high vacuum. Do not nick or scratch the glass or subject it to any undue pressure. Use goggles and heavy gloves for protection.

Focus Adjustment

To perform this adjustment you will need a

- Small plastic-bladed, slotted screwdriver

1. Turn on the DAS mainframe. The monitor screen should show the usual information.
2. Locate the Focus control, R61 (see Figures 5-44 and 5-45), in the display monitor. Adjust the Focus control for the most legible screen display.

Horizontal Adjustments

These steps set the horizontal size and position of the color display. To perform the horizontal adjustments you will need the following equipment:

- Small plastic-bladed screwdriver
- A plastic alignment tool for tuning inductors

1. Turn on the DAS Mainframe. The monitor screen should show the usual information.
2. Locate the Horiz Hold control, R35 (see Figures 5-44 and 5-45), in the display monitor.
3. Rotate R35 counterclockwise until the video display is out of horizontal sync. At this point, rotate R35 back clockwise until the video display just locks in horizontally; then stop. Using tape, mark the left-hand edge of the video display (not the raster edge) on the CRT face plate.
4. Continue rotating R35 clockwise until the video display is out of horizontal sync again (in the opposite direction). At this point, rotate R35 back counterclockwise until the video just locks in horizontally; then stop. With tape, mark the left hand edge of the video display on the CRT face plate again.
5. Observe the distance between the two marks on the CRT faceplate. Rotate R35 until the left-hand edge of the video display is centered between the two marks on the CRT faceplate.
6. Remove the marks from the CRT faceplate.

Video Bias Adjustment

You will need the following equipment to perform this procedure:

- Small plastic-bladed, slotted screwdriver
- Digital multimeter (DMM)

1. Turn on the DAS mainframe if it has been turned off, and warm up for five minutes. The monitor should display the usual informaion.
2. Locate R121 on the Controller module. Set this control to the center of its travel.
3. Locate the Contrast control, R6 (see Figures 5-44 and 5-45), in the display monitor. Rotate this control for minimum brightness.
4. Disconnect the input signals to the display monitor. Do this by removing jumpers on the Main Extender board. The jumpers to remove are listed below.

   From J1 on the Main Extender board

   Jumper B27 — Horizontal sync
   Jumper B28 — Vertical sync
   Jumper B29 — Video

   These jumpers can be removed using needle nose pliers or, working carefully, by hand.
5. Connect the digital multimeter across R18 in the display monitor. (The ground lead should connect near the collector of Q4.)
6. Adjust the Video Bias control, R14 (see Figures 5-44 and 5-45), so the voltage across R18 is $+2.0$ V, ± 0.05 V.
7. Disconnect the DMM.
8. Re-install the jumpers in the Main Extender board.
9. Adjust the Brightness control, R63 (see Figures 5-44 and 5-45), so the entire screen on the CRT is slightly illuminated. Then reduce the brightness just until the screen is black except where there are characters. Further adjustments in contrast should be made from the Controller module.

Horizontal Linearity Adjustment

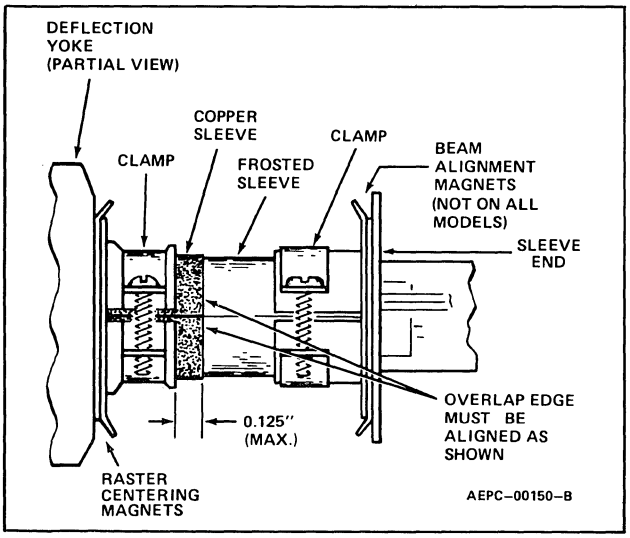
NOTE

This adjustment procedure is required only when a CRT and/or deflection yoke have been replaced.

You will need the following equipment to perform this procedure:

- Slotted screwdriver
- Ruler or tape measure
- Small plastic-bladed screwdriver
- A plastic alignment tool for tuning inductors

1. Turn off the DAS mainframe.
2. Locate the S-shaping transformer, T3 (see Figures 5-44 and 5-45), in the display monitor. Rotate the transformer's slug down to the bottom. (This temporarily minimizes the effect of T3 in the circuit.)
3. Loosen the deflection yoke clamp screw just enough to permit sliding the copper sleeve on the neck of the CRT back and forth. (Refer to Figure 5-46.)
4. Position the copper sleeve so that only 1/8 inch (3.2 mm) extends past the rear lip of the deflection yoke (refer to Figure 5-46). In addition, be sure that the overlap edge of the copper sleeve is aligned properly and is not twisted.
5. Tighten the clamp screw carefully so that the yoke position is not disturbed.



3625-171

Figure 5-46. Partial view of the CRT neck.

6. Turn on the DAS mainframe while holding down the STOP key. Enter the Diagnostics menu by pressing the START SYSTEM key. Select to run tests on single modules, then select slot 0 (the Controller module). Select to run tests in SINGLE mode and select FUNCTION 1, the DISPLAY function. Press START SYSTEM to start the test.

7. The DAS screen should now display a border and cross hairs made of the number 8.

8. (Refer to Figure 5-47.) Observe the extreme left-hand edge characters on the display screen (designated "A" in Figure 5-47). The width of these characters should be equal to the width of the right-hand edge characters (designated "B" in Figure 5-47). If character "A" is wider than character "B", the copper sleeve is extending out too far. If "A" is narrower than "B", the copper sleeve should be pulled out further. Either way, the copper sleeve may have to be repositioned by trial and error if exposing 1/8 inch (3.2 mm) of copper does not provide the desired linearity. Repeat steps 1 through 7, each time adjusting the amount of exposed copper, until the width of character "A" is equal to the width of character "B".

9. With the DAS mainframe turned on, observe the width of a character in the center of the CRT screen (designated "C" in Figure 5-47). It should be narrower than characters "A" and "B".

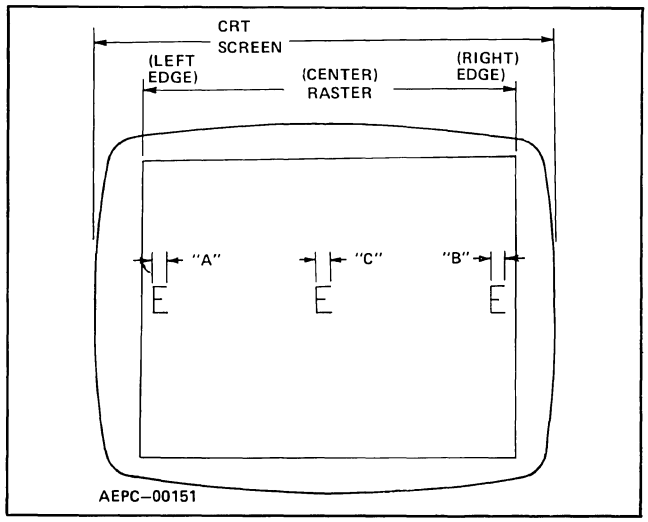


Figure 5-47. Linearity adjustment raster display.

10. Connect the oscilloscope (ac coupled) between the the blue wire pin on the deflection card and chassis ground. A parabolic waveform should appear.

11. Using the small plastic-bladed screwdriver, rotate the slug of T3 upward (away from the circuit board) until the amplitude of the waveform is 125 V peak to peak. This setting makes character "C" the same width as characters "A" and "B".

12. Disconnect the oscilloscope.

Raster Centering Adjustment

NOTE

Raster centering is set at the factory and should not normally require further adjustment.

To perform this procedure you will need a

- Small plastic-bladed screwdriver

1. Turn on the DAS mainframe if it is not on.
2. Position the tabs of the beam alignment magnets so they are horizontally opposing. (Refer to Figure 5-46.)
3. Adjust R52 (vertical size) and L1 (horizontal width) so all edges of the raster are visible. (Refer to Figures 5-44 and 5-45 for the location of these adjustments.)
4. Position the raster centering magnets for the best centering of the raster. (Refer to Figure 5-46.)
5. Readjust size and width (using R52 and L1) of the raster to approximately 6.5 inches (16.5 cm) wide by 4 inches (10.2 cm) high.

CRT Beam Alignment

For optimum character quality in the corners of the video display, a beam alignment magnet may be used on the monitor CRT. If this magnet is not used, disregard this procedure.

NOTE

Adjustment of the raster centering rings must precede the adjustment of the beam alignment magnet.

To perform this procedure you will need a

- Slotted screwdriver

The beam alignment magnet should be positioned on the neck of the CRT between the deflection yoke and the tube base. The correct location of the magnet rings is approximately over the second grid of the electron gun (see Figure 5-46).

1. Turn on the DAS mainframe.
2. Make sure the display monitor is set for optimum contrast (using control R121 on the Controller module) and for optimum focus (see above procedures).

3. Loosen the beam alignment magnet clamping screw just enough to allow the assembly free movement on the CRT neck.

4. While observing the tails on the dots in the corners of the display, rotate the focus rings to minimize the tails.

5. Tighten the clamping screw.

COLOR DISPLAY MONITOR ADJUSTMENT

Pre-adjustment Test

The color display monitor found in DAS9129 mainframes does not, under normal conditions, require adjustment. Do not adjust this monitor unless the screen has become difficult to read and the intensity control on the back of the mainframe does not increase legibility to an acceptable level.

Adjustment Setup Procedure

You will need the following equipment to perform the next adjustment procedures:

- DAS9129 mainframe with the monitor to be adjusted installed
- Slotted screwdriver
- POZIDRIV-type screwdriver
- Main extender board (from the DAS 9100 Service Maintenance Kit).

WARNING

Do not remove or install any panels on a DAS mainframe while the power is on. Doing so could cause a temporary high voltage short to the panel that would be dangerous for the technician.

1. Turn off the DAS mainframe.

2. Remove the top outside panel of the DAS mainframe. Also remove the mainframe side panel that is adjacent to the color display monitor.

3. Remove the eight screws (6-32 x 0.250) securing the side of the black monitor cover to the monitor itself. Do not try to lift the cover off yet.

4. Remove the three screws (6-32 x 0.250) securing the side of the monitor cover to the bottom rail of the mainframe.

CAUTION

Do not bend or dent the soft mu-metal shield. If it is bent or dented, it may retain strong magnetic fields that will distort the color purity. Distortion caused by dents in the mu-metal shield cannot be removed by the degaussing coil.

5. Lift the black enamelled cover and the mu-metal shield out of the mainframe. Observe that the tapered end of the mu-metal shield is toward the rear of the mainframe.

The adjustments on the display monitor are now exposed. There is one display monitor related adjustment located on the Controller board. To reach this adjustment the Controller must be placed on an extender board.

7. Remove the Controller board from slot 0 of the mainframe.

8. Set the square-pin jumpers on the extender board to accept a Controller board. Install the extender board in slot 0 of the mainframe. Install the Controller board on top of the extender board.

There are eight individual adjustments to be made in the color display monitor along with one adjustment on the Controller board. The locations of the monitor adjustments are shown in Figures 5-48 and 5-49.

Focus and Vertical Size Adjustment

These steps set the focus and vertical size of the color monitor display. To perform the focus and vertical adjustments you will need a

- Small plastic-bladed screwdriver

WARNING

The display monitor contains very high voltages. Do not use metal bladed tools when making the following adjustments. Do not touch any circuitry other than the adjustment points. In particular, be careful of the CRT, which may have over 21 kV on the anode.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 0, the Controller.

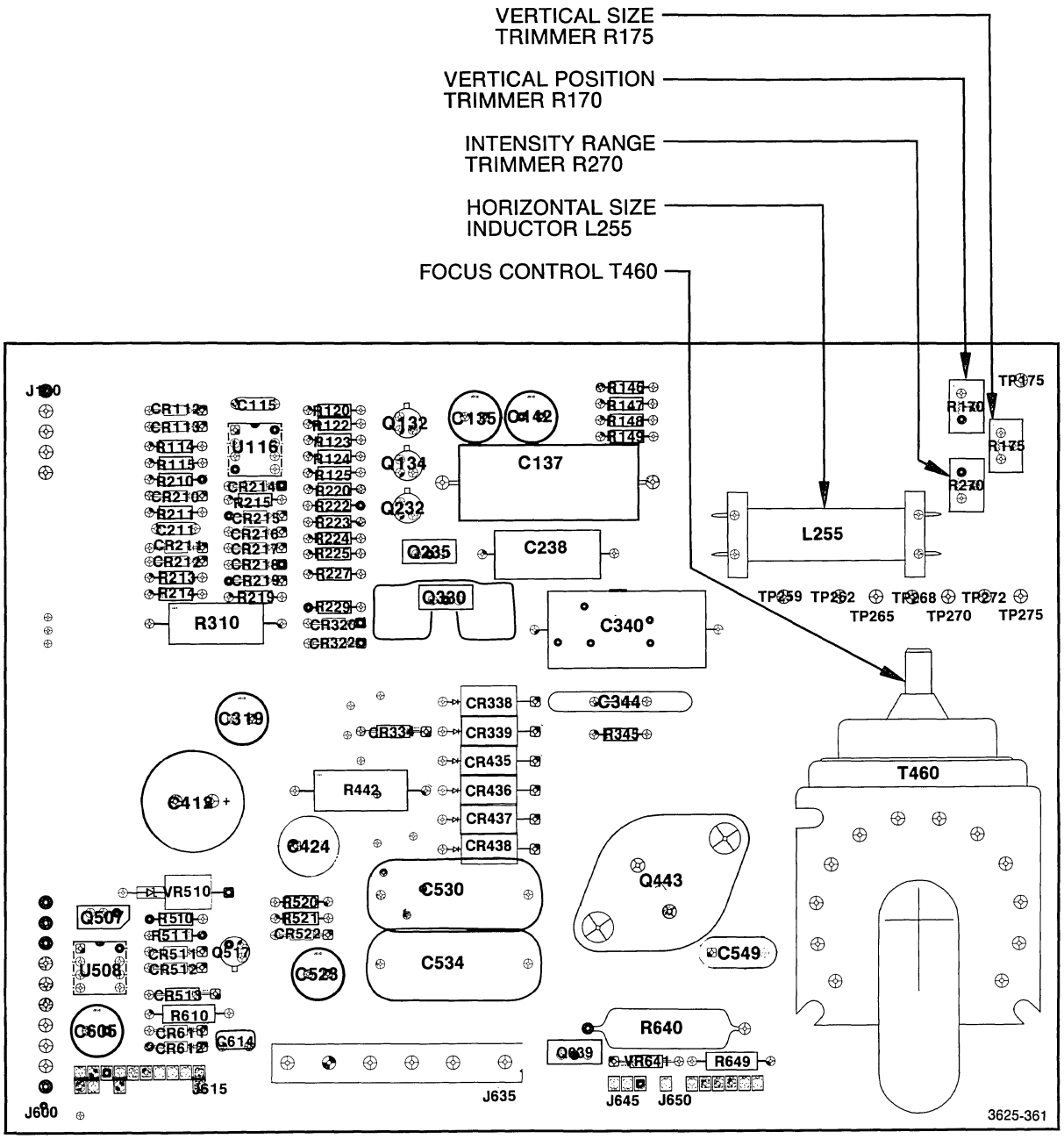


Figure 5-48. Color Display Monitor adjustment locations, deflection circuit board (A30A1).

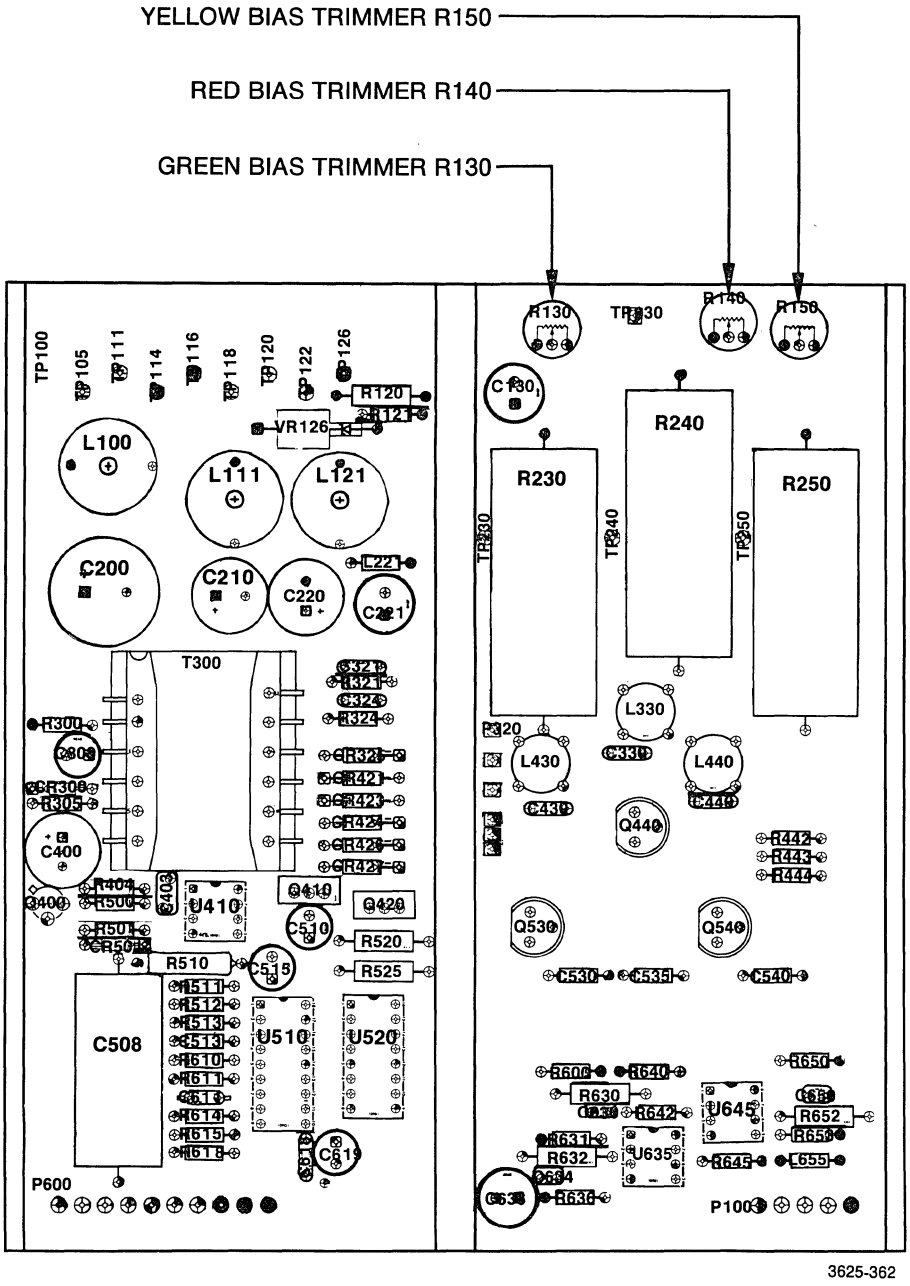


Figure 5-49. Color Display Monitor adjustment locations, Z-axis circuit board (A30A2).

3. Select SINGLE mode, then select to run function 1; the DISPLAYS function. Start this test by pressing START SYSTEM and then pressing SELECT twice. The display monitor should show an all character display.

4. Set the intensity control on the back of the mainframe for a bright display.

5. Adjust the focus control, T460 on the deflection board, for the best focus near the upper left-hand corner of the screen (see Figure 5-48).

6. Adjust the vertical position trimmer potentiometer, R170 on the deflection board, so the top of the display area is approximately 1 cm (3/8 in.) below the top of the display area.

7. Adjust the vertical size trimmer potentiometer, R175 on the deflection board, so the bottom of the display area is approximately 1 cm (3/8 in.) above the bottom of the display area.

8. Verify that the adjustment of the lower edge of the raster did not disturb the location of the upper edge.

Horizontal Adjustment

These steps set the horizontal size and position of the color display. To perform the horizontal adjustments you will need the following equipment:

- Small plastic-bladed screwdriver
- A plastic alignment tool for tuning inductors

The display monitor contains very high voltages. Do not use metal bladed tools when making the following adjustments. Do not touch any circuitry other than the adjustment points. In particular, be careful of the CRT, which may have over 21 kV on the anode.

1. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select to run tests on slot 0, the Controller.

3. Select SINGLE mode, then select to run function 1; the DISPLAYS function. Start this test by pressing START SYSTEM. The display monitor should show a green border and cross hairs made of the number 8.

4. Adjust the intensity range trimmer potentiomenter, R270 on the deflection board, so a slight amount of the raster shows on the screen.

5. Adjust the horizontal size inductor, L255 on the deflection board, so the entire raster shows on the display area of the mainframe (see Figure 5-48).

6. Set switches 1, 2, and 3 of S100 on the Controller board so the raster is centered on the display area. The switches are organized in binary, where a closed switch represents a 1 and an open switch is a 0. As the binary number specified on S100 gets larger the center of the display is shifted more to the right. As the binary number decreases the display shifts to the left.

7. Adjust the horizontal size inductor, L255 on the deflection board, so the raster is approximately 6 mm (1/4 in.) in from both sides of the screen. If necessary, re-adjust S100 to center the display again.

Intensity Adjustments

These steps set the intensity range of the color display. To perform the intensity adjustments you will need a

- Small plastic-bladed screwdriver

WARNING

The display monitor contains very high voltages. Do not use metal bladed tools when making the following adjustments. Do not touch any circuitry other than the adjustment points. In particular, be careful of the CRT, which may have over 21 kV on the anode.

1. Turn off the mainframe. Turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self-test to fail.

2. Press START SYSTEM to enter the Diagnostics menu. Select tests on slot 0, the Controller.

3. Select SINGLE mode, then select to run function 1; the DISPLAYS function. Start this test by pressing START SYSTEM.

4. Press the SELECT key twice. The screen should show a display of all possible characters and colors.

5. Adjust the intensity control on the rear panel of the DAS to minimum.

6. Adjust the red, green, and yellow bias trimmer potentiometers, R130, R140, and R150 on the Z-axis board, to minimum (see Figure 5-49).

7. Adjust the intensity range trimmer potentiometer, R270 on the deflection board, for a dim display (see Figure 5-48).

8. Observe the screen and decide whether the green or the yellow characters are dimmer. Whichever color is dimmer, increase that color's intensity with either trimmer potentiometer R130 (green) or trimmer R150 (yellow) on the Z-axis board. Continue adjusting the potentiometer for the dimmer color until both colors have the same intensity.

9. Compare the yellow-on-black characters to the yellow-on-red characters. Adjust the red intensity trimmer, R140 on the Z-axis board, so the color of the yellow characters is the same. (The yellow-on-red characters will be relatively brighter, and the red background relatively dimmer, but the color will be the same.)

   If the red trimmer, R140, cannot get the yellow colors to match, return the red trimmer to minimum. Adjust the green trimmer, R130 on the Z-axis board, so the yellow characters match in color. After adjusting the green intensity, the yellow intensity will probably need adjusting. Return to step 8 of these procedures to adjust the yellow intensity.

10. Check that at least one of the three intensity trimmer potentiometers, R130, R140, and R150 on the Z-axis board, is set to minimum. If none of these trimmers is set to minimum, then return to step 6 of these procedures and re-adjust the display while making sure that one of the trimmers remains at the minimum setting.

    By leaving one of the trimmers at minimum, power dissipation is minimized so reliability is increased.

11. Continue to observe the diagnostic "screenfull of characters" display. While rotating the rear panel intensity control through its entire range, observe that:

- The screen does not become dim and flickering when the intensity is set to maximum. This means that the writing beam of the CRT has current limited, so the intensity needs to be reduced.

- The raster background does not show when the rear panel intensity control is set to maximum.

- The display remains visible at the minimum rear panel intensity setting.

If the display does not meet all the above criteria, adjust the intensity trimmer, R270 on the deflection board, for the best compromise.

This completes the adjustment of the color display monitor. Turn off the power to the DAS mainframe before re-installing the Controller board and the panels around the display monitor.

TRIGGER/TIME BASE MODULE ADJUSTMENT

Pre-adjustment Test

The Trigger/Time Base board has two related adjustments that control the digital-to-analog converter (DAC). You will need the following equipment to test the accuracy of the DAC.

- DAS mainframe
- Digital multimeter (DMM) with leads
- Main Extender board

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the Trigger/Time Base board from the mainframe.
3. Set the square pin jumpers on the Main Extender board to accept a Trigger/Time Base board.
4. Insert the Main Extender board in the mainframe slot 7. Install the Trigger/Time Base board on the top of the extender.
5. Connect the positive lead of the DMM to test point TP208 on the Trigger/Time Base board (see Figure 5-50). Connect the DMM ground lead to TP105 on the Trigger/Time Base board.
6. Turn on the DMM.
7. Turn on the DAS mainframe while holding down the STOP key. This will cause a self-test diagnostic failure.
8. When the power-up tests are finished, press the START SYSTEM key to enter the Diagnostics menu.
9. Adjust fields in the Diagnostics menu to run SINGLE tests on SLOT 7 (the Trigger/Time Base). Select TEST 6, the DAC THRSH test, to be run and press the START SYSTEM button.
10. The voltage between these test points should equal the voltage shown on the screen ±1%, ±5 mV.

11. Press the SELECT button. Each time this key is pressed, a new voltage should appear on the screen. The voltage at TP208 should equal that voltage ±1%, ±5 mV. If the voltages at the test point fall within this boundary, the Trigger/Time Base does not need adjustment. If this test is not passed, then the Trigger/Time Base DAC needs adjusting. To adjust the DAC, use the following procedure.

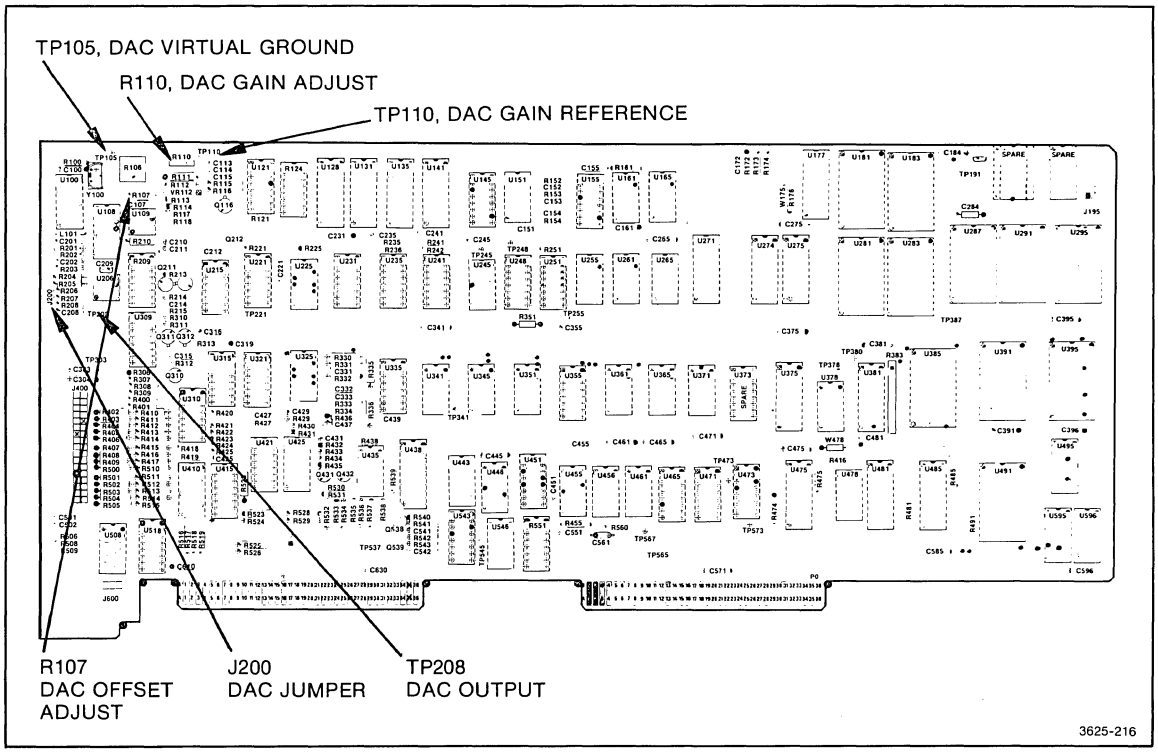


Figure 5-50. Trigger/Time Base board test point and adjustment locations.

DAC Adjustment

This adjustment procedure assumes the pre-adjustment test has just been performed, so the Trigger/Time Base boaard is on an extender and the DAS is in the Diagnostics menu with the DAC THRSH test selected. In addition to the equipment needed for the pre-adjustment test, you will need the following equipment to perform this procedure:

- Small slotted screwdriver
- Square pin shorting jumper

1. The Trigger/Time Base is on an Extender and the DMM is hooked up as described in the pre-adjustment test. The Trigger/Time Base DAC THRSH test is selected in the Diagnostics menu.

2. In the DAS THRSH test, select a 0.00 V output.

3. Move the shorting jumper at J200 on the Trigger/Time Base board from pins 2 and 3 to pins 1 and 2 (see Figure 5-50).

4. Move the positive lead of the DMM to TP110 (see Figure 5-50). Leave the ground lead of the DMM at TP105.

5. Adjust trimmer potentiometer R110 for 1.60 V, ±0.05% across the two test points.

6. Move the positive lead of the DMM to TP208 on the Trigger/Time Base board (see Figure 5-50).

7. Adjust potentiometer R106 (see Figure 5-50) for 0.00 V, ±1 mV across these two points.

8. Move the jumper at J200 from pins 1 and 2 back to pins 2 and 3.

9. Turn off the DAS, disconnect the DMM, and re-install the Trigger/Time Base in the DAS mainframe.

91A32 ACQUISITION MODULE ADJUSTMENTS

Pre-adjustment Test

The 91A32 module has a total of nine adjustments in two different circuitry areas. There are four adjustments to the write-enable circuitry; any test of this area would require as much effort to perform as the actual adjustment, so no pre-adjustment test is given.

There are also five adjustments in the digital-to-analog converter (DAC) circuitry. There is a pre-adjustment test for the DAC, which is given below. You will need the following equipment to perform the DAC pre-adjustment test:

- DAS mainframe
- Digital multimeter (DMM) with leads
- Main Extender board

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.

2. Remove the 91A32 module from the mainframe.

3. Set the square pin jumpers on the Main Extender board to accept a 91A32 module.

4. Insert the Main Extender board in the slot that the 91A32 occupied in the mainframe. Install the 91A32 on top of the extender.

5. Connect the positive lead of the DMM to pin 6 of U122 on the 91A32 (see Figure 5-51). Connect the DMM ground lead to TP147 on the 91A32.

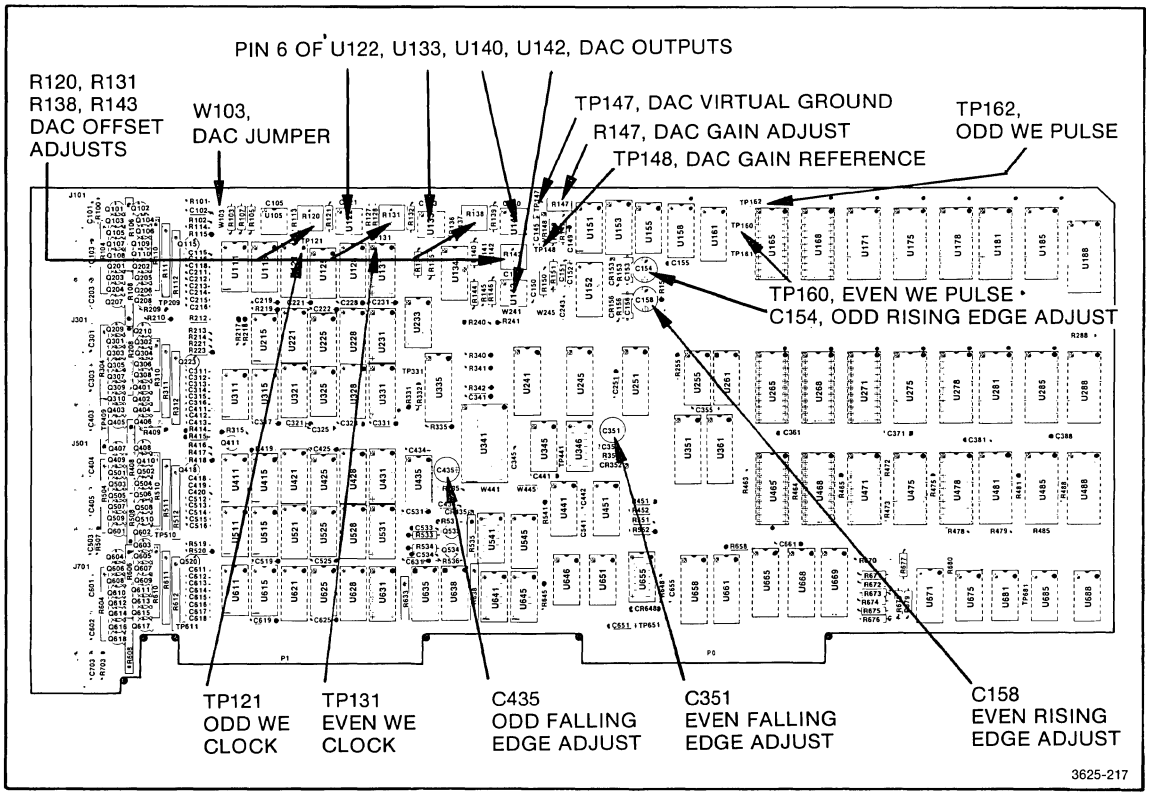


Figure 5-51. 91A32 test point and adjustment locations.

6. Turn on the DMM.

7. Turn on the DAS mainframe while holding down the STOP key to cause a self-test diagnostic failure.

8. When the power-up tests are finished, press the START SYSTEM key to enter the Diagnostics menu.

9. Adjust fields in the Diagnostic menu to run SINGLE tests on the slot with the 91A32 under test in it. Select to run function 3, DAC THRSH. Press START SYSTEM to initiate the test.

10. The voltage read by the DMM should equal the voltage shown on the screen, within ±1%, ±5 mV.

11. Press the SELECT button. Each time this button is pressed a new voltage should appear on the screen. The voltage measured by the DMM should equal the one shown on the screen within ±1%, ±5 mV.

12. Move the positive lead of the DMM to pin 6 of U133. Verify the accuracy of all selectable voltages at this test point (within ±1%, ±5 mV). Repeat the verification at pin 6 of U140 and at pin 6 of U142 (see Figure 5-51). If all the selected voltages are accurate, perform only the 91A32 write-enable adjustment procedure below. If the voltages read are not accurate, perform both the DAC and the write-enable adjustment procedures for the 91A32.

DAC Adjustment

This adjustment procedure assumes the pre-adjustment test has just been performed for this module. Therefore, the 91A32 is on an extender and the DAS is in the Diagnostics menu with the DAC THRSH test selected for the module being adjusted. In addition to the equipment needed for the pre-adjustment test, you will need the following equipment to perform this procedure:

- Small slotted screwdriver
- Square pin shorting jumper

1. The 91A32 is on its extender and the digital multimeter is hooked up as described in the pre-adjustment test. The Diagnostics menu is called up and the 91A32 DAC THRSH test is selected.
2. In the DAC THRSH test, press the SELECT button on the keyboard until 0.00 V is displayed.
3. On W103 of the 91A32, move the shorting jumper at pins 2 and 3 to pins 1 and 2 (see Figure 5-51).
4. Move the positive lead of the DMM to TP148. Leave the ground lead at TP147 (see Figure 5-51).
5. Adjust trimmer potentiometer R147 for 1.60 V, ±0.5% across the two test points.
6. Move the positive lead of the DMM to pin 6 of U122 on the 91A32. Adjust potentiometer R120 for 0.00 V, ±1 mV across the two test points.
7. Move the positive lead of the DMM to pin 6 of U133 and adjust for 0.00 V, ±1 mV using potentiometer R131.
8. Move the positive lead of the DMM to pin 6 of U140 and adjust for 0.00 V, ±1 mV using potentiometer R138.
9. Move the positive lead of the DMM to pin 6 of U142 and adjust for 0.00 V, ±1 mV using potentiometer R143.
10. Remove the jumper from pins 1 and 2 at J103 and replace it on pins 2 and 3.
11. Perform the write-enable adjustments as indicated in the next adjustment procedure.

Write-Enable Adjustment SN B014475 & UP (91A32 only)

This adjustment procedure assumes either the 91A32 DAC adjustment procedure or the pre-adjustment test has just been performed. Therefore, the 91A32 to be adjusted is on an Extender and the DAS is turned on. You will need the following additional equipment for this part of the adjustment:

- Small slotted screwdriver
- 100 MHz oscilloscope with two channels
- Two probes for the above oscilloscope

1. Remove the digital multimeter (DMM) from the 91A32. The DMM will not be needed to make this adjustment.
2. Press the TRIGGER SPEC button on the DAS keyboard.
3. In the Trigger Specification menu, specify all "B" hexadecimal values in the TRIGGER ON field. This will prevent the 91A32 from triggering. No other trigger fields should be set. The screen of the DAS should look like Figure 5-52.

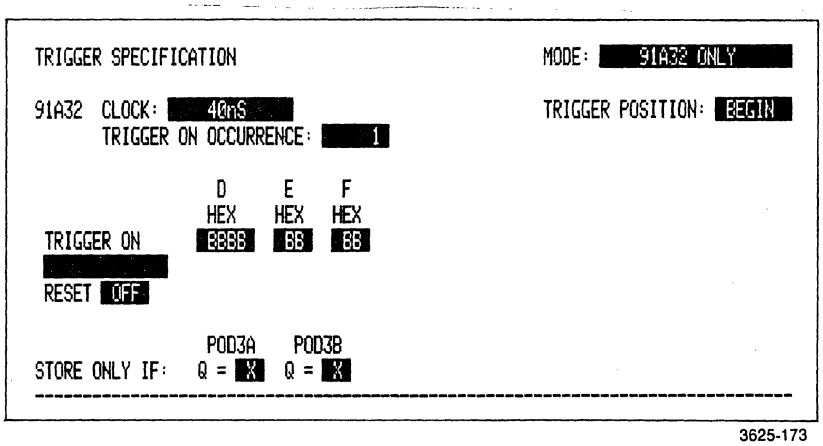


Figure 5-52. 91A32 write-enable adjustment menu.

4. Attach the probe for channel 1 of the oscilloscope to TP131 on the 91A32. Attach the probe for channel 2 of the oscilloscope to TP160 (see Figure 5-51). The ground leads of the probes can be attached at any ground test point on the 91A32.
5. Set the oscilloscope to trigger off a rising edge on channel one.
6. Set the jumpers at each of W241, W245, W441, and W445 to short pins 2 and 3 together.

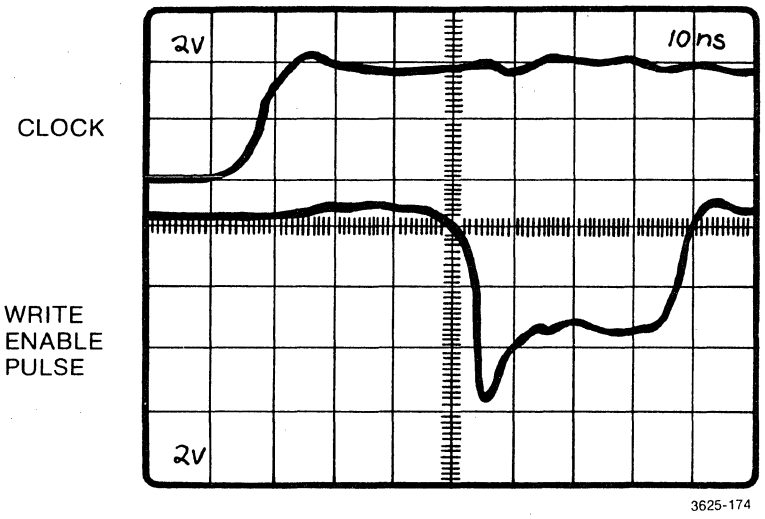


Figure 5-53. 91A32 write-enable timing.

7. Turn on the oscilloscope and press the START ACQUISITION button. Adjust the oscilloscope for a display like the one shown in Figure 5-53 (2 V/div for both channels, time base set to 10 ns/div).

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

8. Adjust variable capacitor C351 so the falling edge on channel 2 of the oscilloscope is 29 ns, ±1 ns after the rising edge in channel 1. If the capacitor cannot be set to this great a delay, change the jumper at W445 to connect pins 1 and 2 (not 2 and 3) and again adjust C351 to 29 ns, ±1 ns.

9. Adjust capacitor C158 so the rising edge on channel 2 is 64 ns, ±1 ns after the rising edge in channel 1. If the capacitor cannot be set to this great a delay, change the jumper at W245 to connect pins 1 and 2 (not 2 and 3) and again adjusting C158 to 64 ns, ±1 ns.

10. Verify that the falling edge on channel 2 was not disturbed by the rising edge adjustment. The oscilloscope display should now look like Figure 5-53. If the time values shown on channel 2 of the oscilloscope are not accurate, perform steps 8 and 9 again until they are correct.

11. Move the probe for channel 1 to TP121. Move the probe for channel 2 to TP162. The ground leads may be left where they were. Again, the oscilloscope display should look like the one shown in Figure 5-53.

12. Adjust variable capacitor C435 so the falling edge on channel 2 of the oscilloscope is 29 ns, ±1 ns after the rising edge in channel 1. If the capacitor cannot be set to this great a delay, change the jumper at W441 to connect pins 1 and 2 (not 2 and 3) and again adjusting C435 to 29 ns, ±1 ns.

13. Adjust capacitor C154 so the rising edge on channel 2 is 64 ns, ±1 ns after the rising edge in channel 1. If the capacitor cannot be set to this great a delay, change the jumper W241 to connect pins 1 and 2 (not 2 and 3) and again adjust C154 to 64 ns, ±1 ns.

14. Verify that the falling edge in channel 2 was not disturbed by the rising edge adjustment. The oscilloscope display should look exactly like Figure 5-53. If the time values shown in channel 2 are not accurate, perform steps 12 and 13 again until they are correct.

15. Disconnect the oscilloscope from the 91A32. Turn off the DAS mainframe and re-install the 91A32 module.

91A08 ACQUISITION MODULE ADJUSTMENTS

Pre-adjustment Test

The 91A08 module has a total of eight adjustments in three different circuitry areas. There are four adjustments to the write-enable circuitry; any test of this area would require as much effort to perform as the actual adjustment, so no pre-adjustment test is given.

There are also three adjustments in the digital to analog converter (DAC) circuitry. There is a pre-adjustment test for the DAC, which is given below.

There is an adjustable delay line that under certain circumstances must be adjusted. The delay line should only be adjusted if one of the following parts of the 91A08 module has been replaced since the last adjustment.

Component Number	Component Type
A13Q601	Transistor
A13Q602	Transistor
A13U701	9685
A31U605	100163
A13U615	100102
A13U511	100102

You will need the the following equipment to perform the pre-adjustment test for the DAC:

- Digital multimeter (DMM) with leads
- Main Extender board

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.

2. Remove the 91A08 module to be tested from the mainframe and disconnect any probes.

3. Set the square pin jumpers on the Main Extender board to accept a 91A08 module.

4. Insert the Main Extender board in slot 6 of the mainframe. This may involve removing a previously installed module from the mainframe. Install the 91A08 on top of the extender. Install a shorting jumper on pins 1 and 2 of J208.

5. Connect the positive lead of the DMM to TP201 on the 91A08 (see Figure 5-54). Connect the DMM ground lead to TP106 on the 91A08.

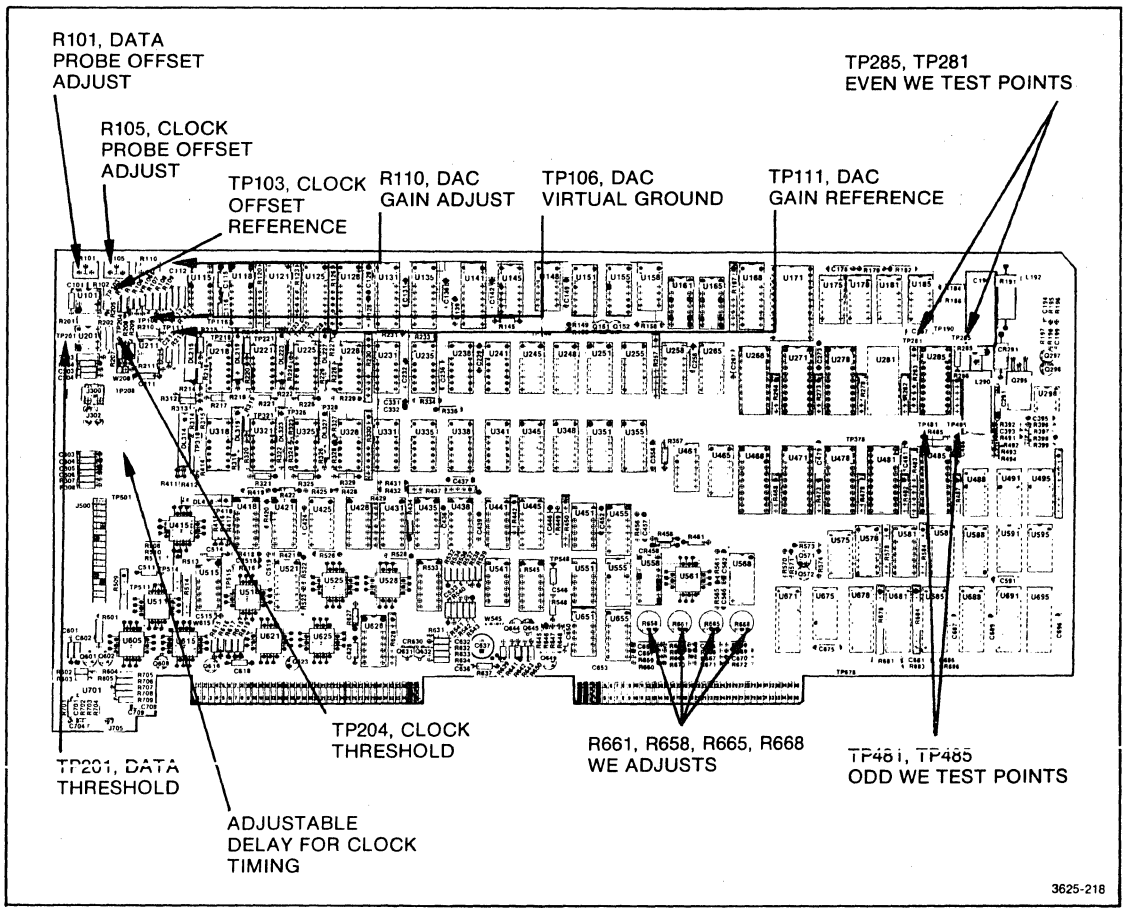


Figure 5-54. 91A08 test point and adjustment locations.

6. Turn on the DMM.

7. Turn on the DAS mainframe while holding down the STOP key to cause a self-test diagnostic failure.

8. When the power-up tests are finished, press the START SYSTEM key to enter the Diagnostics menu.

9. Adjust fields in the Diagnostic menu to run SINGLE tests on the slot with the 91A08 under test in it. Select to run function 5, DAC THRSH. Press START SYSTEM to initiate the test.

10. The voltage between test points TP201 and TP106 should equal the voltage shown on the screen within ±1%, ±5 mV. Measure this voltage with the digital multimeter.

11. Press the SELECT button. Each time this button is pressed, a new voltage should appear on the screen. The voltage shown on the DMM should equal the one shown on the screen within ±1%, ±5 mV.

12. Remove the positive lead of the DMM from TP201 and connect it to TP204. Move the negative lead of the DMM to a GND TP. Press the SELECT button. Each time this button is pressed, a new voltage should appear on the screen. The voltage shown on the DMM should be within the high and low levels shown below. If all the selected voltages are accurate, perform only the 91A08 write-enable adjustment procedure. If the voltages measured are not accurate, perform both the 91A08 DAC and write-enable adjustments.

Menu	Low	Nominal	High
0.00	.749 V	.750 V	.751 V
+1.6000	.101 V	.110 V	.119 V
−1.5875	1.376 V	1.385 V	1.394 V

DAC Adjustment

This adjustment procedure assumes the pre-adjustment test has just been performed for this module. Therefore, the 91A08 is on an extender in slot 6 and the DAS is in the Diagnostics menu with the DAC THRSH test selected for the module being adjusted. In addition to the equipment needed for the pre-adjustment test, you will need the following tools for this procedure:

- Small slotted screwdriver
- Square pin shorting jumper

1. The 91A08 is on its extender and the DMM is hooked up as described in the pre-adjustment test. The Diagnostics menu is called up and the 91A08 DAC THRSH test is selected.

2. In the DAC THRSH test, press the SELECT button on the keyboard until 0.00 V is displayed.

3. Insert the jumper at J208 pins 1 and 2 on the 91A08 (see Figure 5-54).

4. Move the positive lead of the DMM to TP111. Leave the ground lead at TP106 (see Figure 5-54).

5. Adjust trimmer potentiometer R110 for 1.60 V, ±0.5% across the two test points.

6. Move the positive lead of the DMM to TP201 on the 91A08. Adjust potentiometer R101 for 0.00 V, ±1 mV across the two test points.

7. Move the ground or negative lead of the DMM to any convienient ground test point on the 91A08 circuit board.

8. Move the positive lead of the DMM to TP204 and adjust potentiometer R105 for 0.750 V, ±0.5 mV between the two test points.

9. Remove the jumper at J208. (If J208 has three square pins place the jumper on pins 2 and 3.

10. Perform the 91A08 write-enable adjustment procedure.

Write-Enable Adjustment

This procedure assumes either the 91A08 DAC adjustment procedure or the 91A08 pre-adjustment test has just been performed. Therefore, the 91A08 to be adjusted is on an extender and the DAS is turned on. You will need the following additional equipment for this part of the adjustment:

- Small slotted screwdriver
- 350 MHz oscilloscope with two channels
- Two probes for the above oscilloscope

1. Remove the digital multimeter from the 91A08. The DMM will not be needed for this adjustment.

2. Press the TRIGGER SPEC button the DAS keyboard.

3. In the Trigger Specification menu, set the MODE field to 91A08 ONLY and specify all "B" hexadecimal values in the TRIGGER ON field. This will prevent the 91A08 from triggering. Do not change any other fields in the menu. The display of the DAS should now look like Figure 5-55.

4. Attach the probe for channel 1 of the oscilloscope to test point EA0 (TP281) on the 91A08. Attach the probe for channel 2 of the scope to EWE (TP285) (see Figure 5-54). The ground leads of the probes can be attached at any ground test point on the 91A08.

5. Set the oscilloscope to trigger off a rising edge on channel one.

6. Turn on the oscilloscope and press the START ACQUISITION button. Adjust the oscilloscope for a display like the one shown in Figure 5-56 (500 mV/div for both channels, time base set to 10 ns/div).

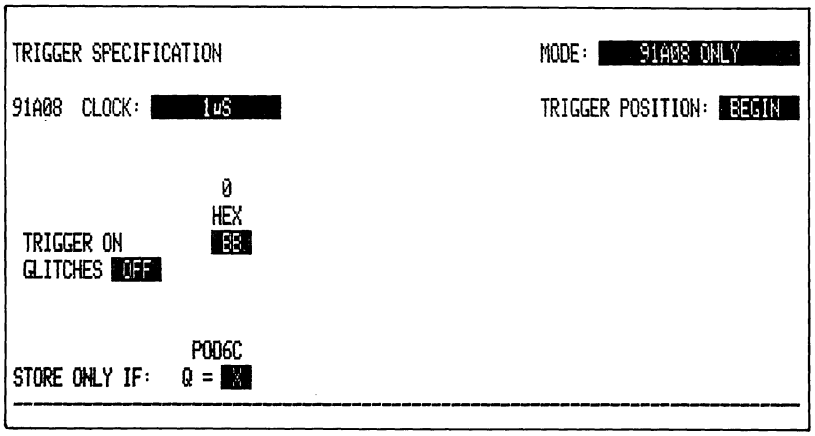


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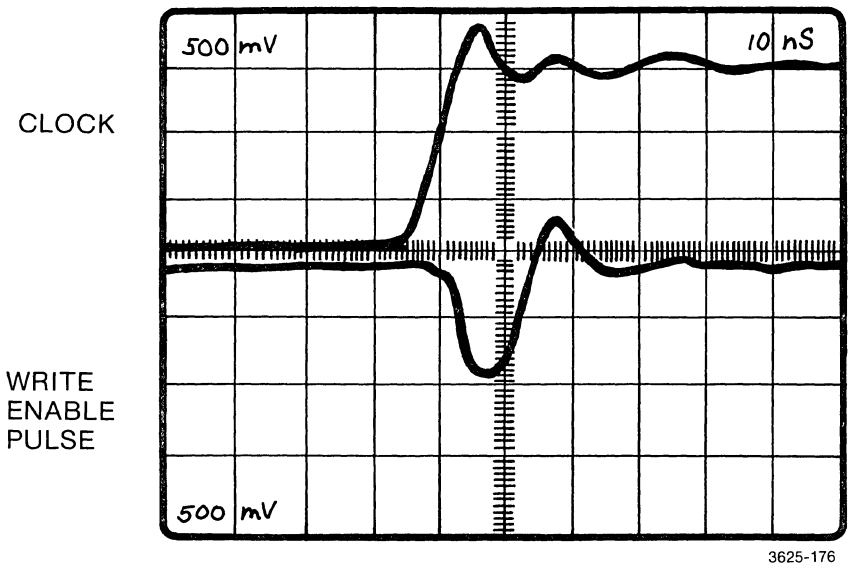
Figure 5-55. 91A08 write-enable adjustment menu.



3625-176

Figure 5-56. 91A08 write-enable timing.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

7. Adjust variable resistor R661 so the falling edge on channel 2 of the scope is 4 ns, ±0.5 ns after the rising edge in channel 1.

8. Adjust resistor R658 so the rising edge on channel 2 is 13 ns, ±0.5 ns after the rising edge in channel 1.

9. Verify that the falling edge on channel 2 was not disturbed by the rising edge adjustment. The oscilloscope display should now look exactly like Figure 5-56. If the time values shown on channel 2 of the scope are not accurate, perform steps 8 and 9 again until they are correct.

10. Move the probe for channel 1 to OW0 (TP481). Move the probe for channel 2 to OWE (TP485). The ground leads may be left where they were. Again, the oscilloscope display should look like the one shown in Figure 5-56.

11. Adjust variable resistor R665 so the falling edge on channel 2 of the oscilloscope is 4 ns, ±0.5 ns after the rising edge in channel 1.

12. Adjust resistor R668 so the rising edge on channel 2 is 13 ns, ±0.5 ns after the rising edge in channel 1.

13. Verify that the falling edge in channel 2 was not disturbed by the rising edge adjustment. The oscilloscope display should look exactly like Figure 5-56. If the time values shown in channel 2 are not accurate, perform steps 12 and 13 again until they are correct.

14. Read the introduction to the 91A08 external clock adjustment to see if that adjustment is needed by the 91A08 being adjusted.

External Clock Adjustment

This adjustment procedure should be performed only if one of the following parts of the 91A08 module has been replaced since the last adjustment.

Component Number	Component Type
A13Q601	Transistor
A13Q602	Transistor
A13U701	9685
A31U605	100163
A13U615	100102
A13U511	100102

This adjustment procedure assumes the 91A08 write-enable adjustment procedure has just been completed. Therefore, the 91A08 to be adjusted is on an extender and the DAS is turned on. (If this adjustment is not applicable, the DAS mainframe should be turned off, the test equipment disconnected, and the 91A08 module re-installed.)

The adjustment procedure involves taking data that is used to calculate the proper length of a cable. The cable acts as a delay line that controls when the clock signal arrives from the 100 MHz Clock Probe.

The following additional equipment is needed for this part of the adjustment:

- P6454 100 MHz Clock Probe
- 350 MHz, 2-channel oscilloscope

- Two probes for above oscilloscope
- 250 MHz variable amplitude pulse generator
- 50 Ω termination for the above pulse generator
- Wire strippers
- Soldering iron and solder

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

1. Connect the P6454 100 MHz Clock Probe to the 91A08 module. Do not connect a data acquisition probe to connector C.

2. Attach the 50 Ω termination to the output of the pulse generator. Adjust the pulse generator to:
   Low Voltage = 0.4 V
   High Voltage = 2.4 V
   Period = 500 ns
   High pulse width = 200 ns

3. Adjust the oscilloscope to:
   Channel A and B = 0.5 V/div
   Sweep = 2 ns/div

4. Attach both of the oscilloscope probes to the output of the pulse generator. Verify that both channels of the oscilloscope have the same propagation delay. If they do not have the same propogation delay, note which channel is slower and read the difference between the two channels to the greatest possible accuracy (increments of 0.2 ns should be possible). Record the difference in nanoseconds as SC. If there is no difference, record 0 ns. The SC value will be used in a later calculation.

5. Remove the oscilloscope from the output of the pulse generator. Connect the output of the pulse generator to the P6454 clock probe's clock input. Connect the ground of the pulse generator to the reference input of the clock probe.

6. Connect the slower of the two oscilloscope channels (the channel that had the right-most rising edge in step 4) to TP511 (if the delay is the same, either probe may be used). Connect the ground of the probe to any convienient ground on the board. Connect the other channel of the scope to the input of the clock probe (DO NOT connect it at the output of the pulse generator). Refer to Figure 5-57.

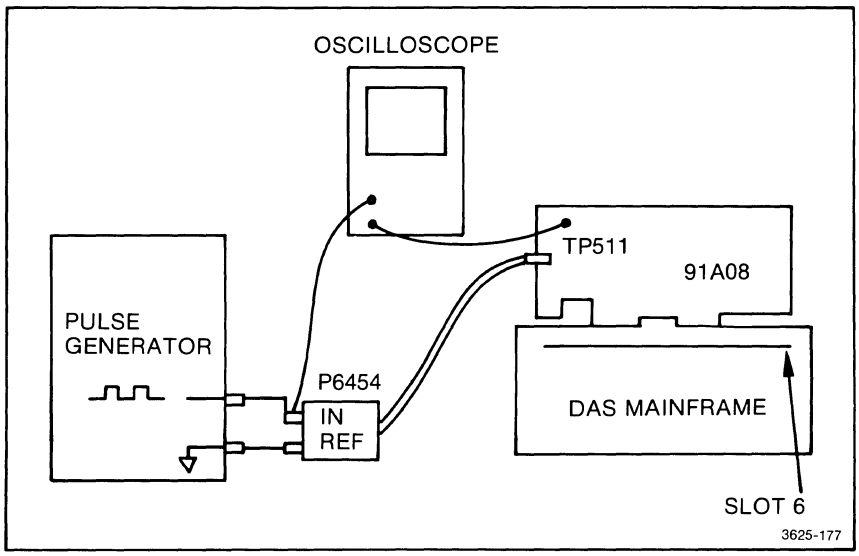


Figure 5-57. 91A08 clock delay adjustment equipment setup.

7. Enter the DAS Trigger Specification menu. The mode should already be set to 91A08 ONLY, and the TRIGGER ON field should contain only Bs. Change the clock to external rising edge. The menu should now look like Figure 5-58.

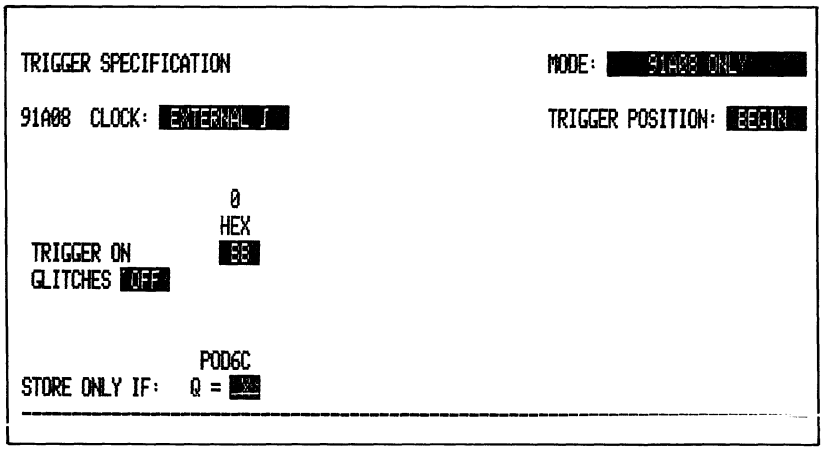


Figure 5-58. 91A08 clock delay adjustment menu.

8. Press the START ACQUISITION key. The channel connected to TP511 should display a clock.

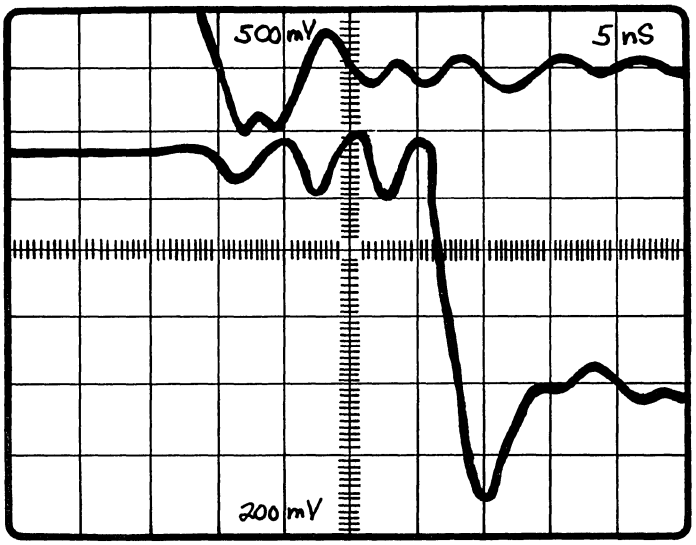


Figure 5-59. 91A08 clock delay adjustment waveform.

9. Adjust each channel of the oscilloscope so each of the two waveforms is centered around a horizontal graticule line. See Figure 5-59.

10. Read the time difference between the point where the input to the clock probe crosses its center line to where the signal on TP511 crosses its center line (the propagation time). Record this time in nanoseconds as TP.

11. Use the following formula to determine how much the clock delay must be lengthened or shortened.

    Adjustment (in) = (TP ns + SC ns − 21 ns) x (8 in/ns)

    Record the adjustment length in inches. Also record whether the result is positive or negative.

12. If the calculated adjustment is less than two inches in either direction, then the delay line is within specifications and does not need to be altered; the procedure is finished. Remove the test equipment, turn off the DAS mainframe, and re-install the 91A08 module.

    If the calculated adjustment is ⩾2 inches, then continue this procedure to perform steps 13 through 15.

13. On the 91A08 board, locate the coaxial cable soldered to jacks J302 and J705. Unsolder this cable from the circuit board and uncoil it from the toroid. If the adjustment length is positive go to step 14a. If the adjustment length is negative go to step 14b.

14a. If the adjustment length is positive, some cable must be removed from the delay line. Measure the distance specified as the adjustment length from either end. Clip the cable at that point (as accurately as possible). Go to step 15.

14b. If the adjustment length is negative, the cable needs to be longer than it is. Measure the length of the present cable. Add to this distance the adjustment length. Get another piece of cable (use only the cable type specified in the parts list). Cut this new cable to the length calculated above (cut as accurately as possible). Install connectors on both ends of the new cable. Throw the old cable away. Go to step 15.

15. Re-coil the modified cable around the toroidal form. Solder one end of the cable to J302 and the other end to J705. Return to step 8 and perform the procedure again from that point to verify that the cable is properly lengthened or shortened.

91P16 PATTERN GENERATOR MODULE ADJUSTMENTS

Pre-adjustment Test

The 91P16 Pattern Generator has a total of three different adjustments in two different circuitry areas. There are two adjustments to the write-enable circuitry of the stack. There is one adjustment to the strobe timing circuitry. Any test of these areas would require as much effort to perform as the actual adjustment, so no pre-adjustment test is given.

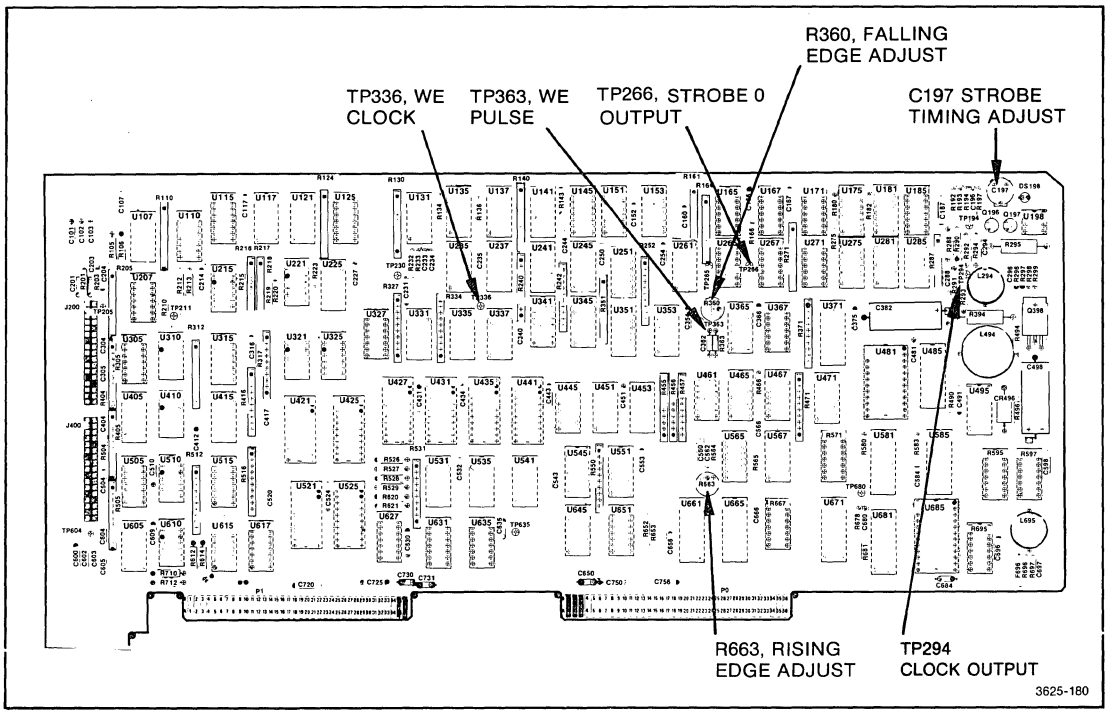


Figure 5-60. 91P16 test point and adjustment locations.

Strobe Timing Adjustment

You will need the following equipment to perform this procedure:

- DAS mainframe
- Main Extender board
- 100 MHz oscilloscope with two channels
- Two probes for the above oscilloscope
- Small slotted screwdriver

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the 91P16 Pattern Generator to be tested from the mainframe.
3. Adjust the square pin shorting jumpers on the Main Extender board to accept a 91P16 module.
4. Insert the Main Extender board in the slot where the 91P16 resided. Install the 91P16 on top of the extender.
5. Turn on the DAS. After the power-up sequence is done, enter the Pattern Generator menu.
6. With the Pattern Generator menu in PROGRAM mode, replace the instructions at sequence zero with the following program:

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0	A	XXXX	CALL	A	01

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If there are Pattern Generator Expanders in the system, there will be more output vector spaces (under the HEX field). Specify all output data as X (don't care). Set the Pattern Generator clock to 2 μs.

7. Enter the Pattern Generator Timing menu. Adjust all strobes shown in the menu to the following value.

DELAY	WIDTH	SHAPE
75nS	150nS	TTL

8. Attach the probe for channel 1 of the oscilloscope to test point TP294 on the 91P16. Attach the probe for channel 2 of the oscilloscope to TP266 (see Figure 5-60). Set the oscilloscope to trigger off a rising edge in channel 1. Attach the ground leads of the probes to any convenient ground point on the Pattern Generator.

9. Turn on the oscilloscope and press the START PAT GEN key on the DAS. Adjust the oscilloscope to show a display like the one shown in Figure 5-61.

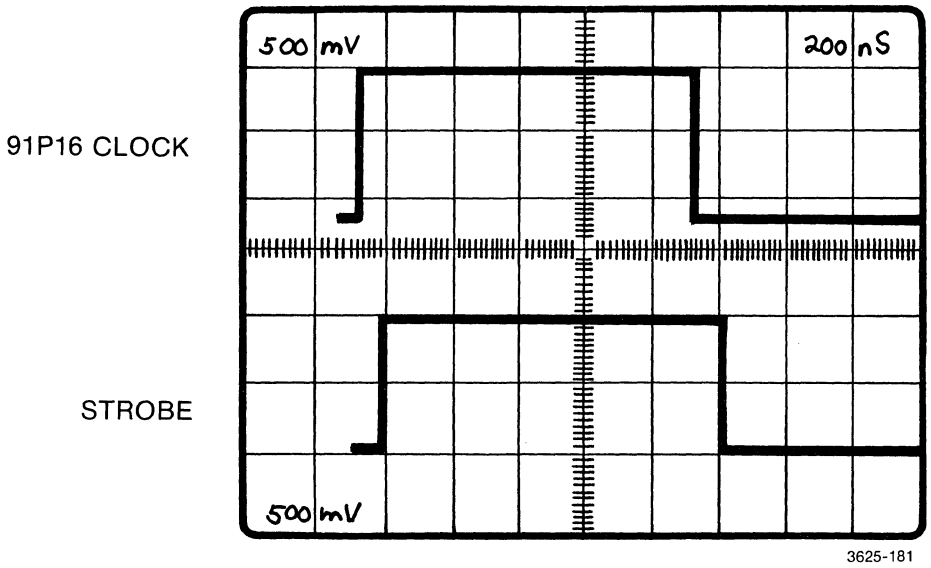

Figure 5-61. 91P16 strobe clock adjustment.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

10. Adjust capacitor C197 so the pulse width shown on channel 1 is 1.00 μs, $\pm$10 ns.

11. Perform the 91P16 write-enable adjustment procedure.

Write-Enable Timing Adjustment

The same equipment used to adjust the 91P16 strobe timing is used for this procedure. This procedure assumes that the strobe timing adjustment has just been performed so the 91P16 is on an extender and the oscilloscope is connected to the 91P16 board. The menu setup for this adjustment and the strobe adjustment is also identical.

1. Move the probe for channel 1 to test point TP336. Put the probe for channel 2 on TP363. Reconnect the probe ground leads as necessary. Adjust the oscilloscope to show a display like the one shown in Figure 5-62.

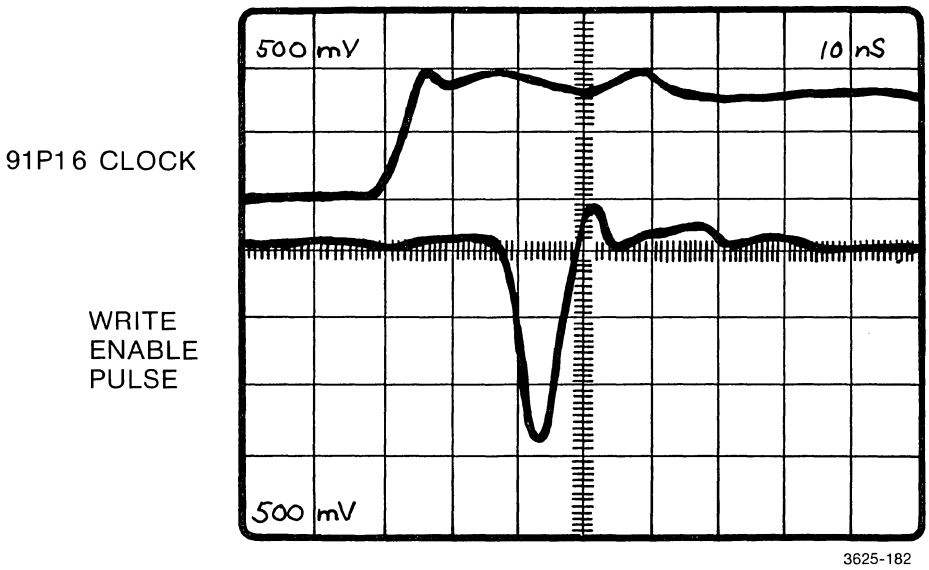

Figure 5-62. 91P16 write-enable adjustment timing.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

2. Adjust potentiometer R360 (see Figure 5-60) so the falling edge in channel 2 is 15 ns, ±1 ns after the rising edge in channel 1.

3. Adjust potentiometer R663 so the rising edge in channel 2 is 25 ns, ±1 ns after the rising edge in channel 1.

4. Verify that the rising edge adjustment did not disturb the accuracy of the falling edge position. The oscilloscope display should look like Figure 5-62. If the time values shown on the oscilloscope are not accurate, perform steps 2 and 3 again until they are correct.

5. Disconnect the oscilloscope. Turn off the DAS mainframe and reinstall the 91P16.

91P32 PATTERN GENERATOR EXPANDER MODULE ADJUSTMENTS

Pre-adjustment Test

The 91P32 Pattern Generator Expander has one adjustment that corrects strobe timing. Any test of this area would require as much effort as the actual adjustment, so no pre-adjustment test is given.

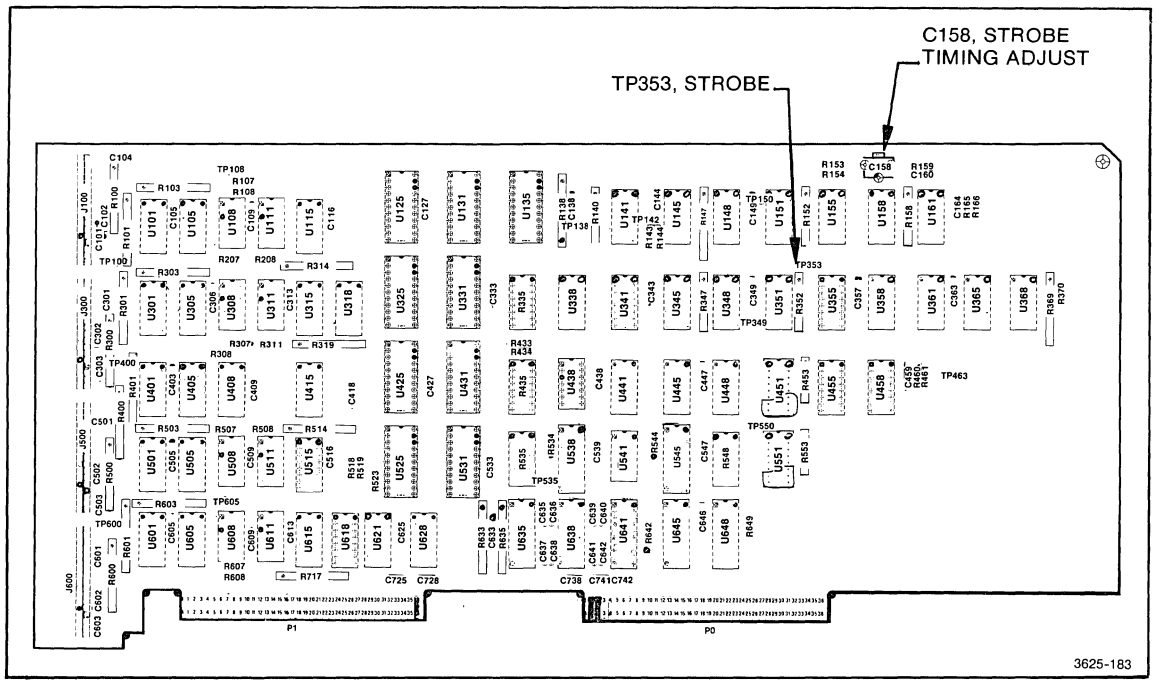

Figure 5-63. 91P32 test point and adjustment locations.

Strobe Timing Adjustment

You will need the following equipment to perform this procedure:

- DAS mainframe
- Main Extender board
- Small slotted screwdriver
- 100 MHz oscilloscope
- One probe for the above oscilloscope

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the Pattern Generator Expander to be adjusted from the mainframe.
3. Adjust the square pin shorting jumpers on the Main Extender board to accept a 91P32 module

4. Insert the Main Extender board in the bus slot where the 91P32 resided in the mainframe. Install the 91P32 on top of the extender.

5. Turn on the DAS. After the power-up sequence is done, enter the Pattern Generator Program menu.

6. With the Pattern Generator menu in PROGRAM mode, replace the instructions at sequence zero with the following program:

SEQ	LABEL	HEX	HEX	HEX	HEX	HEX	INSTRUCTIONS		STROBES
0	A	XXXX	XXXX	XXXX	XXXX	XXXX	CALL	A	0123456789

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If the system being used contains only one 91P32 (the one being adjusted), there will be eight fewer Xs under the HEX field and the DAS will only allow values 0 through 5 to be entered in the STROBES field. Either way, this adjustment will not be affected.

7. Enter the Pattern Generator Timing menu. Adjust all strobes shown in the menu to the following value.

DELAY	WIDTH	SHAPE
75nS	1.5555uS	SET

8. Attach the oscilloscope probe to test point TP353 on the 91P32 (see Figure 5-63). Attach the ground lead of the probe to any convenient ground point on the Pattern Generator Expander. Set the oscilloscope to trigger off a rising edge.

9. Turn on the oscilloscope and press the START PAT GEN key on the DAS. Adjust the oscilloscope to show a display like the one shown in Figure 5-64.

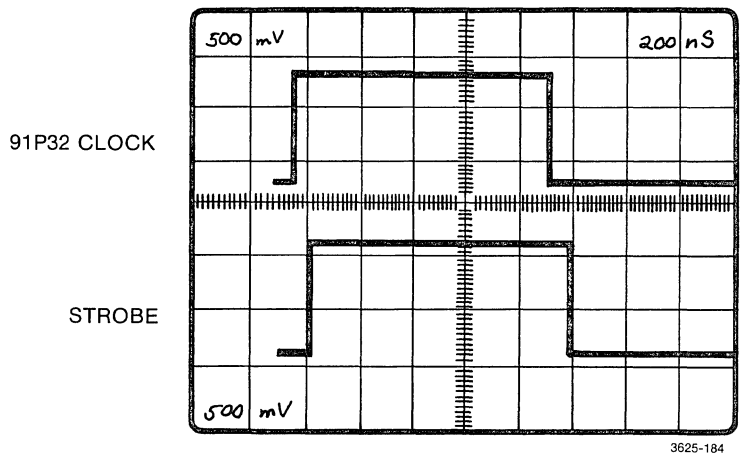


Figure 5-64. 91P32 strobe clock adjustment.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

10. Adjust capacitor C158 so the pulse width shown on channel 2 is 1.00 μs, $\pm$10 ns.

11. Disconnect the oscilloscope. Turn off the DAS mainframe and reinstall the 91P32 module.

TAPE DRIVE (OPTION 01) ADJUSTMENT

Pre-adjustment Test

The tape drive, Option 01 for the DAS, has one adjustment that sets the gain of the programmable gain amplifier. This adjustment should only be performed if the tape drive is repaired or if the drive will not pass the performance check.

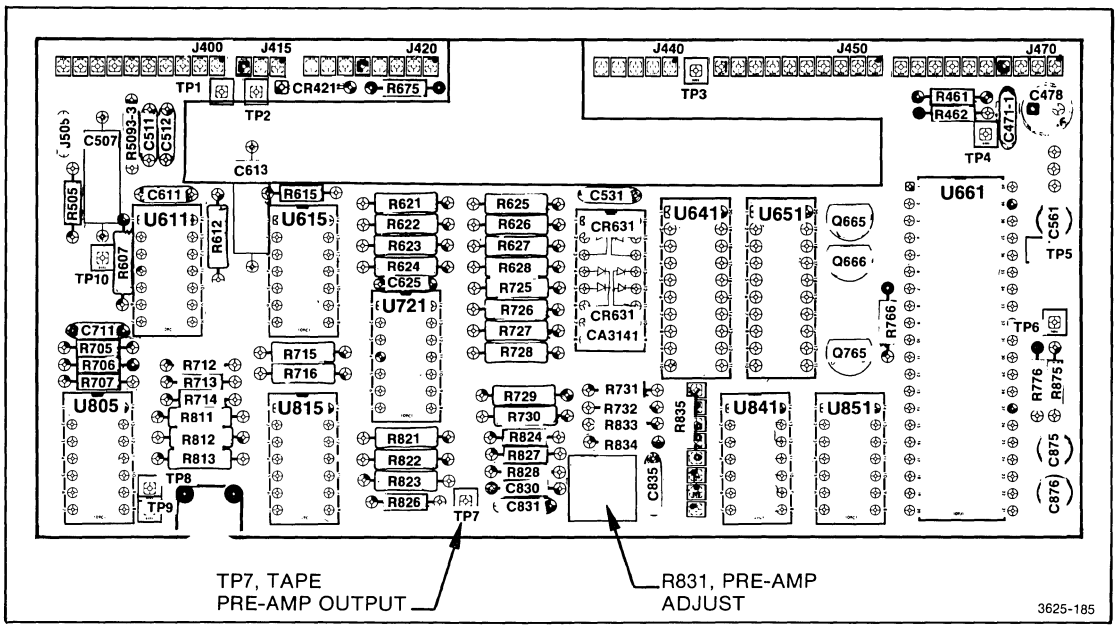


Figure 5-65. Tape Drive test point and adjustment locations.

Readback Gain Adjustment

You will need the following equipment to perform this procedure:

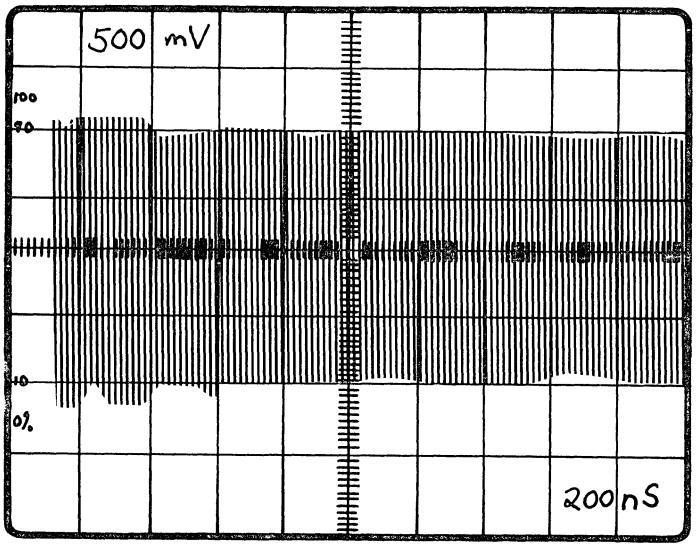
- DAS mainframe
- Tape Drive Extender cable
- DAS formatted data cartridge
- Small slotted screwdriver
- Oscilloscope
- Probe for the above oscilloscope

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

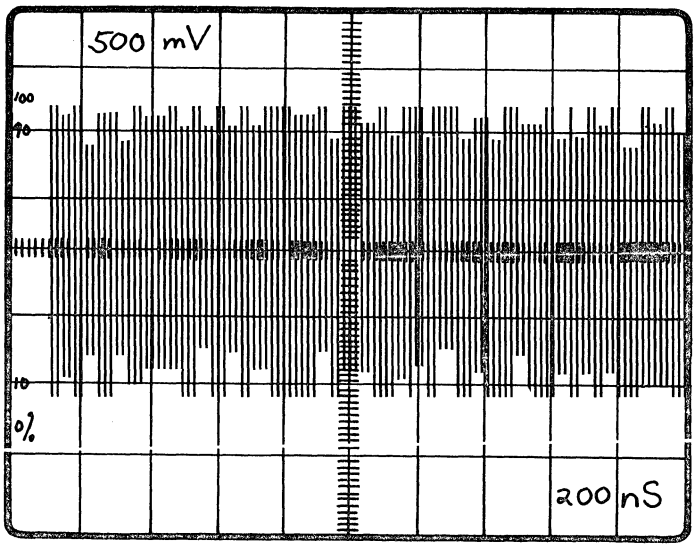
1. Turn off the DAS mainframe.
2. Remove the front fan from the mainframe. The adjustment is located under the front fan housing, and is inaccessible while the front fan is in the mainframe. Instructions for removing the front fan may be found in the Maintenance: General Information section.
3. The top of the tape drive unit should now be exposed for adjustment access. Reinstall only the Controller and Trigger/Time Base boards that were removed while removing the fan. No other modules should be reinstalled at this time.
4. Turn on the DAS mainframe while holding down the STOP key to cause a power-up self-test failure. Press START SYSTEM to enter the diagnostic menu.
5. Select to run tests on slot 0, the Controller. Set the diagnostics for single mode, function 2 (TAPE READ).
6. Insert the DAS formatted data cartridge in the tape drive.
7. Connect a channel of the oscilloscope to TP7 on the Tape Drive Data board (A18A1). Set the oscilloscope 500 mV/div and 2 ms/div with triggering on the positive slope.
8. Press START SYSTEM. There are two waveforms illustrated in Figures 5-66 and 5-67. Figure 5-66 illustrates the expected waveform when a formatted tape with no data is used. Figure 5-67 illustrates the expected waveform from a formatted tape with data.
9. Refer to Figure 5-66 and adjust R831 on the Tape Drive Data board to obtain a 2 V peak-to-peak waveform. Note that the waveform amplitude is data-dependent, and that the 2 V peak-to-peak is an average or center value for this adjustment. The tolerance for the 2 V peak-to-peak is greater than the data-dependent amplitude variations.

10. Turn off the DAS mainframe and disconnect the test equipment. Reinstall the front fan and fan housing and replace all instrument modules.



A
(FORMATTED TAPE)

Figure 5-66. Tape Drive adjustment with no data.



B
(TAPE WITH DATA)

Figure 5-67. Tape Drive waveform with data.

PERFORMANCE CHECK

The Performance Check Procedure provides a detailed check of internal and external product characteristics. These checks can be extensive and time-consuming. Under normal circumstances the Functional Check Procedures will provide an adequate test of product performance in a less costly manner.

The Performance Check Procedure is organized into sets of tests for each sub-assembly of the mainframe, for each type of instrument module, for each probe type, and finally for each option type.

MAIN POWER SUPPLY PERFORMANCE CHECK

There is no performance check procedure for the DAS main power supply. The functional check, given previously, verifies all of the performance requirements of the supply.

+5 V POWER SUPPLY PERFORMANCE CHECK

There is no performance check procedure for the DAS +5 V power supplies. The functional check, given previously, verifies all of the performance requirements of the supplies.

KEYBOARD PERFORMANCE CHECK

There is no performance check procedure for the keyboard. The functional check, given previously, is sufficient to verify the operation of the keyboard.

MOTOROLA DISPLAY MONITOR PERFORMANCE CHECK

There is no performance check procedure for the Motorola Display Monitor. The functional check, given previously, is sufficient to verify the operation of the Motorola Display Monitor.

COLOR DISPLAY MONITOR PERFORMANCE CHECK

WARNING

This procedure makes high voltages (up to 21 kV) accessible to the technician. Watch your fingers while probing in the display monitor.

(1) Performance Check Setup Procedure

You will need the following equipment to perform the next adjustment procedures:

- DAS9129 mainframe with the monitor to be adjusted installed
- Slotted screwdriver
- POZIDRIV-type screwdriver

WARNING

Do not remove or install any panels on a DAS mainframe while the power is on. Doing so could cause a temporary high voltage short to the panel that would be dangerous for the technician.

1. Turn off the DAS mainframe.
2. Remove the top outside panel of the DAS mainframe. Also remove the mainframe side panel that is adjacent to the color display monitor.
3. Remove the eight screws (6-32 x 0.250) securing the black monitor cover to the monitor itself. Do not try to lift the cover off yet.
4. Remove the three screws (6-32 x 0.250) securing the side of the monitor cover to the bottom rail of the mainframe.

CAUTION

Do not bend or dent the soft mu-metal shield. If it is bent or dented, it may retain strong magnetic fields that will distort the color purity. Distortion caused by dents in the mu-metal shield cannot be removed by the degaussing coil.

5. Lift the black enamelled cover and the mu-metal shield out of the mainframe. Observe that the tapered end of the mu-metal shield is toward the rear of the mainframe.

The display monitor is now exposed so test points are accessible for measurements.

(2) Risetime Verification

WARNING

The following measurements are made in a high voltage region (up to 21 kV). Use caution when probing in these areas.

The only performance requirement for the color display monitor that requires checking is the video risetime.

You will need the following additional equipment to perform this procedure:

- 60 MHz oscilloscope with probe
- 2.2 pF, 200 V capacitor

1. Connect the 2.2 pF capacitor to the oscilloscope probe as shown in Figure 5-68. The video signals from the Z-axis board will be monitored through this capacitor.

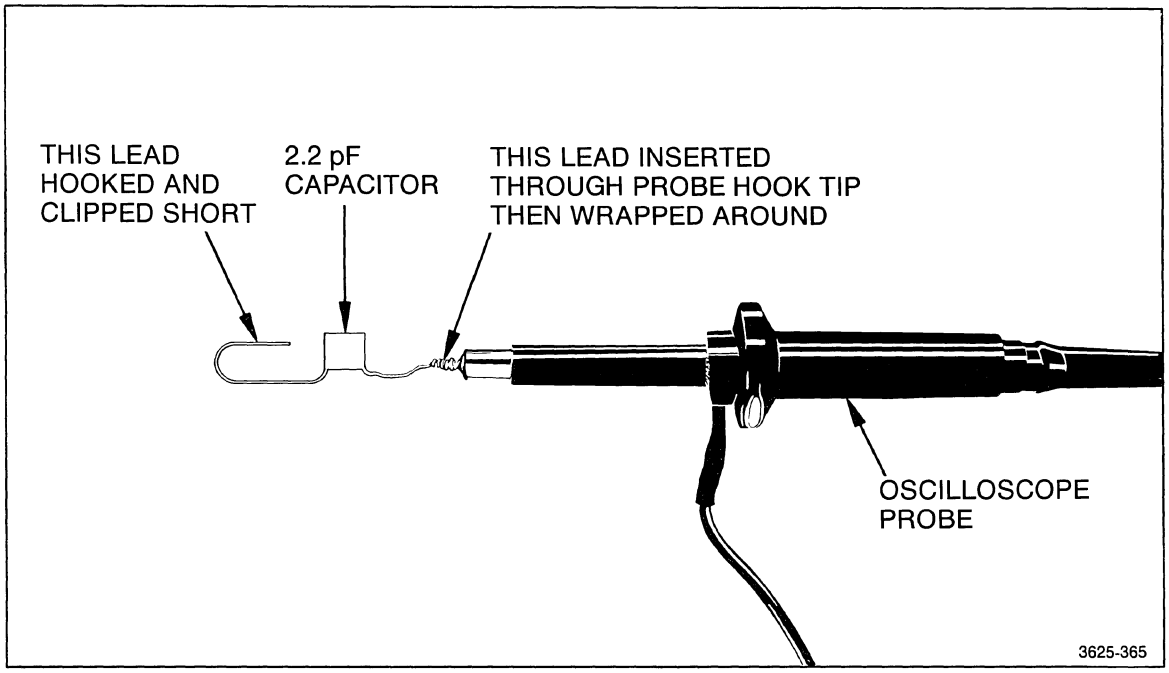


Figure 5-68. Connecting the 2.2 pF capacitor to the oscilloscope probe.

2. Turn on the DAS mainframe.

3. Connect the free end of the 2.2 pF capacitor to test point TP230, the green video signal, on the Z-axis board (see Figure 5-69 for the location of the test point).

4. Adjust the oscilloscope for as stable a trace as possible. The rise time for any video pulses should be less than 35 ns.

5. Remove the free end of the 2.2 pF capacitor from TP230 and connect it to TP240, the red video signal. Again, the rise time for the video should be less than 35 ns.

6. Remove the free end of the 2.2 pF capacitor from TP240 and connect it to TP250, the yellow video signal. The rise time for this signal should be less than 35 ns.

7. Remove the capacitor from the tip of the oscilloscope probe.

This completes the performance check of the color display monitor. There are some supplemental tests to check functionality of the monitor that follow. If you do not wish to perform these extra tests, the test setup may now be dismantled.

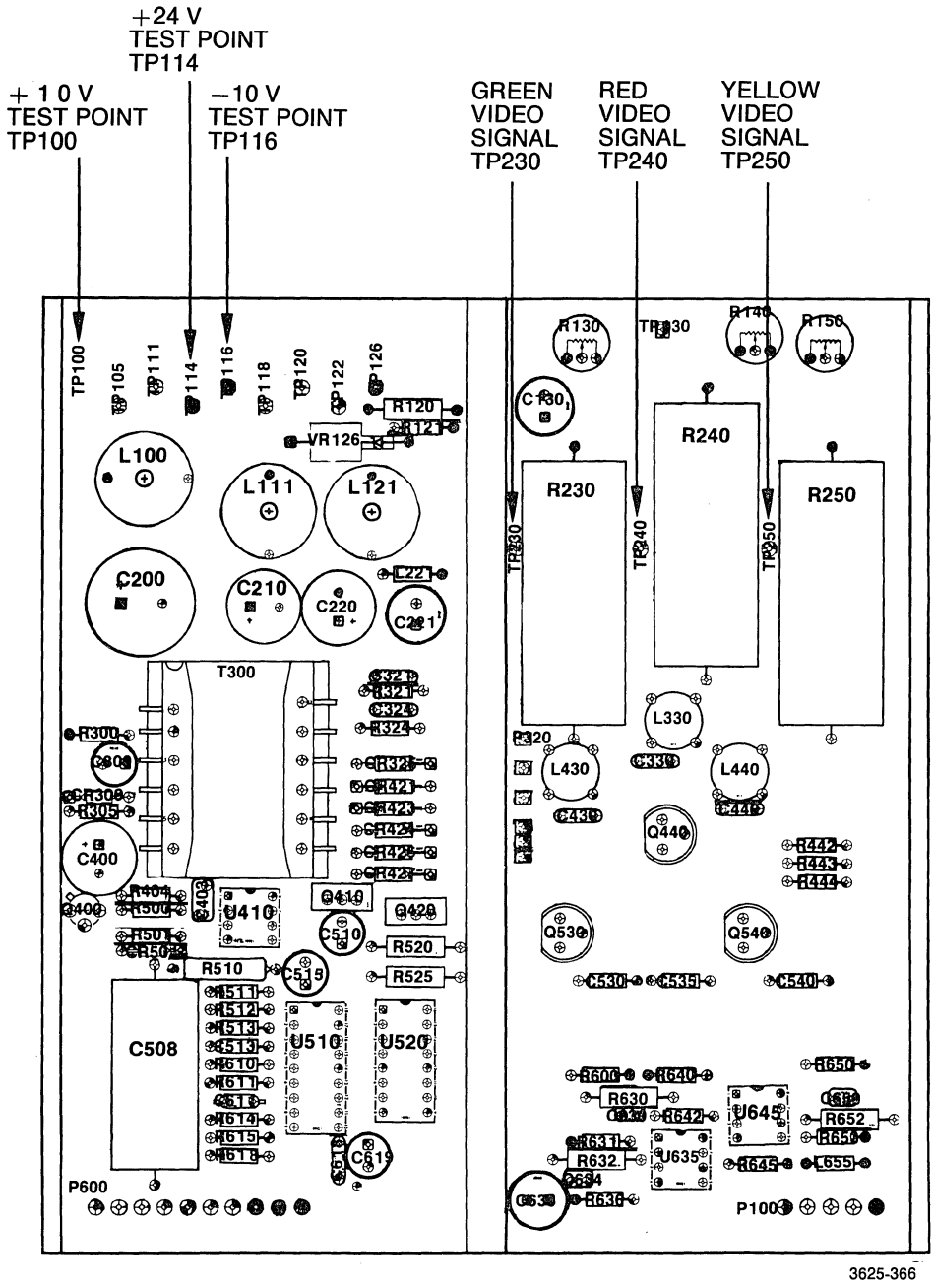


Figure 5-69. Color Display Monitor performance check test points, Z-axis board.

WARNING

Turn off the DAS mainframe before replacing the covers on the display monitor and the mainframe. Failure to do so may cause temporary high voltage shorts in the mainframe.

The next steps are procedures that can be used to check the functionality of the color display monitor.

NOTE

The rest of the tests for the color display monitor are not performance checks. They are supplemental verification procedures that should not be interpreted as performance requirements.

(3) Monitor Power Supply Checks

WARNING

The following measurements are made in a high voltage region (up to 21 kV). Use caution when probing in these areas.

The following checks verify the functions of the display monitor power supply. You will need the following additional equipment to perform these checks:

- 60 MHz oscilloscope with probe
- Digital multimeter (DMM)
- 200 Ω, 10 W resistor

1. The display monitor should still be uncovered and the power to the DAS mainframe should be on.
2. Examine the voltages provided by the display monitor power supply. The power supply and all the following test points are located on the Z-axis board of the monitor.
3. With a DMM, examine the voltage at TP100 on the Z-axis board. The DMM should read between +104 and +116 V dc.
4. Examine the voltage at TP114 on the Z-axis board. The DMM should read between +22.6 and +25.4 V dc.
5. Examine the voltage at TP116 on the Z-axis board. The DMM should read −10.4 and −9.6 V dc.

6. Connect the 200 Ω, 10 W resistor firmly to ground. After making the ground connection, connect the other end of the 200 Ω resistor to TP100 on the Z-axis board (the +110 V supply).

   The connection to ground should cause the +110 V supply to current limit. This is made evident by a dim, flickering display with a reduced scan.

7. Remove the 200 Ω resistor from the +110 V supply. Also remove the resistor from its ground connection (the 200 Ω resistor will not be used again here).

8. Connect an insulated wire firmly to ground. Touch the end of the wire to the following test points on the Z-axis board in sequence. Each time the connection is made, the display should malfunction. Each time the connection is removed, the display should return to normal.

- TP100. The +110 V dc supply
- TP114. The +24 V dc supply
- TP116. The −10 V dc supply

9. Remove the shorting wire from any test point and disconnect the ground connection.

10. With the oscilloscope, observe the voltage at TP105 on the Z-axis board. The waveform should look like Figure 5-70.

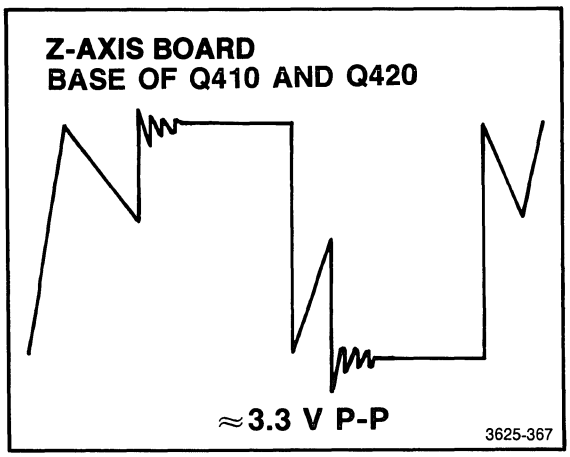


Figure 5-70. Color Display Monitor power supply waveform (horizontal 10 μs/div., vertical 5 V/div).

If the neutral times are wide, or the waveform is not stable, check U510 on the Z-axis board. In particular, examine the beam current sense signals into U510 pins 1 and 2, and the +12 V current sense signals into U510 pins 6 and 7.

11. With the DMM, examine TP100 on the Z-axis board (+110 V dc). While monitoring the voltage on this test point, turn off the DAS mainframe. The voltage should immediately decrease to zero. This prevents bright flashes when the DAS mainframe is turned off and then on again (a dim flash is normal).

If the +110 V supply stays high, check CR552, C523, Q443, and assosciated circuitry on the deflection board.

This completes the supplemental power supply checks. If you do not wish to perform the rest of the supplemental checks, leave the DAS mainframe turned off and reassemble the mechanical package.

NOTE

The following tests are not performance checks. They are supplemental verification procedures that should not be interpreted as performance requirements.

(4) Supplemental Color Display Monitor Checks

WARNING

The following measurements are made in a high voltage region (up to 21 kV) . Use caution when probing in these areas.

The following checks verify a variety of functions in the color display monitor. You will need no additional equipment, beyond that already used in the previous tests.

1. The display monitor should still be uncovered and the power to the DAS mainframe should be on.

2. Use an oscilloscope to monitor test point TP265 (deflection board). The waveform on TP265 is riding on top of approximately 110 V, so the oscilloscope should be ac coupled.

3. TP265 should exhibit a parabolic waveform of approximately 2.2 V amplitude and 16.6 ms period. See Figure 5-71. There should be no lumps and the waveform should be symmetrical. If there are problems, examine U116B and Q507 on the deflection board of the monitor.

4. Remove the oscilloscope from the mainframe. With the DMM, check the voltage on the CRT filament. Connect the low probe of the DMM to test point TP126 on the Z-axis board. Connect the high probe of the DMM to end of R640 on the deflection board that is nearest the transformer shield (see Figure 5-69). The voltage read by the DMM should be 6.0 V dc, ±0.3 V.

5. Remove the DMM from the display monitor. Turn the rear panel intensity control up to maximum. Turn off the DAS mainframe. Turn the mainframe back on while holding down the STOP key.

   If the monitor comes up with a dim, flickering display, the current limit delay circuit is malfunctioning. Check Q400 and associated circuits on the Z-axis board.

6. Turn down the intensity control on the back panel to a comfortable level. Press the START SYSTEM key to enter the Diagnostics menu and select to run tests on slot 0, the Controller.

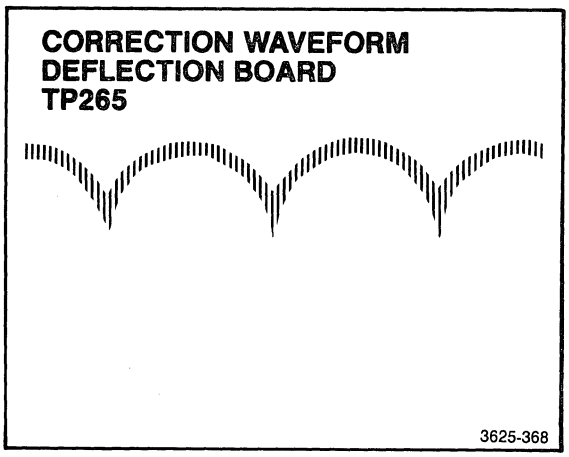


Figure 5-71. Color Display Monitor horizontal bowing correction waveform (horizontal 5 ms/div., vertical 1 V/div).

7. Select SINGLE mode, then select to run function 1; the DISPLAYS function. Start this test by pressing START SYSTEM.

8. Press the SELECT button once to enter an all red display. Carefully note the current setting of the intensity range trimmer, R270 on the deflection board.

9. Increase the rear panel intensity control to maximum. Then increase the intensity range trimmer, R270, while watching the screen of the CRT. The display should collapse to a dim, flickering picture. This verifies that the current limiting circuit is operating.

10. Return the intensity range trimmer, R270 on the deflection board, to its original position. Reduce the rear panel intensity control to a comfortable level.

This completes the supplemental checks of the color display monitor. The test setup may now be dismantled.

WARNING

Turn off the DAS mainframe before replacing the covers on the display monitor and the mainframe. Failure to do so may cause temporary high voltage shorts in the mainframe.

CONTROLLER BOARD PERFORMANCE CHECK

There is no performance check procedure for the Controller board. The functional check, given previously, is sufficient to verify the operation of the Controller board.

TRIGGER/TIME BASE BOARD PERFORMANCE CHECK

To verify complete operation of the Trigger/Time Base board, the functional check for the board should be performed before attempting this performance check. You will need the following equipment to perform this performance check procedure:

- DAS 9100 mainframe
- DAS Service Maintenance Kit
- P6452 External Clock Probe
- 100 MHz frequency counter with 1% resolution
- 2 channel 100 MHz oscilloscope
- 100 MHz pulse generator with variable amplitude and width
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy

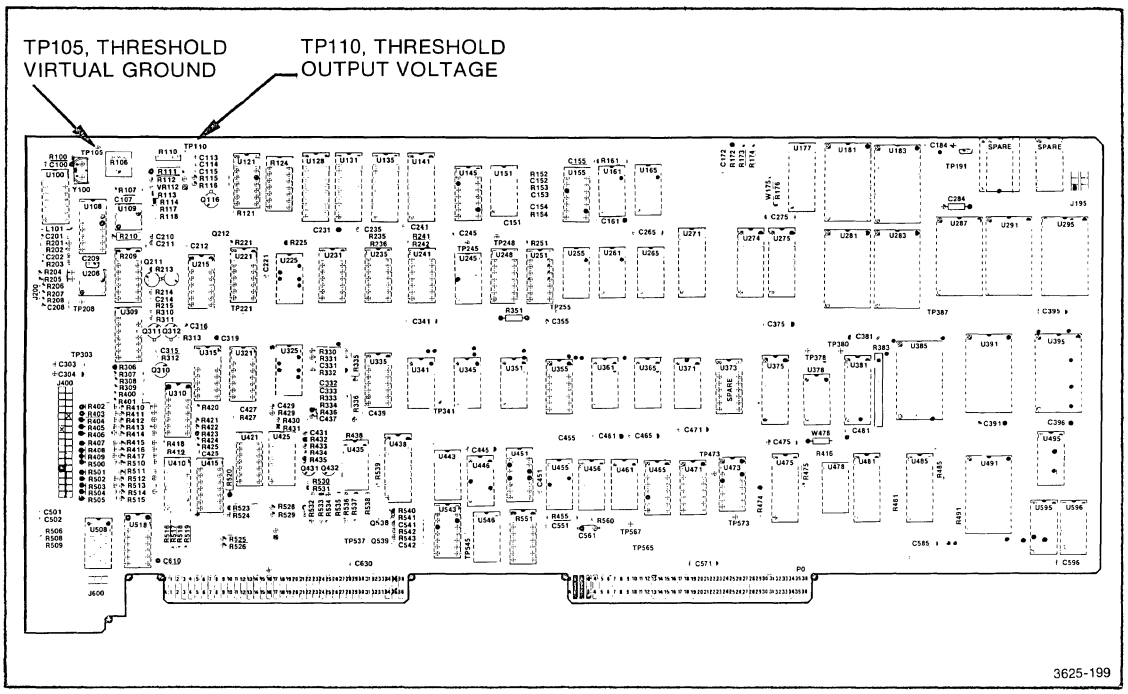


Figure 5-72. Test points on the Trigger/Time Base used in this performance check.

For instructions on use of the various menus, refer to the Operating Information section of this manual. Refer to the beginning of this Verification and Adjustment Procedures section for information on using the Main Extender board in the DAS Service Maintenance Kit.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

(1) Setup for the Performance Check

These steps set up the mainframe for the entire performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove the Trigger/Time Base in the mainframe and install the Main Extender Board from the Service Maintenance Kit in slot 7 of the mainframe. Make sure the jumpers on the extender are in the proper configuration for a Trigger/Time Base.
3. Install the Trigger/Time Base to be tested on top of the extender.
4. Connect the P6452 External Clock Probe to the pod connector at the rear of the Trigger/Time Base module.
5. Verify that the recessed slide switch on the back of the probes is set to the NORM position on the probe.
6. Turn on the DAS mainframe while holding down the STOP key to cause a power-up self-test failure. Enter the Diagnostics menu by pressing START SYSTEM.
7. Select to run diagnostic tests on slot 7. Select SINGLE mode, FUNCTION 6 to run the DAC THRSH function on the Trigger/Time Base board.
8. Connect the DMM to read the voltage between TP105 (ground) and TP208 (positive) on the Trigger/Time Base board (see Figure 5-72).

(2) Threshold Accuracy Check

The next steps verify the accuracy of the digital-to-analog converter (DAC) in the Trigger/Time Base board. This DAC controls the threshold voltage of the P6452 External Clock Probe. These steps assume the immediately preceding test setup is completed.

1. Press the START SYSTEM key. The DAS display should still show the Diagnostics menu. The cursor should be in a field that reads +0.000 V. The DMM should now read somewhere between −0.005 V and +0.005 V.

2. Locate the recessed slide switch on the back of the external clock probe. Set the position of the switch to auxiliary. The DMM should now read between −0.020 V and +0.020 V.

3. Press the SELECT key on the DAS keyboard. The DAC THRESHOLD SET field should read +1.600 V. The DMM should read somewhere between +6.18 V and +6.62 V.

4. Locate the recessed slide switch on the back of the external clock probe. Slide the switch back to the normal position. The DMM should now read between +1.579 V and +1.621 V.

5. Press the SELECT key again. The DAC THRESHOLD SET field should read −1.5875 V. The DMM should read between −1.609 V and −1.566 V.

6. Again locate the recessed slide switch on the back of the external clock probe and set it to the auxilary position. The DMM should now read between −6.56 V and −6.13 V.

7. Set the slide switch on the back of the external clock probe back to the normal position. Disconnect the DMM from the Trigger/Time Base board. Attach the ground of one channel of the oscilloscope to TP105 on the Trigger/Time Base board. Attach the input of the oscilloscope channel to TP208 (see Figure 5-72).

(3) DAC Voltage Selectability Check

The ability of the DAC to select all possible threshold voltages is now tested.

1. Press SELECT on the DAS keyboard. The DAC THRESHOLD SET field should read RAMPING.

2. Adjust the oscilloscope to show a voltage ramp made of discrete steps from high to low. Examine the ramp carefully to see whether any of the bits along the stair steps are misplaced.

3. Disconnect the oscilloscope from the Trigger/Time Base board.

(4) Setup for the External Clock Check

The next steps set up test equipment and the DAS mainframe to perform the external clock check.

1. Connect the external clock probe to pod connector C on the rear edge of the Trigger/Time Base.

2. Connect all seven input lines of the external clock probe to the output of the pulse generator. Connect the GND SENSE line of the probe to the ground of the pulse generator.

3. Press TRIGGER SPEC on the DAS keyboard. The DAS should display the Trigger Specification menu. Move the cursor to the 91A32 CLOCK field.

4. Press SELECT to select the external rising edge clock. Adjacent to the field saying EXTERNAL is a field saying TTL. Move the cursor into the field with TTL and press SELECT. The field should now read VAR.

5. Adjacent to the VAR field is a field containing −1.30 V. Move the cursor into the field saying −1.30 V. Press and hold down the INCR key of the DAS. The field should increment as long as the key is pressed. Set the field to show +0.00 V.

(5) External Clock Check

These steps verify the external clock line receivers. It is assumed that the previous test setup is completed.

1. Set the pulse generator to a 25 MHz (40 ns) pulse wave. Set the pulse wave so the low pulse is 19 ns long. Set the amplitude of the pulse wave to 500 mV peak to peak centered around ground.

2. Examine the output of the pulse generator with the oscilloscope. Verify that the output of the pulse generator has a 19 ns low pulse and a 40 ns cycle time with an amplitude of 500 mV.

3. With the oscilloscope, examine the waveforms on pins B1, A2 and B4 on P1 of the Main Extender board. These pins should show a 40 ns ECL level clock signal. These signals must have a high pulse that is at least 11 ns wide.

4. With the oscilloscope, examine the waveforms on pins A1, B3, and A4 on P1 of the Main Extender board. These pins should show a 40 ns ECL-level clock signal. These signals must have a low pulse that is at least 11 ns wide.

5. Set the pulse generator so the high pulse is 19 ns long. The amplitude and duty cycle should remain the same.

6. Examine the output of the pulse generator with the oscilloscope. Verify that the output of the pulse generator has a 19 ns high pulse and a 40 ns cycle time with an amplitude of 500 mV.

7. With the oscilloscope, examine the waveforms on pins B1, A2 and B4 on P1 of the Main Extender board. These pins should show a 40 ns ECL level clock signal. These signals must have a high pulse that is at least 11 ns wide.

8. With the oscilloscope, examine the waveforms on pins A1, B3, and A4 on P1 of the Main Extender board. These pins should show a 40 ns ECL-level clock signal. These signals must have a low pulse that is at least 11 ns wide.

(6) Internal Clock Check

The next steps verify the accuracy of the internal clock provided by the Trigger/Time Base.

1. Press the TRIGGER SPEC key on the DAS. The display should show the Trigger Specification menu.

2. Move the cursor on the DAS screen into the 91A32 CLOCK field. Press the SELECT button until the field reads 1 μs. Then press the DECR button and hold it down. The field should decrement until it shows 40 ns.

3. Connect the frequency counter to pin A15 on P1 of the Main Extender Board. Press the START ACQUISITION key on the DAS keyboard.

4. The frequency counter should read 25 MHz, $\pm$1%.

This completes the Trigger/Time Base performance check. The test setup may now be dismantled. Turn off the mainframe before removing the Main Extender board or the Trigger/Time Base board. This prevents damage to the extender board, modules, or the mainframe.

91A32 DATA ACQUISITION MODULE PERFORMANCE CHECK

To verify complete operation of the 91A32 Data Acquisition Module, the functional check for the board should be performed before attempting this performance check. You will need the following equipment to complete this performance check procedure.

- DAS mainframe
- DAS Service Maintenance Kit
- DAS Setup/Hold Time Test Fixture
- TM 500 Mainframe
- 50 Ω coaxial cable with male BNC connectors on each end
- 100 MHz, 2 channel oscilloscope
- 100 MHz signal generator with adjustable amplitude
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy
- Four P6452 Data Acquisition Probes
- P6452 External Clock Probe

For instructions on use of the various menus, refer to the Operating Information section of this manual. Refer to the beginning of this Verification and Adjustment Procedures section for information on using the Main Extender board in the DAS Service Maintenance Kit.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

(1) DAS Setup/Hold Time Test Fixture Setup

These steps set up the DAS Setup/Hold Time Test Fixture so the sample rate, data setup and hold, and qualifier setup and hold times can all be verified.

1. Locate the 8-inch coaxial cable that comes with the DAS Setup/Hold Time Test Fixture. Connect this cable between the Data Delay connectors on the test fixture.

CAUTION

The DAS Setup/Hold Time Test Fixture was calibrated with the 8-inch coaxial cable that came with the fixture. The electrical length of this cable is critical to the operation of the fixture. Do not replace this cable with any other, except a cable with the same Tektronix part number.

2. Install the DAS Setup/Hold Time Test Fixture in a TM 500 mainframe according to the instructions that come with the test fixture.

3. Set up the signal generator. Set the signal generator to a 25 MHz output with a 50% duty cycle that is symmetrical about ground. Set the amplitude of the signal generator to 1 V peak to peak.

4. Connect the output of the signal generator to the CLOCK IN of the Setup/Hold Time Test Fixture with a 50 Ω coaxial cable.

(2) DAS Mainframe Setup for the Setup/Hold Time Test

The next steps set up the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe and install the 91A32 module to be tested in slot 2. This may require removing a module already occupying this space.

2. Connect all four of the P6452 Data Acquisition Probes to the pod connectors on the rear edge of the 91A32.

3. Verify that the recessed slide switches on the back of the four probes are all set to NORM.

4. Connect all four data acquisition probes to the four 00-FF outputs of the Setup/Hold Time Test Fixture. (Use the lead sets provided with the test fixture.)

5. Connect the P6452 External Clock Probe to pod connector C of the Trigger/Time Base module in the DAS (slot 7).

6. Verify that the recessed slide switch on the back of the external clock probe is set to the NORM position.

7. Connect the CLK1 input of the external clock probe to the rising edge clock output of the test fixture. For this connection, use the high-speed flying lead set provided with the test fixture.

8. Connect the ground sense lead of the external clock probe to the ground lug of the DAS Setup/Hold Time Test Fixture.

(3) DAS Menu Setup for the Setup/Hold Test

The next steps organize the DAS menus so data can easily be acquired by and read from the 91A32 module under test.

1. Turn on the DAS mainframe.

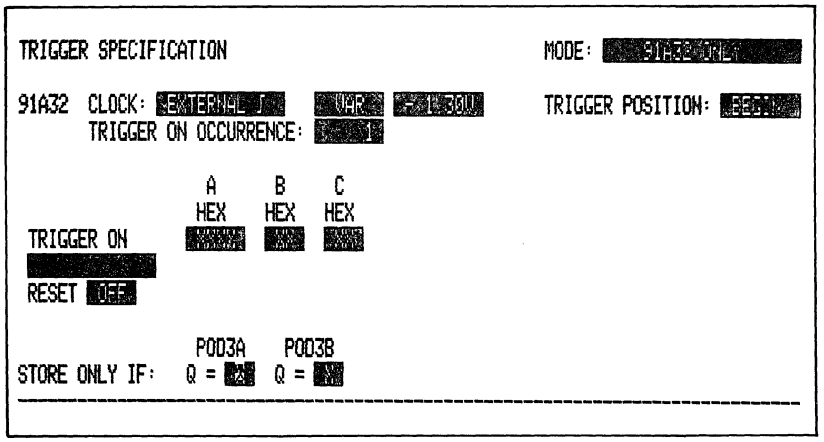
2. Press the TRIGGER SPEC key to enter the Trigger Specification menu.

3. Move the screen cursor into the 91A32 CLOCK field. Press SELECT until external rising edge is selected.

4. Move the cursor on the DAS screen into the field that reads TTL. Press SELECT. This field should now read VAR and the field adjacent to it should read −1.30 V. The DAS screen should now be similar to the menu shown in Figure 5-73.

5. Press the CHANNEL SPEC key on the DAS to enter the Channel Specification menu.

6. The screen should now show the Channel Specification menu. Under THRESHOLD on the third line of the screen are some fields that all read TTL. For groups A, B, and C, change all the TTLs to VAR by moving the cursor into the TTL field and pressing the SELECT key. Groups A, B, and C should now read VAR −1.30 V.



3625-200

Figure 5-73. 91A32 setup/hold time testing trigger.

(4) Adjustments for the 19 ns High Check

The adjustments made in these steps allow the sample rate, setup, hold, and qualifiers to be checked with a non-symmetric clock that has a 19 ns high pulse in a 40 ns period.

1. Turn on the signal generator and the TM 500 mainframe containing the Setup/Hold Time Test Fixture.

2. Examine one of the clock outputs of the setup/hold fixture with the oscilloscope. Adjust the output of the signal generator until the test fixture clock output has a 19 ns high pulse with a 40 ns cycle time.

(5) 19 ns High Data Setup and Hold Time Tests

These steps verify the data setup and hold times with a 19 ns high external clock.

1. Press the "TH 0ns" button on the test fixture.

2. Press the START ACQUISITION key on the DAS. The DAS should trigger and show alternating Fs and 0s in groups A, B, and C on the State Table menu.

3. Press the TIMING DIAGRAM key on the DAS. Adjust the timing diagram to show pods 2A and 2B. Increase the magnification until the waveforms are discernable. All of the waveforms should have a 50% duty cycle and all should be in sync.

4. Adjust the timing diagram to show pods 2C and 2D. The new waveforms should be identical to the waveforms shown on pods 2A and 2B.

5. Press the "TSU 29ns" button on the Setup/Hold test fixture.

6. Press the START ACQUISITION key on the DAS again. The Timing Diagram menu should update itself. The new display should show alternating Fs and 0s with a 50% duty cycle.

7. Adjust the timing diagram to show pods 2A and 2B. The new waveforms should also be identical to all the previous waveforms.

(6) 19 ns High Qualifier A Setup/Hold Time Tests

These steps verify the setup and hold times of qualifier A with a 19 ns high external clock.

1. Press the TRIGGER SPEC key on the DAS. This should display the Trigger Specification menu. Toward the bottom of the menu, set the qualifier for pod 2A to Q=1.

2. Locate the probe attached to pod connector A (use the Pod ID button to check this). Attach the qualifier line of this probe to a qualifier (Q) falling edge output on the test fixture.

3. Press the "TH 0ns" button on the test fixture.

4. Press the START ACQUISITION key on the DAS. Enter the Timing Diagram menu. All acquired data should be Fs (high). Examine the data acquired on all four pods (2A, 2B, 2C, and 2D). All data acquired should be high.

5. Enter the Trigger Specification menu. Set the qualifier for pod 2A to 0.

6. Press the "TSU 29ns" button on the test fixture.

7. Press the START ACQUISITION key on the DAS. Examine the data acquired on the Timing Diagram menu. All data acquired by all four pods should be low this time.

(7) 19 ns High Qualifier B Setup/Hold Time Tests

These steps verify the setup and hold times of qualifier B with a 19 ns high external clock.

1. Enter the Trigger Specification menu. Set the qualifier for pod 2A to Q=X and the qualifier for pod 2B to Q=0.

2. Remove the qualifier line for pod 2A from the test fixture.

3. Locate the probe attached to pod connector B (use the Pod ID button to check this). Attach the qualifier line of this probe to a qualifier (Q) falling edge output on the Setup/Hold test fixture.

4. Press the "TH 0ns" button on the test fixture.

5. Press the START ACQUISITION key on the DAS. Enter the Timing Diagram menu. All acquired data should be 0s (low). Examine the data acquired on all four pods (2A, 2B, 2C, and 2D). All data acquired should be low.

6. Enter the Trigger Specification menu. Set the qualifier for pod 2B to 1.

7. Press the "TSU 29ns" button on the test fixture.

8. Press the START ACQUISITION key on the DAS. Examine the data acquired on the Trigger/Time Base. All data acquired by all four pods should be high this time.

(8) Setup for the 19 ns Low Check

The adjustments made in these steps allow the sample rate, setup, hold, and qualifiers to be checked with a non-symmetric clock that has a 19 ns low pulse in a 40 ns period.

1. Turn on the DAS mainframe, the signal generator, and the TM 500 mainframe containing the Setup/Hold Time Test Fixture.

2. Examine one of the clock outputs of the test fixture with the oscilloscope. Adjust the output of the signal generator until the test fixture clock output has a 19 ns low pulse with a 40 ns cycle time.

(9) 19 ns Low Data Setup/Hold Time Tests

These steps verify the data setup and hold times with a 19 ns low external clock.

1. Press the "TH 0ns" button on the test fixture.

2. Enter the Trigger Specification menu of the DAS. Change all qualifiers to X (don't care).

3. Press the START ACQUISITION key on the DAS. The DAS should trigger and show alternating Fs and 0s in groups A, B, and C on the State Table menu.

4. Press the TIMING DIAGRAM key on the DAS. Adjust the timing diagram to show pods 2A and 2B. Increase the magnification until the waveforms are discernable. All of the waveforms should have a 50% duty cycle and all should be in sync.

5. Adjust the timing diagram to show pods 2C and 2D. The new waveforms should be like the waveforms shown on pods 2A and 2B.

6. Press the "TSU 29ns" button on the test fixture.

7. Press the START ACQUISITION key on the DAS again. The Timing Diagram menu should update itself. The new display should show alternating Fs and 0s with a 50% duty cycle.

8. Adjust the timing diagram to show pods 2A and 2B. The new waveforms should also be identical to all the previous waveforms.

(10) 19 ns Low Qualifier A Setup/Hold Time Tests

These steps verify the setup and hold times of qualifier A with a 19 ns low external clock.

1. Press the TRIGGER SPEC key on the DAS. This should display the Trigger Specification menu. Toward the bottom of the menu, set the qualifier for pod 2A to Q=1.

2. Locate the probe attached to pod connector A (use the Pod ID button to check this). Attach the qualifier line of this probe to a qualifier (Q) falling edge output on the test fixture.

3. Press the "TH 0ns" button on the test fixture.

4. Press the START ACQUISITION key on the DAS. Enter the Timing Diagram menu. All acquired data should be Fs (high). Examine the data acquired on all four pods (2A, 2B, 2C, and 2D). All data acquired should be high.

5. Enter the Trigger Specification menu. Set the qualifier for pod 2A to 0.

6. Press the "TSU 29ns" button on the test fixture.

7. Press the START ACQUISITION key on the DAS. Examine the data acquired on the Timing Diagram menu. All data acquired by all four pods should be low this time.

(11) 19 ns Low Qualifier B Setup/Hold Time Tests

These steps verify the setup and hold times of qualifier B with a 19 ns low external clock.

1. Enter the Trigger Specification menu. Set the qualifier for pod 2A to Q=X and the qualifier for pod 2B to Q=0.

2. Remove the qualifier line for pod 2A from the test fixture.

3. Locate the probe attached to pod connector B (use the Pod ID button to check this). Attach the qualifier line of this probe to a qualifier (Q) falling edge output on the test fixture.

4. Press the "TH 0ns" button on the test fixture.

5. Press the START ACQUISITION key on the DAS. Enter the Timing Diagram menu. All acquired data should be 0s (low). Examine the data acquired on all four pods (2A, 2B, 2C, and 2D). All data acquired should be low.

6. Enter the Trigger Specification menu. Set the qualifier for pod 2B to 1.

7. Press the "TSU 29ns" button on the test fixture.

8. Press the START ACQUISITION key on the DAS. Examine the data acquired on the Trigger/ Time Base. All data acquired by all four pods should be high this time.

At this point the data and qualifier setup, hold, and sample times have been verified for the worst case external clocks. The next steps will require setting the 91A32 module up on an extender board to verify the accuracy of the threshold circuitry and the write-enable pulses.

(12) Mainframe Setup for the Remaining Tests

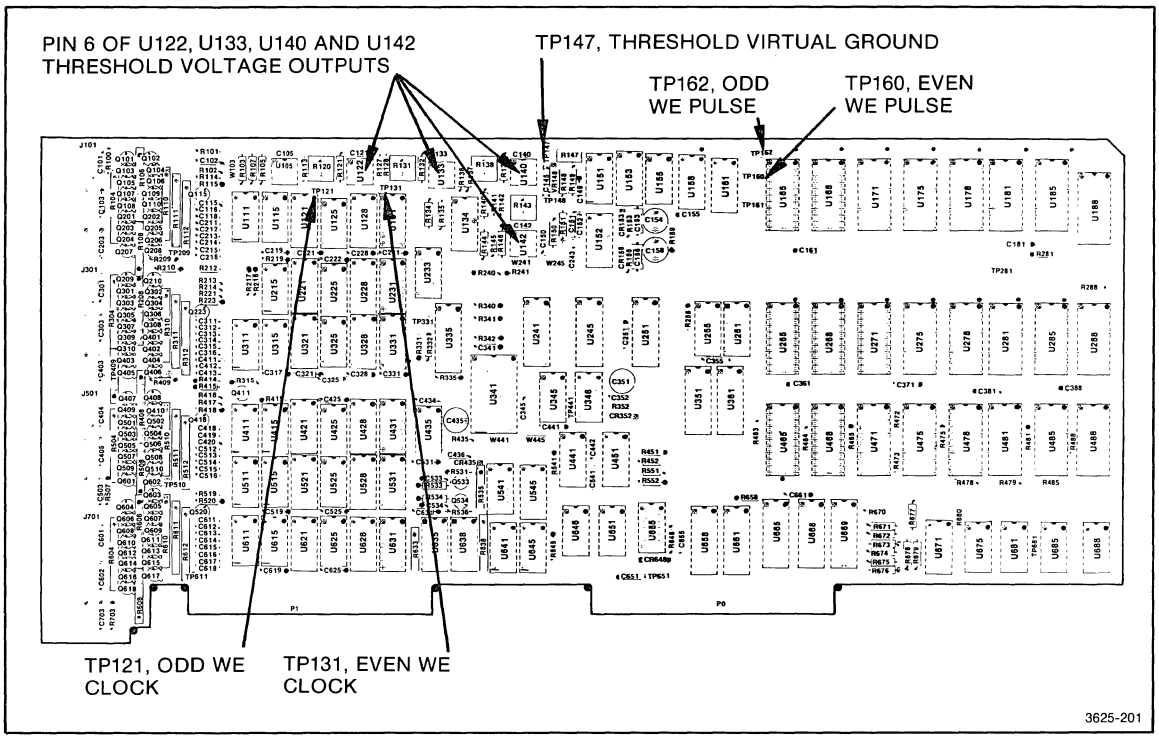


Figure 5-74. Test locations on the 91A32.

The next steps place the 91A32 on an extender board so the circuitry is accessible.

1. Turn off the DAS mainframe.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe that has power applied. Doing so will probably damage the module or sub-assembly.

2. Remove the probes from the rear edge of the 91A32 module in slot 2 and from the test fixture.

3. Remove the 91A32 module being tested from slot 2 of the DAS mainframe.

4. Install the Main Extender board from the DAS Service Maintenance Kit in slot 2 of the mainframe. Make sure the jumpers on the extender board are in the proper configuration for a 91A32 module. (See the beginning of this Verification and Adjustment Procedures section).

5. Install the 91A32 module being tested on top of the extender board.

(13) Setup for the Threshold Accuracy Check

1. Reinstall all four of the data acquisition probes in the four pod connectors at the back of the 91A32 module (do not reconnect the probes to the test fixture).

2. Verify that the recessed slide switch on the back of the probes is set to the NORM position on all four probes.

3. Turn on the DAS mainframe while holding down the STOP key to cause a power-up diagnostic failure.

4. Enter the Diagnostics menu by pressing the START SYSTEM key.

5. Select to run diagnostic tests on slot 2. Select SINGLE mode, FUNCTION 3 to run the DAC THRSH function on the 91A32.

6. Connect the ground lead of the DMM to test point TP147 of the 91A32 (see Figure 5-74).

(14) Threshold Accuracy Check

The next steps verify the accuracy of the digital-to-analog converter (DAC) in the 91A32 module. This DAC controls the threshold voltage of the data acquisition probes. These steps assume the immediately preceding test setup is completed.

1. The DAS display should still show the Diagnostics menu. Press the START SYSTEM key to start the test.

2. The cursor on the DAS screen should be in a field that reads +0.000 V. Hold the positive lead of the DMM to pin 6 of U122 on the 91A32. The DMM should now read somewhere between −0.005 V and +0.005 V. Examine the output of pins 6 of U133, U140, and U142. All of these outputs should read somewhere between −0.005 V and +0.005 V.

3. Press the SELECT key on the DAS. The menu should now show +1.600 V on the display. The DMM should read voltages somewhere between +1.579 V and +1.621 V on pins 6 of U122, U133, U140, and U142.

4. Press the SELECT key. The Diagnostics menu should now show −1.5875 V on the screen. The DMM should read somewhere between −1.609 V and −1.566 V on pins 6 of U122, U133, U140, and U142.

5. Locate the recessed slide switch on the back of each of the P6452 probes attached to the 91A32. Set all of these switches to the AUX position.

6. Press the SELECT button on the DAS twice. The Diagnostics menu should display +0.000 V. The DMM should read somewhere between −0.020 V and +0.020 V when monitoring pins 6 of U122, U133, U140, and U142.

7. Press the SELECT button, The DAC THRESHOLD SET field should read +1.600 V. With the DMM, examine the voltages present at pins 6 of U122, U133, U140, and U142. These voltages should be somewhere between +6.18 V and +6.62 V.

8. Press the SELECT key again. The DAC THRESHOLD SET field should show −1.5875 V. With the DMM, examine the voltages at pins 6 of U122, U133, U140, and U142. All the measured voltages should be between −6.56 V and −6.13 V.

(15) DAC Voltage Selectability Check

The next steps will test the ability of the DAC to select all possible threshold voltages.

1. Disconnect the DMM from the 91A32 module under test.

2. Connect a probe of the oscilloscope to pin 6 of U122. Connect the ground lead of the probe to TP147 on the 91A32 module.

3. Press SELECT on the DAS keyboard. The DAC THRESHOLD SET field should read RAMPING.

4. Adjust the oscilloscope to show a voltage ramp made of discrete steps from high to low. Examine the ramp carefully to see whether any of the bits along the stair-steps are misplaced.

5. Press the STOP key on the DAS to exit the DAC THRSH tests.

(16) Write-Enable Generator Check

The next steps verify the operation of the write-enable generators on the 91A32. This is a part of verifying the sample rate of the 91A32 module.

1. Press the TRIGGER SPEC key on the DAS keyboard. The display should show the Trigger Specification menu.

2. In the Trigger Specification menu, specify all B hexadecimal values in the TRIGGER ON field. All other triggering fields should contain X (don't care). The screen on the DAS should now look like Figure 5-75.

3. Attach the probe for channel 1 of the oscilloscope to test point TP131 on the 91A32. Attach the probe for channel 2 of the scope to TP160 (see Figure 5-74). The ground leads of the probes can be attached at any ground test point on the 91A32.

4. Set the oscilloscope to trigger off a rising edge on channel 1.

5. Turn on the oscilloscope and press the START ACQUISITION key. Adjust the oscilloscope for a display similar to that shown in Figure 5-76 (2 V/div for both channels, time base set to 10 ns/div in illustration).

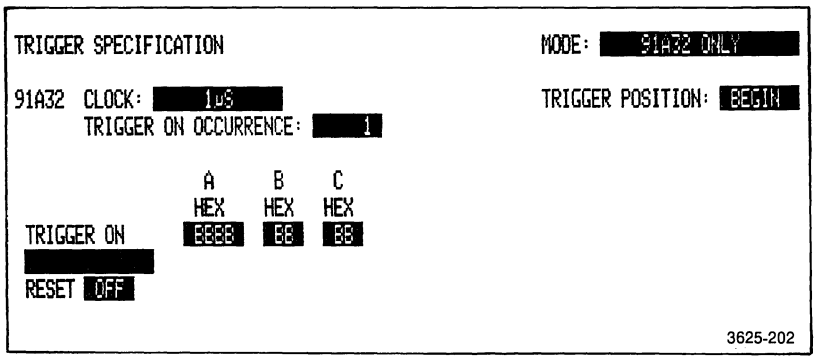


Figure 5-75. 91A32 write-enable check menu.

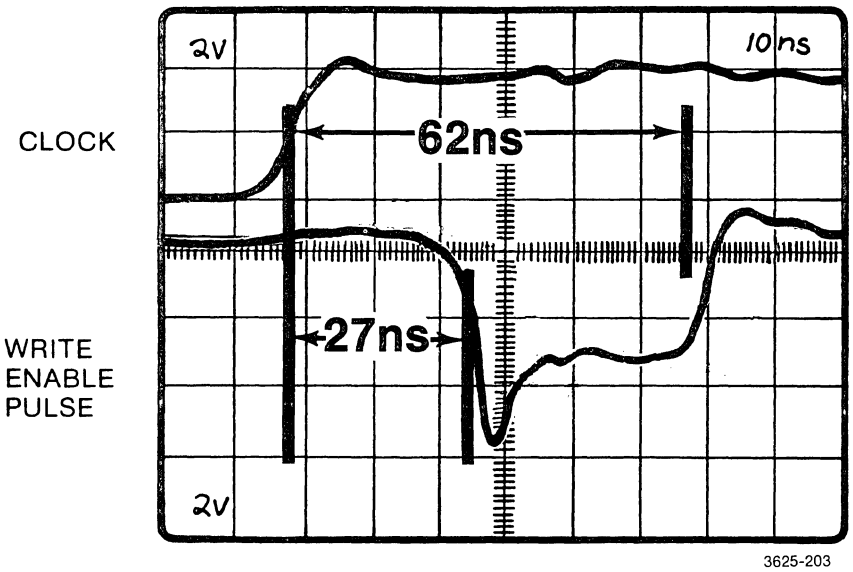


Figure 5-76. 91A32 write-enable timing.

6. The falling edge on channel 2 of the oscilloscope should be 27 ns, ±1 ns after the rising edge in channel 1 (see Figure 5-76).

7. The rising edge on channel 2 of the oscilloscope should be 62 ns, ±1 ns after the rising edge in channel 1. This verifies the operation of the even write-enable generator.

8. Move the probe for channel 1 of the oscilloscope to TP121. Move the probe for channel 2 to TP162.

9. The falling edge on channel 2 of the oscilloscope should be 27 ns, ±1 ns after the rising edge in channel 1 (see Figure 5-76).

10. The rising edge on channel 2 of the oscilloscope should be 62 ns, ±1 ns after the rising edge in channel 1. This verifies the operation of the odd write-enable generator.

This completes the 91A32 module performance check. The test setup may now be dismantled. Turn off the mainframe before removing the Main Extender board or the 91A32 module. This prevents damage to the extender board, modules, or the mainframe.

91A08 DATA ACQUISITION MODULE PERFORMANCE CHECK

To verify complete operation of the 91A08 Data Acquisition Module, the functional check for the board should be performed before attempting this performance check. You will need the following equipment to complete this performance check procedure.

- DAS mainframe
- DAS Service Maintenance Kit
- DAS Setup/Hold Time Test Fixture
- TM 500 Mainframe
- 50 Ω coaxial cable with male BNC connectors on each end
- 350 MHz, 2 channel oscilloscope
- 100 MHz pulse generator with adjustable amplitude
- 100 MHz frequency counter with 1% resolution
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy
- P6452 Data Acquisition Probe
- P6454 100 MHz Clock Probe

For instructions on use of the various menus, refer to the Operating Information section of this manual. Refer to the beginning of this Verification and Adjustment Procedures section for information on using the Main Extender board in the DAS Service Maintenance Kit.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

(1) DAS Setup/Hold Time Test Fixture Setup

These steps set up the DAS Setup/Hold Time Test Fixture so the sample rate, data setup and hold, and qualifier setup and hold times can all be verified.

1. Locate the 8-inch coaxial cable that comes with the DAS Setup/Hold Time Test Fixture. Connect this cable between the Data Delay connectors on the test fixture.

CAUTION

The DAS Setup/Hold Time Test Fixture was calibrated with the 8-inch coaxial cable that came with the fixture. The electrical length of this cable is critical to the operation of the fixture. Do not replace this cable with any other, except a cable with the same Tektronix part number.

2. Install the DAS Setup/Hold Time Test Fixture in a TM 500 mainframe according to the instructions that come with the test fixture.

3. Set up the pulse generator. Set the pulse generator to a 25 MHz output with a 50% duty cycle that is symmetrical about ground. Set the amplitude of the pulse generator to 1 V peak to peak.

4. Connect the output of the pulse generator to the CLOCK IN of the Setup/Hold Time Test Fixture with a 50 Ω coaxial cable.

(2) DAS Mainframe Setup for the Setup/Hold Time Test

The next steps set up the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe and install the 91A08 module to be tested in slot 6. This may require removing a module already occupying this space.

NOTE

For this test, the 91A08 module must be installed in slot 6. No other slot is acceptable for this performance check.

2. Remove any other 91A08 modules that may have been previously installed in the mainframe.

3. Connect the P6452 Data Acquisition Probe to the pod connector on the rear edge of the 91A08.

4. Verify that the recessed slide switch on the back of the probes is set to the NORM position on the data acquisition probe.

5. Connect the data acquisition probe to one of the four 00-FF outputs of the test fixture. (Use one of the lead sets provided with the test fixture.)

6. Install a ground lead in one of the GND SENSE connectors of the data acquisition probe. Connect the hook tip of this lead to the ground lug of the Setup/Hold Time Test Fixture.

7. Connect the P6454 100 MHz Clock Probe to the coaxial connector on the back of the 91A08 module under test (slot 6).

8. Connect the IN input of the 100 MHz Clock Probe to the rising edge clock output of the test fixture.

9. Connect the ground sense lead of the 100 MHz Clock Probe to the ground lug of the test fixture.

(3) DAS Menu Setup for the Setup/Hold Time Test

The next steps organize the DAS menus so data can easily be acquired by and read from the 91A08 module under test.

1. Turn on the DAS mainframe.

2. Press the TRIGGER SPEC key to enter the Trigger Specification menu. (See Figure 5-77.)

3. Move the screen cursor into the MODE field. Set the mode to 91A08 ONLY.

4. Move the screen cursor into the 91A08 CLOCK field. Press SELECT until external rising edge is selected.

5. Press the CHANNEL SPEC key on the DAS to enter the Channel Specification menu.

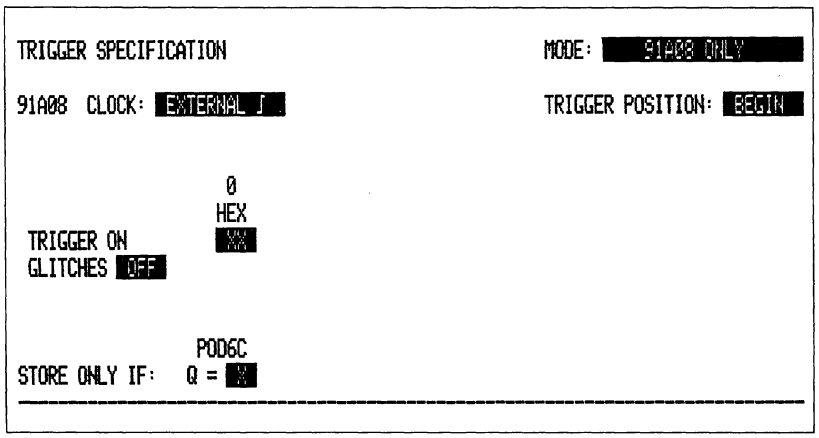
6. The screen should now show the Channel Specification menu. Under the PROBE heading locate the POD 6C field. In the THRESHOLD field for this pod there is a field that reads TTL +1.40 V. Change this field to VAR −1.30 V.

(4) Adjustments for the Data Setup/Hold Time Check

The adjustments made in these steps allow the data sample rate, setup, and hold to be checked.

1. Turn on the pulse generator and the TM 500 mainframe containing the Setup/Hold Time Test Fixture.

2. Examine one of the clock outputs of the test fixture with the oscilloscope. Adjust the output of the pulse generator until the test fixture clock output has a symmetric output with a 10 ns period.



3625-204

Figure 5-77. 91A08 setup/hold time testing trigger.

(5) Data Setup/Hold Time Tests

These steps verify the data setup and hold times at 100 MHz.

1. Press the "TH 0ns" button on the test fixture.

2. Press the START ACQUISITION key on the DAS. The DAS should trigger and show alternating Fs and 0s on the State Table menu in the group that contains the 91A08 being tested.

3. Press the TIMING DIAGRAM key on the DAS. Adjust the timing diagram to show pod 6C. Increase the magnification until the waveforms are discernable. All of the waveforms should have a 50% duty cycle and all should be in sync.

5. Press the "TSU 10ns" button on the test fixture.

6. Press the START ACQUISITION key on the DAS again. The Timing Diagram menu should update itself. The new display should show alternating Fs and 0s with a 50% duty cycle.

(6) 5 ns High Qualifier Setup/Hold Time Tests

These steps verify the setup and hold times of the qualifier with a 5 ns high external clock.

1. Examine one of the clock outputs of the test fixture with the oscilloscope.

2. Adjust the output of the pulse generator until the test fixture clock output has a 15 ns cycle time with a 5 ns low pulse.

3. Locate the probe attached to the 91A08 module. Attach the qualifier line of this probe to a qualifier (Q) falling edge output on the test fixture.

4. Press the "TH 0ns" button on the test fixture.

5. Press the TRIGGER SPEC key on the DAS. This should display the Trigger Specification menu. Toward the bottom of the menu, set the qualifier for pod 6C to Q=1.

6. Press the START ACQUISITION key on the DAS.

7. Enter the Timing Diagram menu. Examine the data acquired by the 91A08. All data acquired should be high.

8. Enter the Trigger Specification menu. Set the qualifier for pod 6C to Q=0.

9. Press the "TSU 15ns" button on the test fixture.

10. Press the START ACQUISITION key on the DAS. Examine the data acquired on the Timing Diagram menu. All data acquired by the 91A08 should be low this time.

(7) 5 ns Low Qualifier Setup/Hold Time Tests

These steps verify the setup and hold times of the qualifier with a 5 ns low external clock.

1. Examine one of the clock outputs of the test fixture with the oscilloscope.

2. Adjust the output of the pulse generator until the test fixture clock output has a 15 ns cycle time with a 5 ns low pulse.

3. Press the "TH 0ns" button on the test fixture.

4. Press the TRIGGER SPEC key on the DAS. This should display the Trigger Specification menu. Toward the bottom of the menu, set the qualifier for pod 6C to Q=1.

5. Press the START ACQUISITION key on the DAS.

6. Enter the Timing Diagram menu. Examine the data acquired by the 91A08. All data acquired should be high.

7. Enter the Trigger Specification menu. Set the qualifier for pod 6C to Q=0.

8. Press the "TSU 15ns" button on the test fixture.

9. Press the START ACQUISITION key on the DAS. Examine the data acquired on the Timing Diagram menu. All data acquired by the 91A08 should be low this time.

(8) Menu Setup for the Glitch Width Test

1. Enter the Trigger Specification menu. Set the qualifier for probe 6C to 6C=X.

2. In the Trigger Specification menu, set the 91A08 CLOCK field to internal 20 ns.

3. Set the GLITCHES field to ON. Adjacent to the GLITCHES field a field should appear that is filled with eight Xs. Change the field to contain all 1s.

4. Press the CHANNEL SPEC key on the DAS to enter the Channel Specification menu.

5. The screen should now show the Channel Specification menu. Under the PROBE heading find locate the POD 6C field. In the THRESHOLD field for this pod there is a field that reads VAR −1.30 V. Change this field to VAR 0.00 V.

(9) Glitch Width Test

The next steps verify that the 91A08 module can detect and store glitches that are 5 ns wide with 350 mV overdrive.

1. Disconnect the data acquisition and 100 MHz Clock Probes from the Setup/Hold Time Test Fixture. Disconnect the pulse generator from the test fixture.

2. Connect all of the data lines of the P6452 Data Acquisition Probe to the output of the pulse generator. Connect the GND SENSE of the probe to the ground of the pulse generator.

3. Set the pulse generator for a 20 ns cycle time with a 5 ns high pulse. Set the amplitude of the pulse to 700 mV. Center the signal around ground. The signal that the 91A08 will be capturing should be similar to Figure 5-78.

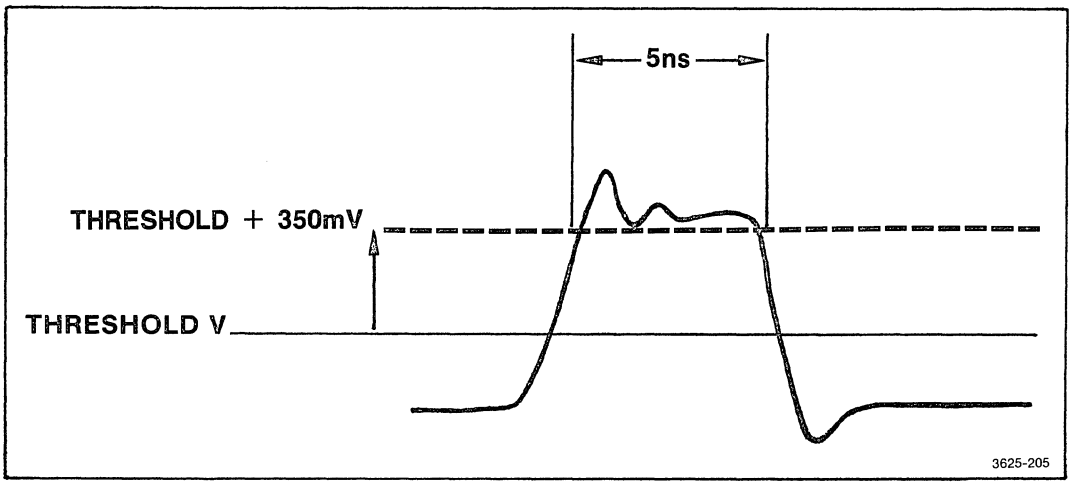


Figure 5-78. Glitch width and height restrictions.

4. Press the START SYSTEM key. The DAS should trigger.

5. Enter the Timing Diagram menu. Set the GLITCH field to ON.

6. Depending on the location of the pulse relative to the internal clock, each pulse can be detected as either a glitch or a data 1. Scan each line of data acquired by pod 6C for glitch symbols. If there are glitch symbols on each line, then the 91A08 module is detecting glitches properly.

(10) Mainframe Setup for the Remaining Tests

To examine the accuracy of the threshold circuits, the internal clock, and the write-enable pulses, the 91A08 module must be placed on an extender board.

1. Turn off the DAS mainframe.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

2. Disconnect the data acquisition and 100 MHz Clock Probes from the rear of the 91A08 module under test.
3. Remove the 91A08 module from the mainframe.
4. Set the jumpers of the Main Extender board from the DAS Service Maintenance Kit to accept a 91A08 module. Install the extender board in slot 6 on the DAS mainframe.
5. Install the 91A08 module on top of the extender board.
6. Reconnect the data acquisition probe to pod connector C at the back of the 91A08 module.

(11) Setup for the Threshold Accuracy Check

1. Verify that the recessed slide switch on the back of the data acquisition probe is set to the NORM position.
2. Turn on the DAS mainframe while holding down the STOP key to cause a power-up diagnostic failure.
3. Enter the Diagnostics menu by pressing the START SYSTEM key.
4. Select to run diagnostic tests on slot 6. Select SINGLE mode, FUNCTION 5 to run the DAC THRSH function on the 91A08.
5. Connect the DMM ground lead of the DMM to test point TP106 of the 91A08 (see Figure 5-79).

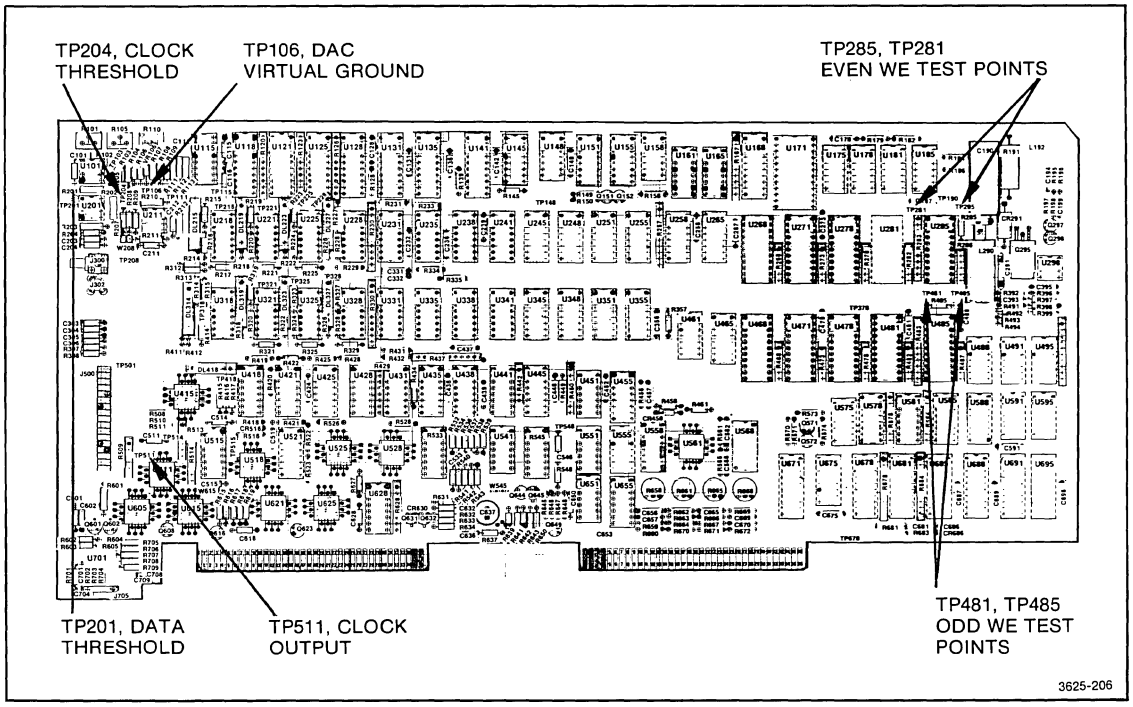


Figure 5-79. Test locations on the 91A08.

(12) Threshold Accuracy Check

The next steps verify the accuracy of the digital-to-analog converter (DAC) in the 91A32 module. This DAC controls the threshold voltage of the data acquisition probe and the 100 MHz Clock Probe. These steps assume the immediately preceding test setup is completed.

1. The DAS display should still show the Diagnostics menu. Press START SYSTEM to start the test.

2. The cursor should be in the field that reads +0.000 V.

3. Hold the positive lead of the DMM to test point TP201 on the 91A08. The DMM should now read somewhere between −0.005 V and +0.005 V.

4. Press the SELECT key on the DAS. The menu should now show +1.600 V on the display. The DMM should read voltages somewhere between +1.579 V and +1.621 V on test point TP201.

5. Press the SELECT key. The Diagnostics menu should now show −1.5875 V on the screen. The DMM should read somewhere between −1.609 V and −1.566 V on test point TP201.

6. Locate the recessed slide switch on the back of the P6452 probe attached to the 91A08. Set this switch to the AUX position.

7. Press the SELECT button on the DAS twice. The Diagnostics menu should display +0.000V. The DMM should read somewhere between −0.020 V and +0.020 V at test point TP201.

8. Press the SELECT button, The DAC THRESHOLD SET field should read +1.600 V. With the DMM, examine the voltage present at test point TP201. This voltage should be somewhere between +6.18 V and +6.62 V.

9. Press the SELECT key again. The DAC THRESHOLD SET field should show −1.5875 V. With the DMM, examine the voltage at test point TP201. The voltage should be between −6.56 V and −6.13 V.

(13) DAC Voltage Selectability Check

The ability of the DAC to select all possible threshold voltages is now tested.

1. Disconnect the DMM from the 91A08 module under test.

2. Connect a probe of the oscilloscope to TP201 on the 91A08 module. Connect the ground lead of the probe to TP106.

3. Press SELECT on the DAS keyboard. The DAC THRESHOLD SET field should read RAMPING.

4. Adjust the oscilloscope to show a voltage ramp made of discrete steps from high to low. Examine the ramp carefully to see whether one or more of the bits along the stair-steps are misplaced.

(14) Write-Enable Generator Check

The next steps verify the operation of the write-enable generators on the 91A08. This is a part of verifying the sample rate of the 91A08 module.

1. Press the TRIGGER SPEC key on the DAS keyboard. The display should show the Trigger Specification menu.

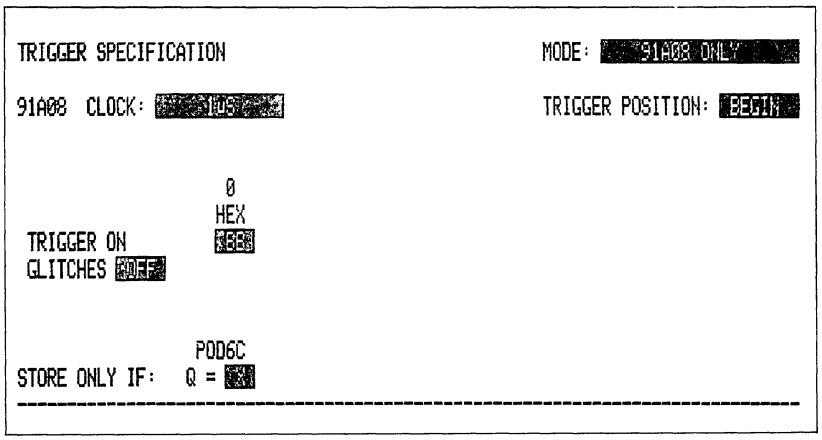
2. In the Trigger Specification menu, enter the MODE field. Adjust this field to 91A08 ONLY. Specify all B hexadecimal values in the TRIGGER ON field. Set the GLITCHES field to OFF. The screen on the DAS should now look like Figure 5-80.

3. Attach the probe for channel 1 of the oscilloscope to test point EA0 (TP281) on the 91A08. Attach the probe for channel 2 of the oscilloscope to test point EWE (TP285) (see Figure 5-79). The ground leads of the probes can be attached at any ground test point on the 91A08.

4. Set the oscilloscope to trigger off a rising edge on channel 1.

5. Turn on the oscilloscope and press the START ACQUISITION key. Adjust the oscilloscope for a display similar to that shown in Figure 5-81 (0.5 V/div for both channels, time base set to 5 ns/div in illustration).

6. The falling edge on channel 2 of the oscilloscope should be 4 ns, ±0.5 ns after the rising edge in channel 1 (see Figure 5-81).



3625-207

Figure 5-80. 91A08 write-enable check menu.

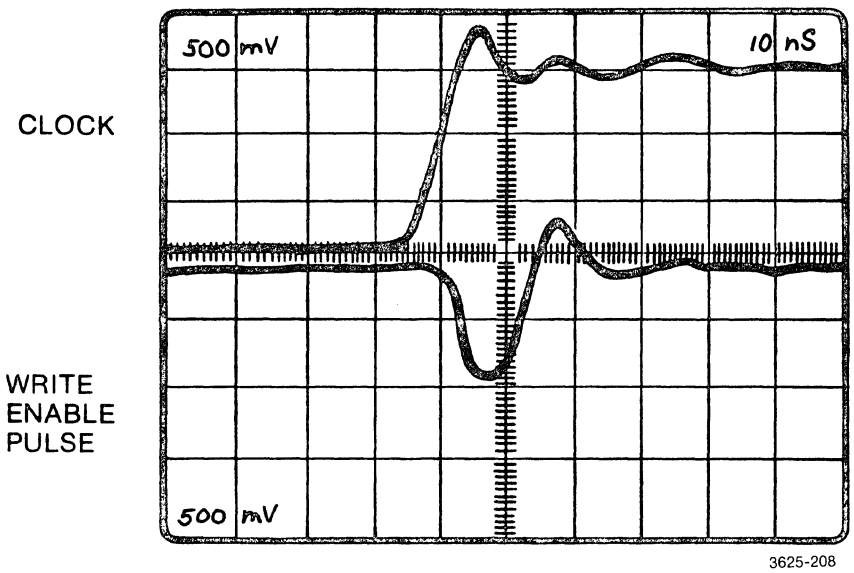


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Figure 5-81. 91A08 write-enable timing.

7. The rising edge on channel 2 of the oscilloscope should be 13 ns, ±0.5 ns after the rising edge in channel 1. This verifies the operation of the even write-enable generator.

8. Move the probe for channel 1 of the oscilloscope to OA0 (TP481). Move the probe for channel 2 to OWE (TP485). The ground leads of the oscilloscope probes may need to be reconnected to new ground points on the 91A08 module.

9. The falling edge on channel 2 of the oscilloscope should be 4 ns, ±0.5 ns after the rising edge in channel 1 (see Figure 5-81).

10. The rising edge on channel 2 of the oscilloscope should be 13 ns, ±0.5 ns after the rising edge in channel 1. This verifies the operation of the odd write-enable generator.

11. Press the STOP key to end the write-enable test.

(15) Internal Clock Check

The next steps verify the accuracy of the internal clock provided by the Trigger/Time Base.

NOTE

The internal clock for the 91A08 module is a function of the Trigger/Time Base board. Problems with the 91A08 internal clock can probably be traced back to the Trigger/Time Base.

1. Press the TRIGGER SPEC key on the DAS. The display should show the Trigger Specification menu.

2. Move the cursor on the DAS screen into the 91A08 CLOCK field. Press the SELECT button until the field reads 1 μs. Then press the DECR button and hold it down. The field should decrement until it shows 10 ns.

3. Connect the frequency counter to TP511 on the 91A08 board. Press the START ACQUISITION key on the DAS keyboard.

4. The frequency counter should read 100 MHz, ±1%.

5. Press STOP then TRIGGER SPEC to return to the Trigger Specification menu. Adjust the 91A08 CLOCK field to 20 ns. Press the START ACQUISITION key on the DAS keyboard.

6. The frequency counter should read 50 MHz, ±1%.

This completes the 91A08 module performance check. The test setup may now be dismantled. Turn off the mainframe before removing the Main Extender board or the 91A08 module. This prevents damage to the extender board, modules, or the mainframe.

91P16 AND 91P32 PATTERN GENERATOR MODULES PERFORMANCE CHECK

This procedure checks the performance of any set of 91P16 and 91P32 modules. Any valid combination of pattern generator modules from an individual 91P16 module, through a combination of one 91P16 and two 91P32 modules, may be checked with this performance check procedure. All 91P16 and 91P32 modules operate as a system, so they must be tested as a system.

To verify complete operation of the 91P16 and/or 91P32 Pattern Generator modules, the functional check for those modules should be performed before attempting this performance check. You will need the following equipment to complete this performance check procedure:

- DAS mainframe
- 91A08 Data Acquisition Module
- P6452 Data Acquisition Probe
- P6454 100 MHz Clock Probe
- 350 MHz, 2 channel oscilloscope
- 100 MHz pulse generator with adjustable amplitude
- 5 V, 2 A power supply
- 100 μF, 10 V aluminum electrolytic capacitor
- Enough P6455 TTL/MOS Pattern Generator Probes to plug into all probe connectors of the modules being tested
- As many 1 μF ceramic capacitors as there are pattern generator probes
- Graph paper
- Ruler or straight edge

and, if a 91P16 Pattern Generator Module is not being tested,

- 91P16 Pattern Generator Module
- Two P6455 TTL/MOS Pattern Generator Probes

For instructions on use of the various menus, refer to the Operating Information section of this manual.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

(1) DAS Mainframe Setup

The next steps set up the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Remove any 91P16 or 91P32 modules that may have previously been installed in the mainframe.
3. Assemble the module or modules to be tested. Install these modules in the mainframe according to Table 5-5.

NOTE

For the purposes of this performance check, the pattern generator modules must be installed according to Table 5-5. The modules are installed in this manner to obtain worst case skew. If Table 5-5 is not followed, the performance check may yield incorrect results.

Table 5-5
91P16 AND 91P32 Performance Check Mainframe Setup

Module(s) Being Tested	Mainframe Setup
One 91P16 only	Install the 91P16 in slot 1
One 91P32 only	Install the 91P32 in slot 5
Two 91P32 modules	Install the 91P32 modules in slots 4 and 5
One 91P16 and One 91P32	Install the 91P16 in slot 1 and the 91P32 in slot 5
One 91P16 and Two 91P32s	Install the 91P16 in slot 1 and the 91P32 modules in slots 4 and 5

4. If a 91P16 module is not being checked, install the extra 91P16 module in slot 1. A 91P16 module is required for this procedure because 91P32 modules are slaves to the 91P16.
5. Install the 91A08 module in slot 6 of the mainframe.
6. Turn on the DAS mainframe.

(2) DAS Probe Setup

The next steps connect the P6455 TTL/MOS Pattern Generator Probes to the DAS and to a +5 V power supply. The probes are also decoupled from variations in the supply.

1. Set the recessed slide switch on the back of all the P6455 TTL/MOS Pattern Generator Probes to NORM.

2. Connect P6455 TTL/MOS Pattern Generator Probes to the pod connectors of all 91P16 and 91P32 modules in the DAS mainframe.

3. Connect a 2 foot (0.6 meter) wire to the +5 V output of the power supply. Connect a 2 foot (0.6 meter) wire to the ground of the power supply. At the end of these two wires connect the 100 μF electrolytic capacitor.

Carefully observe the polarity of the electrolytic capacitor. Connecting the capacitor backwards may cause it to explode.

3. Connect the V_L lines of all the TTL/MOS Pattern Generator Probes to the 2 foot wire attached to the ground output of the +5 V, 2 A power supply.

4. Connect the V_H lines of all the TTL/MOS Pattern Generator Probes to the 2 foot wire attached to the +5 V output of the +5 V, 2 A power supply.

5. Connect one 1 μF ceramic capacitor across the V_H and V_L inputs to each probe. The best and easiest way to connect these capacitors is to hook one end of each ceramic capacitor under the hook tip that connects the probe to the +5 V source. Place the other end of each ceramic capacitor under a hook tip that connects to the ground wire.

6. After connecting all ceramic capacitors, check to make sure that all connections to +5 and ground remain secure.

7. Install lead sets in all of the above probes.

(3) Menu Setup

This menu setup is sufficient for the data skew tests.

1. Enter the Pattern Generator menu.

2. In the Pattern Generator Program menu enter the program shown below.

SEQ	LABEL	HEX	HEX	HEX	HEX	HEX	INSTRUCTIONS		STROBES
0	TEST	0000	0000	0000	0000	0000			
1		FFFF	FFFF	FFFF	FFFF	FFFF	GOTO	TEST	0123456789

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If less than a full configuration is being tested, then the fields under HEX show fewer available positions. Fill all available positions with the appropriate hexadecimal digits.

3. Set the pattern generator clock to internal 40 ns.

4. Press the START PAT GEN key on the DAS.

(4) Graph Organization

The data channel skew and the data-clock timing are verified graphically. The suggested layout for this graph is given next. Refer to Figure 5-82 while laying out the graph paper.

1. Allow ten lines down the graph paper for each pattern generator pod used (from 2 to 10 pods may be used). Allow enough width in each line to write legibly.

2. Across the top of the graph paper, number by 1s from −5 ns to +15 ns, allowing edge at the margins for writing comments. The distance between each number should be uniform. This will be the time axis.

3. List all of the used pattern generator pod connectors down the side of the graph paper followed by the word "CLK". These lines will be used to check the skew between output clock lines.

4. Write "POD 1B" on the next line down. Below where POD 1B is written, write the numbers 0 through 7, one number on each line. These lines will correspond to the data lines of pod 1B.

5. List all other pattern generator probe identifiers down the side of the page followed by the numbers 0 through 7. In this way each separate probe data line is listed on a line of the graph paper.

6. Your graph paper should now have the same basic layout as the graph layout shown in Figure 5-82.

(5) Data for the Clock Skew Verification

NOTE

The skew between clock outputs of the pattern generator modules is not a performance requirement. This information is necessary, however, to find the worst case of data-clock timing.

1. With any convienient high speed pulse (the output of the pattern generator may be used) examine the timing skew between the horizontal inputs of the oscilloscope. The skew should be less than 0.5 ns for the measurements taken in these procedures.

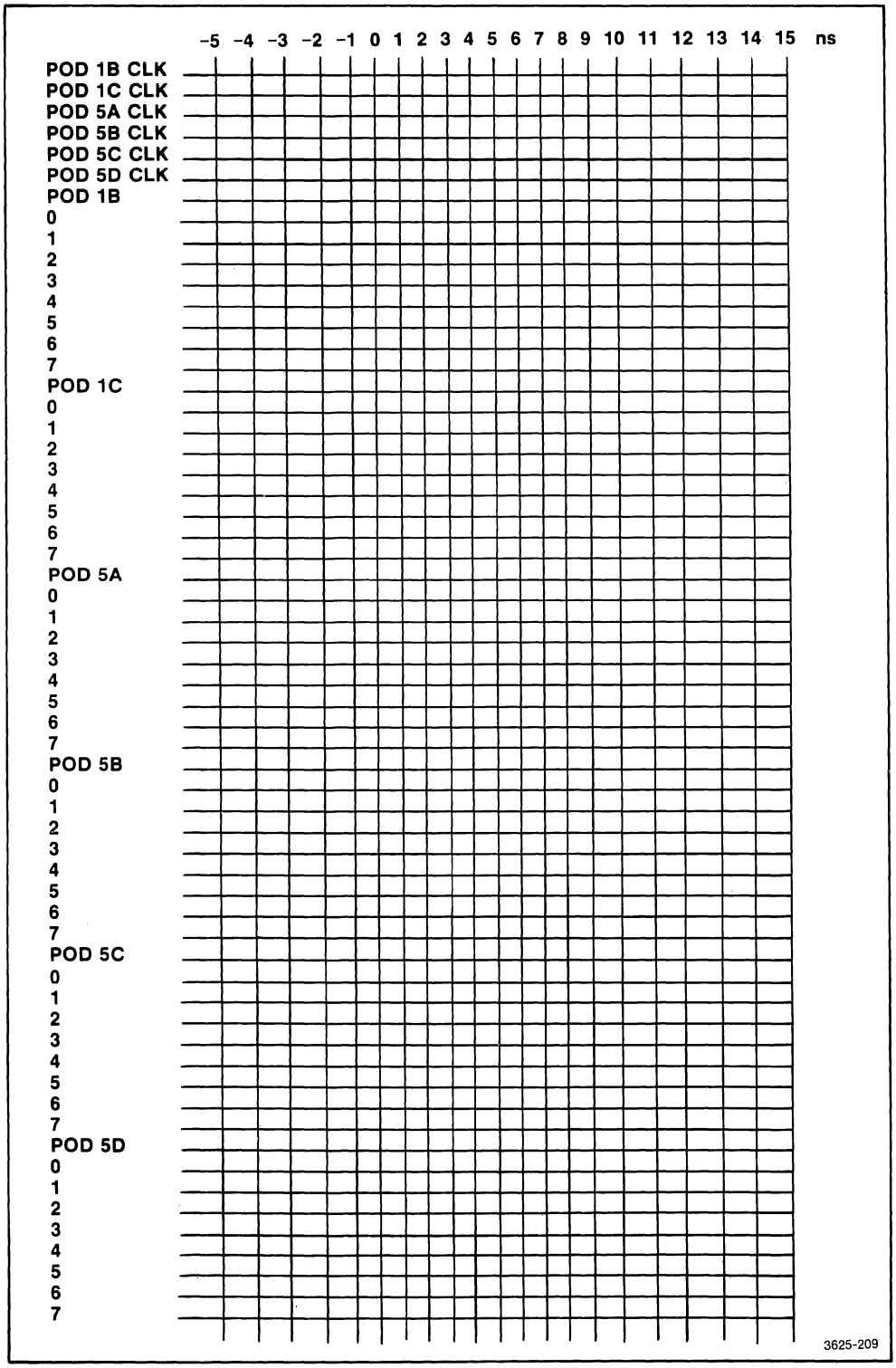

Figure 5-82. Graph layout for the pattern generator skew test.

2. Connect the probe for channel 1 of the oscilloscope to the clock output of the probe attached to pod connector 1B. This clock output will be referred to as the master clock for the duration of this procedure.
3. Connect the probe for channel 2 of the oscilloscope to the clock output of the probe attached to pod connector 1C.
4. Attach the ground leads of the two oscilloscope probes to the ground output of the 5 V, 2 A power supply.
5. If the +5 V power supply and the oscilloscope have not yet been turned on, do so now.
6. Set the oscilloscope to 2 ns/div and 2 V/div. Trigger off a rising edge on channel 2.
7. Examine the traces on the oscilloscope. Count out the time difference (skew) between the two clock signals.
8. Put a dot at the 0 ns position on the line that reads POD 1B CLK.
9. On the line of the graph paper that says POD 1C CLK, put a dot that corresponds to the skew between the two oscilloscope channels. If channel 2 has a rising edge before channel 1, put the skew time for POD 1C CLK on the negative side of the time axis. If channel 2 has a rising edge after channel 1, then put the skew time on the positive side of the time axis.
10. Move the oscilloscope probe for channel 2 from the clock line of the probe attached to pod connector 1C to the next clock line in the list on the graph. Repeat steps 6, 7, and 8, above for this probe clock line. Continue until all clock lines of all probes have been assigned skew times.
11. Your clock skew data should have a format similar to the data shown in Figure 5-83.

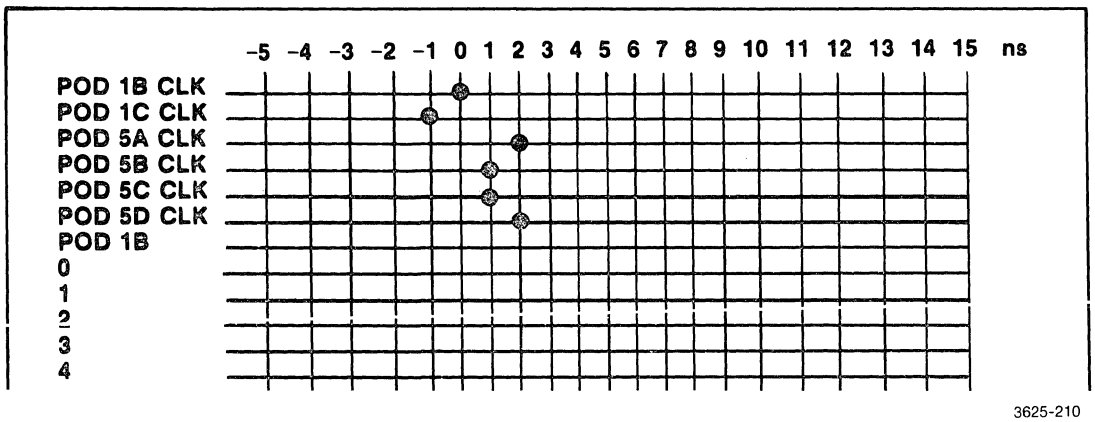

Figure 5-83. Example of clock skew data format.

(6) Data-Clock Timing Verification

The next steps involve finding and recording the amount of time after a rising edge from the master clock the pattern generator data changes from low to high.

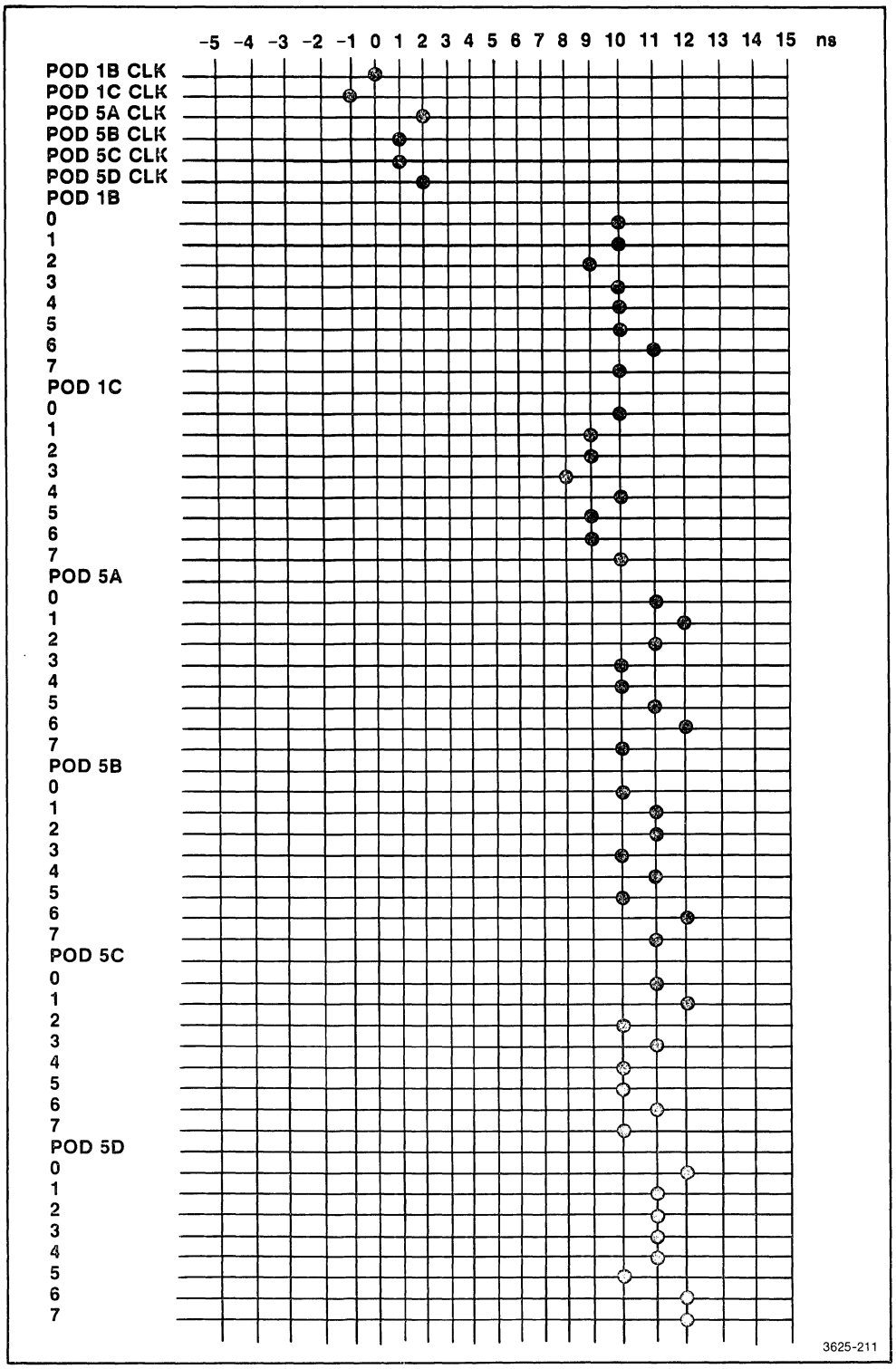

Figure 5-84. Example of data-clock timing format.

1. Connect the probe for channel 2 of the oscilloscope to the 0 data line of the probe connected to pod connector 1B.

2. The rising edge in channel 2 of the oscilloscope should happen between 2 and 15 ns after the rising edge in the clock. Count out the actual time difference between the rising edges.

3. On the line of the graph paper that says 0 under POD 1B, put a dot that corresponds to the time difference between the two rising edges. Channel 2 of the oscilloscope should show a rising edge 2 to 15 ns after the clock, so the dot for POD 1B 0 should be on the positive side of the time axis.

4. Use channel 2 of the oscilloscope to examine the data 1 through data 7 lines of probe 1B. Record the difference between the clock and the data rising edges for each of the data lines. The data record should now be formatted like Figure 5-84.

5. Continue to examine the data channels for each pattern generator probe. Record the time difference between the rising edges for all data channels on the appropriate line of the graph paper.

(7) Calculations for the Data Channel Skew Verification

The next steps tell whether the data skew between pattern generator channels is within specifications. Figure 5-85 is an example of data-clock timing and data skew calculations.

1. Locate the data channel with the rising edge the soonest after the master clock rising edge. This should be the data channel with the dot closest to the 0 ns axis of the graph paper. Circle this dot.

2. Draw a vertical line parallel to the 0 ns axis that goes through the dot just circled.

3. Locate the data channel with the rising edge the furthest from the master clock rising edge. This should be the data channel with the dot furthest from the 0 ns axis of the graph paper. Circle this dot.

4. Draw a vertical line parallel to the 0 ns axis that goes through the dot just circled.

5. Count out the number of nanoseconds between the two lines that were just drawn. This number should be 10 ns or less to satisfy the required specifications. The distance between the two lines represents the skew between the various data channels.

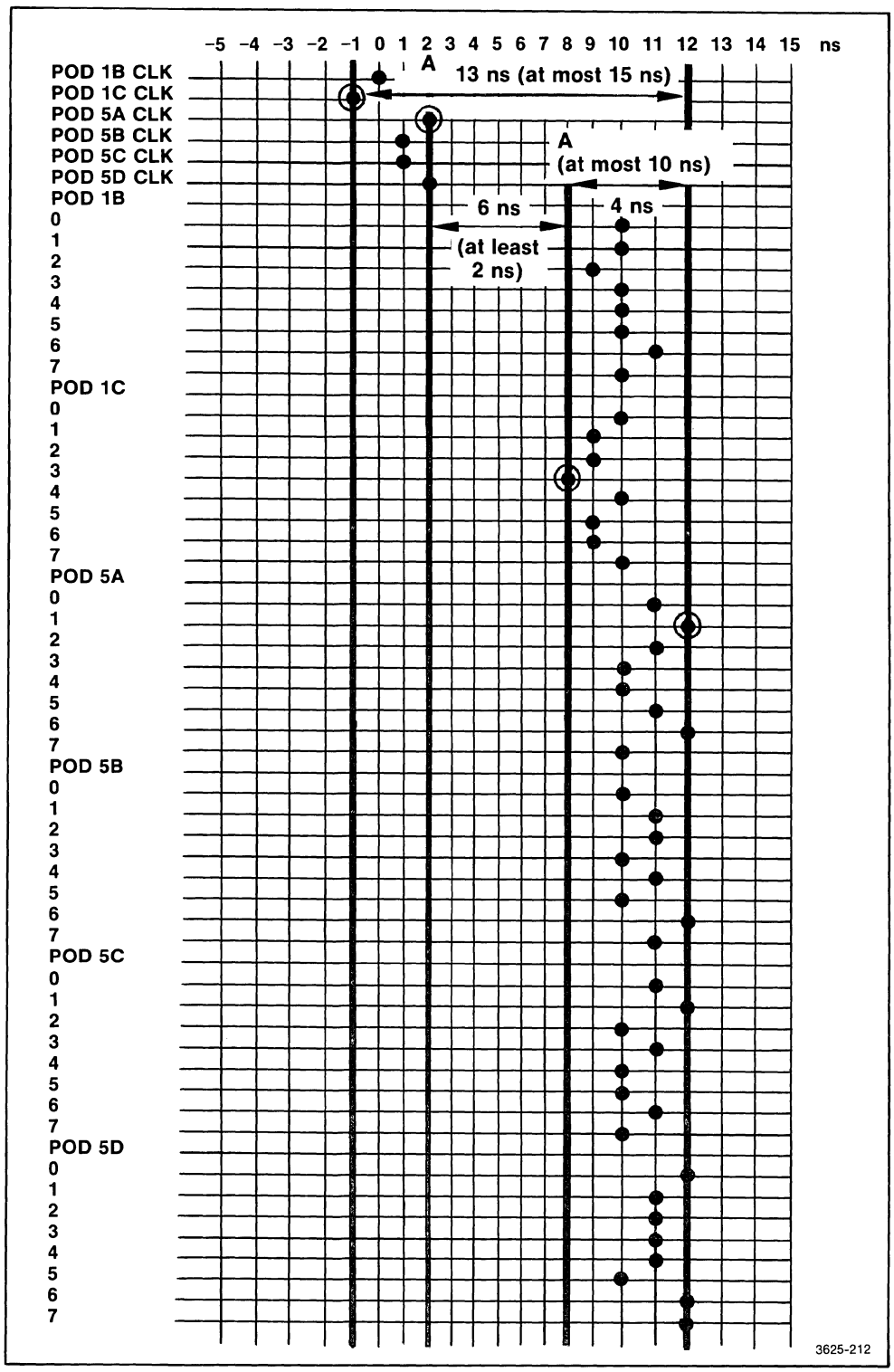

Figure 5-85. Example of data-clock timing and data skew calculations.

(8) Calculations for the Data-Clock Timing Verification

The next steps tell whether the data-clock timing of the pattern generator modules is within specification.

1. Locate the clock channel with the rising edge the latest after the master clock rising edge. This is the clock channel with the dot furthest into the positive side of the time axis. Circle this dot. If there are no clock edges after the master clock, then circle the master clock dot.

2. Draw a vertical line parallel to the 0 ns axis that goes through the dot just circled.

3. Locate the clock channel with the rising edge most previous to the master clock rising edge. This is the clock channel with the dot furthest into the negative side of the time axis. Circle this dot. If there are no clock edges prior to the master clock, then circle the master clock dot.

4. Draw a vertical line parallel to the 0 ns axis that goes through the dot just circled.

5. Locate the line that corresponds to the most positive clock edge. Put some distinguishing mark at the top of this line.

6. Locate the line that corresponds to the data transition closest to the clock edges (drawn when calculating the data channel skew). Put the same distinguishing mark at the top of this line.

7. Count out the number of nanoseconds between the two lines that were just identified. The line for the data should be at least 2 ns after the line for the clock edge. If these lines are less than 2 ns apart, then the pattern generator modules are out of specification.

8. Locate the clock line and the data line that are the farthest away from each other. Count the number of nanoseconds between these two lines. These two lines should be less than 15 ns apart. If these lines are more than 15 ns apart, then the pattern generator modules are out of specification.

(9) First Strobe Delay Verification

This procedure checks the strobe delay accuracy. It assumes that all the previous steps have been performed so the probes and oscilloscope are properly set up.

1. Enter the Pattern Generator Program menu. Set the pattern generator clock to 100 ns.

2. Press the START PAT GEN key.

3. Connect the probe for channel 2 of the oscilloscope to the STRB (strobe) output of the probe attached to pod connector 1B.

4. Adjust the oscilloscope so the rising edges of both channel 1 and channel 2 can be seen.

5. Measure the time after channel 1 (the clock) has a rising edge that channel 2 (the strobe) has a rising edge. This time must fall between 57 ns and 83 ns.

6. Move the probe for oscilloscope channel 2 to the next strobe line. The difference between the rising edges should again fall between 57 ns and 83 ns.

7. Continue to move the probe for oscilloscope channel 2 from strobe line to strobe line until all strobe delay times have been checked. The difference in rise times must always fall between 57 ns and 83 ns.

(10) First Strobe Width Verification

This procedure checks the strobe width accuracy.

1. Adjust the oscilloscope so both the rising and falling edges of the waveform in channel 2 can be seen.

2. Measure the time between the rising and falling edge in channel 2. This time must fall between 30 ns and 50 ns.

3. Move the probe for oscilloscope channel 2 to each strobe line. For each strobe line measure the time between the rising and falling edge in channel 2. This time must always fall between 30 ns and 50 ns.

(11) Second Strobe Delay Verification

These steps finish verifying the accuracy of the strobe delay.

1. Enter the Pattern Generator Program menu. Set the pattern generator clock for 50 μs.

2. Enter the Pattern Generator Timing menu. Set the strobe delay to 40.910 μs for all listed strobes. Leave the width values for all strobes at 40 ns.

3. Press the START PAT GEN key.

4. Adjust the oscilloscope so the rising edges of both channel 1 and channel 2 can be seen. The rising edge for channel 2 will be a very narrow spike.

5. Measure the time difference between the rising edge in channel 1 (the clock) and the rising edge in channel 2 (the strobe). This time must fall between 36.5 μs and 45.0 μs.

6. Move the probe for oscilloscope channel 2 to the next strobe line. The difference between the rising edges should again fall between 36.5 μs and 45.0 μs.

7. Continue to move the probe for oscilloscope channel 2 from one strobe line to the next until all strobe delay times have been checked. The difference in rise times must always fall between 36.5 μs and 45.0 μs.

(12) Second Strobe Width Verification

These steps finish verifying the accuracy of the strobe width.

1. Enter the Pattern Generator Timing menu. Set the strobe delay to 70 ns for all listed strobes. Set the width values for all strobes at 40.880 μs.

2. Press the START PAT GEN key.

3. Adjust the oscilloscope so both the rising and falling edges of the waveform in channel 2 can be seen.

4. Measure the time between the rising and falling edge in channel 2. This time must fall between 36.5 μs and 45.0 μs.

5. Move the probe for oscilloscope channel 2 to each strobe line. For each strobe line, measure the time between the rising and falling edge in channel 2. This time must always fall between 36.5 μs and 45.0 μs.

(13) Mainframe Setup for External Clock Verification

The next steps set up the DAS mainframe for the last performance checks on the 91P16 and 91P32 modules.

1. Turn on the pulse generator.

2. Connect the P6452 External Clock probe to pod connector C on the back of the Trigger/Time Base module (slot 7).

3. Connect the PG CLK line of the external clock probe to the output of the pulse generator. Connect the ground sense line of the external clock probe to the ground output of the pulse generator.

4. Set the pulse generator to a 40 ns cycle time with a 19 ns high pulse. Set the pulse generator to swing between ground and +2.5 V. Verify these settings with the oscilloscope.

5. Connect the P6452 Data Acquisition Probe to pod connector 6A (the 91A08 module).

6. Verify that the recessed slide switchs on the back of the external clock probe and the data acquisition probe are set to the NORM position.

7. Use the Diagnostic Lead Set to connect the P6452 Data Acquisition Probe to the P6455 TTL/MOS Pattern Generator Probe in pod connector 1B.

NOTE

In this special instance, the Diagnostic Lead Set can be expected to operate at 25 MHz.

8. Connect the P6454 100 MHz Clock Probe to the coaxial connector on the back of the 91A08 module in slot 6.

9. Install a ground lead in one of the GND SENSE connectors of the P6452 Data Acquisition Probe.

10. Connect the REF lead of the P6454 100 MHz Clock Probe to the ground lead hanging from the P6452 Data Acquisition Probe. Connect the IN lead of the P6454 probe to the clock line out of the pattern generator probe (the gray flying lead on the pattern generator side of the diagnostic lead set).

(14) 19 ns High External Clock Verification

This setup organizes the menus for the External Clock Verification.

1. Enter the Pattern Generator Program menu. Adjust the program to look like the following listing.

SEQ	LABEL	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	INSTRUCTIONS	STROBES
0		XXXX	XXXX	XXXX	XXXX	XXXX	GOTO 200	
200	200	0000	0000	0000	0000	0000		
201		0101	0101	0101	0101	0101		
202		0202	0202	0202	0202	0202		
203		0404	0404	0404	0404	0404		
204		0808	0808	0808	0808	0808		
205		1010	1010	1010	1010	1010		
206		2020	2020	2020	2020	2020		
207		4040	4040	4040	4040	4040		
208		8080	8080	8080	8080	8080		
209		FFFF	FFFF	FFFF	FFFF	FFFF	GOTO 200	

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2. Set the pattern generator clock to external rising edge. Leave the clock threshold set to TTL.

3. Enter the Trigger Specification menu. Set the MODE field to 91A08 ONLY. Set the 91A08 CLOCK field to external rising edge. The acquisition trigger should be set to Xs (don't care).

4. Press the START SYSTEM key.

5. Enter the Timing Diagram menu. Adjust the menu to display data acquired by pod 6A. The data acquired by pod 6A should look like Figure 5-86.

6. Scan all of the acquired data for this ramp pattern. There should be no dropped bits or unevenness in the pattern.

7. Remove the pattern generator probe from the lead set. If there is a 91P32 module in slot 5, then connect the pattern generator probe from pod connector 5A to the lead set.

8. Press the START ACQUISITION key.

9. The data acquired should again look like Figure 5-86. Scan all of the acquired data for the ramp pattern. There should be no dropped bits or unevenness in the pattern.

10. Remove the pattern generator probe from the lead set. If there is a 91P32 module in slot 4, then connect the pattern generator probe from pod connector 4A to the lead set.

11. Press the START ACQUISITION key.

12. The data acquired should again look like Figure 5-86. Scan all of the acquired data for the ramp pattern. There should be no dropped bits or unevenness in the pattern.

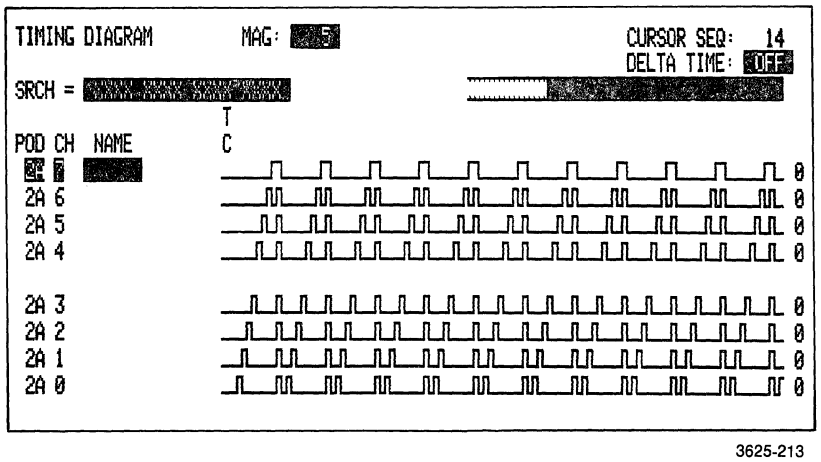

Figure 5-86. Data acquired from the pattern generator.

(15) 19 ns Low External Clock Verification

1. Set the pulse generator to a 40 ns cycle time with a 19 ns low pulse. Set the pulse generator to swing between ground and +2.5 V. Verify these settings with the oscilloscope.

2. Remove the lead set from the pattern generator probe. Connect the pattern generator probe from pod connector 1A to the lead set.

3. Press the START SYSTEM key.

4. Enter the Timing Diagram menu. The display should still show the data acquired by pod 6C. The data acquired should look like Figure 5-86. Scan all of the acquired data for the ramp pattern. There should be no dropped bits or unevenness in the pattern.

5. Remove the lead set from the pattern generator probe. If there is a 91P32 module in slot 5, then connect the pattern generator probe from pod connector 5A to the lead set.

6. Press the START ACQUISITION key.

7. The data acquired should again look like Figure 5-86. Scan all of the acquired data for the ramp pattern. There should be no dropped bits or unevenness in the pattern.

8. Remove the lead set from the pattern generator probe. If there is a 91P32 module in slot 4, then connect the pattern generator probe from pod connector 4A to the lead set.

9. Press the START ACQUISITION key.

10. The data acquired should again look like Figure 5-86. Scan all of the acquired data for the ramp pattern. There should be no dropped bits or unevenness in the pattern.

This completes the 91P16 and 91P32 module performance check. The test setup may now be dismantled. Turn off the DAS mainframe before removing any instrument modules. This prevents damage to the modules or the mainframe.

P6452 DATA ACQUISITION OR EXTERNAL CLOCK PROBE PERFORMANCE CHECK

To verify complete operation of the P6452 probe, the functional check for the probe should be performed before attempting this performance check.You will need the following equipment to complete this performance check procedure:

- DAS mainframe
- DAS Service Maintenance Kit
- 350 MHz, 2 channel oscilloscope
- 100 MHz pulse generator with adjustable amplitude
- Variable dc power supply
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy

and either of the following

- 91A32 Data Acquisition Module

or

- 91A08 Data Acquisition Module

For instructions on use of the various menus, refer to the Operating Information section of this manual. Refer to the beginning of this Verification and Adjustment Procedures section for information on using the Main Extender board in the DAS Service Maintenance Kit.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

(1) Mainframe Setup

The next steps set up the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Install the Main Extender board in any of slots 1 through 6 of the DAS mainframe. Make sure the jumpers on the extender board are set to accept an acquisition module.
3. Install the data acquisition module on top of the extender board. The acquisition module may be either a 91A32 or a 91A08 module.
4. Connect the P6452 probe to one of the pod connectors on the rear edge of the acquisition modules.
5. Verify that the recessed slide switch on the back of the P6452 Data Acquisition Probe is set to the AUX position.
6. Turn on the DAS mainframe.

(2) Rise and Fall Time Check

1. Turn on the pulse generator. Set the pulse generator to output a 10 ns square wave. Set the square wave levels to 2.5 V high and ground low. Verify these settings with the oscilloscope. Also verify that the square wave has a 50% duty cycle.
2. Connect all of the inputs of the P6452 probe to the pulse generator output with a high-speed flying lead set.
3. Connect a ground sense lead from the P6452 probe to the ground of the pulse generator.
4. With one channel of the oscilloscope, examine each output signal from the probe for rise and fall time. Both the rise and fall times should be less than 3 ns from 20% to 80%. See Figure 5-87.

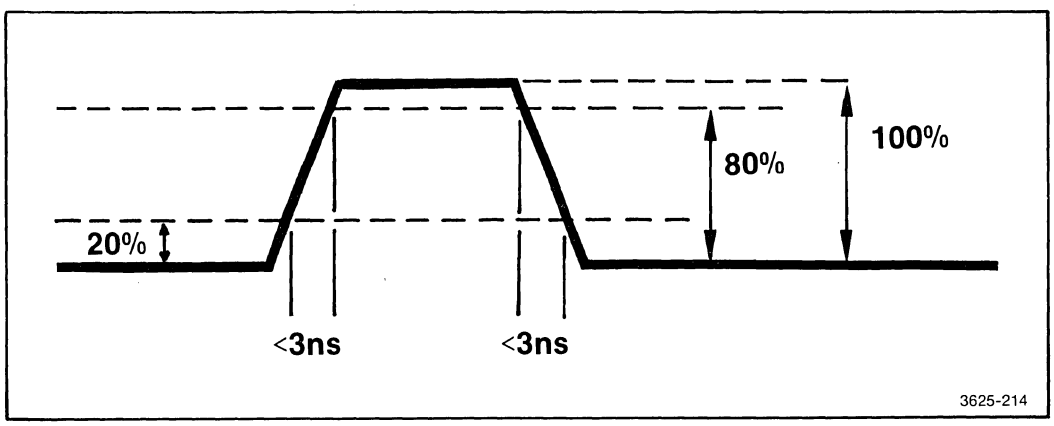

Figure 5-87. P6452 rise and fall times.

The output signals are accessible where the pod connector is soldered on to the acquisition board. Table 5-6 shows the correlation between pin numbers and the output channel from the probe.

Table 5-6
P6452 Signal Locations

Signal name	Pod connector pin number
CH0(H)	3
CH0(L)	2
CH1(H)	6
CH1(L)	5
CH2(H)	9
CH2(L)	8
CH3(H)	12
CH3(L)	11
CH4(H)	15
CH4(L)	14
CH5(H)	18
CH5(L)	17
CH6(H)	21
CH6(L)	20
CH7(H)	24
CH7(L)	23
CH8(H)	27
CH8(L)	26

(3) Setup for the Threshold Accuracy Check

1. Turn off the DAS mainframe.
2. Disconnect the flying lead set and ground connections from the pulse generator.
3. Reconnect all of the inputs of the lead set to the output of the variable dc power supply. Connect the ground sense lead to the ground of the variable power supply.
4. Connect the inputs of the DMM across the outputs of the variable dc power supply. Set the DMM to a range that will measure ±7.5 V.
5. Turn on the mainframe while holding down the STOP key to cause a power-up self-test failure.
6. Enter the Diagnostics menu. Select to run SINGLE functional tests on the slot containing the extender.
7. Select the DAC THRSH test for the module on the extender. Press START SYSTEM to start the DAC THRSH test.
8. Adjust the DAS menu so +0.000 V is selected for the DAC THRSH test.

(4) Threshold Accuracy Check

The next steps verify the threshold detection circuitry of the probe.

1. With the oscilloscope, monitor the output of probe CH0(H). Refer to Table 5-6 for the location of this output.
2. Slowly sweep the voltage out of the dc supply from −0.5 V toward +0.5 V.
3. Watching the oscilloscope, note when the trace changes from an ECL low to an ECL high, and stop the sweep.
4. Read the DMM to find out the voltage when the transition occurred. This voltage should be between −100 mV and +100 mV.
5. Repeat steps 1 through 4 for each of the active high outputs of the probe, CH1(H) through CH8(H). (Refer to Table 5-6 for the location of each output.) Each time the transition voltage should be inside ±100 mV.
6. Adjust the DAS menu so 1.600 V is selected for the DAC THRSH test.
7. With the oscilloscope, monitor the output of probe CH0(H). Refer to Table 5-6 for the location of this output.
8. Slowly sweep the voltage out of the dc supply from -6.0 V toward -8.0 V.

9. Watching the oscilloscope, note when the trace changes from an ECL low to an ECL high, and stop the sweep.

10. Read the DMM to find out the voltage when the transition occurred. This voltage should be between -6.17 V and -6.63 V.

11. Repeat steps 7 through 10 for each of the active high outputs of the probe, CH1(H) through CH8(H). (Refer to Table 5-6 for the location of each output.) Each time the transition voltage should be between +6.17 V and +6.63 V.

12. Adjust the DAS menu so −1.5875 V is selected for the DAC THRSH test.

13. With the oscilloscope, monitor the output of probe CH0(H). Refer to Table 5-6 for the location of this output.

14. Slowly sweep the voltage out of the dc supply from +7.0 V toward +6.0 V.

15. Watching the oscilloscope, note when the trace changes from an ECL low to an ECL high, and stop the sweep.

16. Read the DMM to find out the voltage when the transition occurred. This voltage should be between +6.58 V and +6.12 V.

17. Repeat steps 13 through 16 for each of the active high outputs of the probe, CH1(H) through CH8(H). (Refer to Table 5-6 for the location of each output.) Each time the transition voltage should be between +6.58 V and +6.12 V.

This completes the P6452 probe performance check. The test setup may now be dismantled. Turn off the DAS mainframe before removing the extender or any instrument modules. This prevents damage to the modules or the mainframe.

P6454 100 MHz CLOCK PROBE PERFORMANCE CHECK

To verify complete operation of the P6454 probe, the functional check for the probe should be performed before attempting this performance check. You will need the following equipment to complete this performance check procedure:

- DAS mainframe
- 91A08 Data Acquisition Module
- DAS Service Maintenance Kit
- 350 MHz, 2 channel oscilloscope
- 200 MHz variable sine wave generator with adjustable amplitude
- PG 502 Pulse Generator
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy

- BNC T
- BNC male to dual binding post
- Termination, 50Ω
- 5X Attenuator

For instructions on use of the various menus, refer to the Operating Information section of this manual. Refer to the beginning of this Verification and Adjustment Procedures section for information on using the Main Extender board in the DAS Service Maintenance Kit.

(1) Mainframe Setup

The next steps set up the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Install the Main Extender board in slot 6 of the DAS mainframe. Make sure the jumpers on the extender board are set to accept an acquisition module.
3. Install the 91A08 module on top of the extender board.
4. Connect the P6454 100 MHz Clock Probe to the coaxial connector on the rear edge of the 91A08 module.
5. Turn on the DAS mainframe and enter the Trigger specification menu.
6. Set the trigger mode to 91A08 only. Set the 91A08 clock to EXT ⌋⌈ and trigger on 55.
7. Enter the Channel Specification menu. Set the 91A08 (in slot 6) threshold to variable +0.00V.

(2) Threshold Accuracy Check

1. Connect a 5X attenuator to the output of the pulse generator. Connect a T connector to the 5x terminator.
2. Connect one side of the T connector to a 50Ω termination. Connect to the 50Ω termination a dual male binding post.

3. Connect to the binding post the P6454 Clock probe and a DMM.

4. Set the pulse generator PERIOD to EXT TRIG and PERIOD VARIABLE fully counter clockwise.

5. Set PULSE DURATION to SQ WAVE and pull the BACKTERM switch out. Pull the COMPLEMENT switch out and adjust the output low level for −45mV to −50mV.

6. Press COMPLEMENT switch in and adjust the output high level for +45 to +50mV. Change the PERIOD to .1μs and disconnect the DMM.

7. Connect channel two of the scope to TP511 on the 91A08.

8. Press START ACQUISTION on the DAS and look for an approximate 10MHz signal at an ECL level.

9. Press STOP and enter the CHANNEL SPEC menu and set the 91A08 threshold variable to −2.50V.

10. Remove the 5X attenuator from the pulse generator and repeat steps 3 through 7, adjusting the output high level to −2.62V and the output low level for −2.37V.

11. Press START ACQUISTION on the DAS and look for an approximate 10MHz signal at an ECL level.

12. Press STOP and enter the CHANNEL SPEC menu and set the 91A08 threshold variable to +5.00V. Repeat steps 3 through 7, adjusting the output high level for +5.20V and the output low level to +4.80V

13. Press START ACQUISTION on the DAS and look for an approximate 10MHz signal between +4.80V and +5.20V.

(3) Bandwidth and Sensitivity Measurement

These steps verify the bandwidth of the P6454 100 MHz Clock Probe.

1. Turn on the sine wave generator and terminate the output with 50 Ω. Using a BNC T, connect a scope probe to a Probe tip to BNC adapter and connect a BNC male to dual binding post adapter to the 50 Ω termination. Connect CH 1 of the scope to the Probe to BNC adapter. Set the output of the sine wave generator to 25 MHz. Set the signal amplitude to 700 mV peak to peak centered around ground.

2. Connect the IN lead of the P6454 probe to the positive binding post. Connect the REF lead of the probe to the ground binding post.

3. With the oscilloscope, watch the signal being transmitted by the probe. (This signal is available on the solder side of the 91A08 module across R702. The signal should be a sine wave. AC couple the scope and use a scope probe with a bayonet ground assembly.

4. With the oscilloscope, measure the amplitude of the output of the P6454 probe. To meet the input sensitivity specification, the amplitude should be equal to or greater than 70 mV. Record this amplitude.

5. Multiply the amplitude measurement just taken by 0.707. This gives the amplitude the signal will have when it has lost 3 dB. Record this value.

6. Increase the frequency of the sine wave while maintaining a constant amplitude of 700mV. Continue to increase the frequency of the sine wave until the signal from the probe has decreased by 3 dB.

7. Check the frequency of the sine wave generator at this point. The frequency of the generator should be above 150 MHz.

P6455 TTL/MOS PATTERN GENERATOR PROBE PERFORMANCE CHECK

To verify complete operation of the P6455 probe, the functional check for the probe should be performed before attempting this performance check. You will need the following equipment to complete this performance check procedure:

- DAS mainframe
- 91P16 Pattern Generator Module
- 100 MHz oscilloscope
- Dual variable dc power supply
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy
- Ten 1.5 kΩ resistors

For instructions on use of the various menus, refer to the Operating Information section of this manual.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

(1) Mainframe Setup

The next steps setup the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Install the 91P16 module in slot 1 of the DAS mainframe.
3. Set one channel of the power supply to ground and the other channel to +5 V.
4. Connect the P6455 TTL/MOS Pattern Generator Probe to pod connector B on the rear edge of the 91P16 module.
5. Set the recessed slide switch on the back of the P6455 TTL/MOS Pattern Generator Probe to NORM.
6. Connect the V_L line of the P6455 probe to the power supply output that is currently set to ground.
7. Connect the V_H line of the P6455 probe to the +5 V output of the power supply.
8. Install a high speed lead set in the probe.
9. Turn on the DAS mainframe.
10. Enter the Pattern Generator Program menu. Adjust the program to match the following:

SEQ	LABEL	HEX	INSTRUCTIONS		STROBES
0	TEST	0000			0
1		00FF			
2		0000			
3		00FF	GOTO	TEST	

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11. Set the pattern generator clock to internal 40 ns.

(2) Maximum Frequency Verification

The next steps verify the operation of the probe at 25 MHz with $V_L = 0$ V and $V_H = +5$ V.

1. Press the START PAT GEN key on the DAS keyboard.
2. With the oscilloscope, examine the CLK line out of the probe. The signal should be present at 25 MHz. The amplitude of the signal should be at least 3 V peak to peak.
3. Examine the data lines out of the probe with the oscilloscope. The signal should be present at 12.5 MHz. The amplitude of the signal should be at least 3 V peak to peak.
4. Examine the STRB output of the probe with the oscilloscope. The signal should be present at 6.25 MHz. The width of the high pulse should be between 30 and 50 ns.

(3) Logic Supply Voltage Check

These steps check the limits of the acceptable logic supply voltages.

CAUTION

Some of the following tests take the probe to the limit of acceptable logic thresholds. Do not overshoot these voltages or the probe may be damaged.

1. Enter the Pattern Generator Program menu. Set the pattern generator clock to internal 1 μs.
2. Press the START PAT GEN key.
3. Use the oscilloscope to monitor the CLK output of the P6455 probe. Being careful not to overshoot the target, increase the voltage for the V_H probe supply to +15 V. The CLK output should have a pulse wave that swings near the high and low logic supplies.
4. Examine the other outputs of the probe. All outputs should exhibit pulses with an amplitude similar to the clock line.
5. Use the oscilloscope to monitor the CLK output of the P6455 probe. Being careful not to overshoot the target, decrease the voltage for the V_H probe supply to 0 V.
6. Being careful not to go past the mark, decrease the voltage for the V_L probe supply to −15 V. The CLK output should still have a pulse wave that swings near the high and low logic supplies.
7. Examine the other outputs of the probe. All outputs should exhibit pulses with an amplitude similar to the clock line.

8. Increase the voltage for the V_L probe supply to -12.5 V.

9. Use the oscilloscope to monitor the CLK output of the P6455 probe. Being careful not to overshoot, increase the voltage for the V_H probe supply to $+12.5$ V. The CLK output should show a pulse waveform of approximately 24 V peak to peak.

10. Examine the other outputs of the probe. All outputs should exhibit pulses with an amplitude similar to the clock line.

(4) Current Drain Verification

These steps verify that the probe does not draw more than the specified operating current.

1. Press the STOP key on the DAS. This stops the pattern generator and helps protect the probe during the next connections.

2. Set the DMM to a range that will read 120 mA dc current.

3. Disconnect the power supply from the V_H line of the probe. Connect one lead of the DMM to the V_H line of the probe.

4. Connect one lead of the DMM to the power supply that was providing the voltage to the V_H line of the probe.

5. Enter the Pattern Generator Timing menu. Change the MODE field to STEP.

6. Press the START PAT GEN key. The DMM should indicate that 120 mA or less is being drawn by the probe.

7. Press the START PAT GEN key again. DMM should still indicate that the probe is drawing 120 mA or less.

8. Press the STOP key. This stops the pattern generator and helps protect the probe during the next connections.

9. Disconnect both of the leads of the DMM from the power supply and the probe. Reconnect the V_H line of the probe to the power supply that is set to $+12.5$ V.

10. Disconnect the power supply from the V_L line of the probe. Connect one lead of the DMM to the V_L line of the probe.

11. Connect one lead of the DMM to the power supply that was providing the voltage to the V_L line of the probe.

12. Press the START PAT GEN key. The DMM should indicate that 120 mA or less is being drawn by the probe.

13. Press the START PAT GEN key again. DMM should still indicate that the probe is drawing 120 mA or less.

14. Press the STOP key.

15. Disconnect both of the leads of the DMM from the power supply and the probe. Reconnect the V_L line of the probe to the power supply that is set to −12.5 V.

(5) Output Level Verification

These steps verify the output levels of the P6455 probe.

1. If they are not already present, put gripper tips on all outputs of the lead set.

2. Connect all of the outputs of the probe to 1.5 kΩ resistors. Connect all of the resistors to the ground of the dual power supply. Each probe channel now has a load of approximately 8 mA with either of the output logic states.

3. Press the START PAT GEN key. The probe should now output FF hexadecimal.

4. With the DMM, check the output voltage of all data channels of the probe. All voltages should be greater than +10.9 V.

5. Press the START PAT GEN key. The probe should now output 00 hexadecimal.

6. With the DMM, check the output voltage of all data channels of the probe. All voltages should be less than −12.0 V.

This completes the P6455 TTL/MOS Pattern Generator Probe performance check. The test setup may now be dismantled. Turn off the DAS mainframe before removing any instrument modules. This prevents damage to the modules or the mainframe.

P6456 ECL PATTERN GENERATOR PROBE PERFORMANCE CHECK

To verify complete operation of the P6456 probe, the functional check for the probe should be performed before attempting this performance check. You will need the following equipment to complete this performance check procedure:

- DAS mainframe
- 91P16 Pattern Generator Module
- 100 MHz oscilloscope
- Dual variable dc power supply
- 3.5 digit digital multimeter (DMM) with 0.1% or greater accuracy
- Ten 50 Ω resistors

For instructions on use of the various menus, refer to the Operating Information section of this manual.

NOTE

Measure all waveform durations in the following steps at 50% of the amplitude of the waveform.

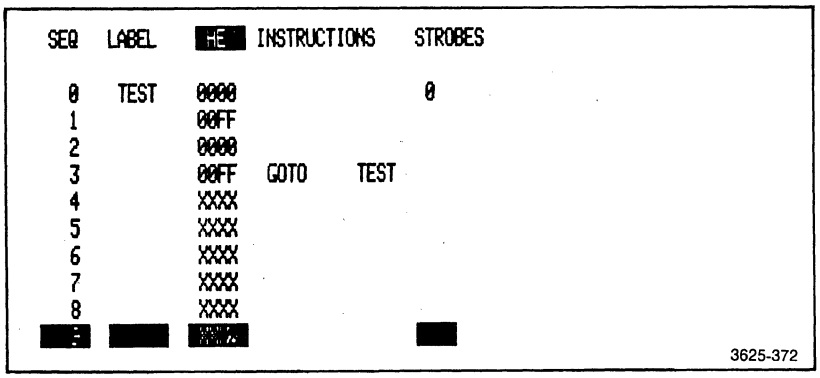
(1) Mainframe Setup

The next steps set up the DAS mainframe in the way recommended for this performance check procedure.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so will probably damage the module or sub-assembly.

1. Turn off the DAS mainframe.
2. Install the 91P16 module in slot 1 of the DAS mainframe.
3. Set the power supply so one channel is adjusted to −3.0 V and the other channel is adjusted to +2.0 V.
4. Connect the P6456 ECL Pattern Generator Probe to pod connector B on the rear edge of the 91P16 module.
5. Set the recessed slide switch on the back of the P6456 ECL Pattern Generator Probe to NORM.
6. Connect the V_L line of the P6456 probe to the power supply output that is currently set to −3.0 V.
7. Connect the V_H line of the P6456 probe to the +2.0 V output of the power supply.
8. Install a high speed lead set in the probe.
9. If they are not already present, put gripper tips on all outputs of the lead set.
10. Connect all of the outputs of the probe to 50 Ω resistors. Connect all of the resistors to the ground of the dual power supply. Each probe channel now has a 100 Ω load for proper ECL operation.
11. Turn on the DAS mainframe.
12. Enter the Pattern Generator Program menu. Adjust the program present to match the following program.
13. Set the pattern generator clock to internal 40 ns.



(2) Maximum Frequency Verification

The next steps verify the operation of the probe at 25 MHz with standard ECL levels.

1. Press the START PAT GEN key on the DAS keyboard.
2. With the oscilloscope, examine the CLK line out of the probe. The signal should be present at 25 MHz. The amplitude of the signal should be at least 0.65 V peak to peak.
3. Examine the data lines out of the probe with the oscilloscope. The signal should be present at 12.5 MHz. The amplitude of the signal should be at least 0.65 V peak to peak.
4. Examine the STRB output of the probe with the oscilloscope. The signal should be present at 6.25 MHz. The width of the high pulse should be between 30 and 50 ns.

(3) Output Level Verification

These steps verify the output levels of the P6456 probe.

1. Enter the Pattern Generator Timing menu. Change the MODE field to STEP.
2. Press the START PAT GEN key. The probe should now output FF hexadecimal.
3. With the DMM, check the output voltage of all data channels of the probe. All voltages should be between +1.4 V and +1.0 V.
4. Press the START PAT GEN key. The probe should now output 00 hexadecimal.
5. With the DMM, check the output voltage of all data channels of the probe. All voltages should be between +0.35 V and +0.0 V.

This completes the P6456 ECL Pattern Generator Probe performance check. The test setup may now be dismantled. Turn off the DAS mainframe before removing any instrument modules. This prevents damage to the modules or the mainframe.

TAPE DRIVE (OPTION 01) PERFORMANCE CHECK

The performance check for the tape drive requires special test equipment that is not available to the general public. If a performance check is desired, the DAS mainframe containing the tape drive must be sent to a Tektronix Service Center. There is a charge for the performance check.

I/O INTERFACE (OPTION 02) PERFORMANCE CHECK

There is no performance check procedure for the I/O Interface. The functional check, given elsewhere, is sufficient to verify the operation of the I/O Interface.

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MANUAL CHANGE INFORMATION

Date: 8-23-84 Change Reference: M51781

Product: DAS 9100 SERIES SERVICE VOL. I Manual Part No.: 070-3625-01

DESCRIPTION

Product Group 57

THIS IS AN ADD PAGE PACKAGE

1. Add the following pages to your manual:
   5-129A, 5-130A, 5-131A, and 5-132A.

2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.

000-2775-00D

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MANUAL CHANGE INFORMATION

Date: 12-17-84 Change Reference: C9/1284

Product: DAS 9100 Series Service Vol. I Manual Part No.: 070-3625-01

DESCRIPTION

THIS IS A PAGE PULL AND REPLACE PACKAGE

1. Remove the designated pages from your manual and insert the following page 1-23, 1-24, 1-27 and 1-28.

2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.