155 Mb/s Optical Line Interface

Agilent Technologies Broadband Series Test System

E1697A

Product Features

- Cell based implementation
- Operates in both cell mode and SONET/SDH frame mode
- Provides access to ATM cells via parallel data ports in byte serial fashion
- Provides physical layer measurements as well as error generation
- Internal traffic generator has 1 foreground channel and up to 100 background channels

The Agilent Technologies E1697A 155 Mb/s Optical Line Interface generates and analyses ATM cell streams contained within a SONET or SDH framing format. It is a single-slot VXI module that provides test capability at the physical and ATM cell layers for the Agilent E4200/E4210 Broadband Series Test System.

The E1697A is capable of operating in both a cell mode and in a SONET/SDH frame mode. This allows the user to not only examine ATM cells mapped into a SONET/SDH frame but also all of the SONET/SDH frame data.

Line interface modules not only connect the device or system under test to your Broadband Series Test System, but also provide physical, convergence, and ATM cell testing capabilities.

Transmission test functionality includes:

- Traffic generation
- Cell error, loss & delay measurements
- Traffic capture & playback

The E1697A 155 Mb/s Optical Line Interface can be used in conjunction with other BSTS line interfaces, dedicated test modules, and test software to perform these tests.

Key Features

Generate Normal or Abnormal Test Traffic

Create and detect erroneous test traffic on demand to test the robustness of a protocol implementation. Sophisticated protocol data unit builder, sequencing, and library functions let you easily create complex and realistic traffic. You can generate test traffic in the foreground channel, and use up to 100 background channels to simulate loading effects.

Cell Error, Loss & Delay Measurements

Bit rate error testing is done by placing PRBS patterns in cells, and looping these cells back through a system under test. The received cells are analyzed to detect PRBS errors. These errors can then be used as a trigger to capture data.

Cell delay, interarrival time, and loss measurements are easily accomplished with the BSTS. Timestamps are inserted in cells transmitted by the line interface. These cells can then be captured, and graphs for both cell delay and cell interarrival time displayed.

Sequence numbers are transmitted in ATM cells and looped back through a system under test. The lost cells can then be detected and counted with statistics or used as a trigger to capture data.

You can generate physical and convergence layer errors and alarms. You can also capture and playback convergence layer frames.

Real-time statistics can be gathered for the physical, convergence and cell layers. Statistics can be reported as errored seconds, event counts, or as error ratios.

Traffic Capture & Playback

Traffic can be captured with a 1500 cell capture memory. Complete control is available - continuously capture with memory buffer lapping, or trigger on user-defined events. Captured traffic can be played back with automatic decoding into an English-language display. Terminology from standards documents is used wherever possible.

Since high-speed networks carry considerable volumes of traffic, you can increase your test productivity by using filters and triggers to display or capture only traffic of interest. Filters let you select virtual channels or paths of interest.

Triggers can be used to capture data matching a specific pattern. For example, triggers can be used to capture cells with header errors or sequence number errors, or upon changes in convergence layer frame bytes.

Includes parallel data ports to transmit and receive ATM cells

The E1697A has two parallel data ports, one to transmit and one to receive ATM cells in byte serial mode. The parallel ports includes byte-wide cell data, a cell synchronization pulse, and a variable rate clock input and output.

Configuration & Use With Other BSTS Line Interfaces, Test Modules & Test Software

Line interface modules can perform physical layer testing with a minimal BSTS configuration consisting of a line interface module and chassis. A complete range of test software applications and dedicated test modules is available to perform upper layer testing.

The E4209 Cell Protocol Processor provides monitoring and simulation test functions at the ATM and adaptation layers by executing optional protocol testing software applications. The CPP performs many functions in hardware that are usually done in software - such as an automatic segmentation and reassembly engine for sophisticated real-time ATM, AAL and other higher layer protocol testing.

Documentation Included

- User's Guide
- Programmer's Guide
- Product Release Notice

Product Numbers

E1697A 155 Mb/s Optical Line Interface (includes AMP 26 pin slimline D socket to DB25 data port cable) wih SC Connectors

Opt # UHV ST Connectors
Opt # UHW FC/PC Connectors

Warranty & Support Options

All BSTS hardware components are warranted for a period of 3 years. Products must be returned to an authorized Agilent service center for service. At the time of purchase you may select warranty option W01, a no-charge option which converts the standard 3-year return to Agilent warranty to a 1-year on-site warranty.

Support option UK6, available at time of purchase, is a standards-compliant calibration which ensures that your BSTS test system operates within specified tolerances. A certificate of calibration is issued for compliance with ISO 9000 standards which require that records documenting the calibration of measuring and test equipment are maintained. Certificates of calibration are not available for products which do not contain components requiring calibration (such as software).

Two other types of calibration, commercial and standards-complaint, are available at any time from your local Agilent service center. Both provide test data and a certificate for your records. With a commercial calibration, any problems are resolved as they are detected, and test data reflecting performance of your calibrated test system is provided. The standards-compliant calibration provides comprehensive before and after test data to document problem resolution.

Technical Specifications

Traffic Generation

Modes

Three Tx/Rx modes are available. In Terminal mode, full signal generation and analysis functions are available. In Repeater mode, the received signal is re-transmitted (physical layer loop back). In Local Loopback mode, the transmit signal is electrically looped to the receiver.

ATM Cell Generation

The transmitted cell stream can contain ATM cells generated internally by the E1697A, and ATM cells generated by an optional E4209 Cell Protocol Processor module. ATM cells generated on-board can consist of one foreground channel to stimulate the channel under test, and up to one hundred background channels for loading purposes. Fill cells are used to occupy unused bandwidth.

Total Bandwidth	• 149.76 Mb/s
Modes	• User-Network Interface (UNI) or Network-Node Interface (NNI)
HEC	• Automatic generation
Fill Cells	• Idle or unassigned
Channel Priority Order	• Foreground, background, CPP (highest to lowest priority)
Channel Control	• VCI • VPI • GFC • Payload Type • Cell Loss Priority
SAR-PDU Support	• AAL-0 • AAL-1

Foreground Channel

Bandwidth	• From 100 b/s to 149.76 Mb/s in 10 b/s increments
Accuracy	• +/- 0.07 ppm
Distribution	• Off • Single burst • Periodic (according to the specified bandwidth)
Channel Depth	• 1500 cells (variable)
Cell Payload	• Timestamp • Single cell PRBS • Cross cell PRBS • Data pattern • Byte access

Background Channels

Number of Channels	• Up to 100
Bandwidth	• 3000 b/s to 149.76 Mb/s in increments of 3000 b/s
Accuracy	• +/- 21 ppm
Distribution	• Off • Periodic
Channel Density	• Bandwidth and cell distribution for each background channel is individually assignable up to maximum bandwidth
Channel Depth	• 16 cells
Cell Payload	• Single cell PRBS • Data pattern • Byte access

Cell Payloads

Payloads	• Time stamp (32-bit departure time stamp value with 100 nanosecond resolution) • Cross cell PRBS-9 • PRBS-15 (inverted and not inverted) • PRBS-23 • Single cell PRBS-9 • Data pattern or byte access
Data Patterns	• User byte • AA55h or FF00h • Incrementing (value of each successive byte is incremented by 1)
Byte Access	• Payload of all cells in the selected channel can be edited by the user in an active channel environment, or off-line as a sequence of PDUs • AAL-1 automatically inserts first payload byte containing SN/SNP values and CSI bit

Erroring Control

Error conditions can be introduced to simulate alarm signals and signal stressing. Error stressing is used to generate incorrect bytes in a test signal.

Error Stressing Control	• Off • On • Pulse On (error condition is normally off; pulses on) • Pulse off (normally on; pulses off) • Sequence On (normally off; alternates on/off/on) • Sequence Off (normally on; alternates off/on/off)
ATM Error Injection	• Cell header or payload bytes with bit error masking
Cell Loss	• Sequence Number in the SAR-PDU is skipped and a fill cell is inserted
PRBS Error Add	• Single bit error add to the PRBS pattern in the cell payload

SONET/SDH Stressing

SONET/SDH Stressing	• SPE pointer errors can be introduced once or at a user defined sequence • Data errors can be introduced singly or at a rate of 1.0E-9 to 1.0E-3 on to the Section/RS BIP, Line/MS BIP,Path BIP, Line/MS FEBE and Path FEBE • Loss of signal for either a single frame, or continuous

ATM & SONET/SDH Measurements

Measurements are sampled every 100 milliseconds and accumulated over the user-specified measurement period. Results from the most recent complete measurement period are retained

Measurement Period	• Range 1 second to 3 days in resolutions of 1 second
Result Types	• Cumulative or latched (based on most recent measurement period)
Result Formats	• Count • Ratio • Seconds
ATM Cell Measurements	• HEC errors • Corrected headers • Cell count • Cell bandwidth • Select Cell Not Received (SCNR) alarm seconds
Cell Delay Measurements	• Cell delay • Inter-arrival time • Cell delay variation
Virtual Channel Errors	• AAL-1 SN/SNP errors • Cell loss • PRBS errors • PRBS sync loss alarm seconds
SONET/SDH Measurements	• Out of frame errors • Loss of frame alignment errors • Loss of pointer errors • Loss of cell synchronization error • Loss of signal errors • Line AIS • Line FERF • Path AIS • Path FERF • Path yellow • Section BIP • Line BIP • Path BIP • Path FEBE • Line FEBE • Uncorrected HEC error

Traffic Capture & Playback

ATM Capture

Provides capture of 1500 cells from the selected ATM cell stream. Capture is manual or event triggered. Manual triggering captures 1500 cells after the trigger. Event triggering captures 750 cells pre-trigger, and 750 cells post-trigger.

Manual	• Triggered on user request
ATM Cell Triggers	• Cell loss • Header error • PRBS error • SN/SNP byte error

SONET/SDH Capture

When in SONET/SDH frame mode, the E1697 line interface captures and displays TOH data, POH data, and path trace messages.

Parallel Data Port

The E1697A line interface has two parallel data ports, one to transmit and one to receive ATM cells in byte serial mode. The parallel ports includes byte-wide cell data, a cell synchronization pulse, and a variable rate clock input and output. Cells may be optionally scrambled and descrambled. Connector D1 is the receive data port interface; connector D2 is the transmit data port interface. The receive data port provides automatic cell delineation using the HEC method as per ITU-T Recommendation I.432. Input cell synchronization is not required.

Data Port Specifications

Clock source	• 155.52 Mb/s using internal clock source; 20 Mb/s to 156 Mb/s using external clock
Clock rate	• 19.44 MHz using internal clock source; 2.5 MHz to 19.5 Mhz using external clock
Line format	• Non Return to Zero (NRZ)
Input and output levels	• TTL
Input impedance	• > 1000 ohms
Source impedance	• 50 ohms (typical)
Required load impedance	• Greater than 500 ohms; less than 15 picoFarad
Recommended cable	• Less than 1 meter of 3M type 3600/26 shielded twisted pair

Timing

Timing relationships between the clock and data for the transmit and receive data ports are shown in figures below.

Figure 1. Parallel data port specifications

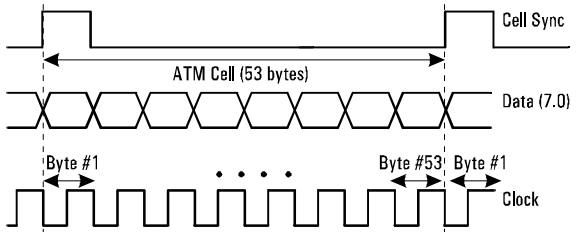


Figure 2. Parallel data port transmit timing

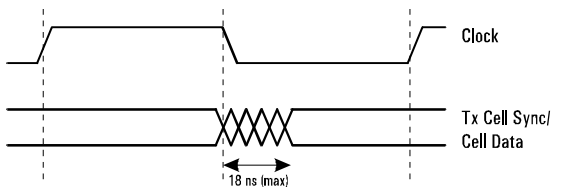
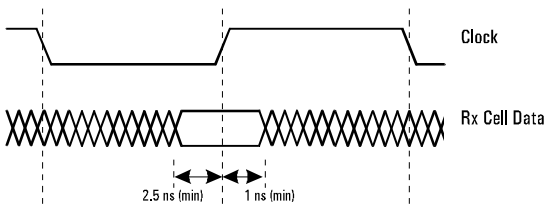


Figure 3. Parallel data port receive timing



Parallel Port Pinouts

The D1 and D2 data ports use high-density 26 pin slim line female D connectors.

Signal	Connector	Adaptor Cable
Data 0	• 3	• 3
Data 1	• 4	• 4
Data 2	• 5	• 5
Data 3	• 6	• 6
Data 4	• 7	• 7
Data 5	• 8	• 8
Data 6	• 9	• 9
Data 7	• 10	• 10
Sync	• 12	• 12
Clock	• 1	• 1
Ground	• 13,14,19,23,25,26	• 13,14,19,25

Front Panel Connectors & Indicators

OC-3 Input	• FC-PC adapter • Rx sensitivity of -24 dBm for 10E-10 residual BER • Input overload greater than -7 dBm • 1310 nm
OC-3 Output	• FC-PC adapter • Class 1 laser • 1310 nm Exceeds Intermediate Reach (IR) specifications
Reference Clock Input	• SMB connector • 1 V p-p input • Nominal 50 ohm impedance • 155.52 MHz with better than a 55/45% duty cycle
Rx/Tx Trigger Outputs	• SMB connectors • TTL outputs • Nominal 50 ohm impedance
Tx Clock/Data Trigger Outputs	• SMB connectors • ECL levels • Clock: 155.52 Mhz with better than a 55/45% duty cycle • Data: 155.52 Mb/s serial stream Timing, propagation delay of 2.5 to 5.0 nanosecond w.r.t. rising clock edge • 50 ohms, terminated to -2 V
Rx Clock/Data Trigger Inputs	• SMB connectors • ECL levels • Clock: 155.52 Mhz with better than a 55/45% duty cycle • Data: 155.52 Mb/s serial stream NRZ timing, setup and hold within 400 picosecond w.r.t. rising edge • 50 ohms, terminated to -2V
LED Indicators	• Failed • Error • Access • Ref Clk • Gating • Signal • BIP

Size, Weight & Power Dissipation

Size	• 1 slot C-size VXI card
Weight	• 1.3 kg (2.9 lb) nominal
Power Dissipation	• 36 Watts (max)

Applicable Standards

ATM Cells	• ITU-T Recommendation I.361 1995 B-ISDN ATM layer specification • Telcordia TA-NWT-001113 1993 Asynchronous Transfer Mode and ATM Adaptation Layer (AAL) Protocols Generic Requirements
SONET/SDH	• SDH as per ITU-T G.708 and I.361 for BSTS CD-ROM software releases prior to version A.10; SDH as per ITU-T G.707 (draft) COM 15-163-E, July 1995 "Draft revised ITU-T recommendation G.707 network node interface for the synchronous digital hierarchy (SDH)" for A.10 and later releases • SONET as per Telcordia TA-NWT-000253 for BSTS CD-ROM software releases prior to version A.10; SONET as specified by Telcordia GR-253-CORE "Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria" for releases A.10 and later
PRBS Patterns	• PRBS-9 as per ITU-T O.153 1992 • PRBS-23 as per ITU-T O.151 1992
EMC	• CISPR11, Class A

Agilent Technologies Broadband Series Test System

The Agilent Technologies BSTS is the industry-standard ATM/BISDN test system for R&D engineering, product development, field trials and QA testing. The latest leading edge, innovative solutions help you lead the fast-packet revolution and reshape tomorrow's networks. It offers a wide range of applications:

- ATM traffic management and signalling
- Packet over SONET/SDH (POS)
- switch/router interworking and performance
- third generation wireless tesing
- complete, automated conformance testing

The BSTS is modular to grow with your testing needs. Because we build all BSTS products without shortcuts according to full specifications, you'll catch problems other test equipment may not detect.

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Specifications subject to change.

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