HEWLETT hp PACKARD

LSI-11 Q-BUS™ INTERFACE

Model 10276A

OPERATING NOTE/NOVEMBER 1978

1. DESCRIPTION.

2. The HP Model 10276A LSI-11, Q-Bus Interface provides a method for easy, fast connection between a Hewlett-Packard Logic Analyzer and an LSI-11 minicomputer. The interface is a dual-height board that plugs directly into the LSI-11 bus to access bus signals. Active circuits on the interface board demultiplex the address and data bus and generate a Logic Analyzer clock signal for analysis of asynchronous bus activity. Switches are provided on the 10276A to allow selective qualification of Q-bus activity so that reads, writes, interrupt vectors, refresh activity, or DMA transfers can be selectively captured or excluded. An additional interface board circuit allows a low or high true signal from the Logic Analyzer or other system to activate the minicomputer HALT input which allows control of minicomputer operation during design or troubleshooting. The 10276A interface can be used as: (1) an I/O peripheral, (2) an expansion module for connection to another mainframe, or (3) by using three DIP terminators (available from Digital Equipment Corporation) as a terminator module. Refer to table 1 for complete specifications.

3. INTERFACE CONNECTIONS.

4. A ribbon cable from the HP Model 10277 (described in paragraph 6) may be connected to the 10276A Interface Board in the minicomputer, or Data and Clock Probe leads can be connected to pins on the interface connectors.

NOTE

Follow the computer manufacturer's instructions for removal and installation of printed circuit boards when using the Model 10276A.

5. ACCESSORIES AVAILABLE.

6. For maximum measurement flexibility, an HP Model 10277 Option 001 General Purpose Probe Interface is available for easy connection to the Q-bus interface. Connection to the system under test is accomplished with a ribbon cable between the interfaces, and the Logic Analyzer pods plug directly into the 10277. Changing electrical configurations for analysis of signals is accomplished by simply changing a plug-in, wire-wrap board in the 10277.

Table 1. Specifications

BUS LOADING: one unit DEC™ load (type 956, P/N DEC 8640 Bus Receiver) with 12 pF maximum shunt capacitance at the edge connector (normally 6 pF).

GENERAL

Weight: net, 0.2 kg (0.4 lb).

Power: when used as interface, 500 mA nominal, 900 mA max; when used as a terminator, 1000 mA nominal, 1600 mA max.

Dimensions: see outline drawing.

Operating Environment: temperature, +5°C to +40°C; humidity, to 95% relative humidity at +40°C; altitude, to 4600 m (15 000 ft); vibration, vibrated in three planes for 15 min. each with 0.3 mm (0.015 in.) excursions, 10 to 55 Hz.

RECOMMENDED ACCESSORIES: HP Model 10277 Option 001 General Purpose Probe Interface. Three DIP Terminators (DEC P/N 1311003-01) available from Digital Equipment Corporation (required to use the 10276A as a terminator).

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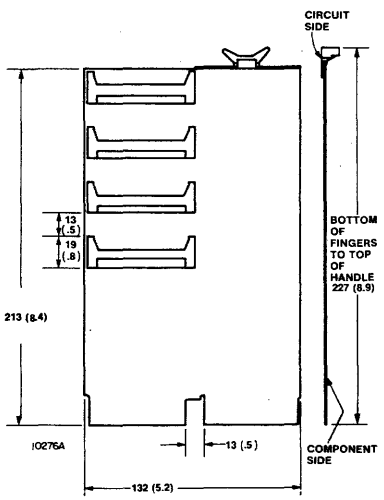
NOTES:

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



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For More Information, Call Your Local HP Sales/Service Office or, in U.S., East (201) 265-5000. Midwest (312) 677-0400. South (404) 436-6181. West (213) 877-1282. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Post Office Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. In Japan, YHP,1-59-1, Yoyogi, Shibuya-ku, Tokyo, 151.

7. Three DIP Terminators (DEC Part No. 1311003-01, available from Digital Equipment Corporation) are required to use the HP 10276A as a terminator.

8. APPLICATIONS.

9. SOFTWARE DEVELOPMENT. The HP 10276A combined with a Logic Analyzer becomes a very powerful software debugging tool because it captures program state flow in real time and permits analysis of software timing loops. Once the software is debugged, optimization can be achieved via information available from the Logic Analyzer.

10. SERVICE AND MAINTENANCE. System signals can be accessed quickly by simply plugging the 10276A into the minicomputer backplane. Detailed analysis of program execution or the bus arbitration process with elapsed time intervals between events permits rapid troubleshooting with minimum computer downtime when software techniques are marginal or cannot be used.

11. PRODUCTION. The ability to analyze program execution during system integration allows you to observe how the system reacts as peripherals are added. Or, by directing the analyzer to trace only the activity to a specific peripheral, problems can be quickly detected and isolated.

12. HARDWARE DEVELOPMENT. During the design of new LSI-11 interfaces, program execution can be viewed in real time. This permits checking actual handshake protocol and tracing program execution while recording the times to perform various functions.

13. INSTALLATION.

14. The 10276A may be used as a general purpose module, as a terminator, or as a cable connector. Installation is as follows:

15. As a general-purpose module:

a. Install jumper W1 and remove jumpers W5 and W7.

b. Install the 10276A into any empty slot, and verify that the termination module is placed at the end of the bus.

c. Perform additional steps in paragraph 18.

16. As a terminator (replacing Module M9400-YB):

a. Install jumpers W1 and W7.

b. Install jumper W5 if installed on M9400-YB Module.

c. Install three 120-ohm resistor packs (DEC Part No. 1311003-01) in XU1, XU7, and XU18 noting pin 1 orientation.

d. Install the 10276A into the mainframe at the end of the bus in place of the M9400-YB Module.

e. Perform additional steps in paragraph 18.

17. As a cable connector (replacing Module M9401):

a. Install jumper W1 and remove jumpers W5 and W7.

b. Install the two ribbon cables from the M9400-YD, YE Module into the 10276A (J1 to J1 and J2 to J2) noting pin 1 orientation.

c. Install the 10276A into the first slot of the expansion chassis in place of the M9401 Module.

d. Perform additional steps under paragraph 18.

18. Perform the following additional steps for any of the three hook-up configurations:

a. Install jumpers AD16 and AD17.

b. If all 16 bits of address are desired, install jumper AD15; or, if a Read/Write flag is desired in place of the MSB of address, connect the common point of AD15 to RDOUT.

c. If it is desired to halt the processor on some external signal (for example, Measurement Enable), place a jumper in L (located beside U23) for an active low signal to halt the processor or in H for an active high to halt the processor. If this feature is not required, then install the N jumper.

d. If state-flow analysis is desired, connect a 40-pin ribbon cable from connector B to connector B on the HP Model 10277 Option 001, noting pin 1 orientations. Connect the external signal for halting the processor to the BNC connector on the 10277 Option 001. Format specifications for the HP Model 1610A or 1615A Logic Analyzers are as follows:

CLOCK: [—]
DATA: [+] Pods 1 and 2
ADDRESS: [+] Pods 3 and 4

e. If control signal analysis is desired, connect two 40-pin ribbon cables between the A and B connectors on the 10276A and the 10277 wire-wrap board noting pin 1 orientations. Connect signals as listed in table 2.

19. PRINCIPLES OF OPERATION.

20. The LSI-11 Q-Bus is an 18-bit multiplexed data bus that operates with asynchronous handshake signals to accomplish data transfers. This allows transfers to occur as fast as a master and slave device

Table 2. Control Signal Connections 10276A/10277

Q-BUS		
PIN NO.	A	B
1	RBS7	GND-ME
2	RWTBT	GND-P4
3	REVNT	MEAS ENBL
4	—	GND-P3
5	RSACK	CLOCK
6	RHALT	GND-CK
7	RSSPARE1	D15
8	RSSPARE2	GND-P2
9	RDOK	D14
10	RSSPARE3	GND-P1
11	RDCOK	D13
12	RSSPARE4	AD15
13	AD17	D12
14	+5 V	AD14
15	RSSPARE5	D11
16	RSSPARE6	AD13
17	AD16	D10
18	RSSPARE7	AD12
19	GND	D9
20	RSSPARE8	AD11
21	RINITH	D8
22	REFH	AD10
23	RDMGO	D7
24	—	AD9
25	RDMRH	D6
26	GND	AD8
27	RIAKOH	D5
28	+5 V	AD7
29	RIRQ	D4
30	—	AD6
31	RSYNC	D3
32	—	AD5
33	RDIN	D2
34	RDOUT	AD4
35	RRPLY	D1
36	RBSPARE1	AD3
37	—	D0
38	RBSPARE2	AD2
39	GND	AD1
40	RBSPARE6	AD0

— Indicates user spare

can respond (see figure 1). Signals on the 10276A are buffered through DEC-type 8640 inverting buffers (see schematic figure 3). For this reason, the load presented to the bus is less than or equal to the standard Q-bus load. The signals are open collector negative true while the signals on the 10276A are positive true logic.

21. For a data out or write, the address is made valid on the bus by the master, and sync is asserted, indicating that the address can be read. The master then places the data on the bus and asserts DOUT. When RPLY is asserted, it signals the master that the data has been received and strobed in. Next, the master releases DOUT signaling that the data will soon be invalid; in response, RPLY is released followed by the release of SYNC concluding the transaction. For a write, the 10276A generates a clock for the Logic Analyzer to strobe in the latched address and data on the asserted edged of RPLY.

22. For a data in or read operation, the address is made valid on the bus and SYNC is asserted. The master then asserts DIN, and some time later, the slave responds with RPLY. After a delay and deskew time of 250 ns from RPLY, the master accepts data from the slave. Next, DIN is released followed by the release of RPLY. Finally, SYNC is released concluding the transaction. The 10276A generates a read clock for the Logic Analyzer to strobe in the latched address and data 250 ns after the asserted edge of RPLY.

23. Since the 10276A can differentiate between various types of transactions, four switches permit selection of only those transactions desired. These switches on the 10276A allow efficient use of a Logic Analyzer by prequalification freeing all channels for data and address tracing.

24. The function of U19, U22, and U25 is to latch the address on the rising edge of SYNC. Qualifier generation is accomplished by U23, U26, U28, U29A, U30 and the four switches. U26B/C and U29A are used to select qualification for interrupts and U23, U26A/F, and U28 are used to generate DMA and refresh qualifiers. All qualifiers are combined at U30 to generate a low true qualifier for U27B or U27A for read or write clock generation respectively. The read qualifier is clocked in U27B on the rising edge of RPLY and is delayed 250 ns before setting U21A and generating a clock to the Logic Analyzer. The write qualifier is clocked into U27A on the rising edge of RPLY which sets U21A immediately. The clock to the Logic Analyzer is delayed and fed back to clear U21A and U27A.

25. The halt circuitry is comprised of U28A/F, CR1, CR2, and Q1. An external signal applied to connector B, pin 3 will turn on Q1 asserting BHALT (active low) if the jumper is installed in H for high true signal or in L for a low true signal to halt the processor. With the jumper in the N position, the transistor is always off. Diodes CR1 and CR2 provide fast turn on/off and require that the output from either U28A or U28F be above 1.2 V before the transistor turns on. A wire-wrap area is provided on the 10276A to allow additional circuitry that may be required for special functions.

26. REPLACEABLE PARTS.

27. Replaceable parts are illustrated in figure 2 and listed in table 3. To order a replaceable part from Hewlett-Packard, address the order to the nearest HP Sales/Service Office. Include the interface model number, reference designation of the part and the HP part number. If a part is not listed, provide a complete description of the part, including function and location.

Table 3. Replaceable Parts

Reference Designation	HP Part No.	Qty	Description	Mfr Code	Mfr Part No.
A1	10276-66501	1	BOARD - LSI-11 Q-BUS INTERFACE	28480	10276-66501
C1 THRU C17	0160-3448	17	CAPACITOR-FXD 1000 PF ±10%, 1KVDC CER	56289	CO16B102F471 KS25-C
C18	0180-0229	1	CAPACITOR-FXD 33UF ±10% 10VDC TA	25088	D33B10KI
C19 THRU C21	0160-2261	3	CAPACITOR-FXD 15PF ±5% 500VDC CER	04222	CNI-NPO-15PF±5%
C22	0140-0175	1	CAPACITOR-FXD 39PF ±2% 300VDC MICA	72136	DM19F3050 RF0100WV1CR
CR1	1901-0518	2	DIODE-SCHOTTKY	28480	1901-0518
CR2	1901-0518		DIODE-SCHOTTKY	28480	1901-0518
JA	1251-5698	4	CONNECTOR		
JB	1251-5698		CONNECTOR		
J1	1251-5698		CONNECTOR		
J2	1251-5698		CONNECTOR		
L1	9100-2259	2	COIL-MLD 1.5UH 10% Q=32 .095D X .25 LG	02172	09-4436-2K
L2	9100-2261	2	COIL-MLD 2.7UH 10% Q=40 .095D X .25 LG	02172	09-4436-5K
L3	9100-2261		COIL-MLD 2.7UH 10% Q=40 .095D X .25 LG	02172	09-4436-5K
L4	9100-2259		COIL-MLD 1.5UH 10% Q=32 .095D X .25 LG	02172	09-4436-2K
MP1	0403-0283	1	PC BOARD PULLER	28480	0403-0283
Q1	1854-0071	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	01295	SKA1124
R1	0684-4711	1	RESISTOR-470 10% .25W FC TC=—400 +600	19701	(CR-25) 1-4-5P-47E
R2	0684-3311	1	RESISTOR-330 10% .25W FC TC=—400 +600	01121	CB3311
R3	0684-6811	1	RESISTOR-680 10% .25W FC TC=—400 +600	2M627	R-25J
R4	0684-1021	1	RESISTOR-1K 10% .25WF TC=—400+600	19701	(CR-25)1-4-5P-100E
R5	0757-0440	1	RESISTOR-7.5K 1% .125W F TC=0±100	07716	CEA-993
R6 THRU R13	0684-1031	8	RESISTOR-10K 10% .25W FC TC=—400 +700	19701	(CR-25) 1-4-5P-1K
S1 THRU S4	3101-2348	4	SWITCH-SPDT	95146	TSS11EG-RA
U1			NOT ASSIGNED (SPARE)		
U2 THRU U6	1820-2178	12	IC-8640 QUAD NOR UNIFIED BUS RCVR	27014	DS8640
U7			NOT ASSIGNED (SPARE)		
U8 THUR U14	1820-2178		IC 8640 QUAD NOR UNIFIED BUS RCVR	27014	DS8640
U15 THRU U18			NOT ASSIGNED (SPARE)		
U19	1820-0693	3	IC-DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP	01295	SN74S74N
U20			NOT ASSIGNED		
U21	1820-0693		IC-DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP	01295	SN74S74N
U22	1820-1730	2	IC-OCTAL D-TYPE FLIP-FLOP	01295	SN74LS273
U23	1820-0691	1	IC-GATE TTL S AND-OR-INV	01295	SN74S64N
U24	1820-0261	1	IC-MONOSTABLE MULTIVIBRATOR	01295	SN74S121N
U25	1820-1730		IC-OCTAL D-TYPE FLIP-FLOP	01295	SN74LS273N
U26	1820-0683	2	IC-HEX INVERTER	01295	SN74S04N
U27	1820-0693		IC-DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP	01295	SN74S74N
U28	1820-0683		IC-HEX INVERTER	01295	SN74S04N
U29	1820-1158	1	IC-GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U30	1820-0688	1	IC-DUAL 4-INPUT NAND	01295	SN74S20N
XU1	1200-0607	3	SOCKET-IC 16-CONT DIP-SLDR	09922	DILB16P-108
XU7	1200-0607		SOCKET-IC 16-CONT DIP-SLDR	09922	DILB16P-108
XU18	1200-0607		SOCKET-IC 16-CONT DIP-SLDR	09922	DILB16P-108

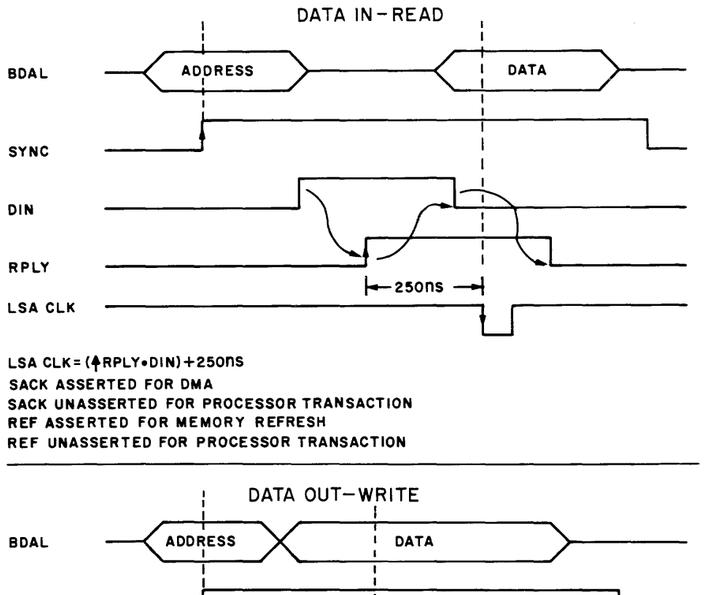

Figure 1. Timing Diagrams

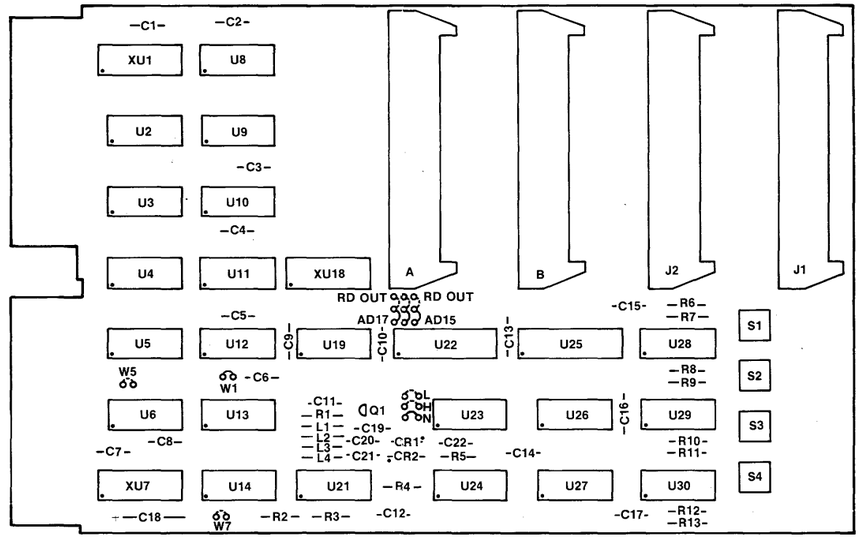

Figure 2. 10276A Component Locations

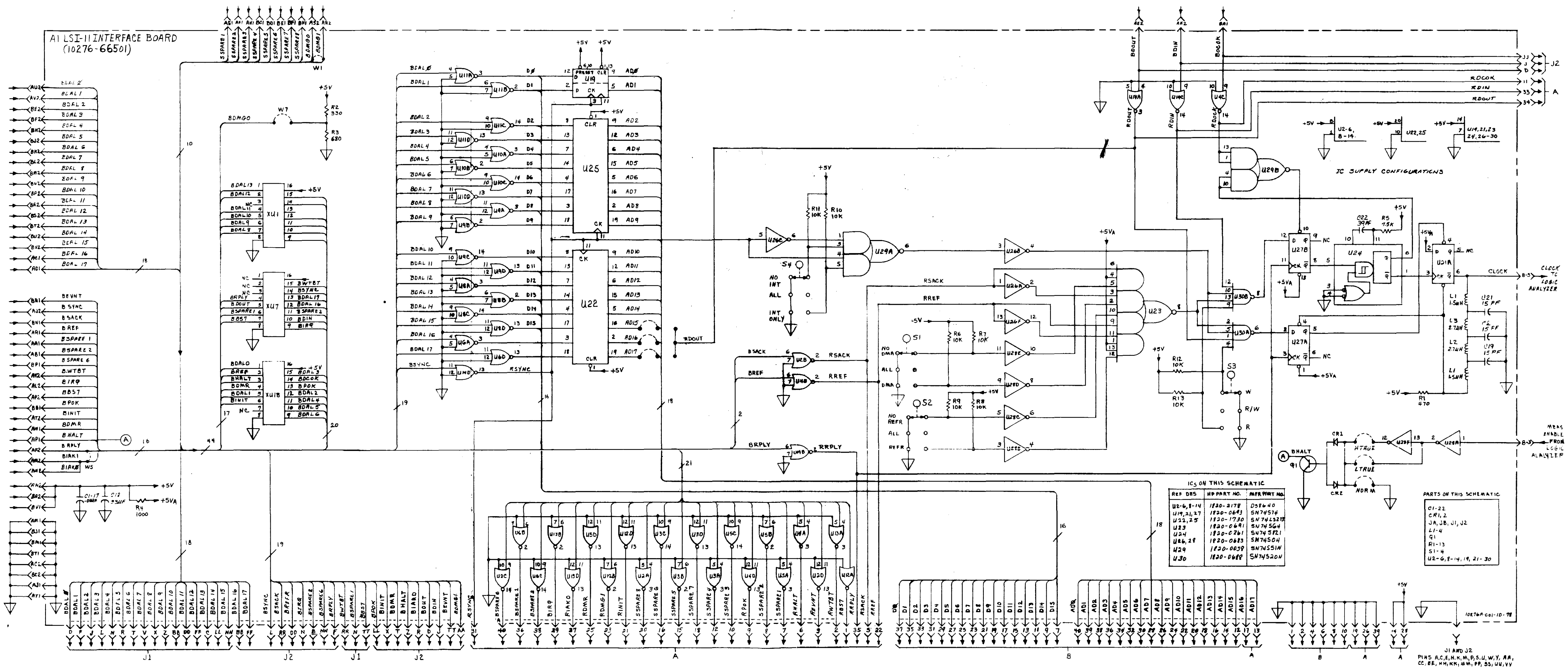

Figure 3. Schematic for 10276A