9010A

Micro-System Troubleshooter

Operator Manual

FLUKE®

Table of Contents

(continued on page ii)

TABLE OF CONTENTS, *continued*

(continued on page iii)

TABLE OF CONTENTS, *continued*

(continued on page iv)

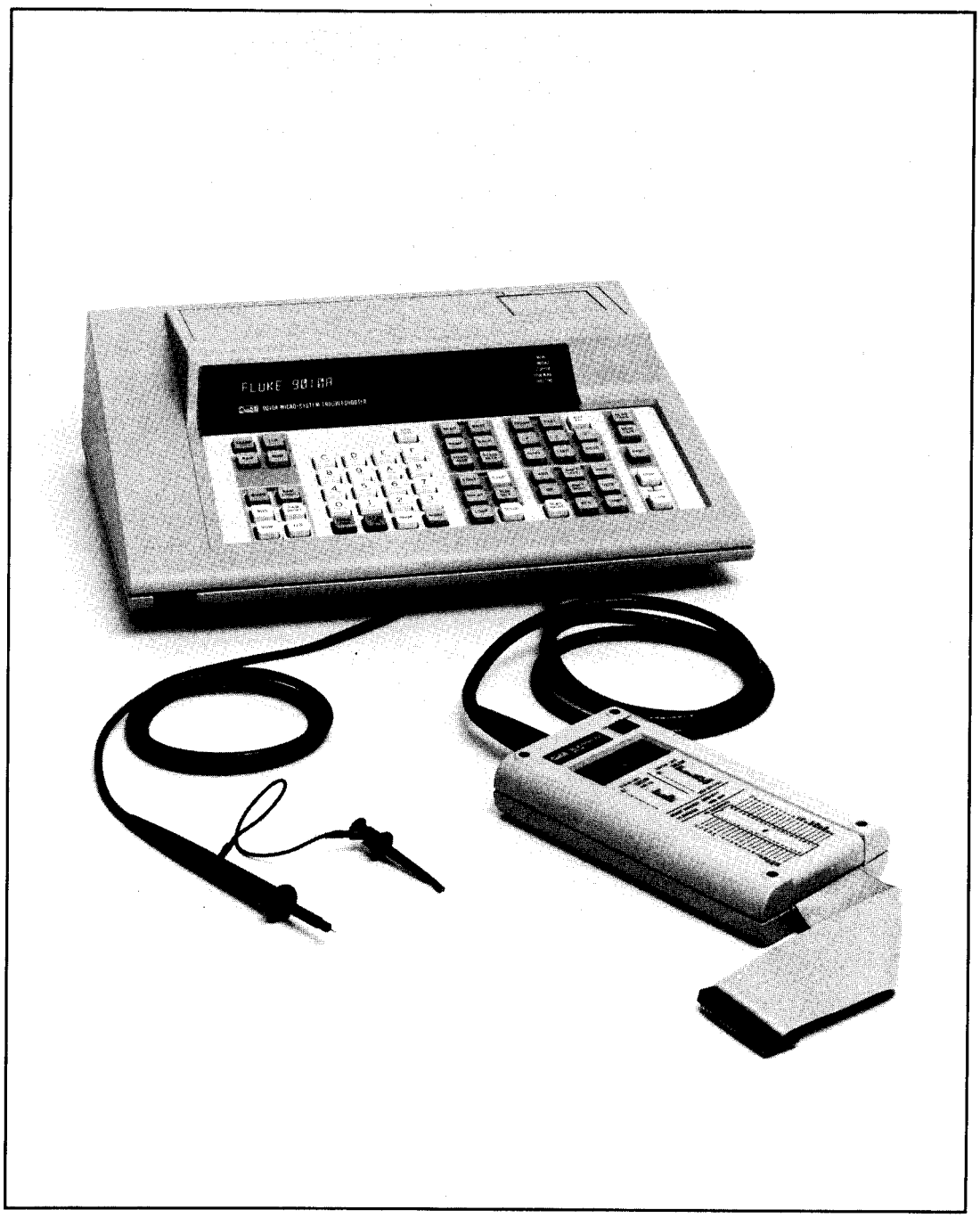
TABLE OF CONTENTS, *continued*

List of Tables

List of Illustrations

(continued on page vii)

LIST OF ILLUSTRATIONS, *continued*



9010A Micro-System Troubleshooter

Section 1
Introduction

1-1. THE 9010A INSTRUCTION MANUAL SET

The 9010A Micro-System Troubleshooter is documented by a set of four manuals: Operator, Programming, Service, and a Reference Guide. The manuals provide the following information:

OPERATOR	Instrument description and specifications, operating instructions including test and troubleshooting techniques, probe use, execution of programs, options and accessories, and routine maintenance by the operator.
PROGRAMMING	Description of instrument programming capabilities, writing, editing, and execution of programs. Little or no previous programming experience required.
SERVICE	Specifications, theory of operation, troubleshooting, repair and maintenance information, a list of replaceable parts, and schematics. Intended for use by a qualified technician.
REFERENCE GUIDE	Quick-reference operating and programming information.

In addition, an Interface Pod Manual is provided with each interface pod. This manual contains the following information:

INTERFACE POD	Specifications, theory of operation, maintenance, a list of replaceable parts, and schematics.

1-2. ORGANIZATION OF THE 9010A OPERATOR MANUAL

The 9010A Operator Manual is divided into the following sections:

1	INTRODUCTION	Introduces the 9010A Instrument Manual Set, describes the 9010A and its features, and lists the instrument specifications.
2	SHIPPING AND SERVICE	Includes information about shipping, line voltage selection, and line fuse and probe fuse replacement.
3	TECHNICAL OVERVIEW	Provides an introduction to the 9010A operating philosophy, and provides illustrations and descriptions of the main instrument, probe and pod. Includes an illustrated description of all the keys on the keyboard and the corresponding operating features.

4 DETAILED OPERATING INFORMATION	Includes detailed operating instructions and information about preparation of 9010A and the UUT, error detection, tests, troubleshooting and operating functions, probe and oscilloscope applications, and cassette tape operation. Accompanying display messages are also provided.
5 OPTIONS AND ACCESSORIES	Provides a description of the RS-232 Interface Option and the accessories available for use with the 9010A.
APPENDICES A, B, C, D, AND E	Provide a list of default values for operations a table of ASCII characters, an alphabetical list and brief description of all display messages, and a list of Fluke Technical Service Centers and Sales Representatives.

1-3. INSTRUMENT DESCRIPTION

The 9010A Microsystem Troubleshooter is a portable service instrument for testing and troubleshooting microprocessor-based equipment. The 9010A provides the following features:

- Keyboard selection of functions and operating modes.
- 32-character display for presentation of test results, operator messages, and prompts.
- Single-keystroke validation of electrical integrity of μP bus.
- Learn function for mapping UUT address space and identifying RAM, ROM, and I/O.
- Comprehensive, functional testing of RAM, ROM, and I/O.
- Nine troubleshooting functions for troubleshooting on or off the bus.
- On-line programming for development of system test and fault isolation programs.
- Consistent prompts and defaults for easy selection and specification of operations
- Detailed error messages for locating UUT failures.
- Dual-function stimulus/response probe for generating bus-synchronized pulses or gathering signatures, counting events, and detecting logic levels.
- Hexadecimal keyboard for data entry.
- Sixteen 32-bit internal registers for storage and manipulation of data.
- Built-in cassette recorder for nonvolatile storage and transfer of test programs and data on minicassettes.
- Optional RS-232 port for remote communication.
- Optional interface pods for interfacing with the following microprocessors: 8080, 8085, Z80, 6800, 6502, and 9900 - with more interface pods to come.

- UUT (unit under test) microprocessor emulation for execution of UUT program code.
- Rear-panel scope trigger output that is synchronized to UUT microprocesor bus events.

The 9010A, shown in Figure 1-1, consists of the main instrument, the probe, and one of the interface pod options. The probe is included with the purchase of the 9010A, and the interface pod option is purchased separately. The stimulus/response probe and interface pod attach to the main instrument by means of cables. The interface pod contains the microprocessor (μP)-dependent circuitry which allows the 9010A to interface with a particular μP-based UUT. The interface pod allows the 9010A to gain access to the UUT (unit under test) by plugging into the μP socket on the UUT. The interface pods, listed in Table 1-1, are described separately in individual manuals.

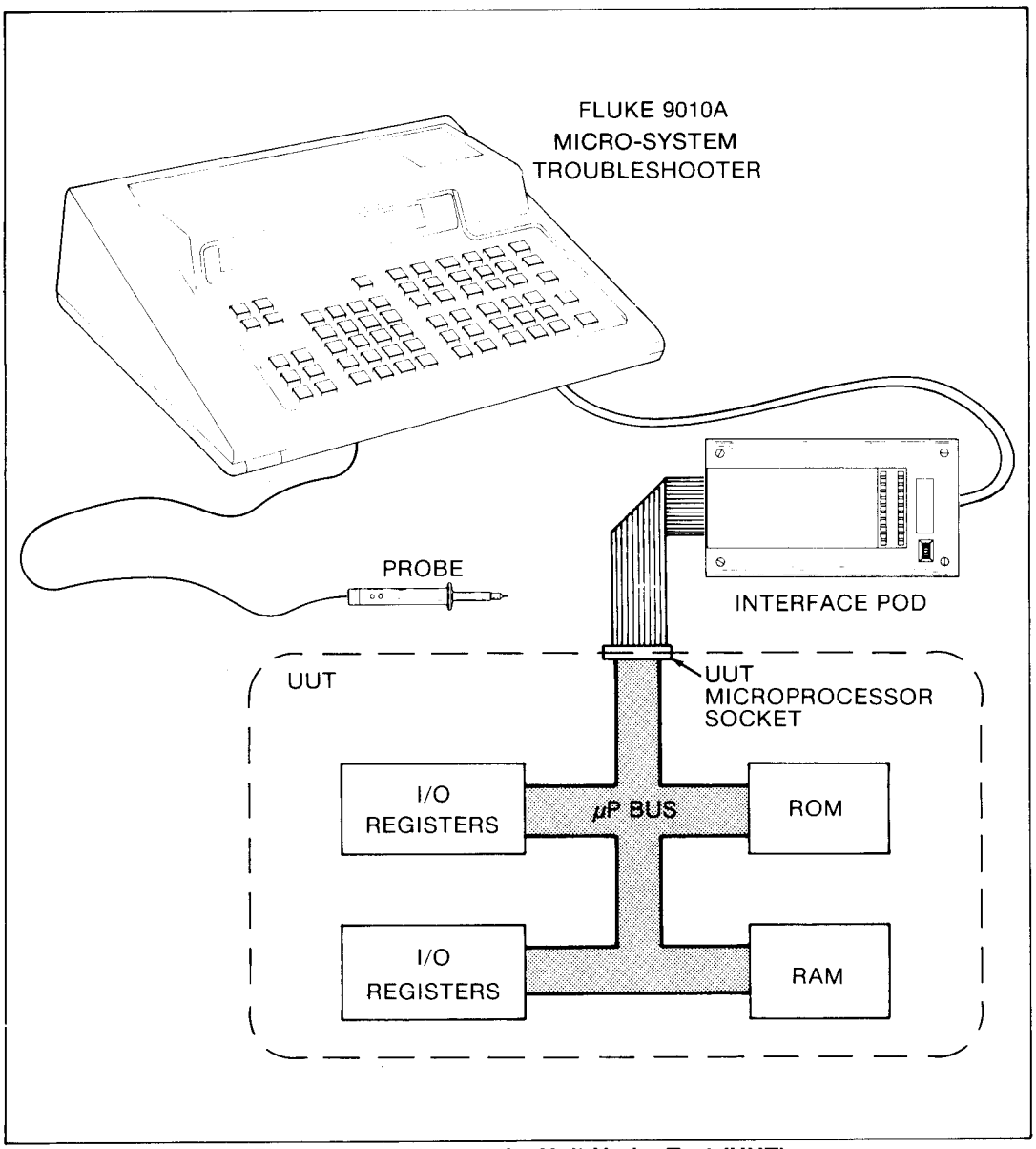


Figure 1-1. 9010A and the Unit Under Test (UUT)

Table 1-1. 9010A Options and Accessories

OPTION/ MODEL NO.	DESCRIPTION
	Accessories
9000A-900	Transit Case
Y8007	Cassette Tapes
	Options
9010A-001	RS-232-Auxiliary Interface
9000A-6502	6502 Interface Pod (8-bit) } Documented separately in individual manuals.
9000A-6800	6800 Interface Pod (8-bit)
9000A-8080	8080 Interface Pod (8-bit)
9000A-8085	8085 Interface Pod (8-bit)
9000A-Z80	Z80 Interface Pod (8-bit)
9000A-9900	9900 Interface Pod (16-bit)
	Additional Interface Pods being developed.

Through the μP socket, the 9010A gains access to all hardware connected to the UUT μP bus, including the address, data, status, and control lines. The 9010A can test or exercise all hardware connected to the UUT μP bus. In addition, the 9010A can emulate the UUT μP.

The main instrument contains the keyboard and display and is housed in a durable plastic case. The main instrument, the probe, and an interface pod fit into a rugged carrying case that is sold as an accessory. The carrying case allows safe, convenient storage during transportation.

Operating power for the 9010A may be selected for one of the following configurations: 100, 120, 220, or 240V ac ±10%; 50 or 60 Hz ±5%. The unit is shipped in the configuration specified at the time of purchase. The voltage selection may be changed in the field by a qualified technician. Instructions about voltage selection are provided in Section 2.

1-4. OPTIONS AND ACCESSORIES

A list of available options and accessories for the 9010A is presented in Table 1-1. The Option 9010A-001 is described in Section 5 of this manual, along with available accessories. The optional interface pods are described separately in individual manuals.

1-5. SPECIFICATIONS

The specifications for the 9010A are provided in Table 1-2. Table 1-2 includes a brief description of the keyboard functions. A more complete description of the keyboard functions is provided in Section 3C, and detailed operating information is provided in Section 4.

Table 1-2. 9010A Specifications

MICROPROCESSOR SUPPORTED	8080, 8085, Z80, 6800, 6502, 9900 (Each requires a separately purchased interface pod; additional interface pods are being developed)
DISPLAY	32 character, 14 segment alphanumeric with decimal points.
KEYBOARD FUNCTIONS	
Data Entry	16-Key hexadecimal keyboard (0 through 9, A through F) for entering data.
ENTER/YES	Used for terminating expressions, responding to questions.
CLEAR/NO	Used for terminating expressions, responding to questions, deleting unwanted input.
Mapping UUT Memory	
LEARN	Locates and identifies RAM, and I/O read-write registers. Computes ROM signatures and identifies read/writable I/O bits.
Viewing UUT Memory	
VIEW RAM, VIEW ROM, VIEW I/O	Allows viewing or editing of UUT address space information.
Functional Tests	
BUS TEST	Checks electrical integrity of UUT microprocessor bus.
ROM TEST	Computes ROM signature and compares to specified ROM signature.
I/O TEST	Checks read-write capability of I/O registers.
RAM SHORT	Quick test for hard RAM errors.
RAM LONG	Comprehensive test of RAM for locating "soft" errors.
AUTO TEST	Performs in sequence BUS TEST, ROM TEST, RAM SHORT and I/O TEST.
Troubleshooting Functions	
READ	Reads from UUT at an operator-specified address and reports value read.
WRITE	Writes operator-specified data to an operator-specified UUT address.
RAMP	Writes a binary incrementing pattern to an operator-specified UUT address.
WALK	Writes a rotating operator-specified bit pattern to the data lines at an operator-specified UUT address.
TOGGL DATA	Toggles an operator-specified data bit at a UUT address from one binary logic state to the other.
TOGGL ADDR	Toggles an operator-specified UUT address bit from one binary logic state to the other.

Table 1-2. 9010A Specifications (cont)

Troubleshooting Functions (cont)	
READ STS	Reads and displays the values of the UUT microprocessor status lines.
WRITE CTL*	Writes operator-specified values to control lines on the UUT microprocessor bus.
TOGGL DATA CTL	Toggles an operator-specified control line from one binary logic state to another.
Mode Controls	
CONT	Continues an interrupted operation (operations are typically interrupted to report errors).
STOP	Halts current 9010A operation.
RPEAT	Repeats the previously performed 9010A operation once.
LOOP	Continuously performs the previous operation.
RUN UUT	Executes UUT program code beginning at an operator-specified address.
Editing	
MORE	Advances display to next line of information or next program step.
PRIOR	Scrolls display to previous line of information or prior program step.
Test Sequencing	Eight functions for entering or executing programs, and creating program messages, branches and loops.
Arithmetic	Eight functions for performing arithmetic on numeric quantities and manipulating data in registers.
Selecting UUT-Specific Operations	
SETUP	Allows the operator to select specific 9010A error detection and operating features to meet the requirements of a particular UUT.
Cassette Tape Operations	
READ TAPE	Reads information from cassette tape into 9010A memory.
WRITE TAPE	Writes information from 9010A memory onto cassette tape.
Probe Controls	
SYNC	Allows specification of probe synchronization to UUT bus events.
HIGH and LOW	Control generation of stimuli by the probe.
READ PROBE	Gathers response information at probe tip and displays signature, logic state history, and event count.

Table 1-2. 9010A Specifications (cont)

RS-232 Interface Option Control	
AUX I/F	Controls transfer of data over RS-232 Interface (if installed).
CASSETTE TAPE	Minicassettes store UUT memory map information, Setup parameters, and programs. Minicassettes type: Verbatim.
PROBE	
General	Single-point stimulus and response probe.
STIMULUS	Pulse high, low, or high and low.
RESPONSE	Signature computation, logic states detected, event count.
Stimulus Mode	
STIMULUS PULSE WIDTH	
Address or data-valid Sync	Equals address-valid or data-valid interval of the interface pod μP.
Free-run	2 μsec nominal.
STIMULUS PULSE AMPLITUDE	
High	>4V at +100 mA
Low	<0.2V at -100 mA
Response Mode	
INDICATOR THRESHOLD	
Logic High (Red)	>2.4V
Logic Low (Green)	<0.8V
Logic Tristate	<2.4V and >0.8V
INDICATOR THRESHOLD ACCURACY	±0.2V
INDICATOR MINIMUM PULSE WIDTH	
Logic High	>75 ns
Logic Tristate	>100 ns
Logic Low	>75 ns
Maximum Safe Input Voltage at Probe Tip	-30V dc to +30V dc
Probe Fuse	The ground clip used with the probe is protected by a series-connected fuse located adjacent to the probe connector. A blown fuse is sensed by the 9010A and reported by a message on the display.

Table 1-2. 9010A Specifications (cont)

9010A OPERATOR-ACCESSIBLE MEMORY	
Tape-Transferable Memory	Approximately 12k bytes for storage of UUT memory map information, Setup parameters, and programs. Contents may be transferred to and from cassette tape or transferred to and from a remote device via the RS-232 Interface Option.
Registers	Sixteen 32-bit registers, 7 dedicated to storage of operating parameters, 9 non-dedicated.
GENERAL	
Power Requirements	100, 120, 220 or 240V ac ±10% 50 or 60 Hz ±5% 40 Watts maximum
Size	11.7 x 38.7 x 31.1 cm. (H x W x L) (4.6 x 15.25 x 12.25 in.) See Figure 1-2.
Weight	5 kg. (11 lb.)
Environmental	
STORAGE TEMPERATURE	
Without Cassette Tape	-40 to +70°C (RH < 95%)
With Cassette Tape	+4 to 50°C (10% to 90% RH)
OPERATING TEMPERATURE	
Without Cassette Tape	0 to 25°C (RH <95%) 25 to 40°C (RH < 75%) 40 to 50°C (RH < 45%)
With Cassette Tape	10 to 25°C (20% to 80% RH) 25 to 30°C (20% to 73% RH) 30 to 35°C (20% to 49% RH) 35 to 40°C (20% to 32% RH) *NOTE: all relative humidity (RH) conditions are non-condensing*

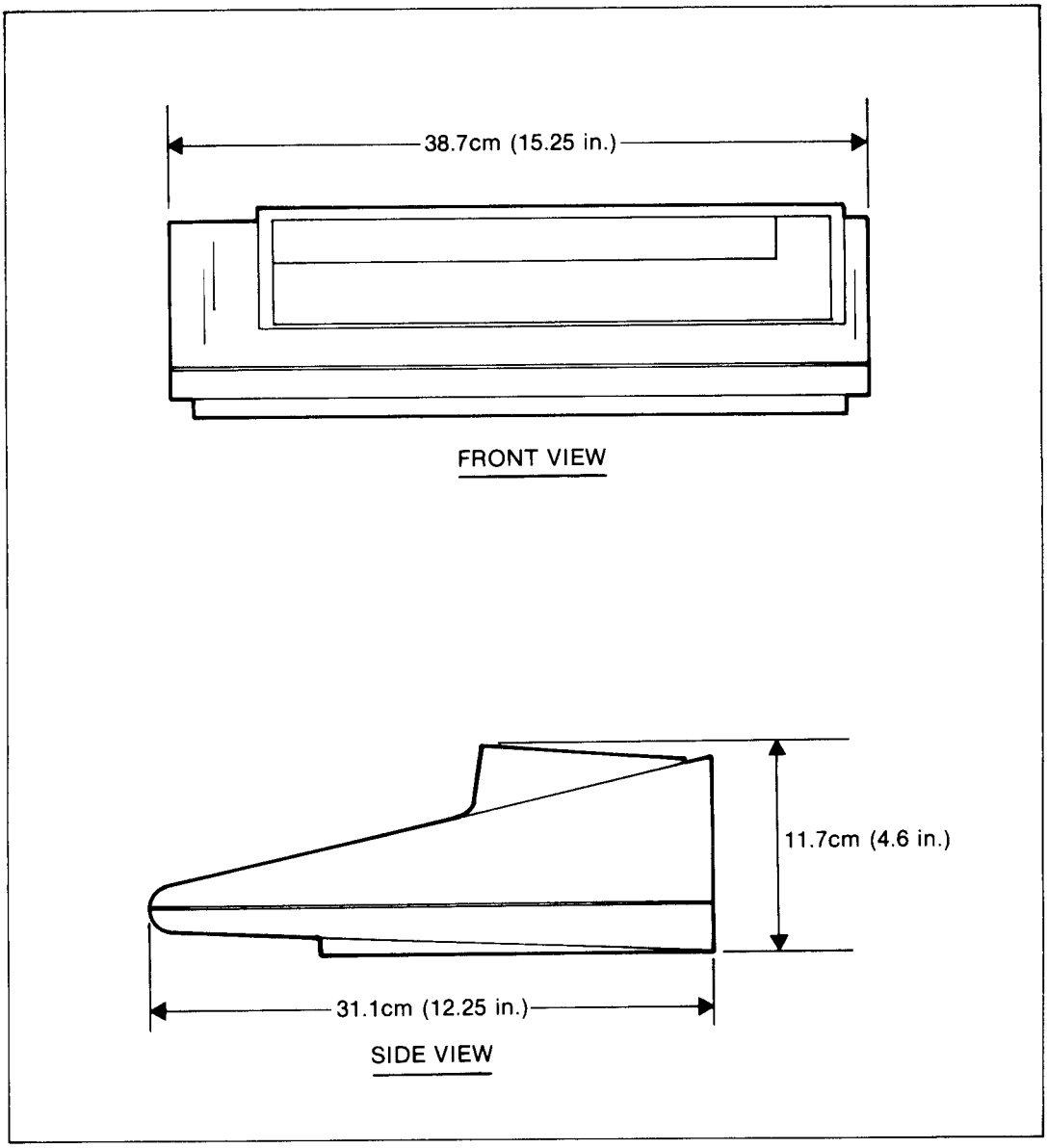


Figure 1-2. 9010A Outline Drawing

Section 2
Shipping and Service

2-1. SHIPPING INFORMATION

The 9010A is packaged and shipped in a foam-packed container. When you receive the 9010A, inspect it thoroughly for possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If reshipment is necessary, use the original container. If the original container is not available, order a new container from John Fluke Mfg. Co., Inc.; P.O Box C9090, Everett, WA 98206; telephone (206) 342-6300.

2-2. LINE FUSE REPLACEMENT

The line fuse (F1) is located in a recessed compartment in the rear panel. Line fuse replacement is illustrated in Figure 2-1. To replace the fuse, proceed as follows:

1. Remove the power cord from the instrument.

2. Slide the clear plastic panel up to expose the fuse compartment.

3. Pull up the plastic lever (as Shown in Figure 2-1) to slide the fuse out of the compartment.

Replace the fuse with one of the proper rating:

For 100 or 120V ac, 1 amp fast-blo (John Fluke #369819)

For 220 or 240V ac, 1/2 amp fast-blo (John Fluke #153858)

2-3. LINE VOLTAGE SELECTION

The 9010A may be operated with a 100, 120, 220, or 240V ac ±10% (250V ac maximum), 50 or 60 Hz ±5% input power line. Any one of the four line voltages may be selected.

The line voltage selection should only be changed by a qualified technician. The line voltage selection is changed by removing and reinserting the voltage selection card. The voltage selection card is inserted into a slot next to the line fuse in the compartment recessed in the rear panel (see Figure 2-2). As a safety precaution, the power cord and the line fuse must be removed to allow access to the voltage selection card. The voltage selection card may be inserted into its slot in any one of four ways, corresponding to the four available line voltages. To change the line voltage, do the following:

1. Remove the line fuse.

2. Using a pair of needlenose pliers (see Figure 2-2), pull the line voltage card straight out.

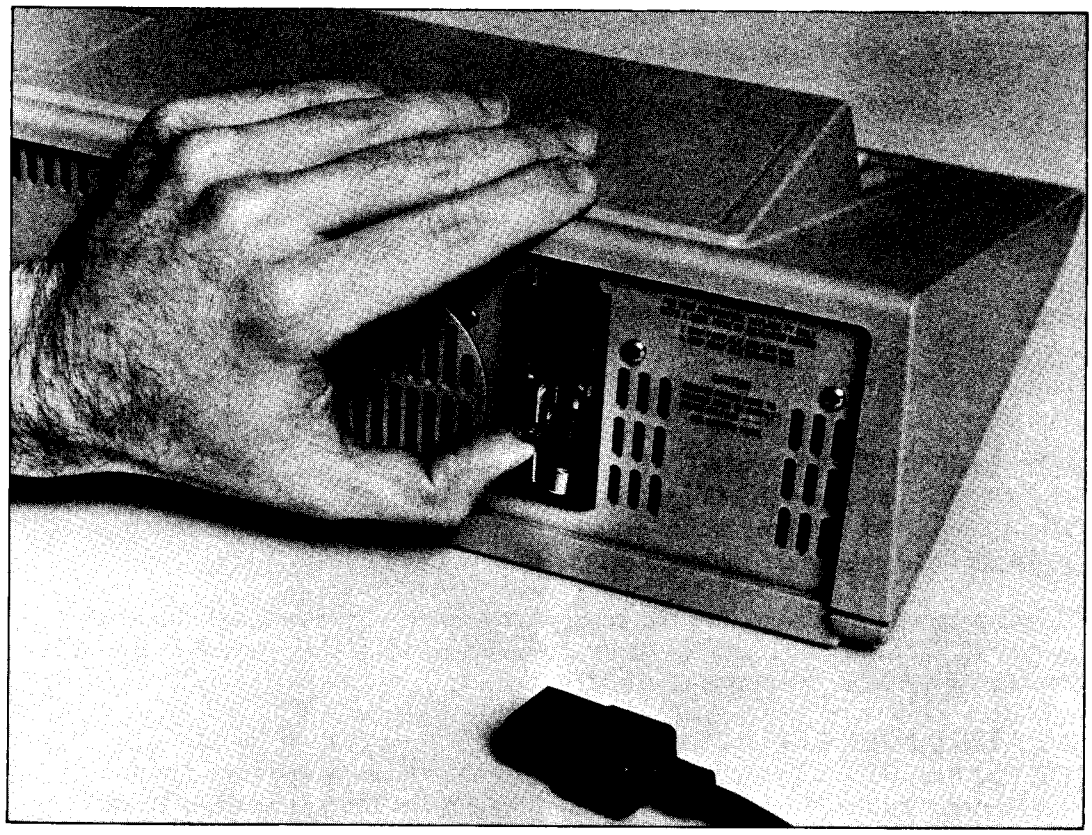


Figure 2-1. Line Fuse Replacement

3. Turn the card and insert it into its slot so that the value of the desired line voltage is the upper value facing the fuse slot. In Figure 2-2, the card is oriented to select 120V.

2-4. PROBE FUSE REPLACEMENT

The 9010A is able to detect when the probe fuse has failed. When this occurs, any operation in progress is interrupted, and the following message is displayed:

REPLACE PROBE FUSE/UNPLUG PROBE

This message prompts the operator to unplug the probe cable or replace the probe fuse. If this message appears, the operator will be unable to initiate any activity with the keyboard until the probe fuse is removed or the probe cable in unplugged. After the proble cable is unplugged or the probe fuse is replaced, the 9010A continues whatever operation was in progress when the blown fuse was detected. The probe fuse is accessible from the front of the instrument, and is located directly under the keyboard to the left of the probe cable connector (see Figure 2-3).

To replace the probe fuse, proceed as follows:

1. Tilt up the front of the instrument and locate the probe fuse-cap.

2. Remove the fuse-cap by turning it 1/8 turn counterclockwise with a screwdriver. The fuse will pull out with the fuse-cap.

3. Replace the fuse with a 1/4-amp fuse.

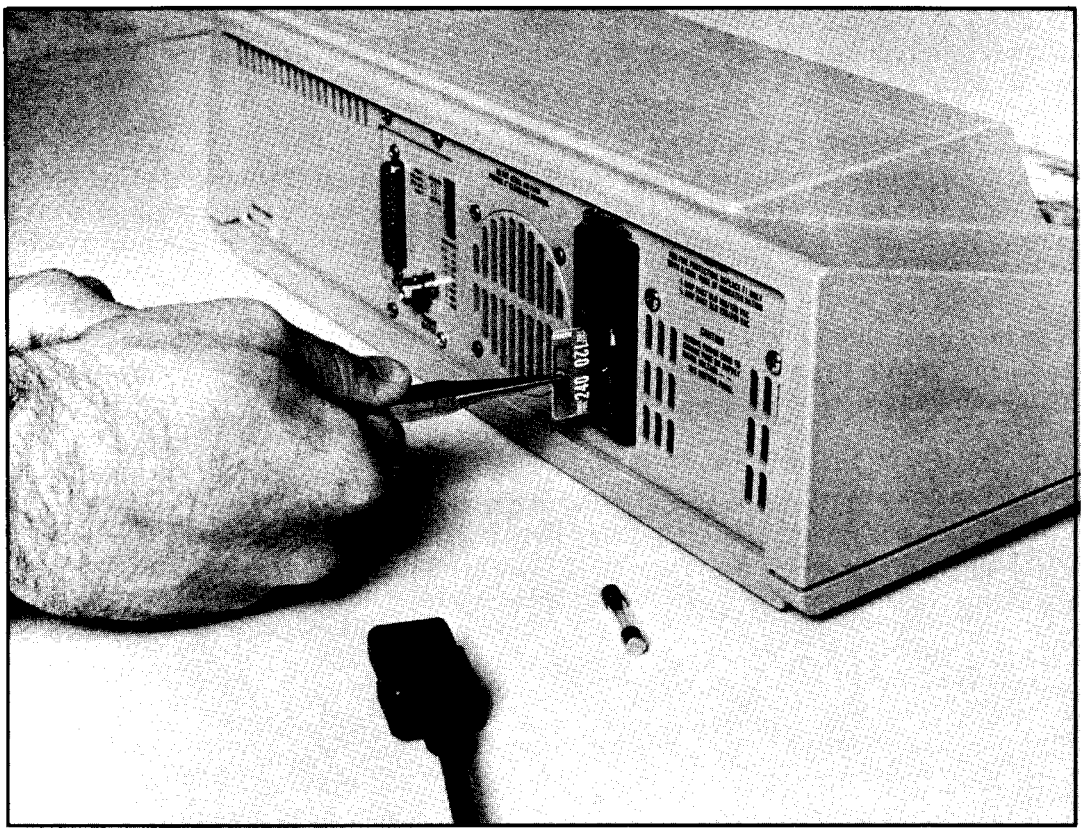


Figure 2-2. Changing the Line Voltage

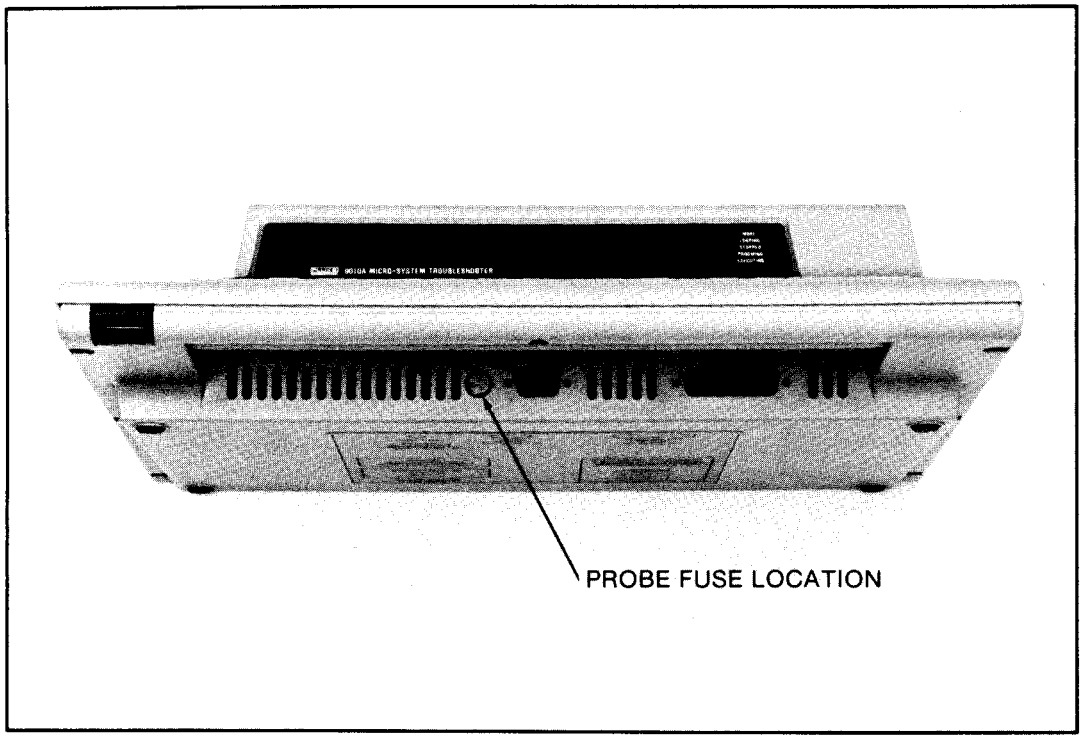


Figure 2-3. Probe Fuse Location

For U.S.A. models, the proper fuse is John Fluke #109314. European models have a slightly different fuse holder and require John Fluke #543504 (European-style fuse, 5 mm by 20 mm).

2-5. TAPE HEAD CLEANING

After a period of use, iron oxide may build up on the tape head. The tape head is the metal bar embedded in the white plastic block that is visible when the tape enclosure is open. Normally the tape head is bright silver in color, but appears dark brown or gray when covered with iron oxide.

The tape head should be kept clean to ensure proper operation. To clean the tape head, moisten a cotton swab with isopropyl alcohol and brush the tape head until all the iron oxide is removed.

2-6. QUESTIONS/PROBLEMS

For additional information, contact your nearest John Fluke Sales Representative (see Appendix E), or the John Fluke Mfg. Co., Inc. at the address and telephone number provided in paragraph 2-1.

Section 3
Technical Overview

This section of the manual provides an overview of the 9010A. Section 3A presents the 9010A view of the UUT and the communication between the UUT and the 9010A. Section 3A also includes an introduction to the 9010A operating philosophy. Section 3B provides a description of the instrument and the internal memory. Section 3C provides a description of the operating features available on the 9010A keyboard. It also includes a description of the function of each key.

Section 3A
The 9010A View of the UUT

3A-1. INTRODUCTION

The interaction between the 9010A and the UUT is based on the capability of a μP to read or write data at an address. Unlike other digital troubleshooting or testing equipment, such as logic analyzers or signature analyzers, the 9010A does not gather information in the time-domain. Through the UUT connection at the UUT μP socket, the 9010A actually takes control of the UUT μP bus and allows the operator to specify read and write operations anywhere in the UUT address space. All of the 9010A operations are derived from this fundamental ability to manipulate data at an address.

The 9010A uniformly views all microprocessors that have up to 32 bits of address and data. In addition to the 32 bits of address and data, the 9010A views the UUT μP as having the following:

- Up to 16 status lines that may be read by the operator. Status lines are defined as inputs to the μP, such as reset or interrupt lines.

- Up to eight control lines that may be explicitly written by the operator and up to eight more that may not be explicitly written by the operator. Control lines are defined as outputs from the μP to the μP bus, such as read enable or write enable lines.

Information about the actual addresses, data size, status lines, and control lines for each μP is supplied to the 9010A main instrument by the interface pod, and is documented in the appropriate interface pod manual. Note that regardless of the nomenclature used by the manufacturer of the UUT μP, the 9010A regards bit 0 as the low order bit (Least Significant Bit) and bit 31 as the high order bit (Most Significant Bit).

3A-2. COMMUNICATION BETWEEN THE 9010A AND THE UUT

The communication between the 9010A (also called 'main instrument' in this manual) and the UUT is shown in Figure 3A-1. Access to the UUT is provided by the interface pod and the probe. The probe may be applied to the UUT to stimulate or read data from logic nodes on the UUT.

The main instrument is designed to be used with any μP. The μP-dependent features of the 9010A are provided by the interface pod that is designed for each particular μP. The interface pod contains a μP of the same type that it replaces in the UUT.

When the main instrument and the interface pod are connected to the UUT, the digital activity normally provided by the UUT μP is provided by the 9010A. The 9010A can take control of the UUT μP bus to exercise and test ROM, RAM, I/O, and all other circuits

interfaced to the bus. The 9010A can also emulate the UUT μP and execute the program code from the UUT memory.

The 9010A can obtain and store information classifying the UUT μP address space into ROM addresses, RAM addresses, and I/O register addresses. The 9010A can determine and store information about the read-write capability of bits in I/O registers, and can compute and store characteristic ROM signatures for blocks of ROM. A ROM signature is a four-digit hexadecimal number that is a shorthand representation of the data contained in an area of ROM memory. In addition to computing ROM signatures, the 9010A is also able to compare UUT ROM signatures with expected ROM signatures and report discrepancies.

The UUT clock is supplied to the interface pod μP, which allows the interface pod μP to execute operations on the UUT μP bus at the speed intended by UUT design. The UUT power supplied at the UUT μP socket does not provide operating power for the interface pod μP. The entire interface pod, including the μP, receives operating power from the 9010A main instrument. However, the interface pod monitors the UUT power supplied at the UUT μP socket and reports to the main instrument if the UUT power fails.

In addition to the address, data, status, and control lines, the 9010A also tests the UUT timing and bus handshake lines. The timing and bus handshake lines are tested to ensure that they can be driven by the μP, even though the operator may not explicitly write to these lines.

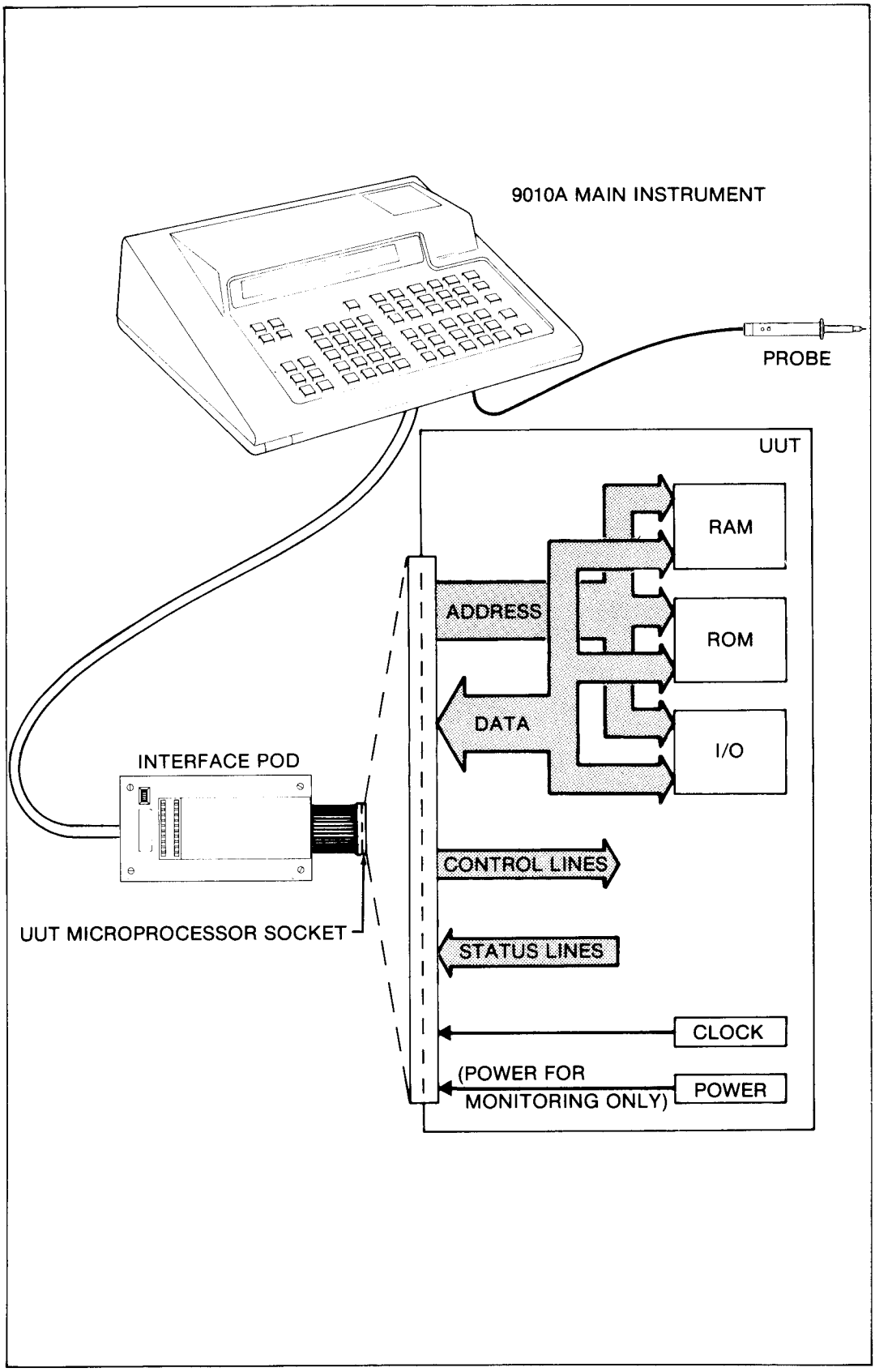


Figure 3A-1. Communication Between the 9010A and the UUT

Section 3B
Main Instrument, Pod, and Probe

3B-1. INTRODUCTION

This section provides a description of the 9010A main instrument, the interface pod, and the probe. It also includes a description of the 9010A internal memory.

3B-2. MAIN INSTRUMENT

The primary external features of the main instrument are shown in Figures 3B-1, 3B-2, and 3B-3. The main instrument contains the keyboard and display along with the master logic, control circuitry, and internal memory.

A built-in cassette recorder allows nonvolatile storage and transfer of test programs and other data on minicassettes. A rear panel TRIGGER OUTPUT enables the operator to synchronize an oscilloscope with UUT bus events while testing or troubleshooting with the 9010A. An optional rear panel RS-232 port allows the 9010A to communicate with remote devices.

Operation and programming of the 9010A is accomplished using the front panel keyboard. An overview of the operating and programming features is provided in Section 3C.

The display is capable of displaying up to 32 characters. If single line messages are longer than 32 characters, the first 32 characters of the message are displayed. The remainder of the message may be scrolled horizontally onto the screen using the MORE and PRIOR keys as described in Section 3C. Multi-line messages may also occur during 9010A operation, and are brought to the display using the same keys.

Five LED annunciators are located to the right of the display. They provide information about the 9010A display and operating modes. When flashing, they indicate the following:

- MORE. Additional message lines exist and may be summoned with the MORE key. The MORE LED is not turned on when the visible line requires scrolling, since the truncated text on the display indicates more text is available.
- LOOPING. The 9010A is recurrently executing some action.
- STOPPED. The STOP key has been presssed and an operation that was being executed has been discontinued.
- PROGMING. The 9010A is in the Programming Mode.
- EXECUTING. The 9010A is in the Executing Mode.

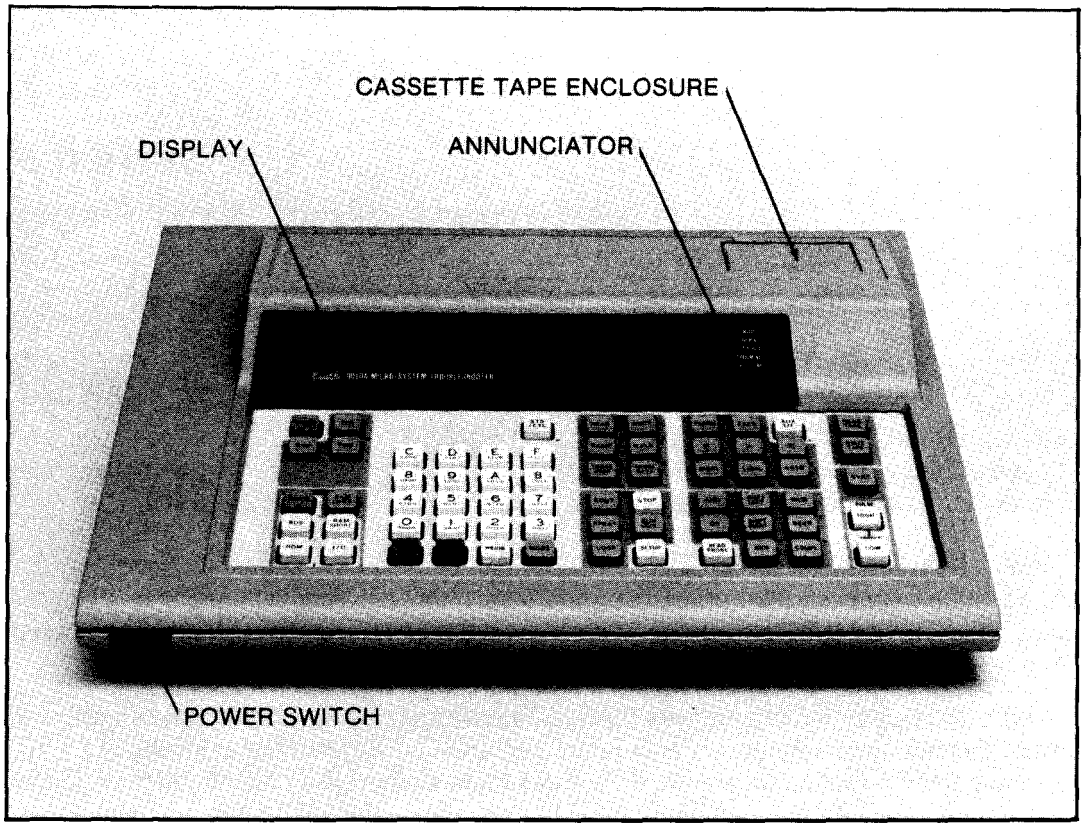


Figure 3B-1. 9010A Front Panel

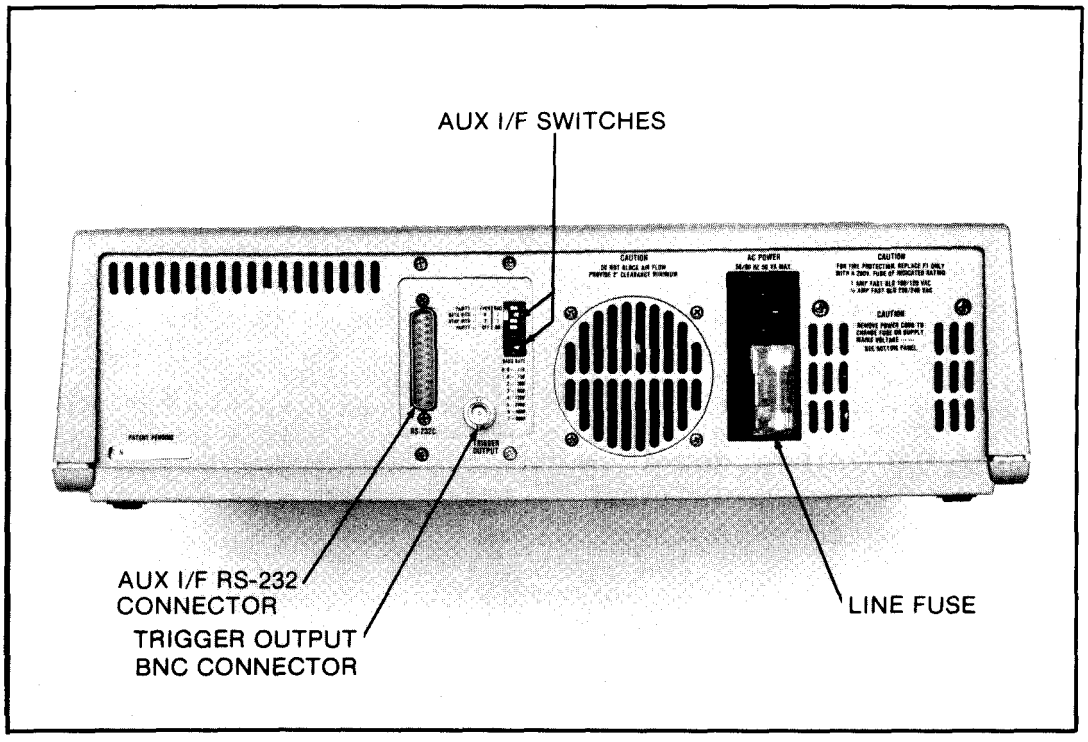


Figure 3B-2. 9010A Rear Panel

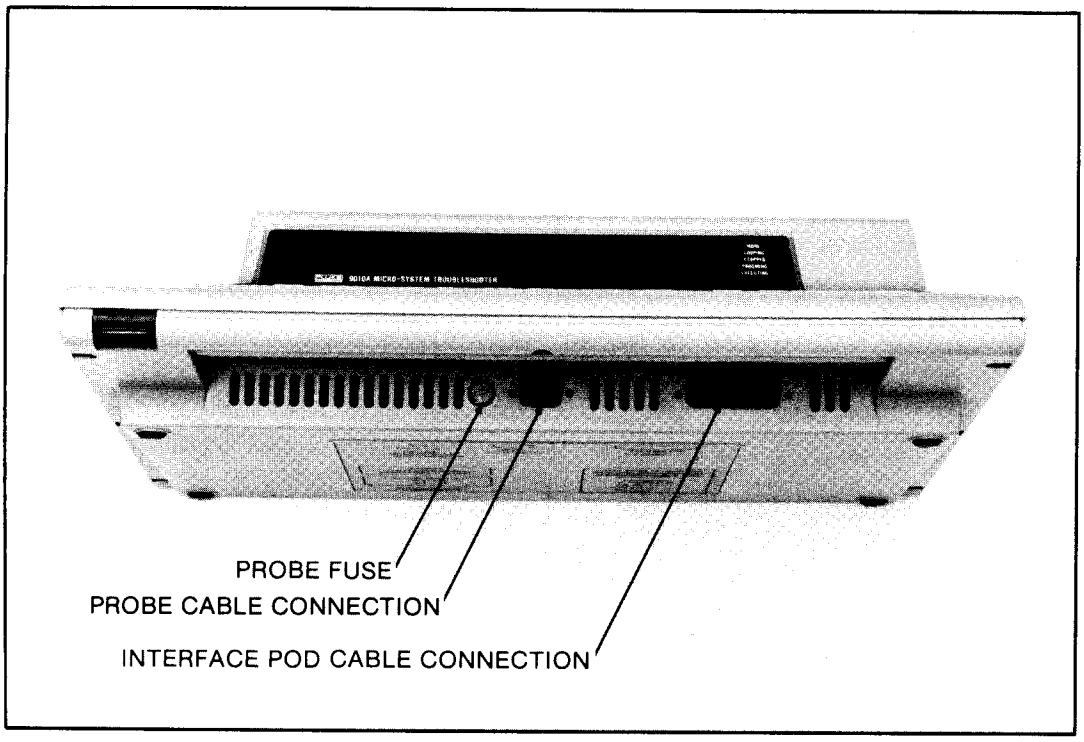


Figure 3B-3. Probe Fuse and Cable Connection

The LOOPING and STOPPED states are mutually exclusive, so the LOOPING and STOPPED annunciators are never flashing simultaneously. Similarly, the Programming and Executing operating modes are mutually exclusive, and the PROGMING and EXECUTING annunciators are never flashing simultaneously. Operating modes are described in Section 4C.

3B-3. INTERFACE POD

The main instrument is designed for use with any μP. The μP-dependent features are provided by the interface pod that is designed for each particular μP or μP family.

The external features of the interface pod are illustrated in Figure 3B-4. The interface pod attaches to the main instrument with a 5-foot cable and to the UUT with a short ribbon cable. A plug at the end of the ribbon cable plugs into the μP socket on the UUT. Each interface pod has a decal which provides information about the μP address assignments, pin assignments, and status and control line functions.

The interface pod has a self-test capability. The plug on the end of the interface pod ribbon cable may be inserted into a self-test socket on the interface pod. When the BUS TEST key is pressed, the result of the self test appears on the display. The self-test socket also provides a convenient place to carry and protect the interface pod plug when not installed in a UUT.

Instructions for installing the interface pod in the UUT and performing the self test are provided in Section 4B. For information about the specifications and operation of a particular interface pod, refer to the appropriate interface pod manual.

3B-4. PROBE

The probe is illustrated in Figure 3B-4. It attaches to the main instrument with a 6-foot cable. The probe shell contains two indicator lights, one red and one green, which indicate

logic levels and events counted. Both alligator and pin-grabber ground clips are provided with the probe. The ground clip screws into the probe shell and should be used to connect the probe to UUT ground during use.

CAUTION

The probe ground clip MUST be connected to UUT ground when the probe is used as a pulser and connection to UUT ground is recommended at other times.

The probe is used to locate faults on the UUT. It provides both stimulus and response functions that may be selected by the operator. Stimulus functions include the generation of high or low pulses for stimulating particular nodes on or off the UUT μP bus. Response functions include logic level detection, event counting, and signature computation.

The timing of probe stimulus or response functions may be free-running or synchronized with the address-valid or data-valid time periods of the UUT μP. This synchronization capability is especially important while troubleshooting μP systems with multiplexed addresses and data. Probe operation is described in Section 4K.

3B-5. 9010A INTERNAL MEMORY

The 9010A provides two areas of internal memory for storage of information useful to the operator. The memory storage is volatile; stored information is lost when power is removed from the 9010A. These two areas of memory are illustrated in Figure 3B-5 and described in the following paragraphs.

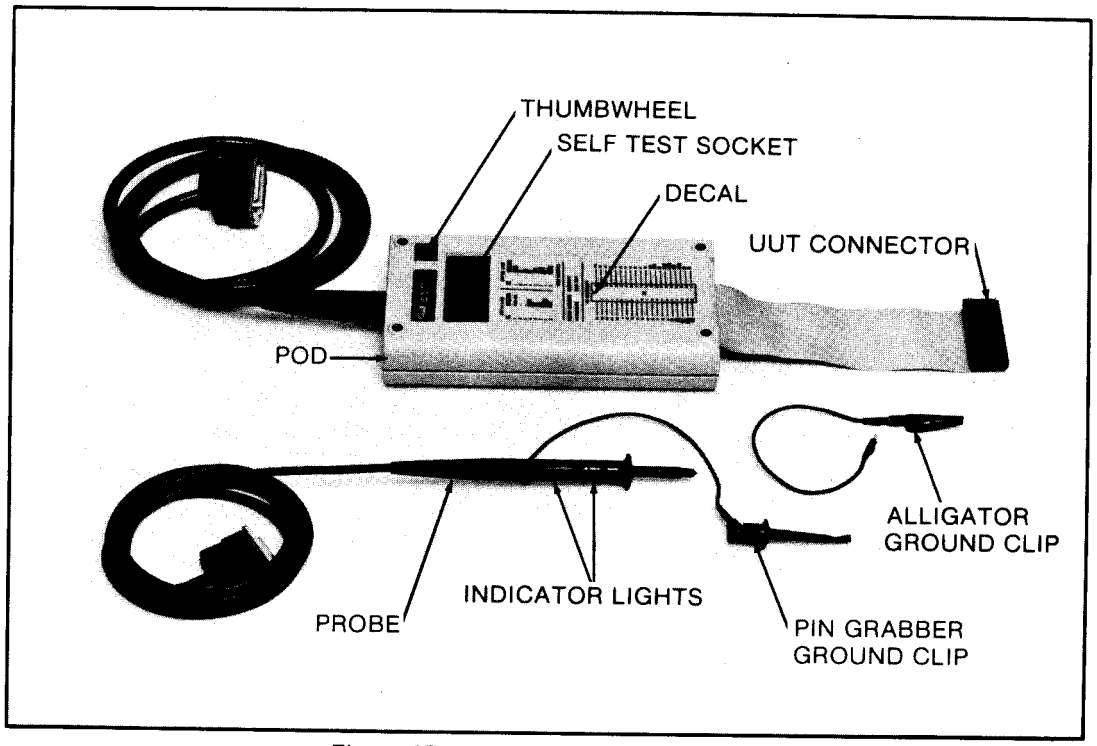


Figure 3B-4. Interface Pod and Probe

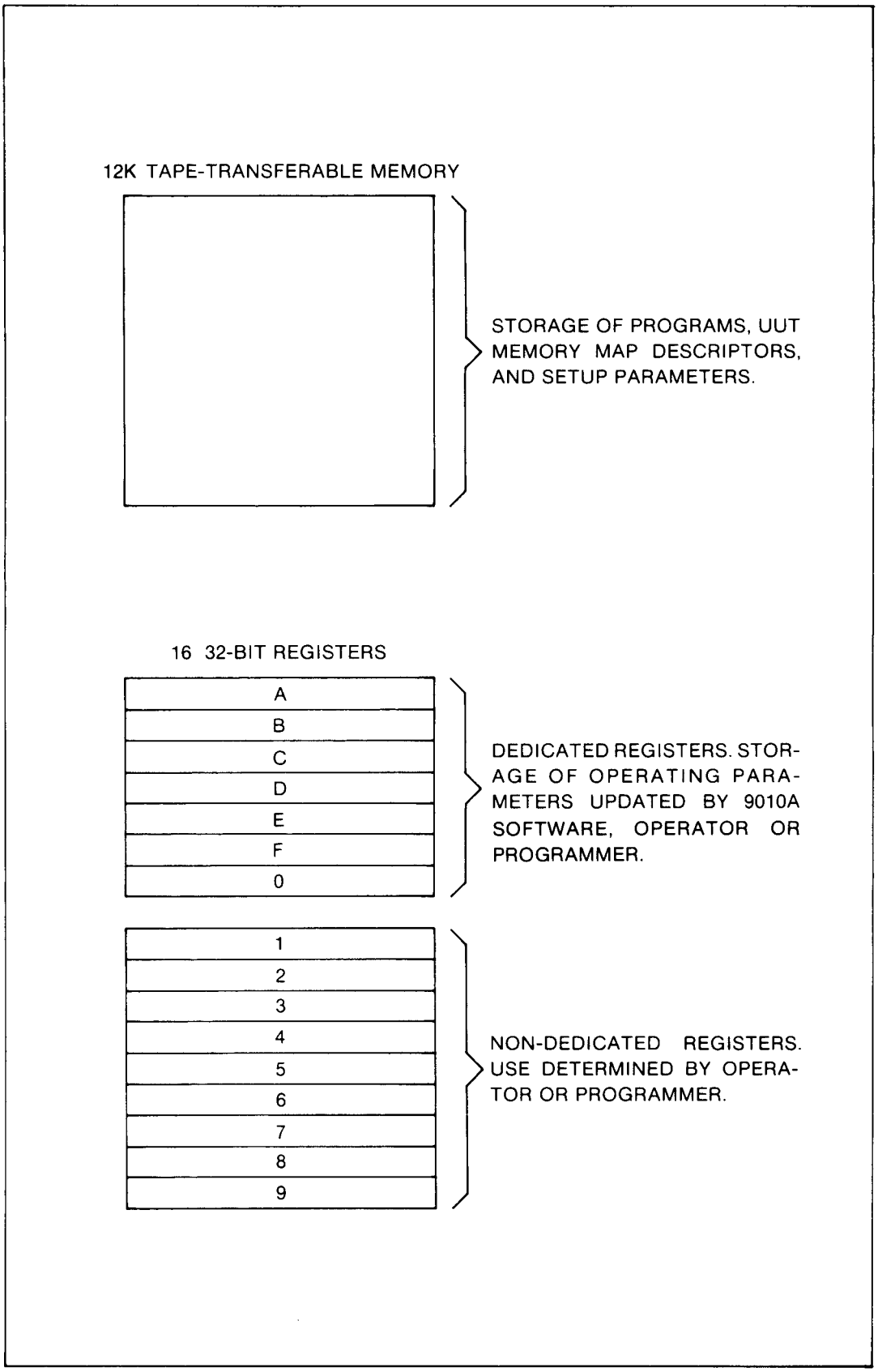


Figure 3B-5. 9010A Internal Memory

3B-6. Tape-Transferable Memory

The first area of memory consists of 12K bytes of tape-transferable memory; (note that in this manual, a byte is defined as equaling eight bits). Information may be written to or read from this area on minicassette tapes. This information may also be sent to remote devices or received from another 9010A. There are three kinds of information that may be stored in this area:

1. Programs that may be executed by the 9010A.

2. UUT address space descriptors obtained through the Learn operation or entered by the operator with the VIEW keys.

3. Setup parameters.

3B-7. Internal Registers

The second area of memory consists of sixteen 32-bit registers. As shown in Figure 3B-5. the registers are labeled 0-9 and A-F. Seven of the registers are dedicated for use by the 9010A software (and may also be used by the operator). Nine of the registers are not used by the 9010A software (non-dedicated), and are available for the sole use of the operator. The entry and manipulation of data within the registers is described in Section 4J.

Register 0 is a dedicated register that is used by the 9010A software to store probe response data obtained during the Read Probe operation. Information stored in Register 0 is described in Section 4K.

Registers A-F are dedicated registers used by the 9010A software to store operating parameters. These registers contain default values supplied by the 9010A when needed during operation. Defaults and default values are described in Section 4E.

Registers 1-9 are non-dedicated registers. The operator may use these registers for temporary storage and manipulation of data during operation. Use of the registers is described in Section 4J. The programmer may incorporate the use of these registers into programs as described in the 9010A Programming Manual.

Section 3C
Keyboard Overview

3C-1. INTRODUCTION

The operator controls all of the 9010A operating, testing, and troubleshooting functions from the main instrument keyboard. Figure 3C-1 provides a list of these functions and indicates the location of the associated keys. The following paragraphs provide brief summaries of the function of each key and provide references to the detailed information available in Sections 4 and 5.

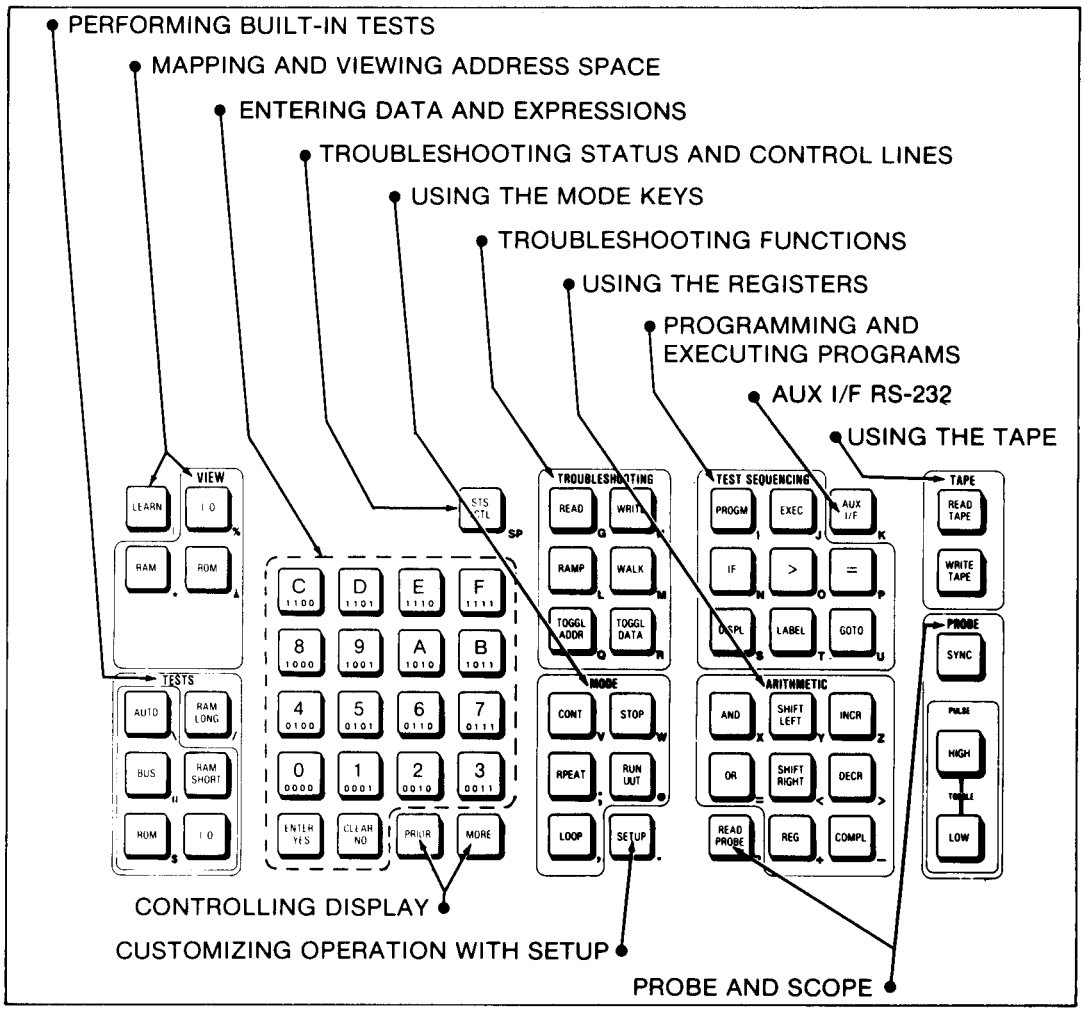


Figure 3C-1. 9010A Keyboard

3C-2. MAPPING AND VIEWING ADDRESS SPACE

The 9010A enables the operator to explore and map the address space of the UUT μP bus. This mapping may be performed automatically by the Learn operation. The Learn operation tests each address location in sequence and identifies it as I/O, RAM, ROM or unassigned. In addition, the Learn operation computes ROM signatures for each block of ROM. It also stores a bit mask for I/O registers specifying which bits have read-write capability. The Learn operation is commonly performed on a properly functioning UUT to provide test parameters that may be stored on cassette tape and used in testing a suspect UUT.

After the Learn operation has been performed, a memory map is stored in 9010A memory describing the assignment of the UUT address space. The VIEW keys may be used to recall and display this memory map. The VIEW keys may also be used to delete, add to, or modify the address space description.

Address space mapping, viewing, and modifying are described in detail in Section 4G. The location of the LEARN and VIEW keys is indicated in Figure 3C-2, and their function is summarized as follows:

- The Learn operation compiles a descriptive memory map of the entire UUT μP address space and stores the map in 9010A memory.
- The I/O View operation recalls the description of UUT I/O address space to the 9010A display and allows viewing or modification of the I/O description.
- The RAM View operation recalls the description of UUT RAM address space to the 9010A display and allows viewing or modification of the RAM description.
- The ROM View operation recalls the description of the UUT ROM address space to the 9010A display and allows viewing or modification of the ROM description.

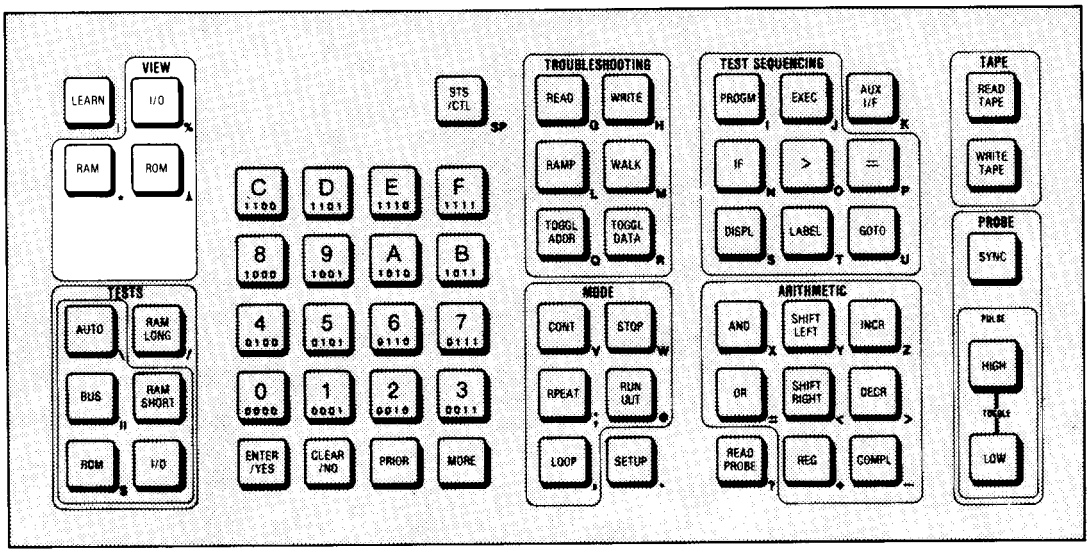


Figure 3C-2. The LEARN and VIEW Keys

3C-3. PERFORMING BUILT-IN TESTS

The 9010A provides six built-in tests that may be performed on the UUT. These tests are performed either on addresses specified by the operator or on the areas of address space for which the 9010A has stored descriptions after the Learn or View operations. These tests are described in detail in Section 4H. The keys are indicated in Figure 3C-3, and the associated functions are summarized as follows:

- The Bus Test tests for proper function of the UUT control lines, data lines, and address lines. It identifies undrivable control lines, data lines held high, held low, or tied together, and address lines held high, held low, or tied together. In each case a display message informs the operator which line or lines are at fault.

- The ROM Test computes a ROM signature for each block of ROM and compares it with the reference ROM signature stored in memory. It reports discrepancies in the ROM signatures and the block of ROM in which the error was detected.

- The I/O Test tests the read-write capability of all bits in I/O registers that are described as having read-write capability by information obtained by the Learn operation or specified by the operator. It reports errors and identifies the I/O address and bit where the error was detected.

- RAM Short tests the read-write capability of each data bit in RAM and the proper function of the data lines and RAM address decoding. Errors are reported and their location is identified.

- Auto Test performs, in sequence, the Bus Test, ROM Test, RAM Short, and I/O Test. Errors are reported and locations are identified as described for the individual tests.

- RAM Long performs all the tests listed for RAM Short, as well as a more elaborate check of address decoding and an elaborate pattern sensitivity test for locating "soft" RAM errors. Errors are reported and their locations are identified.

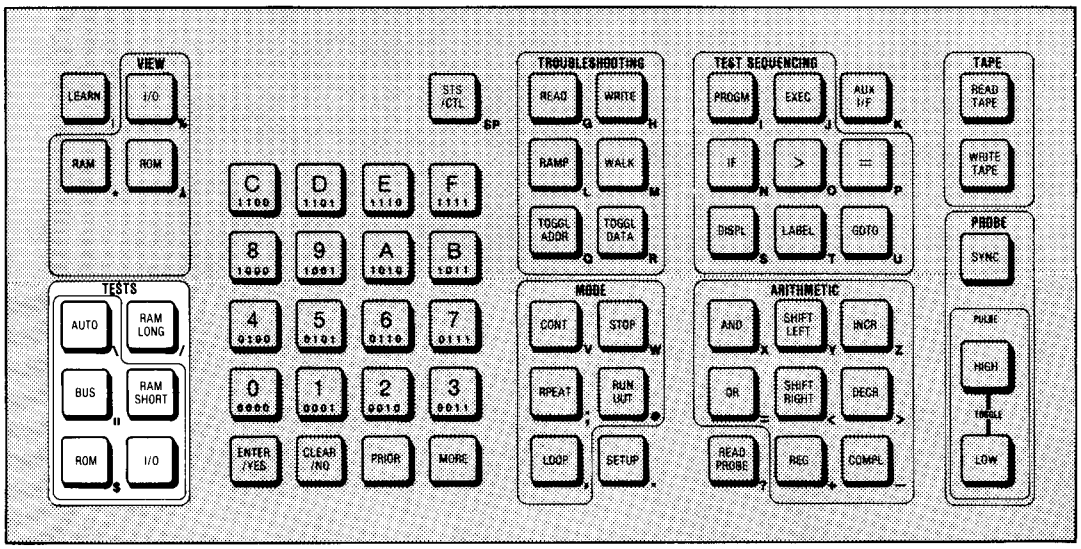


Figure 3C-3. The Test Keys

3C-4. ENTERING DATA AND EXPRESSIONS

Hexadecimal, decimal, or binary data is entered on the 16-key hexadecimal keyboard (0-9, A-F; see Figure 3C-4). Each key is labeled with both hexadecimal and binary values.

The function of the ENTER/YES and CLEAR/NO keys is summarized as follows.

- ENTER/YES is a multi-function key used for terminating expressions or responding to questions appearing on the 9010A display.

- CLEAR/NO is a multi-function key used for clearing entered data or responding to questions appearing on the 9010A display.

The function of the hexadecimal keyboard and the ENTER/YES and CLEAR/NO keys is described throughout Section 4 as need for their use arises during discussion of other functions.

3C-5. CONTROLLING THE DISPLAY

Occasionally, during operation, the 9010A may have information to present to the operator which exceeds the capacity of the 32 character display. This information may consist of a single line message which exceeds 32 characters, or it may consist of a multi-line message. The undisplayed information may be scrolled onto the display using the MORE and PRIOR keys (see Figure 3C-5) as described below:

- MORE shifts a truncated single line message to the left to display the remainder of the line, or advances a multi-line message to the next line in the message.

- PRIOR shifts a truncated single line message to the right or backs up a multi-line message to the previous line in the message.

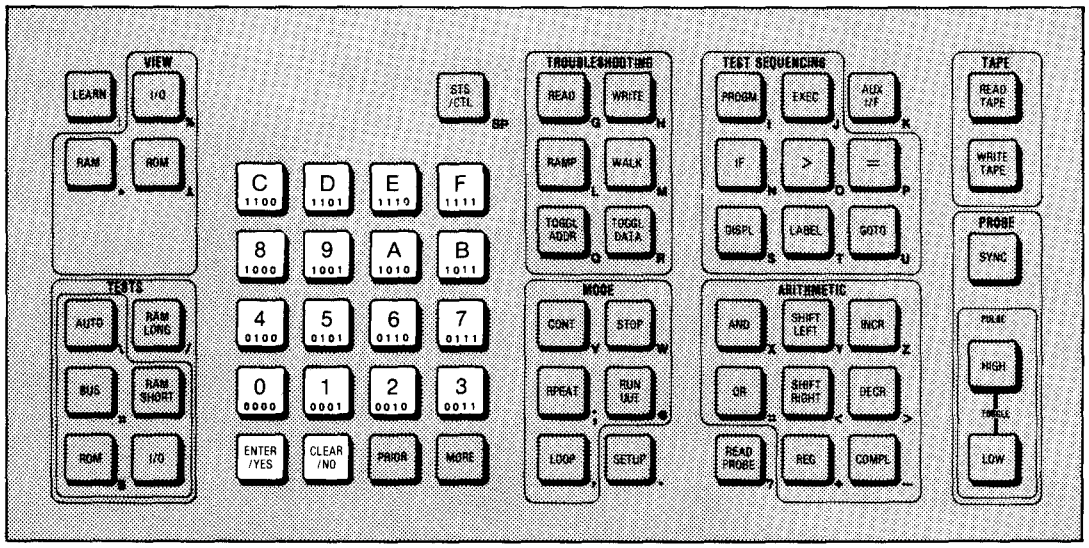


Figure 3C-4. The Hexadecimal Keyboard and the ENTER/YES and CLEAR/NO Keys

When a single line message exceeds 32 characters, the line is truncated at the left. Pressing MORE causes the line to advance eight characters to the left, or until the end of the line is aligned with the right side of the display. Pressing PRIOR backs up the line in a similar manner.

When a multi-line message occurs, the first line is presented on the display and the MORE annunciator flashes. Subsequent lines in the multi-line message may be scrolled onto the display by pressing the MORE key. If subsequent lines are longer than 32 characters, they are truncated at the left when first scrolled onto the display (except in Programming Mode or with the Setup function). This is because more pertinent information in subsequent lines usually occurs at the right side of the line. Pressing the PRIOR key scrolls multi-line messages backward in a similar manner.

An example of the use of the MORE key is shown below. The capital letters correspond to the displayed portion of the message, and the italicized letters correspond to the unseen portion of the message.

If the display is:

SAMPLE LINE LONGER THAN 32 CHARActers
the second line in a multi-line message

Pressing the MORE key obtains:

samplE LINE LONGER THAN 32 CHARACTERS
the second line in a multi-line message

Pressing the MORE key obtains:

sample line longer than 32 characters
the secOND LINE IN A MULTI-LINE MESSAGE

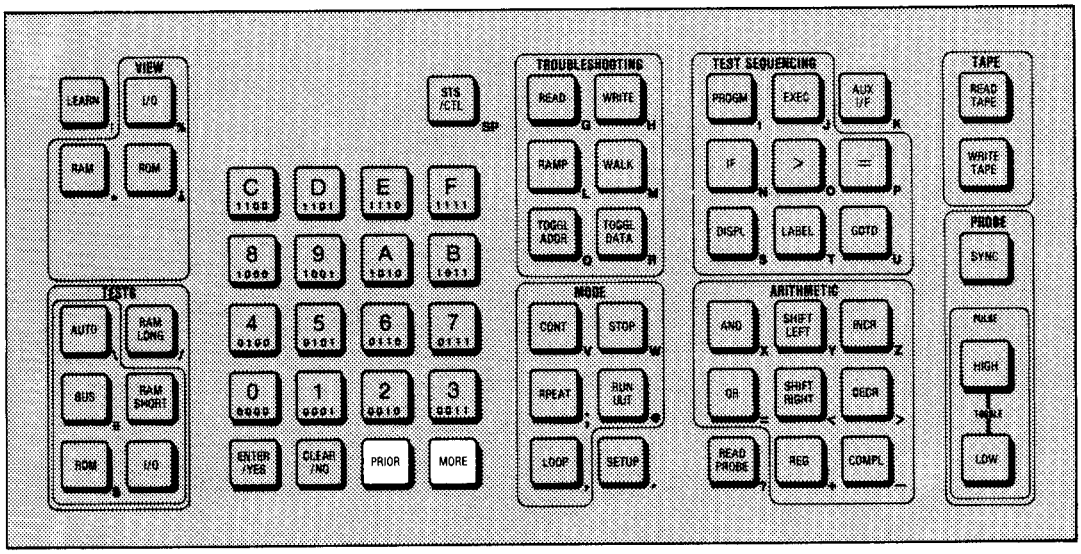


Figure 3C-5. The Display Control Keys, MORE and PRIOR

3C-6. USING THE MODE KEYS

When a particular test or troubleshooting function has been selected and performed, there are several keys which may be used to cause the action to be performed again or stopped. These keys are indicated in Figure 3C-6, and are summarized as follows:

- When looping, the STOP key terminates actions being executed. When already stopped or when performing an operation, pressing the STOP key causes the 9010A to enter the quiescent state.
- The CONT key causes action to continue after the 9010A has interrupted action to report an error that may be looped on (see the LOOP key description).
- RPEAT causes the action previously performed to be repeated once. This allows an operator to save time in repeating operations. An operation may be repeated by a single keystroke, rather than reentering the entire sequence of keystrokes.
- LOOP causes the action previously performed to be repeated continuously. LOOP is particularly useful during troubleshooting. When the 9010A detects an error in the UUT, the 9010A halts any further activity and displays a message to inform the operator an error has occurred. If the operator presses the YES or LOOP key, the 9010A continually repeats the operation during which the UUT error was detected. The operator may then physically manipulate the UUT to locate and remove the cause of the error, while observing the 9010A display or listening for a beep which indicates when the observed error disappears.

The LOOPING LED annunciator flashes while the Loop function is selected. The STOPPED LED annunciator flashes while the 9010A is stopped. RPEAT, LOOP, STOP, AND CONT are further described in Section 4N.

The other key in this group is summarized as follows:

- RUN UUT allows the interface pod μP to execute the program code stored in the UUT. Execution begins at the default address specified by the μP manufacturer or at an address specified by the operator. RUN UUT also allows the operator to indirectly test the UUT μP. This is accomplished by comparing UUT performance with the pod μP in the RUN UUT mode, and UUT performance with the UUT μP. Refer to Section 4N for more information about RUN UUT.

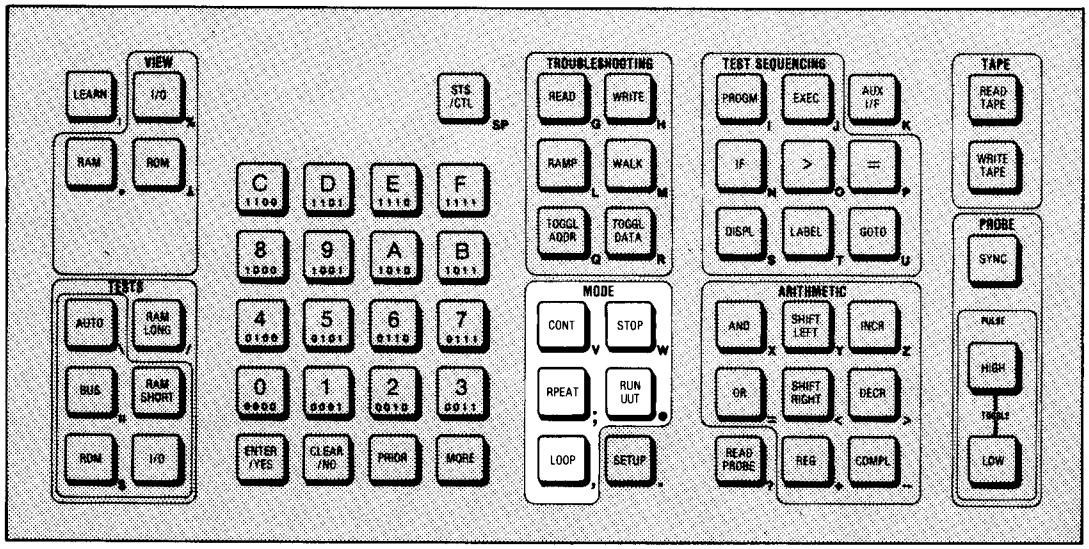


Figure 3C-6. The MODE Keys

3C-7. TROUBLESHOOTING

In addition to the large scale built-in tests which can be performed on large blocks of UUT address space, the 9010A allows the operator to concentrate troubleshooting to particular address locations, bus signals, or devices on the UUT. The troubleshooting function keys are indicated in Figure 3C-7, and their functions are summarized as follows. Refer to Section 4I for more information and for examples of each function.

- The Read function reads an operator-specified location in the UUT μP system and presents the data on the display.
- The Write function writes operator-specified data to an operator-specified location in the UUT μP system.
- The Ramp function performs a series of write operations at an operator-specified location in the UUT μP system. The first write operation in the series writes a zero in all data bits. The numeric value of each successive write operation is incremented by one. The last write operation in the series writes a one in all data bits.
- WALK rotates an operator-specified bit pattern across the data lines at an operator-specified address. This is accomplished by performing a series of write operations. The first write operation writes the operator-specified bit pattern. The 9010A then shifts the bit pattern one bit to the right, wrapping the least significant bit around to the most significant bit position and writes the resulting bit pattern. The 9010A continues to shift and write until the last pattern written is the original pattern shifted left by one.
- TOGGL ADDR toggles an operator-specified address bit from one logic state to the other. This is accomplished by two read operations. The first read operation is performed at the operator-specified address. Then the operator-specified address bit is toggled to its opposite logic state, and a read operation is performed at the resulting address.
- TOGGL DATA toggles an operator-specified data bit from one binary logic state to the other. This is accomplished by two write operations which are performed at an operator-specified address. The first write operation writes the operator-specified data. Then the operator-specified data bit is toggled to its opposite logic state and the 9010A writes the resulting data.

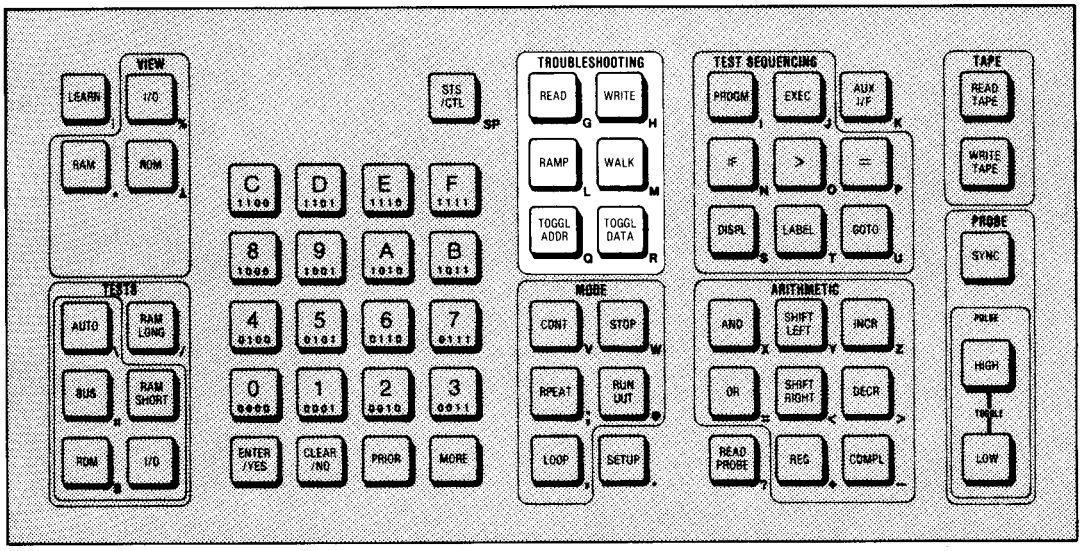


Figure 3C-7. The Troubleshooting Functions Keys

3C-8. TROUBLESHOOTING STATUS AND CONTROL LINES

The STS/CTL key, indicated in Figure 3C-8, allows the operator to troubleshoot UUT μP status lines and control lines. Status lines are defined as inputs to the μP, such as reset or interrupt lines. Control lines are defined as outputs from the μP to the μP bus, such as read enable or write enable lines. The 9010A is capable of handling up to 8 control lines and 16 status lines. The status and control lines for each μP are listed on the interface pod decal and described in the appropriate interface pod manual.

The three STS/CTL troubleshooting functions are invoked by the combined use of the STS/CTL key and the appropriate troubleshooting key. The three functions are summarized as follows. For more information and examples, refer to Section 4I.

- The Read Status function reads the status lines from the μP and presents the information on the display. The Read Status function is useful for monitoring the μP status lines. In programming, for example, the Read Status function may be used to examine a particular status line as a condition in a conditional branch statement.
- The Write Control function writes the control lines to the UUT μP bus. This increases the operator's capability to create desired bus conditions during testing or troubleshooting.
- The Toggle Data Control function toggles an operator-specified control line from one binary logic state to another. This allows the operator to isolate and manipulate any desired control line.

3C-9. CUSTOMIZING OPERATION WITH SETUP

The function of the SETUP key is summarized as follows:

- The Setup function allows the operator to select specific 9010A error detection and operating features to meet the requirements of a particular UUT.

The Setup function does not usually cause any actions to be performed on the UUT, but allows the operator to select desired features which pertain to actions performed by the other 9010A functions. These features include error detection, the start address for performing Run UUT, and many others. The SETUP key is indicated in Figure 3C-8. Information about the Setup function and the list of Setup parameters are provided in Section 4M.

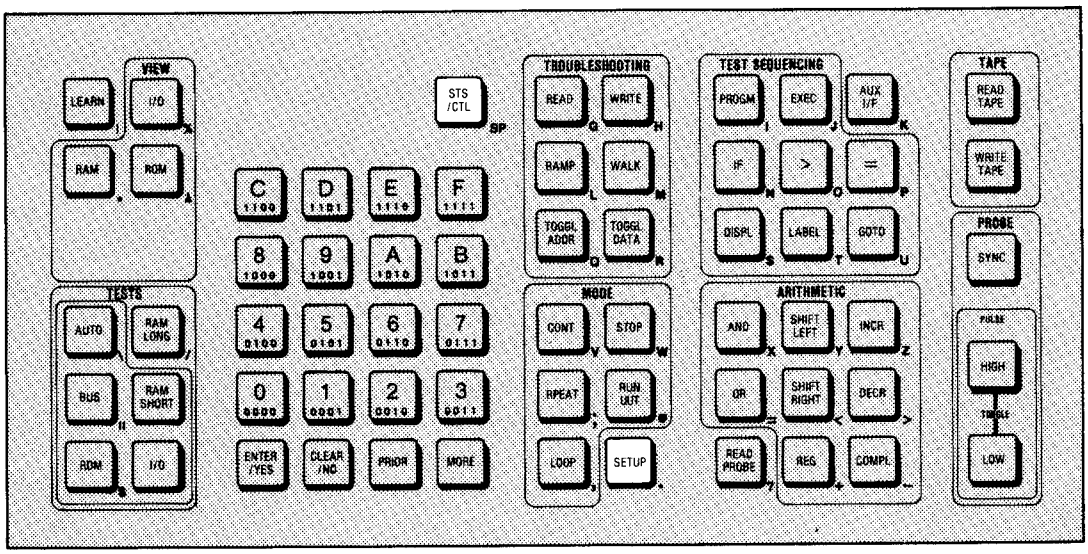


Figure 3C-8. The STS/CTL Key and the SETUP Key

3C-10. USING THE PROBE AND SCOPE TRIGGER OUTPUT

The operation of the probe is controlled by four keys (see Figure 3C-9): SYNC, HIGH, LOW, and READ PROBE. The SYNC key applies to both the stimulus and response modes of probe operation and also applies to the rear panel scope trigger output. The function of the SYNC key is summarized as follows.

- SYNC specifies whether the timing for the scope trigger and the operation of the stimulus or response modes for the probe is unsynchronized (free-running), synchronized to valid addresses on the UUT μP bus, synchronized to valid data on the UUT μP bus, or synchronized to other special μP-dependent timing.

Stimuli generated by the probe are determined by the HIGH and LOW keys. HIGH and LOW are push-push keys which operate together in the following way.

- HIGH In/LOW Out causes the probe to provide high pulses as stimuli.
- HIGH Out/LOW In causes the probe to provide low pulses as stimuli.
- HIGH In/LOW In causes the probe to alternate between high and low pulses as stimuli.
- HIGH Out/LOW Out disables the probe stimulus capability.

The probe is always operating as a response device and is accumulating data about the activity observed at the tip. The logic state at the probe tip is continuously indicated by the red and green indicator lights within the probe shell. Probe response data is made available to the operator with the READ PROBE key. The Read Probe function is summarized as follows.

- The Read Probe function provides accumulated probe data about the logic levels detected, the number of events counted, and the signature computed at the probe tip.

Refer to Section 4K for more information about using the probe and the scope trigger output.

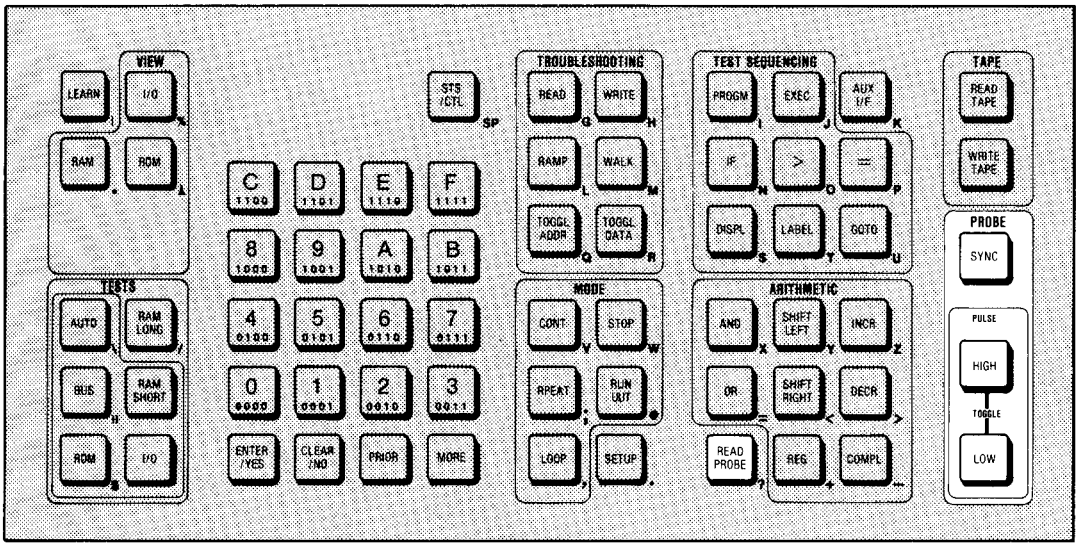


Figure 3C-9. The Probe Control Keys

3C-11. PROGRAMMING AND EXECUTING PROGRAMS

The 9010A provides eight Test Sequencing functions (shown in Figure 3C-10) which aid in constructing or executing programs. The Program function allows the programmer to open or close programs in the Programming Mode, and the Execute function allows the execution of programs stored in 9010A memory. The other six functions include branching, looping, and program step labeling. These six functions are not available in the Immediate Mode, but may only be used in the Programming Mode. Refer to the 9010A Programming Manual for descriptions and examples of their use. Program selection and execution is described in Section 4L of this manual and in the 9010A Programming Manual.

3C-12. AUXILIARY INTERFACE (AUX I/F) OPERATIONS

- AUX I/F allows remote communication between the 9010A and other devices using the RS-232 Interface Option as described in Section 5.

3C-13. REGISTER MANIPULATION

The eight Arithmetic keys (shown in Figure 3C-9) allow the operator to examine, load, and manipulate data within the sixteen 32-bit registers or to specify register contents for data entry. Use of the Arithmetic keys is described in Section 4J of this manual.

3C-14. USING THE TAPE

There are 12K bytes of tape-transferable internal memory that are available for storage of programs, UUT memory map address descriptors (obtained with the Learn or View operations), and Setup parameters. This information may be written to or read from cassette tapes. Tape operation is controlled by two keys (see Figure 3C-10) which are described as follows:

- The Read Tape operation causes the 9010A to read the tape and store its contents. Reading a tape clears any programs, address descriptors, or Setup parameters previously stored in the 9010A.
- The Write Tape operation causes the 9010A to write all programs, address descriptors, and Setup parameters stored in 9010A memory onto the tape. Writing a tape does not disturb the information stored in memory. After the information is written on the tape, the 9010A automatically verifies that the tape contents match the information stored in 9010A memory.

Tape operation is described in Section 4P.

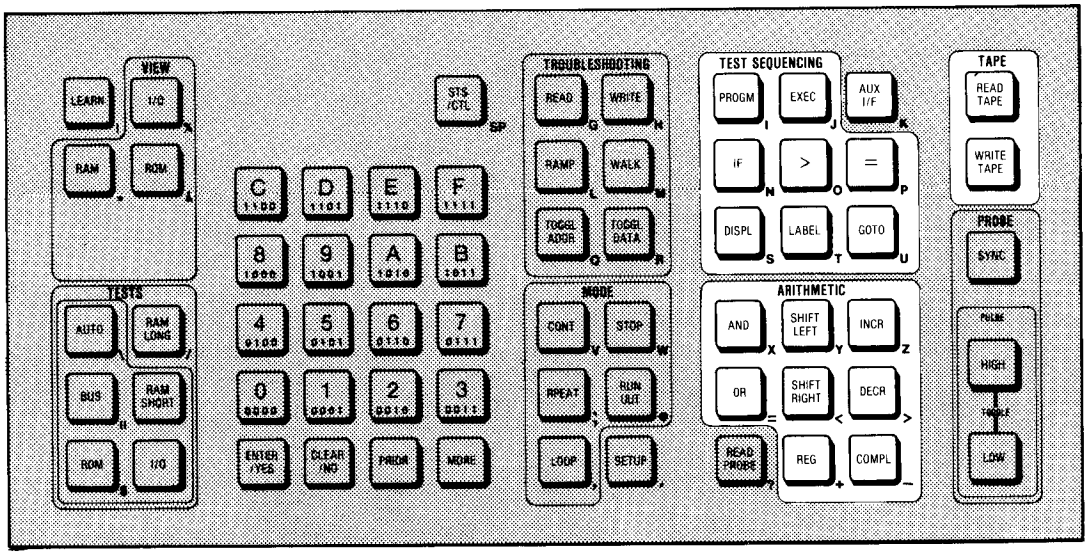


Figure 3C-10. Keys for Programming, AUX I/F, Register Manipulation, and Tape Control

Section 4
Detailed Operating Information

4-1. INTRODUCTION

This section describes the operation of the 9010A. Section 4 is divided into 15 subsections:

4A 9010A PREPARATION
4B UUT PREPARATION AND POD INSTALLATION
4C OPERATING MODES
4D PROMPTS
4E DEFAULTS
4F ERRORS
4G MAPPING AND VIEWING ADDRESS SPACE
4H BUILT-IN TESTS
4I TROUBLESHOOTING FUNCTIONS
4J USING THE REGISTERS
4K TROUBLESHOOTING WITH THE PROBE AND SCOPE
4L TROUBLESHOOTING WITH PROGRAMS
4M CUSTOMIZING OPERATION WITH SETUP
4N USING THE MODE KEYS
4P CASSETTE TAPE OPERATION

The sections are presented in the order in which the operator would expect to encounter them. Sections 4A and 4B describe how to prepare the 9010A and the UUT for operation. Sections 4C, 4D, 4E, and 4F provide an orientation to the operating modes and the 9010A prompt, default, and error detection philosophy. The remainder of the sections provide information about the 9010A tests, functions, and operations, and include examples and applications.

4-2. NUMERIC INPUT AND SYMBOLS USED FOR EXAMPLES

During operation, the 9010A prompts the operator to input different types of numeric data. The 9010A provides consistent cues to the user as to the type of data requested. The data requested may be hexadecimal, decimal, or binary. Note that when decimal values are requested, the 9010A only accepts entry of decimal digits, and does not accept entry of the hexadecimal digits A-F. Likewise, when binary values are requested, the 9010A accepts only entry of binary digits (0 and 1).

The type of numeric input requested during operation is included in the description of the operation of each function in the following sections of this manual. The symbols used in this manual to represent the numeric inputs are summarized in Table 4-1.

Table 4-1. Symbols Used in Examples

TYPE OF INPUT PROMPTED	SYMBOL	RANGE OF VALUES FOR INPUT
Address	*aaaa*	Hexadecimal value in the range 0-FFFFFFFF
Data	*hhhh*	Hexadecimal value in the range 0-FFFFFFFF (The upper limit depends on the interface pod)
ROM Signature	*nnnn*	Hexadecimal value in the range 0-FFFF
I/O Bit Mask	*mmmm*	Hexadecimal value in the range 1-FF (8-bit μp) 1-FFFF (16-bit μp) 1-FFFFFF (24-bit μp) 1-FFFFFFFF (32-bit μp)
Bit Number for: TOGGL DATA	*dd*	Decimal value in the range 0-(n-1) where n= the number of bits in the μp data bus
TOGGL ADDR	*dd*	Decimal value in the range 0-31
TOGGL DATA CTL	*d*	Decimal value in the range 0-7
Program Number	*dd*	Decimal value in the range 0-99

Section 4A
9010A Preparation

4A-1. INTRODUCTION

This section describes how to prepare the 9010A for operation. It includes information about connecting an interface pod, turning on the instrument, and self testing the 9010A and the interface pod.

4A-2. CONNECTING THE INTERFACE POD TO THE 9010A

The interface pod cable plugs into a connector located on the front base of the main instrument under the keyboard. The location of the connector is shown in Figure 4A-1. The cable plug has a sliding metal collar which slides over small metal posts on the connector to lock the plug firmly in place.

To connect the interface pod, follow these steps:

1. Tip up the front of the main instrument to allow access to the connector. This is demonstrated in Figure 4A-1. Be sure 9010A power is off.

2. Slide the metal collar on the cable plug to the left.

3. Plug the cable into the connector and slide the collar to the right so that it locks over the small metal posts on the connector. The plug should now be firmly locked in place.

NOTE

Whenever an interface pod is connected to the 9010A and 9010A power is applied, it is recommended that the BUS TEST key be pressed. This forces a reset on the interface pod and ensures that necessary initial information is sent from the pod to the 9010A. It is also recommended that the Interface Pod Self Test be performed to ensure that the interface pod is operating properly.

4A-3. TURN-ON PROCEDURE

To turn on the instrument, press the green power switch on the front left corner of the instrument. No calibration or warmup time is required.

When the 9010A is first turned on, the internal volatile memory contains no programs and no address descriptors. Setup parameters assume power-on values. When the 9010A is turned off, any stored programs or UUT address descriptors are lost.

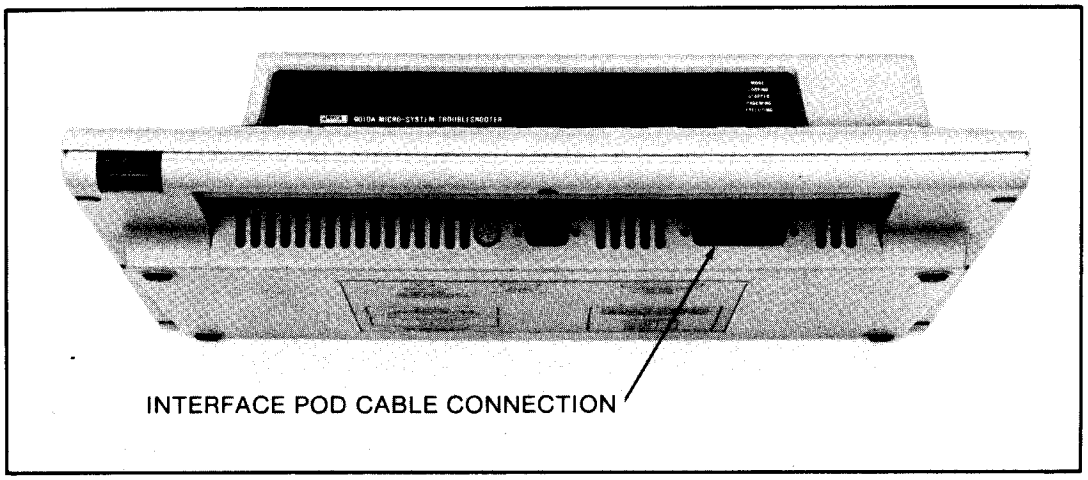


Figure 4A-1. Interface Pod Cable Connection

4A-4. 9010A SELF TEST

When the power is first applied to the 9010A, the following message is displayed:

FLUKE 9000 POWER-UP SELF TEST

The 9010A then performs a self test to verify proper internal operation. If the 9010A is operating properly, the following message is displayed:

FLUKE 9000 POWER-UP OK VER-nn

The letters *nn* represent a number which corresponds to the version of software that is in the 9010A. This number should be specified during any communication with Fluke concerning the instrument.

If the 9010A is not operating properly, after a brief interval, the original self-test message is replaced with the following message:

FLUKE 9000 POWER-UP FAIL mm

where the letters *mm* represent a failure code describing the failure. The failure codes are listed in Table 4A-1. For information about troubleshooting and repairing the 9010A, refer to the 9010A Service Manual.

If the self test fails, repeat the turn-on procedure before contacting your local authorized Fluke Technical Service Center. A list of Service Centers is located in the back of this manual in Appendix E.

The self test may also occur at times other than power-on. The 9010A has a 'watchdog timer' circuit which monitors routine operations in the 9010A and initiates the self test sequence if something appears to be wrong. For example, if a momentary drop in the line power causes the 9010A μP to temporarily malfunction, the monitoring circuit initiates the self test. The self test is identical to the self test performed at power-on, but the messages are slightly different.

The first message displayed is:

FLUKE 9000 RESTARTED SELF TEST

followed by either of these two messages:

FLUKE 9000 RESTARTED OK VER-nn

FLUKE 9000 RESTARTED FAIL mm

After the 9010A is restarted, the memory is intitialized as at power-on, and any stored programs or address descriptors are lost.

4A-5. INTERFACE POD SELF TEST

The interface pod also has a self test. Since the interface pods may operate in an electrically hostile environment, it is recommended that the self test be performed whenever an interface pod is first connected to the 9010A to ensure the pod is operating properly. To perform the pod self test, do the following:

1. Insert the plug at the end of the pod ribbon cable into the self test socket on the interface pod, and turn the thumbwheel to lock the plug in the socket (see Figure 4A-2).

2. Press the BUS TEST key. The 9010A displays one of the following messages:

POD SELF-TEST xxxx OK

POD SELF-TEST xxxx FAIL nn

The letters *xxxx* represent the name of the particular interface pod that is in use (for example, 8080 or 9900). When present, the letters *nn* represent a failure code describing the failure. Refer to the appropriate interface pod manual for an explanation of the failure codes.

Table 4A-1. Self Test Failure Codes

CODE	INDICATED FAILURE
02	RAM failed write FF during power-up
03	RAM failed write FF during restart
04	RAM failed write 00 during power-up
05	RAM failed write 00 during restart
06	RAM failed write FF/00 during power-up
07	RAM failed write FF/00 during restart
08	ROM check failed during power-up
09	ROM check failed during restart
0A	RAM failed write FF and ROM check during power-up
0B	RAM failed write FF and ROM check during restart
0C	RAM failed write 00 and ROM check during power-up
0D	RAM failed write 00 and ROM check during restart
0E	RAM failed write FF/00 and ROM check during power-up
0F	RAM failed write FF/00 and ROM check during restart

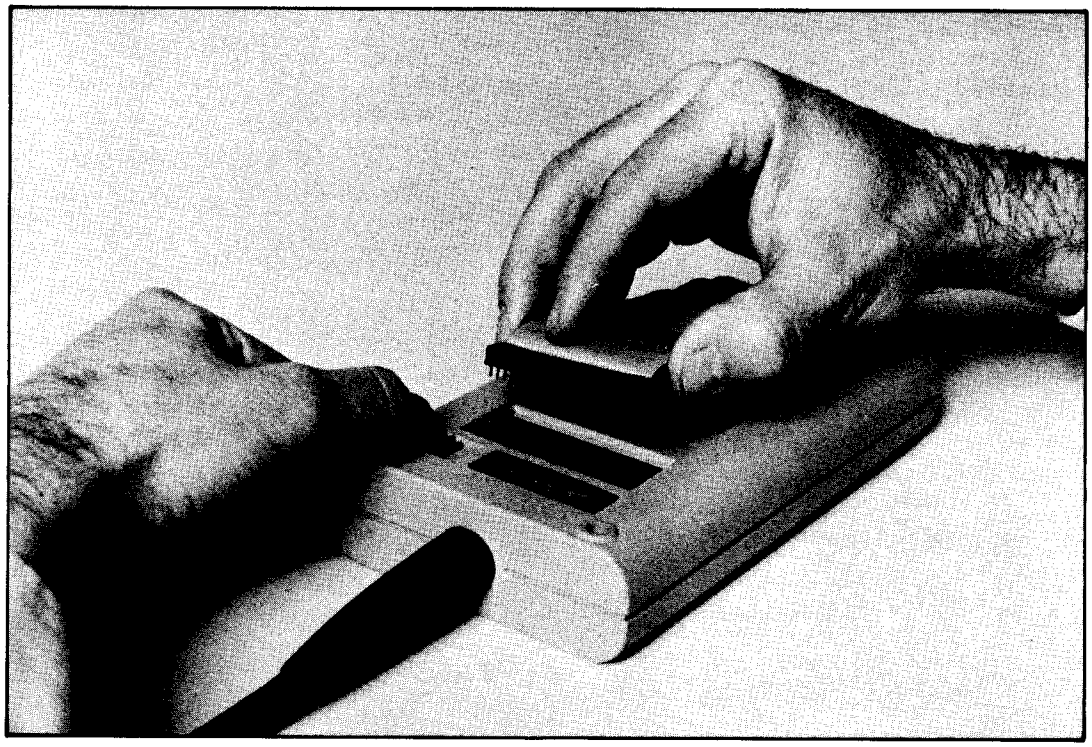


Figure 4A-2. Interface Pod Self Test Connection

Section 4B
UUT Preparation and Pod Installation

4B-1. INTRODUCTION

This section describes how to prepare the unit under test (UUT) for interfacing with the 9010A, and how to install the interface pod in the UUT. It is assumed that the operator is sufficiently familiar with the UUT to follow the pod installation instructions and to avoid the potential hazards as described in this section.

4B-2. UUT PREPARATION

This section describes how to avoid potential operator and instrument hazards when interfacing and operating the 9010A with a UUT.

4B-3. Avoiding Hazards to the Operator, the UUT, and/or UUT Peripheral Devices

Hazards to the operator caused by the UUT should be minimized by the operator's knowledge of the UUT. The operator must be familiar enough with the UUT to avoid potential operator hazards when installing the pod and operating the equipment.

WARNING

TO AVOID ELECTRIC SHOCK AND OTHER HAZARDS TO THE OPERATOR OR DAMAGE TO THE UNIT UNDER TEST (UUT) DO THE FOLLOWING: 1) OBSERVE NORMAL SAFETY PRECAUTIONS FOR OPERATING THE UNIT UNDER TEST 2) REMOVE POWER FROM THE UNIT UNDER TEST AND DISCONNECT HAZARDOUS UUT ANALOG OUTPUTS AND UUT PERIPHERAL DEVICES BEFORE INSTALLING THE INTERFACE POD IN THE UUT; ALL MOTORS, MECHANICAL ACTUATORS, OR THERMAL PRINTHEADS CONTROLLED BY THE UUT MICROPROCESSOR SHOULD BE DISCONNECTED FROM THE UUT 3) BE SURE THAT THE UUT LOGIC COMMON GROUND DOES NOT DEVIATE MORE THAN ±30 VOLTS PEAK FROM EARTH GROUND.

When the UUT μP is replaced by the 9010A, the operator is capable of causing the 9010A to perform a write operation at any address on the UUT μP bus. While this is a tremendous asset when testing and troubleshooting the UUT, the operator must take proper precautions to insure that voltage, heat, mechanical equipment or emanations from the UUT will not create a hazardous condition.

For an example of a potential operator hazard, consider a programmable power supply. If the operator selects and specifies the 9010A Learn operation for the entire UUT μP bus, the 9010A performs write and read operations at every location on the bus. If the digital-

to-analog converter for the output voltages is connected to the bus, a write operation at the d/a converter address could produce unexpected and dangerously high voltages at the output terminal.

For an example of the potential hazard to a UUT or UUT peripheral device, consider a μP-controlled disk drive. If the operator causes the 9010A to perform write operations on the UUT μP bus without removing the output to the disk drive, the 9010A could destroy information stored on the disk by writing random data on the disk.

4B-4. 9010A Overload Protection

The 9010A is designed to operate in electrically hostile UUT environments and to withstand assaults commonly encountered by test equipment, such as electromagnetic interference. The only direct electrical connection between the 9010A and the UUT (except for the probe) is the interface pod which plugs into the UUT μP socket. The interface pod inputs are protected to withstand +12V to -7V, which is more than adequate for potential voltages at the UUT μP socket. This protection generally prevents damage to the UUT or interface pod due to improper insertion of the interface pod plug in the UUT, or installation of the wrong type of interface pod. The probe can withstand inputs of ±30V dc.

4B-5. UUT Power Requirements

The 9010A does not supply any electrical power to the UUT. The operator is responsible for supplying operating power to the UUT while the 9010A is connected. For single or multiple printed circuit boards, this will usually require connecting an external power supply to the board. Power should be removed from the UUT before installing the interface pod.

4B-6. INSTALLATION OF THE POD INTO THE UUT

To install the interface pod into the UUT, use the following procedure:

1. Remove power from the UUT. (The 9010A power should be left on.)

2. Disconnect UUT analog outputs or potentially hazardous UUT peripheral devices as described in Section 4B-3.

3. Gain access to the UUT μP socket and remove the UUT μP. For complex instruments or machinery, this may require mounting the printed circuit board on an extender board or removing the printed circuit board and placing it on a table with connections to a power supply.

4. Turn the pod self-test socket thumbwheel to release the pod plug, and remove the pod plug from the self-test socket.

5. Align the pod plug properly with the UUT μP socket and insert the pod plug into the μP socket as shown in Figure 4B-1. The slanted corner of the pod plug should be aligned with pin 1 of the μP socket.

CAUTION

Be sure that 9010A power is on before turning on UUT power in order to activate input protection circuits within the pod.

6. Apply power to the UUT.

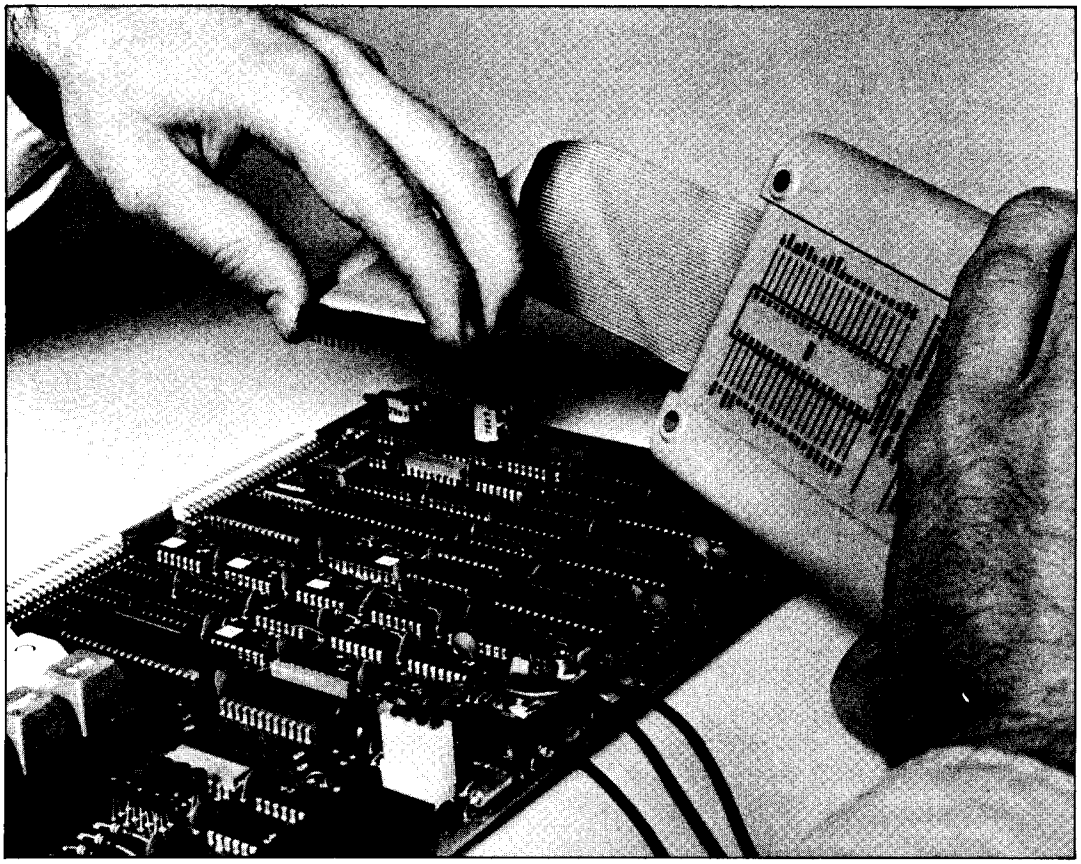


Figure 4B-1. Interface Pod Installation

Section 4C
Operating Modes

4C-1. INTRODUCTION

During operation, the 9010A may be in any one of three operating modes:

1. Immediate Mode
2. Programming Mode
3. Executing Mode

The 9010A may operate in only one of the three operating modes at any time. Operation in the Programming Mode or Executing Mode is indicated by the flashing PROGMING or EXECUTING annunciator at the far right of the display. When the 9010A is operating and neither the PROGMING nor the EXECUTING annunciator is on, the 9010A is in the Immediate Mode.

4C-2. IMMEDIATE MODE

Operation in the Immediate Mode is shown in Figure 4C-1. The 9010A enters the Immediate Mode quiescent state at power-on. The quiescent state is the "ready" state in which the 9010A resides while waiting for the operator to initiate some action.

The operator selects a test, operation, or troubleshooting function by pressing the appropriate key, such as RAM SHORT, LEARN, or READ. Pressing the key initiates the specification process, in which the operator supplies the additional parameters required by the 9010A before the test, operation, or function can be performed. Parameters required during specification may include such things as addresses, data, ROM signatures, or bit numbers. For example, if the Read function is selected, the address where the Read function is to be performed must be specified.

In the Immediate Mode after the specification is complete, the 9010A performs the test, operation, or function as specified. After the performance is complete, the 9010A returns to the quiescent state. Note in Figure 4C-1 that at any point during a specification the operator may abort the current specification and initiate a new specification by pressing the appropriate key, such as RAM SHORT or LEARN. The process of specification is described more fully in Section 4D.

Unless otherwise specified, the operation described in this manual takes place in the Immediate Mode.

4C-3. PROGRAMMING MODE

Operation in the Programming Mode is shown in Figure 4C-2. The 9010A operates in this mode during the creation or editing of programs. The programmer causes the 9010A to enter the Programming Mode by creating or opening a program. Notice that in contrast

to the Immediate Mode, the selection and specification of a test, operation, or troubleshooting function is not performed after the specification is completed. Instead, the specification is stored as a step in a program. The 9010A does not perform the specified action until the program is executed in the Executing Mode.

When the program is closed by the programmer, the 9010A returns to the Immediate Mode quiescent state. The Programming Mode occurs only during programming, and is discussed in Section 4L and in the 9010A Programming Manual.

4C-4. EXECUTING MODE

Executing Mode operation is shown in Figure 4C-3. The 9010A operates in this mode during the execution of programs and performs actions as specified by the program.

The operator causes the 9010A to enter the Executing Mode by specifying the execution of a program. After the program execution is complete, the 9010A returns to the Immediate Mode quiescent state. The Executing Mode and program execution are discussed in Section 4L of this manual and in the 9010A Programming Manual.

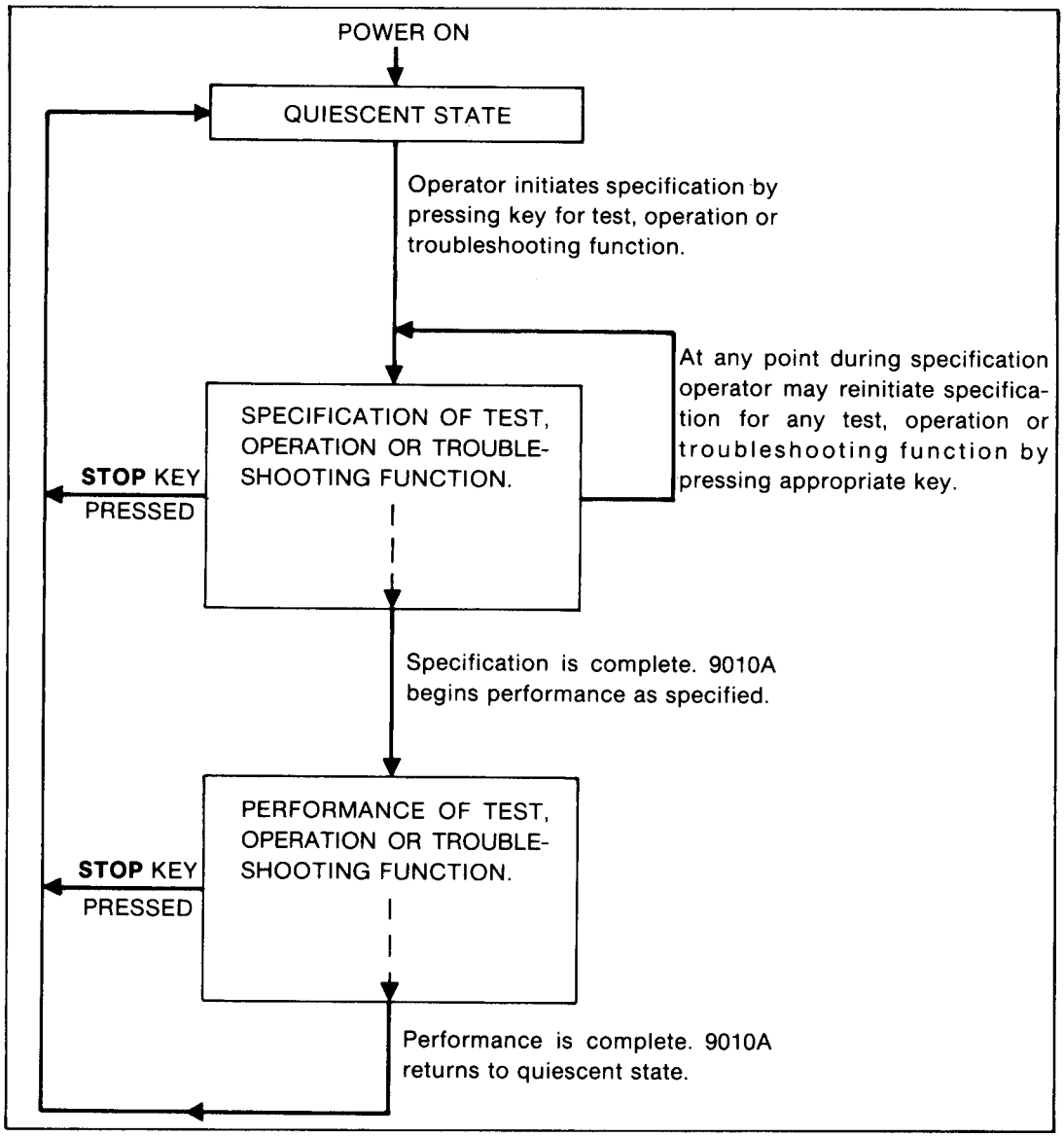


Figure 4C-1. Operation in the Immediate Mode

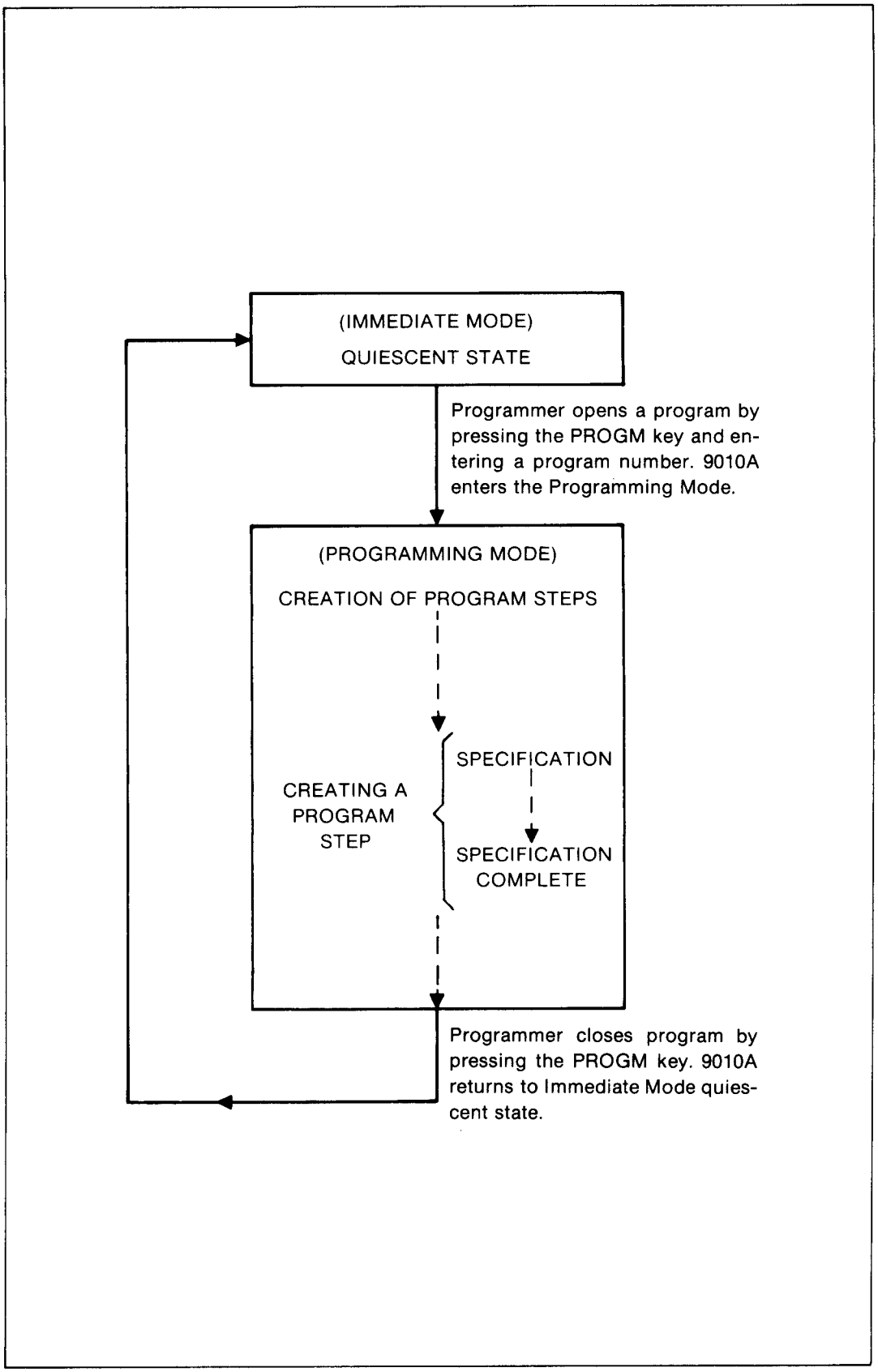


Figure 4C-2. Operation in the Programming Mode

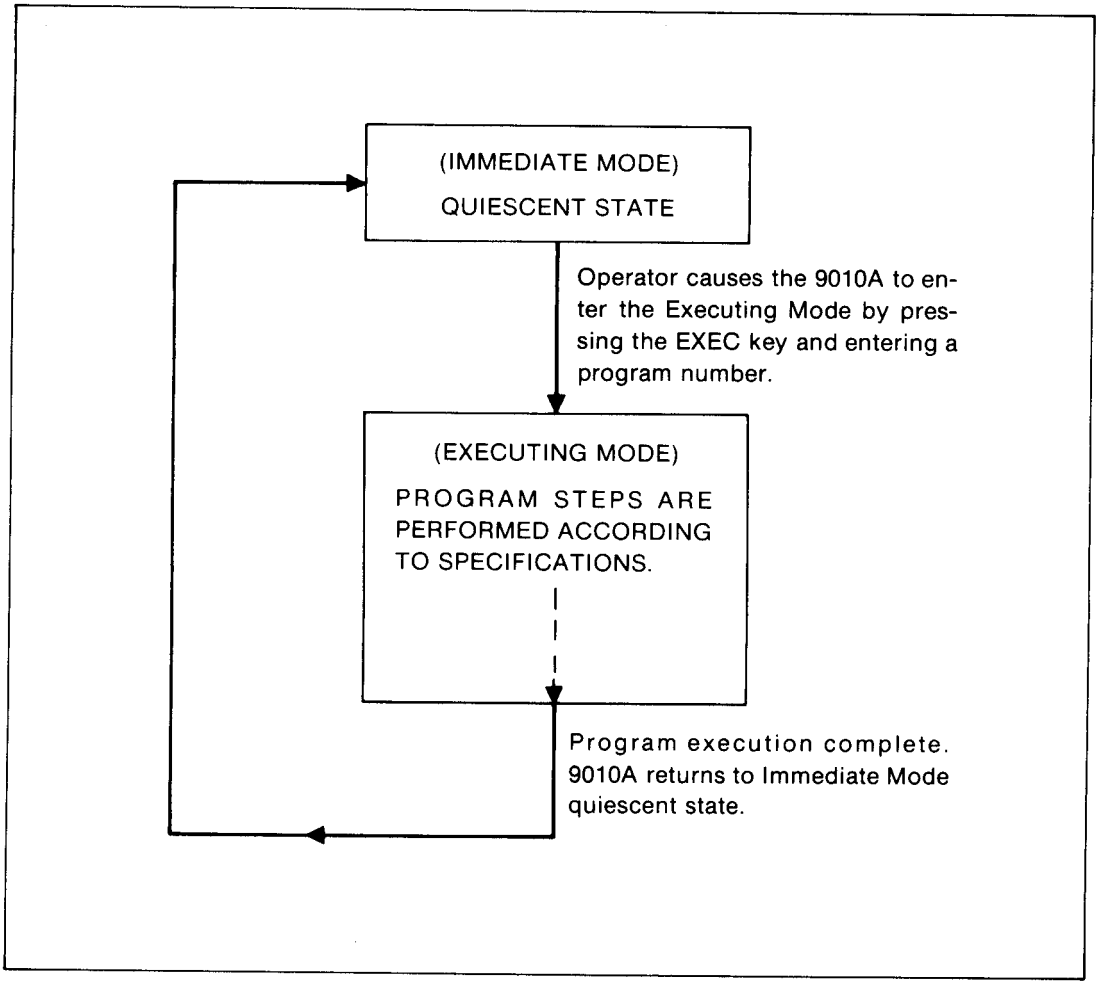


Figure 4C-3. Operation in the Executing Mode

Section 4D
Prompts

4D-1. INTRODUCTION

One feature which makes the 9010A easy to operate is the system of clear, consistent, and understandable prompts. Prompts are requests by the 9010A for more information from the operator. This section describes the information requested by prompts and describes when prompts are encountered during operation.

4D-2. INFORMATION REQUESTED BY PROMPTS

Information requested by prompts may be data, such as an address or numerical expression, or it may be a YES or NO response to a question.

Prompts for data are indicated by a blinking cursor that appears on the display next to the function selected. For example, when the Read troubleshooting function is selected, the 9010A displays the message READ @ _. The underscore (_) is the blinking cursor that serves as a prompt for the operator to define the address location where the Read operation is to take place.

Prompts for a YES or NO response include a question and end with a question mark. For example if the operator specifies the Read function at address 4D77 and the 9010A detects a bad power supply at the UUT μP socket while performing the Read operation, it displays the following message:

BAD PWR SUPPLY @ 4D77-LOOP?

This message asks the operator if the 9010A is to "loop on the error" (looping on errors is described in Section 4F). Pressing the YES key or the LOOP key causes the 9010A to loop on the error. Pressing the NO key or the CONT key causes the 9010A to ignore the detected error.

4D-3. PROMPTS DURING SPECIFICATION

When a 9010A function is selected by pressing the appropriate key, the 9010A usually requires the operator to supply additional operating parameters or specifications for the function before the 9010A can perform the operation on the UUT. The 9010A prompts the operator for the specifications in the order the information is required. For example, when the ROM Test is selected, three specifications must be provided:

1. The first address of the block of addresses on which the ROM Test is to be performed.

2. The last address of the block of addresses on which the ROM Test is to be performed.

3. The ROM signature that is to be compared with the ROM signature computed from the address block.

First, the 9010A prompts for the first address. When an address has been entered by the operator, the 9010A prompts for the second address. When the second address has been entered by the operator, the 9010A prompts for the ROM signature. When the ROM signature has been entered by the operator, the 9010A performs the operation as specified.

The following example shows the steps necessary for specifying the ROM Test over the address block 2000-3FFF with ROM signature 25DA, and the associated displays and prompts.

PRESS	DISPLAY	COMMENT
ROM TEST	*ROM TEST @ _*	Prompt for first address.
2000 ENTER	*ROM TEST @ 2000-_*	First address has been entered, now prompting for second address.
3FFF ENTER	*ROM TEST @ 2000-3FFF SIG _*	Second address has been entered, now prompting for ROM signature.
25DA ENTER	*ROM TEST @ 2000-3FFF SIG 25DA*	Specification complete.

For another example, consider the Write function. When the Write function is selected, the 9010A prompts for two parameters:

1. The address where data is to be written.
2. The data that is to be written.

The following example shows the steps necessary to select the Write function and specify the data FD07 to be written at the address 1C33.

PRESS	DISPLAY	COMMENT
WRITE	*WRITE @ _*	Prompt for address.
1C33 ENTER	*WRITE @ 1C33 = _*	Address has been entered, now prompting for data.
FD07 ENTER	*WRITE @ 1C33 = FD07*	Specification complete.

4D-4. UNDERSTANDING WAIT AFTER SPECIFICATION IS COMPLETE

After the operator completes the specification of the 9010A action, the 9010A appends the word WAIT to the final specification on the display and begins performing the action as specified. The word WAIT assures the operator that the 9010A is performing the action. Most of the troubleshooting functions (such as Read or Write) are performed so quickly that the final specification (including WAIT) is only seen briefly.

4D-5. AUDIBLE FEEDBACK

The 9010A also provides audible feedback in the form of a beep when the operator presses a key at a time when it is not allowed. For example, if the 9010A is in the Immediate Mode and the GOTO key is pressed, the 9010A emits a beep which tells the operator that the function cannot be selected. The GOTO key may only be pressed while the 9010A is in the Programming Mode. The audible beep may also be selected by the programmer for insertion in programs.

Section 4E
Defaults

4E-1. INTRODUCTION

Defaults are parameters, such as addresses or ROM signatures, that are stored in memory and supplied by the 9010A if the prompted specification is not supplied by the operator. This section describes how the operator may use defaults during the specification of a 9010A action.

4E-2. DEFAULTS DURING SPECIFICATION

The operator may invoke a default value by pressing the ENTER key when the 9010A prompts for a specification. For example, when the READ key is pressed, the 9010A prompts for the address where the Read operation is to be performed by displaying the following message:

READ @ _

The operator may default the address specification by pressing ENTER. The 9010A supplies the contents of Register F, which is generally the last address that was specified or used during an operation (see Section 4J), and performs the operation.

The following examples compare the manual entry with the default entry for a troubleshooting function.

PRESS	DISPLAY	COMMENT
READ	*READ @ _*	Prompt for address.
4OFF ENTER	*READ @ 4OFF*	Operator enters the address and the 9010A performs the operation.
READ	*READ @ _*	Prompt for address.
ENTER	*READ @ 4OFF*	Operator defaults address specification by pressing ENTER. The 9010A supplies the address 4OFF and performs the operation.

Defaults are primarily useful in saving the operator time and effort. Defaults allow the operator to enter parameters from a previous operation. The parameters that are to be

used again can be entered with one keystroke (the ENTER key) instead of having to be completely reentered.

For example, if the operator wants to write the same data (7AB3) to two addresses (20F0, 38C6), the data specification may be defaulted as follows:

PRESS	DISPLAY	COMMENT
WRITE	*WRITE @ _*	Prompt for address.
20F0 ENTER	*WRITE @ 20F0 = _*	Prompt for data.
7AB3 ENTER	*WRITE @ 20F0 = 7AB3*	9010A performs the operation as specified.
WRITE	*WRITE @ _*	Prompt for address.
38C6 ENTER	*WRITE @ 38C6 = _*	Prompt for data.
ENTER	*WRITE @ 38C6 = 7AB3*	Operator defaults data specification by pressing ENTER. 9010A supplies data and performs the operation.

Defaults may also be provided during the specification of the functional tests (ROM, RAM, and I/O tests). For example, when the ROM TEST key is pressed, the 9010A prompts for the address and ROM signature specifications as described in Section 4D-3. Rather than manually entering the prompted values, the operator may press the ENTER key when prompted for the first address. This causes the 9010A to supply the UUT ROM descriptors obtained during the Learn operation or entered through the VIEW keys. ROM descriptors and the Learn and View operations are described in Section 4G.

Information on defaults is provided as needed in later sections. A complete list of specifications and defaults for all the 9010A tests, functions, and operations is provided in Appendix B.

Section 4F
Detection of UUT Errors

4F-1. INTRODUCTION

Detecting and reporting errors involving the UUT is critical, since errors in UUT actions are the symptoms available to the operator in diagnosing and repairing the UUT. The 9010A provides a consistent, readily understandable system for handling UUT errors. The 9010A error handling system is described in this section.

4F-2. TYPES OF UUT ERRORS

There are three types of errors involving the UUT that can occur: timeout errors, UUT system errors, and test errors. They are described in the following paragraphs. Table 4F-1 provides a summary and brief description of the error messages for timeout and UUT system errors. Test error messages are summarized and described in Tables 4H-1 and 4H-2.

1. TIMEOUT ERROR.

To perform each action on the UUT, the 9010A must successfully transmit a command consisting of one or more bytes to the interface pod, and the 9010A must successfully receive a response of one or more bytes from the interface pod. Communication of these bytes involves handshaking between the interface pod and the 9010A. If the handshake is not successfully completed and the 9010A is unable to get a response from the interface pod, the 9010A "times out." Any of three timeout error conditions can be detected, and the appropriate timeout error message is displayed.

The three possible one-line timeout error messages are as follows:

POD TIMEOUT -ATTEMPTING RESET
UUT POWER FAIL -ATTEMPTING RESET
POD RESET ERROR -ATTEMPTING RESET

The first message is a non-specific message that indicates a variety of possible causes of the error. These may include a missing UUT clock or a faulty connection between the interface pod and the 9010A.

The second message indicates that the UUT power supply may be out of tolerance, and the UUT clock may be faulty.

The third message indicates that the interface pod may be the cause of the error, and the operator should perform the interface pod self test. When a timeout error occurs, the 9010A attempts to reset the interface pod. If the reset fails, the 9010A continues to attempt the reset until it succeeds or the operator initiates some other action.

Table 4F-1. UUT Error Types and Messages

TYPE	MESSAGE	DESCRIPTION
TIMEOUT ERROR	*POD TIMEOUT - ATTEMPTING RESET*	General error message caused by such things as no UUT clock or a faulty connection between the pod and the 9010A.
	UUT POWER FAIL - ATTEMPTING RESET	UUT power supply possibly at fault.
	POD RESET ERR - ATTEMPTING RESET	Interface pod possibly failing. Operator should perform interface pod self test.
UUT SYSTEM ERROR	*BAD PWR SUPPLY (@ aaaa) - LOOP?**	Improper power supply voltages at UUT μP socket.
	ILLEGAL ADDR @ aaaa - LOOP?	This message appears if the operator keys in an address that is not within the valid μP address space.
	*ACTIVE FORCE LINE (@ aaaa) - LOOP?** *STS BITS bbbb bbbb bbbb bbbb - LOOP?* *ACTIVE INTERRUPT (@ aaaa) - LOOP?** *STS BITS bbbb bbbb bbbb bbbb - LOOP?*	These two-line messages are displayed if any forcing lines or interrupts are detected to be active during an operation. The binary string in the second line corresponds to the status lines documented in the appropriate pod manual. A 1 corresponds to an active line, and a 0 (zero) corresponds to an inactive line. The binary string is shown in groups of four, with up to 16 digits in all.
	*CTL ERR (@ aaaa) - LOOP?** *CTL BITS bbbbbbbb - LOOP?*	This two-line message is displayed when any control line is detected to be not drivable. The binary string *bbbbbbbb* is a mask of 1's and 0's where a 1 corresponds to a line that is not drivable.
	ADDR ERR @ aaaa - LOOP? *ADDR BITS hhhhhhhh - LOOP?* *DATA ERR @ aaaa - LOOP?* *DATA BITS hhhhhhhh - LOOP?*	These two-line messages are displayed when any address or data lines are detected to be not drivable. The hexadecimal string *hhhhhhhh* is a mask where a bit that is 1 corresponds to a line that is not drivable. Address errors or data errors may only be detected if an address is included in the specification of an operation.
TEST ERROR	Test error messages are listed and described with the tests in which they occur in subsequent sections of this manual.	

**Note: The address is included in the error message only if an address is included in the specification of an operation.*

2. UUT SYSTEM ERROR.

The interface pod continually monitors several UUT conditions while the 9010A is in operation. For example, whenever the interface pod writes to a line, the pod monitors the actual logic level on the line. If the value written and the value monitored disagree, a "drivability" error is considered to have occurred. Drivability errors may be detected on control, address, or data lines. These errors typically occur if another bus device is holding a data or address line high or low, or if there are short circuits associated with these lines.

Other UUT conditions monitored during operations include the power supply voltage at the μP socket and interrupt requests. Errors associated with these conditions are called UUT system errors. If an error is detected, the 9010A displays one of the messages listed and described in Table 4F-1.

Note that four of the UUT system error messages listed in Table 4F-1 have parentheses around the address portion of the message, (@ *aaaa*). This is because the address is included in the message only if the operator specifies an address during selection of the operation or if the 9010A used internally generated addresses for the operation that reported the error. For example, the Write Control function requires no address, and no addresses are included in associated UUT system errors. Similarly, the UUT system address or data errors are not reported at all for operations that do not require an address, such as Write Control.

Sometimes it may be useful to disable the detection of a particular UUT system error if the reporting of such an error interferes with testing or troubleshooting. UUT system error detection may be disabled by the Setup function which is described in Section 4M.

3. TEST ERROR.

The largest category of UUT errors is the errors that are associated with the functional tests. The error messages are listed and described with the tests in Section 4H and summarized in Tables 4H-1 and 4H-2.

4F-3. HIERARCHY IN DETECTION OF UUT ERRORS

The three types of UUT errors are hierarchically arranged according to priority. The hierarchy in order of priority is as follows.

1. Timeout Error — Highest priority
2. UUT System Error
3. Test Error — Lowest priority

This hierarchy means that the 9010A detects and reports higher priority errors before lower priority errors. Higher priority errors must be removed or their detection disabled (if possible) before the 9010A detects and reports lower priority errors.

4F-4. LOOPING ON ERRORS WITH THE LOOP FUNCTION

One of the most powerful troubleshooting features of the 9010A is its capacity to continually monitor and report the appearance or disappearance of a UUT failure while the operator physically manipulates the UUT. This monitoring process is accomplished with the Loop function.

When the 9010A detects a UUT error, the 9010A suspends execution of whatever operation is in progress and reports the error. A prompt for the Loop function key is included in many of the error messages. The operator may press the LOOP key to cause the 9010A to continuously perform the operation. The operator stimulates or physically manipulates the UUT to try to remove the cause of the error, while observing the 9010A display or listening for the audible beep to determine if the error is still reported. This process, called "looping on errors," helps the operator to see the effect of his actions and quickly locate the cause of the UUT error.

To illustrate the process of looping on an error, consider the following 9010A display message which reports a UUT system error.

BAD PWR SUPPLY @ aaaa-LOOP?

This message reports that the UUT is not supplying the proper voltage levels at the μP socket. Note that the 9010A beeps to attract the operator's attention when the error is first reported. If the operator presses the LOOP key or the YES key, the 9010A continuously performs the same operation during which the error was reported. If the error condition is corrected during the Loop function, the 9010A continues looping and displays the following message

GOOD PWR SUPPLY @ aaaa

Note that while a prompt for a loop is displayed, the STOPPED annunciator flashes. It discontinues flashing only when the operator initiates some kind of action, such as pressing the LOOP or CONT key. Note also that while the 9010A is looping on an error, the LOOPING annunciator flashes.

When a prompt for a loop appears on the display, the operator may choose not to loop on the error by pressing the NO or CONT (continue) keys. This causes the 9010A to remove the error display message and continue execution of the specified operation that was suspended to report the error.

Note that the use of the Loop function is not restricted to use with errors. The Loop function may also be used with some of the 9010A tests, functions, and operations. Refer to Section 4N for more information.

4F-5. UNDERSTANDING OK OR FAIL

When the 9010A completes the execution of an operator-specified operation, test, or function, such as Learn, ROM Test, or Ramp, the message displayed ends with either the word OK or the word FAIL. For example, if the Read function is specified to be performed at address *aaaa,* when the 9010A completes the operation, one of the following messages is displayed:

READ @ aaaa = hhhh OK
READ @ aaaa = hhhh FAIL

OK at the end of a display message indicates that during the execution of the operation, either no errors occurred, or else all errors that occurred were corrected by the operator before proceeding.

FAIL at the end of a display message indicates that during the execution of the operation, one or more UUT errors were reported but not corrected by the operator. FAIL is a warning to the operator that something in the operation was amiss, and the results may not be reliable.

To illustrate the meaning of FAIL, assume the operator selects and specifies a ROM Test. During the course of the operation, the following message appears:

ROM ERR @ 1000-1FFF-LOOP?

Note that this message is the first line of a two-line message. The operator chooses to ignore the error message and presses the CONT key. The 9010A completes the operation and displays the following message.

ROM TEST FAIL

The message, ROM TEST FAIL, warns the operator that even though the operation was completed, the results are not reliable because an error was detected, reported, and not corrected.

Section 4G
Mapping and Viewing UUT Address Space

4G-1. INTRODUCTION

Troubleshooting any microsystem requires information about the UUT address space. This section describes how the Learn operation may be used to obtain UUT address space information and how the View operations may be used to examine the information. The LEARN and VIEW keys are identified in Figure 4G-1.

4G-2. LEARN

If UUT address space information is not known or is incomplete, the Learn operation may be used to explore and map the UUT memory. The Learn operation is typically performed on a properly operating UUT to obtain valid reference data for use in testing a suspect UUT. For the experienced operator, the Learn operation may also provide clues about the cause of faults when performed on a failing UUT.

The Learn operation tests the UUT address locations and identifies the addresses of blocks of ROM, RAM, and I/O registers. For each block of ROM, the operation computes a ROM signature. For each block of I/O registers, the operation computes an I/O bit mask which indicates which bits in I/O have read-write capability.

The information obtained during the Learn operation typically consists of a list of items, called address descriptors, which comprise the UUT memory map. A possible UUT memory map and the associated address descriptors are shown in Figure 4G-2.

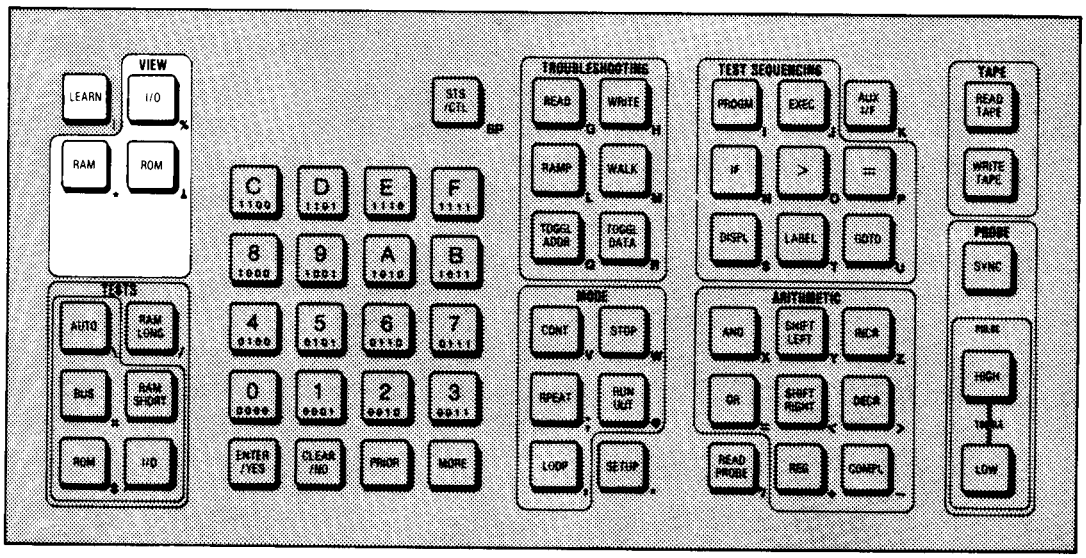


Figure 4G-1. The LEARN and VIEW Keys

Address descriptors stored in 9010A tape-transferable memory. These address descriptors represent the memory map below.

ADDRESS DESCRIPTORS

RAM @ 5000-50FF

ROM @ 0000-0FFF SIG 0D47
ROM @ 3000-4FFF SIG 2B60
ROM @ 7000-70FF SIG 08AA
ROM @ A000-AFFF SIG 44C9

I/O @ 1A00-1A01 BTS 7F

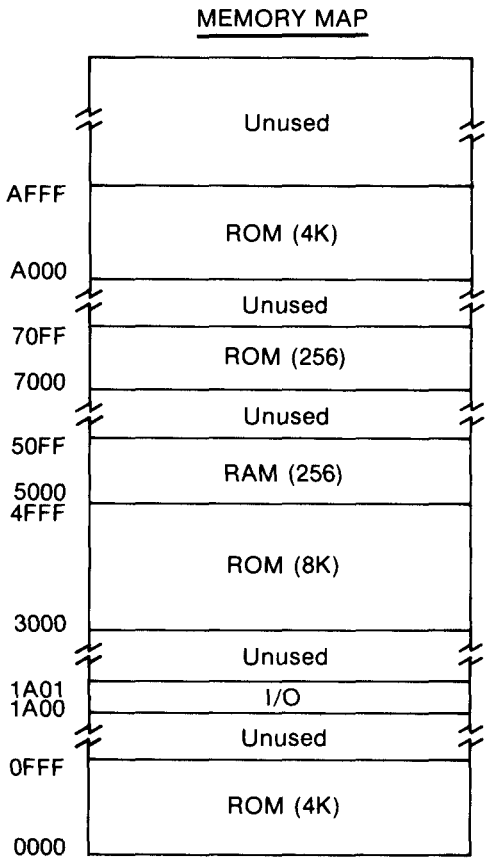


Figure 4G-2. Typical UUT Memory Map and Address Descriptors

In the ROM descriptors listed in Figure 4G-2, the hexadecimal digits following SIG represent the ROM signature computed during the operations for the address space block listed. For example, the ROM signature for the address space 0000-0FFF is OD47.

In the I/O descriptors listed in Figure 4G-2, the hexadecimal digits following BTS represent the bit mask obtained during the operation. In the binary representation of the bit mask, the 1's represent the bits that have read-write capability. The number of bits in the bit mask equals the number of data lines in the UUT μP. For example, if there are 8 data lines in the μP, the bit mask may be any hexadecimal quantity from 1 to FF. Or if there are 16 data lines, the bit mask may be any hexadecimal quantity from 1 to FFFF.

For an example of an I/O bit mask, notice in Figure 4G-2 that the bit mask for the I/O register at 1A00-1A01 is 7F. The hexadecimal value 7F equals the binary value 0lll llll. This implies that all the bits in both I/O registers have read-write capability except the highest order bit.

The UUT memory map is stored in the 9010A tape-transferable memory. It may be examined by using the VIEW keys as described in Section 4G-7.

During the Learn operation, the 9010A writes and reads data patterns to 64-byte blocks (1 byte = 8 bits) for the entire address range of the μP. Based on the data read, the 9010A uses the following criterion to determine whether addresses are ROM, RAM, I/O or unassigned:

- ROM: The addresses cannot be written to, and all address bits are fully decoded.
- RAM: All bits of all addresses for the 64-byte block are write-readable, and all address bits are fully decoded.
- I/O: At least one bit of an address is write-readable, but any other condition for determining RAM fails.
- Unassigned: Anything not identified as ROM, RAM, or I/O.

Note that although the Learn algorithm which obtains the descriptors is very powerful, it does have some limitations. For example, it cannot identify bank switched RAM or I/O which does not have at least one bit that is read-writable. Or if there are multiple blocks of ROM or RAM at contiguous addresses, the Learn operation reports these as a single block of ROM or RAM covering the entire address range. The Learn operation is not intended to be a replacement for schematics or other existent UUT documentation. For this reason, it is recommended that the operator enter address descriptors with the VIEW keys if the descriptors are known.

Also note, however, that the Learn operation can be a very powerful diagnostic tool when performed on a failing UUT. For example, if the operator knows that a UUT has 10 RAM blocks with contiguous addresses, but information from the Learn operation indicates 20 RAM blocks with non-contiguous addresses, then an address decode problem is evident.

4G-3. Specifying the Operation

The only specification required for the Learn operation is the UUT address space on which the operation is to be performed. The operation may be performed on all or part of the UUT address space. Note that the RPEAT and LOOP keys do not affect the operation.

To specify the entire μP address space for the Learn operation, do the following:

1. Press LEARN. The 9010A displays a prompt for the first address by displaying the following message:

   LEARN @ _

2. Press ENTER. The 9010A begins execution on the entire UUT address space specified by the interface pod after displaying the following message:

   LEARN

To specify part of the UUT address space for the operation, do the following:

1. Press LEARN. The 9010A displays a prompt for the first address by displaying the following message:

   LEARN @ _

2. Key in the first address and press ENTER. The 9010A displays the first address and prompts for the second address with the following message:

LEARN @ aaaa-_

3. Key in the second address and press ENTER. The 9010A begins execution on the specified address space after displaying the following message:

LEARN @ aaaa-aaaa

The following example shows the proper steps for specifying the Learn operation over the address range from 1000 to 4FFF and the corresponding display for each step:

PRESS	DISPLAY	COMMENT
LEARN	*LEARN @ _*	Prompt for first address.
1000 ENTER	*LEARN @ 1000-_*	Prompt for second address.
4FFF ENTER	*LEARN @ 1000-4FFF*	Specification complete. Execution proceeds.

4G-4. Generating the UUT Memory Map

After the operator enters the address specifications, the 9010A begins performing the Learn operation. Any presently stored address space descriptors whose addresses are within the address range of the Learn operation are deleted from 9010A memory.

Because of the tremendous number of operations involved, the execution of the operation may take a considerable length of time (typically 10-100 minutes for a common 8-bit μP in a typical UUT). The length of time varies considerably depending on the relative proportion of RAM, ROM, I/O and unassigned memory, as well as the size of the specified address block. To provide assurance that the operation is executing properly, the 9010A appends the following message to the text on the display:

NOW aa00

The digits represented by *aa00* are the hexadecimal digits for the address where the operation is presented taking place. The display is updated every 256 locations. For the example given for the address specification, the display is updated during normal operation as follows:

DISPLAY

LEARN @ 1000-4FFF NOW 1000
LEARN @ 1000-4FFF NOW 1100
LEARN @ 1000-4FFF NOW 1200
LEARN @ 1000-4FFF NOW 1300
LEARN @ 1000-4FFF NOW 1400
etc.

After the Learn operation has explored all of the addresses specified, the following message is briefly displayed:

LEARN @ aaaa-aaaa WAIT

While the WAIT message is on the display, the operation compiles the information that has been obtained and composes the descriptors for the address space that has been

explored. After the information has been compiled, the 9010A replaces the word WAIT with the words OK or FAIL.

The operator may terminate execution of the Learn operation by pressing the STOP key. Note that if the operator terminates execution before the operation is complete, address space information is incomplete. For example, ROM signatures are not compiled until the WAIT message is displayed.

4G-5. Premature Termination of the Learn Operation

The 9010A may store up to 100 address space descriptors during the Learn operation. If 100 descriptors are obtained before the Learn operation is completed, the 9010A checks the descriptors to see if any of them may be consolidated. If this is not possible, the 9010A aborts the Learn operation and displays the following message:

FATAL--MEMORY EXCEEDED FOR LEARN

The 100 address space descriptors are adequate for any normally operating UUT. If the execution is prematurely terminated, it may indicate that something is wrong with the UUT. The descriptors that have been obtained to this point are retained in memory, for they can provide an experienced operator with useful information and possible clues about the cause of the UUT failure.

4G-6. VIEW

The three VIEW keys (VIEW RAM, VIEW ROM, and VIEW I/O) allow the operator to view and edit the UUT memory map. The following paragraphs explain how to accomplish the viewing and editing.

4G-7. Viewing the Memory Map

The address space descriptors for RAM, ROM, or I/O are placed on the display when the operator presses the appropriate VIEW key. Each key places the first descriptor for that type of address block on the display. The flashing MORE annunciator indicates that more descriptors of the type being viewed are available. Other descriptors of the same type may be brought to the display with the MORE and PRIOR keys. For example, if the UUT memory map listed in Figure 4G-2 is present in 9010A memory, the ROM descriptors may be viewed by pressing the ROM VIEW, MORE, and PRIOR keys as follows:

PRESS	DISPLAY	COMMENT
ROM VIEW	*ROM @ 0000-0FFF SIG 0D47*	MORE annunc. flashing
MORE	*ROM @ 3000-4FFF SIG 2B60*	MORE annunc. flashing
MORE	*ROM @ 7000-70FF SIG 08AA*	MORE annunc. flashing
MORE	*ROM @ A000-AFFF SIG 44C9*	MORE annunc. off
PRIOR	*ROM @ 7000-70FF SIG 08AA*	MORE annunc. flashing

The first descriptor in the list appears on the display. The subsequent descriptors are brought to the display with the MORE key, and preceding descriptors with the PRIOR key. The RAM VIEW and I/O VIEW keys operate in a similar manner.

If no address descriptors for the type requested (ROM, RAM, I/O) are present in 9010A memory, the 9010A provides the appropriate message, such as the following:

NO ROM INFO

4G-8. Editing the Memory Map

While viewing the address space descriptors, the UUT memory map may be edited. Descriptors may be added or deleted by using the CLEAR and ENTER keys.

To delete a descriptor that is on the visible display, press CLEAR. The 9010A removes the descriptor from the screen and from 9010A memory. If any more descriptors of that type (RAM, ROM or I/O) exist, the 9010A brings the next descriptor to the display. When descriptors are entirely deleted, the message NO (ROM, RAM, or I/O) INFO appears.

Descriptors may be added while viewing existent descriptors of the same type, or while viewing the message NO (ROM, RAM, or I/O) INFO. For example, only RAM descriptors may be added while viewing other RAM descriptors or the message NO RAM INFO. Similarly, ROM descriptors may be added when viewing ROM descriptors, or I/O descriptors may be added when viewing I/O descriptors.

To add a RAM descriptor:

1. Press RAM VIEW. The 9010A displays existing RAM descriptors.

2. Press ENTER. The 9010A prompts for the first address with the following message:

   RAM @ _

3. Key in the first address and press ENTER. The 9010A displays the first address and prompts for the second address with the following message:

   RAM @ aaaa-_

4. If the operator presses ENTER or keys in a value equal to the first address, the following message is displayed:

   RAM @ aaaa

Key in the second address and press ENTER. The second address must be greater than the value of the first address to be accepted as a unique second address. If the second address is accepted, the 9010A adds the descriptor to the list in 9010A memory and displays the following message:

RAM @ aaaa-aaaa

The following example presents the key sequence and the corresponding displays for entering the RAM descriptor RAM @ D000-DFFF. For this example, it is assumed the 9010A has no RAM descriptors in memory.

PRESS	DISPLAY
RAM VIEW	*NO RAM INFO*
ENTER	*RAM @ _*
D000 ENTER	*RAM @ D000-_*
DFFF ENTER	*RAM @ D000-DFFF*

The RAM descriptor RAM @ D000-DFFF is stored in 9010A memory.

To add an I/O descriptor:

1. Press I/O VIEW. The 9010A displays existent I/O descriptors.

2. Press ENTER. Key in the first and second addresses as prompted by the 9010A. The 9010A accepts the addresses and prompts for the bit mask with the following message:

IO @ aaaa-aaaa BTS _

3. Key in the I/O bit mask (in hexadecimal). The 9010A accepts any hexadecimal quantity from one to hh, where hh corresponds to the value obtained when every bit position on the data lines equals 1. For example, the range of values for the I/O bit mask for an 8-bit μP is 1-FF. The value FF (hexadecimal) equals 1111 1111 (binary), which is the value obtained when every bit position equals 1. Note that is order for an I/O descriptor to be accepted, at least one bit in the bit mask must be specified as read-writable. When the bit mask is keyed in, the 9010A adds the descriptor to the list and displays the following message:

IO @ aaaa-aaaa BTS hh

To add a ROM descriptor:

1. Press ROM VIEW. The 9010A displays existent ROM descriptors.

2. Press ENTER. Key in the first and second addresses as the 9010A prompts for them. The 9010A accepts the addresses and prompts for the ROMsignature by displaying the following message:

ROM @ aaaa-aaaa SIG

3. Complete the procedure by following either of the following steps:

a. Key in the ROM signature. The ROM signature may be any hexadecimal quantity from 0 to FFFF. The 9010A adds the descriptor to the list and displays the following message:

ROM @ aaaa-aaaa SIG nnnn

b. Press ENTER. This causes the 9010A to attempt to compute the ROM signature at the addresses specified from the UUT connected to the 9010A. While the 9010A performs this, it displays the following message:

ROM @ aaaa-aaaa SIG WAIT

When the signature is computed, the 9010A replaces the message portion WAIT with the signature and adds the completed ROM descriptor to the list. Note that UUT system errors may occur during this operation, and if there are any residual errors, the signature may be incorrect.

Section 4H
Built-In Tests

4H-1. INTRODUCTION

There are five built-in tests in the 9010A to automatically test the electrical integrity of the UUT μP bus, the read-write capability of I/O registers, the data in ROM, and the functionality of RAM. These tests are Bus Test, ROM Test, I/O Test, RAM Short, and RAM Long. In addition, Auto Test provides a combination of four of the other tests. The location of the associated keys is indicated in Figure 4H-1.

The following paragraphs describe the specification and performance of each test. Error messages are listed and described in the text and illustrated by examples. A summary of the error messages for Bus Test is provided in Table 4H-1. A summary of the error messages for the other tests is provided in Table 4H-2. The defaults for the tests are described at the end of this section. A summary of the specifications and default values for the tests is provided in Appendix B.

4H-2. BUS TEST

Bus Test is a test of the electrical integrity of UUT control, address, and data buses. Bus Test identifies control lines that are not drivable, as well as address lines that are tied high, low, or tied together, and data lines that are tied high, low, or tied together.

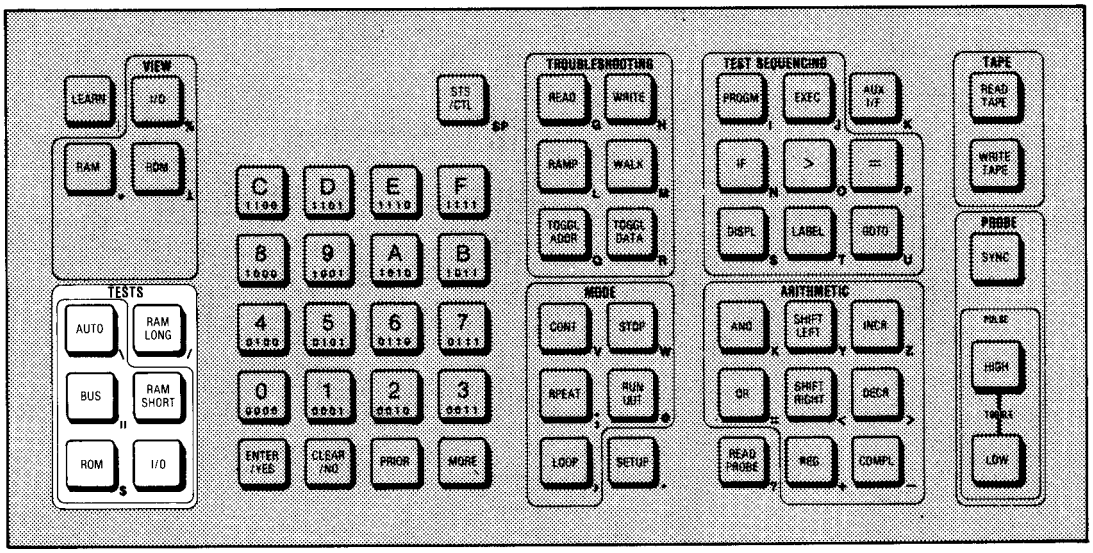


Figure 4H-1. The TEST Keys

Table 4H-1. Bus Test Error Messages

ERROR TYPE	ERROR MESSAGE	NOTE
1. Control Lines Not Drivable	*CTL ERR bbbbbbbb bbbbbbbb - LOOP?*	*1*
2. Address Lines Tied High or Low	*ADDR BIT aa TIED HIGH-LOOP?* *ADDR BIT aa TIED LOW-LOOP?*	*2* *2*
3. Address Lines Tied Together	*ADDR BITS a1 AND a1 TIED-LOOP?*	*3*
4. Data Lines Tied High or Low	*DATA BIT dd TIED HIGH-LOOP?* *DATA BIT dd TIED LOW-LOOP?*	*4* *4*
5. Data Lines Tied Together	*DATA BITS d1 AND d2 TIED-LOOP?*	*5*

NOTES:

1. In the binary 16-bit string *bbbbbbbb bbbbbbbb*, a 1 corresponds to undrivable lines, and a 0 corresponds to drivable lines. Refer to the appropriate interface pod manual for the control lines that corresponds to the bit numbers. Extra bits are reported as 0.

2. The *aa* is a decimal number corresponding to the bit number of the bit tied high or low. The range of values depends on the number of address lines.

3. The *a1* and *a2* are decimal numbers corresponding to the bit numbers of the bits tied together.

4. The *dd* is a decimal number corresponding to the bit number of the bit tied high or low. The range of values depends on the number of data lines.

5. The *d1* and *d2* are decimal numbers corresponding to the bit numbers of the bits tied together.

Table 4H-2. Functional Test Error Messages

TEST	DISPLAY MESSAGE	MESSAGE DESCRIPTION
I/O TEST	*R/W ERR @ aaaa BTS hhhh - LOOP?*	Hexadecimal number *hhhh* is a representation of bits that were not read-writable. 1 = bit specified read-writable and detected not read-writable. 0 = bit specified read-writable or not specified.
ROM TEST	*ROM ERR @ aaaa-aaaa - LOOP?* *SIG WAS mmmm NOT nnnn - LOOP?*	Two-line message. hex string *mmmm* = signature computed during test. Hex string *nnnn* = signature specified before test.
RAM SHORT	*R/W ERR @ aaaa BTS hhhh - LOOP?*	See I/O Test above.
	RAM BITS d1 AND d2 TIED-LOOP?	Decimal numbers *d1* and *d2* are the tied data bits.
	RAM DCD ERR @ aaaa BIT dd - LOOP?	Decimal number *dd* is the address bit that is not decoding properly.
RAM LONG	All error messages associated with RAM Short also apply to RAM Long.	
	RAM PATT ERR @ aaaa - LOOP? *DATA WAS xxxx NOT hhhh - LOOP?*	Two-line message. Hexadecimal number *xxxx* is actual data, hexadecimal number *hhhh* is expected data.
BUS TEST	Bus Test error messages are summarized in Table 4H-1.	
AUTO TEST	There are no error messages unique to Auto Test. Any error messages that might be encountered are described with the tests that Auto Test invokes (Bus Test, ROM Test, ROM Short, and I/O Test).	

4H-3. Specification and Performance of Bus Test

To specify the Bus Test, press the BUS TEST key. No other entries are required.

As soon as the BUS TEST key is pressed, the 9010A begins performing the test and displays the following message.

BUS TEST WAIT

After the Bus Test is completed, the 9010A replaces WAIT with an OK or FAIL.

4H-4. Bus Test Error Messages

The Bus Test error messages are listed in Table 4H-1. Each error type is discussed in the following paragraphs.

1. CONTROL LINES NOT DRIVABLE.

Bus Test exercises the control lines and identifies any that are not drivable by the interface pod. The control lines tested include lines that the operator can explicitly write to, as well as lines the operator cannot explicitly write to, such as timing or handshake lines. Any line where the value written by the interface pod does not equal the value measured by the interface pod at the μP socket is reported as not drivable. An example of a message that might be received with an 8080 microsystem is the following:

CTL ERR 00000000 00010000-LOOP?

This message indicates that the control line corresponding to bit 4 is not drivable. If the operator loops on the error and removes the error, the message changes to the following:

CTL OK 00000000 00000000

2. ADDRESS LINES TIED HIGH OR LOW.

Bus Test exercises the address lines and identifies any bits tied to high or low voltage levels. Bits are tested from lower order to higher order, and any appropriate error messages are displayed. An example of a message that might be displayed is the following:

ADDR BIT 7 TIED HIGH-LOOP?

The operator may choose to loop on the error by pressing the YES or LOOP keys. For an address bit detected high, the action taken by the 9010A to loop on the error is to attempt to read the UUT at address 0000. For an address bit detected low, the action taken to loop on the error is to attempt to read the UUT at the address with all bits set to 1. Note that if problems with the control lines have been reported but not resolved, then detection of tied address lines is not reliable. If the error is removed while looping, the message displayed is the following:

ADDR BIT 7 OK

3. ADDRESS LINES TIED TOGETHER.

Bus Test also identifies address lines that are tied together. If there are more than two lines tied together, Bus Test identifies at least one pair of lines. An example of a message that might occur is the following:

ADDR BITS 7 AND 8 TIED-LOOP?

When looping on an error, the 9010A performs two read operations. The first read operation is performed with the bit corresponding to *a1* set to 1, and all other bits set to 0. The second read operation is performed with the bit corresponding to *a1* set to 0, and all other bits set to 1. Note that if address lines are tied high or low, then the detection of lines tied together is not reliable. If more than two address lines are tied together, Bus Test will detect and report at least one pair of tied lines. If the error is removed while looping, the following message is displayed:

ADDR BITS a1 AND a2 OK

4. DATA LINES TIED HIGH OR LOW.

Bus Test also exercises the data lines and identifies any lines tied to high or low voltage levels. When looping on an error associated with a data line tied high, the 9010A attempts to write 0000 to the data lines of the UUT μP bus at an address specified by a Setup parameter. When looping on an error associated with a data line tied low, the 9010A attempts to write 1's to the data lines of the UUT μP bus at the same Setup parameter address. Instructions for changing Setup parameters are provided in Section 4M. The relevant Setup display message is as follows:

SET-BUS TEST @ FFFF-CHANGE?

Note that the address specified by the Setup parameter should be a location where nothing else would attempt to drive the data lines while the interface pod attempts to write to that address. For example, in some microsystems, writing to a ROM location causes the ROM to attempt to drive the data lines. Note also that if any control or address line errors are reported and not resolved, the detection of data line errors is not reliable. If the error is removed while looping, the following message is displayed:

DATA BIT dd OK

5. DATA LINES TIED TOGETHER.

Bus Test also identifies data lines that are tied together. When the 9010A loops on an error, a pair of complementary data values are written to the UUT at the same address specified by the Setup parameter described in the previous paragraph. The first value is written with the bit corresponding to *d1* written high, and all other bits written low. The second value is written with *d1* written low and all other bits written high. If more than two data lines are tied together, Bus Test will detect and report at least one pair of tied lines. If the error is removed while looping, the following message is displayed:

DATA BITS d1 AND d2 OK

4H-5. SPECIFYING THE ADDRESSES FOR PERFORMING A TEST

When any one of four of the built-in tests (I/O Test, ROM Test, RAM Short, and RAM Long) are selected by the operator, the operator may specify that the test be performed at a single address or a block of addresses. When the operator specifies a block of addresses, the first (lower) address is specified, and then the second (upper) address is specified.

For example, to specify the I/O Test at a block of addresses, do the following:

1. Press the I/O TEST key. The 9010A displays a prompt for the first address with the following message:

IO TEST @ _

2. Key in the first address *aaaa* and press ENTER. The 9010A accepts and displays the first address and prompts for the second address with the following message:

IO TEST @ aaaa-_

3. Key in the second address *aaaa* and press ENTER. The second address must be greater than or equal to the first address to be accepted as a second address. If the second address is accepted, the 9010A displays the second address and prompts for the rest of the I/O Test specification with the following message:

I/O TEST @ aaaa-aaaa BTS _

The first and second addresses for the ROM Test, RAM Short, and RAM Long are specified in the same way as shown for I/O Test.

To specify the I/O Test at a single address, do the following:

1. Press the I/O TEST key. The 9010A displays a prompt for the first address with the following message:

IO TEST @ _

2. Key in the address and press ENTER. Then press ENTER again. The 9010A displays the single specified address and prompts for the rest of the I/O Test specification with the following message:

IO TEST @ aaaa BTS _

The single address for the ROM Test, RAM Short, and RAM Long is specified in the same way as shown for I/O Test.

4H-6. I/O TEST
4H-7. Specification of I/O TEST

To select the I/O TEST, do the following:

1. Key in the first and second addresses as shown in Section 4H-5. The 9010A accepts and displays the addresses and prompts for the bit mask for the block of I/O registers with the following message:

IO TEST @ aaaa-aaaa BTS _

The bit mask is specified in hexadecimal. The number of bits that may be specified in the bit mask equals the number of data lines in the UUT μP. Bits that are equal to 1 in the bit mask correspond to data lines that are to be tested for read-write capability. Bits that are equal to 0 in the bit mask correspond to data lines that are not to be tested for read-write capability. Note that at least one bit must be read-writable for the bit mask to be accepted and the I/O Test performed.

2. Key in the bit mask *mmmm* and press ENTER. The 9010A displays the following message and begins execution of the I/O Test as specified:

IO TEST @ aaaa-aaaa BTS mmmm

The following example shows the proper steps for specifying the I/O TEST at addresses 5017-501F with bit mask 17 (0001 0111) and the corresponding displays.

PRESS	DISPLAY
I/O TEST	*IO TEST @ _*
5017 ENTER	*IO TEST @ 5017- _*
501F ENTER	*IO TEST @ 5017-501F BTS _*
17 ENTER	*IO TEST @ 5017-501F BTS 17 WAIT*

4H-8. Performance of I/O Test

After the I/O Test specifications are complete, the 9010A tests the bits corresponding to a one in the bit mask for read-write capability at each of the locations specified. After completion of the I/O Test, the 9010A appends an OK or FAIL to the message on the display.

During performance of the I/O Test, if any specified bits do not have read-write capability, the 9010A displays the following message:

R/W ERR @ aaaa BTS mmmm-LOOP?

In the I/O error message *aaaa* is the address of the I/O register that is reported to have the faulty bits. In the hexadecimal string *mmmm,* a one corresponds to a bit that is detected not read-writable and is specified as being tested for read-write capability by the bit mask. A zero in the string corresponds to bits that respond as predicted by the bit mask (either read-writable or not read-writable, depending on the bit mask).

If the error is removed while looping, the 9010A displays the following message:

R/W OK @ aaaa BTS 0000

4H-9. Example of I/O Test

In the following example the operator selects the I/O Test and specifies addresses 4F00-4F07 with bit mask 6F. The 9010A displays the following message and begins execution:

R/W TEST @ 4F00-4F07 BTS 6F

While performing the test, the 9010A detects that the first bit at address 4F00 is not read-writable as specified and displays the following message:

R/W ERR @ 4F00 BTS 01-LOOP?

The operator chooses to exercise the error and presses the YES key. After the operator physically manipulates the UUT (for example, by cleaning the UUT pcb with low pressure air, replacing the chip, or by pressing down on suspected chips mounted in sockets) the cause of the error is removed. The 9010A no longer detects the error and displays the following message:

R/W OK @ 4F00 BTS 00

4H-10. ROM TEST

4H-11. Specification of ROM Test

To select the ROM Test, do the following:

1. Key in the first and second addresses.

The 9010A accepts the addresses and prompts for the ROM signature for the address block with the following message:

ROM TEST @ aaaa-aaaa SIG _

2. Key in the ROM signature *nnnn* and press ENTER.

A ROM signature is entered in hexadecimal and must be less than or equal to FFFF. The 9010A accepts the ROM signature, displays the following message, and begins performing the test. Note that the first word in the message is truncated.

M TEST @ aaaa-aaaa SIG nnnn WAIT

The following example shows the proper steps for specifying the ROM Test at addresses 4000-43FF with ROM signature 2D73 and the corresponding displays.

PRESS	DISPLAY
ROM TEST	*ROM TEST @ _*
4000 ENTER	*ROM TEST @ 4000-_*
43FF ENTER	*ROM TEST @ 4000-43FF SIG _*
2D73 ENTER	*M TEST @ 4000-43FF SIG 2D73 WAIT*

4H-12. Performance of ROM Test

After the specifications are complete, the 9010A begins performing the ROM Test. After the ROM Test is completed, the 9010A appends an OK or FAIL to the message on the display.

The 9010A computes the ROM signature for the address block specified and compares it with the specified ROM signature. If the computed and specified ROM signatures are not equal, the 9010A places the first line of the following two-line message on the display. The message may be scrolled using the MORE and PRIOR keys.

ROM ERR @ aaaa-aaaa-LOOP?
SIG WAS mmmm NOT nnnn-LOOP?

The second line in the display shows both the computed and specified ROM signatures which the 9010A found unequal. If the operator exercises the error by pressing the YES or LOOP keys, the 9010A displays the following message:

ROM ERR @ aaaa-aaaa

While the error is exercised, the 9010A continues to compute the ROM signature for the address block specified and compare it with the specified signature. If the cause of the error is removed and the error is no longer detected, the following message is displayed:

ROM OK @ aaaa-aaaa

4H-13. Example of ROM Test

The following example illustrates the ROM Test error message:

The operator selects the ROM TEST and specifies addresses 4000-43FF with ROM signature 2D73. The 9010A begins execution and displays the following message:

M TEST @ 4000-43FF SIG 2D73 WAIT

After the 9010A computes the ROM signature, it detects an error and places the first line of the following two-line message on the display:

ROM ERR @ 4000-43FF-LOOP?
SIG WAS F033 NOT 2D73-LOOP?

The operator chooses to loop on the error and presses the YES key. The 9010A begins looping and displays the following message:

ROM ERR @ 4000-43FF

The operator manipulates the UUT in some way (for example, by cleaning or applying pressure to chips), and the error is no longer detected. The 9010A displays the following message:

ROM OK @ 4000-43FF

4H-14. RAM SHORT

To ensure that all RAM failures are identified and yet optimize test times, the 9010A provides two tests for RAM, RAM Short and RAM Long. As the name implies, RAM Short is a shorter, faster test than RAM Long. RAM Short is designed to quickly identify common RAM failures such as address decoding errors or bits that are not read-writable. The specification and operation of RAM Short is described first, followed by a similar description of RAM Long.

4H-15. Specification of RAM Short

To select the RAM Short test, key in the first and second addresses. The 9010A accepts the addresses and displays the following message:

RAM SHORT @ aaaa-aaaa WAIT

The following example shows the proper steps for specifying RAM Short at addresses 6C00-6FFF and the corresponding displays.

PRESS	DISPLAY
RAM SHORT	*RAM SHORT @_*
6C00 ENTER	*RAM SHORT @ 6C00-_*
6FFF ENTER	*RAM SHORT @ 6C00-6FFF WAIT*

4H-16. Performance of RAM Short

After the specifications are complete, the 9010A begins performing RAM Short. RAM Short is executed on each address block specified. After RAM Short is completed, the 9010A replaces the word WAIT in the message on the display with OK or FAIL.

Performance of RAM Short consists of three phases. Each phase performs unique operations during testing and looping on errors and has unique error messages. The operations and messages for each phase are as follows:

1. A test of the read-write capability of every data bit of every address location in the address block.

If any bits are identified as not read-writable, the following message is displayed:

R/W ERR @ aaaa BTS mmmm-LOOP?

The format of the hexadecimal string *mmmm* is similar to the I/O bit mask. However, a one corresponds to a bit that is identified as not read-writable, and a zero corresponds to a bit that is identified as read-writable. The operator may

choose to loop on the error by pressing the YES or LOOP keys. If the error is removed while looping, the following message is displayed:

R/W OK @ aaaa BTS 0000

2. A test for data lines tied together.

The second phase of the test is not performed if any errors remain from the first phase. If the 9010A detects any data lines tied together in the second phase, it places the following message on the display:

RAM BITS d1 AND d2 TIED-LOOP?

The decimal numbers *d1* and *d2* can range from 0-31, and correspond to the tied data bits. A common cause for this error could be, for example, shorted inputs to data buffers on the two data lines. When looping on the error, the 9010A writes data to the location with one erroneous bit driven high and the other bit driven low, and then reads the data at the location. Then the 9010A performs the same write and read operations with the previous logic levels of the erroneous bits reversed. The second phase of the test is performed at the first location in a RAM block. If the error is removed while looping, the following message is displayed:

RAM BITS d1 AND d2 OK

3. A test for address decoding errors within the address block.

The third phase of the test is not performed if any errors remain from the first or second phase. If the 9010A detects any decoding errors in the RAM address block, it displays the following message:

RAM DCD ERR @ aaaa BIT dd-LOOP?

The decimal number *dd* can range from 0-31 and corresponds to the number of the address bit that the 9010A detects is not being decoded properly. The 9010A detects that the μP writes to the same location whether *dd* equals one or zero. The address *aaaa* is the address with bit *dd* equal to zero. To illustrate this type of error, consider the following error message:

RAM DCD ERR @ 0FE0 BIT 4-LOOP?

To understand this message more clearly, examine the binary values of the addresses 0FE0 and 0FF0.

```
0FE0 = 0000 1111 1110 0000
0FF0 = 0000 1111 1111 0000
                     ↑
                   bit 4
```

What the error message example indicates is that address bit 4 does not function properly to distinguish between addresses 0FE0 and 0FF0.

When looping on the error, the 9010A writes data to the address with the erroneous bit equal to one. Then the 9010A writes different data to the address with the erroneous bit equal to 0 and reads the data at the first address to see if the original

data changed. If the error is removed while looping, the following message is displayed:

RAM DCD OK @ 0FE0 BIT 4

The RAM Short decoding test, which is relatively fast, is not guaranteed to find all decoding errors. However, it has a very high probability of finding errors and is guaranteed to find 100 per cent of the decoding errors that affect all data bits. The RAM Long decoding test, which takes longer to perform, guarantees to find all decoding errors, even those that affect only a single data bit at a single pair of locations.

4H-17. RAM LONG

The RAM Long test requires more time to perform than RAM Short, but is more comprehensive. RAM Long performs all the test operations performed during RAM Short, as well as an elaborate pattern sensitivity test that is able to identify elusive RAM errors.

4H-18. Specification of RAM Long

The steps required to select and specify RAM Long are identical to the steps required to select and specify RAM Short. To select RAM Long, press RAM LONG. Then enter the first and second address as prompted.

4H-19. Performance of RAM Long

After the specifications are complete, the 9010A begins performance of RAM Long. RAM Long is performed on each address block specified. After RAM Long is completed, the 9010A appends an OK or FAIL to the message on the display.

Performance of RAM Long consists of four phases. Each phase performs unique operations during testing and looping on errors and has unique error messages. The first three performance phases are the same as the three performance phases of RAM Short. Refer to the RAM Short test for a description of the operations and messages. The first three performance phases are as follows:

1. A test of the read-write capability of every data bit of every address location in the address block.

2. A test for data lines tied together.

3. A comprehensive test for decoding errors within the address block.

The fourth performance phase is as follows:

4. A test for pattern sensitivity.

The fourth phase is not performed if any errors remain from the first, second, or third phases. If the 9010A identifies any pattern sensitive errors, it places the first line of the following two-line message on the display:

RAM PATT ERR @ aaaa- LOOP?
DATA WAS xxxx NOT hhhh-LOOP?

While looping on the error, the 9010A writes the expected data to the address where the error was detected. Then the 9010A writes data to all the other address locations

in the RAM address block and verifies the data in the original location. If the error is removed while looping, the following message is displayed:

RAM PATT OK @ aaaa

4H-20. AUTO TEST

The Auto Test is a combination of four other tests: Bus Test, ROM Test, RAM Short, and I/O Test. Auto Test is selected by pressing the AUTO TEST key. During execution, the 9010A displays the following message (unless there are error messages):

AUTO TEST WAIT

After the test is completed, the 9010A replaces WAIT with an OK or FAIL. The actions performed by the 9010A are identical to the actions specified previously for the sequence of four tests that comprise Auto Test. The tests are performed in the order listed. The specifications for ROM Test, RAM Short, and I/O Test are the default specifications supplied by the UUT address descriptors. The error messages, the actions taken while looping on errors, and the associated messages are identical to those in the individual tests. Note that the operation of the RPEAT, LOOP, and STOP keys applies to the entire sequence of 9010A actions specified for Auto Test.

4H-21. DEFAULTS

During the specification of ROM Test, I/O Test, RAM Short, or RAM Long, the operator may press ENTER and cause the 9010A to supply default values for many of the prompted values. For example, when the 9010A prompts for the first address for the I/O Test, ROM Test, RAM Short, or RAM Long, the operator may default the entire specification for the test by pressing the ENTER key. The 9010A supplies all UUT address descriptors that are stored in the 9010A memory for that type of memory (I/O, ROM, or RAM). The 9010A then performs the test using the specifications provided by the descriptors (including all address, ROM signature, and I/O bit mask information). For example, assume the Learn operation is performed and the following two descriptors are obtained for RAM:

RAM @ 2000-20FF
RAM @ 4000-41FF

When the 9010A prompts for the first address and the operator presses the ENTER key, the 9010A performs the RAM Test over the two address blocks specified by the descriptors. The relevant display messages, prompted values, and default values are listed in Appendix B.

Section 4I
Troubleshooting Functions

4I-1. INTRODUCTION

The troubleshooting functions allow the operator to concentrate the scope of troubleshooting activity to the stimulation or monitoring of particular address locations or bits on the UUT μP bus. The keys associated with these functions are identified in Figure 4I-1.

Six of the functions are selected by single keystrokes. The keys are listed as follows: READ, WRITE, RAMP, WALK, TOGGL ADDR, and TOGGL DATA. Three of the troubleshooting functions are selected by the combined use of the STS/CTL (Status/Control) key and three of the function keys. The STS/CTL troubleshooting functions are listed as follows: READ STS, WRITE CTL, and TOGGL DATA CTL.

The specification and execution of all the troubleshooting functions are described in the following paragraphs. There are no error messages unique to the troubleshooting functions, although the timeout and UUT system errors may be detected and reported as usual. (The one exception to this is Read STS, during which only timeout errors may be reported, and not UUT system errors.) Note that the RPEAT, LOOP, and STOP keys may be used with any of the functions. A summary of the display messages, prompts, and default values is provided in Appendix B.

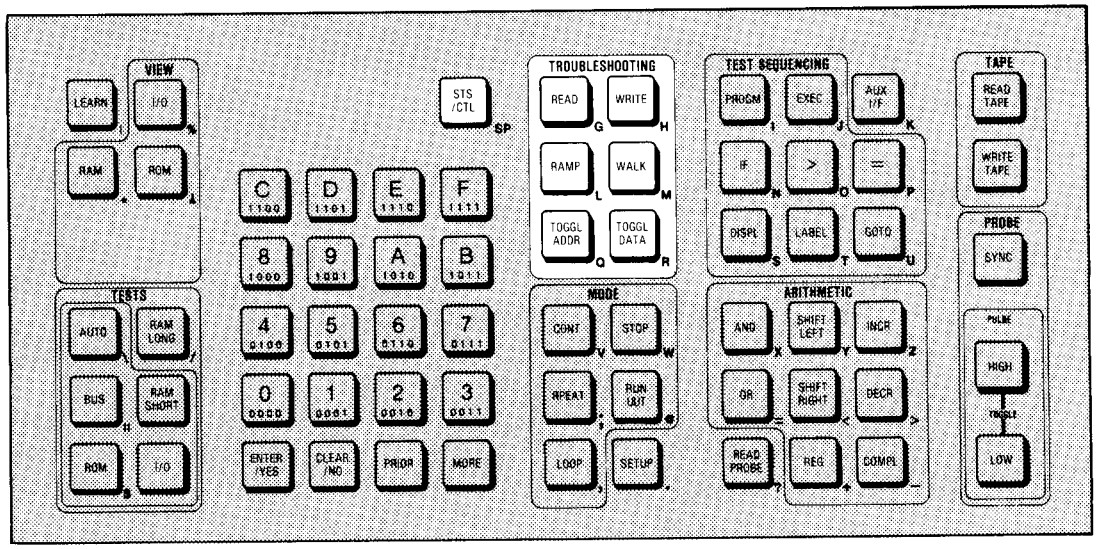


Figure 4I-1. Keys Used for Troubleshooting Functions

4I-2. READ

The Read function causes the 9010A to read the data at an operator-specified location and display the contents.

To select the Read function, do the following:

1. Press READ. The 9010A prompts for the address where the read operation is to take place by displaying the following message:

   READ @ _

2. Key in the address *aaaa* and press ENTER. The 9010A displays the following message:

   READ @ aaaa WAIT

After the specification is complete, the 9010A reads the data at the specified address and displays the data *hhhh* (in hexadecimal) along with an OK or FAIL as follows:

READ @ aaaa = hhhh OK
READ @ aaaa = hhhh FAIL

4I-3. READ STS

The Read STS function causes the 9010A to read the status lines on the μP and display their values.

To select the Read STS function, press the READ key and then the STS/CTL key. The 9010A displays the following message:

READ @ STS WAIT

The 9010A reads the status lines and places the following message on the display:

D @ STS = nnnn nnnn nnnn nnnn OK

Note in the message listed that the 9010A truncates the message on the left so that the pertinent portion of the message is displayed. The binary string *nnnn nnnn nnnn nnnn* represents the 16 possible status lines. A one corresponds to lines that are detected high, and a zero corresponds to lines that are detected low. A microsystem may have 16 or fewer status lines. The status lines for each particular microsystem are documented in the appropriate interface pod manual. The binary strings representing the status lines are always displayed in groups of four. If a μP has 9-12 meaningful status lines, only three groups of four digits are displayed. If a μP has eight or fewer meaningful status lines, only two groups of four digits are displayed. Refer to the appropriate interface pod manual for the meaning of each bit in the string.

4I-4. WRITE

The Write function causes the 9010A to write operator-specified data to an operator-specified address.

To select the Write function, do the following:

1. Press the WRITE key. The 9010A prompts for the address to be written to by displaying the following message:

   WRITE @ _

2. Key in the address *aaaa* and press ENTER. The 9010A prompts for the data to be written by displaying the following message:

WRITE @ aaaa = _

3. Key in the data *hhhh* and press ENTER. The 9010A displays the following message:

WRITE @ aaaa = hhhh WAIT

After the specification is complete the 9010A writes the specified data to the specified address. When the operation is complete, the 9010A replaces WAIT with an OK or FAIL.

4I-5. WRITE CTL

The Write CTL function causes the 9010A to write operator-specified control lines to the operator-specified logic levels.

To select the Write CTL function, do the following:

1. Press the WRITE key and then the STS/CTL key. The 9010A prompts for the binary string specifying the values to write to the control lines by displaying the following message:

WRITE @ CTL = _

2. Key in the desired control information in binary and press ENTER. The 9010A accepts any binary value from 0 to 11111111. The 9010A displays the following message:

WRITE @ CTL = bbbbbbbb WAIT

The binary string *bbbbbbbb* corresponds to the eight possible UUT control lines. The 9010A forces control lines represented by a one high, and forces control lines represented by a zero low. The control lines for each microsystem are documented in the appropriate interface pod manual. Note that the 9010A supplies the value zero for any lines not specified by the operator. Values that are specified for nonexistent control lines are ignored by the 9010A when the function is performed.

After the specification is complete, the 9010A writes the UUT control lines as specified and replaces WAIT with an OK or FAIL.

4I-6. RAMP

The Ramp function causes the 9010A to perform a series of write operations, beginning with all data bits equal to zero, and increasing until all data bits equal one.

To select the Ramp function, do the following:

1. Press the RAMP key. The 9010A prompts for the address where the operation is to be performed by displaying the following message:

RAMP @ _

2. Key in the address *aaaa* and press ENTER. The 9010A displays the following message:

RAMP @ aaaa WAIT

After the specification is complete, the 9010A performs a series of write operations at address *aaaa*. The write operations begin with all data bits equal to zero. The value of the data for each successive write operation increases by one until all data bits are equal to one.

Two views of the Ramp function for an eight-line data bus are presented in Figure 4I-2. The binary values of the data lines are presented at the top. The voltage levels of the same data lines are presented at the bottom as they might appear on a logic analyzer. Note that the frequencies of the data lines are binary divisions of the highest frequency, the data line zero. Only part of the Ramp function is illustrated in Figure 4I-2. After the Ramp function is completed, all bits at the address where the function is performed equal one.

Note that during the write operations the 9010A continues to display the name of the function and the specified address. When the write operations are complete, the 9010A replaces WAIT with an OK or FAIL.

Note that the amount of time required to perform the Ramp function varies greatly, depending on the number of bits in the data bus. For example, while an 8-bit Ramp function is performed in about 1 second, and a 16-bit Ramp function is performed within minutes, a 32-bit Ramp function would take much longer.

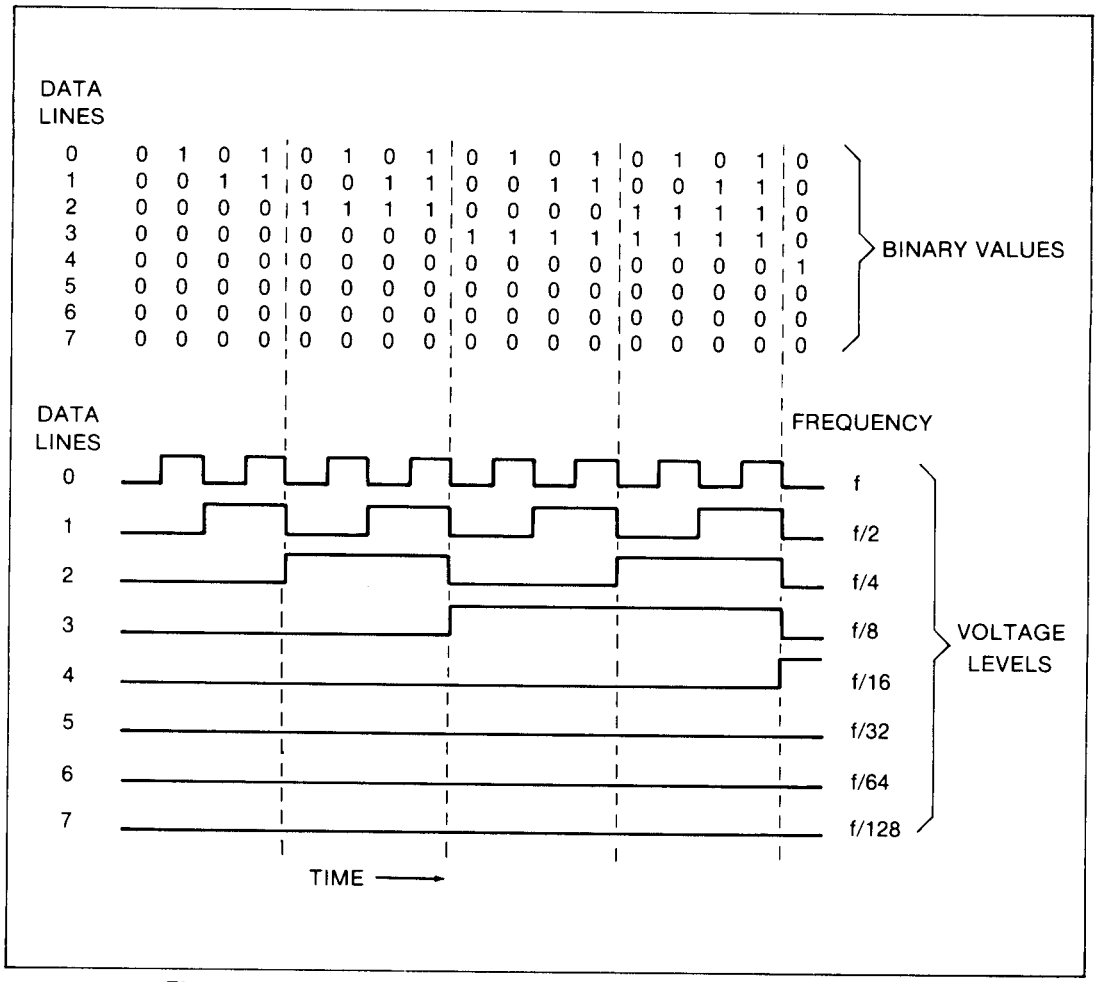


Figure 4I-2. Ramp Function with Binary Values and Voltage Levels

41-7. WALK

The Walk function causes the 9010A to perform a series of write operations at an operator-specified address. First the 9010A writes operator-specified data, then rotates the data one bit, and writes the new data. This process continues until the data is rotated around completely. To select the Walk function, do the following:

1. Press the WALK key. The 9010A prompts for the address where the operation is to be performed by displaying the following message.

   WALK @ _

2. Key in the address and press ENTER. The 9010A prompts for the data for the Walk function by displaying the following message:

   WALK @ aaaa = _

3. Key in the data *hhhh* in hexadecimal and press ENTER. The 9010A accepts hexadecimal values for the data specification. The 9010A displays the following message:

   WALK @ aaaa = hhhh WAIT

After the specification is complete, the 9010A performs the write operations associated with the Walk function at the address *aaaa.* First the 9010A writes *hhhh.* Then it rotates the data to the right, wrapping the lowest bit around to the highest bit position, and writes the resulting data. This rotate and write process continues until the bits have been rotated around to their original position.

The following example illustrates the eight write operations performed by the Walk function on an eight-line data bus. The data specification is entered into the 9010A in hexadecimal (F0), but to make the rotate process easier to see, it is shown here in binary (11110000):

11110000
01111000
00111100
00011110
00001111
10000111
11000011
11100001

Note the during the write operations associated with the Walk function, the 9010A displays the following message:

WALK @ aaaa = hhhh WAIT

When the write operations are complete, the 9010A replaces WAIT with an OK or FAIL.

41-8. TOGGL ADDR

The Toggle Address function causes the 9010A to toggle an operator-specified address bit from one logic state to the other. To select the Toggle Address function, do the following:

1. Press the TOGGL ADDR key. The 9010A prompts for the first address where the operation is to be performed by displaying the following message:

ATOG @ _

2. Key in the address and press ENTER. The 9010A prompts for the address bit that is to be toggled by displaying the following message:

ATOG @ aaaa BIT _

3. Key in the address bit *dd* that is to be toggled. The 9010A accepts any decimal value from 0 to 31 for the address bit. The 9010A displays the following message:

ATOG @ aaaa BIT dd WAIT

When the specification is complete, the 9010A performs two read operations, each at a different address. First the 9010A reads the data at the address specified. Then the 9010A toggles the address bit specified, changing it to the opposite logic level, and reads the data at the resultant address. Note that the data that is read is not presented on the display. While the 9010A performs the two read operations, the 9010A displays the following message:

ATOG @ aaaa BIT dd WAIT

When the two read operations are completed, the 9010A replaces WAIT with an OK or FAIL.

The following example shows the proper steps for specifying TOGGL ADDR at address 1A00 with address bit 3 toggled, and the corresponding display messages:

PRESS	DISPLAY
TOGGL ADDR	*ATOG @ _*
1A00 ENTER	*ATOG @ 1A00 BIT _*
3 ENTER	*ATOG @ 1A00 BIT 3 WAIT*

At this point the 9010A reads the data at address 1A00. Then the 9010A toggles address bit 3, creating the new address 1A08. This is illustrated in binary as follows:

1A00 = 0001 1010 0000 0000
1A08 = 0001 1010 0000 1000
↑
bit 3

After creating the address 1A08, the 9010A reads the data at 1A08.

Note that the Toggle Address Function is particularly useful in tracing and troubleshooting address decode problems.

4I-9. TOGGL DATA

The Toggle Data function causes the 9010A to toggle an operator-specified data bit from one logic state to the other.

To select the Toggle Data function, do the following:

1. Press the TOGGL DATA key. The 9010A prompts for the address where the operation is to be performed by displaying the following message:

DTOG @ _

2. Key in the address and press ENTER. The 9010A prompts for the data that is to be written by displaying the following message:

DTOG @ aaaa = _

3. Key in the data and press ENTER. The 9010A prompts for the bit number of the data bit that is to be toggled by displaying the following message:

DTOG @ aaaa = hhhh BIT _

4. Key in the data bit *dd* in decimal and press ENTER. The 9010A accepts any decimal value from 0 to n-1 where n equals the number of data lines for the μP. The 9010A displays the following message:

DTOG @ aaaa = hhhh BIT dd WAIT

After the specification is complete, the 9010A performs two write operations at the same address. First the 9010A writes the specified data to the specified address. Then the 9010A toggles the specified data bit, changing its logic level to the opposite value, and writes the resulting data to the specified address. While the 9010A performs the two write operations, the following message is displayed:

DTOG @ aaaa = hhhh BIT dd WAIT

When the two write operations are completed, the 9010A replaces WAIT with an OK or FAIL. After the Toggle Data function is performed, the toggled data (from the second write operation) remains in the address where the function is performed.

The following example shows the proper steps for the specification of Toggle Data for a 16-bit μP, and the corresponding display messages. Toggle Data is specified with address D407, data FF00, and data bit 5 to be toggled:

PRESS	DISPLAY
TOGGL DATA	*DTOG @_*
D407 ENTER	*DTOG @ D407 =_*
FF00 ENTER	*DTOG @ D407 = FF00 BIT _*
5 ENTER	*DTOG @ D407 = FF00 BIT 5 WAIT*

At this point the 9010A writes FF00 to address D407. Then the 9010A toggles data bit 5, creating the new data value FF20. This is illustrated in binary as follows:

```
FF00 = 1111 1111 0000 0000
FF20 = 1111 1111 0010 0000
                    ↑
                  bit 5
```

The 9010A writes FF20 to address D407.

Note that the Toggle Data function is particularly useful in tracing and troubleshooting data lines up to and beyond peripheral IC's

4I-10. TOGGL DATA CTL

The Toggle Data Control function causes the 9010A to toggle an operator-specified control line from one logic state to the other.

To select the Toggle Data Control function, do the following:

1. Press the TOGGL DATA key and then the STS/CTL key. The 9010A prompts for the binary string specifying the values to write to the control lines by displaying the following message:

   DTOG @ CTL =_

2. Key in the desired control information in binary and press ENTER.

   The 9010A accepts any binary value from 0 to 11111111. The binary values entered correspond to the UUT control lines. The 9010A forces control lines represented by a one high, and forces control lines represented by a zero low. The control lines for each microsystem are documented in the appropriate interface pod manual. Note that the 9010A supplies the value zero for any lines not specified by the operator.

   The 9010A accepts the binary string *bbbbbbbb* and prompts for the bit number of the control line that is to be toggled by displaying the following message:

   DTOG @ CTL = bbbbbbbb BIT _

3. Key in the bit number *d* in decimal. The 9010A accepts any decimal value from 0 to 7 for the bit number of the control line. The 9010A displays the following message:

   DTOG @ CTL = bbbbbbbb BIT d WAIT

When the specification is complete, the 9010A performs two write operations. First the 9010A writes the control lines as specified. Then the 9010A toggles the specified bit, changing its logic level to the opposite value. Then the 9010A again writes the control lines, with the line corresponding to the toggled bit written to the opposite value. After the write operations are completed, the 9010A replaces WAIT with an OK or FAIL.

The following example shows the proper steps for toggling the INTE control line for an 8080 microsystem. The INTE control line corresponds to bit 2.

PRESS	DISPLAY
TOGGL DATA	*DTOG @ _*
STS/CTL	*DTOG @ CTL = _*
10 ENTER	*DTOG @ CTL = 10 BIT _*
2 ENTER	*DTOG @ CTL = 10 BIT 2 WAIT*

At this point the 9010A performs the two write operations. First it writes the control lines as specified. Then it toggles bit 2 (from 1 to 0) and writes the control lines accordingly. Note that the control lines not specified default to zero.

Section 4J
Using the Registers

4J-1. INTRODUCTION

This section describes how to load and manipulate the contents of the sixteen 32-bit registers in the Immediate Mode. The function of both dedicated and non-dedicated registers is described, and the Arithmetic keys (see Figure 4J-1) are defined and discussed. Applications are also provided showing how to use the Arithmetic keys and the registers when entering data during the specification of tests, functions, or operations.

4J-2. TYPES OF REGISTERS

The function of all the dedicated and non-dedicated registers is described in Table 4J-1. The operator may directly load and manipulate the contents of any of the seven dedicated and nine non-dedicated registers. The seven dedicated registers may also be loaded by the 9010A software. For example, any time the operator enters a data specification or the 9010A performs an operation which places data on the data bus, the 9010A software loadsthe data into Register E. Or any time the operator enters an address specification or the 9010A performs an operation which places an address on the address bus, the 9010A software loads the address into Register F. The nine non-dedicated registers are not loaded by the 9010A software, but are reserved solely for the use of the operator.

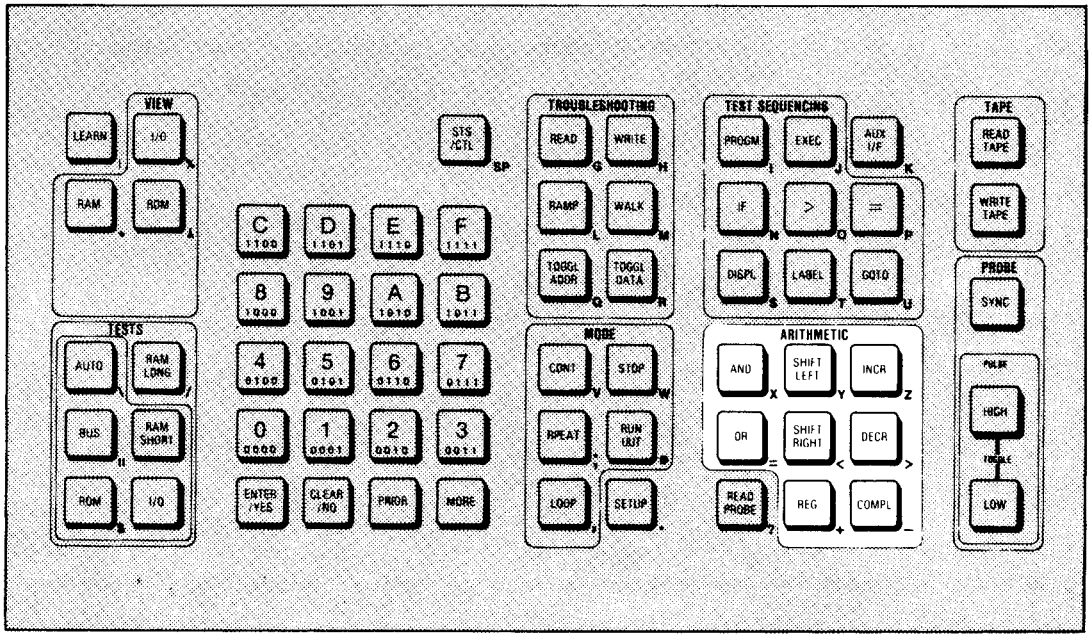


Figure 4J-1. The Eight ARITHMETIC Keys

Table 4J-1. Function of the Sixteen 32-bit Registers

TYPE OF REGISTER	REGISTER	FUNCTION
Dedicated*	A	Stores the last bit mask specified by the operator. Also, if the UUT I/O address descriptors are invoked as default values when the I/O Test is performed, the bit mask specified by the last I/O address descriptor is stored in Register A.
	B	Stores the last ROM signature specified by the operator. Also, if the UUT ROM address descriptors are invoked as default values when the ROM Test is performed, the ROM signature specified by the last ROM address descriptor is stored in Register B.
	C	Stores the last status/control information specified by the operator for Write Control or Toggle Data Control, or generated by the 9010A during Read STS.
	D	Stores the last bit number (in the range 0-31) specified by the operator for the Toggle Address, Toggle Data, or Toggle Data Control functions.
	E	Stores the last data specified by the operator or generated by the 9010A during operation.
	F	Stores the last address specified by the operator or generated by the 9010A during an operation involving the interface pad.
	O	Stores data accumulated during the Read Probe operation.
Non-Dedicated	1-9	Non-dedicated registers for sole use by the operator for storage and manipulation of data as specified by operator.
*Also available to the operator for storage and manipulation of data.		

Note that the fact that the 9010A software may load values into the dedicated registers does not prevent the operator from directly loading values into the dedicated registers with the Arithmetic keys. Note also that the values contained in the dedicated registers are the default values supplied by the 9010A as required during the specification of troubleshooting functions. If power is removed from the 9010A and then reapplied, the contents of each register are set to zero.

4J-3. DEFINING THE ARITHMETIC KEYS

The location of the eight Arithmetic keys is shown in Figure 4J-1. The keys consist of five unary operators, two binary operators, and one register selection key:

Register Selection	Unary Operators	Binary Operators
REG	INCR	AND
	DECR	OR
	COMPL	
	SHIFT LEFT	
	SHIFT RIGHT	

- REG allows the operator to specify any one of the 16 registers for use in performing an operation or for examining or entering data into a register.

The unary operators are called unary operators because they specify operations which may be performed on only one register at a time. The function of the five unary operator keys is described as follows:

- INCR increments the binary value of a register by one.
- DECR decrements the binary value of a register by one.
- COMPL replaces the value stored in the register with its binary ones complement.
- SHIFT LEFT shifts the binary contents of the register one bit to the left. The farthest left bit is discarded; the farthest right bit becomes zero.
- SHIFT RIGHT shifts the binary contents of the register one bit to the right. The farthest right bit is discarded; the farthest left bit becomes zero.

The binary operators are called binary operators because they perform an operation with two registers or with a register and a hexadecimal value. The function of the binary operator keys is described as follows:

- AND performs the logical bit-wise AND operation between two registers or a register and a hexadecimal value. The rules for the logical AND operation are as follows:

  1 AND 1 = 1
  1 AND 0 = 0
  0 AND 1 = 0
  0 AND 0 = 0

- OR performs the logical bit-wise OR operation between two registers or a register and a hexadecimal value. The rules for the logical OR operation are as follows:

  1 OR 1 = 1
  1 OR 0 = 1
  0 OR 1 = 1
  0 OR 0 = 0

Examples of the function of the unary and binary operators and the register selection key are provided in Table 4J-2.

4J-4. ENTERING DATA INTO A REGISTER

Any hexadecimal value in the range 0 to FFFFFFFF may be entered into a register. The following example shows the keystrokes needed to place the value 40CC into Register 2.

PRESS	DISPLAY
REG 2	*REG2 = _*
40CC ENTER	*REG2 = 40CC*

4J-5. EXAMINING THE CONTENTS OF A REGISTER

The following example shows the keystrokes needed to examine Register 2 and the corresponding display messages. Assume in the example that Register 2 contains the value 40CC.

Table 4J-2. Unary and Binary Operators

For these examples, assume Register 5 = 000000DF
Register E = 000000F4

Note that operations involving Register 5 use the value obtained from the previous operation.

Press	Display	Comment
REG 5 ENTER	*REG5 = DF*	Examine contents of Register 5
INCR 5	*INC REG5 = EO*	Increment the contents of Register 5
DECR 5	*DEC REG5 = DF*	Decrement the contents of Register 5
COMPL 5	*CPL REG5 = FFFFFF20*	Complement the contents of Register 5 (complement of DF = FFFFFF20 for the 32-bit register)
SHIFT LEFT 5	*SHL REG5 = FFFFFE40*	Examine the previous contents of Register 5 in hexadecimal and binary: FFFFFF20 (hexadecimal) = 1111 1111 1111 1111 1111 1111 0010 0000 (binary) After the shift left: FFFFFE40 (hexadecimal) = 1111 1111 1111 1111 1111 1110 0100 0000 (binary)
SHIFT RIGHT 5	*SHR REG5 = 7FFFFF20*	Note the contents of Register 5 from the previous operation. After the shift right operation the contents are: 7FFFFF20 (hexadecimal) = 0111 1111 1111 1111 1111 1111 0010 0000 (binary)
REG 5 AND	*REG5 = 7FFFFF20 AND_*	The contents of Register 5 are displayed along with a prompt for a register or hexadecimal number following the AND.
REG E ENTER	*REG5 = 20*	The logical AND operation is performed and the contents are placed in Register 5. 7FFFFF20 logical AND with 000000F4 equals 00000020
REG 5 OR	*REG5 = 20 OR _*	The contents of Register 5 are displayed along with a prompt for a register or hexadecimal number following the OR.
REG E ENTER	*REG5 = F4*	The logical OR operation is performed and the contents are placed in Register 5. 00000020 logical OR with 000000F4 equals 000000F4

PRESS	DISPLAY
REG	*REG_*
2	*REG2 = _*
ENTER	*REG2 = 40CC*

4J-6. USING REGISTERS FOR DATA ENTRY

Any time the 9010A displays a prompt for entry of a hexadecimal value, the operator may also enter the contents of a register with the REG key. For example, when the 9010A displays a prompt for an address, the contents of a register may be entered. The following example shows the keystrokes necessary to enter the contents of Register 8 when specifying the READ troubleshooting function. Assume in this example that Register 8 contains the value 7A30.

PRESS	DISPLAY
READ	*READ @ _*
REG	*READ @ REG_*
8	*READ @ 7A30 _*
ENTER	*READ @ 7A30 = hhhh OK*

Note that as soon as the register is specified, the prompt for the register number (REG_) is replaced by the register contents. In this case, when the register contents are entered and the ENTER key is pressed, the specification is complete, and the 9010A performs the Read operation as specified. Other 9010A functions and operations accept the entry of register contents in the same manner as shown in this example.

4J-7. ARITHMETIC OPERATIONS DURING DATA ENTRY

The operator may also use the unary and binary operators to modify the contents of a register and then enter the register contents. There are particularly powerful applications when the operators are used with the dedicated registers that store default values. The following examples show how the operators may be used during data entry.

4J-8. Performing Operations at Sequential Addresses

The INCR and DECR keys can provide shortcuts when specifying data for operations that are to be performed at sequential addresses. For example, assume that the operator wants to examine the data at five sequential address locations, from A000 to A004. The following example shows how to specify and examine the locations sequentially, using the INCR key.

PRESS	DISPLAY	COMMENT
READ	*READ @ _*	Prompt for address.
A000 ENTER	*READ @ A000 = hhhh OK*	The operation is performed at the first address.
READ	*READ @_*	Prompt for address.
INCR	*READ @ A001_*	When the INCR key is pressed, the contents of the default register (Register F) are incremented and entered.

continued

PRESS	DISPLAY	COMMENT
ENTER	*READ @ A001 = hhhh OK*	The operation is performed at the second address.
READ INCR ENTER	*READ @ A002 = hhhh OK*	The operation is performed at the third address.
READ INCR ENTER	*READ @ A003 = hhhh OK*	The operation is performed at the fourth address.
READ INCR ENTER	*READ @ A004 = hhhh OK*	The operation is performed at the fifth address.

4J-9. Complementing a Value with the CPL and the AND Keys

Sometimes the operator may want to complement a value at a particular address location. For example, assume that the operator knows that the address 2010 contains the data 55. The operator wants to obtain the ones complement of 55 and write the new value to the address. The microsystem stores 8-bit data. The following steps show how this is accomplished.

PRESS	DISPLAY	COMMENT
READ 2010 ENTER	*READ @ 2010 = 55 OK*	This step is done to verify that address 2010 contains 55, and to place the values 2010 and 55 in the address and data default registers.
WRITE ENTER	*WRITE @ 2010 = _*	This step invokes the default address 2010.
COMPL	*WRITE @ 2010 = FFFFFFAA_*	This step complements and displays the value contained in the data default register (55). But this value is the 32-bit complement of 55, which is too large to write to the 8-bit microsystem.
AND FF	*WRITE @ 2010 = FFFFFFAA AND FF_*	The AND operation is used with FF to "mask off" the unwanted upper 24 bits. FFFFFFAA AND 000000FF = AA
ENTER	*WRITE @ 2010 = AA OK*	The 9010A performs the specified operation.

4J-10. Turning Bits On with the OR Key

Often it is useful to turn a bit on (set it equal to 1). For example, consider a bank-switched RAM which is switched according to the values of the fourth and fifth bits of the data at a PIA (peripheral interface adapter). The address of the PIA is 40FF. When the fourth and fifth bits of the data at address 40FF equal 1, one bank of RAM is selected. When the fourth and fifth bits of the data at address 40FF equal 0, another bank is selected. The following steps show how this is accomplished.

PRESS	DISPLAY	COMMENT
READ 40FF ENTER	*READ @ 40FF = A3 OK*	The data at the PIA is A3 (hexadecimal) or 1010 0011 (binary). Note that the fourth and fifth bits equal 0.
WRITE ENTER	*WRITE @ 40FF = _*	The default value 40FF is supplied for the address.
REG E	*WRITE @ 40FF = A3 _*	Register E is specified because it contains the data that is to be modified.
OR 18	*WRITE @ 40FF = A3 OR 18_*	The value 18 is selected for the OR operation because the fourth and fifth bits equal 1 (0001 1000).
ENTER	*WRITE @ 40FF = BB OK*	A3 (1010 0011) OR 18 (0001 1000) = BB (1011 1011) The new data is written to the PIA, which changes the fourth and fifth bits to one, thus selecting the other bank of RAM.

Note that the AND key may be used in a similar manner to turn bits off.

Section 4K
Troubleshooting with the Probe and a Scope

4K-1. INTRODUCTION

This section describes the use of the probe and an oscilloscope. It describes both stimulus and response modes of probe operation, probe and scope synchronization, and some basic techniques for using the probe. The probe control keys are shown in Figure 4K-1. The probe electrical specifications are shown in Table 4K-1.

NOTE

Each probe is factory-calibrated for compatibility with the particular main instrument with which it is shipped. If the probe is used with another 9010A, the probe may not perform within the specifications listed. During normal use the probe requires calibration only once a year. Probe calibration (listed under probe compensation) is described in the 9010A Service Manual.

4K-2. CONNECTING THE PROBE TO THE 9010A

CAUTION

Do not proceed with probe operation unless the probe ground clip is connected to a ground connection on the UUT. Failure to connect the probe ground clip could result in damage to the 9010A.

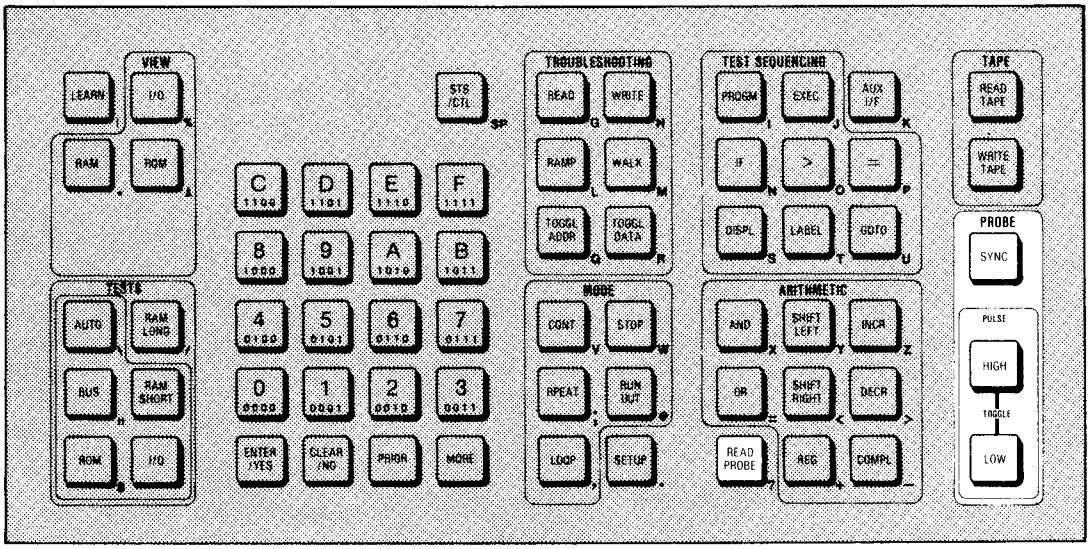


Figure 4K-1. The Probe Control Keys

The probe cable plugs into a connector which is located on the front base of the main instrument under the keyboard (see Figure 4K-2). The probe cable is connected in the same way as the interface pod cable. To connect the probe cable, follow these steps:

1. Tip up the front of the main instrument to allow access to the connector.

2. Slide the metal collar on the cable plug to the left.

3. Plug the cable into the connector and slide the collar to the right so that it locks over the small metal posts on the connector. The plug should now be firmly locked in place.

4. Connect the probe ground clip to the UUT ground.

Table 4K-1. Probe Electrical Specifications

STIMULUS MODE	
Stimulus Pulse Width:	
ADDRESS OR DATA VALID SYNC	Equals address valid or data valid interval of the interface pod μP
FREE-RUN	2 μsec nominal
Stimulus Pulse Amplitude	High: >4V at + 100 mA Low: <0.2V at -100 mA
RESPONSE MODE	
INDICATOR THRESHOLD	Logic High (Red): >2.4V Logic Low (Green): <0.8V Logic Invalid: >2.4V and <0.8V
INDICATOR THRESHOLD ACCURACY	+/-0.2V
INDICATOR MINIMUM PULSE WIDTH	Logic High: >75 ns Logic Invalid >100 ns Logic Low: >75 ns
MAXIMUM SAFE INPUT VOLTAGE AT PROBE TIP: ...	-30 dc to +30V dc

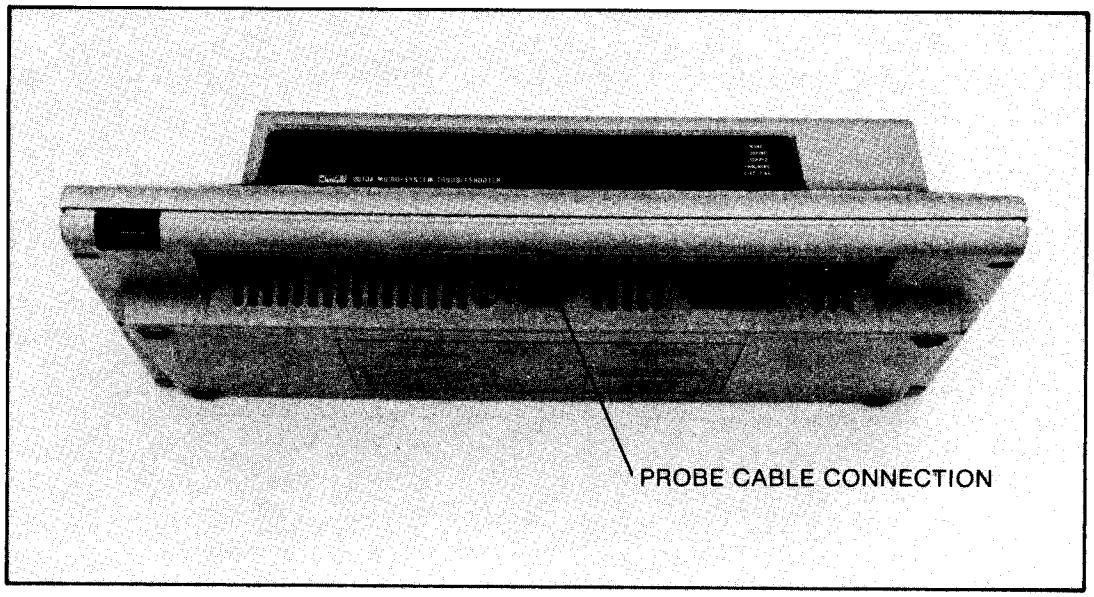


Figure 4K-2. Probe Connection

Note that if an interface pod is connected to the UUT and the operator connects the probe ground clip to the UUT supply, the probe fuse will blow. Refer to Section 2-4 for information about probe fuse replacement.

4K-3. SYNCHRONIZATION

The operator may synchronize the probe stimulus or probe response operation to events on the μP bus. There are three possible synchronization modes: address sync (valid address periods), data sync (valid data periods), or free-run (asynchronous).

Synchronization modes are selected with the SYNC key. To select the desired synchronization mode, do the following:

1. Press the SYNC key. The 9010A prompts for the synchronization mode desired by displaying the following message:

   SYNC MODE <0-F>_

2. Select one of three modes by pressing the appropriate key as shown below:

DESIRED MODE	PRESS	DISPLAY
Valid Address	A	*SYNC MODE <0-F>ADDRESS OK*
Valid Data	D	*SYNC MODE <0-F> DATA OK*
Free-Run	F	*SYNC MODE <0-F> FREE-RUN OK*

Depending on the interface pod, other synchronization modes may be available. When the 9010A first receives power free-run is selected.

Whenever a synchronization mode is selected by pressing key A, D, or F, the 9010A clears any probe response data accumulated to that point. This is true even if the mode selected is the same as the mode in use. To determine the synchronization mode presently in use without clearing the accumulated probe response, press the SYNC key and then the ENTER key. The 9010A displays the mode in use.

The relationship between synchronization and probe use is summarized in Table 4K-2. More information is provided about each type of probe use in the following paragraphs.

4K-4. PROBE STIMULUS WITH THE HIGH AND LOW KEYS

The probe is capable of producing stimulus pulses that may be used to force μP bus lines high or low. The two push-push keys, HIGH and LOW, determine which stimulus the 9010A generates. Refer to Table 4K-3 for the type of stimulus generated.

If the probe is in free-run, the pulses are generated at a frequency of approximately 1 kHz. If the probe is in address sync or data sync, the frequency of pulse generation varies, depending on the type of μP and the UUT clock. The stimulus pulse width in free-run is approximately 2 μs. The stimulus pulse width in one of the synchronized modes is equal to the sync pulse width for the interface pod μP.

4K-5. PROBE RESPONSE WITH THE READ PROBE KEY

The Read Probe operation allows the operator to observe probe response data gathered at the probe tip. Response data includes an event count, a history of the logic levels detected, and a signature that is computed from successive logic states.

Table 4K-2. Relationship of Probe Use to Synchronization

PROBE USE	ADDRESS OR DATA SYNC	FREE-RUN
PROBE STIMULUS (determined by HIGH and LOW keys)	One pulse per address or data valid period. Pulse equals period in length.	2 μs pulses at 1 kHz.
PROBE RESPONSE (start and stop points determined by Read Probe operation)		
Event Count*	Counts all events (unaffected by sync).	Counts all events.
Signature Gathering	Counts only during address or data valid period.	No signatures gathered in free-run.
Logic Level History	Records only during address or data valid period (only high or low levels recorded, not invalid).	Records any levels at any time.
INDICATOR LIGHTS	Indicates probe tip activity only during address or data valid period.	Indicates probe tip activity during all times.

*An event occurs when a signal falls below the high threshold (+2.4V)

Table 4K-3. Probe Stimulus with the HIGH and LOW Keys

HIGH KEY	LOW KEY	TYPE OF STIMULUS GENERATED
In	Out	High pulses.
Out	In	Low pulses.
In	In	Toggle between high and low pulses.
Out	Out	No stimulus generated.

The Read Probe operation is shown in Figure 4K-3. When the READ PROBE key is pressed, the data accumulated since the last time the READ PROBE key was pressed is shown on the display and placed in Register 0. For example, in Figure 4K-3, when the READ PROBE key is pressed at point B, the 9010A displays the data accumulated between point A and point B. The format for the Read Probe display message and the contents of Register 0 are shown in Table 4K-4.

Note that the Read Probe operation is a passive, data-displaying operation, and does not by itself provide any stimulus to the logic node where the probe is placed. The operator must cause the 9010A to perform a function (such as a Read, Write or Ramp function) which stimulates the node while the 9010A is accumulating data with the probe.

Note also that the probe detects all activity at the probe tip, including its own stimulus pulses. For this reason, it is usually a good practice to disable the probe stimulus capability while accumulating data for the Read Probe operation.

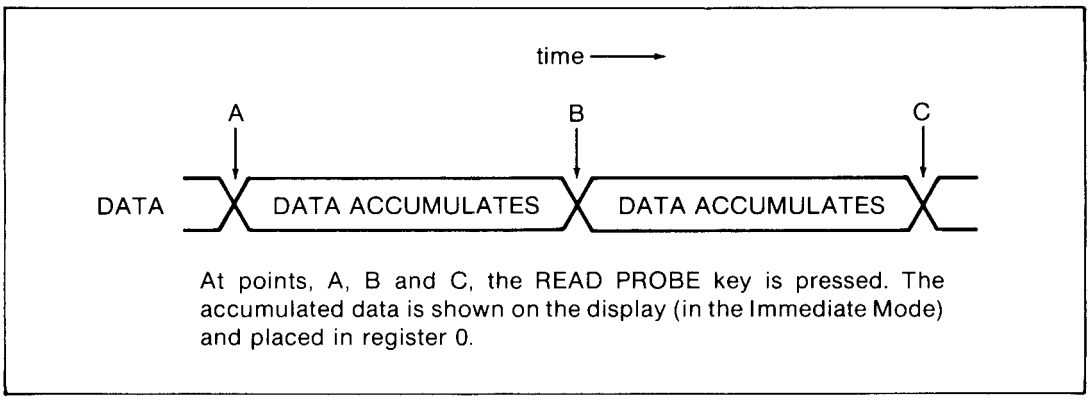


Figure 4K-3. Read Probe Operation

4K-6. Counting Events

The event counter allows the operator to verify that a given number of falling-edge events occur between two successive Read Probe operations. By doing this, it allows the operator to test circuits which are asynchronous to the bus.

The event counter is a 7-bit circular counter. Each time the READ PROBE key is pressed, the event count is displayed, the counter is set to zero, and the count begins again. When the counter reaches 127 counts, it starts over at zero. It does this continually as long as events occur. The event counter is unaffected by the synchronizationmode selected. It counts all events that occur at the probe tip, regardless of whether the probe is in address sync, data sync, or free-run.

It is important to note that the counter is incremented when the falling edge of the signal at the probe tip passes the +2.4V threshold (see Figure 4K-4). Therefore, if the signal is toggling between low and invalid levels (but never exceeding and falling below the +2.4V threshold), the 9010A does not register any counts.

4K-7. Logic Level History

When the READ PROBE key is pressed, any logic levels (high, invalid or low) that have been detected during the period since the last time the READ PROBE key was pressed are displayed. Note that the display message indicates the *history* of the logic levels, and not simply the logic level at the moment the READ PROBE key is pressed.

If the probe is in address sync or data sync, the logic levels are only recorded during the address valid or data valid periods. In free-run the logic levels are recorded for the entire time.

4K-8. Gathering Signatures

A signature is an algorithmic compression (cyclic redundancy check) of a digital bit stream into a four digit hexadecimal number. A given sequence of logic states at the probe tip produces a signature that characterizes that sequence. The idea of using signatures is to obtain them from data in a known-good UUT, and then compare the good values with values obtained from the suspect UUT.

The general procedure for gathering signatures is as follows:

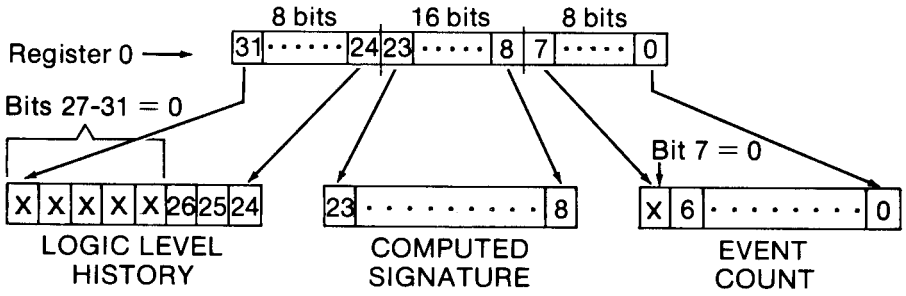
DISPLAY MESSAGE FORMAT: *PROBE-LVL abc COUNT ddd SIG nnnn*

a = *L* if logic low detected, blank otherwise
b = *X* if invalid logic level detected (this level is not detected in a synchronization mode), blank otherwise
c = *H* if logic high detected, blank otherwise
ddd = decimal number between 0 and 127
nnnn = hexadecimal signature between 0000 and FFFF

Example: *PROBE-LVL L H COUNT 060 SIG 264D*

This message indicates that the probe detected the low and high logic levels, 60 events were counted, and a signature of 264D was computed.

The probe response data is stored in bits 0-31 of Register 0 as follows:



Bit 24 = 1 if logic high detected

Bit 25 = 1 if logic invalid detected

Bit 26 = 1 if logic low detected

If register 0 is examined with the REG key, the contents are displayed as a seven-digit hexadecimal quantity. (Note that the eighth hexadecimal digit is always zero, and is not displayed). For the example above, the contents of Register 0 are displayed as the following:

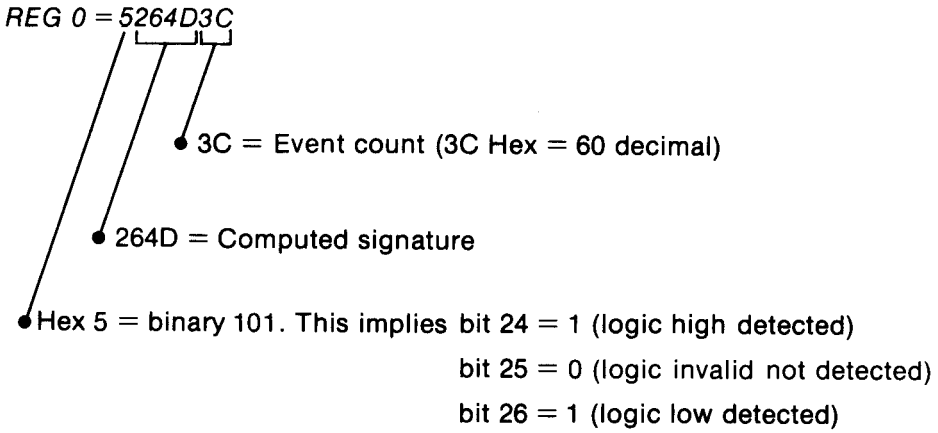


Table 4K-4. Format of Read Probe Display Message and Contents of Register 0

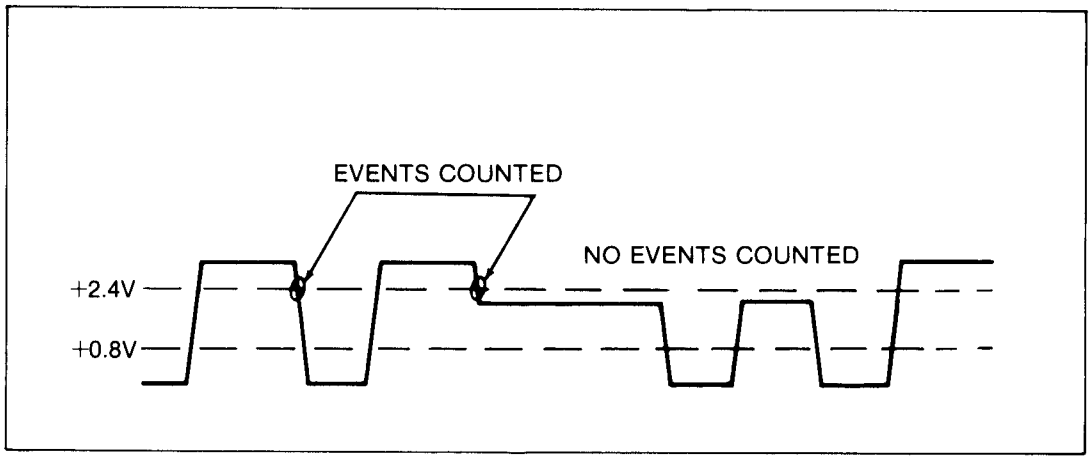


Figure 4K-4. Counting Events on the Falling Edge

1. Disable the probe stimulus capability and specify the address or data synchronization.

2. Place the probe at the desired circuit node.

3. Press the READ PROBE key to provide the starting point for accumulating data.

4. Select and specify one or more 9010A functions (such as the Ramp function) which generate a bit stream at the circuit node.

5. After the specified 9010A functions have been performed, press the READ PROBE key to display the signature.

Note that the probe must be in address sync or data sync to gather signatures. No signatures are computed in free-run. Only data occuring during the address valid or data valid periods are computed in the signature, even though other data may be on the bus at other times.

For an example of how signatures may be used, consider a UUT with a faulty display. To test the UUT display, place the probe on one of the data lines to the UUT display buffer (with the probe stimulus capabilities disabled). Press the READ PROBE key. This provides the starting point for gathering the data.

Now specify the Ramp troubleshooting function so that it is performed once at one of the display addresses. When the Ramp operation has been completed, press the READ PROBE key. The data is displayed on the 9010A. The operator can observe the computed signature and compare it with an expected signature. Obviously, in order for signature computation to be meaningful, the operator must gather the correct reference signature from a properly operating UUT.

4K-9. SCOPE TRIGGER OUTPUT

The rear panel oscilloscope TRIGGER OUTPUT (see Figure 4K-5) allows the operator to synchronize an oscilloscope to the data valid or address valid periods on the UUT μP bus. The TRIGGER OUTPUT pulse is shown in Figure 4K-6. The 100 mV pulse is the differentiated sync pulse from the interface pod, which is the same pulse that synchronizes the probe operation to the data valid or address valid periods.

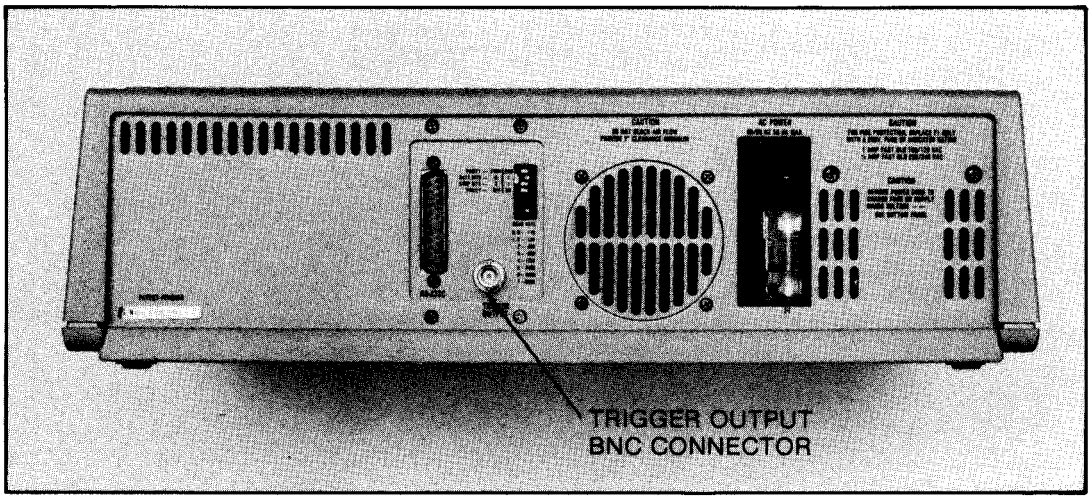


Figure 4K-5. Rear Panel TRIGGER OUTPUT BNC Connector

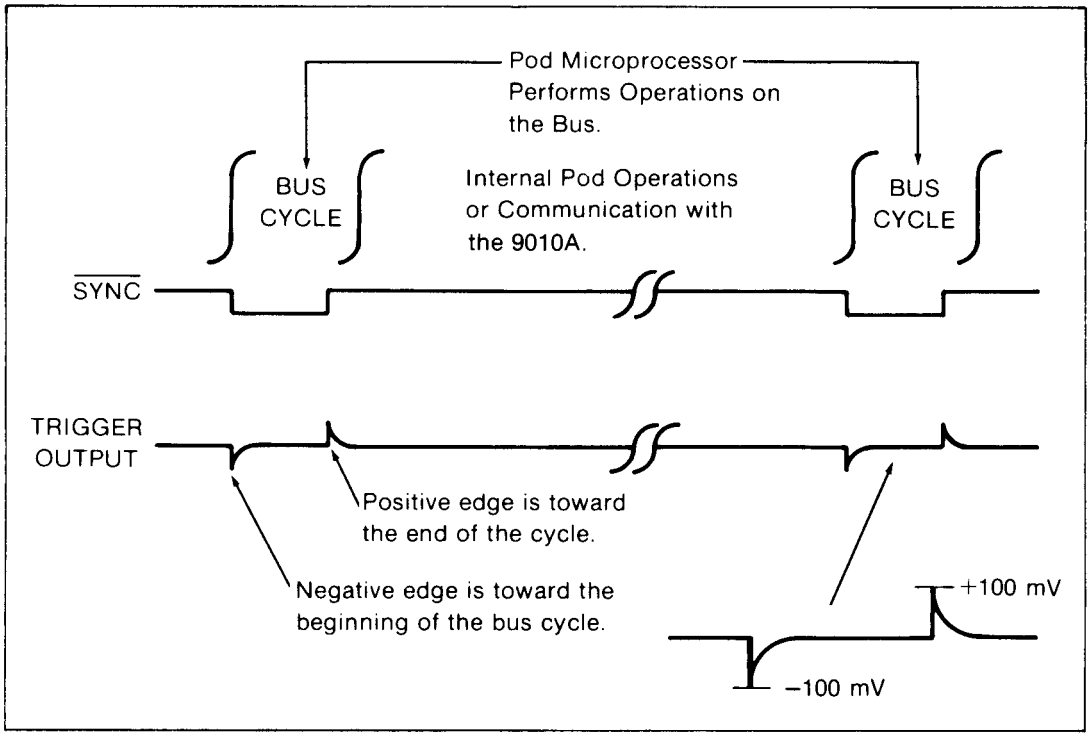


Figure 4K-6. Rear Panel TRIGGER OUTPUT Pulse

The actual timing of the sync signal and the TRIGGER OUTPUT pulse depends on the type of μP, and whether the probe is in data sync or address sync. Figure 4K-6 shows the general relationship between the sync signal, the TRIGGER OUTPUT pulse, and the other activity on the bus. Notice that the negative edge of the TRIGGER OUTPUT pulse is toward the beginning of the bus cycle. The positive edge of the TRIGGER OUTPUT pulse is toward the end of the bus cycle. For specific information about the timing, refer to the approriate interface pod manual.

4K-10. INDICATOR LIGHTS

The red and green indicator lights on the probe indicate the voltage levels detected at the probe tip. There are four general principles which govern indicator light behavior:

1. When the green light is on, it indicates that valid low data (<0.8V) is detected for periods greater than 75 ns.

2. When the red light is on, it indicates that valid high data (>2.4V) is detected for periods greater than 75 ns.

3. When both lights are off, an invalid logic level (between 0.8V and 2.4V) is present. Invalid intervals of less than 100 ns are not detected.

4. When an indicator light turns on, it remains on for a minimum of 0.25 seconds to allow narrow pulses to be observed.

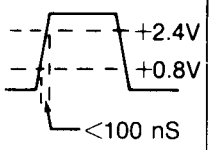
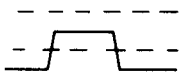
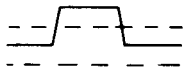
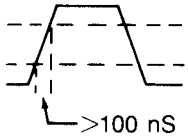
Table 4K-5, which is based on these four principles, lists and explains all combinations of indicator light behavior. Note that when a synchronization mode is selected, the indicator lights do not report the probe tip voltage levels except during the synchronization interval. This allows the operator to isolate and observe events during desired intervals.

Consider the following example: first the operator selects the data valid synchronization and specifies a looping Read operation; then the operator places the probe on a data line which is zero during the Read operation;the green indicator light is on continuously, which indicates a low voltage during the time interval reported; the indicator lights disregard the voltage levels during the non-data valid intervals.

In order to make brief single-pulse transitions readily visible to the operator, the probe indicator light remains lit for a minimum of about 0.25 seconds, even if the detected pulse is very brief. For example, assume that the operator wants to check to see if a ROM chip is enabled during a Read operation at a particular address. The operator places the probe on the ROM enable line, specifies a Read operation at the desired address, and observes the probe while the Read operation is executed. Even if the low pulse on the enable line would be too brief for the eye to easily perceive, the probe indicator light remains on long enough to easily see if the ROM is enabled.

Note that, like the Read Probe operation, the indicator lights report all activity at the probe tip, including stimulus and response activity. For example, if the 9010A is generating high stimulus pulses and the probe is simply held in the air, the red light flashes to indicate the transitions are detected at the probe tip.

Table 4K-5. Probe Indicator Light Activity

CONDITION	DESCRIPTION
Green on continuously, red off	Indicates a steady dc low.
Red on continuously, green off	Indicates a steady dc high.
Both lights off	Indicates the line remains in the invalid logic continuously.
Both red and green on continuously	Indicates that a line is toggling* between high and low, but is staying in the invalid area for less than 100 ns. An example of this would be a clearly defined square wave. 
Green flashing, red off	Indicates the line is toggling* in between logic low and invalid. 
Red flashing, green off	Indicates the line is toggling* in between logic high and invalid. 
Both lights flashing	Indicates the line is toggling* between all three logic states. 

*The toggling rate is not related to the flashing rate.

Section 4L
Troubleshooting With Programs

4L-1. INTRODUCTION

One of the most powerful troubleshooting tools available with the 9010A is the program. This section presents a brief overview of what programs are about and how to execute them. For information about how to create, examine, or modify programs, refer to the 9010A Programming Manual.

4L-2. OVERVIEW OF PROGRAMS

Programs are sequences of 9010A operations and functions that are created by the programmer. Most of the 9010A operations and functions may be included as steps in programs, such as the functional tests or troubleshooting functions. Some of the test sequencing keys are used exclusively in programs. The test sequencing keys direct the flow of the programs and allow the construction of conditional and unconditional branches, step labeling, and display of programmer-generated messages or prompts. The arithmetic keys allow the programmer to store and manipulate data in the sixteen 32-bit registers.

There are two main types of testing that are performed with programs: go/no-go and guided-fault isolation. Go/no-go tests are the simplest from the operator's point of view because the operator needs only to observe the results.

Guided-fault isolation tests are also simple to perform because the programmer-generated messages guide the operator each step of the way and specify what action the operator is to perform next. Such action may involve replacing an IC, placing the probe at a particular location and pressing CONT, or entering data. Using such techniques, an experienced programmer may construct test procedures which can quickly guide an operator to the cause of the UUT failure, even if the operator is unfamiliar with the UUT.

4L-3. EXECUTING PROGRAMS

To execute a program, do the following:

1. Press the EXEC key. The 9010A prompts for the program number by displaying the following message:

   EXECUTE PROGRAM _

2. Key in the program number *dd* in decimal and press ENTER. The range of possible program numbers is from 0 to 99. If the program exists in memory, the 9010A begins executing the program and displays the following message:

   EXECUTE PROG dd

If the program does not exist in memory, the following message is displayed:

EXECUTE PROGRAM dd - NOT FOUND

When the program number is entered and accepted by the 9010A, the 9010A enters the Executing Mode as indicated by the flashing EXECUTING annunciator.

To discontinue a program while it is being executed, press the STOP key. This causes the 9010A to enter the stopped state (unless it is stopped already) and causes the STOPPED annunciator to flash continuously. When the 9010A is executing a program and is in the stopped state, any Immediate Mode action (such as a Read function or a Bus Test) may be selected, which causes the 9010A to discontinue executing the program, enter the Immediate Mode, and display the associated message.

During execution, no part of the actual program is visible on the display except for the programmer-generated messages which are intended for display by the programmer. Usually these messages inform the operator of the results of some action performed during the test program, or they specify some action the operator is to perform. Error messages are displayed as usual and are discussed following the next paragraph.

Note that after a program has completed execution and the 9010A has reentered the Immediate Mode, the operator may press REPEAT to cause the program to be executed again. Similarly, pressing LOOP causes the program to be executed recurrently.

4L-4. ERROR MESSAGES DURING EXECUTION

Any of the errors that may be detected and reported in the Immediate Mode may be detected and reported in the Executing Mode. These include the Timeout errors, UUT System errors, and Test errors. In addition,there are five fatal error messages that may be encountered only when executing or attempting to execute programs. The error messages are called fatal because they abort the program that is being executed and return the 9010A to the Immediate Mode. There is no possibility of looping on a fatal error or disregarding it and continuing with the program. The five fatal error messages are listed and described in Table 4L-1.

Table 4L-1. Fatal Error Messages

ERROR MESSAGE	DESCRIPTION
FATAL - MEMORY EXCEEDED FOR LEARN	The address descriptors obtained during a Learn operation have exceeded the 9010A internal memory. This situation is described in Section 4G.
FATAL - ATTEMPTED RECURSION *FATAL - DEPTH EXCEEDED* *FATAL-NUMERIC VALUE OUT OF RANGE* *FATAL-PROGRAM NOT FOUND*	These messages indicate something is wrong with the construction of the program, and can only be corrected by modifying the program. For an explanation of what specific corrections are needed, refer to the 9010A Programming Manual.

Section 4M
Customizing Operation With Setup

4M-1. INTRODUCTION

Although many of the μP-dependent requirements for each microsystem are provided by the design of the interface pod, each UUT may have particular operating requirements beyond those met by the interface pod design. The Setup function allows the operator to select specific operating features and parameters to meet particular UUT requirements.

4M-2. THE SETUP MENU

The Setup function does not directly cause any actions to be performed on the UUT that are normally visible to the operator. Pressing the SETUP key invokes a menu comprised of a sequence of one-line messages. The Setup messages are listed and described in Table 4M-1 in the order in which they are scrolled with the MORE key. When the Setup menu is first invoked by pressing the SETUP key, the 9010A enters the Setup menu at the point where it last exited. Whenever a Setup message is present on the display, pressing SETUP brings the first message in Table 4M-1 to the display. The circular Setup menu may be scrolled forward or backward with the MORE and PRIOR keys.

There are two types of Setup messages. One type involves the reporting of UUT errors or the enabling of μP lines. This type of message ends with the word YES or NO, and may be changed by pressing the YES or NO key. For example, the following message indicates that the 9010A will report the detection of a bad UUT power supply, a UUT system error:

SET-TRAP BAD PWR SUPPLY? YES

To disable the reporting of this error, press the NO key. The last word in the message changes to NO.

The other type of Setup message involves the specification of operating parameters. This type of message ends as follows: CHANGE? An example of this type of message is as follows:

SET-RUN UUT @ 0000-CHANGE?

The message presented indicates that the RUN UUT operation begins execution at the address 0000. To change the address, press the YES key, key in the desired address, and press the ENTER key. Operating parameters for other Setup messages that end with CHANGE? may be specified in a similar manner.

The actual number of Setup messages varies, depending on the type of interface pod that is connected to the main instrument. Each μP may have up to eight lines that may be enabled or disabled with a Setup parameter. Typically the lines are such things as Ready,

Hold, Wait, or Bus Request. Each line that may be enabled or disabled has a separate message in the Setup menu. The format for the message is listed in Table 4M-1. The lines that may be enabled or disabled are documented in the appropriate interface pod manual.

The Setup function is only available in the Immediate Mode. Note that the Setup messages are listed in Table 4M-1 with the default values that are specified by the 9010A at power-on. Note also that if the operator makes any changes or modifications in the Setup messages, the Setup information transferred to the tape or AUX I/F reflects the changes made by the operator.

Table 4M-1. Setup Messages (Power-On Valves Shown)

DISPLAY MESSAGE	DESCRIPTION
SET - TRAP BAD PWR SUPPLY? YES *SET - TRAP ILLEGAL ADDRESS? YES* *SET - TRAP ACTIVE INTERRUPT? NO* *SET - TRAP ACTIVE FORCE LINE? YES* *SET - TRAP CTL ERR? YES* *SET - TRAP ADDR ERR? YES* *SET - TRAP DATA ERR? YES*	The first seven messages correspond to the seven UUT system errors. If YES is selected, the UUT system error is reported to the operator is it occurs. If NO is selected, the UUT system error is not reported to the operator if it occurs. UUT system errors are described in Table 4F-1.
SET - ENABLE xxxx? NO	This message appears for each μp line that may be enabled or disabled. The letters *xxxx* correspond to the name of the line, such as ready or wait. The actual names and number of lines are documented in the appropriate interface pod manual.
SET - BUS TEST @ aaaa - CHANGE?	When the Bus Test is performed, testing of data lines occurs at the address listed.
SET - RUN UUT @ aaaa - CHANGE?	When the address for the Run UUT operation is allowed to default, this address is used.
SET - TIMEOUT 200 - CHANGE?	The parameter following the word TIMEOUT represents a count of how long the 9010A waits before timing out on an interface pod operation. The parameter may be any decimal number between 0 and 60,000.
SET - EXERCISE ERRORS? YES	If YES is selected, the 9010A displays detected error messages and prompts the operator to loop on the errors. If NO is selected, the errors are not reported to the operator, but error messages are transmitted to the RS-232 if it is connected (without the -LOOP? portion of the message).
SET - BEEP ON ERR TRANSITION? YES	The YES enables the audible beep which sounds whenever an error is detected and reported. The beep also sounds whenever the error is removed.

Table 4M-1. Setup Messages (Power-On Values Shown) (cont)

DISPLAY MESSAGE	DESCRIPTION
The following Setup parameters relate to the operation of the optional AUX I/F. If the 9010A detects at power-on that the optional AUX I/F is not installed, the following Setup parameters do not appear in the Setup menu. For a complete description of the following Setup parameters and the AUX I/F, refer to Section 5 of this manual.	
SET - STALL 13-CHANGE?	Any hexadecimal value from 0 to FF may be entered. The corresponding ASCII character is the stall character.
SET - UNSTALL 11-CHANGE?	Any hexadecimal value from 0 to FF may be entered. The corresponding ASCII character is the unstall character.
SET - NEWLINE 00000D0A - CHANGE?	This is the terminator sequence and timing delay between lines.
SET - LINESIZE 79 — CHANGE?	This is the maximum line length for data transmission from the 9010A. The length may be any decimal value from 10 to 255.

Note: The μP Enable lines, the Bus Test address, and the Run UUT default address are pod-dependent, and are supplied to the 9010A by the interface pod that is connected.

Section 4N
Using the Mode Keys

4N-1. INTRODUCTION

The five mode keys are shown in Figure 4N-1. Four of the modes are functions that modify the performance of actions which have been specified: the Continue (CONT), Stop (STOP), Repeat (RPEAT), and Loop (LOOP) mode functions. These four functions are related and are described together. The fifth mode, the Run UUT (RUN UUT) Mode, is also described in this section.

4N-2. STOP, CONTINUE, REPEAT, AND LOOP FUNCTIONS

The effect that the Stop, Continue, Repeat, and Loop functions have on the activity of the 9010A depends on the activity that is taking place at the time the function key is pressed. The effect of the Stop, Continue, Repeat, and Loop functions is most easily described and understood when discussed in a particular context. There are two general cases; one case where errors are involved, and the other case where errors are not involved. Each case is discussed in the following paragraphs.

4N-3. Stop, Continue, Repeat, and Loop Functions With No Errors Involved

The effect of the Stop, Repeat, and Loop functions is diagrammed in Figure 4N-2. The messages in the boxes are displayed on the 9010A and represent states in which the 9010A resides while associated activity is taking place. The numbered lines or paths represent transitions between the states, and the words beside the path numbers indicate the action that causes the transition to take place. For example, the word RPEAT beside a number indicates that the RPEAT key has been pressed. The flashing LOOPING or STOPPED annunciators are also indicated in Figure 4N-2. The significance of the paths and messages is described in Table 4N-1.

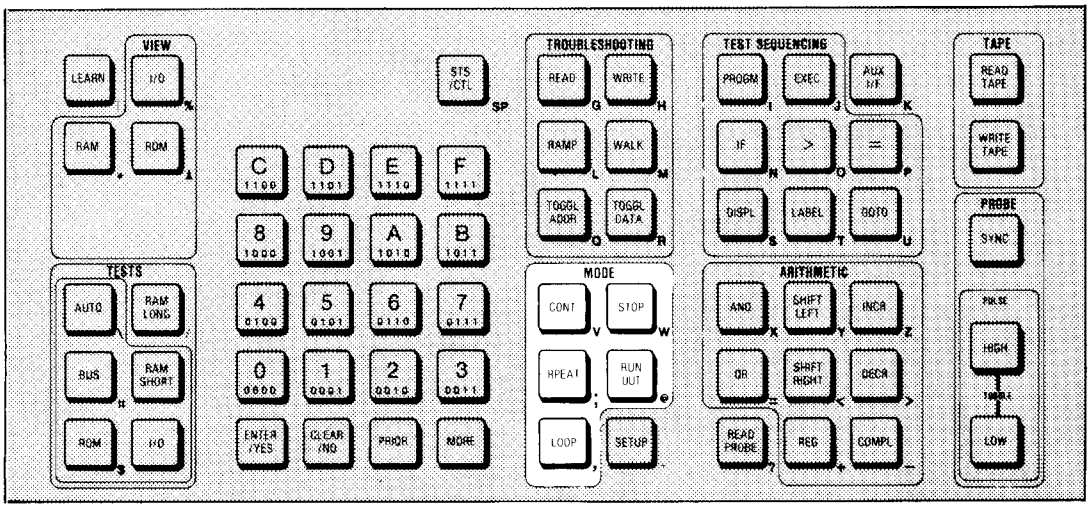


Figure 4N-1. The MODE Keys

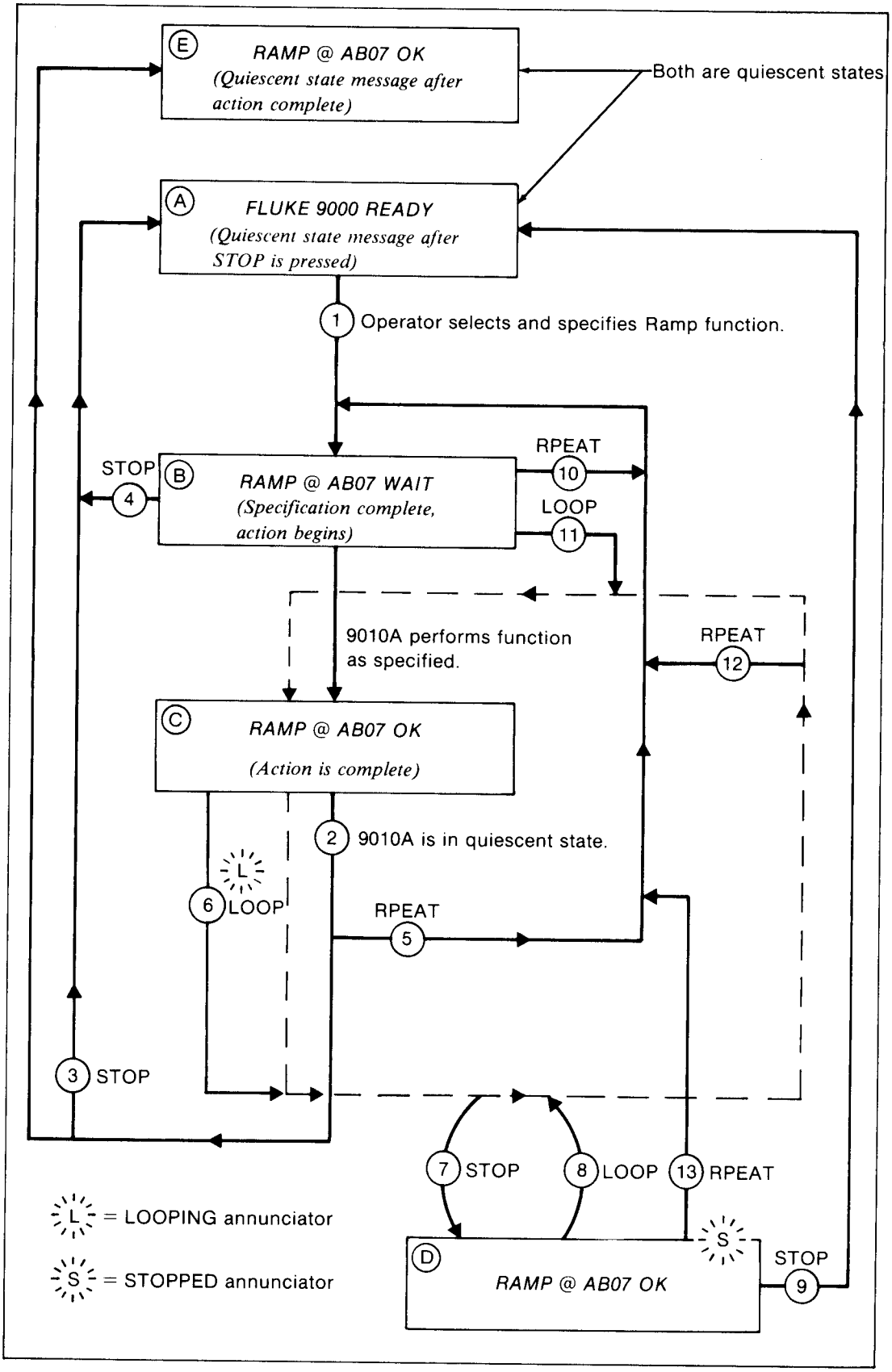


Figure 4N-2 Effect of the Stop, Repeat, and Loop Functions with No Errors Involved

Table 4N-1. Effect of the Stop, Repeat, and Loop Functions

PATH OR MESSAGE	SIGNIFICANCE
A	The diagram begins with the 9010A in the quiescent state at message A.
1	The operator selects and specifies the Ramp function which brings about message B.
B	Since no errors appear during performance, message C appears.
C/E	At this point, the 9010A has completed the performance of the specified function and has returned to the quiescent state. Note that message C and E are identical and represent the same state. Path 2 and message E are shown on the diagram to emphasize that the 9010A returns to the quiescent state which is the same state as shown at message A.
3	Pressing STOP does not change the state, since the 9010A is already in the quiescent state, but it does cause message A to appear.
4	If the STOP key is pressed before the performance is complete the 9010A enters the quiescent state. In actual practice an 8-bit Ramp function is performed so quickly that the operator is usually not able function is performed so quickly that the operator is usually not able to tell if the performance was aborted. For longer operations, such as a 16-bit Ramp, Learn operation, or the ROM Test, it is possible to observe that the performance is aborted.
5	If the RPEAT key is pressed after the function has been performed, the 9010A again performs the function.
6	If the LOOP key is pressed after the function has been performed, the 9010A enters the looping state (indicated by the flashing LOOPING annunciator) and recurrently performs the function as indicated by the dashed line.
7	If the 9010A is looping and the STOP key is pressed, the 9010A enters the stopped state (indicated by the flashing STOPPED annunciator) at message D.
D	While in the stopped state, the 9010A waits for the operator to initiate further activity.
8	If the LOOP key is pressed while the 9010A is in a stopped state, the 9010A resumes looping (the STOPPED annunciator stops flashing and the LOPPING annunciator resumes flashing).
9	If the STOP key is pressed while the 9010A is in a stopped state, the 9010A returns to the quiescent state (message A).
10	If the RPEAT key is pressed before the 9010A completes the performance of the specified function, the 9010A discontinues the present performance and begins the performance again.

Table 4N-1. Effect of the Stop, Repeat, and Loop Functions (cont)

PATH OR MESSAGE	SIGNIFICANCE
11	If the LOOP key is pressed before the 9010A completes the performance of the specified function, the 9010A enters the looping state.
12	If the RPEAT key is pressed while the 9010A is looping, the 9010A performs the function once.
13	If the RPEAT key is pressed while the 9010A is stopped, the 9010A enters the looping state.

The function that is specified in the diagram in Figure 4N-2 is the Ramp function. However, the effect of the Mode functions is consistent, and the principles illustrated in the diagram may be generalized to include the other troubleshooting functions and the built-in tests.

Note that the Continue function is not shown in Figure 4N-2. This is because the Continue function has no meaningful effect on 9010A Immediate Mode operation unless errors are involved. If errors are not involved, pressing the CONT key causes the 9010A to beep.

4N-4. Stop, Continue, Repeat, and Loop Functions With Errors Involved

The effect of the Stop, Continue, Repeat, and Loop functions is diagrammed in Figure 4N-3. The messages in the boxes and the numbered paths indicate states and transitions as they did in Figure 4N-2.

The main difference between Figure 4N-2 and Figure 4N-3 is that the activity diagrammed in Figure 4N-3 involves the detection of two kinds of errors. The RAM Short Test is specified in Figure 4N-3. The two errors that are detected consist of a R/W error and a control (CTL) error. The two errors are on different levels in the error hierarchy. The R/W error is a test error, and the control error is a higher priority error, a UUT system error. Figure 4N-3 shows how the Mode functions affect the activity when an error is initially reported, when the 9010A is looping on the error, or when an error is detected while the 9010A is already looping on an error. The significance of the messages and paths is described in Table 4N-2.

Note that Figure 4N-3 and Table 4N-2 are not an exhaustive presentation of all possible mode key interactions. Figure 4N-3 and Table 4N-2 illustrate the most important principles of mode key use when errors are involved. Since the 9010A system of error handling and mode key interaction is consistent, the operator can gain an understanding of mode key use by grasping the major principles involved.

4N-5. RUN UUT MODE

The Run UUT Mode allows the interface pod μP to execute the program code stored in the UUT. This allows the operator to check the operation of the UUT under normal operating conditions without having to remove the interface pod and reinsert the UUT μP. The Run UUT Mode also allows the operator to indirectly test the UUT μP. This is accomplished by comparing UUT performance with the 9010A in the Run UUT Mode and UUT performance with the interface pod removed and the UUT μP reinserted.

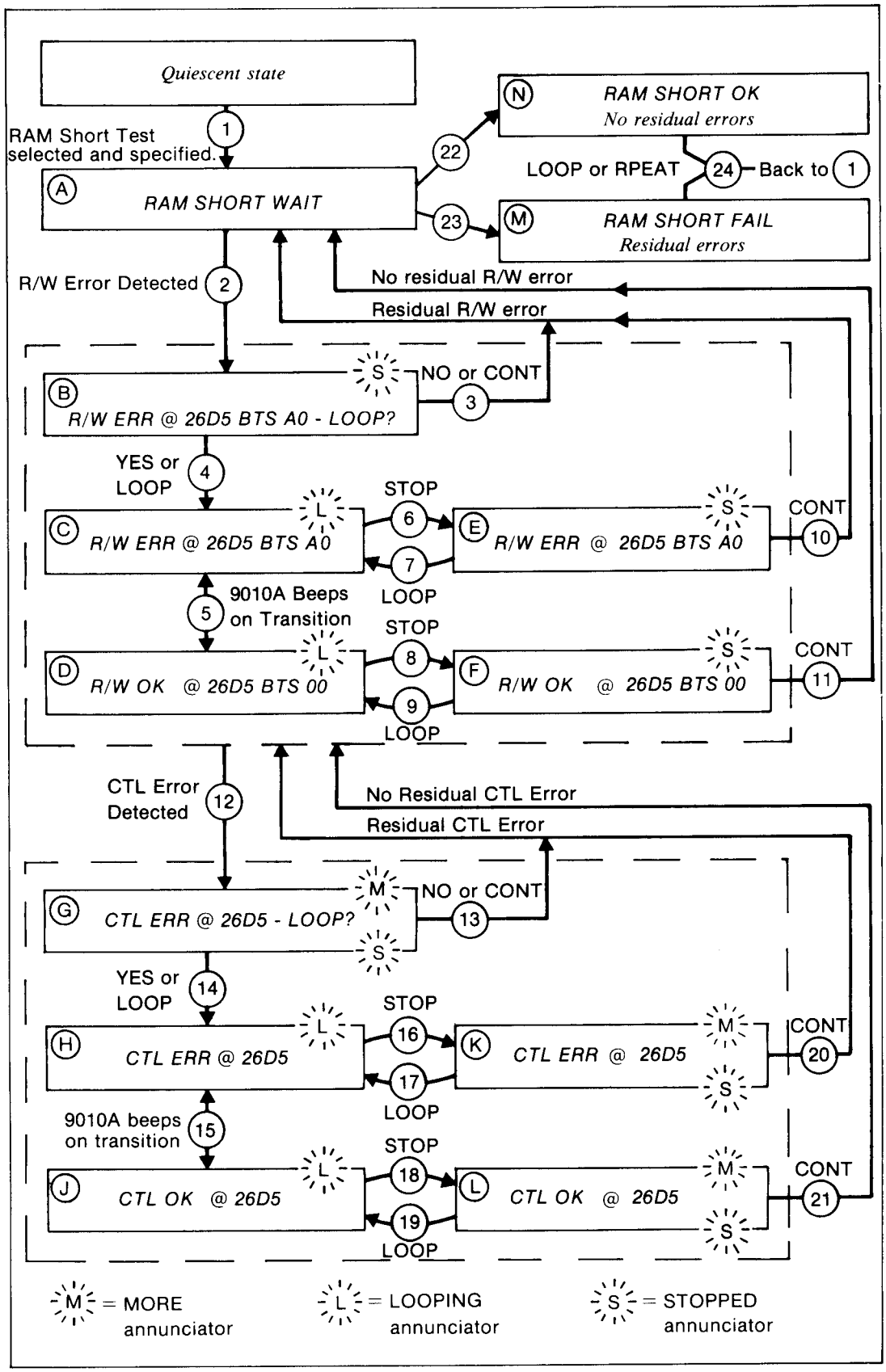


Figure 4N-3. Effect of the Stop, Continue, Repeat and Loop Functions with Errors Involved

Table 4N-2. Effect of the Stop, Continue, and Loop Functions

PATH OR MESSAGE	SIGNIFICANCE
1/A	The diagram begins with the 9010A in the quiescent state. The operator specifies the RAM Short Test, and the 9010A begins performing the test.
2	During performance of the test, a R/W error is detected and reported at message B.
B	When an error is reported, performance of the test halts and the 9010A enters the stopped state (indicated by the STOPPED annunciator) and displays a prompt for a loop.
3	If the NO or CONT keys are pressed while the 9010A is in the stopped state, the 9010A continues performance of the RAM SHORT Test. However, since the R/W error has not been removed this causes the "FAIL" message to appear on the display when the test is completed at message M.
4	If the LOOP or YES keys are pressed while the 9010A is in the stopped state, the 9010A enters the looping state (indicated by the LOOPING annunciator) and message C appears.
5/C/D	The messages C and D are each messages that may appear during the looping state. Message C indicates the error is present, or that there was a residual (unremoved) UUT system error the last time the 9010A looped on the R/W error. Message D indicates that no error is present. Path 5 indicates the result of the action taken by the operator which either removes (message D) or reestablishes (message C) the error. For example, if the R/W error is caused by a loose connection on the pcb, the operator may flex the pcb back and forth, causing the error to disappear (message D) or reappear (message C). Note that the 9010A beeps when the message displayed changes between messages C and D. This allows the operator to concentrate on the UUT without having to observe the display to see if the error is present or has been removed.
6/E	If the operator presses the STOP key while the 9010A is looping, the 9010A enters the stopped state and message E is displayed.
7	If the operator presses the LOOP key while the 9010A is in the stopped state at message E, the 9010A resumes looping and message C is displayed.
8/9	Paths 8 and 9 are caused by the same actions as paths 6 and 7. The only difference is that messages D and F do not report the R/W error.
10/11	If the CONT key is pressed while the 9010A is in the stopped state, the 9010A continues the RAM SHORT Test. Note, however, that path 10 exits from message E which reports an error. Since the error has not been removed, this causes the "FAIL" message to appear on the display when the test is completed at message M. Path 11 exits from message F which does not report the R/W error, and does not cause the "FAIL" message to appear.

Table 4N-2. Effect of the Stop, Continue, and Loop Functions (cont)

PATH OF MESSAGE	SIGNIFICANCE
12	Assume that while the 9010A is looping on the R/W error (at either message C or D) the higher priority CTL (control) error is detected and reported at message G.
G	The 9010A enters the stopped state and prompts for a loop. The MORE annunciator indicates that the second line of the two-line CTL error message is available (CTL BITS 00010011-LOOP?) and may be brought to the display by pressing the MORE key.
13	If the NO or CONT keys are pressed while the 9010A is in the stopped state, the 9010A returns to the lower level R/W error. The unremoved CTL error causes the (ERR) message to appear at message C.
14	If the LOOP or YES keys are pressed while the 9010A is in the stopped state, the 9010A enters the looping state and message H appears.
15/H/J	The interrelationships between path 15 and messages H and J are very similar to those described for path 5 and messages C and D.
16/17	Paths 16 and 17 are caused by the same actions as described for paths 6 and 7.
18/19	Paths 18 and 19 are caused by the same actions as described for paths 8 and 9.
K/L	Messages K and L have meanings similar to messages E and F. The MORE annunciator indicates that the second line of the CTL error message is available and may be brought to the display by pressing the MORE key.
20/21	Paths 20 and 21 are similar to paths 10 and 11 except that when the CONT key is pressed, the 9010A returns to the lower level R/W error, rather than continuing with the RAM Short Test. For path 20, the unremoved CTL error causes the "ERR" message to appear at message C.
22/N	If no residual errors are returned to message A, message N is presented when the test is completed.
23/M	If one or more residual errors remain, message M is presented when the test is completed.
24	If the LOOP or RPEAT keys are pressed while the 9010A is in the quiescent state at messages M or N, the 9010A loops or repeats the test from path 1. One difference is that if the LOOP key is pressed, the "WAIT" message does not appear as part of message A while the test is performed.
NOTE:	*Although the Repeat function is not shown anywhere else in the diagram except at path 24, the Repeat function may be used elsewhere. Once the specification of the test has been completed (path 1), pressing the RPEAT key at any point thereafter causes the 9010A to return to path 1 and begin performing the test as specified.*

While the interface pod is operating in the Run UUT Mode, the main instrument may be used for any other activity that does not require access to the UUT. For example, the UUT memory map may be examined with the VIEW keys.

To select the Run UUT Mode, do the following:

1. Press the RUN UUT key. The 9010A displays a prompt for the address where the program execution is to begin by displaying the following message:

   RUN UUT @ _

2. The operator may do either of the following:

   a. Key in the address and press ENTER. The interface pod begins executing the UUT program code at the specified address and displays the following message:

      RUN UUT @ aaaa - MAY NEED RESET

   b. Press ENTER. This causes the interface pod to supply the initial address. The interface pod begins executing the UUT program code in a manner similar to the UUT μP power-up sequence. For example, in a 6800 microsystem, the interface pod reads the address vector at the address FFFE and begins execution at the address specified by the vector. During execution, the 9010A displays the following message:

      RUN UUT - MAY NEED RESET

The interface pod μP is either able to execute the UUT program code in the Run UUT Mode, or it is able to communicate with the main instrument, but it is not able to do both. When the 9010A enters the Run UUT Mode, the main instrument temporarily reliquishes control over the interface pod μP so that the μP can execute the UUT program code. The message MAY NEED RESET reminds the operator that the UUT may not begin executing its own program code without a hardware reset at the UUT. For example, a PIA or an interface may not respond to the μP without the reset. When a troubleshooting function, a test, or an operation is selected by the operator, the 9010A performs a reset on the μP if the 9010A is in the Run UUT Mode and resumes control over the interface pod μP.

During entry into the Run UUT mode, the 9010A still monitors and reports any UUT system errors or timeout errors that may occur. If the 9010A displays a prompt asking if it should loop on an error, and the operator chooses not to loop on a reported error, the following message appears:

RUN UUT FAIL

The FAIL message does not mean the 9010A was not able to enter the Run UUT Mode. It means that the error that has been detected and reported might have prevented the UUT program code from executing as expected. There are no error messages which are provided exclusively with the Run UUT Mode.

Note that in the Run UUT Mode the interface pod does not supply address or data synchronization pulses to the probe. Thus, the probe is effectively disabled if it is synchronized to address valid or data valid time intervals during Run UUT. However, the probe may be switched to the free-running mode without affecting the Run UUT Mode of the 9010A.

Section 4P
Cassette Tape Operation

4P-1. INTRODUCTION

This section describes the operation of the cassette tape. It includes information about cassette loading, the Read Tape and Write Tape operations, and error detection.

4P-2. TAPE-TRANSFERABLE DATA

Tape-transferable data may consist of test programs, UUT memory map descriptors, and Setup parameters. No other type of data may be written to or read from the 9010A cassette tape. The storage capacity of the 9010A memory which stores the tape-transferable data is 12K bytes.

4P-3. LOADING THE CASSETTE INTO THE 9010A

Cassette loading is illustrated in Figure 4P-1. To load a cassette into the 9010A, follow these steps.

1. Press the eject button at the left rear of the cassette enclosure to release the cassette enclosure.

2. Select the desired side of the cassette, turn it face up with the open side of the cassette facing the rear, insert the cassette, and close the enclosure.

NOTE

After a period of use, iron oxide may build up on the tape head. The tape head should be kept clean to ensure proper operation. If the tape head appears to have a gray or dark brown residue, clean with a cotton swab and isopropyl alcohol.

4P-4. READ TAPE

To select the Read Tape operation, press the READ TAPE key. The 9010A displays the following messages:

READ TAPE - ARE YOU SURE?

If the operator presses the NO key, the 9010A displays the following message:

READ TAPE ABORTED

If the operator presses the READ TAPE key and then the YES key, the 9010A displays the following message:

READ TAPE WAIT

Figure 4P-1. Cassette Loading

The 9010A rewinds the tape (if necessary) and begins reading information from the tape. If the 9010A does not detect any errors during the operation, the 9010A completes the operation and displays the following message:

READ TAPE OK

Errors that may be detected with the Read Tape operation are described in Table 4P-1. Note that if the Read Tape operation fails, the 9010A memory is restored to power-on values.

Note also that tapes will usually develop soft errors before they develop hard errors. If the Read Tape operation fails, the operator should try the operation again. If the operation is successful, it is recommended that the operator immediately perform the Write Tape operation with a new cassette to prevent the loss of data.

The Read Tape operation may not be interrupted by the operator and then continued. It is possible to abort the operation by pressing the key for another function, such as STOP or a troubleshooting function. Aborting the Read Tape operation before it is completed removes any data stored by the operator in the 9010A internal memory.

4P-5. WRITE TAPE

To select the Write Tape operation, press the WRITE TAPE key. The 9010A displays the following message:

WRITE TAPE - ARE YOU SURE?

If the operator presses the NO key, the 9010A displays the following:

WRITE TAPE ABORTED

Table 4P-1. Tape Operation Error Messages

ERROR MESSAGE	DESCRIPTION
READ TAPE - NO CASSETTE *WRITE TAPE - NO CASSETTE*	These messages may be presented during the selection of the operations. They indicate that no cassette is loaded in the 9010A.
READ TAPE FAIL	There are a variety of possible causes: Cassette enclosure open. Loss of synchronization or overruns during transfer of data. Unmatching checksums. When the 9010A transfers data from internal memory to the tape, it generates a checksum from the data and stores the checksum with the data. When the Read Tape operation occurs, the 9010A generates a checksum from the data that is read from the tape and compares the new checksum with the checksum stored on tape. If the checksums do not agree, the FAIL message appears.
WRITE TAPE FAIL	There are a variety of possible causes: Cassette enclosure open. Loss of synchronization or overruns during transfer of data. Failure of the byte-for-byte data comparison test.

If the operator presses the WRITE TAPE key and then the YES key, the 9010A displays the following message:

WRITE TAPE WAIT

The 9010A rewinds the tape (if necessary) and begins writing information on the tape. When all the data has been transferred from internal memory, the 9010A again rewinds the tape. Then the 9010A performs a byte-for-byte comparison of the data on the tape and the data stored in memory. If no errors are detected, the 9010A displays the following message:

WRITE TAPE OK

Errors that may be detected with the Write Tape operation are described in Table 4P-1.

The Write Tape operation may not be interrupted by the operator and then continued. It is possible to abort the operation by pressing the key for another function, such as STOP or a troubleshooting function. Aborting the Write Tape operation does not affect the internal memory of the 9010A.

4P-6. WRITE TAPE PROTECTION

Later models of the 9010A have a Write Tape protection feature. The cassettes have a plastic punchout tab which may be removed to disable the Write Tape

operation. This protects data already written on the tape. The location of the plastic tab is indicated in Figure 4P-2. A plastic tab is located on each side of the cassette, and the removal of the tab affects only the side on which it is located. Removal of the tab does not affect the Read Tape operation.

If a cassette is inserted which has the tab removed and the WRITE TAPE key is pressed, the 9010A detects that the tape is Write Tape protected and presents the following message:

WRITE TAPE - WRITE PROTECTED

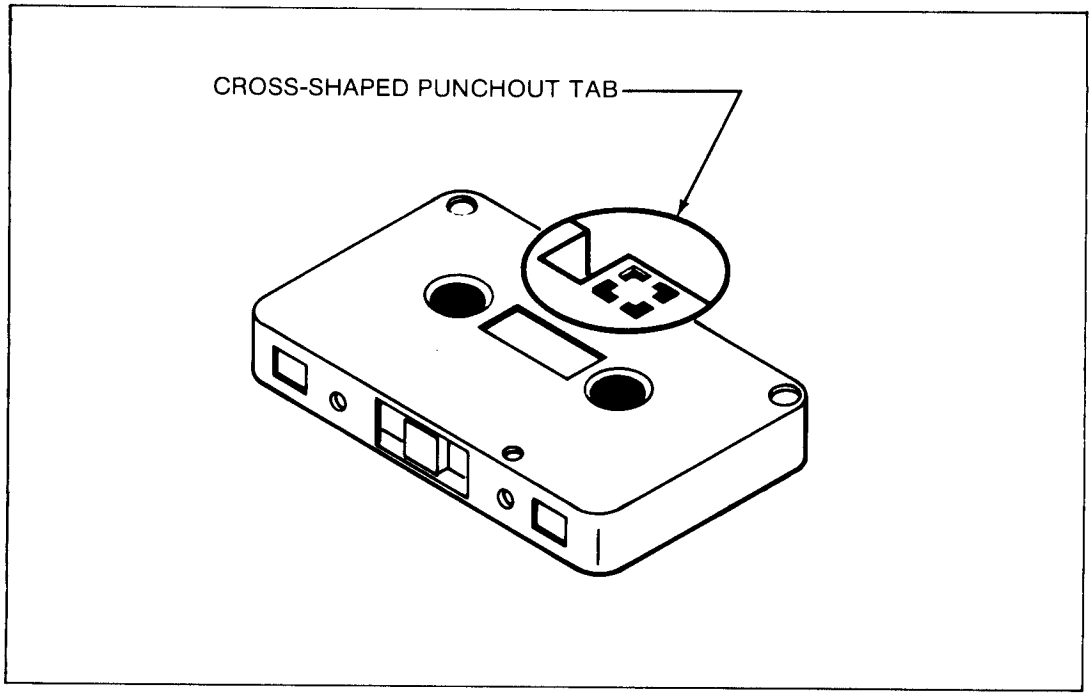


Figure 4P-2. Tab Location for Write Tape Protection

Section 5
Options and Accessories

5-1. INTRODUCTION

This section contains information about options and accessories available for use with the 9010A.

Accessory information can be identified with "500" paragraph numbers. For options, relevant page and paragraph numbers contain the option number.

Accessories

500-1. INTRODUCTION

This section describes the accessories available for use with the 9010A Micro-System Troubleshooter. Each accessory is described separately. Further information is supplied with the accessory.

500-2. Y8007 CASSETTE TAPES

The cassette tapes are illustrated in Figure 5-1. Each side of the doublesided cassette tapes has the capacity to store the contents of 9010A memory. Either side of the cassette may be write-protected by removing a punchout plastic tab from the cassette. Accessory model number Y8007 consists of a pack of 10 tapes.

500-3. 9000A-900 TRANSIT CASE

The 9000A-900 Transit Case, shown in Figure 5-2, allows safe, convenient transportation of the 9010A Micro-System Troubleshooter, the probe, and any one of the interface pods. The Transit Case can also accommodate several cassette tapes.

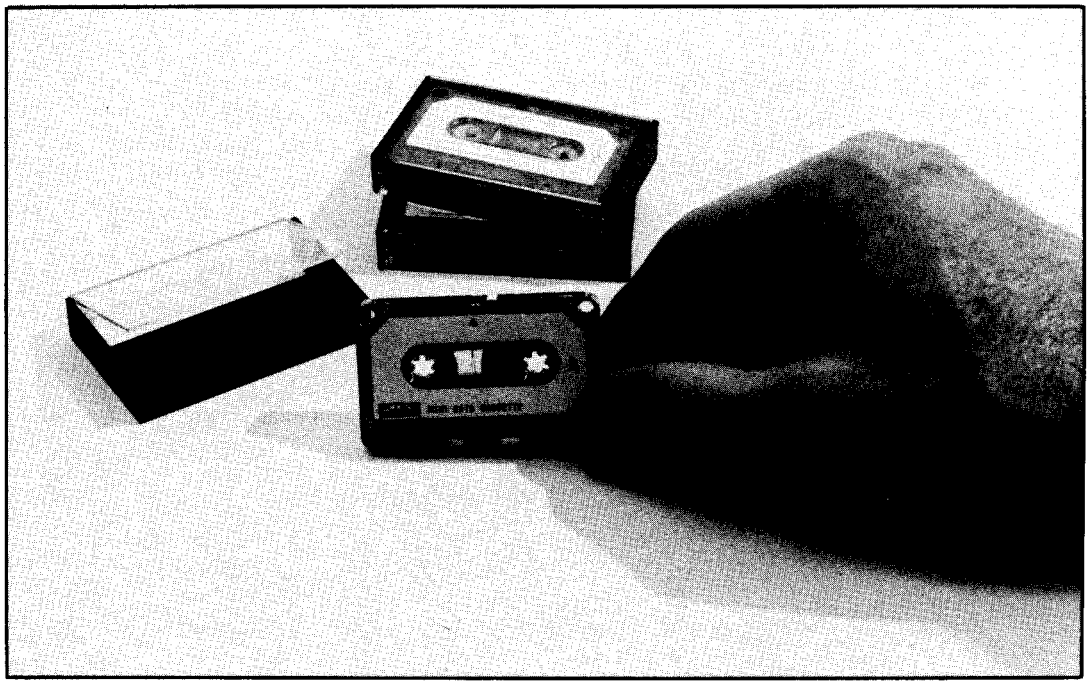


Figure 5-1. Y8007 Cassette Tapes

Figure 5-2. 9000A-900 Transit Case

Option -001
RS-232 Auxiliary Interface

001-1. INTRODUCTION

This section provides a description of the RS-232 Auxiliary Interface (AUX I/F) Option 9010A-001. It includes a general description of the AUX I/F, the AUX I/F operations, the operator-selectable data transmission parameters, and the AUX I/F error handling.

All of the information in this section pertains to AUX I/F operation in the Immediate Mode. AUX I/F operates much differently in the Executing Mode. AUX I/F operation in the Executing Mode is described in the 9010A Programming Manual. For information about the data format for AUX I/F Write and AUX I/F Read in both the Immediate Mode and the Executing Mode, refer to the 9010A Programming Manual.

001-2. GENERAL DESCRIPTION, SPECIFICATIONS, AND CABLE CONNECTION

The AUX I/F allows the 9010A to communicate with remote devices, such as a printer, a computer, or another 9010A, via the rear panel RS-232 port. The AUX I/F is factory-installable only. The data transmission is full-duplex asynchronous, with operator-selectable baud rates, line terminators, line size, data bits (seven or eight), stop bits (one or two), parity (odd, even, or none). The AUX I/F specifications are listed in Table 001-1.

The 9010A is connected to a remote device with a standard 25-pin RS-232 cable. The 9010A rear panel RS-232 port is a male connector. The pin assignments for the connector are shown in Figure 001-1.

001-3. AUX I/F OPERATIONS

There are seven possible AUX I/F operations. Six of the operations are for sending data, and one is for receiving data. AUX I/F operations exist for sending address space descriptors, the SETUP parameters, stored programs (as a group or individually), all existing program numbers, and all data contained in tape-transferable memory. The one AUX I/F operation for receiving data stores the data received in the tape-transferable memory. The AUX I/F operations are summarized in Table 001-2.

Note that all the AUX I/F operations except AUX I/F Write and AUX I/F Read send information in a form that may be easily read by the operator. For example, when the AUX I/F Program operation is used to send information to a printer, the programs contained in 9010A memory are printed out step-by-step and can be read by the operator. However, the information transferred with the complementary operations AUX I/F Write and AUX I/F Read is meaningful primarily to another machine (such as a 9010A) and is not intended to be read by the operator. The format of the AUX I/F Write and AUX I/F Read operations is described in the 9010A Programming Manual.

Table 001-1. AUX I/F Specifications

DATA RATES	110 to 9600 baud
DATA BITS	7 or 8
STOP BITS	1 or 2
PARITY	Odd, Even, No Parity

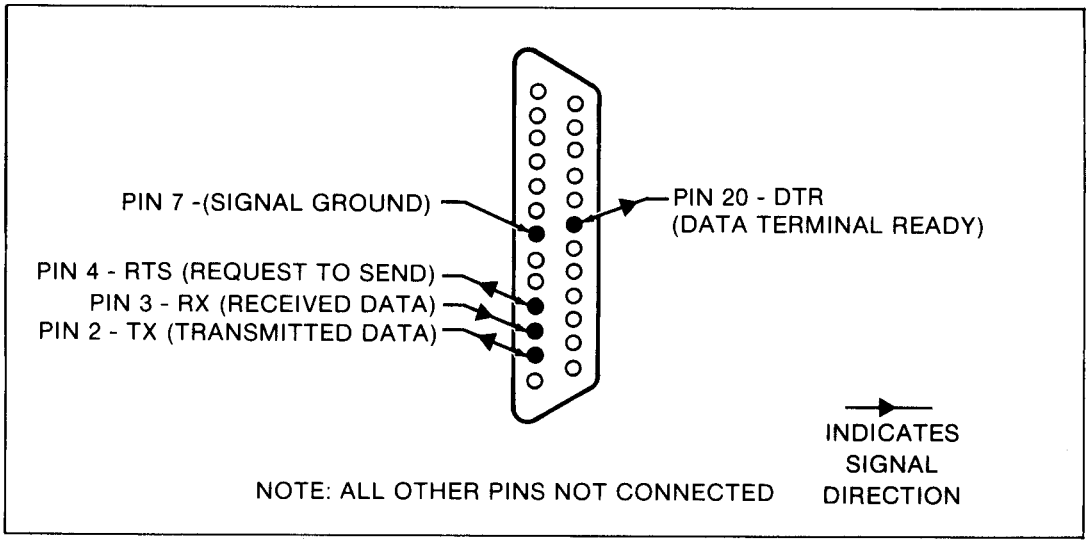


Figure 001-1. AUX I/F RS-232 Pin Connections

Table 001-2. AUX I/F Operations

PRESS THIS KEY (s)	DISPLAY MESSAGE	DESCRIPTION OF 9010A ACTION
AUX I/F	*AUX INTERFACE NOT PRESENT*	The 9010A detects that the AUX I/F is not installed.
AUX I/F	*AUX - SELECT ACTION _*	The 9010A requests more information.
AUX I/F LEARN	*LIST ADDR SPACE INFO -*	The 9010A begins sending all address descriptors.
	LIST ADDR SPACE INFO - COMPLETE	Word COMPLETE is appended when all descriptors are sent.
AUX I/F LEARN	*NO ADDRESS SPACE INFO*	No address descriptors are contained in 9010A memory.
AUX I/F SETUP	*LIST SETUP INFO -*	The 9010A begins sending the Setup parameters.
	LIST SETUP INFO - COMPLETE	Word COMPLETE is appended when all Setup parameters are sent.

Table 001-2. AUX I/F Operations (cont)

PRESS THIS KEY (s)	DISPLAY MESSAGE	DESCRIPTION OF 9010A ACTION
AUX I/F PROGM	*LIST ALL PROGRAMS -*	The 9010A begins sending all programs contained in 9010A memory.
	LIST ALL PROGRAMS - COMPLETE	Word COMPLETE is appended when all programs are sent.
AUX I/F PROGM	*NO PROGRAMS DEFINED*	No programs are contained in 9010A memory.
AUX I/F =	*LIST PROGRAM NUMBERS -*	The 9010A begins sending the numbers of existing programs.
	LIST PROGRAM NUMBERS - COMPLETE	Word COMPLETE is appended when all program numbers are sent.
AUX I/F =	*NO PROGRAMS DEFINED*	No programs are contained in 9010A memory.
AUX I/F *nn* ENTER	*LIST PROGRAM nn -*	The 9010A begins sending program number *nn*.
	LIST PROGRAM nn - COMPLETE	Word COMPLETE is appended when program number *nn* is sent.
	LIST PROGRAM nn - NOT FOUND	Words NOT FOUND are appended if program number *nn* is not contained in 9010A memory.
AUX I/F WRITE	*AUX-SENDING*	The 9010A sends all information contained in tape-transferable memory.
	AUX-SENDING - COMPLETE	Word COMPLETE is appended when all information is sent.
AUX I/F READ	*AUX-RECEIVE - ARE YOU SURE?*	Memory protection message.
NO	*AUX-RECEIVE ABORTED*	The AUX I/F Read operation is aborted.
YES	*AUX-RECEIVING -*	The 9010A sends the terminator characters once as a trigger and waits to receive data.
	AUX-RECEIVING - COMPLETE	Word COMPLETE is appended when the AUX I/F Read operation is completed.

The AUX I/F operations are initiated by pressing the AUX I/F key. If the AUX I/F is installed in the 9010A, the 9010A displays a prompt for further specification of the AUX I/F operation by displaying the following message:

AUX - SELECT ACTION _

At this point the operator may press the appropriate key or keys to complete the specification of the operation. For example, to send all the programs stored in 9010A memory, press the PROGM key. The 9010A begins sending to the remote device all the programs stored. The following message is displayed while the data is being sent.

LIST ALL PROGRAMS -

When all the data has been sent, the 9010A displays the following message:

LIST ALL PROGRAMS - COMPLETE

Notice in Table 001-2 that the AUX I/F Read operation displays the following message after the AUX I/F and READ keys are pressed:

AUX-RECEIVE - ARE YOU SURE?

The operator must press the YES key to initiate the operation. The 9010A displays a similar question when the Read Tape operation is selected. The reason for this is to protect the contents of the tape-transferable memory. When the AUX I/F Read operation is performed, the 9010A stores the information received in the tape-transferable memory. Without the YES key specification, the operator might unintentionally clear the memory contents.

001-4. SELECTING DATA TRANSMISSION PARAMETERS

The baud rate, parity, number of data bits, and number of stop bits are selected by adjusting switches on the rear panel of the 9010A. The other data transmission parameters are selected through the Setup function via the keyboard.

The rear panel switches are shown in Figure 001-2. The decal by the switches identifies the corresponding values for each switch setting. Table 001-3 shows the values and settings for each switch. The data transmission parameters that are selected through the Setup function are described by topic in the following paragraphs.

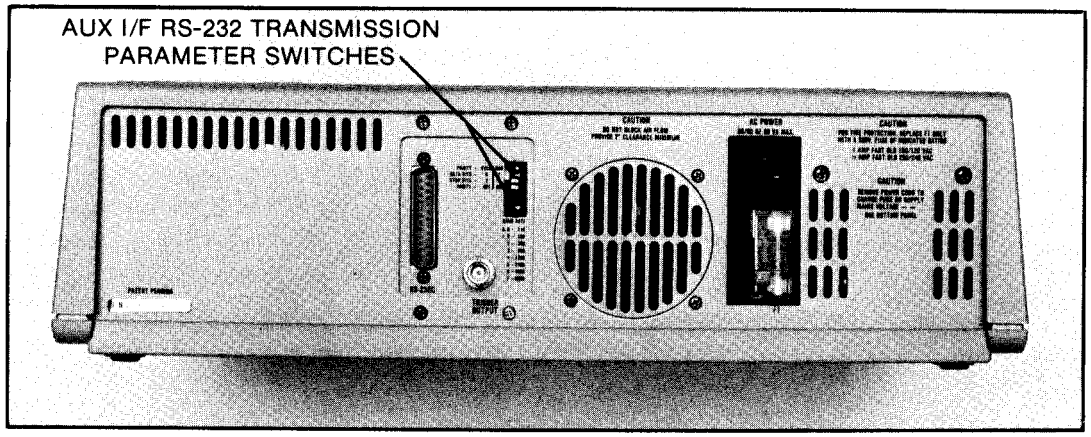


Figure 001-2. AUX I/F RS-232 Rear Panel Switches

Table 001-3. RS-232 Switches

	SWITCH NUMBER	POSITION AND VALUE		PARAMETER
		LEFT	RIGHT	
DIP SWITCHES	4	Even	Odd	Parity
	3	8	7	Data Bits
	2	2	1	Stop Bits
	1	Off	On	Parity

	SWITCH POSITION	BAUD RATE
ROTATING DECIMAL SWITCH	0	110
	1	150
	2	300
	3	600
	4	1200
	5	2400
	6	4800
	7	9600
	8	110
	9	150

001-5. Line Size

The 9010A allows the operator to specify the number of characters transmitted for each line. The number for the line size may be any decimal number between 10 and 255. The line size is selected with the following Setup parameter:

SET-LINESIZE 79-CHANGE?

001-6. Line Terminator Sequence and Delay Between Lines

When the 9010A is sending data through the AUX I/F, a terminator sequence is sent at the end of each line. The characters that are sent may be selected by changing the Setup message shown in Figure 001-3.

The eight hexadecimal digits in the Setup parameter have the following meaning: The first two digits may have any hexadecimal value between 0 and FF. The two digits represent a count which corresponds to a timing delay between the transmission of lines. The timing delay is approximately 2.4 ms/count, providing a total timing delay range of 0 to .6 seconds.

The last six hexadecimal digits are the ASCII terminator characters which are sent at the end of each line when the 9010A is sending data. The characters are also sent once as the initial trigger when the AUX I/F Read operation is selected. The characters are sent left to right. Zeros are not sent. There are two digits per character.

Any character in the ASCII character set may be specified for the terminator sequence (see Appendix D). The terminator sequence at power-on (000D0A) is shown in Figure 001-3; 000D0A corresponds to the ASCII carriage return (0D) and linefeed (0A). Note that the two leading zeros are not sent.

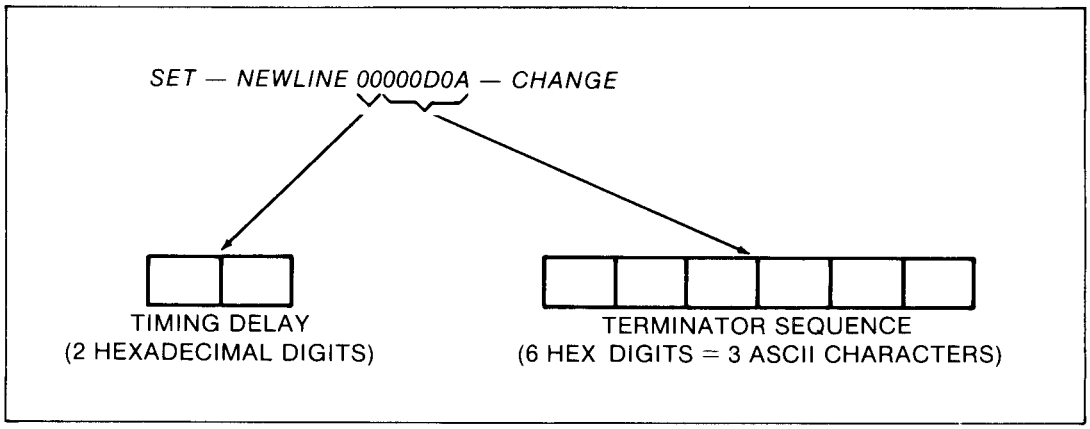


Figure 001-3. Setup Parameter: Terminator Sequence and Delay Between Lines

The selection of the terminator sequence allows the operator to meet the needs of a wide variety of remote devices. For example, if the remote device provides its own linefeed at the end of each line, the terminator sequence would consist of only the carriage return (00000D). Or, if a double space is needed between lines, the terminator sequence would be a carriage return and two linefeeds (0D0A0A).

001-7. The X-ON/X-OFF Protocol

To ensure maximum efficiency during the transmission of data from the 9010A to a remote device, the 9010A provides X-ON and X-OFF (or Unstall and Stall) characters. The Stall and Unstall characters are determined by the following Setup messages:

SET-STALL 13-CHANGE?
SET-UNSTALL 11-CHANGE?

The operator may select any ASCII character for the Stall and Unstall characters. The characters are entered in the Setup messages as hexadecimal digits. The characters shown in the two Setup messages are the default characters provided by the 9010A at power-on (Stall = CTRL S, Unstall = CTRL Q). The 9010A responds to Stall and Unstall characters during any of the AUX I/F operations where the 9010A is sending data.

A typical application of the Stall and Unstall characters might involve a printer, a comparatively slow device. While the printer is receiving data from the 9010A, the printer monitors the amount of data in its input buffer. When the input buffer is almost full, the printer sends the Stall character to the 9010A. When the 9010A receives the Stall character, it stops sending data and appends the word STALLED to the display. When the printer is ready for more data, it sends the Unstall character to the 9010A, which then removes the word STALLED from the display, and the 9010A resumes sending data.

Note that when receiving (AUX I/F Read), the 9010A does not use X-ON or X-OFF, since it will keep up with transmission at all baud rates up to 9600 baud.

001-8. ERROR HANDLING DURING AUX I/F OPERATION

When the AUX I/F Read is taking place, there are six possible error messages that may be displayed by the 9010A. The error messages are listed and described in Table 001-4. If an error is detected and reported, the AUX I/F Read operation is aborted. While receiving, pressing any key (including the HIGH or LOW Keys) will cause the AUX I/F Read operation to be aborted.

Table 001-4. Error Messages During AUX I/F Read Operation

ERROR MESSAGE	DESCRIPTION
AUX-RECEIVING - PARITY ERROR	Parity detected to be in error. Only possible if parity is on.
AUX-RECEIVING - FRAMING ERROR	Synchronization lost during transmission.
AUX-RECEIVING - CHECKSUM ERROR	The line-by-line checksum detected to be in error. Indicates data transmission problem.
AUX-RECEIVING - OVERFLOW ERROR	9010A memory filled.
AUX-RECEIVING - ERROR	Miscellaneous transmission problems.
AUX-RECEIVING - ABORT ERROR	AUX I/F operation aborted because a key was pressed during operation.

Appendix A
Glossary

NOTE

The words in CAPITALS within the text are terms defined elsewhere in this glossary.

ADDRESS is a location on the UUT MICROPROCESSOR BUS.

ADDRESS BLOCK is a set of contiguous addresses in UUT address space. It is specified by giving the lower (first) address, and then the upper (higher) address.

ADDRESS DESCRIPTOR is a parameter stored in the 9010A TAPE-TRANSFERABLE MEMORY which describes the location and type of UUT memory. There are three types of address descriptors: RAM descriptors, ROM descriptors (which include a ROM SIGNATURE for each ADDRESS BLOCK of ROM), and I/O descriptors (which include a BIT MASK specifying the read-writable bits).

AND is the logic operation defined by the following rule:
Given that A AND B = C
If A = 1
and B = 1
Then C = 1
If either A or B = 0
Then C = 0
For example: 1011 AND 1000 is 1000

ASCII is the American Standard Code for Information Interchange. The ASCII character set is a standardized code set of 128 7-bit characters, including full alphabet (upper and lower case), numerics, and many useful control characters (see Appendix D).

BAUD RATE is the serial transfer rate in bits per second, including all bits used to identify the start and end of characters or messages.

BINARY is a number system based on zero (0) and one (1) representations. Counting in BINARY looks like 0, 1, 10, 11, 100, 101, 110, 111, 1000, ...

BIT is a contraction of binary digit. A BIT is either a one or a zero and represents the smallest single unit of MICROPROCESSOR information. In all references in this manual, eight BITS are considered equal to one BYTE.

BIT MASK is a numeric representation of the BITS in an I/O register, with each BIT in the BIT MASK corresponding to a BIT in the I/O register. In the 9010A, BIT MASKS are used in a variety of contexts, including the reporting of errors or specifying read-writable bits.

BYTE is a grouping of eight BITS. Often a 7-bit ASCII character is referred to as a BYTE, with the eighth BIT available for parity if needed.

CONTROL LINES are outputs from a MICROPROCESSOR to the MICROPROCESSOR BUS, such as a read-enable or write-enable line.

DEDICATED REGISTERS are the seven 9010A 32-bit internal registers (0 and A through F) which are loaded with useful operating parameters by 9010A software during operation. Dedicated registers may also be loaded by the operator or programmer.

DEFAULT information is information that is supplied by the 9010A when the operator does not provide the SPECIFICATION that is required by the 9010A.

EXECUTING MODE is the operating mode in which the 9010A performs the actions specified by the PROGRAM STEPS contained in the PROGRAM that is being executed.

EXECUTION refers to the performing of the 9010A actions specified in the PROGRAM by the programmer. The execution of a PROGRAM takes place in the EXECUTING MODE.

HANDSHAKE LINES are lines that coordinate the transfer of data between a MICROPROCESSOR and the MICROPROCESSOR BUS.

HEXADECIMAL is a number system based on 16 rather than 10. Sometimes called hex, the system uses A, B, C, D, E, and F to represent the six additional numbers. Counting in HEXADECIMAL looks like: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, ...

IMMEDIATE MODE is the operating mode in which 9010A actions specified by the operator are performed as soon as they are specified.

I/O refers to the UUT Input/Output registers, an area of UUT ADDRESS SPACE which allows the microprocessor to communicate with other devices on the MICROPROCESSOR BUS, such as a keyboard or display.

LOOPING refers to the action by the 9010A in which the 9010A recurrently performs a test, function, or the exercising of an error.

LOOPING ON AN ERROR refers to the actions performed on the UUT by the 9010A to check if an error is still detected or has been removed.

μP is an abbreviation for MICROPROCESSOR.

MICROPROCESSOR BUS is the set of parallel conductors which allow the flow of signals between the MICROPROCESSOR and memory devices or I/O devices. The actual architecture of the bus depends on the MICROPROCESSOR. The 9010A views the MICROPROCESSOR BUS as being made up of 32 address lines, 32 data lines, 8 control lines, and 16 status lines. Each interface pod sends information to the 9010A

which modifies the 9010A view of the bus according to the actual architecture of the particular MICROPROCESSOR.

MICROSYSTEM is a set of components, circuits, printed circuit boards, or devices that are controlled by a common microprocessor, including the microprocessor external memory and input/output circuitry and devices.

NON-DEDICATED REGISTERS are the nine 9010A 32-bit internal registers (1 through 9) which are not used by 9010A software, but are available for the exclusive use of the operator or programmer.

OR is the logic operation defined by the following rule:
Given that A OR B = C
If either A = 1
or B = 1
Then C = 1
If both A and B = 0
Then C = 0
For example, 1011 OR 1000 is 1011.

PERFORM refers to the act by the 9010A of carrying out the actions specified by the operator.

PIA is an abbreviation of Peripheral Interface Adapter, a chip which provides the interface between the MICROPROCESSOR BUS and another device.

PROGRAM is a set of steps written by the programmer in the PROGRAMMING MODE that specifies the 9010A operations and functions that are performed during the EXECUTION of the PROGRAM.

PROGRAM CODE refers to the set of instructions written by the UUT manufacturer and stored in UUT ROM that tell the UUT MICROPROCESSOR how to operate the UUT.

PROGRAM STEP is a line in a PROGRAM which specifies what action the 9010A is to perform.

PROGRAMMING MODE is the 9010A operating mode in which PROGRAMS are created by the programmer. In the PROGRAMMING MODE, 9010A actions specified by the programmer are not performed immediately, but are stored as PROGRAM STEPS in the PROGRAM.

PROMPT is a message or portion of a message displayed by the 9010A which requests the operator to enter data or press a key.

QUIESCENT STATE is the ready state in which the 9010A waits for the operator to initiate an action.

RAM is an abbreviation for Random Access Memory, but by common usage it has come to mean semiconductor memory that the operator can read or write to.

ROM is an abbreviation for Read Only Memory, which is permanent memory that contains data written by the manufacturer of the UUT.

ROM SIGNATURE is a four-digit HEXADECIMAL number that is a shorthand representation of the data contained in an area of ROM memory. The ROM signature is obtained by successively dividing the data in ROM by a binary number. The resulting signature identifies the data from which it is obtained, and provides a convenient way of comparing data in one UUT ROM with data in another UUT ROM. In the 9010A, ROM signatures may be computed during the Learn operation, the ROM View operation, and the ROM Test. During the ROM Test, a ROM signature is computed and compared with an expected value to verify that the data in the ROM is correct.

RS-232 is an interconnection standard agreed upon by participating manufacturers of data communication equipment for the transfer of digital SERIAL DATA.

SERIAL DATA is transmitted one BIT at a time over a single wire at a predefined BAUD RATE.

SOFTWARE refers to the PROGRAM CODE stored in memory.

SPECIFICATION is additional data that is keyed into the 9010A after the initial selection of a function or operation. Specifications are required by the 9010A before the 9010A can PERFORM the selected function or operation.

STALL, sometimes called X-OFF, is a character sent to the 9010A during transmission of data over the RS-232 interface which tells the 9010A to stop sending data. See UNSTALL.

STATUS LINES are inputs from a MICROPROCESSOR BUS to the MICROPROCESSOR, such as reset or interrupt lines.

STOPPED STATE is the state in which the 9010A halts the performance of an operation or function and reports an error. The STOPPED STATE is indicated by the stopped annunciator.

TAPE-TRANSFERABLE MEMORY is the area of 9010A internal memory which stores PROGRAMS, ADDRESS DESCRIPTORS, and Setup function parameters.

UNSTALL, sometimes called X-ON, is a character sent to the 9010A during transmission of data over the RS-232 interface which tells the 9010A to resume sending data. See STALL.

μP is an abbreviation for MICROPROCESSOR.

UUT is an abbreviation for Unit Under Test. UUT is a general term referring to any microprocessor-based machine with which the 9010A is interfaced.

Appendix B
Specification, Prompt, and Default Summary

Appendix B lists all the prompts and defaults for the specification of all the 9010A tests, functions, and operations. The display messages are listed in the first column. The values that are requested by the prompts in the display messages are listed in the second column. The third column lists the default values (if any) that are supplied by the 9010A if the ENTER key is pressed.

Table B-1. Specification, Prompt, and Default Summary

DISPLAY MESSAGE	9010A PROMPTS FOR THIS VALUE:	PRESSING THE ENTER KEY CAUSES THE 9010A TO SUPPLY THIS VALUE (S).
Learn Operation		
LEARN @ _	First Address	Entire uP Address Space as Specified by Interface Pod.
LEARN @ aaaa-_	Second Address	First Address (*aaaa*)
*LEARN @ aaaa-aaaa **	NA	NA
View Operation -- UUT Address Descriptors		
IO @ _	First Address	NA
IO @ aaaa-_	Second Address	NA
IO @ aaaa (-aaaa) BTS _	Read/Write Bit Mask	NA
*IO @ aaaa (-aaaa) BTS hhhh **	NA	NA
RAM @ -	First Address	NA
RAM @ aaaa-	Second Address	NA
*RAM @ aaaa (-aaaa) **	NA	NA
ROM @ _	First Address	NA
ROM @ aaaa-_	Second Address	NA
ROM @ aaaa (-aaaa) SIG _	ROM Signature	9010A Computes Signature
*ROM @ aaaa (-aaaa) SIG nnnn**	NA	NA
Built-In Tests		
*BUS TEST **	NA	NA
*AUTO TEST **	NA	NA
ROM TEST @ _	First Address	UUT ROM Descriptors (Specification Complete)

Table B-1. Specification, Prompt, and Default Summary (cont)

DISPLAY MESSAGE	9010A PROMPTS FOR THIS VALUE	PRESSING THE ENTER KEY CAUSES THE 9010A TO SUPPLY THIS VALUE (s).
Built-In Tests (cont)		
ROM TEST @ aaaa-_	Second Address	First Address *(aaaa)*
ROM TEST @ aaaa (-aaaa) SIG _	ROM Signature	REGB Contents
*ROM TEST @ aaaa (-aaaa) SIG nnnn **	NA	NA
IO TEST @ _	First Address	UUT IO Descriptors (Specification Complete)
IO TEST @ aaaa-_	Second Address	First Address (*aaaa*)
IO TEST @ aaaa (-aaaa) BTS _	Read/Write Bit Mask	REGA Contents
IO TEST @ aaaa (-aaaa) BTS hhhh	NA	NA
RAM SHORT @ _	First Address	UUT RAM Descriptors (Specification Complete)
RAM SHORT @ aaaa-_	Second Address	First Address (*aaaa*)
*RAM SHORT @ aaaa (-aaaa) **	NA	NA
RAM LONG @ _	First Address	UUT RAM Descriptors (Specification Complete)
RAM LONG @ aaaa-_	Second Address	First Address (*aaaa*)
*RAM LONG @ aaaa (-aaaa) **	NA	NA
Troubleshooting Functions		
READ @ _	Address	REGF Contents
*READ @ aaaa **	NA	NA
*READ @ STS **	NA	NA
WRITE @ _	Address	REGF Contents
WRITE @ aaaa = _	Data To Be Written	REGE Contents
*WRITE @ aaaa = hhhh **	NA	NA
WRITE @ CTL = _	NA	NA
*WRITE @ CTL = mmmmmmmm **	NA	NA
RAMP @ _	Address	REGF Contents
*RAMP @ aaaa **	NA	NA
WALK @ _	Address	REGF Contents
WALK @ aaaa = _	Data To Be Written	REGE Contents
*WALK @ aaaa = hhhh **	NA	NA
ATOG @ _	Address	REGF Contents
ATOG @ aaaa BIT _	Bit Number of Address Bit To Be Toggled	REGD Contents
*ATOG @ aaaa BIT dd **	NA	NA

Table B-1. Specification, Prompt, and Default Summary (cont)

DISPLAY MESSAGE	9010A PROMPTS FOR THIS VALUE	PRESSING THE ENTER KEY CAUSES THE 9010A TO SUPPLY THIS VALUE (s).
Troubleshooting Functions (cont)		
DTOG @ _	Address	REGF Contents
DTOG @ aaaa = _	Data To Be Written	REGE Contents
DTOG @ aaaa = hhhh BIT _	Bit Number of Data Bit To Be Toggled	REFD Contents
*DTOG @ aaaa = hhhh BIT dd **	NA	NA
DTOG @ CTL = _	Control Line Information	REGC Contents
DTOG @ CTL = bbbbbbbb BIT _	Bit Number of Control Line To Be Toggled	REGD Contents
*DTOG @ CTL = bbbbbbbb BIT d **	NA	NA
UUT uP Emulation Mode		
RUN UUT @ _	Address Where Execution of UUT Program Code Begins	Address Specified by Setup Parameter
*RUN UUT (@ aaaa) **		NA
Executing Programs		
EXECUTE PROGRAM _	Number of Program To Be Executed	Last Program Executed
*EXECUTE PROGRAM dd **	NA	NA

NOTES:

*Indicates the display message when the specification is complete and execution begins.

(-aaaa) = Second Address Optional
NA = Not Applicable
dd = Decimal Value
aaaa = Hexadecimal Value
hhhh = Hexadecimal Value
nnnn = Hexadecimal Value
mmmmmmmm = Binary Value

Appendix C
Message List

The messages in this appendix are arranged in alphabetical order for quick reference. The numbers and letters in parentheses after each introductory sentence refer to the section of this manual in which each message is located. Some of the messages in this list appear only in the 9010A Programming Manual as indicated.

Table C-2. Message List

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with the detection of and looping on the active force line pending UUT system error (4F-2).	
ACTIVE FORCE LINE(@ address)	
ACTIVE FORCE LINE(@ address) -LOOP	
The following messages are associated with the detection of and looping on the active interrupt UUT system error (4F-2).	
ACTIVE INTERRUPT(@ address)	Looping/Error Present
ACTIVE INTERRUPT(@ address) -LOOP	Initial Detection
The following message is associated with the active interrupt UUT system error (4F-2).	
ACTIVE INTERRUPT(@ aaaa) -LOOP?	
The following messages are associated with the detection of address line tied high from Bus Test and Auto Test (4H-4).	
ADDR BIT aa OK	Looping or Stopped/Error Absent
ADDR BIT aa TIED HIGH	Looping or Stopped/Error Present
ADDR BIT aa TIED HIGH-LOOP?	Initial Detection
The following messages are associated with the detection of address lines tied low from Bus Test and Auto Test (4H-4).	
ADDR BIT aa OK	Looping or Stopped / Error Absent
ADDR BIT aa TIED LOW	Looping or Stopped / Error Present
ADDR BIT aa TIED LOW-LOOP?	Initial Detection

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with detection of address lines tied high from Bus Test and Auto Test (4H-4).	
ADDR BIT a1 AND a2 OK	Looping Error Absent
ADDR BITS a1 AND a2 TIED	Looping Error Present
ADDR BITS a1 AND a2 TIED-LOOP?	Initial Detection
The following messages are the second lines of messages associated with UUT system errors detecting and reporting address lines with drivability errors (4F-2).	
ADDR BITS hhhhhhhh	Stopped Error Present/Absent
ADDR BITS hhhhhhhh - LOOP?	Initial Detection
The following messages are the first lines of two-line messages associated with UUT system errors indicating address line drivability errors (4F-2).	
ADDR ERR @ aaaa	Looping/Error Present
ADDR ERR @ aaaa - LOOP?	Initial Detection
ADDR OK @ aaaa	Looping/Error Absent
The following messages are associated with specifying and performing the Toggle Address troubleshooting function (4I-8).	
ATOG @ _	Prompt for Address
ATOG @ addr BIT _	Prompt for Address Bit Number
ATOG @ addr BIT bit	Specification Complete
ATOG @ addr BIT bit FAIL	Unsuccessful Completion
ATOG @ addr BIT bit OK	Successful Completion
ATOG @ addr BIT bit WAIT	Specification Complete and in Progress
The following messages are associated with Auto Test (4H-20).	
AUTO TEST	Specification Complete
AUTO TEST FAIL	Unsuccessful Completion
AUTO TEST OK	Successful Completion
AUTO TEST WAIT	Specification Completion and in Progress
The following messages may be displayed when an AUX I/F operation is selected (001-3).	
AUX INTERFACE NOT PRESENT	AUX I/F Not Installed
AUX - SELECT ACTION	Prompt for Selection of Operation
The following messages may be displayed when an AUX I/F Read operation is selected (001-3 and 001-8).	
AUX-RECEIVE ABORTED	Operation Aborted
AUX-RECEIVE - ARE YOU SURE?	Memory Protection
AUX-RECEIVING -	Operation in Progress
AUX-RECEIVING - COMPLETE	Operation Completed

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following error messages may be displayed when the AUX I/F Read operation is selected (001-8).	
AUX-RECEIVING - ABORT ERROR	Operation Aborted
AUX-RECEIVING - CHECKSUM ERROR	Error in Line-by-Line Checksum; Data Transmission Problems
AUX-RECEIVING - ERROR	Miscellaneous Transmission Problems
AUX-RECEIVING - FRAMING ERROR	Synchronization Lost During Transmission
AUX-RECEIVING - OVERFLOW ERROR	Memory Filled
AUX-RECEIVING - PARITY ERROR	Parity In Error
The following messages may be displayed when an AUX I/F Write operation is selected (001-3).	
AUX-SENDING -	Operation in Progress
AUX-SENDING - COMPLETE	All Information Is Sent
AUX-SENDING STALLED	Stall Character Received from Remote Device
The following messages are associated with the detection of and looping on the UUT system error of improper power supply voltages at the UUT μP socket (4F-2).	
BAD PWR SUPPLY(@ aaaa)-LOOP?	Initial Detection
BAD PWR SUPPLY(@ aaaa)-YES	Looping/Error Present
The following messages are associated with Bus Test (4H-2).	
BUS TEST	Specification Complete
BUS TEST FAIL	Unsuccessful Completion
BUS TEST OK	Successful Completion
BUS TEST WAIT	Operation in Progress
The following messages are associated with complementing a register (4J-3).	
*CPL REG_*	Prompt for Register Number
CPL REG x = newvalue	Successful Completion
The following messages are the second lines of messages associated with UUT system errors detecting and reporting control lines with drivability errors (4F-2).	
CTL BITS bbbbbbbb	Stopped/Error Present
CTL BITS bbbbbbbb-LOOP?	Initial Detection
CTL BITS 00000000	Stopped/Error Absent
The following messages are the first lines of two-line messages associated with UUT system errors indicating control line drivability errors (4F-2).	
CTL ERR(@ aaaa)	Looping/Error Present
CTL ERR(@ aaaa)-LOOP?	Initial Detection
CTL OK (@ aaaa)	Looping/Error Absent

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with the detection of and looping on Bus Test or Auto Test control drivability errors (4H-4).	
CTL ERR bbbbbbbb bbbbbbbb	Looping/Error Present
CTL ERR bbbbbbbb bbbbbbbb-LOOP?	Initial Detection
CTL OK 00000000 00000000	Looping/Error Absent
The following messages are associated with the detection and exercising of data lines tied low in Bus Test and Auto Test (4H-4).	
DATA BIT dd OK	Looping/Error Absent
DATA BIT dd TIED LOW	Looping/Error Present
DATA BIT dd TIED LOW-LOOP?	Initial Detection
The following messages are associated with the detection and exercising of data lines tied high in Bus Test and Auto Test (4H-4).	
DATA BIT dd OK	Looping/Error Absent
DATA BIT dd TIED HIGH	Looping/Error Present
DATA BIT dd TIED HIGH-LOOP?	Initial Detection
The following messages are associated with the detection of data lines tied together from Bus Test and Auto Test (4H-4).	
DATA BITS d1 AND d2 OK	Looping/Error Absent
DATA BITS d1 AND d2 TIED	Looping/Error Present
DATA BITS d1 AND d2 TIED-LOOP?	Initial Detection
The following messages are the second lines of messages associated with UUT system errors detecting and reporting data lines with drivability errors (4F-2).	
DATA BITS hhhhhhhh	Looping/Error Present
DATA BITS hhhhhhhh-LOOP?	Initial Detection
DATA BITS 00000000	Looping/Error Absent
The following messages are the first lines of two-line messages associated with UUT system errors indicating data line drivability errors (4F-2).	
DATA ERR @ aaaa	Looping/Error Present
DATA ERR @ aaaa-LOOP?	Initial Detection
DATA OK @ aaaa	Looping/Error Absent
The following messages are the second lines of a RAM Long error message (4H-17).	
DATA WAS xxxx	Stopped/Error Absent
DATA WAS xxxx NOT hhhh	Stopped/Error Present
DATA WAS xxxx NOT hhhh-LOOP?	Initial Report

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with decrementing a register (4J-3).	
*DEC REG_*	Prompt for Register Number
DEC REG x = newvalue	Successful Completion
The following message is in response to an attempt to delete an entire test by pressing the CLEAR key when the first program step is displayed in the Programming mode (Programming Manual).	
DELETE PROG nn - ARE YOU SURE?	Response to Pressing CLEAR Key
The following message is associated with the DISPLAY key (Programming Manual).	
DPY-	Response to Pressing DISPLAY Key
DPY-Text	Specification Complete
The following messages are associated with the Toggle Data function (4I-9).	
DTOG @ _	Prompt for Address
DTOG @ address = _	Prompt for Data
DTOG @ address = data BIT _	Prompt for Bit Number
DTOG @ address = data BIT bit	Specification Complete
DTOG @ address = data BIT bit FAIL	Unsuccessful Completion
DTOG @ address = data BIT bit OK	Successful Completion
DTOG @ address = data BIT bit WAIT	Operation in Progress
The following messages are associated with the Data Toggle Control function (4I-10).	
DTOG @ CTL = _	Prompt for Control Lines
DTOG @ = control BIT _	Prompt for Bit Number
DTOG @ CTL = control BIT bit	Specification Complete
DTOG @ CTL = control BIT bit FAIL	Unsuccessful Completion
DTOG @ CTL = control BIT bit OK	Successful Completion
DTOG @ CTL = control BIT bit WAIT	Operation in Progress
The following message refers to errors associated with labels when attempting to exit the Programming Mode (Programming Manual).	
DUPLICATE LABEL x	Label *x* Is Used More Than Once
The following message appears as the last message of a program in the Programming Mode (Programming Manual).	
END OF PROGRAM nn	
The following program messages are associated with executing programs (4L-3).	
EXECUTE PROGRAM _	Prompt for Program Number
EXECUTE PROGRAM nn	Specification Complete
EXECUTE PROGRAM nn - NOT FOUND	Program Not Stored in Memory

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with fatal errors that cause exits from the Executing Mode. The last four messages indicate something is wrong with the construction of the program and must be changed (4L-4).	
FATAL-ATTEMPTED RECURSION	Program Called Itself as Subroutine
FATAL-DEPTH EXCEEDED	Program Called More Than 10 Levels Away
FATAL-MEMORY EXCEEDED FOR LEARN	Address Descriptors Exceed Internal Memory
FATAL-NUMERIC VALUE OUT OF RANGE	Specified Expression Not Within uP Range
FATAL-PROGRAM NOT FOUND	Program Called Non-Existent Program
FATAL-TEST NOT FOUND	Program Called Non-Existent Program
The following messages are associated with the power-up self test.	
FLUKE 9000 POWER-UP FAIL nn	9010A Fails Self Test
FLUKE 9000 POWER-UP OK VER-nn	9010A Passes Self Test
FLUKE 9000 POWER-UP SELF TEST	Initial Power-Up Message
The following message is the quiescent state message associated with the STOP key (4N-2).	
FLUKE 9000 READY	Immediate Mode Quiescent State
The following messages are associated with the restart self test (4A-4).	
FLUKE 9000 RESTARTED FAIL nn	9010A Fails Self Test
FLUKE 9000 RESTARTED OK VER-nn	9010A Passes Self Test
FLUKE 9000 RESTARTED SELF-TEST	In Progress
The following message is associated with the detection of and looping on the UUT system error of improper power supply voltages at the UUT uP socket (4F-2).	
GOOD PWR SUPPLY(@ aaaa)	Looping/Error Absent
The following messages are associated with the specification of the GOTO step in the Programming Mode (Programming Manual).	
GOTO _	Prompt for Hexadecimal Number
GOTO x	Specification Complete
The following messages are associated with the specification of the IF step in the Programming Mode (Programming Manual).	
IF _	Prompt for Expression
IF expr	First Expression Specified, Prompt For Operator
IF expr op _	Operator Specified, Prompt for Second Expression
*IF expr op expr_*	Second Expression Specified, Prompt for GOTO
IF expr op expr GOTO _	GOTO Specified, Prompt for Hex Number
IF expr op expr GOTO x	Specification Complete
The following message is associated with the Illegal Address UUT system error (4F-2).	
ILLEGAL ADDR @ aaaa-LOOP?	Address Not Within Valid uP Address Space

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with incrementing a register (4J-3).	
*INC REG_*	Prompt for Register Number
INC REGx = newvalue	Successful Completion
The following messages in the Programming Mode inform the programmer that the 9010A's memory for storing programs is full (Programming Manual).	
INSUFFICIENT MEM TO CREATE PROG	
INSUFFICIENT MEM TO SAVE KEY	
INSUFFICIENT MEM TO SAVE STEP	
The following messages are associated with viewing and editing UUT IO address descriptors (4G-7).	
IO @ _	Prompt for First Address
IO @ addr-_	prompt for Second Address
IO @ addr-addr BTS _	Prompt for Bit Mask
IO @ addr-addr BTS bits	UUT IO Descriptor Complete
The following messages are associated with IO Test (4H-6).	
IO TEST	Specification Complete
IO TEST @ _	Prompt for Address
IO TEST @ addr-_	Prompt for Second Address
IO TEST @ addr-addr BTS _	Second address specified, Prompt for Bit Mask
IO TEST @ addr-addr BTS bits	Specification Complete
IO TEST @ addr-addr BTS bits FAIL	Unsuccessful Completion
IO TEST @ addr-addr BTS bit OK	Successful Completion
IO TEST @ addr-addr BTS bits WAIT	In Progress
IO TEST @ addr BTS _	Second Address Defaulted, Prompt for Bit Mask
IO TEST @ addr BTS bits	Specification Complete
IO TEST @ addr BTS bits FAIL	Unsuccessful Completion
IO TEST @ addr BTS bits OK	Successful Completion
IO TEST @ addr BTS bits WAIT	In Progress
IO TEST FAIL	Unsuccessful Completion
IO TEST OK	Successful Completion
IO TEST WAIT	In Progress
The following messages are associated with specification of a label in the Programming Mode (Programming Manual).	
LABEL _	Prompt for Hexadecimal Digit
LABEL x	Specification Complete

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with the LEARN operation (4G-2).	
LEARN	Specification Complete
LEARN @ _	Prompt for First Address
LEARN @ addr-_	Prompt for Second Address
LEARN @ addr-addr FAIL	Unsuccessful Completion
LEARN @ addr-addr NOW aa00	In Progress
LEARN @ addr-addr OK	Successful Completion
LEARN @ addr-addr WAIT	In Progress
LEARN @ addr-addr WAIT	Unsuccessful Completion
LEARN @ addr NOW aa00	In Progress
LEARN @ addr OK	Successful Completion
LEARN @ addr WAIT	In Progress
LEARN FAIL	Unsuccessful Completion
LEARN NOW aa00	In Progress
LEARN OK	Successful Completion
LEARN WAIT	In Progress
The following messages maybe displayed when an AUX I/F Learn operation is selected (001-3).	
LIST ADDR SPACE INFO -	Selection of AUX I/F Learn Operation
LIST ADDR SPACE INTO - COMPLETE	AUX I/F Learn Operation Complete
LIST ADDR SPACE INFO - STALLED	Stall Character Received
The following messages may be dsplayed when an AUX I/F Program operation is selected (001-3).	
LIST ALL PROGRAMS -	Begin Sending All Programs in Memory
LIST ALL PROGRAMS - COMPLETE	All Programs in Memory Sent
LIST ALL PROGRAMS - STALLED	Stall Character Received
The following messages may be displayed when an AUX I/F nn ENTER operation is selected (001-3).	
LIST PROGRAM nn -	Begin Sending Program Number nn
LIST PROGRAM nn - COMPLETE	Program Number nn Sent
LIST PROGRAM nn - NOT FOUND	Program Number nn Is Not Contained in Memory
LIST PROGRAM nn - STALLED	Stall Character Received
The following messages may be displayed when an AUX I/F = (equals) operation is selected (001-3).	
LIST PROGRAM NUMBERS -	Begin Sending Numbers of Existing Numbers
LIST PROGRAM NUMBERS - COMPLETE	All Program Numbers are Sent
LIST PROGRAM NUMBERS - STALLED	Stall Character Received

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages may be displayed when an AUX I/F SETUP operation is selected (001-3).	
LIST SETUP INFO-	Begin Sending Setup Parameters
LIST SETUP INFO - COMPLETE	All Setup Parameters Are Sent
LIST SETUP INFO - STALLED	Stall Character Received
The following message refers to errors associated with labels when attempting to exit the Programming Mode (Programming Manual).	
MISSING LABEL x	A Branch Step Refers to *x*
The following message may appear in response to the selection of the AUX I/F Learn operation (001-3).	
NO ADDRESS SPACE INFO	No Address Descriptors Are in Memory
The following messages are associated with the removal of the active interrupt UUT system error (4F-2).	
NO FORCE LINE(@ address)	No Force Line Reported
NO INTERRUPT(@ aaaa)	No Active Interrupt Pending
The following message may appear in response to the selection of the AUX I/F = (equals) operation or in response to the selection of the AUX I/F Program operation (001-3).	
NO PROGRAMS DEFINED	No Programs Are in Memory
The following messages are associated with VIEW keys when no UUT address space descriptors of the selected types exist (4G-6).	
NO IO INFO	Response to VIEW I/O Key
NO RAM INFO	Response to VIEW RAM Key
NO ROM INFO	Response to VIEW ROM key
The following message is associated with the detection of 9010A timeout errors (4F-2).	
POD RESET ERR - ATTEMPTING RESET	Possible Pod Failure; Perform Pod Self Test
The following messages are associated with the interface pod self test (4A-5).	
POD SELF TEST xxxx OK	Pod Passes Self Test
POD SELF TEST FAIL nn	Pod Fails Self Test
The following message is associated with the detection of 9010A timeout errors (4F-2).	
POD TIMEOUT - ATTEMPTING RESET	General Error Message

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following message is associated with the Read Probe operation in the Immediate Mode (4K-5).	
PROBE-LVL abc COUNT ddd SIG nnnn	
The following messages are associated with entry into and exit from the Programming Mode (Programming Manual).	
PROG nn CLOSED - xxxxx BYTES LEFT	Closing a Program
PROG nn DELETED — xxxxx BYTES LEFT	Deleting a Program
PROGRAM _	Prompt for Program Number
PROGRAM nn CREATED	Program Created
PROGRAM nn OPENED - xx BYTES	Existing Program Opened
PROGRAMS nn nn nn nn nn	List of Existing Programs
The following messages are associated with viewing and editing UUT RAM descriptors (4G-6).	
RAM @ _	Prompt for Address
RAM @ addr	Specification Complete
RAM @ addr-_	Prompt for Second Address
RAM @ addr-addr	Specification Complete
The following messages are associated with reporting and exercising certain classes of RAM errors in both RAM Short as well as RAM Long (4H-16).	
RAM BITS d1 AND d2 OK	Looping/Error Absent
RAM BITS d1 AND d2 TIED	Looping/Error Present
RAM BITS d1 AND d2 TIED-LOOP?	Initial Detection
RAM DCD ERR @ addr BIT bb	Looping/Error Present
RAM DCD ERR @ addr BIT bb-LOOP?	Initial Detection
RAM DCD OK @ addr BIT bb	Looping/Error Absent
The following messages are associated with the specification of RAM Long (4H-17).	
RAM LONG	Specification Complete
RAM LONG @ _	Prompt for Address
RAM LONG @ addr	Specification Complete
RAM LONG @ addr-_	Prompt for Second Address
RAM LONG @ addr-addr	Specification Complete
RAM LONG @ addr-addr FAIL	Unsuccessful Completion
RAM LONG @ addr-addr OK	Successful Completion
RAM LONG @ addr-addr WAIT	In Progress
RAM LONG @ addr FAIL	Unsuccessful Completion
RAM LONG @ addr OK	Successful Completion
RAM LONG @ addr WAIT	In Progress
RAM LONG FAIL	Unsuccessful Completion
RAM LONG OK	Successful Completion
RAM LONG WAIT	In Progress

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are errors that occur exclusively in RAM Long (4H-19).	
RAM PATT ERR @ addr	Looping/Error Present
RAM PATT ERR @ addr-LOOP?	Initial Detection
RAM PATT OK @ addr	Looping/Error Absent
The following messages are associated with the specification of RAM Short (4H-15).	
RAM SHORT	Specification Complete
RAM SHORT @ _	Prompt for Address
RAM SHORT @ addr	Specification Complete
RAM SHORT @ addr _	Prompt for Second Address
RAM SHORT @ addr-addr	Specification Complete
RAM SHORT @ addr-addr FAIL	Unsuccessful Completion
RAM SHORT @ addr-addr OK	Successful Completion
RAM SHORT @ addr-addr WAIT	In Progress
RAM SHORT @ addr FAIL	Unsuccessful Completion
RAM SHORT @ addr OK	Successful Completion
RAM SHORT @ addr WAIT	In Progress
RAM SHORT FAIL	Unsuccessful Completion
RAM SHORT OK	Successful Completion
RAM SHORT WAIT	In Progress
The following messages are associated with the Ramp function (4I-6).	
RAMP @ _	Prompt for Address
RAMP @ addr	Specification Complete
RAMP @ addr FAIL	Unsuccessful Completion
RAMP @ addr OK	Successful Comletion
RAMP @ addr WAIT	In Progress
The following messages are associated with the Read function (4I-2).	
READ @ _	Prompt for Address
READ @ addr	Specification Complete
READ @ addr = data FAIL	Unsuccessful Completion
READ @ addr = data OK	Successful Completion
READ @ addr = data WAIT	In Progress
The following messages are associated with the Read Status function (4I-3).	
READ @ STS	Specification Complete
READ @ STS = bbbb bbbb bbbb FAIL	Unsuccessful Completion
READ @ STS = bbbb bbbb bbbb OK	Successful Completion
READ @ STS = WAIT	In Progress

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following message is the specification of the Read Probe operation in the Programming Mode (Programming Manual).	
READ PROBE	
The following messages are associated with the Read Tape function (4P-4).	
READ TAPE - ABORTED	Operation Aborted
READ TAPE - ARE YOU SURE?	Memory Protection
READ TAPE FAIL	Unsuccessful Completion
READ TAPE - NO CASSETTE	Cassette Missing
READ TAPE OK	Successful Completion
READ TAPE WAIT	Specification Complete
The following messages occur while assigning values to registers initiated by the REG key (4J-3).	
*REG_*	Prompt for Register Number
REGn = _	Register Selected
REGn = value	Successful Completion
The following message occurs whenever the 9010A detects that the probe fuse has blown (2-4).	
REPLACE PROBE FUSE/UNPLUG PROBE	
The following messages are associated with viewing and editing UUT ROM descriptors (4G-6).	
ROM @ _	Prompt for Address
ROM @ addr _	First Address Specified
ROM @ addr-addr SIG _	Second Address Specified
ROM @ addr-addr SIG ssss	Specification Complete
ROM @ addr-addr SIG WAIT	Computing Signatures from UUT
ROM @ addr SIG _	Prompt for Signature
ROM @ addr SIG ssss	Specification Complete
ROM @ addr SIG WAIT	Computing Signatures from UUT
The following messages are associated with the detection of or looping on ROM errors (first line of message only) (4H-12).	
ROM ERR @ addr	Looping/Error Present
ROM ERR @ addr-LOOP?	Initial Detection
ROM OK @ addr	Looping/Error Absent
ROM ERR @ addr-addr	Looping/Error Present
ROM ERR @ addr-addr-LOOP?	Initial Detection
ROM OK @ addr-addr	Looping/Error Absent

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with setting up ROM Test (4H-11).	
ROM TEST	Specification Complete
ROM TEST @ _	Prompt for First Address
ROM TEST @ addr-_	Prompt for Second Address
ROM TEST @ addr-addr SIG _	Second Address Specified; Prompt for Signature
ROM TEST @ addr-addr SIG ssss	Specification Complete
ROM TEST @ addr-addr SIG ssss FAIL	Unsuccessful Completion
ROM TEST @ addr-addr SIG ssss OK	Successful Completion
ROM TEST @ addr-addr SIG ssss WAIT	In Progress
ROM TEST @ addr SIG-_	Second Address Defaulted; Prompt for Signature
ROM TEST @ addr SIG ssss	Specification Complete
ROM TEST @ addr SIG ssss FAIL	Unsuccessful Completion
ROM TEST @ addr SIG ssss OK	Successful Completion
ROM TEST @ addr SIG ssss WAIT	In Progress
ROM TEST FAIL	Unsuccessful Completion
ROM TEST OK	Successful Completion
ROM TEST WAIT	In Progress
The following messages are associated with setting up the Run UUT Mode (4N-5).	
RUN UUT @ _	Prompt for Address
RUN UUT @ addr-MAY NEED RESET	Specification Complete
RUN UUT - MAY NEED RESET	Specification Complete
RUN UUT FAIL	Unsuccessful Action
RUN UUT @ addr FAIL	Unsuccessful Action
The following messages are associated with read-write errors generated by IO Test, RAM Short, and RAM Long (4H-1).	
R/W ERR @ addr BTS mask	Looping/Error Present
R/W ERR @ addr BTS mask-LOOP?	Initial Detection
R/W OK @ addr BTS 0000	Looping/Error Absent
The following messages are associated with the Setup messages (4M-2).	
SET-BEEP ON ERR TRANSITION? NO	Do Not Beep on Appearance or Disappearance of Error
SET-BEEP ON ERR TRANSITION? YES	Beep on Appearance or Disappearance of Error
SET-BUS TEST @ _	Prompt for New Bus Test Address
SET-BUS TEST @ aaaa-CHANGE?	Execution Address (Pod-Dependent)
SET-ENABLE xxxx? NO	μP Enable Line *xxxx* Enabled
SET-ENABLE xxxx? YES	μP Enable Line *xxxx* Enabled
SET-EXERCISE ERRORS? NO	Error Looping (Exercising) Disabled
SET-EXERCISE ERRORS? YES	Error Looping (Exercising) Enabled
SET-LINESIZE _	Prompt for New Line Size
SET-LINESIZE 79-CHANGE?	Maximum Line Length (AUX I/F)
SET-NEWLINE _	Prompt for New Terminator Sequence and Timing Delay

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
Setup Messages (cont)	
SET-NEWLINE 00000D0A-CHANGE?	Terminator Sequence and Timing Delay (AUX I/F)
SET-RUN UUT @ _	Prompt for New Run UUT Starting Address
SET-RUN UUT @ aaaa-CHANGE?	Default Address for Execution (Pod Dependent)
SET-STALL _	Prompt for New Stall Character
SET-STALL 13-CHANGE?	Stall Character
SET-TIMEOUT _	Prompt for New Delay Count
SET-TIMEOUT 200-CHANGE?	Delay Before Timeout
SET-TRAP ACTIVE FORCE LINE? NO	Do Not Report UUT System Error
SET-TRAP ACTIVE FORCE LINE? YES	Report UUT System Error
SET-TRAP ACTIVE INTERRUPT? NO	Do Not Report UUT System Error
SET-TRAP ACTIVE INTERRUPT? YES	Report UUT System Error
SET-TRAP ADDR ERR? NO	Do Not Report UUT System Error
SET-TRAP ADDR ERR? YES	Report UUT System Error
SET-TRAP BAD PWR SUPPLY? NO	Do Not Report UUT System Error
SET-TRAP BAD PWR SUPPLY? YES	Report UUT System Error
SET-TRAP CTL ERR? NO	Do Not Report UUT System Error
SET-TRAP CTL ERR? YES	Report UUT System Error
SET-TRAP DATA ERR? NO	Do Not Report UUT System Error
SET-TRAP DATA ERR? YES	Report UUT System Error
SET-TRAP ILLEGAL ADDRESS? NO	Do Not Report UUT System Error
SET-TRAP ILLEGAL ADDRESS? YES	Report UUT System Error
SET-UNSTALL _	Prompt for New Unstall Character
SET-UNSTALL 11-CHANGE?	Stall Character (AUX I/F)
The following messages are associated with the Shift Left operation (4J-3).	
*SHL REG_*	Prompt for Register Number
SHL REGx = newvalue	Successful Completion
The following messages are associated with the Shift Right operation (4J-3).	
*SHR REG_*	Prompt for Register Number
SHR REGx = newvalue	Successful Completion
The following messages are the second line of the message associated with the detection of and looping on errors in ROM Test (4H-12).	
SIG WAS mmmm	Error Absent
SIG WAS mmmm NOT nnnn	Looping on Error
SIG WAS mmmm NOT nnnn-LOOP?	Initial Detection
The following message is the first message in a program (Programming Manual).	
START OF PROGRAM nn	

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following message appears in the Programming Mode when the programmer attempts to enter a program step that is too long (Programming Manual).	
STEP TOO LONG	
The following message is the stop step as seen in the Programming Mode (Programming Manual).	
STOP	
The following messages can be the second line of a forcing line or active interrupt UUT system error (4F-2).	
STS BITS bbbb bbbb bbbb bbbb	Stopped While Looping
STS BITS bbbb bbbb bbbb bbbb-LOOP?	Detection of Error
The following messages are associated with the specification of probe synchronization (4K-3).	
SYNC <0-F> - _	Prompt for Hexadecimal Digit
SYNC <0-F> ADDRESS (OK)	Address Sync
SYNC <0-F> DATA (OK)	Data Sync
SYNC <0-F> FREE-RUN (OK)	Free-Run
SYNC <0-F> x (OK)	Hexadecimal Digit
The following message is associated with the detection of a timeout error (4F-2).	
UUT POWER FAIL - ATTEMPTING RESET	Reporting Bad Power Supply
The following messages are associated with the Walk function (4I-7).	
WALK @ _	Prompt for Address
WALK @ addr = _	Prompt for Data
WALK @ addr = data	Specification Complete
WALK @ addr = data FAIL	Unsuccessful Completion
WALK @ addr = data OK	Successful Completion
WALK @ addr = data WAIT	In Progress
The following messages are associated with the Write function (4I-4).	
WRITE @ _	Prompt for Address
WRITE @ addr = _	Prompt for Data
WRITE @ addr = data	Specification Completed
WIRTE @ addr = data FAIL	Unsuccessful Completion
WRITE @ addr = data OK	Successful Completion
WRITE @ addr = data WAIT	In Progress

Table C-2. Message List (cont)

DISPLAY MESSAGE	DESCRIPTION
The following messages are associated with the Write Control function (4I-5).	
WRITE @ CTL = _	Prompt for Control Lines
WRITE @ CTL = control	Specification Complete
WRITE @ CTL = control FAIL	Unsuccessful Completion
WRITE @ CTL = control OK	Successful Completion
WRITE @ CTL = control WAIT	In Progress
The following messages are associated with the Write Tape operation (4P-5).	
WRITE TAPE ABORTED	Operation Aborted
WRITE TAPE - ARE YOU SURE?	Tape Protection
WRITE TAPE FAIL	Unsuccessful Completion
WRITE TAPE - NO CASSETTE	Cassette Missing
WRITE TAPE OK	Successful Completion
WRITE TAPE WAIT	Operation in Progress
WRITE TAPE - WRITE PROTECTED	Cassette Is Write-Protected

Appendix D
ASCII and Hexadecimal/Decimal Conversion Tables

This appendix section contains information on the ASCII character set, hexadecimal to decimal conversion, and decimal to hexadecimal conversion.

Table D-1. Hexadecimal to Decimal Conversion

DECIMAL EQUIVALENT				HEX DIGIT
DIGIT POSITION				
3	2	1	0	
0	0	0	0	0
4096	256	16	1	1
8192	512	32	2	2
12288	768	48	3	3
16384	1024	64	4	4
20480	1280	80	5	5
24576	1536	96	6	6
28672	1792	112	7	7
32768	2048	128	8	8
36864	2304	144	9	9
40960	2560	160	10	A
45056	2816	176	11	B
49152	3072	192	12	C
53248	3328	208	13	D
57344	3584	224	14	E
61440	3840	240	15	F

Table D-2. Decimal to Hexadecimal Conversion

HEXADECIMAL EQUIVALENT					DECIMAL DIGIT
DIGIT POSITION					
4	3	2	1	0	
0	0	0	0	0	0
2710	3E8	64	A	1	1
4E20	7D0	C8	14	2	2
7530	BB8	12C	1E	3	3
9C40	FA0	190	28	4	4
C350	1388	1F4	32	5	5
EA60	1770	258	3C	6	6
11170	1B58	2BC	46	7	7
13880	1F40	320	50	8	8
15F90	2328	384	5A	9	9

Table D-3. ASCII Character Set

ASCII CHAR.	DECIMAL	OCTAL	HEX	BINARY 7654 3210	DEV. NO.	MESSAGE ATN=TRUE		ASCII CHAR.	DECIMAL	OCTAL	HEX	BINARY 7654 3210	DEV. NO.	MESSAGE ATN=TRUE	
NUL	0	000	00	0000 0000			ADDRESSED COMMANDS	@	64	100	40	0100 0000	0	MTA	TALK ADDRESSES
SQH	1	001	01	0000 0001		GTL		A	65	101	41	0100 0001	1	MTA	
STX	2	002	02	0000 0010				B	66	102	42	0100 0010	2	MTA	
ETX	3	003	03	0000 0011				C	67	103	43	0100 0011	3	MTA	
EOT	4	004	04	0000 0100		SDC		D	68	104	44	0100 0100	4	MTA	
ENQ	5	005	05	0000 0101		PPC		E	69	105	45	0100 0101	5	MTA	
ACK	6	006	06	0000 0110				F	70	106	46	0100 0110	6	MTA	
BELL	7	007	07	0000 0111				G	71	107	47	0100 0111	7	MTA	
BS	8	010	08	0000 1000		GET		H	72	110	48	0100 1000	8	MTA	
HT	9	011	09	0000 1001		TCT		I	73	111	49	0100 1001	9	MTA	
LF	10	012	0A	0000 1010				J	74	112	4A	0100 1010	10	MTA	
VT	11	013	0B	0000 1011				K	75	113	4B	0100 1011	11	MTA	
FF	12	014	0C	0000 1100				L	76	114	4C	0100 1100	12	MTA	
CR	13	015	0D	0000 1101				M	77	115	4D	0100 1101	13	MTA	
SO	14	016	0E	0000 1110				N	78	116	4E	0100 1110	14	MTA	
SI	15	017	0F	0000 1111				O	79	117	4F	0100 1111	15	MTA	
DLE	16	020	10	0001 0000			UNIVERSAL COMMANDS	P	80	120	50	0101 0000	16	MTA	
DC1	17	021	11	0001 0001		LLO		Q	81	121	51	0101 0001	17	MTA	
DC2	18	022	12	0001 0010				R	82	122	52	0101 0010	18	MTA	
DC3	19	023	13	0001 0011				S	83	123	53	0101 0011	19	MTA	
DC4	20	024	14	0001 0100		DCL		T	84	124	54	0101 0100	20	MTA	
NAK	21	025	15	0001 0101		PPU		U	85	125	55	0101 0101	21	MTA	
SYN	22	026	16	0001 0110				V	86	126	56	0101 0110	22	MTA	
ETB	23	027	17	0001 0111				W	87	127	57	0101 0111	23	MTA	
CAN	24	030	18	0001 1000		SPE		X	88	130	58	0101 1000	24	MTA	
EM	25	031	19	0001 1001		SPD		Y	89	131	59	0101 1001	25	MTA	
SUB	26	032	1A	0001 1010				Z	90	132	5A	0101 1010	26	MTA	
ESC	27	033	1B	0001 1011				[	91	133	5B	0101 1011	27	MTA	
FS	28	034	1C	0001 1100				\	92	134	5C	0101 1100	28	MTA	
GS	29	035	1D	0001 1101				]	93	135	5D	0101 1101	29	MTA	
RS	30	036	1E	0001 1110				^	94	136	5E	0101 1110	30	MTA	
US	31	037	1F	0001 1111				_	95	137	5F	0101 1111		UNT	
SPACE	32	040	20	0010 0000	0	MLA	LISTEN ADDRESSES	`	96	140	60	0110 0000	0	MSA	SECONDARY ADDRESSES
!	33	041	21	0010 0001	1	MLA		a	97	141	61	0110 0001	1	MSA	
"	34	042	22	0010 0010	2	MLA		b	98	142	62	0110 0010	2	MSA	
#	35	043	23	0010 0011	3	MLA		c	99	143	63	0110 0011	3	MSA	
$	36	044	24	0010 0100	4	MLA		d	100	144	64	0110 0100	4	MSA	
%	37	045	25	0010 0101	5	MLA		e	101	145	65	0110 0101	5	MSA	
&	38	046	26	0010 0110	6	MLA		f	102	146	66	0110 0110	6	MSA	
'	39	047	27	0010 0111	7	MLA		g	103	147	67	0110 0111	7	MSA	
(	40	050	28	0010 1000	8	MLA		h	104	150	68	0110 1000	8	MSA	
)	41	051	29	0010 1001	9	MLA		i	105	151	69	0110 1001	9	MSA	
*	42	052	2A	0010 1010	10	MLA		j	106	152	6A	0110 1010	10	MSA	
+	43	053	2B	0010 1011	11	MLA		k	107	153	6B	0110 1011	11	MSA	
,	44	054	2C	0010 1100	12	MLA		l	108	154	6C	0110 1100	12	MSA	
-	45	055	2D	0010 1101	13	MLA		m	109	155	6D	0110 1101	13	MSA	
.	46	056	2E	0010 1110	14	MLA		n	110	156	6E	0110 1110	14	MSA	
/	47	057	2F	0010 1111	15	MLA		o	111	157	6F	0110 1111	15	MSA	
0	48	060	30	0011 0000	16	MLA		p	112	160	70	0111 0000	16	MSA	
1	49	061	31	0011 0001	17	MLA		q	113	161	71	0111 0001	17	MSA	
2	50	062	32	0011 0010	18	MLA		r	114	162	72	0111 0010	18	MSA	
3	51	063	33	0011 0011	19	MLA		s	115	163	73	0111 0011	19	MSA	
4	52	064	34	0011 0100	20	MLA		t	116	164	74	0111 0100	20	MSA	
5	53	065	35	0011 0101	21	MLA		u	117	165	75	0111 0101	21	MSA	
6	54	066	36	0011 0110	22	MLA		v	118	166	76	0111 0110	22	MSA	
7	55	067	37	0011 0111	23	MLA		w	119	167	77	0111 0111	23	MSA	
8	56	070	38	0011 1000	24	MLA		x	120	170	78	0111 1000	24	MSA	
9	57	071	39	0011 1001	25	MLA		y	121	171	79	0111 1001	25	MSA	
:	58	072	3A	0011 1010	26	MLA		z	122	172	7A	0111 1010	26	MSA	
;	59	073	3B	0011 1011	27	MLA		{	123	173	7B	0111 1011	27	MSA	
<	60	074	3C	0011 1100	28	MLA		|	124	174	7C	0111 1100	28	MSA	
=	61	075	3D	0011 1101	29	MLA		}	125	175	7D	0111 1101	29	MSA	
>	62	076	3E	0011 1110	30	MLA		~	126	176	7E	0111 1110	30	MSA	
?	63	077	3F	0011 1111		UNL			127	177	7F	0111 1111			

Note: The shaded portions of Table D-3 are included for reference.