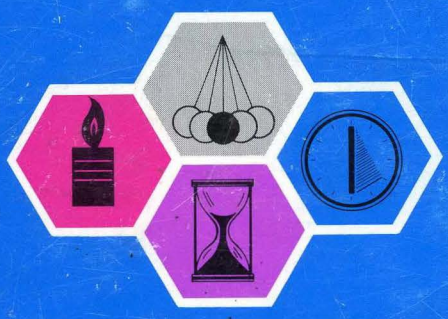
INSTRUCTION MANUAL
MODEL 9210
TIME CODE TRANSLATOR



DATUM TTI
TIMING DIVISION

INSTRUCTION MANUAL

MODEL 9210

TIME CODE TRANSLATOR

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Number	Title
15584	AGC Amplifier
15585	Bandpass Filter
15599	DC Code
15603	Filter Switch
15622	Failsafe
15662	Minor Time Counter
15663	36-Bit Buffer
15664	Major Time Counter
15666	Front Panel Display
15673	Decoder #1
15675	Sync Mode
15722	RAW Supply
15728	Regulator (+15V, +5V, -15V)
15788	Decoder #2

DRAWING LIST

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Number	Title
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②	Input and Decode
④	AC Failsafe
④	DC Code and Failsafe
⑤	Decoder Control Logic
⑦	Sync Mode and Loading
⑧	Minor Time Counter
⑨	Major Time Counter
⑩	Display
	SCHEMATIC DIAGRAMS
15584	AGC Amplifier
15585	Band Pass Filter
15599	DC Code
15603	Filter Switch
15622	Failsafe
15662	Minor Time Counter
15663	36-Bit Buffer
15664	Major Time Counter
15666	Front Panel Display
15673	Decoder #1
15675	Sync Mode
15722	RAW Supply
15728	Regulator (+15V, +5V, -15V)
15788	Decoder #2

CHAPTER ONE

GENERAL DESCRIPTION

1.1 INTRODUCTION

This instruction manual contains procedures and descriptive information for proper installation, operation, and maintenance of the Model 9210 Time Code Translator (TCT).

1.2 DOCUMENTATION

Since the 9210 has many options designed to meet individual instrumentation requirements, this manual is divided into two sections. The first section describes all configurations of the 9210 basic instrument and comes complete with logics, specifications and schematics. The second section or appendix contains information on all modifications and special options added to the basic 9210. The appendix also contains the top assembly drawing and any other special documentation applicable to this unit.

Each engineering drawing or specification in this instruction manual is identified by a unique DATUM file number which is located on the specification sheet or at the lower righ corner of the drawing sheet. The file numbers assigned to the circuit-card assemblies or schematic drawings are the same as the part numbers assigned to the corresponding cards.

1.3 PURPOSE OF EQUIPMENT

The DATUM Model 9210 Time Code Translator operates as a reader using a serial time code as a time base.

The 9210 relies upon an input serial time code for its time base. This code is typically a member of the IRIG family. The carrier frequency of the time code is used for the clock and the time information is automatically set into the major time counter.

The terms derived from both the minor and the major time counters are also used to drive option circuits which develop the serial time codes, parallel outputs, and pulse trains, etc.

1.4 PHYSICAL DESCRIPTION

The 9210 is constructed in a 3-1/2" package requiring a minimum 19" rack mounting. A decimal display, located on the front panel, shows translated time. All controls are located either on the front panel or on a subpanel, located just behind the front panel, with the controls facing in an upward position. To reach the controls on the subpanel, the 9210 must be pulled forward about 6 inches. Chassis slides are provided to allow this to be done easily.

1.5 SPECIFICATIONS

Refer to Table 1-1 for the specifications applicable to the Model 9210 Time Code Translator. Changes or additions to these specifications, if any, are listed in Appendix A.

Refer to Figures 1-1 through 1-6 for the applicable IRIG Time Code formats.

TABLE 1-1

SPECIFICATIONS

1. AC POWER
   a) 115 VAC or 230 VAC ±10%
   b) 48 - 400 Hz
   c) Less than 100 watts

2. CARRIER CODE INPUTS
   a) Formats: IRIG A, IRIG B, IRIG C, IRIG E, IRIG G, IRIG H
   b) Carrier Frequencies:
      IRIG A - 10 kHz
      IRIG B - 1 kHz
      IRIG C - 1 kHz or 100 Hz
      IRIG E - 1 kHz or 100 Hz
      IRIG G -100 kHz
      IRIG H - 1 kHz or 100 Hz
   c) Modulation Ratio: 2:1 to 6:1
   d) Input Signal Level:
      1. Hi Input: 0.05 volts to 50.0 volts peak-to-peak
      2. Lo Input: 0.01 volts to 10.0 volts peak-to-peak
   e) Input Impedance: Greater than 15 k ohms, single-ended
   f) Frequency Range: 25 Hz to 500 kHz

3. DC CODE INPUTS (OPTIONAL)
   a) Logic Polarity: Positive true or negative true
   b) Formats: IRIG A, IRIG B, IRIG C, IRIG E, IRIG G or IRIG H
   c) Playback Ratios:

IRIG A	1:1 to 16:1
IRIG B	1:1 to 128:1
IRIG C	1:1 to 128:1
IRIG E	1:1 to 128:1
IRIG G	1:1 to 4:1
IRIG H	1:1 to 128:1

d) Input Signal Conditions

1. Voltage Levels: positive, negative, or bi-polar
2. Amplitude Range: ±1 volt to 50 volts peak
3. Input Impedance: greater than 8 k ohms, single-ended
4. Rise and Fall Times: Less than 1 microsecond

4. ENVIRONMENT

a) Temperature: 0°C to +50°C

b) Humidity: Up to 95% relative

5. SIZE AND CONFIGURATION

a) Chassis: 3-1/2 inches high, 19 inches wide, 17 inches deep

b) Mounting: Standard 19-inch equipment cabinet with chassis slides supplied.

IRIG FORMAT A:

1. Time: Universal Time (UT-2).

2. Time frame: 0.1 second.

3. Code Digit Weighting options. BCD, SB or both:

   a. Binary Coded Decimal time-of-year Code Word—34 binary digits.
      (1) Seconds, minutes, hours, days and 0.1 seconds.
      (2) Recycles yearly.

   b. Straight Binary time-of-day Code Word—17 binary digits.
      (1) Seconds only.
      (2) Recycles each 24 hours.

4. Code Word structure:

   a. BCD: Word begins at Index Count 1. Binary coded Elements occur between Position Identifier Elements (7 for seconds; 7 for minutes; 6 for hours; 8 and 2 for days) until the Code Word is complete. An Index Marker occurs between decimal digits in each group to provide separation for visual resolution.

   b. SB: Word begins at Index Count 80. Five decimal digits (17 binary coded elements) occur with a Position Identifier between the 9th and 10th binary coded elements.

5. Least significant digit occurs first, except for fractional seconds information which occurs following the day-of-year information.

6. Element rates Available:

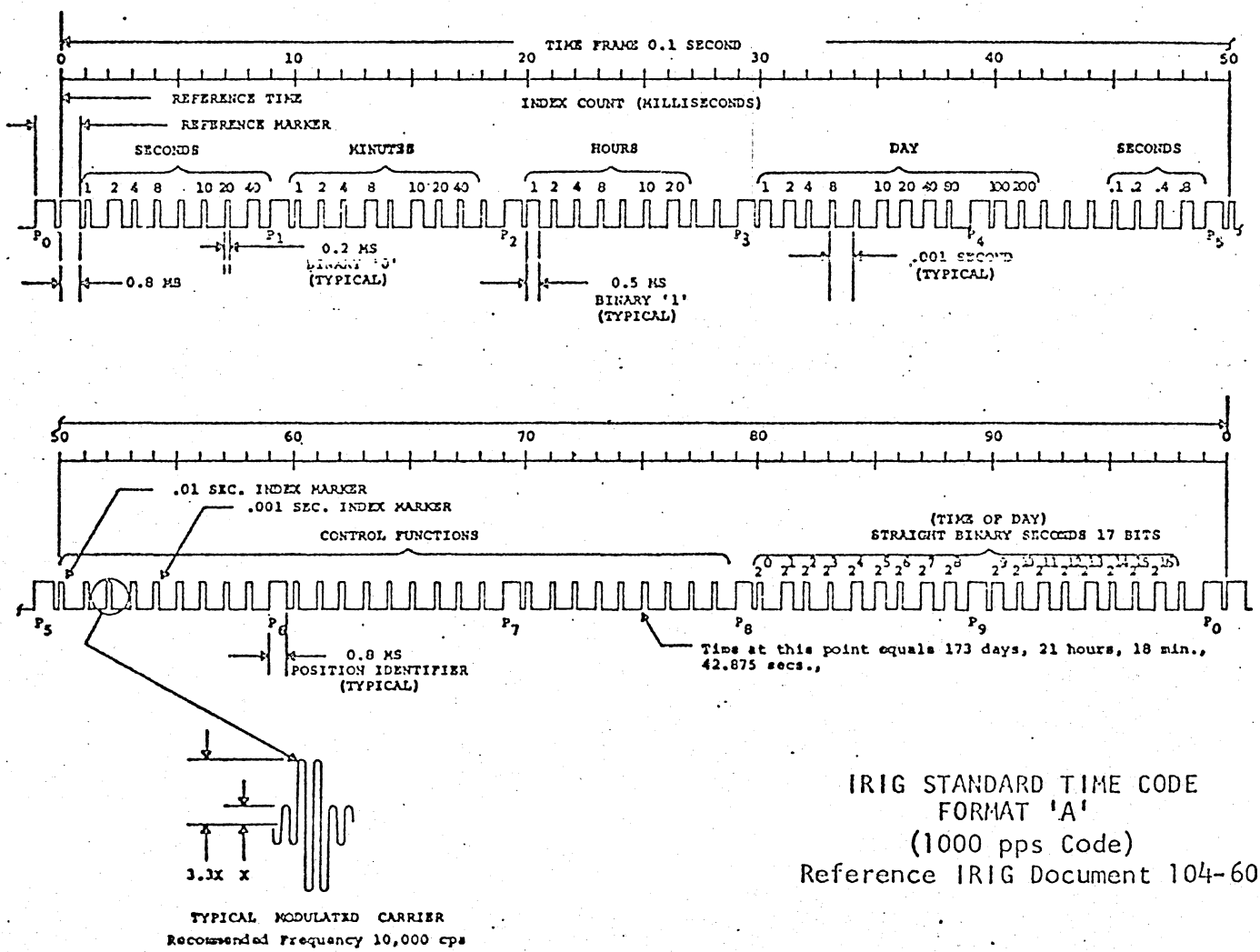
   a. 1000 per second (basic Element rate).
   b. 100 per second.
   c. 10 per second.

7. Element identification:

   a. "On time" reference point for all Elements is the leading edge.
   b. Index Marker ..... 0.2 milliseconds.
      (Binary Zero or uncoded Element).
   c. Code Digit ..... 0.5 milliseconds.
      (Binary one).
   d. Position Identifier — 100 per second. ..... 0.8 milliseconds.
      (Refers to the leading edge of the succeeding Element).
   e. Reference Marker—10 per second ..... Two consecutive Position Identifiers.
      (The "on time" point, to which the Code Word refers, is the leading edge of the second Position Identifier).

8. Resolution: 1 millisecond (unmodulated).
   0.1 millisecond (modulated).

9. Carrier modulation not normally required, 10 kc. recommended when modulated.



IRIG STANDARD TIME CODE
FORMAT 'A'
(1000 pps Code)
Reference IRIG Document 104-60

Figure 1-1. IRIG Time Code, Format "A"

IRIG FORMAT B:

1. Time: Universal Time (UT-2).

2. Time Frame: 1.0 second.

3. Code Digit Weighting options: BCD, SB or both.

   a. Binary Coded Decimal time-of-year Code Word—30 binary digits.
      (1) Seconds, minutes, hours and days.
      (2) Recycles yearly.

   b. Straight Binary time-of-day Code Word—17 binary digits.
      (1) Seconds only.
      (2) Recycles each 24 hours.

4. Code Word structure:

   a. BCD: Word begins at Index Count 1. Binary coded Elements occur between Position Identifier Elements (7 for seconds, 7 for minutes; 6 for hours, 8 and 2 for days) until the Code Word is complete. An Index Marker occurs between decimal digits in each group to provide separation for visual resolution.

   b. SB: Word begins at Index Count 80. Five decimal digits (17 binary coded elements) occur with a Position Identifier between the 9th and 10th binary coded elements.

5. Least significant digit occurs first.

6. Element rates available:

   a. 100 per second (basic Element rate).
   b. 10 per second
   c. 1 per second.

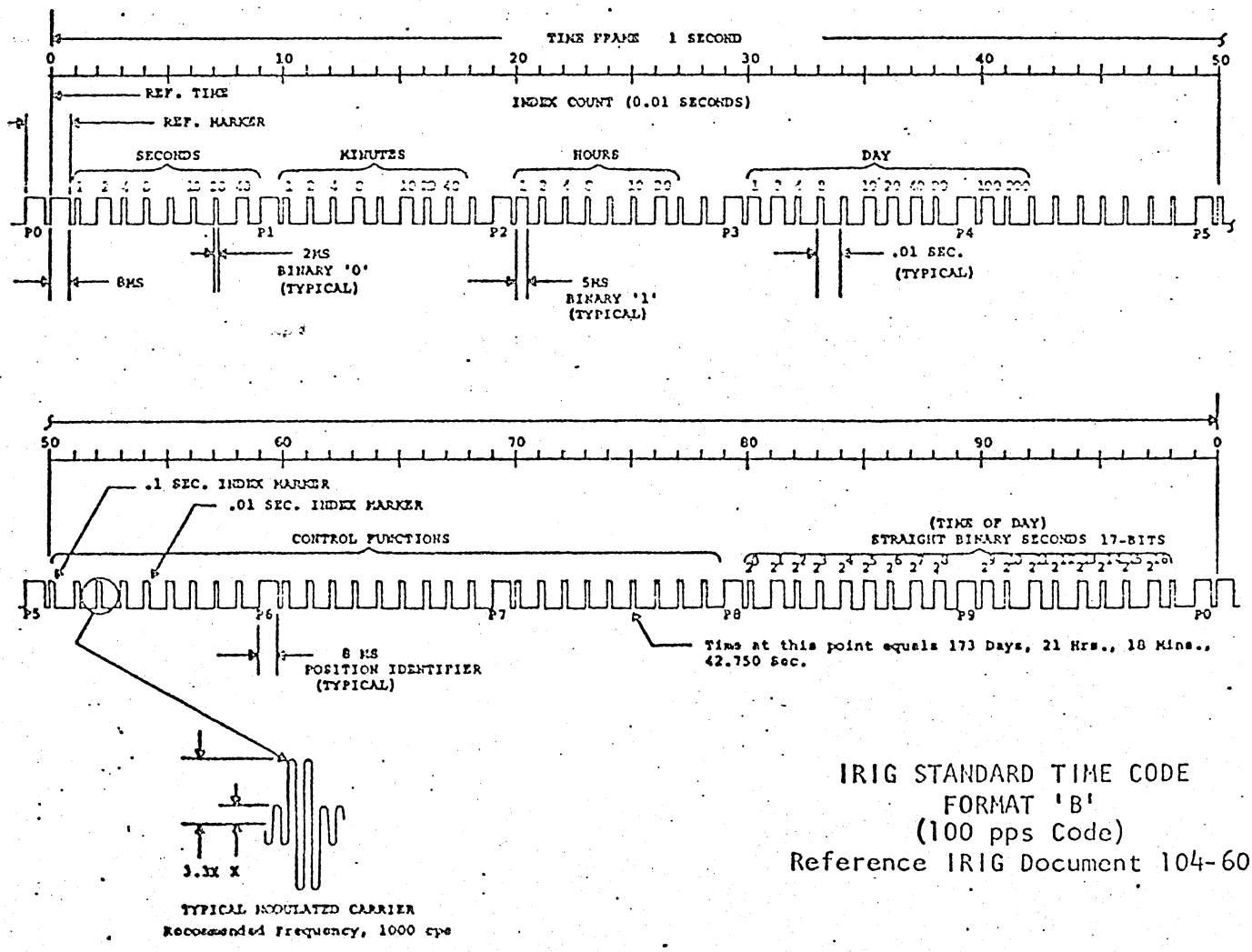
7. Element identification:

   a. "On time" reference point for all Elements is the leading edge.
   b. Index Marker ..... 2 milliseconds.
      (Binary zero or uncoded Element).
   c. Code Digit ..... 5 milliseconds.
      (Binary one).
   d. Position Identifier—10 per second ..... 8 milliseconds.
      (Refers to the leading edge of the succeeding Element).
   e. Reference Marker—1 per second ..... Two consecutive Position Identifiers.

   (The "on time" point, to which the Code Word refers, is the leading edge of the second Position Identifier).

8. Resolution: 10 milliseconds (unmodulated).
   1 millisecond (modulated).

9. Carrier frequency: 1 kc. when modulated.



IRIG STANDARD TIME CODE
FORMAT 'B'
(100 pps Code)
Reference IRIG Document 104-60

Figure 1-2. IRIG Time Code, Format "B"

IRIG FORMAT C:

1. Time: Universal Time (UT-2).

2. Time Frame: 1 minute.

3. Code Digit Weighting options: Binary Coded Decimal time-of-year Code Word only—23 binary digits.
   a. Minutes, hours and days.
   b. Recycles yearly.

4. Code Word structure: BCD Word begins at Index Count 10. Binary coded Elements occur between Position Identifier Elements (7 for minutes; 6 for hours, 8 and 2 for days) until the Code Word is complete. An Index Marker occurs between decimal digits in each group to provide separation for visual resolution.

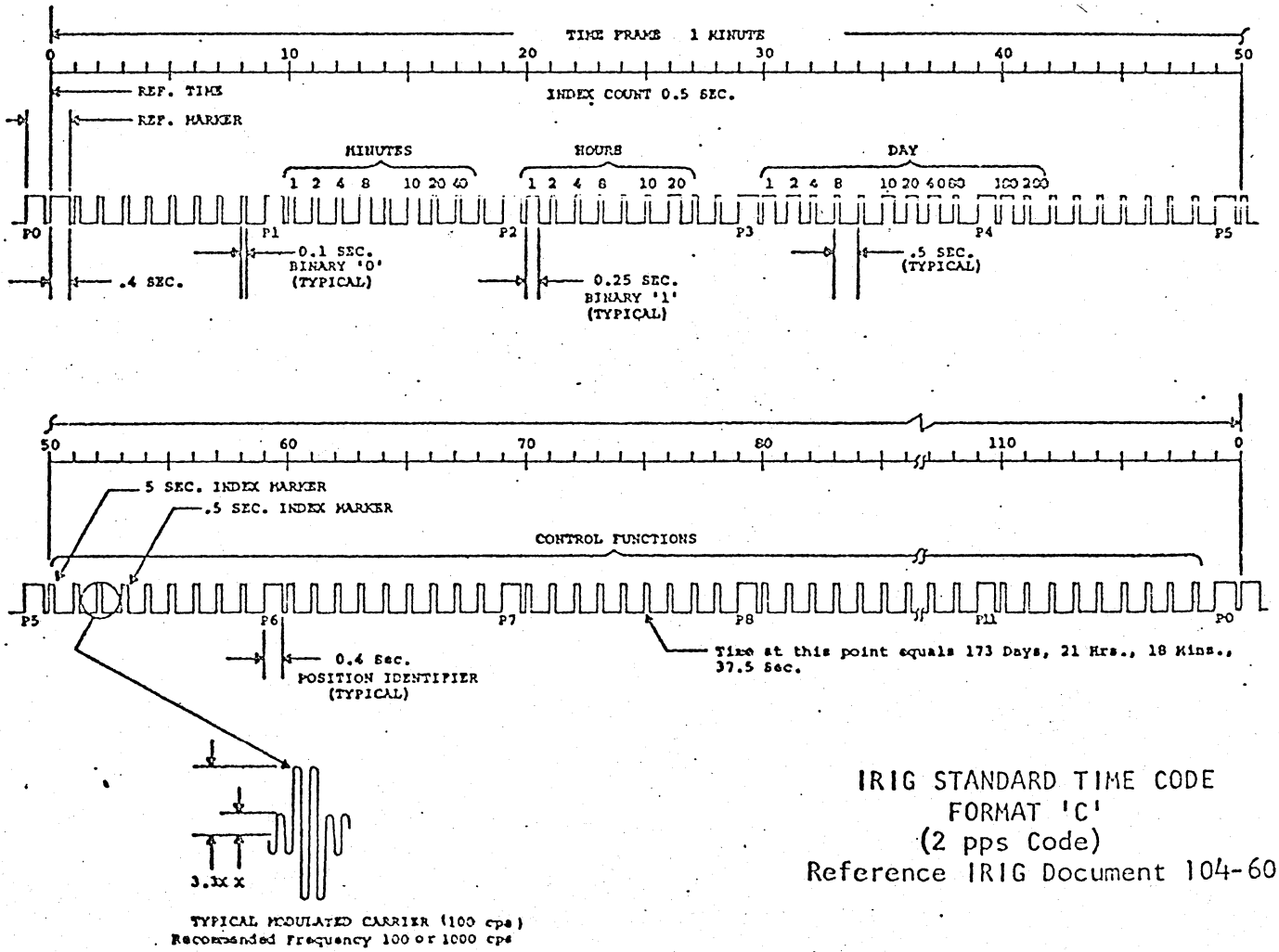
5. Least significant digit occurs first.

6. Element rates available:
   a. 2 per second (basic Element rate).
   b. 1 per 5 seconds.
   c. 1 per minute.

7. Element identification:
   a. "On time" reference point for all Elements is the leading edge.
   b. Index Marker ..... 0.1 seconds. (Binary zero or uncoded Element).
   c. Code Digit ..... 0.25 seconds. (Binary one).
   d. Position Identifier—1 per 5 seconds ..... 0.4 seconds. (Refers to the leading edge of the succeeding Element).
   e. Reference Marker—1 per minute ..... Two consecutive Position Identifiers. (The "on time" point, to which the Code Word refers, is the leading edge of the second Position Identifier).

8. Resolution: 0.5 seconds (unmodulated).
   0.01 seconds (modulated 100 cps).
   0.001 seconds (modulated 1000 cps).

9. Carrier frequency: 100 or 1000 cycles when modulated.



IRIG STANDARD TIME CODE
FORMAT 'C'
(2 pps Code)
Reference IRIG Document 104-60

Figure 1-3. IRIG Time Code, Format "C"

IRIG FORMAT E:

1. Time: Universal Time (UT-2).

2. Time Frame: 10 seconds.

3. Code Digit Weighting: BCD time-of-year Code Word — 26 Binary digits.

   a. Seconds, minutes, hours and days.

   b. Recycles yearly.

4. Code Word structure:

   BCD Word begins at Index Count 6. Binary coded Elements occur between Position Identifier Elements (3 for seconds, 7 for minutes; 6 for hours; 8 and 2 for days) until the Code Word is complete. An Index Marker occurs between decimal digits in each group to provide separation for visual resolution.

5. Least significant digit occurs first.

6. Element rates available:

   a. 10 per second (basic Element rate).
   b. 1 per second.
   c. 0.1 per second.

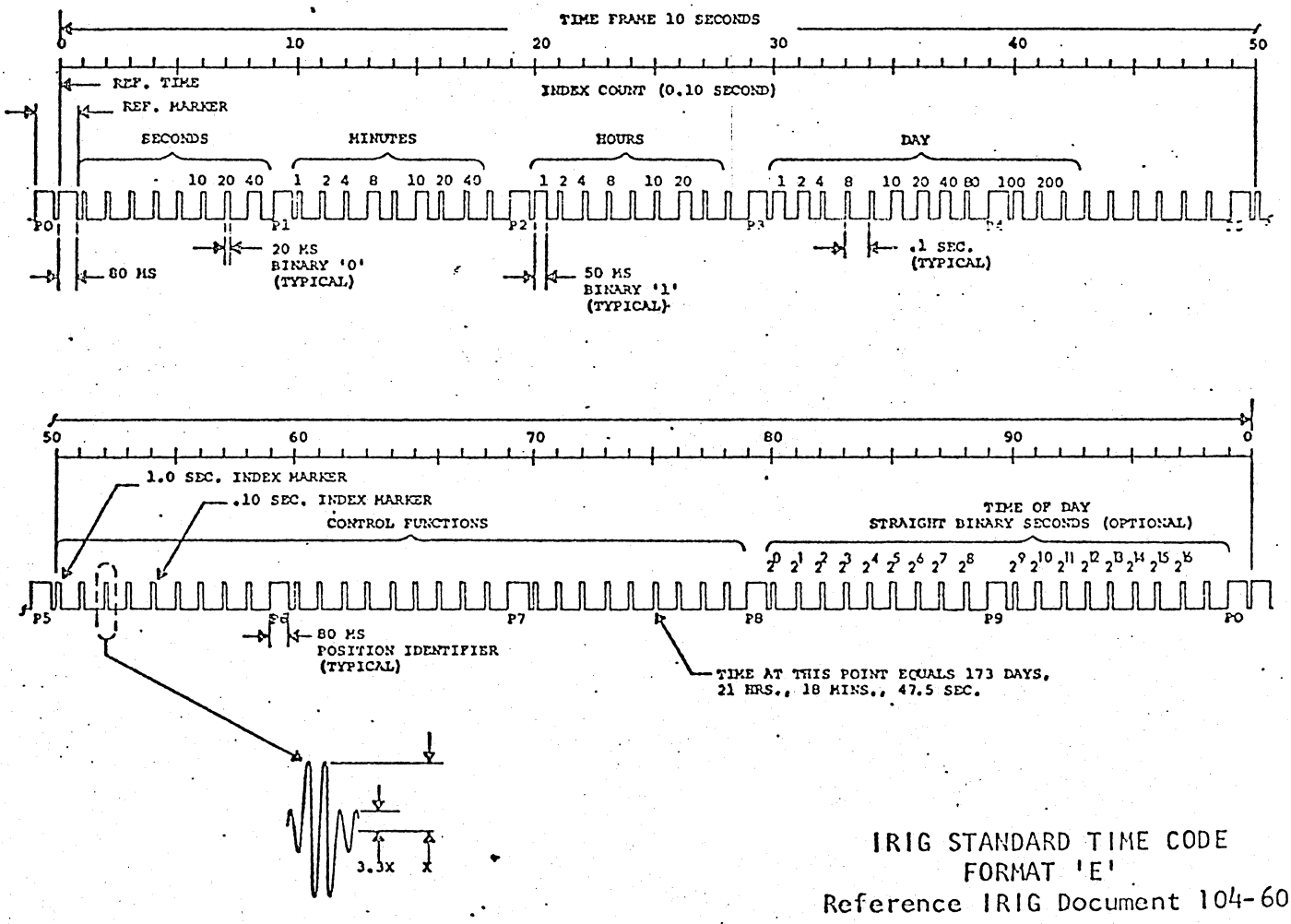
7. Element identification:

   a. "On time" reference point for all Elements is the leading edge.
   b. Index Marker ..... 20 milliseconds. (Binary zero or uncoded Element).
   c. Code Digit ..... 50 milliseconds. (Binary one).
   d. Position Identifier—1 per second ..... 80 milliseconds. (Refers to the leading edge of the succeeding Element).
   e. Reference Marker—1 per 10 seconds ..... Two consecutive Position Identifiers.

   (The "on time" point, to which the Code Word refers, is the leading edge of the second Position Identifier).

8. Resolution: 100 milliseconds (unmodulated).
   1 millisecond (modulated).

9. Carrier frequency: 1 kc. when modulated.



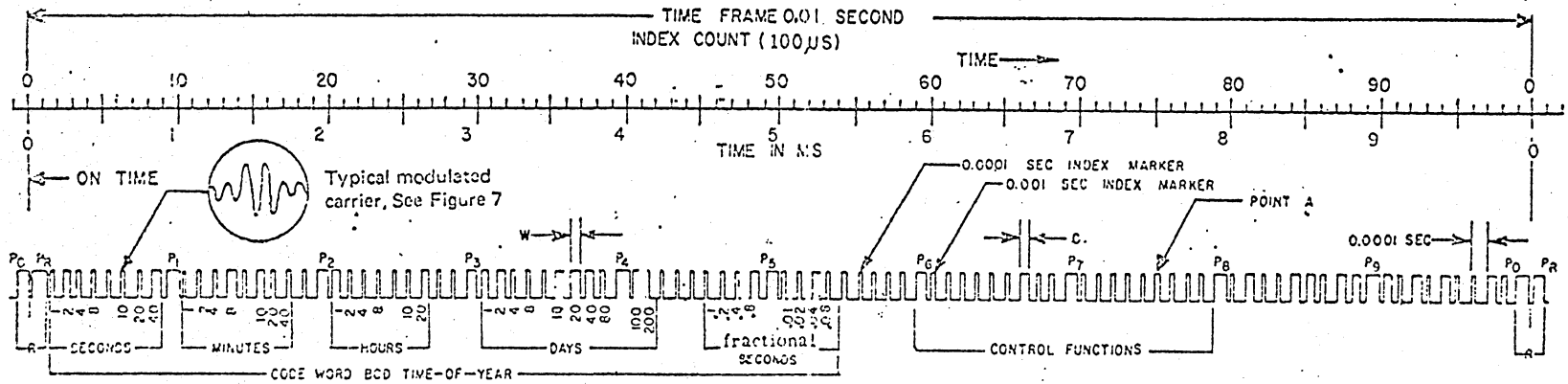
IRIG STANDARD TIME CODE
FORMAT 'E'
Reference IRIG Document 104-60

Figure 1-4. IRIG Time Code, Format "D"

General:

Format G, Signal G001, is composed of the following:

1) 100 pps frame reference markers R=(P_0 and P_R)
2) Binary coded decimal time-of-year code word (38 digits)
3) Control functions (18 digits)
4) 1000 pps position identifiers (P_0 through P_9)
5) 10000 pps index markers.



R REFERENCE MARKER (THE "ON TIME" POINT TO WHICH THE CODE WORDS REFER, IS THE LEADING EDGE OF P_R)
P_R REFERENCE ELEMENT (0.08 MS DURATION)
P_0 - P_9 POSITION IDENTIFIERS (0.08 MS DURATION)
W WEIGHTED CODE DIGIT (0.05 MS DURATION)
C WEIGHTED CONTROL ELEMENT (0.05 MS DURATION)
DURATION OF INDEX MARKERS, UNWEIGHTED CODE & CONTROL ELEMENTS=0.02MS

TIME AT POINT A= 21:18:42+0.8+0.04+0.0075
21 HOUR 18 MINUTE 42.8475 SECOND ON DAY 173

Specific

The beginning of each 0.01 second time frame is identified by two consecutive 0.08 ms elements (P_0 and P_R). The leading edge of the second 0.08 ms element (P_R) is the "on time" reference point for the succeeding time code. 1000 pps position identifiers P_0, P_1.....P_9 (0.08 ms duration) occur 0.1 ms before 1000 pps "on time" and refer to the leading edge of the succeeding element.

The time code word and the control functions presented during the time frame are pulse width coded. The binary "zero" and index markers have a duration of 0.02 ms, and the binary "one" has a duration of 0.05 ms. The leading edge is the 10K pps "on time" reference point for all elements.

The binary coded decimal (BCD) time-of-year code word consists of 38 digits beginning at index count 1. The binary coded subword elements occur between position identifiers P_0 and P_6, (7 for seconds; 7 for minutes; 6 for hours; 10 for days; 4 for tenths of seconds; 4 for hundredths of seconds) until the code word is complete. An index marker occurs between the decimal digits in each subword to provide separation for visual resolution. The least significant digit occurs first except for the fractional second information which follows the day-of-year information. The BCD code recycles yearly. Each BCD element is identified on the BCD Time-Of-Year Code Chart.

Eighteen control functions occur between position identifiers P_6 and P_8. Any control function element or combination of control function elements can be programmed to read a binary "one" during any specified number of time frames. Each control element is identified on the Control Function Chart.

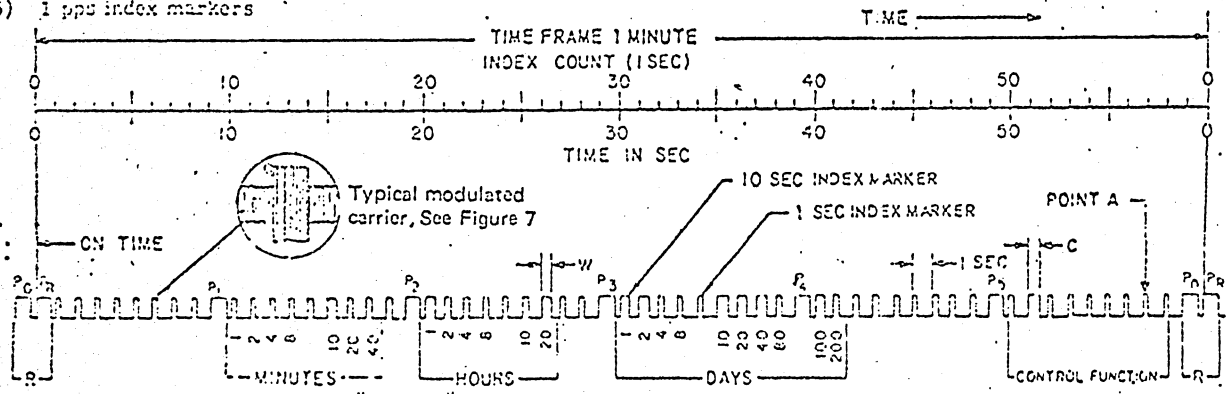
Format G, Signal G001

Figure 1-5. IRIG Time Code, Format "G"

General:

Format H, Signal H001, is composed of the following:

1) 1 ppm frame reference markers R=(P_0 and P_R)
2) Binary coded decimal time-of-year code word (23 digits)
3) Control functions (9 digits)
4) 6ppm position identifiers (P_0 through P_5)
5) 1 pps index markers



R REFERENCE MARKER (THE "ON TIME" POINT TO WHICH THE CODE WORD REFERS IS THE LEADING EDGE OF P_R)

P_R REFERENCE ELEMENT (0.8 SEC DURATION)

P_0-P_5 POSITION IDENTIFIERS (0.8 SEC DURATION)

W WEIGHTED CODE DIGIT (0.5 SEC DURATION)

C WEIGHTED CONTROL ELEMENT (0.5 SEC DURATION)

DURATION OF INDEX MARKERS UNWEIGHTED CODE AND CONTROL ELEMENTS = 0.2 SEC

TIME AT POINT A= 21:10:57
= 21 HOUR + 10 MINUTE + 57 SECOND ON DAY 173

Specific

The beginning of each 1 minute time frame is identified by two consecutive 0.8 second elements (P_0 and P_R). The leading edge of the second 0.8 second element (P_R) is the "on time" reference point for the succeeding time code. 6 ppm position identifiers P_0, P_1.....P_5 (0.8 second duration) occur 1 second before 6 ppm "on time" and refer to the leading edge of the succeeding element.

The time code word and the control functions presented during the time frame are pulse width coded. The binary "zero" and the index markers have a duration of 0.2 second, and the binary "one" has a duration of 0.5 second. The leading edge is the 1 pps "on time" reference point for all elements.

The binary coded decimal (BCD) time-of-year code consists of 23 binary digits beginning at index count 10. The binary coded subword elements occur between position identifiers P_0 and P_5 (7 for minutes; 6 for hours; 10 for days) until the code word is complete. An index marker occurs between the decimal digits in each subword to provide separation for visual resolution. The least significant digit occurs first. The BCD code recycles yearly. Each BCD element is identified on the BCD Time-Of-Year Code Chart.

Nine control functions occur between position identifiers P_5 and P_0. Any control function element or combination of control function elements can be programmed to read a binary "one" during any specified number of time frames. Each control function is identified on the Control Function Chart.

Format H, Signal H001

Figure 1-6. IRIG Time Code, Format "H"

CHAPTER TWO

INSTALLATION

2.1 INTRODUCTION

This chapter provides an installation procedure for the Model 9210 Time Code Translator.

2.2 INSTALLATION PROCEDURE

Upon receiving the 9210 make a thorough inspection of the instrument and its accessories. Any damage or loss of equipment should be reported immediately to the responsible carrier, If no damage is found, install the 9210 as outlined in the following steps.

a. Using appropriate hardware, install the 9210 in standard 19-inch rack or cabinet at the desired location.

NOTE

Approximately 20 inches of free space in front of the rack or cabinet is required for installation (and removal) of the 9210. After installation, a minimum of six inches of free space must be maintained to allow the 9210 to slide out of the rack or cabinet for access to the subpanel controls.

b. Ensure that the POWER toggle switch is in the OFF position. Connect primary power source to power input connector on rear of 9210 power supply.

c. Make appropriate connections to 9210 input/output connectors.

NOTE

Input/Output cable assemblies are not supplied and must, therefore, be fabricated using the connector plugs supplied with the 9210. Refer to the top assembly drawing in Appendix A for connector J-numbers and pin assignments.

(1) Connect IRIG A, B, C, E, G, or H carrier modulated code to the input connector.

(2) If 9210 is to be used in conjunction with a Tape Search Control Unit, connect tape search output connector to the Tape Search Control Unit with the cable provided.

(3) Connect all optional input/output cables to rear panel.

d. The unit is now ready for operation.

CHAPTER THREE

OPERATION

3.1 INTRODUCTION

This chapter contains a list of the Model 9210 Time Code Translator front panel and control panel controls and indicators together with a short description of their function. In most cases, the operating procedure for a switch or the interpretation of an indicator reading is included as part of the switch or indicator description. General procedures required to operate and adjust the 9210 are also included in this chapter. Special procedures applicable to a specific model, when required, are inserted in Appendix A.

The names of the front panel and control panel controls and indicators are capitalized and underlined in the text. They are spelled exactly as they appear on the unit. Control position and indicator states are capitalized only. For example, "Set the POWER switch to the ON position".

3.2 CONTROLS AND INDICATORS

Except where otherwise indicated, all 9210 operating controls and status indicators are located on the front panel or on the control panel. The purpose and function of these controls and indicators are described in the following paragraphs. The controls and indicators are illustrated on the top assembly diagram included in Appendix A.

3.3 CONTROLS

a. POWER Switch. The POWER switch controls all sections of the unit. All logic is operational when the POWER switch is set to the ON position. All voltages are removed when the POWER switch is in the OFF position.

b. MODE Control. The MODE rotary switch selects the number of frames to be by-passed before the unit is synchronized to the input code.

The 9210 is controlled by an input time code signal. In some units, FRAME BYPASS control settings are used to select the number of time frames containing non-consecutive time data that will be accepted before the counters will be corrected to agree with the input time data. Noise on the input signal can cause the translator to read erroneous data. To detect this data, advantage is taken of the fact that time code data is sequential, i.e., updated in each frame by the length of time required per frame. Therefore, any change in sequence may be regarded as an error. The capability to select the number of error frames that will be accepted before the counters update provides a means of compensating for these errors in normal forward operation, while retaining the ability to respond to input time-code changes. In general, FRAME BYPASS control positions should be selected according to input signal reliability. For extremely poor quality signals, choosing higher by-pass positions prevents needless updating and restores the original continuity to the time code. When the input signal is relatively error-free, choosing a lower rate decreases the response time for valid changes in continuity should these occur.

The rotary control may also be set to select 00. In this mode, the counters are not updated by the input time code. The 9210 utilizes the carrier of the input

signal as a time base, and generates all outputs by dividing the carrier frequency.

c. Polarity Switch. The POL switch is set to indicate the polarity of the input time code carrier. Amplitude-modulated time code signals change amplitude to indicate a mark precisely as the carrier signal crosses its zero-voltage axis. Positive (+) polarity is defined as a positive-going zero-axis crossing at the on-time edge of a mark pulse. Negative (-) polarity is defined as a negative-going zero-axis crossing at this edge. If it is unknown, the polarity of the time code signal can be determined by examination with an oscilloscope.

d. FWD/REV Switch. The FWD/REV switch is set to indicate the time-code "direction". In normal operation, where the time indicated by the code increments in successive frames, this control is set to the FWD position. In this mode the leading edge of the time code index markers are on time and the FRAME BYPASS circuitry is operational. For reverse operation where the time indicated by the input time code decrements in successive frames, this control must be set to the REV position.

NOTE

If the 9210 is used in conjunction with a Tape Search and Control Unit the FWD/REV switch is disabled when connection is made.

e. INPUT CODE Selector Switch. The INPUT CODE switch selects up to nine input code formats. The following table indicates the input code format corresponding to each position of the switch.

POSITION	CODE FORMATS
1	IRIG G - 100 kHz carrier
2	IRIG A - 10 kHz carrier
3	IRIG B - 1 kHz carrier
4	IRIG C - 100 Hz carrier
5	IRIG C - 1 kHz carrier
6	IRIG E - 100 Hz carrier
7	IRIG E - 1 kHz carrier
8	IRIG H - 100 Hz carrier
9	IRIG H - 1 kHz carrier

f. FILTERS Selector Switches. The two FILTERS selection switches, PLAYBACK and SEARCH, are identical.

As indicated by their titles, these selectors are intended for use in tape search operations when the 9210 is operated in conjunction with a tape search unit. Each control selects the center frequency for an optimally flat, Butterworth response filter, with a roll-off of 24 db per octave and a bandwidth of from f/3 to 1.5f. Two controls are provided because playback and search of a tape are usually done at normal and high speed, respectively, and different filter center frequencies must be selected during each phase of the operation. The PLAYBACK or SEARCH filter is selected automatically

by a control signal from the tape search unit. When the 9210 is operated without a tape search unit, only the PLAYBACK filters are operative.

Each control consists of a dual concentric rotary switch. The inner switch ring (decade multiplier) selects a basic center frequency, and the outer switch ring (binary multiplier) selects a factor by which this frequency is multiplied to determine the actual filter center frequency. The NORM setting of the decade multiplier selects "straight through" operation; there is no filtering other than normal amplifier "roll-off". The X1 setting of the decade multiplier establishes a basic center frequency of 1 kHz. The center frequencies that can be selected are shown by Table 3-1.

The filters are addressed by terms from the FILTERS controls. The decade multiplier address terms are designated U1 and U2; the binary multiplier address terms are V1, V2, V4, and V8. Remote filter addressing may be provided as an option. In this case, the same addressing scheme is used. Table 3-2 shows the filter address code.

BINARY MULTIPLIER	DECADE MULTIPLIER		
	X.1	X1	X10
1/128	-	-	78 Hz
1/64	-	15.6 Hz	156 Hz
1/32	-	31.2 Hz	312 Hz
1/16	-	62.5 Hz	625 Hz
1/8	12.5 Hz	125 Hz	1.25 kHz
1/4	25 Hz	250 Hz	2.5 kHz
1/2	50 Hz	500 Hz	5 kHz
1	100 Hz	1 kHz	10 kHz
2	200 Hz	2 kHz	20 kHz
4	400 Hz	4 kHz	40 kHz
8	800 Hz	8 kHz	80 kHz
16	1.6 kHz	16 kHz	.16 MHz
32	3.2 kHz	32 kHz	.32 MHz
64	6.4 kHz	64 kHz	.64 MHz
128	12.8 kHz	128 kHz	1.28 MHz
256	25.6 kHz	256 kHz	2.56 MHz

Table 3-1. Playback and Search Filter Center Frequencies

U_2	U_1	MULT.
0	0	0.1
0	1	1
1	0	10
1	1	NORM

DECADE MULTIPLIER

V_1	V_2	V_4	V_8	MULT.
0	0	0	0	1/128
0	0	0	1	1/64
0	0	1	0	1/32
0	0	1	1	1/16
0	1	0	0	1/8
0	1	0	1	1/4
0	1	1	0	1/2
0	1	1	1	1
1	0	0	0	2
1	0	0	1	4
1	0	1	0	8
1	0	1	1	16
1	1	0	0	32
1	1	0	1	64
1	1	1	0	128
1	1	1	1	256

BINARY MULTIPLIER

Reference Frequency: 1 kHz

Logic Levels: 0 = -15V
1 = Open

Table 3-2. Filter Addresses

g. FAILSAFE Switch (Optional). Located on internal control panel behind the front panel. In the IN position, the 9210 uses a VCO as the unit's clock. Operation of the 9210 is dependent on the filter switch setting. (See Operating Procedures and under Control and Indicators see FILTERS Switch.) In the OUT position, the 9210 operates normally using the code carrier as its time base.

h. DC Code (Optional). Located on internal control panel behind the front panel. When the 9210 is operated in this mode, it accepts the DC code envelopes for an input code. This mode depends upon the filter selector switch setting for operation (see Operating Procedures and Specifications).

NOTE

This switch is a three (3) position rotary switch which selects the following:
AC - Selects normal operation
DC - Selects DC code operation
AC Failsafe - Selects failsafe operation

3.4 INDICATORS

(1) SYNC ERROR. Indicates a synchronization error. This indicator turns off when synchronization has been verified. This indicator is not functional in the reverse mode.

(2) LOSS OF SIGNAL. Indicates that the input code has dropped below the preset input threshold detector level.

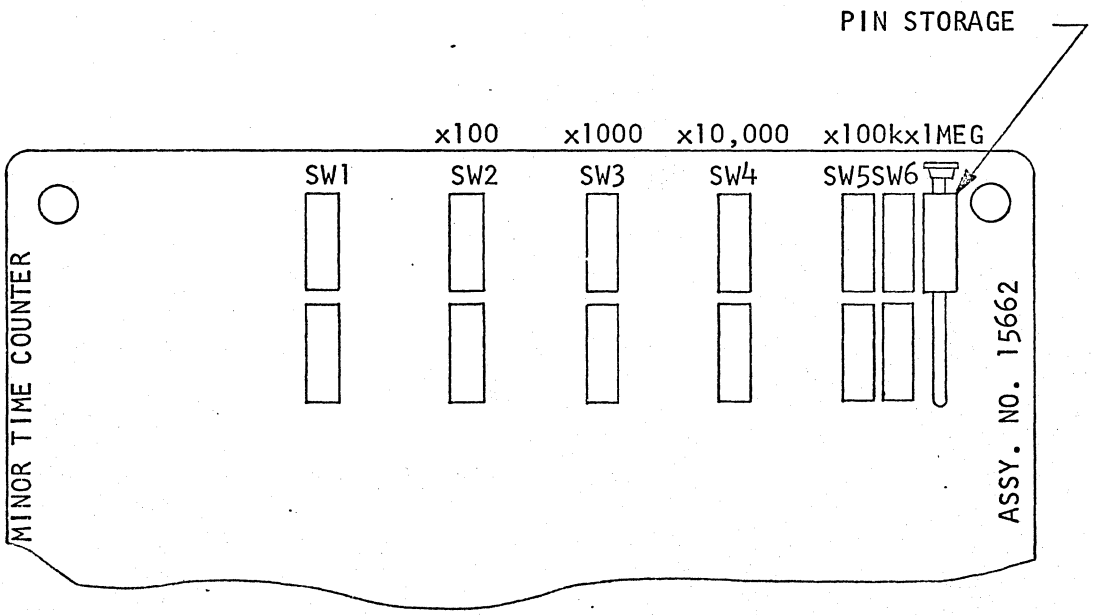
3.5 PROGRAMMING CONTROL POINTS

The following functions are controlled by pin switches located on the card assemblies.

a. Minor Time Counter Clock Speed-Up Control (Assembly No. 15662). These control points are included for maintenance purposes only and are designed to be used as an aid for testing slow codes and pulse rates. These control points are located on Assembly 15662.

Switch 1	Pin In	Speeds up counter x 10
Switch 2	Pin In	Speeds up counter x 100
Switch 3	Pin In	Speeds up counter x 1000
Switch 4	Pin In	Speeds up counter x 10,000
Switch 5	Pin In	Speeds up counter x 100,000
Switch 6	Pin In	Speeds up counter x 1,000,000

Store pin in yellow storage position marked PIN for normal operation.

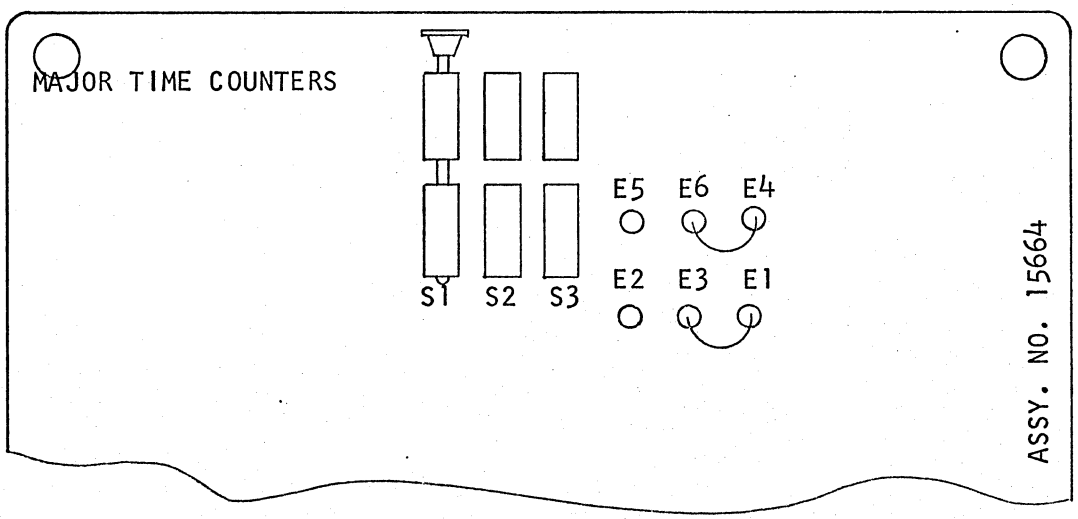


b. Major Time Counter Radix Control (Assembly 15664).

(1) Mode A: Calendar Year (The 9210 is normally shipped in this configuration.)

Jumpers must be soldered from E4 to E6 and from E1 to E2 on front of board. See Figure below.

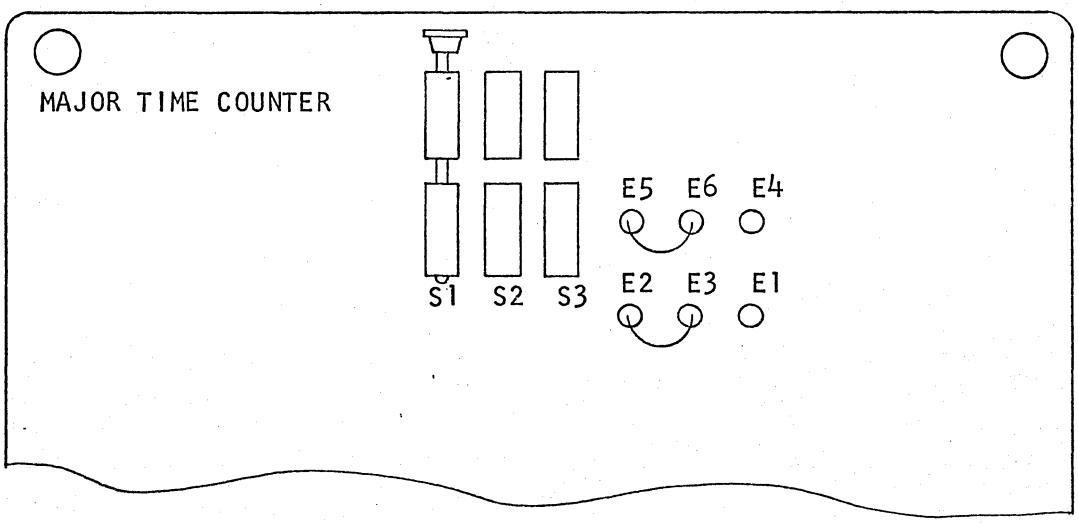
(a)	Switch 1	Pin In Normal Year	Counter will automatically radix to day 1 one second after 365 days, 23 hours, 59 minutes, 59 seconds count.
(b)	Switch 2	Pin In Leap Year	Counter will automatically radix to day 1 one second after 366 days, 23 hours, 59 minutes, 59 seconds count.
(c)	Switch 3	Pin In ID	Counter will automatically radix to day 0 one second after 999 days, 23 hours, 59 minutes, 59 seconds count.



(2) Mode B: Elapsed Time Year

Jumpers must be soldered from E4 to E5 and from E1 to E3 on front of board. See Figure below.

(a)	Switch 1	Pin In Leap Year	Counter will automatically radix to day 0 one second after 365 days, 23 hours, 59 minutes, 59 seconds count.
(b)	Switch 2	Pin In Normal Year	Counter will automatically radix to day 0 one second after 999 days, 23 hours, 59 minutes, 59 seconds count.



c. DC Code Input Polarity Switch (Optional - See Top Assembly Drawing.)

SW-2

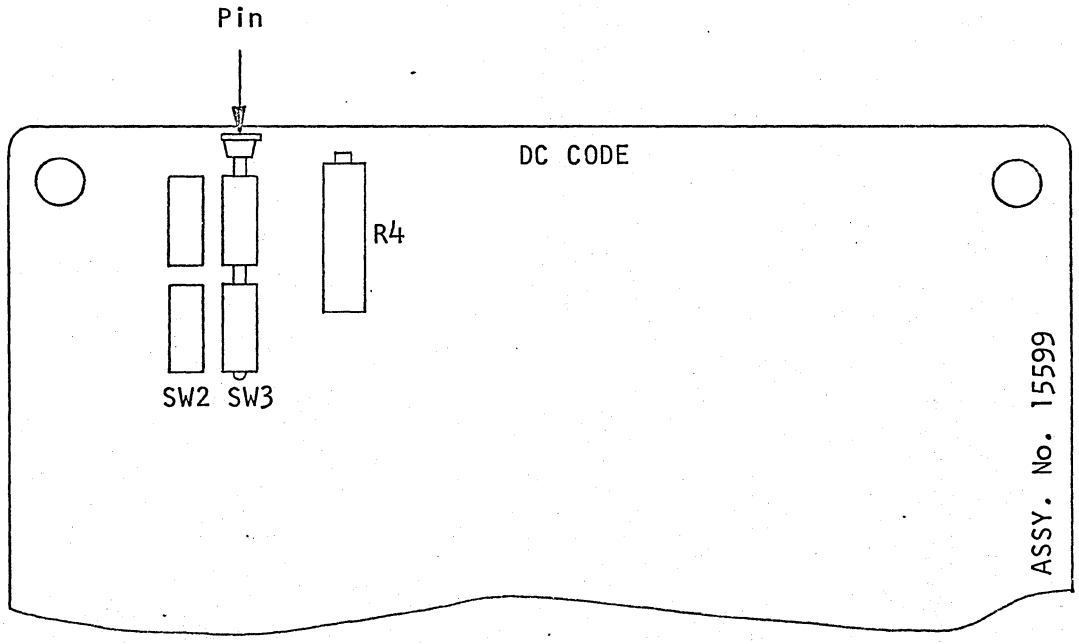
When a pin is installed in the SW-2 position, the 9210 will accept a DC input code of 0V to NEG (-) voltage.

SW-3

When a pin is installed in the SW-3 position, the 9210 will accept a DC input code of 0V to a POS(+) voltage.

R4

Used to set operating point of input shaper. (Refer to paragraph 3.9b for adjustment procedure.)



d. Minor Time Synchronization (Assembly 15675)

(1) SW1 and SW2 selects either every frame of synchronization or selected frames to be by-passed.

(a) SW1 IN

The minor time counter will be synchronized only after the selected number of frames has been counted.

(b) SW2 IN

The minor time counter will be synchronized every time frame.

3.6 OPERATING PROCEDURES

This section contains operating procedures for the 9210. Set-up programming control points described in paragraph 3.5 for desired unit operating configuration before performing these procedures.

3.7 POWER ON/OFF

a. To activate the unit, set the POWER switch, located on the front panel to the ON position.

b. To remove power from the unit, set the POWER switch to the OFF position.

3.8 TRANSLATOR MODE

(Refer to top assembly drawing for J numbers of input and output connectors.)

a. Set the MODE switch to TRANSLATE or any one of the FRAME BYPASS positions. (Do not use the 00 FRAME BYPASS position as this disables the synchronization circuits.)

b. If the input code modulation is phased such that the first half cycle of the mark amplitude pulse is positive-going, place the polarity switch in the positive (+) position. If the first half cycle of the mark pulse on the input code is negative-going, place the polarity switch to the negative (-) position.

c. If the 9210 is NOT used in conjunction with a Tape Search Control Unit and the input code is coming in in the forward direction, place the FWD/REV switch to FWD. If the code is coming in in reverse direction, place the FWD/REV switch to REV.

d. Select the proper input code position using the following table.

Position 1	IRIG G	100 kHz carrier
Position 2	IRIG A	10 kHz carrier
Position 3	IRIG B	1 kHz carrier
Position 4	IRIG C	100 Hz carrier
Position 5	IRIG C	1 kHz carrier
Position 6	IRIG E	100 Hz carrier
Position 7	IRIG E	1 kHz carrier
Position 8	IRIG H	100 Hz carrier
Position 9	IRIG H	1 kHz carrier

e. Select the proper playback filter. (Refer to Controls and Indicators for details of filter frequency selection.)

Example: If IRIG B is used as the input code and it is being played back on a 1 to 1 ratio, select a 1 kHz filter. To do this, set the base frequency selector (large outer knob) to 1, and set the filter multiplier (small inner knob) to the X1 position. This selects a playback filter of 1 kHz.

f. To set the high speed search filters, select the search filter frequency in a similar manner. First determine the desired frequency by multiplying the 1 to 1 base frequency of the input code by the speed-up factor of the search speed.

Example: The input code is IRIG B 1 kHz carrier frequency to be searched at a speed-up ratio of 64 times normal. The search filter must then be set to 64 kHz. (Search filter frequency = Code base frequency x search speed-up ratio.) Therefore, set the base frequency selector switch (large outer knob) to 64 and set the filter multiplier (small inner knob) to the X1 position.

3.9 OPTIONAL TRANSLATE MODES (See top assembly drawing).

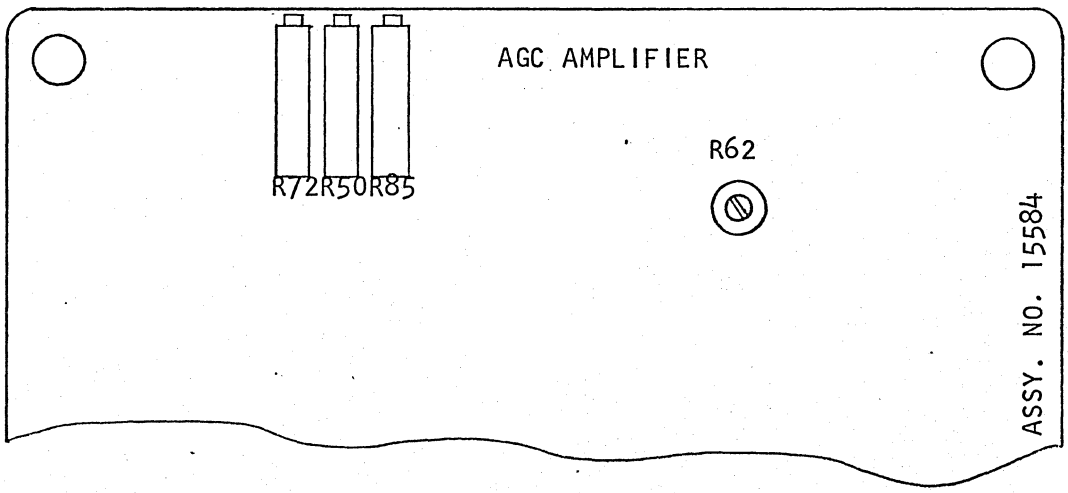
a. (AC) FAILSAFE (located on subpanel behind front panel).

(1) In AC FAILSAFE operation, a voltage controlled oscillator (VCO) is used as the timebase of the 9210. The frequency of the VCO is determined by the filter switches and must be selected in a similar fashion as the filter frequency selection was. Therefore, refer to the playback and search

filter operating procedure Paragraph 3.8. Also refer to the Controls and Indicators Section on the input FILTERS switch.

(2) AC FAILSAFE Threshold Adjustment (located on the AGC Card Assembly 15584). The input threshold adjustment range is approximately 250 mv to 5 v referred to the input code. If the input code amplitude is below the preset value of the threshold potentiometer, all synchronization controls in the 9210 are locked out. Two methods of adjusting the threshold are as follows:

METHOD ONE: With a normal input code between 250 mv and 5 volts, adjust pot R85 in a clockwise direction until the TRANSLATOR STATUS, LOSS OF SIGNAL lamp turns on. Then turn the threshold pot R85 counterclockwise until the LOSS OF SIGNAL lamp goes off and does not flicker. Remove the input code and the LOSS OF SIGNAL lamp should come on again.



METHOD TWO: This method requires an oscilloscope to monitor the input signal, and it requires that the input signal level be adjustable. With this method, the input low level threshold can be set to a known value. Set the input code amplitude to the desired low threshold level and then adjust R85 on Assembly 15584 so that the LOSS OF SIGNAL lamp flickers on and off. Where the input code amplitude is lowered below this level, the LOSS OF SIGNAL lamp should be on continuously and conversely, when the input code is raised above the threshold level, the LOSS OF SIGNAL lamp should extinguish.

NOTE

When operating in the AC FAILSAFE mode, the MODE switch should be operated in the 4, 8, or 16 FRAME BYPASS positions in order to allow resynchronization of the decoder without disrupting the outputs of the 9210 as the input code transverses above and below the preset threshold.

b. DC CODE (Optional)

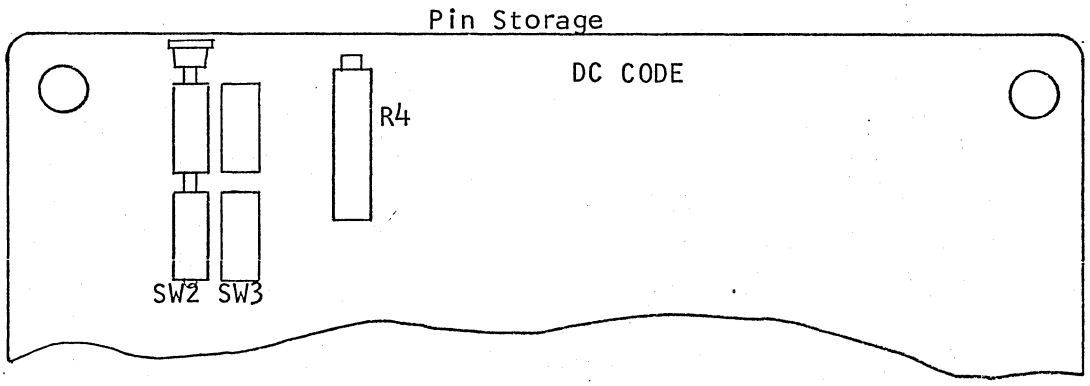
(1) Connect a DC shift code to the input connector. (See Top Assembly Drawing).

(2) Set selector switch to DC CODE.

(3) In order to translate a DC Code signal, the operator must know the normal carrier frequency of the DC Code being used, select that carrier frequency on the FILTERS PLAYBACK switch, and set the search multiple of that frequency on the FILTERS SEARCH switch. (Refer to Translator Operating Procedure Paragraph 3.10. Also refer to the Controls and Indicators section on the FILTERS switch.)

(4) Set all front panel switches as in Paragraph 3.8.

(5) If the input code has a zero (0) volt baseline and goes to a positive voltage, place the switch selector pin on the DC Code Card Assembly 15599 to the SW3 position (see drawing in Controls and Indicators). If the input code has a zero (0) volt baseline and goes to a negative voltage, place the switch selector pin in the SW2 position on Assembly 15599.



(6) The front panel polarity switch should be in the positive (+) position when the baseline of the input code is zero volts. When the baseline of the input DC code is either a positive voltage or a negative voltage, the front panel polarity switch should be placed in the negative (-) position.

(7) Threshold Potentiometer. With all other switches properly set and a DC input code applied, adjust R4 on Assy. 15599 for a normal time indication on the front panel NIXIE display. If using a scope, observe TP-1 of Assy. 15599 for the reconstructed DC code envelope as R4 is adjusted.

CHAPTER FOUR

THEORY OF OPERATION

4.1 INTRODUCTION

This chapter describes the functional operations of the basic circuits group of the Model 9210 Time Code Translator. Changes to or special features added to the basic unit are described in Appendix A. Also included in this appendix are the functional descriptions for the option circuits group. These descriptions include information about pulse rate signal outputs, parallel time code outputs, serial time code outputs and other customer-selected options. Terms used on drawings are defined in Chapter 7. All drawings for the basic unit are included in Chapter 7. Special option drawings, including the unit top assembly diagram, are included in Appendix A.

The logic drawings and functional descriptions are arranged in circled number order as defined on the unit block diagram. Numeric reference designations are used to identify circuit groups on these logic diagrams. Circuit card types used are correlated to these reference designations with a table located by the logic diagram title block.

The actual physical location of each circuit card is listed on top assembly diagram. Space is provided on the logic diagram to insert the circuit card physical location next to the reference designation. This numbering method permits assignment of fixed reference designators on the logic diagrams without restricting the actual chassis slot location of a particular circuit card.

4.2 FUNCTIONAL DESCRIPTION

The basic Model 9210 Time Code Translator takes a serial time code input, reads or decodes the time code and supplies outputs in the desired forms.

Refer to the unit block diagram for the logic organization of the 9210. Circled numbers on the block diagram refer to logic term origin points. Reference to the logic diagram having the same circled number will expand that portion of the block diagram.

NOTE

Although the 9210 translates multiple codes, the decode process is similar, therefore, only the IRIG B decoder in the forward direction is considered in this chapter.

a. TRANSLATE Mode. The significant circuits for this mode (Figure 4-1) are:

(1) Input Amplifier -- Its function is to restore the input code signal and provide a constant amplitude signal to the decode and detection circuitry.

(2) Serial-to-Parallel Converter -- Its function is to detect digital data in the input format and assign it to storage in the Major Time Counter. This section also contains the necessary circuits to synchronize the frequency dividers.

(3) Frequency Dividers (pulse counter and register control) -- These counters divide the code carrier frequency. Once synchronized to the input time code by the decoding circuitry in the serial-to-parallel section, this counter provides the

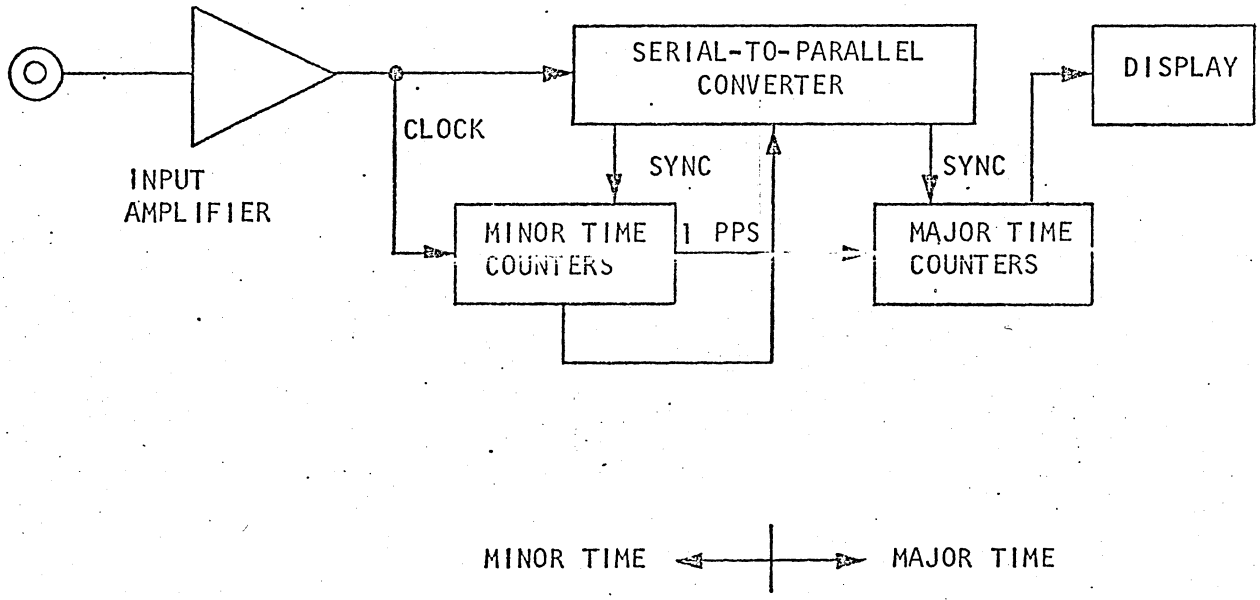


Figure 4-1. Translator, Simplified Block Diagram

terms necessary to index the digital data contained in the input code. It locates each code bit and assigns this code to its storage location in the Major Time Counter.

(4) Major Time Counter -- This section is a counter which stores the value being read from the input code. It is updated with a 1 pps output from the frequency dividers. The 1 pps signal is permuted to count in the format of the time code; usually seconds, minutes, hours, and days. Inclusion of days is optional. The accumulated count is the basis for most of the outputs supplied by the unit.

(5) Display -- This section takes the Major Time Counter data and provides a visual display of the accumulated time for the benefit of the user.

4.3 AGC AND FILTERS (1)

4.4 INPUT FILTERS AND AMPLIFIERS.

The input code amplitude is normalized to an amplitude of 1 V p-p over the input range by the preamplifier. The purpose of the preamplifier is to condition the input code to the proper level to be accepted by the input bandpass filters. Since the 9210 is primarily used as a tape search system, two sets of input filters are provided, one for the playback (normal) mode of operation and the second for the search (highspeed) mode of operation. The 3 db points

of the selected filter are f/3 and 1.5f with a slope of 12 db per octave. The output of the filter is then amplified by the main AGC amplifier whose purpose is to boost the amplitude of the input code to approximately 6 V p-p suitable to be used by the code stripper and zero-axis detector. This amplifier also extends the input range of the 9210 from 10 mv to 10 v p-p.

4.5 CODE STRIPPER.

The code stripper consists of an adjustable threshold detector designated as the mark detector. The threshold of the mark detector is an adjustable negative DC voltage. The absolute value of the threshold voltage is set to be greater than the most negative peak of the space amplitude of the carrier, but less than the negative peaks of the mark amplitude of the carrier as illustrated in Figure 4-3. Therefore, the mark detector produces one pulse ($\overline{MD}$) for each negative-going cycle of each mark pulse contained on the input time code.

4.6 ZERO-AXIS DETECTOR

The zero-axis detector has an adjustable reference set to trigger at the positive-going zero-axis crossing of each carrier cycle. The output of the zero-axis detector ($\overline{ZAD}$) is one pulse for every carrier cycle of the input code. The positive-going edge of the ZAD pulse is on-time with the positive axis crossing of the input code.

4.7 AC CODE AND FAILSAFE (4) (Optional, See Top Assembly)

In order to facilitate reliable translator operation on noisy tapes

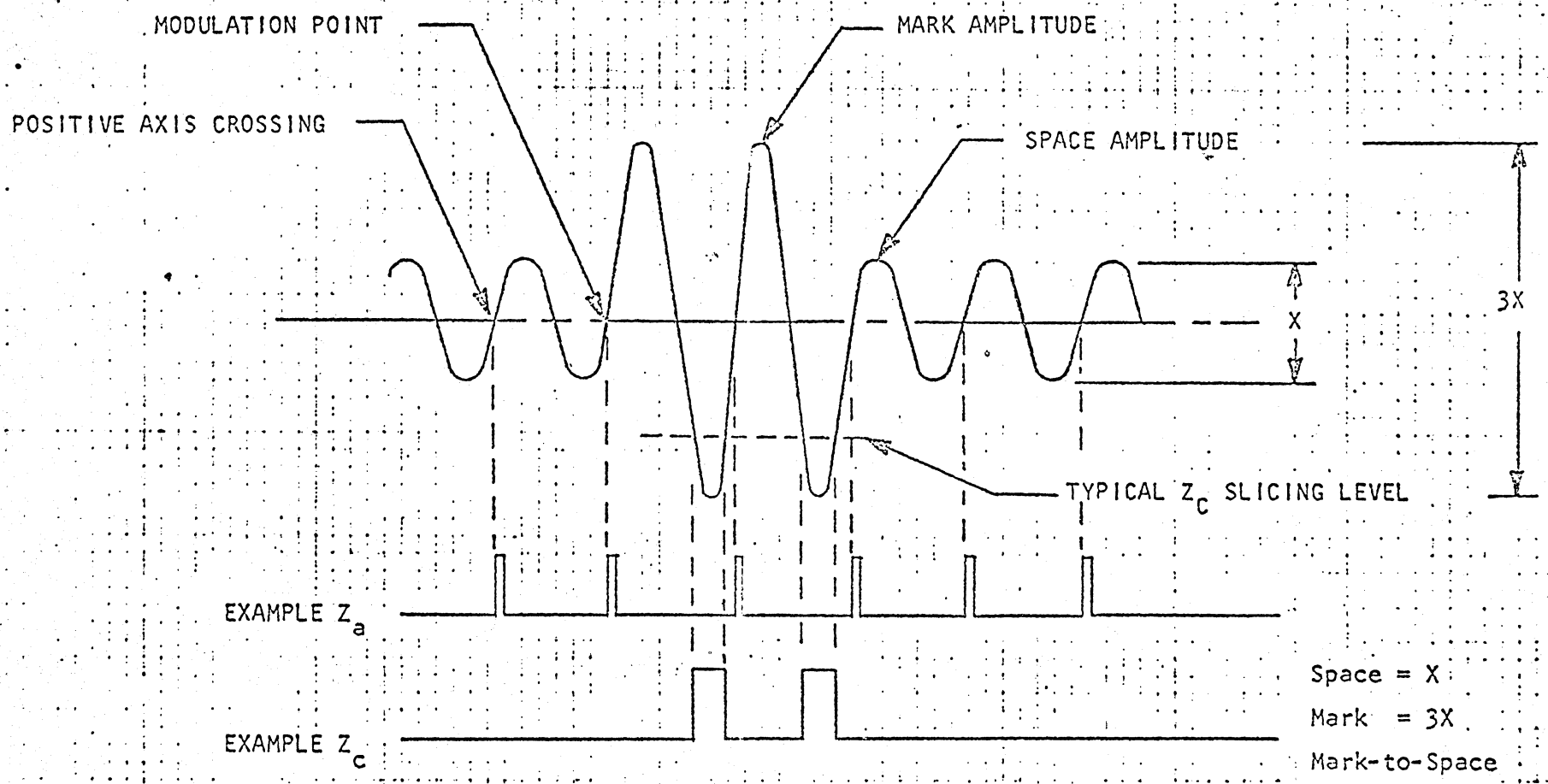


Figure 4-2. Typical Modulated Time Code, Timing Diagram

with intermittent drop outs on the time code, a failsafe option is provided. The failsafe option consists of a voltage controlled oscillator (VCO). The center frequency of the VCO is always 5.12 megacycle and then divided by N to provide a squarewave output equivalent in frequency to the input code carrier frequency. The frequency is automatically selected by the filter switches both in playback and in the search modes of operation.

The normal ZAD pulses received from the AGC and filter logic are compared against the output of the VCO for frequency differences. An error voltage is produced by the phase comparator that is proportional to frequency difference. It is used to correct the frequency of the VCO. The output of the VCO is then substituted in the translator for the original ZAD pulses. The VCO will flywheel through ZAD pulse drop outs.

When the input signal is lost, the AGC goes to a maximum position. Noise on the input could give erroneous ZAD pulses that could drive the VCO off frequency. To prevent this from happening, an adjustable threshold detector is provided. If the input code drops below the preset level of the threshold detector, all synchronization circuits or both the VCO and the 9210 translator are locked out.

NOTE

When operating in the FAILSAFE Mode, the MODE switch should be operated in the 4, 8, or 16 FRAME BYPASS positions in order to allow for resynchronization of the decoder without disrupting the outputs of the 9210 as the input code transverses above and below the preset threshold.

4.8 DC CODE AND FAILSAFE (4) (Optional, See Top Assy. Dwg.)

DC Code translation requires a VCO to synthesize the carrier frequency of the input code. Therefore, the failsafe option is always provided in conjunction with the DC Code option. (For failsafe operation, see Paragraph 4.7.) When used for DC code operation, the VCO is operated at the equivalent carrier frequency of the input code. For example, in IRIG B the output frequency of the VCO at a 1:1 playback ratio would be 1 KC. The input DC Code is converted to TTL compatible levels and the leading edge of each pulse is used as a reference to lock the VCO on frequency. The output of the VCO is then used for the ZAD pulses by the decoder. The code envelope is gated with the VCO output to produce synthesized ØC pulses (MD) to be used for mark detection in the decoder. As in AC failsafe, the filter switches are used to select the center frequency of the VCO. This is accomplished by selecting the equivalent carrier frequency of the input code on the filter switch.

4.9 INPUT AND DECODE LOGIC (2)

4.10 ENVELOPE DETECTOR

The input and decode logic receives the $\overline{MD}$ and $\overline{ZAD}$ pulses from the code stripper and zero axis detector. It utilizes these pulses in three decoder flip-flops (DF1, DF2, and DF3) to produce a DC envelope of the input time code (see Figure 4-4). The three decoder flip-flops are gated in such a way as to give the decoder single cycle noise immunity. Note that one cycle of the carrier during the mark pulse has dropped below the threshold of the mark detector. DF1 and DF2 reacted to this dropout. However, two cycles of the carrier must be below the threshold before DF3 reacts. In the same manner, two

cycles must be above the threshold during the space interval in order to cause DF3 to react.

The leading edge of DF3 is two carrier cycles (2 ms) late with respect to the input time code. This edge is used to produce a mark sync pulse ($\overline{MS}$). This pulse occurs at a 100 pps rate and is delayed by 2 ms in respect to the mark pulses on the IRIG B input code.

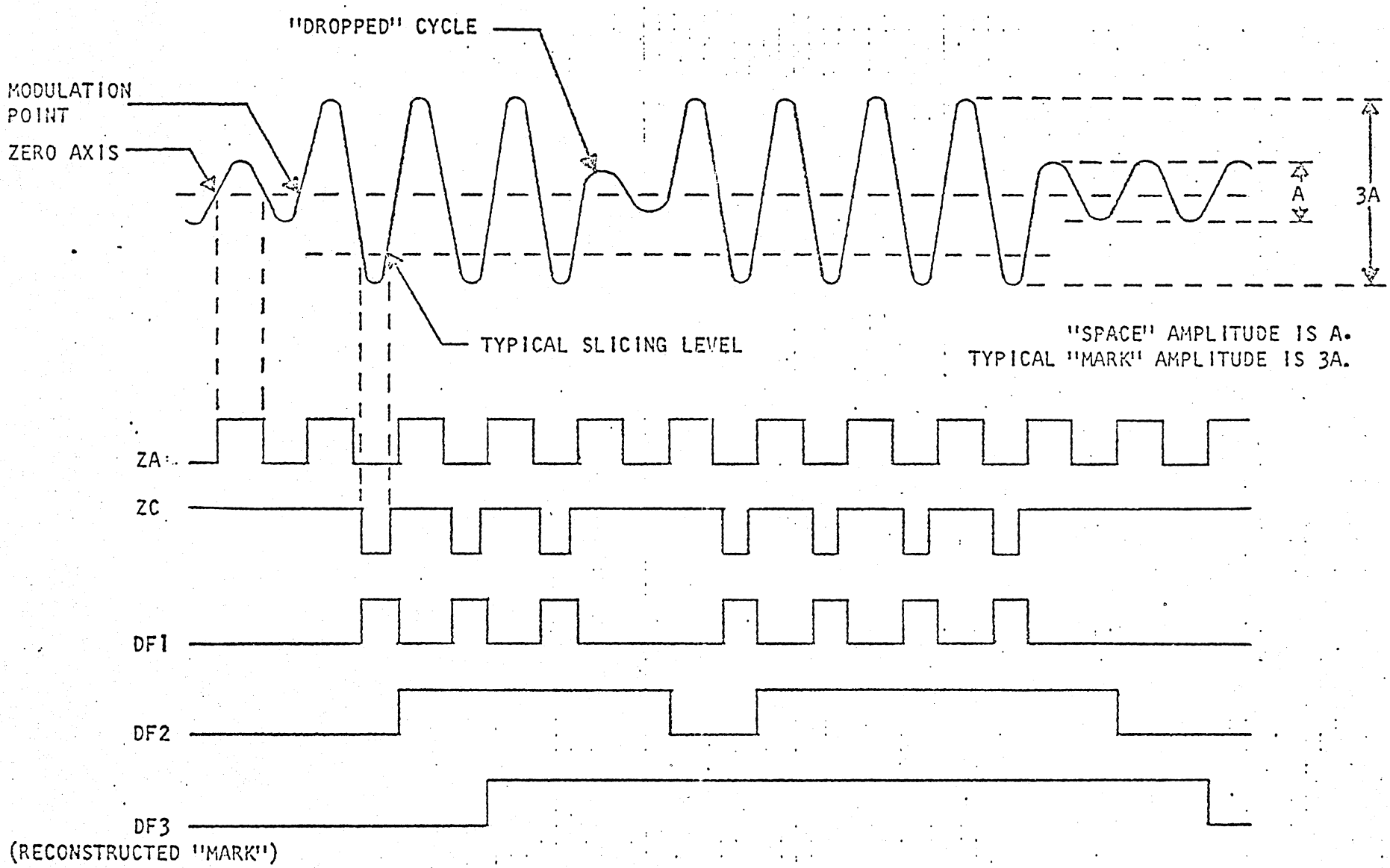


Figure 4-3. Envelope Detector, Timing Diagram

4.11 PULSE COUNTER AND REGISTER CONTROL (2)

The pulse counter consists of a group of four divide-by-ten counters (DCU's) that are synchronized with the incoming time code to produce "ON TIME" pulses that are ten times the pulse rate of the input code.

The pulse counter is synchronized with the mark pulses of the input time code by the mark sync pulse ($\overline{MS}$). $\overline{MS}$ is generated two carrier cycles late with respect to the input code mark amplitude pulses, therefore the first DCU is set to a count of two (2).

The frame sync pulse is generated by the DF4 flip-flop. The set enable of DF4 is true if DF3, which is the reconstructed input code DC envelope, is true during Z8 time. Z8 is a decode output of the pulse counter. The only time DF3 is in a true state at Z8 time is during a position identifier (8ms wide pulse) contained in the input code, referenced in Figure 4-5. Therefore, DF4 is set during each position identifier pulse and conversely if DF3 is in a false state at Z8 time, the reset enable for DF4 is true allowimg DF4 to be reset. Once during the IRIG B time frame, two consecutive position identifier pulses occur. This is at the start of each frame. DF4 will be true when the second set enable pulse occurs. This can happen only once per time frame. DF4 gated with the set enable DF4 term is used to generate the frame sync pulse (FS1). FS1 occurs once per frame and is delayed from the start of the time frame by 8.5 ms.

Terms SF1, SF2, SF4, and SF8 are outputs of a 4-bit shift register. In the translator mode the data input to this shift register is DF3 and the clock is Z5 which occurs during the interval between a binary '1' and a binary '0'. This, if DF3 is true at Z5 time, SF1 is set true and if DF3 is false at Z5 time, SF1 is set false. This

sets the state of DF3 into the 4-bit shift register. That is to say, if the code contains a binary '1' the shift register will contain a binary '1' for the same bit. This 4-bit shift register, therefore, will always contain 4 consecutive pulses of the same input serial time code to be presented in parallel form to the major time counter (reference Paragraph 4.25).

4.12 FWD/REV CONTROL (2)

These gates determine, which direction, either forward or reverse, that the unit is operating in. The control is done by the FWD/REV switch on the front panel.

NOTE

When the unit is operating in conjunction with a Tape Search and Control Unit the FWD/REV switch is disabled when the cable between the two units are connected.

4.13 CODE SELECT AND RATE COUNTER CONTROL (5)

This logic determines which code is to be translated. The contents of the CODE SELECT switch is fed into these gates which determine the gating arrangement for the pulse rate counter (reference Paragraph 4.11).

4.14 MINOR TIME RATE CONTROL (5)

The Minor Time Rate Control logic is used to program the clock entry to the Minor Time Counter. The Minor Time Clock control gates the Minor Time counters to accept the 1 kHz clock generated from the carrier frequency of the IRIG B code. The 1 kHz clock is gated to clock mscl (milliseconds counter one) flip-flop via the term slkc. The 1 kHz is then divided down to the 1 pps output frequency of the Minor Time Counter.

4.15 SECONDS CONTROL (5)

The seconds control logic determines the synchronization of certain parts of the Minor and Major Counters for different codes.

4.16 REGISTER CONTROL (5)

The Register Control logic receives ZC8 (a pulse ten times the pulse rate of the code) from the pulse counter and register control logic (reference Paragraph 4-11) and divides it in binary to define each element of the time code word.

4.17 MINOR TIME RESET AND CONTROL (5)

To synchronize the Minor Time Counter to the time frame of the input time code, MTR (Minor Time Reset) is generated. This pulse is generated by counting the exact number of pulses in each frame and outputting a pulse, MTR, which occurs "On Time" for all codes. MTR, is then routed through the frame bypass logic to determine if the Minor Time Counter is to be synchronized or not.

4.18 SYNC MODE AND LOADING (7)

4.19 ERROR COUNTER RESET

The Error Counter Reset logic selects a count from the Minor Time Counter, which occurs once per frame for the code being translated. This is done to ensure that only one error per time frame can be detected. The selected count is also sent to the Tape Search Connector as FRP (Frame Rate Pulse) if no error was detected.

4.20 LOAD CONTROL

This set of gates enables the Major Time Scan Terms to strobe the Major Time Counter, when the term load is in a true state.

4.21 SCAN AND COMPARATOR

The 30-bit BCD terms generated by the Major Time Counter are gated with the Major Time Scan terms (decoded terms from the Register Control Logic) and compared with the 4-bit shift register output (SF1-SF8) of the input and decode for equality.

4.22 ERROR DETECTOR

Any time an error is detected during the code time frame it is stored by the Error Detector flip-flop ED1. ED1 is reset at the end of each frame by FRP and is set by the first detected error; therefore, only one error per frame is counted. Each time an error is detected, the ERROR lamp comes on and remains on until the error is cleared.

4.23 ERROR COUNTER

The Error Counter is a binary permuted down counter. The number of frames to be counted before a load command is given is loaded into the counter from the contents of the MODE switch. When ED1 is reset it decrements the counter until the selected number has been counted and only then can the load command be given. Once the count has been reached the command is constant and "jamming" continues until a time frame has passed without an error (ED1 being set) and at this time the error counter is again loaded with the contents of the MODE switch. SW1 and SW2 (pins on sync mode card) select whether or not the Minor Time Counter is controlled by the FRAME BYPASS switch or not. If the pin is in the SW1 position the Minor Time Counter is allowed reset only if the Error Counter has counted the number of frames to be bypassed. If the pin is in the SW2 position, the Minor Time Counter is allowed to be reset each time frame.

4.24 MINOR TIME COUNTER (8)

The Minor Time Counter accepts a clock frequency equal to the carrier frequency of the input code and divides the selected clock by decade

division down to 1 pps. The Minor Time is automatically synchronized to the input. The BCD outputs of the Minor Time (Figure 4-6) are buffered and used to drive the options included with the 9210 basic unit. The 1 pps output is used as the clock for the Major Time Counters.

4.25 MAJOR TIME COUNTERS (9)

The time-of-year information in the Major Time Counters is derived from the input time code via the parallel 4-bit data lines SF1-SF8. This data is strobed into the Major Time Counters by the sUSC-sHDC terms. The time-of-year information is constantly compared with the time on the input code for accuracy by the sync mode and load logic, and corrected as necessary.

The Major Time Counters are incremented by the 1 pps clock from the Minor Time Counter.

The output of the Major Time Counter (Figure 4-7) are buffered and used to drive the display logic and any options where required.

4.26 DISPLAY LOGIC (10)

The display logic accepts the 30-bit BCD parallel outputs of the Major Time Counter and converts it to decimal form suitable to drive NIXIE type indicator tubes.

4.27 POWER SUPPLY (Refer to Power Wirimg Diagram in Appendix A for Specific Wiring Information)

The 9210 is designed to option several different configurations of power inputs and internal battery.

(1) AC OPERATION

Input to the power transformer is 115 volts ±10%, 50 to 400 Hz or 230 volts ±10%.

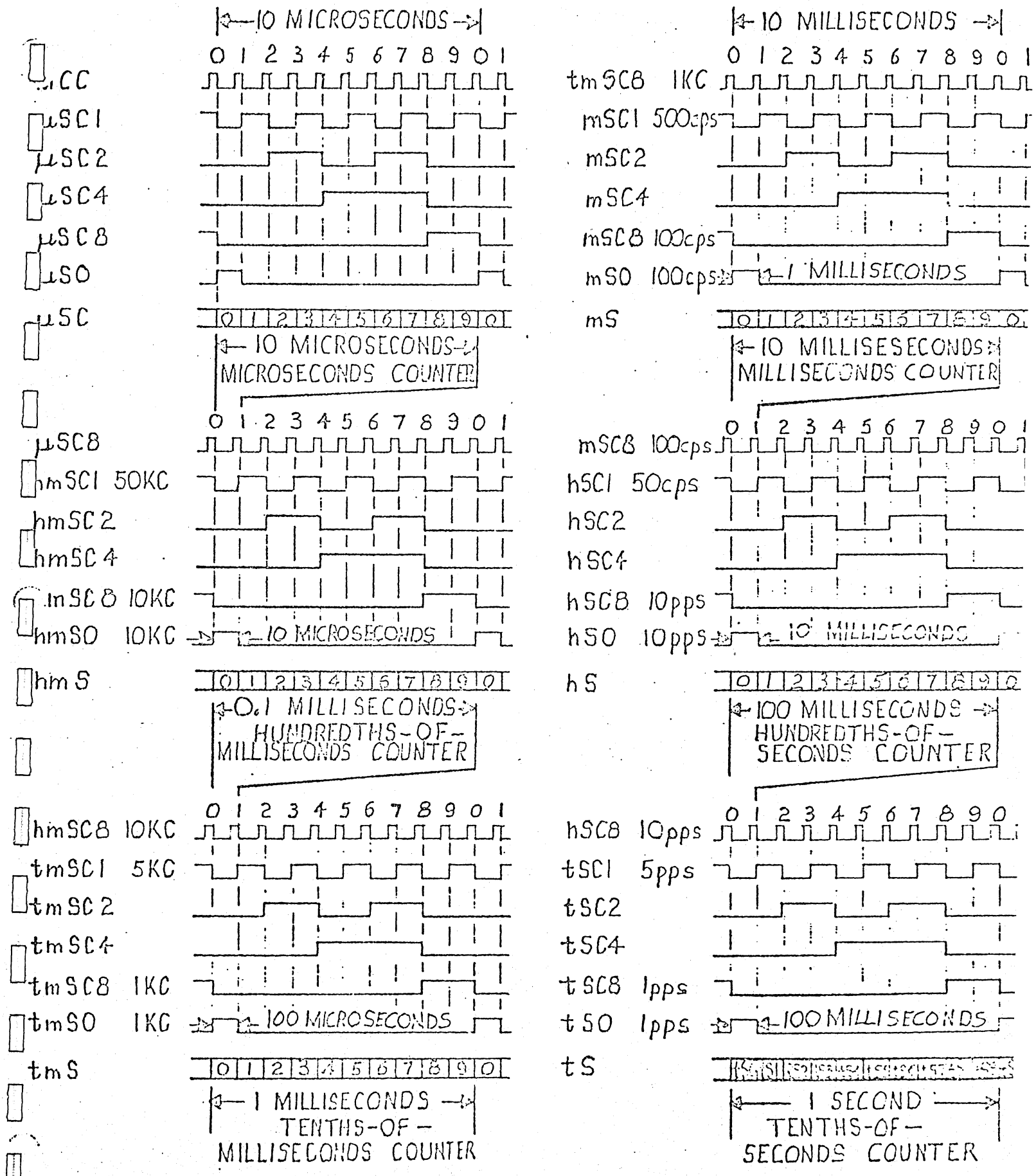


Figure 4-5 Minor Time Counter, Timing Diagram

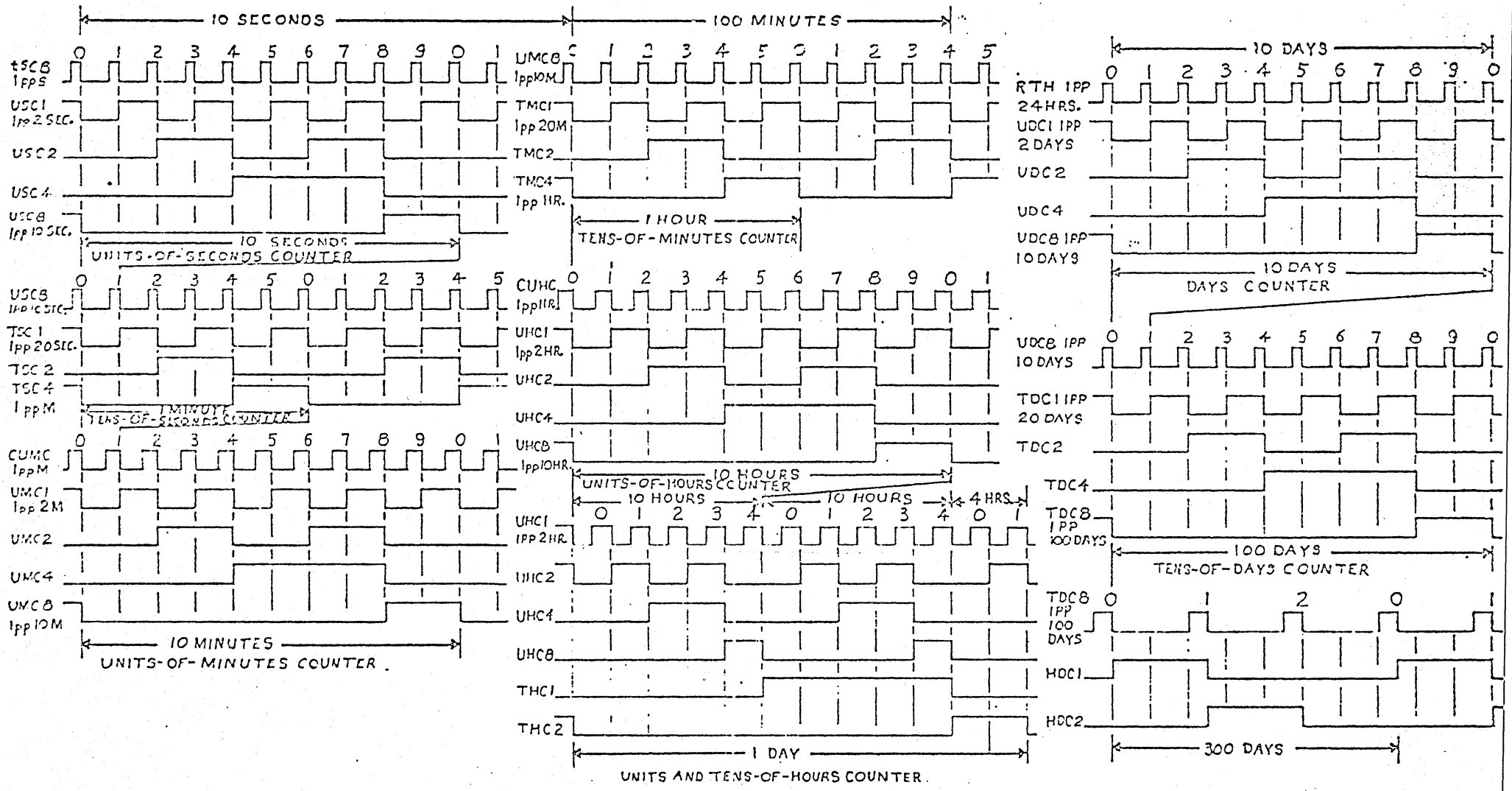


Figure 4-6 Major Time Counter, Timing Diagram

NOTE

The unit is normally shipped in 115 volt configuration, but if 230 volt operation is required the only thing necessary is to change the tap on the input transformer, refer to Wiring Diagram for this information.

The output of the transformer drives a bridge rectifier which supplies +23VDC to the internal regulators.

a. Assembly 15728 - Regulator. This assembly is a +5 volt, +15 volt and -15 volt regulated supply. The 15728 assembly receives a raw unregulated power input of about 23 volts. It is a switching regulator which very efficiently reduces this voltage to a +5 volt regulated output. The efficiency is around 70%. Current pulses into Regulator A1 are supplied through Transistors Q1 and Q2. When Q1 and Q2 are turned off, current is supplied through CR1, thus the energy storage in this device is the inductor L1. This circuit switches at a frequency in the range of 10 to 20 KC. Thus a squarewave is observed on L1 and CR1. This squarewave is AC coupled and DC stored to provide an unregulated output which is used to feed the -15 volt regulators. Chip A2, along with the power transistors Q5 and Q6 become a ±15volt regulator with current limiting resistors R15 and R17. Current limiting is provided through resistors R7 and R8 (for +5v) being an adjustment for maximum current allowed. Over-voltage protection

is provided by CR5 and CR6 when the voltage exceeds about .7 volts CR5 conducts turning on CR6, which pulls the output to ground. Remote Sensing is available through E6; thus, regulation is at the point of distribution. Therefore, resistance in the wire out to the distribution points does not affect the regulation.

CHAPTER FIVE

MAINTENANCE

5.1 INTRODUCTION

This chapter describes the general techniques for maintenance of timing equipment. Special maintenance information, if required, is included with the descriptions contained in the Appendix A.

5.2 PREVENTIVE MAINTENANCE

This instrument consists of solid-state electronic circuits which require very little attention. In general, the equipment will meet its performance requirements without periodic adjustments.

If a routine for periodic inspection and testing is desired, refer to Table 5-1. Equipment can be tested using the performance specifications of Chapter One and those included in Appendix A as the minimum standard of operation. If variations in performance are noted from the standards listed, the general troubleshooting procedures of Paragraph 5-3 should be followed to locate the cause of the malfunction.

When circuit components are replaced, circuit adjustments may be affected. Perform all applicable adjustment procedures included in this chapter or included with the descriptions contained in Appendix A.

Table 5-1. PERIODIC MAINTENANCE SCHEDULE

Task	Interval	Procedure
Inspect The Following:		
Controls	Semi-Annually	If a front panel control does not rotate freely, the shaft may be bent or the knob may be damaged. Replace the control or knob.
Card Guides	Annually	Realign or replace broken or misaligned card guides. This can result from mishandling.
Circuit Cards	Semi-Annually	Replace any cracked cards. These may result in intermittent failures.
Resistors	Semi-Annually	Check resistance of any discolored resistor.
Cables	Semi-Annually	Check for frayed insulation and wiring. Ensure that no cables are squeezed between subassemblies. When replacing cards, check for bent or spread connector pins. An attempt to install the wrong card may have spread the pins.
Clean The Following:		
Housing	Semi-Annually	Clean interior and exterior with a dry cloth. Use an alcohol-moistened cloth for removing grease deposits.
Circuit Cards	Semi-Annually	Wipe with an alcohol-moistened cloth.
Resin Deposits	After Soldering	Remove with an alcohol-moistened cloth or use spray with Freon from an aerosol can.

The equipment should be cleaned periodically to prevent accumulations of dust from affecting proper cooling of the equipment. Clean around components, replace filters as required, and oil the fan once a year.

5.3 TROUBLE SHOOTING PROCEDURE

The following suggestions are general in nature and are based on established electronic troubleshooting procedures. They are provided only as a guide to expedite repairs, not as a substitute for the experience and good judgment of the technician.

In troubleshooting electronic equipment, sources of problems can be divided into two categories: improper operating procedures and equipment malfunctions. Operating procedures can be reviewed before checking equipment. Equipment malfunctions can be systematically found by dividing the equipment into functional areas as illustrated on the block diagrams.

Each area, in turn, can be divided into smaller areas such as power circuits, basic timing circuits, etc. In this way those areas not involved in the problem can be eliminated from consideration until the source of the problem is localized to a circuit card. This circuit card can then be replaced and the equipment again checked for proper operation. The defective circuit card can then be returned to the factory for repair.

The steps in this troubleshooting procedure are summarized as follows:

a. Check equipment operating procedures
b. Check equipment visual indications
c. Check power inputs and power supply fuses and circuit breakers.

d. Check power circuits
e. Check basic timing circuits
f. Check individual circuit cards

Under certain conditions, circuit card replacement can cause more damage. This can occur when the circuit card damage is a symptom of the malfunction and not the actual cause. To avoid damage to replacement circuit cards, these cards should not be replaced in a haphazard manner.

Since some instrument malfunctions are the result of related system activities or external noise, replacement of a circuit card may not eliminate the malfunction. In this case, the existing indications must be re-evaluated in light of the new information and the search for the cause of the malfunction must be expanded into other system areas.

5.4 ADJUSTMENTS

5.5 AGC AMPLIFIER ADJUSTMENTS (Drawing 15584)

a. Apply an input signal to the unit within its normal operating range (See Specifications, Chapter One).

b. Observe the signal at TP1 with an oscilloscope.

c. Adjust R50 for one ØC pulse for every carrier cycle contained in a normal mark amplitude pulse.

d. Observe the signal at TP2 with an oscilloscope.

e. Adjust R72 for an optimum squarewave output form at TP2.

f. Observe the signal at TP3 with the oscilloscope.

g. Adjust R62 for 0 volt DC offset at TP3.

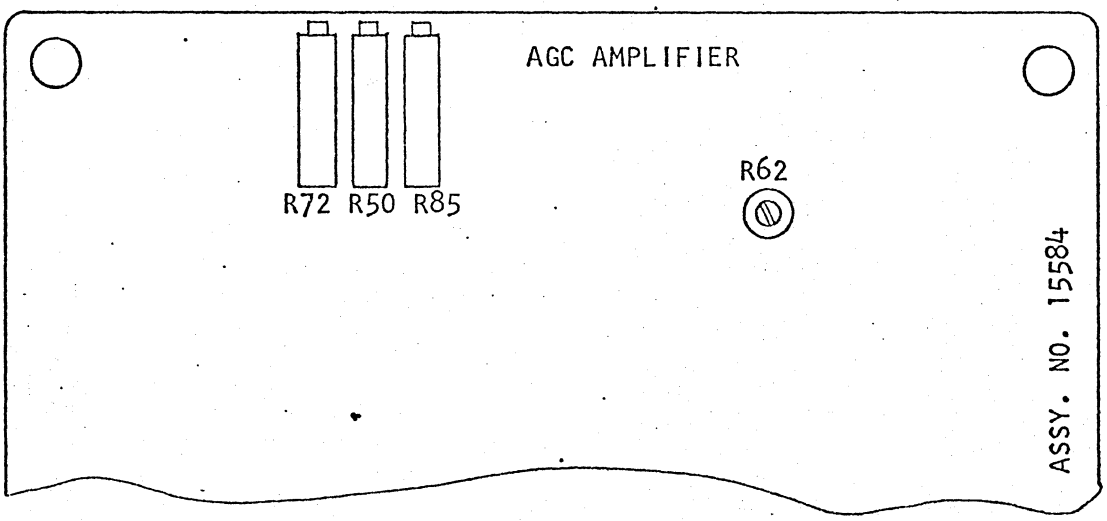
h. Observe the input signal with an oscilloscope.

i. Set the input code amplitude to the desired threshold level that is within the operating range of the unit (See Specifications, Chapter One).

j. Adjust R85 on Assembly 15584 so that the LOSS OF SIGNAL lamp flickers on and off.

k. Lower the input code amplitude below the threshold level. The LOSS OF SIGNAL lamp should turn off.

l. Raise the input code amplitude above the threshold level. The LOSS OF SIGNAL lamp should turn off.



5.6 DC CODE ADJUSTMENT (Drawing 15599)

a. Connect a DC shift code to the input connector (See Top Assembly Drawing).

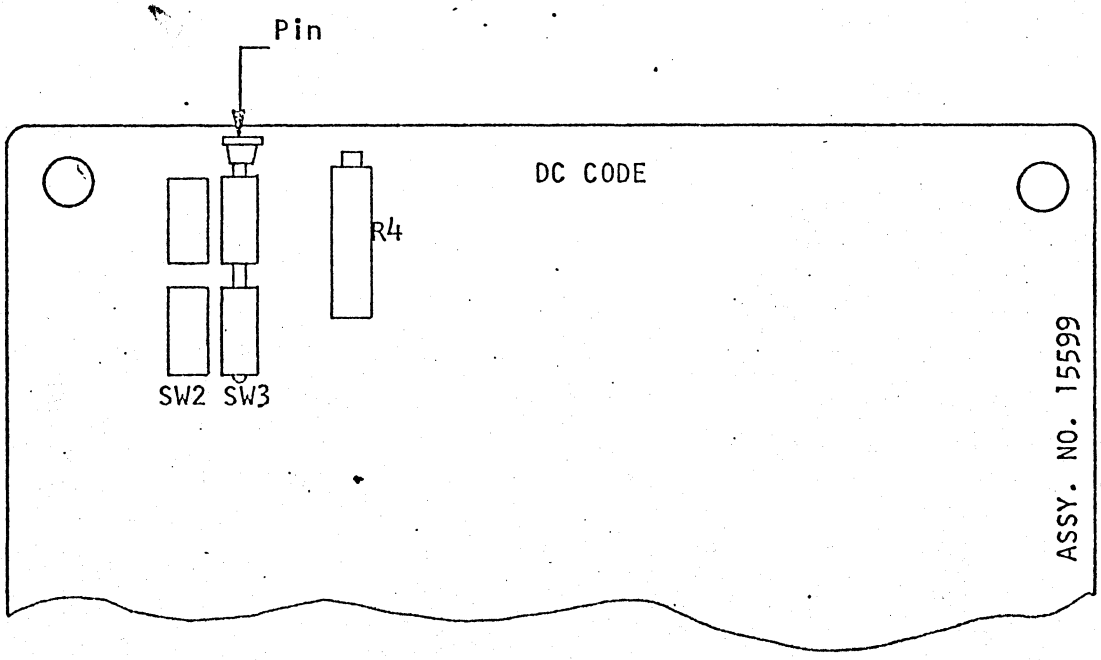
b. Set front panel selector switch to DC CODE position.

c. Set PLAYBACK and SEARCH FILTERS switches to the DC code carrier frequency (Refer to translator operating procedures in Paragraph 3-8. Also refer to the FILTERS switch section on Controls, Paragraph 3-3).

d. Set up front panel switches as called out in Paragraph 3.9b.

e. Set up DC Code switches on Card 15599 as called out in Paragraph 3.5c.

f. Adjust R4 on Assembly 15599 for a normal reconstructed DC code envelope. Check for proper time indication on the front panel NIXIE display.



5.7 POWER SUPPLY ADJUSTMENT

a. Regulator (Assembly 15723)

1. Monitor E5 with a voltmeter.

2. Adjust R10 for +5 volts, ±5%.

3. Adjust R6 for maximum current allowed.

b. Regulator (Assembly 15728)

1. Monitor E5 with a voltmeter

2. Adjust R10 for +5 volts, ±5%.

3. Adjust R6 for maximum current allowed.

CHAPTER SIX

MATERIALS LIST

This chapter contains the materials list applicable to the circuit cards of the basic unit. The recommended spare parts list, the chassis materials lists, and the materials lists for special options added to the basic unit are located in Appendix A. The following materials lists are included in this chapter.

Number	Title
15584	AGC Amplifier
15585	Band Pass Filter
15599	DC Code
15603	Filter Switch
15622	Failsafe
15662	Minor Time Counter
15663	36-Bit Buffer
15664	Major Time Counter
15666	Front Panel Display
15673	Decoder #1
15675	Sync Mode
15722	Raw Supply
15728	Regulator (+15v, +5v, -15v)
15788	Decoder #2

Datapin MATERIALS LIST

REV

1 OF 3

DATE: 1-31-70 JOB NO: TITLE: AGC AMPLIFIER

DRAWN: MILES QUANTITY: ASS'Y NO: 15584

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0100	RESISTOR 10Ω 1/4W 5%	DATUM	7				R25, 32, 33, 63, 64, 86, 87
2	-0201	200Ω		1				R29
3	-0301	300Ω		3				R66, 78, 80
4	-0911	910Ω		2				R75, 82
5	-0152	1.5K		2				R34, 57
6	-0302	3K		13				R11, 19, 27, 28, 30, 40, 41, 47, 52, 54, 65, 69, 70
7	-0512	5.1K		9				R7, 8, 13, 23, 45, 77, 79, 81, 84
8	-0272	2.7K		1				R5
9	-0752	7.5K		1				R49
10	-0103	10K		5				R15, 21, 43, 68, 17
11	-0153	15K		1				R26
12	-0203	20K		4				R16, 39, 73, 74
13	-0303	30K		2				R67, 71
14	-0683	68K		3				R24, 46, 51.
15	-0104	100K		2				R20, 42
16	-824	820K		1				R3
17	-0105	1 MEG		5				R14, 22, 35, 89, 90
18	0102-0115	1.1 MEG 1/4W 5%		1				R44
19	0102-0225	2.2MEG 1/4W, 5%		3				R55, 60, 88
20	0102-0473	47K 1/4W 5%		1				R1
21	0102-0513	RESISTOR 51K 1/4W 5%	DATUM	4				R53, 54, 58, 59
22								
23	0220-0474	CAPACITOR .47μf, 35V, 10%	DATUM	3				C7, 28, 29
24	0102-0510	RESISTOR 51Ω 1/4W 5%	DATUM	2				K4, 6
25	0225-0101	CAPACITOR 100 PF 100V	DATUM	1				C11
26	0212-0472	CAPACITOR .0047μf 100V	DATUM	3				C5, 16, 23
27	0212-0104	CAPACITOR .1μf 100V	DATUM	3				C10, 19, 20
28	0212-0124	CAPACITOR .12μf, 100V, 1%	DATUM	1				C1

Datum, Inc — MATERIALS LIST

DATE: 1-31-70 JOB NO: TITLE: AGC AMPLIFIER

DRAWN: MILES QUANTITY: ASS'Y NO: 15584

REV

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
29	0220-0476	CAPACITOR 47 µf 35V	DATUM	5				C4,9,15,18,24
30	0201-0470	CAPACITOR 47 pf 100V 5%	DATUM	2				C12,22
31	CS13BC475K	CAPACITOR 4.7 µf 35V	MIL-C-2665B	1				C6
32	0212-0223	CAPACITOR .022 µf 100V 5%	DATUM	2				C2,3
33	0500-0306	DIODE IN914A	DATUM	6				CR1 - CR6
34	0515-1001	DIODE IN707A ZENER 7.1V	DATUM	2				CR7,10
35	IN759A	DIODE, ZENER 12V	IOR	2				CR8,9
36	0154-1001	POT 1K 62PR1K	DATUM	1				R62
37	0301-9710	AMPLIFIER 710CE	DATUM	5				A1,2,4,5,7
38	µ5B770239	AMPLIFIER	FAIRCHILD	2				A3,6
39	170217	P.C. BOARD	DATUM	1				
40	0550-7700	TRANSISTOR 2N3643	DATUM	2				Q18,19
41	0550-7705	2N3565		1				Q11
42	0555-6600	2N3645		7				Q3,6,7,10,14,17,20
43	0570-8009	2N3970.		5				Q4,5,13,15,16
44	0570-8703	TRANSISTOR U1487E		5				Q1,2,,8,9,12
45	0102-0183	RESISTOR 18K, 1/4W, 5%		1				R2
46	0153-5001	POT 5K 76PR5K		1				R50
47								
48	0104-0101	RESISTOR 100Ω 1/2W 5%	DATUM	1				R83
49	76PR500K	POT 500K	BECKMAN	1				R85
50	0102-0202	RESISTOR 2K 1/4W 5%	DATUM	1				R9
51	0102-0682	RESISTOR 6.8K 1/4W 5%	DATUM	1				R12
52	0153-5002	POT, 50K 76PR50K	DATUM	1				R72
53	0102-0102	RESISTOR 1K 1/4W 5%	DATUM	2				R10,61
54	0212-0103	CAPACITOR .01µf 100V	DATUM	8				C8,13,14,17,21,25,26,27,3
55	0102-0393	RESISTOR 39K 1/4W 5%	DATUM	3				R66,67,68
56	0102-0123	RESISTOR 12K 1/4W 5%	DATUM	1				R48

Datum Inc — MATERIALS LIST

REV

3 OF 3

DATE: 3-20-70 JOB NO: _____ TITLE: AGC AMPLIFIER

DRAWN: MILES QUANTITY: _____ ASS'Y NO: 15584

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
57	0102-0472	RESISTOR 4.7 K 1/4W 5%	DATUM	1				R18
58	0102-0753	RESISTOR 75K 1/4W 5%	DATUM	1				R31
59	RC20GF301J	RESISTOR 300Ω 1/2W 5%	MIL-R-11	1				R76
61	1706-2010	TERMINAL . 2010B USECO	DATUM	3				TP1-3
63	A-15584	ASSY AID DWG	DATUM	REF				

MATERIALS LIST

REV A- RELEASED

REV D

1 OF 3

DATE: 13 MAR 1970 JOB NO: _____ TITLE: BAND PASS FILTER

DRAWN: J. GILLBANK QUANTITY: _____ ASS'Y NO: 15585

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0120	RESISTOR, 120Ω, 1/4W, 5%	DATUM	2				R29, 35
2	0301	300Ω		2				R92, 93
3	0331	330Ω		1				R98
4	0681	680Ω		2				R26, 32
5	0821	820Ω		1				R101
6	0182	1.8K		2				R28, 34
7	0202	2K		2				R49, 91
8	0222	2.2K		1				R66
9	0132	1.3K		2				R16, 22
10	0332	3.3K		1				R67
11	0472	4.7K		1				R86
12	0512	5.1K		2				R97
13	0562	5.6K		1				R68
14	0622	6.2K		1				R87
15	0103	10K		4				R14, 20, 88, 100
16	0682	6.8K		2				R13, 19
17	0183	18K		2				R15, 21
18	0203	20K		6				R45, 47, 48, 90, 108, 109
19	0223	22K		1				R60
20	0153	15K		2				R5, 10
21	0333	33K		1				R61
22	0473	47K		1				R80
23	0102-0563	56K		1				R62
24	0102-0623	62K		1				R81
25	0102-0104	100K	DATUM	6				R3, 8, 44, 46, 82, 99
26	0102-0683	68K	DATUM	2				R2, 7
27	0102-0184	180K	DATUM	2				R4, 9
28	0102-0224	RESISTOR, 220K, 1/4W, 5%	DATUM	1				R54

Turpin — MATERIALS LIST

REV B

DATE: 13 MAR 1970 JOB NO: _____ TITLE: BAND PASS FILTER

DRAWN: J. GILLBANK QUANTITY: _____ ASS'Y NO: 15585

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
29	0102-0334	RESISTOR, 330K, 1/4W, 5%	DATUM	1				R55
30	0102-0474	470K	DATUM	1				R74
31	0102-0564	560K	DATUM	1				R56
32	RC07GF624J	620K		1				R75
33	0102-0105	1M	DATUM	7				R76, 102-107
34	0102-0226	RESISTOR, 22M, 1/4W, 5%	DATUM	42				R1, 6, 11, 12, 17, 18, 23, 24, 25, 30, 31, 36, 37, 38, 39, 40, 41, 42, 43, 50, 51, 52, 53, 57, 58, 59, 63, 64, 65, 69, 70 71, 72, 73, 77, 78, 79 83, 84, 85, 89, 94
41	0102-0102	RESISTOR, 1K, 1/4W, 5%	DATUM	2				R27, 33
42	0102-0513	RESISTOR, 51K, 1/4W, 5%	DATUM	1				R96
45	390-000 X5P0 330K	CAPACITOR, 33pf	ERIE	1				C9
46	390-000 X5P0 680K	68pf	ERIE	1				C5
47	390-000 X5P0 121K	120pf	ERIE	2				C14, 19
48	0226-0821	820pf	DATUM	1				C6
49								
50	ZA2B182J	.0018μf	IMB	3				C4, 12, 17
51	0212-0153	.015μf	DATUM	1				C8
52								
53	0212-0333	.033μf	DATUM	3				C3, 13, 18
54	0212-0104	.1μf	DATUM	2				C20, 21
55	0220-0474	.47μf, 35V	DATUM	1				C1
56	0212-0224	CAPACITOR, .22μf	DATUM	5				C7, 10, 11, 15, 16

Datum, Inc. MATERIALS LIST

REV B

SHEET 2 OF 3

DATE: 13MAR1970 JOB NO: _____ TITLE: BAND PASS FILTER

DRAWN: J. GILLBANK QUANTITY: _____ ASS'Y NO: 15585

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
57	0500-306	DIODE, IN914A, 40V	DATUM	46				CR1 - CR46
58	0515-0961-B	DIODE, IN961B, 10V	DATUM	2				CR47, 48
60	0550-7700	TRANSISTOR 2N3643	DATUM	2				Q26, 50
61	0550-7705	TRANSISTOR, 2N3565	DATUM	2				Q23, 24
62	0570-8004	TRANSISTOR, 2N3970	DATUM	20				Q11-Q22, 27, 28, 29,
								36, 38, 39, 40, 47
63	0570-8703	TRANSISTOR, U1487E	DATUM	26				Q1-Q10, 25, 30-35
								37, 41-46, 48, 49
66	170231	P.C. BOARD	DATUM	1				
68	A-15585	ASSY AID DWG	DATUM	REF				

Datum, Inc — MATERIALS LIST

REV 1 of 1

DATE: 3-12-70 JOB NO: _____ TITLE: D C CODE

DRAWN: I C QUANTITY: _____ ASS'Y NO: 15599

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0222	RESISTOR 2.2K 1/4W, 5%	DATUM	3				R3, 5, 8
2	0102-0562	5.6K		6				R6, 7, 9-12
3	0102-0103	10K		1				R2
4	0102-0473	RESISTOR 47K 1/4, 5%		1				R1
5	0153-5001	POT 5K		1				R4
6	0102-0391	RESISTOR 390Ω 1/4W, 5%		1				R13
7								
8	0212-0103	CAPACITOR .01μf		1				C11
9	0212-0104	CAPACITOR .1μf		3				C2, 3, 8
10	0220-0475	CAPACITOR 4.7μf, 35V		6				C1, 4, 5, 6, 9, 10
11	0225-0152	CAPACITOR 1500PF		1				C12
12	0301-8280	IC NE8280A		1				A13
13	0301-8490	IC NE8490A		3				A5, 8, 11
14	0301-0322	IC SP322B		2				A7, 12
15	0301-0384	IC SP384A		1				A3
16	0301-0387	IC SP387A		4				A2, 4, 9, 10, 14
17	0301-7710	IC 710CE	DATUM	1				A1
18								
19	0500-8102	DIODE 1N914A	DATUM	2				CR2, 4
20	0515-0152-1	DIODE, ZENER 5.6V	DATUM	2				CR1, 3
21	0515-0961-2	DIODE, ZENER 10V		1				CR6
22	0515-1004	DIODE, ZENER 1N703, 3V		1				CR5
23	1706-2460	SHORTING PIN RSTSM-24		1				
24	1706-3000	TEST POINT, BLACK		1				COM
25	1706-3002	TEST POINT, RED	DATUM	4				SW 2, 3,
26								
27	FREE STOCK	TERMINAL 2010 B	VIFCO	6				TP1 - TP5
28	170242	P.C. BOARD	DATUM	1				

Datum, inc. — MATERIALS LIST

REV 1 OF 1

DATE: 2-14-70 JOB NO: TITLE: SWITCH FILTER CARD

DRAWN: T. ASKIER QUANTITY: ASS'Y NO: 15603

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0512	RESISTOR. 5.1K, 1/4W, 5%	DATUM	2				R3, R6
2								
3	0102-0102	RESISTOR, 1K, 1/4W, 5%		2				R4, R7
4	0102-0103	RESISTOR, 10K, 1/4W, 5%		6				R11-R16
5	0102-0203	RESISTOR, 20K, 1/4 W, 5%		4				R5, 8, 9, 10
6	0212-0104	CAPACITOR .1μf		1				C1
7	0301-7400	I.C. N7400		1				A1
8								
9	0500-0306	DIODE, SILICON 1N914A		14				CR1-14
10								
11	0550-7705	TRANSISTOR 2N3565		2				Q2, Q4
12	0555-6600	TRANSISTOR 2N3645	DATUM	2				Q1, Q3
13	1206-1006	SWITCH 951006	DATUM	2				
14	170232	P.C. BOARD	DATUM	1				
15	A-15603	ASSY AID DWG	DATUM	REF				

Datum, inc. MATERIALS LIST

REV 1 OF 2

DATE: 6 MAY 1970 JOB NO: _____ TITLE: VCO FAILSAFE

DRAWN: J GILLBANK QUANTITY: _____ ASS'Y NO: 15622

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0100	RESISTOR 10Ω, 1/4W, 5%	DATUM	2				R47, 48
2	0102-0101	100Ω		1				R18
3	0102-0511	510Ω		6				R26, 27, 28, 29, 30, 31
4	0751	750Ω		2				R11, 19
5	0102	1K		2				R4, 17
6	0152	1.5K		1				R20
7	0202	2K		1				R45
8	0272	2.7K		1				R25
9	0302	3K		3				R2, 22, 23
10	0512	5.1K		3				R1, 7, 21
11	0682	6.8K		1				R5
12	0822	8.2K		1				R24
13	0103	10K		12				R9, 10, 12, 13, 14, 33, 35, 37, 39, 41, 43, 46
14	0333	33K		1				R15
15	0473	47K		1				R16
16	0334	330K		1				R44
17	0105	1M		1				R8
18	0102-0225	2.2M 1/4W, 5%	DATUM	6				R32, 34, 36, 38, 40, 42
19	76PR500K	RESISTOR 500K	BECKMAN	1				R6
20	0102-0510	RESISTOR 51Ω 1/4W 5%	DATUM	1				R3
25	390-000-X5P0-680K	CAPACITOR 68pf 100V 10%	ERIE	1				C8
26	0225-0331	330pf 100V 10%	DATUM	1				C2
27	0212-0103	.01μf 100V	DATUM	3				C6, 7, 12
28	0220-0474	CAPACITOR .47μf, 35V	DATUM	1				C3

Datapoint

MATERIALS LIST

REV 2 OF 2

DATE: 6 MAY 1970 JOB NO: _____ TITLE: VCO FAILSAFE

DRAWN: J. GILLBANK QUANTITY: _____ ASS'Y NO: 15622

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
29	0220-0475	CAPACITOR 4.7μf, 35V	DATUM	5				C1, 5, 9, 10, 11
30		CAPACITOR, FACTORY SELECT	DATUM	1				C4
34	0301-8290	I.C. N8290A		2				A14, 15
35	0301-8291	I.C. N8291A		3				A8, 12, 16
36	0301-8490	I.C. N8490A		1				A2
37	8880	I.C. N8880A		3				A1, 3, 4
38	8881	I.C. N8881A		3				A7, 11, 13
39	0322	I.C. SP322B		3				A6, 9, 10
40	0380	I.C. SP380A		1				A5
41	0301-9710	I.C. 710CE		2				A17, 18
44	0500-306	DIODE 1N914A		16				CR1, 4-18
45	0515-0961-2	DIODE 1N961B		2				CR2, 19
46	0515-1004	DIODE 1N703A		2				CR3, 20
49	0555-6600	TRANSISTOR 2N3645		2				Q1, 4
50	0570-8703	TRANSISTOR U1487E		7				Q2, 5, 6, 7, 8, 9, 10
51	0570-4342	TRANSISTOR 2N4342		2				Q3, 11
53	1706-3000	TESTPOINT 119437-C	DATUM	1				COM
54	1706-2610	TERMINAL 2010B	USECO	2				TP1, 2
76	170253	P.C. BOARD	DATUM	1				

Datum, Inc. MATERIALS LIST

REV

DATE: 12-9-70 JOB NO: _____ TITLE: MINOR TIME COUNTER

DRAWN: I Cadwyer QUANTITY: _____ ASS'Y NO: 15662

1 of 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102 - 0562	RESISTOR 5.6K 1/4W, 5%	DATUM	11				R1 - 11
2								
3								
4	0212 - 0104	CAPACITOR .1µf, 100V		2				C2, 4
5	0220 - 0335	CAPACITOR 3.3 µf, 35V		2				C1, 3
6								
7	0301 - 7403	IC US7403A		8				A7-10, 12, 13, 17, 18
8	0301 - 7400	IC N7400A		1				A14
9	0301 - 7402	IC N7402A		2				A15, 19
10	0301 - 8280	IC N8280A ALT. 74196	DATUM	6				A1 - 6
11	0301 - 7410	IC N7410A ALT N8H70	DATUM	2				A11, 16
12								
13								
14	1706-3002	TEST POINT, RED	DATUM	12				SW1 - 6
15	1706-2400	SHORTING PIN		1				
16	1706-3006	TEST POINT, YELLOW		1				
17	1706-2010	TERMINAL 2010B		7				TP1-6, COM
18								
19	170310	P.C. BOARD	DATUM	1				

Datum inc

MATERIALS LIST

REV

DATE: 12-18-70 JOB NO: _____ TITLE: 36 BIT BUFFER

DRAWN: MILES QUANTITY: _____ ASS'Y NO: 15663S

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0222	RESISTOR 2.2K 1/4W 5%	DATUM	1				R1
2								
3								
4								
5	0212-0104	CAPACITOR .1 μf 100V	"	3				C2,3,5
6	0220-0335	CAPACITOR 3.3 μf 35V	"	2				C1,4
7								
8								
9	0301-7408	2 WAY AND GATE USN7408A	DATUM	9				A1-9
10								
11								
12	1706-3000	TEST POINT 119437-C (BLACK)	DATUM	1				COM
13	1706-2010	TERMINAL (20108 USECO)	DATUM	1				TP1
14								
15	170311	P.C. BOARD	DATUM	1				
17	A-15663	ASSY AID DWG	DATUM	REF				
19	DS-107-1-14C	SOCKET	JOLO IND	9				

Datum, inc. — MATERIALS LIST

DATE: 12-28-70 JOB NO: _____ TITLE: MAJOR TIME COUNTER

DRAWN: R. FLOCK QUANTITY: _____ ASS'Y NO: 15664

REV 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0561	RESISTOR, 560Ω, 1/4w, 5%	DATUM	2				R23, 24
2	" -0472	" 4.7K " "	"	1				R19
3	" -0512	" 5.1K " "	"	1				R22
4	" -0562	" 5.6K " "	"	19				R1-12, 14-18, 20, 25
5	" -0473	" 47K " "	"	2				R13, 21
6								
7	0212-0103	CAPACITOR .01 uf @ 100V	"	2				C5, 6
8	0212-0104	" .1 uf "	"	2				C2, 3
9	0220-0475	" 4.7 uf @ 35V	"	2				C1, 4
10	0225-0681	" 680pf (370)	"	1				C10
11	0225-0821	" 820pf (8003)	"	2				C8, 9
12	0225-0152	" 1500pf (3009)	"	1				C7
13								
14	0201-7400	I.C. N7400A	"	1				A14
15	" -7408	" N7408A	"	4				A7, 8, 10, 11
16	" -7411	" N7411A	"	1				A16
17	" -7432	" N7432A	"	1				A15
18	" -8280	" N8280A	"	7				A2-6, 12, 13
19	" -8293	" N8293A	"	2				A1, 18
20	" -7123	" SN74123N	"	2				A9, 17
21	1706-2400	SHORTING PIN RS75M-24	DATUM	1				
22	1706-3000	TEST POINT - BLACK	DATUM	1				COM
23	1706-2010	TERMINAL 2010B	"	5				TP1-5
24	1706-3002	TEST POINT RED	"	6				SW1-3
25	170312	P.C. BOARD	"	1				
26								
27	A-15664	ASSEMBLY AID DWG	DATUM	REF				

Datum, inc.

MATERIALS LIST

REV 1 OF 1

DATE: 1-6-71 JOB NO: TITLE: NIXIE DISPLAY (9110, 9210, 9310)

DRAWN: MILES QUANTITY: ASS'Y NO: 15666 BASIC

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1								
2								
3								
4	0104-0273	RESISTOR 27K 1/2 W 5%		9				R7-R15
5								
6								
7	0212-0104	CAPACITOR .1μf 100V	"	2				C2.3
8	0212-0105-1	" 1μf 400V	"	1				C5
9	0220-0475	CAPACITOR 4.7μf 35V	"	2				C1, 4
10								
11	0301-7441	I.C., NIXIE DRIVER N7441	"	9				A1-A9
12								
13								
14								
15	1708-3789	I.C. SOCKET 16 PIN DIP SOLDER	"	9				XA1-XA9
16	1708-0144	NIXIE SOCKET SK144A	"	9				XDS6-XDS14
17								
18								
19	2203-5991	NIXIE TUBE B5991	DATUM	9				DS6-DS14
20								
21								
22								
23	1300-11	STANDOFF	CAMBION	4				
24								
25								
26								
27	A-15666	ASS'Y. AID DWG.	DATUM	REF				
28	170313	P.C. BOARD	DATUM	1				

Datum, inc. MATERIALS LIST

REV

DATE: 2-17-71 JOB NO: TITLE: DECODER NO. 1

DRAWN: MILES QUANTITY: ASS'Y NO: 15673

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0222	RESISTOR 2.2K 1/4W 5%	DATUM	2				R1, 11
2	0102-0562	" 5.6K 1/4W 5%	"	12				R2-10, 12-14
3								
4	0212-0103	CAPACITOR .01μf 100V	"	3				C2, 4, 5
5	0220-0335	" 3.3μf 35V	"	2				C1, 3
6	0225-0221	" 220 Pf 100V	"	2				C6, 7
7	0212-0153	" .015 μf 100V	"	3				C8, 9, 10
8	0301-7400	I.C. N7400A	"	1				A5
9	0301-7402	" N7402A	DATUM	1				A8
10	0301-7403	" SN7403N	"	2				A2, 3
11	0301-7404	" N7404A	"	2				A4, 9
12	0301-7408	" N7408A	"	3				A11, 14, 19
13	0301-7411	" N7411A	"	1				A15
14	0301-7418	" US7418A	"	1				A7
15	0301-7450	" N7450A	"	1				A12
16	0301-7474	" N7474A	"	1				A21
17	SN74H106	"	T.I	1				A18
18	0301-7107	" SN74107	DATUM	1				A1
19	0301-7123	" SN74123N	"	1				A13
20	SN74194	"	T.I.	1				A6
21	0301-8280	I.C. N8280A	DATUM	4				A10, 16, 17, 20
22								
23								
24	1706-2010	TERMINAL 2010B	"	10				TP1-TP9. COM
25								
26	A-15673	ASSY AID DWG	"	REF				
27								

Datum, Inc. MATERIALS LIST

REV

DATE: 2-15-71 JOB NO: _____ TITLE: SYNC MODE

DRAWN: MILES QUANTITY: _____ ASS'Y NO: 15675

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0102	RESISTOR 1K 1/4 W 5%	DATUM	5				R2-6
2	0102-0222	" 2.2K " "	"	5				R1,13,14,16,17
3	0102-0562	" 5.6K " "	"	8				R7-12,15,18
4								
5	0212-0103	CAPACITOR .01 µf 100V	"	3				C2,4,5
6	0220-0335	" 3.3µf 35V	"	2				C1,3
7								
8	0301-7402	I.C. N7402A	DATUM	1				A13
9	0301-7403	" N7403A	"	3				A1,9,17
10	0301-7404	" N7404A	"	2				A6,18
11	0301-7408	" N7408A	"	1				A11
12	0301-7418	" N7418A	"	1				A12
13	0301-7474	" N7474A	"	1				A8
14	0301-7476	" SN7476N	"	1				A15
15	0301-7107	" SN74107N	"	1				A14
16	SN74154N	"	TEXAS INST.	1			T/S	A10
17	SN74193N	"	TEXAS INST.	1			T/S	A16
18	N8234A	"	SIGNETICS	4			T/S	A2-A5
19	0301-8242	I.C. N8242A	DATUM	1				A7
20								
21	1706-2010	TERMINAL 2010B	"	8				TP1-TP8
22	1706-2400	SHORTING PIN RSTSM-24	"	1				
23	1706-3000	TEST POINT 119437-C BLK	"	1				COM
24	1706-3002	" " 119437-B RED	"	4				SW1,2
25								
26	170286	P.C. BOARD	DATUM	1				
	A-15675	ASSY AID DWG	DATUM	REF				

Datum, inc.

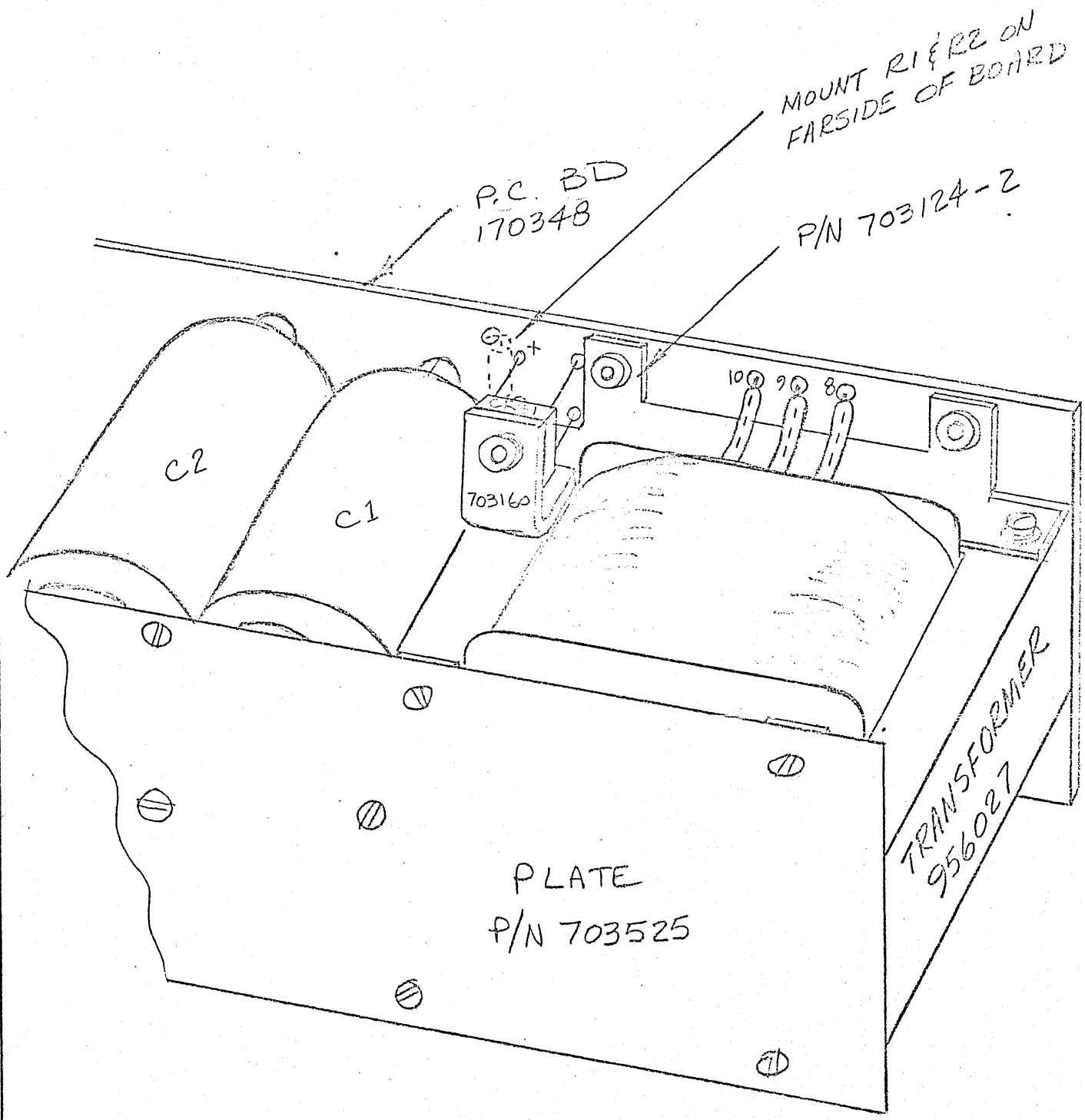
MATERIALS LIST

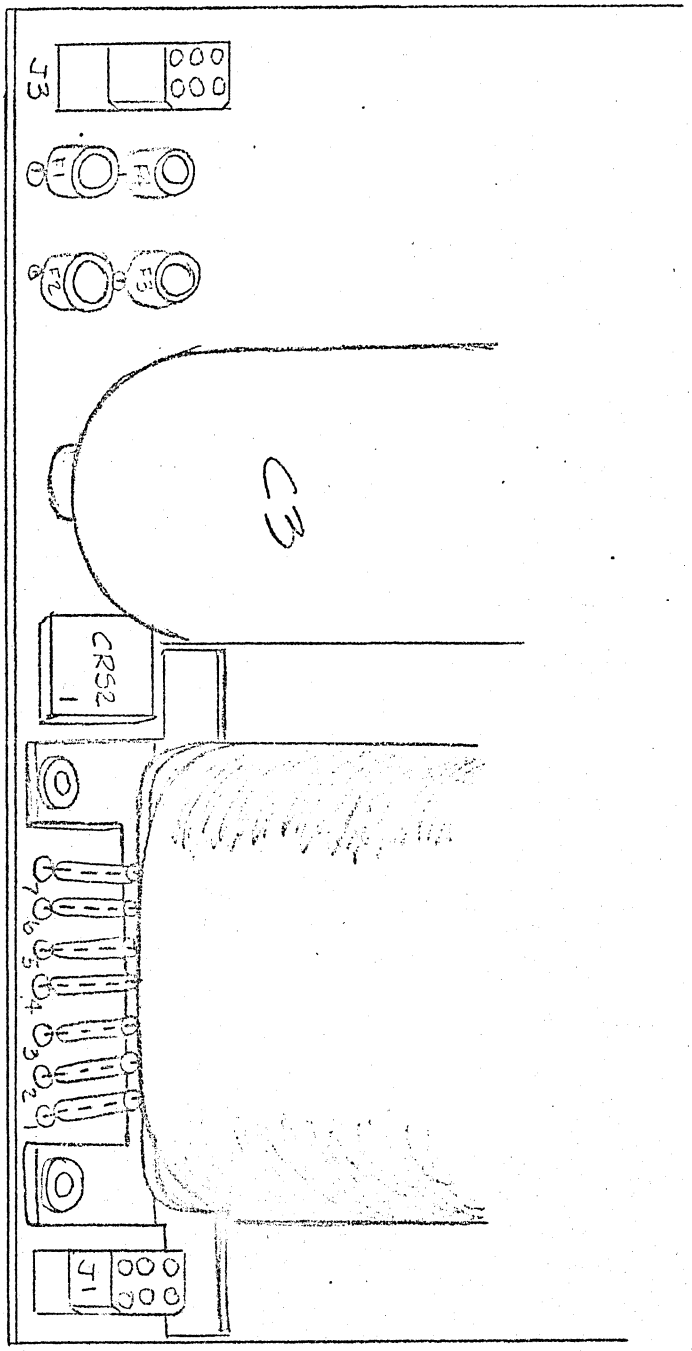
DATE: 6-8-71 JOB NO: TITLE: POWER SUPPLY

DRAWN: A. MARTINEZ QUANTITY: ASS'Y NO: 15722

REV

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0104-0222	RESISTOR 2.2K, ½W, 5%	DATUM	1				R1
2	RC20GF474J	RESISTOR 470K, ½W, 5%	81349	1				R2
3	0219-0107	CAPACITOR 100uf, 350V	DATUM	1				C3
4	0219-0588	CAPACITOR 5800uf, 40V	"	2				C1, 2
5	0540-0198	RECTIFIER VH148	"	1				CR51
6	0540-0447	RECTIFIER VS447	"	1				CR52
7	0703-0250	FUSE ¼ AMP	"	1				F2
8	0703-4002	FUSE 4 AMP	"	1				F1
9			"					
10	956027	TRANSFORMER (12176)	"	1				T1
11								
12	VR-3	CAP CLAMP (MODIFY PER D).	MALLORY	2				CR51
13	703536	CAPACITOR CLAMP MOD.	DATUM	2				C1 & C2
14	703124-1	TRANSFORMER MTG BRKT	"	2				
15	703124-2	" " "	"	2				
16	703160	HEAT SINK	"	1				
17	703525	POWER SUPPLY PLATE	"	1				
18								
19	703548A	P.C. BOARD	"	1				
20								
21	1625-6R	RECEPTACLE	MOLEX	2				J1 & J3
22	1625-6P-1	PLUG	"	2				
23	1560	PINS	"	12				
24	1561	SOCKETS	"	12				
25								
26		NOTE: RECEPT. J1 HAS PINS,						
27		J3 HAS SOCKETS						


MOUNT R1 & R2 ON FARSIDE OF BOARD
P.C. BD 170348
P/N 703124-2
C2
C1
703160
10
9
8
TRANSFORMER 956027
PLATE
P/N 703525


T3
F1
F2
F3
C3
CR52
1
4
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1

Datum, Inc. — MATERIALS LIST

REV 1 of 2

DATE: 7-2-71 JOB NO: _____ TITLE: REGULATOR ASS'Y.

DRAWN: MARTINEZ QUANTITY: _____ ASS'Y NO: 15728

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0220	RESISTOR 22Ω ¼W 5%	DATUM	1				R4
2	0680	68Ω		2				R2, 12
3	0101	100Ω		3				R13, 14, 16
4	0332	3.3K		1				R11
5	0682	6.8K		1				R9
6	0393	39K		1				R1
7	0473	47K		2				R5, 6
8	0102-0754	750K ¼W 5%	DATUM	1				R3
9	CW-2B	.1Ω, 3W	DALE	1				R7
10	CW-2B .5Ω	.5Ω, 3W	DALE	1				R15
11	CW-2B-1Ω	RESISTOR 1Ω, 3W	DALE	1				R17
12								
13	0134-1001	POT 1K 6ZPR	DATUM	1				R10
14	0222-0203	CAPACITOR .022uf 100V		1				C6
15	0220-0475	4.7uf 35V		1				C2
16	0220-0476	47uf 35V		2				C1, 3
17	0220-0107	100uf 10V		1				C4
18	0226-0103-1	.01μf 100V		2				C8, 10
19	0226-0104	.1μf 10V	DATUM	2				C5, 7
20	CS13BE107K	CAPACITOR 100uf 20V	SPRAGUE	2				C9, 11
21	0301-9305	AMPLIFIER CA3035	DATUM	1				A1
22	SG2501D	IC (TO-116)	SILICON GENERAL	1				A2
23	0515-0752-1	DIODE, ZENER, IN752A, 5.6V	DATUM	1				CR5
24	0500-0306	DIODE 1N914A		1				CR2
25	0510-3880	DIODE 1N3880R		1				CR1
26	0570-3715	TRANSISTOR, 2N3715	DATUM	1				Q1
27	MCR106-1	DIODE	MOTOROLA	1				CR6
28	MJE521	TRANSISTOR	MOTOROLA	1				Q5

Datum, inc. MATERIALS LIST

REV 2 of 2

DATE: 7-2-71 JOB NO: _____ TITLE: REGULATOR ASS'Y.

DRAWN: MARTINEZ QUANTITY: _____ ASS'Y NO: 15728

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
29	0550-7705	TRANSISTOR ZN3565	DATUM	1				Q4
30	MJE 371	TRANSISTOR	MOTOROLA	1				Q6
31	0555-6005	TRANSISTOR ZN2905A	DATUM	1				Q2
32	0555-6600	TRANSISTOR ZN3645		1				Q3
33	956045	CHOKE		1				L1
34	1705-8000	IC SOCKET (8 PIN RD.)		1				A1
35	2325-1009	RETAINER - TOROID		2				L1
36	FREE STOCK	INSULATOR TO-3		1				Q3
37	FREE STOCK	MICA INSULATOR - DIODE		2				CR1
38	FREE STOCK	MICA INSULATOR - TRANSISTOR	DATUM	1				Q1
39	5-330865-5	COMPONENT LEAD SOCKET	AMP	2				Q1 BASE & EMITTER
40	5-60494	EYELET	UNITED SHOE	4				L1 (2) CR1 (2)
41	2534	NYLON SPACER BUSHING	H.H. SMITH	2				Q1
42	9534B-B-0440-3	RIVET MOUNT STANDOFF	AMATOM	2				Q1
43	350-1246-10-07	RIVET MOUNT STANDOFF	CAMBION	1				L1
44	DS-107-1-14C	IC SOCKET 14 PIN	JOLO IND	1				A2
45	FREE STOCK	NYLON SCREW #4	DATUM	1				Q5,6
46	703501	HEAT SINK	DATUM	1				
47	170364	P.C. BOARD	DATUM	1				
48								
49	A-15728	ASSEMBLY AID	DATUM	1				
50	IN4934	DIODE	MOTOROLA	2				CR3,4
51								
52								
53								
54								
55								

Datum, inc. — MATERIAL LIST

REV

DATE: 2-11-72 JOB NO: TITLE: DECODER #2

DRAWN: MILES QUANTITY: ASS'Y NO: 15788

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0222	RESISTOR 2.2K 1/4 W 5%	DATUM	1				R2
2	0102-0562	" 5.6 K " "	"	7				R1, 3-8
3								
4	0212-0103	CAPACITOR .01 μf 100V	"	3				C2, 4, 5
5	0220-0335	" 3.3 μf 35V	"	2				C1, 3
6								
7	0301-7400	I.C. N7400A	"	1				A13
8	" -7402	" N7402A	"	2				A5, 18
9	" -7404	" N7404A	"	1				A11
10	" -7408	" N7408A	"	1				A14
11	" -7411	" N7411A	"	1				A4
12	" -7418	" N7418A	"	1				A10
13	" -7432	" N7432A	"	4				A1, 6, 7, 17
14	" -7151	" SN74151N	"	1				A15
15	" -8280	" N8280A	"	2				A2, 16
16	0301-8288	" N8288A	"	1				A3
17	SN74154N	" 24 LEAD	TEXAS INST	1				A9
18	SN74193N	"	" "	1				A8
19								
20	1706-2010	TERMINAL 2010B	DATUM	7				TP1-7
21	1706-3000	TEST POINT 119437-C BLK	"	1				COM
22								
23	170317	P.C. BOARD	"	1				
24								
25	A-15788	ASSEMBLY AID	"	REF				

CHAPTER SEVEN

DRAWINGS

7.1 INTRODUCTION

This chapter contains a set of diagrams pertaining to the basic unit only. The top assembly diagram and other option drawings not included in this chapter are included in Appendix A. The diagrams provide information on the organization and location of components within the unit. The diagrams provided are:

a. Top Assembly Diagram
b. Block Diagrams
c. Logic Diagrams
d. Schematic Diagrams

7.2 TOP ASSEMBLY DIAGRAM

This diagram, located in Appendix A, shows the location of each circuit card as well as pertinent mechanical details of the unit. Each top assembly diagram has a key which identifies all logic cards used in the unit. This key provides the following information:

a. Logic Location
b. Physical Location
c. Assembly Number
d. Title

FOR EXAMPLE: Partial Key on Top Assembly Diagram

ROW A

2-1	13	15509	Decoder
Logic Location	Physical Location	Assembly No.	Title

The first number, (2), in the Logic Location column represents the circled number of an associated logic diagram. The next number, (1), signifies that it is the first type of card used to implement that logic. The Physical Location column shows that the card is located in Slot 13. The top of the key indicates that the card is in Row A. The Assembly No. column identifies the card as a type 15509 card. The Title identifies the function of the card as a decoder.

7.3 LOGIC DIAGRAMS

There is one Logic Diagram illustrating each of the major functions called out on the block diagrams. These Logic functions may be implemented with one or more circuit card types. The Logic Drawings contain two numbers. The circled number identifies the origin point for terms on that Logic Diagram. The second number is the File Number assigned to the drawing. The Logic Drawings are arranged in circled-number order as illustrated on the unit and option block diagrams. Numeric reference designations are used to identify circuit card groups on these logic diagrams.

Each Logic Diagram also has a key which provides information about all cards used to implement the Logic function. No physical location is given. The key provides the following information:

a. Logic Location
b. Assembly No.
c. Title

FOR EXAMPLE: Partial Key on Logic Diagram

1		15509	Decoder	(2) Title Block
Logic Location	Physical Location	Assembly No.	Title	

The logic circled number, (2), is found in the Title Block. The next number, 1, is found in the Logic Location column. It signifies that it is the first type of card used to impliment the desired logic function. The assembly type is identified as a type 15509 card. The Title identifies the function of the card as a decoder. There is nothing specified in the Physical Location column.

7.4 SCHEMATIC DIAGRAMS

The Schematic Diagram for each card assembly is numbered to correspond to the card type number. This number appears on the Top Assembly Drawing, and it stamped on the assembly itself. Schematic diagrams that, for the most part, illustrate integrated circuits are drawn as logic diagrams; discrete components required to complete logic circuits may also be shown. Individual logic elements are identified by an alpha-numeric location designator that indicates column (A-N) and row (1-4) of the integrated circuit in which it is contained. Circuit card outputs are identified by actual pin numbers.

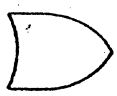
The integrated circuit is shown on the card assembly drawing, at the intersection of the column and row indicated. The integrated circuits are identified on the assembly drawings by their manufacturer's part number. Discrete components are identified by "X" numbers, adjacent to their symbol on the diagrams. There are X1 through X21 locations for discrete components on each circuit card. Schmatic diagrams with conventional symbols are included in the manual for circuits that use mainly discrete components.

7.5 GENERAL LOGIC SYMBOLS

The Logic Symbols used on DATUM drawings are derived from MIL

STD 806B and are utilized in such a manner that signals can be traced through the logic in terms of HIGH and LOW (+2.5 to +5v) and (0V) by examination of the Logic Symbols without the need to memorize the electrical characteristics (NAND, NOR, AND, OR, etc.) of the circuits. The HIGH and LOW signal level indication is illustrated by a straight line for a HIGH signal and a small circle for the LOW signal level. The following symbol shapes are shown in Figure 7-1.

The use of straight lines or circles at inputs and outputs of these basic symbols completely defines the function the circuit performs, the input signal levels required to activate the circuit, and the output signal level when the circuit is activated. See examples in Figure 7-2.



OR SYMBOL

AND SYMBOL

Figure 7-1 Basic Logic Symbols

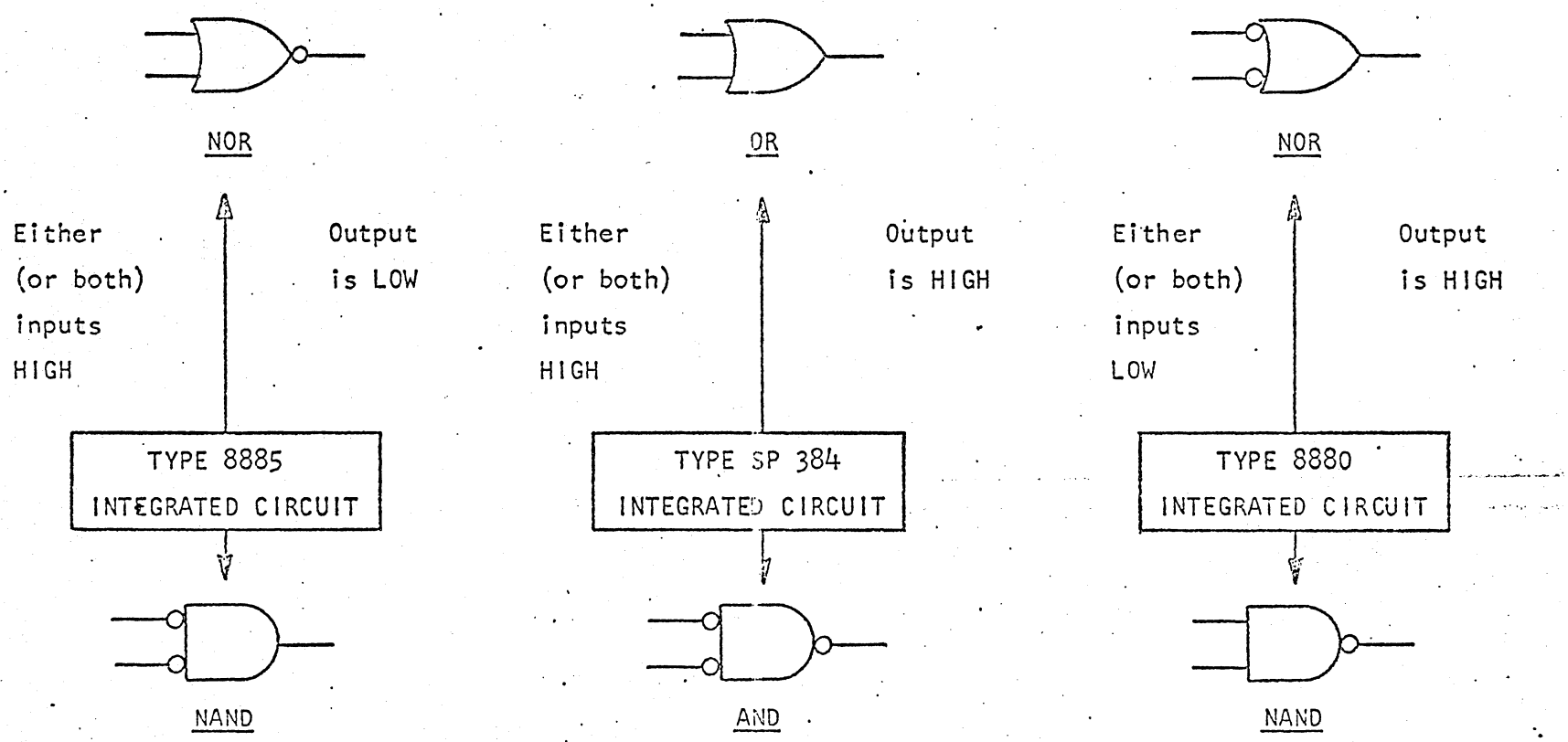


Figure 7-2. Complimentary Logic Symbols

The logic symbols on the drawings indicate function; identical elements may be indicated by different symbols. This is because of the duality inherent in logic elements. For example, a Type 8885 Integrated Circuit can be used as a HIGH input NOR or a LOW input NAND. Similarly, a Type 8880 Integrated Circuit can be used as a LOW input NOR or a HIGH input NAND, and a Type SP384 Integrated Circuit can be used as a HIGH input OR or a LOW input AND. A LOW wired OR or a HIGH wired AND function can also be implemented with certain integrated circuits by connecting the outputs together and adding an external discrete pull-up resistor. Figure 7-3 is an example of this configuration. Figure 7-4 is an example of a 4-to-10 line decoder.

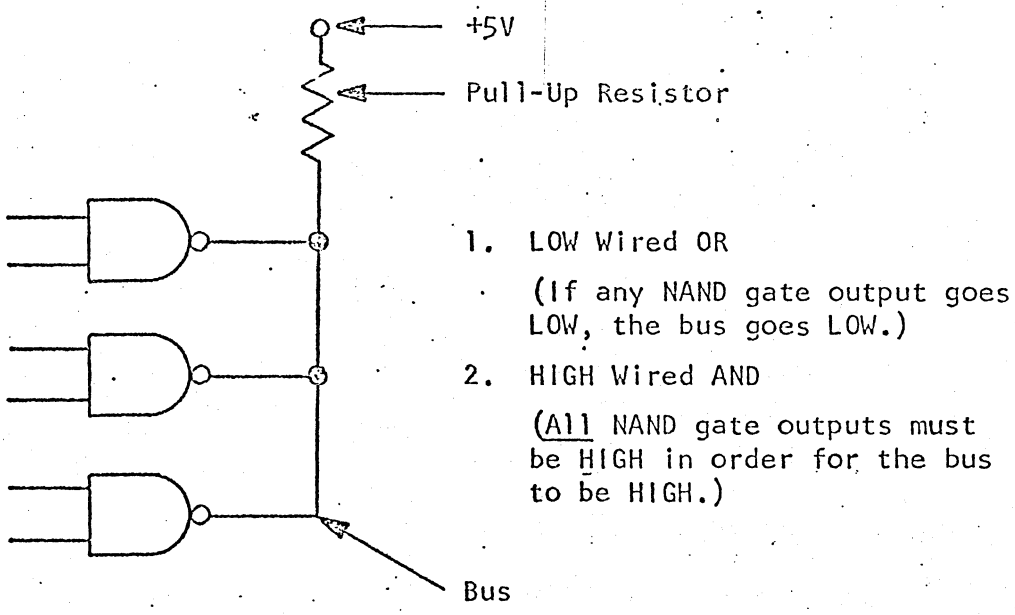


Figure 7-3. Dot Logic Symbols

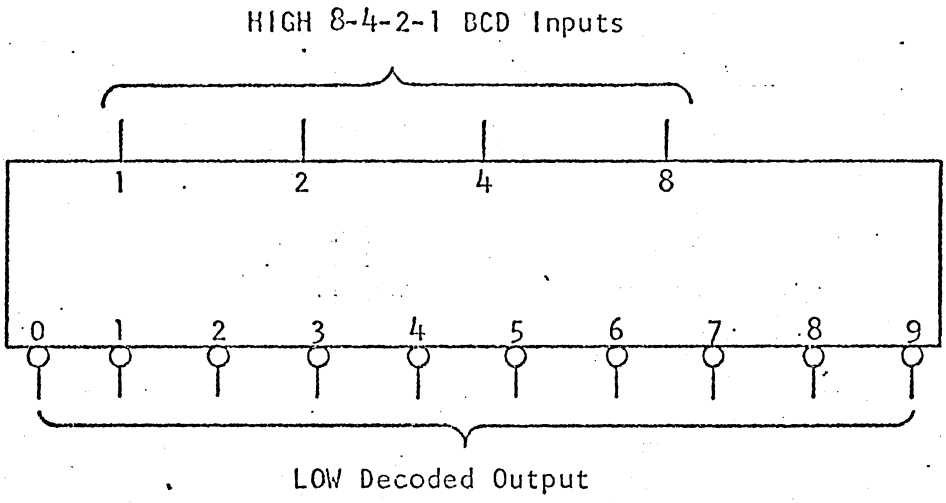


Figure 7-4. 4-to-10 Line Decoder

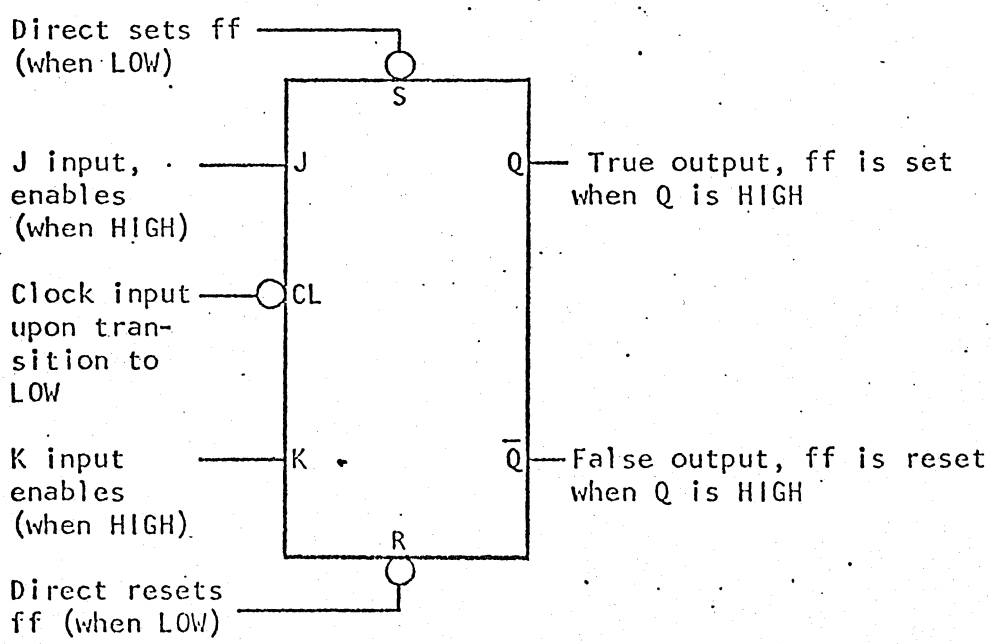
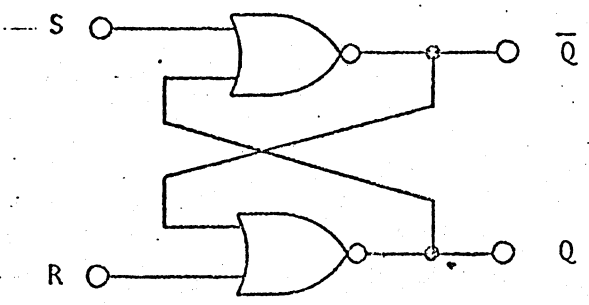


Figure 7-5. J-K Flip-Flop

The following truth table is for the J-K flip-flop illustrated in Figure 7-5. Clocking occurs when the clock signal makes a transition from HIGH to LOW level. A set and reset input controls the flip-flop all the time. The set or reset signal control is LOW.

Input Levels Before Clock		F.F. State After Clock
J	K	
Low	Low	Same as Before Clock
Low	High	Reset
High	Low	Set
High	High	Opposite of Before Clock

An R-S flip-flop (sometimes called a latch) can be formed by interconnecting NOR gates. This flip-flop, and its truth table, are shown in Figure 7-6. Triggering occurs as the R or S input goes HIGH. LOW is indicated by 0, HIGH by 1.



R S	$\overline{Q}$ Q
0 0	No change
0 1	0 1
1 0	1 0
1 1	Indeterminate

Figure 7-6. R-S Flip-Flop

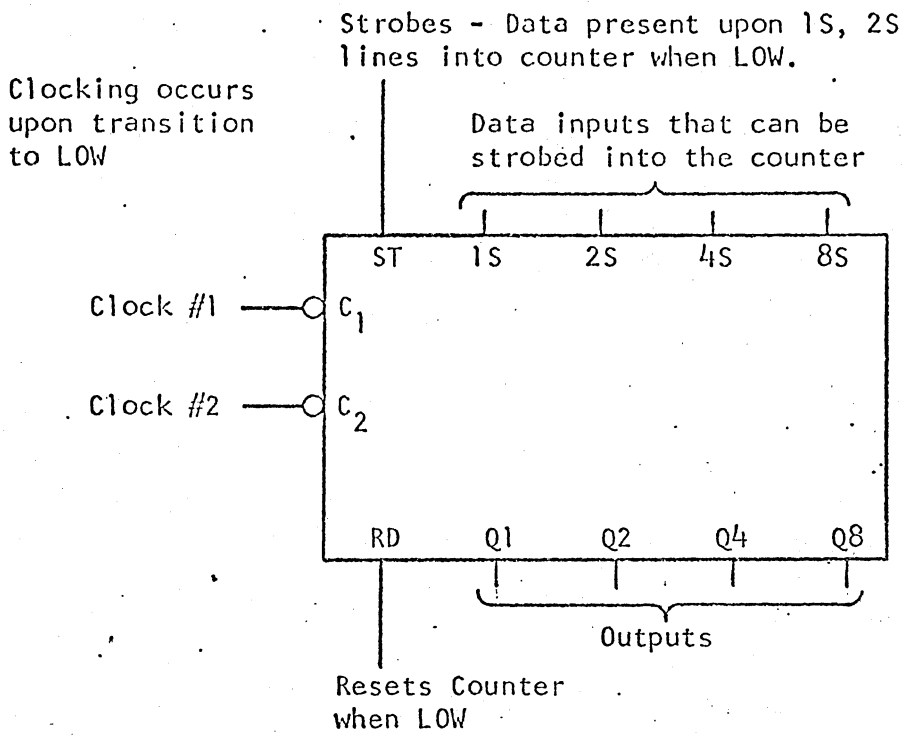


Figure 7-7. Counter

The symbol for a counter is shown in Figure 7-7. Note that the clocking action takes place upon the transition from the HIGH level to the LOW level while the strobe and reset functions are active all the time the strobe or reset signal is at the LOW level.

Clock #1 (C1) toggles the first flip-flop (Q1) in the counter. Flip-flop Q1 divides by two. Clock #2 (C2) clocks the next three flip-flops (Q2, Q4, Q8) in a divide-by-5 configuration. Connecting Q1 output to Clock #2 provides a 1-2-4-8 BCD coded divide-by-10 configuration, which is often referred to as a decade counter. This circuit is also used quite regularly as a four-bit register, particularly where a data display register is required.

7.6 SPECIAL LOGIC SYMBOLS

Pulse shapers, one-shots, or other logic circuits can be formed by adding discrete components (capacitors, resistors) to integrated circuits. The functions of these circuits can be determined by calculating the effects of the components (such as time constants) on the circuit.

If further information is desired about the integrated circuits, it is recommended that the DCL Series 8000 and the UTILOGIC II Designer's Handbooks be acquired from the Signetics Corporation, 811 East Arques Avenue, Sunnyvale, California 94086.

7.7 USING THE DIAGRAMS

The procedures for using the diagrams are fairly simple and follow conventional procedures. Additional information is provided on locating physical component locations from the logic diagrams and locating the logic diagram source of a logic term.

7.8 LOCATING LOGIC TERM SOURCE DRAWING

To locate the Source Logic Drawing of a logic term, follow the signal in a reverse direction until a logic circled number is found. Look up the Logic Drawing with the same circled number in the Title Block. Locate the desired term on that drawing.

7.9 GOING FROM LOGIC DIAGRAM TO PHYSICAL LOCATION

To determine the Physical Location of a component starting from a Logic Diagram, the logic diagram circled number is prefixed to the Logic Location number listed in the key on the Logic Diagram. Using previous examples, a two is prefixed to a one: 2-1. Locate this number on the Top Assembly Diagram in the Logic Location column. Look in the Physical Location Column. This number combined with the row information at the top of the key specified which slot the card is in. Assembly numbers are then compared to ensure that the card types are the same. Refer to the schematic with the assembly number for circuit details. For convenience, the row and slot information should be copied into the Physical Location column on the Logic Diagram for future reference. To save time, this information can be completed for the other cards called out on the Logic Diagram.

7.10 LOGIC TERMS

Mnemonic terms are used on Logic Diagrams to indicate signals. The glossary of terms in this chapter lists the meaning of each term. The terms are arranged in alpha-numeric order.

Terms with an overscore (bar) indicate the FALSE state of the defined term. An asterisk (*) following a term indicates that the designated term has been buffered, or that the shape of the pulse represented by the term has been altered.

GLOSSARY OF TERMS

TERM	POINT OF ORIGIN REF. NO.	DEFINITION
A.C.	4	Indicates A.C. Mode of Operation
A.C.F.	4	Indicates A.C. Failsafe Mode of Operation
Auto Start	6A	External Start
Aux	2	Auxiliary Mode
A+G	5	Selects either IRIG A or IRIG G input time code.
$\overline{A+G}$	5	Inverse of A+G
CFL	4	FL clock. This term is compared with $\overline{CFX}$ to determine the VCO frequency.
$\overline{CFX}$	4	FX clock. This term is used to sync the VCO.
CLK	2	Clock, which is ten times pulse rate of input code.
CSR	2	Clock Shift Register
CODE	1	The filtered, constant, time-code modulated input signal.
C+C'+28	5	Selects either IRIG C 1kc, IRIG C 100 cycles or NASA 28 Input Time Code
DF1 - DF8	2	Decoder flip-flops - reconstructs the input time code modulation envelope.
DZ5	2	Selected clock to DF4
DZ8	2	Selected clock to DF4
E+H'	5	Selects either IRIG E 1kc or IRIG H 100 cycles input code.
FRP	7	Frame Rate Pulse
$\overline{FSA}$	4	Unit in Failsafe condition
FSI	2	Frame Sync Pulse
$\overline{FSI}$	2	Inverse of FSI
$\overline{FWD}$	2	Indicate Reverse Operation
FWD1	2	Indicates forward operation
$\overline{FWD2}$	2	FWD Buffered

GLOSSARY OF TERMS

(Continued)

TERM	POINT OF ORIGIN REF. NO.	DEFINITION
GEN	2	Generate Mode Command
$\overline{GO}$		A term derived from the Tape Search Unit commanding unit to stop.
HDC1-HDC8	9	BCD hundreds of days counts
hmsc1-hmsc8	8	BCD hundredths of milliseconds counts
hsc1-hsc8	8	BCD hundreds of milliseconds counts
HOLD	2	HOLD command
$\overline{HOLD}$	2	Inverse of HOLD
H+H'	5	Selects either IRIG H 1 kc or IRIG H 100 cycles input time code
IRIG A	5	Selects IRIG A input time code
IRIG C	5	Selects IRIG C input time code
IRIG E+SLO	5	Selects IRIG E 1 kc or one of the slow codes
IRIG G	5	Selects IRIG G input time code
$\overline{IRIG\ G}$	5	Inverse of IRIG G
IRIG H	5	Selects IRIG H input time code
LOAD	7	Coincidental with jam time
MCC	6	Megacycle clock
MCC**	3	Minor Time Clock
$\overline{MD}$	1	Mark Detector Pulses
$\overline{MS}$	2	Mark Sync
MTR	5	Minor Time Reset
$\overline{MTR}$	7	Inverse of MTR
MTS		Minor Time Strobe
MSC1-MSC8	8	BCD Milliseconds Count
$N \cdot \overline{F}$	5A	NASA Loads or Reverse Operation
RDC	9	Reset Days Count
RDF4	2	Reset DF4
RHc	9	Reset Hours Count
Rtsc	5	Reset tens-of-seconds count

GLOSSARY OF TERMS

(Continued)

TERM	POINT OF ORIGIN REF. NO.	DEFINITION
Rusc	5	Reset unit-of-seconds count
Rhsc	5	Reset hundreds-of-milliseconds count
Rtsc	5	Reset tenths-of-seconds count
SCF2	5A	Enable Load XC 2
SEARCH		Term to select input filters
SEI	7	Sync Error Indicator
SF1-SF8	2	Data bits to load Major Time Counter
SLO	5	Slow Code Selected
$\overline{\text{START}}$	2	Term derived from START pushbutton
$\overline{\text{START}}$*	2	$\overline{\text{START}}$ buffered
STROBE	7	Comparison Enable to Sync Mode
S100 $\sim$	5	100 cycles code selected to Minor Time Counter
S1kc	5	1 kHz code selected to Minor Time Counter
S10kc	5	10 kHz code selected to Minor Time Counter
S100kc	5	100 kHz code selected to Minor Time Counter
TD	1	Threshold Detector
TDC1-TDC8	9	BCD tens-of-days count
TMC1-TMC4	9	BCD tens-of-minutes count
THC1-THC2	9	BCD tens-of-hours count
TRANS	2	Trans Mode Command
$\overline{\text{TRANS}}$	2	Trans Buffered
TRANS + Z8	2	Trans Mode and Z8
TSC1-TSC4	9	BCD tens-of-seconds count
TSE		Tape Search Enabled
tmsc1-tmsc8	8	BCD tenths-of-milliseconds count

GLOSSARY OF TERMS

(Continued)

TERM	POINT OF ORIGIN REF. NO.	DEFINITION
tsc1-tsc8	8	BCD tenths-of-seconds count.
UDC1-UDC8	9	BCD Unit-of-Days count
UHC1-UHC8	9	BCD Unit-of-Hours count
UMC1-UMC8	9	BCD Unit-of-Minutes Count
USC1-USC8	9	BCD Unit-of-Seconds Count
U1	1	Filter Power of Ten Selector
U2	1	Filter Power of Ten Selector
V1	1	Filter Power of Two Selector
V2	1	Filter Power of Two Selector
V3	1	Filter Power of Two Selector
V4	1	Filter Power of Two Selector
VCO	4	Voltage Control Oscillator Output
XC1-XC16		Output of binary counter that counts position marks.
YC4	5	Envelope Counter Pulse
YC5	5	Envelope Counter Pulse
ZAD	1	Zero Axis Detector
ZC1-ZC8	2	Envelope Counter Pulses
ØA	2	Phase A; Negative On-Time Edge of of Carrier
ØB	2	Inverse of ØA
1kc	8	Sample time at 1 kc rate
1pps	8	One pulse per second
1ppsclk	8	One pulse per second clock to Major Time Counter
.01s	5	Select FRP for one hundredth time frame
.1s	5	Select FRP for one tenth time frame
1s	5	Select FRP for 1 second time frame
10s	5	Select FRP for 10 second time frame
10s + 60s	5	Defines either 10 second or 60 second time frame
60s	5	Select FRP for 60 second time frame

GLOSSARY OF TERMS

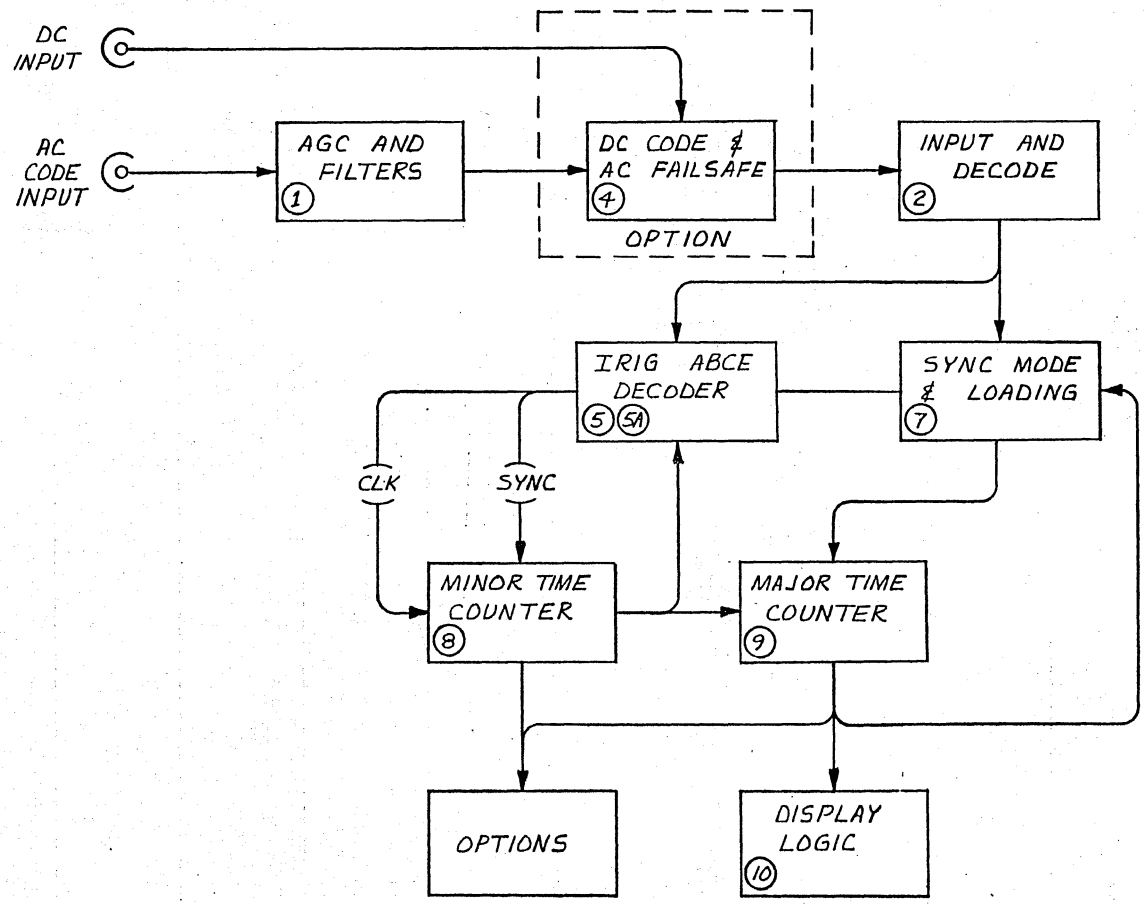
(Continued)

TERM	POINT OF ORIGIN REF. NO.	DEFINITION
60s+E'	5	Defines either IRIG E 100 cycles or 60 second time frame
28+C	5	Defines either NASA 28-bit or IRIG C 1 kc time frame
ΔCLK	8	Selected clock to Minor Time Counter
Δ1kc	8	Selected 1kc clock in Minor Time Counter
Δ10kc	8	Selected 10kc clock in Minor Time Counter
Δ100~	8	Selected 100 cycles clock in Minor Time Counter

DRAWING LIST

Circled Numbers	Title
LOGIC AND BLOCK DIAGRAMS	
9210-8000	9210 Block Diagram
①	AGC and Filters
②	Input and Decode
④	AC Failsafe
⑤	Decoder Control Logic
⑦	Sync Mode and Loading
⑧	Minor Time Counter
⑨	Major Time Counter
⑩	Display Logic
SCHEMATIC DIAGRAMS	
15584	AGC Amplifier
15585	Band Pass Filter
15599	DC Code
15603	Filter Switch
15622	Failsafe
15662	Minor Time Counter
15663	36-Bit Buffer
15664	Major Time Counter
15666	Front Panel Display
15673	Decoder #1
15675	Sync Mode
15722	Raw Supply
15728	Regulator (+15V, +5V, -15V)
15788	Decoder #2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03 XXX ±.010 ANGLES ±1/2°

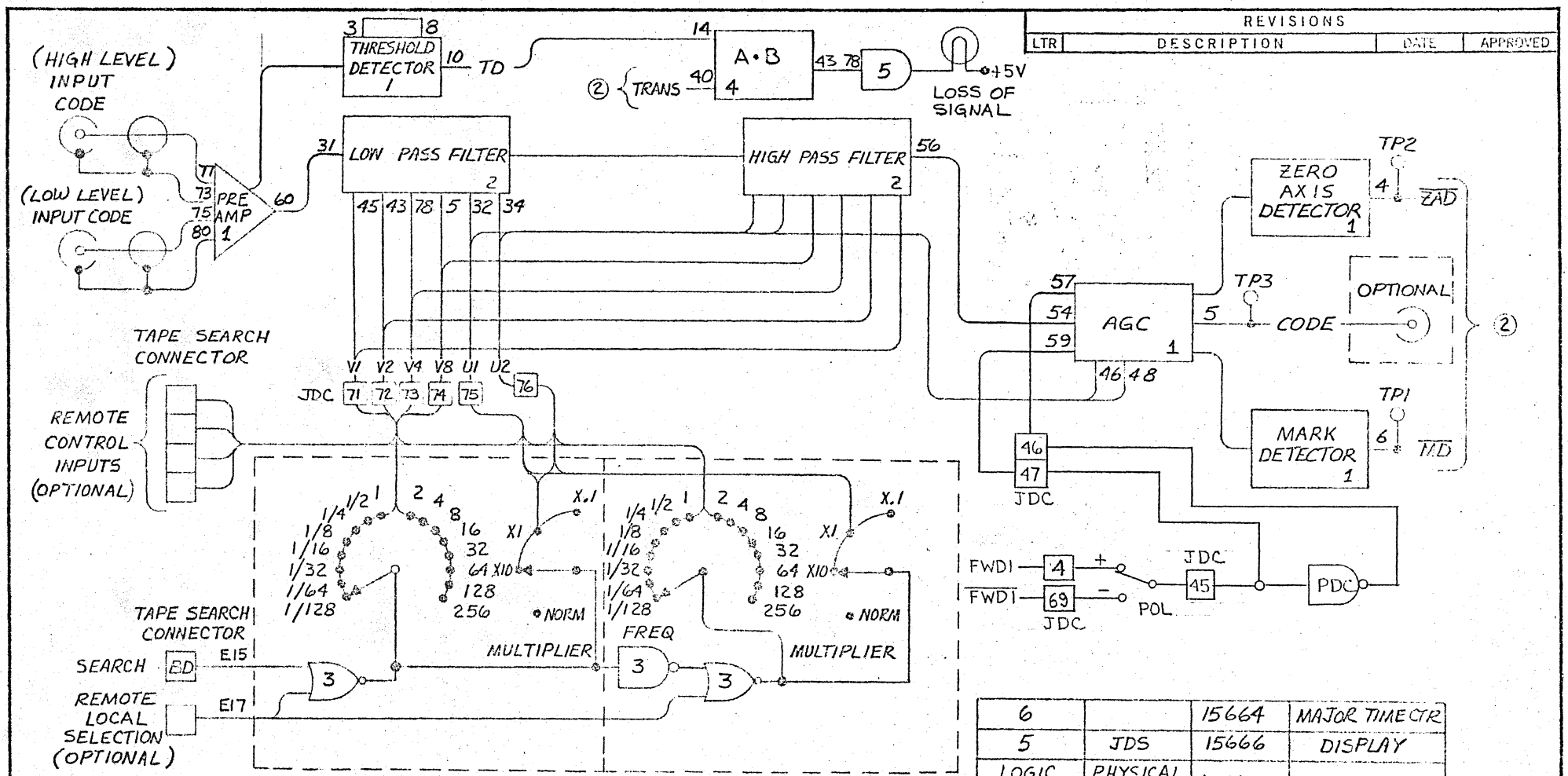
TITLE
9210 BLOCK DIAGRAM

DWN J. GILLBANK	16 JUN 1970	DES		6-16
CHK	6-16	ENGR		6-16
SCALE NONE		FSC 31160		

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE		SHT 1 OF 1	REV
B	9210-8000		

DIETZGEN 196 MG-10



LOGIC LOCATION	PHYSICAL LOCATION	ASSY. NO.	TITLE
6		15664	MAJOR TIME CTR
5	JDS	15666	DISPLAY
4		15673	DECODER #1
3	TB2	15603	FILTER SWITCH
2		15585	BAND PASS FILTER
1		15584	AGC AMPLIFIER

NOTE:

1. SEE TOP ASSEMBLY DRAWING FOR CONNECTOR NUMBERS.

LTR	DESCRIPTION	DATE	APPROVED

REVISIONS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOL .XX ± .03, .XXX ± .010, ANGLES ± 1°

TITLE: AGC AND FILTERS (1)

Datum Inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

DWN KAIN 4/7/72 | CHK | ENG | MFG Helms 4/14/72 | QC | SCALE NONE | DWG 31180 | SIZE B | 9310-8110 | SHT 1 | REV

DIETZGEN 196 MG 10

REVISIONS			
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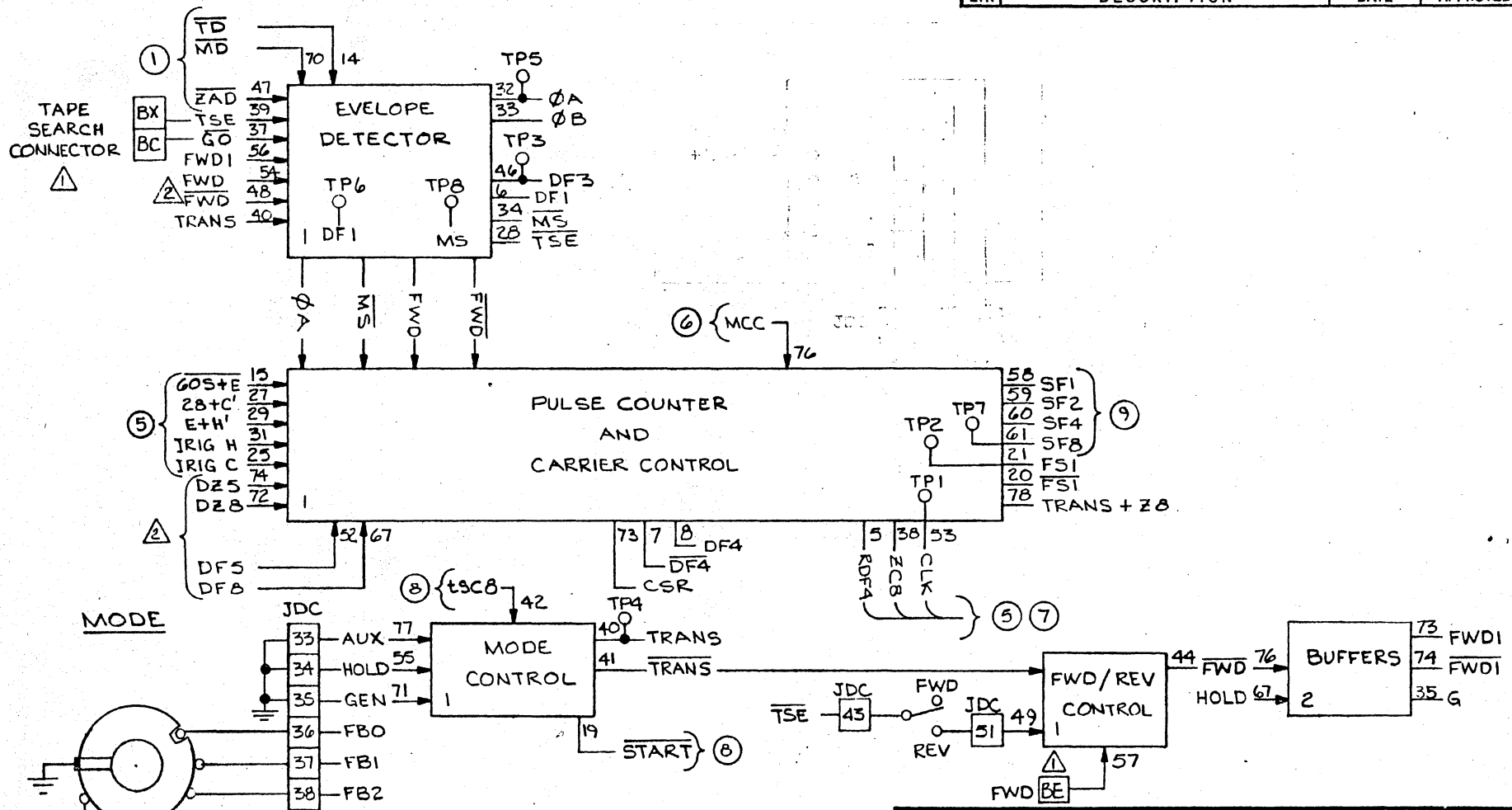


NOTES:
2. FROM NASA DECODER IF USED
1. SEE TOP ASSY. FOR CONN. NO.

LOGIC LOCATION	PHYSICAL LOCATION	ASSY. NO.	TITLE
2		15675	SYNC MODE
1		15673	DECODER #1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03, XXX ± .010, ANGLES ± 1/2°

TITLE: INPUT AND DECODE (2)

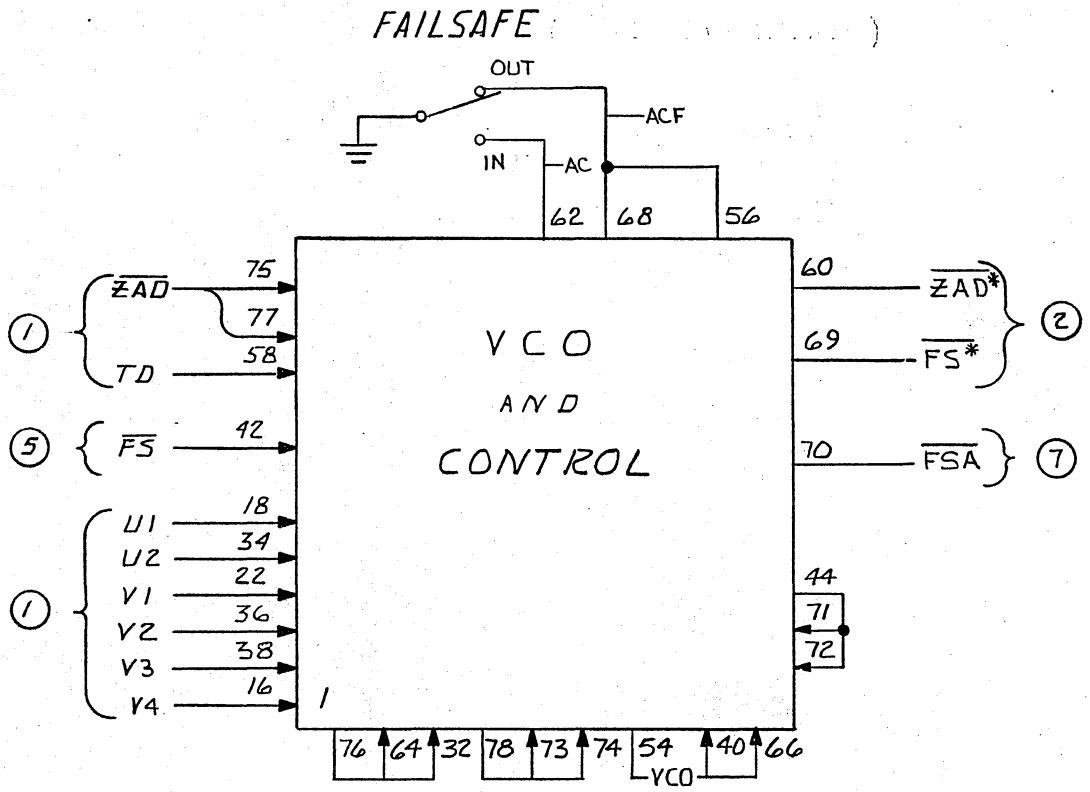
DWN MARTINEZ 6/20/72 | DES | CHK | ENGR HELMS 7/3/72 | SCALE NONE | FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 9210-8021 | SIZE | SHT 1 OF 1 | REV

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1		15622	VCO FAILSAFE
LOGIC LOCATION	PHYSICAL LOCATION	ASSY NO.	TITLE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

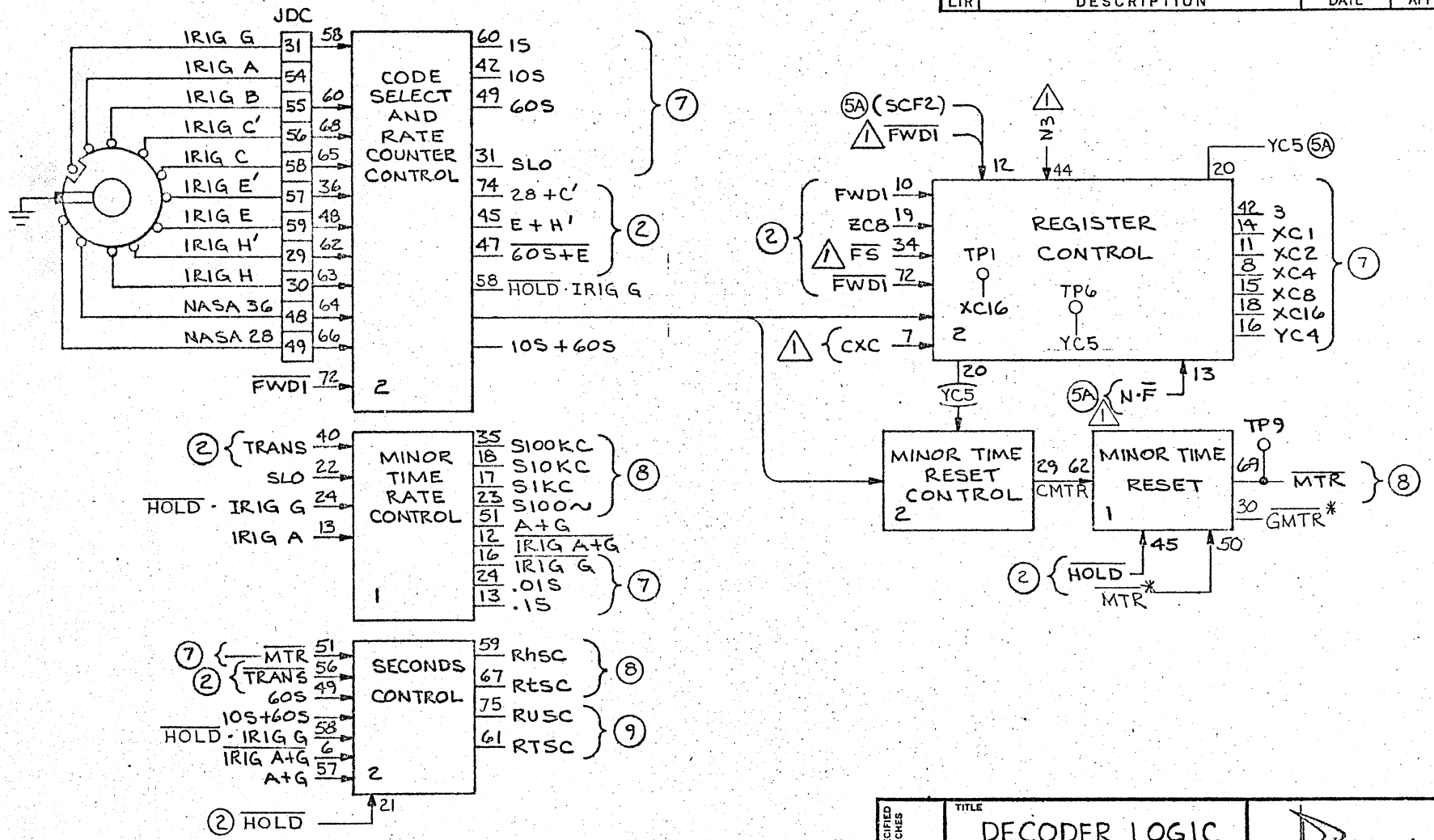
TITLE: AC FAILSAFE (4)

DWN	BENEDICT	6/21/11	DES		6-22
CHK		6-22	ENGR		6-22
SCALE	NONE		FSC	31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	SHT	OF	REV
B	9310-8096		

DIETZGEN 196 MG-10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

2		15788	DECODE#2
1		15673	DECODE#1
LOGIC LOCATION	PHYSICAL LOCATION	ASSY. NO.	TITLE

NOTES:

1. COMES FROM NASA DECODER IF USED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE

DECODER LOGIC CONTROL

5

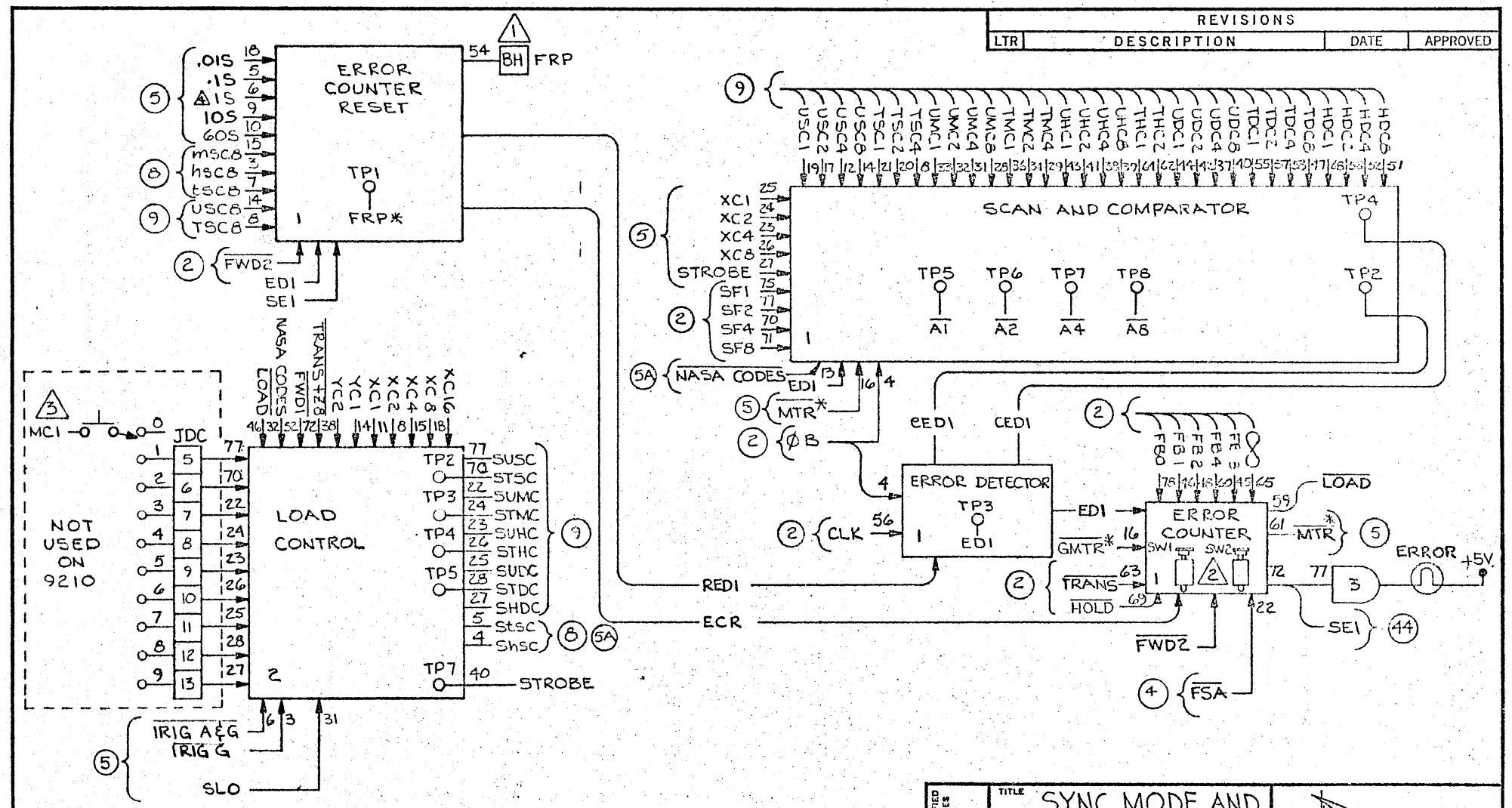
DWN	KAIN	4/7/72	DES		
CHK			ENGR	HELMS	4/12/72
SCALE	NONE		FSC	31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

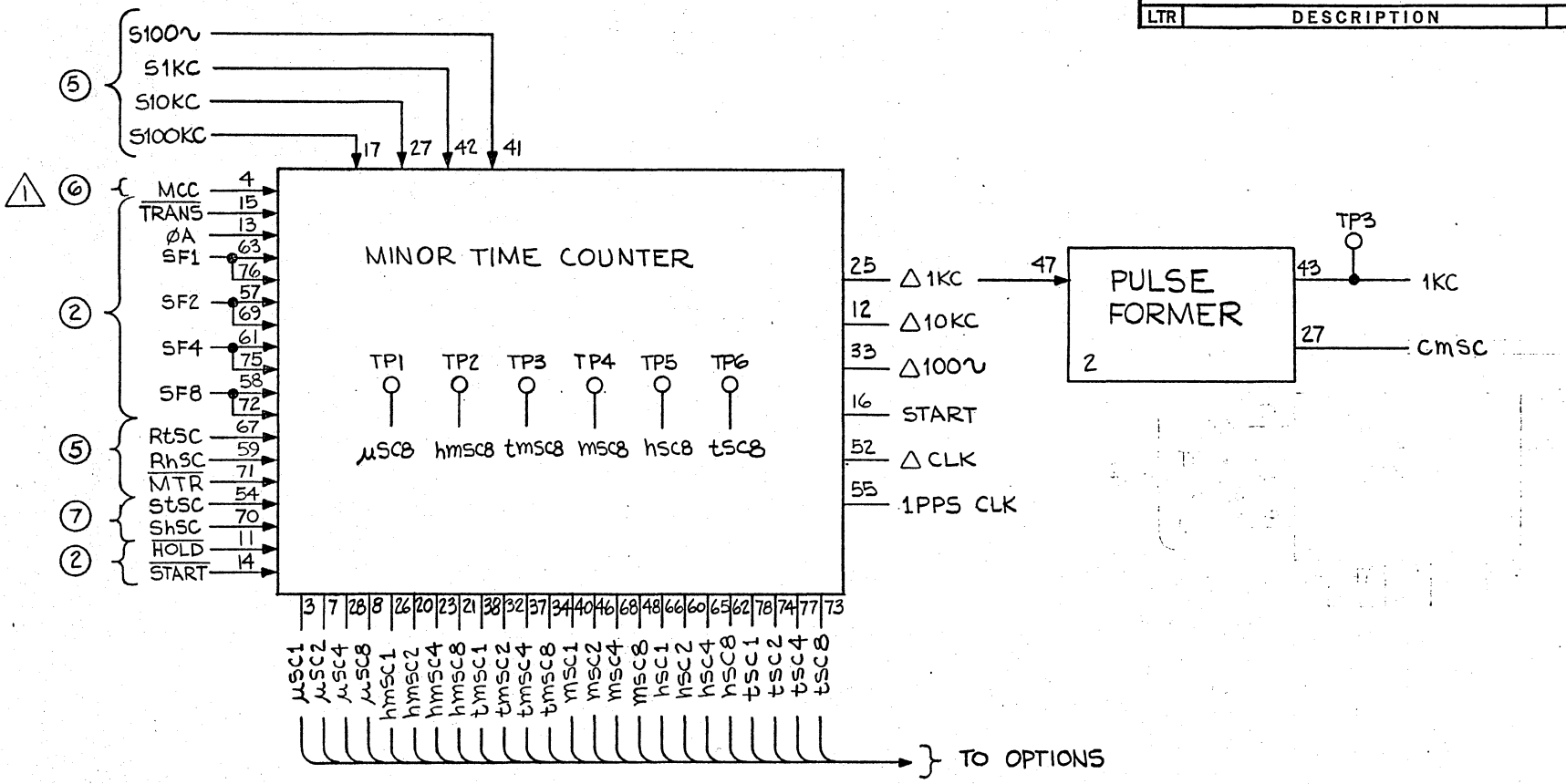
SIZE	SHT	OF	REV
B	1	1	

9310-8112

DIETZGEN 196 M0-10


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
ERROR COUNTER RESET
TP1
FRP*
FRP
BH
.01S
.1S
1S
10S
60S
mSC8
hSC8
tSC8
USC8
TSC8
FWD2
EDI
SE1
SCAN AND COMPARATOR
TP4
TP2
TP5
TP6
TP7
TP8
A1
A2
A4
A8
XC1
XC2
XC4
XC8
STROBE
SF1
SF2
SF4
SF8
NASA CODES
MTR*
ØB
CLK
NASA CODES LOAD
FWD1
TRANS+Z8
YC2
YC1
XC1
XC2
XC4
XC 8
XC16
IMC1
JDC
NOT USED ON 9210
LOAD CONTROL
TP2
SUSC
ST5C
TP3
SUMC
STMC
TP4
SUHC
STHC
TP5
SUDC
STDC
SHDC
Stsc
Shsc
TP7
STROBE
IRIG A&G
IRIG G
SLO
ERROR DETECTOR
TP3
EDI
CEDI
EEDI
REDI
ECR
GMTR*
ERROR COUNTER
SW1
SW2
LOAD
MTR*
TRANS
HOLD
FWD2
SE1
FSA
ERROR
+5V
NOTES:
4. COMES FROM NASA DECODER IF USED
3. GND IF ADV/RET NOT USED.
2. SW1 FOR NORMAL MINOR TIME SYNC.
1. SEE TOP ASSY FOR CONN. NO.
3 JDS 15666 DISPLAY
2 15788 DECODE NO.2
1 15675 SYNC MODE
LOGIC LOCATION
PHYSICAL LOCATION
ASSY. NO.
TITLE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°
TITLE
7 SYNC MODE AND LOAD COUNTER LOGIC
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN MARTINEZ 3/5/71
CHK 3/5
DES 3/5
ENGR 3/5
SCALE NONE
FSC 31160
B
9310-8111
SIZE
SHT 1 OF 1
REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTE:
1. ORIGINATES ON ③ IF ADV/RET OPTION INSTALLED

LOGIC LOCATION	PHYSICAL LOCATION	ASSY. NO.	TITLE
2		15664	MAJOR TIME CTR
1		15662	MINOR TIME CTR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE
MINOR TIME COUNTER
⑧

DWN MILES	3/2/71	DES	3/2
CHK	3/2	ENGR	3/2
SCALE NONE		FSC 31160	

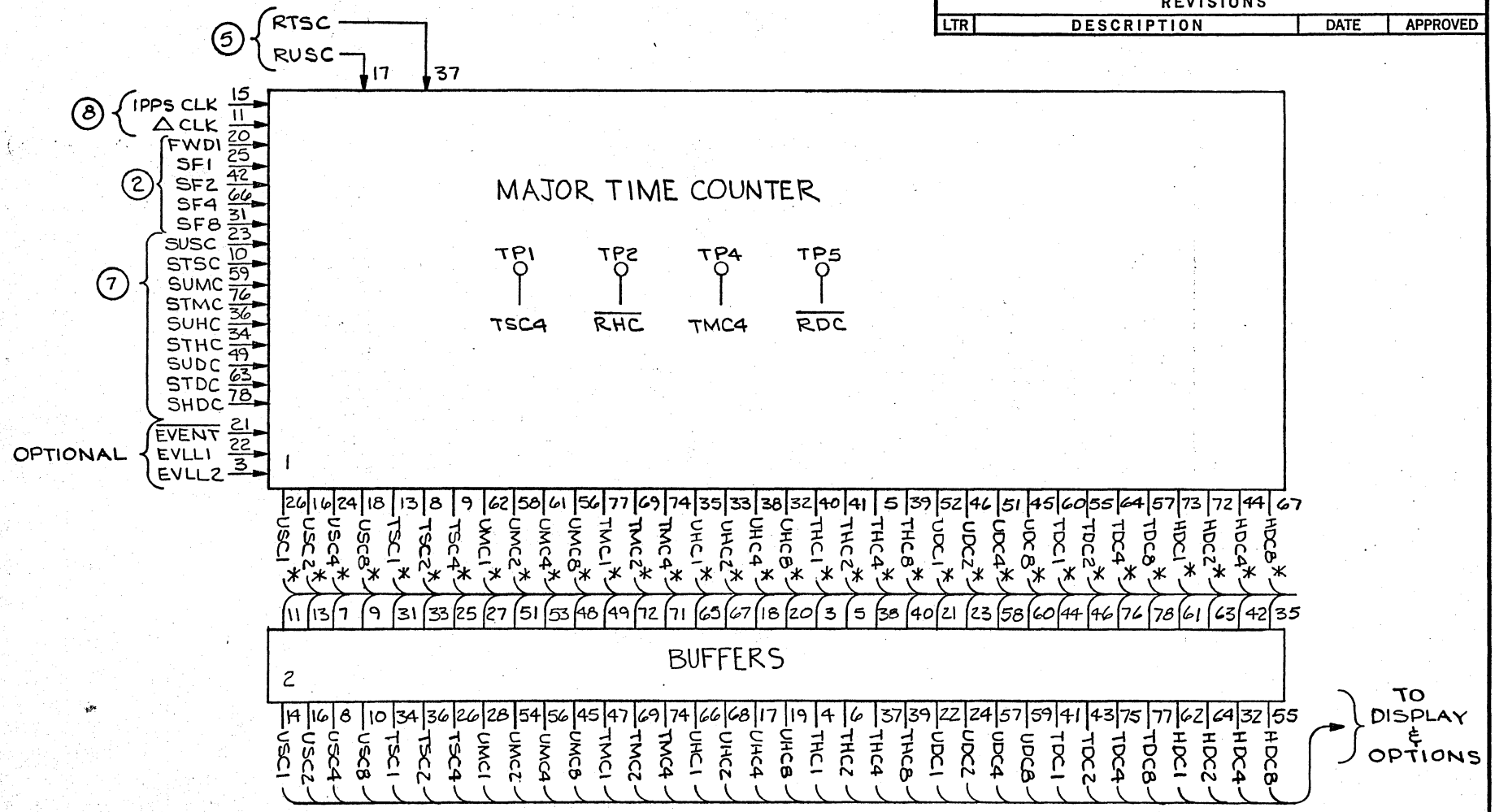
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 9310-8077 | REV

SIZE | SHT 1 OF 1

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



LOGIC LOCATION	PHYSICAL LOCATION	ASSY. NO.	TITLE
2		15663	36 BIT BUFFER
1		15664	MAJOR TIME COUNTER

NOTES:
1. COMES FROM MC1 WHEN MANUAL SYNC USED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE
9 MAJOR TIME COUNTER

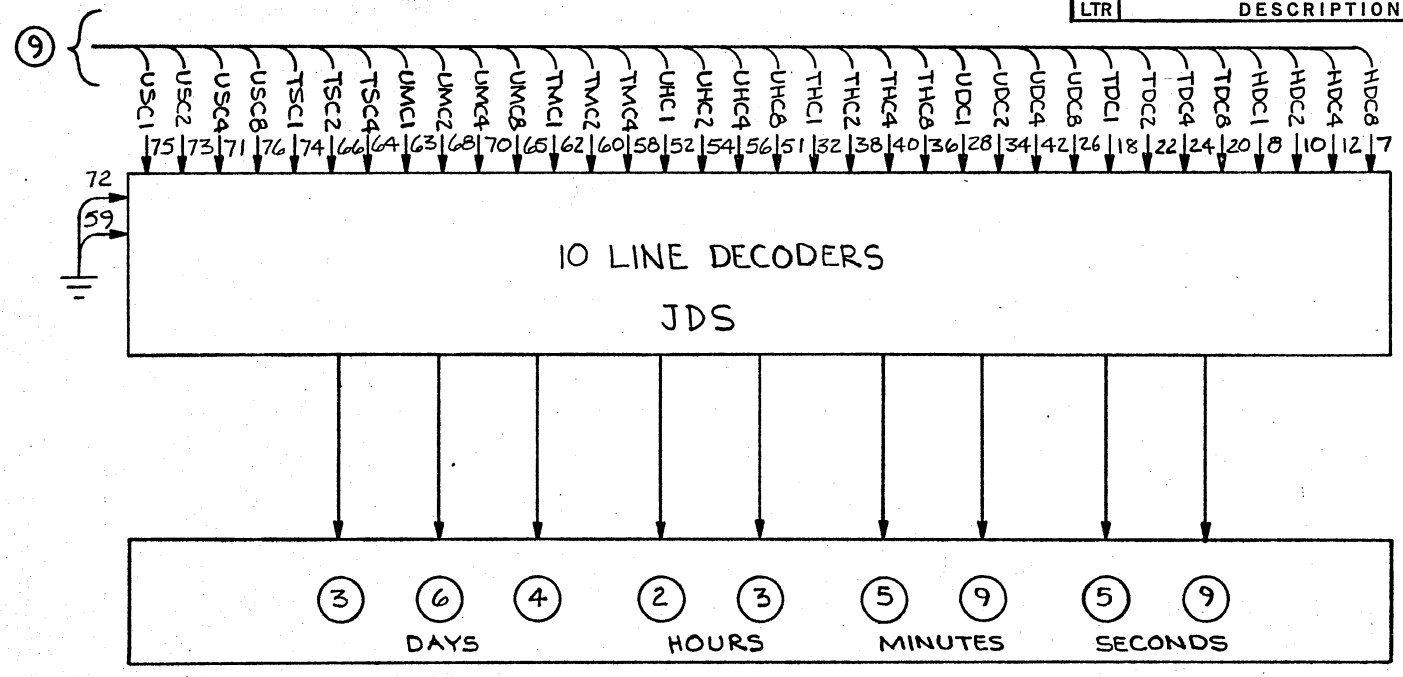
DWN MARTINEZ	3/3/71	DES		3/3
CHK	3/3	ENGR		3/3
SCALE NONE		FSC 31160		

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE		SHT 1 OF 1	REV
B	9310-8078		

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



JDS LOGIC LOCATION	JDS PHYSICAL LOCATION	15666 ASSY. NO.	FRONT PNL. DISPLAY TITLE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

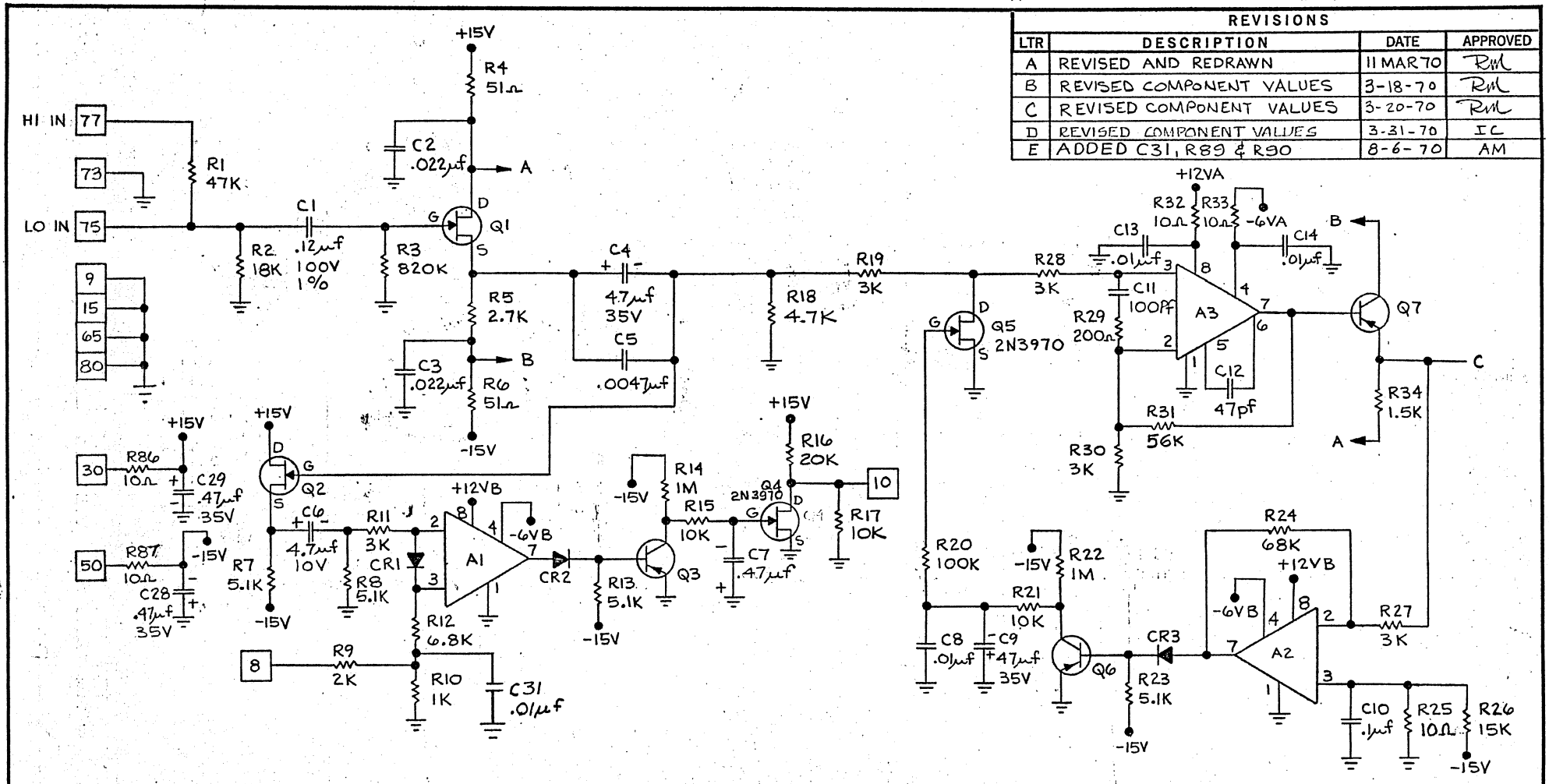
TITLE
DISPLAY LOGIC
(10)

DWN	MARTINEZ	2/26/11	DES	LR	2/26
CHK	LR	2/26	ENGR	LR	2/26
SCALE	NONE		FSC	31160	

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE		SHT		OF		REV
B	9310-8079	1		1		

DIETZGEN 196 MQ-10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REVISED AND REDRAWN	11 MAR 70	RML
B	REVISED COMPONENT VALUES	3-18-70	RML
C	REVISED COMPONENT VALUES	3-20-70	RML
D	REVISED COMPONENT VALUES	3-31-70	IC
E	ADDED C31, R89 & R90	8-6-70	AM

PART NO.	MFR	COMPONENT
710CE	AMELCO	A1, 2, 4, 5, 7
µ5B710239	FAIRCHILD	A3, 6
U1487E	AMELCO	Q1, 2, 4, 9, 8, 12, 15, 16

3. ALL DIODES ARE IN914A.

2. ALL FIELD EFFECT TRANSISTORS ARE U1487E.

1. ALL TRANSISTORS ARE 2N3645.

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: AGC AMPLIFIER

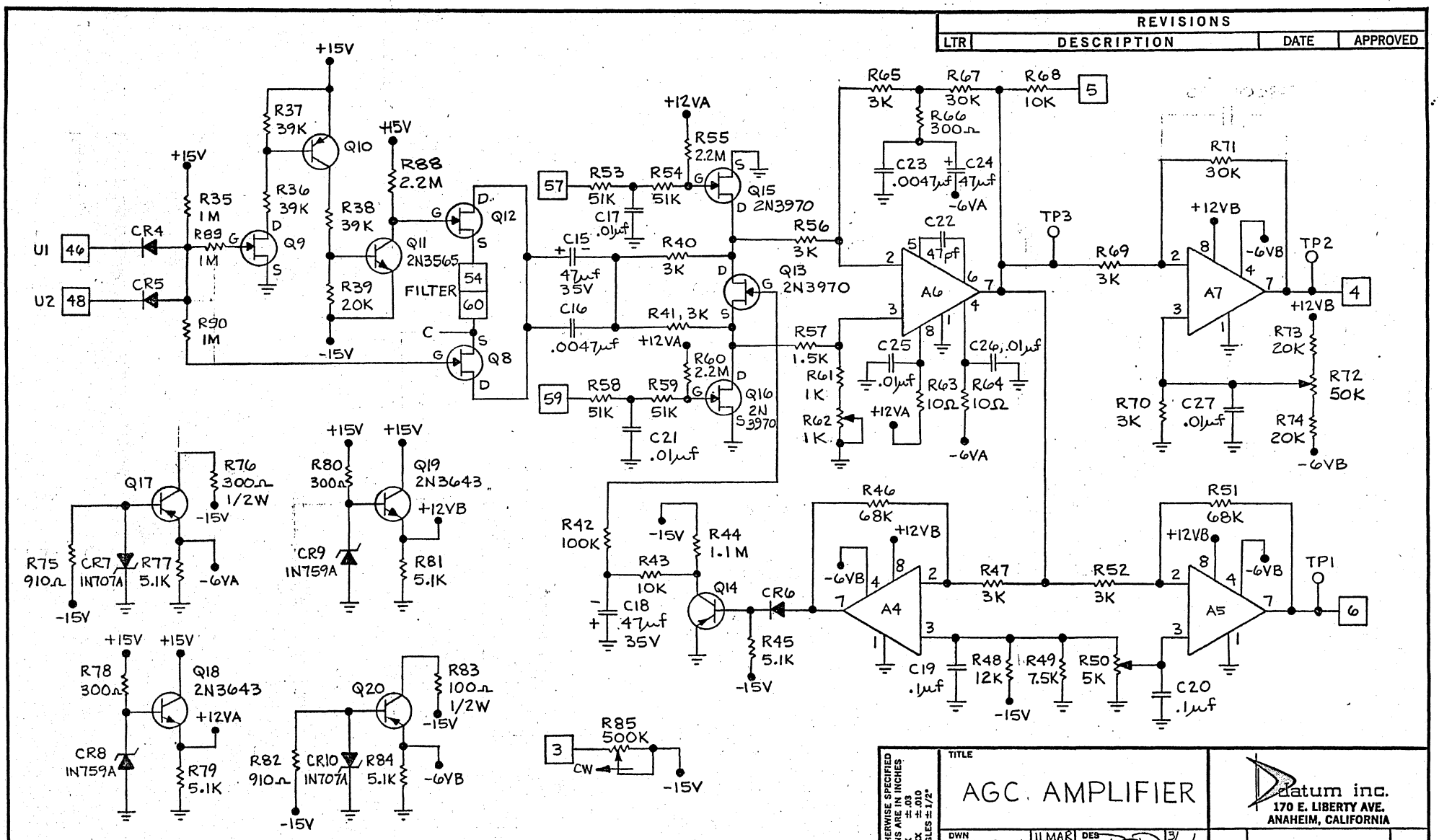
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

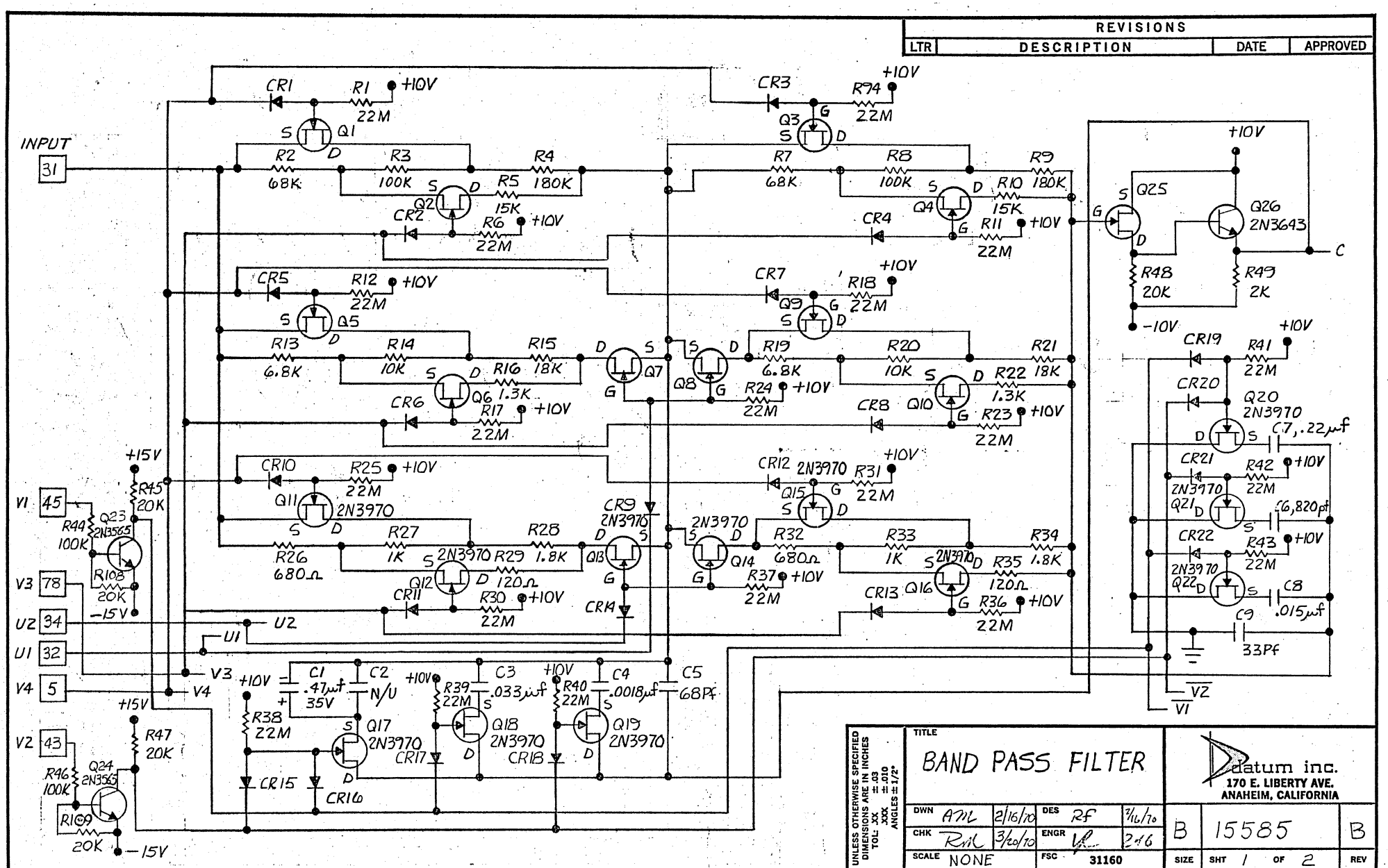
DWN	J. GILLBANK	11MAR 1970	DES	ROD	3/10/70
CHK	RML	3/19/70	ENGR		3/10
SCALE	NONE		FSC	31160	

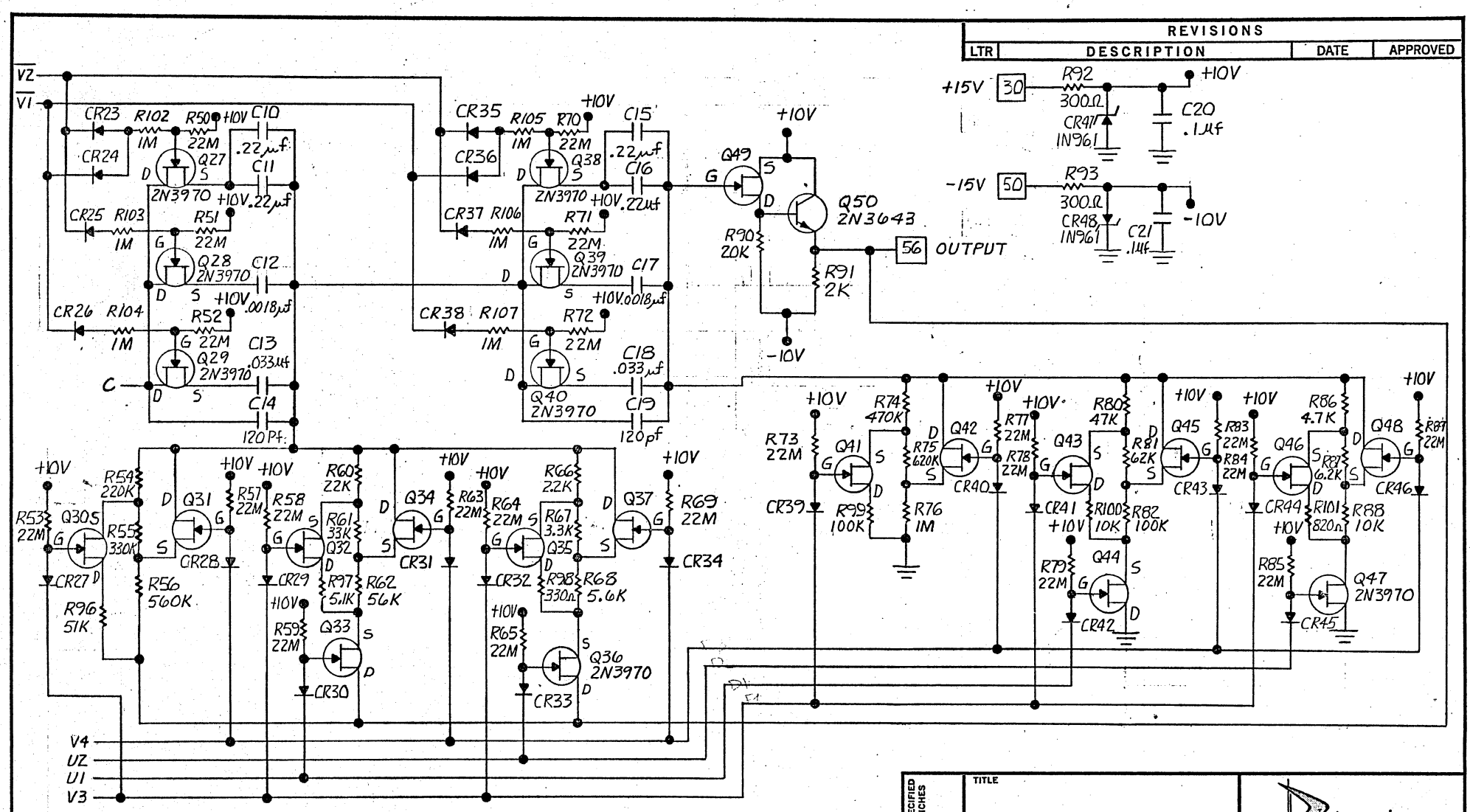
B | 15584 | E

SIZE | SHT 1 OF 2 | REV

DIETZGEN 196MG-10


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
+15V
R37 39K
Q10
R36 39K
R38 39K
R39 20K
R88 2.2M
Q11 2N3565
Q12
R35 1M
R89 1M
Q9
CR4
CR5
U1
46
U2
48
R90 1M
-15V
FILTER
54
60
C
Q8
+12VA
R55 2.2M
Q15 2N3970
57
R53 51K
R54 51K
C17 .01µf
C15 47µf 35V
C16 .0047µf
R40 3K
R41, 3K
R56 3K
Q13 2N3970
59
R58 51K
R59 51K
C21 .01µf
R60 2.2M
Q16 2N3970
R57 1.5K
R61 1K
R62 1K
C25 .01µf
R63 10Ω
R64 10Ω
C26, .01µf
+12VA
-6VA
R65 3K
R67 30K
R68 10K
5
R66 300Ω
C23 .0047µf
C24 47µf
-6VA
C22 47pf
A6
TP3
R69 3K
R71 30K
+12VB
-6VB
TP2
A7
4
+12VB
R73 20K
R72 50K
R74 20K
R70 3K
C27 .01µf
-6VB
Q17
R76 300Ω 1/2W
-15V
R75 910Ω
CR7 IN707A
R77 5.1K
-6VA
+15V
R80 300Ω
Q19 2N3643
+12VB
CR9 IN759A
R81 5.1K
R42 100K
R44 1.1M
R43 10K
C18 47µf 35V
Q14
CR6
R45 5.1K
R46 68K
+12VB
-6VB
A4
R47 3K
R52 3K
R51 68K
A5
TP1
6
C19 .1µf
R48 12K
R49 7.5K
R50 5K
C20 .1µf
Q18 2N3643
R78 300Ω
+12VA
CR8 IN759A
R79 5.1K
Q20
R83 100Ω 1/2W
R82 910Ω
CR10 IN707A
R84 5.1K
-6VB
3
R85 500K
CW
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ±.03
XXX ±.010
ANGLES ±1/2°
TITLE
AGC AMPLIFIER
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN J. GILLBANK 11 MAR 1970
DES 3/10/70
CHK 3/19/70
ENGR 3/10
SCALE NONE
FSC 31160
B
15584
E
SIZE
SHT 2 OF 2
REV
DIETZGEN 196MG-10


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
INPUT
31
CR1
R1
+10V
22M
Q1
R2
68K
R3
100K
R4
R5
180K
15K
Q2
CR2
R6
22M
CR3
R74
22M
Q3
R7
68K
R8
100K
R9
R10
180K
15K
Q4
CR4
R11
22M
CR5
R12
22M
Q5
R13
6.8K
R14
10K
R15
R16
18K
1.3K
Q6
CR6
R17
22M
Q7
CR7
R18
22M
Q9
R19
6.8K
Q8
R24
22M
R20
10K
R21
R22
18K
1.3K
Q10
CR8
R23
22M
+15V
R45
20K
V1
45
R44
100K
Q23
2N3565
R108
20K
-15V
V3
78
U2
34
U1
32
V4
5
V2
43
R46
100K
Q24
2N3565
R109
20K
CR10
R25
22M
Q11
2N3970
R26
680Ω
R27
1K
R28
R29
1.8K
120Ω
2N3970
Q12
CR11
R30
22M
CR9
2N3970
Q13
CR14
CR12
2N3970
R31
22M
Q15
2N3970
Q14
R37
22M
R32
680Ω
R33
1K
R34
R35
1.8K
120Ω
2N3970
Q16
CR13
R36
22M
U2
U1
V3
V4
C1
.47μf
35V
C2
N/U
R38
22M
Q17
2N3970
CR15
CR16
C3
.033μf
R39
22M
Q18
2N3970
CR17
C4
.0018μf
R40
22M
Q19
2N3970
CR18
C5
68Pf
R47
20K
Q25
Q26
2N3643
R48
20K
R49
2K
C
-10V
CR19
R41
22M
CR20
Q20
2N3970
C7, .22μf
CR21
R42
22M
Q21
2N3970
C6, 820pf
CR22
R43
22M
Q22
2N3970
C8
.015μf
C9
33Pf
VZ
VI
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: XX ±.03
XXX ±.010
ANGLES ±1/2°
TITLE
BAND PASS FILTER
DWN AML 2/16/70
CHK RML 3/20/70
SCALE NONE
DES RF 3/16/70
ENGR VL 2-16
FSC 31160
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B
15585
B
SIZE
SHT 1 OF 2
REV
DIETZGEN 196MG-10



3. ALL RESISTORS ARE ¼ W CARBON, ± 5%
2. ALL FIELD EFFECT TRANSISTORS ARE AMELCO U1487E
1. ALL DIODES ARE IN914A
NOTE: UNLESS OTHERWISE SPECIFIED

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

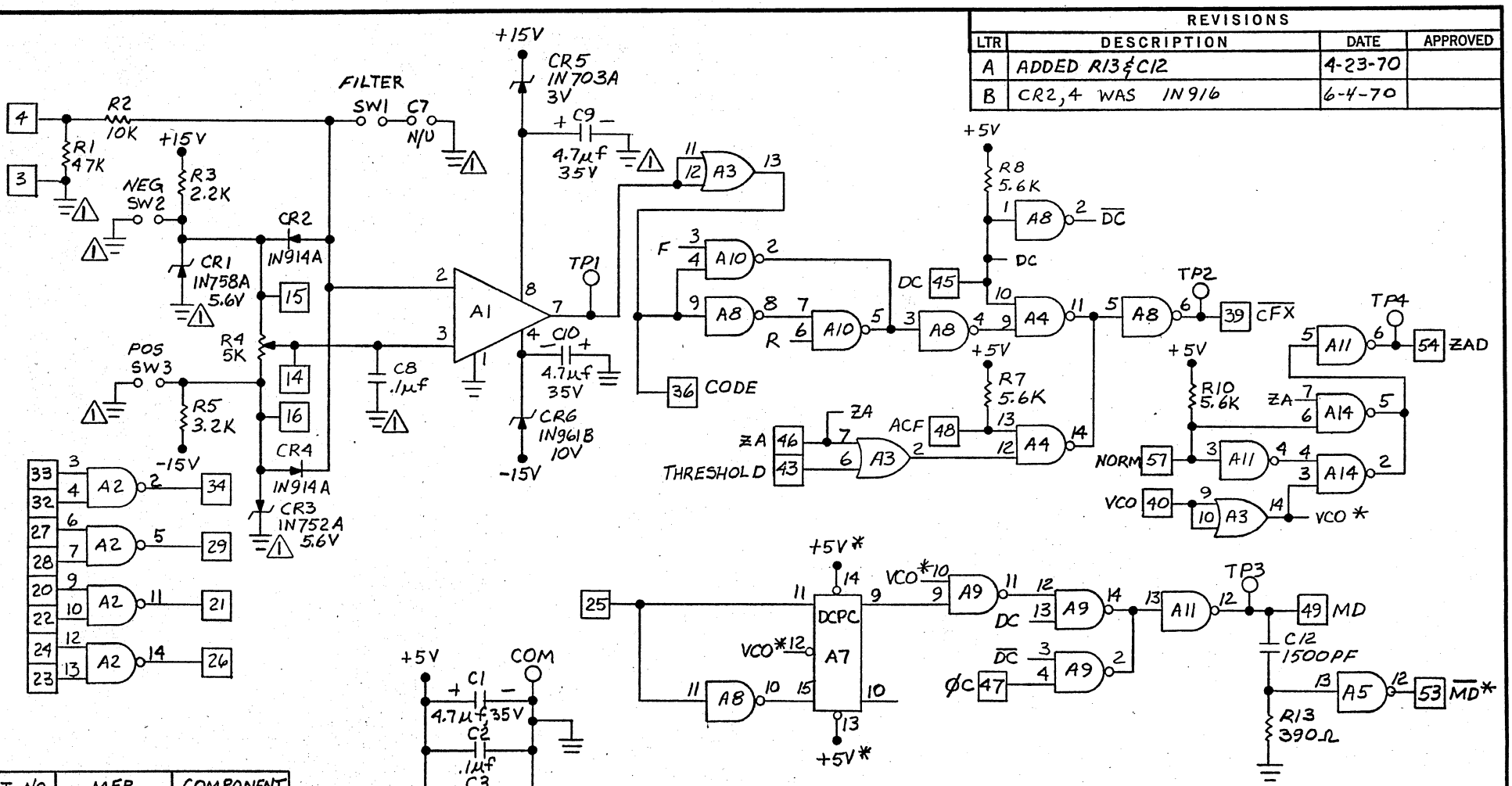
TITLE: BAND PASS FILTER

DWN ASKIER	2-17-0	DES RF	4/4/10	
CHK RM	3/10/10	ENGR	2-16	
SCALE NONE		FSC 31160		

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 15585 | B
SIZE | SHT 2 OF 2 | REV

DIETZGEN 196MG-10



PART NO.	MFR	COMPONENT
710CE	AMELCO	A1
SP384A	SIGNETICS	A3
SP387A	↕	A2,4,9,10,14
N8490A		A5,8,11
SP322B		A7,12
N8280A	SIGNETICS	A13

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: DC CODE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

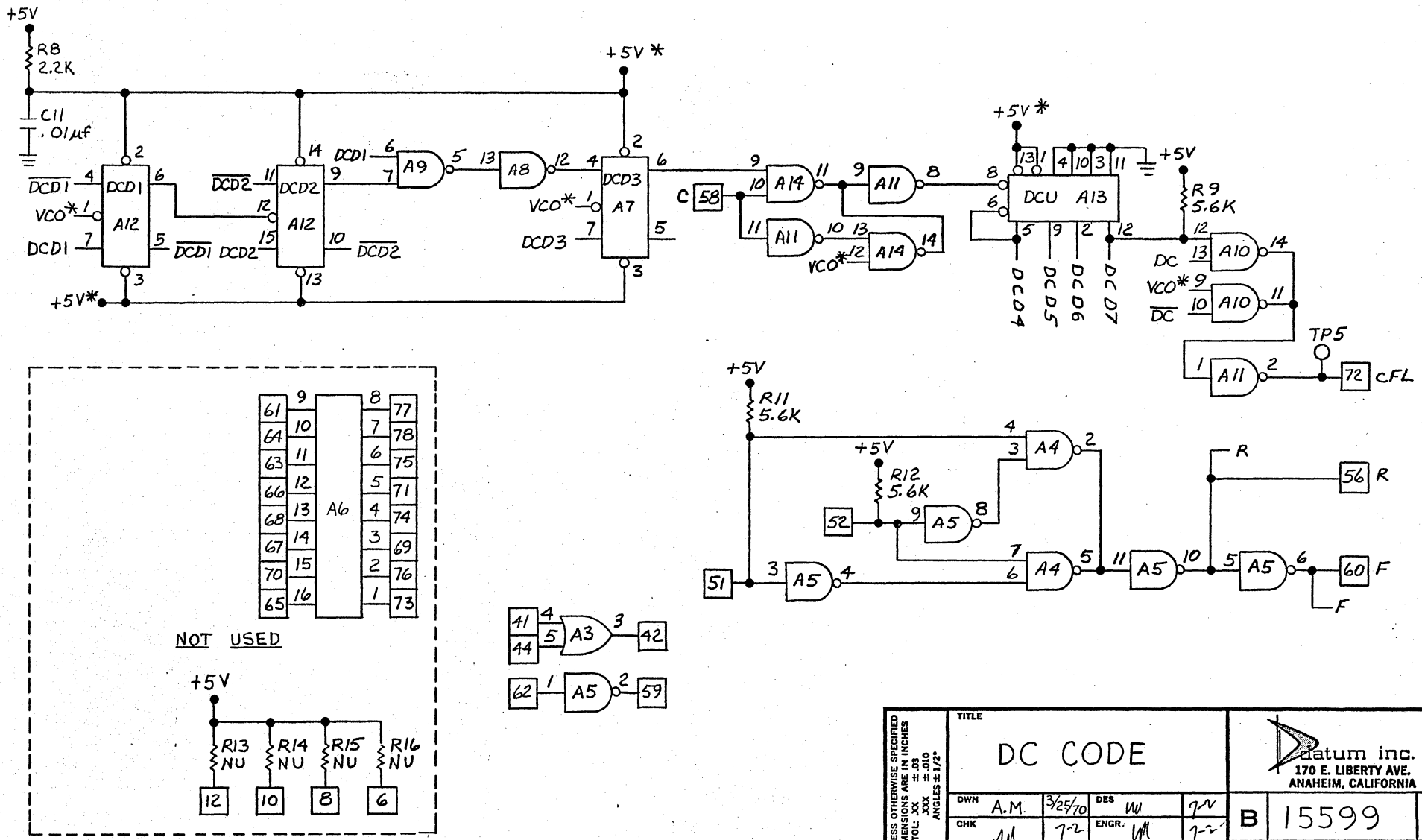
DWN	AM	3/25/70	DES		
CHK			ENGR		
SCALE	NONE		FSC	31160	

B | 15599 | B

SIZE | SHT 1 OF 2 | REV

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

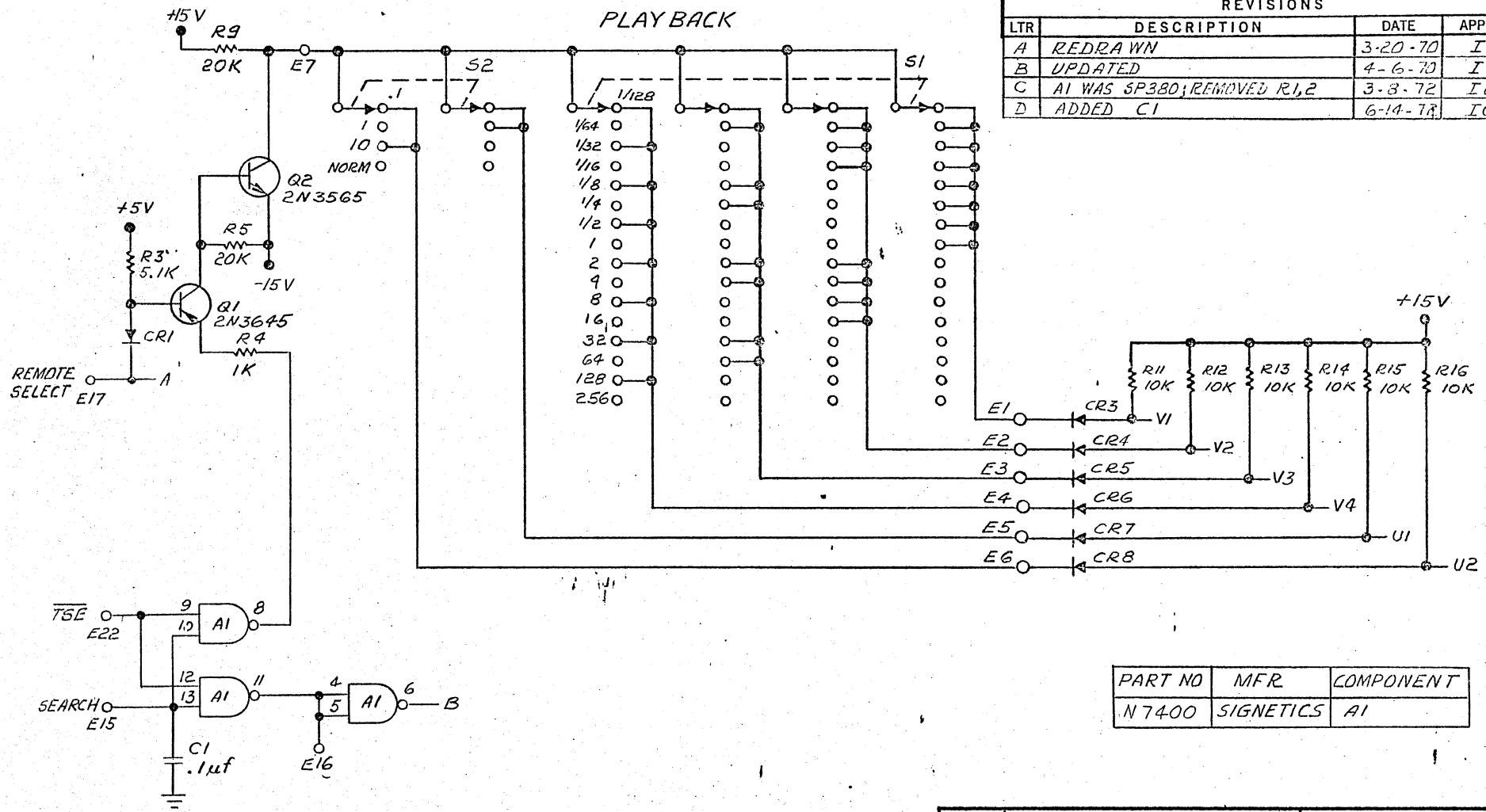
TITLE

DC CODE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	A.M.	3/25/70	DES	W	7-2
CHK		7-2	ENGR.		7-2
SCALE	NONE		FSC	31160	

SIZE		SHT		OF		REV
B	15599	2		2		B



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REDRAWN	3-20-70	I.C.
B	UPDATED	4-6-70	IC
C	A1 WAS SP380; REMOVED R1,2	3-8-72	IC
D	ADDED C1	6-14-72	IC

PART NO	MFR	COMPONENT
N7400	SIGNETICS	A1

1. ALL DIODES ARE IN914A

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: SWITCH FILTER CARD

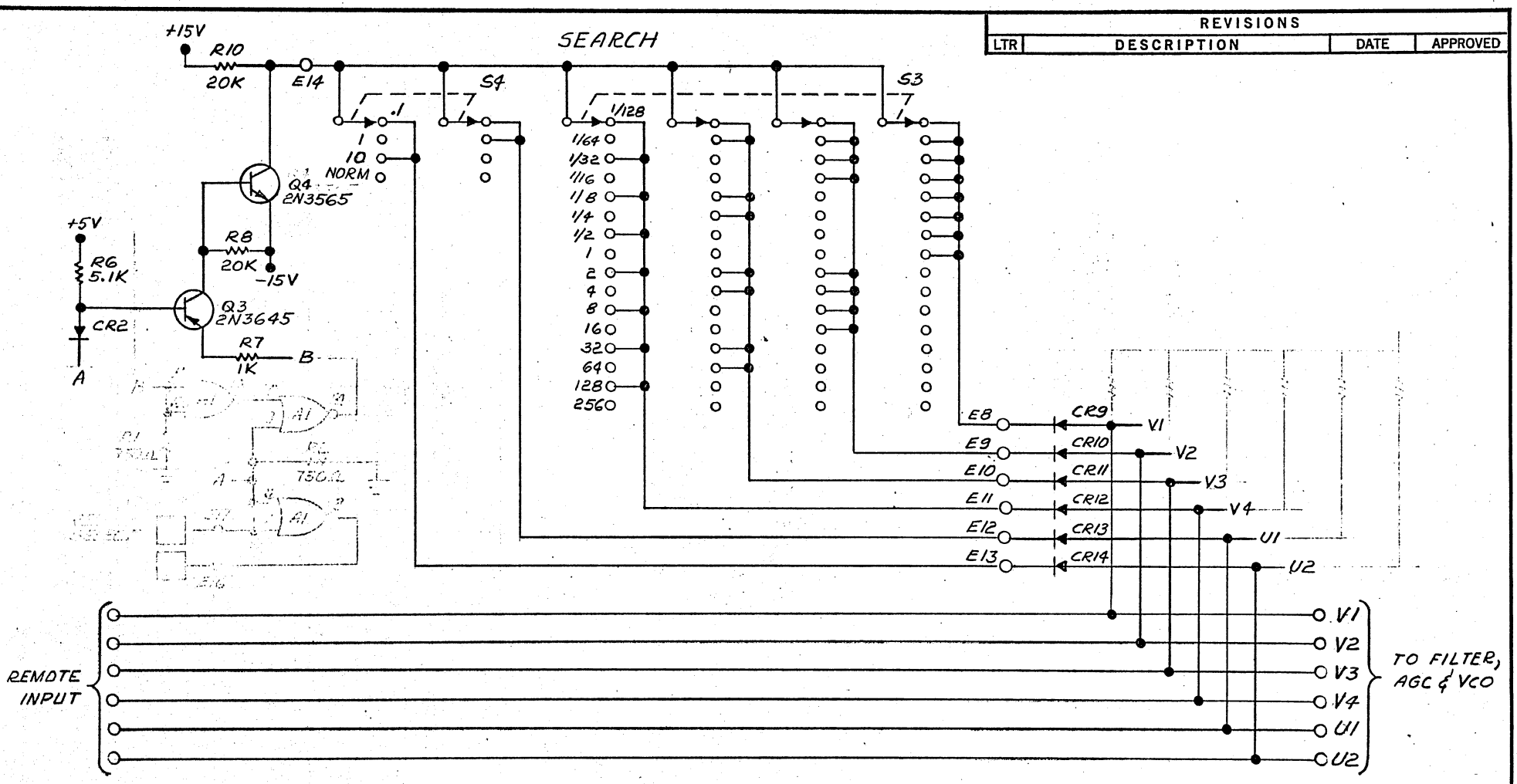
DWN	I.C.	3-20-70	DES	IC	A-7
CHK	RML	4/13/70	ENGR		A-7
SCALE	NONE		FSC	31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 15603 | D

SIZE | SHT 1 OF 2 | REV

DIETZGEN 196MQ-10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE

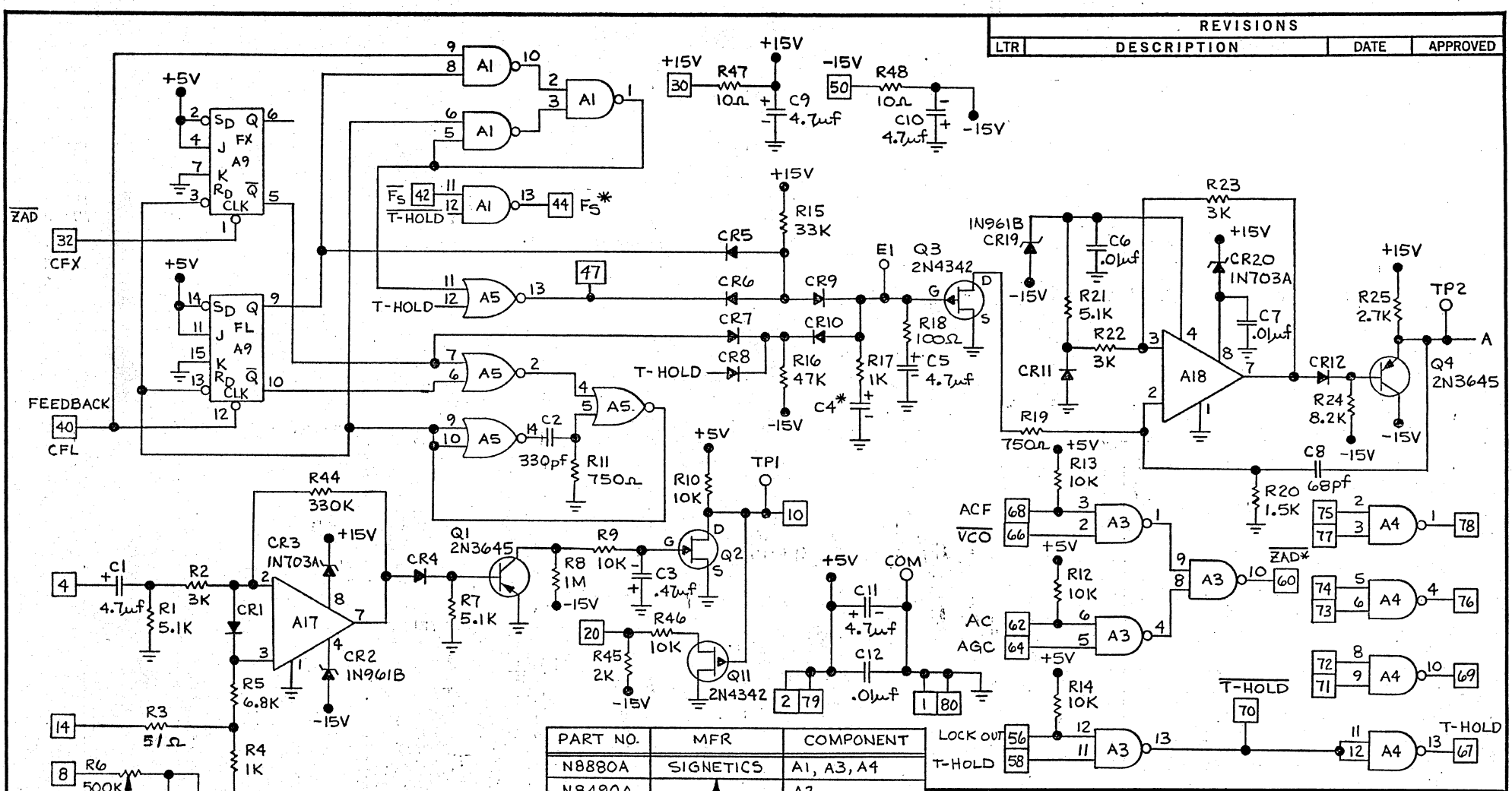
SWITCH FILTER CARD

DWN	I.C.	3-20-0	DES	IC	4-7
CHK	RM	4/1/70	ENGR	MC	4-7
SCALE	NONE		FSC	31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE		REV
B	15603	D
	SHT 2 OF 2	

DIETZGEN 196MG-10



PART NO.	MFR	COMPONENT
N8880A	SIGNETICS	A1, A3, A4
N8490A	↑	A2
SP380A		A5
SP322B		A6, A9, A10
N8881A		A7, A11, A13
N8291A	↓	A8, A12, A16
N8290A	SIGNETICS	A14, A15
710CE	AMELCO	A17, A18

3. "*" INDICATES SELECTED FOR LOW LEAKAGE
2. ALL TRANSISTORS ARE AMELCO U1487E.
1. ALL DIODES ARE IN914A.

NOTE: UNLESS OTHERWISE SPECIFIED

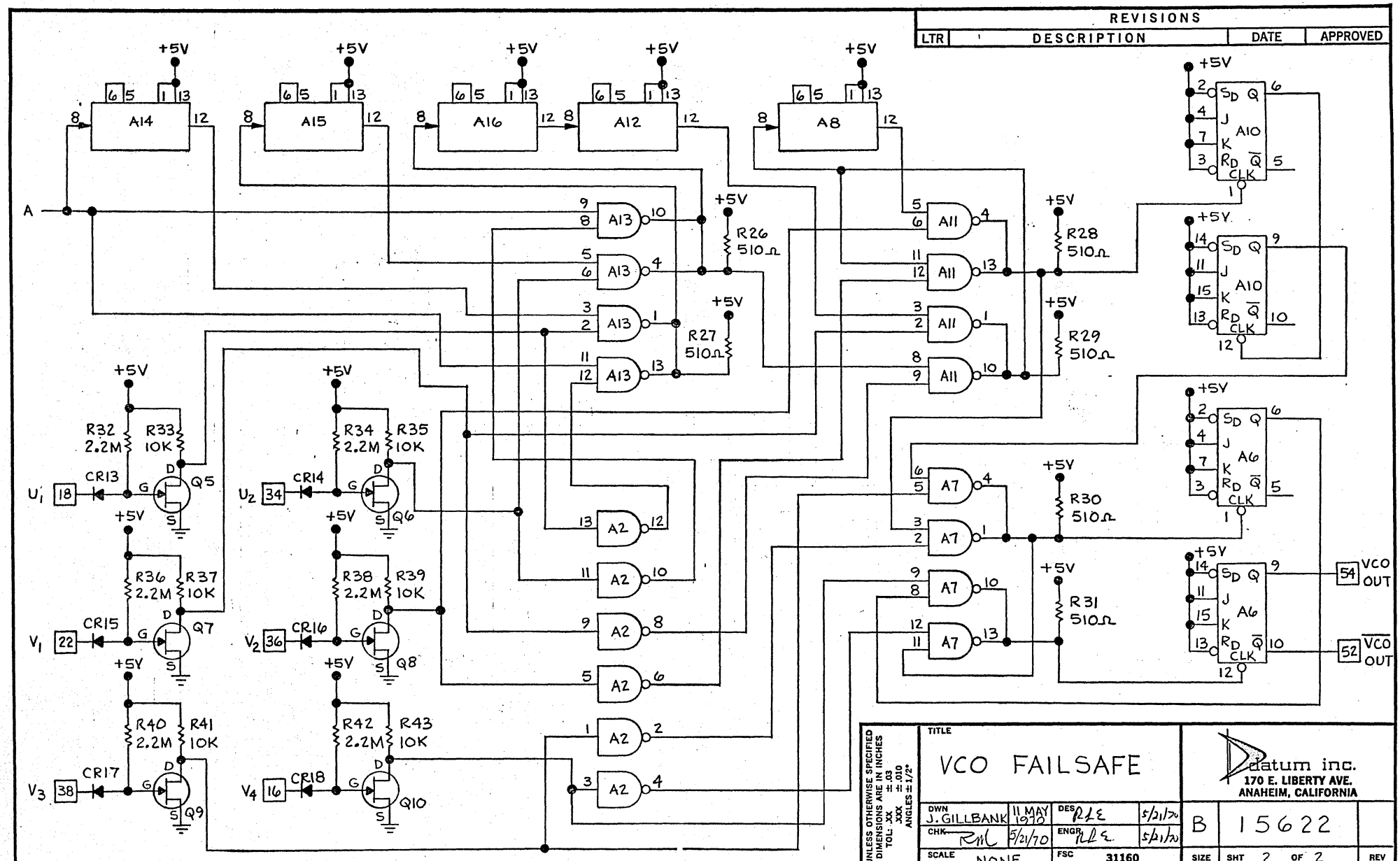
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: VCO FAILSAFE

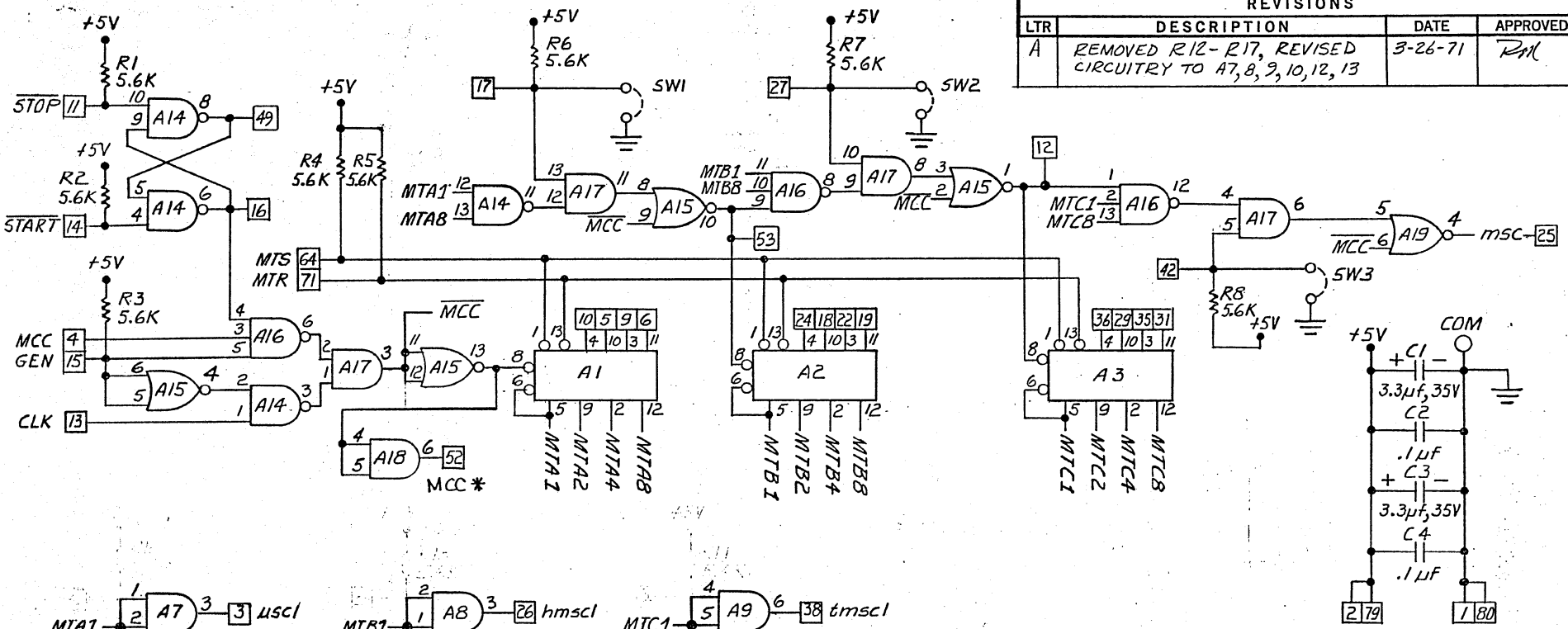
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

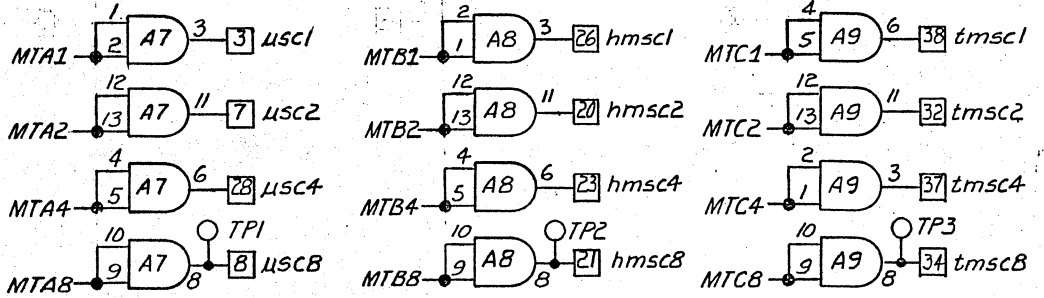
DWN J. GILLBANK	11 MAY 1970	DES RLE	5/21/70	B	15622
CHK RM	5/21/70	ENGR RLE	5/21/70		
SCALE NONE		FSC 31160		SIZE	SHT 1 OF 2 REV

DIETZGEN 196 MG-10



DIETZGEN 196 MG-10





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REMOVED R12-R17, REVISED CIRCUITRY TO A7, 8, 9, 10, 12, 13	3-26-71	RM

PART NO	MFR	ALTERNATE	REF. DES.
N7408A	NATIONAL		A7-10,12,13,17,18
N7402A	NATIONAL		A15, 19
N7400A	NATIONAL		A14
N7410A	NATIONAL	N8H70	A11, 16
N8280A	SIGNETICS	74196	A1-6

VOLTAGE	+23	+15	+5	-15
W C CURRENT	0	0	575 ma	0
TYPICAL	0	0	325ma	0

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

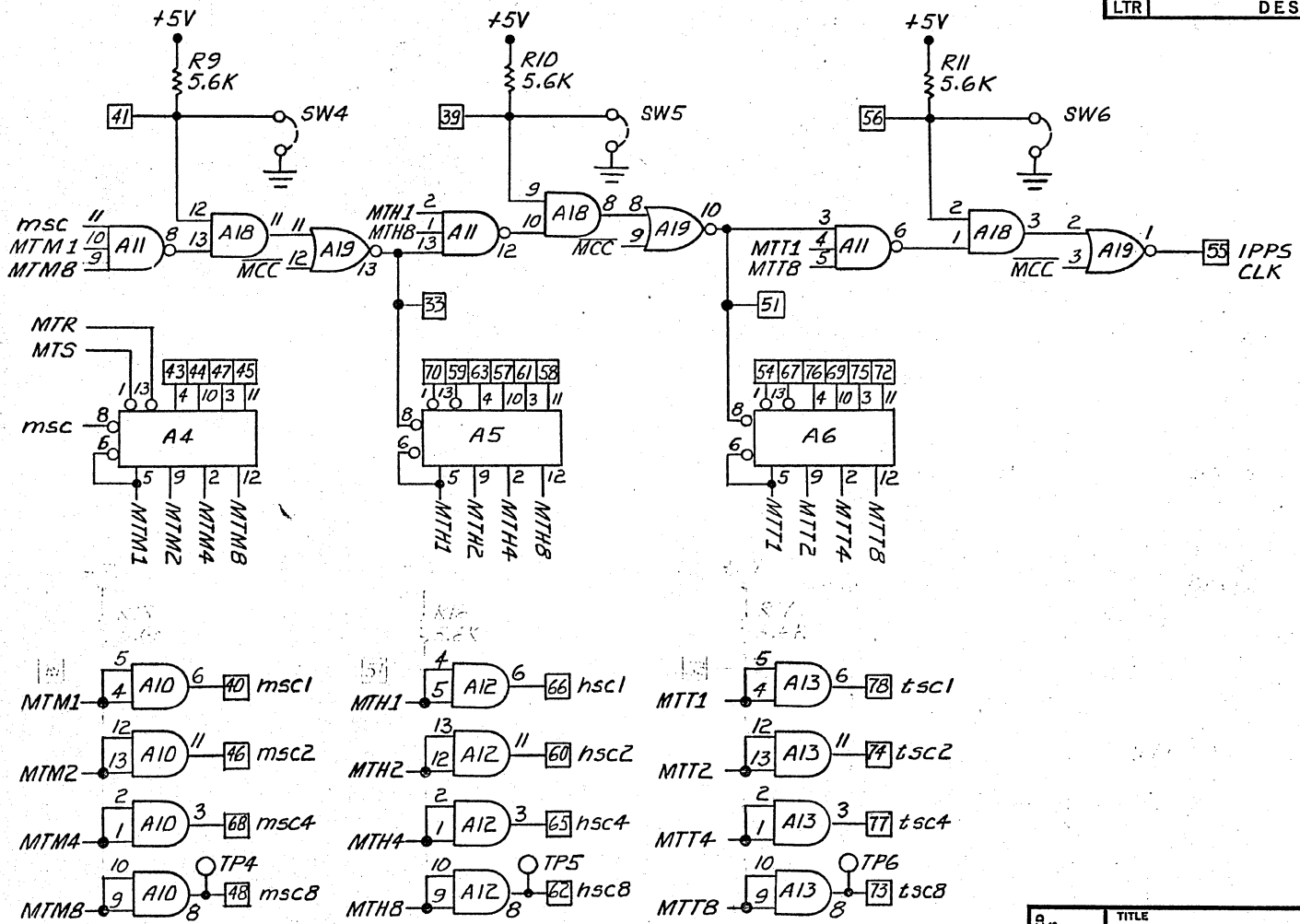
TITLE: MINOR TIME COUNTER

DWN IC	12/9/70	DES IC	12/9/70	B	15662 A
CHK RM	12/11/70	ENGR VR	12-29-70		
SCALE NONE		FSC 31160		SIZE	SHT 1 OF 2 REV

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

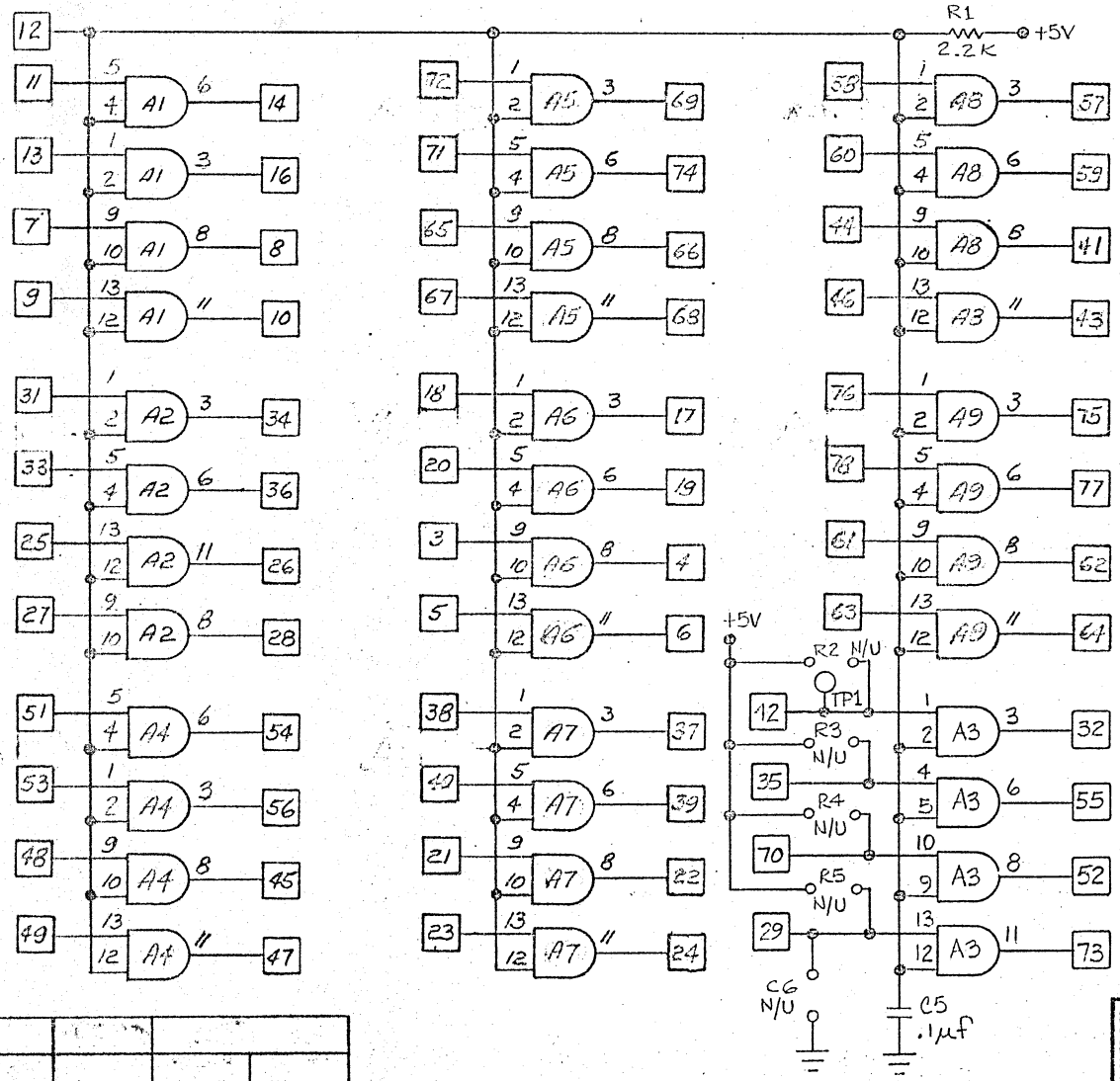
DIETZGEN 196 MG-10

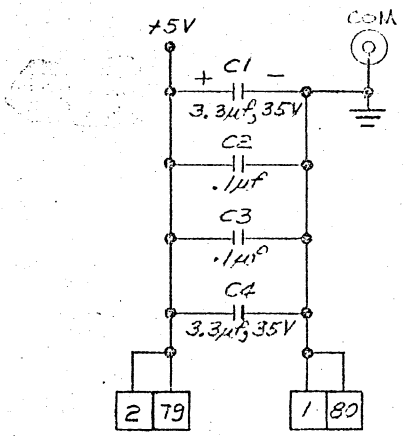
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°	TITLE: MINOR TIME COUNTER			datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
	DWN IC 12/9/70	DES IC 12/9/70	B	15662	A
	CHK RM 12/11/70	ENGR [illegible] 12-29-70			
	SCALE NONE	FSC 31160	SIZE	SHT 2 OF 2	REV

DIETZGEN 196 MG-10





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

INPUTS	OUTPUTS	
SPECIFICATIONS		

USN7408	SPRAGUE	A1-A9
PART NO.	MFR.	COMPONENT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

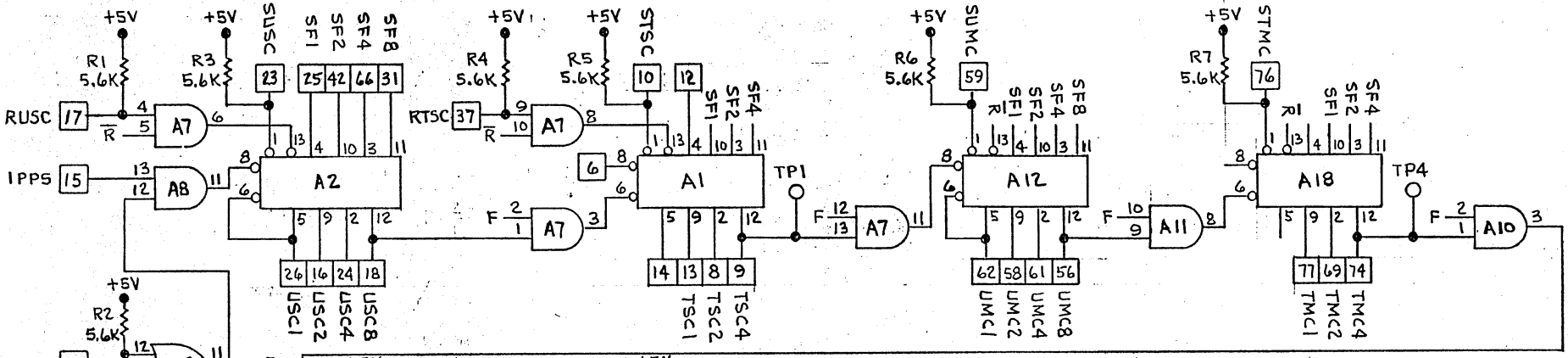
TITLE
36 BIT BUFFER

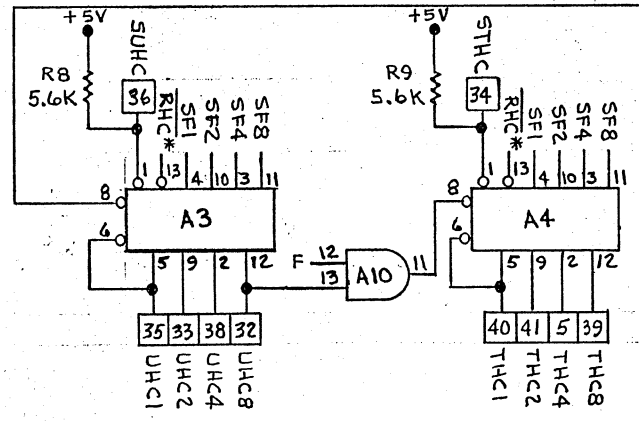
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

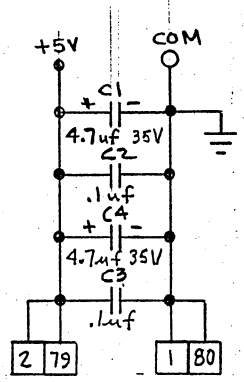
DWN MILES		DES			B	15663	
CHK		ENGR		12-17			
SCALE NONE		FSC 31160			SIZE	SHT 1 OF 1	REV

DIETZGEN 196MO-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	A16-3 WAS $\overline{\text{EVENT}}$, A16-12 WAS CONNECTED TO A17-2	4-16-71	RM







PART NO	MFR	COMPONENT
N7400A	SIGNETICS	A14
N7408A	↕	A7,8,10,11
N7411A		A16
N7432A		A15
N8280A	↕	A2-6,12,13
N8288A	SIGNETICS	A1,18
SN74123	T.I.	A9,17

TYPICAL	0	0	500	0
W/C CURRENT	0	0	675 ma	0
VOLTAGE	+20V	+15V	+5V	-15V.

⚠1 FOR COMPONENT VALUES OF 15664-1 ASSY., SEE TABLE 1, SHEET 2 OF 2

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: MAJOR TIME COUNTER

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DATE	DES	DATE
R. Hoac	12-29-70	LM	12-29
CHK	12-29	ENGR	12-29
SCALE NONE		FSC 31160	

B | 15664 ⚠1 | A

SIZE | SHT 1 OF 2 | REV

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

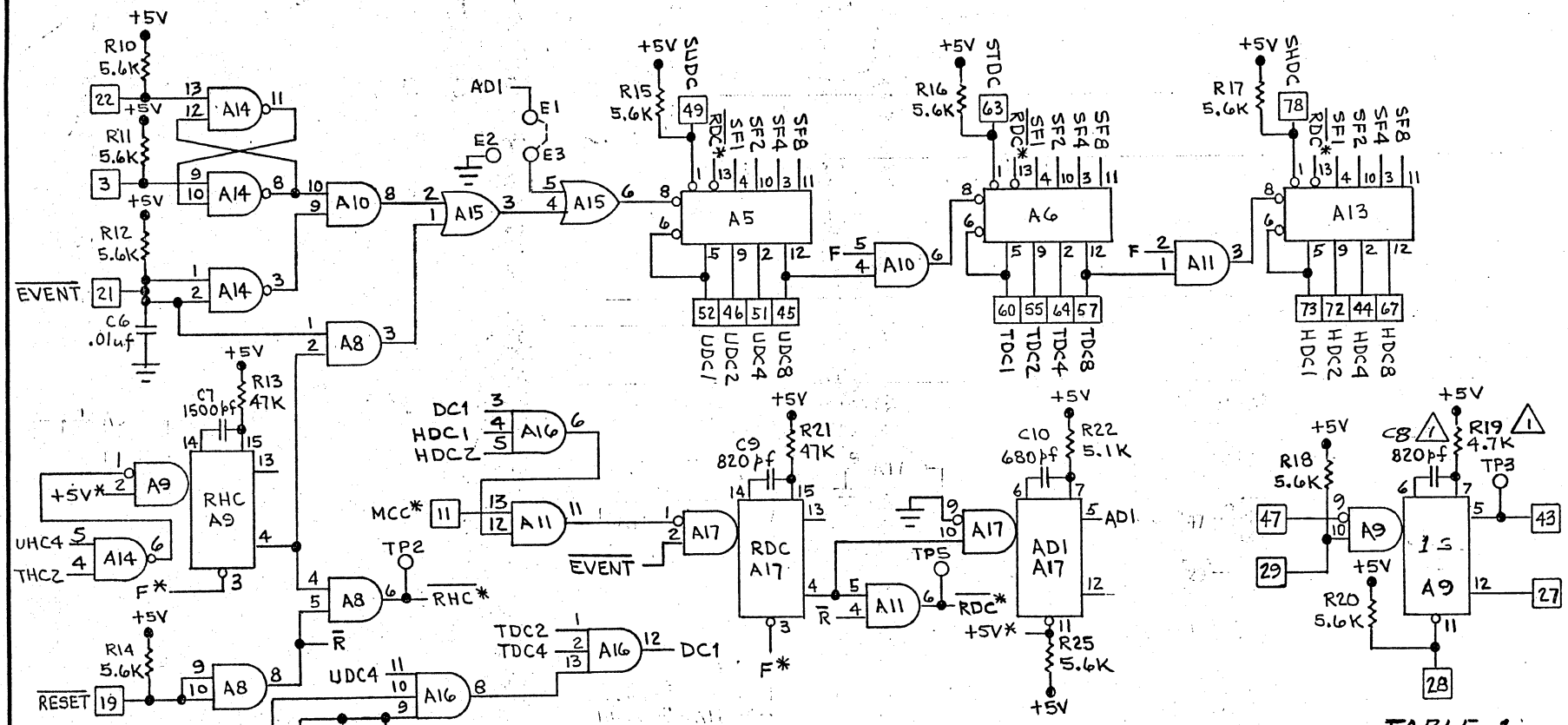


TABLE 1

ASSY	REFERENCE DESG.	VALUE
-1	R19	12K 1/4W 5%
	C8	3.4 uf @ 6V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: MAJOR TIME COUNTER

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

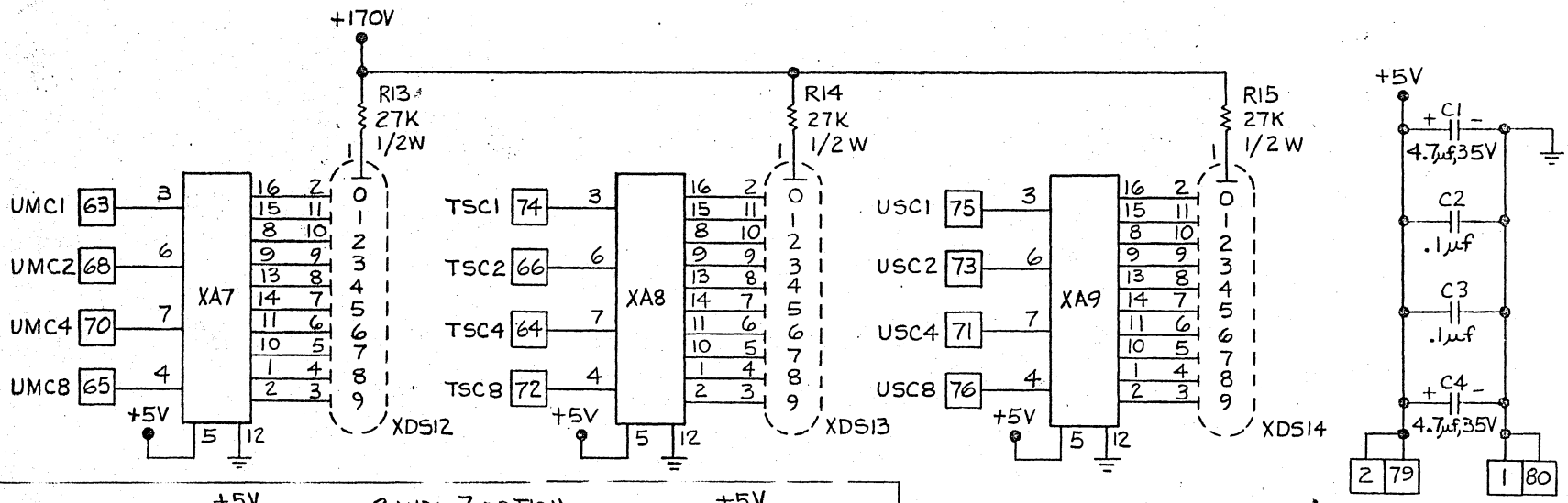
DWN	DATE	DES	DATE
R. Flocic	12-29-70	UR	12-29
CHK	12-29	ENGR	12-29
SCALE NONE		FSC 31160	

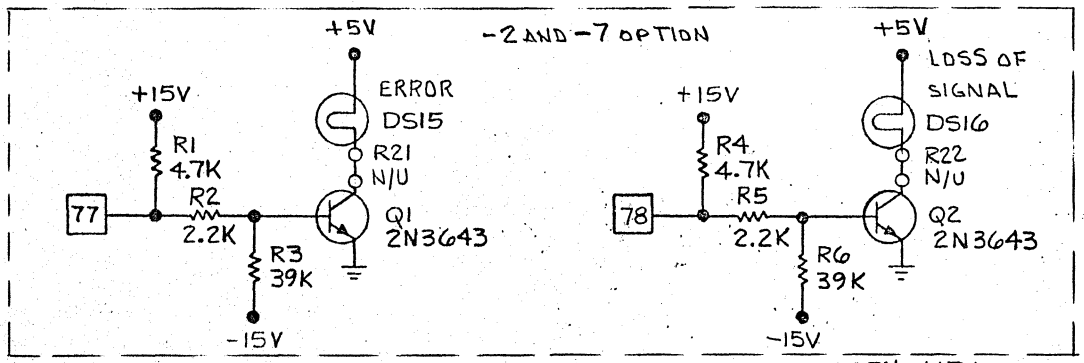
B | 15664 ⚠1 | A

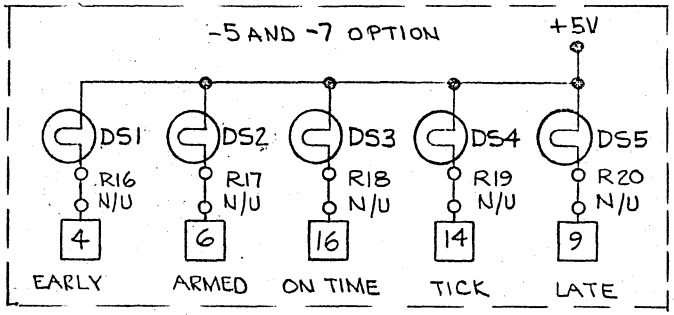
SIZE | SHT 2 OF 2 | REV

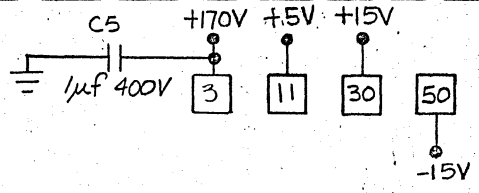
DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED









PART NO.	MFR	COMPONENT
N7441B	NATIONAL	A1 THRU A9
SK144	BURROUGHS	XDS6 THRU XDS14
B5991	BURROUGHS	DS6 THRU DS14
CML830297	CHICAGO MINIATURE	DS1 THRU DS5, 15, 16

1. A1-A9 ARE 74141 ON -1 ASSY.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03, XXX ± .010, ANGLES ± 1/2°

TITLE: FRONT PANEL DISPLAY

DWN	MILES	1/7/71	DES	RML	1/7/71
CHK	R.L	1/11/71	ENGR		1-7
SCALE	NONE		FSC	31160	

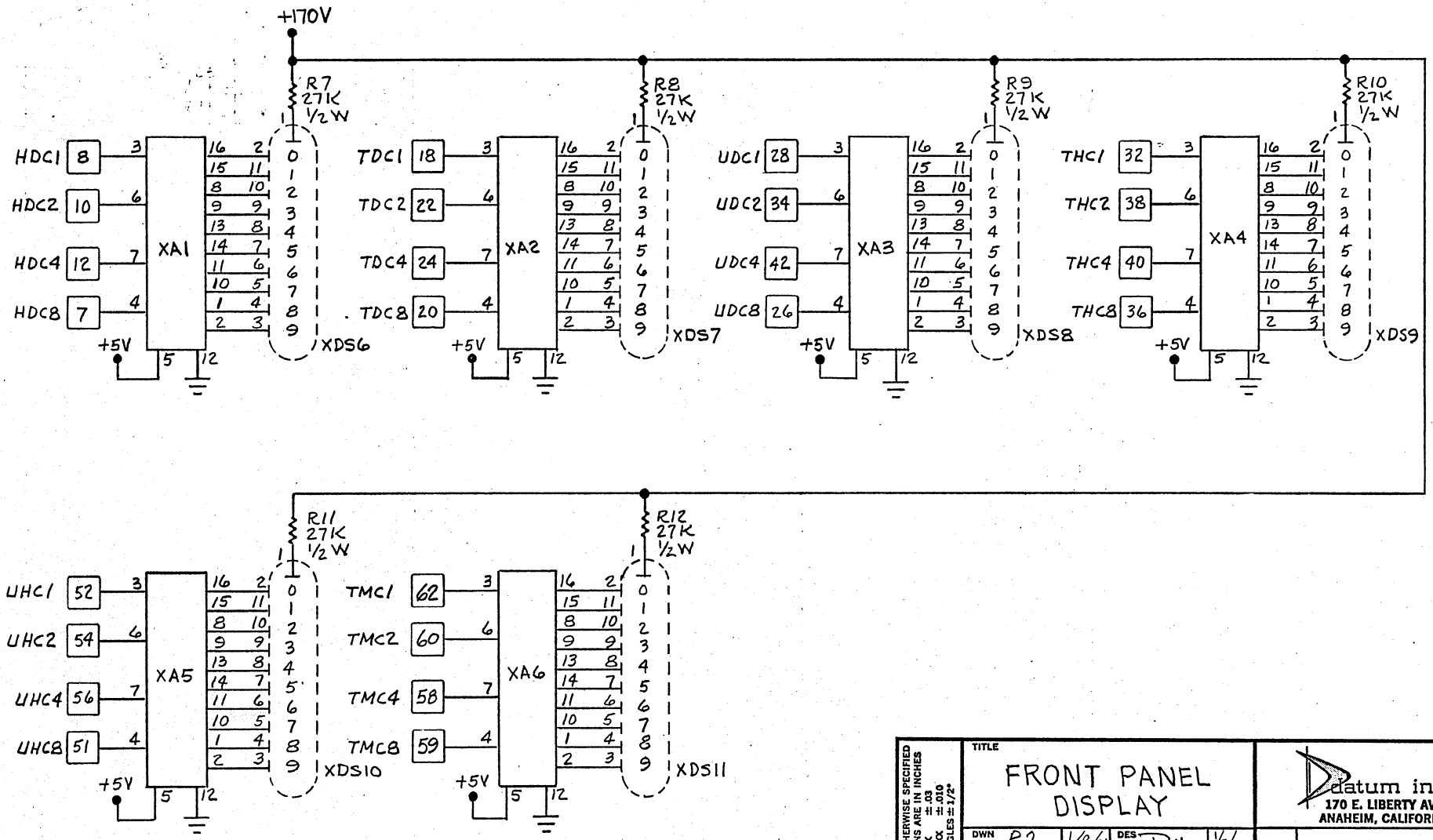
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B 15666

SIZE | SHT 1 OF 2 | REV

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE
FRONT PANEL DISPLAY

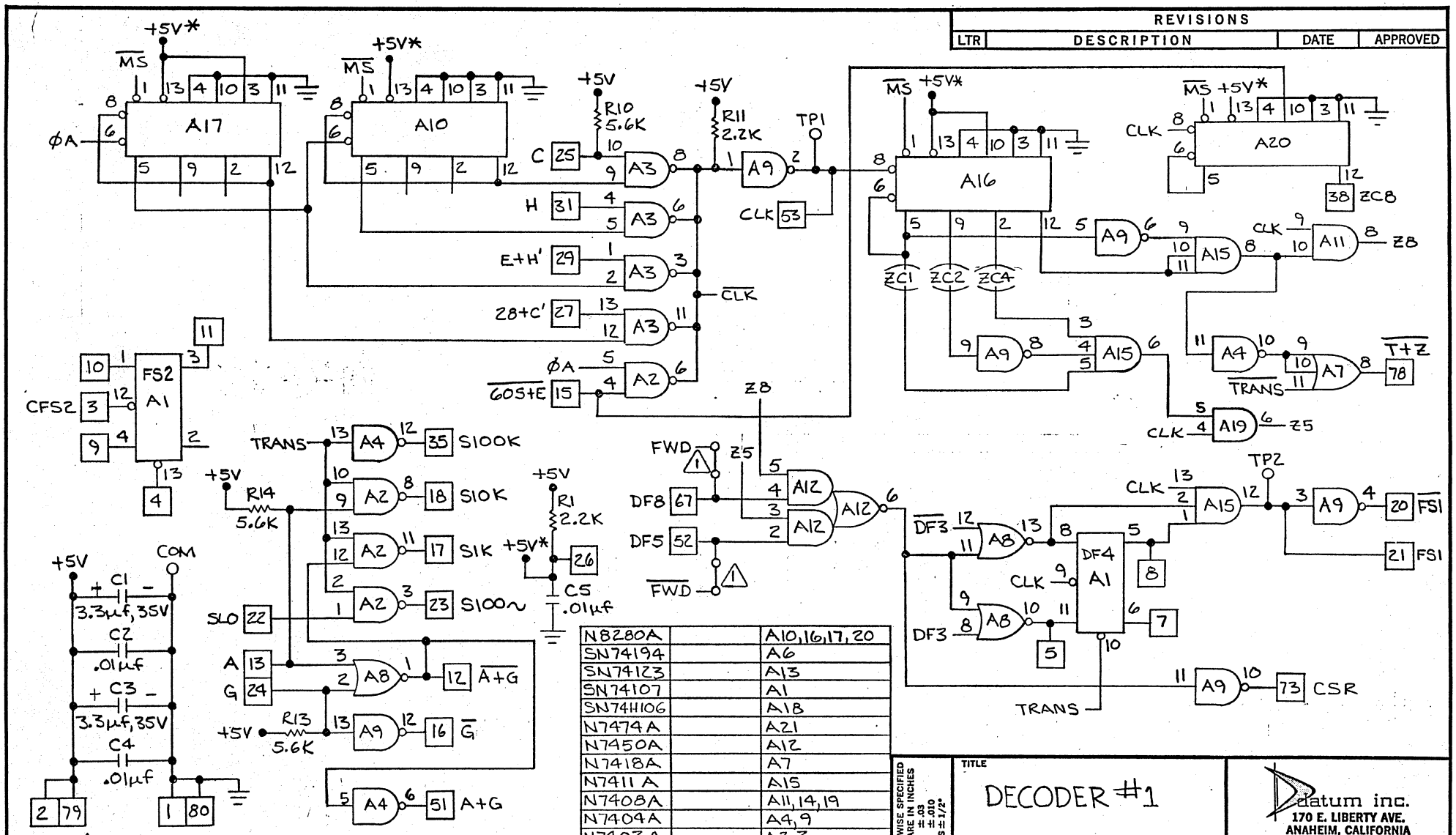
DWN	R.Z.	1/8/71	DES	RM	1/7/70
CHK	R.Z.	1/11/71	ENGR	JR	1-7
SCALE	NONE		FSC	31160	

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

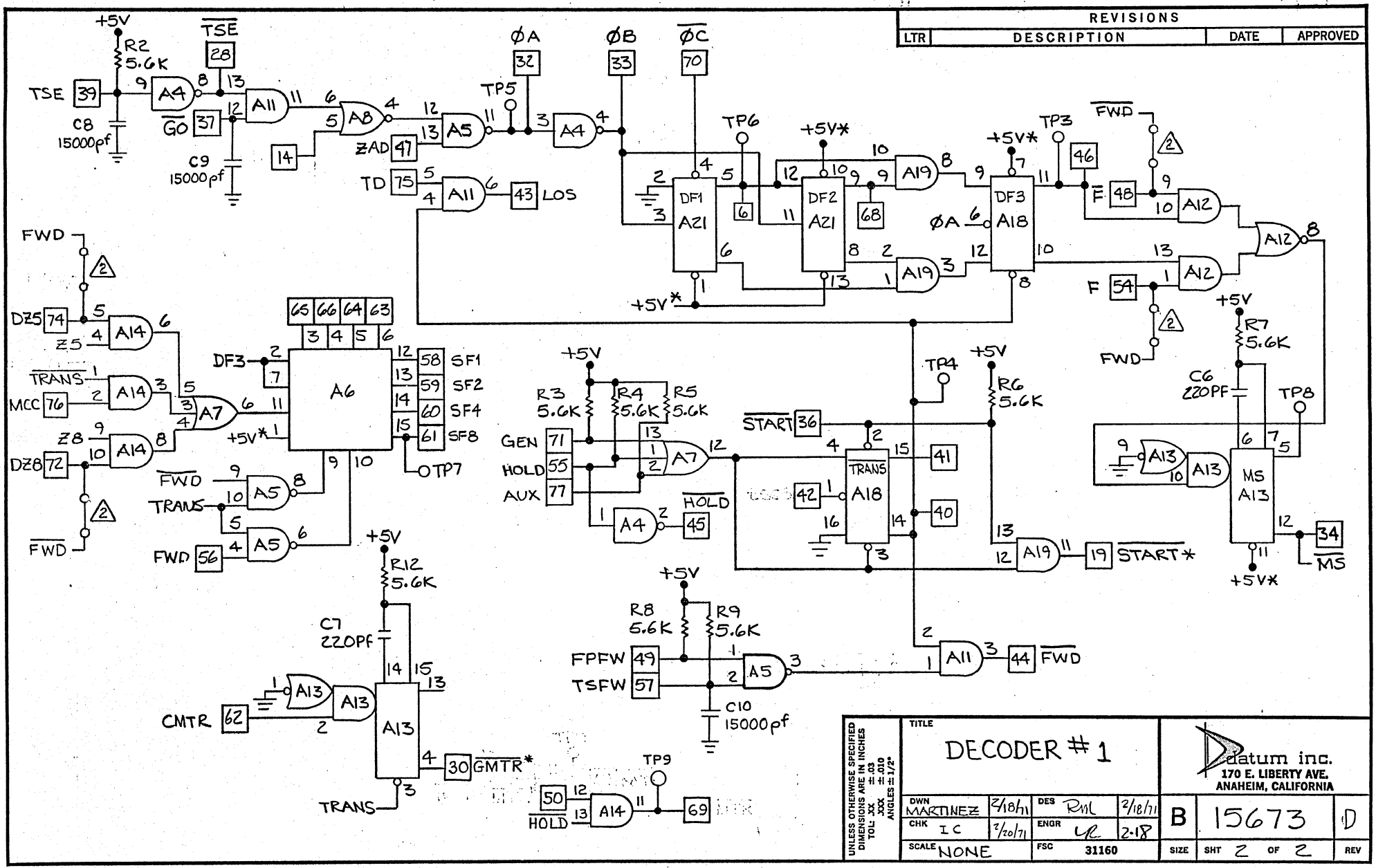
B 15666

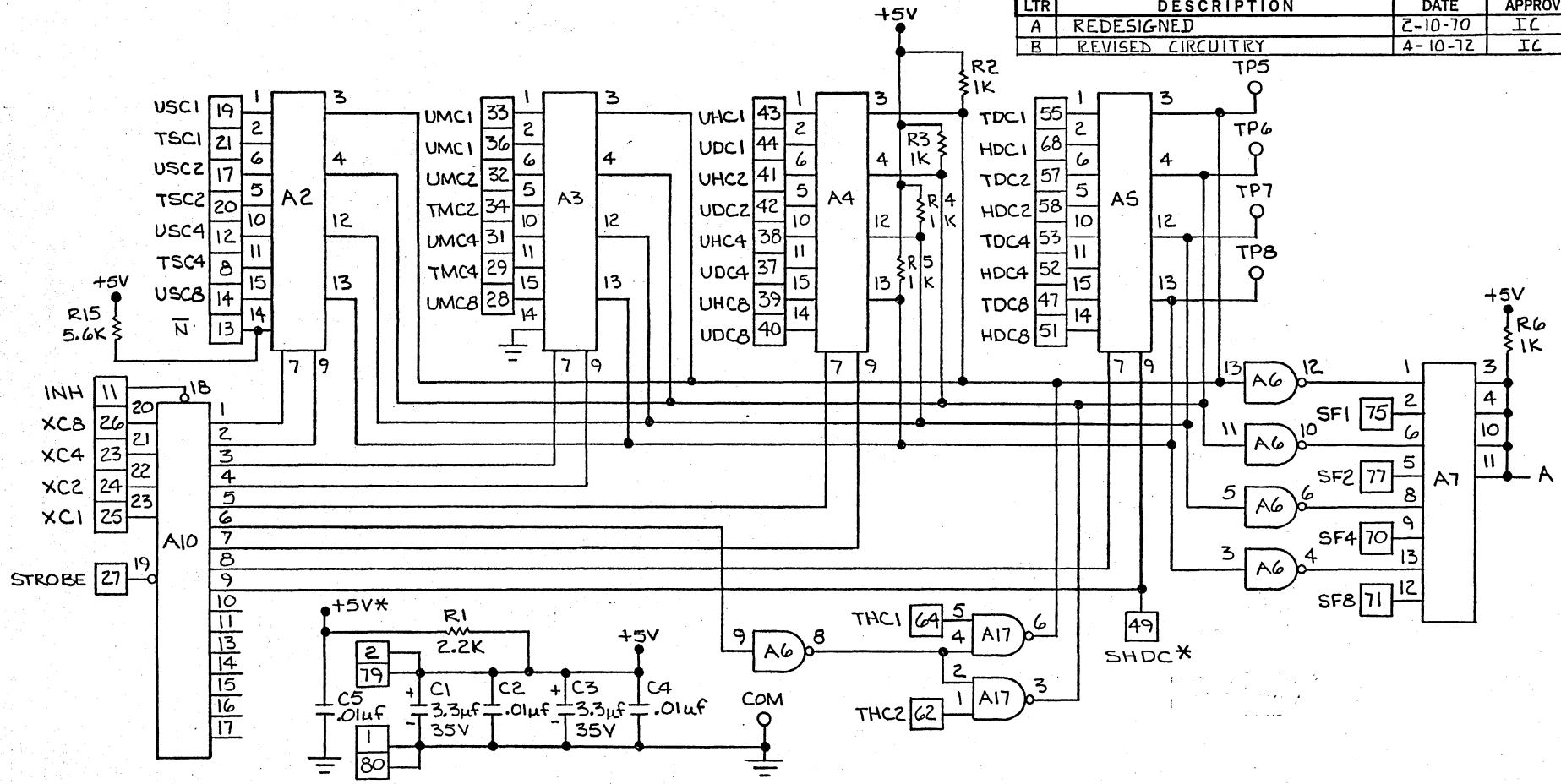
SIZE SHT 2 OF 2 REV

DIETZGEN 196 MG-10



DIETZGEN 196 MQ-10


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
+5V
R2 5.6K
TSE
39
TSE
28
A4
A11
A8
A5
A4
ØA
32
ØB
33
ØC
70
TP5
TP6
C8 15000pf
C9 15000pf
GO
37
14
ZAD
47
TD
75
A11
43
LOS
DF1 AZ1
DF2 AZ1
DF3 A18
A19
A19
A19
+5V*
TP3
FWD
46
F
48
A12
A12
A12
F
54
FWD
FWD
DZ5
74
Z5
A14
TRANS
MCC
76
A14
A7
Z8
DZ8
72
A14
FWD
DF3
A6
65 66 64 63
SF1
SF2
SF4
SF8
58
59
60
61
TP7
+5V*
FWD
TRANS
A5
A5
FWD
56
R3 5.6K
R4 5.6K
R5 5.6K
GEN
71
HOLD
55
AUX
77
A7
A4
HOLD
45
START
36
TRANS A18
42
41
40
TP4
R6 5.6K
A19
19
START*
+5V
R7 5.6K
C6 220PF
TP8
A13
A13
MS A13
34
MS
+5V*
R12 5.6K
C7 220PF
A13
A13
A13
CMTR
62
GMTR*
30
TRANS
R8 5.6K
R9 5.6K
FPFW
49
TSFW
57
A5
C10 15000pf
A11
44
FWD
TP9
50
HOLD
A14
69
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ± 1/2°
TITLE
DECODER # 1
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN MARTINEZ 2/18/71
DES RML 2/18/71
CHK IC 2/20/71
ENGR LR 2.18
SCALE NONE
FSC 31160
B
15673
D
SIZE
SHT 2 OF 2
REV
DIETZGEN 196 MG-10



LTR	DESCRIPTION	DATE	APPROVED
A	REDESIGNED	2-10-70	IC
B	REVISED CIRCUITRY	4-10-72	IC

REVISIONS

PART NO.	MFR.	REF. DES.
N8242A	SIGNETICS	A7
N8234A	SIGNETICS	A2-A5
SN74193N	TEX. INST.	A16
SN74154N	↕	A10
SN74107N	↕	A14
SN7476N	TEX. INST.	A15

PART NO.	MFR.	REF. DES.
N7474A	NATIONAL	A8
N7418A	↕	A12
N7408A	↕	A11
N7404A	↕	A6, 18
N7403A	↕	A1, 9, 17
N7402A	NATIONAL	A13

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03, XXX ±.010, ANGLES ±1/2°

TITLE: SYNC MODE

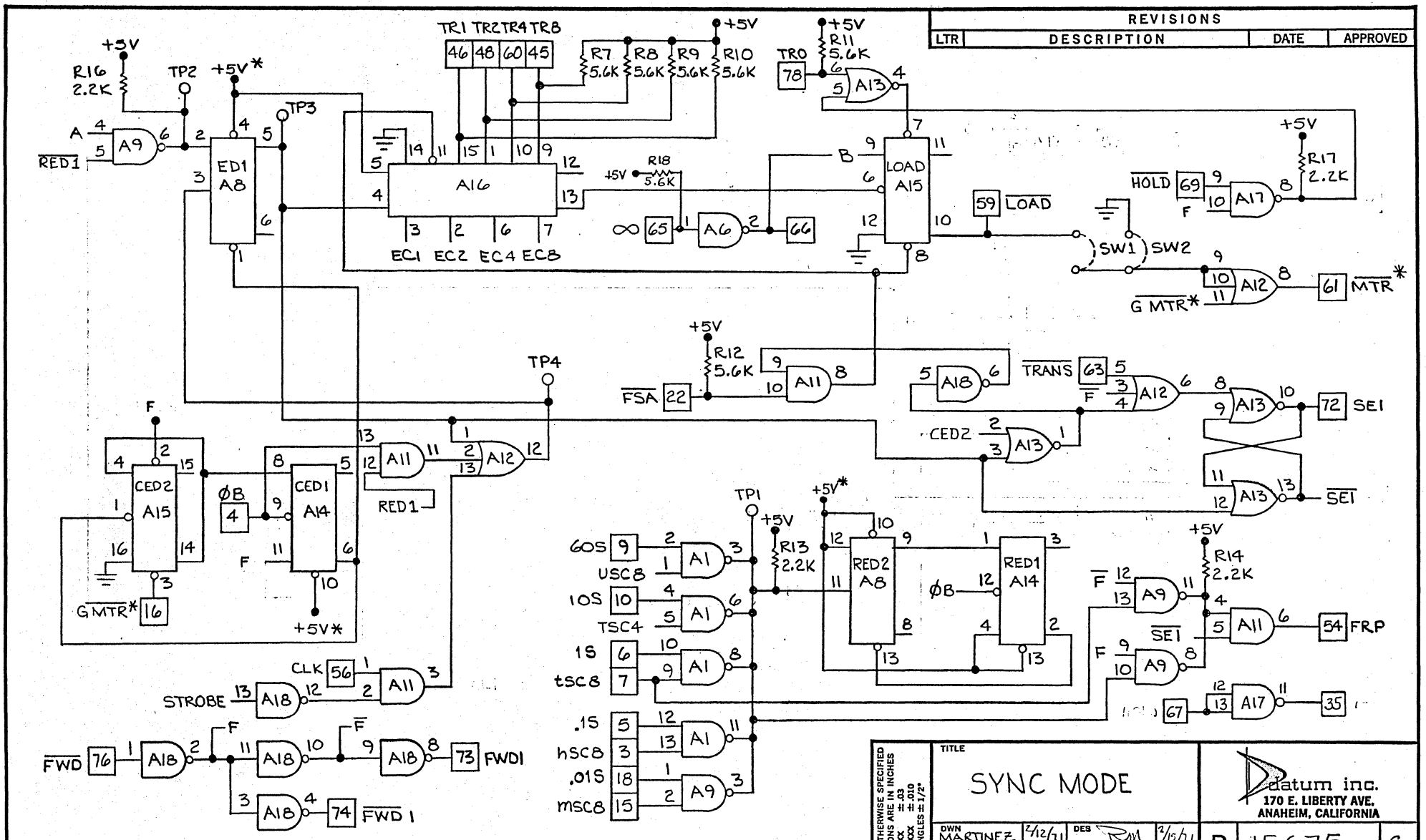
DWN	MARTINEZ	2/12/71	DES	RM	2/15/71
CHK	IC	2/20/71	ENGR		2-15
SCALE	NONE		FSC	31160	

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 15675 | C

SIZE | SHT 1 OF 2 | REV

DIETZGEN 196 MG-10



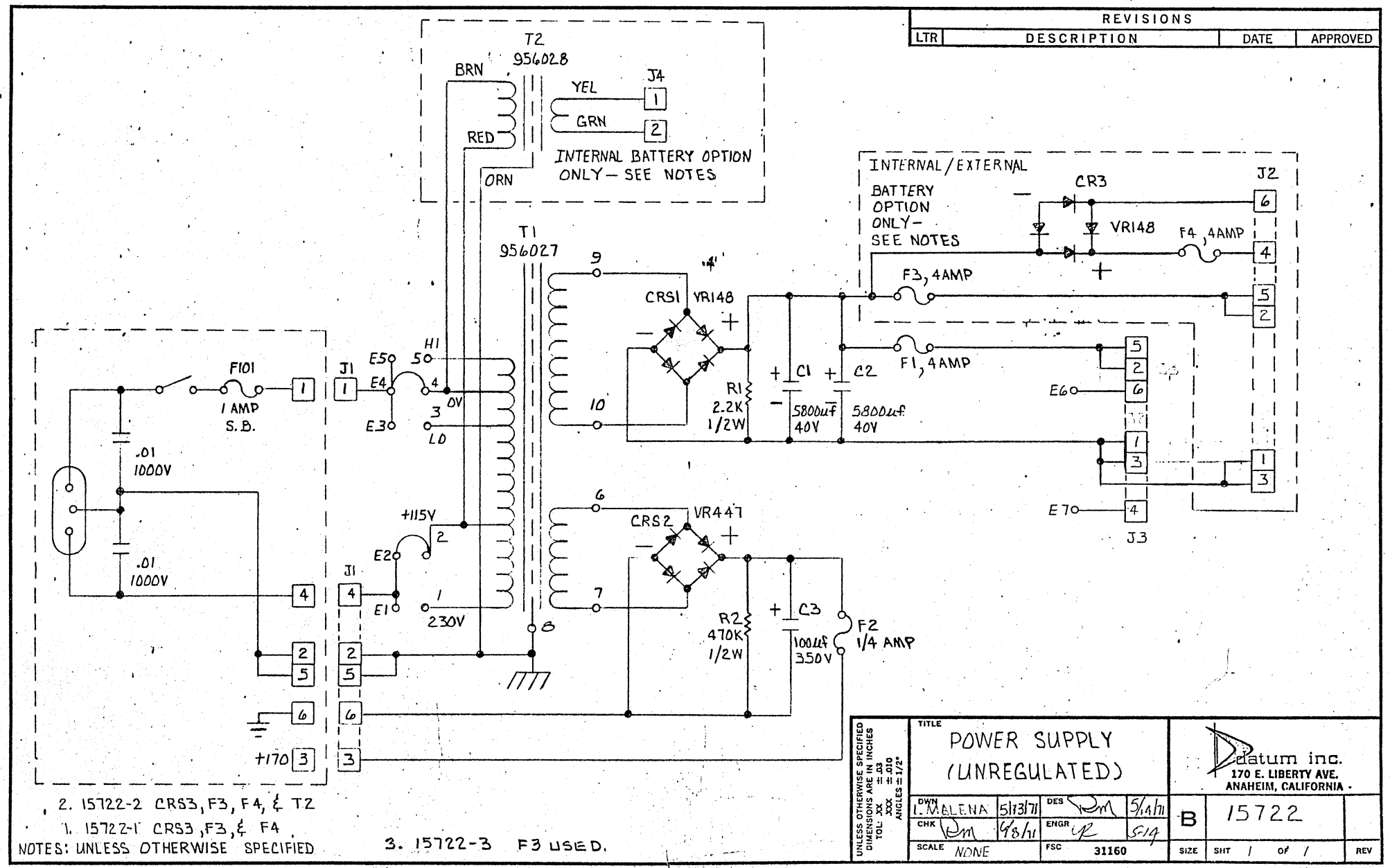
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03 XXX ±.010 ANGLES ±1/2°

TITLE: SYNC MODE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN MARTINEZ	2/12/71	DES RM	2/15/71	B	15675	C
CHK IC	2/20/71	ENGR YL	2-15			
SCALE NONE		FSC 31160		SIZE	SHT 2 OF 2	REV

DIETZGEN 196 MG-10



2. 15722-2 CRS3, F3, F4, & T2

1. 15722-1 CRS3, F3, & F4

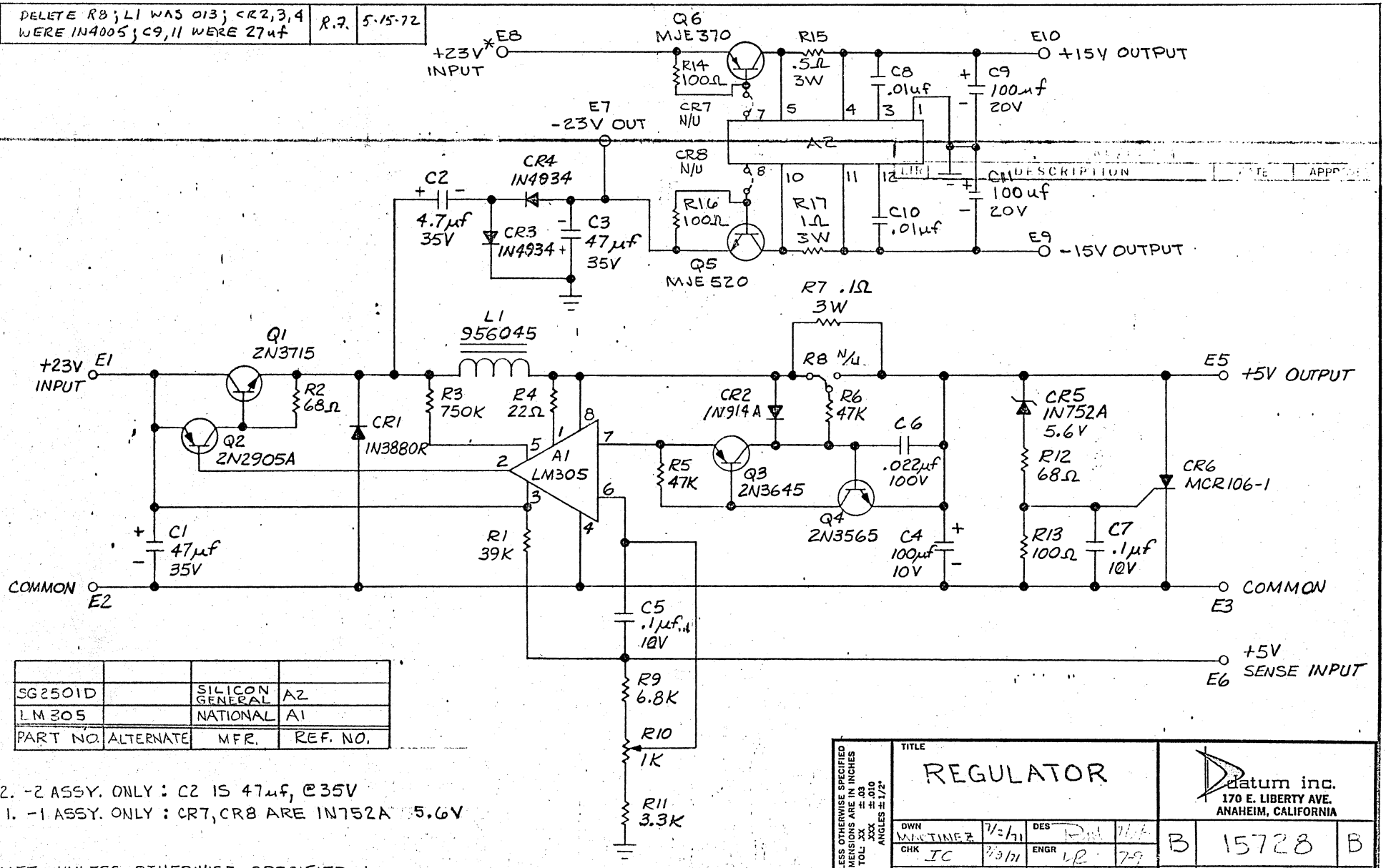
NOTES: UNLESS OTHERWISE SPECIFIED

3. 15722-3 F3 USED.

DIETZGEN 196 MG-10

TF15712

B	DELETE R8; L1 WAS 013; CR2,3,4 WERE IN4005; C9,11 WERE 27uf	R.T.	5-15-72



SG2501D		SILICON GENERAL	A2
LM305		NATIONAL	A1
PART NO.	ALTERNATE	MFR.	REF. NO.

2. -2 ASSY. ONLY : C2 IS 47µf, @35V
1. -1 ASSY. ONLY : CR7, CR8 ARE IN752A 5.6V

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: REGULATOR

DWN WHITING 7/21/71 DES [illegible]

CHK IC 7/21/71 ENGR LP 7-9

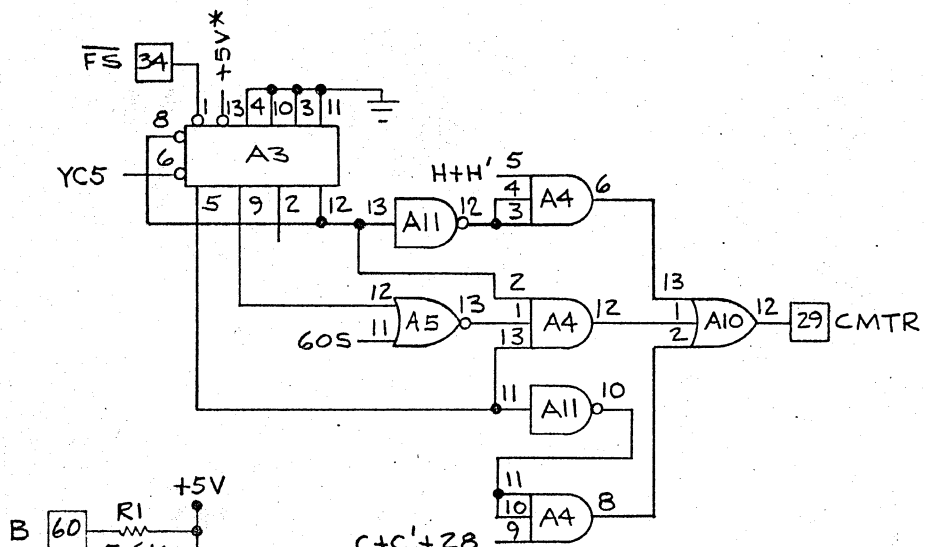
SCALE NONE FSC 31160

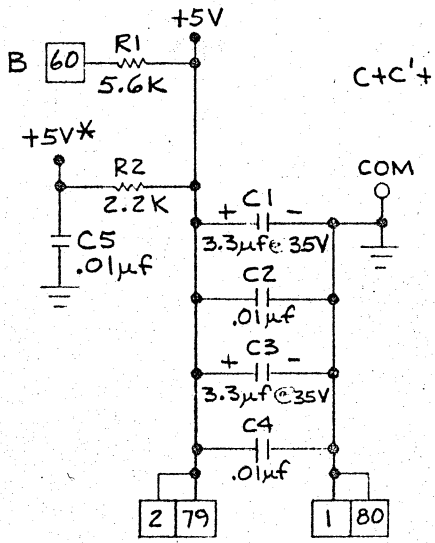
datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

B | 15728 | B

SIZE | SHT 1 OF 1 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REVISED CIRCUITRY	4-10-72	IC





PART NO.	MFR.	REF. NO.
N8288A	SIGNETICS	A3
N8280A	SIGNETICS	A2,16
SN74193N	TEX. INST.	A8
SN74154N	TEX. INST.	A9
SN7415IN	TEX. INST.	A15
N7432A	NATIONAL	A1,6,7,12,17
N7418A	↕	A10
N7411A	↕	A4
N7408A	↕	A14
N7404A	↕	A11
N7402A	↕	A5,A18
N7400A	NATIONAL	A13

NOTE: ⚠1 CUT ETCH AND INSTALL A12 FOR -1 ASSY.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

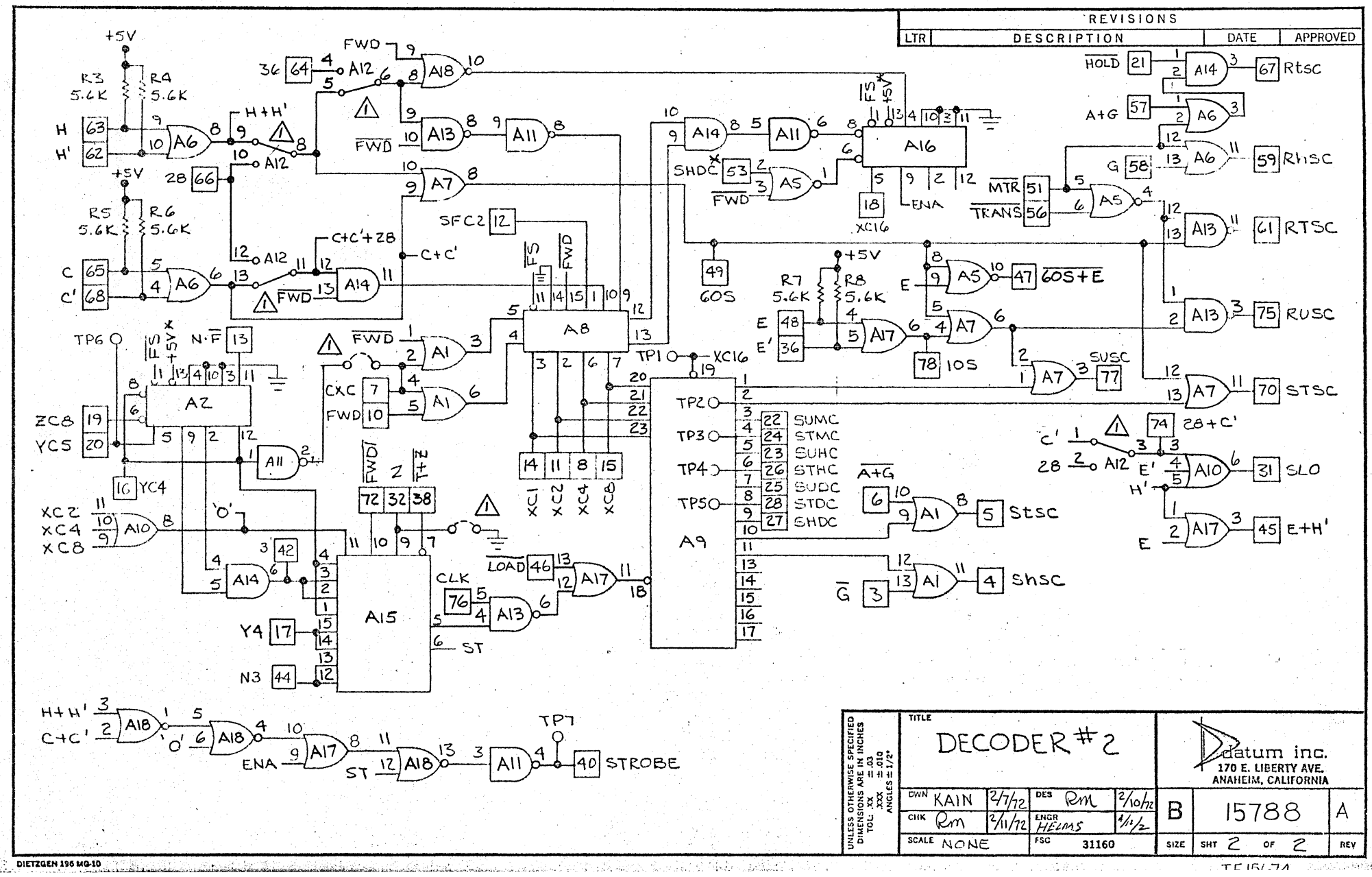
TITLE: DECODER #2

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN KAIN	2/7/72	DES RM	2/10/72	B	15788	A
CHK RM	2/11/72	ENGR HELMS	11/2/2			
SCALE NONE		FSC 31160		SIZE	SHT 1 OF 2	REV

DIETZGEN 196 MQ-10

TF 15674


REVISIONS
LTR DESCRIPTION DATE APPROVED
+5V
R3 5.6K
R4 5.6K
H
H'
A6
H+H'
A12
FWD
A18
A13
A11
A7
SFC2
C+C'+ZB
C+C'
R5 5.6K
R6 5.6K
C
C'
FWD
A14
A1
A8
TP6
N·F
A2
ZC8
YC8
YC4
XC2
XC4
XC8
A10
'0'
Z
T+Z
A15
Y4
N3
CLK
LOAD
ST
A17
A16
SHDC
ENA
XC16
A5
MTR
TRANS
HOLD
A14
A+G
A6
G
RtSC
RhSC
RTSC
RUSC
STSC
SUSC
60S+E
60S
R7 5.6K
R8 5.6K
E
E'
A17
78 10S
28+C'
SLO
E+H'
TP1
TP2
TP3
TP4
TP5
A9
SUMC
STMC
SUHC
STHC
SUDC
STDC
SHDC
StSC
ShSC
TP7
STROBE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°
TITLE
DECODER #2
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN KAIN 2/7/72
DES RM 2/10/72
CHK RM 2/11/72
ENGR HELMS 4/1/72
SCALE NONE
FSC 31160
B
15788
A
SIZE
SHT 2 OF 2
REV
DIETZGEN 196 MG-10

APPENDIX A

EQUIPMENT MODIFICATIONS AND OPTIONS

TABLE OF CONTENTS

Paragraph	Title	Page
	Unit Configuration List	
A-1	Introduction	
A-2	Basic Unit Changes or Modifications	
A-3	Option Modification	
A-4	Specifications	
A-5	Option Descriptions	
	Slow Code (9110-8082)	29
	Tape Search Outputs (9310-8082)	44
	Pulse Rate Outputs (9310-8113)	45
A-6	Output Connector Pin List	
	Recommended Spare Parts	

MATERIALS LIST

Title	Number
Recommended Spare Parts List	9210-111A
Time Code Translator	9210-111A
36-Bit Buffer	15663
Slow Code	15672

MODIFICATIONS
(9210-8017)

Drawing 9310-8113 term was: Δ100Ω is: mSC8.

DRAWING LIST

Title	Circled Number	File Number
Logic and Block Diagrams		
Top Assembly Diagram		9210-111A
Block Diagram, Options		9210-8019
Slow Code	(29)	9110-8082
Tape Search Outputs	(44)	9310-8082
Pulse Rate Outputs	(45)	9310-8113
Schematic Diagrams		
36-Bit Buffer		15663
Slow Code		15672

UNIT LOGIC CONFIGURATION LIST

Model 9210-111A

Item	Title	Circled Number	Basic Drawing Number	Option Drawing Number
1.	Top Assembly			9210-111A
2.	Block Diagram, Options		9310-8068	
3.	Block Diagram, Options			9210-8019
4.	AGC and Filters	(1)	9310-8069	
5.	Input and Decode	(2)	9310-8070	
6.	Decoder Logic Control	(5)	9310-8112	
7.	Sync Mode and Loading	(7)	9310-8111	
8.	Minor Time Counter	(8)	9310-8077	
9.	Major Time Counter	(9)	9310-8078	
10.	Display Logic	(10)	9310-8079	
11.	Tape Search Outputs	(44)		9310-8082
12.	Pulse Rate Outputs	(45)		9310-8113
13.	Modification			9210-8017
14.				
15.				
16.				
17.				
18.				

APPENDIX A

EQUIPMENT MODIFICATIONS AND OPTIONS

A-1 INTRODUCTION

This appendix contains information relation to modifications and options added to the basic Model 9310 Time Code Generator/Translator. Also included in this appendix are the top assembly diagram, logic configuration list, and the input/output specifications applicable to this unit. The logic configuration list contains a complete logic drawing list. This appendix also contains the recommended spare parts list and drawings not contained in Chapters Six or Seven but applicable to this unit.

A-2. BASIC UNIT CHANGES OR MODIFICATIONS

There no modification to the basic unit.

A-3 OPTION MODIFICATIONS

The pulse rates output logic was modified, Reference Drawing 9210-8017.

A-4 OUTPUT SPECIFICATIONS

a. PULSE RATE OUTPUTS

	Carrier Pulse Rate
1. Frequencies:	1 Kpps
	100 pps
	10 pps

2. Amplitude: +5V ±1.25V peak, maximum

3. Source Impedance: dtl/ttl compatible

b. TAPE SEARCH OUTPUTS

1. Parallel Outputs: 46 lines representing tenths-of-milliseconds, milliseconds, seconds, minutes, hours, and days in 8-4-2-1 binary coded decimal.

2. Amplitude
   (a) Binary 1: +5V ±1.25V
   (b) Binary 0: 0V ±0.4V

3. Source Impedance: dtl/ttl compatible

c. FORMAT DATUM SLOW CODE
   (a) Amplitude, adjustable binary one=10v, binary zero =6v, nominal.
   (b) Source impedance, less than 100 ohms.

A-5 OPTION DESCRIPTIONS

The option circuits, illustrated in block diagram form, convert the time-of-day information contained in the minor and major time counters into the desired serial and time code formats for transmission to external equipment. These circuits also include buffering circuits as required. Descriptions of these circuits are included in circled-number order following this paragraph.

FIVE RATE SLOW CODE ENCODER (29)

INTRODUCTION

This description contains a functional explanation of the five-rate slow code encoder.

BI-LEVEL SLOW CODE DESCRIPTION

The serial code, Figure 1, is a 33-bit amplitude-width modulated dc level-shift code. The code is composed of a reference marker and four sub-code words of seconds, minutes, hours, and days. Each sub-code word is weighted in a binary-coded decimal manner.

The frame is divided into precise intervals. Leading edges of all pulses are coincident with the leading edges of the time code frame intervals. The sum of the coded time refers to the leading edge of the code word reference marker.

One pulse is deleted at the beginning and the end of the time code word and between each digit in a code word. Two pulses are deleted between each digit in a code word. Two pulses are deleted between each digit. Index markers complete the time frame after the time-of-year word has been read.

The amplitude and pulse-widths of the time frame information are as follows:

Amplitude

Binary 1: +10V dc nominal
Binary 0: +6V dc nominal

Pulse Width

Reference marker:	100% of frame interval
Binary 1:	50% of frame interval
Binary 0:	25% of frame interval

FUNCTIONAL DESCRIPTION

The five-rate slow code encoder scans the contents of the major time counter to develop a serial train the format illustrated in Figure 1. The code rate is selected by a front panel rotary switch; this switch is a binary coded decimal switch which selects one of nine positions. The first position being an OFF position. The encoder consists of a 33-bit shift register which is loaded with the contents of the major time counter and shifted out, according to which rate was selected. The pulse-width generator inserts the reference and index marker and provides the correct pulse-width as defined for the code. An output amplifier encodes the amplitude information and outputs a dc envelope of the desired characteristics.

SLOW CODE RATE Switch

Position 1.	OFF
Position 2.	1 SEC
Position 3.	5 SEC
Position 4.	10 SEC
Position 5.	60 SEC
Position 6.	600 SEC
Position 7.	NOT USED
Position 8.	NOT USED
Position 9.	NOT USED

FRAME INTERVAL GENERATOR

The frame interval generator divides the frame period listed in Figure 1 into either 50 or 60 unique intervals. The FRAME RATE switch selects the bit rate counter clock rate. The bit rate counter outputs determine the percentage divisions of the frame interval period, divides the frame period into precise intervals and supplies the clock to the shift register.

SHIFT REGISTER

This circuit contains a 33-bit shift register which is loaded with the contents of the major time counter once per frame as determined by the FRAME RATE switch. The data is then shifted out to the pulse-width generator at the clock rate supplied by the frame interval generator.

PULSE-WIDTH GENERATOR

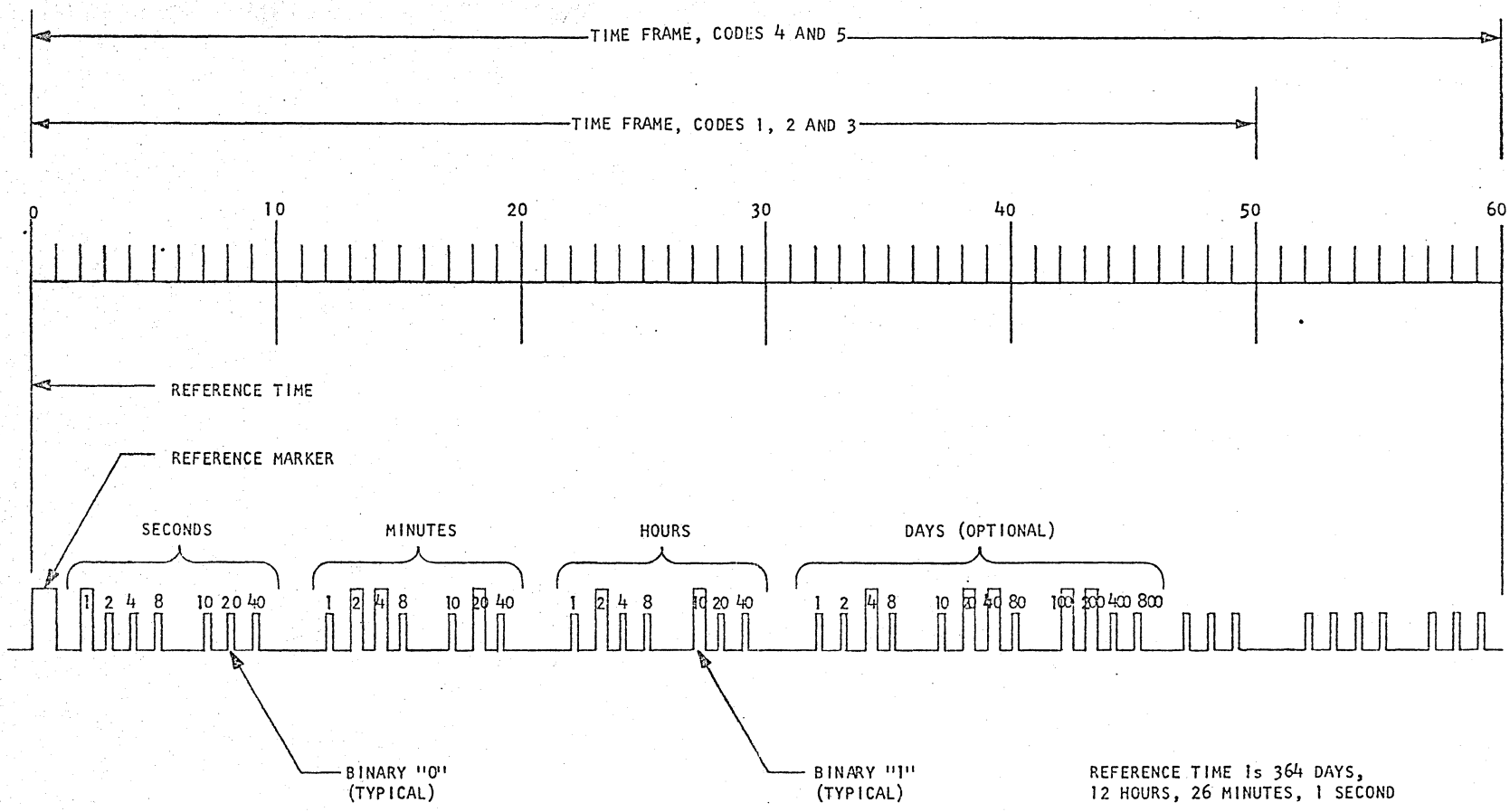
This circuit contains gates to insert the reference and index markers, delete pulses between the BCD bits and sub-words, and provide the correct pulse-widths for the information as required. The pulse-width generator provides two outputs to an output amplifier.

A. "$\overline{1}$" - This output is false for a binary 1 or reference marker.

B. "$\overline{0}$" - This output is false for a binary 0 or an index marker.

AMPLIFIER

The amplifier provides tri-level pulse output for the coded information received from the pulse-width generator. The output data amplitude is adjustable from 0V dc to +10V dc. A binary 0 has approximately 60% of amplitude of a binary 1.



CODE	PULSE RATE	FRAME PERIOD	BINARY ZERO	BINARY ONE	FRAME REFERENCE PULSE
1	50 PPS	1 SEC	4 MS	10 MS	20 MS
2	10 PPS	5 SEC	20 MS	50 MS	100 MS
3	5 PPS	10 SEC	40 MS	100 MS	200 MS
4	1 PPS	60 SEC	200 MS	500 MS	1,000 MS
5	1 PPS 10S	10 MIN	2 SEC	5 SEC	10 SEC

datum inc.

BI-LEVEL SLOW CODE REV.A

Figure 1.

TAPE SEARCH OUTPUTS (44)

INTRODUCTION

This description contains a functional explanation of the tape search outputs included with the basic unit.

FUNCTIONAL DESCRIPTION

This logic consists of 46 buffers which allow control signals and major time counter outputs to drive circuits in a tape search unit.

The logic isolates the output lines from the internal counters so that external loading or shorting cannot affect the time integrity of the basic unit. The buffers are non-inverting drivers, therefore, when the input is high (+5V) the output is high.

Voltage outputs are also supplied at the output connector to power the tape search unit.

PULSE RATE OUTPUTS (45)

INTRODUCTION

This description contains a functional explanation of the pulse rate outputs included with the basic unit.

FUNCTIONAL DESCRIPTION

This logic buffers minor time counter outputs for use by external equipment. Four pulse rate outputs are applied to one or more output connectors as illustrated on the unit top assembly diagram. The repetition rates of the output pulses range from 1-kpps down to 1-pps in divisions of 10. The negative-going edge of each pulse output is normally defined as on time.

GENERATE Mode Pulse Outputs

All pulse rates are available in the GENERATE mode. The pulse rate outputs, except the 1-kpps output, have a 20 percent duty cycle. The 1-kpps output has a pulse-width of approximately one microsecond.

TRANSLATE Mode Pulse Outputs

For input codes having a carrier frequency of 1-kHz or greater, pulse rates of 1 kpps and less are available. For the IRIG C and IRIG E input codes having a 100 Hz carrier frequency, pulse rates of 100 pps and less are available.

OUTPUT CONNECTOR PIN LIST

A. BNC Connectors

Connector	Signal
J8	Slow Code
J12	1 pps
J13	10 pps
J14	100 pps
J15	1 kpps

B. J2 Tape Search Outputs

Pin	Signal	Pin	Signal
1 A	HD2	AP	hs8
B	HD1	AR	hs4
C	TD8	AS	hs2
D	TD4	AT	hs1
E	TD2	AU	ms8
F	TD1	AV	ms4
H	UD8	AW	ms2
J	UD4	AX	ms1
K	UD2	AY	tms8
10 L	UD1	AZ	tms4
M	TH2	BA	tms2
N	TH1	BB	tms1
P	UH8	BC	GO
R	UH4	BD	SEARCH
S	UH2	BE	FWD
T	UH1	BF	SAMPLE INHIBIT
U	TM4 (10 Min)	BH	FRP
V	TM2	BJ	GND
W	TM1	BK	GND
20 X	UM8	BL	GND
Y	UM4 (1 Min)	BM	GND
Z	UM2	BN	GND
AA	UM1	BP	+20V
AB	TS4	BR	+20V
AC	TS2 (10 sec)	BS	-15V
AD	TS1	BT	+5V
AE	US8	BU	+5V
AF	US4 (1 sec)	BV	+5V
AH	US2	BW	SYNC ERROR
30 AJ	US1	BX	TSE
~~AX~~ AK	ts8	CA	HD8
AL	ts4 (0.1 sec)	CB	HD4
AM	ts2	CC	TH8
34 AN	ts1	68 CD	TH4

RECOMMENDED SPARE PARTS

MODEL 9210-111A TIME CODE TRANSLATOR

(ORDER BY NUMBER)

ITEM NO.	NAME AND DESCRIPTION	MANUFACTURER'S PART NO.	MANUFACTURER	TOTAL IN SYS.	RECOM'D SPARES
1.	AGC Amplifier	15584	DATUM	1	1
2.	Filter	15585n	DATUM	1	1
3.	Minor Time Counter	15662	DATUM	1	1
4.	36-Bit Buffer	15663	DATUM	3	1
5.	Major Time Counter	15664	DATUM	1	1
6.	Decoder #1	15673	DATUM	1	1
7.	Decoder #2	15788	DATUM	1	1
8.	Sync Mode	15675	DATUM	1	1
9.	Slow Code	15672	DATUM	1	1
10.	Regulator	15728	DATUM	1	1
11.					
12.					
13.					
14.					
15.					
16.					
17.					

ITEM NO.	NAME AND DESCRIPTION	MANUFACTURER'S PART NO.	MANUFACTURER	TOTAL IN SYS.	RECOM'D SPARES
The following circuit assemblies are semi-modular and can either be stocked as spares assemblies complete or components can be maintained as maintenance support.					
	Front Panel Display less Nixie Indicators	15666	DATUM		
a.	IC	SN 7441	T.I.	9	2
b.	Transistor	2N3643		2	1
c.	NIXIE Tube	B5991	Burroughs	9	2
d.	Lamp	S7-4752-3731-500	Monsanto	2	2
	Filter Switch Assembly	15603	DATUM	1	
a.	IC	SP380	Signetics	1	1
b.	Diode	IN914		14	5
c.	Transistor	2N3565		2	1
d.	Transistor	2N3645		2	1

Datum, inc. — MATERIALS LIST

DATE: 4-18-72 JOB NO: TITLE: TIME CODE TRANSLATOR REV 1 OF 2

DRAWN: R. FLOCK QUANTITY: ASS'Y NO: 9210-111 A

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0226-0103	CAPACITOR .01 uf @ 1000V	DATUM	2				
2	1702-0040	CONN 80P	"	10				
3	1704-0090	RECEPT 90P	"	1				J2
4	1704-0090-1	PLUG	"	1				
5	1704-1002	RECEPT BNC	"	7				J3, 8, 10, 12-15
6	1704-1061-1	RECEPT	"	1				J16
7	1792-8017	PIN	"	90				
8	1795-0001	WASHER	"	7				
9	1795-0002	WASHER	"	7				
10	2340-0020	SLIDE	"	2				
11	2524-702m	KNOB	"	1				
12	4000-2004	PWR CORD	"	1				
13								
14	703192	FT PANEL ASSY	"	1				
15								
16	914015-1	CARD GUIDE	"	3				
17	914015-2	" "	"	3				
18	703104-1	GUSSET R.H.	"	1				
19	703104-2	" L.H.	"	1				
20	703105	MTG BLOCK	"	4				
21	703108	FRONT PLATE	"	1				
22	703109	CTR SUPPORT	"	1				
23	703110	P.S. SUPPORT	"	1				
24	703111-2	CONTROL PANEL	"	1				
25	703116-1	MTG BLOCK	"	4				
26	703116-2	" "	"	2				
27	703117	" "	"	1				

Datum, Inc. — MATERIALS LIST

REV 2 OF 2

DATE: 4-18-72 JOB NO: TITLE: TIME CODE TRANSLATOR

DRAWN: R. FLOCK QUANTITY: ASS'Y NO: 9210-111A

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
[illegible]	703119	MTG BLOCK	DATUM	1				
10	703145-1	COVER	"	1				
11	703145-2	COVER	"	1				
12	703146-1	BUTCH PLATE	"	2				
13	703167-1	REAR PANEL	"	1				
14	703171	CONN PLATE	"	1				
15								
16	15723	REGULATOR	"	1				
17	170291	DIST CARD	"	1				
18	15722	PWR SUPPLY	"	1				
19	15666	DISPLAY	"	1				
20	15594	AGC	"	1				
21	15535	FILTER	"	1				
22	15673	DECODE #1	"	1				
23	15733	DECODE #2	"	1				
24	15662	MINOR TIME	"	1				
25	15663	36 BIT BUFFER	"	3				
26	15672	SLOW CODE	"	1				
27	15675	SYNC MODE	"	1				
28	15669	MAJOR TIME	"	1				
29								
30	951013	SWITCH (MARCO-OAK)	"	1				
31	1104002-111	CONN 80P	WINCHESTER	4				
32	653	HOLE PLUG 1/2"	A.H. SMITH	5				

Datum inc

MATERIALS LIST

REV

DATE: 12-18-70 JOB NO: TITLE: 36 BIT BUFFER

DRAWN: MILES QUANTITY: ASS'Y NO: 15663S

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	M&R/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0222	RESISTOR 2.2K 1/4W 5%	DATUM	1				R1
2								
3								
4								
5	0212-0104	CAPACITOR .1μf 100V	"	3				C2,3,5
6	0220-0335	CAPACITOR 3.3μf 35V	"	2				C1,4
7								
8								
9	0301-7408	2 WAY AND GATE USN7408A	DATUM	9				A1-9
10								
11								
12	1706-3000	TEST POINT 119437-C (BLACK)	DATUM	1				COM
13	1706-2010	TERMINAL (20108 USECO)	DATUM	1				TP1
14								
15	170311	P.C. BOARD	DATUM	1				
17	A-15663	ASSY AID DWG	DATUM	REF				
19	DS-107-1-14C	SOCKET	JOLO IND	9				

Datum, Inc. — MATERIALS LIST

REV

DATE: 5-15-71 JOB NO: TITLE: SLOW CODE S-M-H-D

DRAWN: L. MALENA QUANTITY: ASS'Y NO: 15672

SHT 1 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
1	0102-0102	RESISTOR 1K 1/4W 5%	DATUM	3				R6, 7, 20
2	" -0222	" 2.2K " "	"	1				R16
3	" -0272	" 2.7K " "	"	3				R9, 13, 14
4	" -0472	" 4.7K " "	"	6				R1-5, 19
5	" -0562	" 5.6K " "	"	3				R8, 10, 11
6		"						
7	0108-0820	RESISTOR 82Ω 2W 5%	"	1				R15
8	0102-0302	" 3K 1/4W 5%	"	2				R17, 18
9	0153-1002	POT 10K 76PR10K	"	1				R12
10								
11	0212-0472	CAPACITOR .0047uf 100V	"	1				C1
12	" -0103	" .01uf 100V	"	3				C2, 7, 9
13	0212-0104	" .1uf 100V	"	2				C4, 6
14	0220-0475	" 4.7uf 35V	DATUM	3				C3, 5, 8
15	0225-0821	" 820pf 100V	"	1				C10
16								
17	0301-7400	I.C. N7400A	DATUM	1				A10
18	0301-7402	" N7402A	"	1				A15
19	0301-7406	" N7406A	"	1				A17
20	0301-7408	" N7408A	"	2				A13, 14
21	0301-7418	" N7418A	"	1				A11
22	0301-7432	" N7432A	"	1				A9
23	0301-7107	" N7107A	"	1				A12
24	0301-8280	" N8280A	"	2				A2, 3
25	0301-7496	" SN7496	"	1				A1
26	0301-7151	" SN7451	DATUM	2				A16, 8
27	SN74165	I.C. SN74165	TEX INST	4				A4, 5, 6, 7

Datum, Inc. MATERIALS LIST

DATE: 5-15-71 JOB NO: _____ TITLE: SLOW CODE S-M-H-D

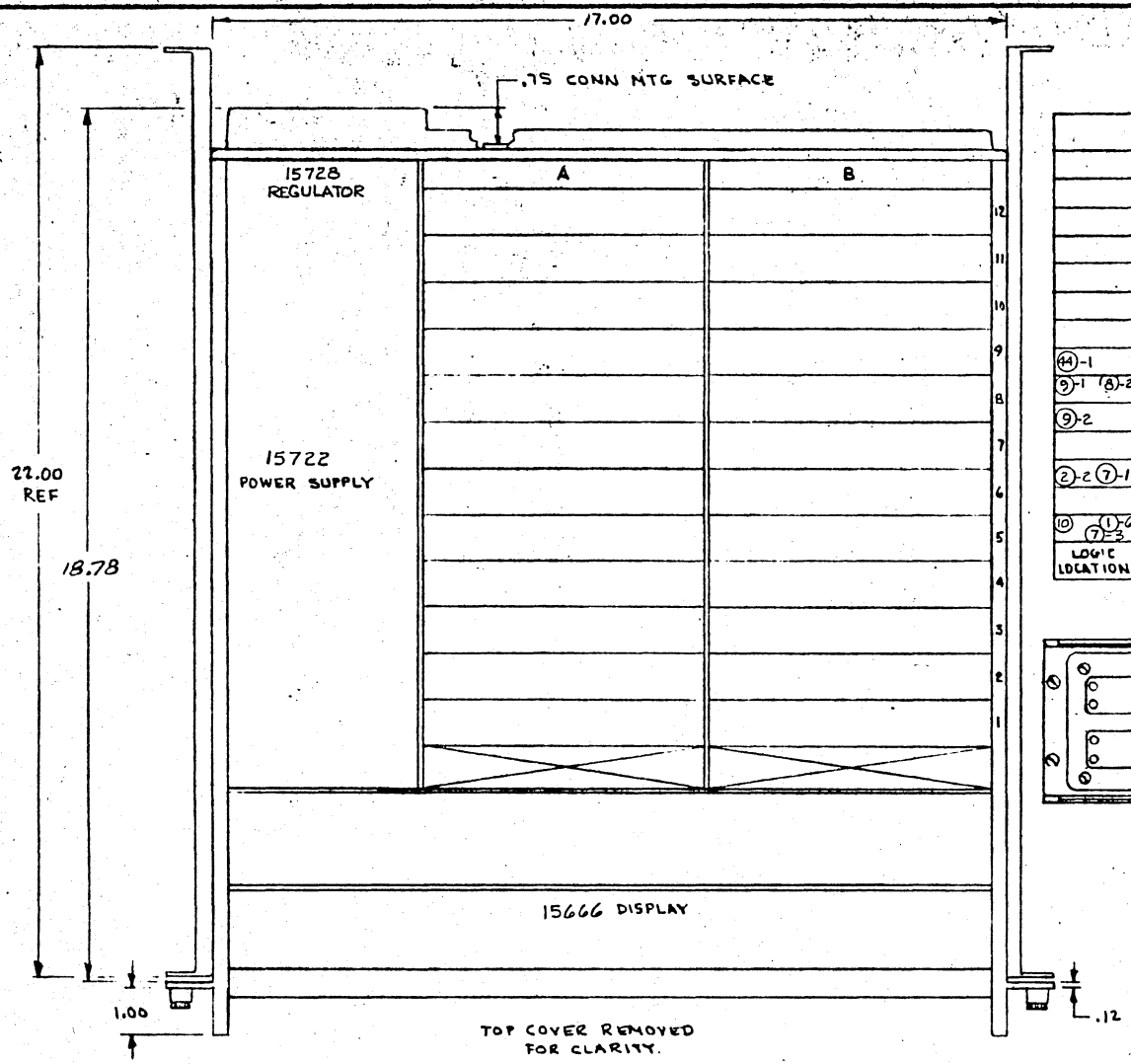
DRAWN: L. MALENA QUANTITY: _____ ASS'Y NO: 15672

REV

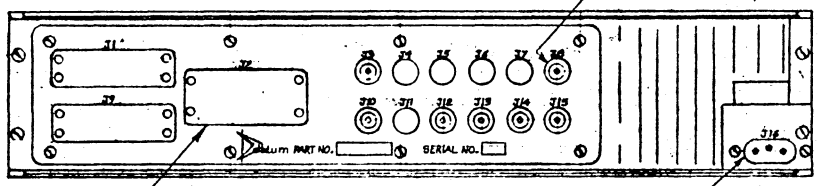
SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	UNIT TOTAL	LOT TOTAL	UNIT COST		REF. DES.
29	0500-0366	DIODE IN914A	DATUM	3				CR2, 3, 4
30	0515-0361-2	DIODE, ZENER, 1N961B, 10V	"	1				CR1
31	0500-0116	DIODE, SILICON, 3 JUNCTION	"	1				CR5
32	0550-0520	TRANSISTOR MJE 520	"	1				Q5
33	0550-7700	" 2N3643	"	2				Q2, Q4
34	0550-7705	TRANSISTOR 2N3565	"	2				Q1, 3
35								
36	1706-2010	TERMINAL 2010B	"	4				TP1-4
37								
38								
39	2303-0001	HEAT SINK PA2-1CB	"	1				Q5
40								
41	A-15672	ASSY AID DWG	"	REF				
42	17034I	P.C. BOARD	DATUM	1				

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

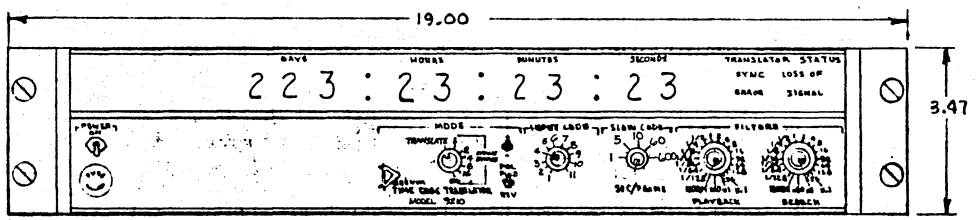


A				B			
	12				12		
	11			(29)-1	11	15672	SLOW CODE
	10				10		
	9				9		
	8				8		
	7				7		
	6			(44)-2	6	15663	36 BIT BUFFER
(44)-1	5	15663	36 BIT BUFFER	(8)-1	5	15662	MINOR TIME
(9)-1 (8)-2	4	15664	MAJOR TIME	(5)-2 (7)-2	4	15788	DECODE #2
(9)-2	3	15663	36 BIT BUFFER	(1)-4 (2)-1 (5)-1	3	15673	DECODE #1
	2			(1)-2	2	15585	FILTER
(2)-2 (7)-1	1	15675	SYNC MODE	(1)-1	1	15584	AGC
(10) (7) (1)-6 (2)-3	JDS	15666	DISPLAY	(1)-3	TB2	15603	FILTER SWITCH
LOGIC LOCATION	PHYSICAL LOCATION	ASSY NO.	TITLE	LOGIC LOCATION	PHYSICAL LOCATION	ASSY NO.	TITLE



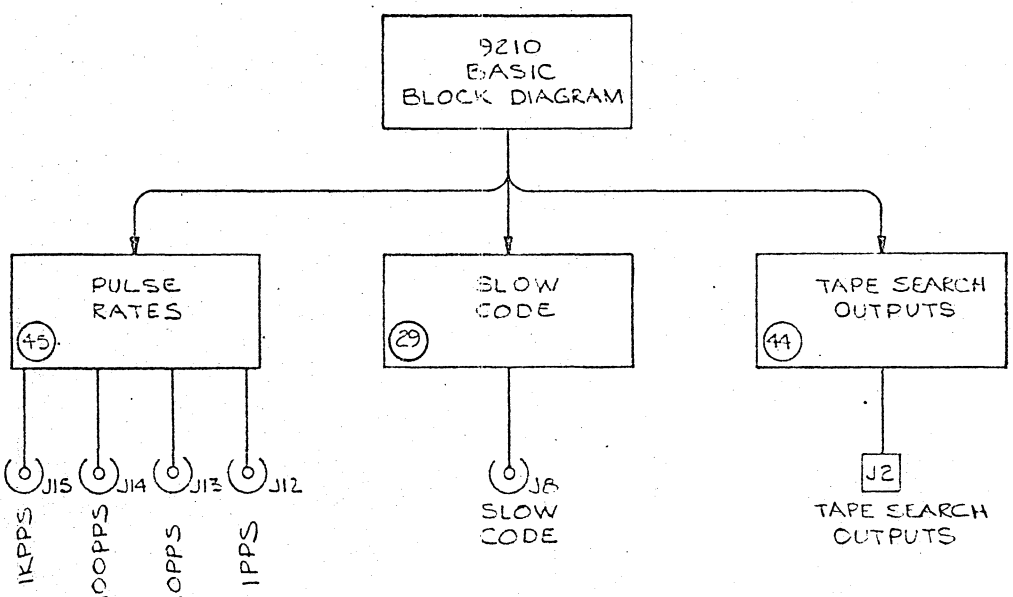
REAR VIEW

4. SEE 9210 MODIFICATION 9210-8017
   801549 (SLOW CODE), 801550 (MODIF. TO BASIC)
3. SEE WIRELIST-801525 (BASIC), 801206 (TAPESEARCH), 801524 (PULSE RATES)
   - J16 - AC POWER
   - J15 - 1KPPS
   - J14 - 100PPS
   - J13 - 10PPS
   - J12 - 1PPS
   - J11 -
   - J10 CODE INPUT (LO)
   - J9 -
   - J8 - SLOW CODE
   - J7 -
   - J6 -
   - J5 -
   - J4 -
   - J3 - CODE INPUT (HI)
   - J2 - TAPE SEARCH OUTPUTS
2. J1 -
1. JONATHAN # 110 QDP20-2 TILT SLIDES SUPPLIED (23" TRAVEL).



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .02 ANGLES ± 1/2°	TITLE: TIME CODE TRANSLATOR		Datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA
	DWN MARTINEZ 4/27/72	DES	9210-111A
	CHK	ENGR HELMS 5/11/72	
	SCALE NONE	FSC 21160	SIZE — SHT 1 OF 1 — REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



(9) 9110-8082
(44) 9310-8082
(45) 9310-8113

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

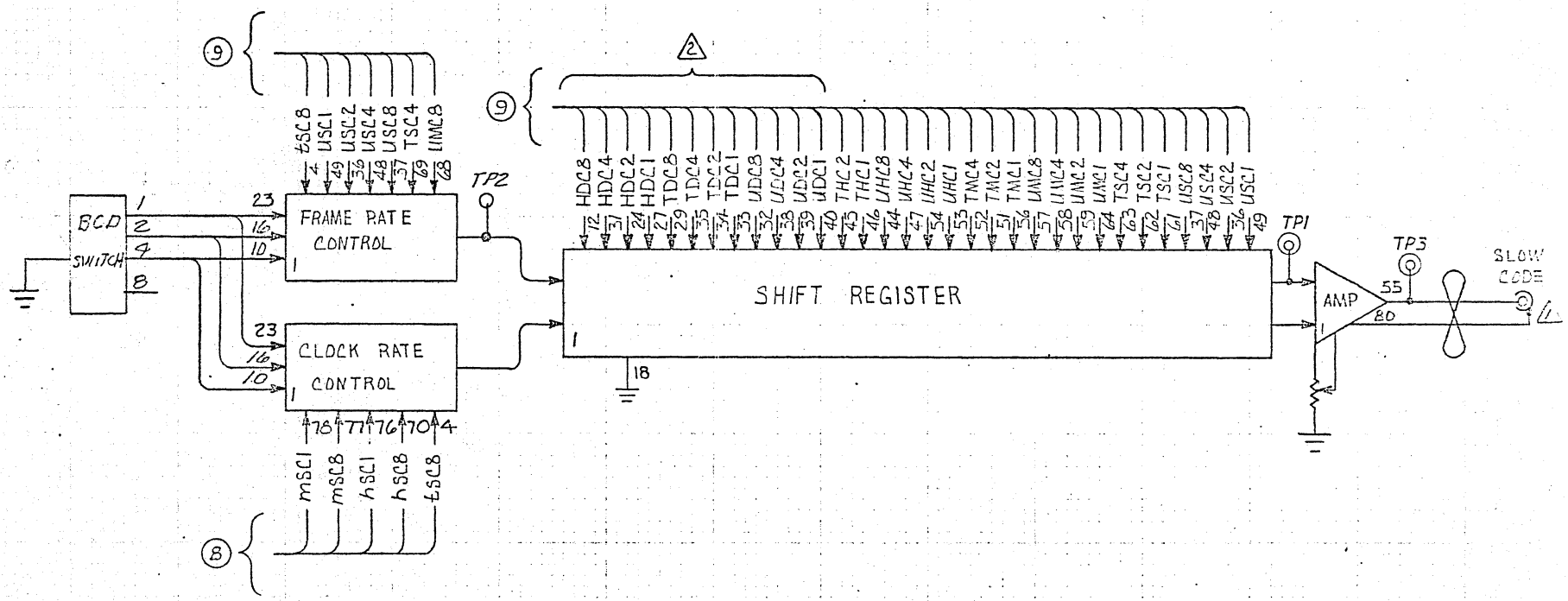
TITLE
9210-111A
BLOCK DIAGRAM

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	CHK	DES	ENGR
MARTINEZ 5/27/72			

SCALE NONE | FSC 31160 | B | 9210-8013 | SIZE | SHT 1 OF 1 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



⚠2 GND IF DAYS NOT USED

NOTES: ⚠1 SEE TOP ASSY FOR CONN NO.

1		15672	SLOW CODE S-M-H-D
LOGIC LOCATION	PHYSICAL LOCATION	ASSY NO.	TITLE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE

5 RATE

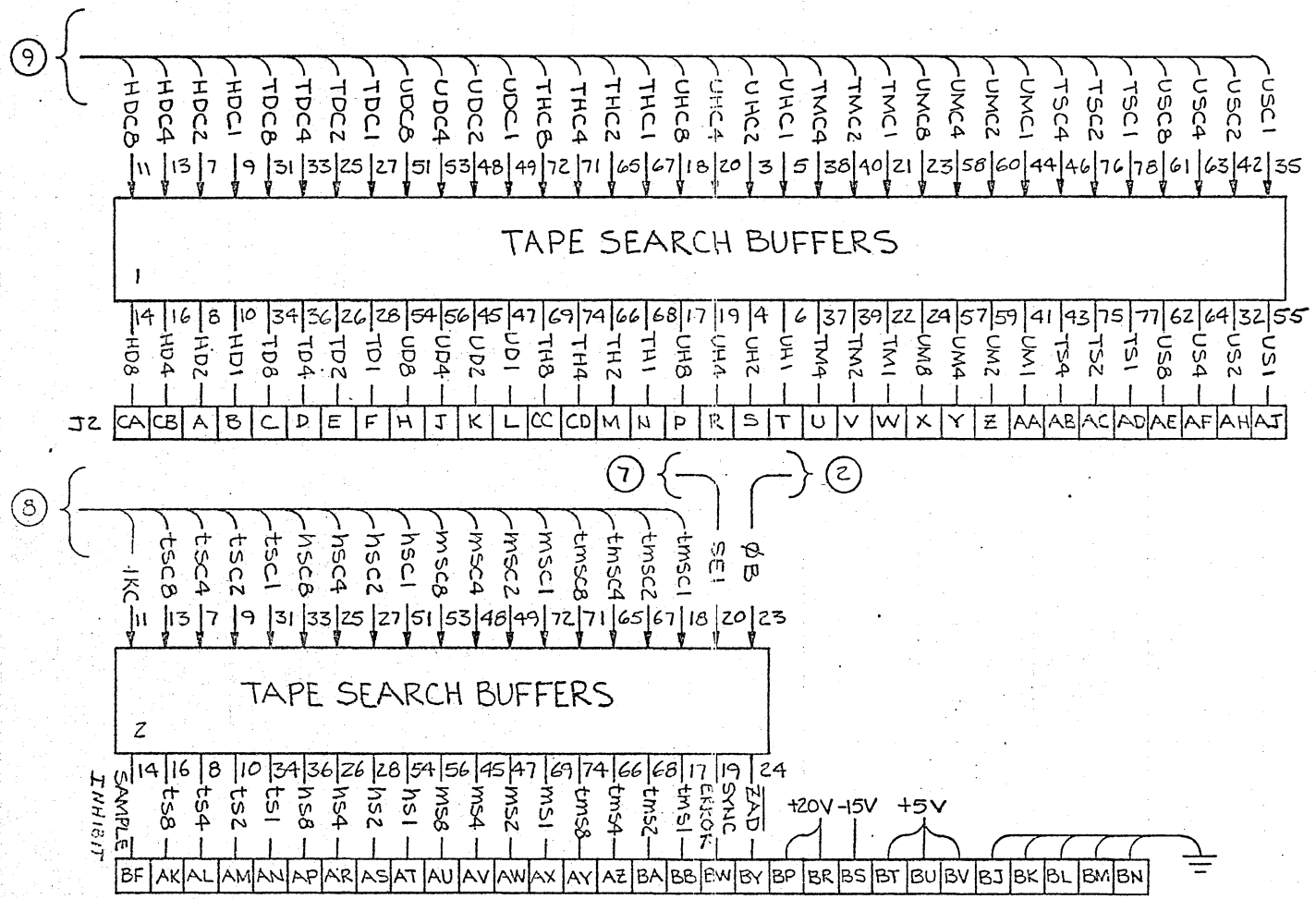
(S) SLOW CODE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	L. MALENA	4/30/71	DES		
CHK			ENGR		
SCALE			FSC	31160	

SIZE | SHT | OF | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



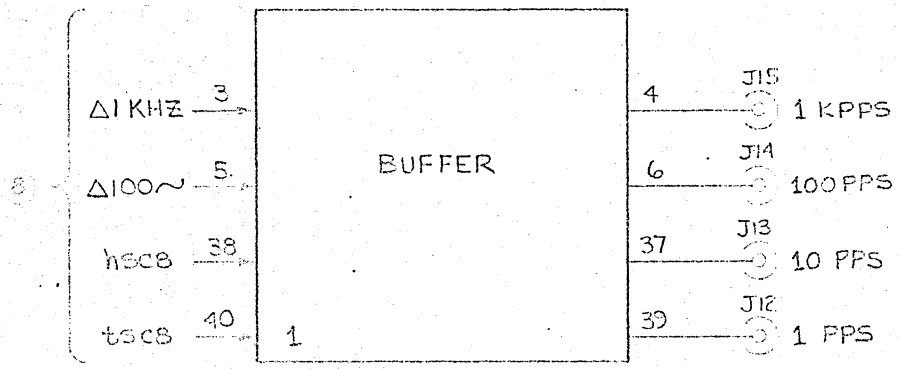
LOGIC LOCATION	PHYSICAL LOCATION	ASSY. NO.	TITLE
2		15663	36 BIT BUFFER
1		15663	36 BIT BUFFER

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE
TAPE SEARCH OUTPUT LOGIC
(11)

DWN MARTINEZ	2/26/71	DES [illegible]	2/26		
CHK [illegible]	2/26	ENGR [illegible]	2/26		
SCALE NONE		FSC 31160		SIZE B	9310-8082
				SHT 1 OF 1	REV

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA



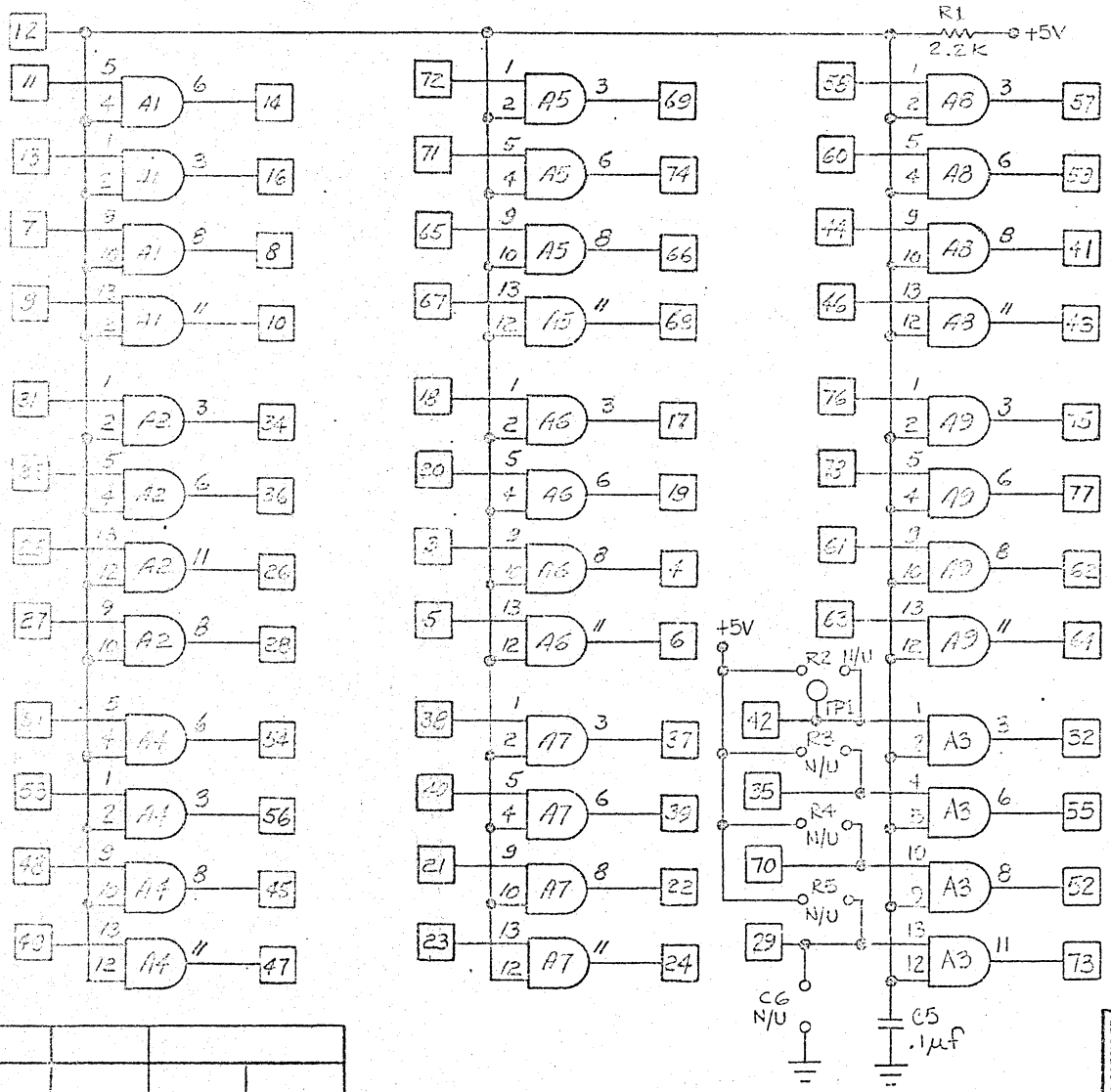
1		15663	36 BIT BUFFER
LOGIC LOCATION	PHYSICAL LOCATION	ASSY. No.	TITLE

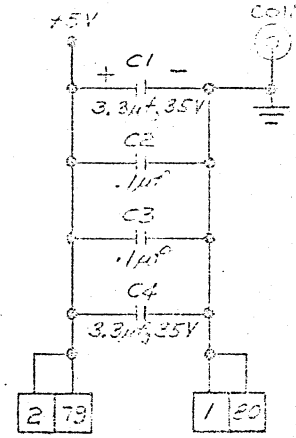
TITLE
PULSE RATES
15

KAIN

NONE

B 9310-0113





REVISIONS			
LTR	DESCRIPTION	DATE	APPD

INPUTS	OUTPUTS		
SPECIFICATIONS			

USN7408	SPRAGUE	A1-A8
PART NO.	MFR.	COMPONENT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE

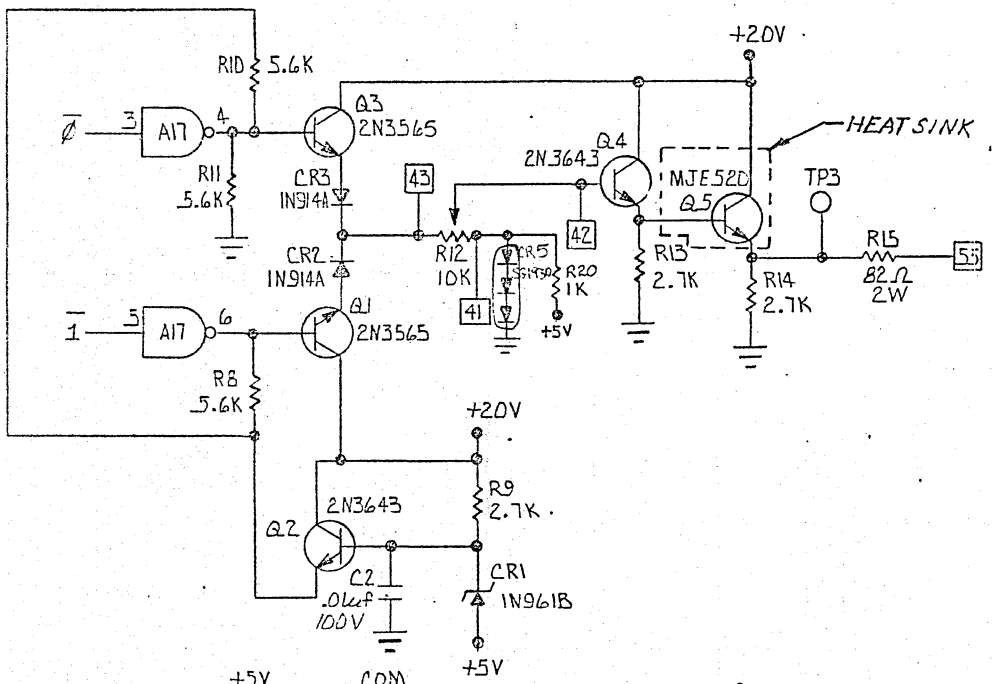
36 BIT BUFFER

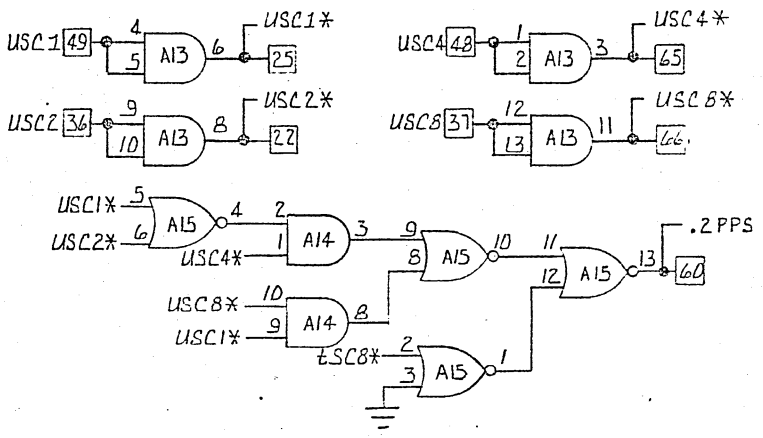
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

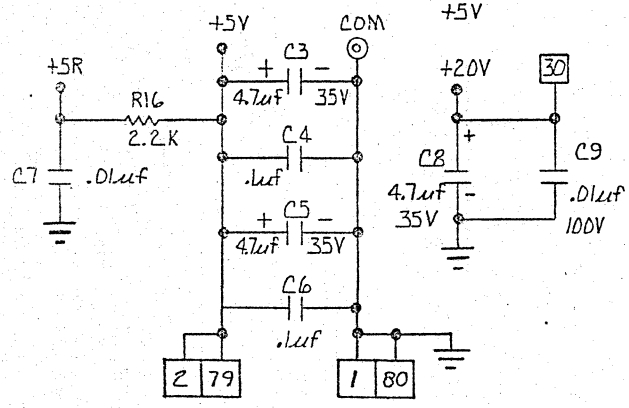
DWN [illegible] | DES [illegible] | CHK [illegible] | ENGR [illegible]

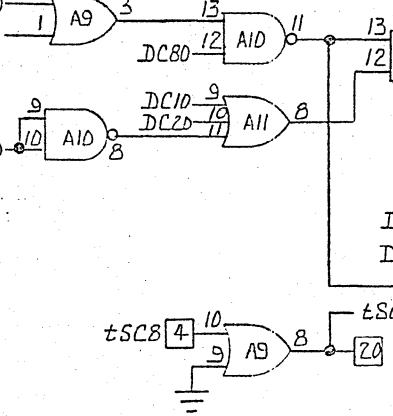
SCALE NONE | FSC 31190 | SIZE B | 15663 | SHT 1 OF 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADDED CR5 & R20. C10 WAS .01μf, 100V R17 WAS 680Ω, A5-14 WAS TO GND.	9-15-71	BM









UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°

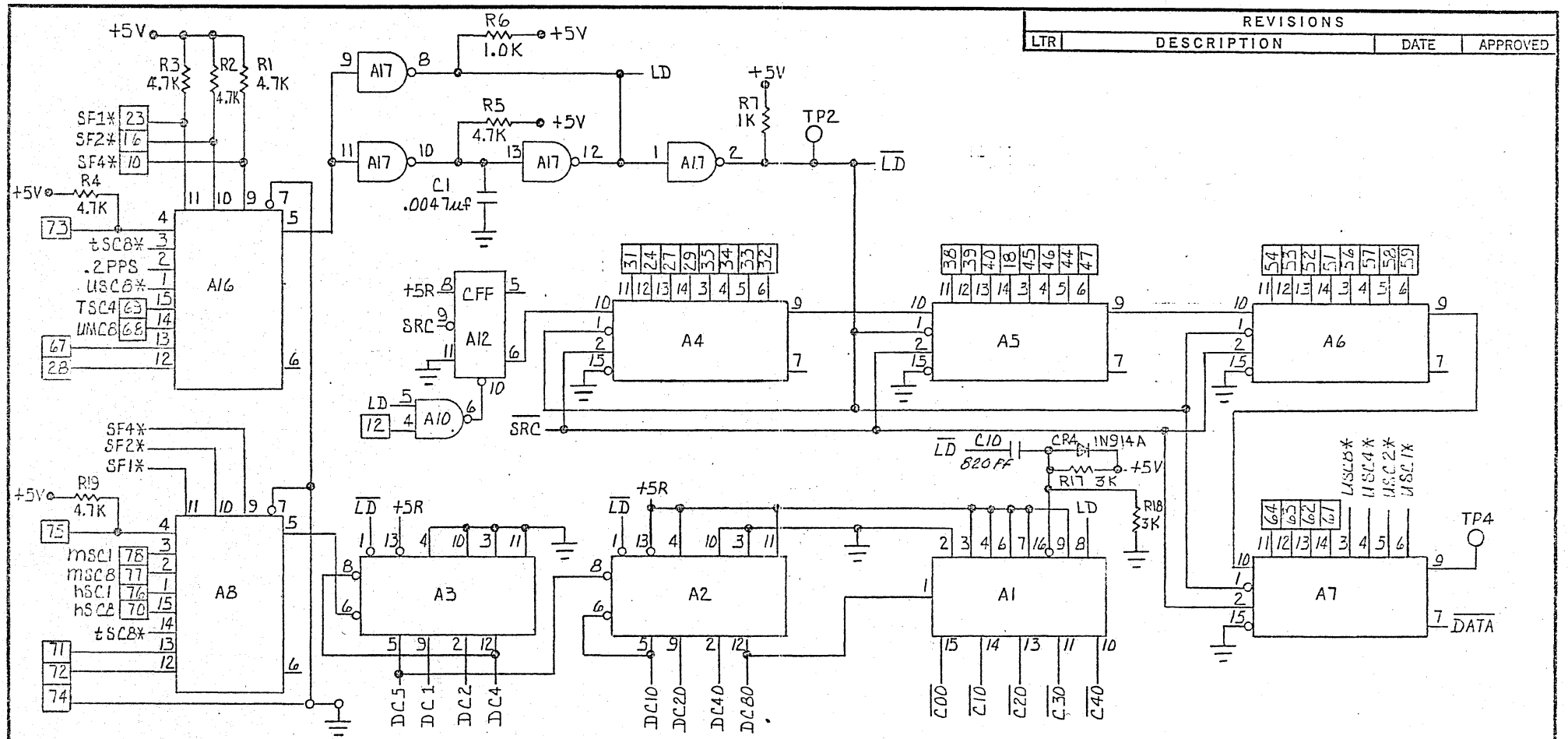
TITLE
SLOW CODE S-M-H-D

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	[illegible]	5-24-71	DES	[illegible]	6/10/71
CHK	[illegible]	5-28	ENGR	[illegible]	5-[illegible]
SCALE	NONE		FSC	31160	

B | 15672 | A

SIZE | SHT 1 OF 2 | REV



				N7432A-		NATIONAL	A9
SN74165		TEX. INST.	A4,5,6,7	N7418A			A11
SN74151		TEX INST.	A8,16	N7408A			A13 14
SN7496		TEX INST.	A1	N7406A			A17
N8280A		SIGNETICS	A2,3	N7402A			A15
N7407A		NATIONAL	A12	N7400A		NATIONAL	A10
PART NO.	ALTERNATE	MFR.	REF NO.	PART NO.	ALTERNATE	MFR.	REF NO.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: SLOW CODE S-M-H-D

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN L. MALENA	6-10-71	DES RM	6/11/71	B	15672
CHK	6-10	ENGR			
SCALE NONE		FSC 31160		SIZE	SHT 2 OF 2 REV

DATUM, INC. Timing Division ▪ 170 East Liberty Avenue ▪ Anaheim, California 92801 ▪ 714 / 879-3070 ▪ TWX 910 / 592-1289