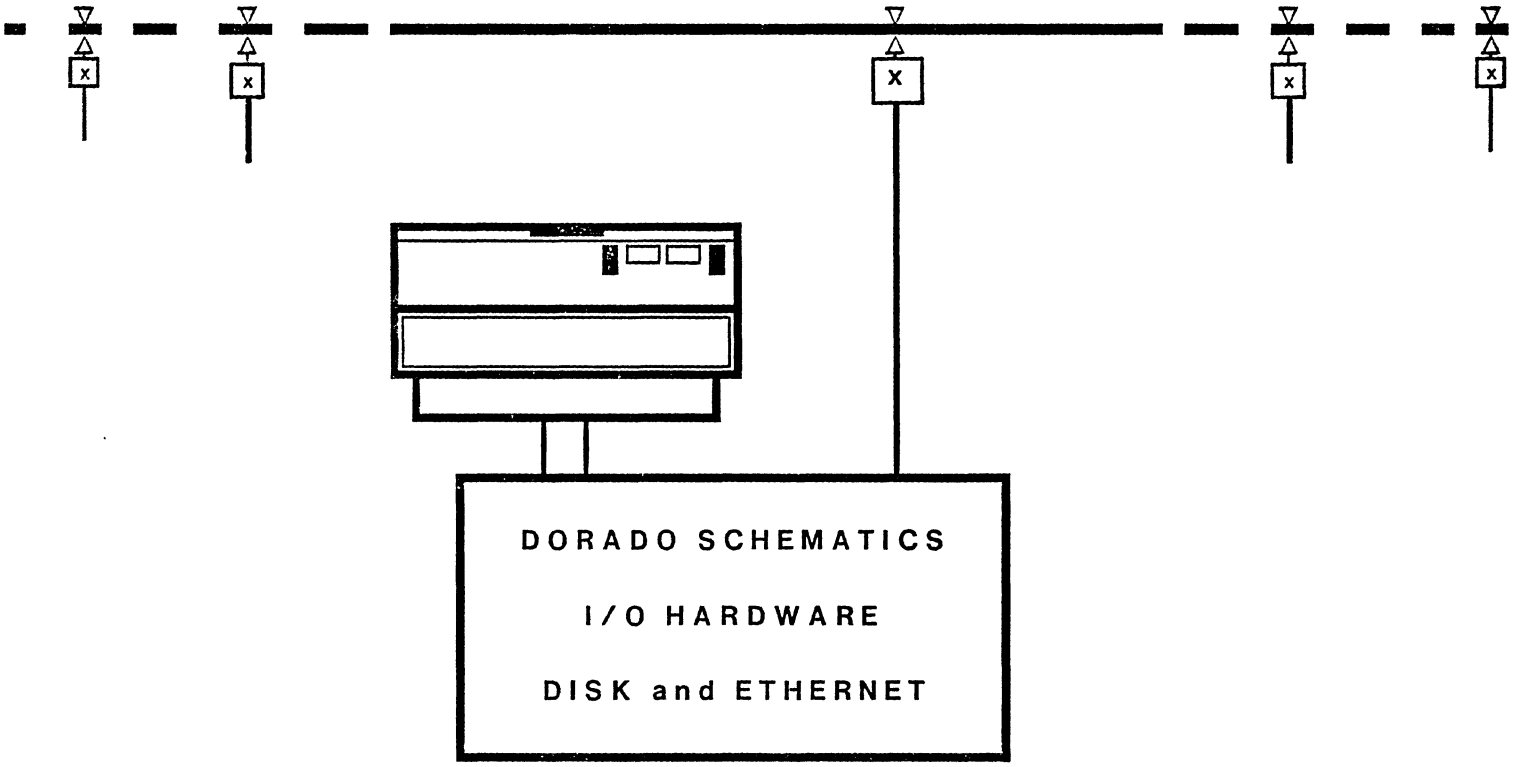
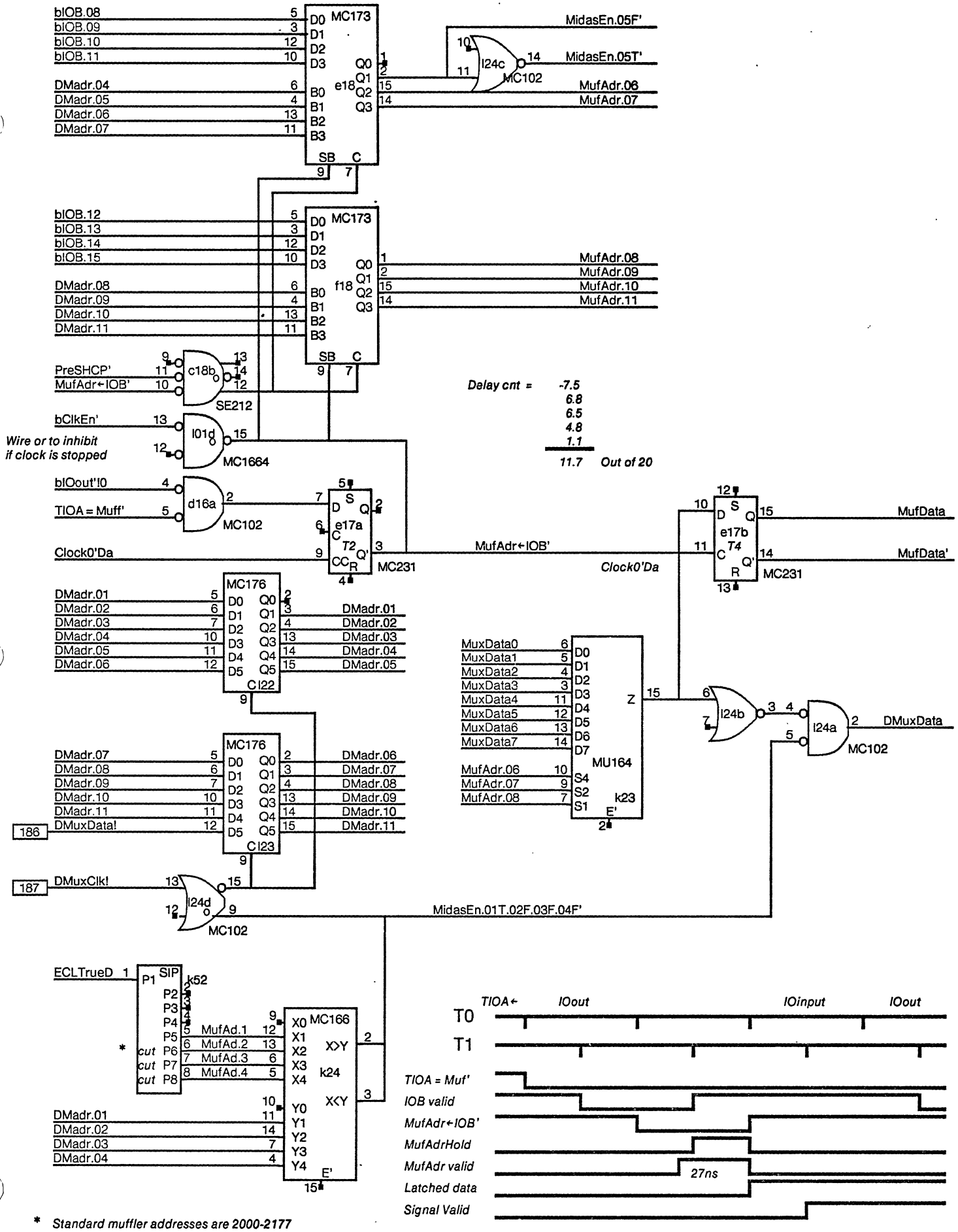


DORADO SCHEMATICS

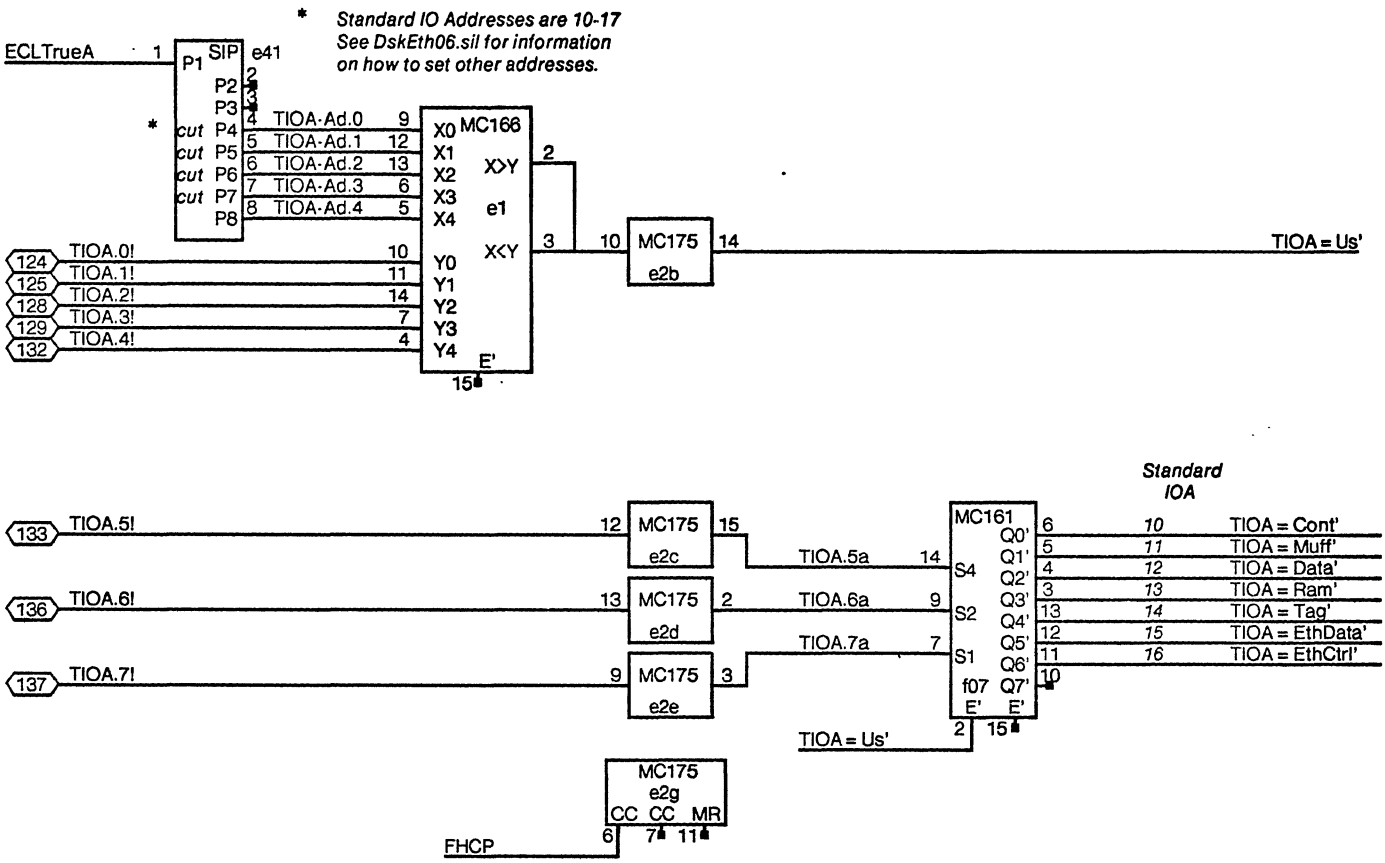
I/O HARDWARE

DISK and ETHERNET



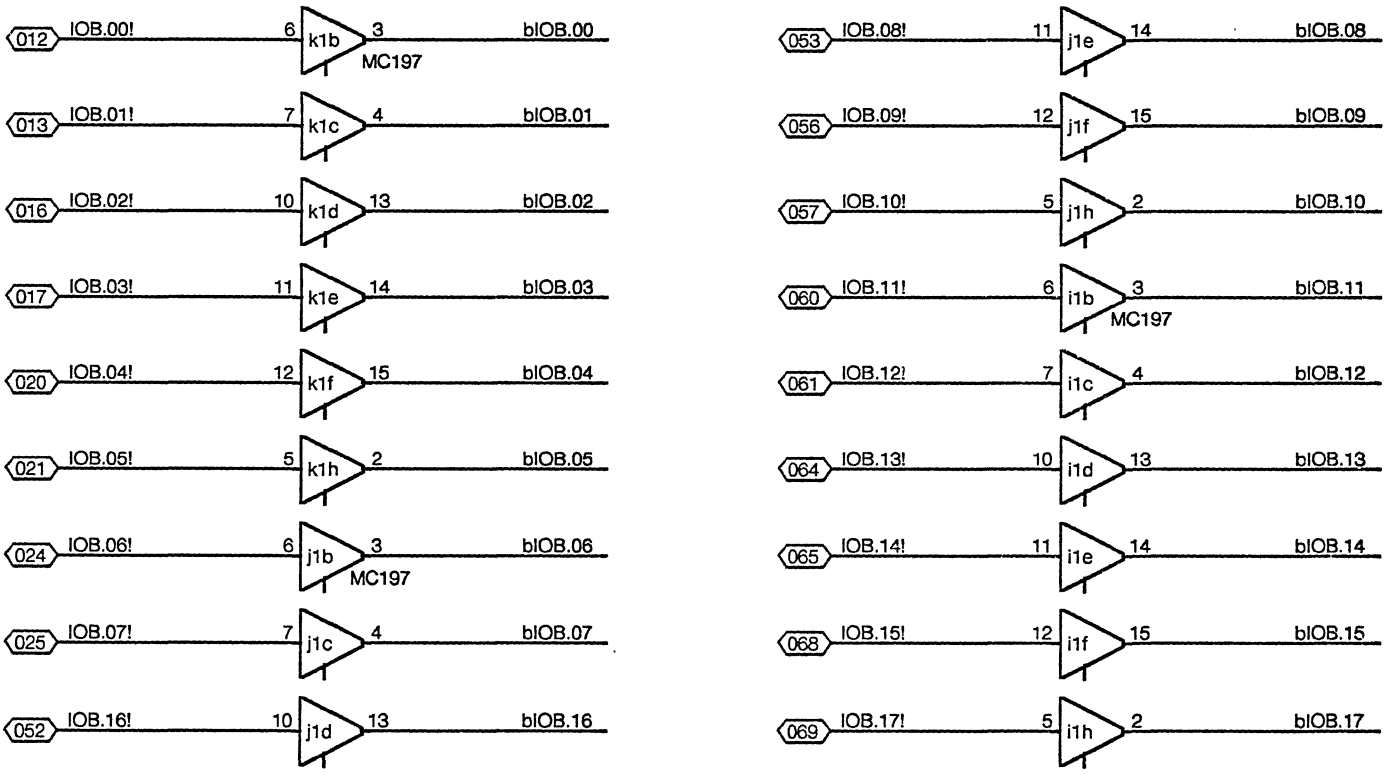
* *Standard muffler addresses are 2000-2177*
See DskEth06.sil for information
on how to set other addresses

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMux Control	DskEth01.sil	Roger Bates	Ce	7/19/79	01



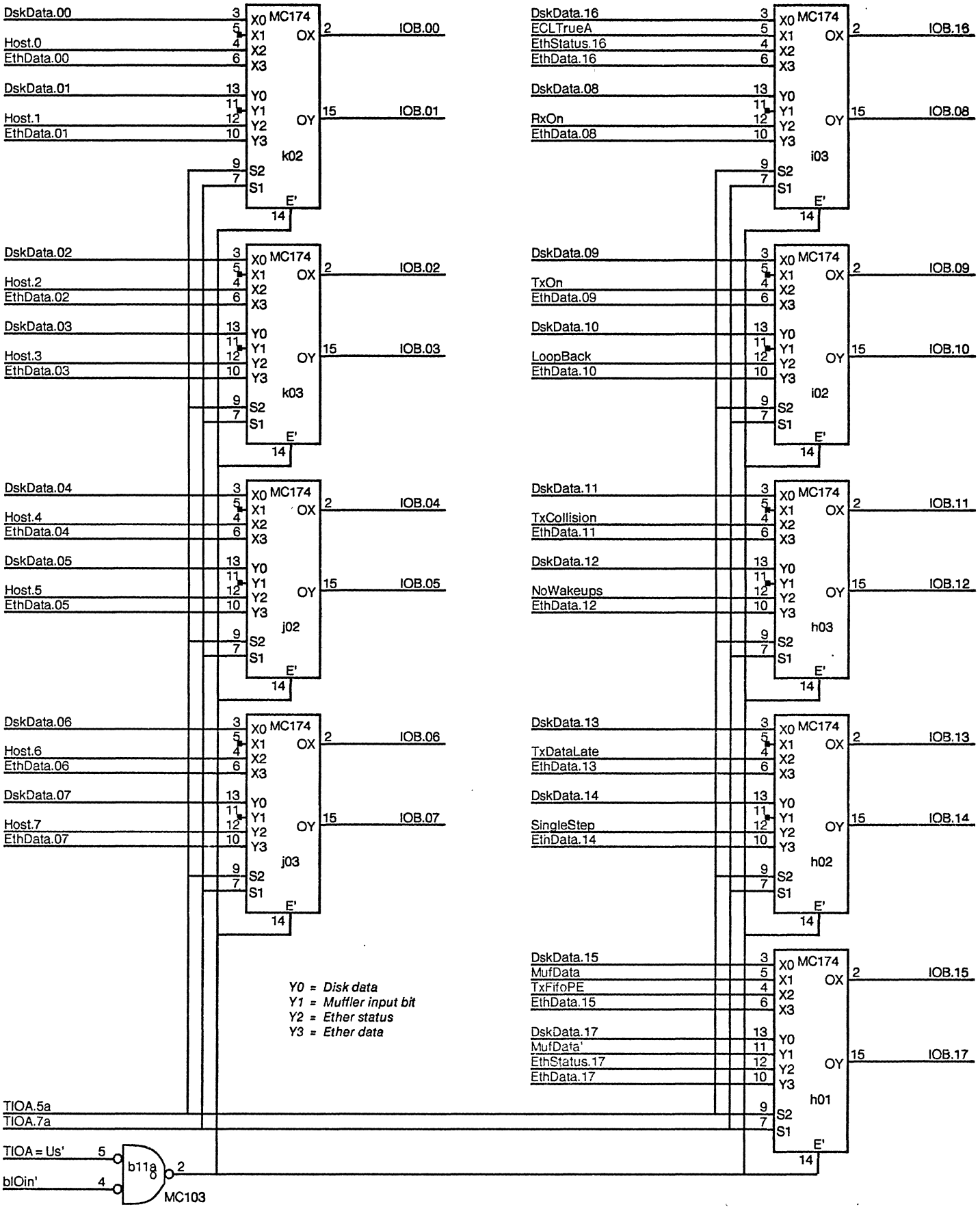
IO Address decoding

IOB receivers

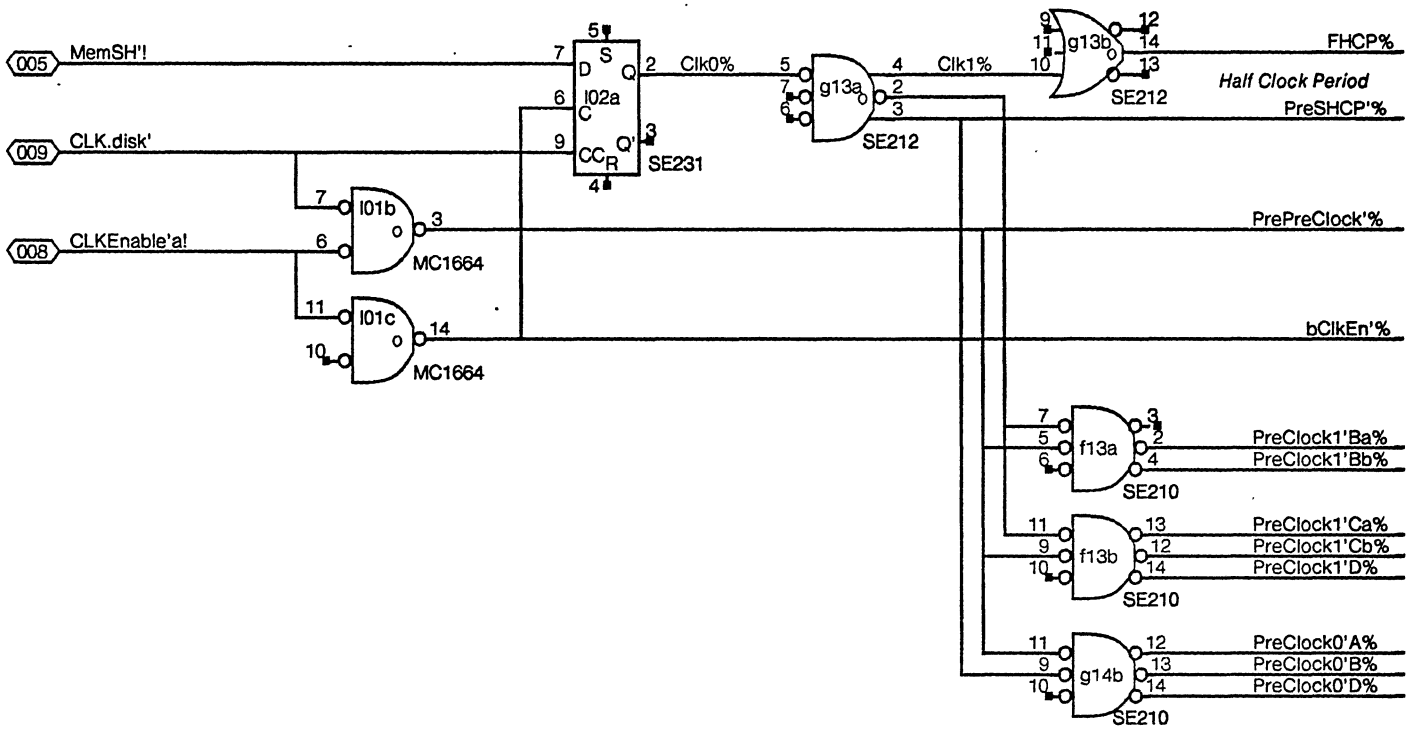


NOTE: IOB data received by this board is tested as part of the disk controller (Pg 18) Both the disk and the Ethernet check the data parity after it has gone through the respective FIFO's.

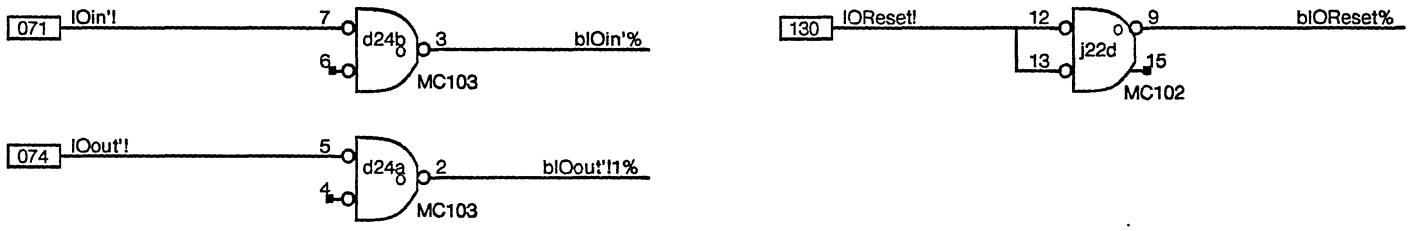
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	IOA & IOB	DskEth02.sil	Bates/Boggs	Ce	7/19/79	02



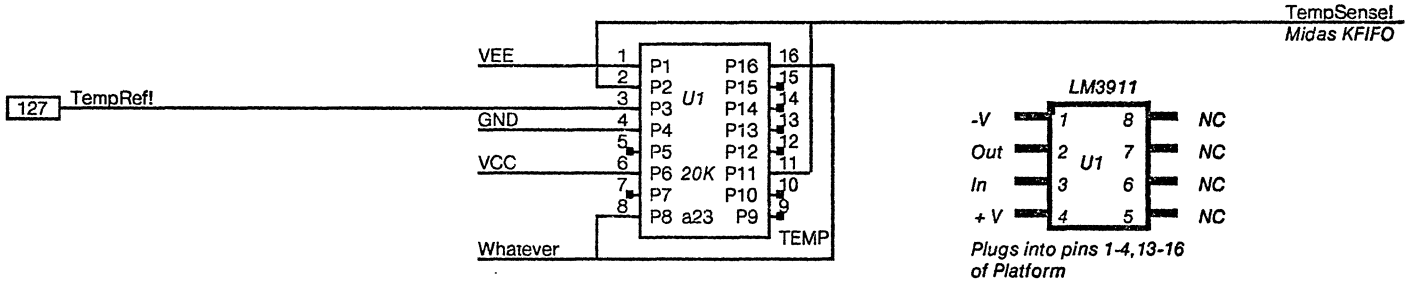
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	IOB data Select/Drivers	DskEth03.sil	Bates/Boggs	Ce	9/24/79	03



Common Clock circuitry



Common IO circuitry



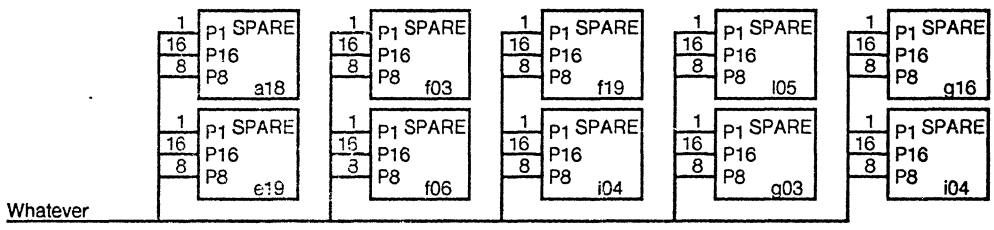
Temperature Sensor

Power connections are as follows:

Stitch-Weld: 1 & 16 are GND
8 is -5

Multiwire: 16 is GND
8 is -5

except in locations
a18, g03, and g16
which are uncommitted



Spare Socket locations for Multiwire

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clocks & IO Signals	DskEth04.sil	Bates/Boggs	Ce	7/23/79	04

-2v	Drive 3	Drive 2	IOA	Drive 1	Drive 0	IOB	Ethernet	IOB	Clk	+ 12v

	A (184)	B (168)	C (152)	D (136)	E (120)	F (102)	G (84)	H (68)	I (52)	J (36)	K (20)	L	
1	Sec Cnt LS169 X	8,13 MC102	Disk IO MC1650	Sec Cnt LS08	TIOA MC166 X	Disk IO MC1650	Dr Cont 8T98	IOB MC174 X	IOB MC197	IOB MC197	IOB MC197	Clock ,13 MC1664	1
41		SIP		SIP	SIP		SIP	SIP					41
2	Sec Cnt LS169 X	MC125	Disk IO MC1650	Disk IO N125	TIOA MC175	Disk IO MC1650	Disk IO N125	IOB MC174 X	MC174 X	MC174 X	IOB MC174 X	Clock SE231	2
3	Sec Cnt N123	ECC MC176	MC124	Sec Cnt LS153 X	TW MC109			IOB MC174 X	IOB MC174 X	IOB MC174 X	IOB MC174 X	5,6,12 MC195	3
42				SIP			IOB SIP						42
4	Sec Cnt PLAT X	ECC MC176	ECC MC113	Dr Cont LS174 X	TW MC231	IOB MC170 X	IOB MC170 X	Rx TW MC231		Tx TW MC231	Rx Tw MC135	5,6 MC231	4
5	Sec Cnt N123	ECC MC176	ECC MC113	Dr Cont S288 X	TW MC231	Disk IO MC174 X	Host MC170 X	TW Com MC109	4,5 MC103	Rx CRC F9401 X	5,11 MC102		5
43													43
6	Sec Cnt LS169 X	ECC MC176	Clock ,8 SE212	Dr Cont LS155 X	TW Bit Cl MC231		Test MC175	4,8 MC231	Clock SE212	Clock SE210	RxCRC,11 MC125	6,4 MC135	6
7	Sec Cnt LS169 X	ECC MC158	ECC MC176	MC102	Muf MU164 X	TIOA MC161 X	Test MC158	1,4,10 MC124	Clock SE210	Clock SE210	RxSR Dmp MC135	Rx EOP MC231	7
44													44
8	Sec Cnt LS174 X	ECC,9 MC158	ECC MC176	FIFO F145A X	Out Reg MC176 X	Sh Reg MC176 X	In Reg MC173 X	Rx FSM MC176	Rx SR MC141 X	Rx Fifo F145A X	Rx Par MC170 X	4,12 MC105	8
9	Sec Cnt LS174 X	Out Reg MC231	MC231	FIFO F145A X	Out Reg MC170 X	Sh Reg F00 X	In Reg MC173 X	Rx FSM MCM149 X	Rx SR MC141 X	Rx Fifo F145A X	Rx Reg MC176 X	Rx Write F16 X	9
45													45
10	Sec Cnt LS174 X	Bit Cl F16 X	MC104	FIFO F145A X	Out Reg MC176 X	Sh Reg F00 X	In Reg MC173 X	Rx FSM MCM149 X	Rx SR MC141 X	Rx Fifo F145A X	Rx Reg MC176 X	Rx Fifo MCM149 X	10
11	Sec Cnt LS174 X	MC103	MC103	FIFO F145A X	Out Reg MC170 X	Sh Reg F00 X	In Reg MC173 X	Rx FSM MCM149 X	Rx SR MC141 X	Rx Fifo F145A X	Rx Reg MC176 X	Rx Fifo MC158 X	11
46													46
12	Muf MU164 X	MC231	MC195	FIFO F145A X	Out Reg MC176 X	Sh Reg F00 X	In Reg MC173 X	Rx FSM MC176	Rx FSM MC136 X	Rx Fifo F145A X	Rx Par MC170 X	Rx Read F16 X	12
13	Muf MU164 X	Muf MU164 X	Errors MC197	MC102	Cont MC135	Clock SE210	Clock SE212	Tx FSM MC176	Tx FSM MC136 X	Tx Fifo F145A X	Tx Par MC170 X	Tx Write F16 X	13
47													47
14	Fifo Cnt MC158 X	Fifo Cnt MCM149 X	Fifo Cnt ,4 MC176	Cont MC171 X	Cont MC231	Cont F00 X	Clock SE210	Tx FSM MCM149 X	Tx SR MC141 X	Tx Fifo F145A X	Tx Reg MC176 X	Tx Fifo MC158 X	14
15	Fifo Cnt F16 X	Fifo Cnt MC231	Fifo Cnt MC231	Bit Cl SE210	Cont MC231	Cont F00 X	Tx FSM MC102	Tx FSM MCM149 X	Tx SR MC141 X	Tx Fifo F145A X	Tx Reg MC176 X	Tx Fifo MCM149 X	15
48													48
16	Fifo Cnt F16 X	Clock SE212	Cont MC135	Fifo Cnt ,2 MC102	Ram MC145A X	Ram MC145A X		Tx FSM MCM149 X	Tx SR MC141 X	Tx Fifo F145A X	Tx Reg MC176 X	Tx Read F16 X	16
17	Muf MU164 X	Clock SE211	Clock SE210	TAG MC125	Muf MC231	Ram MC145A X	Tx CRC F9401 X	Tx FSM MC176	Tx SR MC141 X	Tx Fifo F145A X	Tx Par MC170 X	8,10 MC105	17
49													49
18		Clock SE210	Clock SE212	Muf MC173 X	Muf MC173 X	Muf MC173 X	ETX MU164 X	Tx CRC MC125	Clock SE210	Clock SE210	9,10 MC104	FIFOs MC176	18
19	3, 5 MC100	MC195	CNT MC136 X	Disk Muf MC173 X			ERX MU164 X	ETX MU164 X	EFIFO MU164 X	Pend MC135	Coll MC135	GotBit MC135	19
50													50
20	Ram MC139 X	Ram F16	CNT MC136 X	TAG MC135	TAG MC173 X	TAG MC173 X	Rx PD MC176 X	ERX MU164 X	8,12 MC124	Ether Clk K1115A X	TxGo MC231	Tx PE MC231	20
21	Ram MC139 X	Ram F16 X	CNT MC136 X	TAG MCM149 X	TAG MC173 X	TAG MC173 X	Rx PD F16 X	9, PE MC106	Ether Clk MC210	Ether Clk MC136 X	Status MC170 X	EFIFO MU164 X	21
51													51
22	Ram F16 X	Muf MU164 X	Muf MU164 X	TAG F16 X	TAG MC125	TAG MC125	TAG 8T98	Rx PD MCM149 X	10 MC231	7,10.11.13 MC102	7, 8 MC135	Muf MC176 X	22
23	Temp LM3911 X	Dr Stat MC109	Dr Stat MC103	Muf MU164 X	TAG MC125	TAG MC125	TAG 8T98	Next,8 MC105	Next,7,12 MC104	Next MC113	Muf MU164 X	Muf MC176 X	23
52				SIP	SIP					SIP	SIP		52
24	Next MC195	Dr Stat MC124	Dr Stat MC124	Clock MC103	Muf MU164 X	Muf MU164 X	TAG 8T98	Next MC176	Next MC104	5,6,13 MC176	Muf MC166 X	Muf MC102	24

	A	B	C	D	E	F	G	H	I	J	K	L	
	(10)	(26)	(42)	(58)	(74)	(92)	(110)	(126)	(142)	(158)	(174)		

-5v	Next	Disk daisy chain cable	IOAtt	Muffler	+ 5v

31	chips common to Disk & Ether
137	chips specific to Disk
111	chips specific to Ether
9	spare chip positions
288	total chip positions

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Stitch-Weld board Layout	DskEth05.sil	Bates/Boggs	Ce	9/24/79	05

Cut SIP legs at k52 to set the
Muffler addresses for the board.
* Standard addresses are 2000-2177.

	Muff Addr	P5	P6	P7	P8
	0000-0177	cut	cut	cut	cut
	0200-0377	cut	cut	cut	
	0400-0577	cut	cut		cut
	0600-0777	cut	cut		
	1000-1177	cut		cut	cut
	1200-1377	cut		cut	
	1400-1577	cut			cut
	1600-1777	cut			
*	2000-2177		cut	cut	cut
	2200-2377		cut	cut	
	2400-2577		cut		cut
	2600-2777		cut		
	3000-3177			cut	cut
	3200-3377			cut	
	3400-3577				cut
	3600-3777				

Cut SIP legs at j52 to set the
Task numbers for the Ethernet.
* Standard tasks are 6 & 7.

	Tasks	P6	P7	P8
	2 & 3			cut
	4 & 5		cut	
*	6 & 7		cut	cut
	8 & 9	cut		
	10 & 11	cut		cut
	12 & 13	cut	cut	
	14 & 15	cut	cut	cut

Cut SIP legs at e41 to set the
IOA bus addresses for the board.
* Standard addresses are 10-17.

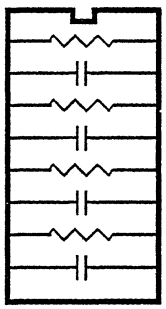
	IOA	P4	P5	P6	P7	P8
	000-007	cut	cut	cut	cut	cut
*	010-017	cut	cut	cut	cut	
	020-027	cut	cut	cut		cut
	030-037	cut	cut	cut		
	040-047	cut	cut		cut	cut
	050-057	cut	cut		cut	
	060-067	cut	cut			cut
	070-077	cut	cut			
	100-107	cut		cut	cut	cut
	110-117	cut		cut	cut	
	120-127	cut		cut		cut
	130-137	cut		cut		
	140-147	cut			cut	cut
	150-157	cut			cut	
	160-167	cut				cut
	170-177	cut				
	200-207		cut	cut	cut	cut
	210-217		cut	cut	cut	
	220-227		cut	cut		cut
	230-237		cut	cut	cut	
	240-247		cut		cut	cut
	250-257		cut			
	260-267		cut			cut
	270-277		cut			
	300-307			cut	cut	cut
	310-317			cut	cut	
	320-327			cut		cut
	330-337			cut		
	340-347				cut	cut
	350-357				cut	
	360-367					cut
	370-377					

The EtherFifo ROMs are identical and interchangeable.
The DiskRead, EtherRcvr and EtherXmtr ROMs are not.

Name	Type	#	Location		
DskEth					
Disk					
DiskRead	SG139	2	a20	a21	
DiskTag	MC149	1	d21		
DiskUnits	S288	1	d05		
DiskFifo	MC149	1	b14		
Ether					
EtherPD	MC149	1	h22		
EtherRcvr	MC149	3	h09	h10	h11
EtherFifo	MC149	2	l10	l15	
EtherXmtr	MC149	3	h14	h15	h16

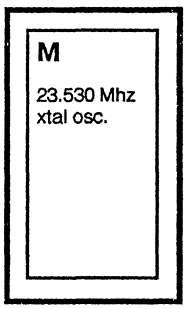
"DoradoProms DskEth" gets all proms for the DskEth board.
"DoradoProms Disk" gets all proms for the Trident half of the board.
"DoradoProms Ether" gets all proms for the Ethernet half of the board.

PLAT at a04

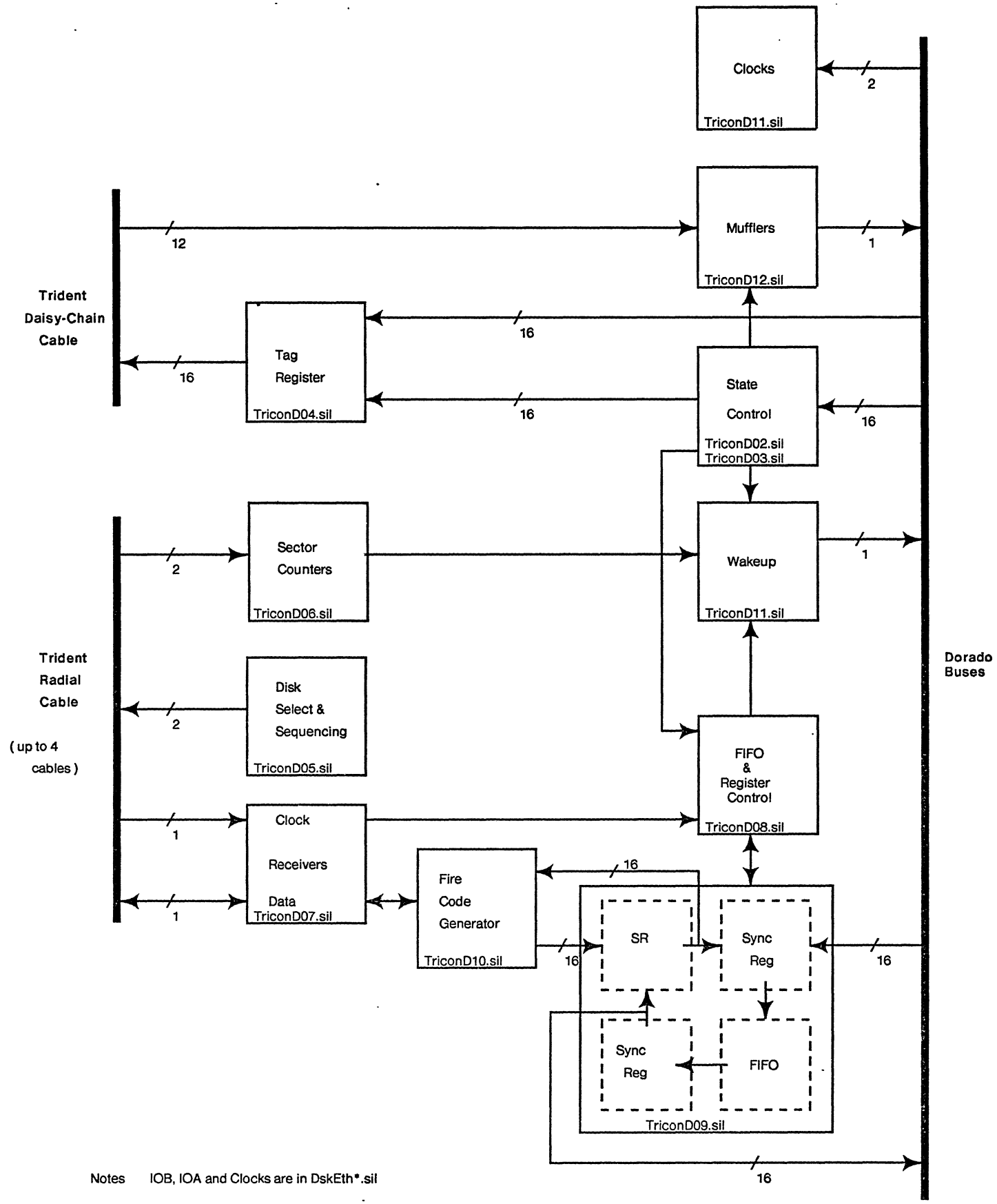


All resistors 27K
All capacitors 330pf

K1115A at j20

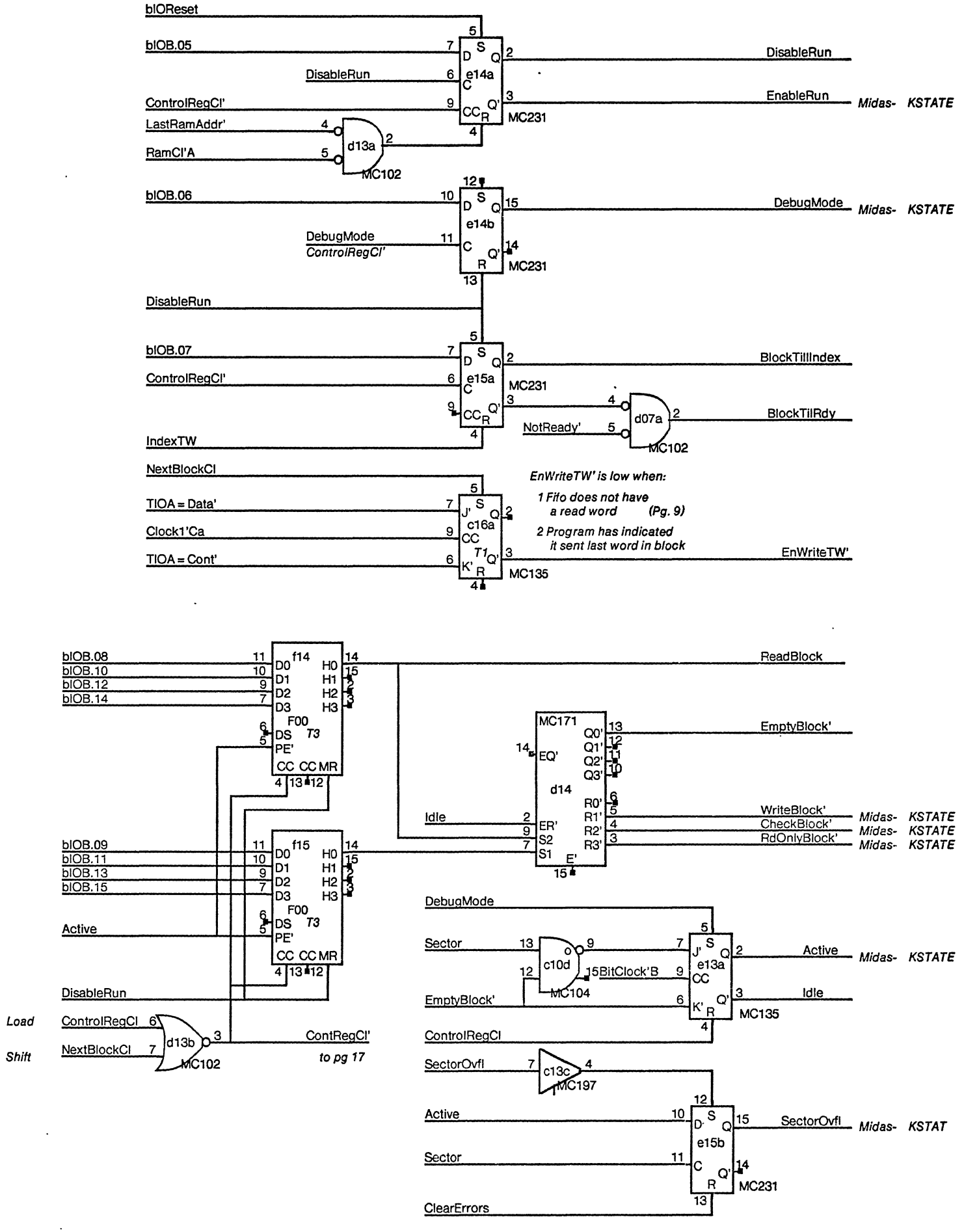


Logo is near pin 1.
This is a 14 pin pkg.
Board pins 8 & 9 aren't used.
Remove bypass cap above pin 1

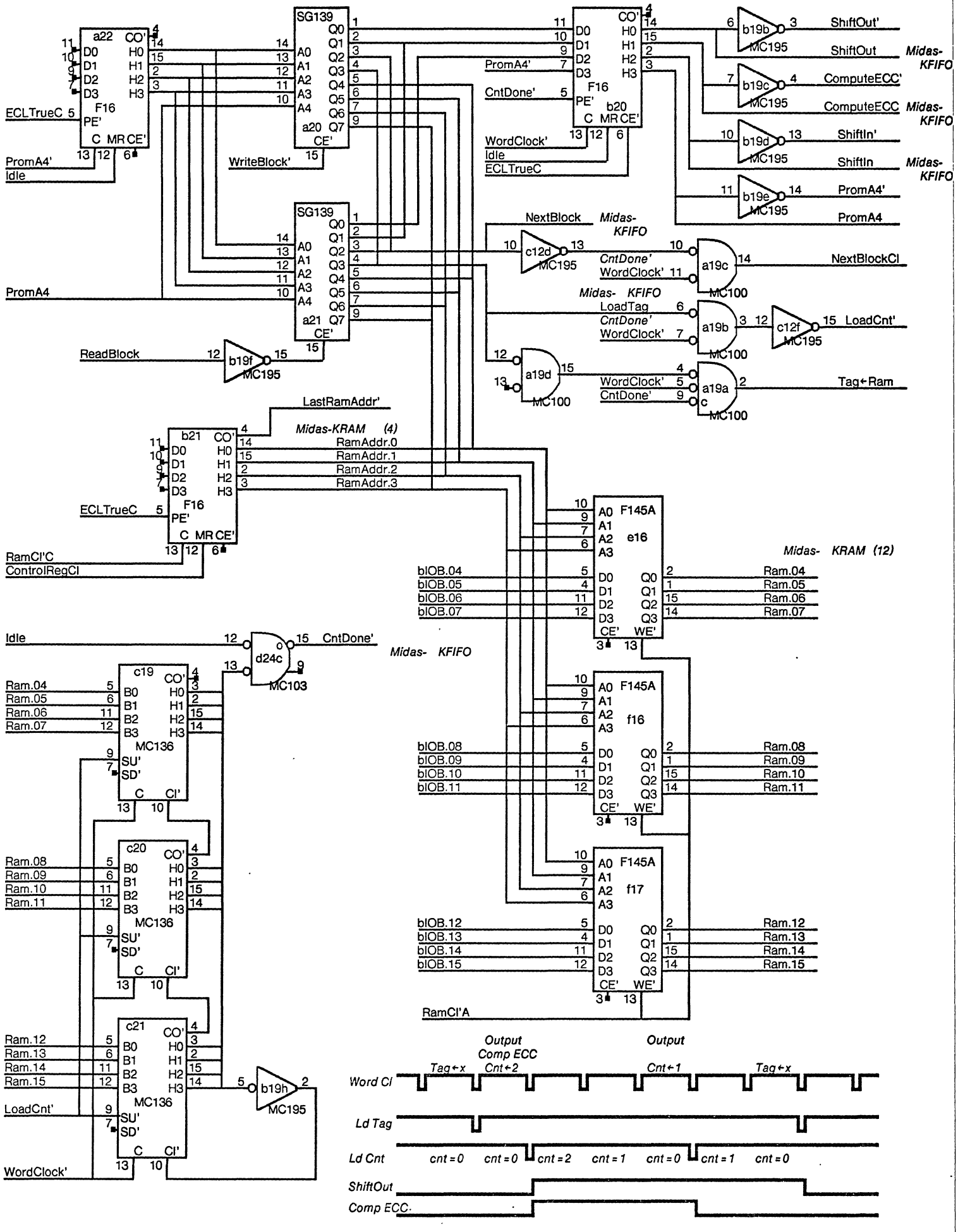


Notes IOB, IOA and Clocks are in DskEth*.sil

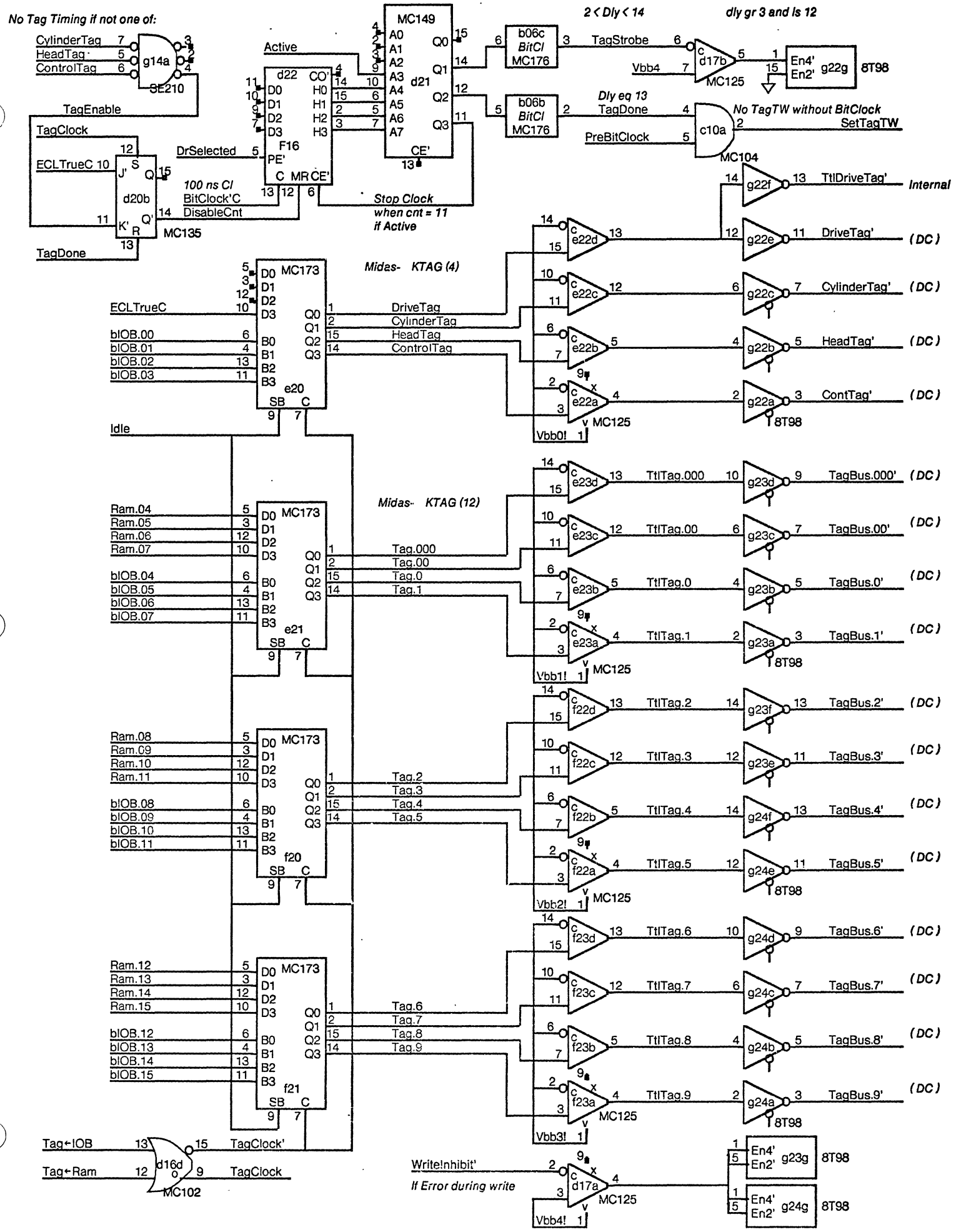
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Dorado Disc Controller	TriconD01.sil	Roger Bates	Ce	7/19/79	07



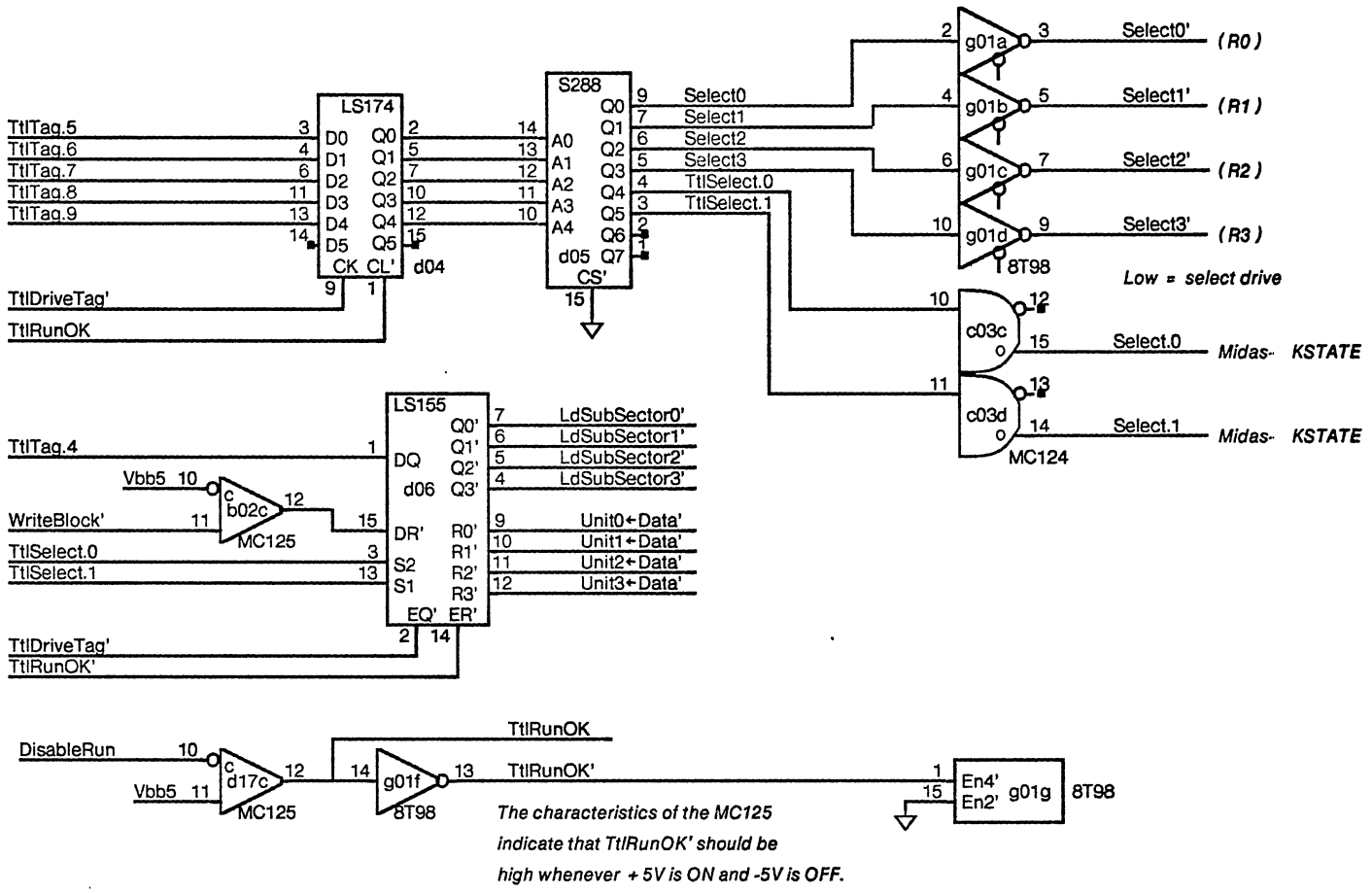
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	State Control Register	TriconD02.sil	Roger Bates	Ce	9/24/79	08

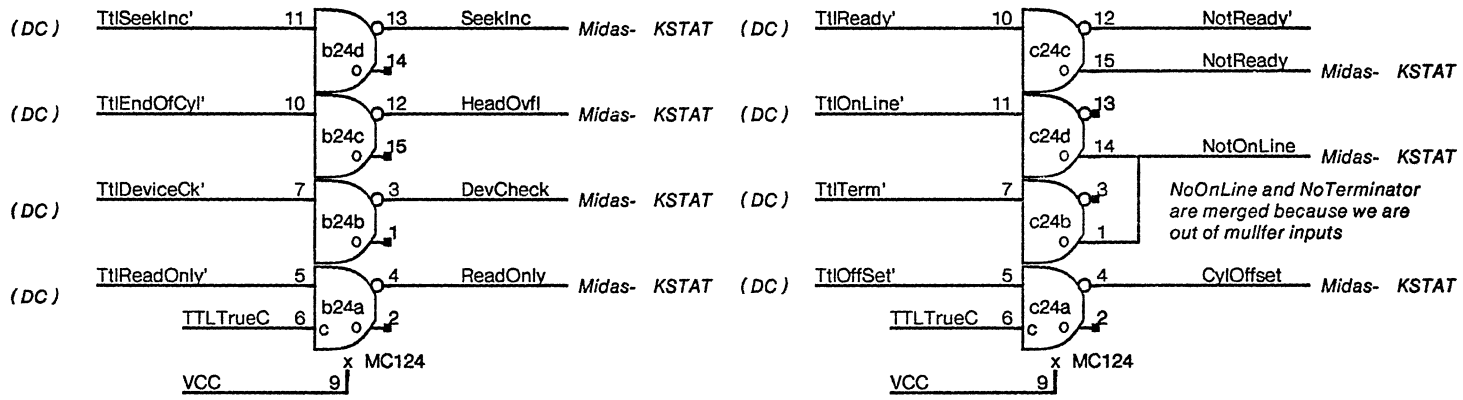


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Control RAM and Format Counter	TriconD03.sil	Roger Bates	Ce	9/24/79	09

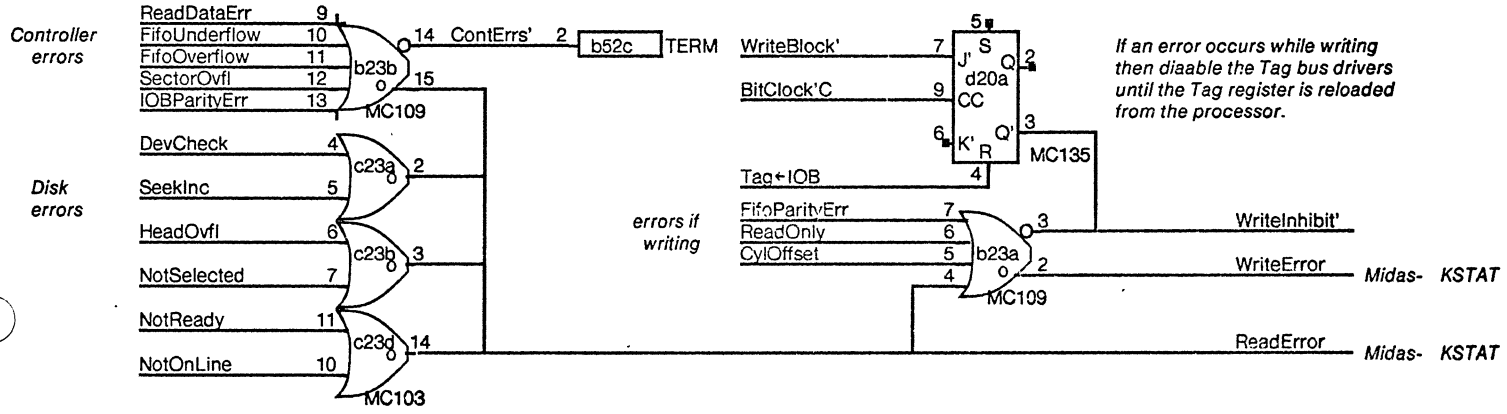


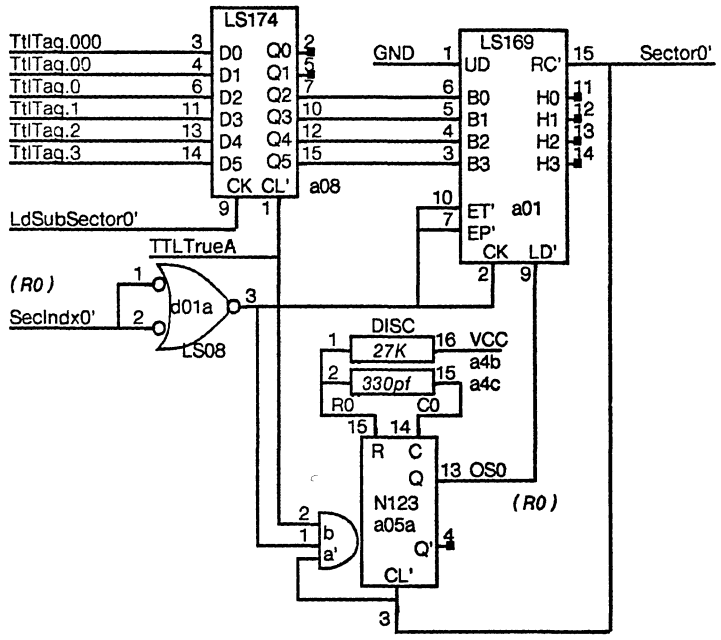
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	TAG register & Bus Drivers	TriconD04.sil	Roger Bates	Ce	7/23/79	10

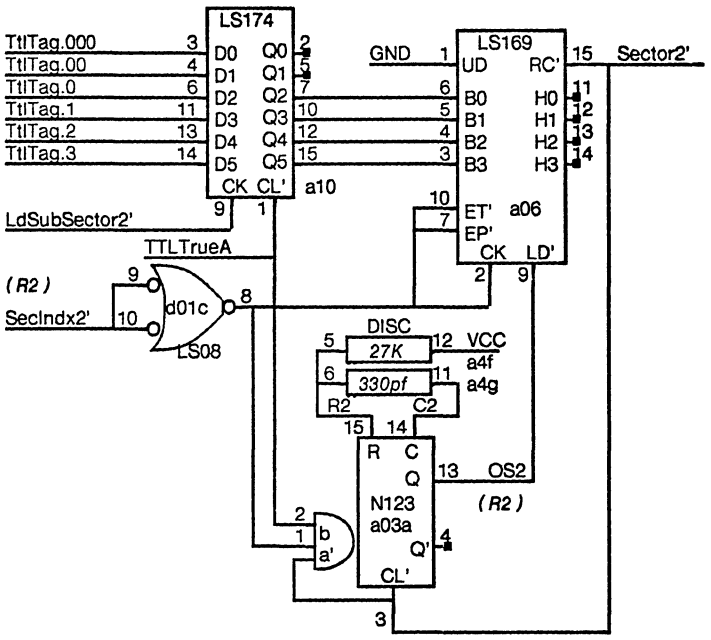

TtlTag.5
TtlTag.6
TtlTag.7
TtlTag.8
TtlTag.9
LS174
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
CK CL'
d04
TtlDriveTag'
TtlRunOK
S288
Q0
Q1
Q2
Q3
Q4
Q5
Q6
d05 Q7
CS'
A0
A1
A2
A3
A4
Select0
Select1
Select2
Select3
TtlSelect.0
TtlSelect.1
g01a
g01b
g01c
g01d
8T98
Select0' (R0)
Select1' (R1)
Select2' (R2)
Select3' (R3)
Low = select drive
c03c
c03d
MC124
Select.0 Midas- KSTATE
Select.1 Midas- KSTATE
TtlTag.4
LS155
DQ
d06
Q0' Q1' Q2' Q3'
DR' S2 S1
R0' R1' R2' R3'
EQ' ER'
LdSubSector0'
LdSubSector1'
LdSubSector2'
LdSubSector3'
Unit0←Data'
Unit1←Data'
Unit2←Data'
Unit3←Data'
Vbb5
b02c
MC125
WriteBlock'
TtlSelect.0
TtlSelect.1
TtlDriveTag'
TtlRunOK'
DisableRun
d17c
g01f
TtlRunOK
TtlRunOK'
En4' En2' g01g
The characteristics of the MC125 indicate that TtlRunOK' should be high whenever +5V is ON and -5V is OFF.

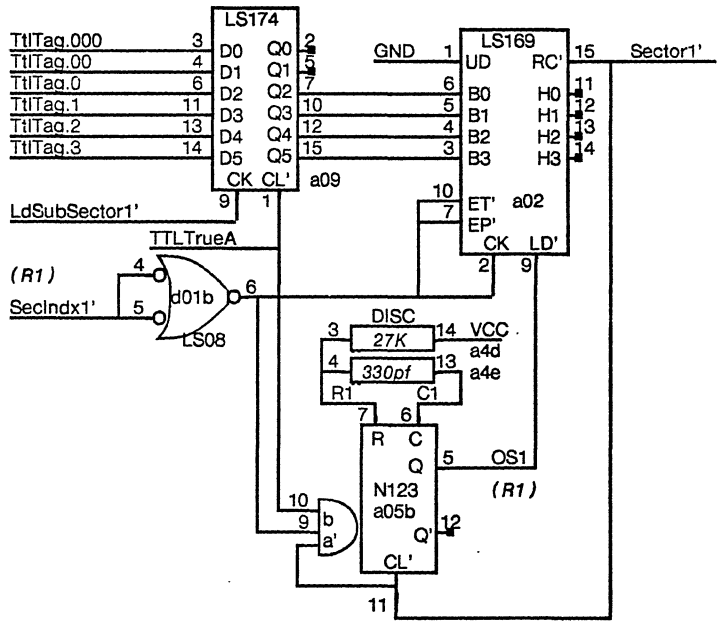

(DC)
TtlSeekInc'
b24d
SeekInc Midas- KSTAT
TtlEndOfCyl'
b24c
HeadOvfl Midas- KSTAT
TtlDeviceCk'
b24b
DevCheck Midas- KSTAT
TtlReadOnly'
b24a
ReadOnly Midas- KSTAT
TTLTrueC
VCC
x MC124
TtlReady'
c24c
NotReady' NotReady Midas- KSTAT
TtlOnLine'
c24d
NotOnLine Midas- KSTAT
TtlTerm'
c24b
NoOnLine and NoTerminator are merged because we are out of mullfer inputs
TtlOffSet'
c24a
CylOffset Midas- KSTAT

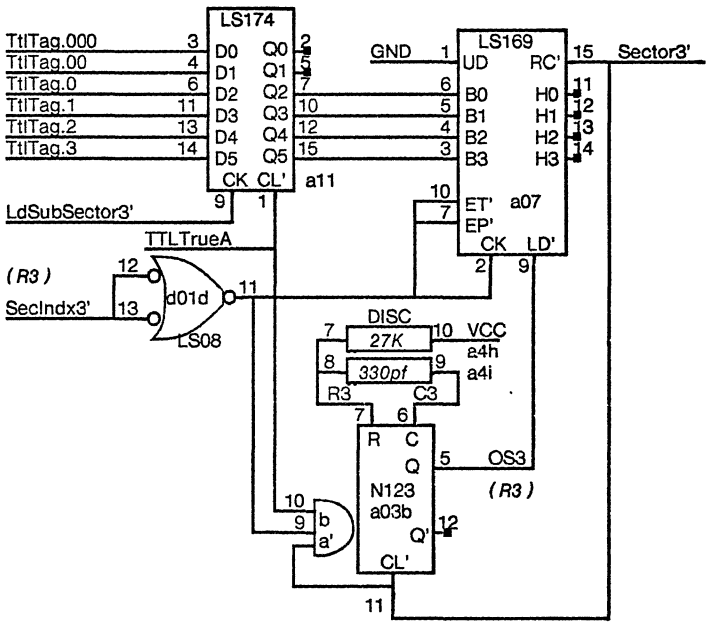
Midas- KSTAT

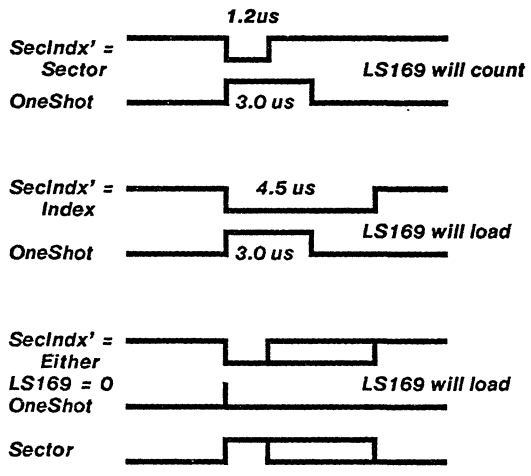

Controller errors
ReadDataErr
FifoUnderflow
FifoOverflow
SectorOvfl
IOBParityErr
b23b
MC109
ContErrs'
b52c
TERM
Disk errors
DevCheck
SeekInc
HeadOvfl
NotSelected
NotReady
NotOnLine
c23a
c23b
c23d
MC103
errors if writing
WriteBlock'
BitClock'C
Tag←IOB
d20a
MC135
FifoParityErr
ReadOnly
CylOffset
b23a
MC109
WriteInhibit'
WriteError Midas- KSTAT
ReadError Midas- KSTAT
If an error occurs while writing then diaable the Tag bus drivers until the Tag register is reloaded from the processor.

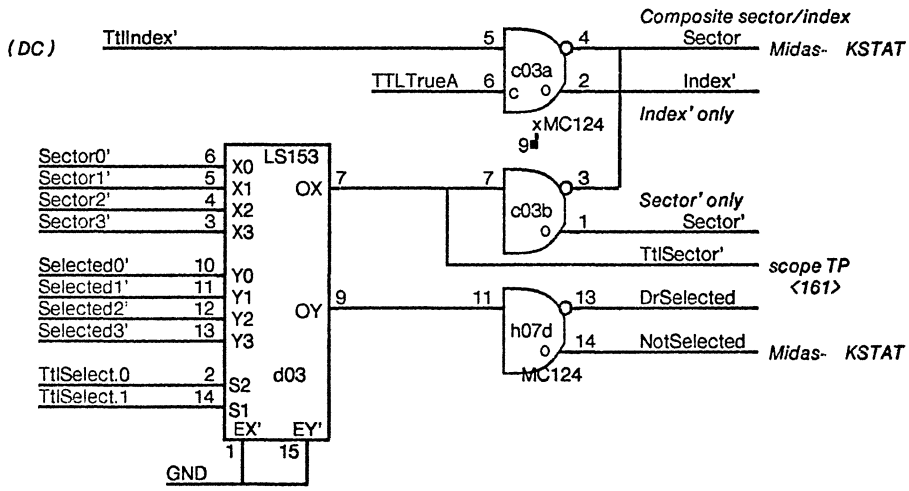








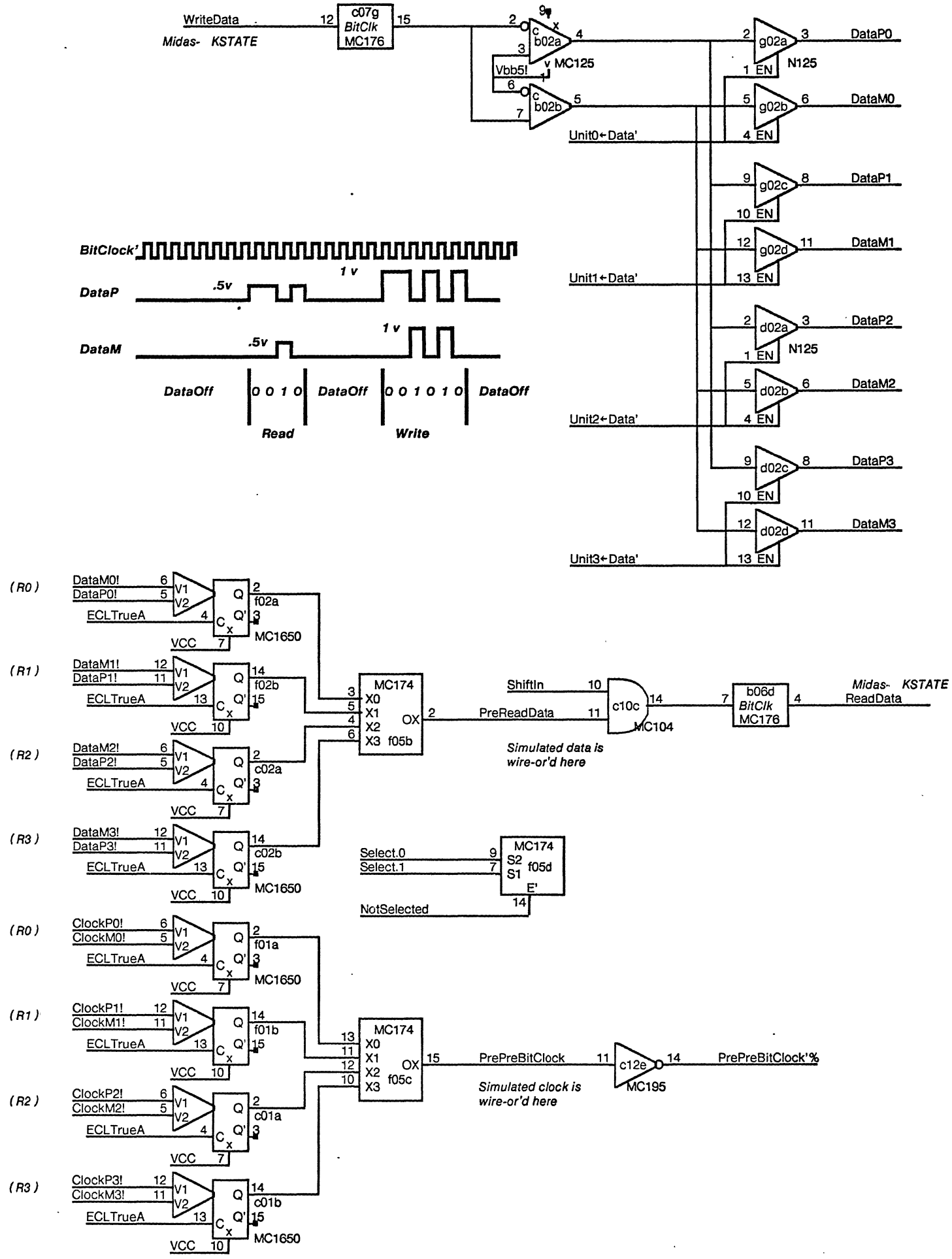




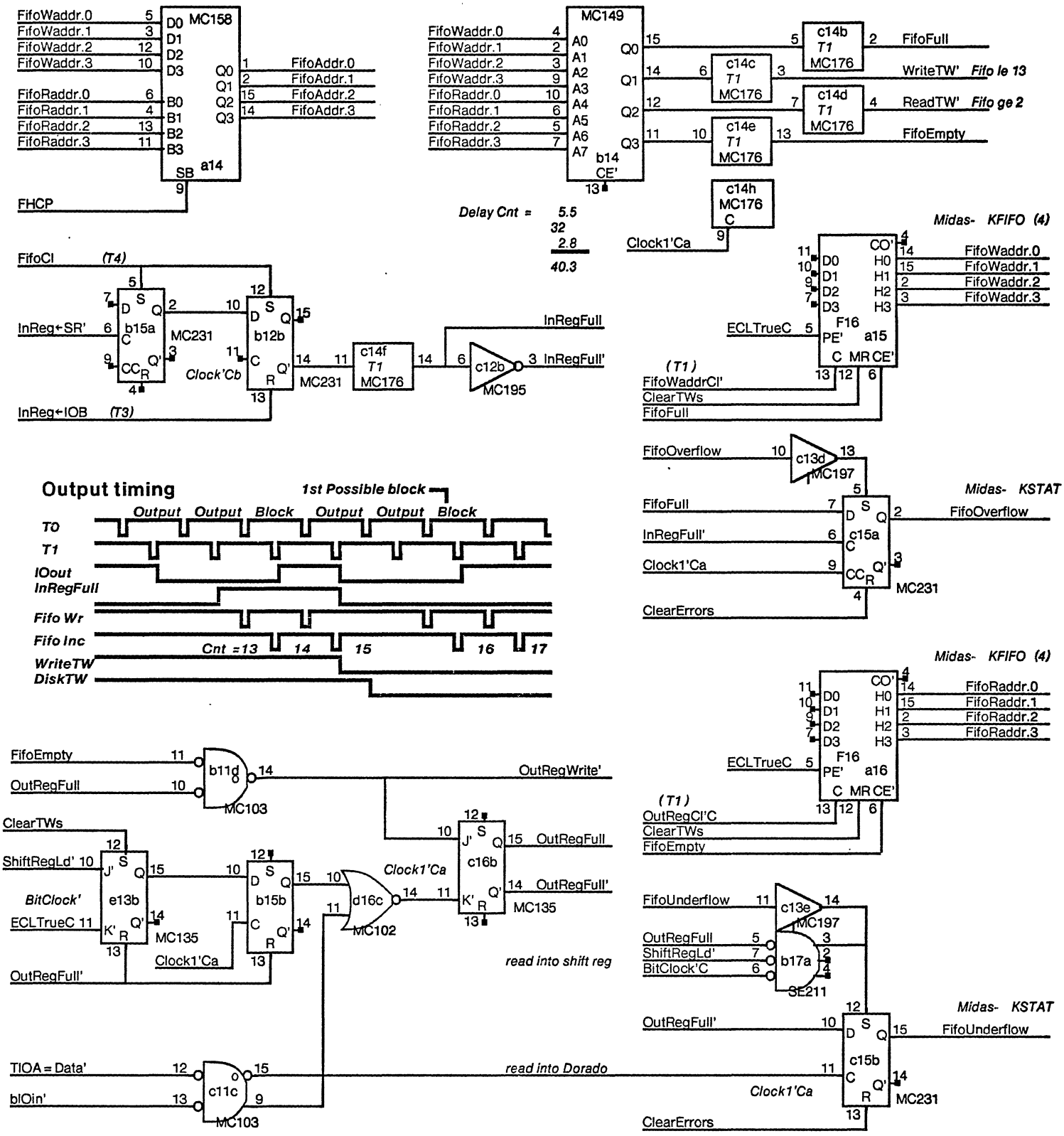
The above sector counters require the TRIDENT disk to have its sector counters set to provide 117 "sub-sector" pulses per revolution. This is done by setting the disk jumpers as follows:

	X6A	X6B
	4 - 11	2 - 13
	5 - 10	3 - 12
		4 - 11
		5 - 10
		6 - 09

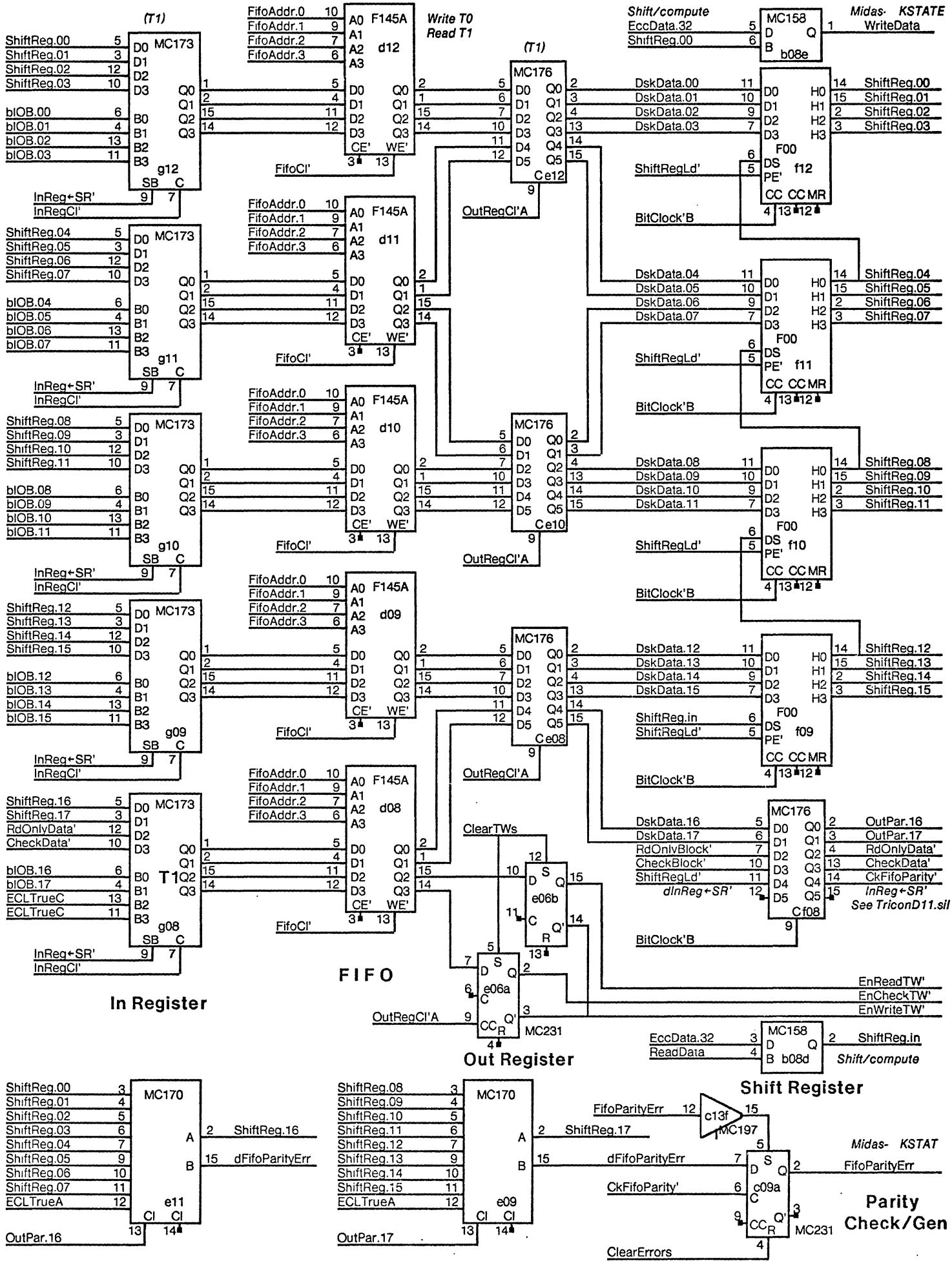
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Sector Length Counters	TriconD06.sil	Roger Bates	Ce	7/24/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clock and Data Input	TriconD07.sil	Roger Bates	Ce	7/23/79	13

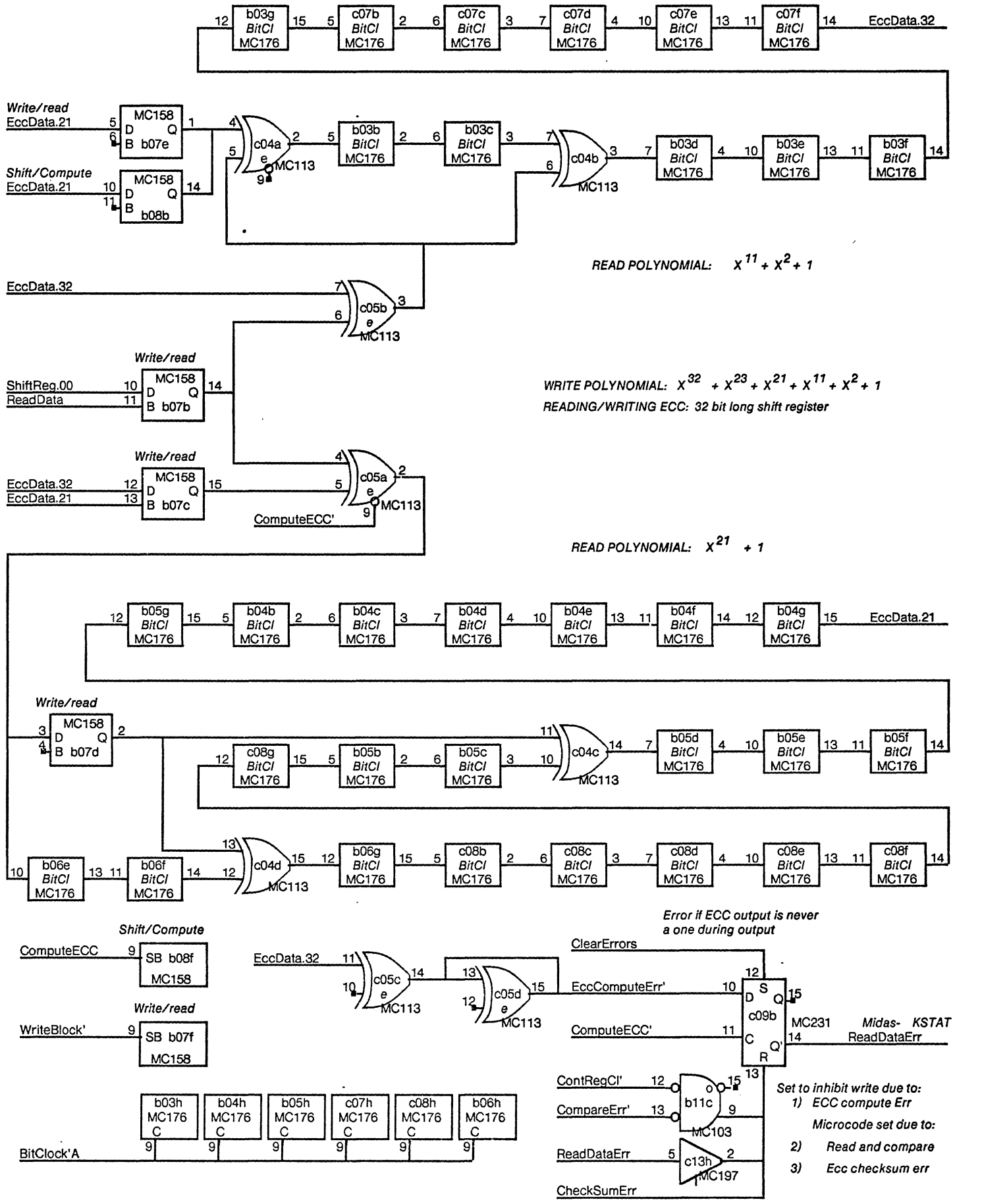


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	FIFO Control	TriconD08.sil	Roger Bates	Ce	9/24/79	14

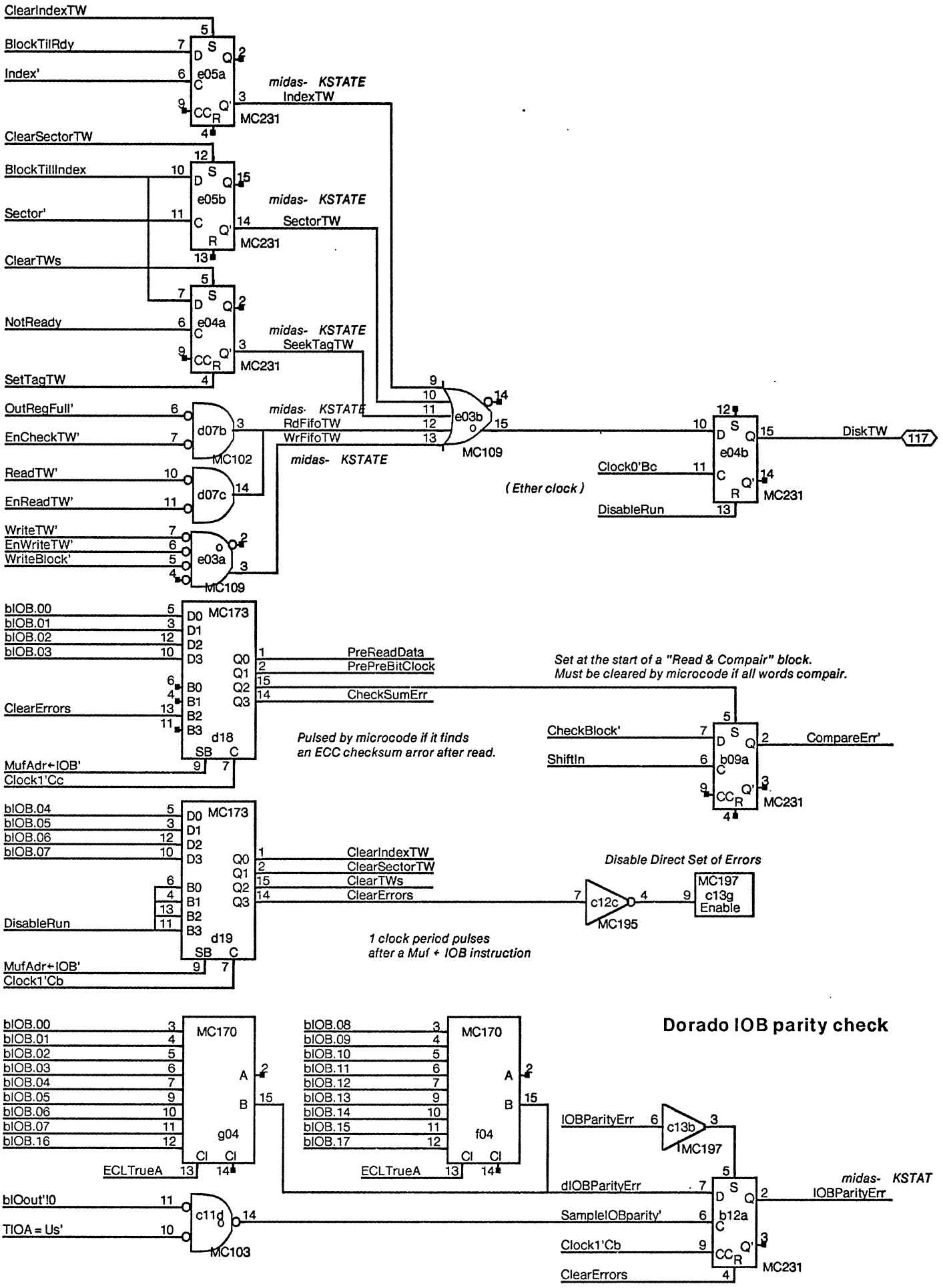


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	FIFO and Shift Register	TriconD09.sil	Roger Bates	Ce	7/08/79	15

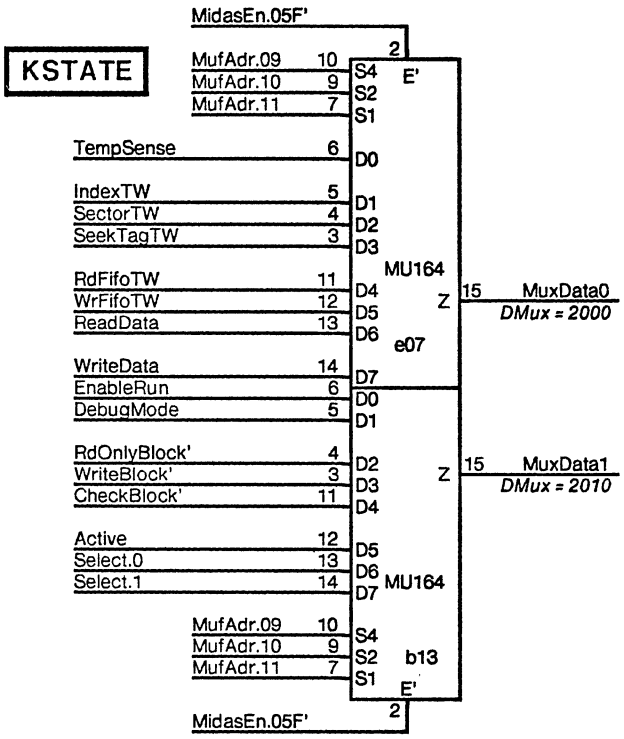
POLYNOMIAL DIVIDER FOR FIRE CODE GENERATION

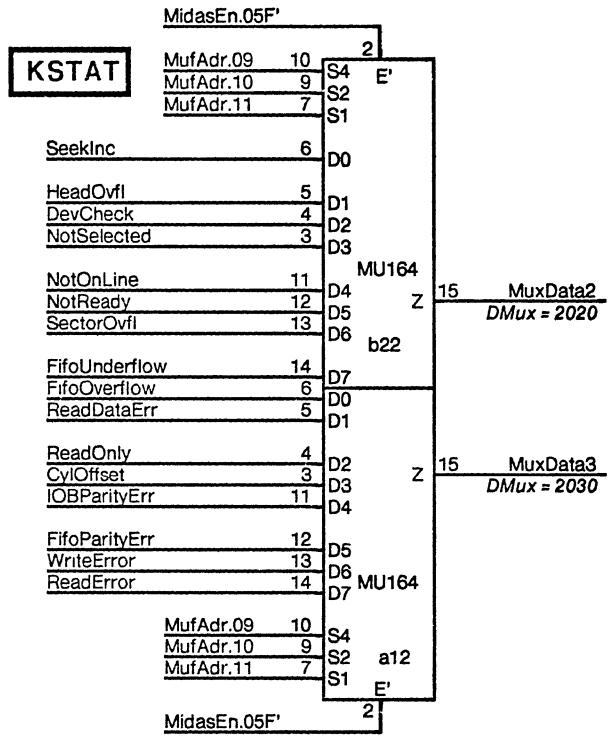


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Fire Code Generator	TriconD10.sil	Roger Bates	Ce	7/08/79	16



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Buss Parity Task Wake-Up	TriconD11.sil	Roger Bates	Ce	7/08/79	17

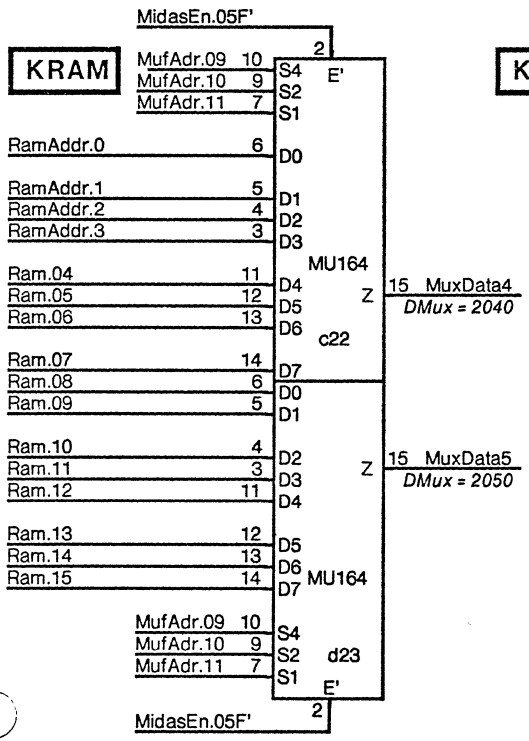


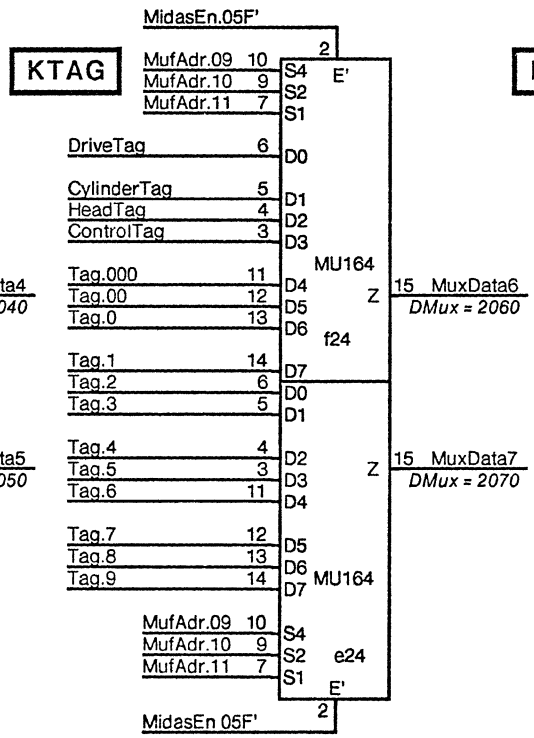


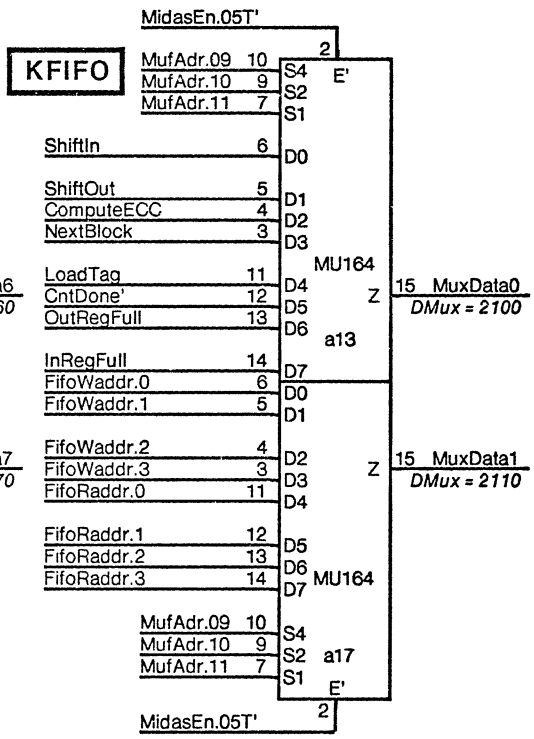
Muffler addresses are:

Value listed for Program input
Value plus 2000 for Midas input

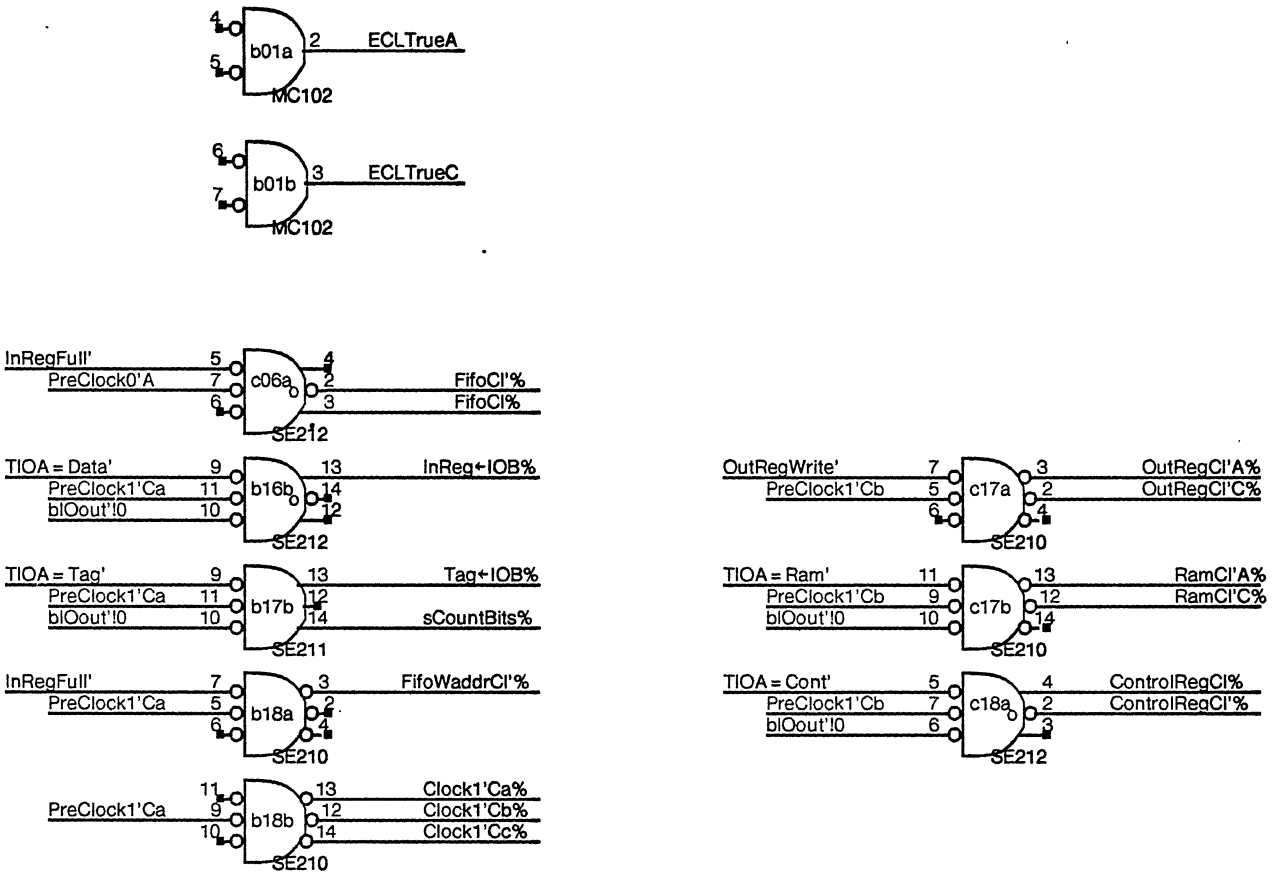
Values from 120 to 177 are used by the Ethernet





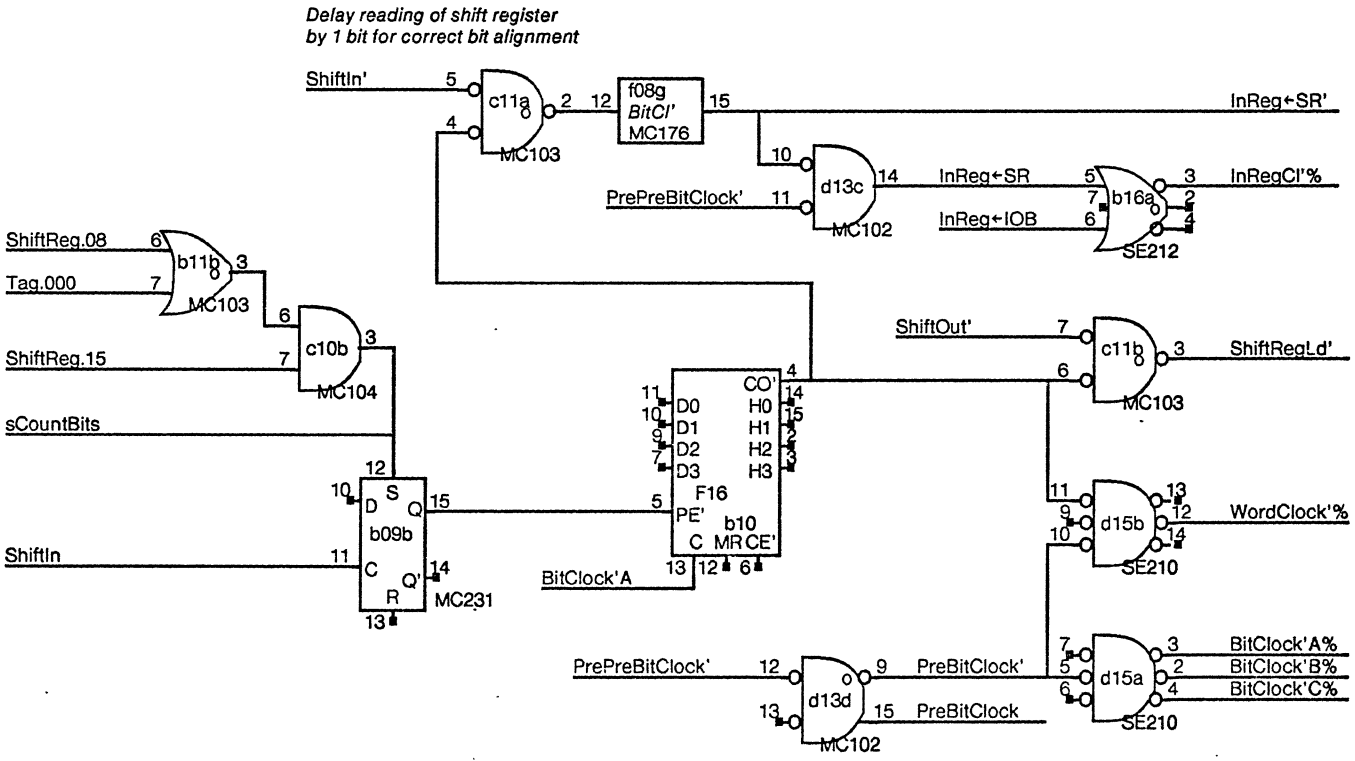


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMUX CONTROL	TriconD12.sil	Roger Bates	Ce	7/08/79	18

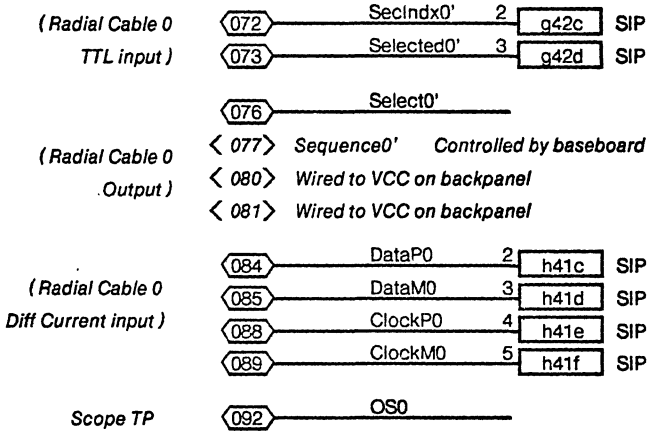


System Clocks

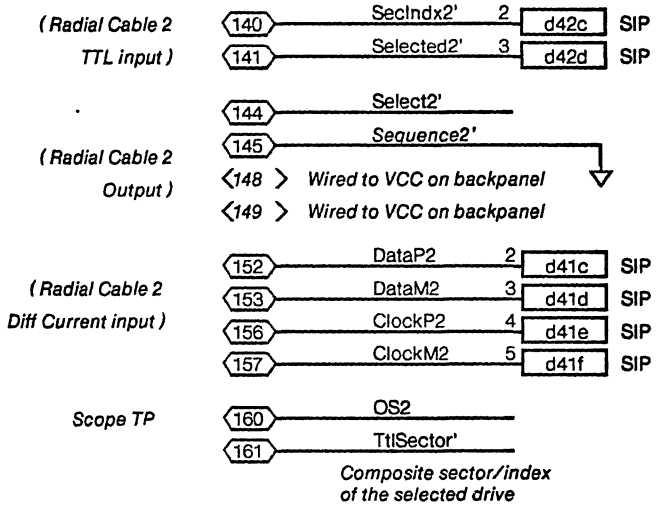
Disk Clocks



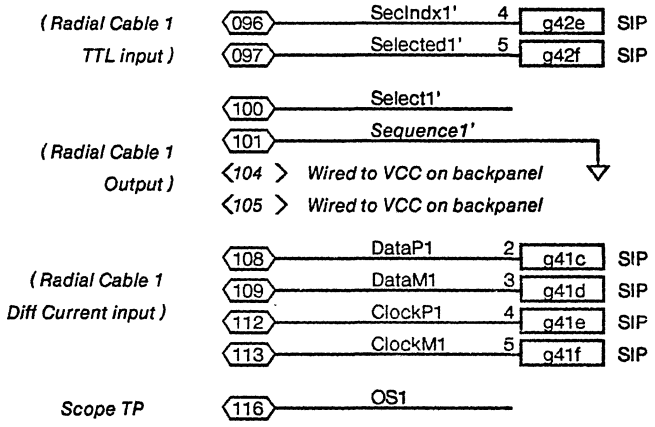
Radial Cable for Drive 0



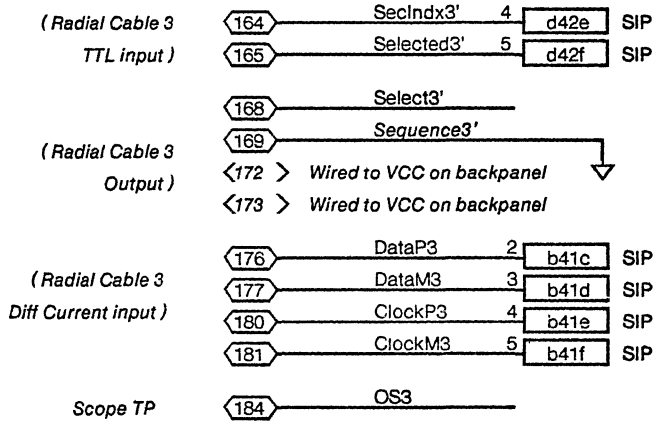
Radial Cable for Drive 2



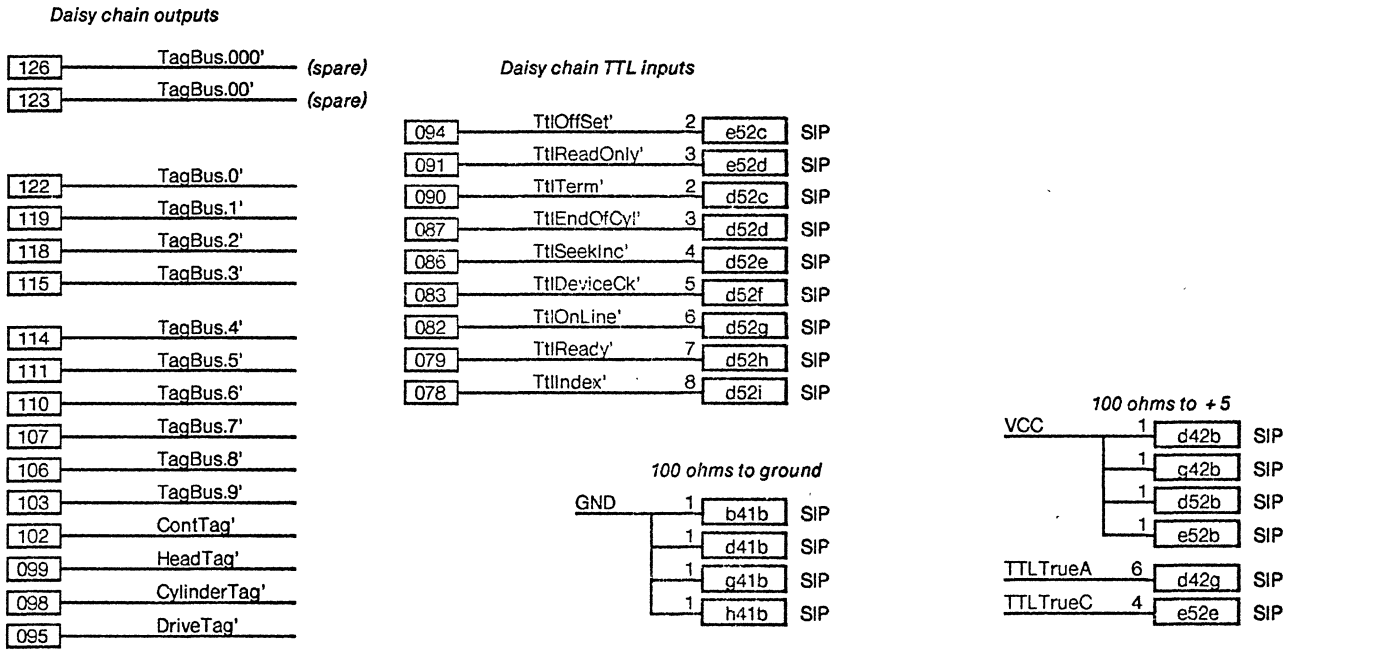
Radial Cable for Drive 1



Radial Cable for Drive 3

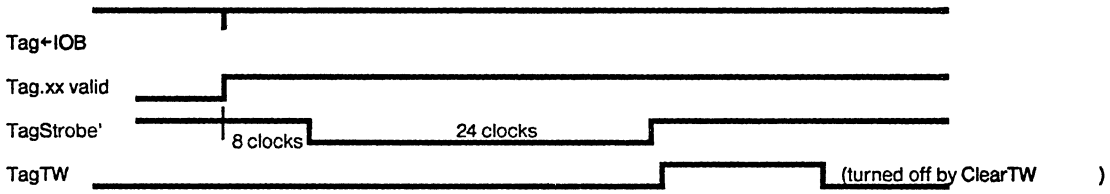


Daisy Chain Cable

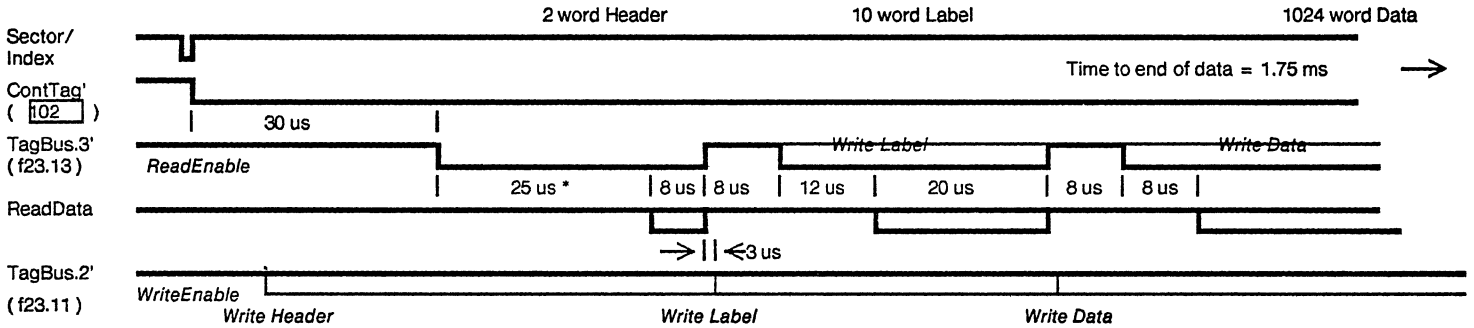


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	I/O Signals & Terminators	TriconD14.sil	Roger Bates	Ce	7/08/79	20

Head or Cylinder Tag Instruction



Read or Write Instruction

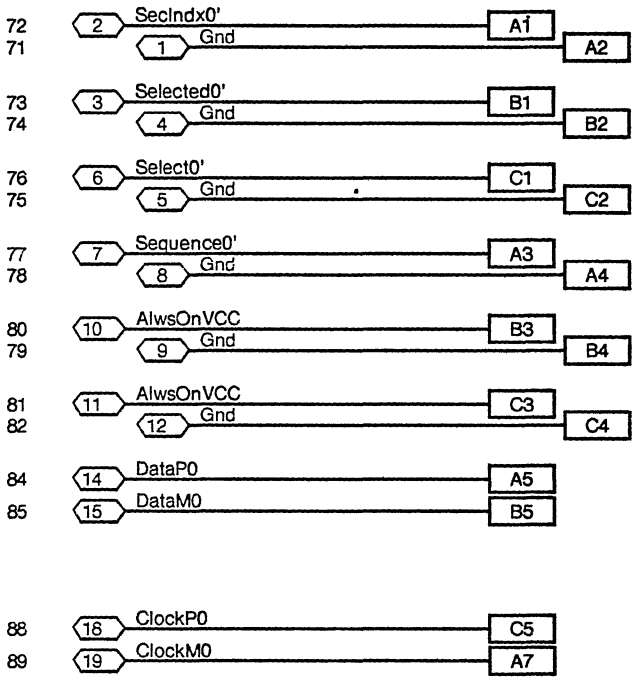


* This value if for reading a pack on the same drive that Headers were written
It may vary by + /- 15 us on other drives

Radial Cable for Drive 0

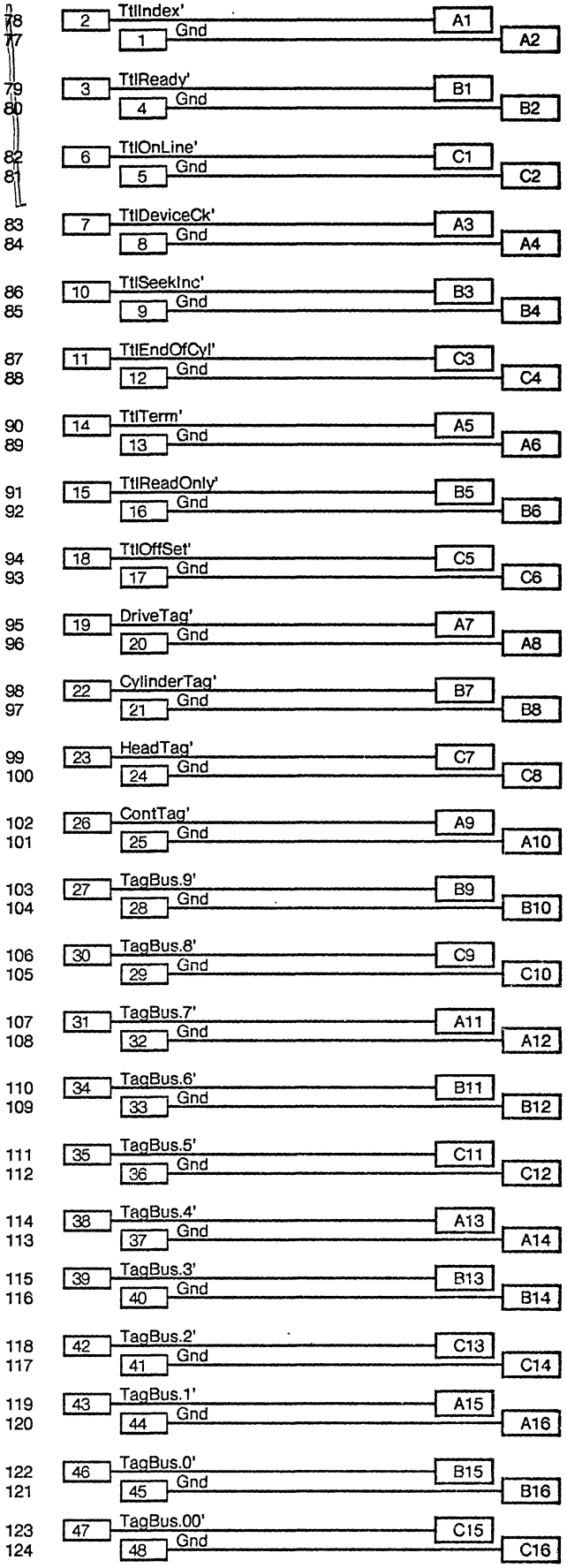
RADIAL CONECTOR

AMP 204729-1



DAISEY CHAIN CABLE

AMP 204733-1



Radial Cable for Drive 0

AMP 204742-1

Cal-Comp
Assembly 12433

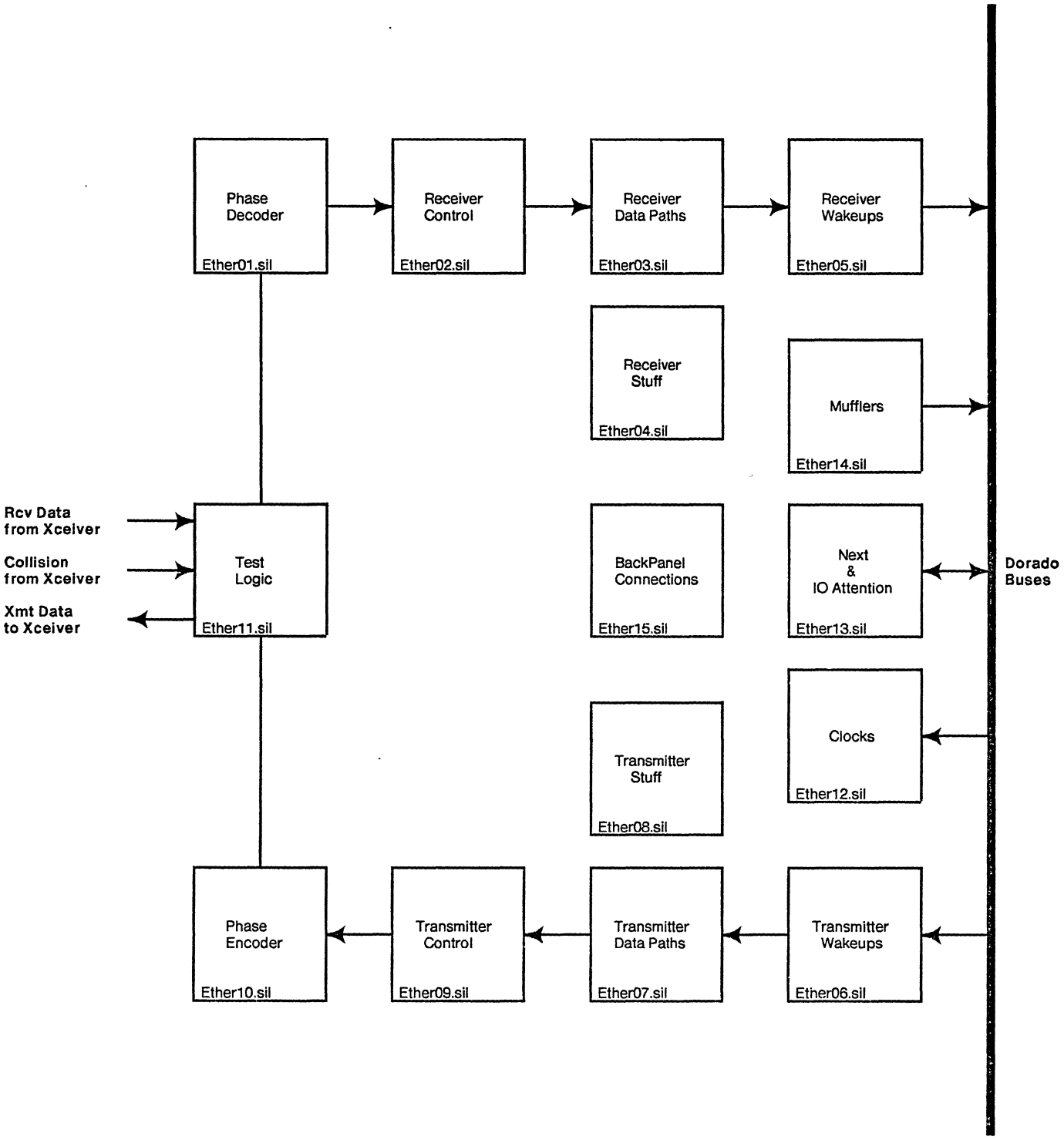
A1	SecIndx0'	violet	E04	
A2	Gnd	black		E03
B1	Selected0'	brown	E08	
B2	Gnd	black		E07
C1	Select0'	green	E12	
C2	Gnd	black		E11
A3	Sequence0'	blue	E10	
A4	Gnd	black		E09
B3	AlwsOnVCC	white	E02	
B4	Gnd	black		E05
C3	AlwsOnVCC	red	E01	
C4	Gnd	black		E05
A5	DataP0	Orenge	E14	
B5	DataM0	black	E16	
C5	ClockP0	Yellow	E18	
A7	ClockM0	Black	E20	

DAISEY CHAIN CABLE

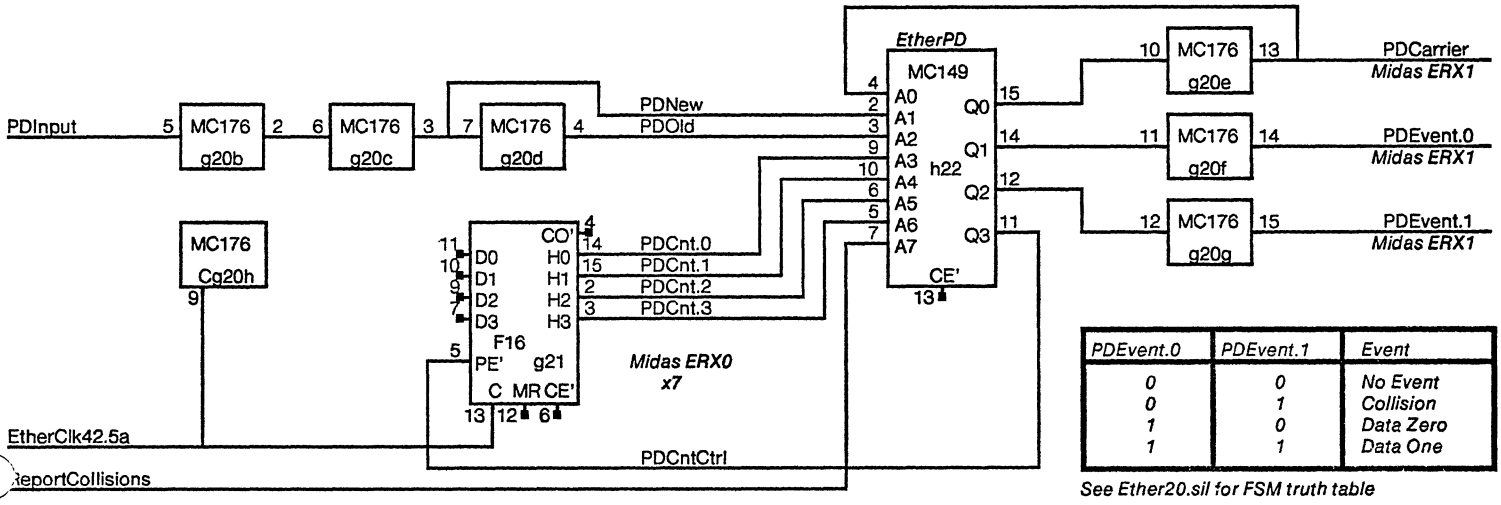
AMP 204746-1

Cal-Comp
Assembly 12424

A1	TtlIndex'	E06	
A2	Gnd		E06G
B1	TtlReady'	E08	
B2	Gnd		E08G
C1	TtlOnLine'	E14	
C2	Gnd		E14G
A3	TtlDeviceCk'	E12	
A4	Gnd		E12G
B3	TtlSeekInc'	E16	
B4	Gnd		E16G
C3	TtlEndOfCyl'	E02	
C4	Gnd		E02G
A5	TtlTerm'	E35	
A6	Gnd		E35G
B5	TtlReadOnly'	E10	
B6	Gnd		E10G
C5	TtlOffSet'	E04	
C6	Gnd		E04G
A7	Not used		
A8	Gnd		
B7	CylinderTag'	E39	
B8	Gnd		E39G
C7	HeadTag'	E40	
C8	Gnd		E40G
A9	ContTag'	E37	
A10	Gnd		E37G
B9	TagBus.9'	E38	
B10	Gnd		E38G
C9	TagBus.8'	E36	
C10	Gnd		E36G
A11	TagBus.7'	E34	
A12	Gnd		E34G
B11	TagBus.6'	E32	
B12	Gnd		E32G
C11	TagBus.5'	E30	
C12	Gnd		E30G
A13	TagBus.4'	E28	
A14	Gnd		E28G
B13	TagBus.3'	E26	
B14	Gnd		E26G
C13	TagBus.2'	E24	
C14	Gnd		E24G
A15	TagBus.1'	E22	
A16	Gnd		E22G
B15	TagBus.0'	E20	
B16	Gnd		E20G
C15	Not used		
C16	Gnd		

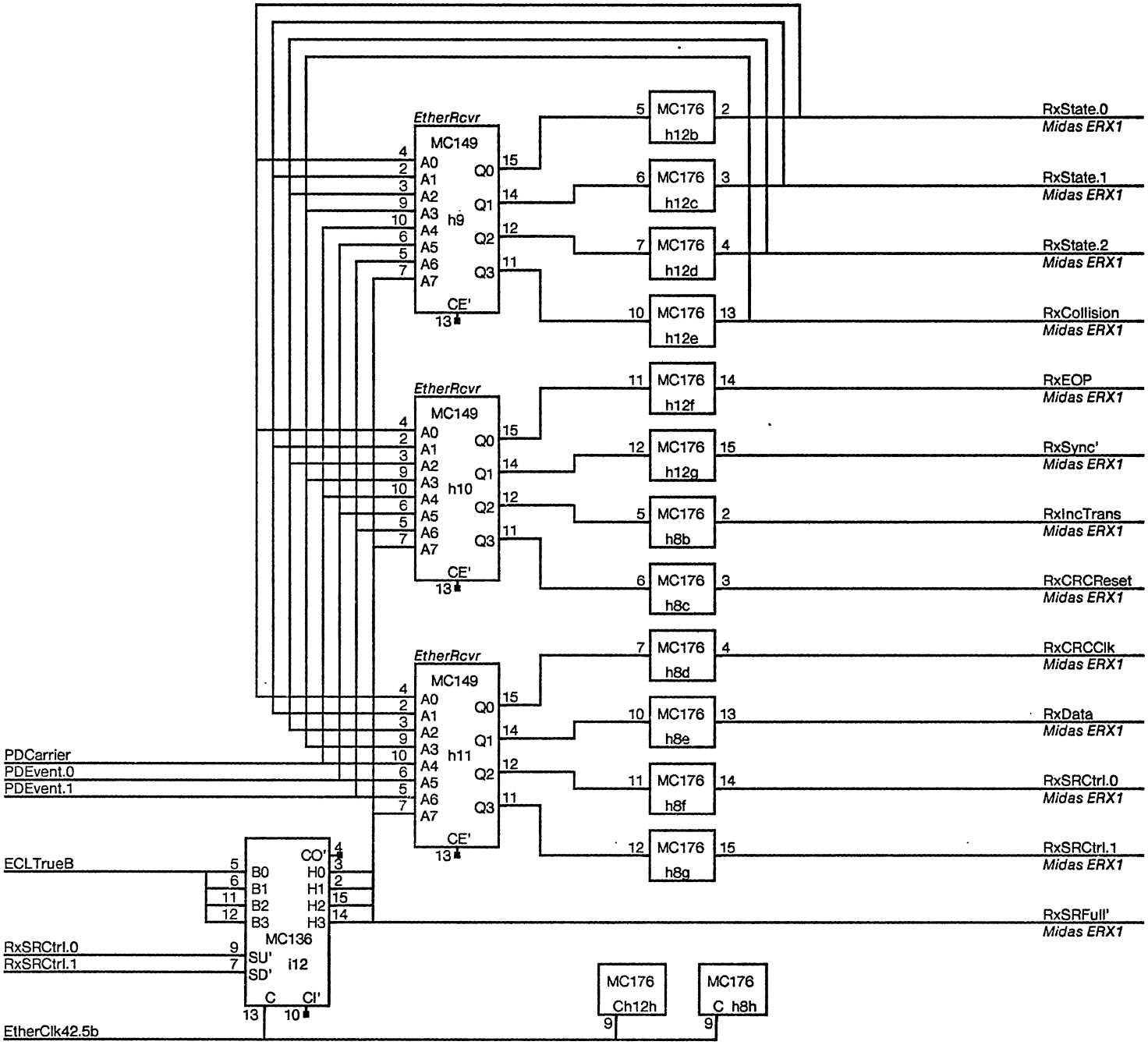


See DskEth*.sil for IOA, IOB, Muffler Control and Board Clocks



PDEvent.0	PDEvent.1	Event
0	0	No Event
0	1	Collision
1	0	Data Zero
1	1	Data One

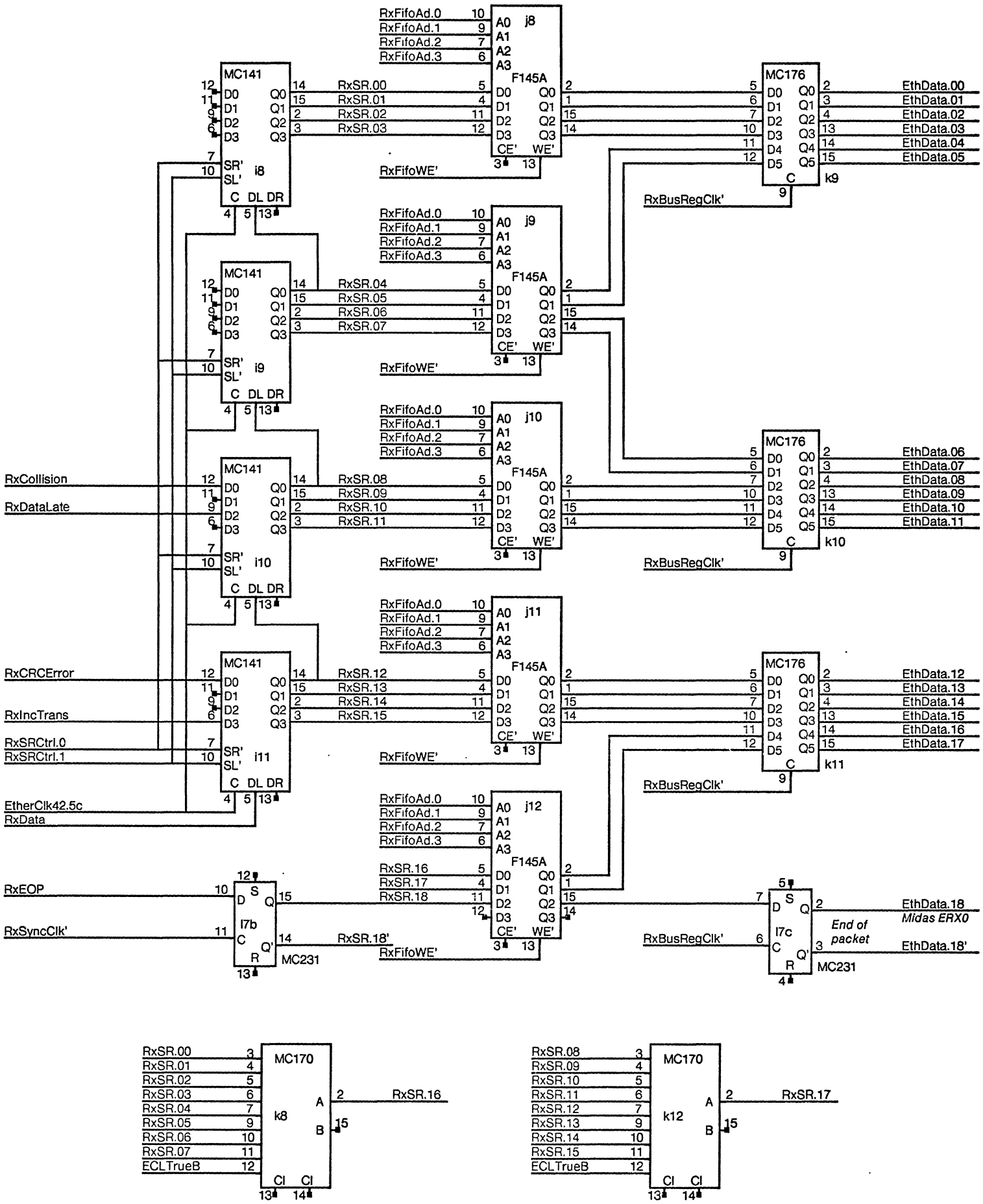
See Ether20.sil for FSM truth table



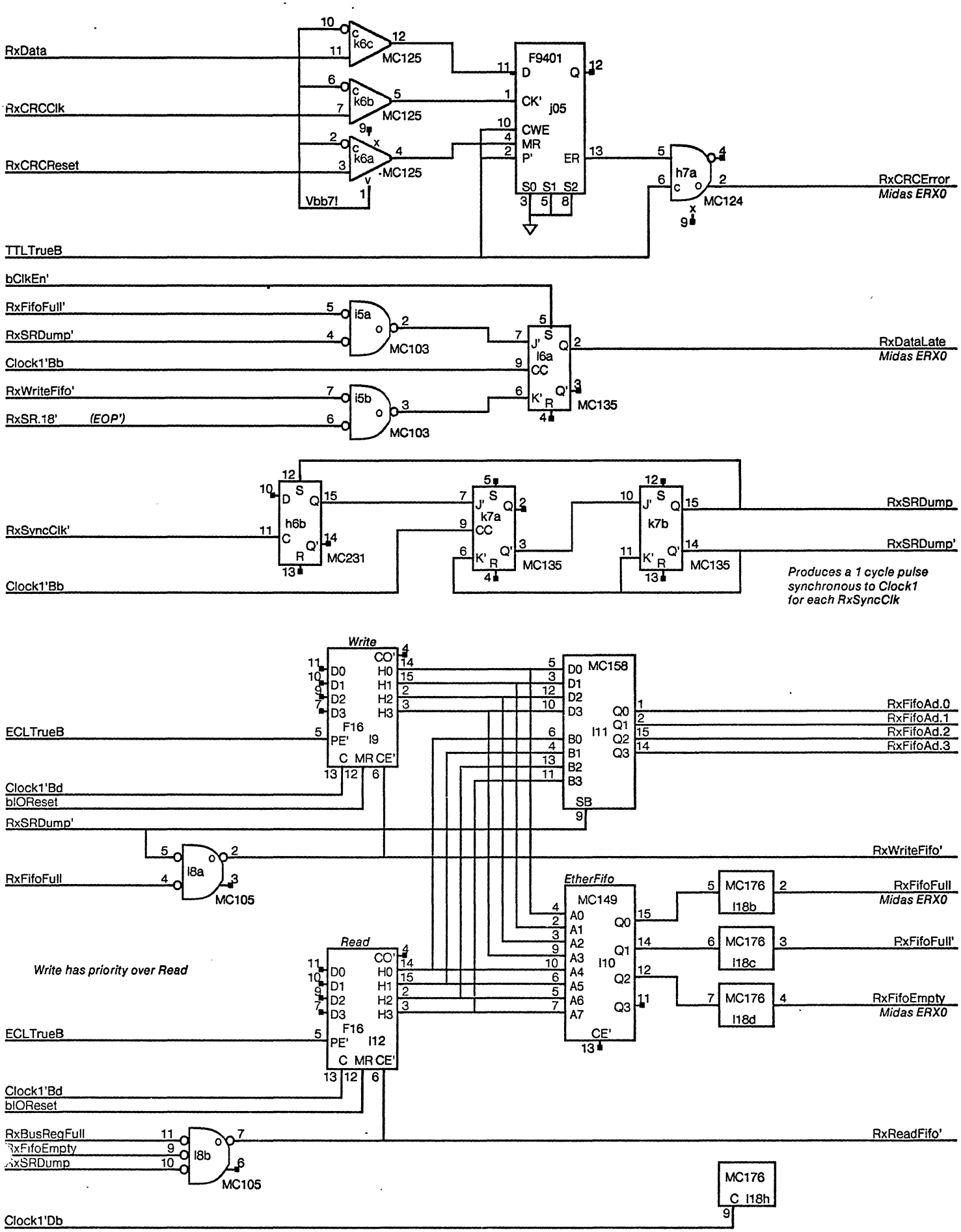
See Ether18.sil for timing diagrams

The slowest Dorado clock speed at which the receiver works is 85 ns (T0 to T1)

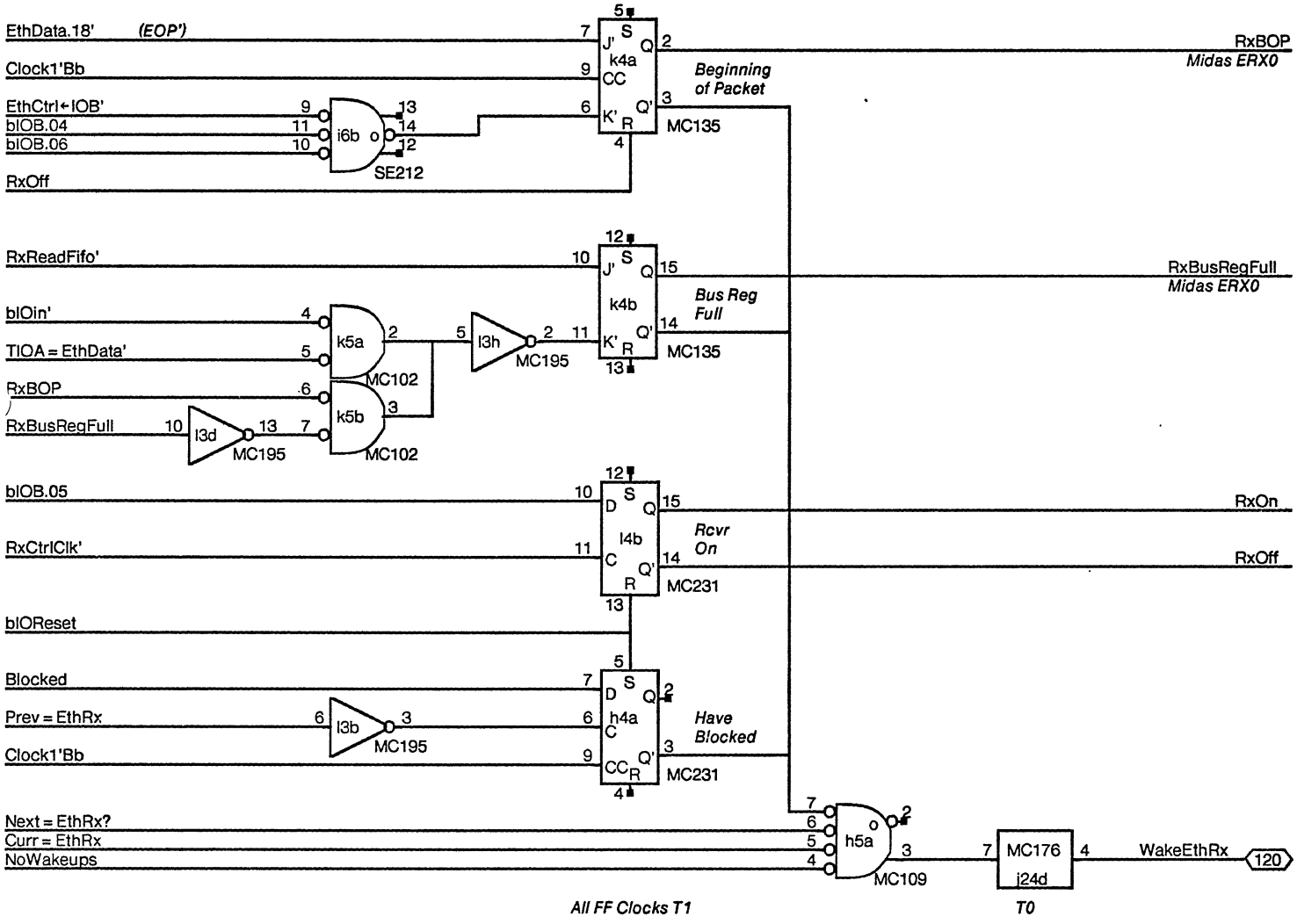
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Control	Ether02.sil	David Boggs	Ce	9/24/79	25



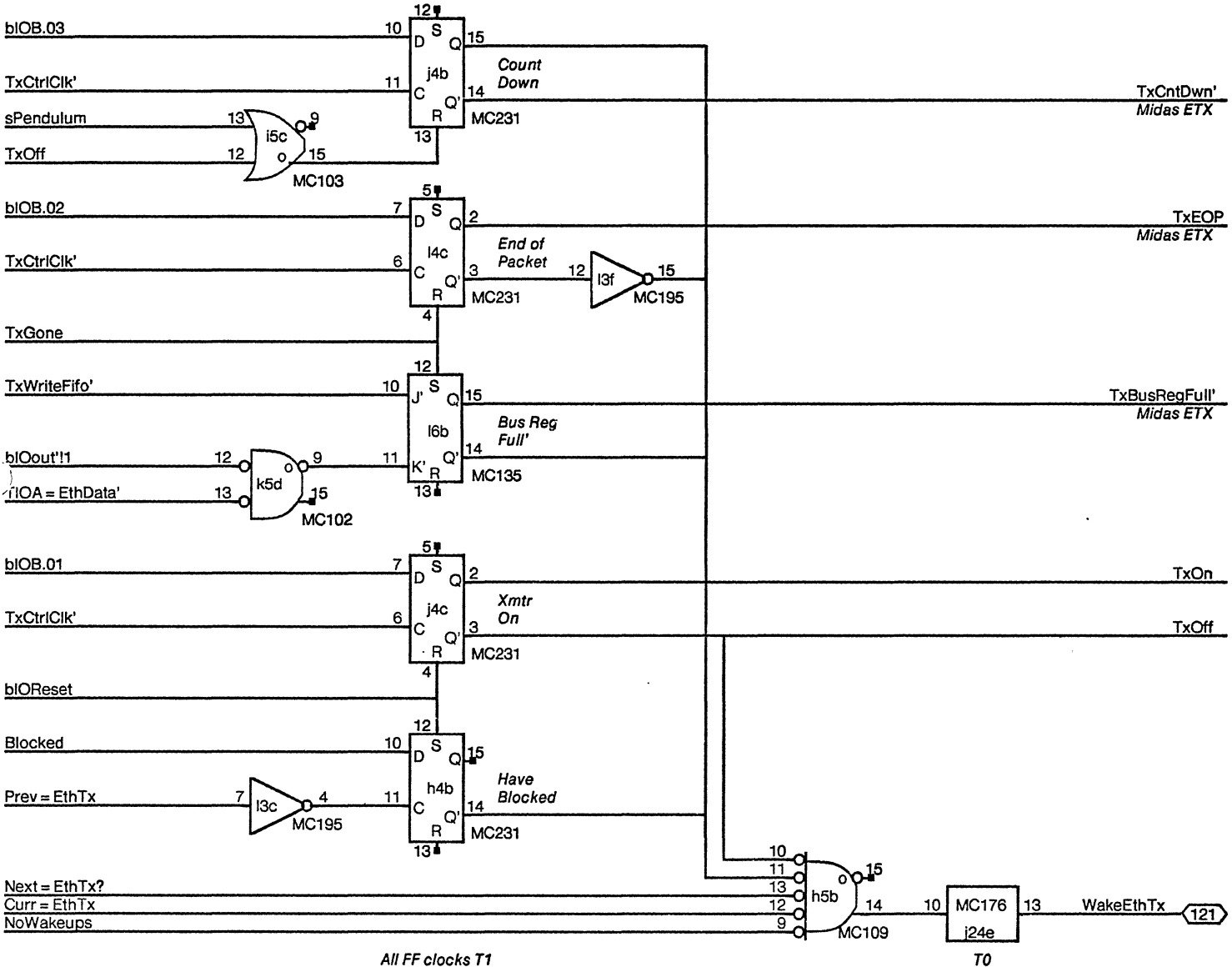
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Data Paths	Ether03.sil	David Boggs	Ce	7/08/79	26



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Stuff	Ether04.sil	David Boggs	Ce	7/08/79	27

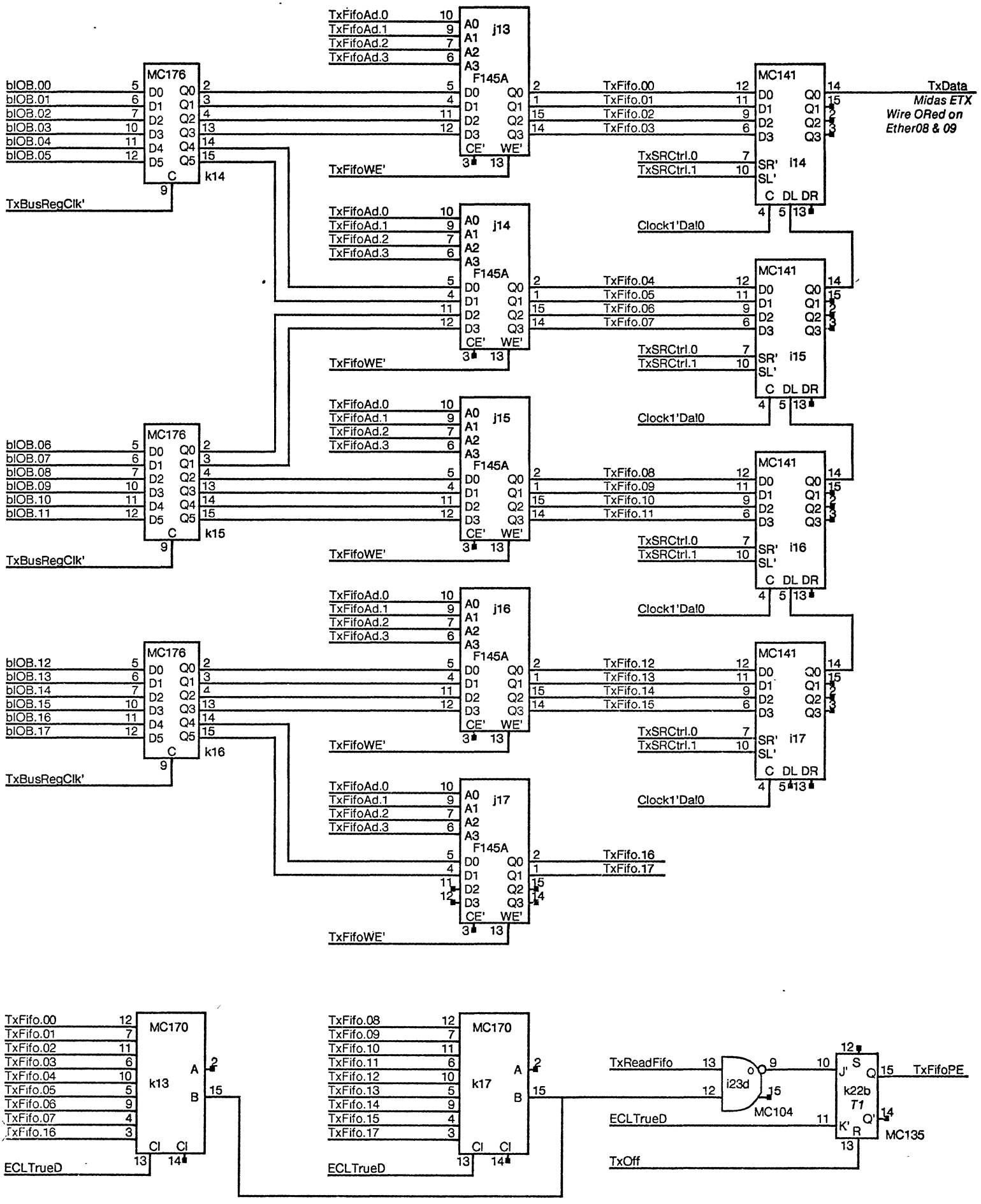


See Ether21 & 22.sil for wakeup timing diagrams

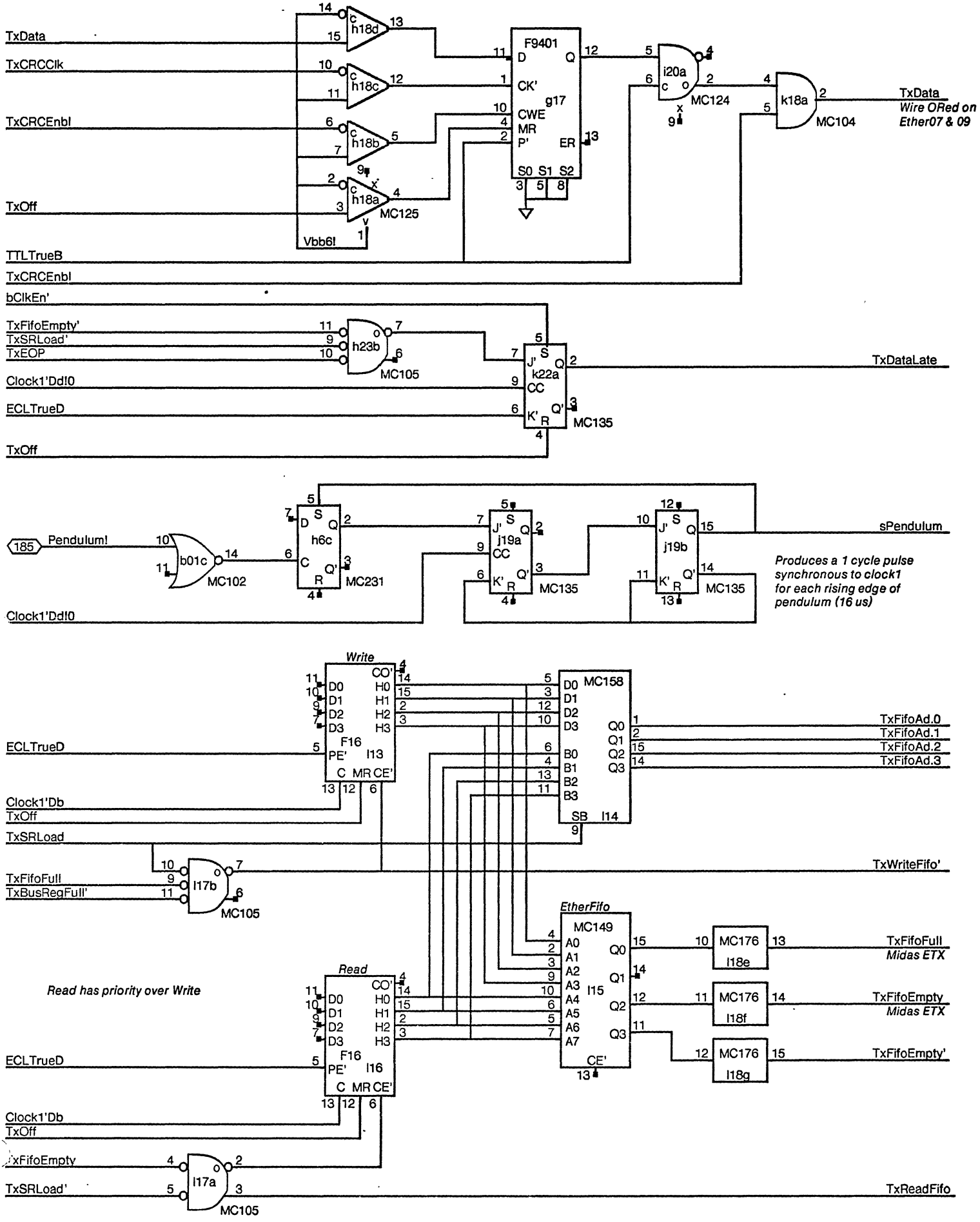


See Ether21 & 22.sil for wakeup timing diagrams

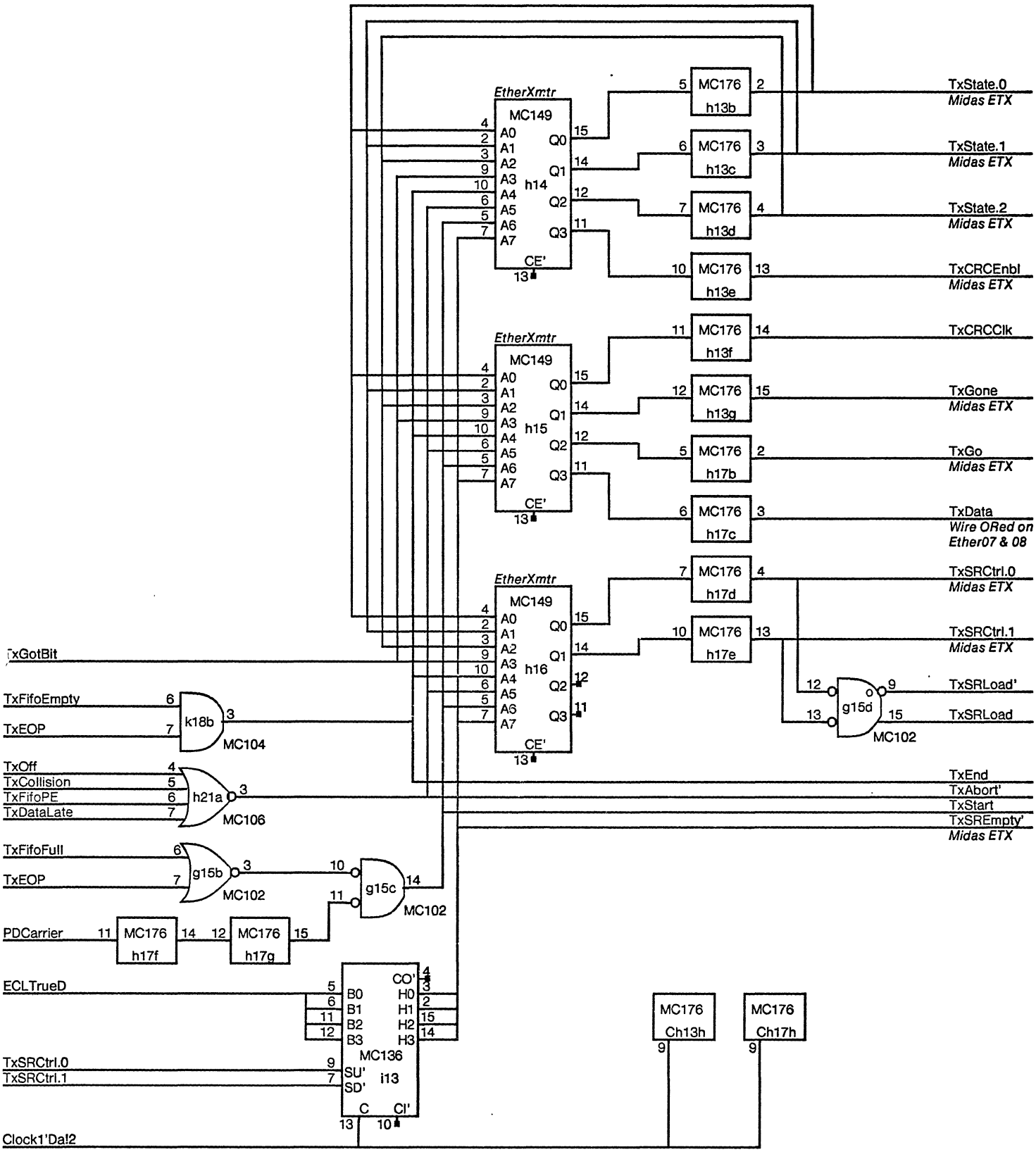
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Wakeups	Ether06.sil	David Boggs	Ce	7/08/79	29



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Data Paths	Ether07.sil	David Boggs	Ce	7/08/79	30

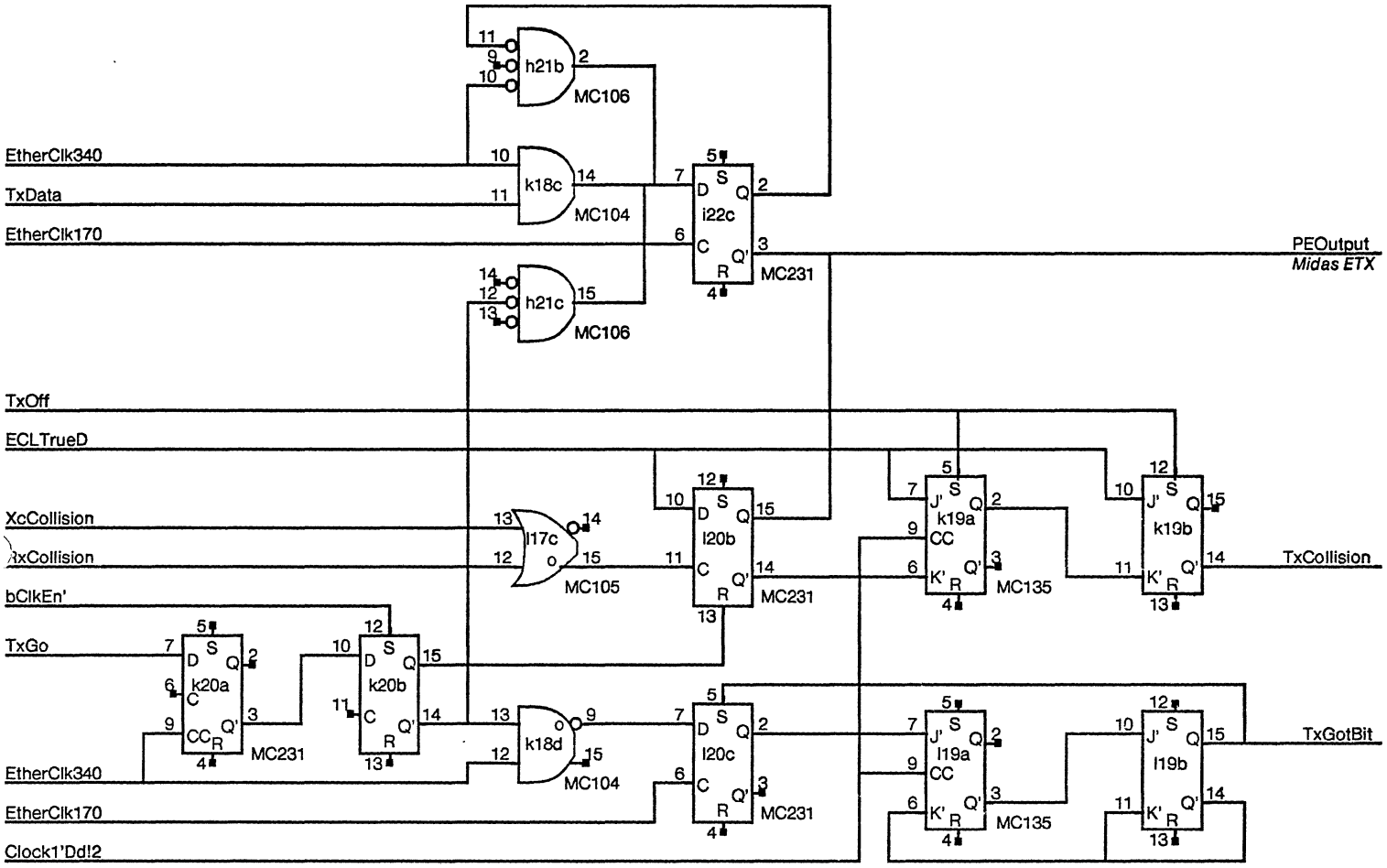


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Stuff	Ether08.sil	David Boggs	Ce	7/08/79	31



See Ether17.sil for timing diagrams

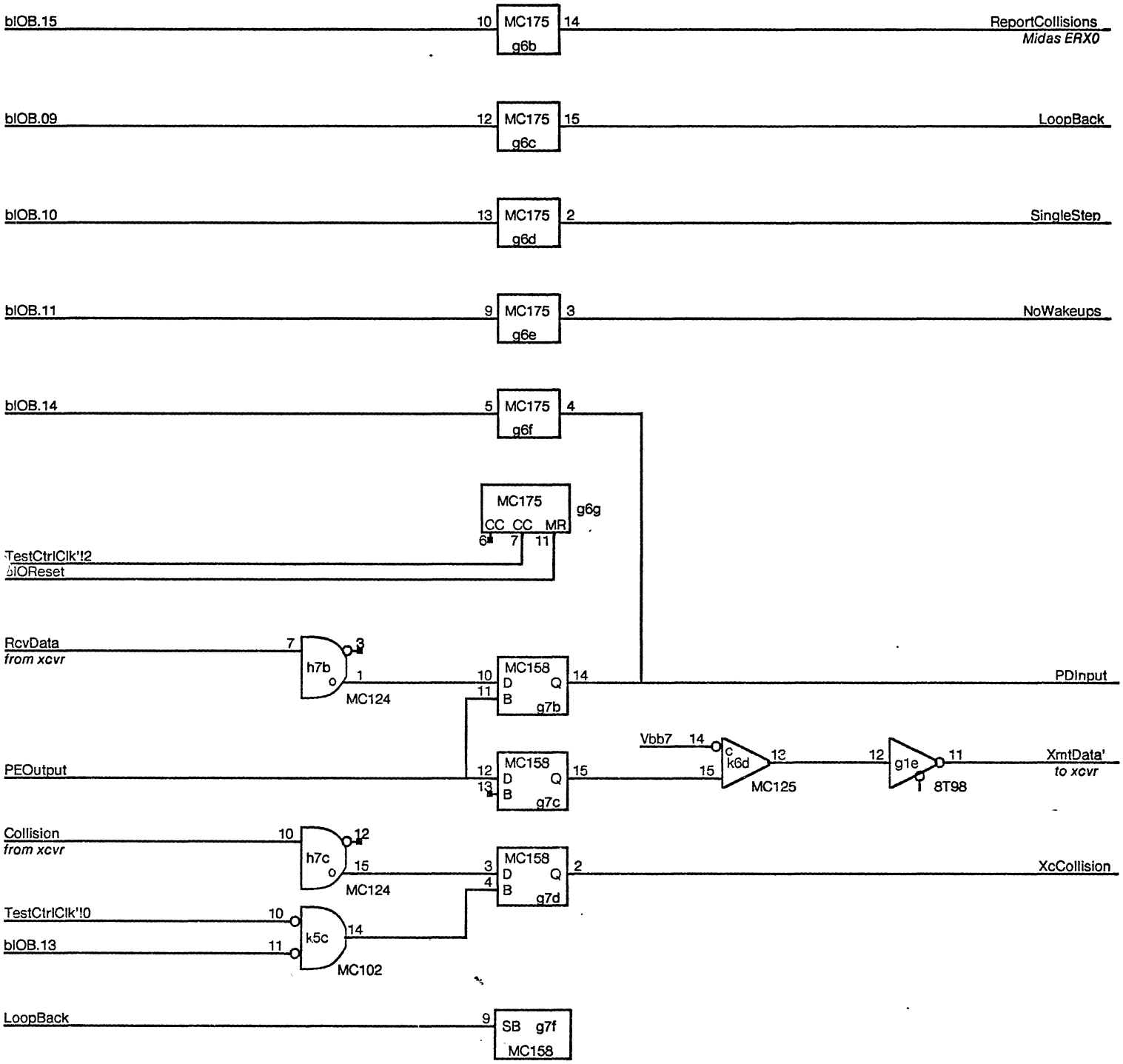
XEROX PARC	Project: Dorado	Drawing: Transmitter Control	File: Ether09.sil	Designer: David Boggs	Rev: Ce	Date: 9/24/79	Page: 32



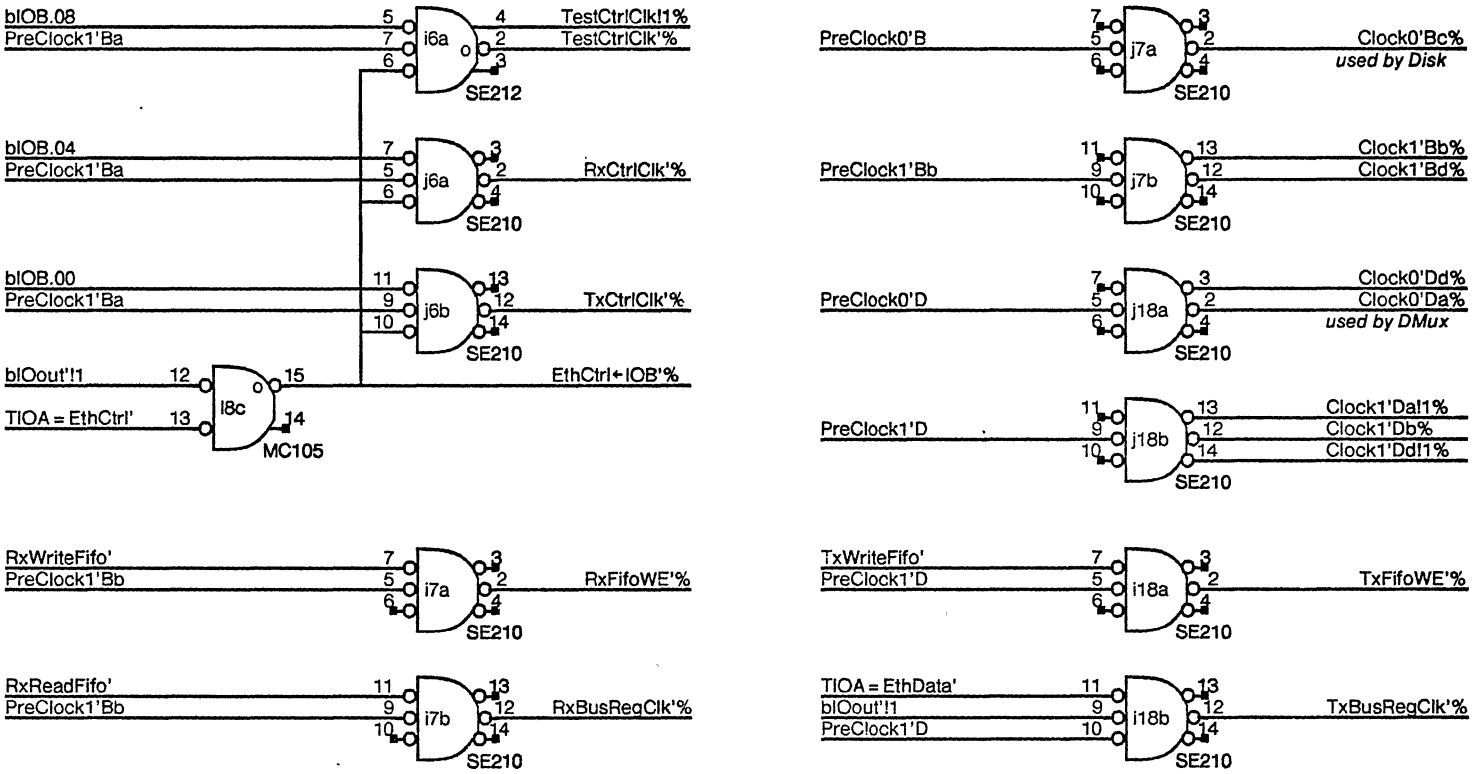
See Ether19.sil for timing diagrams

The slowest Dorado clock speed at which the transmitter works is 42.5 ns (T0 to T1)

525 ns < length of jam < 915 ns

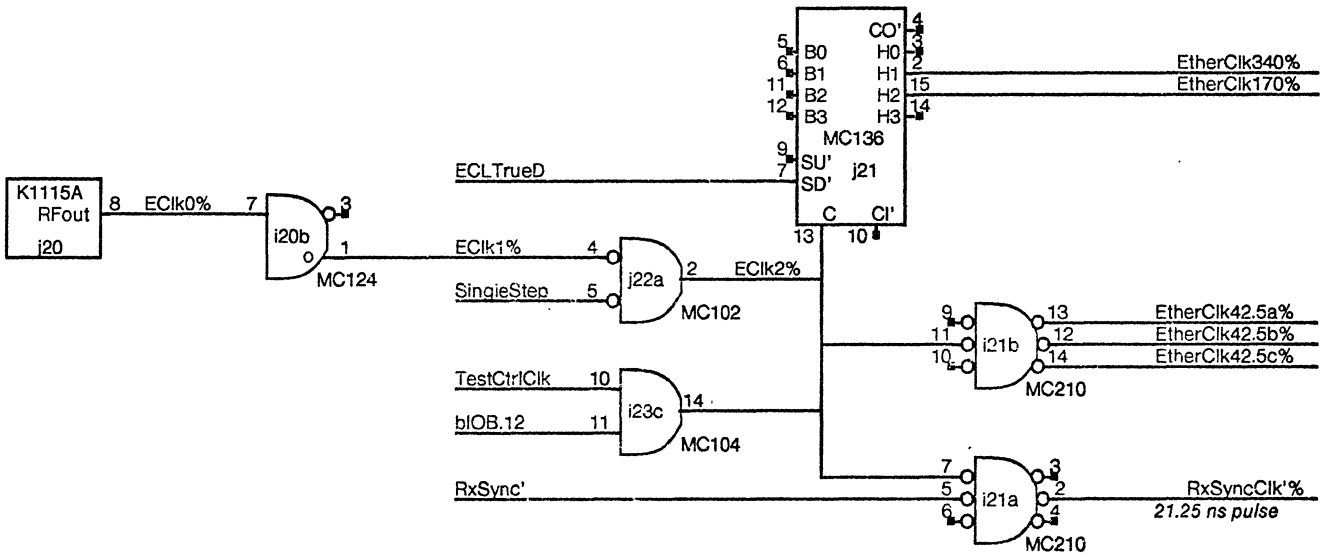


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Test Logic	Ether11.sil	David Boggs	Ce	7/08/79	34

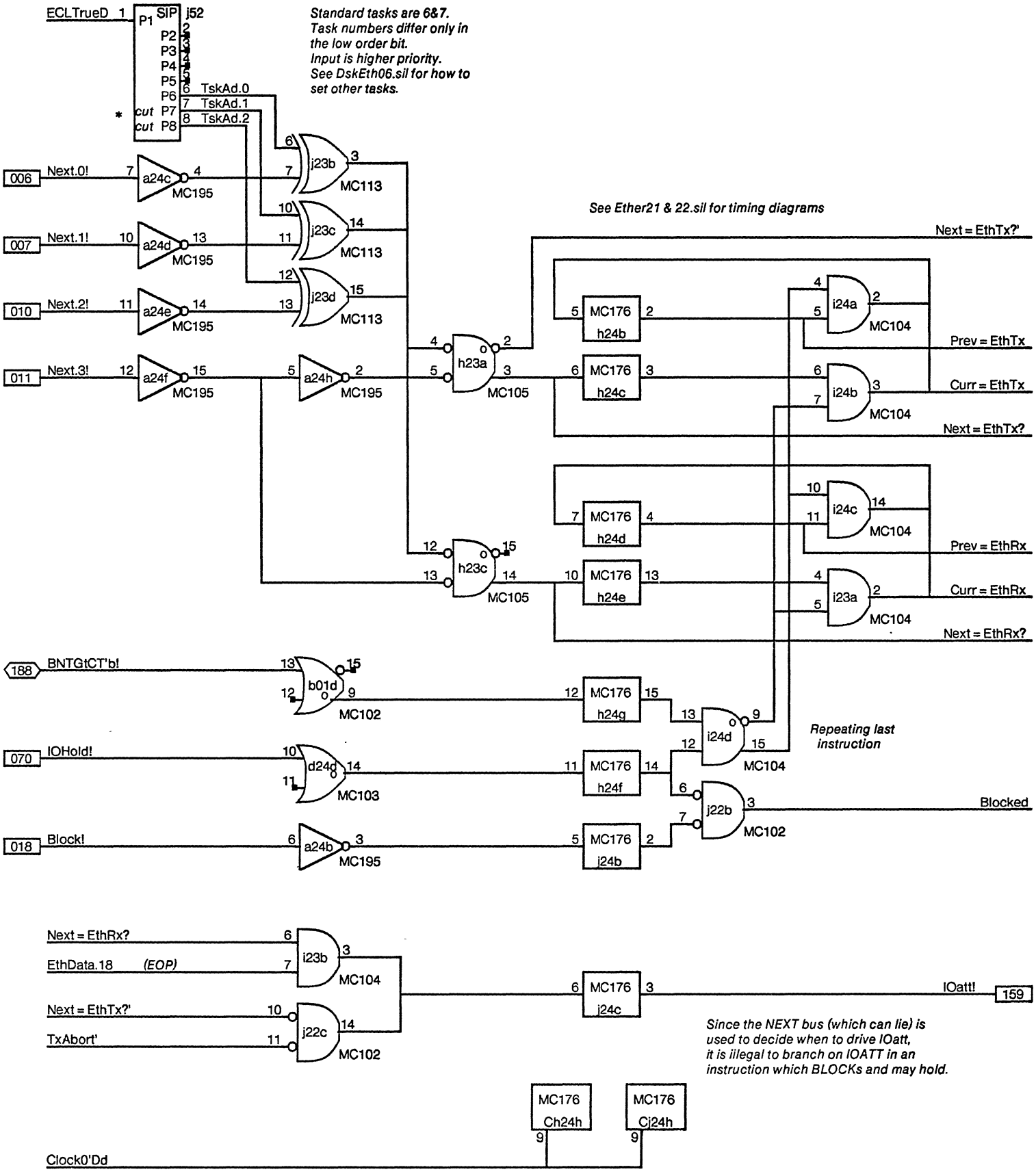


Dorado Synchronous Clocks

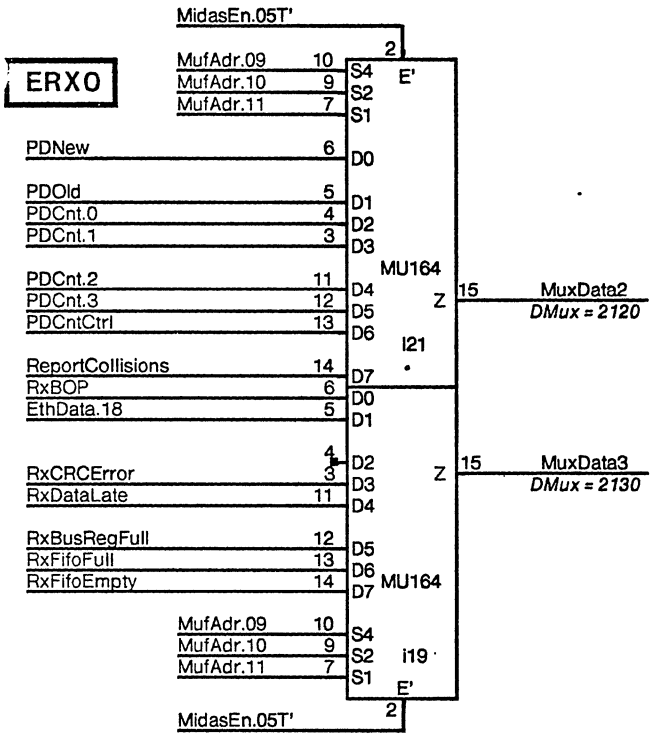
Free-running Ether Clocks

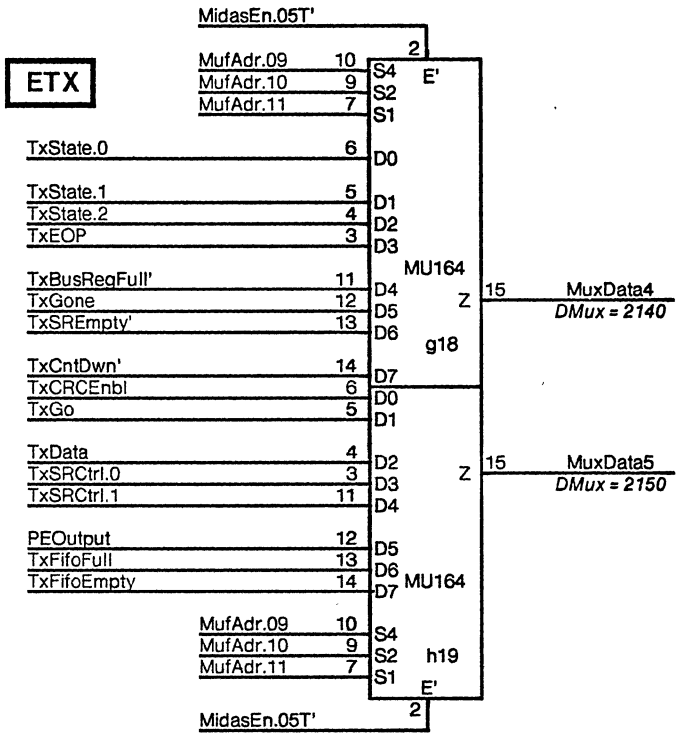


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clocks	Ether12.sil	David Boggs	Ce	9/24/79	35

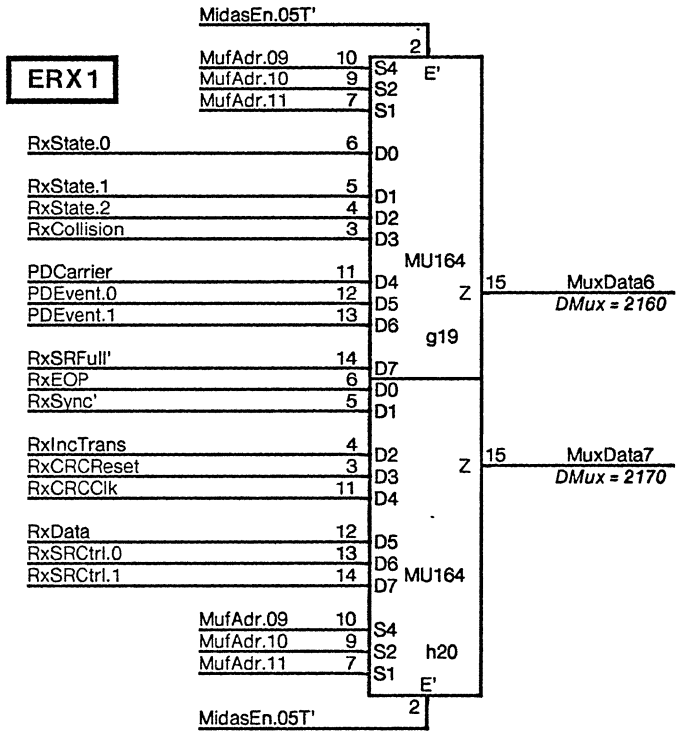


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Next & IOAttention	Ether13.sil	David Boggs	Ce	7/08/79	36

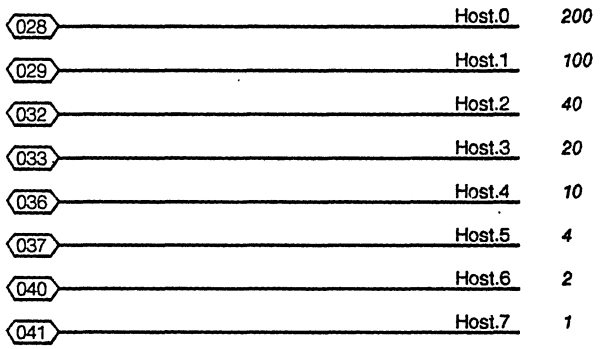


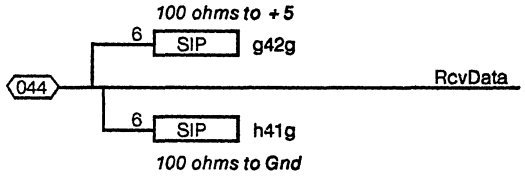


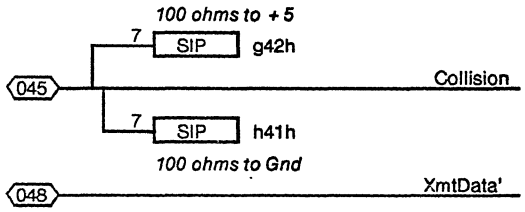
See DskEth01.sil for muffler control logic.
DMux addresses 2000-2117 are used by the disk.

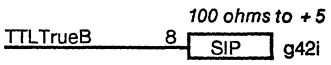


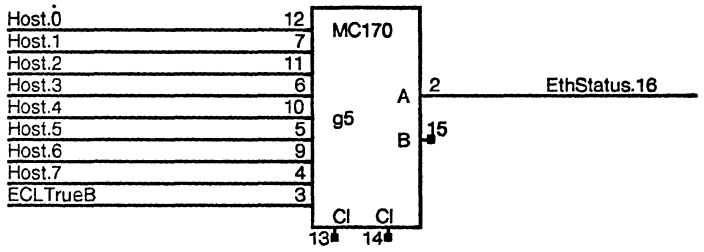
To set a host address bit to 1
pull it up to gnd through 91 ohms.

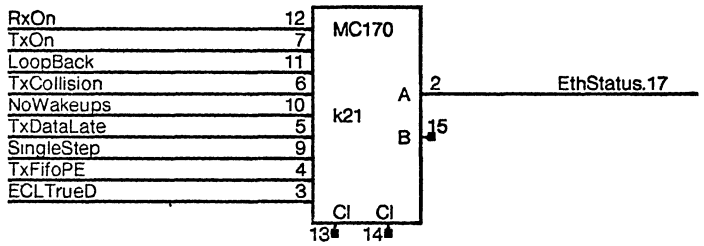


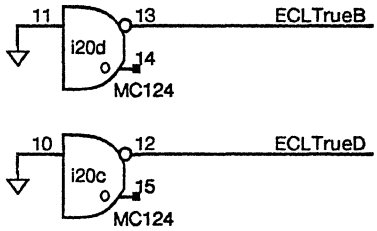


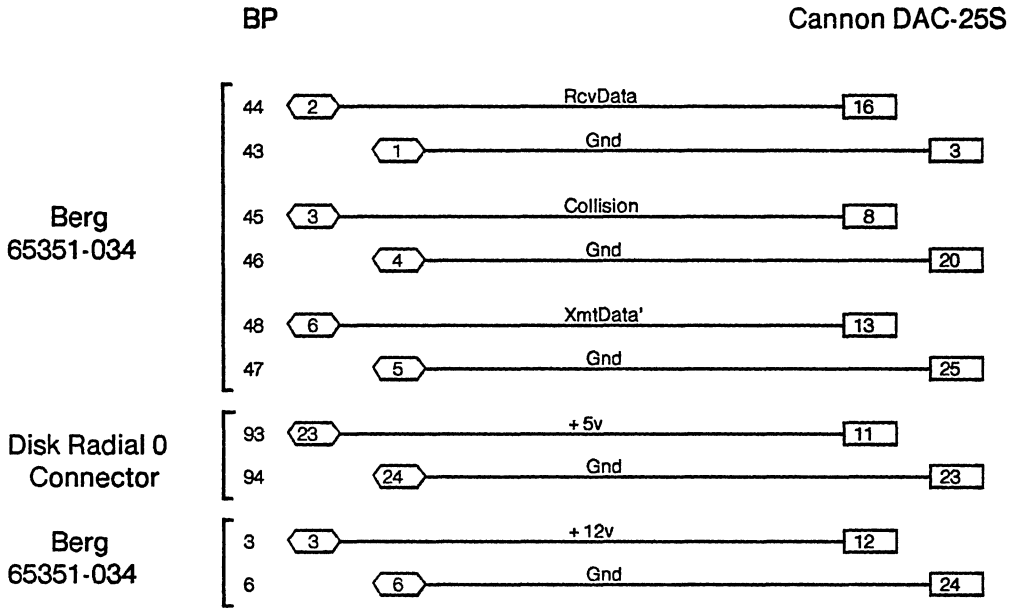






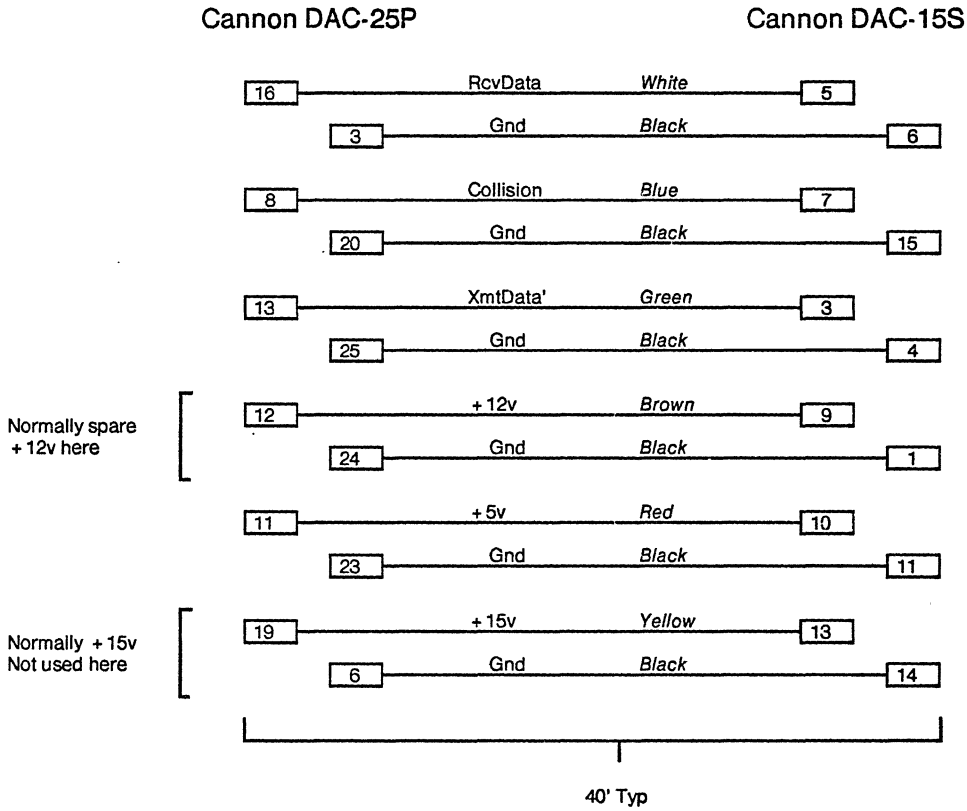




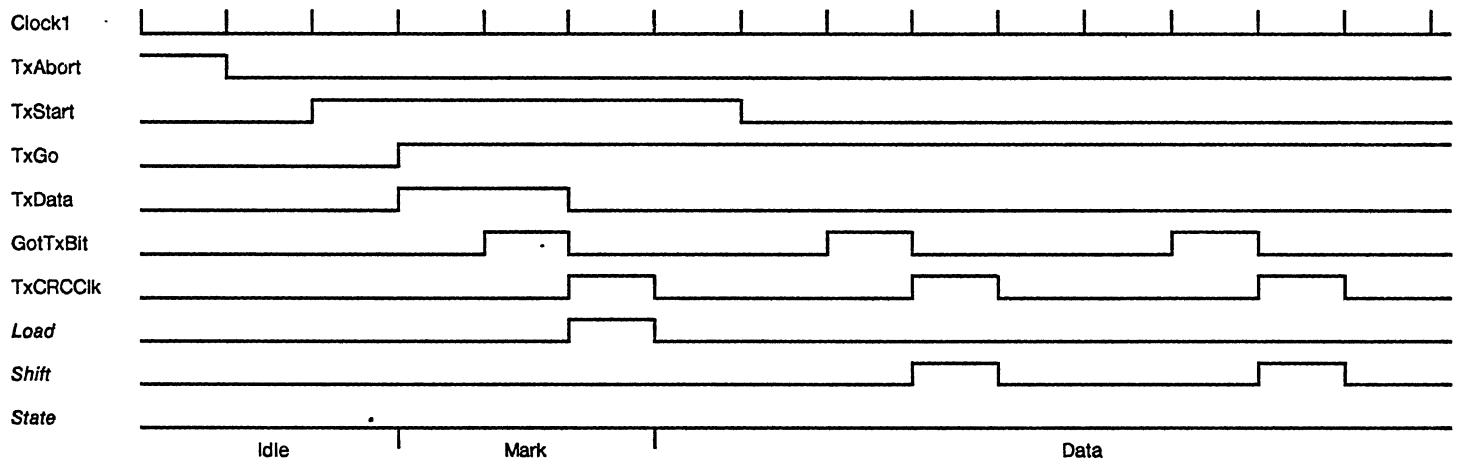


Internal Cable

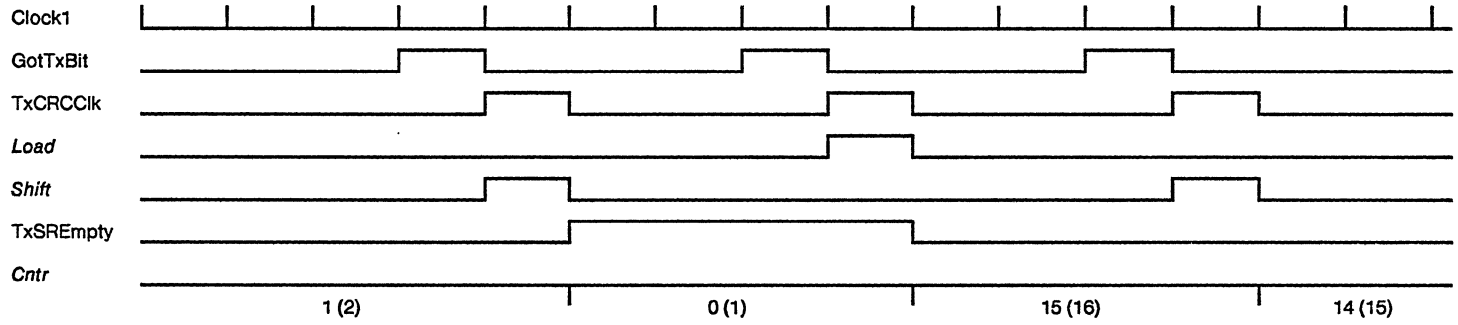
External Cable



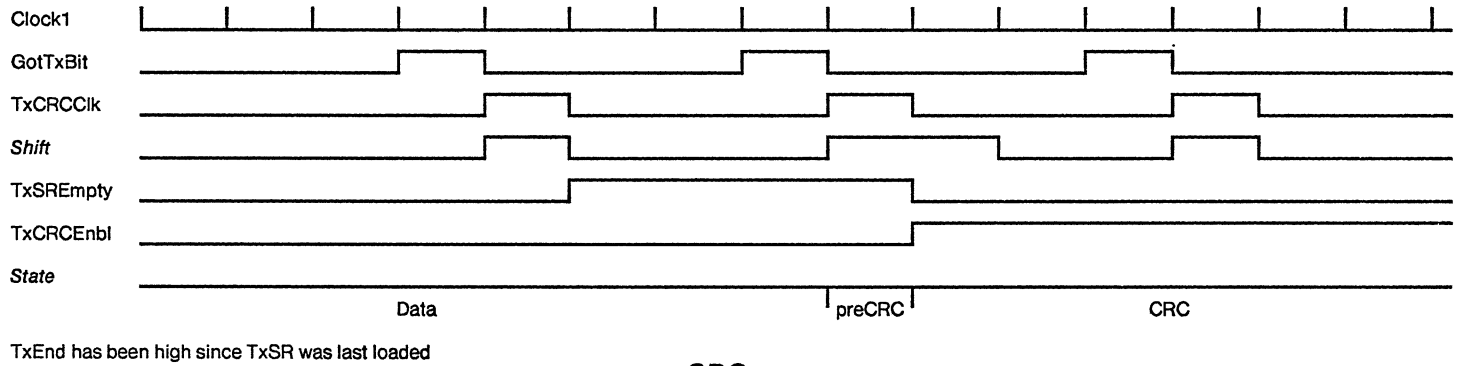
This is a standard Alto II
Ethernet external cable
part # 216411



Startup

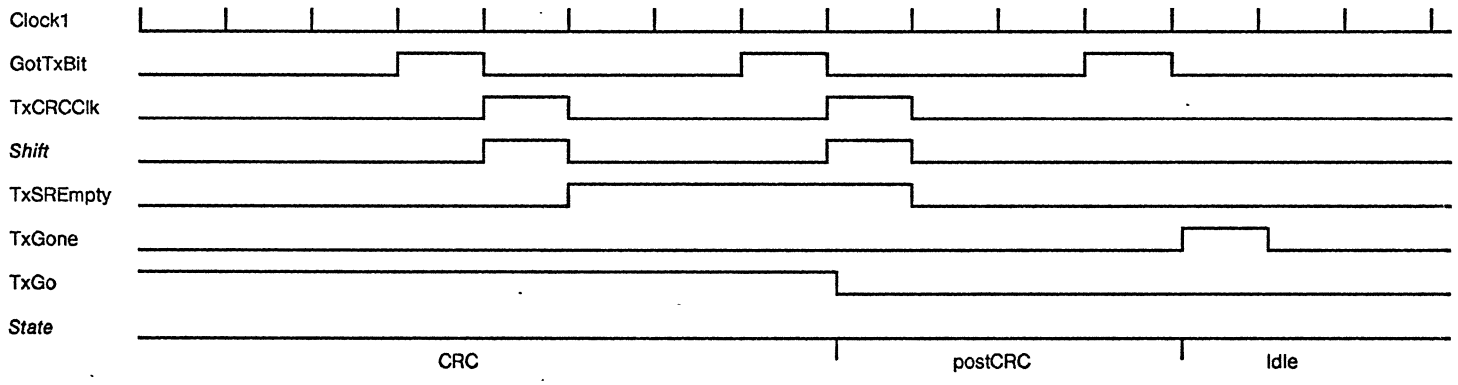


Loading Tx Shift Register



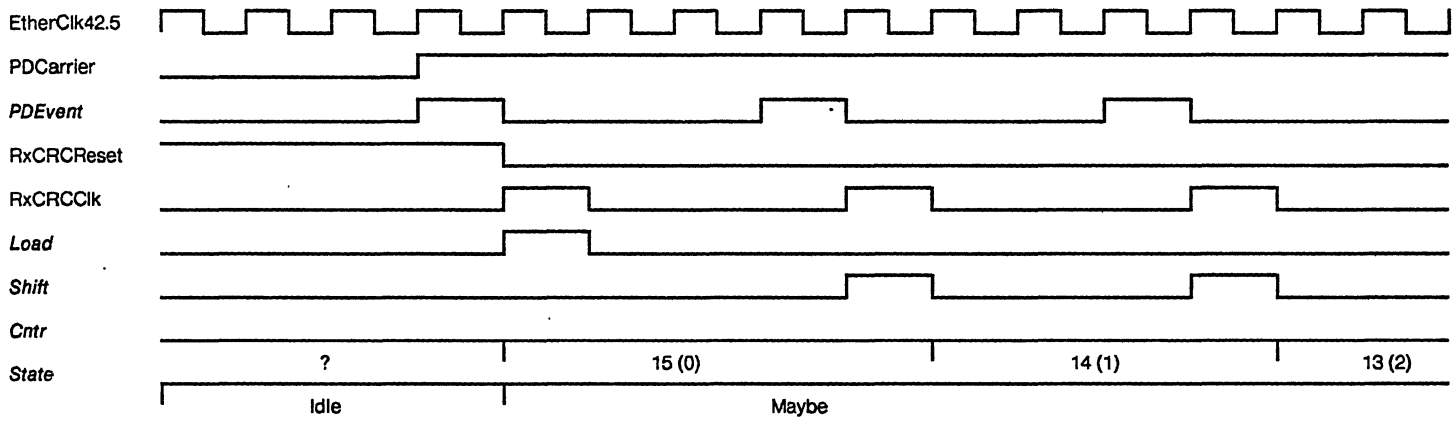
TxEnd has been high since TxSR was last loaded

CRC

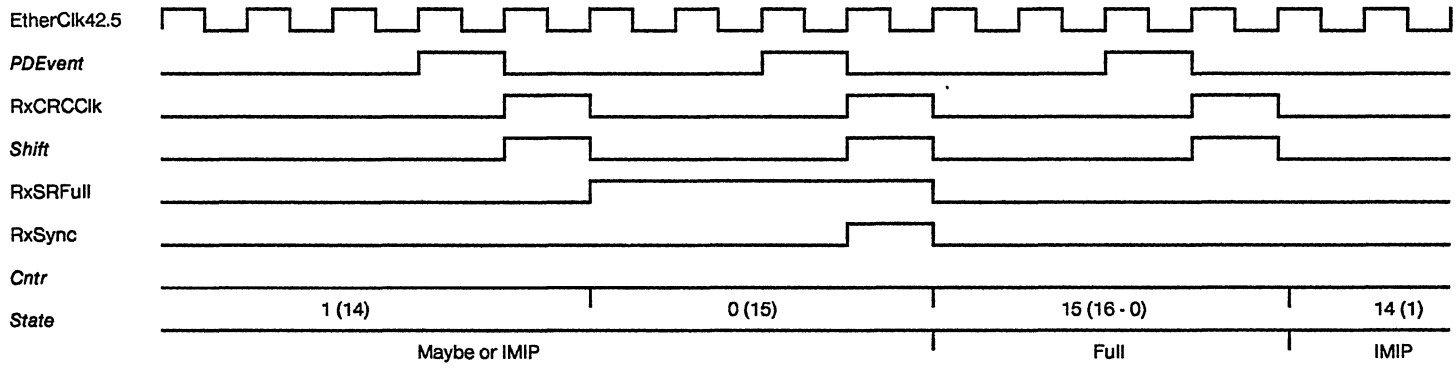


ShutDown

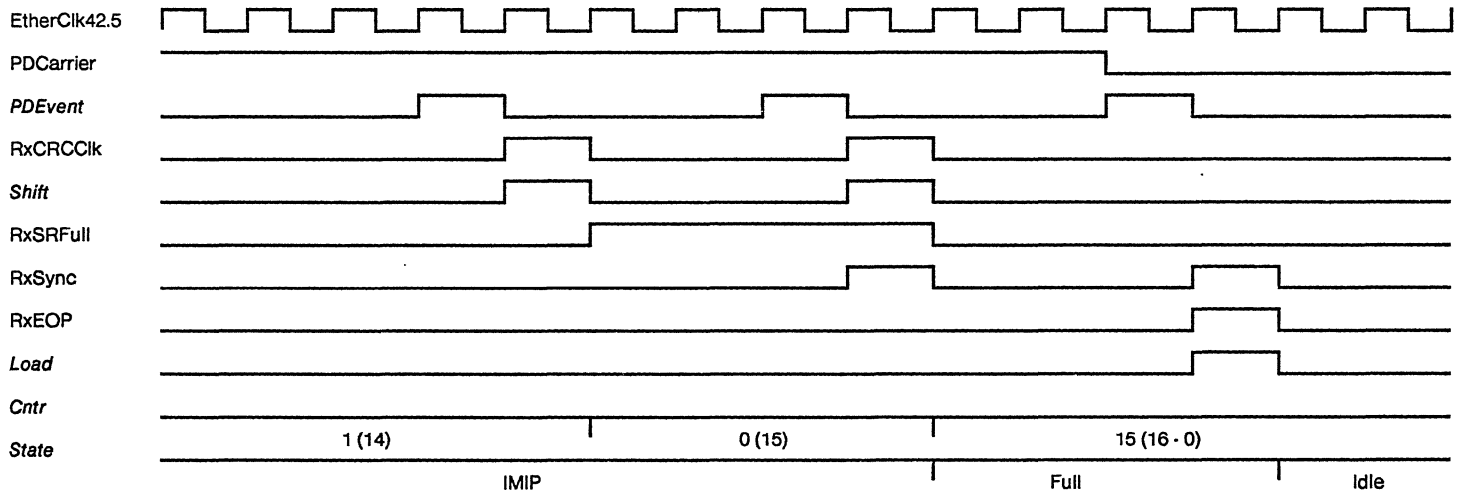
XEROX PARC	Project: Dorado	Reference: Transmitter Timing	File: Ether17.sil	Designer: David Boggs	Rev: Ce	Date: 7/08/79	Page: 40



Startup



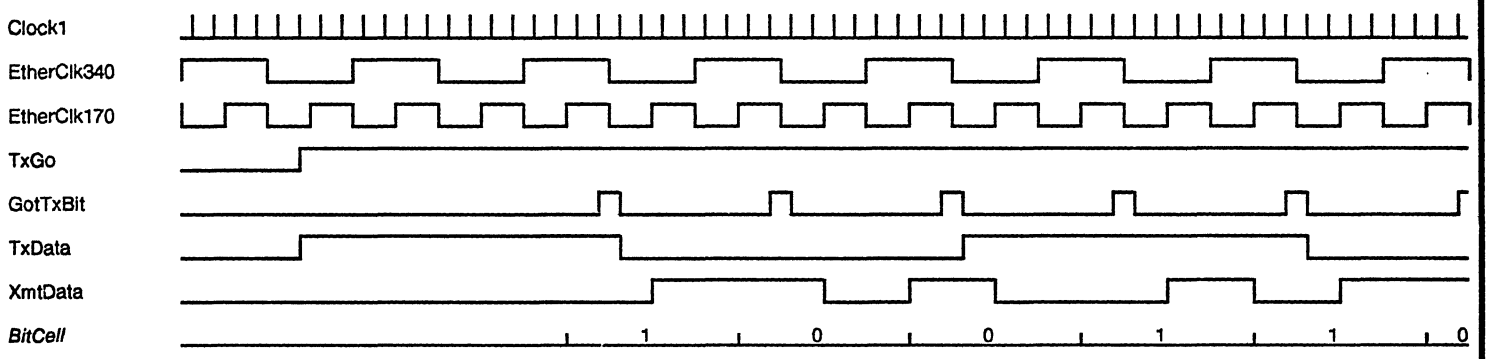
Dumping Rx Shift Register



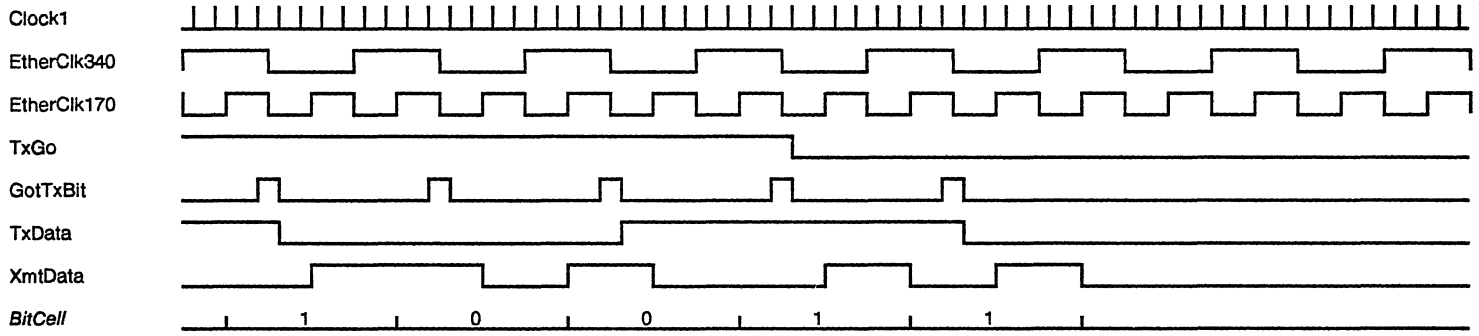
ShutDown

Cntr notation is <cntr value>(< # occupied postions>)
Phase decoder events are encoded in PDEvent.x
Shift and Load are encoded in RxSRCtrl.x
state is encoded in RxState.x
shift also decrements Cntr

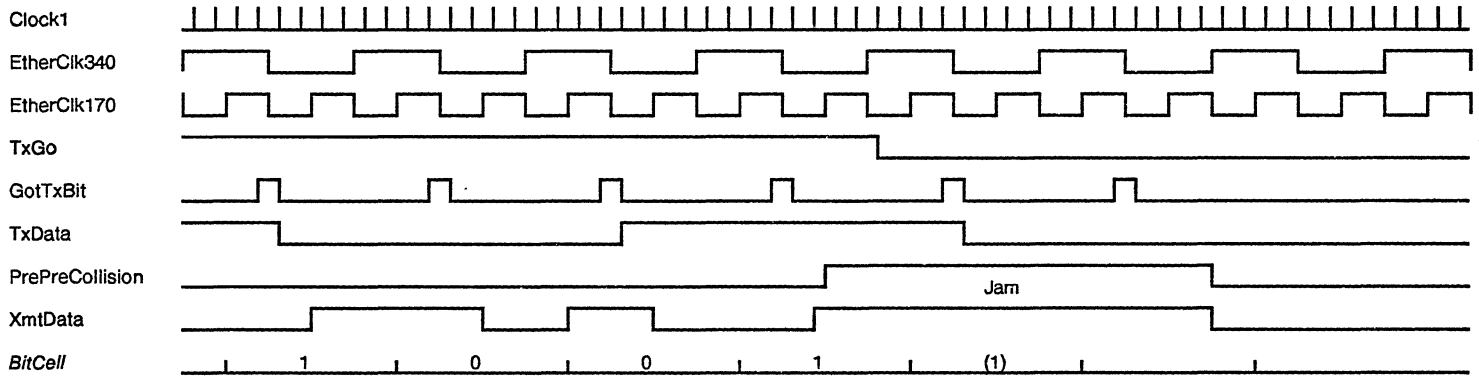
XEROX PARC	Project: Dorado	Reference: Receiver Timing	File: Ether18.sil	Designer: David Boggs	Rev: Ce	Date: 7/08/79	Page: 41



Startup



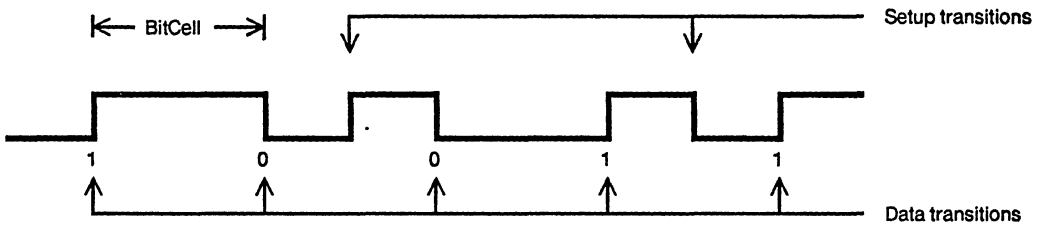
Shutdown



PrePreCollision is the output of the first stage of the Collision synchronizer

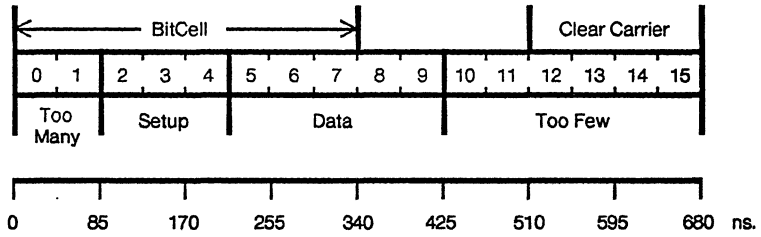
Collision

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Phase Encoder Timing	Ether19.sil	David Boggs	Ce	7/08/79	42



A bitcell is nominally 340 ns.

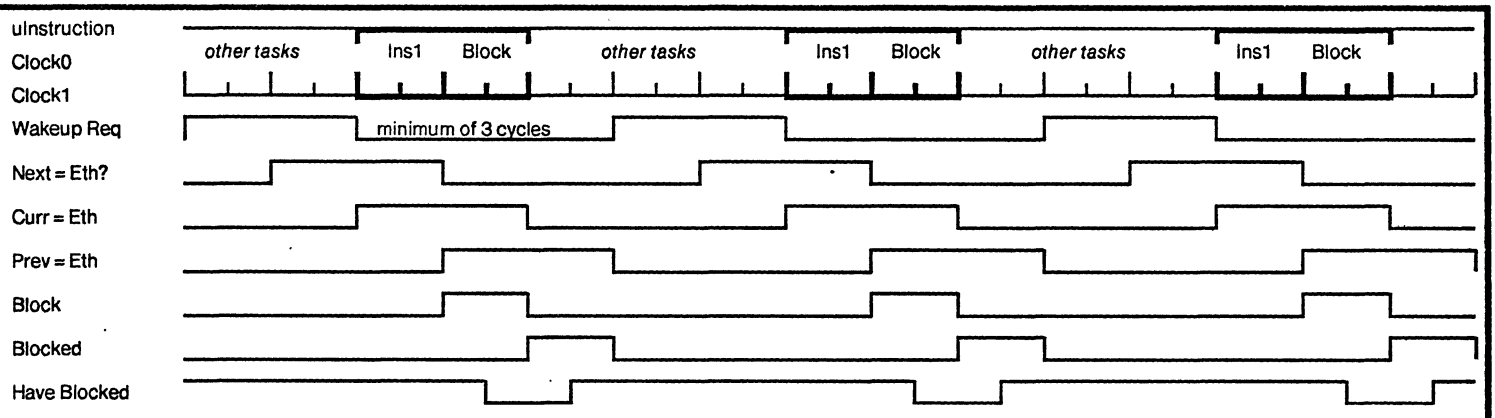
A sample is nominally 42.5 ns.



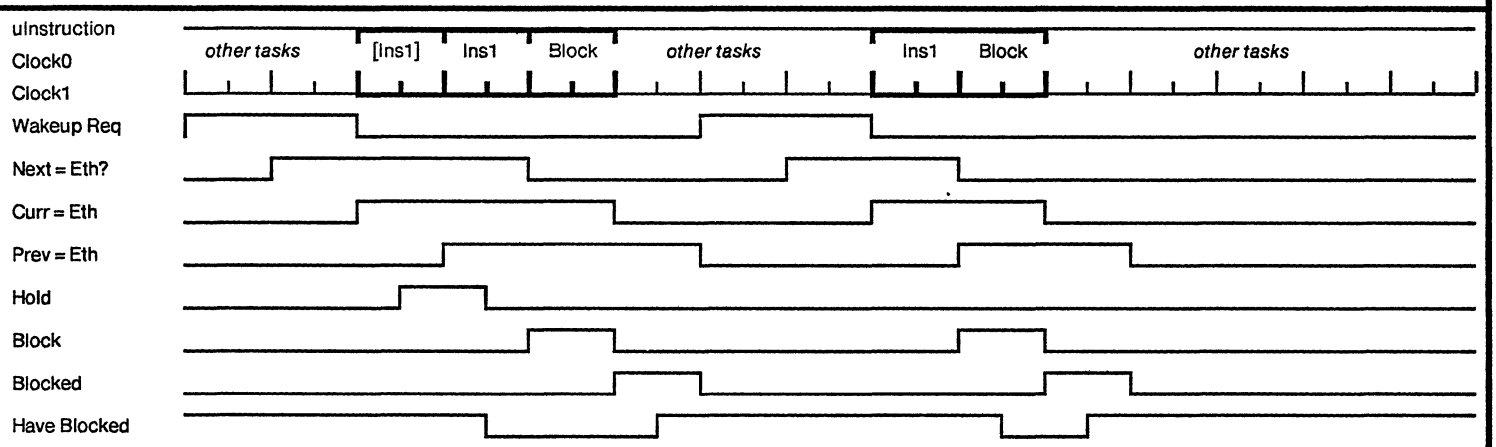
Inputs				Outputs			Comment
Carrier	Old	New	Cnt	Carrier	Event	CntCtrl	
Low	Low	Low	d/c	Low	NoEvent	Count	Idle
Low	Low	High	d/c	High	One	Reset	Start of packet (start bit)
Low	High	Low	d/c	High	Collision	Reset	Impossible
Low	High	High	d/c	Low	NoEvent	Count	Impossible
High	Low	High	0-1	High	Collision	Count	Too many transitions
High	High	Low	0-1	High	Collision	Count	Too many transitions
High	Low	High	2-4	High	NoEvent	Count	Setup transition (zero next)
High	High	Low	2-4	High	NoEvent	Count	Setup transition (one next)
High	Low	High	5-9	High	One	Reset	Data transition
High	High	Low	5-9	High	Zero	Reset	Data transition
High	Low	High	10-15	High	Collision	Reset	Too few transitions
High	High	Low	10-15	High	Collision	Reset	Too few transitions
High	Low	Low	0-11	High	NoEvent	Count	Active
High	High	High	0-11	High	NoEvent	Count	Active
High	Low	Low	12-15	Low	Collision	Reset	End of packet
High	High	High	12-15	High	Collision	Reset	Jam

"Impossible" conditions can happen right after power up.

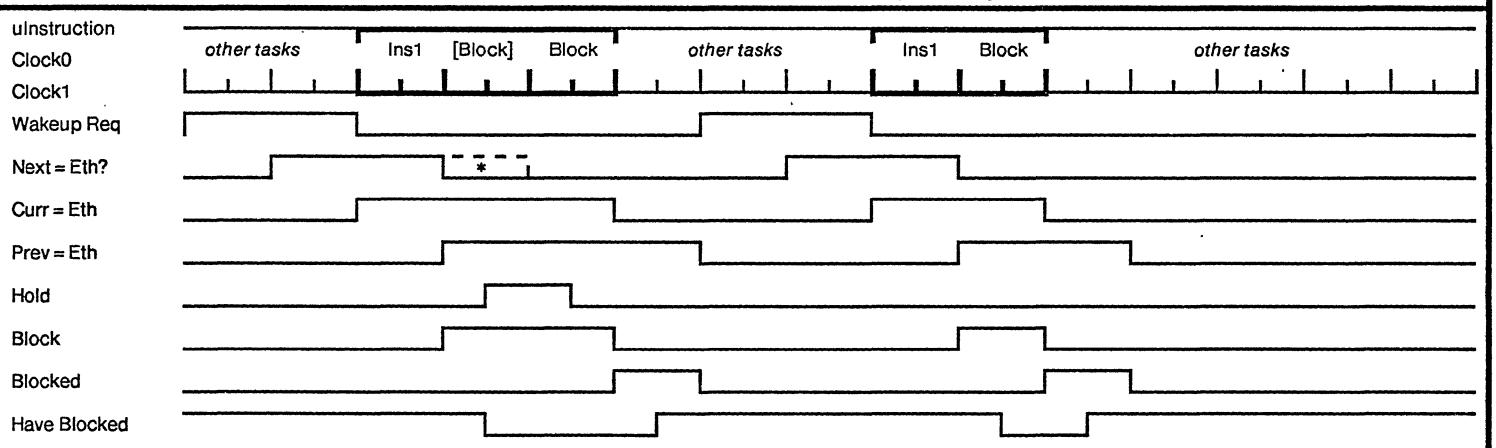
d/c means "don't care".



Normal case

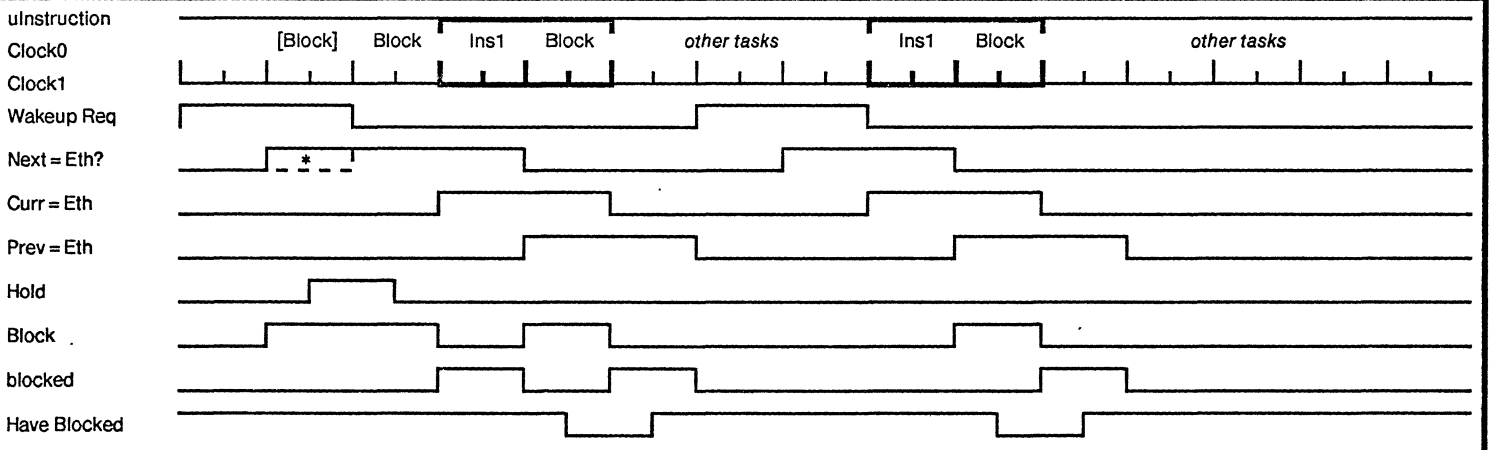


Hold in first instruction & not preempted



* NEXT bus is wrong

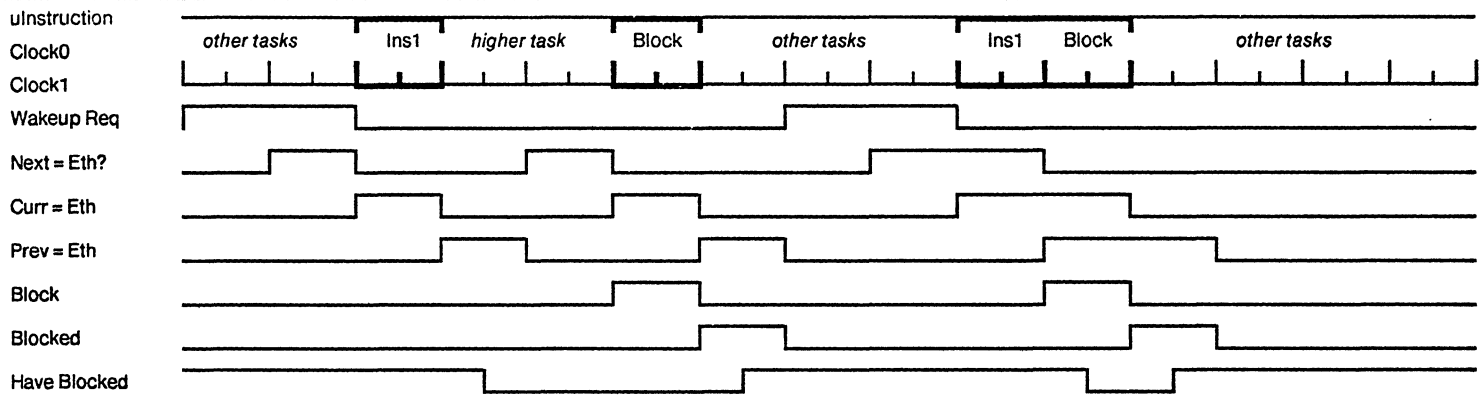
Block & Hold & not preempted



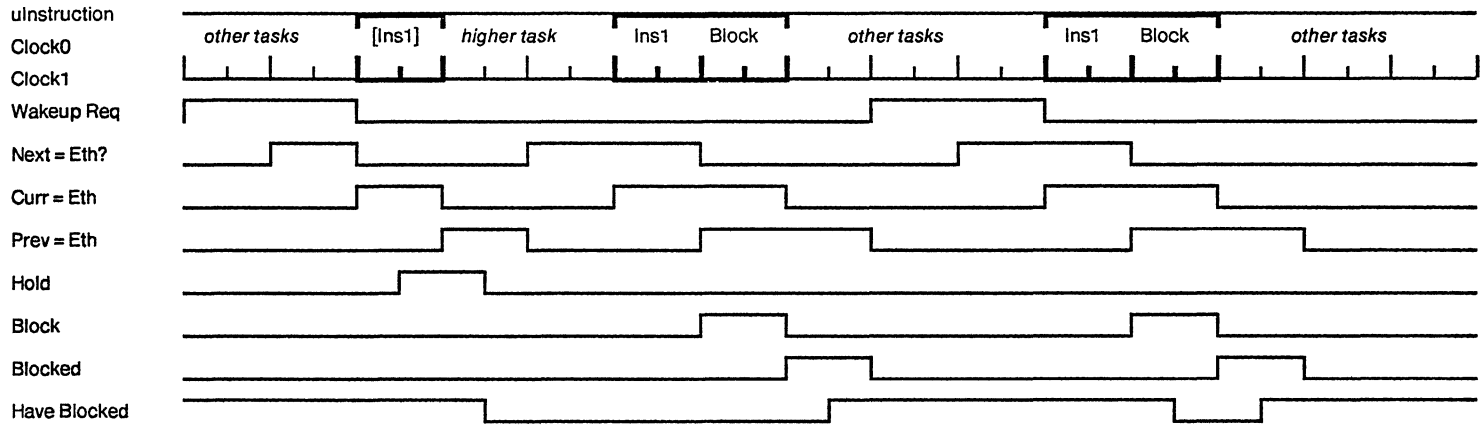
* NEXT bus is wrong

Block & Hold & (BNT = Eth < CTask)

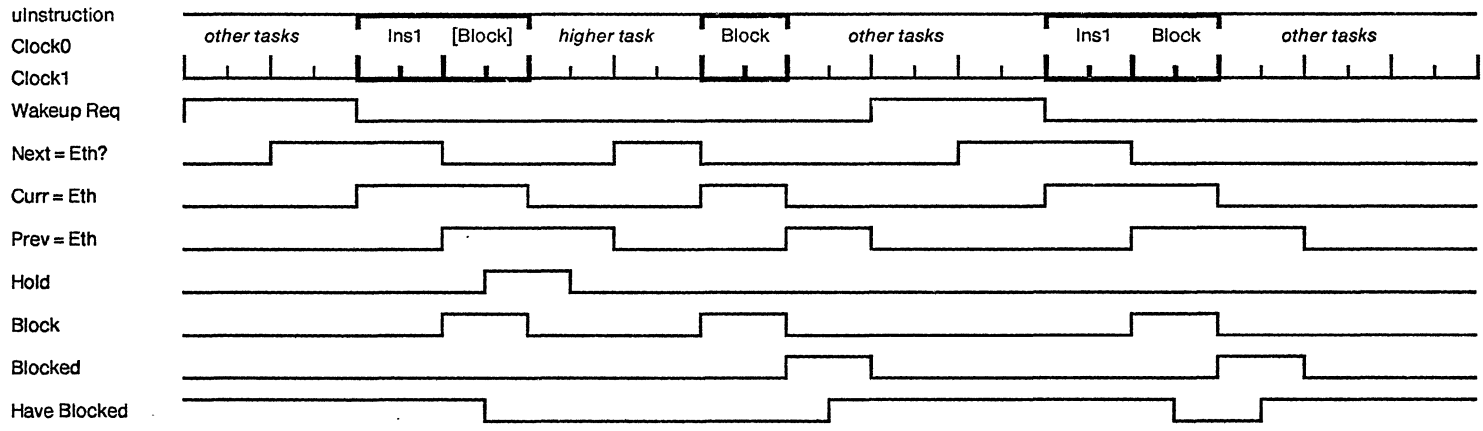
XEROX PARC	Project: Dorado	Reference: Wakeup Timing	File: Ether21.sil	Designer: David Boggs	Rev: Ce	Date: 7/08/79	Page: 44



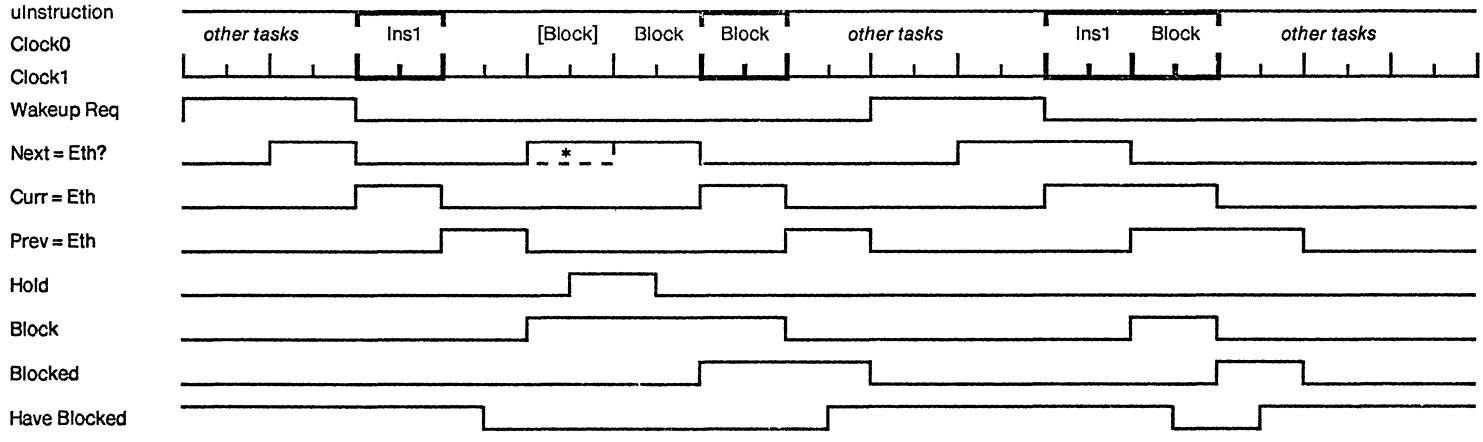
Preemption after first instruction



Hold in first instruction & then preempted



Block & Hold & then preempted



* NEXT bus is wrong

Block & Hold & (BNT = Eth < CTask) while Eth is preempted

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Wakeup Timing	Ether22.sil	David Boggs	Ce	7/08/79	45

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Tx Cmd Enbl'	Tx On	Tx EOP	Tx Cnt Dwn	Rx Cmd Enbl'	Rx On	Rx BOP'		Test Cmd Enbl'	Loop Back	Single Step	No Wake ups	Test Clock	Test Coll'	Test Data	Report Colls

Output

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Host Address								Rx On	Tx On	Loop Back	Tx Coll	No Wake ups	Tx Data Late	Single Step	Tx Fifo PE
028	029	032	033	036	037	040	041								

Input

The host address is set by jumpers on the right backplane.

To set a bit to one, pull it up to ground through 91 ohms.

Page Numbers: Yes First Page: 1
Columns: 2 Edge Margin: .8" Between Columns: .0"
Heading:
DskEth-Rev-Ce.ps
COMPONENTS:

8T98:	10	11	34			
DISC:	12					
F00:	8	15				
F145A:	9	15	26	30		
F16:	9	10	14	19	24	27
	31					
F9401:	27	31				
K1115A:	35					
LS08:	12					
LS153:	12					
LS155:	11					
LS169:	12					
LS174:	11	12				
MC100:	9					
MC102:	1	4	8	10	14	17
	19	28	29	31	32	34
	35	36				
MC103:	3	4	9	11	14	16
	17	19	27	29	36	
MC104:	8	10	13	19	30	31
	32	33	35	36		
MC105:	27	31	33	35	36	
MC106:	32	33				
MC109:	11	17	28	29		
MC113:	16	36				
MC124:	11	12	27	31	34	35
	38					
MC125:	10	11	13	27	31	34
MC135:	8	10	11	14	27	28
	29	30	31	33		
MC136:	9	25	32	35		
MC141:	26	30				
MC149:	10	14	24	25	27	31
	32					
MC158:	14	15	16	27	31	34
MC161:	2					
MC1650:	13					
MC166:	1	2				
MC1664:	1	4				
MC170:	15	17	26	30	38	
MC171:	8					
MC173:	1	10	15	17		
MC174:	3	13				
MC175:	2	34				
MC176:	1	10	13	14	15	16
	19	24	25	26	27	28
	29	30	31	32	36	
MC195:	9	13	14	17	28	29
	36					
MC197:	2	8	14	15	16	17
MC210:	35					
MC231:	1	8	14	15	16	17
	19	26	27	28	29	31
	33					
MU164:	1	18	37			
N123:	12					
N125:	13					
S288:	11					
SE210:	4	10	19	35		
SE211:	14	19				
SE212:	1	4	19	28	35	
SE231:	4					
SG139:	9					
SIP:	1	2	20	36	38	
SPARE:	4					
TEMP:	4					
TERM:	11					

SIGNAL NAMES:

```
+:              1(1)   2(1)   3(1)   4(1)   8(1)   9(1)
               10(1)  11(1)  12(1)  13(1)  14(1)  15(1)
               16(1)  17(1)  18(1)  19(1)  20(1)  24(1)
               25(1)  26(1)  27(1)  28(1)  29(1)  30(1)
               31(1)  32(1)  33(1)  34(1)  35(1)  36(1)
               37(1)  38(1)
Active:         8(3)  10(1)  18(1)
bClkEn':        1(1)  27(1)  31(1)  33(1)
bClkEn'%:       4(1)
bIOB.00:        2(1)  10(1)  15(1)  17(2)  30(1)  35(1)
bIOB.01:        2(1)  10(1)  15(1)  17(2)  29(1)  30(1)
bIOB.02:        2(1)  10(1)  15(1)  17(2)  29(1)  30(1)
bIOB.03:        2(1)  10(1)  15(1)  17(2)  29(1)  30(1)
bIOB.04:        2(1)   9(1)  10(1)  15(1)  17(2)  28(1)
               30(1)  35(1)
bIOB.05:        2(1)   8(1)   9(1)  10(1)  15(1)  17(2)
               28(1)  30(1)
bIOB.06:        2(1)   8(1)   9(1)  10(1)  15(1)  17(2)
               28(1)  30(1)
bIOB.07:        2(1)   8(1)   9(1)  10(1)  15(1)  17(2)
               30(1)
bIOB.08:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  35(1)
bIOB.09:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  34(1)
bIOB.10:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  34(1)
bIOB.11:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  34(1)
bIOB.12:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  35(1)
bIOB.13:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  34(1)
bIOB.14:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  34(1)
bIOB.15:        1(1)   2(1)   8(1)   9(1)  10(1)  15(1)
               17(1)  30(1)  34(1)
bIOB.16:        2(1)  15(1)  17(1)  30(1)
bIOB.17:        2(1)  15(1)  17(1)  30(1)
bIOin':         3(1)  14(1)  28(1)
bIOin'%:        4(1)
bIOout'!0:      1(1)  17(1)  19(4)
bIOout'!1:     29(1)  35(2)
bIOout'!1%:     4(1)
bIOReset:       8(1)  27(2)  28(1)  29(1)  34(1)
bIOReset%:      4(1)
BitClock'A:    16(1)  19(1)
BitClock'A%:   19(1)
BitClock'B:     8(1)  15(5)
BitClock'B%:   19(1)
BitClock'C:    10(1)  11(1)  14(1)
BitClock'C%:   19(1)
Block!:        36(1)
Blocked:       28(1)  29(1)  36(1)
BlockTillIndex: 8(1)  17(1)
BlockTilRdy:    8(1)  17(1)
BNTGtCT'b!:    36(1)
C0:            12(1)
C1:            12(1)
C2:            12(1)
C3:            12(1)
CheckBlock':    8(1)  15(1)  17(1)  18(1)
CheckData':    15(2)
CheckSumErr:   16(1)  17(1)
CkFifoParity': 15(2)
ClearErrors:    8(1)  14(2)  15(1)  16(1)  17(3)
ClearIndexTW:  17(2)
ClearSectorTW: 17(2)
ClearTWs:      14(3)  15(1)  17(2)
CLK.disk':      4(1)
Clk0%:          4(1)
Clk1%:          4(1)
CLKEnable'a!:   4(1)
Clock0'Bc:     17(1)
Clock0'Bc%:    35(1)
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Clock0'Da:        1(1)
Clock0'Da%:      35(1)
Clock0'Dd:       36(1)
Clock0'Dd%:      35(1)
Clock1'Bb:       27(2)   28(2)
Clock1'Bb%:      35(1)
Clock1'Bd:       27(2)
Clock1'Bd%:      35(1)
Clock1'Ca:        8(1)   14(3)
Clock1'Ca%:      19(1)
Clock1'Cb:       17(2)
Clock1'Cb%:      19(1)
Clock1'Cc:       17(1)
Clock1'Cc%:      19(1)
Clock1'Da!0:     30(4)
Clock1'Da!1%:    35(1)
Clock1'Da!2:     32(1)
Clock1'Db:       27(1)   31(2)
Clock1'Db%:      35(1)
Clock1'Dd!0:     31(2)
Clock1'Dd!1%:    35(1)
Clock1'Dd!2:     33(1)
ClockM0:         20(1)
ClockM0!:        13(1)
ClockM1:         20(1)
ClockM1!:        13(1)
ClockM2:         20(1)
ClockM2!:        13(1)
ClockM3:         20(1)
ClockM3!:        13(1)
ClockP0:         20(1)
ClockP0!:        13(1)
ClockP1:         20(1)
ClockP1!:        13(1)
ClockP2:         20(1)
ClockP2!:        13(1)
ClockP3:         20(1)
ClockP3!:        13(1)
CntDone':         9(3)   18(1)
Collision:       34(1)   38(1)
CompareErr':     16(1)   17(1)
ComputeECC:       9(1)   16(1)   18(1)
ComputeECC':      9(1)   16(2)
ContErrs':       11(1)
ContRegCl':       8(1)   16(1)
ControlRegCl:     8(2)    9(1)
ControlRegCl%:   19(1)
ControlRegCl':    8(2)
ControlRegCl'%:  19(1)
ControlTag:      10(2)   18(1)
ContTag':        10(1)   20(1)
Curr=EthRx:      28(1)   36(1)
Curr=EthTx:      29(1)   36(1)
CylinderTag:     10(2)   18(1)
CylinderTag':    10(1)   20(1)
CylOffset:       11(2)   18(1)
DataM0:          13(1)   20(1)
DataM0!:         13(1)
DataM1:          13(1)   20(1)
DataM1!:         13(1)
DataM2:          13(1)   20(1)
DataM2!:         13(1)
DataM3:          13(1)   20(1)
DataM3!:         13(1)
DataP0:          13(1)   20(1)
DataP0!:         13(1)
DataP1:          13(1)   20(1)
DataP1!:         13(1)
DataP2:          13(1)   20(1)
DataP2!:         13(1)
DataP3:          13(1)   20(1)
DataP3!:         13(1)
DebugMode:        8(3)   18(1)
DevCheck:        11(2)   18(1)
dFifoParityErr:  15(2)
dIOBParityErr:   17(1)
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DisableCnt:      10(1)
DisableRun:       8(4)   11(1)   17(2)
DiskTW:          17(1)
DMadr.01:         1(3)
DMadr.02:         1(3)
DMadr.03:         1(3)
DMadr.04:         1(4)
DMadr.05:         1(3)
DMadr.06:         1(3)
DMadr.07:         1(3)
DMadr.08:         1(3)
DMadr.09:         1(3)
DMadr.10:         1(3)
DMadr.11:         1(3)
DMuxClk!:         1(1)
DMuxData:         1(1)
DMuxData!:        1(1)
DriveTag:        10(1)   18(1)
DriveTag':       10(1)   20(1)
DrSelected:      10(1)   12(1)
DskData.00:       3(1)   15(1)
DskData.01:       3(1)   15(1)
DskData.02:       3(1)   15(1)
DskData.03:       3(1)   15(1)
DskData.04:       3(1)   15(1)
DskData.05:       3(1)   15(1)
DskData.06:       3(1)   15(1)
DskData.07:       3(1)   15(1)
DskData.08:       3(1)   15(1)
DskData.09:       3(1)   15(1)
DskData.10:       3(1)   15(1)
DskData.11:       3(1)   15(1)
DskData.12:       3(1)   15(1)
DskData.13:       3(1)   15(1)
DskData.14:       3(1)   15(1)
DskData.15:       3(1)   15(1)
DskData.16:       3(1)   15(1)
DskData.17:       3(1)   15(1)
EccComputeErr': 16(1)
EccData.21:      16(4)
EccData.32:      15(2)   16(4)
EClk0%:          35(1)
EClk1%:          35(1)
EClk2%:          35(1)
ECLTrueA:         2(2)    3(1)   13(8)   15(2)   17(2)   19(1)
ECLTrueB:        25(1)   26(2)   27(2)   38(2)
ECLTrueC:         9(3)   10(2)   14(3)   15(2)   19(1)
ECLTrueD:         1(1)   30(3)   31(3)   32(1)   33(1)   35(1)
                 36(1)   38(2)
EmptyBlock':      8(2)
EnableRun:        8(1)   18(1)
EnCheckTW':      15(1)   17(1)
EnReadTW':       15(1)   17(1)
EnWriteTW':       8(1)   15(1)   17(1)
EthCtrl←IOB':    28(1)
EthCtrl←IOB'%:   35(1)
EthData.00:       3(1)   26(1)
EthData.01:       3(1)   26(1)
EthData.02:       3(1)   26(1)
EthData.03:       3(1)   26(1)
EthData.04:       3(1)   26(1)
EthData.05:       3(1)   26(1)
EthData.06:       3(1)   26(1)
EthData.07:       3(1)   26(1)
EthData.08:       3(1)   26(1)
EthData.09:       3(1)   26(1)
EthData.10:       3(1)   26(1)
EthData.11:       3(1)   26(1)
EthData.12:       3(1)   26(1)
EthData.13:       3(1)   26(1)
EthData.14:       3(1)   26(1)
EthData.15:       3(1)   26(1)
EthData.16:       3(1)   26(1)
EthData.17:       3(1)   26(1)
EthData.18:      26(1)   36(1)   37(1)
EthData.18':     26(1)   28(1)
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EtherClk170:     33(2)
EtherClk170%:    35(1)
EtherClk340:     33(2)
EtherClk340%:    35(1)
EtherClk42.5a:   24(1)
EtherClk42.5a%:  35(1)
EtherClk42.5b:   25(1)
EtherClk42.5b%:  35(1)
EtherClk42.5c:   26(1)
EtherClk42.5c%:  35(1)
EthStatus.16:     3(1)   38(1)
EthStatus.17:     3(1)   38(1)
FHCP:             2(1)   14(1)
FHCP%:            4(1)
FifoAddr.0:      14(1)   15(5)
FifoAddr.1:      14(1)   15(5)
FifoAddr.2:      14(1)   15(5)
FifoAddr.3:      14(1)   15(5)
FifoCl:          14(1)
FifoCl%:         19(1)
FifoCl':         15(5)
FifoCl'%:        19(1)
FifoEmpty:       14(3)
FifoFull:        14(3)
FifoOverflow:    11(1)   14(2)   18(1)
FifoParityErr:   11(1)   15(2)   18(1)
FifoRaddr.0:     14(3)   18(1)
FifoRaddr.1:     14(3)   18(1)
FifoRaddr.2:     14(3)   18(1)
FifoRaddr.3:     14(3)   18(1)
FifoUnderflow:   11(1)   14(2)   18(1)
FifoWaddr.0:     14(3)   18(1)
FifoWaddr.1:     14(3)   18(1)
FifoWaddr.2:     14(3)   18(1)
FifoWaddr.3:     14(3)   18(1)
FifoWaddrCl':    14(1)
FifoWaddrCl'%:   19(1)
Gnd:              1(1)    2(1)    3(1)    4(1)    8(1)    9(1)
                 10(1)   11(1)   12(1)   13(1)   14(1)   15(1)
                 16(1)   17(1)   18(1)   19(1)   20(1)   24(1)
                 25(1)   26(1)   27(1)   28(1)   29(1)   30(1)
                 31(1)   32(1)   33(1)   34(1)   35(1)   36(1)
                 37(1)   38(1)
GND:              4(1)   12(5)   20(1)
HeadOvfl:        11(2)   18(1)
HeadTag:         10(2)   18(1)
HeadTag':        10(1)   20(1)
Host.0:           3(1)   38(2)
Host.1:           3(1)   38(2)
Host.2:           3(1)   38(2)
Host.3:           3(1)   38(2)
Host.4:           3(1)   38(2)
Host.5:           3(1)   38(2)
Host.6:           3(1)   38(2)
Host.7:           3(1)   38(2)
Idle:             8(2)    9(3)   10(1)
Index':          12(1)   17(1)
IndexTW:          8(1)   17(1)   18(1)
InRegCl':        15(5)
InRegCl'%:       19(1)
InRegFull:       14(1)   18(1)
InRegFull':      14(2)   19(2)
InReg←IOB:       14(1)   19(1)
InReg←IOB%:      19(1)
InReg←SR:        19(1)
InReg←SR':       14(1)   15(5)   19(1)
IOatt!:          36(1)
IOB.00:           3(1)
IOB.00!:          2(1)
IOB.01:           3(1)
IOB.01!:          2(1)
IOB.02:           3(1)
IOB.02!:          2(1)
IOB.03:           3(1)
IOB.03!:          2(1)
IOB.04:           3(1)
```