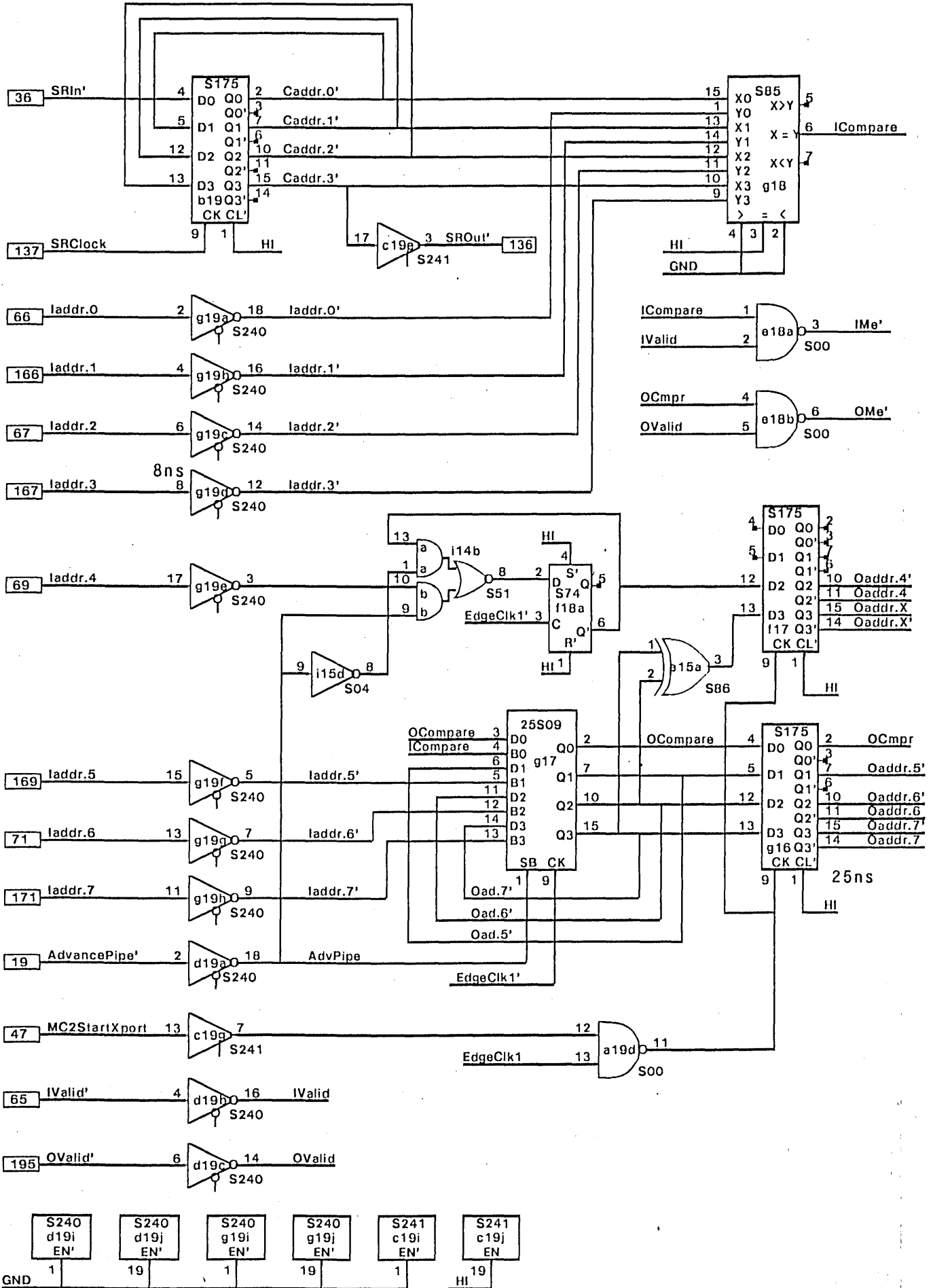
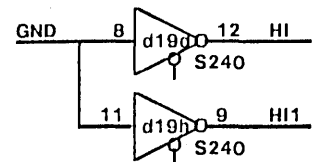
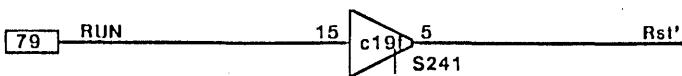
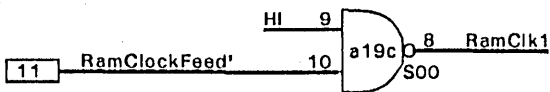
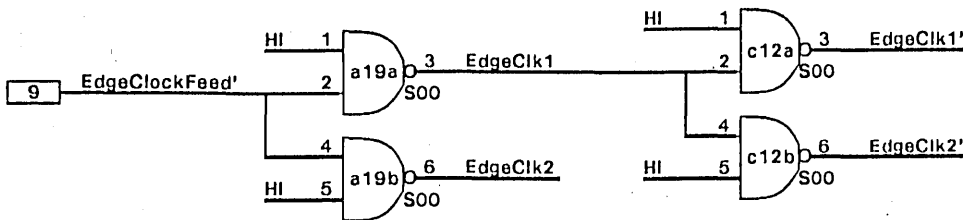
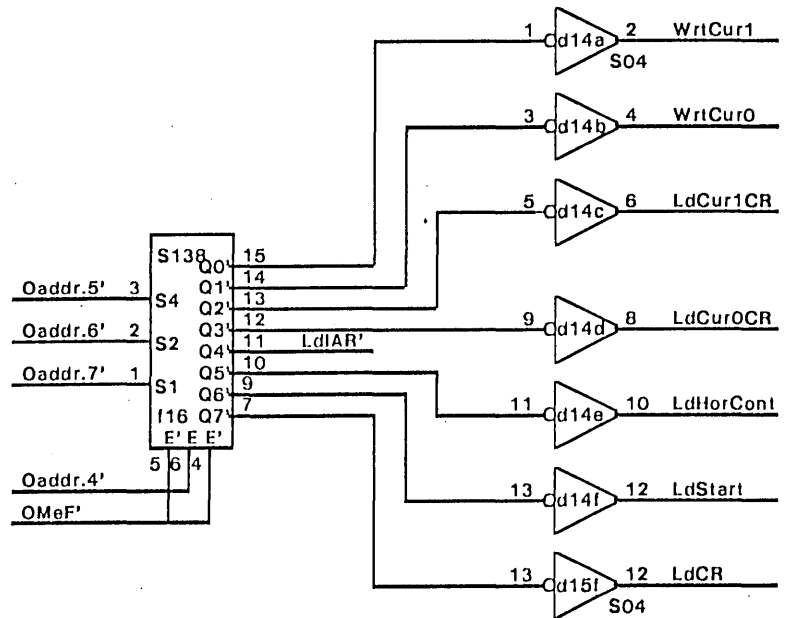
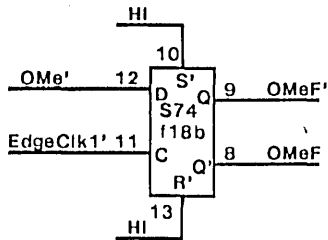
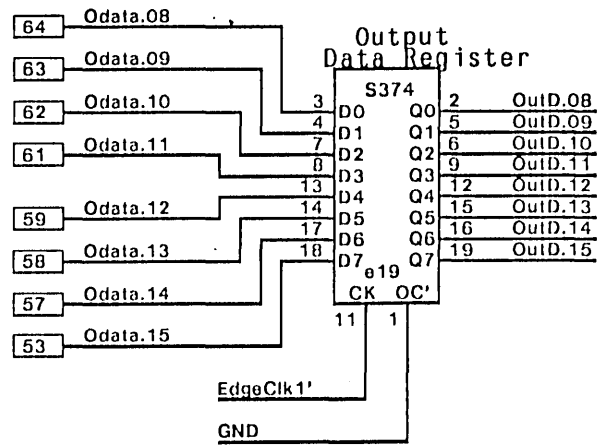
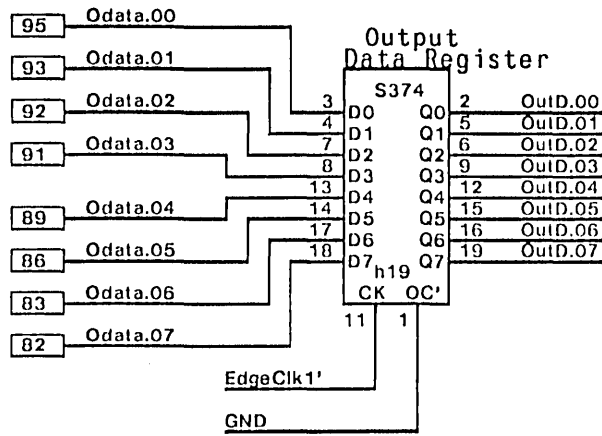
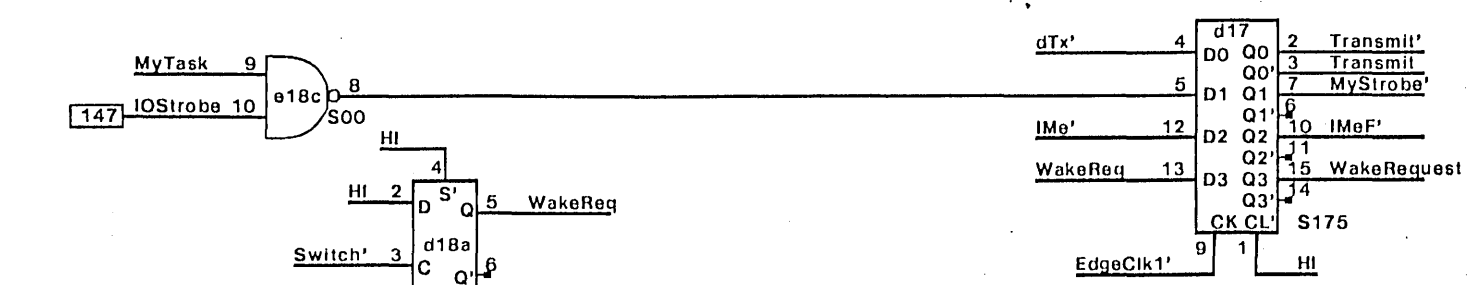
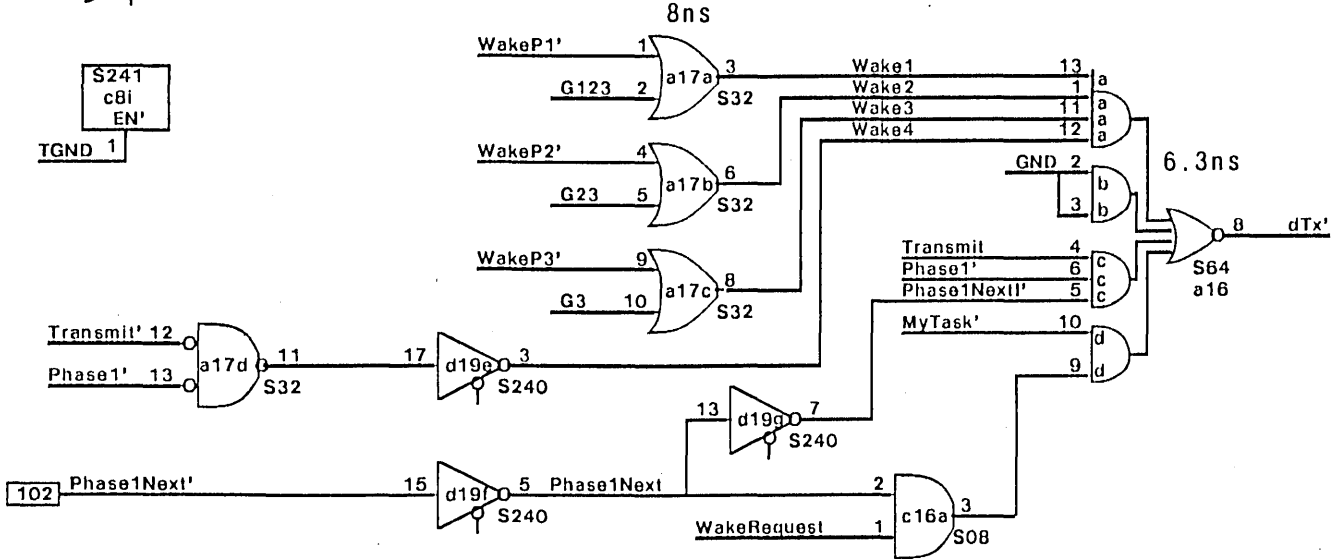
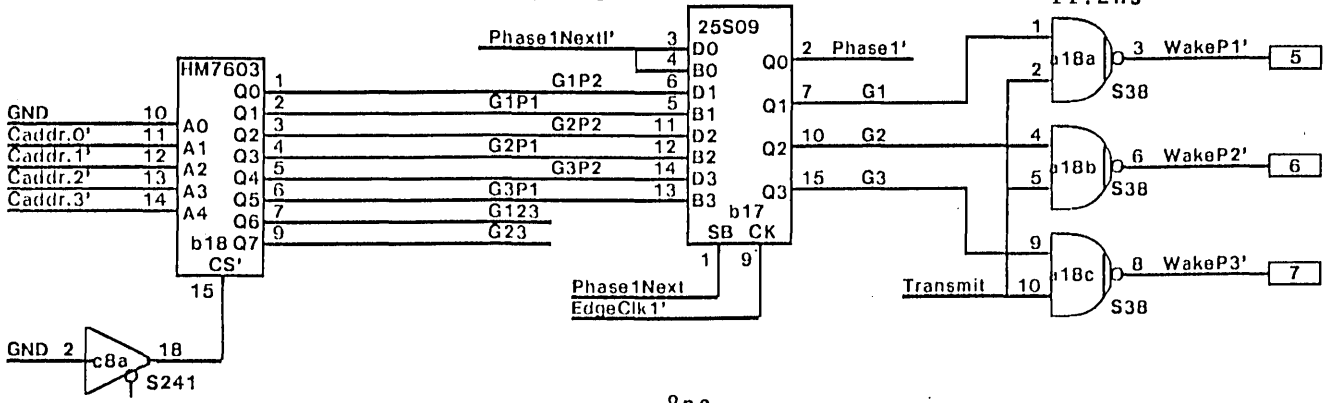


Controller Addressing

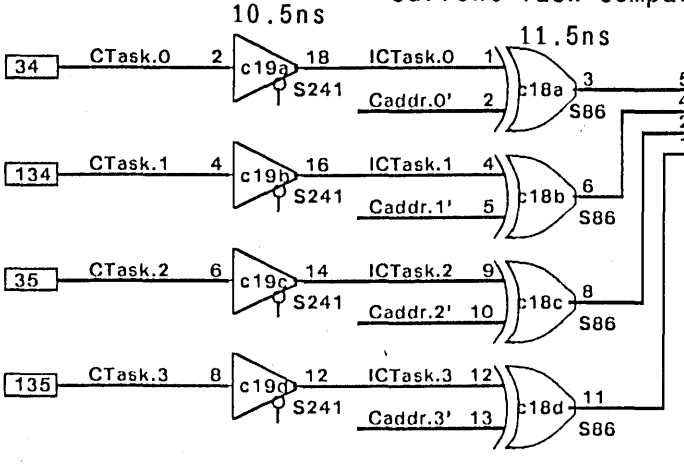




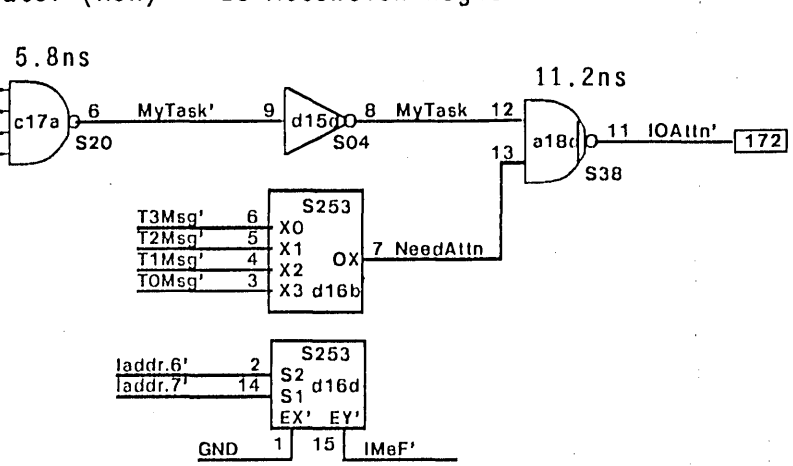
WakeUp Priority Encoding Logic19ns



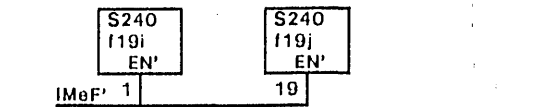
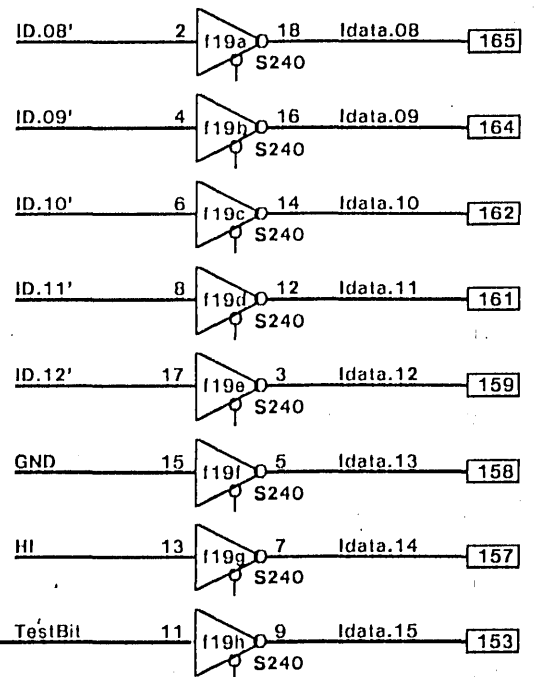
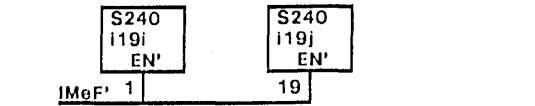
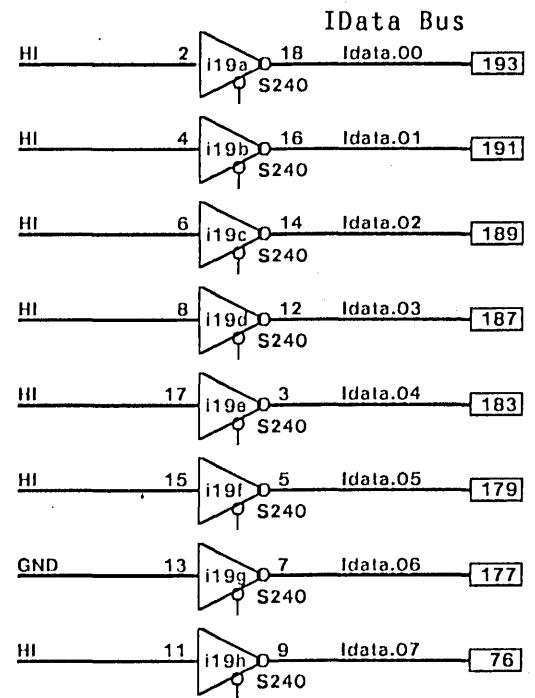
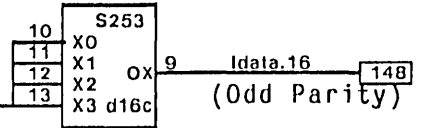
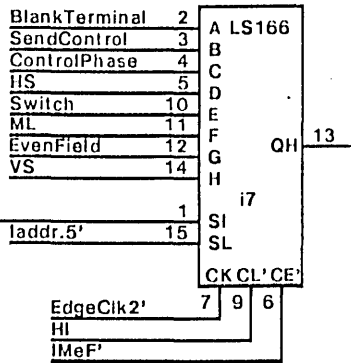
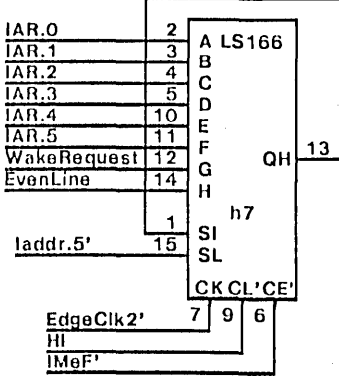
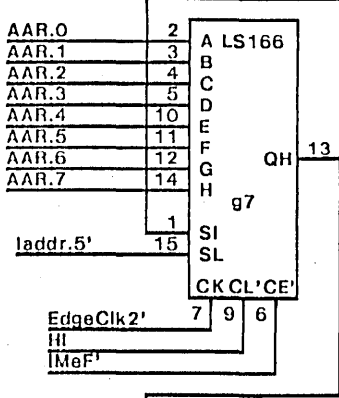
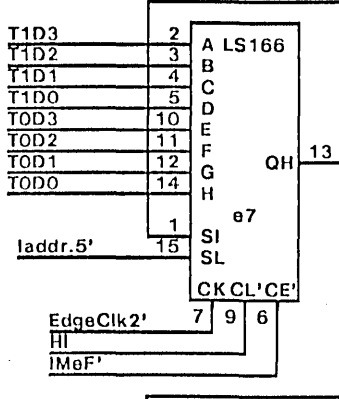
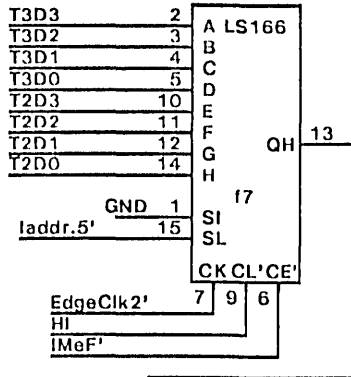
Current Task Comparator (XOR)



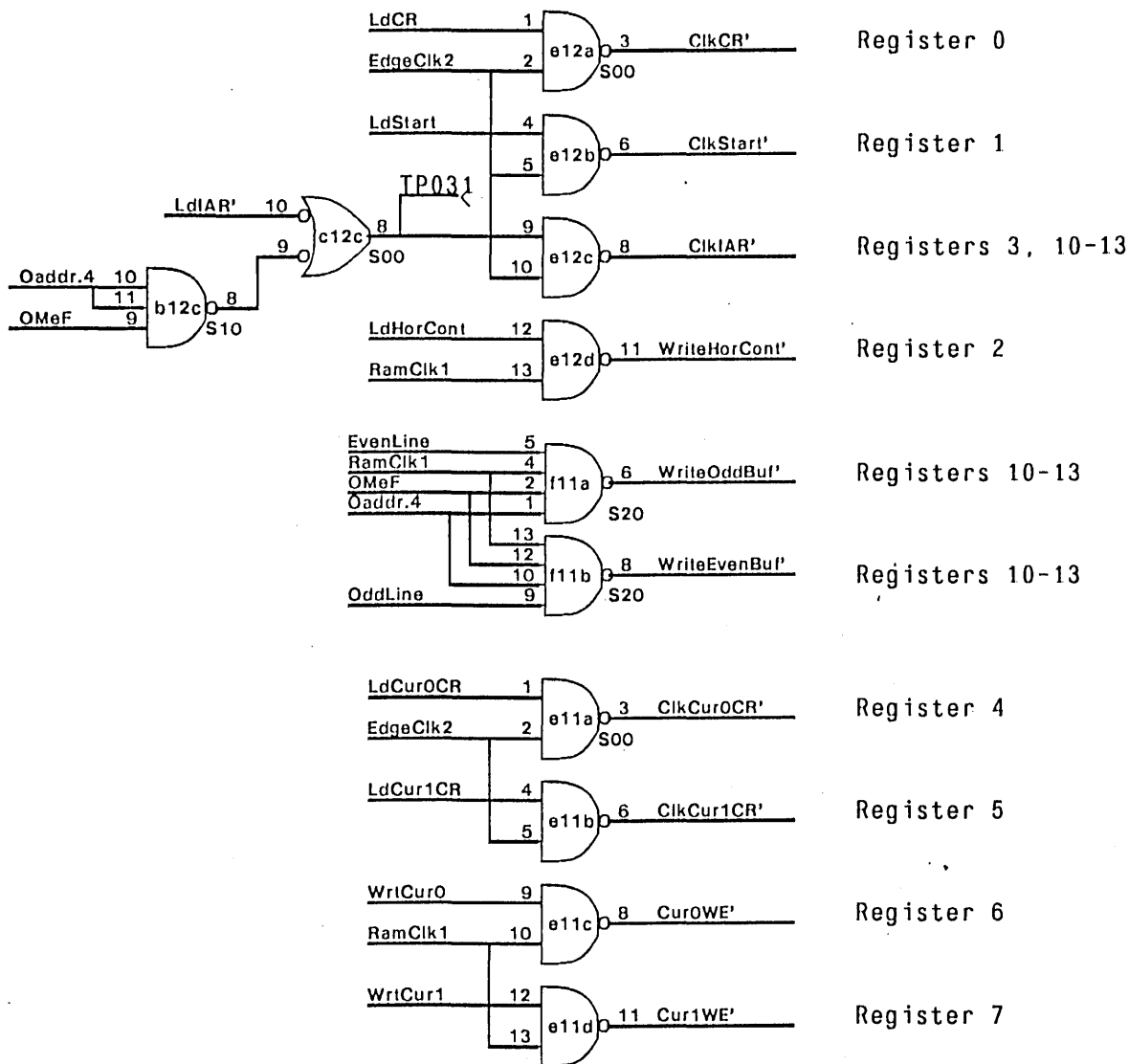
IO Attention Logic



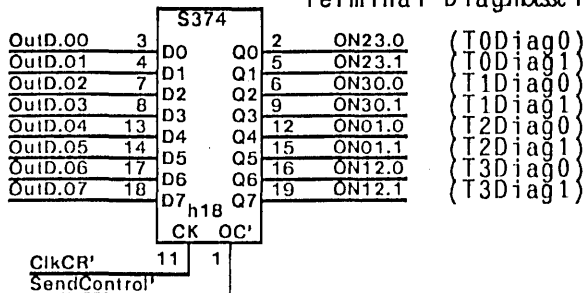
Test Shift Reg.
(40-bit)



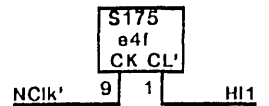
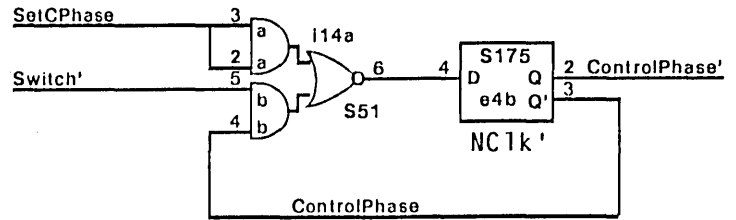
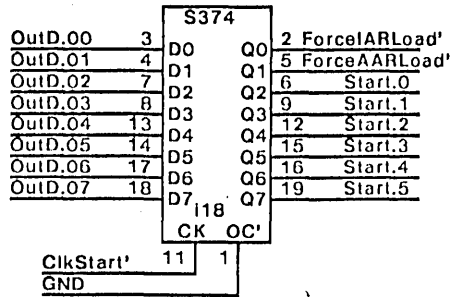
Note: Load: if Input Reg. with address > 4
 Shift: if Input Reg. with address < 4



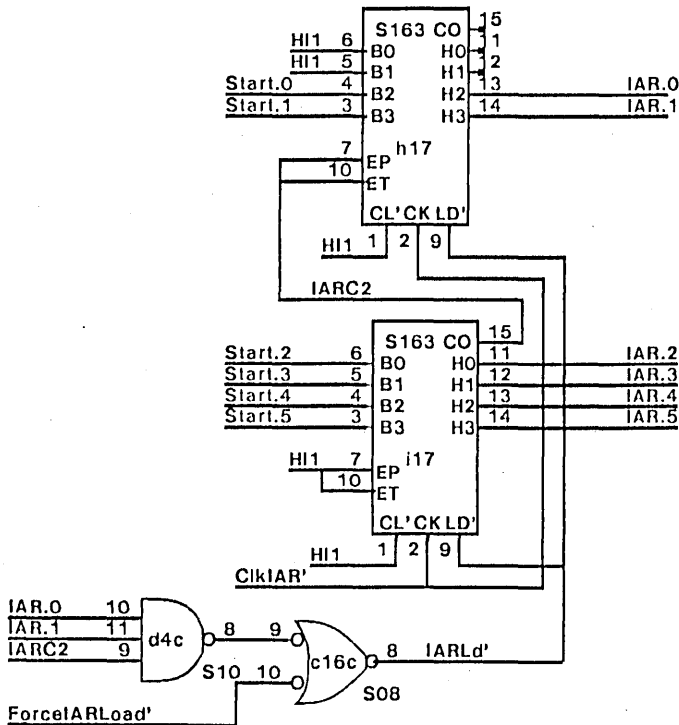
Diagnostic Reg.
Tri-State
Terminal Diagnostic



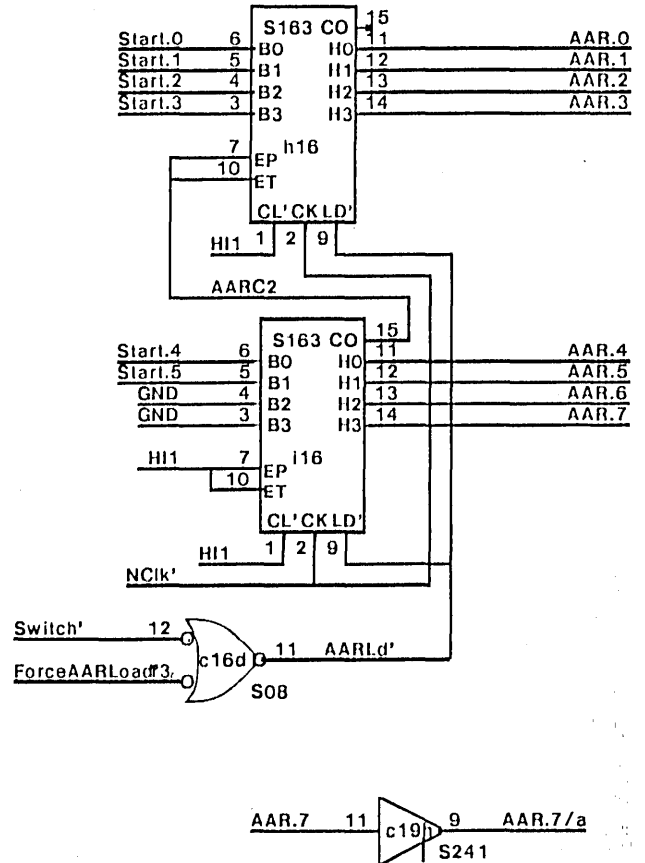
Starting Addr. Reg.



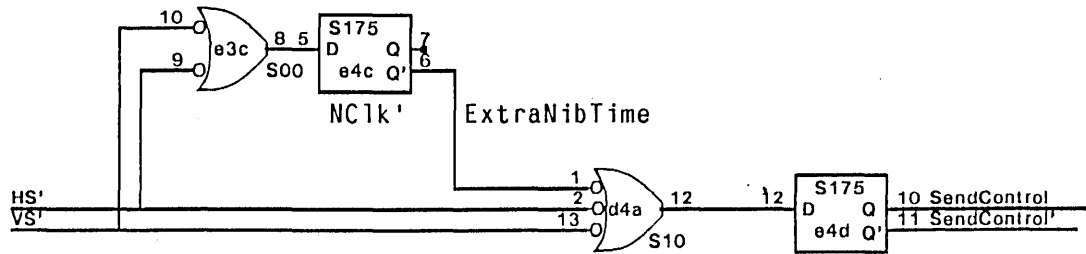
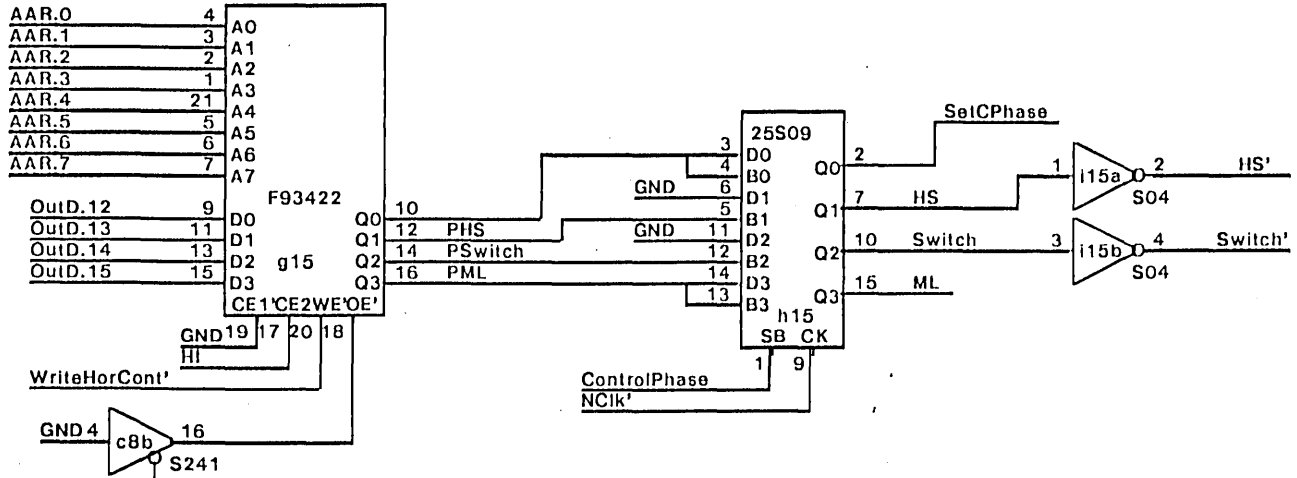
Inactive Addr. Reg.



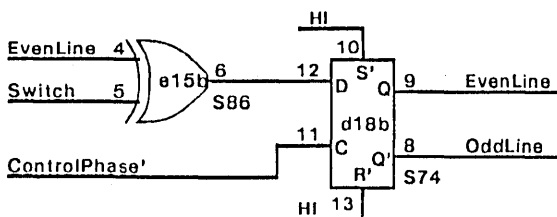
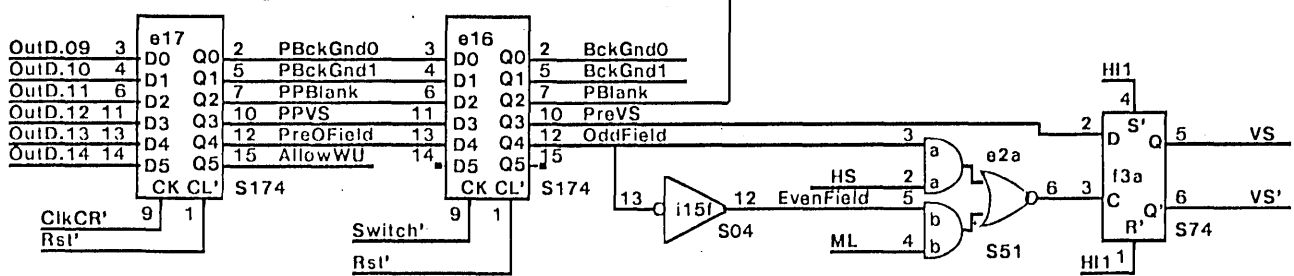
Active Addr. Reg.



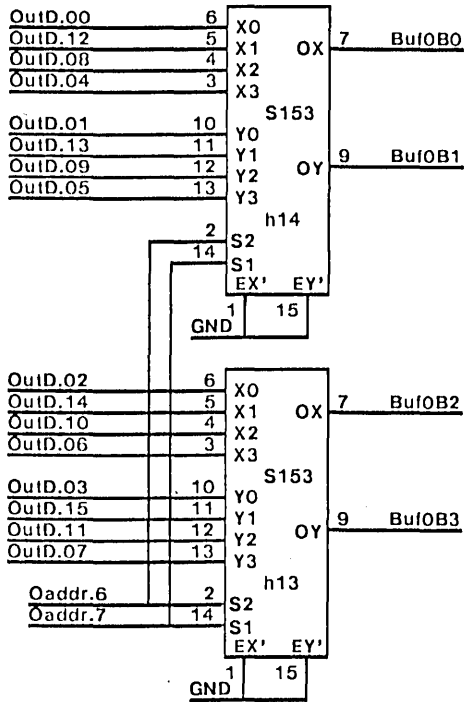
Hor. Control RAM



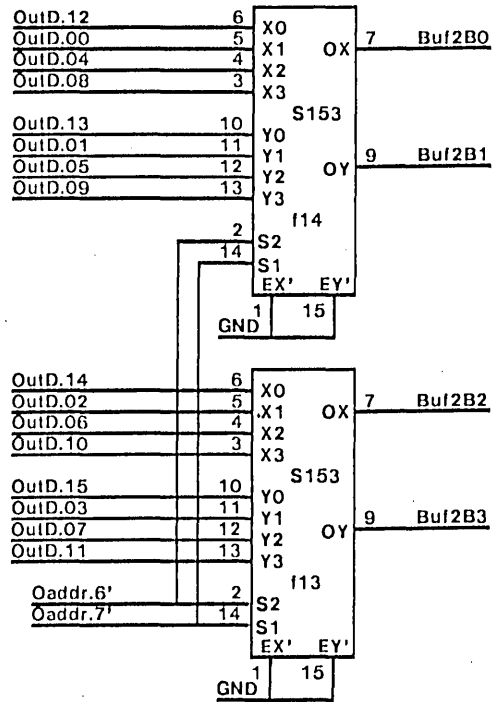
Control Register Synchronized CR



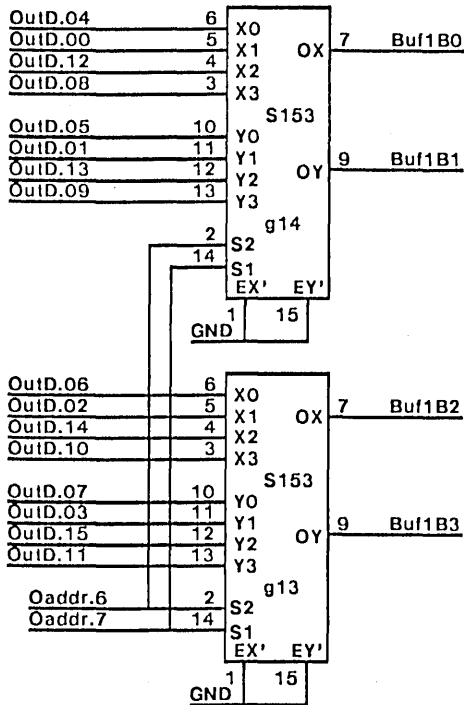
Input Shift Mux
for Buffer 0



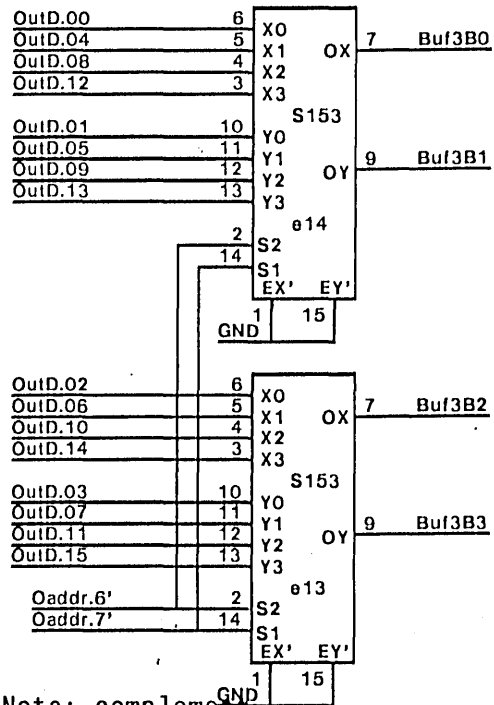
for Buffer 2



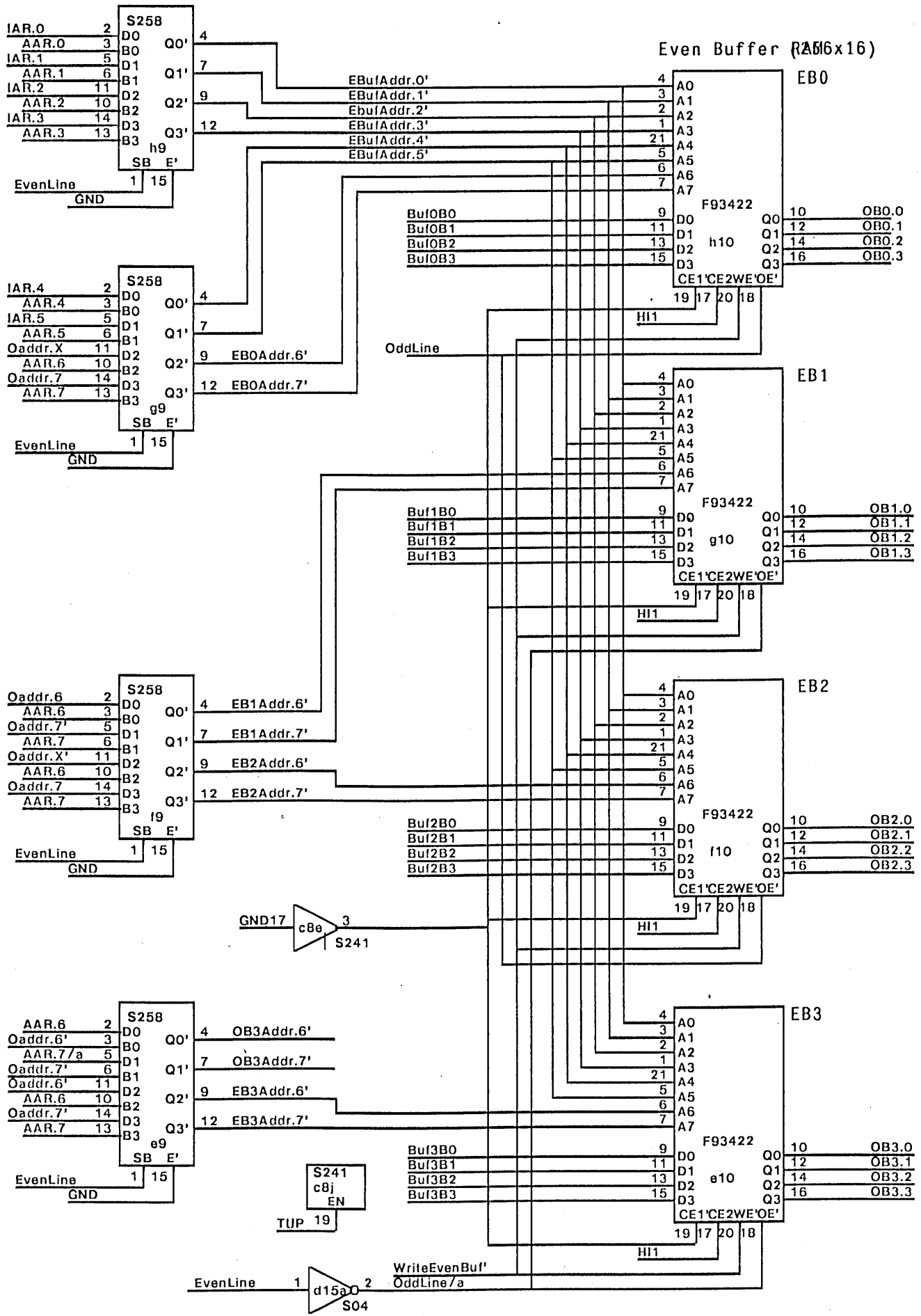
for Buffer 1

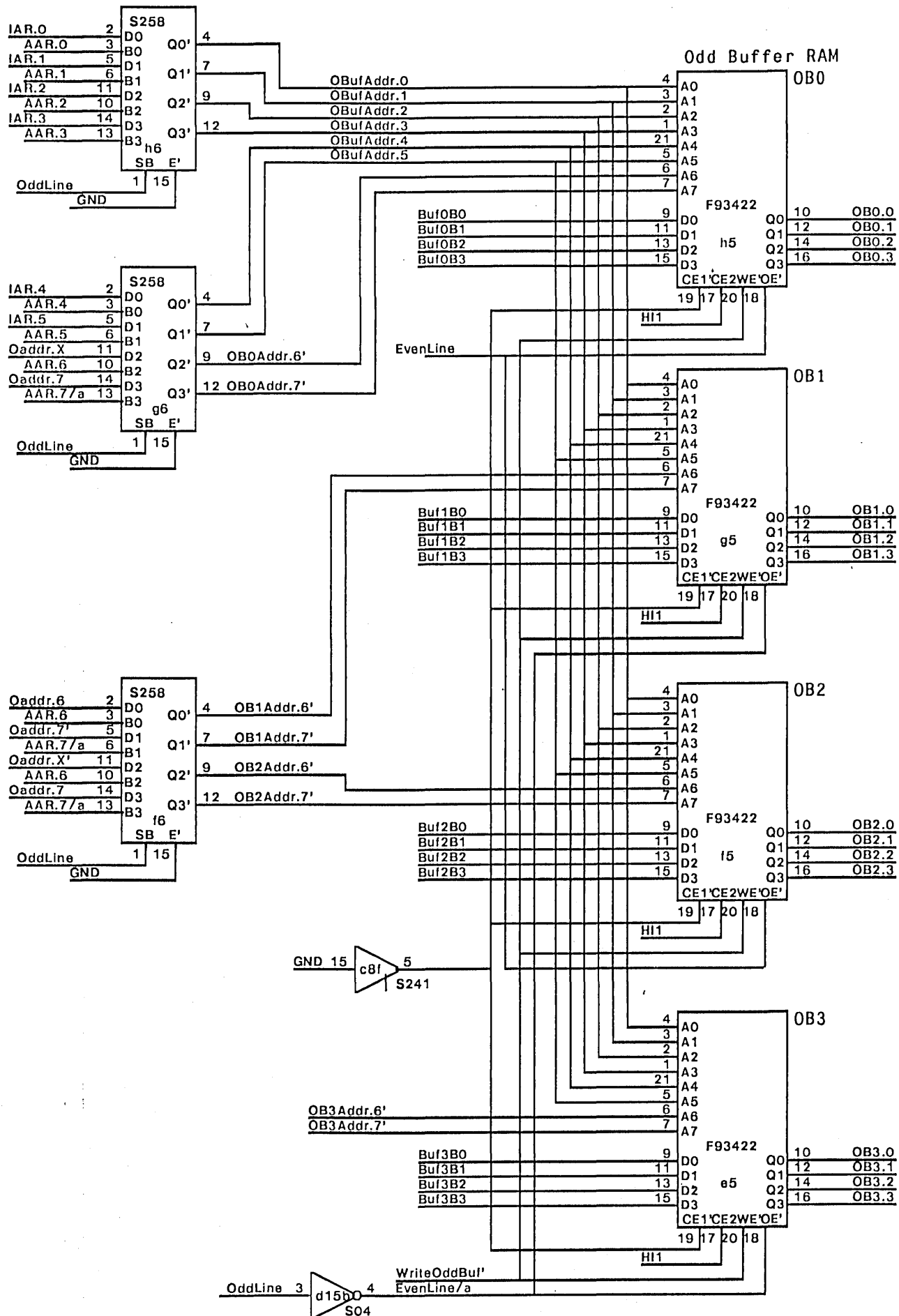


for Buffer 3

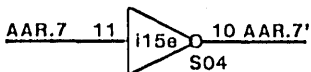
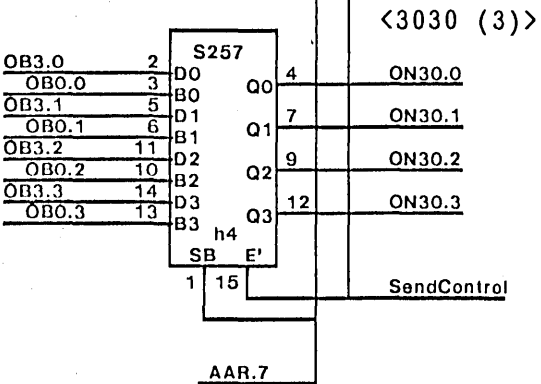
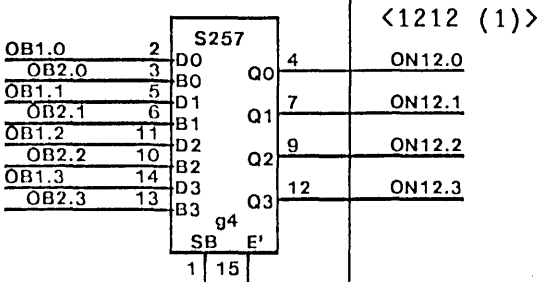
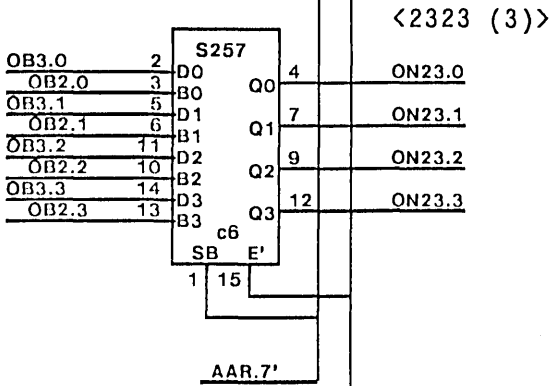
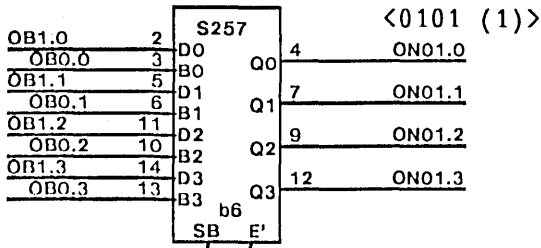


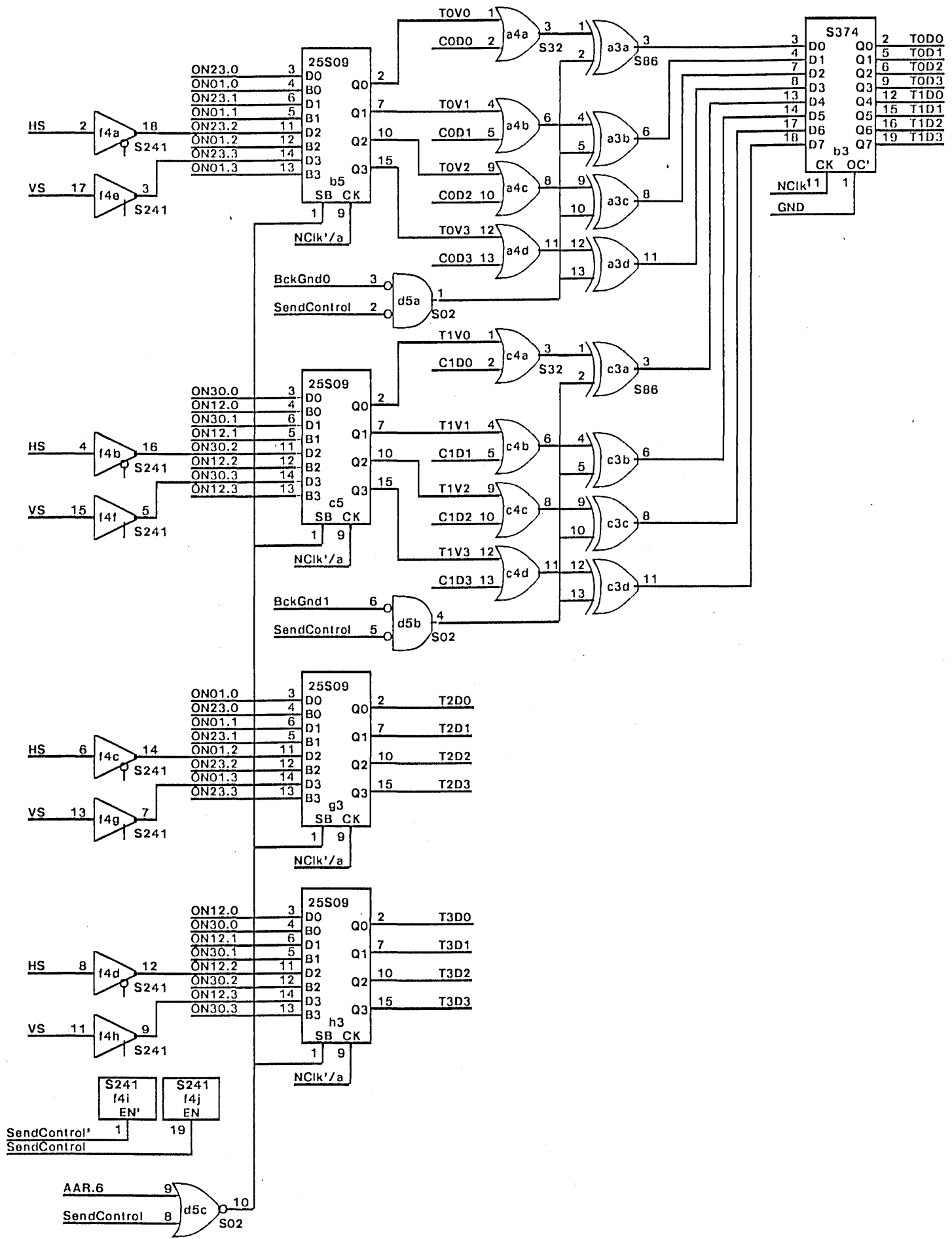
Note: complement
Oaddr.6,7 lines
used for better
load sharing

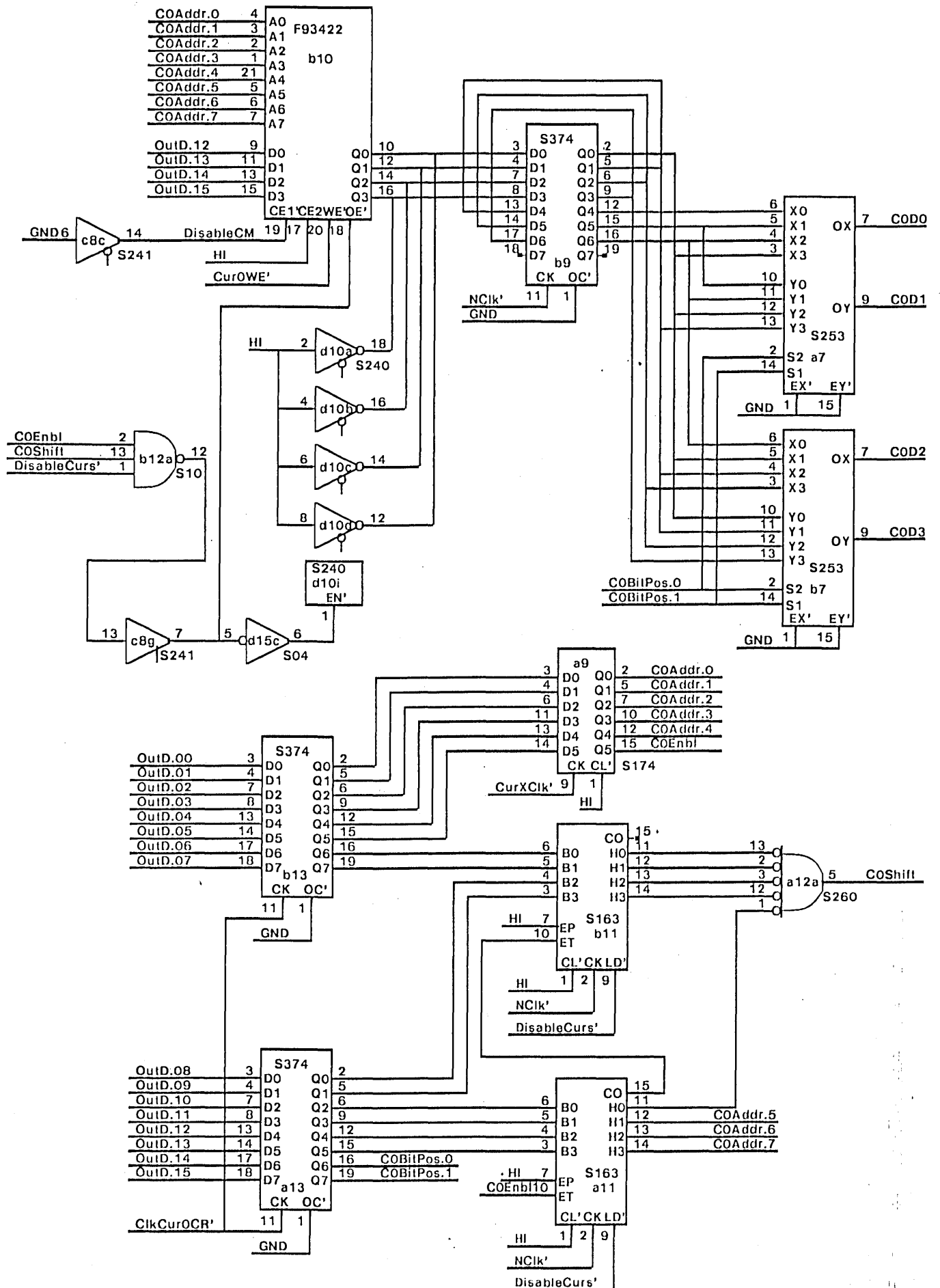


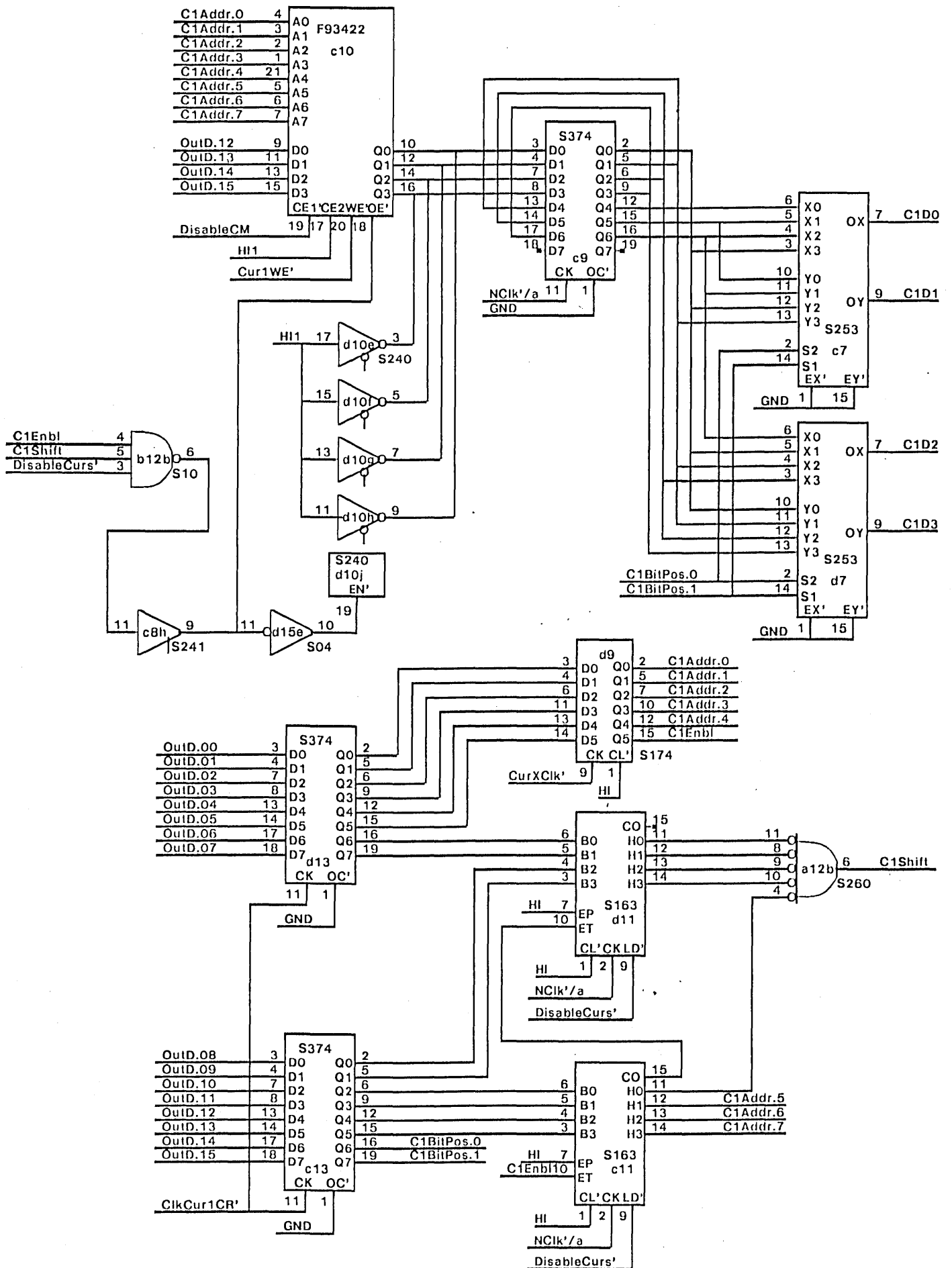


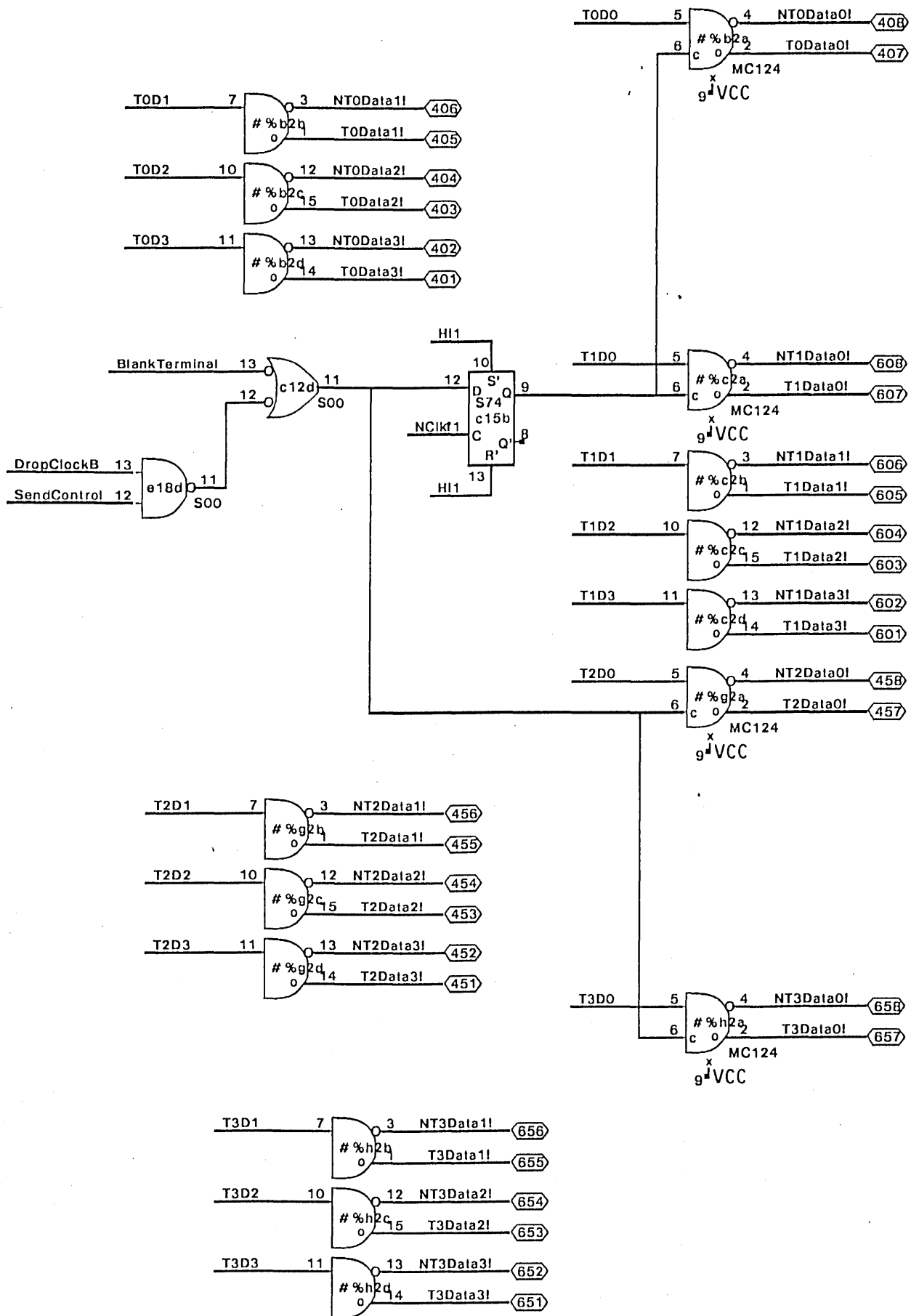
Tri-State



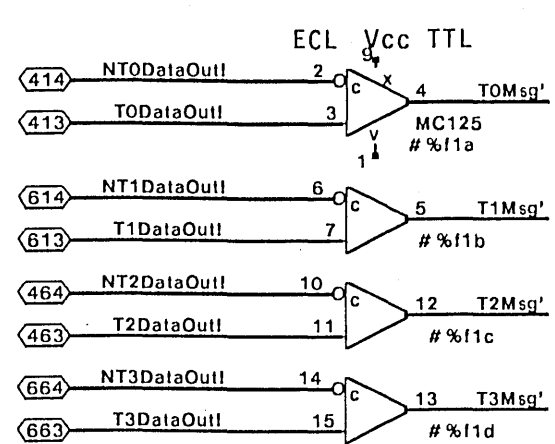
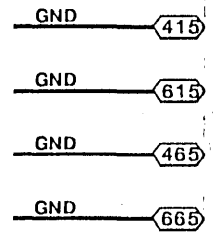
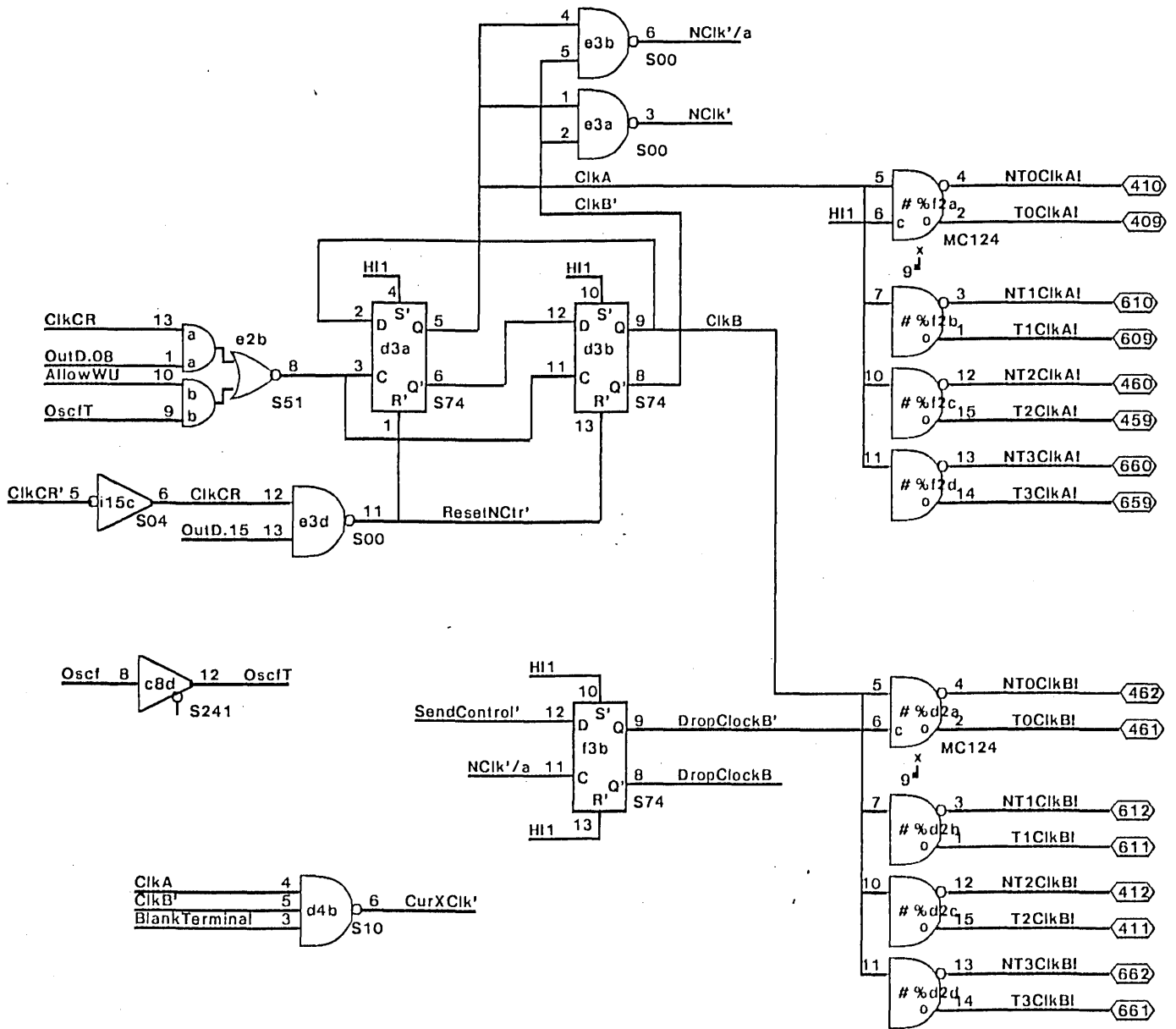




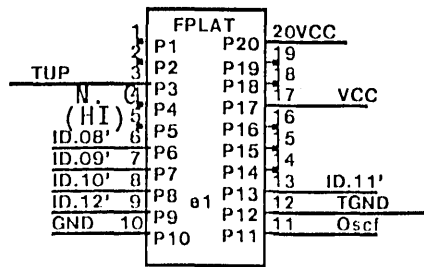




See page 17 for terminators



Oscillator & ID



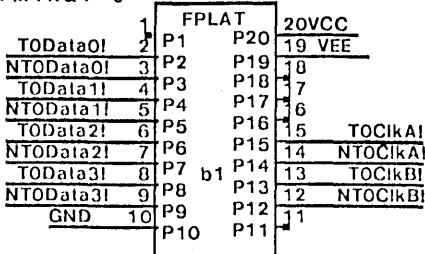
Note: 14-Pin crystal should be install in this 20-pin platform as follows

Crystal	PLAT
Pin 1: N. C.	P4
7: GND	P10
8: Output	P11
14: +V dc	P17

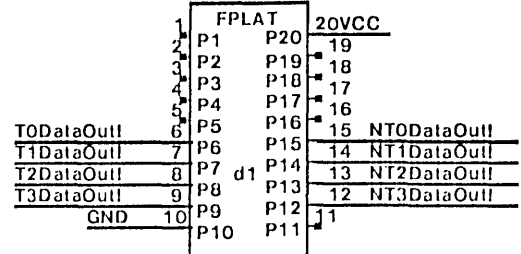
ID Modifier must have even number of p

Note: These platforms are shown as 20 pin units. They are actually 16 pin r with pin 8 of the network inserted into pin 9 of the 20-pin pattern. They are shown as 20 pins so that ROUTE will not try to cut any traces on the

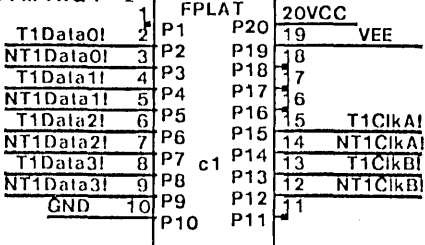
Terminal 0 220 ohm



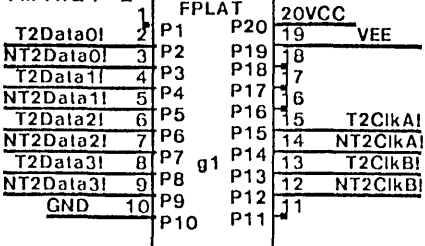
100 ohm



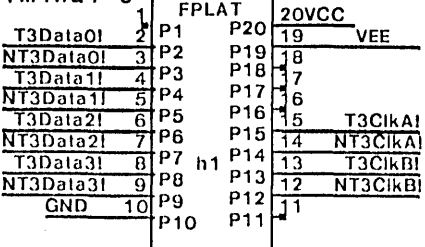
Terminal 1 220 ohm



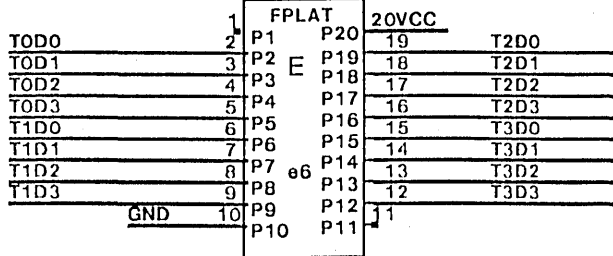
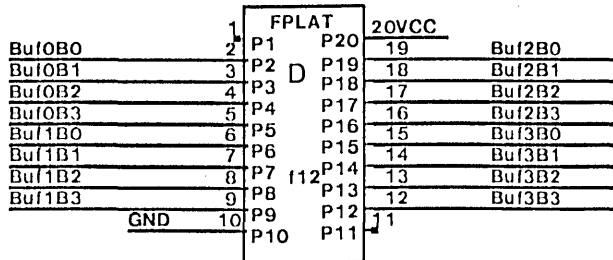
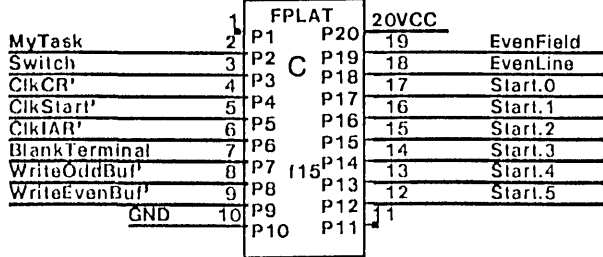
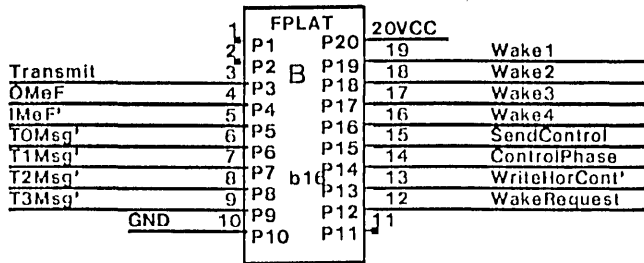
Terminal 2 220 ohm



Terminal 3 220 ohm

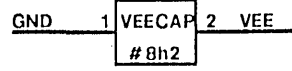
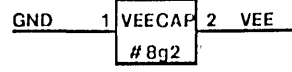
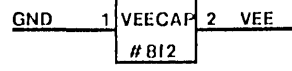
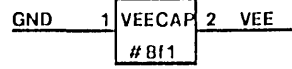
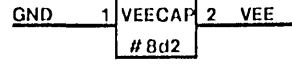
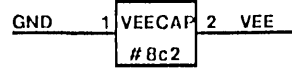
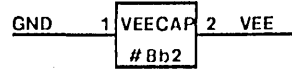


Test Clips:

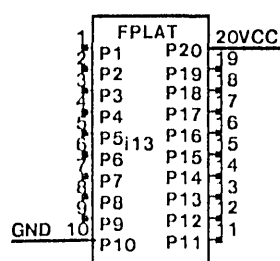
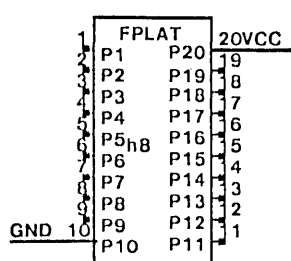
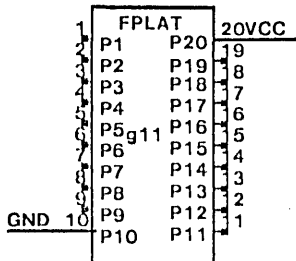
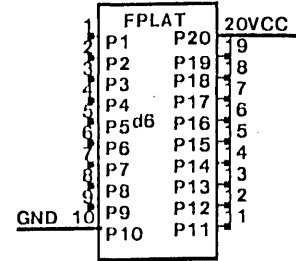
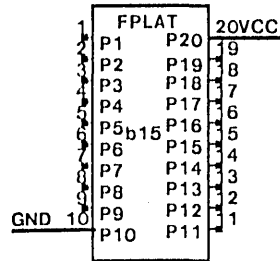
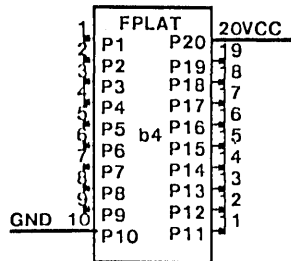
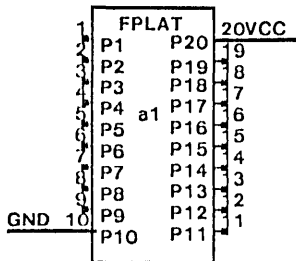


Filter Caps for ECL chips:

These capacitors mount between pins 2 and 19 of a 20 pin pattern due to the offset pr



Spare Positions (for Multiwire):



Rev C: Minor changes to logic found necessary during checkout.
Re-layout to eliminate crossover of connections to I/O connectors.
Made all I/O connectors male.
Added hardware cursor to channels 1 & 2.
All logic pages changed and renumbered.

Rev D: Synchronized BckGnd0 and BckGnd1 with Switch. Log. Dwg. p. 7.
Added SendControl to Background control to maintain proper polarity of Control signals. Log. Dwg. p. 12.
Changed control gate for Output shift register from S10 to S02. Log. Dwg. p. 6, 12, & 16.
Changed Blank function in Control register to Unblank so that Rst' results in blanked display. Log. Dwg. p. 7.

Rev E: Page 05; OAddr4' Input changed to OAddr4.OMeF and S10 gate (b12c) utilized for that .
Page 07; Control Register, PPUnblank changed to PPBlank, EnOsc changed to Allow WU, S74 (c15a) deleted
Sync CR - PUnblank changed to PBlank
S00 (e18d) changed to S02 (d5d). ControlPhase' input changed to ControlPhase.
Inverter (i15f) used instead of S02 (d5d). New wire EnblCurs' added.
Page 13; SendControl' changed to EnblCurs' on the input of S10 (b12a) and load inputs of S163 (b11 and a11). Typo corrected - Output control inputs on b13 and a13 changed from Hi to GND
Page 14; SendControl' changed to EnblCurs' on the input of S10 (b12b) and load inputs of S163 (d11 and c11). Typo corrected - Output control inputs on d13 and c13 changed from Hi to GND
Page 15; SendControl' input on S00 (c12) changed to DropClockB.SendControl, and S00 gate added (e18d)
Page 16; NClk gate input changed from ClkB to ClkB'. EnOsc input on S51 changed to Allow WU
DropClockB' signal added on the output of S74 (f3b). S10 gate (d4b) added to produce CurXClk'. Corrected typo - OutD.09 changed to OutD.15 on the input os S51
Page 17; Pullup and pulldown resistors added to the Crystal Plat (also in UTVFCSplats.sil)
Added test chip S241 in loc.cb. Its symbols are scattered on several pages. Added test points on most pages.

Rev F: Corrected error made in adding the test points on page 9 and 10. Changed EdgeClock2' to EdgeClock1' (Etch layout-related) on p.2. Changed S166 to LS166 on page 4. Cosmetics on p.17.

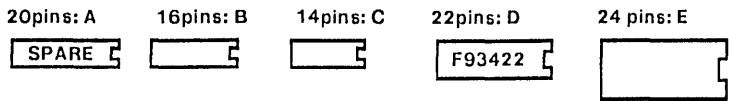
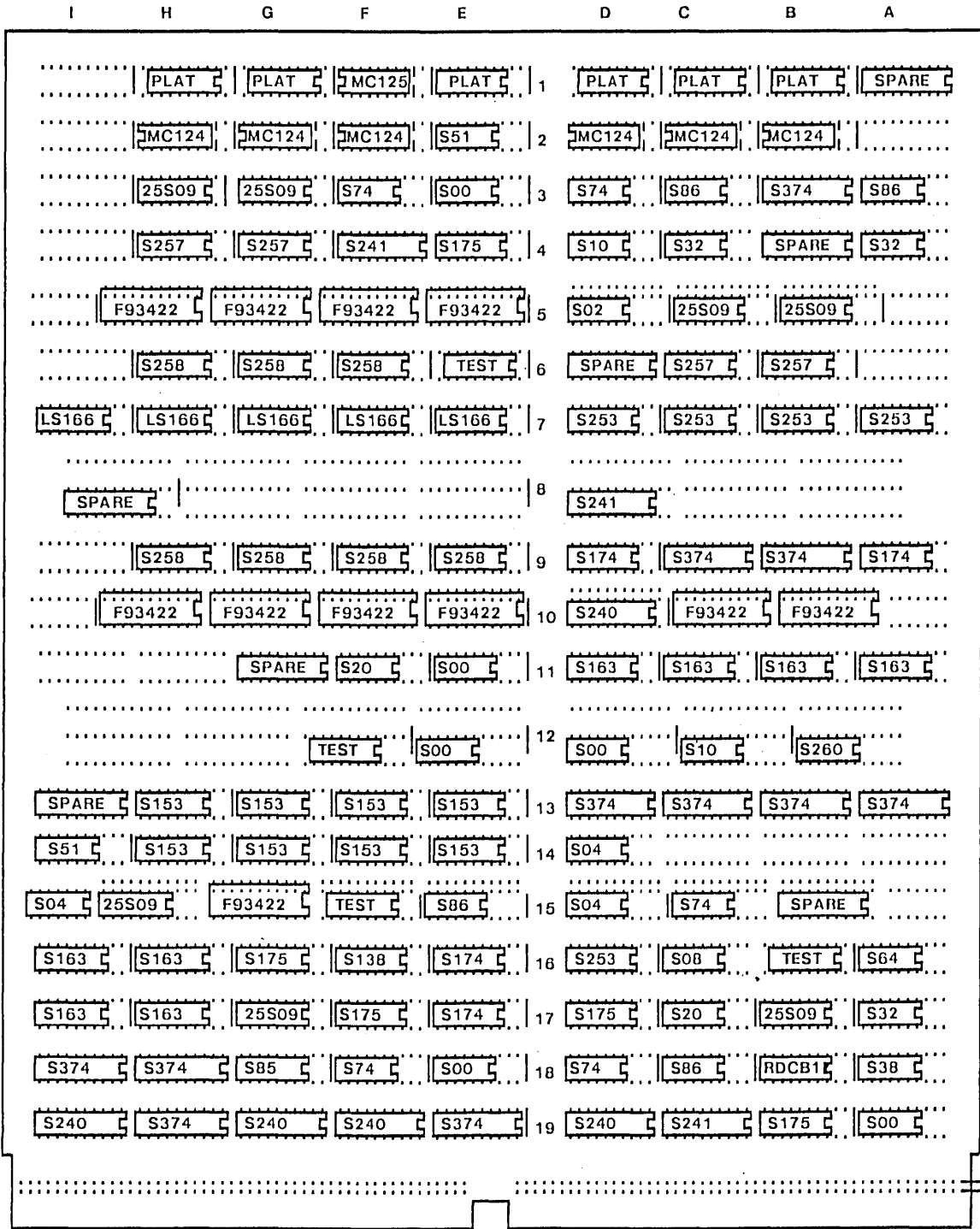
Rev G_a created from Rev F by CPT on 3/25/79:

Renamed EnableCurs' to be DisableCurs'
Removed Test points from diagrams.
Reversed ECL chips so that pin 16 (gnd) will be trace-wired.
Made all platforms 20pins so that ROUTE will not do any cuts.
Added spare 20pin positions (for Multiwire) in a1, b4, b15, d6, g11, h8, and i13.

Changes for revision G_b (7/18/80 - CPT)

- 1) Connected pin 15 of all 4 terminal connectors to ground (p 16).
- 2) Created latched signal MyStrobe' (pg. 3).

Note: The I/O connector area is loaded with 4 15pin MALE D-series connectors.
 Note: All platforms except a1 have pin 8 of the platform in pin 9 of the pattern.
 Note REVERSAL of all ECL Chips (MC124, MC125)

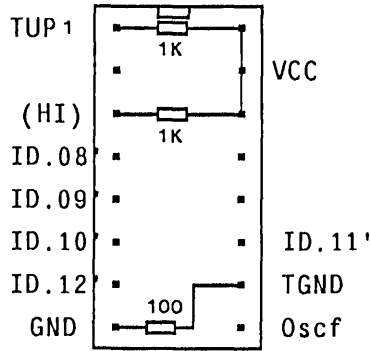


16 pins REVERSED: F
 Typical of ECL chips

Note: The short vertical lines indicate filter capacitor locations.
 (103 Total)

Broken vertical lines indicate VEE filter caps for ECL chips. These are mounted from pin 2 o pin 19 of the 20 pin pattern.
 (7 total)

Platform e1 (oscillator):



Note: The oscillator is mounted on the platform as follows:

Oscillator Pin number	Platform Pin number
1	2
7	8
8	9
14	15

Oscillator is Motorola K1100A series

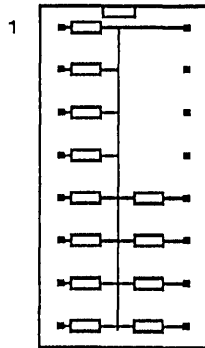
Note: ID.08' - ID.12' are wired to HI (pin 3) or Gnd (pin 8) depending on the oscillator frequency as follows:

Oscillator f:	50mhz	20mhz					
ID.08' (pin 4)	Hi	Hi					
ID.09' (pin 5)	Hi	Hi					
ID.10' (pin 6)	Hi	Gnd					
ID.11' (pin 11)	Gnd	Hi					
ID.12' (pin 7)	Gnd	Gnd					

Platforms b1, c1, g1, h1

Xerox P/N 703W11691 (15 resistors) is acceptable

All resistors 220 ohm, 1/4 w.



Platform d1:

Xerox P/N 703W00891 (8 resistors) is acceptable substitute

All resistors 100ohm 1/4 or 1/8 watt, 10%

