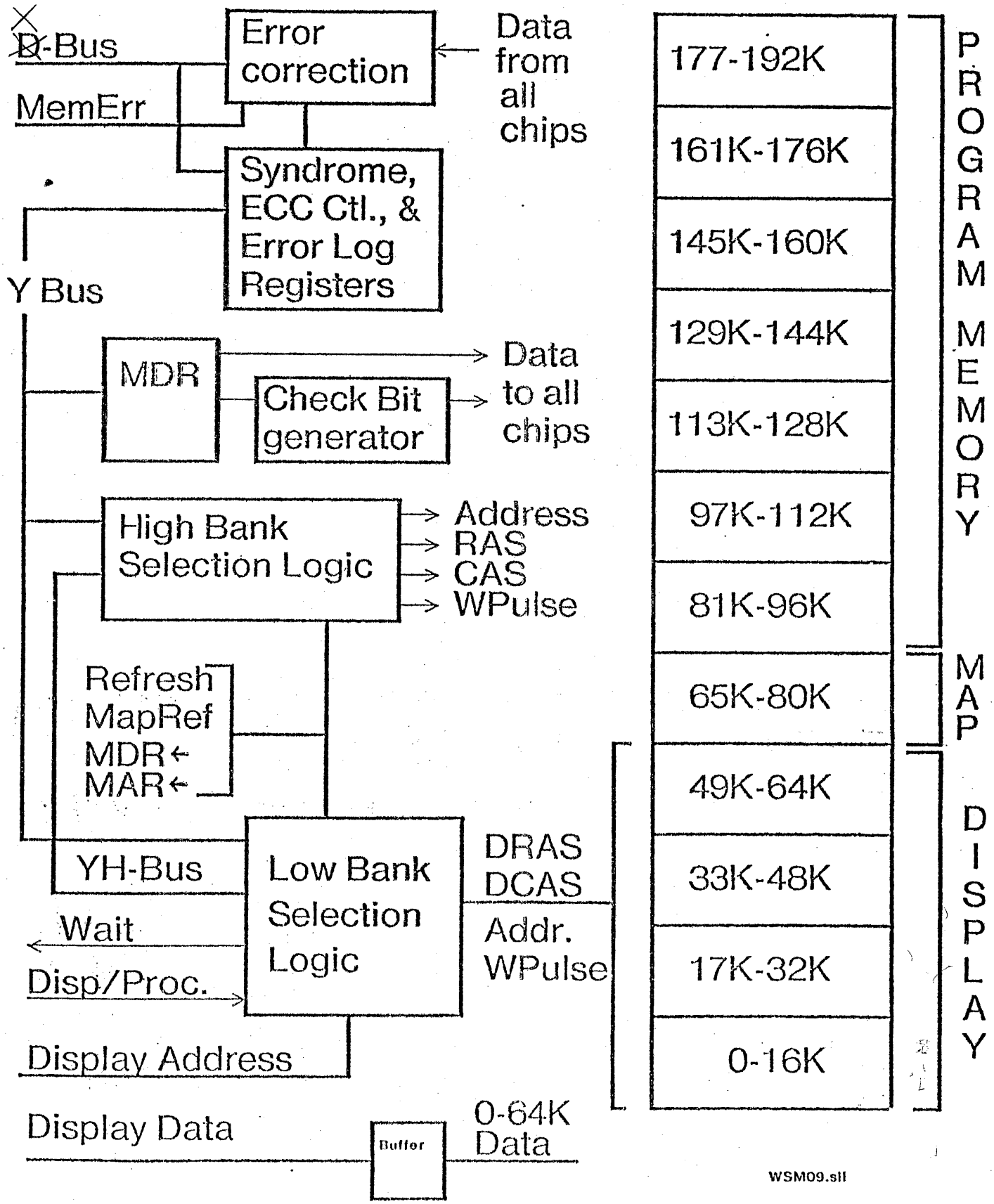
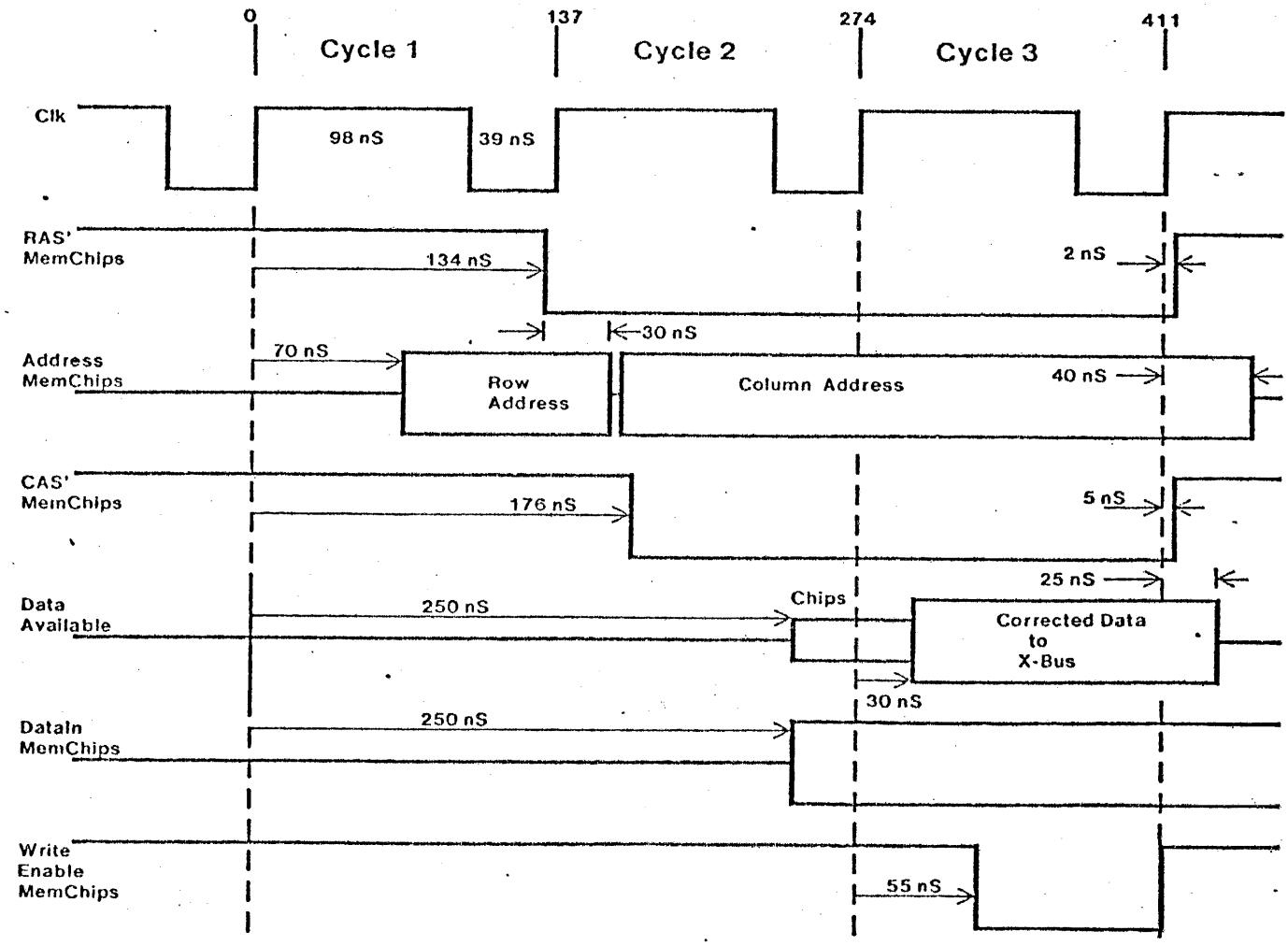
Inside the Memory System





Normal Memory References through Processor Port

XEROX
BUSINESS SYSTEMS
Systems Development Department

To: Distribution

Date: October 8, 1979

From: Ron Crane

Org: SDD/SDT

Subject: **Dandelion Memory System**

Filed: [IRIS]<Workstation>MCTL>MCTLmemo.press

Dist.:WS Design group

This memo covers several aspects of the memory system for the Dandelion processor. The memory system reads and writes 16 bit words for both the processor and the display. The low bank is shared between the two. Error correction is performed on all words delivered to the processor. The memory cycle time is 411 nanoseconds (nS). The low 64K words are located on the memory control card, with up to 128K words located on the storage card. If 64K memory chips are used instead of 16K chips, these numbers can be multiplied by 4.

Memory Functions

This section provides a description of each of the functions of the memory system as viewed from the processor. Both a system level diagram and a detail block diagram of the memory system are on the following page.

Read

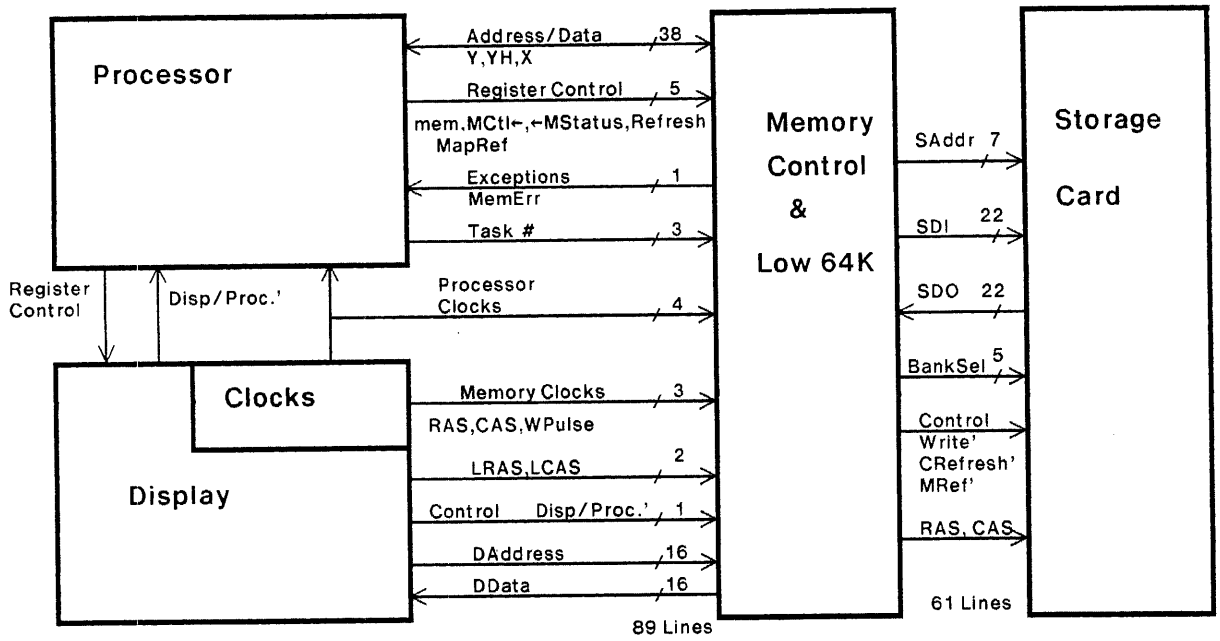
A read operation is started by placing the memory address on the Y bus and asserting 'mem' in the first cycle of a click. Bank selection is done by the 2 low order bits present on the YH bus and Y0,1 , while the word selection within the chip is done by the low 14 bits on the Y bus. The data can be read back to the X bus at the end of the third cycle by asserting 'mem' during the third cycle of a click. The address must meet a bit dependent setup time, because the RAS signal actually latches the most significant 7 bits of the address in a bank during the first cycle of a click. All data read back is error corrected unless the correction inhibit bit is set in the MCtl register.

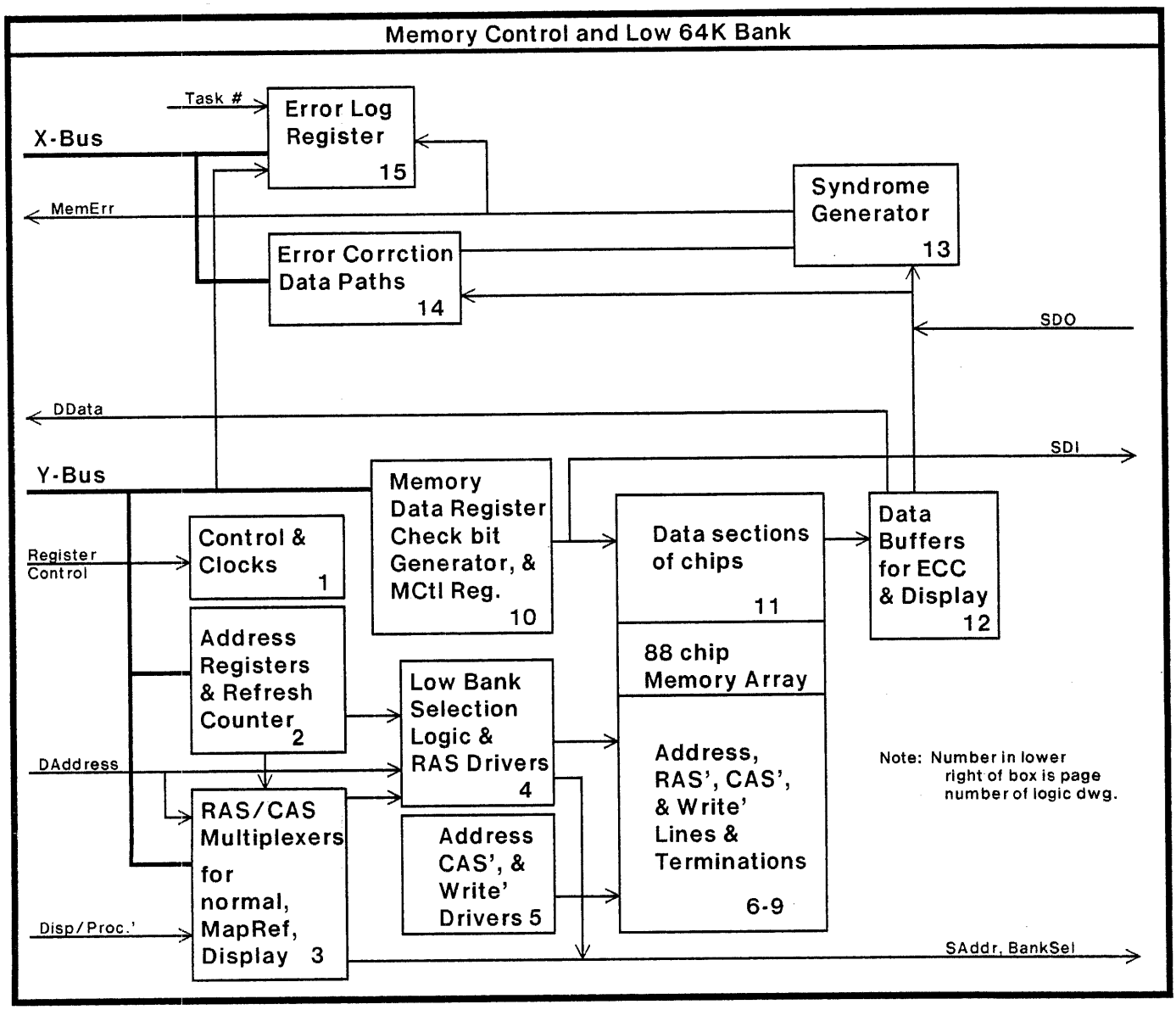
Write

A write operation starts just like a read operation with the address sent out in the first cycle of a click. The data to be stored must be delivered to the memory during the second cycle of a click, by asserting 'mem' in the second cycle, and placing the data on the Y bus. Error correction check bits are always calculated and stored automatically by the memory system.

Map Reference

A map reference memory read is just like a regular read, except that the 22 bits supplied by the Y and YH busses are shifted around to facilitate indexing into a page map, which in combination with microcode, provides a 22 bit virtual memory system. The low 8 bits supplied are discarded (since they are the word location on the page), and the high 14 bits (virtual page number) are moved to the low 14 bits used for the address into real memory. The high 4 bits are 0100, thus fixing the location of the 16K map between 65K and 80K in real memory. In microcode, MapRef should only be selected during cycle 1, and never during cycles 2 or 3, since nothing will happen. A diagram of this is included in the logic drawings.


Processor
Address/Data 38
Y,YH,X
Register Control 5
mem.MCtl←,←MStatus,Refresh
MapRef
Exceptions 1
MemErr
Task # 3
Register Control
Disp/Proc.'
Processor Clocks 4
Clocks
Display
Memory Clocks 3
RAS,CAS,WPulse
LRAS,LCAS 2
Control Disp/Proc.' 1
DAddress 16
DData 16
89 Lines
Memory Control & Low 64K
SAddr 7
SDI 22
SDO 22
BankSel 5
Control
Write'
CRefresh'
MRef'
RAS, CAS
61 Lines
Storage Card


Memory Control and Low 64K Bank
Task #
X-Bus
Error Log Register 15
MemErr
Syndrome Generator 13
Error Corrction Data Paths 14
SDO
DData
SDI
Y-Bus
Memory Data Register Check bit Generator, & MCtl Reg. 10
Data sections of chips 11
Data Buffers for ECC & Display 12
Register Control
Control & Clocks 1
Address Registers & Refresh Counter 2
Low Bank Selection Logic & RAS Drivers 4
88 chip Memory Array
Address, RAS', CAS', & Write' Lines & Terminations 6-9
DAddress
RAS/CAS Multiplexers for normal, MapRef, Display 3
Address CAS', & Write' Drivers 5
Disp/Proc.'
SAddr, BankSel
Note: Number in lower right of box is page number of logic dwg.

Refresh

The memory controller contains circuitry to facilitate memory refresh. In particular, the counter is included on the board and all banks of memory are refreshed at the same time. The CAS (column address strobe) signal is suppresed during refresh, thus minimizing the current used in refresh. Refresh is initiated by asserting the refresh control signal from the processor during cycle 1 of a click. Refresh should not be asserted during cycle 2 or 3 of a click or when the display is using the low bank, since nothing will happen in these cases. While the 16K chips require only 128 refresh cycles every 2 mS, it is recommended that microcode implement 256 refresh cycles every 2 mS until it is clear that 64K memory chips can be delivered with 256 cycles every 4 mS.

Display Lockout

The low 64K of the memory is shared between the display and the processor. The display has priority. System timing is cyclic, with 5 clicks per round. When actually scanning a line, the display consumes clicks 1 through 4, leaving click 5 for the processor. Thus, only one click out of 5 is available for use by memory refresh, display handling, and cursor microcode. About half the bandwidth remains in the 5th click for emulator use after memory refresh, display, and cursor tasks have been subtracted.

Lockout occurs only if the display is outputting a line from memory and access to the low bank is attempted. Accesses to the high bank(s) are not affected. Lockout does not occur during retrace intervals (horizontal and vertical), or during any other period of display inactivity (such as partially or completely shutting off the display). By convention, time critical hardware tasks using the first 4 clicks must never attempt access to the low (display) memory bank since a lockout could occur causing extra delay. See the display controller description for exact details of display timing.

Lockout is implemented by generation of a wait signal in the processor whenever a bank 0 (low 64K bank) access is attempted and the display is already using the low bank. The processor suspends the microcode which started in that click, and continues as normal the arbitration of what runs in the next click. In this manner, lockout in one click does not hold up operation in the following click.

Error Correction

Since soft errors can occur in the memory (alpha particles from the package, etc.) error correction circuitry is included in the memory system. Six check bits added to the 16 bit word provide single error correction and double error detection (SEC-DED). No explicit indication of single errors is provided, although the status of any particular operation can be read from the Status & Errors register after an operation. Error correction can be disabled, and the check bit positions in memory selectively set by writing into the MCtl register and reading the MStatus register.

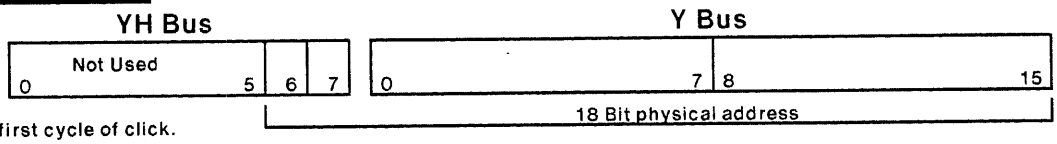
Double Error Logging

A double error signal is available and also latched on a per task basis in the MStatus register. Thus, a task, upon entering a critical data transfer phase, could clear its particular bit, perform the task, and then check to see if its bit was set (double eror). If an error did occur, its effect would be limited to events in that interval, over which some corrective action might be taken.

General Comments on Memory Programming

Details of memory programming are contained in the next figure, describing the memory registers. As mentioned earlier, neither MapRef nor refresh should be asserted in cycles other than cycle 1. In addition, refresh should not be asserted whenever the display is using the low bank.

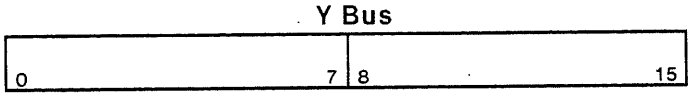
MAR← Memory Address Register



MAR← mem during first cycle of click.

Action: Contents of YH(6,7),,Y(0,15) is used as memory address. Access is started.

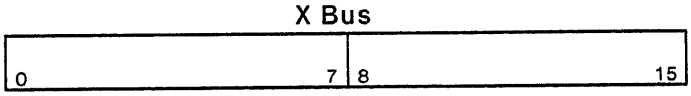
MDR← Memory Data Register



MDR← mem during second cycle of click.

Action: Contents of Y Bus go into memory location specified by contents of MAR as loaded during first cycle of click. No write occurs if the low 64K bank is selected and it is already being used by the display.

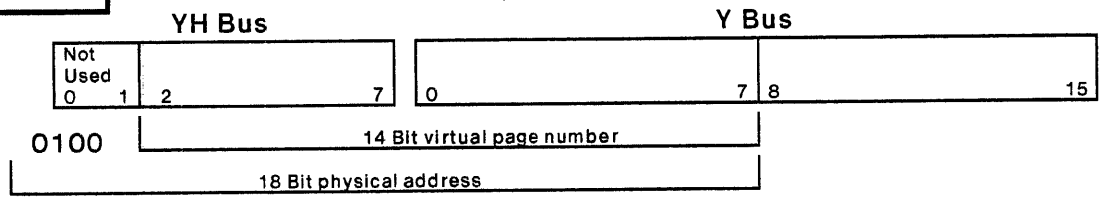
← MD Memory Data



←MD mem during third cycle of click.

Action: Memory data to X-Bus is single error corrected if MCtl bit 15 is set. The status of a given read operation can be found by looking in MStatus before the next memory read (←MD) is done. The occurance of both single and double errors are indicated here. This operation gives the contents of the memory cell specified during cycle 1, independent of whether a write was specified during cycle 2.

MapRef Map Reference



MapRef during cycle 1 of click. (not during cycle 2 or 3)

Acton: This action is the same as a MAR← except that the physical address is derived differently. An access is started in the 65K - 80K bank of memory. The location accessed is specified by the 14 bit page number.

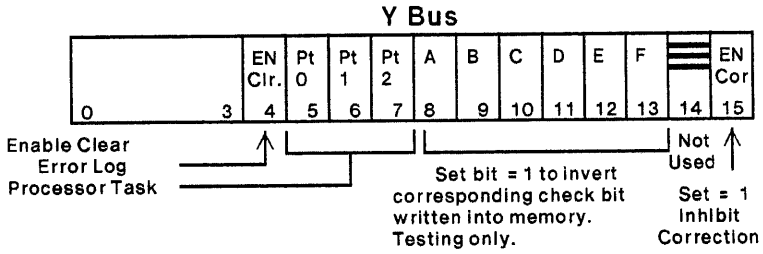
Refresh

Refresh during cycle 1 of click. (not during cycle 2, 3, or when display is using low 64K bank)

Action: A RAS only cycle is initiated in all memory chips. Row Address is supplied from an internal 7 bit counter which is incremented once per occurance of refresh.
DO NOT USE refresh if the display is using the low bank of memory during that cycle. No refresh will occur.

MCtl← Memory Control Register

MCtl← during any cycle.

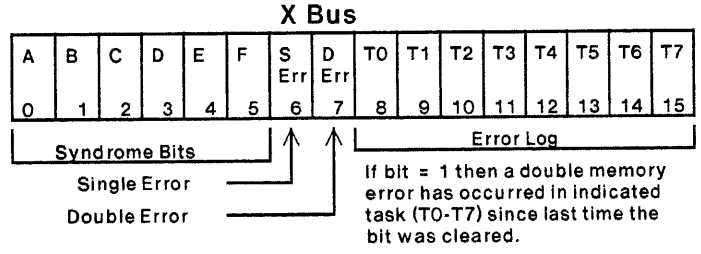


Action: Normally this register is set to 0. A-F can be set to one to test syndrome bits and error indications. Individual bits of the error log can be cleared by setting bit 4 and using Pt0-2 to specify the bit to be cleared. Bit 15, Inhibit correction, affects only the data being read. Check bits are always generated and stored in memory during writes.

← MStatus Memory Status

← MStatus during any cycle.

Action:
This register is loaded every time memory data is read by the processor (←MD). High byte has status of most recent memory access. Low byte latches any occurance of double error on a per task basis. Register is 0 if no errors logged.



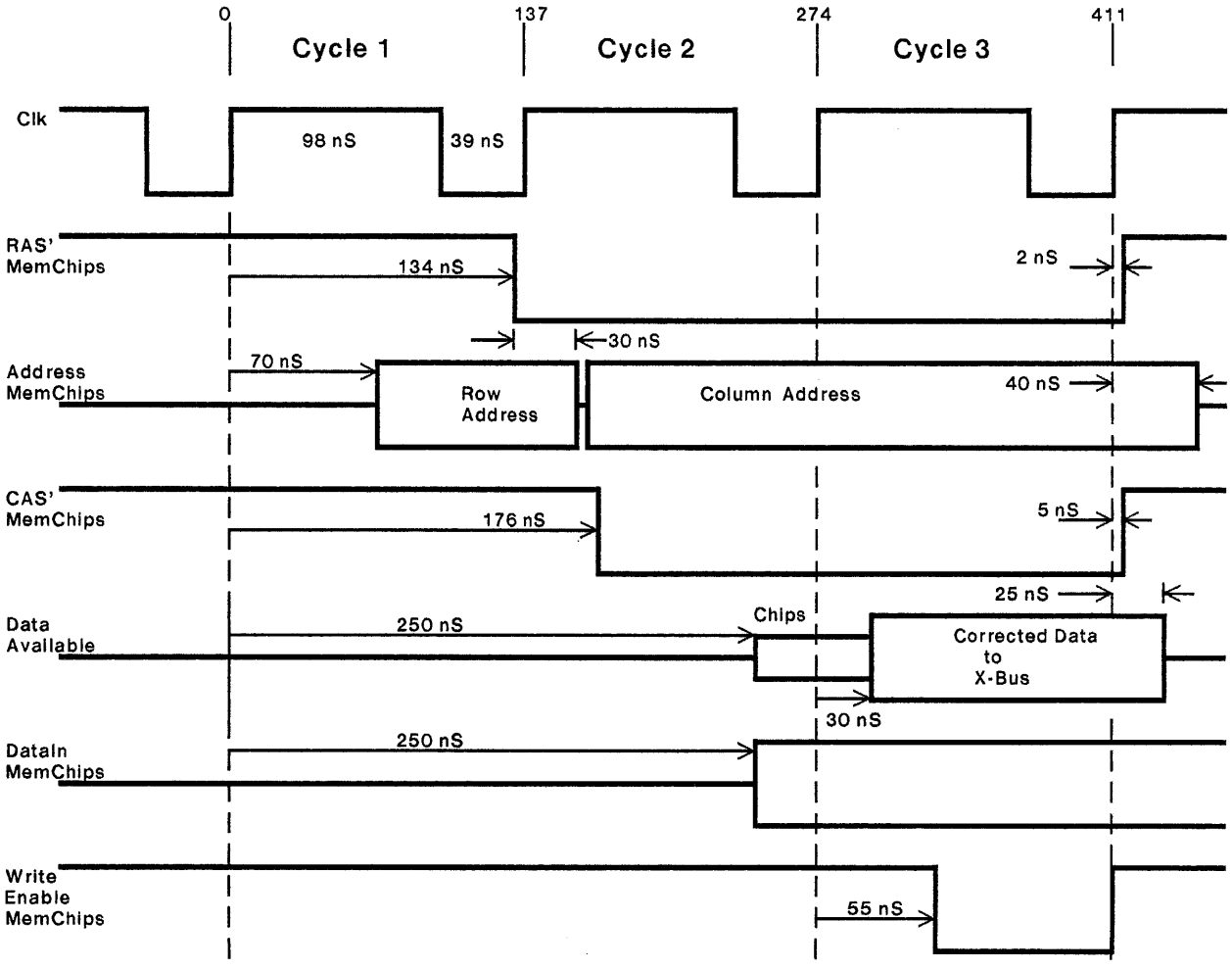
Dandelion Memory Registers

Memory Timing

Typical memory timing is shown based on measurement of processor port of the first stitchweld card. Both the processor and display ports will be described.

Processor timing is shown below. The memory address must be valid on the Y and YH busses early enough that the proper bank is selected and address lines valid for RAS' (row address strobe). The column address bits are latched by the RAS' signal. The CAS' (column address strobe) signal occurs 42 nS after the RAS' signal and latches the column address in the memory chips. Data becomes valid at the output of the chips at a maximum of 150 nS after RAS' or 100 nS after CAS', whichever is later. (Because 16K chips are used, 1 of the 7 bits used for RAS must come from the low byte. The contents of the low byte are often the result of an arithmetic operation computing the next address (high byte is held fixed). The maximum settling time of the high nibble of the low byte is too long if a carry from the low nibble occurs. Consequently, bit 12 (instead of bit 8) of the low byte is used during RAS. Consistent juggling occurs for map references so that this is invisible to the microcoder. This affects only the maximum run of sequential page mode accesses as described below.)

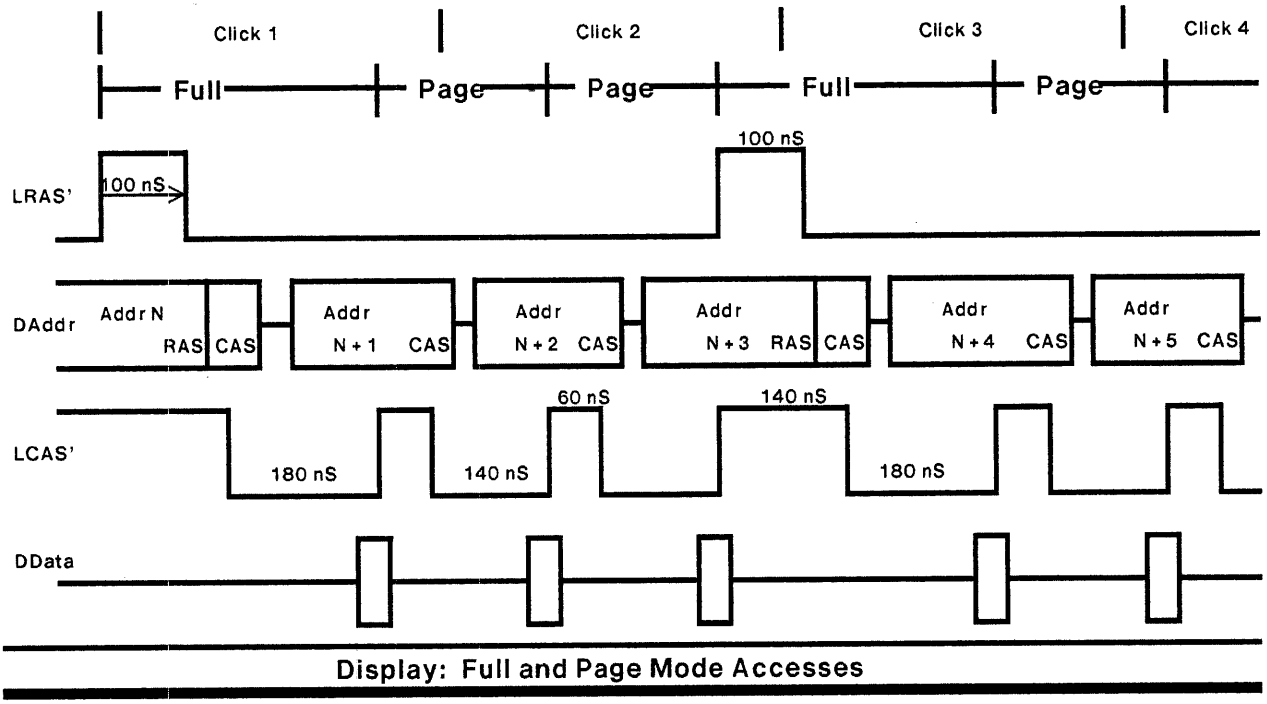
When writing into memory, the data to be written must be supplied during the second cycle of a click. The data is actually written in the latter half of the third click. Notice that up until the presence of the write pulse, all signalling is identical to a read cycle. The memory chips latch and hold the old data on their outputs during a write pulse if it occurs more than 150 nS after the RAS' signal. Thus, it is possible to write into a location and read data from it, all in the same memory cycle.



Normal Memory References through Processor Port

The display port supports both full and page mode accesses. The data delivered to the display port is not error corrected. The full access cycle time is 280 nS and the page mode access time is 200 nS. While the full access time is smaller than that specified in the data sheets (320 nS) for continuous operation, it is the average that is important, and the average cycle time in this case is 342 nS (6 full accesses per round, counting click 5). A page mode access occurs when the RAS' signal goes low and the CAS' signal cycles several times, strobing several different column addresses (low 7 bits) into the memory chips while retaining the same row address. (Because bit 12 is used during RAS, the maximum number of sequential page mode accesses between full accesses is 7, since bit 12 will change on every 8th access. The insertion of full accesses at the appropriate times is handled by the display controller.) The display controller generates all the timing and address signals for the display port.

In normal operation, the display controller will seize the low bank of memory for 4 clicks of every round. It will start with a full access which is aligned on a click boundary, and then proceed with page and full accesses until the end of click 4. The other page or full accesses will not necessarily be synchronized with any click or cycle boundaries. They are packed so as to maximize the number of accesses during the 4 clicks the display has the memory.



Display: Full and Page Mode Accesses

Memory Interface Signals

There are 6 groups of signals for the memory control card. They are power, data/address, error, register control, processor clocks, and memory clocks.

Power (29 watts typical)

+ 12 volts
+5 volts
-5 volts
Ground

Data/Address Busses

Y Bus	16	data must meet 15 nS setup time, address meets setup based on bit position (Y0-7 65nS, Y8-11 11nS, Y12-15 36nS)
X Bus	16	data available 45 nS min. before end of cycle 3
YH Bus	8	data must meet 80 nS setup time (includes 2 extra lines)
Display Data	16 lines	
Display Address	16 lines	
Task#	3 lines	(used for error logging)

Error Indication

MemError — available approximately 45 nS before end of cycle 3

Register Control

setup time = 70 nS

The control section of the processor must supply signals to load registers and enable data output to the bus.

mem		When ANDed with cycle 1,2, or 3 produces the following:
c1	MAR←	Loads memory address reg. from Y & YH busses
c2	MDR←	Loads memory data reg. from Y bus & starts write
c3	←MD	Gates memory data to X bus
MCtl←'		Control reg. with check bit inversion, bank select, and ECC enable bits
←MStatus'		Gates MStatus register to X bus
MapRef	c1 only	Does a MAR←, but with juggled bits.
Refresh'	c1 only	Causes a refresh operation and increments refresh counter
Disp/Proc.'		Goes high when display port is using low 64K.

Memory clocks

(LH - low-high transition, HL - high-low transition)

RAS'	HL 121 nS into cycle 1 re: qualified clock. LH at end of c3
CAS	LH 24 nS into cycle 2 re: qualified clock. HL at end of c3
LRAS'	Same as RAS, except when low bank is used by display
LCAS	Same as CAS, except when low bank is used by display
WPulse	LH 40 nS after qualified clock, HL 19 nS before qualified clock

Processor clocks

Cycle1'	Low during cycle 1 of click.
Cycle2'	Low during cycle 2 of click.
Cycle3'	Low during cycle 3 of click.
ppClock	137 nS period with 39 nS pulse width (LH - -7 nS, HL - 91 nS)

Memory Banks & Standby Power

The system (including the storage card) contains a total of 12 - 16K memory columns. To minimize power consumption, only one column at a time is cycled for normal memory accesses, and two at a time if the display is using the low 64K while the processor is using one of the higher banks. During refresh, all banks receive a RAS only cycle. Cycling all banks continuously in refresh cycles causes a drain of 3.75 amperes from the + 12 volt supply while cycling only 2 banks with normal memory references consumes 1 ampere.

System Parts Cost

The memory card can be broken up into control and error correction logic, and memory chips. Below are the chip counts and cost estimates for both the memory control card (64K) and storage card (128K).

Component		Mem. Control + 64K		128K Storage	
		IC's	$	IC's	$
Memory logic	@$ 1	77	77	26	26
Memory chips	@$ 5	88	440	176	880
Bypass Caps	@$ .20	165	33	202	41
PC Board		-	100	-	100
	Total	**165**	**$650**	**202**	**$1047**

Probability of Single and Double Errors

The following calculations yield probabilities of errors due to independent random processes in each chip. They do not include correlated events such as power line transients or static discharges which could affect all of the chips at the same time. A memory with 22 bits/word is assumed.

The hard failure rate is assumed to be .04%/1000 hours. The mean time to a single hard chip failure is about 13 months (9470 hrs.) for a 192K system using 16K memory chips.

The soft error rate for the chips is assumed to be 1%/1000 hours. Following are the probabilities of 0, 1, and 2 soft errors in a 22 bit word in a 10 hour period. 10 hours was selected as the interval over which errors could accumulate, with the system being reset after 10 hours. It is expected that most systems would be rebooted at least once in 10 hours. The mean time between single errors is 38 intervals and the mean time between double errors is approximately 36,200 intervals. It should be pointed that these probabilities are those that one would expect to measure with a program which continually scans through all memory cells looking for an error. If a program is confined to a small segment of memory, it would perceive a proportionately smaller probability of soft error.

Prob.(0 errors in 22 bit word in 12 bank system in 10 hr. interval) = .9736
Prob.(1 single error in 22 bit word in 12 bank system in 10 hr. interval) = .0263
Prob.(1 double error in 22 bit word in 12 bank system in 10 hr. interval) = 2.76×10^{-5}

Error Correction Logic

The error correction logic generates 6 check bits which are stored with each 16 bit word to provide single error correction and double error detection. 6 chips are used to generate the check bits. 25 chips are used to generate the syndrome bits, correct the data bits, and provide the capability of recording errors on a per task basis. Details of the error correction logic, including correction code tables, are included in the logic drawings.

RAS-CAS Multiplexer

Between the leading edges of the RAS and CAS pulses, the contents of the address lines to the memory chips must change from the row address to the column address. This transition must occur after the 20 nS hold time requirement for the row address and before the column address setup requirement of 10 nS after the CAS pulse (i.e. setup time = -10 nS). Since CAS' follows RAS' by only 42 nS, this leaves a 32 nS window in which the transition can take place. The design center for typical chips is 30 nS which allows for a 10 nS delay in the RAS' buffer chip or 22 nS extra delay in the delay line, multiplexer and address driver circuits. The RAS-CAS multiplexer is switched by a delayed version of RAS, with the delay generated on board to minimize possible skew.

The delay circuit is implemented using an inductor, capacitor, and resistor (single element delay line terminated in its characteristic impedance of 360 ohms) feeding a gate. This is used in preference to a packaged delay line because it costs less, takes less space, and will be easier to adjust when converting to a printed circuit board which will probably require adjustment of the delay. To minimize noise pickup, the delay components should be located next to the gate receiving the signal. (Delay in seconds $D = (LC)^{.5}$ Impedance in ohms $Z = (L/C)^{.5}$: L-Henries, C-Farads)

Memory Array Line Termination

It is important to terminate the lines driving memory chip inputs to prevent damage due to undershoot on the high-low transitions. The memory chips require that their inputs never go below -1 volt, to prevent forward biasing some internal parts of the chip and causing damage. Undershoot (and overshoot) result from the transmission line behvior of the signal lines in the array. This behavior becomes evident whenever the signal risetimes are comparable to the propagation time through the line (5nS and 3nS respectively for this system). Either series drive or shunt termination can be used with the lines. Both of these are shown in the following figure. The series drive consumes less power, since there is no steady state current flow, but it has a much longer propagation time.

Because speed is important in this system, the direct drive with matched termination was selected. The Shottky TTL drivers have an asymmetrical outout capability; they sink more current than they can source. For this reason, the termination resistor is terminated to a +2 volt source instead of ground. To obtain this voltage without excessive dissipation, half of the address lines are driven with the true value of the address while the other half are driven with the complement of the address. All of the termination resistors are tied to a common capacitor tied to ground. This amounts to a voltage divider with half of resistors tied high and the other half tied low, since each true value has a complement.

The last figure gives results of tests on the D0 96K storage card. This is of interest because it provides a reasonable estimate of what impedances might be expected for the address and control lines on a PWA. The impedance of the trace loaded with chips is in the 50 to 60 ohm range. Using a 62 ohm resistor to 1.9 volts results in a source current requirement of 25 mA and a sink current requirement of 29 mA. The effect of a 20 mA source current on chip temperature rise is tabulated in the bottom box of the figure. The dissipation in the S241 is the largest, since it contains 8 drivers. The extra junction rise should not cause trouble, however, since the 54S241 is rated to 125°C with the same .5 watt internal dissipation (i.e. a 55°C rise above the commercial part spec.). To ease the dissipation slightly, the termination resistor values are selected to produce about .4 volt undershoot, a value slightly larger than the characteristic impedance of the line.

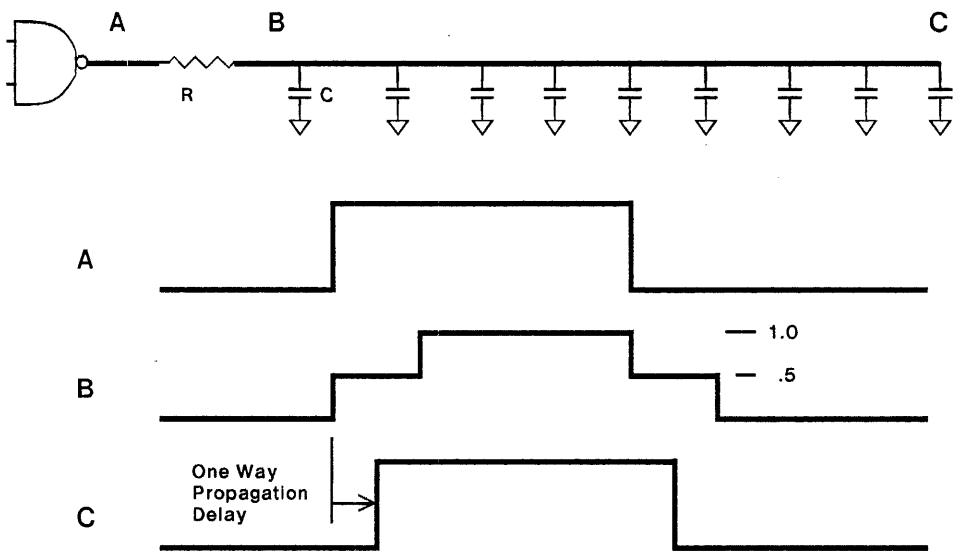
Power Supply Considerations

The memory system requires +12 volts, +5 volts, and -5.2 volts, all with a tolerance of $\pm$10%. The -5.2 volt supply must never go positive with respect to ground when the +12 volt supply is on. While the chip manufacturer does not require it, they suggest that the -5 volt supply be the first to come on and the last to go off. The supplies should be bypassed at entry to the board and at every logic chip and every third memory chip.

Propagation Delays and Line Termination

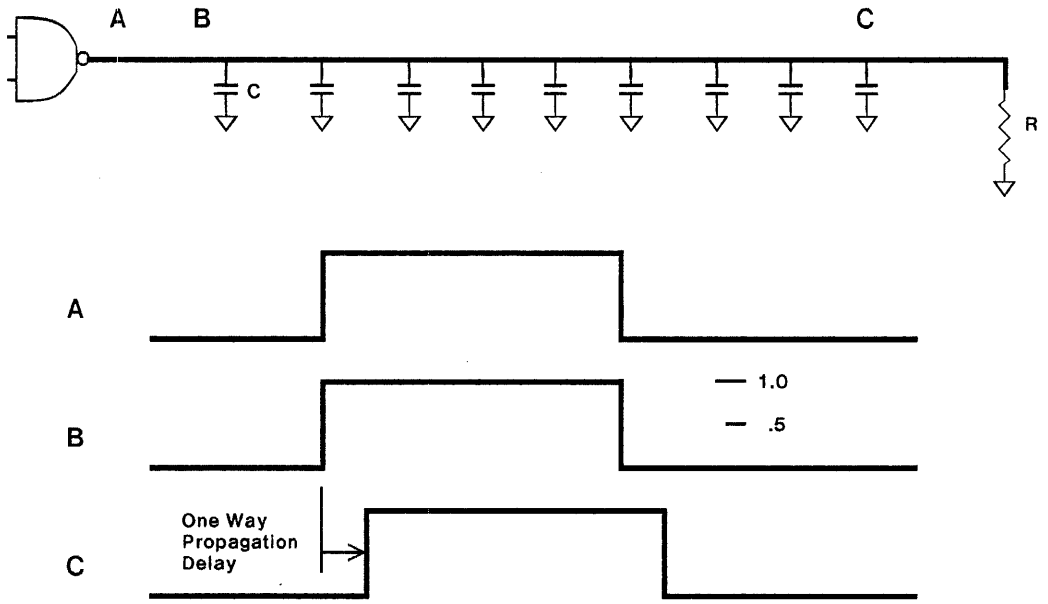
Purpose is to minimize ringing and undershoot on the signal line.

Series Drive



Note that point B takes the longest to see a full signal swing.
This termination technique takes less drive current.
Resistor value, R, should be same or slightly less than line impedance.

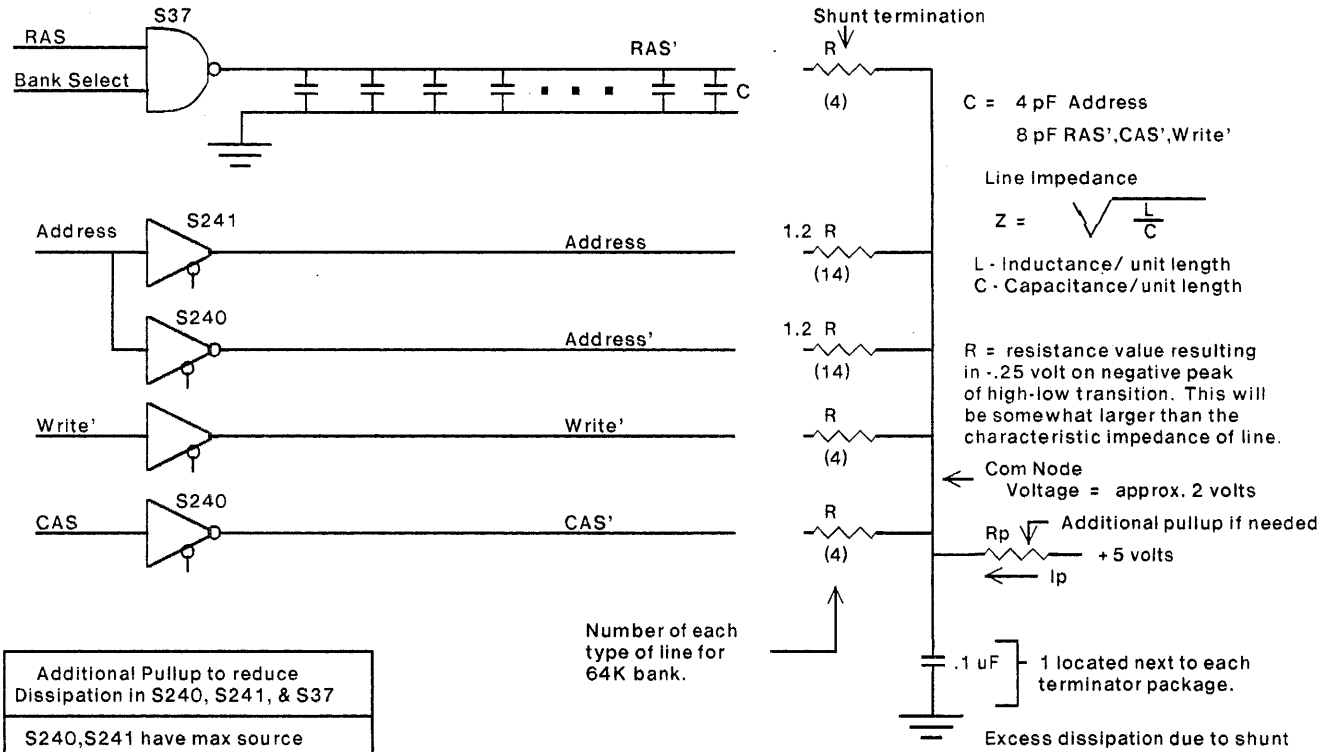
Direct Drive with Matched Termination



Termination resistor requires large drive current in logic high state. Terminating resistor to +2 volts instead of ground eases this problem considerably.

Resistor R, should be same or slightly more than line impedance.

Prop01.sil



Additional Pullup to reduce Dissipation in S240, S241, & S37

S240,S241 have max source current of 15 mA. A voltage source of 4 volts with a 25 ohm series resistor makes a reasonable model of the S240 output when in the high state. Thus, logic high output voltage must be 4 - .015x25 = 3.625 V or greater. Terminator current must not exceed 15 mA and consequently the common node voltage supplied to terminators may have to be raised by use of an additional pullup resistor. Below is a table of terminator resistor values, R, and associated pullup resistor parameters. The 64 mA sink spec is also met by the following values.

Term R	Com Node V	Additional Pullup Rp	Ip	Rp Diss.
47	2.92	2.2	.94 A	1.95 W
75	2.5	6.8	.37	.92
100	2.13	22	.13	.36
121	1.82	Infinite	0	0

RAS'	*Column 1*
CAS'	
Write'	
Address00	
Address01	
Address02	
Address03	
Address04	
Address05	
Address06	
RAS'	*Column 2*
CAS'	
Write'	
Address00'	
Address01'	
Address02'	
Address03'	
Address04'	
Address05'	
Address06'	

Columns must be paired to balance current from address lines.

Number of 1's & 0's contributing to the capacitor voltage under verious conditions

No Access	Write	Refresh
14 - 1	14 - 1	14 - 1
14 - 0	14 - 0	14 - 0
8 - 1	6 - 1	8 - 1
4 - CAS	4 - CAS RAS Write'	4 - RAS
22 + 1.33	20 + 1.33 + .25 + .85	22 + 1
23.33	22.43	23

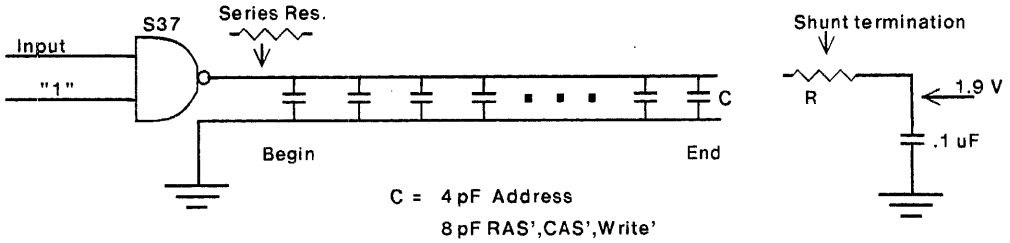
Capacitor voltage =

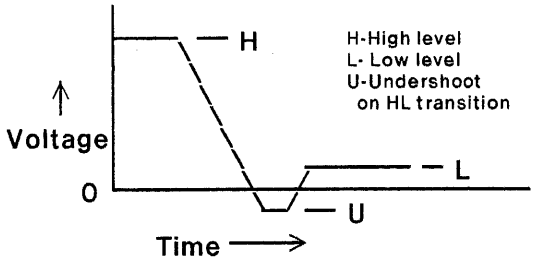
$\frac{23}{40} \times V_H = .575 \times 3.3V = 1.89V$

This can be increased by use of additional pullup shown above.

Shunt termination of the memory drive lines can speed up the memory. See 96K storage card tests. Supplying 2 volts for the terminating resistors can be accomplished by inverting the signal to half of the address lines. This guarantees a level half way between logic high and logic low. Connection of terminators for RAS, CAS, and write moves this level up somewhat and causes some variation during different operating conditions of the memory. This variation is not too great as can be seen from the calculation in the box above. Biasing the termination voltage upward with an extra pullup could be used to reduce the power dissipation in the driver chips when in the high state. With R greater than about 120 ohms, this should not be necessary.

Memory Line Drive and Termination





Tests on D0 96K Storage Card 6-24-79

CAS Line

		S37 Input	S37 Output	18 Mem. Chips Begin	18 Mem. Chips End	Termination	Voltages H	Voltages L	Voltages U	Extra Supply Current
Series	LH *	0 nS	4 nS	9 nS	8 nS	27 ohm	4 V	.2	-.4	0
	HL	0	6.5	12	9.5	series				
Shunt	LH	0	4.5	5.5	8	62 ohms	3.5	.3	-.3	.01 A
	HL	0	4.5	5.5	8	to 1.9 V				
		———				R = 100 ohm to 1.9 V	———		-.75 V	

Addr. Line

		S37 Input	S37 Output	18 Mem. Chips Begin	18 Mem. Chips End	Termination	Voltages H	Voltages L	Voltages U	Extra Supply Current
Series	LH *	0 nS	4 nS	8 nS	7 nS	R = 27 ohm	3.8V	.2	-.7	0
	HL	0	5	9	7.5	series				
		———				R = 0 ohms	———		3.0 V	
Shunt	LH	0	4	5	7	R = 62 ohm	3.45	.3	-.4	.01
	HL	0	4	4.5	7	to 1.9 V				

** Time is from 1.3 V point on input to .8 V for HL and 2.8 V for LH.*
18 chips in row 9" long
Risetime and falltime for shunt terminated line = 5nS.
Propagation time for 10" line with 6 loads LH- 3 nS HL- 2 nS. *(TTL loads)*
Extra supply current is that due to the 62 ohm shunt termination.
Undershoot is measured at the end of the line.

Power Consumption

108 memory chips MK4116-2

Conditons	+12 V	+5 V
RAS cycling 310 nS -L & 100 nS - H	1.41 A	.07 A
CAS cycling 310 nS -L & 100 nS - H	.07	.07
RAS & CAS cycling L- 310 nS H- 100 nS	2.13 A	.14 A
Quiescent current	.07	0

Effect on IC package dissipation

Package	Thermal Resistance junction to ambient	Internal Dissipation	Extra dissipation for 20 mA @ 3.5 V out	Extra Junction temp. rise	Total temp. rise
S241 20 pin	80 °C / watt	.5 W	.24 W	19.2 °C	59.2 °C
S37 14 pin	100 °C / watt	.18 W	.12 W	12 °C	30 °C

ceramic packages

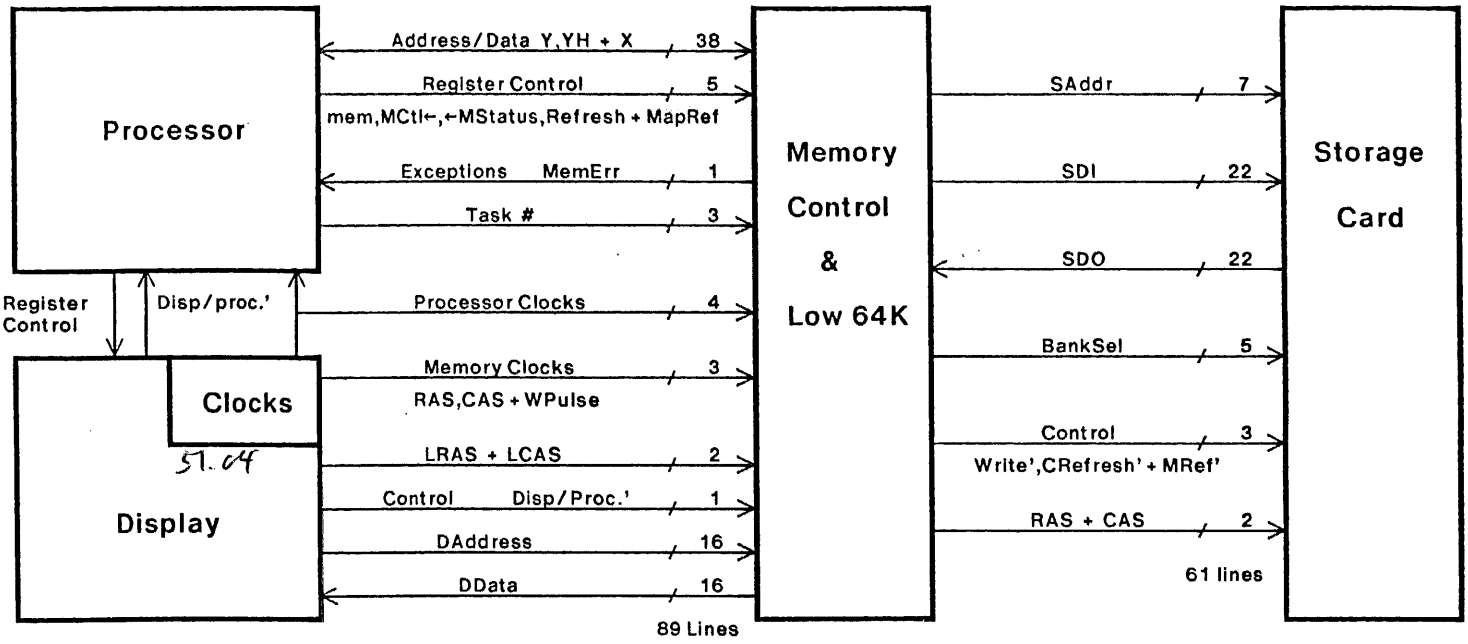
TABLE OF CONTENTS

SHEET

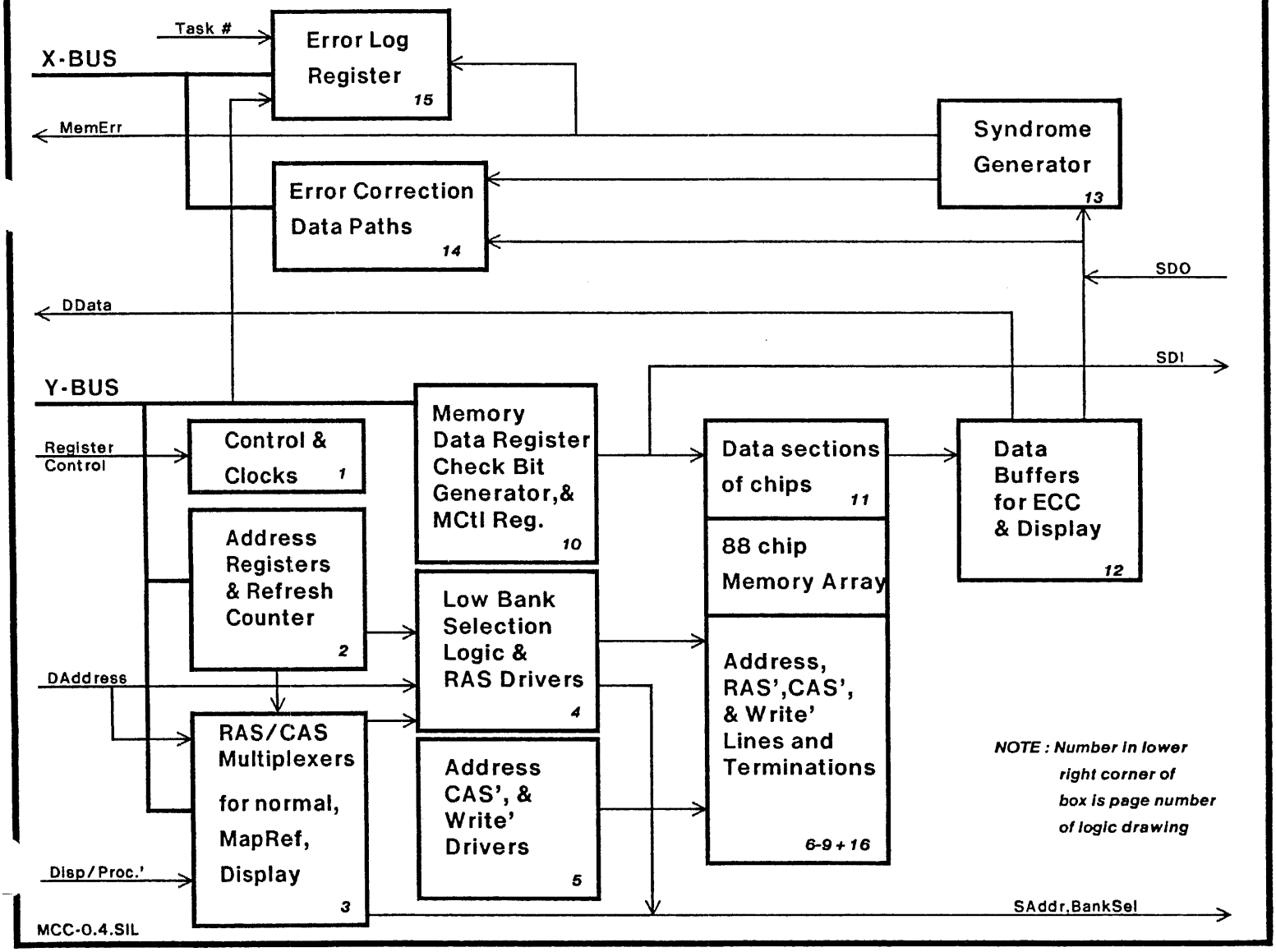
0.4 MEMORY CONTROL CARD BLOCK DIAGRAM

1. WRITE, CREFRESH', MREF, LDMDR, CYCLE RCV, MDCLK, ←MD'
2. REFRESH COUNTER, CAS REGISTERS
3. ADDRESS SELECTION LOGIC, RASDLY, LRASDLY
4. MEMORY BANK SELECTION
5. LOW 64K BANK DRIVERS FOR ADDRESS, CAS', WRITE'
6. LOW BANK A
7. LOW BANK B
8. LOW BANK C
9. LOW BANK D
10. DATA REGISTER, CONTROL REGISTER, CHECK BIT GENERATOR
11. MEMORY CHIP DATA PATHS
12. MEMORY DATA BUFFERS
13. SYNDROME GENERATOR
14. ERROR CORRECTION DATA PATHS
15. ERROR LOG REGISTER
16. RESISTORS AND R-DIPS
17. CAPS, DIODES, AND FUSES
18. TEST POINTS
19. FILTER CAPS
20. FILTER CAPS
21. TEST POINT AND EDGE CONNECTOR LISTINGS
22. EDGE CONNECTOR LISTING
23. EDGE CONNECTOR AND SIGNAL LISTINGS
24.-45. SIGNAL LISTING

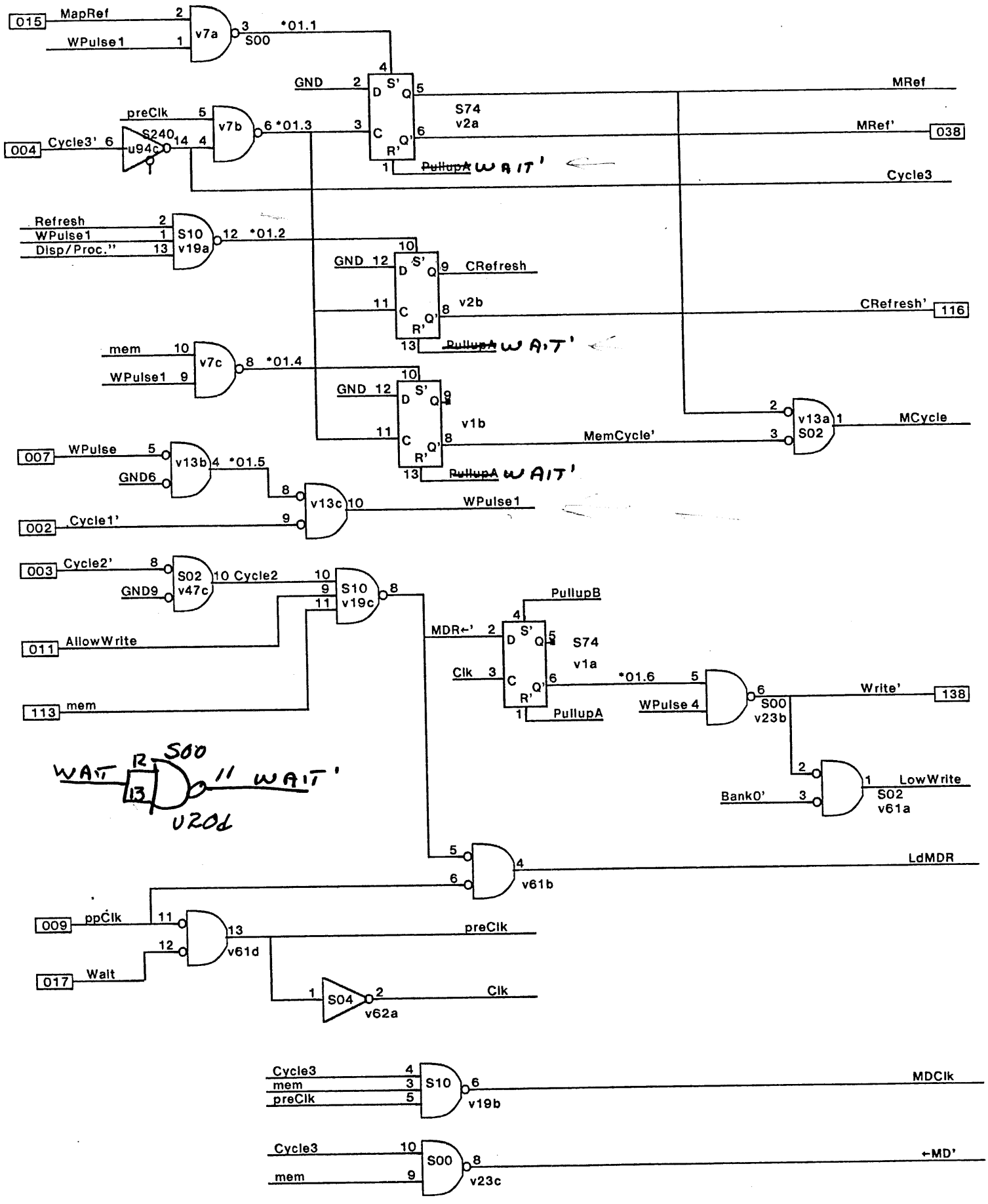
MEMORY SYSTEM



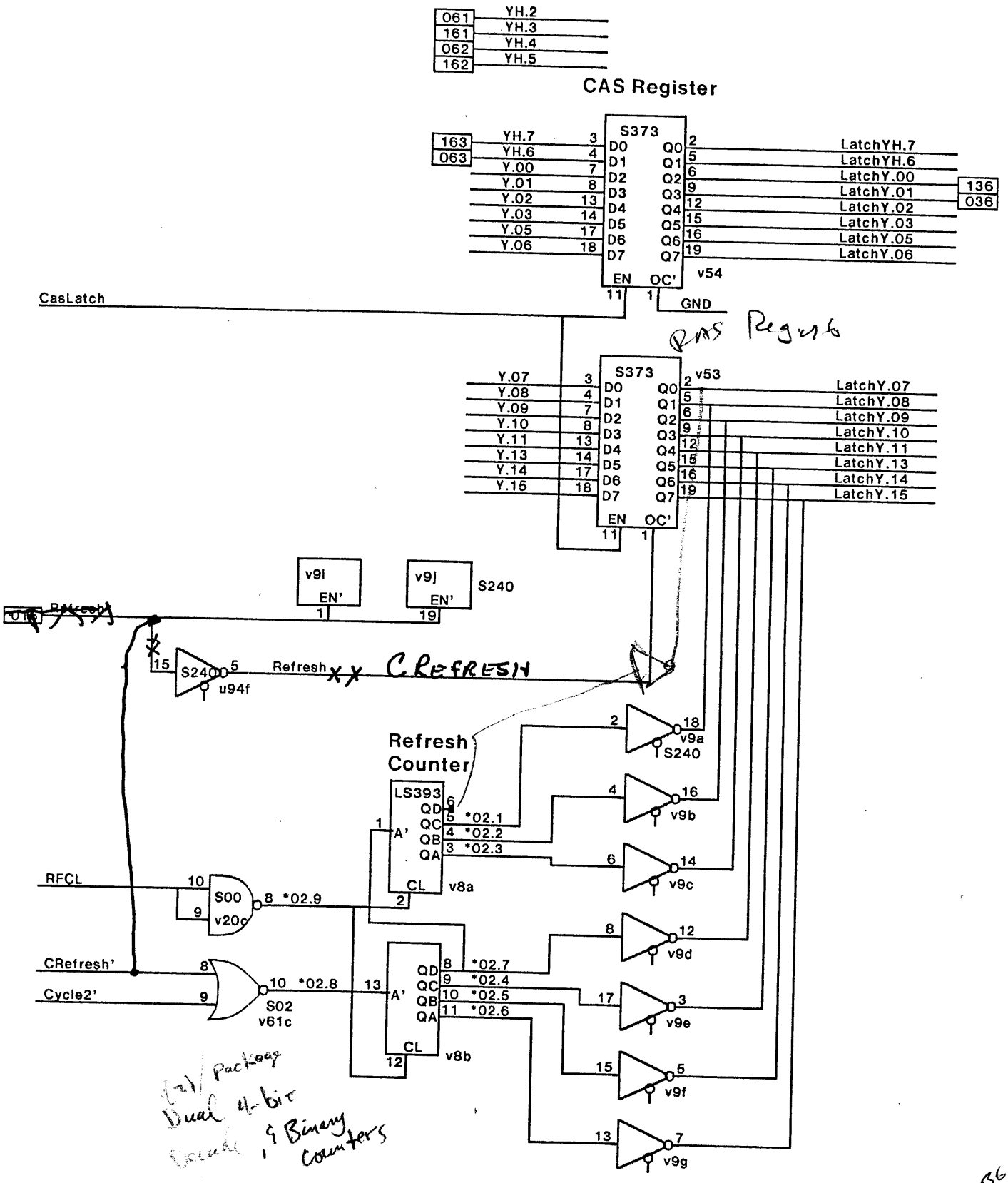
Memory Control and Low 64K bank



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 0.4 OF	



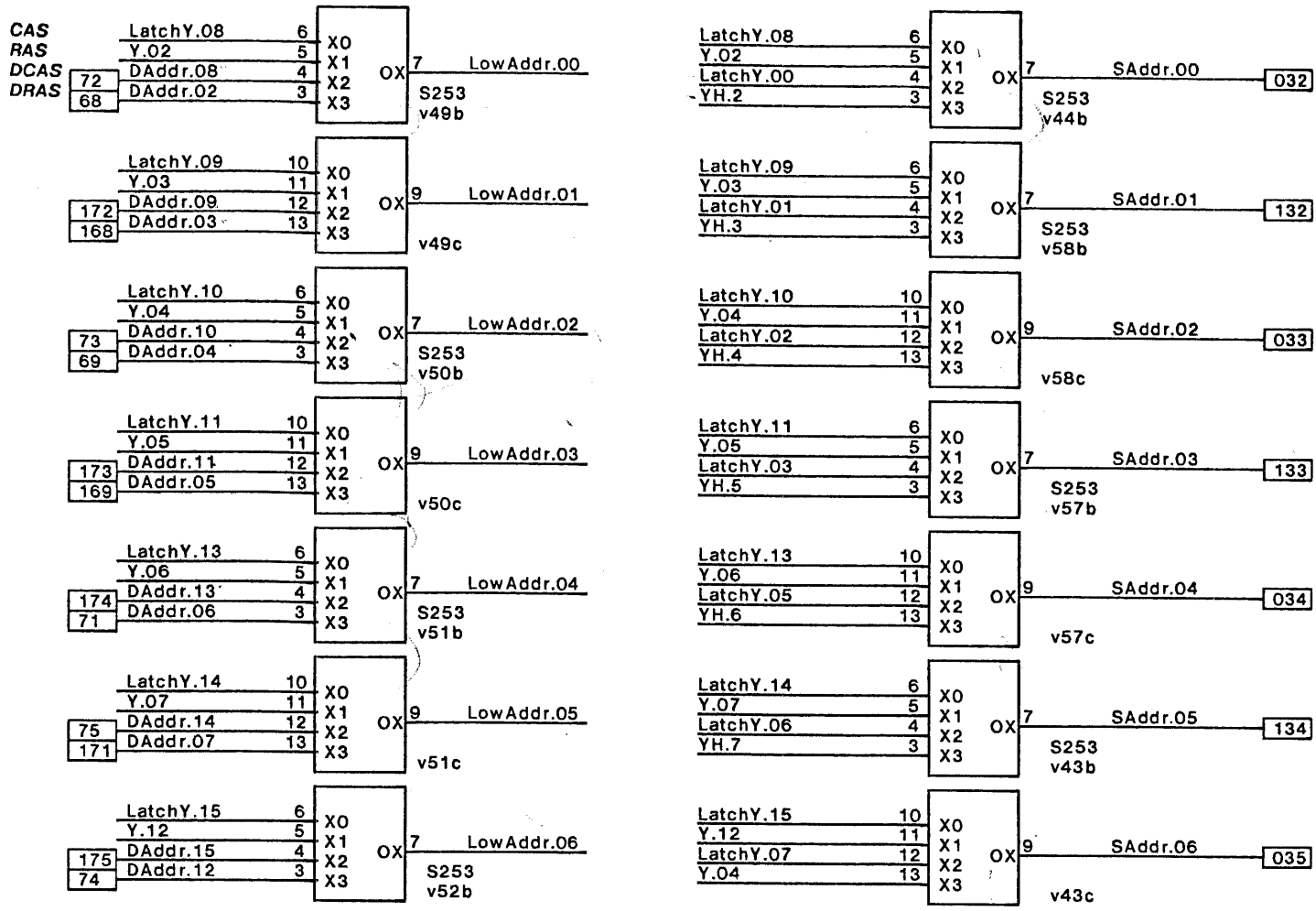
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 1 OF	



8-6 9 36

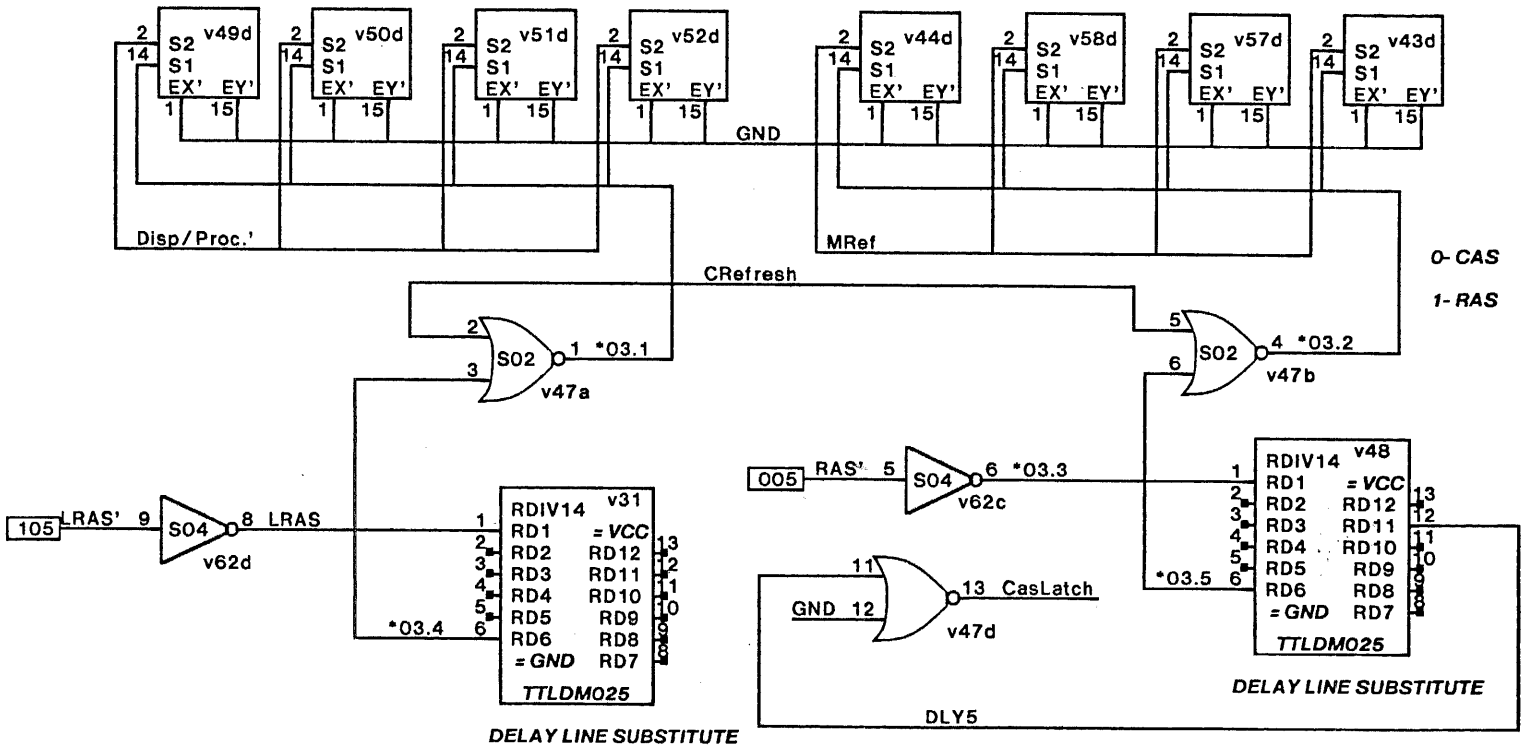
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 2 OF	B

S 157

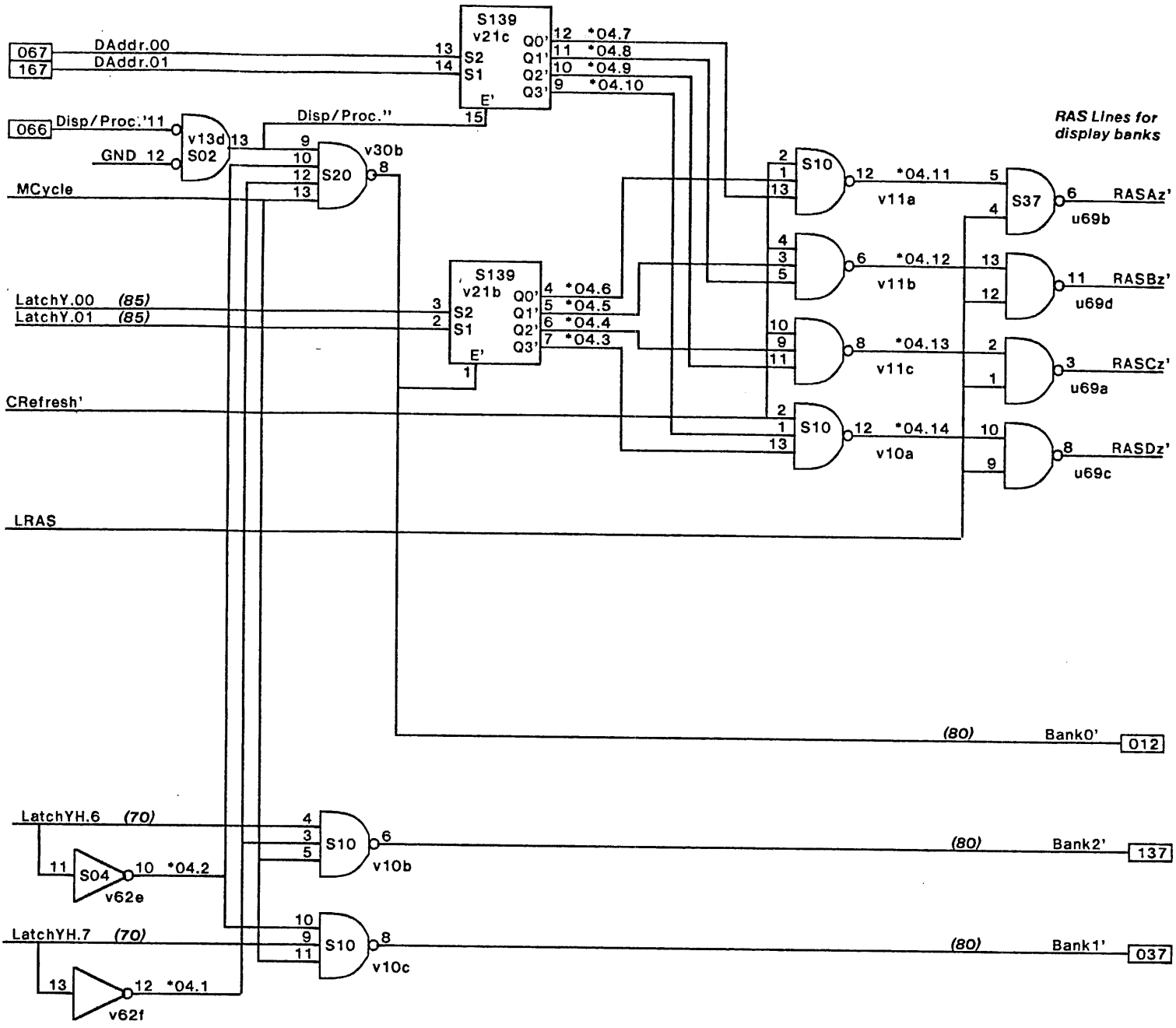


Low Bank Selection

High Bank Selection



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 3 OF	B



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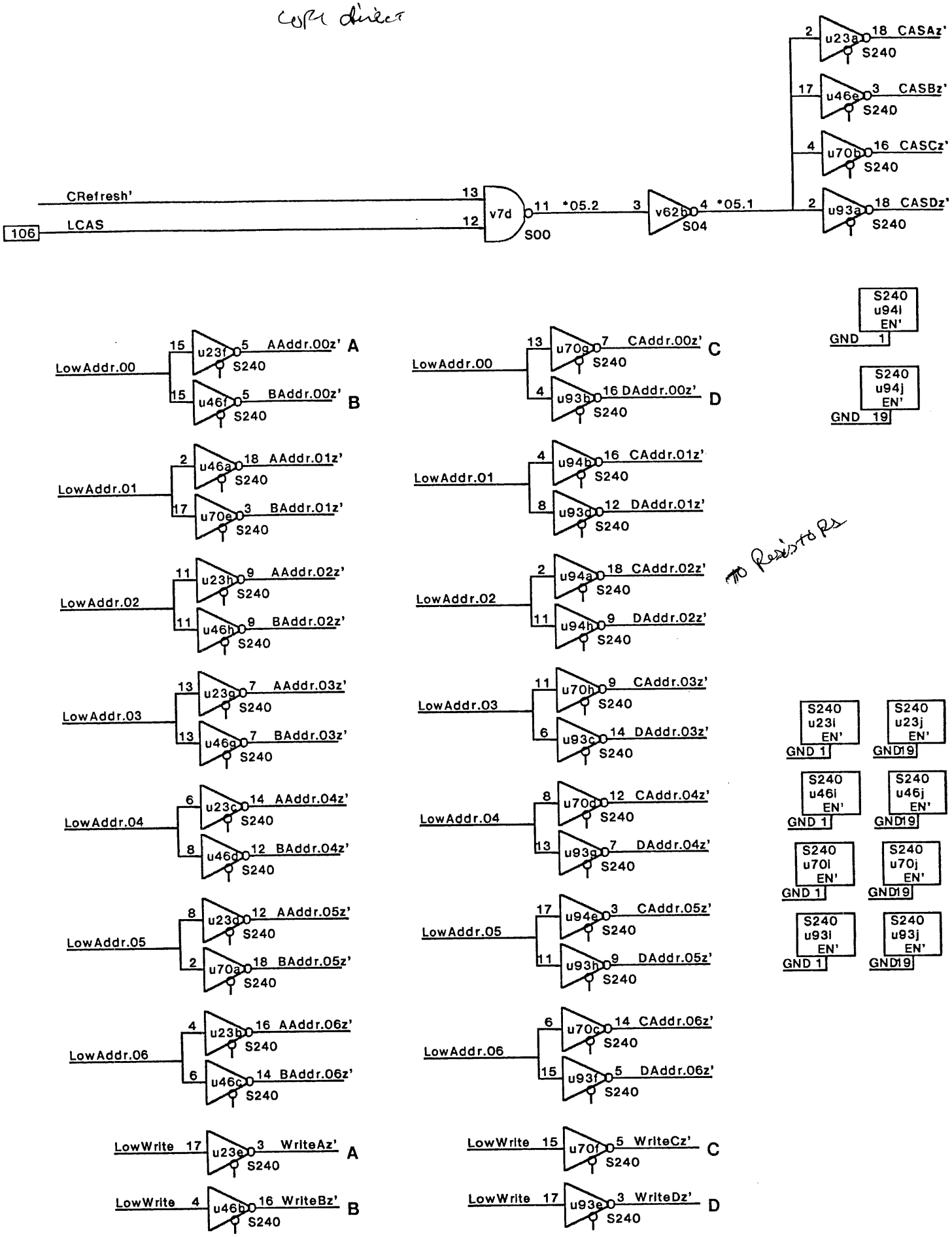
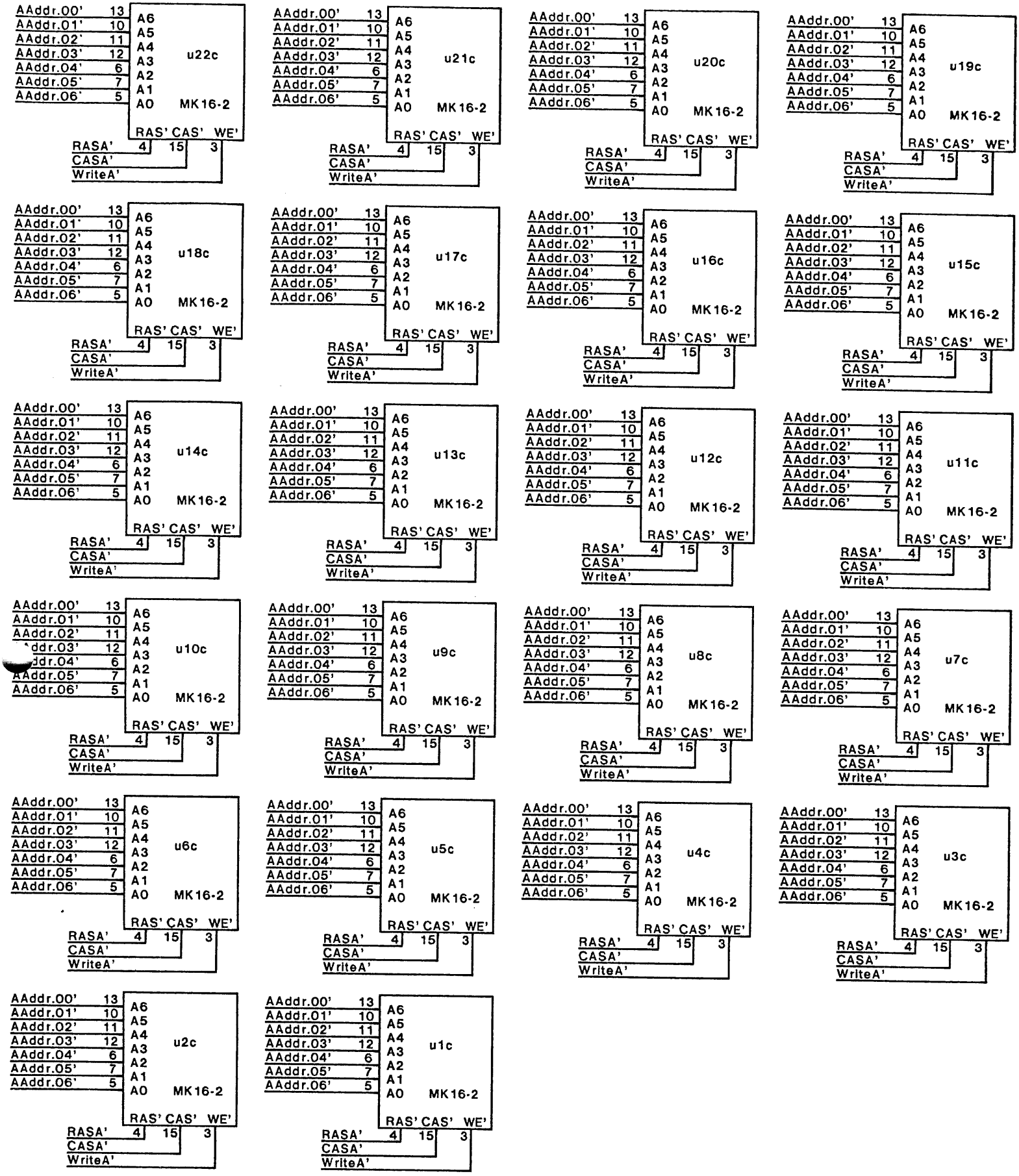
	TITLE SCHEMATIC, MCC Memory Bank Selection	A4	SHEET 4 OF	B



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 5 OF	B



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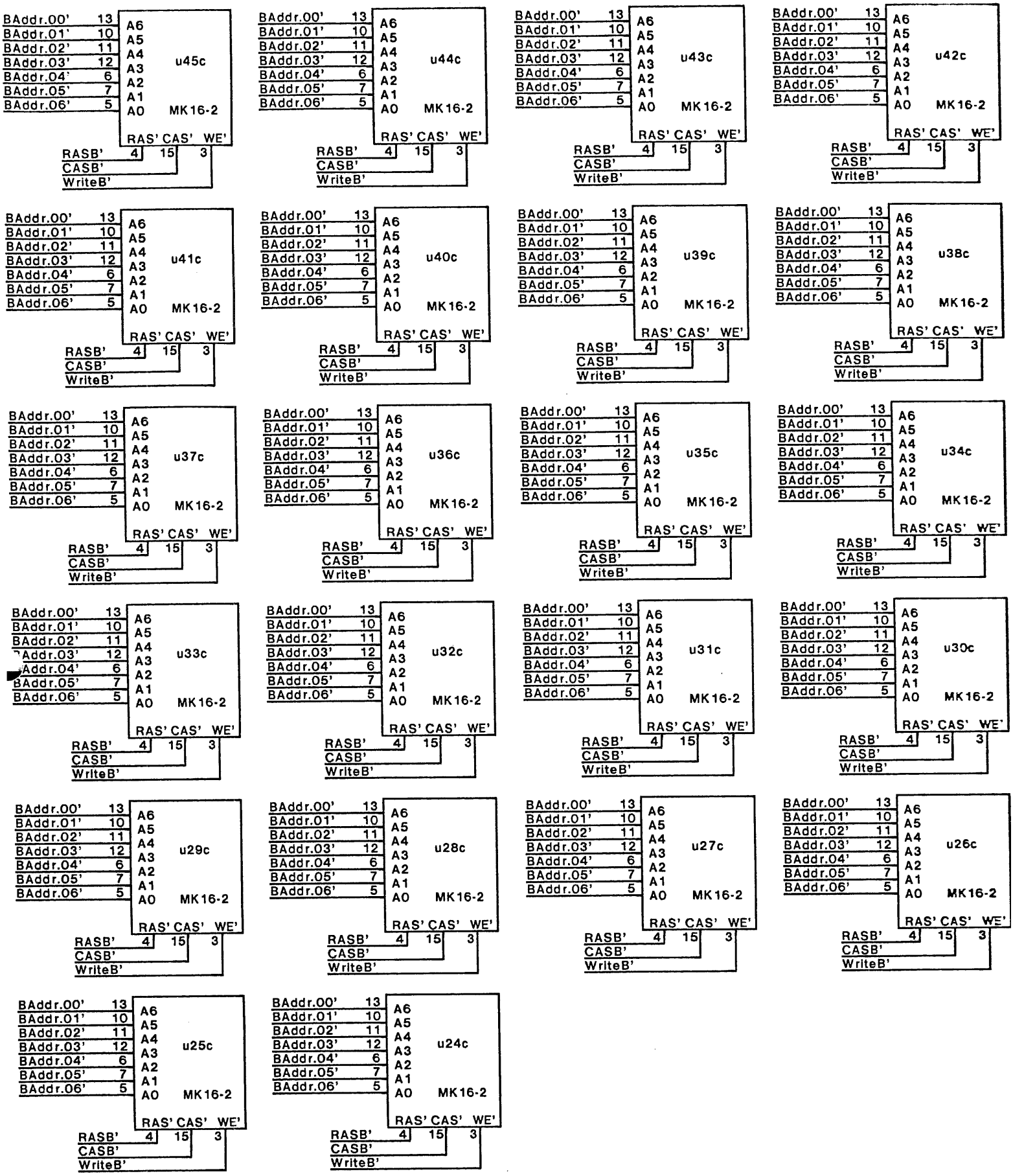
	TITLE SCHEMATIC, MCC	A4	SHEET 6 OF	B



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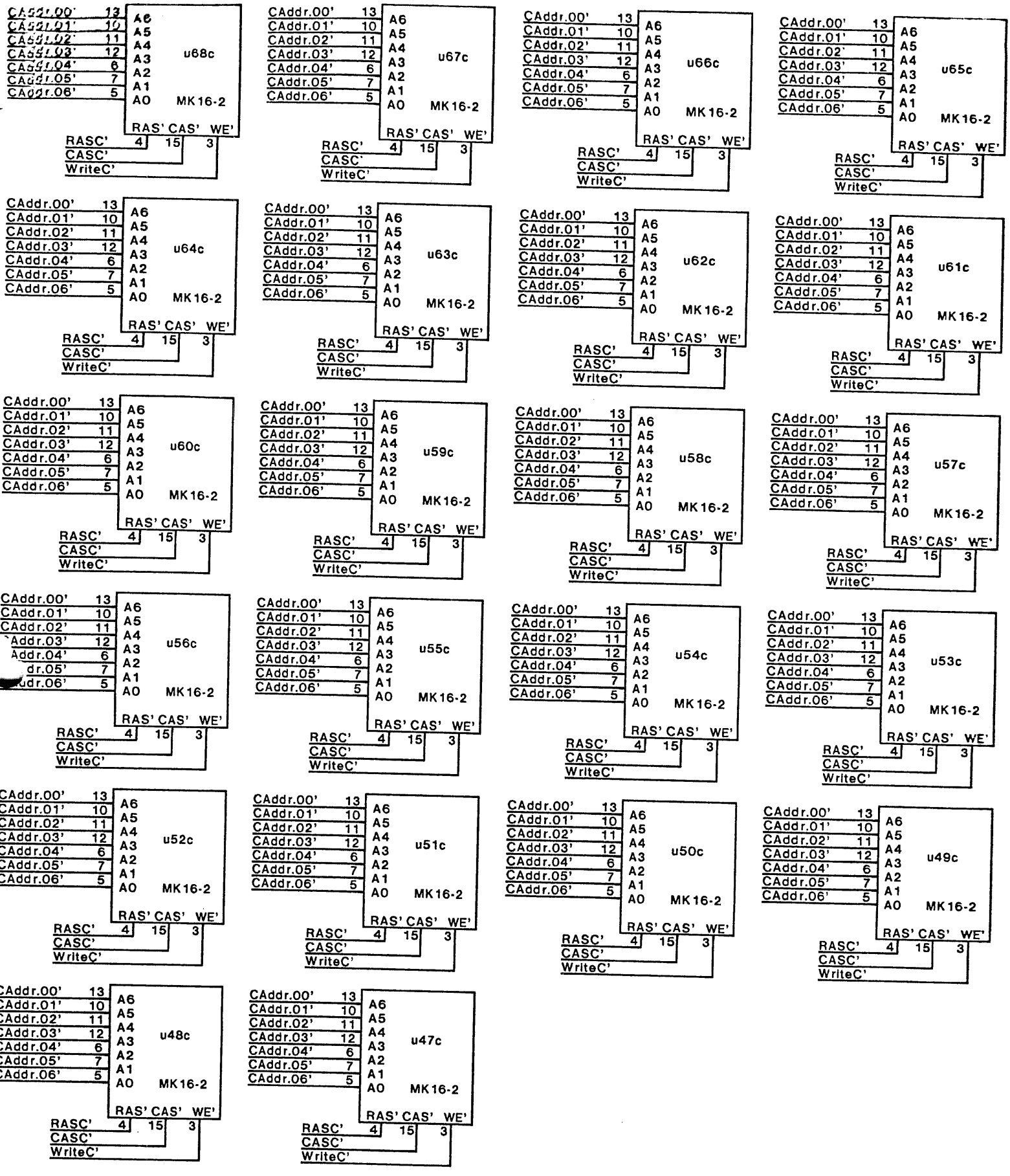
	TITLE SCHEMATIC, MCC	A4	SHEET 7 OF	B



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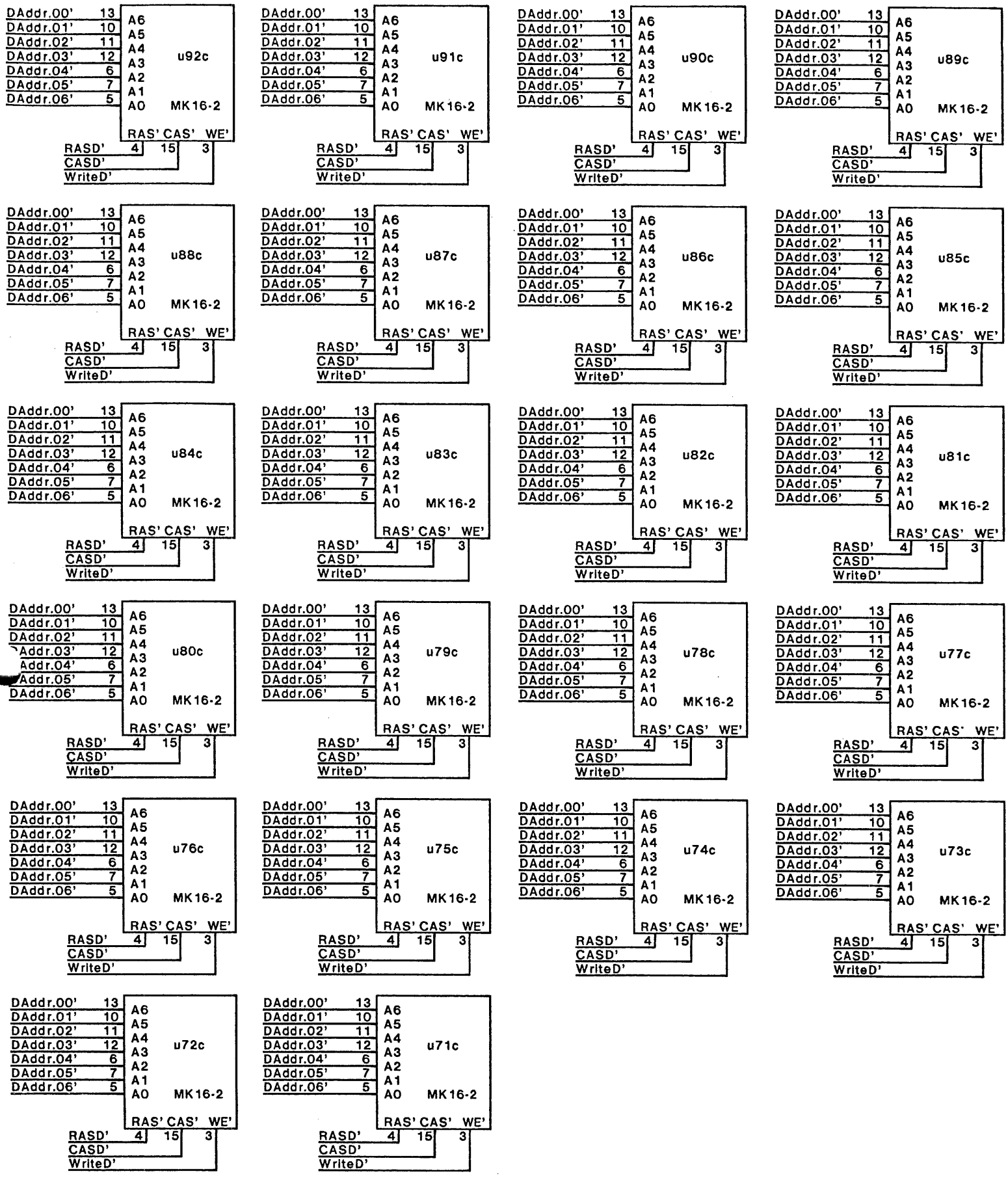
	TITLE SCHEMATIC, MCC		SHEET 8 OF	



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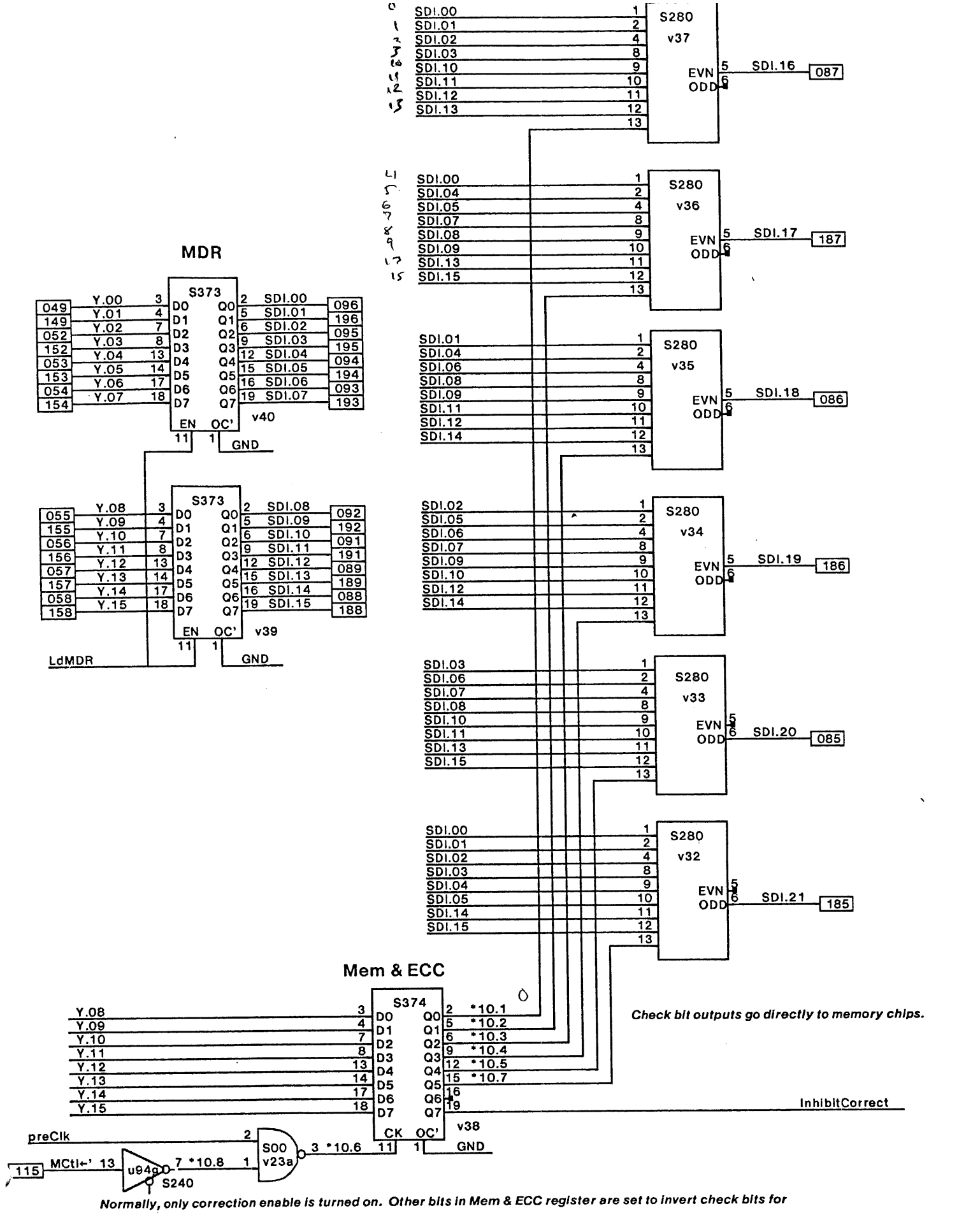
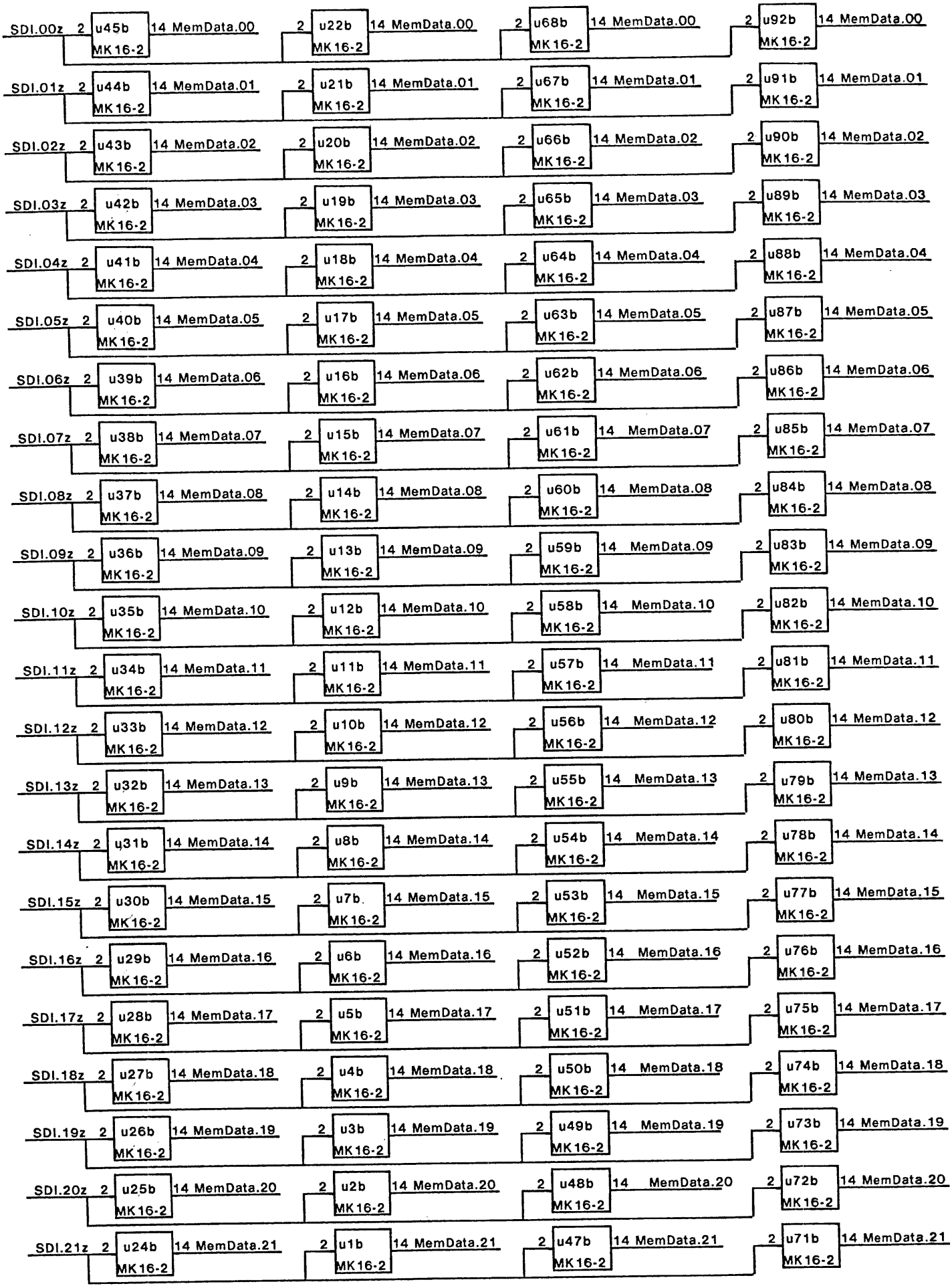
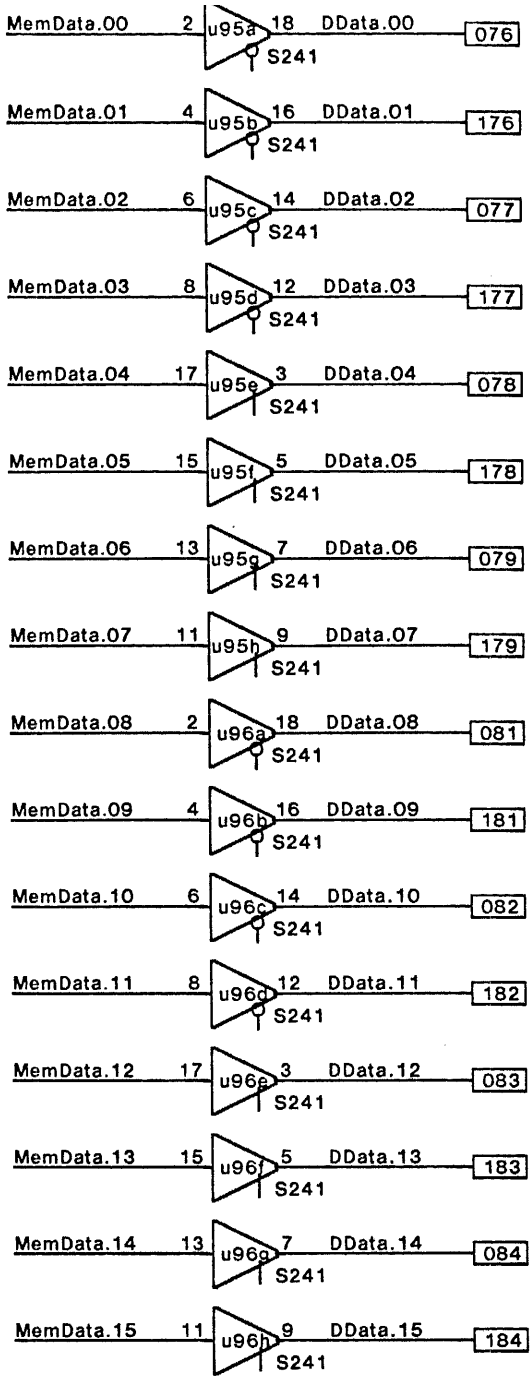
	TITLE SCHEMATIC, MCC	A4	SHEET 9 OF	B



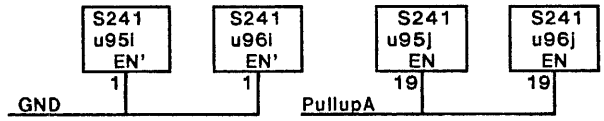
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 10 OF	B

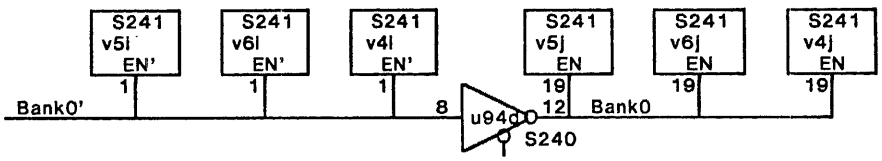


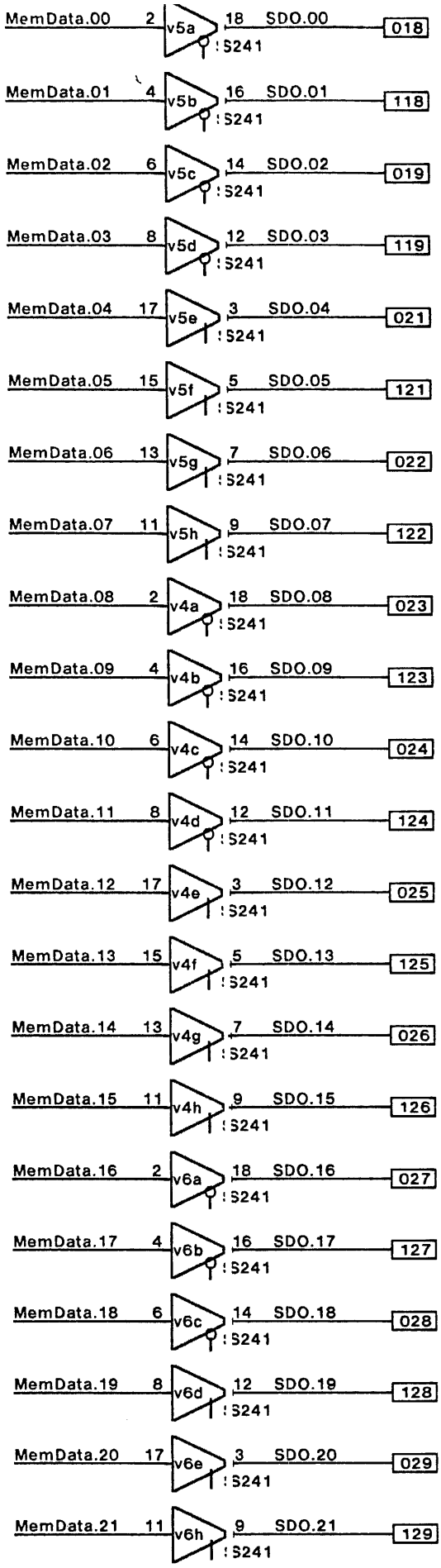
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 11 OF	B



Display Data Buffers

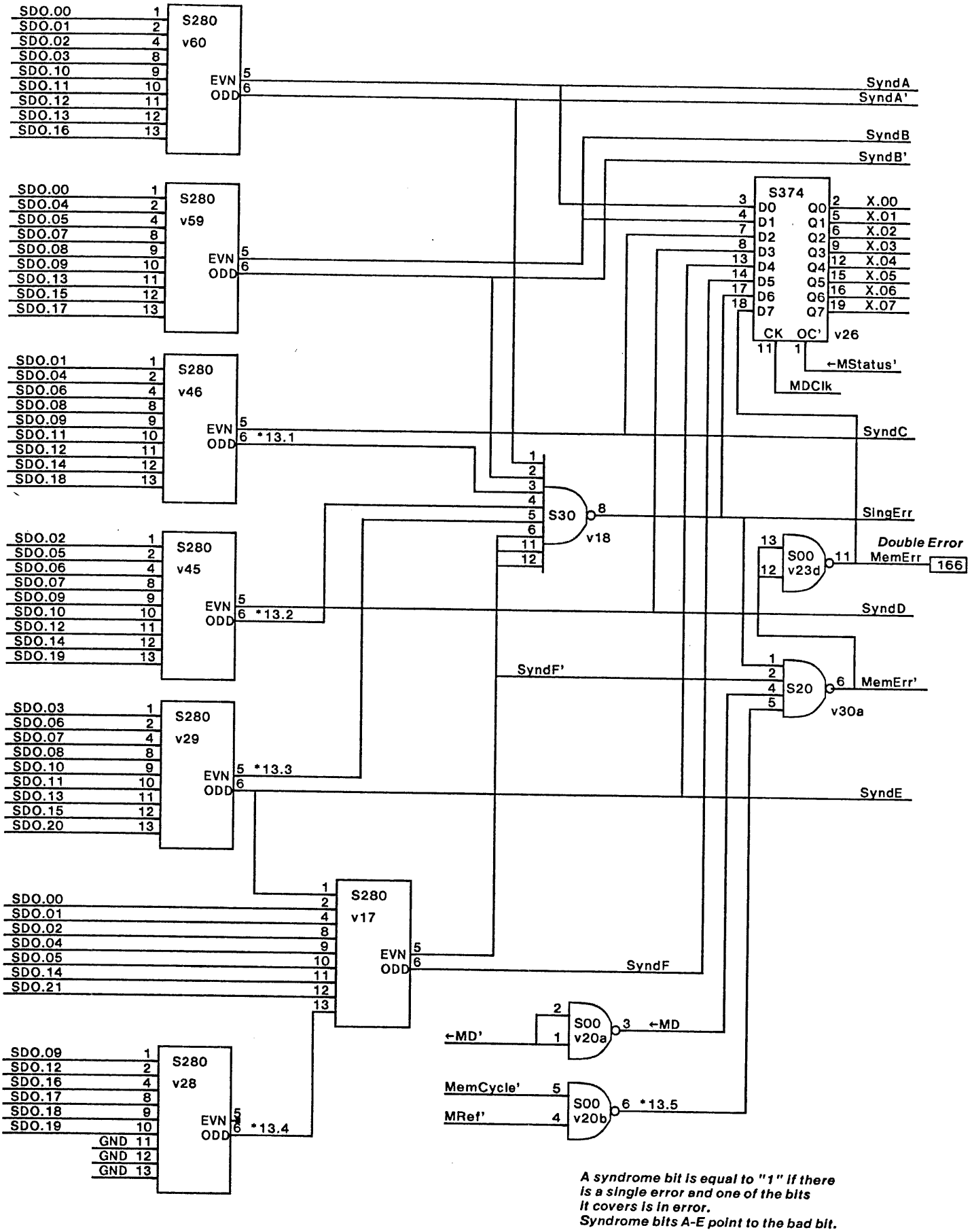






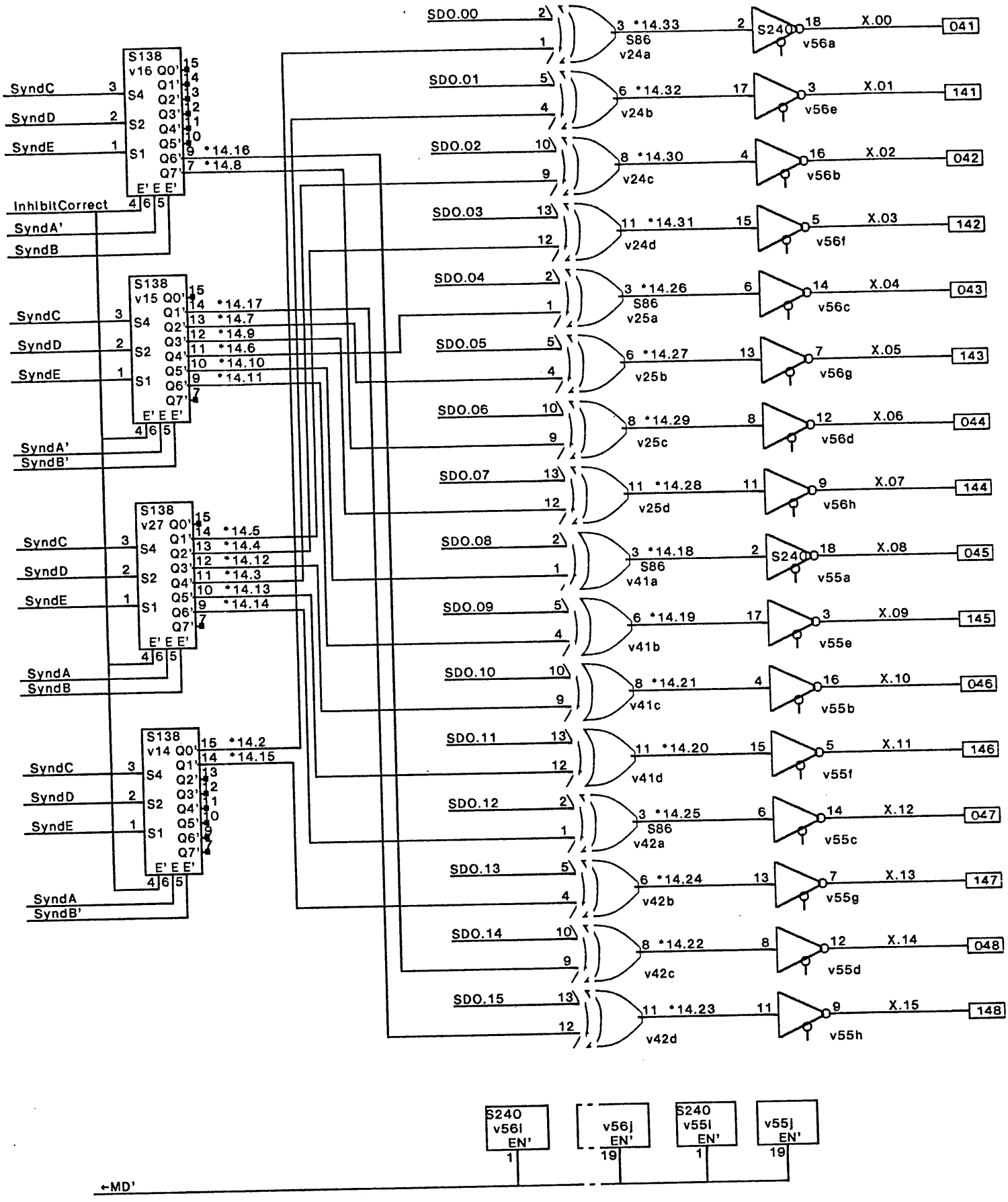
Main Data Buffer s

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217
	TITLE SCHEMATIC, MCC		SHEET 12 OF
			SHEET REV. B



A syndrome bit is equal to "1" if there is a single error and one of the bits it covers is in error. Syndrome bits A-E point to the bad bit.

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 13 OF	B

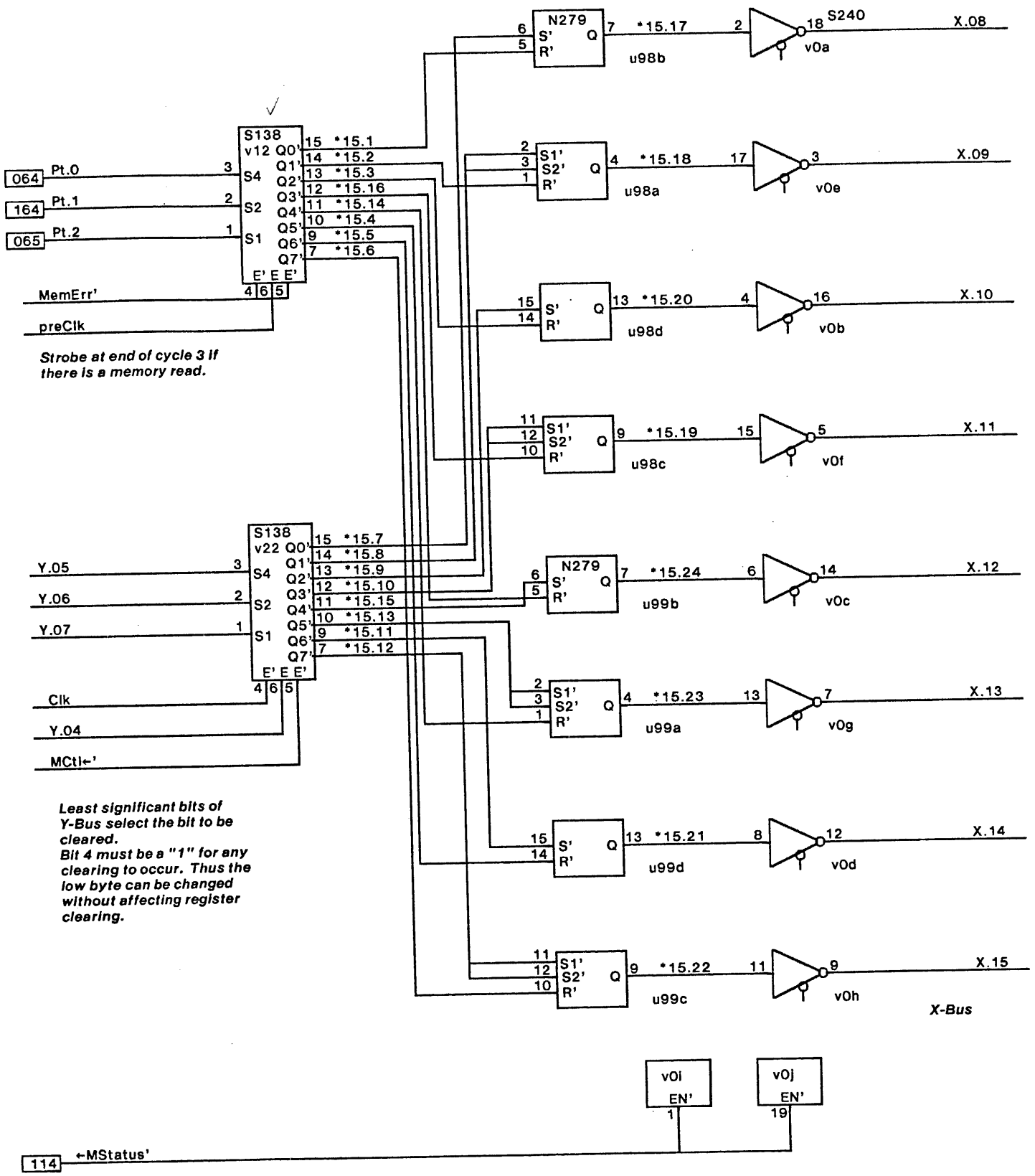


Syndrome Bits point to the bad bit. SyndA is most significant bit & SyndE is LSB.
Syndrome bit is a '1' if one of the bits it covers is in error.

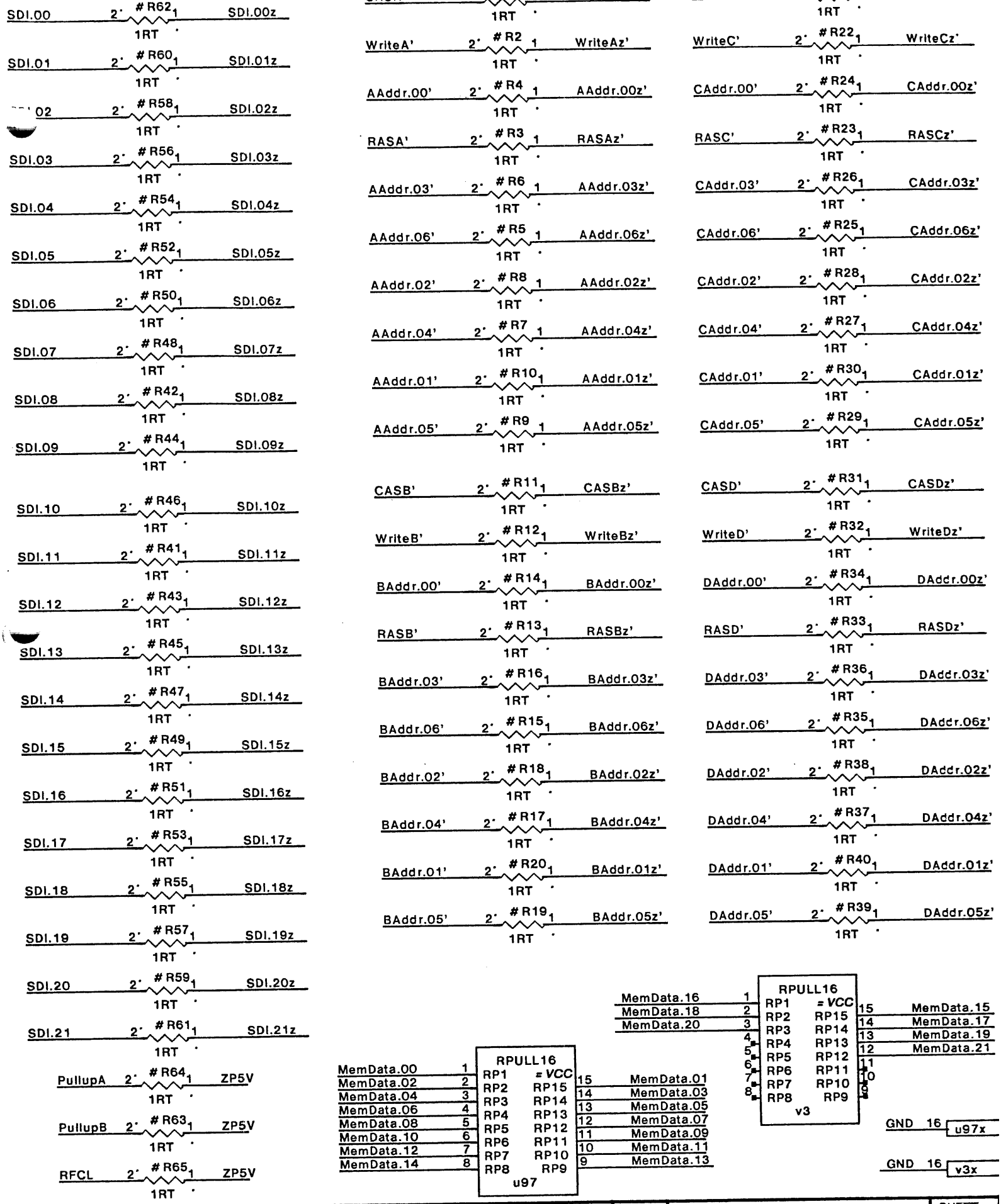
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 14 OF	

Errors Register

Bit is 1 if there was an error.



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 15 OF	



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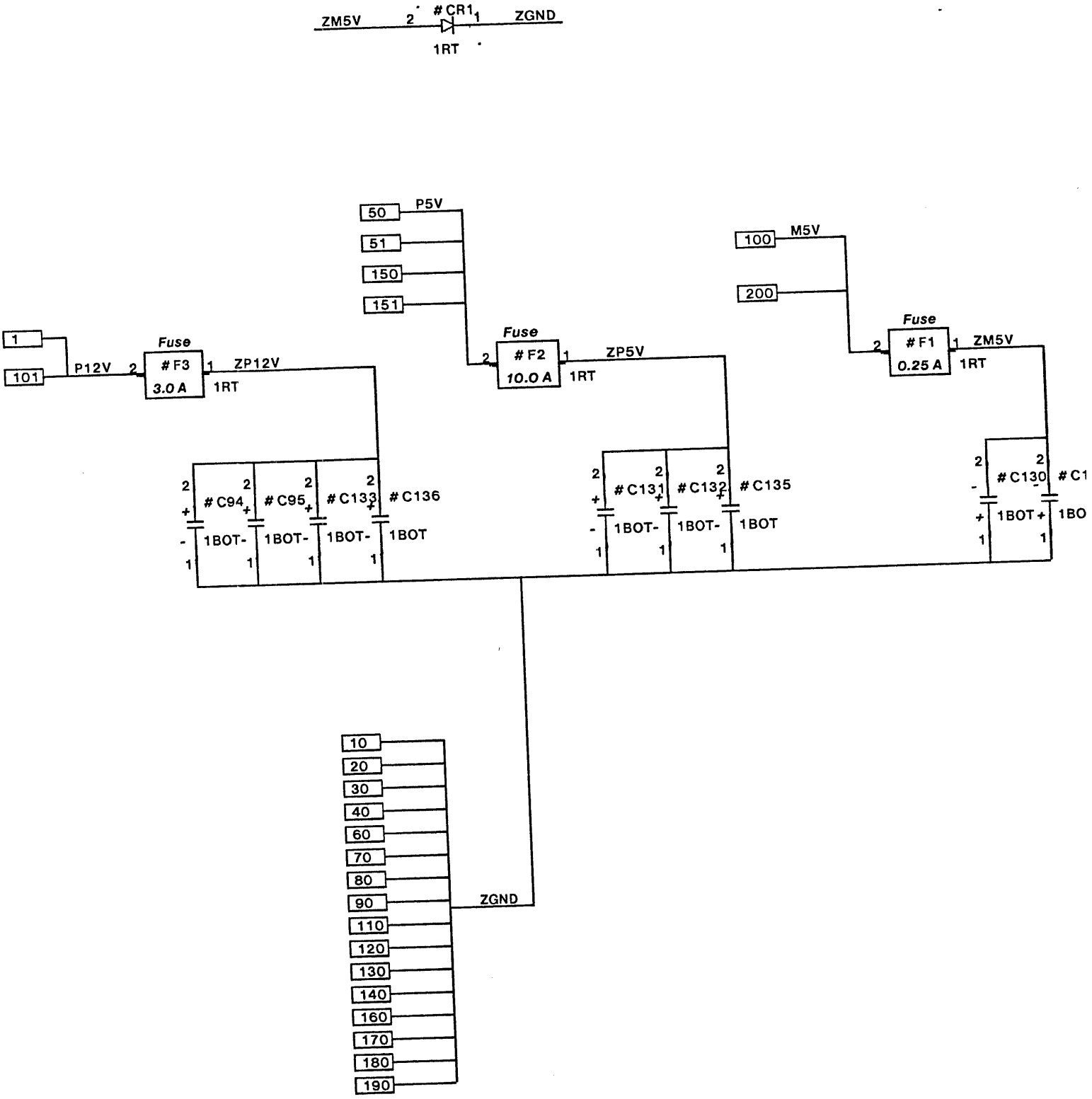
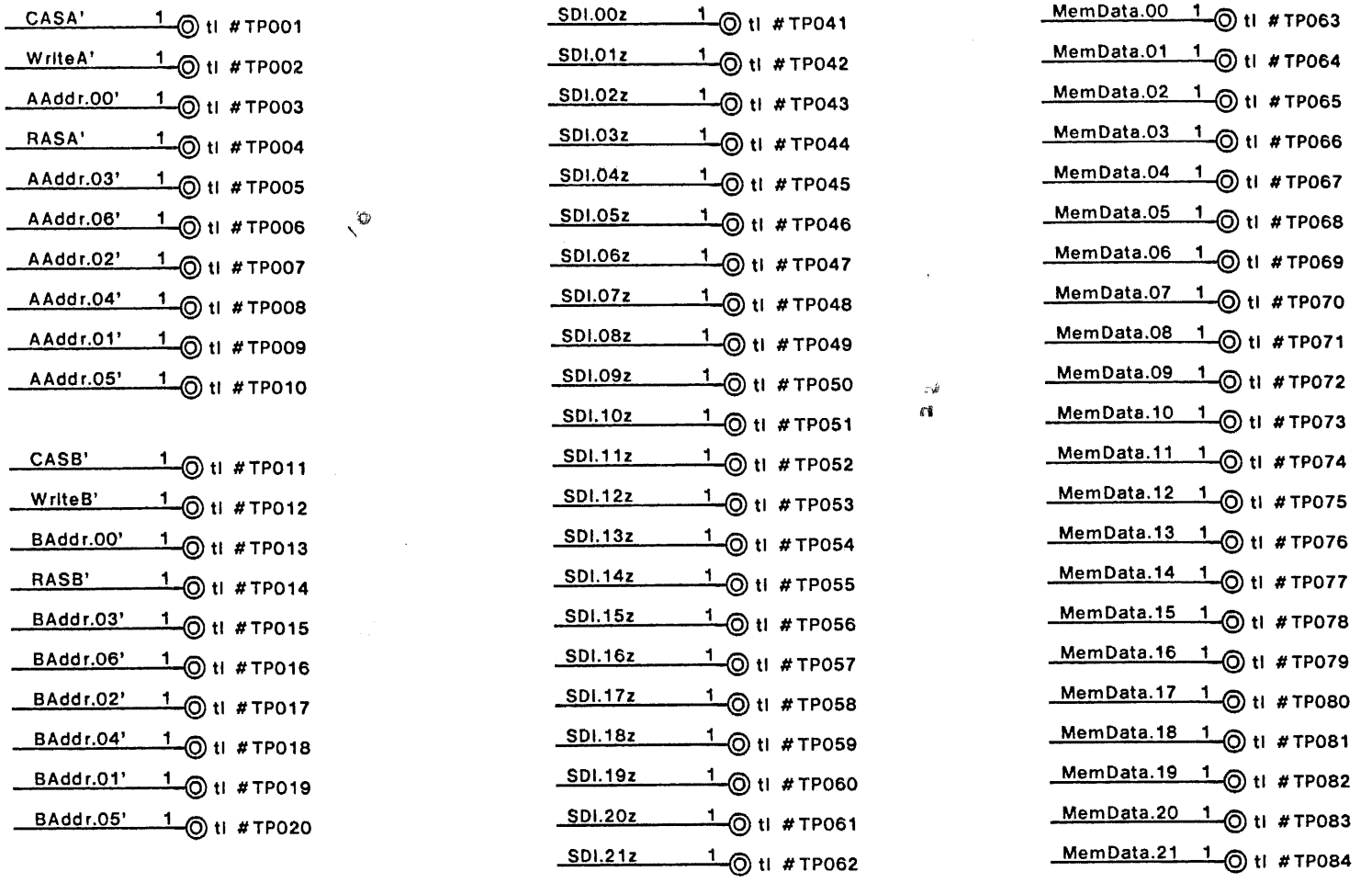
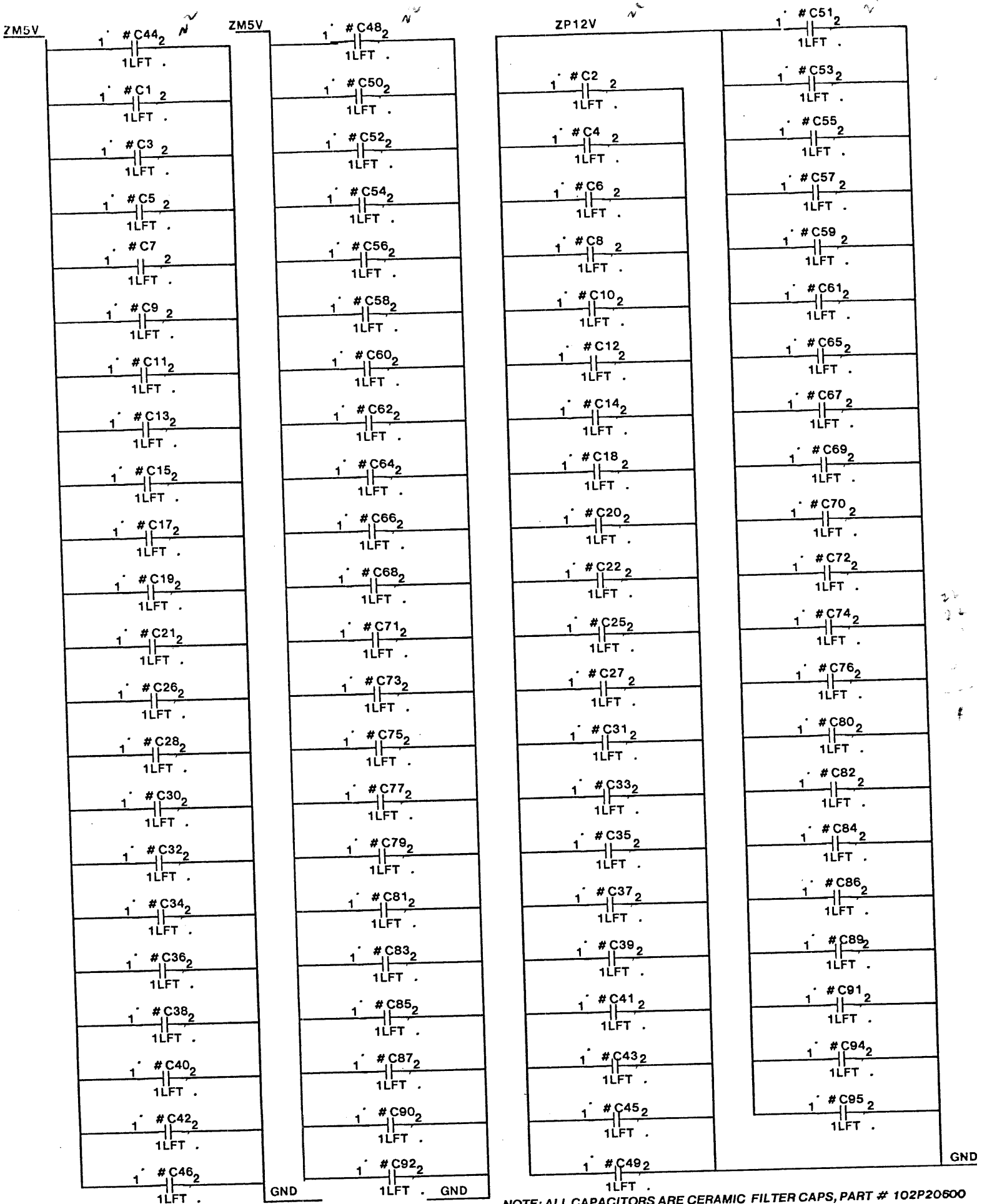
	TITLE SCHEMATIC, MCC		SHEET 16 OF	



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 17 OF	

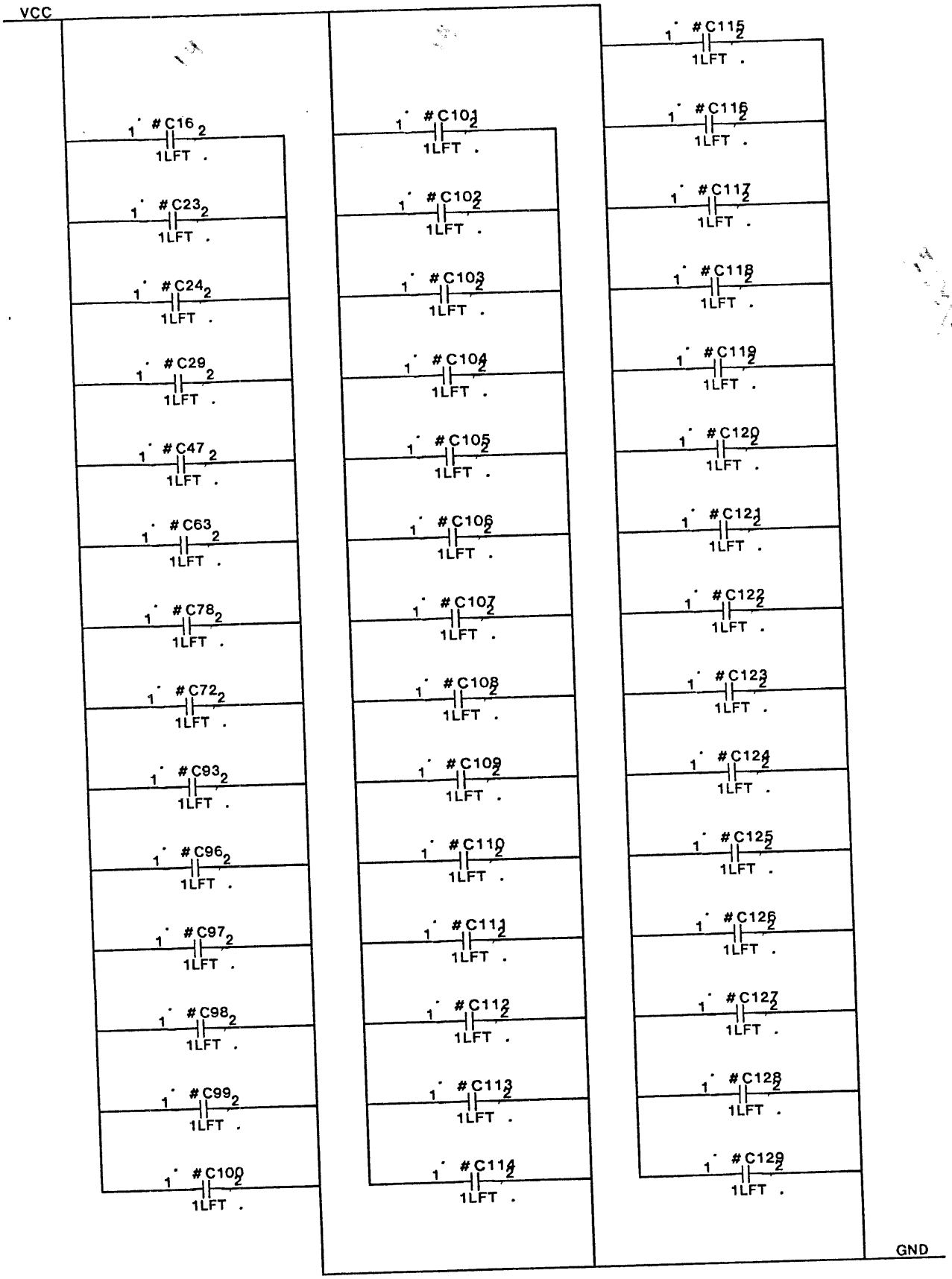


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 18 OF	



NOTE: ALL CAPACITORS ARE CERAMIC FILTER CAPS, PART # 102P20600

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 19 OF	



NOTE: ALL CAPACITORS ARE CERAMIC FILTER CAPS, PART # 102P20600

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11217	SHEET REV. B
	TITLE SCHEMATIC, MCC		SHEET 20 OF	

Comments:

1) *Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299*
2) *The last item on lines below, preceeded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.*
3) *Line with no page number was a continuation of the previous line.*

```
#TP001    .1i  CASA'              ;18
#TP002    .1i  WriteA'            ;18
#TP003    .1i  AAddr.00'          ;18
#TP004    .1i  RASA'              ;18
#TP005    .1i  AAddr.03'          ;18
#TP006    .1i  AAddr.06'          ;18
#TP007    .1i  AAddr.02'          ;18
#TP008    .1i  AAddr.04'          ;18
#TP009    .1i  AAddr.01'          ;18
#TP010    .1i  AAddr.05'          ;18
#TP011    .1i  CASB'              ;18
#TP012    .1i  WriteB'            ;18
#TP013    .1i  BAddr.00'          ;18
#TP014    .1i  RASB'              ;18
#TP015    .1i  BAddr.03'          ;18
#TP016    .1i  BAddr.06'          ;18
#TP017    .1i  BAddr.02'          ;18
#TP018    .1i  BAddr.04'          ;18
#TP019    .1i  BAddr.01'          ;18
#TP020    .1i  BAddr.05'          ;18
#TP021    .1i  CASC'              ;18
#TP022    .1i  WriteC'            ;18
#TP023    .1i  CAddr.00'          ;18
#TP024    .1i  RASC'              ;18
#TP025    .1i  CAddr.03'          ;18
#TP026    .1i  CAddr.06'          ;18
#TP027    .1i  CAddr.02'          ;18
#TP028    .1i  CAddr.04'          ;18
#TP029    .1i  CAddr.01'          ;18
#TP030    .1i  CAddr.05'          ;18
#TP031    .1i  CASD'              ;18
#TP032    .1i  WriteD'            ;18
#TP033    .1i  DAddr.00'          ;18
#TP034    .1i  RASD'              ;18
#TP035    .1i  DAddr.03'          ;18
#TP036    .1i  DAddr.06'          ;18
#TP037    .1i  DAddr.02'          ;18
#TP038    .1i  DAddr.04'          ;18
#TP039    .1i  DAddr.01'          ;18
#TP040    .1i  DAddr.05'          ;18
#TP041    .1i  SDI.00z            ;18
#TP042    .1i  SDI.01z            ;18
#TP043    .1i  SDI.02z            ;18
#TP044    .1i  SDI.03z            ;18
#TP045    .1i  SDI.04z            ;18
#TP046    .1i  SDI.05z            ;18
#TP047    .1i  SDI.06z            ;18
#TP048    .1i  SDI.07z            ;18
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#TP052    .1i  SDI.11z            ;18
#TP053    .1i  SDI.12z            ;18
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#TP058    .1i  SDI.17z            ;18
#TP059    .1i  SDI.18z            ;18
#TP060    .1i  SDI.19z            ;18
#TP061    .1i  SDI.20z            ;18
#TP062    .1i  SDI.21z            ;18
#TP063    .1i  MemData.00         ;18
#TP064    .1i  MemData.01         ;18
#TP065    .1i  MemData.02         ;18
#TP066    .1i  MemData.03         ;18
#TP067    .1i  MemData.04         ;18
#TP068    .1i  MemData.05         ;18
#TP069    .1i  MemData.06         ;18
#TP070    .1i  MemData.07         ;18
#TP071    .1i  MemData.08         ;18
#TP072    .1i  MemData.09         ;18
#TP073    .1i  MemData.10         ;18
#TP074    .1i  MemData.11         ;18
#TP075    .1i  MemData.12         ;18
#TP076    .1i  MemData.13         ;18
#TP077    .1i  MemData.14         ;18
#TP078    .1i  MemData.15         ;18
#TP079    .1i  MemData.16         ;18
#TP080    .1i  MemData.17         ;18
#TP081    .1i  MemData.18         ;18
#TP082    .1i  MemData.19         ;18
#TP083    .1i  MemData.20         ;18
#TP084    .1i  MemData.21         ;18
#TP085    .1i  MCycle             ;18
#TP086    .1i  LatchY.02          ;18
#TP087    .1i  LatchY.03          ;18
#TP088    .1i  LatchY.05          ;18
#TP089    .1i  LatchY.06          ;18
#TP090    .1i  LatchY.07          ;18
#TP091    .1i  LatchY.08          ;18
#TP092    .1i  LatchY.09          ;18
#TP093    .1i  LatchY.10          ;18
#TP094    .1i  LatchY.11          ;18
#TP095    .1i  LatchY.13          ;18
#TP096    .1i  LatchY.14          ;18
#TP097    .1i  LatchY.15          ;18
#TP098    .1i  RFCL               ;18
#TP099    .1i  PullupB            ;18

E001           P12V               ;17
E002           Cycle1'            ;1
```

E003	Cycle2'	;1	E069	DAddr.04	;3
E004	Cycle3'	;1	E070	ZGND	;17
E005	RAS'	;3	E071	DAddr.06	;3
E007	WPulse	;1	E072	DAddr.08	;3
E009	ppClk	;1	E073	DAddr.10	;3
E010	ZGND	;17	E074	DAddr.12	;3
E011	AllowWrite	;1	E075	DAddr.14	;3
E012	Bank0'	;4	E076	DData.00	;12
E015	MapRef	;1	E077	DData.02	;12
E016	Refresh'	;2	E078	DData.04	;12
E017	Wait	;1	E079	DData.06	;12
E018	SDO.00	;12	E080	ZGND	;17
E019	SDO.02	;12	E081	DData.08	;12
E020	ZGND	;17	E082	DData.10	;12
E021	SDO.04	;12	E083	DData.12	;12
E022	SDO.06	;12	E084	DData.14	;12
E023	SDO.08	;12	E085	SDI.20	;10
E024	SDO.10	;12	E086	SDI.18	;10
E025	SDO.12	;12	E087	SDI.16	;10
E026	SDO.14	;12	E088	SDI.14	;10
E027	SDO.16	;12	E089	SDI.12	;10
E028	SDO.18	;12	E090	ZGND	;17
E029	SDO.20	;12	E091	SDI.10	;10
E030	ZGND	;17	E092	SDI.08	;10
E032	SAddr.00	;3	E093	SDI.06	;10
E033	SAddr.02	;3	E094	SDI.04	;10
E034	SAddr.04	;3	E095	SDI.02	;10
E035	SAddr.06	;3	E096	SDI.00	;10
E036	LatchY.01	;2	E100	M5V	;17
E037	Bank1'	;4	E101	P12V	;17
E038	MRef'	;1	E105	LRAS'	;3
E040	ZGND	;17	E106	LCAS	;5
E041	X.00	;14	E110	ZGND	;17
E042	X.02	;14	E113	mem	;1
E043	X.04	;14	E114	←MStatus'	;15
E044	X.06	;14	E115	MCtl←'	;10
E045	X.08	;14	E116	CRefresh'	;1
E046	X.10	;14	E118	SDO.01	;12
E047	X.12	;14	E119	SDO.03	;12
E048	X.14	;14	E120	ZGND	;17
E049	Y.00	;10	E121	SDO.05	;12
E050	P5V	;17	E122	SDO.07	;12
E051	P5V	;17	E123	SDO.09	;12
E052	Y.02	;10	E124	SDO.11	;12
E053	Y.04	;10	E125	SDO.13	;12
E054	Y.06	;10	E126	SDO.15	;12
E055	Y.08	;10	E127	SDO.17	;12
E056	Y.10	;10	E128	SDO.19	;12
E057	Y.12	;10	E129	SDO.21	;12
E058	Y.14	;10	E130	ZGND	;17
E060	ZGND	;17	E132	SAddr.01	;3
E061	YH.2	;2	E133	SAddr.03	;3
E062	YH.4	;2	E134	SAddr.05	;3
E063	YH.6	;2	E136	LatchY.00	;2
E064	Pt.0	;15	E137	Bank2'	;4
E065	Pt.2	;15	E138	Write'	;1
E066	Disp/Proc.'	;4	E140	ZGND	;17
E067	DAddr.00	;4	E141	X.01	;14
E068	DAddr.02	;3	E142	X.03	;14

```
E143            X.05            ;14
E144            X.07            ;14
E145            X.09            ;14
E146            X.11            ;14
E147            X.13            ;14
E148            X.15            ;14
E149            Y.01            ;10
E150            P5V             ;17
E151            P5V             ;17
E152            Y.03            ;10
E153            Y.05            ;10
E154            Y.07            ;10
E155            Y.09            ;10
E156            Y.11            ;10
E157            Y.13            ;10
E158            Y.15            ;10
E160            ZGND            ;17
E161            YH.3            ;2
E162            YH.5            ;2
E163            YH.7            ;2
E164            Pt.1            ;15
E166            MemErr          ;13
E167            DAddr.01        ;4
E168            DAddr.03        ;3
E169            DAddr.05        ;3
E170            ZGND            ;17
E171            DAddr.07        ;3
E172            DAddr.09        ;3
E173            DAddr.11        ;3
E174            DAddr.13        ;3
E175            DAddr.15        ;3
E176            DData.01        ;12
E177            DData.03        ;12
E178            DData.05        ;12
E179            DData.07        ;12
E180            ZGND            ;17
E181            DData.09        ;12
E182            DData.11        ;12
E183            DData.13        ;12
E184            DData.15        ;12
E185            SDI.21          ;10
E186            SDI.19          ;10
E187            SDI.17          ;10
E188            SDI.15          ;10
E189            SDI.13          ;10
E190            ZGND            ;17
E191            SDI.11          ;10
E192            SDI.09          ;10
E193            SDI.07          ;10
E194            SDI.05          ;10
E195            SDI.03          ;10
E196            SDI.01          ;10
E200            M5V             ;17

*01.1:  v07.3o, v02.4i ;1

*01.2:  v19.12o, v02.10i  ;1

*01.3:  v02.11i, v01.11i, v07.6o   ;1
*01.3:  v02.3i

*01.4:  v07.8o, v01.10i   ;1

*01.5:  v13.4o, v13.8i ;1

*01.6:  v01.6o, v23.5i ;1

*02.1:  v08.5o, v09.2i ;2

*02.2:  v08.4o, v09.4i ;2

*02.3:  v08.3o, v09.6i ;2

*02.4:  v08.9o, v09.17i   ;2

*02.5:  v08.10o, v09.15i  ;2

*02.6:  v08.11o, v09.13i  ;2

*02.7:  v08.1i, v08.8o, v09.8i  ;2

*02.8:  v61.10o, v08.13i  ;2

*02.9:  v08.12i, v20.8o, v08.2i ;2

*03.1:  v47.1o, v52.14i, v51.14i   ;3
*03.1:  v50.14i, v49.14i

*03.2:  v47.4o, v43.14i, v57.14i   ;3
*03.2:  v58.14i, v44.14i

*03.3:  v62.6o, v48.1i ;3

*03.4:  v47.3i, v31.6i ;3

*03.5:  v47.6i, v48.6i ;3

*04.10: v21.9o, v10.1i ;4

*04.11: v11.12o, u69.5i   ;4

*04.12: v11.6o, u69.13i   ;4

*04.13: v11.8o, u69.2i ;4

*04.14: v10.12o, u69.10i  ;4

*04.1:  v62.12o, v10.3i, v30.12i   ;4

*04.2:  v62.10o, v10.10i, v30.10i  ;4

*04.3:  v21.7o, v10.13i   ;4

*04.4:  v21.6o, v11.9i ;4

*04.5:  v21.5o, v11.3i ;4
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*04.6: v21.4o, v11.1i ;4

*04.7: v21.12o, v11.13i ;4

*04.8: v21.11o, v11.5i ;4

*04.9: v21.10o, v11.11i ;4

*05.1: u70.4i, u46.17i, u23.2i ;5
*05.1: v62.4o, u93.2i

*05.2: v07.11o, v62.3i ;5

*10.1: v38.2o, v37.13i ;10

*10.2: v38.5o, v36.13i ;10

*10.3: v38.6o, v35.13i ;10

*10.4: v38.9o, v34.13i ;10

*10.5: v38.12o, v33.13i ;10

*10.6: v23.3o, v38.11i ;10

*10.7: v38.15o, v32.13i ;10

*10.8: u94.7o, v23.1i ;10

*13.1: v46.6o, v18.3i ;13

*13.2: v45.6o, v18.4i ;13

*13.3: v29.5o, v18.5i ;13

*13.4: v28.6o, v17.13i ;13

*13.5: v20.6o, v30.5i ;13

*14.10: v15.10o, v41.1i ;14

*14.11: v15.9o, v41.4i ;14

*14.12: v27.12o, v41.9i ;14

*14.13: v27.10o, v41.12i ;14

*14.14: v27.9o, v42.1i ;14

*14.15: v14.14o, v42.4i ;14

*14.16: v16.9o, v42.9i ;14

*14.17: v15.14o, v42.12i ;14

*14.18: v41.3o, v55.2i ;14

*14.19: v41.6o, v55.17i ;14

*14.20: v41.11o, v55.15i ;14

*14.21: v41.8o, v55.4i ;14

*14.22: v42.8o, v55.8i ;14

*14.23: v42.11o, v55.11i ;14

*14.24: v42.6o, v55.13i ;14

*14.25: v42.3o, v55.6i ;14

*14.26: v25.3o, v56.6i ;14

*14.27: v25.6o, v56.13i ;14

*14.28: v25.11o, v56.11i ;14

*14.29: v25.8o, v56.8i ;14

*14.2: v14.15o, v24.1i ;14

*14.30: v24.8o, v56.4i ;14

*14.31: v24.11o, v56.15i ;14

*14.32: v24.6o, v56.17i ;14

*14.33: v24.3o, v56.2i ;14

*14.3: v27.11o, v24.4i ;14

*14.4: v27.13o, v24.9i ;14

*14.5: v27.14o, v24.12i ;14

*14.6: v15.11o, v25.1i ;14

*14.7: v15.13o, v25.4i ;14

*14.8: v16.7o, v25.9i ;14

*14.9: v15.12o, v25.12i ;14

*15.10: v22.12o, u98.12i, u98.11i ;15

*15.11: v22.9o, u99.15i ;15

*15.12: v22.7o, u99.11i, u99.12i ;15

*15.13: v22.10o, u99.2i, u99.3i ;15

*15.14: v12.11o, u99.5i ;15

*15.15: v22.11o, u99.6i ;15

*15.16: v12.12o, u98.10i ;15

*15.17: u98.7o, v00.2i ;15

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 24 OF	B

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*15.18: u98.4o, v00.17i   ;15
*15.19: u98.9o, v00.15i   ;15
*15.1:  v12.15o, u98.5i   ;15
*15.20: u98.13o, v00.4i   ;15
*15.21: u99.13o, v00.8i   ;15
*15.22: u99.9o, v00.11i   ;15
*15.23: u99.4o, v00.13i   ;15
*15.24: u99.7o, v00.6i ;15
*15.2:  v12.14o, u98.1i   ;15
*15.3:  v12.13o, u98.14i  ;15
*15.4:  v12.10o, u99.1i   ;15
*15.5:  v12.9o, u99.14i   ;15
*15.6:  v12.7o, u99.10i   ;15
*15.7:  v22.15o, u98.6i   ;15
*15.8:  v22.14o, u98.3i, u98.2i ;15
*15.9:  v22.13o, u98.15i  ;15

AAddr.00': u22.13i  ;6
AAddr.00': u21.13i  ;6
AAddr.00': u20.13i  ;6
AAddr.00': u19.13i  ;6
AAddr.00': u18.13i  ;6
AAddr.00': u17.13i  ;6
AAddr.00': u16.13i  ;6
AAddr.00': u15.13i  ;6
AAddr.00': u14.13i  ;6
AAddr.00': u13.13i  ;6
AAddr.00': u12.13i  ;6
AAddr.00': u11.13i  ;6
AAddr.00': u10.13i  ;6
AAddr.00': u09.13i  ;6
AAddr.00': u08.13i  ;6
AAddr.00': u07.13i  ;6
AAddr.00': u06.13i  ;6
AAddr.00': u05.13i  ;6
AAddr.00': u04.13i  ;6
AAddr.00': u03.13i  ;6
AAddr.00': u02.13i  ;6
AAddr.00': u01.13i  ;6
AAddr.00': #R4.2i   ;16
AAddr.00': #TP003.1i   ;18

AAddr.00z':   u23.5o   ;5
AAddr.00z':   #R4.1o   ;16

AAddr.01': u22.10i  ;6
AAddr.01': u21.10i  ;6
AAddr.01': u20.10i  ;6
AAddr.01': u19.10i  ;6
AAddr.01': u18.10i  ;6
AAddr.01': u17.10i  ;6
AAddr.01': u16.10i  ;6
AAddr.01': u15.10i  ;6
AAddr.01': u14.10i  ;6
AAddr.01': u13.10i  ;6
AAddr.01': u12.10i  ;6
AAddr.01': u11.10i  ;6
AAddr.01': u10.10i  ;6
AAddr.01': u09.10i  ;6
AAddr.01': u08.10i  ;6
AAddr.01': u07.10i  ;6
AAddr.01': u06.10i  ;6
AAddr.01': u05.10i  ;6
AAddr.01': u04.10i  ;6
AAddr.01': u03.10i  ;6
AAddr.01': u02.10i  ;6
AAddr.01': u01.10i  ;6
AAddr.01': #R10.2i  ;16
AAddr.01': #TP009.1i   ;18

AAddr.01z':   u46.18o  ;5
AAddr.01z':   #R10.1o  ;16

AAddr.02': u22.11i  ;6
AAddr.02': u21.11i  ;6
AAddr.02': u20.11i  ;6
AAddr.02': u19.11i  ;6
AAddr.02': u18.11i  ;6
AAddr.02': u17.11i  ;6
AAddr.02': u16.11i  ;6
AAddr.02': u15.11i  ;6
AAddr.02': u14.11i  ;6
AAddr.02': u13.11i  ;6
AAddr.02': u12.11i  ;6
AAddr.02': u11.11i  ;6
AAddr.02': u10.11i  ;6
AAddr.02': u09.11i  ;6
AAddr.02': u08.11i  ;6
AAddr.02': u07.11i  ;6
AAddr.02': u06.11i  ;6
AAddr.02': u05.11i  ;6
AAddr.02': u04.11i  ;6
AAddr.02': u03.11i  ;6
AAddr.02': u02.11i  ;6
AAddr.02': u01.11i  ;6
AAddr.02': #R8.2i   ;16
AAddr.02': #TP007.1i   ;18

AAddr.02z':   u23.9o   ;5
AAddr.02z':   #R8.1o   ;16

AAddr.03': u22.12i  ;6
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AAddr.03': u21.12i  ;6
AAddr.03': u20.12i  ;6
AAddr.03': u19.12i  ;6
AAddr.03': u18.12i  ;6
AAddr.03': u17.12i  ;6
AAddr.03': u16.12i  ;6
AAddr.03': u15.12i  ;6
AAddr.03': u14.12i  ;6
AAddr.03': u13.12i  ;6
AAddr.03': u12.12i  ;6
AAddr.03': u11.12i  ;6
AAddr.03': u10.12i  ;6
AAddr.03': u09.12i  ;6
AAddr.03': u08.12i  ;6
AAddr.03': u07.12i  ;6
AAddr.03': u06.12i  ;6
AAddr.03': u05.12i  ;6
AAddr.03': u04.12i  ;6
AAddr.03': u03.12i  ;6
AAddr.03': u02.12i  ;6
AAddr.03': u01.12i  ;6
AAddr.03': #R6.2i   ;16
AAddr.03': #TP005.1i   ;18

AAddr.03z':   u23.7o   ;5
AAddr.03z':   #R6.1o   ;16

AAddr.04': u22.6i   ;6
AAddr.04': u21.6i   ;6
AAddr.04': u20.6i   ;6
AAddr.04': u19.6i   ;6
AAddr.04': u18.6i   ;6
AAddr.04': u17.6i   ;6
AAddr.04': u16.6i   ;6
AAddr.04': u15.6i   ;6
AAddr.04': u14.6i   ;6
AAddr.04': u13.6i   ;6
AAddr.04': u12.6i   ;6
AAddr.04': u11.6i   ;6
AAddr.04': u10.6i   ;6
AAddr.04': u09.6i   ;6
AAddr.04': u08.6i   ;6
AAddr.04': u07.6i   ;6
AAddr.04': u06.6i   ;6
AAddr.04': u05.6i   ;6
AAddr.04': u04.6i   ;6
AAddr.04': u03.6i   ;6
AAddr.04': u02.6i   ;6
AAddr.04': u01.6i   ;6
AAddr.04': #R7.2i   ;16
AAddr.04': #TP008.1i   ;18

AAddr.04z':   u23.14o  ;5
AAddr.04z':   #R7.1o   ;16

AAddr.05': u22.7i   ;6
AAddr.05': u21.7i   ;6
AAddr.05': u20.7i   ;6
AAddr.05': u19.7i   ;6
AAddr.05': u18.7i   ;6
AAddr.05': u17.7i   ;6
AAddr.05': u16.7i   ;6
AAddr.05': u15.7i   ;6
AAddr.05': u14.7i   ;6
AAddr.05': u13.7i   ;6
AAddr.05': u12.7i   ;6
AAddr.05': u11.7i   ;6
AAddr.05': u10.7i   ;6
AAddr.05': u09.7i   ;6
AAddr.05': u08.7i   ;6
AAddr.05': u07.7i   ;6
AAddr.05': u06.7i   ;6
AAddr.05': u05.7i   ;6
AAddr.05': u04.7i   ;6
AAddr.05': u03.7i   ;6
AAddr.05': u02.7i   ;6
AAddr.05': u01.7i   ;6
AAddr.05': #R9.2i   ;16
AAddr.05': #TP010.1i   ;18

AAddr.05z':   u23.12o  ;5
AAddr.05z':   #R9.1o   ;16

AAddr.06': u22.5i   ;6
AAddr.06': u21.5i   ;6
AAddr.06': u20.5i   ;6
AAddr.06': u19.5i   ;6
AAddr.06': u18.5i   ;6
AAddr.06': u17.5i   ;6
AAddr.06': u16.5i   ;6
AAddr.06': u15.5i   ;6
AAddr.06': u14.5i   ;6
AAddr.06': u13.5i   ;6
AAddr.06': u12.5i   ;6
AAddr.06': u11.5i   ;6
AAddr.06': u10.5i   ;6
AAddr.06': u09.5i   ;6
AAddr.06': u08.5i   ;6
AAddr.06': u07.5i   ;6
AAddr.06': u06.5i   ;6
AAddr.06': u05.5i   ;6
AAddr.06': u04.5i   ;6
AAddr.06': u03.5i   ;6
AAddr.06': u02.5i   ;6
AAddr.06': u01.5i   ;6
AAddr.06': #R5.2i   ;16
AAddr.06': #TP006.1i   ;18

AAddr.06z':   u23.16o  ;5
AAddr.06z':   #R5.1o   ;16

AllowWrite:   E11, v19.9i ;1

BAddr.00': u26.13i  ;7
BAddr.00': u30.13i  ;7
BAddr.00': u34.13i  ;7
BAddr.00': u38.13i  ;7
BAddr.00': u42.13i  ;7
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BAddr.00': u24.13i  ;7
BAddr.00': u25.13i  ;7
BAddr.00': u43.13i  ;7
BAddr.00': u39.13i  ;7
BAddr.00': u35.13i  ;7
BAddr.00': u31.13i  ;7
BAddr.00': u27.13i  ;7
BAddr.00': u28.13i  ;7
BAddr.00': u32.13i  ;7
BAddr.00': u36.13i  ;7
BAddr.00': u40.13i  ;7
BAddr.00': u44.13i  ;7
BAddr.00': u45.13i  ;7
BAddr.00': u41.13i  ;7
BAddr.00': u37.13i  ;7
BAddr.00': u33.13i  ;7
BAddr.00': u29.13i  ;7
BAddr.00': #R14.2i  ;16
BAddr.00': #TP013.1i   ;18

BAddr.00z':   u46.5o   ;5
BAddr.00z':   #R14.1o  ;16

BAddr.01': u26.10i  ;7
BAddr.01': u30.10i  ;7
BAddr.01': u34.10i  ;7
BAddr.01': u38.10i  ;7
BAddr.01': u42.10i  ;7
BAddr.01': u24.10i  ;7
BAddr.01': u25.10i  ;7
BAddr.01': u43.10i  ;7
BAddr.01': u39.10i  ;7
BAddr.01': u35.10i  ;7
BAddr.01': u31.10i  ;7
BAddr.01': u27.10i  ;7
BAddr.01': u28.10i  ;7
BAddr.01': u32.10i  ;7
BAddr.01': u36.10i  ;7
BAddr.01': u40.10i  ;7
BAddr.01': u44.10i  ;7
BAddr.01': u45.10i  ;7
BAddr.01': u41.10i  ;7
BAddr.01': u37.10i  ;7
BAddr.01': u33.10i  ;7
BAddr.01': u29.10i  ;7
BAddr.01': #R20.2i  ;16
BAddr.01': #TP019.1i   ;18

BAddr.01z':   u70.3o   ;5
BAddr.01z':   #R20.1o  ;16

BAddr.02': u26.11i  ;7
BAddr.02': u30.11i  ;7
BAddr.02': u34.11i  ;7
BAddr.02': u38.11i  ;7
BAddr.02': u42.11i  ;7
BAddr.02': u24.11i  ;7
BAddr.02': u25.11i  ;7
BAddr.02': u43.11i  ;7

BAddr.02': u39.11i  ;7
BAddr.02': u35.11i  ;7
BAddr.02': u31.11i  ;7
BAddr.02': u27.11i  ;7
BAddr.02': u28.11i  ;7
BAddr.02': u32.11i  ;7
BAddr.02': u36.11i  ;7
BAddr.02': u40.11i  ;7
BAddr.02': u44.11i  ;7
BAddr.02': u45.11i  ;7
BAddr.02': u41.11i  ;7
BAddr.02': u37.11i  ;7
BAddr.02': u33.11i  ;7
BAddr.02': u29.11i  ;7
BAddr.02': #R18.2i  ;16
BAddr.02': #TP017.1i   ;18

BAddr.02z':   u46.9o   ;5
BAddr.02z':   #R18.1o  ;16

BAddr.03': u26.12i  ;7
BAddr.03': u30.12i  ;7
BAddr.03': u34.12i  ;7
BAddr.03': u38.12i  ;7
BAddr.03': u42.12i  ;7
BAddr.03': u24.12i  ;7
BAddr.03': u25.12i  ;7
BAddr.03': u43.12i  ;7
BAddr.03': u39.12i  ;7
BAddr.03': u35.12i  ;7
BAddr.03': u31.12i  ;7
BAddr.03': u27.12i  ;7
BAddr.03': u28.12i  ;7
BAddr.03': u32.12i  ;7
BAddr.03': u36.12i  ;7
BAddr.03': u40.12i  ;7
BAddr.03': u44.12i  ;7
BAddr.03': u45.12i  ;7
BAddr.03': u41.12i  ;7
BAddr.03': u37.12i  ;7
BAddr.03': u33.12i  ;7
BAddr.03': u29.12i  ;7
BAddr.03': #R16.2i  ;16
BAddr.03': #TP015.1i   ;18

BAddr.03z':   u46.7o   ;5
BAddr.03z':   #R16.1o  ;16

BAddr.04': u26.6i   ;7
BAddr.04': u30.6i   ;7
BAddr.04': u34.6i   ;7
BAddr.04': u38.6i   ;7
BAddr.04': u42.6i   ;7
BAddr.04': u24.6i   ;7
BAddr.04': u25.6i   ;7
BAddr.04': u43.6i   ;7
BAddr.04': u39.6i   ;7
BAddr.04': u35.6i   ;7
BAddr.04': u31.6i   ;7
```

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 27 OF	B

```
BAddr.04': u27.6i   ;7
BAddr.04': u28.6i   ;7
BAddr.04': u32.6i   ;7
BAddr.04': u36.6i   ;7
BAddr.04': u40.6i   ;7
BAddr.04': u44.6i   ;7
BAddr.04': u45.6i   ;7
BAddr.04': u41.6i   ;7
BAddr.04': u37.6i   ;7
BAddr.04': u33.6i   ;7
BAddr.04': u29.6i   ;7
BAddr.04': #R17.2i  ;16
BAddr.04': #TP018.1i   ;18

BAddr.04z':   u46.12o  ;5
BAddr.04z':   #R17.1o  ;16

BAddr.05': u26.7i   ;7
BAddr.05': u30.7i   ;7
BAddr.05': u34.7i   ;7
BAddr.05': u38.7i   ;7
BAddr.05': u42.7i   ;7
BAddr.05': u24.7i   ;7
BAddr.05': u25.7i   ;7
BAddr.05': u43.7i   ;7
BAddr.05': u39.7i   ;7
BAddr.05': u35.7i   ;7
BAddr.05': u31.7i   ;7
BAddr.05': u27.7i   ;7
BAddr.05': u28.7i   ;7
BAddr.05': u32.7i   ;7
BAddr.05': u36.7i   ;7
BAddr.05': u40.7i   ;7
BAddr.05': u44.7i   ;7
BAddr.05': u45.7i   ;7
BAddr.05': u41.7i   ;7
BAddr.05': u37.7i   ;7
BAddr.05': u33.7i   ;7
BAddr.05': u29.7i   ;7
BAddr.05': #R19.2i  ;16
BAddr.05': #TP020.1i   ;18

BAddr.05z':   u70.18o  ;5
BAddr.05z':   #R19.1o  ;16

BAddr.06': u26.5i   ;7
BAddr.06': u30.5i   ;7
BAddr.06': u34.5i   ;7
BAddr.06': u38.5i   ;7
BAddr.06': u42.5i   ;7
BAddr.06': u24.5i   ;7
BAddr.06': u25.5i   ;7
BAddr.06': u43.5i   ;7
BAddr.06': u39.5i   ;7
BAddr.06': u35.5i   ;7
BAddr.06': u31.5i   ;7
BAddr.06': u27.5i   ;7
BAddr.06': u28.5i   ;7
BAddr.06': u32.5i   ;7
BAddr.06': u36.5i   ;7
BAddr.06': u40.5i   ;7
BAddr.06': u44.5i   ;7
BAddr.06': u45.5i   ;7
BAddr.06': u41.5i   ;7
BAddr.06': u37.5i   ;7
BAddr.06': u33.5i   ;7
BAddr.06': u29.5i   ;7
BAddr.06': #R15.2i  ;16
BAddr.06': #TP016.1i   ;18

BAddr.06z':   u46.14o  ;5
BAddr.06z':   #R15.1o  ;16

Bank0': v61.3i   ;1
Bank0': v21.1i, v30.8o, E12  ;4
Bank0': v04.1i, v06.1i, v05.1i  ;12
Bank0': u94.8i

Bank0:  v06.19i, v05.19i, u94.12o  ;12
Bank0:  v04.19i

Bank1': v10.8o, E37 ;4

Bank2': v10.6o, E137   ;4

CAddr.00': u49.13i  ;8
CAddr.00': u53.13i  ;8
CAddr.00': u57.13i  ;8
CAddr.00': u61.13i  ;8
CAddr.00': u65.13i  ;8
CAddr.00': u50.13i  ;8
CAddr.00': u54.13i  ;8
CAddr.00': u58.13i  ;8
CAddr.00': u62.13i  ;8
CAddr.00': u66.13i  ;8
CAddr.00': u67.13i  ;8
CAddr.00': u63.13i  ;8
CAddr.00': u59.13i  ;8
CAddr.00': u55.13i  ;8
CAddr.00': u51.13i  ;8
CAddr.00': u47.13i  ;8
CAddr.00': u48.13i  ;8
CAddr.00': u52.13i  ;8
CAddr.00': u56.13i  ;8
CAddr.00': u60.13i  ;8
CAddr.00': u64.13i  ;8
CAddr.00': u68.13i  ;8
CAddr.00': #R24.2i  ;16
CAddr.00': #TP023.1i   ;18

CAddr.00z':   u70.7o   ;5
CAddr.00z':   #R24.1o  ;16

CAddr.01': u49.10i  ;8
CAddr.01': u53.10i  ;8
CAddr.01': u57.10i  ;8
CAddr.01': u61.10i  ;8
CAddr.01': u65.10i  ;8
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```
CAddr.01': u66.10i  ;8
CAddr.01': u62.10i  ;8
CAddr.01': u58.10i  ;8
CAddr.01': u54.10i  ;8
CAddr.01': u50.10i  ;8
CAddr.01': u47.10i  ;8
CAddr.01': u51.10i  ;8
CAddr.01': u55.10i  ;8
CAddr.01': u59.10i  ;8
CAddr.01': u63.10i  ;8
CAddr.01': u67.10i  ;8
CAddr.01': u68.10i  ;8
CAddr.01': u64.10i  ;8
CAddr.01': u60.10i  ;8
CAddr.01': u56.10i  ;8
CAddr.01': u52.10i  ;8
CAddr.01': u48.10i  ;8
CAddr.01': #R30.2i  ;16
CAddr.01': #TP029.1i   ;18

CAddr.01z':   u94.16o  ;5
CAddr.01z':   #R30.1o  ;16

CAddr.02': u49.11i  ;8
CAddr.02': u53.11i  ;8
CAddr.02': u57.11i  ;8
CAddr.02': u61.11i  ;8
CAddr.02': u65.11i  ;8
CAddr.02': u66.11i  ;8
CAddr.02': u62.11i  ;8
CAddr.02': u58.11i  ;8
CAddr.02': u54.11i  ;8
CAddr.02': u50.11i  ;8
CAddr.02': u47.11i  ;8
CAddr.02': u51.11i  ;8
CAddr.02': u55.11i  ;8
CAddr.02': u59.11i  ;8
CAddr.02': u63.11i  ;8
CAddr.02': u67.11i  ;8
CAddr.02': u68.11i  ;8
CAddr.02': u64.11i  ;8
CAddr.02': u60.11i  ;8
CAddr.02': u56.11i  ;8
CAddr.02': u52.11i  ;8
CAddr.02': u48.11i  ;8
CAddr.02': #R28.2i  ;16
CAddr.02': #TP027.1i   ;18

CAddr.02z':   u94.18o  ;5
CAddr.02z':   #R28.1o  ;16

CAddr.03': u49.12i  ;8
CAddr.03': u53.12i  ;8
CAddr.03': u57.12i  ;8
CAddr.03': u61.12i  ;8
CAddr.03': u65.12i  ;8
CAddr.03': u66.12i  ;8
CAddr.03': u62.12i  ;8
CAddr.03': u58.12i  ;8
CAddr.03': u54.12i  ;8
CAddr.03': u50.12i  ;8
CAddr.03': u47.12i  ;8
CAddr.03': u51.12i  ;8
CAddr.03': u55.12i  ;8
CAddr.03': u59.12i  ;8
CAddr.03': u63.12i  ;8
CAddr.03': u67.12i  ;8
CAddr.03': u68.12i  ;8
CAddr.03': u64.12i  ;8
CAddr.03': u60.12i  ;8
CAddr.03': u56.12i  ;8
CAddr.03': u52.12i  ;8
CAddr.03': u48.12i  ;8
CAddr.03': #R26.2i  ;16
CAddr.03': #TP025.1i   ;18

CAddr.03z':   u70.9o   ;5
CAddr.03z':   #R26.1o  ;16

CAddr.04': u49.6i   ;8
CAddr.04': u53.6i   ;8
CAddr.04': u57.6i   ;8
CAddr.04': u61.6i   ;8
CAddr.04': u65.6i   ;8
CAddr.04': u66.6i   ;8
CAddr.04': u62.6i   ;8
CAddr.04': u58.6i   ;8
CAddr.04': u54.6i   ;8
CAddr.04': u50.6i   ;8
CAddr.04': u47.6i   ;8
CAddr.04': u51.6i   ;8
CAddr.04': u55.6i   ;8
CAddr.04': u59.6i   ;8
CAddr.04': u63.6i   ;8
CAddr.04': u67.6i   ;8
CAddr.04': u68.6i   ;8
CAddr.04': u64.6i   ;8
CAddr.04': u60.6i   ;8
CAddr.04': u56.6i   ;8
CAddr.04': u52.6i   ;8
CAddr.04': u48.6i   ;8
CAddr.04': #R27.2i  ;16
CAddr.04': #TP028.1i   ;18

CAddr.04z':   u70.12o  ;5
CAddr.04z':   #R27.1o  ;16

CAddr.05': u49.7i   ;8
CAddr.05': u53.7i   ;8
CAddr.05': u57.7i   ;8
CAddr.05': u61.7i   ;8
CAddr.05': u65.7i   ;8
CAddr.05': u66.7i   ;8
CAddr.05': u62.7i   ;8
CAddr.05': u58.7i   ;8
CAddr.05': u54.7i   ;8
CAddr.05': u50.7i   ;8
CAddr.05': u47.7i   ;8
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CAddr.05': u51.7i   ;8
CAddr.05': u55.7i   ;8
CAddr.05': u59.7i   ;8
CAddr.05': u63.7i   ;8
CAddr.05': u67.7i   ;8
CAddr.05': u68.7i   ;8
CAddr.05': u64.7i   ;8
CAddr.05': u60.7i   ;8
CAddr.05': u56.7i   ;8
CAddr.05': u52.7i   ;8
CAddr.05': u48.7i   ;8
CAddr.05': #R29.2i  ;16
CAddr.05': #TP030.1i   ;18

CAddr.05z':   u94.3o   ;5
CAddr.05z':   #R29.1o  ;16

CAddr.06': u49.5i   ;8
CAddr.06': u53.5i   ;8
CAddr.06': u57.5i   ;8
CAddr.06': u61.5i   ;8
CAddr.06': u65.5i   ;8
CAddr.06': u66.5i   ;8
CAddr.06': u62.5i   ;8
CAddr.06': u58.5i   ;8
CAddr.06': u54.5i   ;8
CAddr.06': u50.5i   ;8
CAddr.06': u47.5i   ;8
CAddr.06': u51.5i   ;8
CAddr.06': u55.5i   ;8
CAddr.06': u59.5i   ;8
CAddr.06': u63.5i   ;8
CAddr.06': u67.5i   ;8
CAddr.06': u68.5i   ;8
CAddr.06': u64.5i   ;8
CAddr.06': u60.5i   ;8
CAddr.06': u56.5i   ;8
CAddr.06': u52.5i   ;8
CAddr.06': u48.5i   ;8
CAddr.06': #R25.2i  ;16
CAddr.06': #TP026.1i   ;18

CAddr.06z':   u70.14o  ;5
CAddr.06z':   #R25.1o  ;16

CASA':  u22.15i  ;6
CASA':  u21.15i  ;6
CASA':  u20.15i  ;6
CASA':  u19.15i  ;6
CASA':  u18.15i  ;6
CASA':  u17.15i  ;6
CASA':  u16.15i  ;6
CASA':  u15.15i  ;6
CASA':  u14.15i  ;6
CASA':  u13.15i  ;6
CASA':  u12.15i  ;6
CASA':  u11.15i  ;6
CASA':  u10.15i  ;6
CASA':  u09.15i  ;6

CASA':  u08.15i  ;6
CASA':  u07.15i  ;6
CASA':  u06.15i  ;6
CASA':  u05.15i  ;6
CASA':  u04.15i  ;6
CASA':  u03.15i  ;6
CASA':  u02.15i  ;6
CASA':  u01.15i  ;6
CASA':  #R1.2i   ;16
CASA':  #TP001.1i   ;18

CASAz': u23.18o  ;5
CASAz': #R1.1o   ;16

CASB':  u44.15i  ;7
CASB':  u45.15i  ;7
CASB':  u43.15i  ;7
CASB':  u42.15i  ;7
CASB':  u38.15i  ;7
CASB':  u39.15i  ;7
CASB':  u41.15i  ;7
CASB':  u40.15i  ;7
CASB':  u36.15i  ;7
CASB':  u37.15i  ;7
CASB':  u35.15i  ;7
CASB':  u34.15i  ;7
CASB':  u30.15i  ;7
CASB':  u31.15i  ;7
CASB':  u33.15i  ;7
CASB':  u32.15i  ;7
CASB':  u28.15i  ;7
CASB':  u29.15i  ;7
CASB':  u27.15i  ;7
CASB':  u26.15i  ;7
CASB':  u25.15i  ;7
CASB':  u24.15i  ;7
CASB':  #R11.2i  ;16
CASB':  #TP011.1i   ;18

CASBz': u46.3o   ;5
CASBz': #R11.1o  ;16

CASC':  u68.15i  ;8
CASC':  u64.15i  ;8
CASC':  u60.15i  ;8
CASC':  u56.15i  ;8
CASC':  u52.15i  ;8
CASC':  u48.15i  ;8
CASC':  u47.15i  ;8
CASC':  u51.15i  ;8
CASC':  u55.15i  ;8
CASC':  u59.15i  ;8
CASC':  u63.15i  ;8
CASC':  u67.15i  ;8
CASC':  u66.15i  ;8
CASC':  u62.15i  ;8
CASC':  u58.15i  ;8
CASC':  u54.15i  ;8
CASC':  u50.15i  ;8
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```
CASC':  u49.15i  ;8
CASC':  u53.15i  ;8
CASC':  u57.15i  ;8
CASC':  u61.15i  ;8
CASC':  u65.15i  ;8
CASC':  #R21.2i  ;16
CASC':  #TP021.1i   ;18

CASCz': u70.16o  ;5
CASCz': #R21.1o  ;16

CASD':  u92.15i  ;9
CASD':  u91.15i  ;9
CASD':  u90.15i  ;9
CASD':  u89.15i  ;9
CASD':  u85.15i  ;9
CASD':  u86.15i  ;9
CASD':  u87.15i  ;9
CASD':  u88.15i  ;9
CASD':  u84.15i  ;9
CASD':  u83.15i  ;9
CASD':  u82.15i  ;9
CASD':  u81.15i  ;9
CASD':  u77.15i  ;9
CASD':  u78.15i  ;9
CASD':  u79.15i  ;9
CASD':  u80.15i  ;9
CASD':  u76.15i  ;9
CASD':  u75.15i  ;9
CASD':  u74.15i  ;9
CASD':  u73.15i  ;9
CASD':  u71.15i  ;9
CASD':  u72.15i  ;9
CASD':  #R31.2i  ;16
CASD':  #TP031.1i   ;18

CASDz': u93.18o  ;5
CASDz': #R31.1o  ;16

CasLatch:  v53.11i, v54.11i  ;2
CasLatch:  v47.13o  ;3

Clk:    v01.3i   ;1
Clk:    v62.2o   ;1
Clk:    v22.4i   ;15

CRefresh': v02.8o, E116   ;1
CRefresh': v61.8i   ;2
CRefresh': v11.10i, v11.4i, v11.2i ;4
CRefresh': v10.2i
CRefresh': v07.13i  ;5

CRefresh:  v02.9o   ;1
CRefresh:  v47.2i, v47.5i ;3

Cycle1':   E2, v13.9i  ;1

Cycle2':   E3, v47.8i  ;1
Cycle2':   v61.9i   ;2

Cycle2: v47.10o, v19.10i  ;1

Cycle3':   E4, u94.6i  ;1

Cycle3: v07.4i, u94.14o   ;1
Cycle3: v19.4i   ;1
Cycle3: v23.10i  ;1

DAddr.00': u73.13i  ;9
DAddr.00': u77.13i  ;9
DAddr.00': u81.13i  ;9
DAddr.00': u85.13i  ;9
DAddr.00': u89.13i  ;9
DAddr.00': u71.13i  ;9
DAddr.00': u72.13i  ;9
DAddr.00': u90.13i  ;9
DAddr.00': u86.13i  ;9
DAddr.00': u82.13i  ;9
DAddr.00': u78.13i  ;9
DAddr.00': u74.13i  ;9
DAddr.00': u75.13i  ;9
DAddr.00': u79.13i  ;9
DAddr.00': u83.13i  ;9
DAddr.00': u87.13i  ;9
DAddr.00': u91.13i  ;9
DAddr.00': u92.13i  ;9
DAddr.00': u88.13i  ;9
DAddr.00': u84.13i  ;9
DAddr.00': u80.13i  ;9
DAddr.00': u76.13i  ;9
DAddr.00': #R34.2i  ;16
DAddr.00': #TP033.1i   ;18

DAddr.00:  E67, v21.13i   ;4

DAddr.00z':   u93.16o  ;5
DAddr.00z':   #R34.1o  ;16

DAddr.01': u73.10i  ;9
DAddr.01': u77.10i  ;9
DAddr.01': u81.10i  ;9
DAddr.01': u85.10i  ;9
DAddr.01': u89.10i  ;9
DAddr.01': u71.10i  ;9
DAddr.01': u72.10i  ;9
DAddr.01': u90.10i  ;9
DAddr.01': u86.10i  ;9
DAddr.01': u82.10i  ;9
DAddr.01': u78.10i  ;9
DAddr.01': u74.10i  ;9
DAddr.01': u75.10i  ;9
DAddr.01': u79.10i  ;9
DAddr.01': u83.10i  ;9
DAddr.01': u87.10i  ;9
DAddr.01': u91.10i  ;9
DAddr.01': u92.10i  ;9
DAddr.01': u88.10i  ;9
DAddr.01': u84.10i  ;9
```

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 31 OF	B

```
DAddr.01': u80.10i  ;9
DAddr.01': u76.10i  ;9
DAddr.01': #R40.2i  ;16
DAddr.01': #TP039.1i   ;18

DAddr.01:  E167, v21.14i  ;4

DAddr.01z':   u93.12o  ;5
DAddr.01z':   #R40.1o  ;16

DAddr.02': u73.11i  ;9
DAddr.02': u77.11i  ;9
DAddr.02': u81.11i  ;9
DAddr.02': u85.11i  ;9
DAddr.02': u89.11i  ;9
DAddr.02': u71.11i  ;9
DAddr.02': u72.11i  ;9
DAddr.02': u90.11i  ;9
DAddr.02': u86.11i  ;9
DAddr.02': u82.11i  ;9
DAddr.02': u78.11i  ;9
DAddr.02': u74.11i  ;9
DAddr.02': u75.11i  ;9
DAddr.02': u79.11i  ;9
DAddr.02': u83.11i  ;9
DAddr.02': u87.11i  ;9
DAddr.02': u91.11i  ;9
DAddr.02': u92.11i  ;9
DAddr.02': u88.11i  ;9
DAddr.02': u84.11i  ;9
DAddr.02': u80.11i  ;9
DAddr.02': u76.11i  ;9
DAddr.02': #R38.2i  ;16
DAddr.02': #TP037.1i   ;18

DAddr.02:  E68, v49.3i ;3

DAddr.02z':   u94.9o   ;5
DAddr.02z':   #R38.1o  ;16

DAddr.03': u73.12i  ;9
DAddr.03': u77.12i  ;9
DAddr.03': u81.12i  ;9
DAddr.03': u85.12i  ;9
DAddr.03': u89.12i  ;9
DAddr.03': u71.12i  ;9
DAddr.03': u72.12i  ;9
DAddr.03': u90.12i  ;9
DAddr.03': u86.12i  ;9
DAddr.03': u82.12i  ;9
DAddr.03': u78.12i  ;9
DAddr.03': u74.12i  ;9
DAddr.03': u75.12i  ;9
DAddr.03': u79.12i  ;9
DAddr.03': u83.12i  ;9
DAddr.03': u87.12i  ;9
DAddr.03': u91.12i  ;9
DAddr.03': u92.12i  ;9
DAddr.03': u88.12i  ;9
DAddr.03': u84.12i  ;9
DAddr.03': u80.12i  ;9
DAddr.03': u76.12i  ;9
DAddr.03': #R36.2i  ;16
DAddr.03': #TP035.1i   ;18

DAddr.03:  E168, v49.13i  ;3

DAddr.03z':   u93.14o  ;5
DAddr.03z':   #R36.1o  ;16

DAddr.04': u73.6i   ;9
DAddr.04': u77.6i   ;9
DAddr.04': u81.6i   ;9
DAddr.04': u85.6i   ;9
DAddr.04': u89.6i   ;9
DAddr.04': u71.6i   ;9
DAddr.04': u72.6i   ;9
DAddr.04': u90.6i   ;9
DAddr.04': u86.6i   ;9
DAddr.04': u82.6i   ;9
DAddr.04': u78.6i   ;9
DAddr.04': u74.6i   ;9
DAddr.04': u75.6i   ;9
DAddr.04': u79.6i   ;9
DAddr.04': u83.6i   ;9
DAddr.04': u87.6i   ;9
DAddr.04': u91.6i   ;9
DAddr.04': u92.6i   ;9
DAddr.04': u88.6i   ;9
DAddr.04': u84.6i   ;9
DAddr.04': u80.6i   ;9
DAddr.04': u76.6i   ;9
DAddr.04': #R37.2i  ;16
DAddr.04': #TP038.1i   ;18

DAddr.04:  E69, v50.3i ;3

DAddr.04z':   u93.7o   ;5
DAddr.04z':   #R37.1o  ;16

DAddr.05': u73.7i   ;9
DAddr.05': u77.7i   ;9
DAddr.05': u81.7i   ;9
DAddr.05': u85.7i   ;9
DAddr.05': u89.7i   ;9
DAddr.05': u71.7i   ;9
DAddr.05': u72.7i   ;9
DAddr.05': u90.7i   ;9
DAddr.05': u86.7i   ;9
DAddr.05': u82.7i   ;9
DAddr.05': u78.7i   ;9
DAddr.05': u74.7i   ;9
DAddr.05': u75.7i   ;9
DAddr.05': u79.7i   ;9
DAddr.05': u83.7i   ;9
DAddr.05': u87.7i   ;9
DAddr.05': u91.7i   ;9
DAddr.05': u92.7i   ;9
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```
DAddr.05': u88.7i   ;9
DAddr.05': u84.7i   ;9
DAddr.05': u80.7i   ;9
DAddr.05': u76.7i   ;9
DAddr.05': #R39.2i  ;16
DAddr.05': #TP040.1i   ;18

DAddr.05:  E169, v50.13i  ;3

DAddr.05z':   u93.9o   ;5
DAddr.05z':   #R39.1o  ;16

DAddr.06': u73.5i   ;9
DAddr.06': u77.5i   ;9
DAddr.06': u81.5i   ;9
DAddr.06': u85.5i   ;9
DAddr.06': u89.5i   ;9
DAddr.06': u71.5i   ;9
DAddr.06': u72.5i   ;9
DAddr.06': u90.5i   ;9
DAddr.06': u86.5i   ;9
DAddr.06': u82.5i   ;9
DAddr.06': u78.5i   ;9
DAddr.06': u74.5i   ;9
DAddr.06': u75.5i   ;9
DAddr.06': u79.5i   ;9
DAddr.06': u83.5i   ;9
DAddr.06': u87.5i   ;9
DAddr.06': u91.5i   ;9
DAddr.06': u92.5i   ;9
DAddr.06': u88.5i   ;9
DAddr.06': u84.5i   ;9
DAddr.06': u80.5i   ;9
DAddr.06': u76.5i   ;9
DAddr.06': #R35.2i  ;16
DAddr.06': #TP036.1i   ;18

DAddr.06:  E71, v51.3i ;3

DAddr.06z':   u93.5o   ;5
DAddr.06z':   #R35.1o  ;16

DAddr.07:  E171, v51.13i  ;3

DAddr.08:  E72, v49.4i ;3

DAddr.09:  E172, v49.12i  ;3

DAddr.10:  E73, v50.4i ;3

DAddr.11:  E173, v50.12i  ;3

DAddr.12:  E74, v52.3i ;3

DAddr.13:  E174, v51.4i   ;3

DAddr.14:  E75, v51.12i   ;3

DAddr.15:  E175, v52.4i   ;3

DData.00:  u95.18o, E76   ;12

DData.01:  u95.16o, E176  ;12

DData.02:  u95.14o, E77   ;12

DData.03:  u95.12o, E177  ;12

DData.04:  u95.3o, E78 ;12

DData.05:  u95.5o, E178   ;12

DData.06:  u95.7o, E79 ;12

DData.07:  u95.9o, E179   ;12

DData.08:  u96.18o, E81   ;12

DData.09:  u96.16o, E181  ;12

DData.10:  u96.14o, E82   ;12

DData.11:  u96.12o, E182  ;12

DData.12:  u96.3o, E83 ;12

DData.13:  u96.5o, E183   ;12

DData.14:  u96.7o, E84 ;12

DData.15:  u96.9o, E184   ;12

Disp/Proc.'': v19.13i  ;1
Disp/Proc.'': v30.9i, v13.13o   ;4
Disp/Proc.'': v21.15i

Disp/Proc.':  v51.2i, v50.2i ;3
Disp/Proc.':  v49.2i, v52.2i
Disp/Proc.':  E66, v13.11i   ;4

DLY5:   v47.11i, v48.12o  ;3

GND:    v02.2i   ;1
GND:    v02.12i  ;1
GND:    v47.9i   ;1
GND:    v13.6i   ;1
GND:    v01.12i  ;1
GND:    v54.1i   ;2
GND:    v43.1i, v57.15i, v57.1i ;3
GND:    v58.15i, v58.1i, v44.15i
GND:    v44.1i, v52.15i, v52.1i
GND:    v51.15i, v51.1i, v50.15i
GND:    v50.1i, v49.15i, v49.1i
GND:    v43.15i
GND:    v47.12i  ;3
GND:    v13.12i  ;4
GND:    u94.1i   ;5
GND:    u94.19i  ;5
```

```
GND:    u23.1i   ;5
GND:    u23.19i  ;5
GND:    u46.19i  ;5
GND:    u46.1i   ;5
GND:    u93.1i   ;5
GND:    u93.19i  ;5
GND:    u70.19i  ;5
GND:    u70.1i   ;5
GND:    v38.1i   ;10
GND:    v39.1i   ;10
GND:    v40.1i   ;10
GND:    u95.1i, u96.1i ;12
GND:    v28.13i  ;13
GND:    v28.12i  ;13
GND:    v28.11i  ;13
GND:    u97.16i  ;16
GND:    v03.16i  ;16
GND:    #C46.2o, #C42.2o, #C40.2o  ;19
GND:    #C38.2o, #C36.2o, #C34.2o
GND:    #C32.2o, #C30.2o, #C28.2o
GND:    #C26.2o, #C21.2o, #C19.2o
GND:    #C17.2o, #C15.2o, #C13.2o
GND:    #C11.2o, #C9.2o, #C7.2o
GND:    #C5.2o, #C3.2o, #C1.2o
GND:    #C44.2o
GND:    #C92.2o, #C90.2o, #C87.2o  ;19
GND:    #C85.2o, #C83.2o, #C81.2o
GND:    #C79.2o, #C77.2o, #C75.2o
GND:    #C73.2o, #C71.2o, #C68.2o
GND:    #C66.2o, #C64.2o, #C62.2o
GND:    #C60.2o, #C58.2o, #C56.2o
GND:    #C54.2o, #C52.2o, #C50.2o
GND:    #C48.2o
GND:    #C95.2o, #C94.2o, #C91.2o  ;19
GND:    #C89.2o, #C86.2o, #C84.2o
GND:    #C82.2o, #C80.2o, #C76.2o
GND:    #C74.2o, #C72.2o, #C70.2o
GND:    #C69.2o, #C67.2o, #C65.2o
GND:    #C61.2o, #C59.2o, #C57.2o
GND:    #C55.2o, #C53.2o, #C51.2o
GND:    #C45.2o, #C43.2o, #C41.2o
GND:    #C39.2o, #C37.2o, #C35.2o
GND:    #C33.2o, #C31.2o, #C27.2o
GND:    #C25.2o, #C22.2o, #C20.2o
GND:    #C18.2o, #C14.2o, #C12.2o
GND:    #C10.2o, #C8.2o, #C6.2o
GND:    #C4.2o, #C2.2o, #C49.2o
GND:    #C129.2o, #C128.2o, #C127.2o  ;20
GND:    #C126.2o, #C125.2o, #C124.2o
GND:    #C123.2o, #C122.2o, #C121.2o
GND:    #C120.2o, #C119.2o, #C118.2o
GND:    #C117.2o, #C116.2o, #C115.2o
GND:    #C114.2o, #C113.2o, #C112.2o
GND:    #C111.2o, #C110.2o, #C109.2o
GND:    #C108.2o, #C107.2o, #C106.2o
GND:    #C105.2o, #C104.2o, #C103.2o
GND:    #C102.2o, #C101.2o, #C100.2o
GND:    #C99.2o, #C98.2o, #C97.2o
GND:    #C96.2o, #C93.2o, #C72.2o

GND:    #C78.2o, #C63.2o, #C47.2o
GND:    #C29.2o, #C24.2o, #C23.2o
GND:    #C16.2o

InhibitCorrect:  v38.19o  ;10
InhibitCorrect:  v15.4i, v27.4i ;14
InhibitCorrect:  v14.4i, v16.4i

LatchY.00: v54.6o, E136   ;2
LatchY.00: v44.4i   ;3
LatchY.00: v21.3i   ;4

LatchY.01: v54.9o, E36 ;2
LatchY.01: v58.4i   ;3
LatchY.01: v21.2i   ;4

LatchY.02: v54.12o  ;2
LatchY.02: v58.12i  ;3
LatchY.02: #TP086.1i   ;18

LatchY.03: v54.15o  ;2
LatchY.03: v57.4i   ;3
LatchY.03: #TP087.1i   ;18

LatchY.05: v54.16o  ;2
LatchY.05: v57.12i  ;3
LatchY.05: #TP088.1i   ;18

LatchY.06: v54.19o  ;2
LatchY.06: v43.4i   ;3
LatchY.06: #TP089.1i   ;18

LatchY.07: v53.2o   ;2
LatchY.07: v43.12i  ;3
LatchY.07: #TP090.1i   ;18

LatchY.08: v09.18o, v53.5o   ;2
LatchY.08: v49.6i   ;3
LatchY.08: v44.6i   ;3
LatchY.08: #TP091.1i   ;18

LatchY.09: v09.16o, v53.6o   ;2
LatchY.09: v49.10i  ;3
LatchY.09: v58.6i   ;3
LatchY.09: #TP092.1i   ;18

LatchY.10: v09.14o, v53.9o   ;2
LatchY.10: v50.6i   ;3
LatchY.10: v58.10i  ;3
LatchY.10: #TP093.1i   ;18

LatchY.11: v09.12o, v53.12o  ;2
LatchY.11: v50.10i  ;3
LatchY.11: v57.6i   ;3
LatchY.11: #TP094.1i   ;18

LatchY.13: v09.3o, v53.15o   ;2
LatchY.13: v51.6i   ;3
LatchY.13: v57.10i  ;3
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LatchY.13: #TP095.1i   ;18

LatchY.14: v09.5o, v53.16o   ;2
LatchY.14: v51.10i  ;3
LatchY.14: v43.6i   ;3
LatchY.14: #TP096.1i   ;18

LatchY.15: v09.7o, v53.19o   ;2
LatchY.15: v52.6i   ;3
LatchY.15: v43.10i  ;3
LatchY.15: #TP097.1i   ;18

LatchYH.6: v54.5o   ;2
LatchYH.6: v62.11i, v10.4i   ;4

LatchYH.7: v54.2o   ;2
LatchYH.7: v62.13i, v10.9i   ;4

LCAS:   E106, v07.12i  ;5

LdMDR:  v61.4o   ;1
LdMDR:  v40.11i, v39.11i  ;10

LowAddr.00:   v49.7o   ;3
LowAddr.00:   u46.15i, u23.15i  ;5
LowAddr.00:   u93.4i, u70.13i   ;5

LowAddr.01:   v49.9o   ;3
LowAddr.01:   u70.17i, u46.2i   ;5
LowAddr.01:   u93.8i, u94.4i ;5

LowAddr.02:   v50.7o   ;3
LowAddr.02:   u94.11i, u94.2i   ;5
LowAddr.02:   u46.11i, u23.11i  ;5

LowAddr.03:   v50.9o   ;3
LowAddr.03:   u46.13i, u23.13i  ;5
LowAddr.03:   u93.6i, u70.11i   ;5

LowAddr.04:   v51.7o   ;3
LowAddr.04:   u93.13i, u70.8i   ;5
LowAddr.04:   u46.8i, u23.6i ;5

LowAddr.05:   v51.9o   ;3
LowAddr.05:   u70.2i, u23.8i ;5
LowAddr.05:   u93.11i, u94.17i  ;5

LowAddr.06:   v52.7o   ;3
LowAddr.06:   u93.15i, u70.6i   ;5
LowAddr.06:   u46.6i, u23.4i ;5

LowWrite:  v61.1o   ;1
LowWrite:  u46.4i   ;5
LowWrite:  u23.17i  ;5
LowWrite:  u70.15i  ;5
LowWrite:  u93.17i  ;5

LRAS':  E105, v62.9i   ;3

LRAS:   v62.8o, v31.1i ;3
LRAS:   u69.9i, u69.1i, u69.12i ;4
LRAS:   u69.4i

M5V:    E100, E200, #F1.2i   ;17

MapRef: E15, v07.2i ;1

MCtl←': E115, u94.13i  ;10
MCtl←': v22.5i   ;15

MCycle: v13.1o   ;1
MCycle: v10.5i, v10.11i, v30.13i   ;4
MCycle: #TP085.1i   ;18

MDClk:  v19.6o   ;1
MDClk:  v26.11i  ;13

MDR←':  v61.5i, v19.8o, v01.2i  ;1

mem:    E113, v19.11i  ;1
mem:    v19.3i   ;1
mem:    v23.9i   ;1
mem:    v07.10i  ;1

MemCycle': v01.8o, v13.3i ;1
MemCycle': v20.5i   ;13

MemData.00:   u45.14o  ;11
MemData.00:   u22.14o  ;11
MemData.00:   u68.14o  ;11
MemData.00:   u92.14o  ;11
MemData.00:   v05.2i   ;12
MemData.00:   u95.2i   ;12
MemData.00:   u97.1i   ;16
MemData.00:   #TP063.1i   ;18

MemData.01:   u21.14o  ;11
MemData.01:   u67.14o  ;11
MemData.01:   u91.14o  ;11
MemData.01:   u44.14o  ;11
MemData.01:   v05.4i   ;12
MemData.01:   u95.4i   ;12
MemData.01:   u97.15o  ;16
MemData.01:   #TP064.1i   ;18

MemData.02:   u43.14o  ;11
MemData.02:   u20.14o  ;11
MemData.02:   u66.14o  ;11
MemData.02:   u90.14o  ;11
MemData.02:   v05.6i   ;12
MemData.02:   u95.6i   ;12
MemData.02:   u97.2i   ;16
MemData.02:   #TP065.1i   ;18

MemData.03:   u42.14o  ;11
MemData.03:   u19.14o  ;11
MemData.03:   u65.14o  ;11
MemData.03:   u89.14o  ;11
```

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 35 OF	B

```
MemData.03:   v05.8i   ;12
MemData.03:   u95.8i   ;12
MemData.03:   u97.14o  ;16
MemData.03:   #TP066.1i   ;18

MemData.04:   u41.14o  ;11
MemData.04:   u18.14o  ;11
MemData.04:   u64.14o  ;11
MemData.04:   u88.14o  ;11
MemData.04:   v05.17i  ;12
MemData.04:   u95.17i  ;12
MemData.04:   u97.3i   ;16
MemData.04:   #TP067.1i   ;18

MemData.05:   u40.14o  ;11
MemData.05:   u17.14o  ;11
MemData.05:   u63.14o  ;11
MemData.05:   u87.14o  ;11
MemData.05:   v05.15i  ;12
MemData.05:   u95.15i  ;12
MemData.05:   u97.13o  ;16
MemData.05:   #TP068.1i   ;18

MemData.06:   u39.14o  ;11
MemData.06:   u16.14o  ;11
MemData.06:   u62.14o  ;11
MemData.06:   u86.14o  ;11
MemData.06:   v05.13i  ;12
MemData.06:   u95.13i  ;12
MemData.06:   u97.4i   ;16
MemData.06:   #TP069.1i   ;18

MemData.07:   u38.14o  ;11
MemData.07:   u15.14o  ;11
MemData.07:   u61.14o  ;11
MemData.07:   u85.14o  ;11
MemData.07:   v05.11i  ;12
MemData.07:   u95.11i  ;12
MemData.07:   u97.12o  ;16
MemData.07:   #TP070.1i   ;18

MemData.08:   u37.14o  ;11
MemData.08:   u14.14o  ;11
MemData.08:   u60.14o  ;11
MemData.08:   u84.14o  ;11
MemData.08:   v04.2i   ;12
MemData.08:   u96.2i   ;12
MemData.08:   u97.5i   ;16
MemData.08:   #TP071.1i   ;18

MemData.09:   u36.14o  ;11
MemData.09:   u13.14o  ;11
MemData.09:   u59.14o  ;11
MemData.09:   u83.14o  ;11
MemData.09:   v04.4i   ;12
MemData.09:   u96.4i   ;12
MemData.09:   u97.11o  ;16
MemData.09:   #TP072.1i   ;18

MemData.10:   u35.14o  ;11
MemData.10:   u12.14o  ;11
MemData.10:   u58.14o  ;11
MemData.10:   u82.14o  ;11
MemData.10:   v04.6i   ;12
MemData.10:   u96.6i   ;12
MemData.10:   u97.6i   ;16
MemData.10:   #TP073.1i   ;18

MemData.11:   u34.14o  ;11
MemData.11:   u11.14o  ;11
MemData.11:   u57.14o  ;11
MemData.11:   u81.14o  ;11
MemData.11:   v04.8i   ;12
MemData.11:   u96.8i   ;12
MemData.11:   u97.10o  ;16
MemData.11:   #TP074.1i   ;18

MemData.12:   u33.14o  ;11
MemData.12:   u10.14o  ;11
MemData.12:   u56.14o  ;11
MemData.12:   u80.14o  ;11
MemData.12:   v04.17i  ;12
MemData.12:   u96.17i  ;12
MemData.12:   u97.7i   ;16
MemData.12:   #TP075.1i   ;18

MemData.13:   u32.14o  ;11
MemData.13:   u09.14o  ;11
MemData.13:   u55.14o  ;11
MemData.13:   u79.14o  ;11
MemData.13:   v04.15i  ;12
MemData.13:   u96.15i  ;12
MemData.13:   u97.9o   ;16
MemData.13:   #TP076.1i   ;18

MemData.14:   u31.14o  ;11
MemData.14:   u08.14o  ;11
MemData.14:   u54.14o  ;11
MemData.14:   u78.14o  ;11
MemData.14:   v04.13i  ;12
MemData.14:   u96.13i  ;12
MemData.14:   u97.8i   ;16
MemData.14:   #TP077.1i   ;18

MemData.15:   u30.14o  ;11
MemData.15:   u07.14o  ;11
MemData.15:   u53.14o  ;11
MemData.15:   u77.14o  ;11
MemData.15:   v04.11i  ;12
MemData.15:   u96.11i  ;12
MemData.15:   v03.15o  ;16
MemData.15:   #TP078.1i   ;18

MemData.16:   u29.14o  ;11
MemData.16:   u06.14o  ;11
MemData.16:   u52.14o  ;11
MemData.16:   u76.14o  ;11
MemData.16:   v06.2i   ;12
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MemData.16:   v03.1i   ;16
MemData.16:   #TP079.1i   ;18

MemData.17:   u28.14o  ;11
MemData.17:   u05.14o  ;11
MemData.17:   u51.14o  ;11
MemData.17:   u75.14o  ;11
MemData.17:   v06.4i   ;12
MemData.17:   v03.14o  ;16
MemData.17:   #TP080.1i   ;18

MemData.18:   u27.14o  ;11
MemData.18:   u04.14o  ;11
MemData.18:   u50.14o  ;11
MemData.18:   u74.14o  ;11
MemData.18:   v06.6i   ;12
MemData.18:   v03.2i   ;16
MemData.18:   #TP081.1i   ;18

MemData.19:   u26.14o  ;11
MemData.19:   u03.14o  ;11
MemData.19:   u49.14o  ;11
MemData.19:   u73.14o  ;11
MemData.19:   v06.8i   ;12
MemData.19:   v03.13o  ;16
MemData.19:   #TP082.1i   ;18

MemData.20:   u25.14o  ;11
MemData.20:   u02.14o  ;11
MemData.20:   u48.14o  ;11
MemData.20:   u72.14o  ;11
MemData.20:   v06.17i  ;12
MemData.20:   v03.3i   ;16
MemData.20:   #TP083.1i   ;18

MemData.21:   u24.14o  ;11
MemData.21:   u01.14o  ;11
MemData.21:   u47.14o  ;11
MemData.21:   u71.14o  ;11
MemData.21:   v06.11i  ;12
MemData.21:   v03.12o  ;16
MemData.21:   #TP084.1i   ;18

MemErr':   v23.12i, v23.13i, v30.6o   ;13
MemErr':   v12.4i, v12.5i ;15

MemErr: v26.18i, v23.11o, E166  ;13

MRef':  v02.6o, E38 ;1
MRef':  v20.4i   ;13

MRef:   v13.2i, v02.5o ;1
MRef:   v57.2i, v58.2i, v44.2i  ;3
MRef:   v43.2i

P12V:   E1, E101, #F3.2i  ;17

P5V:    E50, E51, E150, E151, #F2.2i  ;17

ppClk:  v61.6i, E9, v61.11i  ;1

preClk: v07.5i   ;1
preClk: v62.1i, v61.13o   ;1
preClk: v19.5i   ;1
preClk: v23.2i   ;10
preClk: v12.6i   ;15

Pt.0:   E64, v12.3i ;15

Pt.1:   E164, v12.2i   ;15

Pt.2:   E65, v12.1i ;15

PullupA:   v02.1i   ;1
PullupA:   v01.1i   ;1
PullupA:   v02.13i  ;1
PullupA:   v01.13i  ;1
PullupA:   u95.19i, u96.19i  ;12
PullupA:   #R64.2i  ;16

PullupB:   v01.4i   ;1
PullupB:   #R63.2i  ;16
PullupB:   #TP099.1i   ;18

RAS':   E5, v62.5i  ;3

RASA':  u22.4i   ;6
RASA':  u21.4i   ;6
RASA':  u20.4i   ;6
RASA':  u19.4i   ;6
RASA':  u18.4i   ;6
RASA':  u17.4i   ;6
RASA':  u16.4i   ;6
RASA':  u15.4i   ;6
RASA':  u14.4i   ;6
RASA':  u13.4i   ;6
RASA':  u12.4i   ;6
RASA':  u11.4i   ;6
RASA':  u10.4i   ;6
RASA':  u09.4i   ;6
RASA':  u08.4i   ;6
RASA':  u07.4i   ;6
RASA':  u06.4i   ;6
RASA':  u05.4i   ;6
RASA':  u04.4i   ;6
RASA':  u03.4i   ;6
RASA':  u02.4i   ;6
RASA':  u01.4i   ;6
RASA':  #R3.2i   ;16
RASA':  #TP004.1i   ;18

RASAz': u69.6o   ;4
RASAz': #R3.1o   ;16

RASB':  u44.4i   ;7
RASB':  u45.4i   ;7
RASB':  u43.4i   ;7
RASB':  u42.4i   ;7
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XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11217	SHEET REV.
	TITLE SCHEMATIC, MCC	A4	SHEET 37 OF	B

```
RASB':   u38.4i   ;7
RASB':   u39.4i   ;7
RASB':   u41.4i   ;7
RASB':   u40.4i   ;7
RASB':   u36.4i   ;7
RASB':   u37.4i   ;7
RASB':   u35.4i   ;7
RASB':   u34.4i   ;7
RASB':   u30.4i   ;7
RASB':   u31.4i   ;7
RASB':   u33.4i   ;7
RASB':   u32.4i   ;7
RASB':   u28.4i   ;7
RASB':   u29.4i   ;7
RASB':   u27.4i   ;7
RASB':   u26.4i   ;7
RASB':   u25.4i   ;7
RASB':   u24.4i   ;7
RASB':   #R13.2i  ;16
RASB':   #TP014.1i   ;18

RASBz': u69.11o  ;4
RASBz': #R13.1o  ;16

RASC':   u68.4i   ;8
RASC':   u64.4i   ;8
RASC':   u60.4i   ;8
RASC':   u56.4i   ;8
RASC':   u52.4i   ;8
RASC':   u48.4i   ;8
RASC':   u47.4i   ;8
RASC':   u51.4i   ;8
RASC':   u55.4i   ;8
RASC':   u59.4i   ;8
RASC':   u63.4i   ;8
RASC':   u67.4i   ;8
RASC':   u66.4i   ;8
RASC':   u62.4i   ;8
RASC':   u58.4i   ;8
RASC':   u54.4i   ;8
RASC':   u50.4i   ;8
RASC':   u49.4i   ;8
RASC':   u53.4i   ;8
RASC':   u57.4i   ;8
RASC':   u61.4i   ;8
RASC':   u65.4i   ;8
RASC':   #R23.2i  ;16
RASC':   #TP024.1i   ;18

RASCz': u69.3o   ;4
RASCz': #R23.1o  ;16

RASD':   u92.4i   ;9
RASD':   u91.4i   ;9
RASD':   u90.4i   ;9
RASD':   u89.4i   ;9
RASD':   u85.4i   ;9
RASD':   u86.4i   ;9
RASD':   u87.4i   ;9

RASD':   u88.4i   ;9
RASD':   u84.4i   ;9
RASD':   u83.4i   ;9
RASD':   u82.4i   ;9
RASD':   u81.4i   ;9
RASD':   u77.4i   ;9
RASD':   u78.4i   ;9
RASD':   u79.4i   ;9
RASD':   u80.4i   ;9
RASD':   u76.4i   ;9
RASD':   u75.4i   ;9
RASD':   u74.4i   ;9
RASD':   u73.4i   ;9
RASD':   u71.4i   ;9
RASD':   u72.4i   ;9
RASD':   #R33.2i  ;16
RASD':   #TP034.1i   ;18

RASDz': u69.8o   ;4
RASDz': #R33.1o  ;16

Refresh':  v09.1i, u94.15i, E16 ;2
Refresh':  v09.19i

Refresh:   v19.2i   ;1
Refresh:   u94.5o, v53.1i ;2

RFCL:   v20.9i, v20.10i   ;2
RFCL:   #R65.2i  ;16
RFCL:   #TP098.1i   ;18

SAddr.00:  v44.7o, E32 ;3

SAddr.01:  v58.7o, E132   ;3

SAddr.02:  v58.9o, E33 ;3

SAddr.03:  v57.7o, E133   ;3

SAddr.04:  v57.9o, E34 ;3

SAddr.05:  v43.7o, E134   ;3

SAddr.06:  v43.9o, E35 ;3

SDI.00: v40.2o, E96 ;10
SDI.00: v37.1i   ;10
SDI.00: v36.1i   ;10
SDI.00: v32.1i   ;10
SDI.00: #R62.2i  ;16

SDI.00z:   u22.2i, u68.2i, u92.2i  ;11
SDI.00z:   u45.2i
SDI.00z:   #R62.1o  ;16
SDI.00z:   #TP041.1i   ;18

SDI.01: v40.5o, E196   ;10
SDI.01: v37.2i   ;10
SDI.01: v35.1i   ;10
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SDI.01: v32.2i   ;10
SDI.01: #R60.2i  ;16

SDI.01z:   u21.2i, u67.2i, u91.2i  ;11
SDI.01z:   u44.2i
SDI.01z:   #R60.1o  ;16
SDI.01z:   #TP042.1i   ;18

SDI.02: v40.6o, E95 ;10
SDI.02: v37.4i   ;10
SDI.02: v34.1i   ;10
SDI.02: v32.4i   ;10
SDI.02: #R58.2i  ;16

SDI.02z:   u20.2i, u66.2i, u90.2i  ;11
SDI.02z:   u43.2i
SDI.02z:   #R58.1o  ;16
SDI.02z:   #TP043.1i   ;18

SDI.03: v40.9o, E195   ;10
SDI.03: v37.8i   ;10
SDI.03: v33.1i   ;10
SDI.03: v32.8i   ;10
SDI.03: #R56.2i  ;16

SDI.03z:   u19.2i, u65.2i, u89.2i  ;11
SDI.03z:   u42.2i
SDI.03z:   #R56.1o  ;16
SDI.03z:   #TP044.1i   ;18

SDI.04: v40.12o, E94   ;10
SDI.04: v36.2i   ;10
SDI.04: v35.2i   ;10
SDI.04: v32.9i   ;10
SDI.04: #R54.2i  ;16

SDI.04z:   u18.2i, u64.2i, u88.2i  ;11
SDI.04z:   u41.2i
SDI.04z:   #R54.1o  ;16
SDI.04z:   #TP045.1i   ;18

SDI.05: v40.15o, E194  ;10
SDI.05: v36.4i   ;10
SDI.05: v34.2i   ;10
SDI.05: v32.10i  ;10
SDI.05: #R52.2i  ;16

SDI.05z:   u17.2i, u63.2i, u87.2i  ;11
SDI.05z:   u40.2i
SDI.05z:   #R52.1o  ;16
SDI.05z:   #TP046.1i   ;18

SDI.06: v40.16o, E93   ;10
SDI.06: v35.4i   ;10
SDI.06: v34.4i   ;10
SDI.06: v33.2i   ;10
SDI.06: #R50.2i  ;16

SDI.06z:   u16.2i, u62.2i, u86.2i  ;11
SDI.06z:   u39.2i
SDI.06z:   #R50.1o  ;16
SDI.06z:   #TP047.1i   ;18

SDI.07: v40.19o, E193  ;10
SDI.07: v36.8i   ;10
SDI.07: v34.8i   ;10
SDI.07: v33.4i   ;10
SDI.07: #R48.2i  ;16

SDI.07z:   u15.2i, u61.2i, u85.2i  ;11
SDI.07z:   u38.2i
SDI.07z:   #R48.1o  ;16
SDI.07z:   #TP048.1i   ;18

SDI.08: v39.2o, E92 ;10
SDI.08: v36.9i   ;10
SDI.08: v35.8i   ;10
SDI.08: v33.8i   ;10
SDI.08: #R42.2i  ;16

SDI.08z:   u14.2i, u60.2i, u84.2i  ;11
SDI.08z:   u37.2i
SDI.08z:   #R42.1o  ;16
SDI.08z:   #TP049.1i   ;18

SDI.09: v39.5o, E192   ;10
SDI.09: v36.10i  ;10
SDI.09: v35.9i   ;10
SDI.09: v34.9i   ;10
SDI.09: #R44.2i  ;16

SDI.09z:   u13.2i, u59.2i, u83.2i  ;11
SDI.09z:   u36.2i
SDI.09z:   #R44.1o  ;16
SDI.09z:   #TP050.1i   ;18

SDI.10: v39.6o, E91 ;10
SDI.10: v37.9i   ;10
SDI.10: v34.10i  ;10
SDI.10: v33.9i   ;10
SDI.10: #R46.2i  ;16

SDI.10z:   u12.2i, u58.2i, u82.2i  ;11
SDI.10z:   u35.2i
SDI.10z:   #R46.1o  ;16
SDI.10z:   #TP051.1i   ;18

SDI.11: v39.9o, E191   ;10
SDI.11: v37.10i  ;10
SDI.11: v35.10i  ;10
SDI.11: v33.10i  ;10
SDI.11: #R41.2i  ;16

SDI.11z:   u11.2i, u57.2i, u81.2i  ;11
SDI.11z:   u34.2i
SDI.11z:   #R41.1o  ;16
SDI.11z:   #TP052.1i   ;18
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SDI.12: v39.12o, E89   ;10
SDI.12: v37.11i  ;10
SDI.12: v35.11i  ;10
SDI.12: v34.11i  ;10
SDI.12: #R43.2i  ;16

SDI.12z:   u10.2i, u56.2i, u80.2i  ;11
SDI.12z:   u33.2i
SDI.12z:   #R43.1o  ;16
SDI.12z:   #TP053.1i   ;18

SDI.13: v39.15o, E189  ;10
SDI.13: v37.12i  ;10
SDI.13: v36.11i  ;10
SDI.13: v33.11i  ;10
SDI.13: #R45.2i  ;16

SDI.13z:   u09.2i, u55.2i, u79.2i  ;11
SDI.13z:   u32.2i
SDI.13z:   #R45.1o  ;16
SDI.13z:   #TP054.1i   ;18

SDI.14: v39.16o, E88   ;10
SDI.14: v35.12i  ;10
SDI.14: v34.12i  ;10
SDI.14: v32.11i  ;10
SDI.14: #R47.2i  ;16

SDI.14z:   u08.2i, u54.2i, u78.2i  ;11
SDI.14z:   u31.2i
SDI.14z:   #R47.1o  ;16
SDI.14z:   #TP055.1i   ;18

SDI.15: v39.19o, E188  ;10
SDI.15: v36.12i  ;10
SDI.15: v33.12i  ;10
SDI.15: v32.12i  ;10
SDI.15: #R49.2i  ;16

SDI.15z:   u07.2i, u53.2i, u77.2i  ;11
SDI.15z:   u30.2i
SDI.15z:   #R49.1o  ;16
SDI.15z:   #TP056.1i   ;18

SDI.16: v37.5o, E87 ;10
SDI.16: #R51.2i  ;16

SDI.16z:   u06.2i, u52.2i, u76.2i  ;11
SDI.16z:   u29.2i
SDI.16z:   #R51.1o  ;16
SDI.16z:   #TP057.1i   ;18

SDI.17: v36.5o, E187   ;10
SDI.17: #R53.2i  ;16

SDI.17z:   u05.2i, u51.2i, u75.2i  ;11
SDI.17z:   u28.2i
SDI.17z:   #R53.1o  ;16
SDI.17z:   #TP058.1i   ;18

SDI.18: v35.5o, E86 ;10
SDI.18: #R55.2i  ;16

SDI.18z:   u04.2i, u50.2i, u74.2i  ;11
SDI.18z:   u27.2i
SDI.18z:   #R55.1o  ;16
SDI.18z:   #TP059.1i   ;18

SDI.19: v34.5o, E186   ;10
SDI.19: #R57.2i  ;16

SDI.19z:   u03.2i, u49.2i, u73.2i  ;11
SDI.19z:   u26.2i
SDI.19z:   #R57.1o  ;16
SDI.19z:   #TP060.1i   ;18

SDI.20: v33.6o, E85 ;10
SDI.20: #R59.2i  ;16

SDI.20z:   u02.2i, u48.2i, u72.2i  ;11
SDI.20z:   u25.2i
SDI.20z:   #R59.1o  ;16
SDI.20z:   #TP061.1i   ;18

SDI.21: v32.6o, E185   ;10
SDI.21: #R61.2i  ;16

SDI.21z:   u01.2i, u47.2i, u71.2i  ;11
SDI.21z:   u24.2i
SDI.21z:   #R61.1o  ;16
SDI.21z:   #TP062.1i   ;18

SDO.00: v05.18o, E18   ;12
SDO.00: v60.1i   ;13
SDO.00: v59.1i   ;13
SDO.00: v17.2i   ;13
SDO.00: v24.2i   ;14

SDO.01: v05.16o, E118  ;12
SDO.01: v60.2i   ;13
SDO.01: v46.1i   ;13
SDO.01: v17.4i   ;13
SDO.01: v24.5i   ;14

SDO.02: v05.14o, E19   ;12
SDO.02: v60.4i   ;13
SDO.02: v45.1i   ;13
SDO.02: v17.8i   ;13
SDO.02: v24.10i  ;14

SDO.03: v05.12o, E119  ;12
SDO.03: v60.8i   ;13
SDO.03: v29.1i   ;13
SDO.03: v24.13i  ;14

SDO.04: v05.3o, E21 ;12
SDO.04: v59.2i   ;13
SDO.04: v46.2i   ;13
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SDO.04: v17.9i   ;13
SDO.04: v25.2i   ;14

SDO.05: v05.5o, E121   ;12
SDO.05: v59.4i   ;13
SDO.05: v45.2i   ;13
SDO.05: v17.10i  ;13
SDO.05: v25.5i   ;14

SDO.06: v05.7o, E22 ;12
SDO.06: v46.4i   ;13
SDO.06: v45.4i   ;13
SDO.06: v29.2i   ;13
SDO.06: v25.10i  ;14

SDO.07: v05.9o, E122   ;12
SDO.07: v59.8i   ;13
SDO.07: v45.8i   ;13
SDO.07: v29.4i   ;13
SDO.07: v25.13i  ;14

SDO.08: v04.18o, E23   ;12
SDO.08: v59.9i   ;13
SDO.08: v46.8i   ;13
SDO.08: v29.8i   ;13
SDO.08: v41.2i   ;14

SDO.09: v04.16o, E123  ;12
SDO.09: v59.10i  ;13
SDO.09: v46.9i   ;13
SDO.09: v45.9i   ;13
SDO.09: v28.1i   ;13
SDO.09: v41.5i   ;14

SDO.10: v04.14o, E24   ;12
SDO.10: v60.9i   ;13
SDO.10: v45.10i  ;13
SDO.10: v29.9i   ;13
SDO.10: v41.10i  ;14

SDO.11: v04.12o, E124  ;12
SDO.11: v60.10i  ;13
SDO.11: v46.10i  ;13
SDO.11: v29.10i  ;13
SDO.11: v41.13i  ;14

SDO.12: v04.3o, E25 ;12
SDO.12: v60.11i  ;13
SDO.12: v46.11i  ;13
SDO.12: v45.11i  ;13
SDO.12: v28.2i   ;13
SDO.12: v42.2i   ;14

SDO.13: v04.5o, E125   ;12
SDO.13: v60.12i  ;13
SDO.13: v59.11i  ;13
SDO.13: v29.11i  ;13
SDO.13: v42.5i   ;14

SDO.14: v04.7o, E26 ;12
SDO.14: v46.12i  ;13
SDO.14: v45.12i  ;13
SDO.14: v17.11i  ;13
SDO.14: v42.10i  ;14

SDO.15: v04.9o, E126   ;12
SDO.15: v59.12i  ;13
SDO.15: v29.12i  ;13
SDO.15: v42.13i  ;14

SDO.16: v06.18o, E27   ;12
SDO.16: v60.13i  ;13
SDO.16: v28.4i   ;13

SDO.17: v06.16o, E127  ;12
SDO.17: v59.13i  ;13
SDO.17: v28.8i   ;13

SDO.18: v06.14o, E28   ;12
SDO.18: v46.13i  ;13
SDO.18: v28.9i   ;13

SDO.19: v06.12o, E128  ;12
SDO.19: v45.13i  ;13
SDO.19: v28.10i  ;13

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WriteB':   u28.3i   ;7
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WriteB':   u27.3i   ;7
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WriteB':   u25.3i   ;7
WriteB':   u24.3i   ;7
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WriteB':   #TP012.1i   ;18

WriteBz':  u46.16o  ;5
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WriteC':   u68.3i   ;8
WriteC':   u64.3i   ;8
WriteC':   u60.3i   ;8
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WriteC':   u49.3i   ;8
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```
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WriteC':   u61.3i   ;8
WriteC':   u65.3i   ;8
WriteC':   #R22.2i  ;16
WriteC':   #TP022.1i   ;18

WriteCz':  u70.5o   ;5
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WriteD':   u92.3i   ;9
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Y.00:   v54.7i   ;2
Y.00:   E49, v40.3i ;10

Y.01:   v54.8i   ;2
Y.01:   E149, v40.4i   ;10

Y.02:   v54.13i  ;2
Y.02:   v49.5i   ;3
Y.02:   v44.5i   ;3
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Y.03:   v54.14i  ;2
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Y.03:   v58.5i   ;3
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Y.04:   v43.13i  ;3
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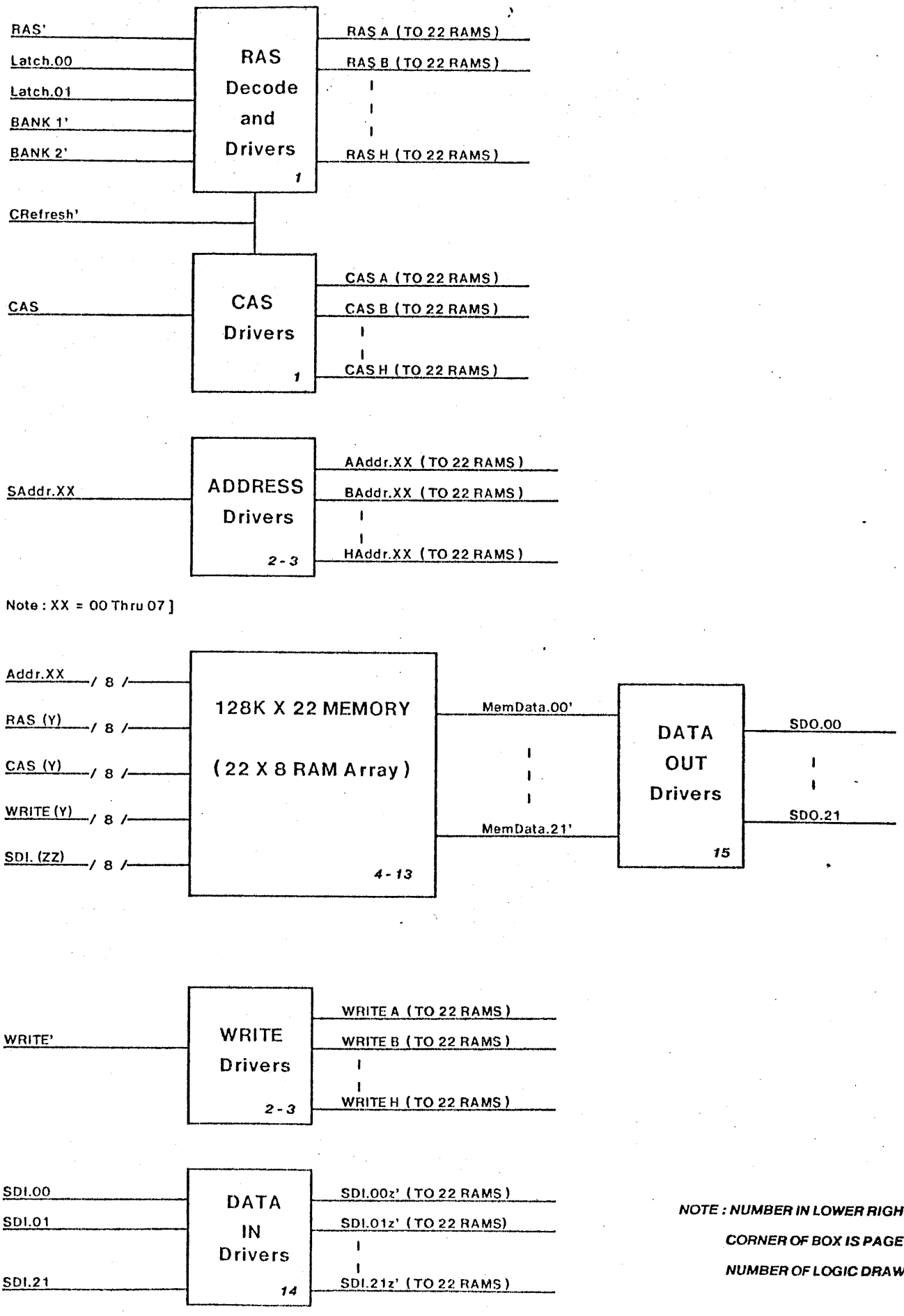

NOTE : NUMBER IN LOWER RIGHT CORNER OF BOX IS PAGE NUMBER OF LOGIC DRAWING

MSC-0.4.SIL

MEMORY STORAGE CARD BLOCK DIAGRAM

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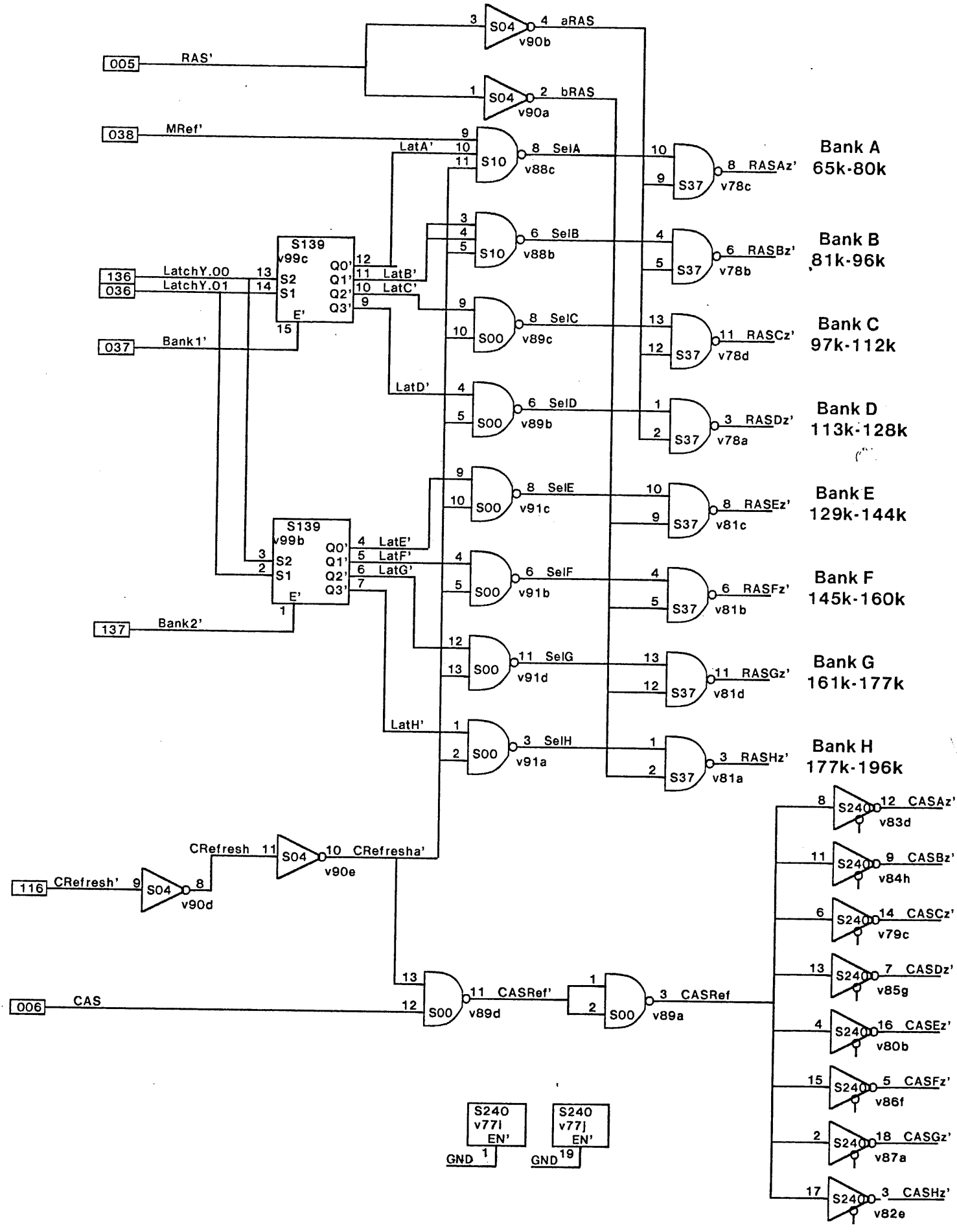

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
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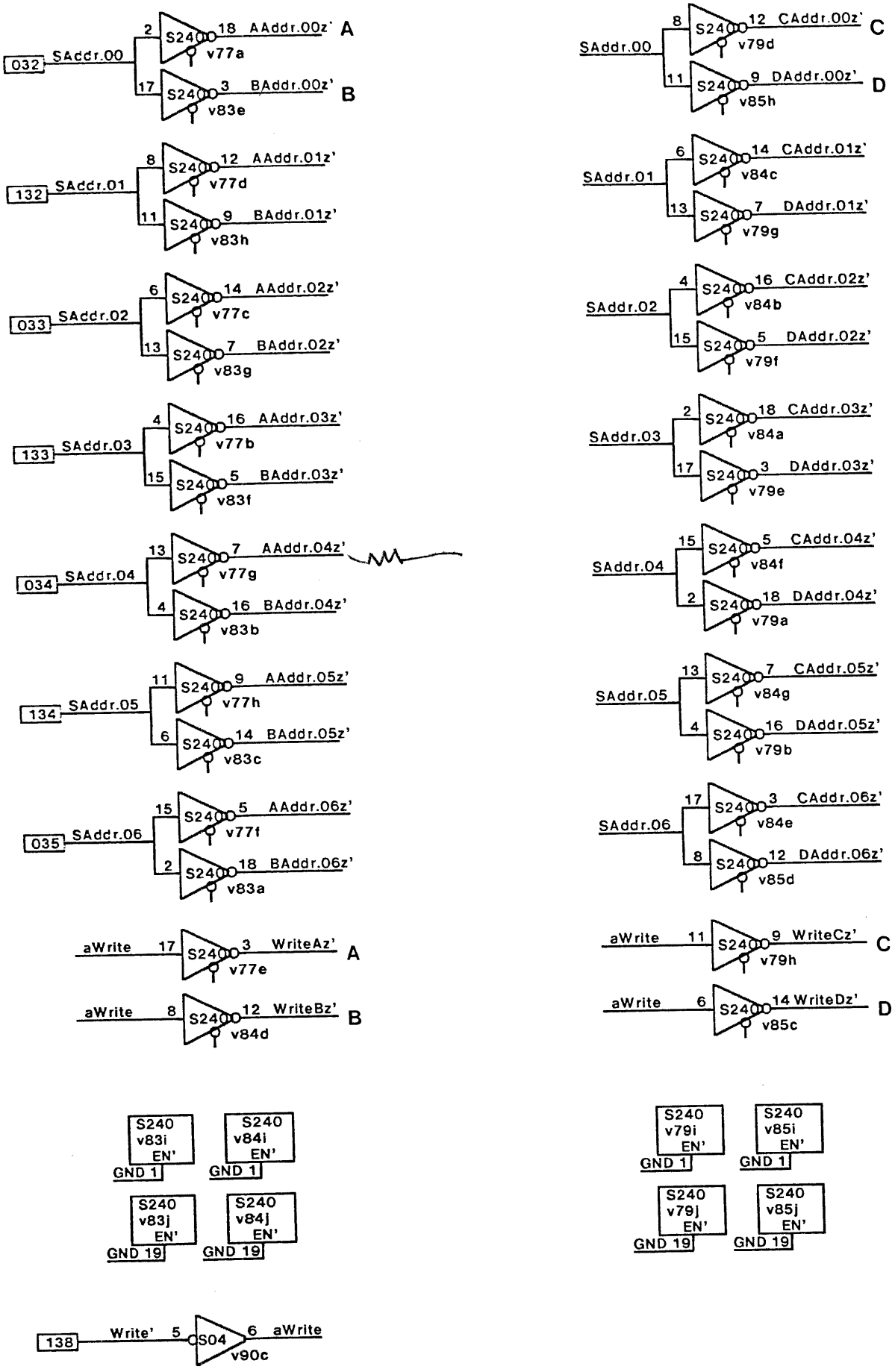

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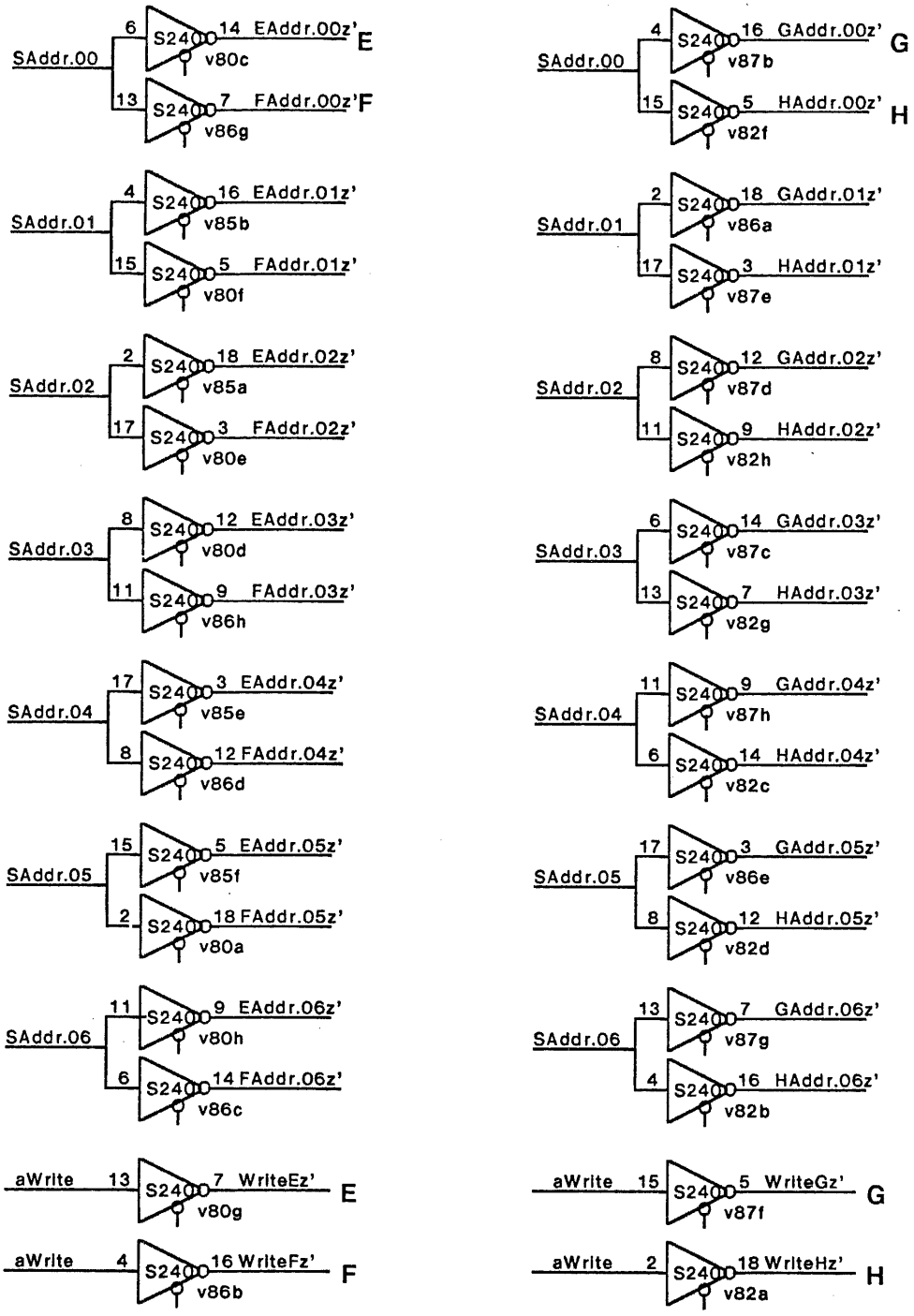

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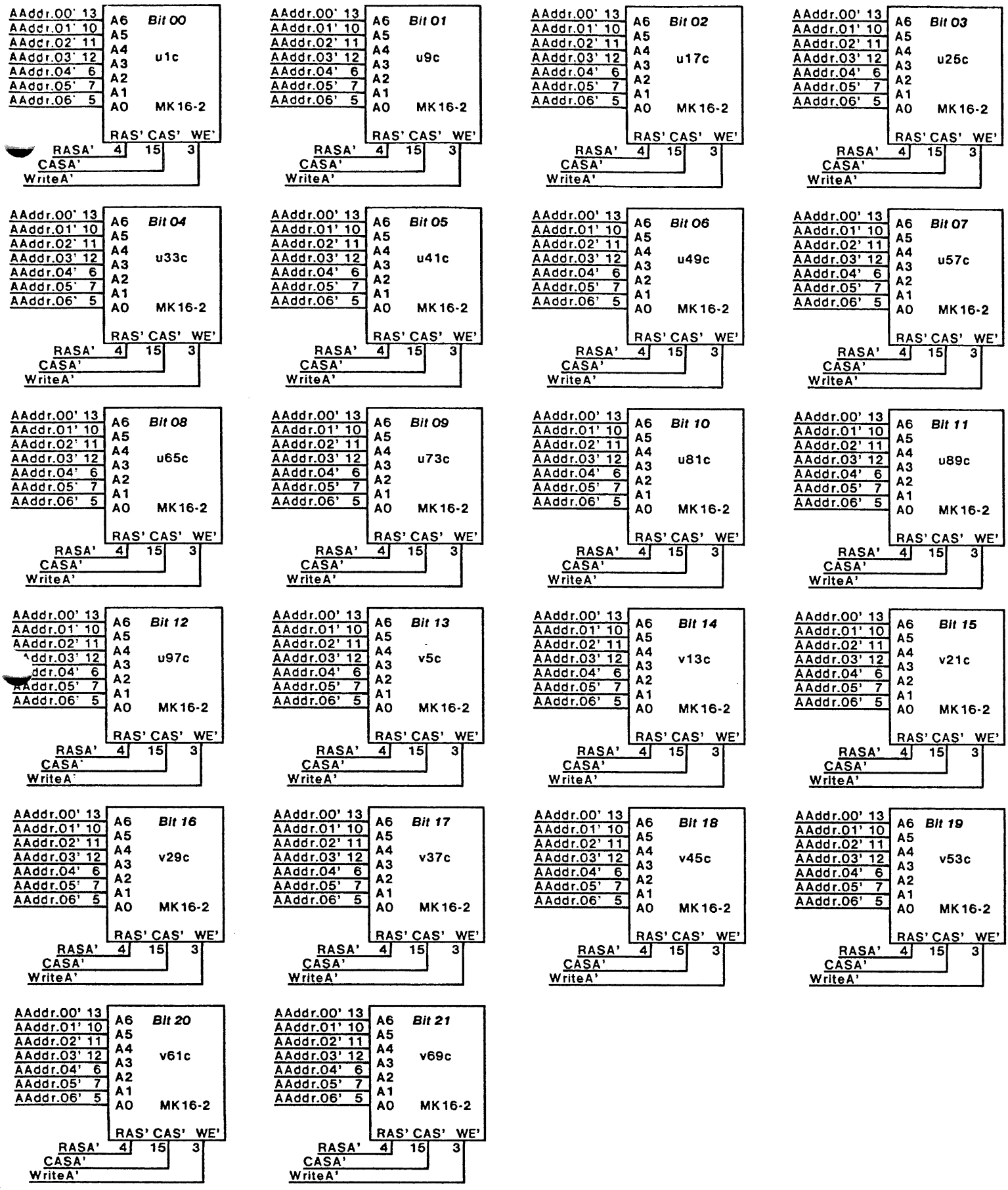

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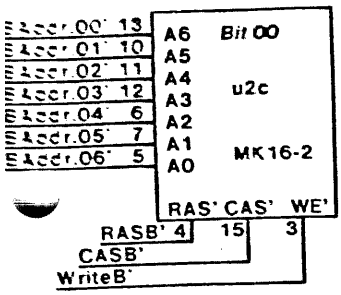
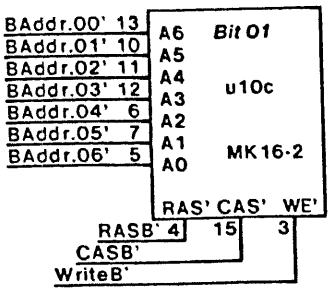
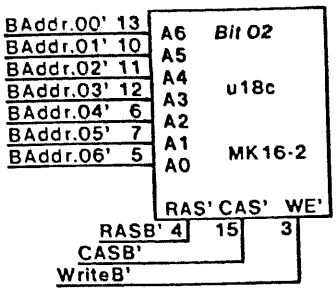
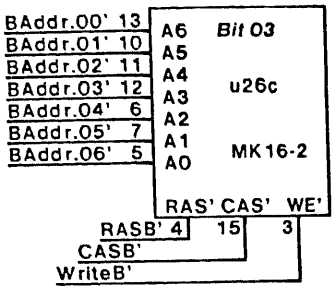
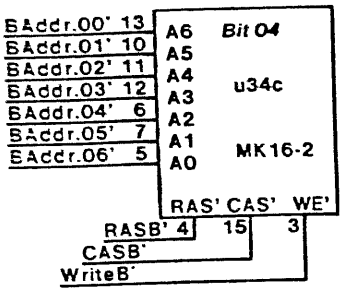
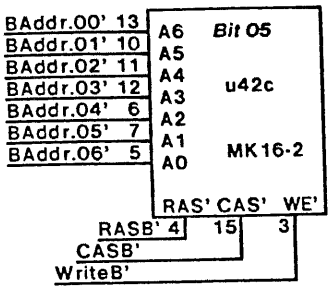


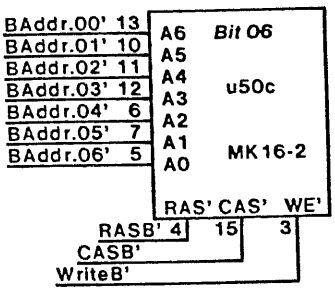


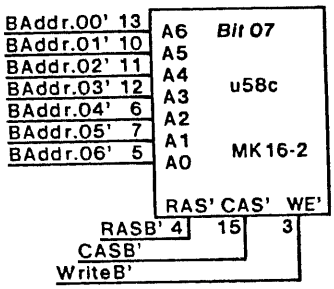


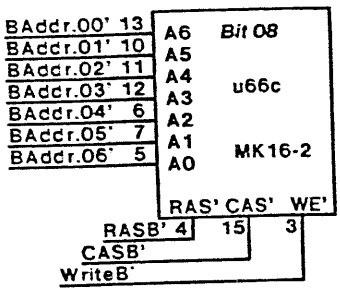


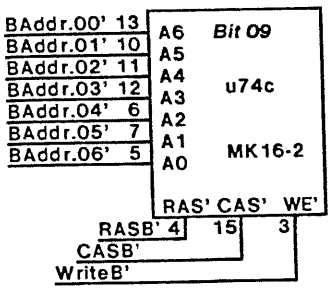


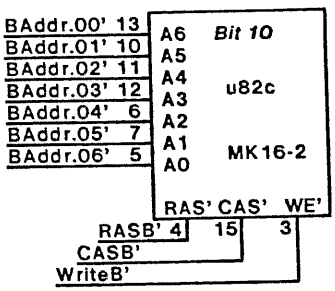


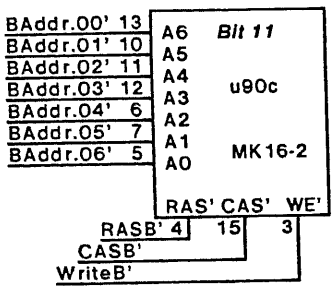


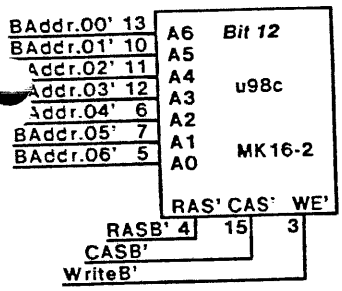


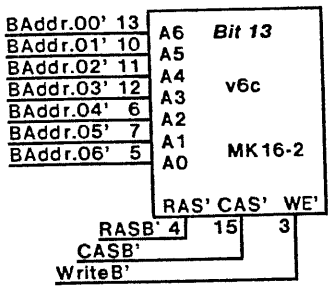


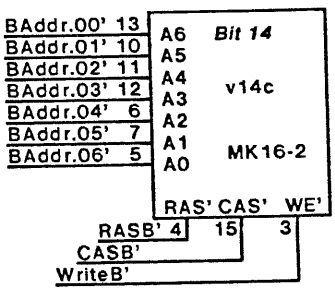


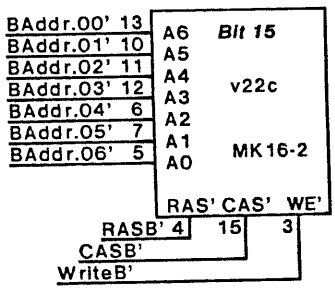


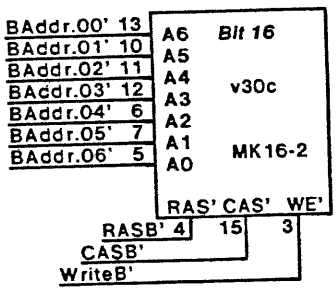


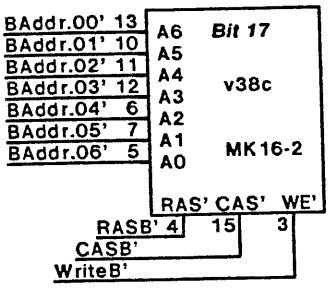


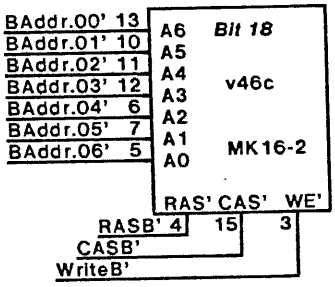


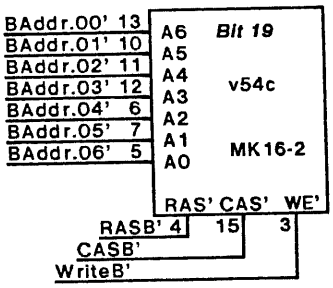


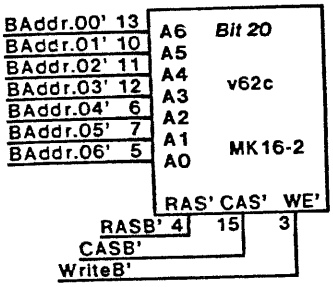


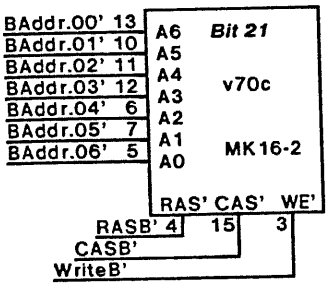




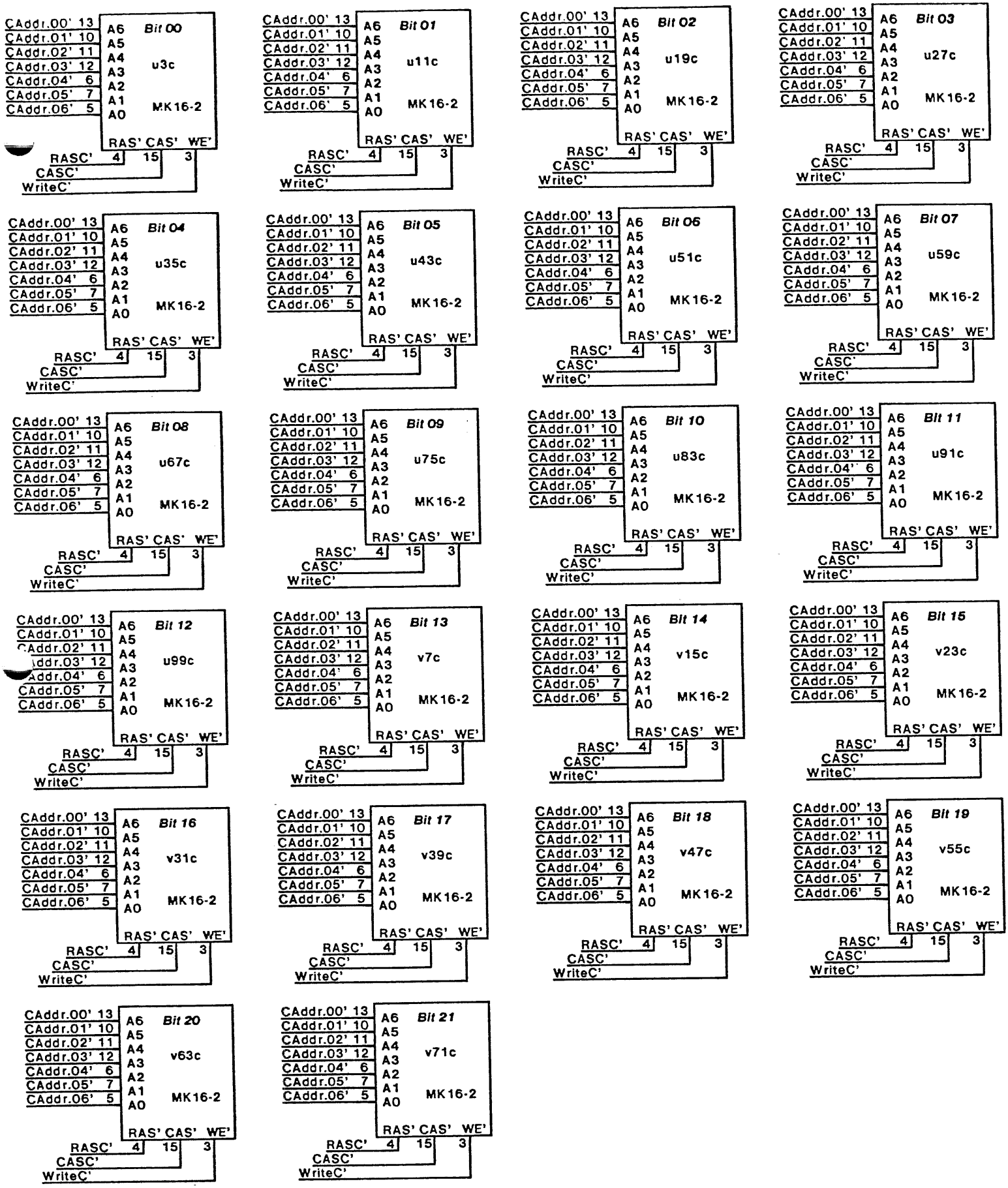




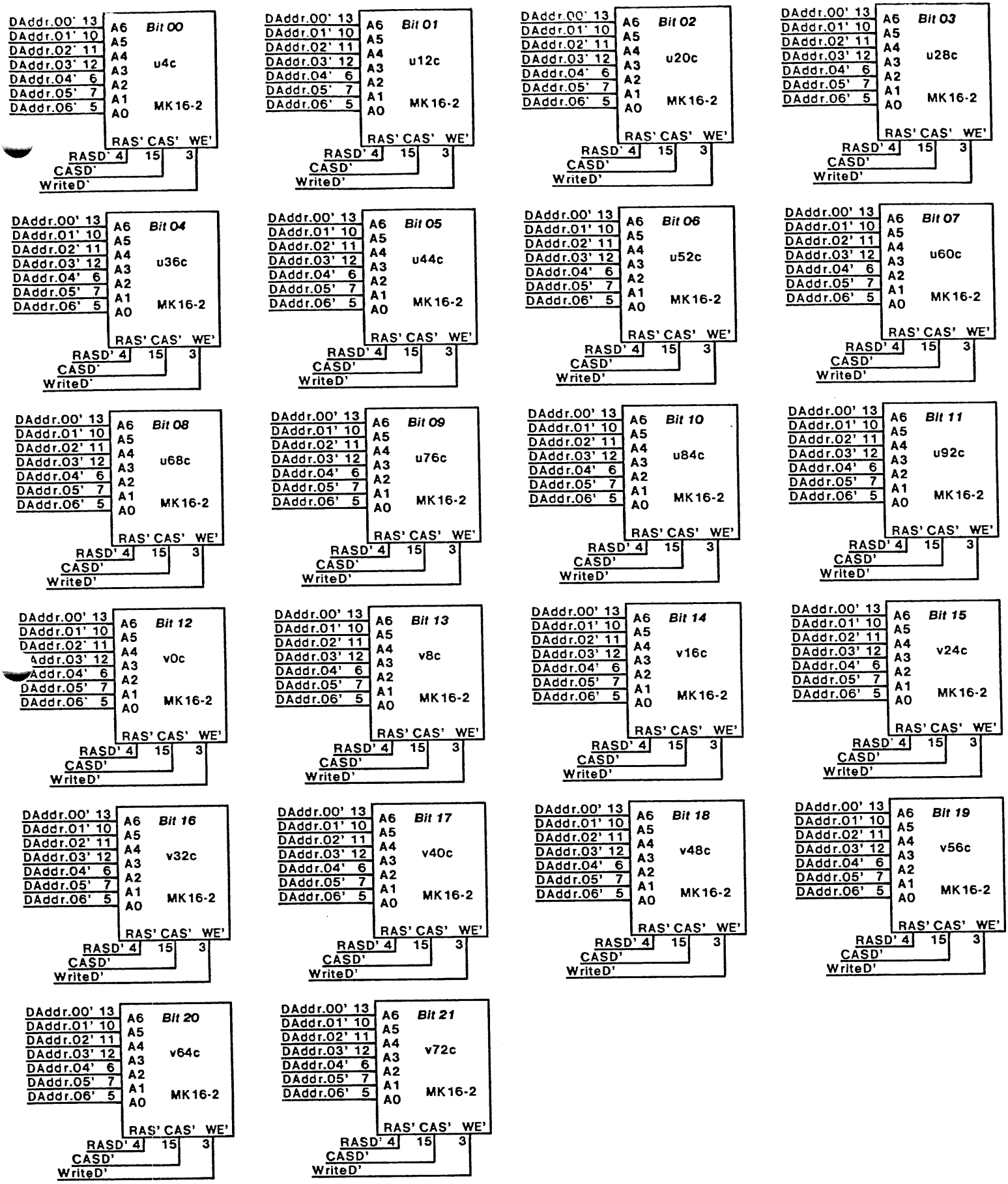




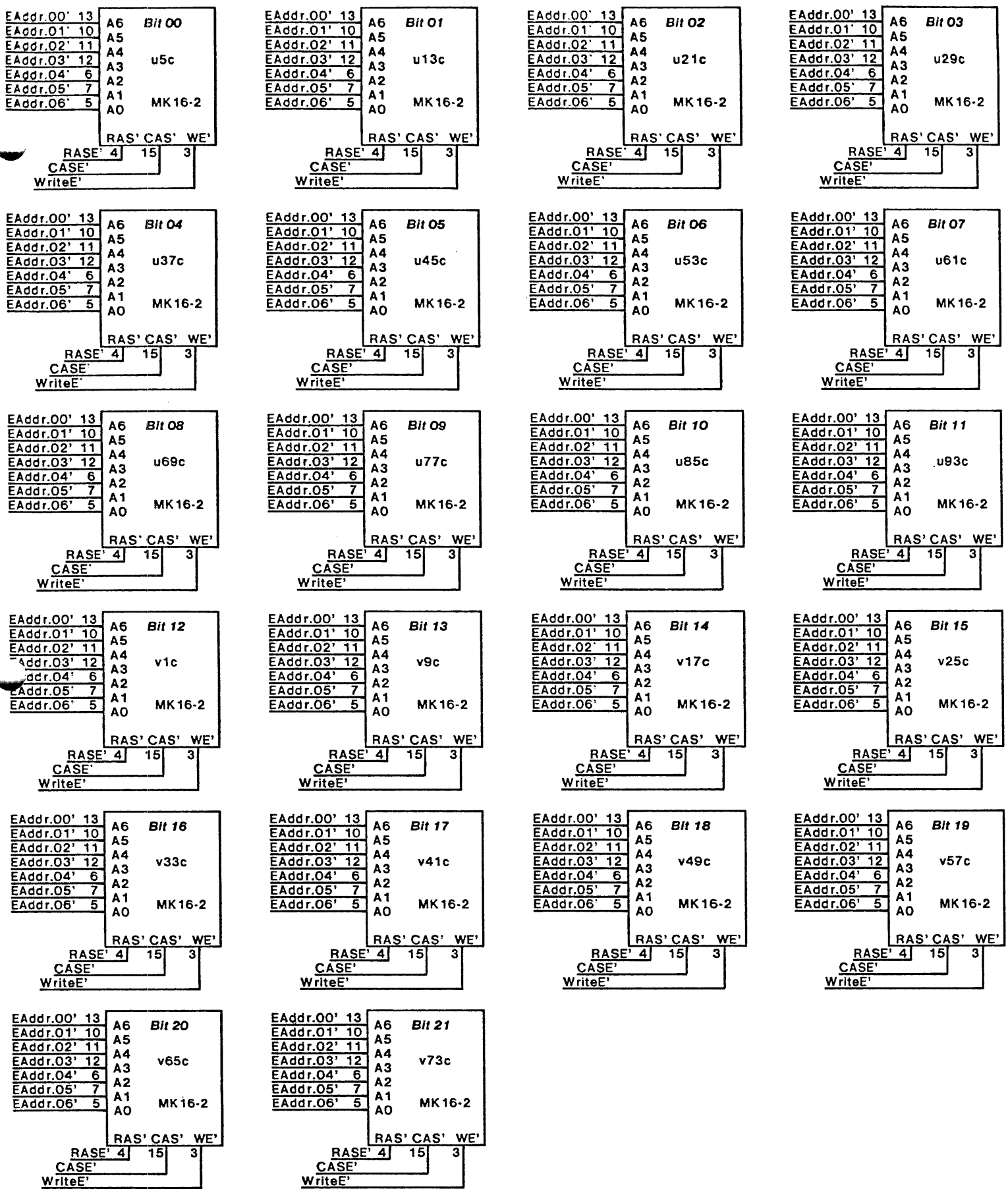
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 05 OF	



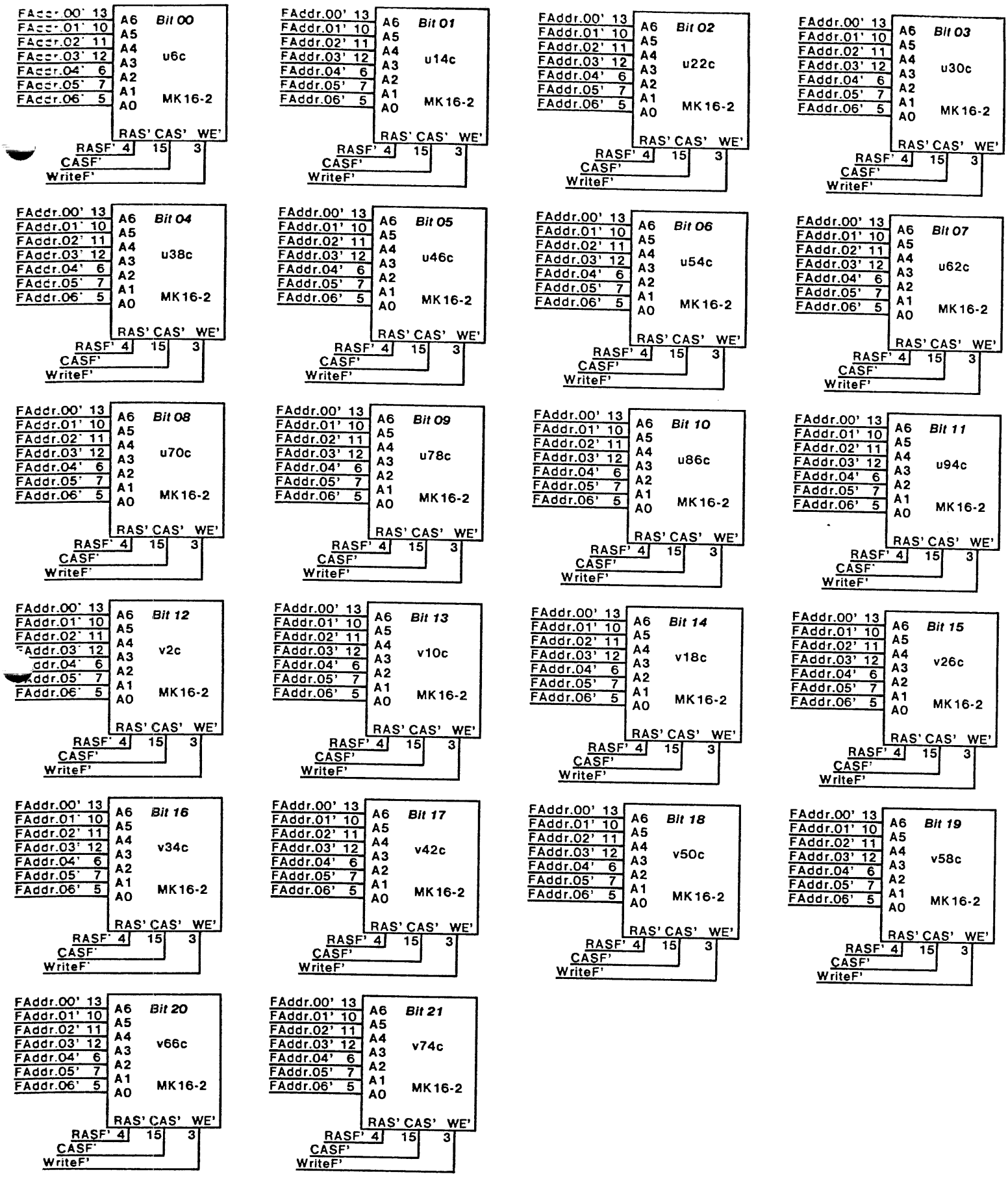
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 06 OF	B



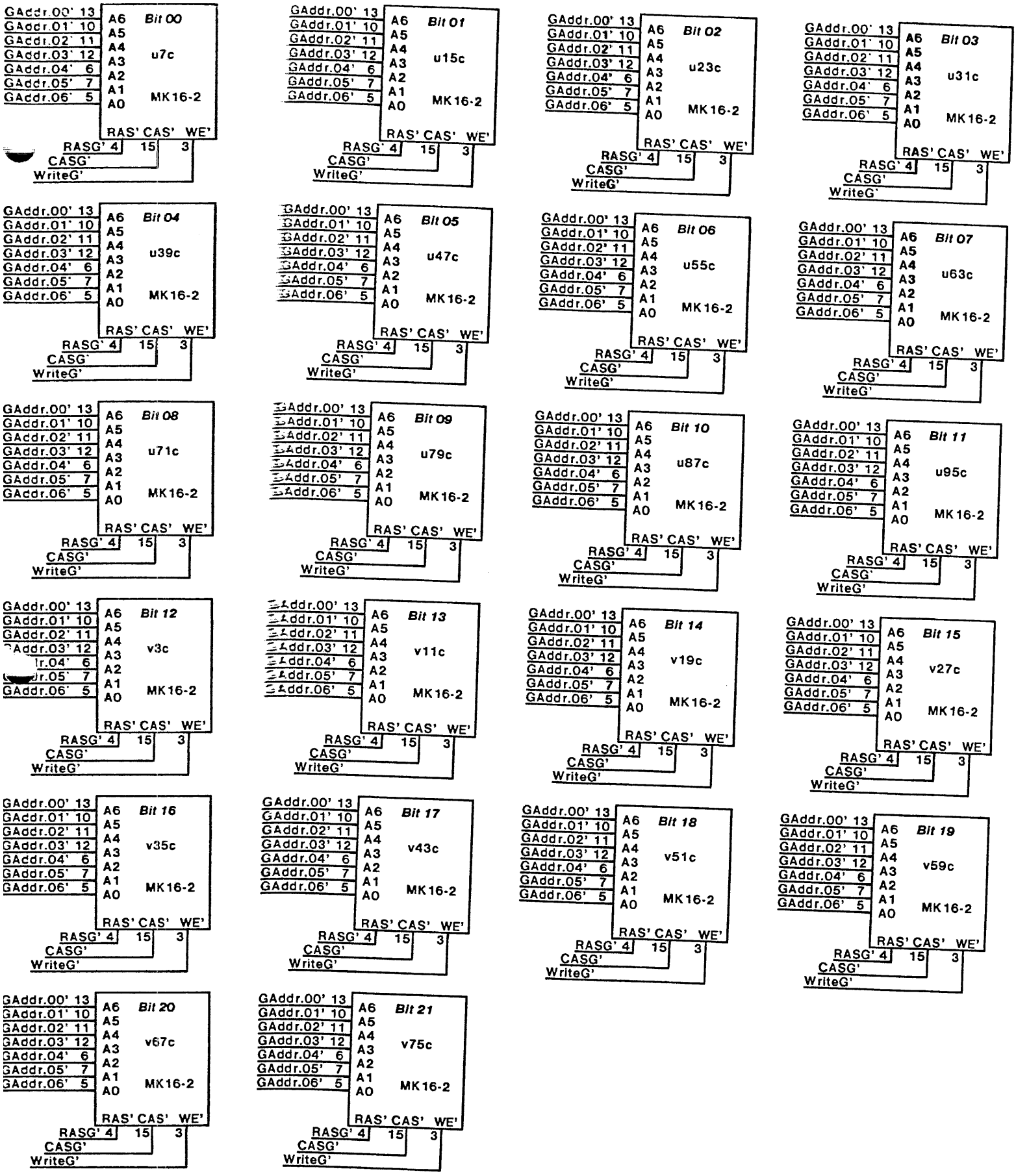
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 07 OF	



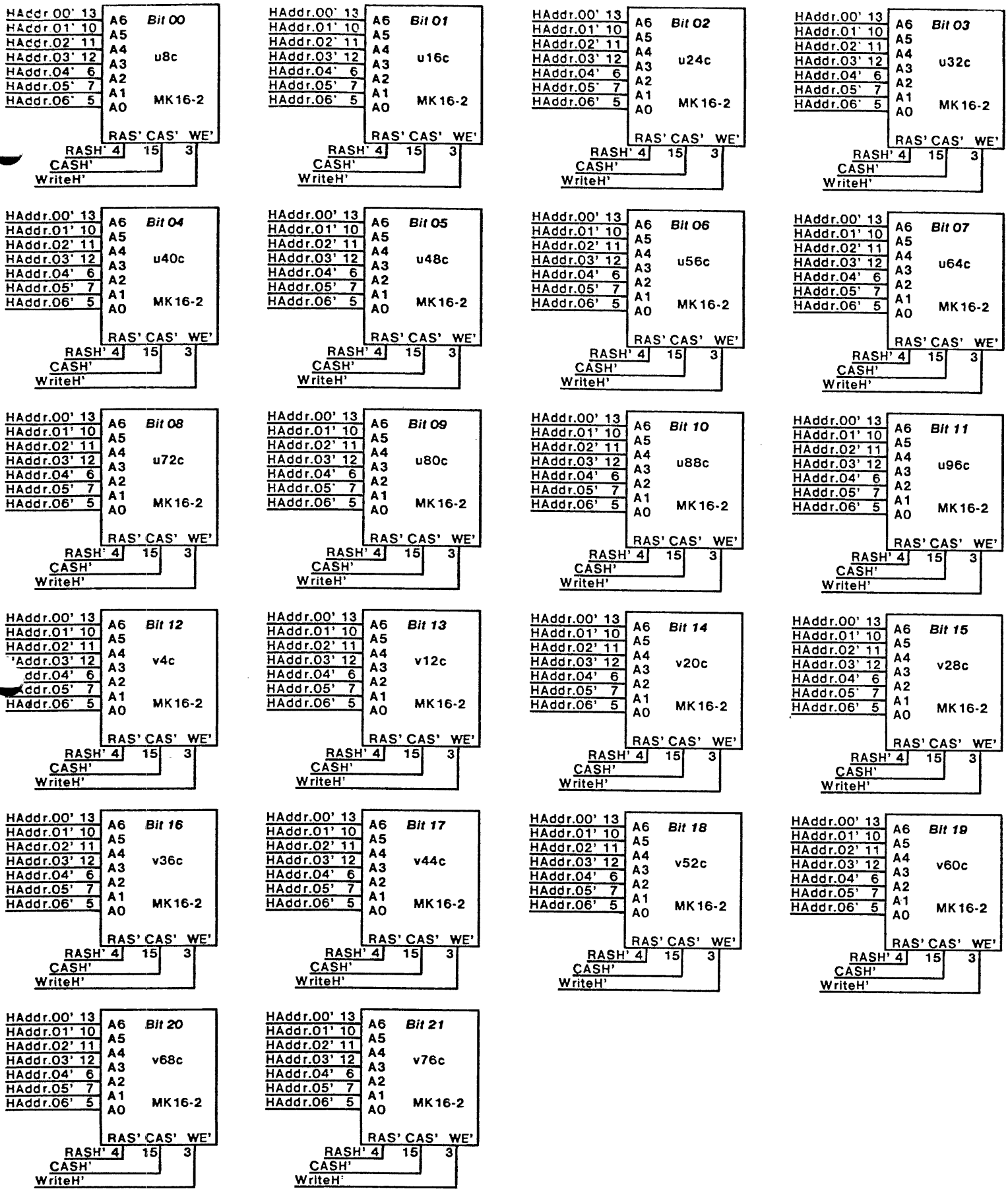
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 08 OF	B



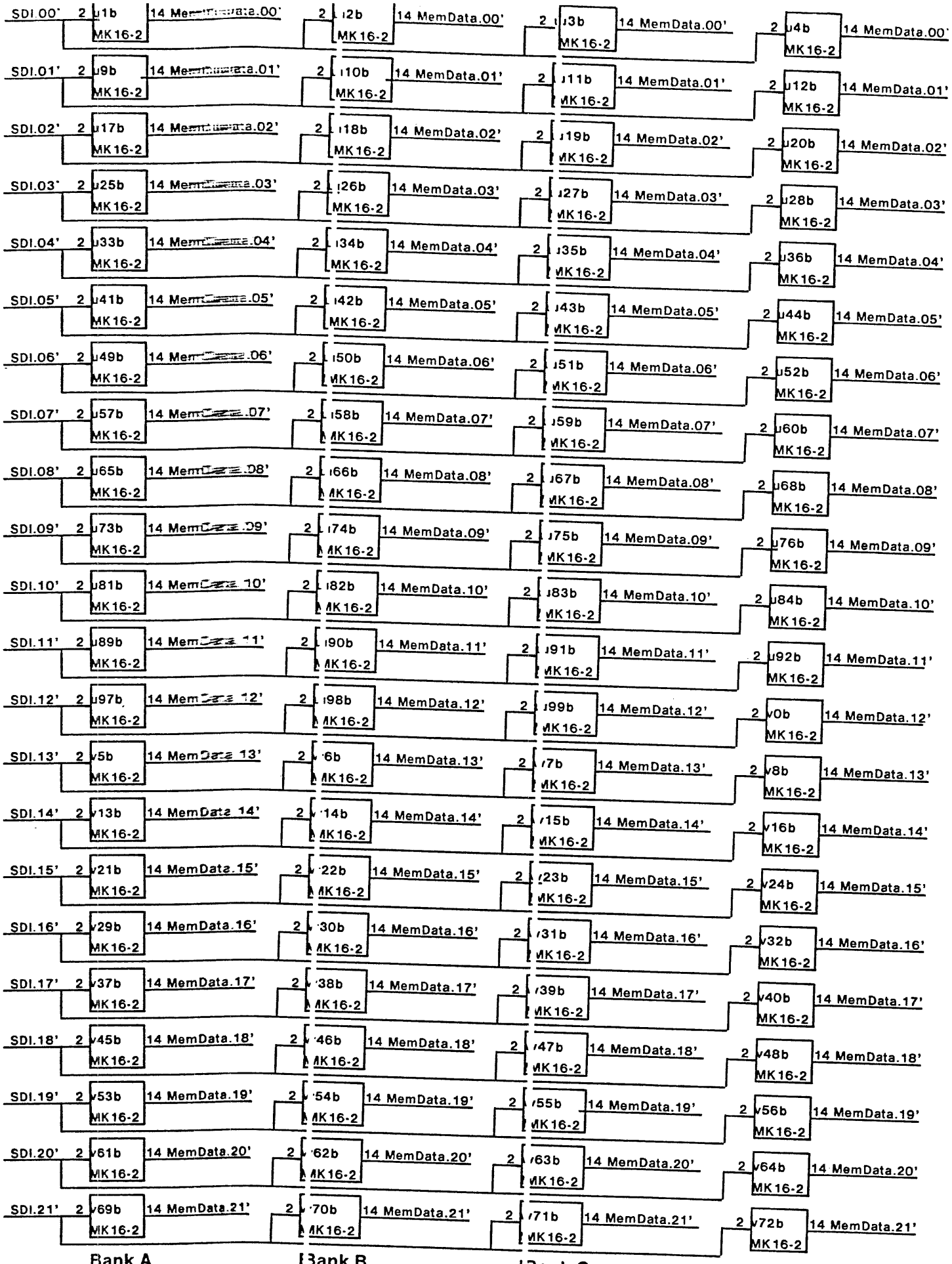
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 09 OF	B



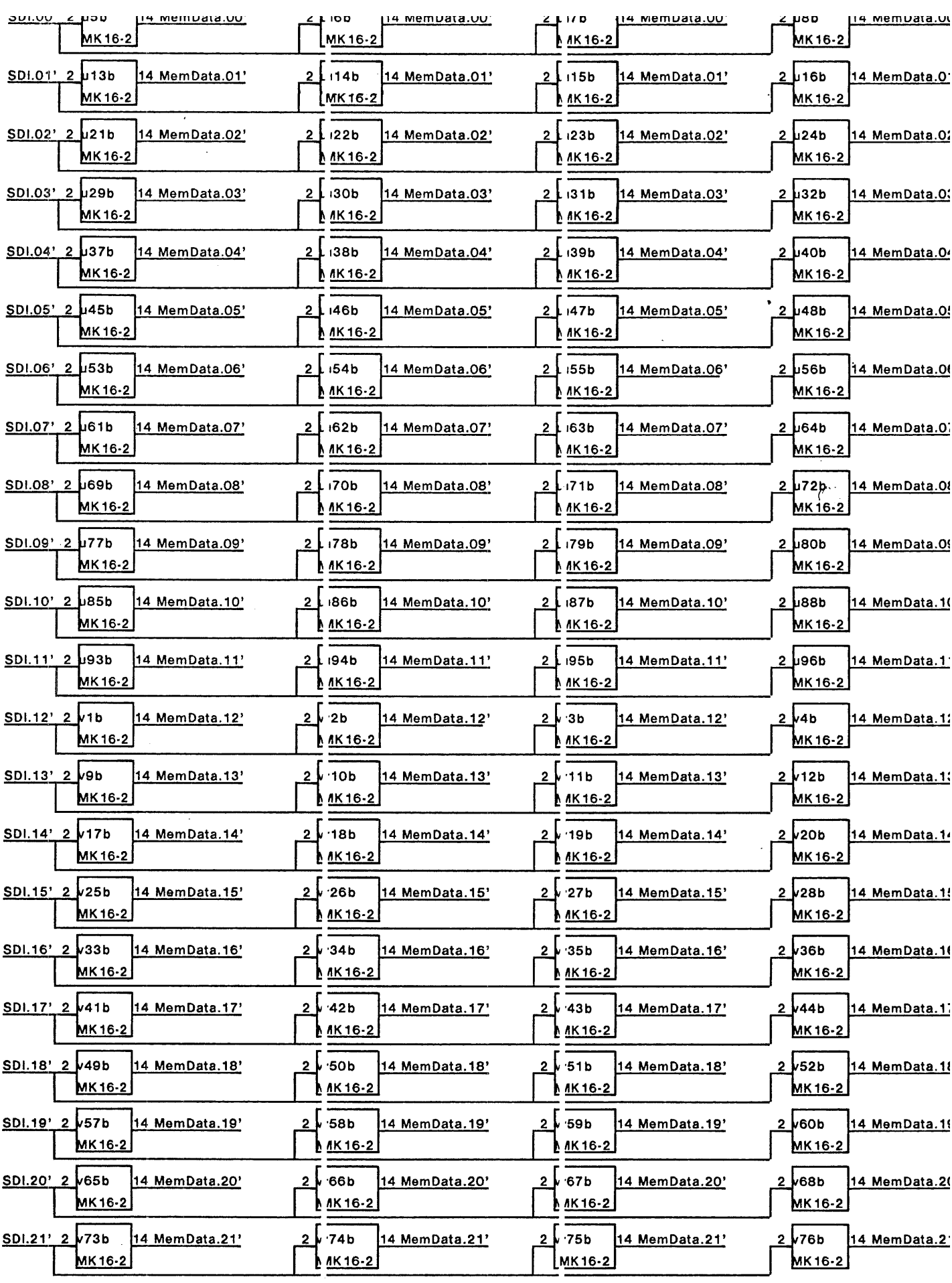
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 10 OF	



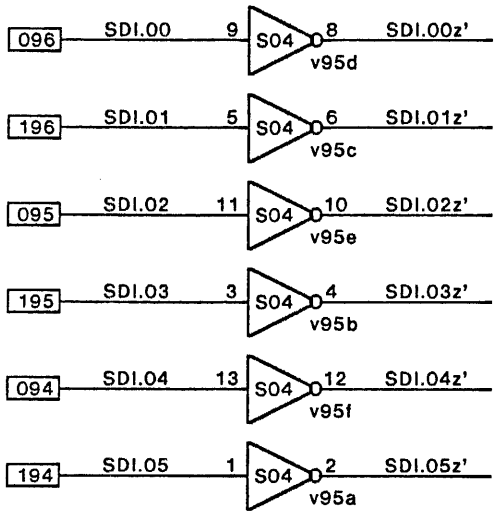
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC			SHEET 11 OF	

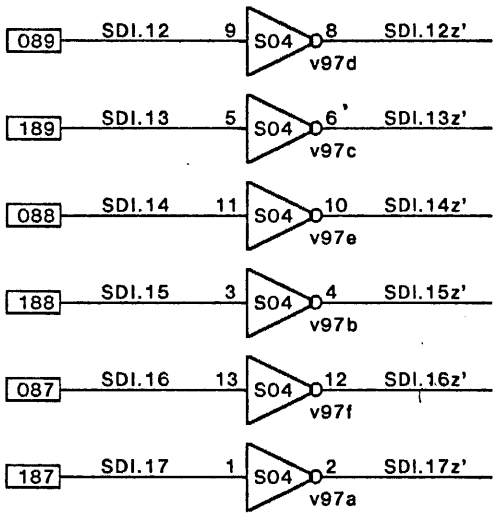


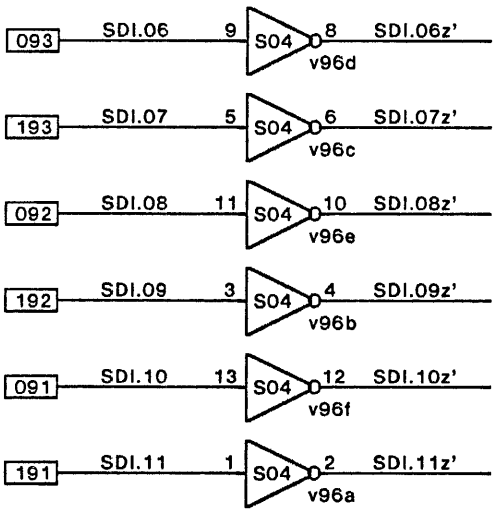
XEROX	PROPRIETARY NOTE ON COVER SHEET A PPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 12 OF	

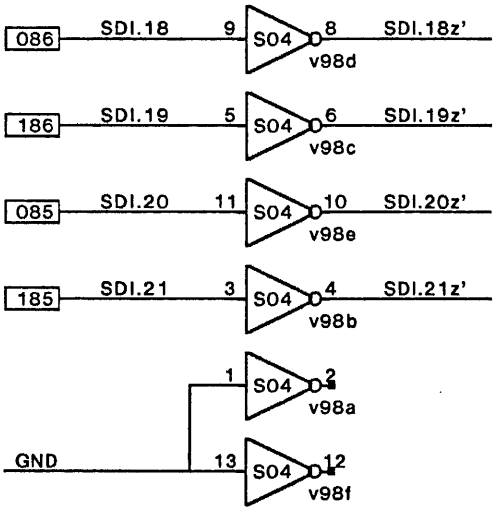


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 13 OF	

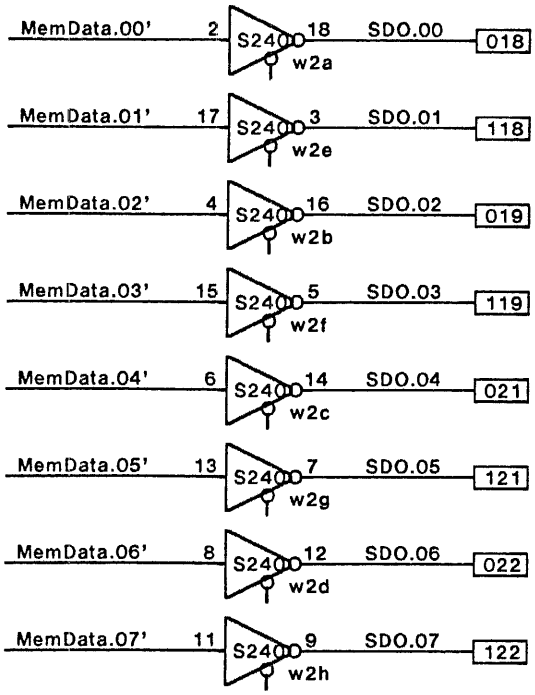


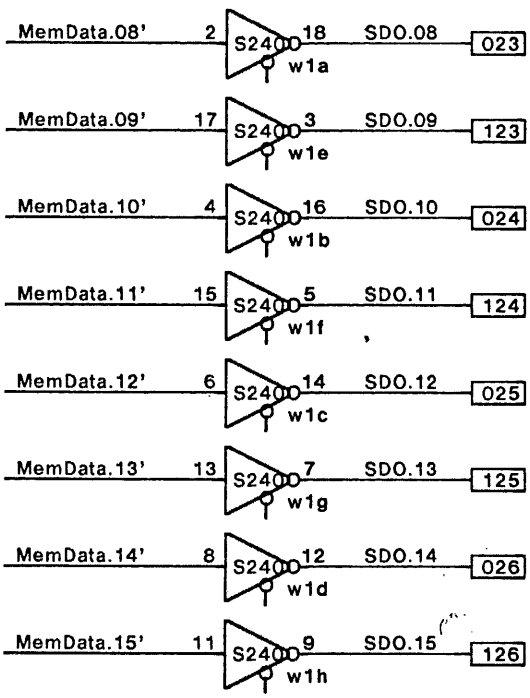


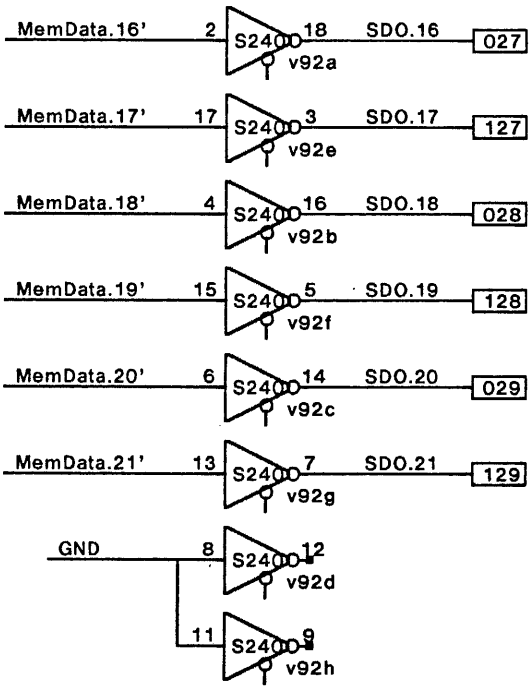


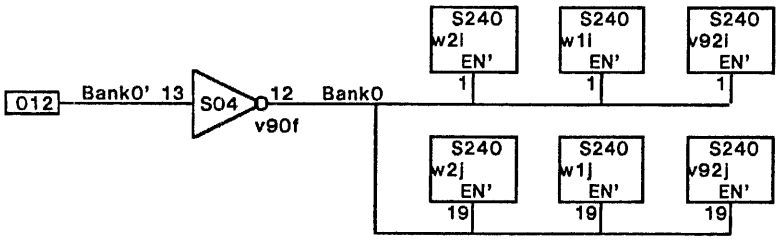


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 14 OF	B

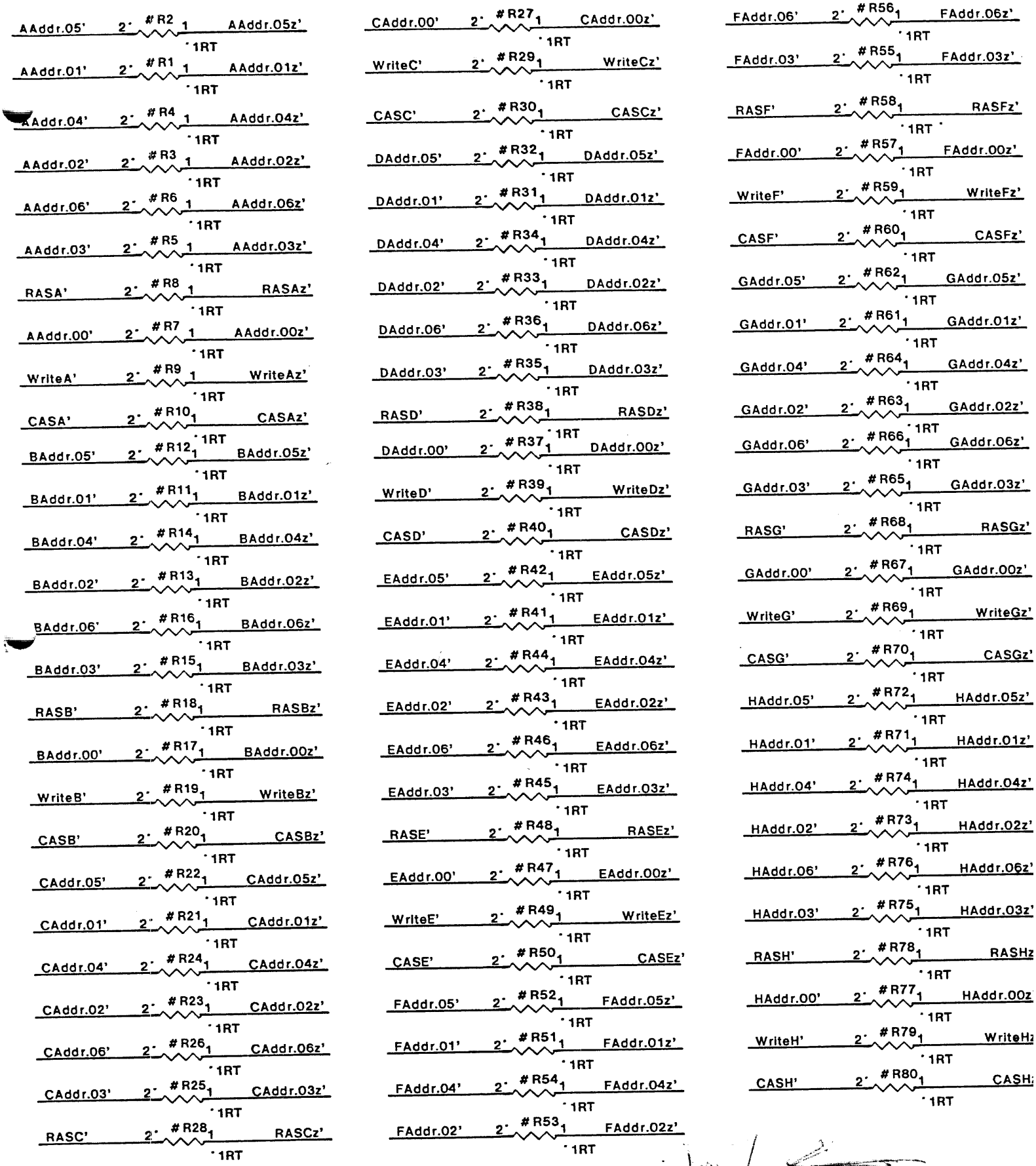




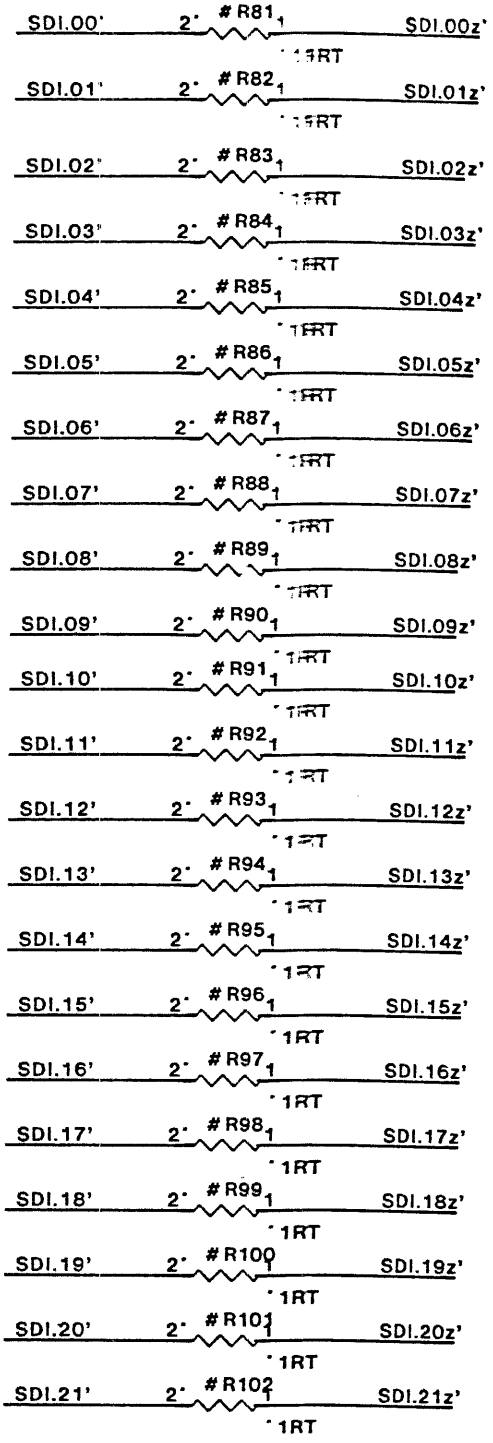


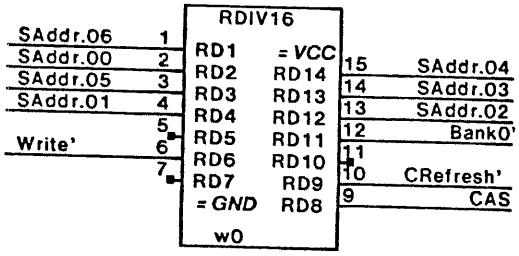


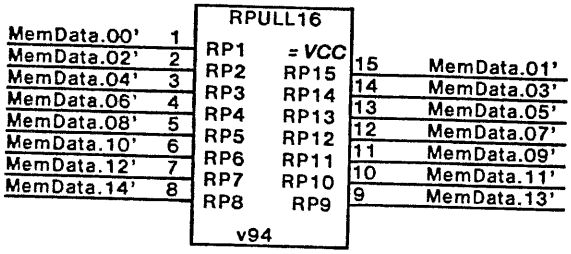
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 15 OF	B

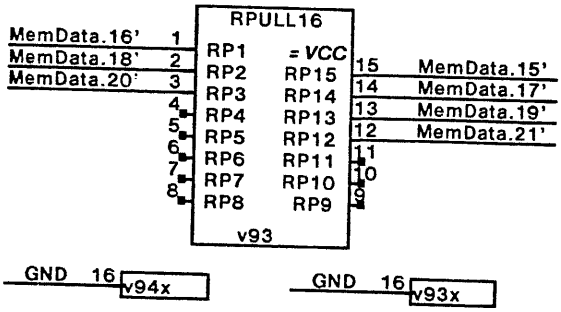


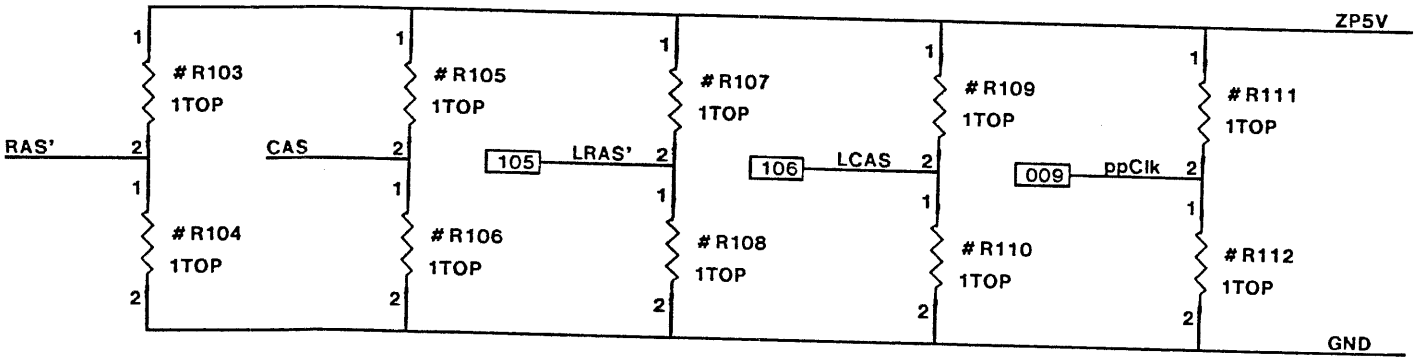
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 16 OF	B



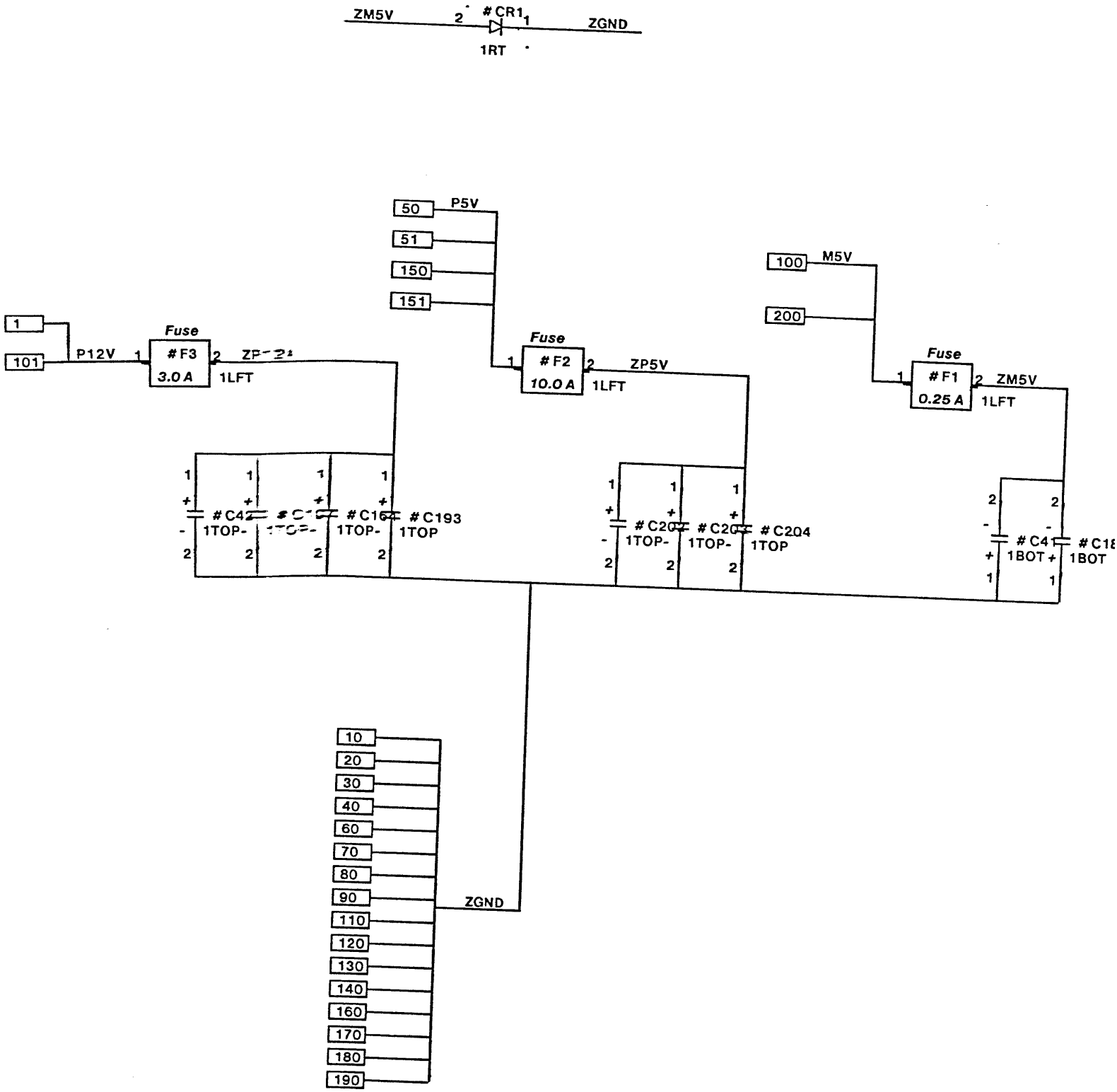




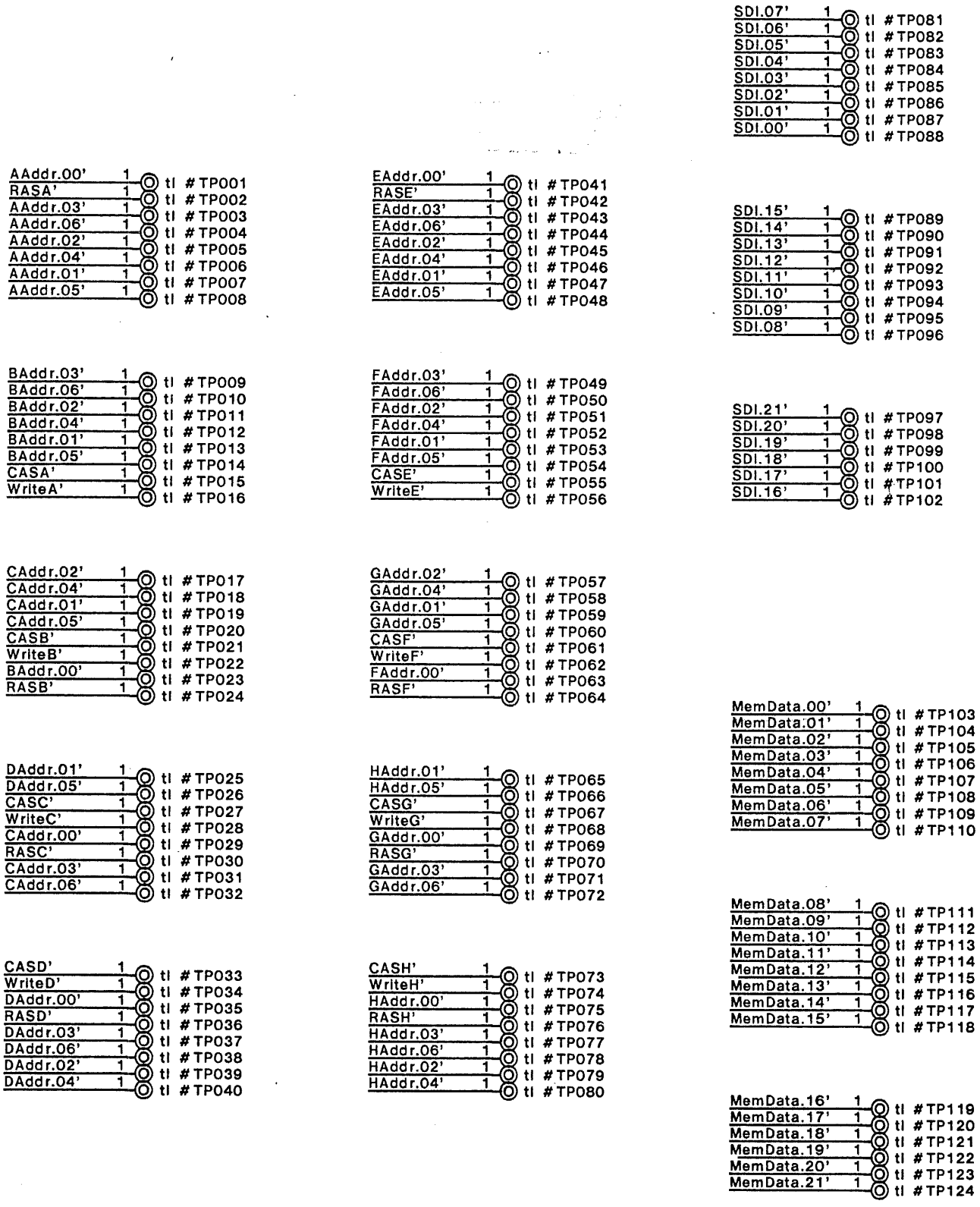




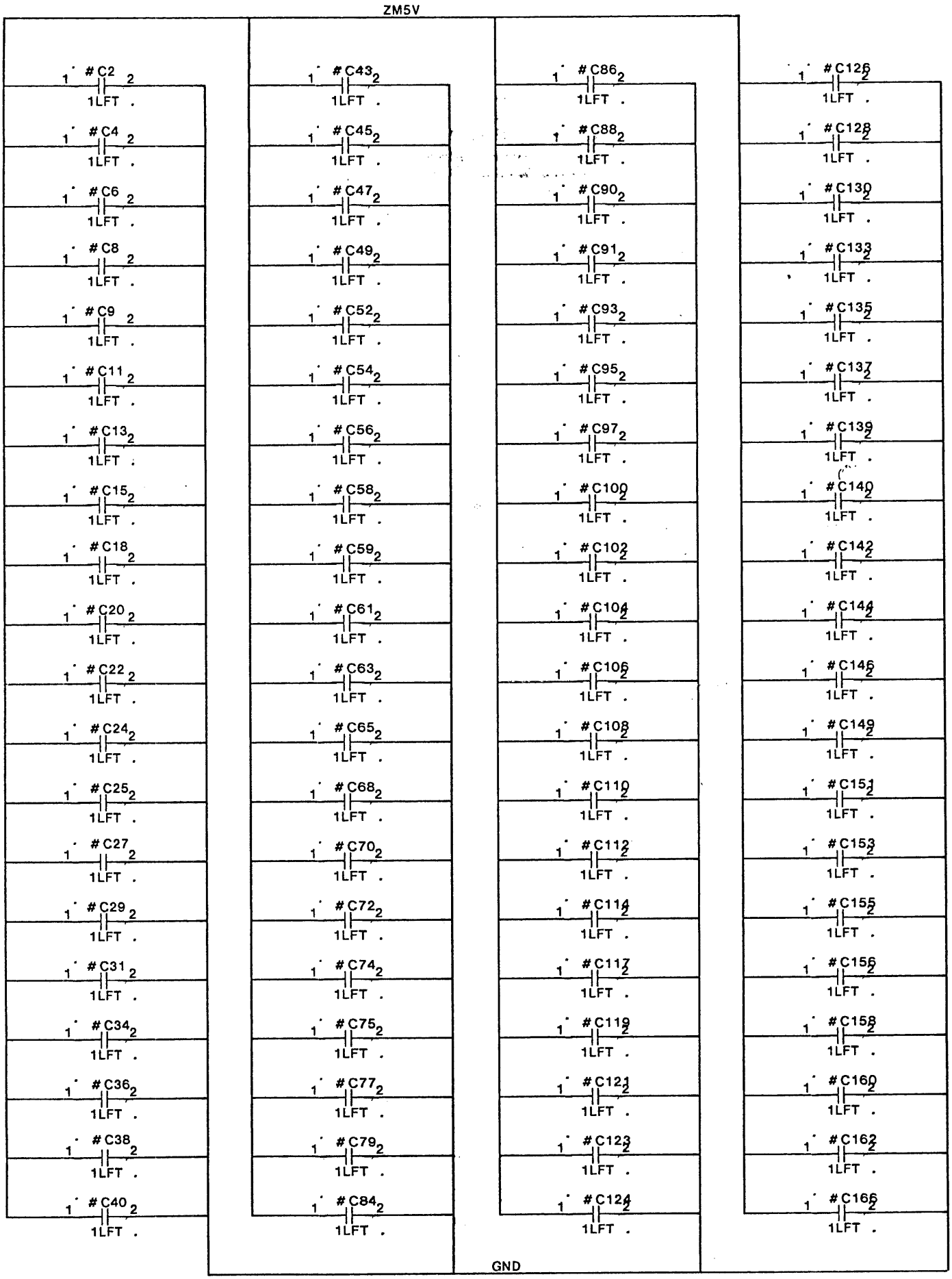
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 17 OF	B



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 18 OF	

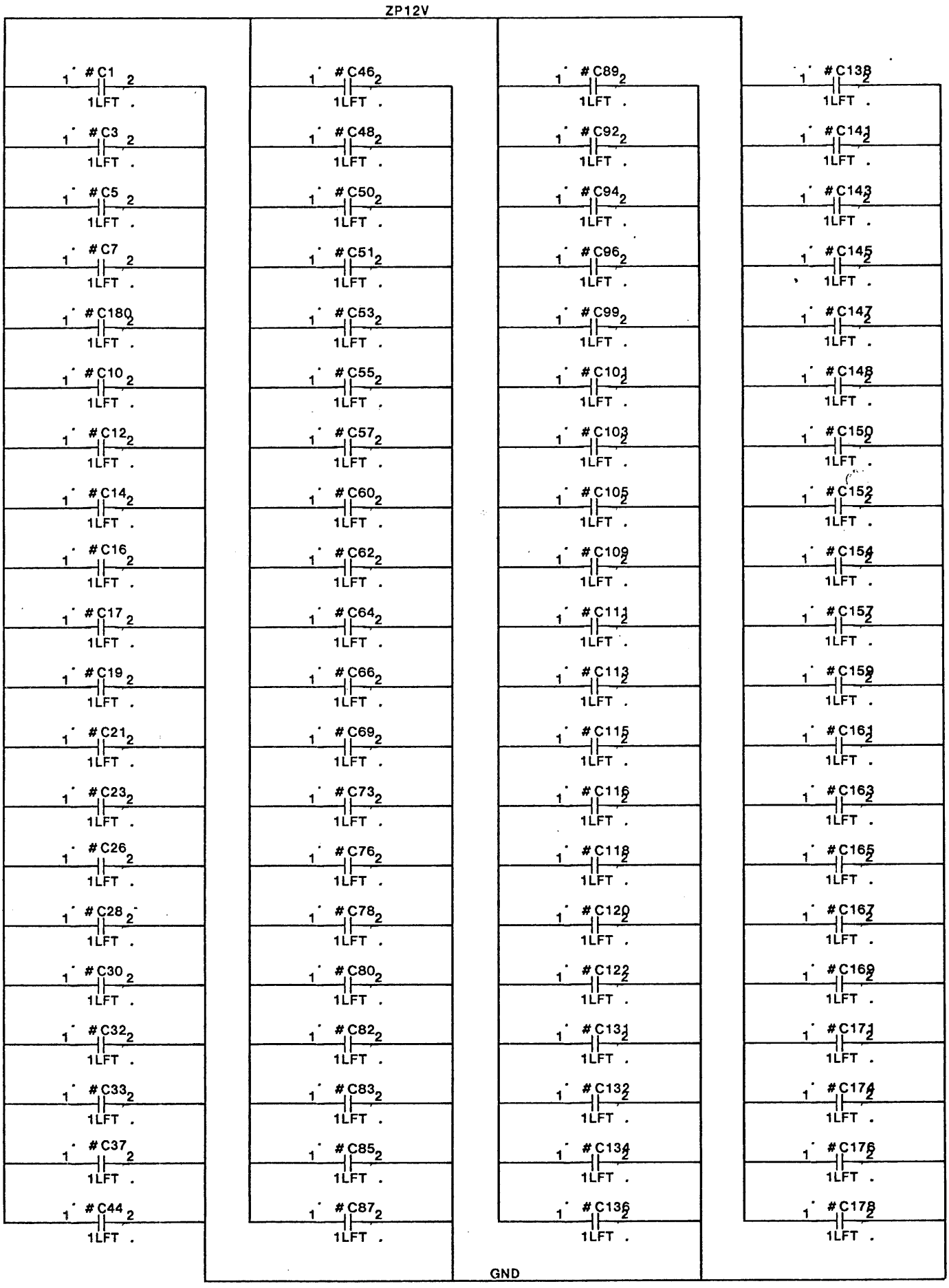


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 19 OF	B



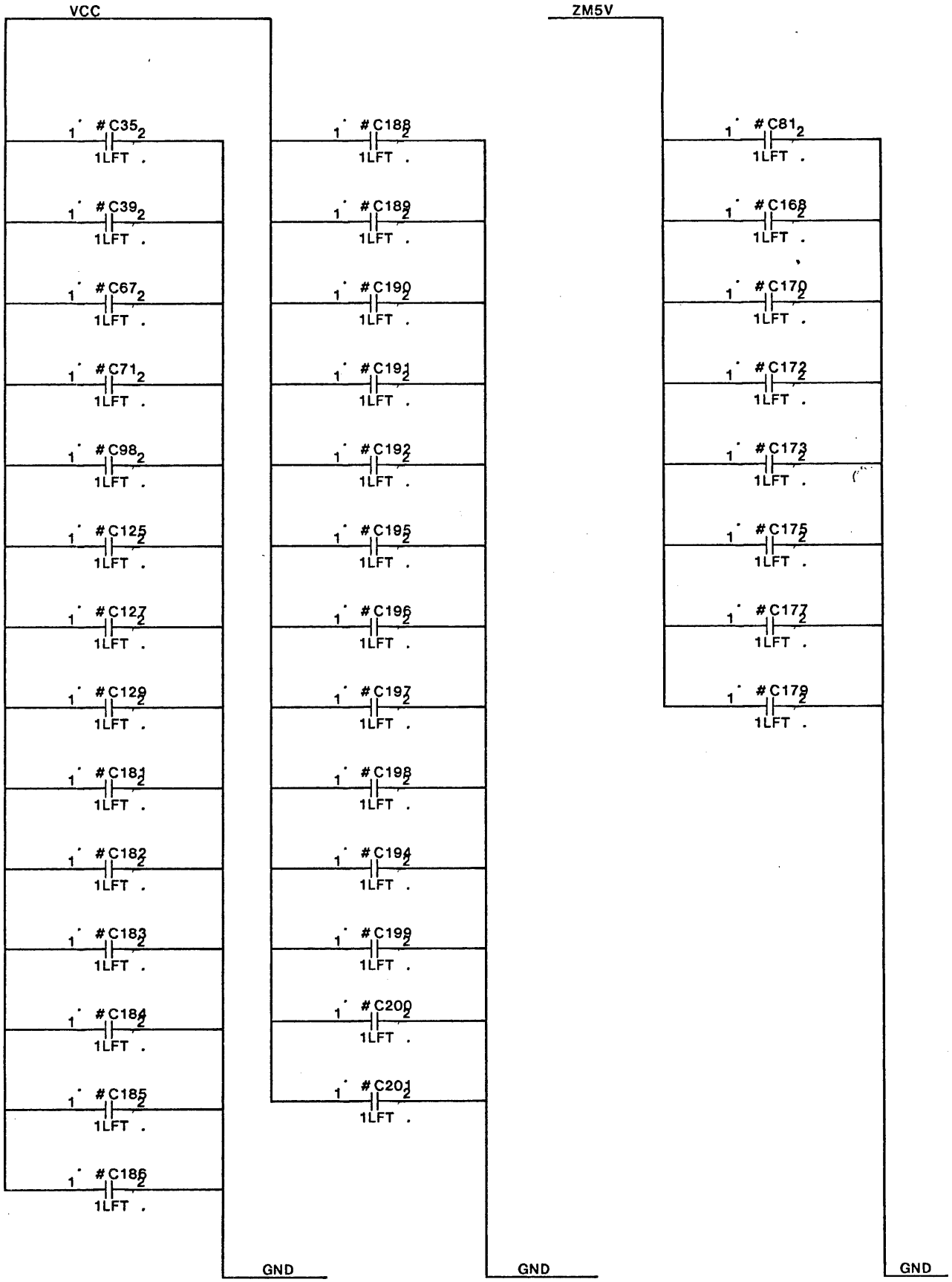
NOTE: ALL CAPACITORS ARE CERAMIC FILTER CAPS, PART # 102P20600

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 20 OF	



NOTE: ALL CAPACITORS ARE CERAMIC FILTER CAPS, PART # 102P20600

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 21 OF	



NOTE: ALL CAPACITORS ARE CERAMIC FILTER CAPS, PART # 102P20600

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11186	SHEET REV. B
	TITLE SCHEMATIC, MSC		SHEET 22 OF	

Comments:

1) *Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299*
2) *The last item on lines below, preceeded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.*
3) *Line with no page number was a continuation of the previous line.*

```
#TP001    .1i  AAddr.00'        ;20
#TP002    .1i  RASA'            ;20
#TP003    .1i  AAddr.03'        ;20
#TP004    .1i  AAddr.06'        ;20
#TP005    .1i  AAddr.02'        ;20
#TP006    .1i  AAddr.04'        ;20
#TP007    .1i  AAddr.01'        ;20
#TP008    .1i  AAddr.05'        ;20
#TP009    .1i  BAddr.03'        ;20
#TP010    .1i  BAddr.06'        ;20
#TP011    .1i  BAddr.02'        ;20
#TP012    .1i  BAddr.04'        ;20
#TP013    .1i  BAddr.01'        ;20
#TP014    .1i  BAddr.05'        ;20
#TP015    .1i  CASA'            ;20
#TP016    .1i  WriteA'          ;20
#TP017    .1i  CAddr.02'        ;20
#TP018    .1i  CAddr.04'        ;20
#TP019    .1i  CAddr.01'        ;20
#TP020    .1i  CAddr.05'        ;20
#TP021    .1i  CASB'            ;20
#TP022    .1i  WriteB'          ;20
#TP023    .1i  BAddr.00'        ;20
#TP024    .1i  RASB'            ;20
#TP025    .1i  DAddr.01'        ;20
#TP026    .1i  DAddr.05'        ;20
#TP027    .1i  CASC'            ;20
#TP028    .1i  WriteC'          ;20
#TP029    .1i  CAddr.00'        ;20
#TP030    .1i  RASC'            ;20
#TP031    .1i  CAddr.03'        ;20
#TP032    .1i  CAddr.06'        ;20
#TP033    .1i  CASD'            ;20
#TP034    .1i  WriteD'          ;20
#TP035    .1i  DAddr.00'        ;20
#TP036    .1i  RASD'            ;20
#TP037    .1i  DAddr.03'        ;20
#TP038    .1i  DAddr.06'        ;20
#TP039    .1i  DAddr.02'        ;20
#TP040    .1i  DAddr.04'        ;20
#TP041    .1i  EAddr.00'        ;20
#TP042    .1i  RASE'            ;20
#TP043    .1i  EAddr.03'        ;20
#TP044    .1i  EAddr.06'        ;20
#TP045    .1i  EAddr.02'        ;20
#TP046    .1i  EAddr.04'        ;20
#TP047    .1i  EAddr.01'        ;20
#TP048    .1i  EAddr.05'        ;20
#TP049    .1i  FAddr.03'        ;20
#TP050    .1i  FAddr.06'        ;20
#TP051    .1i  FAddr.02'        ;20
#TP052    .1i  FAddr.04'        ;20
#TP053    .1i  FAddr.01'        ;20
#TP054    .1i  FAddr.05'        ;20
#TP055    .1i  CASE'            ;20
#TP056    .1i  WriteE'          ;20
#TP057    .1i  GAddr.02'        ;20
#TP058    .1i  GAddr.04'        ;20
#TP059    .1i  GAddr.01'        ;20
#TP060    .1i  GAddr.05'        ;20
#TP061    .1i  CASF'            ;20
#TP062    .1i  WriteF'          ;20
#TP063    .1i  FAddr.00'        ;20
#TP064    .1i  RASF'            ;20
#TP065    .1i  HAddr.01'        ;20
#TP066    .1i  HAddr.05'        ;20
#TP067    .1i  CASG'            ;20
#TP068    .1i  WriteG'          ;20
#TP069    .1i  GAddr.00'        ;20
#TP070    .1i  RASG'            ;20
#TP071    .1i  GAddr.03'        ;20
#TP072    .1i  GAddr.06'        ;20
#TP073    .1i  CASH'            ;20
#TP074    .1i  WriteH'          ;20
#TP075    .1i  HAddr.00'        ;20
#TP076    .1i  RASH'            ;20
#TP077    .1i  HAddr.03'        ;20
#TP078    .1i  HAddr.06'        ;20
#TP079    .1i  HAddr.02'        ;20
#TP080    .1i  HAddr.04'        ;20
#TP081    .1i  SDI.07'          ;20
#TP082    .1i  SDI.06'          ;20
#TP083    .1i  SDI.05'          ;20
#TP084    .1i  SDI.04'          ;20
#TP085    .1i  SDI.03'          ;20
#TP086    .1i  SDI.02'          ;20
#TP087    .1i  SDI.01'          ;20
#TP088    .1i  SDI.00'          ;20
#TP089    .1i  SDI.15'          ;20
#TP090    .1i  SDI.14'          ;20
#TP091    .1i  SDI.13'          ;20
#TP092    .1i  SDI.12'          ;20
#TP093    .1i  SDI.11'          ;20
#TP094    .1i  SDI.10'          ;20
#TP095    .1i  SDI.09'          ;20
#TP096    .1i  SDI.08'          ;20
#TP097    .1i  SDI.21'          ;20
#TP098    .1i  SDI.20'          ;20
#TP099    .1i  SDI.19'          ;20
#TP100    .1i  SDI.18'          ;20
#TP101    .1i  SDI.17'          ;20
#TP102    .1i  SDI.16'          ;20
```

```
#TP103    .1i  MemData.00'     ;20
#TP104    .1i  MemData.01'     ;20
#TP105    .1i  MemData.02'     ;20
#TP106    .1i  MemData.03'     ;20
#TP107    .1i  MemData.04'     ;20
#TP108    .1i  MemData.05'     ;20
#TP109    .1i  MemData.06'     ;20
#TP110    .1i  MemData.07'     ;20
#TP111    .1i  MemData.08'     ;20
#TP112    .1i  MemData.09'     ;20
#TP113    .1i  MemData.10'     ;20
#TP114    .1i  MemData.11'     ;20
#TP115    .1i  MemData.12'     ;20
#TP116    .1i  MemData.13'     ;20
#TP117    .1i  MemData.14'     ;20
#TP118    .1i  MemData.15'     ;20
#TP119    .1i  MemData.16'     ;20
#TP120    .1i  MemData.17'     ;20
#TP121    .1i  MemData.18'     ;20
#TP122    .1i  MemData.19'     ;20
#TP123    .1i  MemData.20'     ;20
#TP124    .1i  MemData.21'     ;20

E001          P12V             ;19
E005          RAS'             ;02
E006          CAS              ;02
E009          ppClk            ;18
E010          ZGND             ;19
E012          Bank0'           ;16
E018          SDO.00           ;16
E019          SDO.02           ;16
E020          ZGND             ;19
E021          SDO.04           ;16
E022          SDO.06           ;16
E023          SDO.08           ;16
E024          SDO.10           ;16
E025          SDO.12           ;16
E026          SDO.14           ;16
E027          SDO.16           ;16
E028          SDO.18           ;16
E029          SDO.20           ;16
E030          ZGND             ;19
E032          SAddr.00         ;03
E033          SAddr.02         ;03
E034          SAddr.04         ;03
E035          SAddr.06         ;03
E036          LatchY.01        ;02
E037          Bank1'           ;02
E038          MRef'            ;02
E040          ZGND             ;19
E050          P5V              ;19
E051          P5V              ;19
E060          ZGND             ;19
E070          ZGND             ;19
E080          ZGND             ;19
E085          SDI.20           ;15
E086          SDI.18           ;15
E087          SDI.16           ;15
E088          SDI.14           ;15
E089          SDI.12           ;15
E090          ZGND             ;19
E091          SDI.10           ;15
E092          SDI.08           ;15
E093          SDI.06           ;15
E094          SDI.04           ;15
E095          SDI.02           ;15
E096          SDI.00           ;15
E100          M5V              ;19
E101          P12V             ;19
E105          LRAS'            ;18
E106          LCAS             ;18
E110          ZGND             ;19
E116          CRefresh'        ;02
E118          SDO.01           ;16
E119          SDO.03           ;16
E120          ZGND             ;19
E121          SDO.05           ;16
E122          SDO.07           ;16
E123          SDO.09           ;16
E124          SDO.11           ;16
E125          SDO.13           ;16
E126          SDO.15           ;16
E127          SDO.17           ;16
E128          SDO.19           ;16
E129          SDO.21           ;16
E130          ZGND             ;19
E132          SAddr.01         ;03
E133          SAddr.03         ;03
E134          SAddr.05         ;03
E136          LatchY.00        ;02
E137          Bank2'           ;02
E138          Write'           ;03
E140          ZGND             ;19
E150          P5V              ;19
E151          P5V              ;19
E160          ZGND             ;19
E170          ZGND             ;19
E180          ZGND             ;19
E185          SDI.21           ;15
E186          SDI.19           ;15
E187          SDI.17           ;15
E188          SDI.15           ;15
E189          SDI.13           ;15
E190          ZGND             ;19
E191          SDI.11           ;15
E192          SDI.09           ;15
E193          SDI.07           ;15
E194          SDI.05           ;15
E195          SDI.03           ;15
E196          SDI.01           ;15
E200          M5V              ;19

AAddr.00': u01.13i  ;05
AAddr.00': u09.13i  ;05
AAddr.00': u17.13i  ;05
AAddr.00': u25.13i  ;05
AAddr.00': u33.13i  ;05
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XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 24 OF	B

```
AAddr.00': u41.13i  ;05
AAddr.00': u49.13i  ;05
AAddr.00': u57.13i  ;05
AAddr.00': u65.13i  ;05
AAddr.00': u73.13i  ;05
AAddr.00': u81.13i  ;05
AAddr.00': u89.13i  ;05
AAddr.00': u97.13i  ;05
AAddr.00': v05.13i  ;05
AAddr.00': v13.13i  ;05
AAddr.00': v21.13i  ;05
AAddr.00': v29.13i  ;05
AAddr.00': v37.13i  ;05
AAddr.00': v45.13i  ;05
AAddr.00': v53.13i  ;05
AAddr.00': v61.13i  ;05
AAddr.00': v69.13i  ;05
AAddr.00': #R7.2i   ;17
AAddr.00': #TP001.1i   ;20

AAddr.00z':   v77.18o  ;03
AAddr.00z':   #R7.1o   ;17

AAddr.01': u01.10i  ;05
AAddr.01': u09.10i  ;05
AAddr.01': u17.10i  ;05
AAddr.01': u25.10i  ;05
AAddr.01': u33.10i  ;05
AAddr.01': u41.10i  ;05
AAddr.01': u49.10i  ;05
AAddr.01': u57.10i  ;05
AAddr.01': u65.10i  ;05
AAddr.01': u73.10i  ;05
AAddr.01': u81.10i  ;05
AAddr.01': u89.10i  ;05
AAddr.01': u97.10i  ;05
AAddr.01': v05.10i  ;05
AAddr.01': v13.10i  ;05
AAddr.01': v21.10i  ;05
AAddr.01': v29.10i  ;05
AAddr.01': v37.10i  ;05
AAddr.01': v45.10i  ;05
AAddr.01': v53.10i  ;05
AAddr.01': v61.10i  ;05
AAddr.01': v69.10i  ;05
AAddr.01': #R1.2i   ;17
AAddr.01': #TP007.1i   ;20

AAddr.01z':   v77.12o  ;03
AAddr.01z':   #R1.1o   ;17

AAddr.02': u01.11i  ;05
AAddr.02': u09.11i  ;05
AAddr.02': u17.11i  ;05
AAddr.02': u25.11i  ;05
AAddr.02': u33.11i  ;05
AAddr.02': u41.11i  ;05
AAddr.02': u49.11i  ;05
AAddr.02': u57.11i  ;05
AAddr.02': u65.11i  ;05
AAddr.02': u73.11i  ;05
AAddr.02': u81.11i  ;05
AAddr.02': u89.11i  ;05
AAddr.02': u97.11i  ;05
AAddr.02': v05.11i  ;05
AAddr.02': v13.11i  ;05
AAddr.02': v21.11i  ;05
AAddr.02': v29.11i  ;05
AAddr.02': v37.11i  ;05
AAddr.02': v45.11i  ;05
AAddr.02': v53.11i  ;05
AAddr.02': v61.11i  ;05
AAddr.02': v69.11i  ;05
AAddr.02': #R3.2i   ;17
AAddr.02': #TP005.1i   ;20

AAddr.02z':   v77.14o  ;03
AAddr.02z':   #R3.1o   ;17

AAddr.03': u01.12i  ;05
AAddr.03': u09.12i  ;05
AAddr.03': u17.12i  ;05
AAddr.03': u25.12i  ;05
AAddr.03': u33.12i  ;05
AAddr.03': u41.12i  ;05
AAddr.03': u49.12i  ;05
AAddr.03': u57.12i  ;05
AAddr.03': u65.12i  ;05
AAddr.03': u73.12i  ;05
AAddr.03': u81.12i  ;05
AAddr.03': u89.12i  ;05
AAddr.03': u97.12i  ;05
AAddr.03': v05.12i  ;05
AAddr.03': v13.12i  ;05
AAddr.03': v21.12i  ;05
AAddr.03': v29.12i  ;05
AAddr.03': v37.12i  ;05
AAddr.03': v45.12i  ;05
AAddr.03': v53.12i  ;05
AAddr.03': v61.12i  ;05
AAddr.03': v69.12i  ;05
AAddr.03': #R5.2i   ;17
AAddr.03': #TP003.1i   ;20

AAddr.03z':   v77.16o  ;03
AAddr.03z':   #R5.1o   ;17

AAddr.04': u01.6i   ;05
AAddr.04': u09.6i   ;05
AAddr.04': u17.6i   ;05
AAddr.04': u25.6i   ;05
AAddr.04': u33.6i   ;05
AAddr.04': u41.6i   ;05
AAddr.04': u49.6i   ;05
AAddr.04': u57.6i   ;05
AAddr.04': u65.6i   ;05
AAddr.04': u73.6i   ;05
AAddr.04': u81.6i   ;05
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XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 25 OF	B

```
AAddr.04': u89.6i   ;05
AAddr.04': u97.6i   ;05
AAddr.04': v05.6i   ;05
AAddr.04': v13.6i   ;05
AAddr.04': v21.6i   ;05
AAddr.04': v29.6i   ;05
AAddr.04': v37.6i   ;05
AAddr.04': v45.6i   ;05
AAddr.04': v53.6i   ;05
AAddr.04': v61.6i   ;05
AAddr.04': v69.6i   ;05
AAddr.04': #R4.2i   ;17
AAddr.04': #TP006.1i   ;20

AAddr.04z':   v77.7o   ;03
AAddr.04z':   #R4.1o   ;17

AAddr.05': u01.7i   ;05
AAddr.05': u09.7i   ;05
AAddr.05': u17.7i   ;05
AAddr.05': u25.7i   ;05
AAddr.05': u33.7i   ;05
AAddr.05': u41.7i   ;05
AAddr.05': u49.7i   ;05
AAddr.05': u57.7i   ;05
AAddr.05': u65.7i   ;05
AAddr.05': u73.7i   ;05
AAddr.05': u81.7i   ;05
AAddr.05': u89.7i   ;05
AAddr.05': u97.7i   ;05
AAddr.05': v05.7i   ;05
AAddr.05': v13.7i   ;05
AAddr.05': v21.7i   ;05
AAddr.05': v29.7i   ;05
AAddr.05': v37.7i   ;05
AAddr.05': v45.7i   ;05
AAddr.05': v53.7i   ;05
AAddr.05': v61.7i   ;05
AAddr.05': v69.7i   ;05
AAddr.05': #R2.2i   ;17
AAddr.05': #TP008.1i   ;20

AAddr.05z':   v77.9o   ;03
AAddr.05z':   #R2.1o   ;17

AAddr.06': u01.5i   ;05
AAddr.06': u09.5i   ;05
AAddr.06': u17.5i   ;05
AAddr.06': u25.5i   ;05
AAddr.06': u33.5i   ;05
AAddr.06': u41.5i   ;05
AAddr.06': u49.5i   ;05
AAddr.06': u57.5i   ;05
AAddr.06': u65.5i   ;05
AAddr.06': u73.5i   ;05
AAddr.06': u81.5i   ;05
AAddr.06': u89.5i   ;05
AAddr.06': u97.5i   ;05
AAddr.06': v05.5i   ;05
AAddr.06': v13.5i   ;05
AAddr.06': v21.5i   ;05
AAddr.06': v29.5i   ;05
AAddr.06': v37.5i   ;05
AAddr.06': v45.5i   ;05
AAddr.06': v53.5i   ;05
AAddr.06': v61.5i   ;05
AAddr.06': v69.5i   ;05
AAddr.06': #R6.2i   ;17
AAddr.06': #TP004.1i   ;20

AAddr.06z':   v77.5o   ;03
AAddr.06z':   #R6.1o   ;17

aRAS:   v90.4o, v78.9i, v78.5i  ;02
aRAS:   v78.12i, v78.2i

aWrite: v90.6o   ;03
aWrite: v77.17i  ;03
aWrite: v84.8i   ;03
aWrite: v79.11i  ;03
aWrite: v85.6i   ;03
aWrite: v80.13i  ;04
aWrite: v86.4i   ;04
aWrite: v87.15i  ;04
aWrite: v82.2i   ;04

BAddr.00': u02.13i  ;06
BAddr.00': u34.13i  ;06
BAddr.00': u66.13i  ;06
BAddr.00': u98.13i  ;06
BAddr.00': v30.13i  ;06
BAddr.00': v62.13i  ;06
BAddr.00': v70.13i  ;06
BAddr.00': v38.13i  ;06
BAddr.00': v06.13i  ;06
BAddr.00': u74.13i  ;06
BAddr.00': u42.13i  ;06
BAddr.00': u10.13i  ;06
BAddr.00': u18.13i  ;06
BAddr.00': u50.13i  ;06
BAddr.00': u82.13i  ;06
BAddr.00': v14.13i  ;06
BAddr.00': v46.13i  ;06
BAddr.00': v54.13i  ;06
BAddr.00': v22.13i  ;06
BAddr.00': u90.13i  ;06
BAddr.00': u58.13i  ;06
BAddr.00': u26.13i  ;06
BAddr.00': #R17.2i  ;17
BAddr.00': #TP023.1i   ;20

BAddr.00z':   v83.3o   ;03
BAddr.00z':   #R17.1o  ;17

BAddr.01': u02.10i  ;06
BAddr.01': u34.10i  ;06
BAddr.01': u66.10i  ;06
BAddr.01': u98.10i  ;06
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```
BAddr.01': v30.10i  ;06
BAddr.01': v62.10i  ;06
BAddr.01': v70.10i  ;06
BAddr.01': v38.10i  ;06
BAddr.01': v06.10i  ;06
BAddr.01': u74.10i  ;06
BAddr.01': u42.10i  ;06
BAddr.01': u10.10i  ;06
BAddr.01': u18.10i  ;06
BAddr.01': u50.10i  ;06
BAddr.01': u82.10i  ;06
BAddr.01': v14.10i  ;06
BAddr.01': v46.10i  ;06
BAddr.01': v54.10i  ;06
BAddr.01': v22.10i  ;06
BAddr.01': u90.10i  ;06
BAddr.01': u58.10i  ;06
BAddr.01': u26.10i  ;06
BAddr.01': #R11.2i  ;17
BAddr.01': #TP013.1i   ;20

BAddr.01z':   v83.9o   ;03
BAddr.01z':   #R11.1o  ;17

BAddr.02': u02.11i  ;06
BAddr.02': u34.11i  ;06
BAddr.02': u66.11i  ;06
BAddr.02': u98.11i  ;06
BAddr.02': v30.11i  ;06
BAddr.02': v62.11i  ;06
BAddr.02': v70.11i  ;06
BAddr.02': v38.11i  ;06
BAddr.02': v06.11i  ;06
BAddr.02': u74.11i  ;06
BAddr.02': u42.11i  ;06
BAddr.02': u10.11i  ;06
BAddr.02': u18.11i  ;06
BAddr.02': u50.11i  ;06
BAddr.02': u82.11i  ;06
BAddr.02': v14.11i  ;06
BAddr.02': v46.11i  ;06
BAddr.02': v54.11i  ;06
BAddr.02': v22.11i  ;06
BAddr.02': u90.11i  ;06
BAddr.02': u58.11i  ;06
BAddr.02': u26.11i  ;06
BAddr.02': #R13.2i  ;17
BAddr.02': #TP011.1i   ;20

BAddr.02z':   v83.7o   ;03
BAddr.02z':   #R13.1o  ;17

BAddr.03': u02.12i  ;06
BAddr.03': u34.12i  ;06
BAddr.03': u66.12i  ;06
BAddr.03': u98.12i  ;06
BAddr.03': v30.12i  ;06
BAddr.03': v62.12i  ;06
BAddr.03': v70.12i  ;06
BAddr.03': v38.12i  ;06
BAddr.03': v06.12i  ;06
BAddr.03': u74.12i  ;06
BAddr.03': u42.12i  ;06
BAddr.03': u10.12i  ;06
BAddr.03': u18.12i  ;06
BAddr.03': u50.12i  ;06
BAddr.03': u82.12i  ;06
BAddr.03': v14.12i  ;06
BAddr.03': v46.12i  ;06
BAddr.03': v54.12i  ;06
BAddr.03': v22.12i  ;06
BAddr.03': u90.12i  ;06
BAddr.03': u58.12i  ;06
BAddr.03': u26.12i  ;06
BAddr.03': #R15.2i  ;17
BAddr.03': #TP009.1i   ;20

BAddr.03z':   v83.5o   ;03
BAddr.03z':   #R15.1o  ;17

BAddr.04': u02.6i   ;06
BAddr.04': u34.6i   ;06
BAddr.04': u66.6i   ;06
BAddr.04': u98.6i   ;06
BAddr.04': v30.6i   ;06
BAddr.04': v62.6i   ;06
BAddr.04': v70.6i   ;06
BAddr.04': v38.6i   ;06
BAddr.04': v06.6i   ;06
BAddr.04': u74.6i   ;06
BAddr.04': u42.6i   ;06
BAddr.04': u10.6i   ;06
BAddr.04': u18.6i   ;06
BAddr.04': u50.6i   ;06
BAddr.04': u82.6i   ;06
BAddr.04': v14.6i   ;06
BAddr.04': v46.6i   ;06
BAddr.04': v54.6i   ;06
BAddr.04': v22.6i   ;06
BAddr.04': u90.6i   ;06
BAddr.04': u58.6i   ;06
BAddr.04': u26.6i   ;06
BAddr.04': #R14.2i  ;17
BAddr.04': #TP012.1i   ;20

BAddr.04z':   v83.16o  ;03
BAddr.04z':   #R14.1o  ;17

BAddr.05': u02.7i   ;06
BAddr.05': u34.7i   ;06
BAddr.05': u66.7i   ;06
BAddr.05': u98.7i   ;06
BAddr.05': v30.7i   ;06
BAddr.05': v62.7i   ;06
BAddr.05': v70.7i   ;06
BAddr.05': v38.7i   ;06
BAddr.05': v06.7i   ;06
BAddr.05': u74.7i   ;06
```

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 27 OF	B

```
BAddr.05': u42.7i   ;06
BAddr.05': u10.7i   ;06
BAddr.05': u18.7i   ;06
BAddr.05': u50.7i   ;06
BAddr.05': u82.7i   ;06
BAddr.05': v14.7i   ;06
BAddr.05': v46.7i   ;06
BAddr.05': v54.7i   ;06
BAddr.05': v22.7i   ;06
BAddr.05': u90.7i   ;06
BAddr.05': u58.7i   ;06
BAddr.05': u26.7i   ;06
BAddr.05': #R12.2i  ;17
BAddr.05': #TP014.1i   ;20

BAddr.05z':   v83.14o  ;03
BAddr.05z':   #R12.1o  ;17

BAddr.06': u02.5i   ;06
BAddr.06': u34.5i   ;06
BAddr.06': u66.5i   ;06
BAddr.06': u98.5i   ;06
BAddr.06': v30.5i   ;06
BAddr.06': v62.5i   ;06
BAddr.06': v70.5i   ;06
BAddr.06': v38.5i   ;06
BAddr.06': v06.5i   ;06
BAddr.06': u74.5i   ;06
BAddr.06': u42.5i   ;06
BAddr.06': u10.5i   ;06
BAddr.06': u18.5i   ;06
BAddr.06': u50.5i   ;06
BAddr.06': u82.5i   ;06
BAddr.06': v14.5i   ;06
BAddr.06': v46.5i   ;06
BAddr.06': v54.5i   ;06
BAddr.06': v22.5i   ;06
BAddr.06': u90.5i   ;06
BAddr.06': u58.5i   ;06
BAddr.06': u26.5i   ;06
BAddr.06': #R16.2i  ;17
BAddr.06': #TP010.1i   ;20

BAddr.06z':   v83.18o  ;03
BAddr.06z':   #R16.1o  ;17

Bank0': E12, v90.13i   ;16
Bank0': w00.12o  ;18

Bank0:  w01.1i, w02.1i, w02.19i ;16
Bank0:  w01.19i, v92.19i, v90.12o
Bank0:  v92.1i

Bank1': E37, v99.15i   ;02

Bank2': E137, v99.1i   ;02

bRAS:   v90.2o, v81.9i, v81.5i  ;02
bRAS:   v81.12i, v81.2i

CAddr.00': u03.13i  ;07
CAddr.00': u35.13i  ;07
CAddr.00': u67.13i  ;07
CAddr.00': u99.13i  ;07
CAddr.00': v31.13i  ;07
CAddr.00': v63.13i  ;07
CAddr.00': v71.13i  ;07
CAddr.00': v39.13i  ;07
CAddr.00': v07.13i  ;07
CAddr.00': u75.13i  ;07
CAddr.00': u43.13i  ;07
CAddr.00': u11.13i  ;07
CAddr.00': u19.13i  ;07
CAddr.00': u51.13i  ;07
CAddr.00': u83.13i  ;07
CAddr.00': v15.13i  ;07
CAddr.00': v47.13i  ;07
CAddr.00': v23.13i  ;07
CAddr.00': u91.13i  ;07
CAddr.00': u59.13i  ;07
CAddr.00': u27.13i  ;07
CAddr.00': v55.13i  ;07
CAddr.00': #R27.2i  ;17
CAddr.00': #TP029.1i   ;20

CAddr.00z':   v79.12o  ;03
CAddr.00z':   #R27.1o  ;17

CAddr.01': u03.10i  ;07
CAddr.01': u35.10i  ;07
CAddr.01': u67.10i  ;07
CAddr.01': u99.10i  ;07
CAddr.01': v31.10i  ;07
CAddr.01': v63.10i  ;07
CAddr.01': v71.10i  ;07
CAddr.01': v39.10i  ;07
CAddr.01': v07.10i  ;07
CAddr.01': u75.10i  ;07
CAddr.01': u43.10i  ;07
CAddr.01': u11.10i  ;07
CAddr.01': u19.10i  ;07
CAddr.01': u51.10i  ;07
CAddr.01': u83.10i  ;07
CAddr.01': v15.10i  ;07
CAddr.01': v47.10i  ;07
CAddr.01': v23.10i  ;07
CAddr.01': u91.10i  ;07
CAddr.01': u59.10i  ;07
CAddr.01': u27.10i  ;07
CAddr.01': v55.10i  ;07
CAddr.01': #R21.2i  ;17
CAddr.01': #TP019.1i   ;20

CAddr.01z':   v84.14o  ;03
CAddr.01z':   #R21.1o  ;17

CAddr.02': u03.11i  ;07
CAddr.02': u35.11i  ;07
```

```
CAddr.02': u67.11i  ;07
CAddr.02': u99.11i  ;07
CAddr.02': v31.11i  ;07
CAddr.02': v63.11i  ;07
CAddr.02': v71.11i  ;07
CAddr.02': v39.11i  ;07
CAddr.02': v07.11i  ;07
CAddr.02': u75.11i  ;07
CAddr.02': u43.11i  ;07
CAddr.02': u11.11i  ;07
CAddr.02': u19.11i  ;07
CAddr.02': u51.11i  ;07
CAddr.02': u83.11i  ;07
CAddr.02': v15.11i  ;07
CAddr.02': v47.11i  ;07
CAddr.02': v23.11i  ;07
CAddr.02': u91.11i  ;07
CAddr.02': u59.11i  ;07
CAddr.02': u27.11i  ;07
CAddr.02': v55.11i  ;07
CAddr.02': #R23.2i  ;17
CAddr.02': #TP017.1i   ;20

CAddr.02z':   v84.16o  ;03
CAddr.02z':   #R23.1o  ;17

CAddr.03': u03.12i  ;07
CAddr.03': u35.12i  ;07
CAddr.03': u67.12i  ;07
CAddr.03': u99.12i  ;07
CAddr.03': v31.12i  ;07
CAddr.03': v63.12i  ;07
CAddr.03': v71.12i  ;07
CAddr.03': v39.12i  ;07
CAddr.03': v07.12i  ;07
CAddr.03': u75.12i  ;07
CAddr.03': u43.12i  ;07
CAddr.03': u11.12i  ;07
CAddr.03': u19.12i  ;07
CAddr.03': u51.12i  ;07
CAddr.03': u83.12i  ;07
CAddr.03': v15.12i  ;07
CAddr.03': v47.12i  ;07
CAddr.03': v23.12i  ;07
CAddr.03': u91.12i  ;07
CAddr.03': u59.12i  ;07
CAddr.03': u27.12i  ;07
CAddr.03': v55.12i  ;07
CAddr.03': #R25.2i  ;17
CAddr.03': #TP031.1i   ;20

CAddr.03z':   v84.18o  ;03
CAddr.03z':   #R25.1o  ;17

CAddr.04': u03.6i   ;07
CAddr.04': u35.6i   ;07
CAddr.04': u67.6i   ;07
CAddr.04': u99.6i   ;07
CAddr.04': v31.6i   ;07
CAddr.04': v63.6i   ;07
CAddr.04': v71.6i   ;07
CAddr.04': v39.6i   ;07
CAddr.04': v07.6i   ;07
CAddr.04': u75.6i   ;07
CAddr.04': u43.6i   ;07
CAddr.04': u11.6i   ;07
CAddr.04': u19.6i   ;07
CAddr.04': u51.6i   ;07
CAddr.04': u83.6i   ;07
CAddr.04': v15.6i   ;07
CAddr.04': v47.6i   ;07
CAddr.04': v23.6i   ;07
CAddr.04': u91.6i   ;07
CAddr.04': u59.6i   ;07
CAddr.04': u27.6i   ;07
CAddr.04': v55.6i   ;07
CAddr.04': #R24.2i  ;17
CAddr.04': #TP018.1i   ;20

CAddr.04z':   v84.5o   ;03
CAddr.04z':   #R24.1o  ;17

CAddr.05': u03.7i   ;07
CAddr.05': u35.7i   ;07
CAddr.05': u67.7i   ;07
CAddr.05': u99.7i   ;07
CAddr.05': v31.7i   ;07
CAddr.05': v63.7i   ;07
CAddr.05': v71.7i   ;07
CAddr.05': v39.7i   ;07
CAddr.05': v07.7i   ;07
CAddr.05': u75.7i   ;07
CAddr.05': u43.7i   ;07
CAddr.05': u11.7i   ;07
CAddr.05': u19.7i   ;07
CAddr.05': u51.7i   ;07
CAddr.05': u83.7i   ;07
CAddr.05': v15.7i   ;07
CAddr.05': v47.7i   ;07
CAddr.05': v23.7i   ;07
CAddr.05': u91.7i   ;07
CAddr.05': u59.7i   ;07
CAddr.05': u27.7i   ;07
CAddr.05': v55.7i   ;07
CAddr.05': #R22.2i  ;17
CAddr.05': #TP020.1i   ;20

CAddr.05z':   v84.7o   ;03
CAddr.05z':   #R22.1o  ;17

CAddr.06': u03.5i   ;07
CAddr.06': u35.5i   ;07
CAddr.06': u67.5i   ;07
CAddr.06': u99.5i   ;07
CAddr.06': v31.5i   ;07
CAddr.06': v63.5i   ;07
CAddr.06': v71.5i   ;07
CAddr.06': v39.5i   ;07
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```
CAddr.06': v07.5i   ;07
CAddr.06': u75.5i   ;07
CAddr.06': u43.5i   ;07
CAddr.06': u11.5i   ;07
CAddr.06': u19.5i   ;07
CAddr.06': u51.5i   ;07
CAddr.06': u83.5i   ;07
CAddr.06': v15.5i   ;07
CAddr.06': v47.5i   ;07
CAddr.06': v23.5i   ;07
CAddr.06': u91.5i   ;07
CAddr.06': u59.5i   ;07
CAddr.06': u27.5i   ;07
CAddr.06': v55.5i   ;07
CAddr.06': #R26.2i  ;17
CAddr.06': #TP032.1i   ;20

CAddr.06z':   v84.3o   ;03
CAddr.06z':   #R26.1o  ;17

CAS:    E6, v89.12i ;02
CAS:    w00.9o   ;18
CAS:    #R106.1i, #R105.2i   ;18

CASA':  u01.15i  ;05
CASA':  u09.15i  ;05
CASA':  u17.15i  ;05
CASA':  u25.15i  ;05
CASA':  u33.15i  ;05
CASA':  u41.15i  ;05
CASA':  u49.15i  ;05
CASA':  u57.15i  ;05
CASA':  u65.15i  ;05
CASA':  u73.15i  ;05
CASA':  u81.15i  ;05
CASA':  u89.15i  ;05
CASA':  u97.15i  ;05
CASA':  v05.15i  ;05
CASA':  v13.15i  ;05
CASA':  v21.15i  ;05
CASA':  v29.15i  ;05
CASA':  v37.15i  ;05
CASA':  v45.15i  ;05
CASA':  v53.15i  ;05
CASA':  v61.15i  ;05
CASA':  v69.15i  ;05
CASA':  #R10.2i  ;17
CASA':  #TP015.1i   ;20

CASAz': v83.12o  ;02
CASAz': #R10.1o  ;17

CASB':  u02.15i  ;06
CASB':  u10.15i  ;06
CASB':  u18.15i  ;06
CASB':  u26.15i  ;06
CASB':  u34.15i  ;06
CASB':  u42.15i  ;06
CASB':  u50.15i  ;06
CASB':  u58.15i  ;06
CASB':  u66.15i  ;06
CASB':  u74.15i  ;06
CASB':  u82.15i  ;06
CASB':  u90.15i  ;06
CASB':  u98.15i  ;06
CASB':  v06.15i  ;06
CASB':  v14.15i  ;06
CASB':  v22.15i  ;06
CASB':  v30.15i  ;06
CASB':  v38.15i  ;06
CASB':  v46.15i  ;06
CASB':  v54.15i  ;06
CASB':  v62.15i  ;06
CASB':  v70.15i  ;06
CASB':  #R20.2i  ;17
CASB':  #TP021.1i   ;20

CASBz': v84.9o   ;02
CASBz': #R20.1o  ;17

CASC':  u03.15i  ;07
CASC':  u11.15i  ;07
CASC':  u19.15i  ;07
CASC':  u27.15i  ;07
CASC':  u35.15i  ;07
CASC':  u43.15i  ;07
CASC':  u51.15i  ;07
CASC':  u59.15i  ;07
CASC':  u67.15i  ;07
CASC':  u75.15i  ;07
CASC':  u83.15i  ;07
CASC':  u91.15i  ;07
CASC':  u99.15i  ;07
CASC':  v07.15i  ;07
CASC':  v15.15i  ;07
CASC':  v23.15i  ;07
CASC':  v31.15i  ;07
CASC':  v39.15i  ;07
CASC':  v47.15i  ;07
CASC':  v55.15i  ;07
CASC':  v63.15i  ;07
CASC':  v71.15i  ;07
CASC':  #R30.2i  ;17
CASC':  #TP027.1i   ;20

CASCz': v79.14o  ;02
CASCz': #R30.1o  ;17

CASD':  u04.15i  ;08
CASD':  u12.15i  ;08
CASD':  u20.15i  ;08
CASD':  u28.15i  ;08
CASD':  u36.15i  ;08
CASD':  u44.15i  ;08
CASD':  u52.15i  ;08
CASD':  u60.15i  ;08
CASD':  u68.15i  ;08
CASD':  u76.15i  ;08
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```
CASD':  u84.15i  ;08
CASD':  u92.15i  ;08
CASD':  v00.15i  ;08
CASD':  v08.15i  ;08
CASD':  v16.15i  ;08
CASD':  v24.15i  ;08
CASD':  v32.15i  ;08
CASD':  v40.15i  ;08
CASD':  v48.15i  ;08
CASD':  v56.15i  ;08
CASD':  v64.15i  ;08
CASD':  v72.15i  ;08
CASD':  #R40.2i  ;17
CASD':  #TP033.1i   ;20

CASDz': v85.7o   ;02
CASDz': #R40.1o  ;17

CASE':  u05.15i  ;09
CASE':  u13.15i  ;09
CASE':  u21.15i  ;09
CASE':  u29.15i  ;09
CASE':  u37.15i  ;09
CASE':  u69.15i  ;09
CASE':  v01.15i  ;09
CASE':  v33.15i  ;09
CASE':  v65.15i  ;09
CASE':  v73.15i  ;09
CASE':  v41.15i  ;09
CASE':  v09.15i  ;09
CASE':  u77.15i  ;09
CASE':  u45.15i  ;09
CASE':  u53.15i  ;09
CASE':  u85.15i  ;09
CASE':  v17.15i  ;09
CASE':  v49.15i  ;09
CASE':  v57.15i  ;09
CASE':  v25.15i  ;09
CASE':  u93.15i  ;09
CASE':  u61.15i  ;09
CASE':  #R50.2i  ;17
CASE':  #TP055.1i   ;20

CASEz': v80.16o  ;02
CASEz': #R50.1o  ;17

CASF':  u06.15i  ;10
CASF':  u38.15i  ;10
CASF':  u70.15i  ;10
CASF':  v02.15i  ;10
CASF':  v34.15i  ;10
CASF':  v66.15i  ;10
CASF':  v74.15i  ;10
CASF':  v42.15i  ;10
CASF':  v10.15i  ;10
CASF':  u78.15i  ;10
CASF':  u46.15i  ;10
CASF':  u14.15i  ;10
CASF':  u22.15i  ;10

CASF':  u54.15i  ;10
CASF':  u86.15i  ;10
CASF':  v18.15i  ;10
CASF':  v50.15i  ;10
CASF':  v58.15i  ;10
CASF':  v26.15i  ;10
CASF':  u94.15i  ;10
CASF':  u62.15i  ;10
CASF':  u30.15i  ;10
CASF':  #R60.2i  ;17
CASF':  #TP061.1i   ;20

CASFz': v86.5o   ;02
CASFz': #R60.1o  ;17

CASG':  v59.15i  ;11
CASG':  v27.15i  ;11
CASG':  u95.15i  ;11
CASG':  u63.15i  ;11
CASG':  u31.15i  ;11
CASG':  u23.15i  ;11
CASG':  u15.15i  ;11
CASG':  u07.15i  ;11
CASG':  u39.15i  ;11
CASG':  u71.15i  ;11
CASG':  v03.15i  ;11
CASG':  v35.15i  ;11
CASG':  v67.15i  ;11
CASG':  v75.15i  ;11
CASG':  v43.15i  ;11
CASG':  v11.15i  ;11
CASG':  u79.15i  ;11
CASG':  u47.15i  ;11
CASG':  u55.15i  ;11
CASG':  u87.15i  ;11
CASG':  v19.15i  ;11
CASG':  v51.15i  ;11
CASG':  #R70.2i  ;17
CASG':  #TP067.1i   ;20

CASGz': v87.18o  ;02
CASGz': #R70.1o  ;17

CASH':  u08.15i  ;12
CASH':  u40.15i  ;12
CASH':  u72.15i  ;12
CASH':  v04.15i  ;12
CASH':  v36.15i  ;12
CASH':  v68.15i  ;12
CASH':  v76.15i  ;12
CASH':  v44.15i  ;12
CASH':  v12.15i  ;12
CASH':  u80.15i  ;12
CASH':  u48.15i  ;12
CASH':  u16.15i  ;12
CASH':  u24.15i  ;12
CASH':  u56.15i  ;12
CASH':  u88.15i  ;12
CASH':  v20.15i  ;12
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CASH':  v52.15i  ;12
CASH':  v60.15i  ;12
CASH':  v28.15i  ;12
CASH':  u96.15i  ;12
CASH':  u64.15i  ;12
CASH':  u32.15i  ;12
CASH':  #R80.2i  ;17
CASH':  #TP073.1i   ;20

CASHz': v82.3o   ;02
CASHz': #R80.1o  ;17

CASRef':   v89.11o, v89.2i, v89.1i ;02

CASRef: v89.3o, v85.13i, v79.6i ;02
CASRef: v84.11i, v83.8i, v80.4i
CASRef: v86.15i, v87.2i, v82.17i

CRefresh': E116, v90.9i   ;02
CRefresh': w00.10o  ;18

CRefresh:  v90.8o, v90.11i   ;02

CRefresha':   v89.13i, v90.10o  ;02
CRefresha':   v91.2i, v91.13i
CRefresha':   v91.5i, v91.10i
CRefresha':   v89.5i, v89.10i
CRefresha':   v88.5i, v88.11i

DAddr.00': u04.13i  ;08
DAddr.00': u36.13i  ;08
DAddr.00': u68.13i  ;08
DAddr.00': v00.13i  ;08
DAddr.00': v32.13i  ;08
DAddr.00': v64.13i  ;08
DAddr.00': v72.13i  ;08
DAddr.00': v40.13i  ;08
DAddr.00': v08.13i  ;08
DAddr.00': u76.13i  ;08
DAddr.00': u44.13i  ;08
DAddr.00': u12.13i  ;08
DAddr.00': u20.13i  ;08
DAddr.00': u52.13i  ;08
DAddr.00': u84.13i  ;08
DAddr.00': v16.13i  ;08
DAddr.00': v48.13i  ;08
DAddr.00': v56.13i  ;08
DAddr.00': v24.13i  ;08
DAddr.00': u92.13i  ;08
DAddr.00': u60.13i  ;08
DAddr.00': u28.13i  ;08
DAddr.00': #R37.2i  ;17
DAddr.00': #TP035.1i   ;20

DAddr.00z':   v85.9o   ;03
DAddr.00z':   #R37.1o  ;17

DAddr.01': u04.10i  ;08
DAddr.01': u36.10i  ;08
DAddr.01': u68.10i  ;08
DAddr.01': v00.10i  ;08
DAddr.01': v32.10i  ;08
DAddr.01': v64.10i  ;08
DAddr.01': v72.10i  ;08
DAddr.01': v40.10i  ;08
DAddr.01': v08.10i  ;08
DAddr.01': u76.10i  ;08
DAddr.01': u44.10i  ;08
DAddr.01': u12.10i  ;08
DAddr.01': u20.10i  ;08
DAddr.01': u52.10i  ;08
DAddr.01': u84.10i  ;08
DAddr.01': v16.10i  ;08
DAddr.01': v48.10i  ;08
DAddr.01': v56.10i  ;08
DAddr.01': v24.10i  ;08
DAddr.01': u92.10i  ;08
DAddr.01': u60.10i  ;08
DAddr.01': u28.10i  ;08
DAddr.01': #R31.2i  ;17
DAddr.01': #TP025.1i   ;20

DAddr.01z':   v79.7o   ;03
DAddr.01z':   #R31.1o  ;17

DAddr.02': u04.11i  ;08
DAddr.02': u36.11i  ;08
DAddr.02': u68.11i  ;08
DAddr.02': v00.11i  ;08
DAddr.02': v32.11i  ;08
DAddr.02': v64.11i  ;08
DAddr.02': v72.11i  ;08
DAddr.02': v40.11i  ;08
DAddr.02': v08.11i  ;08
DAddr.02': u76.11i  ;08
DAddr.02': u44.11i  ;08
DAddr.02': u12.11i  ;08
DAddr.02': u20.11i  ;08
DAddr.02': u52.11i  ;08
DAddr.02': u84.11i  ;08
DAddr.02': v16.11i  ;08
DAddr.02': v48.11i  ;08
DAddr.02': v56.11i  ;08
DAddr.02': v24.11i  ;08
DAddr.02': u92.11i  ;08
DAddr.02': u60.11i  ;08
DAddr.02': u28.11i  ;08
DAddr.02': #R33.2i  ;17
DAddr.02': #TP039.1i   ;20

DAddr.02z':   v79.5o   ;03
DAddr.02z':   #R33.1o  ;17

DAddr.03': u04.12i  ;08
DAddr.03': u36.12i  ;08
DAddr.03': u68.12i  ;08
DAddr.03': v00.12i  ;08
DAddr.03': v32.12i  ;08
```

```
DAddr.03': v64.12i  ;08
DAddr.03': v72.12i  ;08
DAddr.03': v40.12i  ;08
DAddr.03': v08.12i  ;08
DAddr.03': u76.12i  ;08
DAddr.03': u44.12i  ;08
DAddr.03': u12.12i  ;08
DAddr.03': u20.12i  ;08
DAddr.03': u52.12i  ;08
DAddr.03': u84.12i  ;08
DAddr.03': v16.12i  ;08
DAddr.03': v48.12i  ;08
DAddr.03': v56.12i  ;08
DAddr.03': v24.12i  ;08
DAddr.03': u92.12i  ;08
DAddr.03': u60.12i  ;08
DAddr.03': u28.12i  ;08
DAddr.03': #R35.2i  ;17
DAddr.03': #TP037.1i   ;20

DAddr.03z':   v79.3o   ;03
DAddr.03z':   #R35.1o  ;17

DAddr.04': u04.6i   ;08
DAddr.04': u36.6i   ;08
DAddr.04': u68.6i   ;08
DAddr.04': v00.6i   ;08
DAddr.04': v32.6i   ;08
DAddr.04': v64.6i   ;08
DAddr.04': v72.6i   ;08
DAddr.04': v40.6i   ;08
DAddr.04': v08.6i   ;08
DAddr.04': u76.6i   ;08
DAddr.04': u44.6i   ;08
DAddr.04': u12.6i   ;08
DAddr.04': u20.6i   ;08
DAddr.04': u52.6i   ;08
DAddr.04': u84.6i   ;08
DAddr.04': v16.6i   ;08
DAddr.04': v48.6i   ;08
DAddr.04': v56.6i   ;08
DAddr.04': v24.6i   ;08
DAddr.04': u92.6i   ;08
DAddr.04': u60.6i   ;08
DAddr.04': u28.6i   ;08
DAddr.04': #R34.2i  ;17
DAddr.04': #TP040.1i   ;20

DAddr.04z':   v79.18o  ;03
DAddr.04z':   #R34.1o  ;17

DAddr.05': u04.7i   ;08
DAddr.05': u36.7i   ;08
DAddr.05': u68.7i   ;08
DAddr.05': v00.7i   ;08
DAddr.05': v32.7i   ;08
DAddr.05': v64.7i   ;08
DAddr.05': v72.7i   ;08
DAddr.05': v40.7i   ;08
DAddr.05': v08.7i   ;08
DAddr.05': u76.7i   ;08
DAddr.05': u44.7i   ;08
DAddr.05': u12.7i   ;08
DAddr.05': u20.7i   ;08
DAddr.05': u52.7i   ;08
DAddr.05': u84.7i   ;08
DAddr.05': v16.7i   ;08
DAddr.05': v48.7i   ;08
DAddr.05': v56.7i   ;08
DAddr.05': v24.7i   ;08
DAddr.05': u92.7i   ;08
DAddr.05': u60.7i   ;08
DAddr.05': u28.7i   ;08
DAddr.05': #R32.2i  ;17
DAddr.05': #TP026.1i   ;20

DAddr.05z':   v79.16o  ;03
DAddr.05z':   #R32.1o  ;17

DAddr.06': u04.5i   ;08
DAddr.06': u36.5i   ;08
DAddr.06': u68.5i   ;08
DAddr.06': v00.5i   ;08
DAddr.06': v32.5i   ;08
DAddr.06': v64.5i   ;08
DAddr.06': v72.5i   ;08
DAddr.06': v40.5i   ;08
DAddr.06': v08.5i   ;08
DAddr.06': u76.5i   ;08
DAddr.06': u44.5i   ;08
DAddr.06': u12.5i   ;08
DAddr.06': u20.5i   ;08
DAddr.06': u52.5i   ;08
DAddr.06': u84.5i   ;08
DAddr.06': v16.5i   ;08
DAddr.06': v48.5i   ;08
DAddr.06': v56.5i   ;08
DAddr.06': v24.5i   ;08
DAddr.06': u92.5i   ;08
DAddr.06': u60.5i   ;08
DAddr.06': u28.5i   ;08
DAddr.06': #R36.2i  ;17
DAddr.06': #TP038.1i   ;20

DAddr.06z':   v85.12o  ;03
DAddr.06z':   #R36.1o  ;17

EAddr.00': u05.13i  ;09
EAddr.00': u37.13i  ;09
EAddr.00': u69.13i  ;09
EAddr.00': v01.13i  ;09
EAddr.00': v33.13i  ;09
EAddr.00': v65.13i  ;09
EAddr.00': v73.13i  ;09
EAddr.00': v41.13i  ;09
EAddr.00': v09.13i  ;09
EAddr.00': u77.13i  ;09
EAddr.00': u45.13i  ;09
```

```
EAddr.00': u13.13i  ;09
EAddr.00': u21.13i  ;09
EAddr.00': u53.13i  ;09
EAddr.00': u85.13i  ;09
EAddr.00': v17.13i  ;09
EAddr.00': v49.13i  ;09
EAddr.00': v25.13i  ;09
EAddr.00': u93.13i  ;09
EAddr.00': u61.13i  ;09
EAddr.00': u29.13i  ;09
EAddr.00': v57.13i  ;09
EAddr.00': #R47.2i  ;17
EAddr.00': #TP041.1i   ;20

EAddr.00z':   v80.14o  ;04
EAddr.00z':   #R47.1o  ;17

EAddr.01': u05.10i  ;09
EAddr.01': u37.10i  ;09
EAddr.01': u69.10i  ;09
EAddr.01': v01.10i  ;09
EAddr.01': v33.10i  ;09
EAddr.01': v65.10i  ;09
EAddr.01': v73.10i  ;09
EAddr.01': v41.10i  ;09
EAddr.01': v09.10i  ;09
EAddr.01': u77.10i  ;09
EAddr.01': u45.10i  ;09
EAddr.01': u13.10i  ;09
EAddr.01': u21.10i  ;09
EAddr.01': u53.10i  ;09
EAddr.01': u85.10i  ;09
EAddr.01': v17.10i  ;09
EAddr.01': v49.10i  ;09
EAddr.01': v25.10i  ;09
EAddr.01': u93.10i  ;09
EAddr.01': u61.10i  ;09
EAddr.01': u29.10i  ;09
EAddr.01': v57.10i  ;09
EAddr.01': #R41.2i  ;17
EAddr.01': #TP047.1i   ;20

EAddr.01z':   v85.16o  ;04
EAddr.01z':   #R41.1o  ;17

EAddr.02': u05.11i  ;09
EAddr.02': u37.11i  ;09
EAddr.02': u69.11i  ;09
EAddr.02': v01.11i  ;09
EAddr.02': v33.11i  ;09
EAddr.02': v65.11i  ;09
EAddr.02': v73.11i  ;09
EAddr.02': v41.11i  ;09
EAddr.02': v09.11i  ;09
EAddr.02': u77.11i  ;09
EAddr.02': u45.11i  ;09
EAddr.02': u13.11i  ;09
EAddr.02': u21.11i  ;09
EAddr.02': u53.11i  ;09
EAddr.02': u85.11i  ;09
EAddr.02': v17.11i  ;09
EAddr.02': v49.11i  ;09
EAddr.02': v25.11i  ;09
EAddr.02': u93.11i  ;09
EAddr.02': u61.11i  ;09
EAddr.02': u29.11i  ;09
EAddr.02': v57.11i  ;09
EAddr.02': #R43.2i  ;17
EAddr.02': #TP045.1i   ;20

EAddr.02z':   v85.18o  ;04
EAddr.02z':   #R43.1o  ;17

EAddr.03': u05.12i  ;09
EAddr.03': u37.12i  ;09
EAddr.03': u69.12i  ;09
EAddr.03': v01.12i  ;09
EAddr.03': v33.12i  ;09
EAddr.03': v65.12i  ;09
EAddr.03': v73.12i  ;09
EAddr.03': v41.12i  ;09
EAddr.03': v09.12i  ;09
EAddr.03': u77.12i  ;09
EAddr.03': u45.12i  ;09
EAddr.03': u13.12i  ;09
EAddr.03': u21.12i  ;09
EAddr.03': u53.12i  ;09
EAddr.03': u85.12i  ;09
EAddr.03': v17.12i  ;09
EAddr.03': v49.12i  ;09
EAddr.03': v25.12i  ;09
EAddr.03': u93.12i  ;09
EAddr.03': u61.12i  ;09
EAddr.03': u29.12i  ;09
EAddr.03': v57.12i  ;09
EAddr.03': #R45.2i  ;17
EAddr.03': #TP043.1i   ;20

EAddr.03z':   v80.12o  ;04
EAddr.03z':   #R45.1o  ;17

EAddr.04': u05.6i   ;09
EAddr.04': u37.6i   ;09
EAddr.04': u69.6i   ;09
EAddr.04': v01.6i   ;09
EAddr.04': v33.6i   ;09
EAddr.04': v65.6i   ;09
EAddr.04': v73.6i   ;09
EAddr.04': v41.6i   ;09
EAddr.04': v09.6i   ;09
EAddr.04': u77.6i   ;09
EAddr.04': u45.6i   ;09
EAddr.04': u13.6i   ;09
EAddr.04': u21.6i   ;09
EAddr.04': u53.6i   ;09
EAddr.04': u85.6i   ;09
EAddr.04': v17.6i   ;09
EAddr.04': v49.6i   ;09
```

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 34 OF	B

```
EAddr.04': v25.6i   ;09
EAddr.04': u93.6i   ;09
EAddr.04': u61.6i   ;09
EAddr.04': u29.6i   ;09
EAddr.04': v57.6i   ;09
EAddr.04': #R44.2i  ;17
EAddr.04': #TP046.1i   ;20

EAddr.04z':   v85.3o   ;04
EAddr.04z':   #R44.1o  ;17

EAddr.05': u05.7i   ;09
EAddr.05': u37.7i   ;09
EAddr.05': u69.7i   ;09
EAddr.05': v01.7i   ;09
EAddr.05': v33.7i   ;09
EAddr.05': v65.7i   ;09
EAddr.05': v73.7i   ;09
EAddr.05': v41.7i   ;09
EAddr.05': v09.7i   ;09
EAddr.05': u77.7i   ;09
EAddr.05': u45.7i   ;09
EAddr.05': u13.7i   ;09
EAddr.05': u21.7i   ;09
EAddr.05': u53.7i   ;09
EAddr.05': u85.7i   ;09
EAddr.05': v17.7i   ;09
EAddr.05': v49.7i   ;09
EAddr.05': v25.7i   ;09
EAddr.05': u93.7i   ;09
EAddr.05': u61.7i   ;09
EAddr.05': u29.7i   ;09
EAddr.05': v57.7i   ;09
EAddr.05': #R42.2i  ;17
EAddr.05': #TP048.1i   ;20

EAddr.05z':   v85.5o   ;04
EAddr.05z':   #R42.1o  ;17

EAddr.06': u05.5i   ;09
EAddr.06': u37.5i   ;09
EAddr.06': u69.5i   ;09
EAddr.06': v01.5i   ;09
EAddr.06': v33.5i   ;09
EAddr.06': v65.5i   ;09
EAddr.06': v73.5i   ;09
EAddr.06': v41.5i   ;09
EAddr.06': v09.5i   ;09
EAddr.06': u77.5i   ;09
EAddr.06': u45.5i   ;09
EAddr.06': u13.5i   ;09
EAddr.06': u21.5i   ;09
EAddr.06': u53.5i   ;09
EAddr.06': u85.5i   ;09
EAddr.06': v17.5i   ;09
EAddr.06': v49.5i   ;09
EAddr.06': v25.5i   ;09
EAddr.06': u93.5i   ;09
EAddr.06': u61.5i   ;09

EAddr.06': u29.5i   ;09
EAddr.06': v57.5i   ;09
EAddr.06': #R46.2i  ;17
EAddr.06': #TP044.1i   ;20

EAddr.06z':   v80.9o   ;04
EAddr.06z':   #R46.1o  ;17

FAddr.00': u06.13i  ;10
FAddr.00': u38.13i  ;10
FAddr.00': u70.13i  ;10
FAddr.00': v02.13i  ;10
FAddr.00': v34.13i  ;10
FAddr.00': v66.13i  ;10
FAddr.00': v74.13i  ;10
FAddr.00': v42.13i  ;10
FAddr.00': v10.13i  ;10
FAddr.00': u78.13i  ;10
FAddr.00': u46.13i  ;10
FAddr.00': u14.13i  ;10
FAddr.00': u22.13i  ;10
FAddr.00': u54.13i  ;10
FAddr.00': u86.13i  ;10
FAddr.00': v18.13i  ;10
FAddr.00': v50.13i  ;10
FAddr.00': v58.13i  ;10
FAddr.00': v26.13i  ;10
FAddr.00': u94.13i  ;10
FAddr.00': u62.13i  ;10
FAddr.00': u30.13i  ;10
FAddr.00': #R57.2i  ;17
FAddr.00': #TP063.1i   ;20

FAddr.00z':   v86.7o   ;04
FAddr.00z':   #R57.1o  ;17

FAddr.01': u06.10i  ;10
FAddr.01': u38.10i  ;10
FAddr.01': u70.10i  ;10
FAddr.01': v02.10i  ;10
FAddr.01': v34.10i  ;10
FAddr.01': v66.10i  ;10
FAddr.01': v74.10i  ;10
FAddr.01': v42.10i  ;10
FAddr.01': v10.10i  ;10
FAddr.01': u78.10i  ;10
FAddr.01': u46.10i  ;10
FAddr.01': u14.10i  ;10
FAddr.01': u22.10i  ;10
FAddr.01': u54.10i  ;10
FAddr.01': u86.10i  ;10
FAddr.01': v18.10i  ;10
FAddr.01': v50.10i  ;10
FAddr.01': v58.10i  ;10
FAddr.01': v26.10i  ;10
FAddr.01': u94.10i  ;10
FAddr.01': u62.10i  ;10
FAddr.01': u30.10i  ;10
FAddr.01': #R51.2i  ;17
```

```
FAddr.01': #TP053.1i   ;20

FAddr.01z':   v80.5o   ;04
FAddr.01z':   #R51.1o  ;17

FAddr.02': u06.11i  ;10
FAddr.02': u38.11i  ;10
FAddr.02': u70.11i  ;10
FAddr.02': v02.11i  ;10
FAddr.02': v34.11i  ;10
FAddr.02': v66.11i  ;10
FAddr.02': v74.11i  ;10
FAddr.02': v42.11i  ;10
FAddr.02': v10.11i  ;10
FAddr.02': u78.11i  ;10
FAddr.02': u46.11i  ;10
FAddr.02': u14.11i  ;10
FAddr.02': u22.11i  ;10
FAddr.02': u54.11i  ;10
FAddr.02': u86.11i  ;10
FAddr.02': v18.11i  ;10
FAddr.02': v50.11i  ;10
FAddr.02': v58.11i  ;10
FAddr.02': v26.11i  ;10
FAddr.02': u94.11i  ;10
FAddr.02': u62.11i  ;10
FAddr.02': u30.11i  ;10
FAddr.02': #R53.2i  ;17
FAddr.02': #TP051.1i   ;20

FAddr.02z':   v80.3o   ;04
FAddr.02z':   #R53.1o  ;17

FAddr.03': u06.12i  ;10
FAddr.03': u38.12i  ;10
FAddr.03': u70.12i  ;10
FAddr.03': v02.12i  ;10
FAddr.03': v34.12i  ;10
FAddr.03': v66.12i  ;10
FAddr.03': v74.12i  ;10
FAddr.03': v42.12i  ;10
FAddr.03': v10.12i  ;10
FAddr.03': u78.12i  ;10
FAddr.03': u46.12i  ;10
FAddr.03': u14.12i  ;10
FAddr.03': u22.12i  ;10
FAddr.03': u54.12i  ;10
FAddr.03': u86.12i  ;10
FAddr.03': v18.12i  ;10
FAddr.03': v50.12i  ;10
FAddr.03': v58.12i  ;10
FAddr.03': v26.12i  ;10
FAddr.03': u94.12i  ;10
FAddr.03': u62.12i  ;10
FAddr.03': u30.12i  ;10
FAddr.03': #R55.2i  ;17
FAddr.03': #TP049.1i   ;20

FAddr.03z':   v86.9o   ;04

FAddr.03z':   #R55.1o  ;17

FAddr.04': u06.6i   ;10
FAddr.04': u38.6i   ;10
FAddr.04': u70.6i   ;10
FAddr.04': v02.6i   ;10
FAddr.04': v34.6i   ;10
FAddr.04': v66.6i   ;10
FAddr.04': v74.6i   ;10
FAddr.04': v42.6i   ;10
FAddr.04': v10.6i   ;10
FAddr.04': u78.6i   ;10
FAddr.04': u46.6i   ;10
FAddr.04': u14.6i   ;10
FAddr.04': u22.6i   ;10
FAddr.04': u54.6i   ;10
FAddr.04': u86.6i   ;10
FAddr.04': v18.6i   ;10
FAddr.04': v50.6i   ;10
FAddr.04': v58.6i   ;10
FAddr.04': v26.6i   ;10
FAddr.04': u94.6i   ;10
FAddr.04': u62.6i   ;10
FAddr.04': u30.6i   ;10
FAddr.04': #R54.2i  ;17
FAddr.04': #TP052.1i   ;20

FAddr.04z':   v86.12o  ;04
FAddr.04z':   #R54.1o  ;17

FAddr.05': u06.7i   ;10
FAddr.05': u38.7i   ;10
FAddr.05': u70.7i   ;10
FAddr.05': v02.7i   ;10
FAddr.05': v34.7i   ;10
FAddr.05': v66.7i   ;10
FAddr.05': v74.7i   ;10
FAddr.05': v42.7i   ;10
FAddr.05': v10.7i   ;10
FAddr.05': u78.7i   ;10
FAddr.05': u46.7i   ;10
FAddr.05': u14.7i   ;10
FAddr.05': u22.7i   ;10
FAddr.05': u54.7i   ;10
FAddr.05': u86.7i   ;10
FAddr.05': v18.7i   ;10
FAddr.05': v50.7i   ;10
FAddr.05': v58.7i   ;10
FAddr.05': v26.7i   ;10
FAddr.05': u94.7i   ;10
FAddr.05': u62.7i   ;10
FAddr.05': u30.7i   ;10
FAddr.05': #R52.2i  ;17
FAddr.05': #TP054.1i   ;20

FAddr.05z':   v80.18o  ;04
FAddr.05z':   #R52.1o  ;17

FAddr.06': u06.5i   ;10
```

```
FAddr.06': u38.5i   ;10
FAddr.06': u70.5i   ;10
FAddr.06': v02.5i   ;10
FAddr.06': v34.5i   ;10
FAddr.06': v66.5i   ;10
FAddr.06': v74.5i   ;10
FAddr.06': v42.5i   ;10
FAddr.06': v10.5i   ;10
FAddr.06': u78.5i   ;10
FAddr.06': u46.5i   ;10
FAddr.06': u14.5i   ;10
FAddr.06': u22.5i   ;10
FAddr.06': u54.5i   ;10
FAddr.06': u86.5i   ;10
FAddr.06': v18.5i   ;10
FAddr.06': v50.5i   ;10
FAddr.06': v58.5i   ;10
FAddr.06': v26.5i   ;10
FAddr.06': u94.5i   ;10
FAddr.06': u62.5i   ;10
FAddr.06': u30.5i   ;10
FAddr.06': #R56.2i  ;17
FAddr.06': #TP050.1i   ;20

FAddr.06z':   v86.14o  ;04
FAddr.06z':   #R56.1o  ;17

GAddr.00': u07.13i  ;11
GAddr.00': u39.13i  ;11
GAddr.00': u71.13i  ;11
GAddr.00': v03.13i  ;11
GAddr.00': v35.13i  ;11
GAddr.00': v67.13i  ;11
GAddr.00': v75.13i  ;11
GAddr.00': v43.13i  ;11
GAddr.00': v11.13i  ;11
GAddr.00': u79.13i  ;11
GAddr.00': u47.13i  ;11
GAddr.00': u15.13i  ;11
GAddr.00': u23.13i  ;11
GAddr.00': u55.13i  ;11
GAddr.00': u87.13i  ;11
GAddr.00': v19.13i  ;11
GAddr.00': v51.13i  ;11
GAddr.00': v59.13i  ;11
GAddr.00': v27.13i  ;11
GAddr.00': u95.13i  ;11
GAddr.00': u63.13i  ;11
GAddr.00': u31.13i  ;11
GAddr.00': #R67.2i  ;17
GAddr.00': #TP069.1i   ;20

GAddr.00z':   v87.16o  ;04
GAddr.00z':   #R67.1o  ;17

GAddr.01': u07.10i  ;11
GAddr.01': u39.10i  ;11
GAddr.01': u71.10i  ;11
GAddr.01': v03.10i  ;11
GAddr.01': v35.10i  ;11
GAddr.01': v67.10i  ;11
GAddr.01': v75.10i  ;11
GAddr.01': v43.10i  ;11
GAddr.01': v11.10i  ;11
GAddr.01': u79.10i  ;11
GAddr.01': u47.10i  ;11
GAddr.01': u15.10i  ;11
GAddr.01': u23.10i  ;11
GAddr.01': u55.10i  ;11
GAddr.01': u87.10i  ;11
GAddr.01': v19.10i  ;11
GAddr.01': v51.10i  ;11
GAddr.01': v59.10i  ;11
GAddr.01': v27.10i  ;11
GAddr.01': u95.10i  ;11
GAddr.01': u63.10i  ;11
GAddr.01': u31.10i  ;11
GAddr.01': #R61.2i  ;17
GAddr.01': #TP059.1i   ;20

GAddr.01z':   v86.18o  ;04
GAddr.01z':   #R61.1o  ;17

GAddr.02': u07.11i  ;11
GAddr.02': u39.11i  ;11
GAddr.02': u71.11i  ;11
GAddr.02': v03.11i  ;11
GAddr.02': v35.11i  ;11
GAddr.02': v67.11i  ;11
GAddr.02': v75.11i  ;11
GAddr.02': v43.11i  ;11
GAddr.02': v11.11i  ;11
GAddr.02': u79.11i  ;11
GAddr.02': u47.11i  ;11
GAddr.02': u15.11i  ;11
GAddr.02': u23.11i  ;11
GAddr.02': u55.11i  ;11
GAddr.02': u87.11i  ;11
GAddr.02': v19.11i  ;11
GAddr.02': v51.11i  ;11
GAddr.02': v59.11i  ;11
GAddr.02': v27.11i  ;11
GAddr.02': u95.11i  ;11
GAddr.02': u63.11i  ;11
GAddr.02': u31.11i  ;11
GAddr.02': #R63.2i  ;17
GAddr.02': #TP057.1i   ;20

GAddr.02z':   v87.12o  ;04
GAddr.02z':   #R63.1o  ;17

GAddr.03': u07.12i  ;11
GAddr.03': u39.12i  ;11
GAddr.03': u71.12i  ;11
GAddr.03': v03.12i  ;11
GAddr.03': v35.12i  ;11
GAddr.03': v67.12i  ;11
GAddr.03': v75.12i  ;11
```

```
GAddr.03': v43.12i  ;11
GAddr.03': v11.12i  ;11
GAddr.03': u79.12i  ;11
GAddr.03': u47.12i  ;11
GAddr.03': u15.12i  ;11
GAddr.03': u23.12i  ;11
GAddr.03': u55.12i  ;11
GAddr.03': u87.12i  ;11
GAddr.03': v19.12i  ;11
GAddr.03': v51.12i  ;11
GAddr.03': v59.12i  ;11
GAddr.03': v27.12i  ;11
GAddr.03': u95.12i  ;11
GAddr.03': u63.12i  ;11
GAddr.03': u31.12i  ;11
GAddr.03': #R65.2i  ;17
GAddr.03': #TP071.1i   ;20

GAddr.03z':   v87.14o  ;04
GAddr.03z':   #R65.1o  ;17

GAddr.04': u07.6i   ;11
GAddr.04': u39.6i   ;11
GAddr.04': u71.6i   ;11
GAddr.04': v03.6i   ;11
GAddr.04': v35.6i   ;11
GAddr.04': v67.6i   ;11
GAddr.04': v75.6i   ;11
GAddr.04': v43.6i   ;11
GAddr.04': v11.6i   ;11
GAddr.04': u79.6i   ;11
GAddr.04': u47.6i   ;11
GAddr.04': u15.6i   ;11
GAddr.04': u23.6i   ;11
GAddr.04': u55.6i   ;11
GAddr.04': u87.6i   ;11
GAddr.04': v19.6i   ;11
GAddr.04': v51.6i   ;11
GAddr.04': v59.6i   ;11
GAddr.04': v27.6i   ;11
GAddr.04': u95.6i   ;11
GAddr.04': u63.6i   ;11
GAddr.04': u31.6i   ;11
GAddr.04': #R64.2i  ;17
GAddr.04': #TP058.1i   ;20

GAddr.04z':   v87.9o   ;04
GAddr.04z':   #R64.1o  ;17

GAddr.05': u07.7i   ;11
GAddr.05': u39.7i   ;11
GAddr.05': u71.7i   ;11
GAddr.05': v03.7i   ;11
GAddr.05': v35.7i   ;11
GAddr.05': v67.7i   ;11
GAddr.05': v75.7i   ;11
GAddr.05': v43.7i   ;11
GAddr.05': v11.7i   ;11
GAddr.05': u79.7i   ;11
GAddr.05': u47.7i   ;11
GAddr.05': u15.7i   ;11
GAddr.05': u23.7i   ;11
GAddr.05': u55.7i   ;11
GAddr.05': u87.7i   ;11
GAddr.05': v19.7i   ;11
GAddr.05': v51.7i   ;11
GAddr.05': v59.7i   ;11
GAddr.05': v27.7i   ;11
GAddr.05': u95.7i   ;11
GAddr.05': u63.7i   ;11
GAddr.05': u31.7i   ;11
GAddr.05': #R62.2i  ;17
GAddr.05': #TP060.1i   ;20

GAddr.05z':   v86.3o   ;04
GAddr.05z':   #R62.1o  ;17

GAddr.06': u07.5i   ;11
GAddr.06': u39.5i   ;11
GAddr.06': u71.5i   ;11
GAddr.06': v03.5i   ;11
GAddr.06': v35.5i   ;11
GAddr.06': v67.5i   ;11
GAddr.06': v75.5i   ;11
GAddr.06': v43.5i   ;11
GAddr.06': v11.5i   ;11
GAddr.06': u79.5i   ;11
GAddr.06': u47.5i   ;11
GAddr.06': u15.5i   ;11
GAddr.06': u23.5i   ;11
GAddr.06': u55.5i   ;11
GAddr.06': u87.5i   ;11
GAddr.06': v19.5i   ;11
GAddr.06': v51.5i   ;11
GAddr.06': v59.5i   ;11
GAddr.06': v27.5i   ;11
GAddr.06': u95.5i   ;11
GAddr.06': u63.5i   ;11
GAddr.06': u31.5i   ;11
GAddr.06': #R66.2i  ;17
GAddr.06': #TP072.1i   ;20

GAddr.06z':   v87.7o   ;04
GAddr.06z':   #R66.1o  ;17

GND:    v77.1i   ;02
GND:    v77.19i  ;02
GND:    v84.1i   ;03
GND:    v83.1i   ;03
GND:    v79.1i   ;03
GND:    v85.1i   ;03
GND:    v83.19i  ;03
GND:    v84.19i  ;03
GND:    v85.19i  ;03
GND:    v79.19i  ;03
GND:    v87.1i   ;04
GND:    v82.1i   ;04
GND:    v86.1i   ;04
```

```
                                    13i   ;15
                                    8i    ;16

                                    10.2i, #R108.2i  ;18
                                    04.2i
                                    23.2o, #C121.2o  ;21
                                    17.2o, #C114.2o
                                    10.2o, #C108.2o
                                    04.2o, #C102.2o
                                    .2o, #C95.2o
                                    .2o, #C90.2o
                                    .2o, #C84.2o
                                    .2o, #C75.2o
                                    .2o, #C70.2o
                                    .2o, #C63.2o
                                    .2o, #C58.2o
                                    .2o, #C52.2o
                                    .2o, #C45.2o
                                    .2o, #C38.2o
                                    .2o, #C31.2o
                                    .2o, #C25.2o
                                    .2o, #C20.2o
                                    .2o, #C13.2o
                                    .2o, #C8.2o
                                    .2o, #C2.2o
                                    2.2o, #C160.2o
                                    .2o, #C155.2o
                                    .2o, #C149.2o
                                    .2o, #C142.2o
                                    .2o, #C137.2o
                                    .2o, #C130.2o
                                    .2o
                                    4.2o, #C132.2o  ;22
                                    2.2o, #C120.2o
                                    6.2o, #C115.2o
                                    3.2o, #C109.2o
                                    5.2o, #C101.2o
GND:    #C99.2o, #C96.2o, #C94.2o
GND:    #C92.2o, #C89.2o, #C87.2o
GND:    #C85.2o, #C83.2o, #C82.2o
GND:    #C80.2o, #C78.2o, #C76.2o
GND:    #C73.2o, #C69.2o, #C66.2o
GND:    #C64.2o, #C62.2o, #C60.2o
GND:    #C57.2o, #C55.2o, #C53.2o
GND:    #C51.2o, #C50.2o, #C48.2o
GND:    #C46.2o, #C44.2o, #C37.2o
GND:    #C33.2o, #C32.2o, #C30.2o
GND:    #C28.2o, #C26.2o, #C23.2o
GND:    #C21.2o, #C19.2o, #C17.2o
GND:    #C16.2o, #C14.2o, #C12.2o
GND:    #C10.2o, #C180.2o, #C7.2o
GND:    #C5.2o, #C3.2o, #C1.2o
GND:    #C178.2o, #C176.2o, #C174.2o
GND:    #C171.2o, #C169.2o, #C167.2o
GND:    #C165.2o, #C163.2o, #C161.2o
GND:    #C159.2o, #C157.2o, #C154.2o
GND:    #C152.2o, #C150.2o, #C148.2o
GND:    #C147.2o, #C145.2o, #C143.2o
GND:    #C141.2o, #C138.2o
GND:    #C179.2o, #C177.2o, #C175.2o  ;23
GND:    #C173.2o, #C172.2o, #C170.2o
GND:    #C168.2o, #C81.2o
GND:    #C186.2o, #C185.2o, #C184.2o  ;23
GND:    #C183.2o, #C182.2o, #C181.2o
GND:    #C129.2o, #C127.2o, #C125.2o
GND:    #C98.2o, #C71.2o, #C67.2o
GND:    #C39.2o, #C35.2o
GND:    #C201.2o, #C200.2o, #C199.2o  ;23
GND:    #C194.2o, #C198.2o, #C197.2o
GND:    #C196.2o, #C195.2o, #C192.2o
GND:    #C191.2o, #C190.2o, #C189.2o
GND:    #C188.2o

HAddr.00': u08.13i  ;12
HAddr.00': u40.13i  ;12
HAddr.00': u72.13i  ;12
HAddr.00': v04.13i  ;12
HAddr.00': v36.13i  ;12
HAddr.00': v68.13i  ;12
HAddr.00': v76.13i  ;12
HAddr.00': v44.13i  ;12
HAddr.00': v12.13i  ;12
HAddr.00': u80.13i  ;12
HAddr.00': u48.13i  ;12
HAddr.00': u16.13i  ;12
HAddr.00': u24.13i  ;12
HAddr.00': u56.13i  ;12
HAddr.00': u88.13i  ;12
HAddr.00': v20.13i  ;12
HAddr.00': v52.13i  ;12
HAddr.00': v60.13i  ;12
HAddr.00': v28.13i  ;12
HAddr.00': u96.13i  ;12
HAddr.00': u64.13i  ;12
HAddr.00': u32.13i  ;12
HAddr.00': #R77.2i  ;17
HAddr.00': #TP075.1i   ;20

HAddr.00z':   v82.5o   ;04
HAddr.00z':   #R77.1o  ;17

HAddr.01': u08.10i  ;12
HAddr.01': u40.10i  ;12
HAddr.01': u72.10i  ;12
HAddr.01': v04.10i  ;12
HAddr.01': v36.10i  ;12
HAddr.01': v68.10i  ;12
HAddr.01': v76.10i  ;12
HAddr.01': v44.10i  ;12
HAddr.01': v12.10i  ;12
HAddr.01': u80.10i  ;12
HAddr.01': u48.10i  ;12
```

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HAddr.01': u16[illegible].10i  ;12
HAddr.01': u24[illegible].10i  ;12
HAddr.01': u56[illegible].10i  ;12
HAddr.01': u88[illegible].10i  ;12
HAddr.01': v20[illegible].10i  ;12
HAddr.01': v52[illegible].10i  ;12
HAddr.01': v60[illegible].10i  ;12
HAddr.01': v28[illegible].10i  ;12
HAddr.01': u96[illegible].10i  ;12
HAddr.01': u64[illegible].10i  ;12
HAddr.01': u32[illegible].10i  ;12
HAddr.01': #R7[illegible].2i   ;17
HAddr.01': #TP[illegible]5.1i    ;20

HAddr.01z':    v[illegible]7.3o    ;04
HAddr.01z':    #R71.1o   ;17

HAddr.02': u08.11i  ;12
HAddr.02': u40.11i  ;12
HAddr.02': u72.11i  ;12
HAddr.02': v04.11i  ;12
HAddr.02': v36.11i  ;12
HAddr.02': v68.11i  ;12
HAddr.02': v76.11i  ;12
HAddr.02': v44.11i  ;12
HAddr.02': v12.11i  ;12
HAddr.02': u80.11i  ;12
HAddr.02': u48.11i  ;12
HAddr.02': u16.11i  ;12
HAddr.02': u24.11i  ;12
HAddr.02': u56.11i  ;12
HAddr.02': u88.11i  ;12
HAddr.02': v20.11i  ;12
HAddr.02': v52.11i  ;12
HAddr.02': v60.11i  ;12
HAddr.02': v28.11i  ;12
HAddr.02': u96.11i  ;12
HAddr.02': u64.11i  ;12
HAddr.02': u32.11i  ;12
HAddr.02': #R73.2i  ;17
HAddr.02': #TP079.1i    ;20

HAddr.02z':    v82.9o    ;04
HAddr.02z':    #R73.1o   ;17

HAddr.03': u08.12i  ;12
HAddr.03': u40.12i  ;12
HAddr.03': u72.12i  ;12
HAddr.03': v04.12i  ;12
HAddr.03': v36.12i  ;12
HAddr.03': v68.12i  ;12
HAddr.03': v76.12i  ;12
HAddr.03': v44.12i  ;12
HAddr.03': v12.12i  ;12
HAddr.03': u80.12i  ;12
HAddr.03': u48.12i  ;12
HAddr.03': u16.12i  ;12
HAddr.03': u24.12i  ;12
HAddr.03': u56.12i  ;12
HAddr.03': u88.12i  ;12
HAddr.03': v20.12i  ;12
HAddr.03': v52.12i  ;12
HAddr.03': v60.12i  ;12
HAddr.03': v28.12i  ;12
HAddr.03': u96.12i  ;12
HAddr.03': u64.12i  ;12
HAddr.03': u32.12i  ;12
HAddr.03': #R75.2i  ;17
HAddr.03': #TP077.1i    ;20

HAddr.03z':    v82.7o    ;04
HAddr.03z':    #R75.1o   ;17

HAddr.04': u08.6i   ;12
HAddr.04': u40.6i   ;12
HAddr.04': u72.6i   ;12
HAddr.04': v04.6i   ;12
HAddr.04': v36.6i   ;12
HAddr.04': v68.6i   ;12
HAddr.04': v76.6i   ;12
HAddr.04': v44.6i   ;12
HAddr.04': v12.6i   ;12
HAddr.04': u80.6i   ;12
HAddr.04': u48.6i   ;12
HAddr.04': u16.6i   ;12
HAddr.04': u24.6i   ;12
HAddr.04': u56.6i   ;12
HAddr.04': u88.6i   ;12
HAddr.04': v20.6i   ;12
HAddr.04': v52.6i   ;12
HAddr.04': v60.6i   ;12
HAddr.04': v28.6i   ;12
HAddr.04': u96.6i   ;12
HAddr.04': u64.6i   ;12
HAddr.04': u32.6i   ;12
HAddr.04': #R74.2i  ;17
HAddr.04': #TP080.1i    ;20

HAddr.04z':    v82.14o   ;04
HAddr.04z':    #R74.1o   ;17

HAddr.05': u08.7i   ;12
HAddr.05': u40.7i   ;12
HAddr.05': u72.7i   ;12
HAddr.05': v04.7i   ;12
HAddr.05': v36.7i   ;12
HAddr.05': v68.7i   ;12
HAddr.05': v76.7i   ;12
HAddr.05': v44.7i   ;12
HAddr.05': v12.7i   ;12
HAddr.05': u80.7i   ;12
HAddr.05': u48.7i   ;12
HAddr.05': u16.7i   ;12
HAddr.05': u24.7i   ;12
HAddr.05': u56.7i   ;12
HAddr.05': u88.7i   ;12
HAddr.05': v20.7i   ;12
HAddr.05': v52.7i   ;12
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HAddr.05': v60.7i   ;12
HAddr.05': v28.7i   ;12
HAddr.05': u96.7i   ;12
HAddr.05': u64.7i   ;12
HAddr.05': u32.7i   ;12
HAddr.05': #R72.2i  ;17
HAddr.05': #TP066.1i   ;20

HAddr.05z':   v82.12o  ;04
HAddr.05z':   #R72.1o  ;17

HAddr.06': u08.5i   ;12
HAddr.06': u40.5i   ;12
HAddr.06': u72.5i   ;12
HAddr.06': v04.5i   ;12
HAddr.06': v36.5i   ;12
HAddr.06': v68.5i   ;12
HAddr.06': v76.5i   ;12
HAddr.06': v44.5i   ;12
HAddr.06': v12.5i   ;12
HAddr.06': u80.5i   ;12
HAddr.06': u48.5i   ;12
HAddr.06': u16.5i   ;12
HAddr.06': u24.5i   ;12
HAddr.06': u56.5i   ;12
HAddr.06': u88.5i   ;12
HAddr.06': v20.5i   ;12
HAddr.06': v52.5i   ;12
HAddr.06': v60.5i   ;12
HAddr.06': v28.5i   ;12
HAddr.06': u96.5i   ;12
HAddr.06': u64.5i   ;12
HAddr.06': u32.5i   ;12
HAddr.06': #R76.2i  ;17
HAddr.06': #TP078.1i   ;20

HAddr.06z':   v82.16o  ;04
HAddr.06z':   #R76.1o  ;17

LatA':  v99.12o, v88.10i  ;02

LatB':  v99.11o, v88.4i, v88.3i ;02

LatC':  v99.10o, v89.9i   ;02

LatchY.00: v99.3i, E136, v99.13i   ;02

LatchY.01: v99.2i, E36, v99.14i ;02

LatD':  v99.9o, v89.4i ;02

LatE':  v99.4o, v91.9i ;02

LatF':  v99.5o, v91.4i ;02

LatG':  v99.6o, v91.12i   ;02

LatH':  v99.7o, v91.1i ;02

LCAS:   E106, #R110.1i, #R109.2i   ;18

LRAS':  E105, #R108.1i, #R107.2i   ;18

M5V:    E100, E200, #F1.1i   ;19

MemData.00':  u01.14o  ;13
MemData.00':  u02.14o  ;13
MemData.00':  u03.14o  ;13
MemData.00':  u04.14o  ;13
MemData.00':  u05.14o  ;14
MemData.00':  u06.14o  ;14
MemData.00':  u07.14o  ;14
MemData.00':  u08.14o  ;14
MemData.00':  w02.2i   ;16
MemData.00':  v94.1i   ;18
MemData.00':  #TP103.1i   ;20

MemData.01':  u09.14o  ;13
MemData.01':  u10.14o  ;13
MemData.01':  u11.14o  ;13
MemData.01':  u12.14o  ;13
MemData.01':  u13.14o  ;14
MemData.01':  u14.14o  ;14
MemData.01':  u15.14o  ;14
MemData.01':  u16.14o  ;14
MemData.01':  w02.17i  ;16
MemData.01':  v94.15o  ;18
MemData.01':  #TP104.1i   ;20

MemData.02':  u17.14o  ;13
MemData.02':  u18.14o  ;13
MemData.02':  u19.14o  ;13
MemData.02':  u20.14o  ;13
MemData.02':  u21.14o  ;14
MemData.02':  u22.14o  ;14
MemData.02':  u23.14o  ;14
MemData.02':  u24.14o  ;14
MemData.02':  w02.4i   ;16
MemData.02':  v94.2i   ;18
MemData.02':  #TP105.1i   ;20

MemData.03':  u25.14o  ;13
MemData.03':  u26.14o  ;13
MemData.03':  u27.14o  ;13
MemData.03':  u28.14o  ;13
MemData.03':  u29.14o  ;14
MemData.03':  u30.14o  ;14
MemData.03':  u31.14o  ;14
MemData.03':  u32.14o  ;14
MemData.03':  w02.15i  ;16
MemData.03':  v94.14o  ;18
MemData.03':  #TP106.1i   ;20

MemData.04':  u33.14o  ;13
MemData.04':  u34.14o  ;13
MemData.04':  u35.14o  ;13
MemData.04':  u36.14o  ;13
MemData.04':  u37.14o  ;14
```

```
MemData.04'   [illegible].14o  ;14
MemData.04'   [illegible].14o  ;14
MemData.04'   [illegible].14o  ;14
MemData.04'   [illegible]5i   ;16
MemData.04'   [illegible]3i   ;18
MemData.04'   [illegible]07.1i   ;20

MemData.05'   [illegible]14o  ;13
MemData.05'   [illegible]14o  ;13
MemData.05'   [illegible]14o  ;13
MemData.05'   [illegible]14o  ;13
MemData.05'   [illegible]14o  ;14
MemData.05'   [illegible]14o  ;14
MemData.05'   [illegible]14o  ;14
MemData.05'   [illegible]14o  ;14
MemData.05'   [illegible]13i  ;16
MemData.05'   [illegible]13o  ;18
MemData.05'   [illegible]03.1i   ;20

MemData.06'   [illegible].14o  ;13
MemData.06'   [illegible].14o  ;13
MemData.06'   [illegible].14o  ;13
MemData.06'   [illegible].14o  ;13
MemData.06'   [illegible].14o  ;14
MemData.06'   [illegible].14o  ;14
MemData.06'   [illegible].14o  ;14
MemData.06'   [illegible].14o  ;14
MemData.06'   [illegible]3i   ;16
MemData.06'   [illegible]4i   ;18
MemData.06'   [illegible]09.1i   ;20

MemData.07'   [illegible].14o  ;13
MemData.07'   [illegible].14o  ;13
MemData.07'   [illegible].14o  ;13
MemData.07'   [illegible].14o  ;13
MemData.07'   u61.14o  ;14
MemData.07'   u62.14o  ;14
MemData.07'   u63.14o  ;14
MemData.07'   u64.14o  ;14
MemData.07'   w02.11i  ;16
MemData.07'   v94.12o  ;18
MemData.07'   #TP110.1i   ;20

MemData.08'   u65.14o  ;13
MemData.08'   u66.14o  ;13
MemData.08'   u67.14o  ;13
MemData.08'   u68.14o  ;13
MemData.08'   u69.14o  ;14
MemData.08'   u70.14o  ;14
MemData.08'   u71.14o  ;14
MemData.08'   u72.14o  ;14
MemData.08'   w01.2i   ;16
MemData.08'   v94.5i   ;18
MemData.08'   #TP111.1i   ;20

MemData.09'   u73.14o  ;13
MemData.09'   u74.14o  ;13
MemData.09'   u75.14o  ;13
MemData.09'   u76.14o  ;13
MemData.09'   u77.14o  ;14
MemData.09'   u78.14o  ;14
MemData.09'   u79.14o  ;14
MemData.09'   u80.14o  ;14
MemData.09'   w01.17i  ;16
MemData.09'   v94.11o  ;18
MemData.09'   #TP112.1i   ;20

MemData.10'   u81.14o  ;13
MemData.10'   u82.14o  ;13
MemData.10'   u83.14o  ;13
MemData.10'   u84.14o  ;13
MemData.10'   u85.14o  ;14
MemData.10'   u86.14o  ;14
MemData.10'   u87.14o  ;14
MemData.10'   u88.14o  ;14
MemData.10'   w01.4i   ;16
MemData.10'   v94.6i   ;18
MemData.10'   #TP113.1i   ;20

MemData.11'   u89.14o  ;13
MemData.11'   u90.14o  ;13
MemData.11'   u91.14o  ;13
MemData.11'   u92.14o  ;13
MemData.11'   u93.14o  ;14
MemData.11'   u94.14o  ;14
MemData.11'   u95.14o  ;14
MemData.11'   u96.14o  ;14
MemData.11'   w01.15i  ;16
MemData.11'   v94.10o  ;18
MemData.11'   #TP114.1i   ;20

MemData.12'   u97.14o  ;13
MemData.12'   u98.14o  ;13
MemData.12'   u99.14o  ;13
MemData.12'   v00.14o  ;13
MemData.12'   v01.14o  ;14
MemData.12'   v02.14o  ;14
MemData.12'   v03.14o  ;14
MemData.12'   v04.14o  ;14
MemData.12'   w01.6i   ;16
MemData.12'   v94.7i   ;18
MemData.12'   #TP115.1i   ;20

MemData.13'   v05.14o  ;13
MemData.13'   v06.14o  ;13
MemData.13'   v07.14o  ;13
MemData.13'   v08.14o  ;13
MemData.13'   v09.14o  ;14
MemData.13'   v10.14o  ;14
MemData.13'   v11.14o  ;14
MemData.13'   v12.14o  ;14
MemData.13'   w01.13i  ;16
MemData.13'   v94.9o   ;18
MemData.13'   #TP116.1i   ;20

MemData.14'   v13.14o  ;13
MemData.14'   v14.14o  ;13
MemData.14'   v15.14o  ;13
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MemData.14':  v16.14o  ;13
MemData.14':  v17.14o  ;14
MemData.14':  v18.14o  ;14
MemData.14':  v19.14o  ;14
MemData.14':  v20.14o  ;14
MemData.14':  w01.8i   ;16
MemData.14':  v94.8i   ;18
MemData.14':  #TP117.1i   ;20

MemData.15':  v21.14o  ;13
MemData.15':  v22.14o  ;13
MemData.15':  v23.14o  ;13
MemData.15':  v24.14o  ;13
MemData.15':  v25.14o  ;14
MemData.15':  v26.14o  ;14
MemData.15':  v27.14o  ;14
MemData.15':  v28.14o  ;14
MemData.15':  w01.11i  ;16
MemData.15':  v93.15o  ;18
MemData.15':  #TP118.1i   ;20

MemData.16':  v29.14o  ;13
MemData.16':  v30.14o  ;13
MemData.16':  v31.14o  ;13
MemData.16':  v32.14o  ;13
MemData.16':  v33.14o  ;14
MemData.16':  v34.14o  ;14
MemData.16':  v35.14o  ;14
MemData.16':  v36.14o  ;14
MemData.16':  v92.2i   ;16
MemData.16':  v93.1i   ;18
MemData.16':  #TP119.1i   ;20

MemData.17':  v37.14o  ;13
MemData.17':  v38.14o  ;13
MemData.17':  v39.14o  ;13
MemData.17':  v40.14o  ;13
MemData.17':  v41.14o  ;14
MemData.17':  v42.14o  ;14
MemData.17':  v43.14o  ;14
MemData.17':  v44.14o  ;14
MemData.17':  v92.17i  ;16
MemData.17':  v93.14o  ;18
MemData.17':  #TP120.1i   ;20

MemData.18':  v45.14o  ;13
MemData.18':  v46.14o  ;13
MemData.18':  v47.14o  ;13
MemData.18':  v48.14o  ;13
MemData.18':  v49.14o  ;14
MemData.18':  v50.14o  ;14
MemData.18':  v51.14o  ;14
MemData.18':  v52.14o  ;14
MemData.18':  v92.4i   ;16
MemData.18':  v93.2i   ;18
MemData.18':  #TP121.1i   ;20

MemData.19':  v53.14o  ;13
MemData.19':  v54.14o  ;13
MemData.19':  v55.14o  ;13
MemData.19':  v56.14o  ;13
MemData.19':  v57.14o  ;14
MemData.19':  v58.14o  ;14
MemData.19':  v59.14o  ;14
MemData.19':  v60.14o  ;14
MemData.19':  v92.15i  ;16
MemData.19':  v93.13o  ;18
MemData.19':  #TP122.1i   ;20

MemData.20':  v61.14o  ;13
MemData.20':  v62.14o  ;13
MemData.20':  v63.14o  ;13
MemData.20':  v64.14o  ;13
MemData.20':  v65.14o  ;14
MemData.20':  v66.14o  ;14
MemData.20':  v67.14o  ;14
MemData.20':  v68.14o  ;14
MemData.20':  v92.6i   ;16
MemData.20':  v93.3i   ;18
MemData.20':  #TP123.1i   ;20

MemData.21':  v69.14o  ;13
MemData.21':  v70.14o  ;13
MemData.21':  v71.14o  ;13
MemData.21':  v72.14o  ;13
MemData.21':  v73.14o  ;14
MemData.21':  v74.14o  ;14
MemData.21':  v75.14o  ;14
MemData.21':  v76.14o  ;14
MemData.21':  v92.13i  ;16
MemData.21':  v93.12o  ;18
MemData.21':  #TP124.1i   ;20

MRef':  E38, v88.9i ;02

P12V:   E1, E101, #F3.1i  ;19

P5V:    E50, E51, E150, E151, #F2.1i  ;19

ppClk:  E9, #R112.1i, #R111.2i  ;18

RAS':   E5, v90.1i, v90.3i   ;02
RAS':   #R104.1i, #R103.2i   ;18

RASA':  u01.4i   ;05
RASA':  u09.4i   ;05
RASA':  u17.4i   ;05
RASA':  u25.4i   ;05
RASA':  u33.4i   ;05
RASA':  u41.4i   ;05
RASA':  u49.4i   ;05
RASA':  u57.4i   ;05
RASA':  u65.4i   ;05
RASA':  u73.4i   ;05
RASA':  u81.4i   ;05
RASA':  u89.4i   ;05
RASA':  u97.4i   ;05
RASA':  v05.4i   ;05
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RASA':  v13.4i   ;05
RASA':  v21.4i   ;05
RASA':  v29.4i   ;05
RASA':  v37.4i   ;05
RASA':  v45.4i   ;05
RASA':  v53.4i   ;05
RASA':  v61.4i   ;05
RASA':  v69.4i   ;05
RASA':  #R8.2i   ;17
RASA':  #TP002.1i   ;20

RASAz': v78.8o   ;02
RASAz': #R8.1o   ;17

RASB':  u02.4i   ;06
RASB':  u10.4i   ;06
RASB':  u18.4i   ;06
RASB':  u26.4i   ;06
RASB':  u34.4i   ;06
RASB':  u42.4i   ;06
RASB':  u50.4i   ;06
RASB':  u58.4i   ;06
RASB':  u66.4i   ;06
RASB':  u74.4i   ;06
RASB':  u82.4i   ;06
RASB':  u90.4i   ;06
RASB':  u98.4i   ;06
RASB':  v06.4i   ;06
RASB':  v14.4i   ;06
RASB':  v22.4i   ;06
RASB':  v30.4i   ;06
RASB':  v38.4i   ;06
RASB':  v46.4i   ;06
RASB':  v54.4i   ;06
RASB':  v62.4i   ;06
RASB':  v70.4i   ;06
RASB':  #R18.2i  ;17
RASB':  #TP024.1i   ;20

RASBz': v78.6o   ;02
RASBz': #R18.1o  ;17

RASC':  u03.4i   ;07
RASC':  u11.4i   ;07
RASC':  u19.4i   ;07
RASC':  u27.4i   ;07
RASC':  u35.4i   ;07
RASC':  u43.4i   ;07
RASC':  u51.4i   ;07
RASC':  u59.4i   ;07
RASC':  u67.4i   ;07
RASC':  u75.4i   ;07
RASC':  u83.4i   ;07
RASC':  u91.4i   ;07
RASC':  u99.4i   ;07
RASC':  v07.4i   ;07
RASC':  v15.4i   ;07
RASC':  v23.4i   ;07
RASC':  v31.4i   ;07
RASC':  v39.4i   ;07
RASC':  v47.4i   ;07
RASC':  v55.4i   ;07
RASC':  v63.4i   ;07
RASC':  v71.4i   ;07
RASC':  #R28.2i  ;17
RASC':  #TP030.1i   ;20

RASCz': v78.11o  ;02
RASCz': #R28.1o  ;17

RASD':  u04.4i   ;08
RASD':  u12.4i   ;08
RASD':  u20.4i   ;08
RASD':  u28.4i   ;08
RASD':  u36.4i   ;08
RASD':  u44.4i   ;08
RASD':  u52.4i   ;08
RASD':  u60.4i   ;08
RASD':  u68.4i   ;08
RASD':  u76.4i   ;08
RASD':  u84.4i   ;08
RASD':  u92.4i   ;08
RASD':  v00.4i   ;08
RASD':  v08.4i   ;08
RASD':  v16.4i   ;08
RASD':  v24.4i   ;08
RASD':  v32.4i   ;08
RASD':  v40.4i   ;08
RASD':  v48.4i   ;08
RASD':  v56.4i   ;08
RASD':  v64.4i   ;08
RASD':  v72.4i   ;08
RASD':  #R38.2i  ;17
RASD':  #TP036.1i   ;20

RASDz': v78.3o   ;02
RASDz': #R38.1o  ;17

RASE':  u05.4i   ;09
RASE':  u13.4i   ;09
RASE':  u21.4i   ;09
RASE':  u29.4i   ;09
RASE':  u37.4i   ;09
RASE':  u69.4i   ;09
RASE':  v01.4i   ;09
RASE':  v33.4i   ;09
RASE':  v65.4i   ;09
RASE':  v73.4i   ;09
RASE':  v41.4i   ;09
RASE':  v09.4i   ;09
RASE':  u77.4i   ;09
RASE':  u45.4i   ;09
RASE':  u53.4i   ;09
RASE':  u85.4i   ;09
RASE':  v17.4i   ;09
RASE':  v49.4i   ;09
RASE':  v57.4i   ;09
RASE':  v25.4i   ;09
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RASE':  u93.4i   ;09
RASE':  u61.4i   ;09
RASE':  #R48.2i  ;17
RASE':  #TP042.1i   ;20

RASEz': v81.8o   ;02
RASEz': #R48.1o  ;17

RASF':  u06.4i   ;10
RASF':  u38.4i   ;10
RASF':  u70.4i   ;10
RASF':  v02.4i   ;10
RASF':  v34.4i   ;10
RASF':  v66.4i   ;10
RASF':  v74.4i   ;10
RASF':  v42.4i   ;10
RASF':  v10.4i   ;10
RASF':  u78.4i   ;10
RASF':  u46.4i   ;10
RASF':  u14.4i   ;10
RASF':  u22.4i   ;10
RASF':  u54.4i   ;10
RASF':  u86.4i   ;10
RASF':  v18.4i   ;10
RASF':  v50.4i   ;10
RASF':  v58.4i   ;10
RASF':  v26.4i   ;10
RASF':  u94.4i   ;10
RASF':  u62.4i   ;10
RASF':  u30.4i   ;10
RASF':  #R58.2i  ;17
RASF':  #TP064.1i   ;20

RASFz': v81.6o   ;02
RASFz': #R58.1o  ;17

RASG':  v59.4i   ;11
RASG':  v27.4i   ;11
RASG':  u95.4i   ;11
RASG':  u63.4i   ;11
RASG':  u31.4i   ;11
RASG':  u23.4i   ;11
RASG':  u15.4i   ;11
RASG':  u07.4i   ;11
RASG':  u39.4i   ;11
RASG':  u71.4i   ;11
RASG':  v03.4i   ;11
RASG':  v35.4i   ;11
RASG':  v67.4i   ;11
RASG':  v75.4i   ;11
RASG':  v43.4i   ;11
RASG':  v11.4i   ;11
RASG':  u79.4i   ;11
RASG':  u47.4i   ;11
RASG':  u55.4i   ;11
RASG':  u87.4i   ;11
RASG':  v19.4i   ;11
RASG':  v51.4i   ;11
RASG':  #R68.2i  ;17

RASG':  #TP070.1i   ;20

RASGz': v81.11o  ;02
RASGz': #R68.1o  ;17

RASH':  u08.4i   ;12
RASH':  u40.4i   ;12
RASH':  u72.4i   ;12
RASH':  v04.4i   ;12
RASH':  v36.4i   ;12
RASH':  v68.4i   ;12
RASH':  v76.4i   ;12
RASH':  v44.4i   ;12
RASH':  v12.4i   ;12
RASH':  u80.4i   ;12
RASH':  u48.4i   ;12
RASH':  u16.4i   ;12
RASH':  u24.4i   ;12
RASH':  u56.4i   ;12
RASH':  u88.4i   ;12
RASH':  v20.4i   ;12
RASH':  v52.4i   ;12
RASH':  v60.4i   ;12
RASH':  v28.4i   ;12
RASH':  u96.4i   ;12
RASH':  u64.4i   ;12
RASH':  u32.4i   ;12
RASH':  #R78.2i  ;17
RASH':  #TP076.1i   ;20

RASHz': v81.3o   ;02
RASHz': #R78.1o  ;17

SAddr.00:  E32, v83.17i, v77.2i ;03
SAddr.00:  v85.11i, v79.8i   ;03
SAddr.00:  v82.15i, v87.4i   ;04
SAddr.00:  v86.13i, v80.6i   ;04
SAddr.00:  w00.2i   ;18

SAddr.01:  E132, v83.11i, v77.8i   ;03
SAddr.01:  v79.13i, v84.6i   ;03
SAddr.01:  v87.17i, v86.2i   ;04
SAddr.01:  v80.15i, v85.4i   ;04
SAddr.01:  w00.4i   ;18

SAddr.02:  E33, v83.13i, v77.6i ;03
SAddr.02:  v79.15i, v84.4i   ;03
SAddr.02:  v82.11i, v87.8i   ;04
SAddr.02:  v80.17i, v85.2i   ;04
SAddr.02:  w00.13o  ;18

SAddr.03:  E133, v83.15i, v77.4i   ;03
SAddr.03:  v79.17i, v84.2i   ;03
SAddr.03:  v82.13i, v87.6i   ;04
SAddr.03:  v86.11i, v80.8i   ;04
SAddr.03:  w00.14o  ;18

SAddr.04:  E34, v83.4i, v77.13i ;03
SAddr.04:  v79.2i, v84.15i   ;03
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XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 45 OF	B

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SAddr.04:  v82.6i, v87.11i   ;04
SAddr.04:  v86.8i, v85.17i   ;04
SAddr.04:  w00.15o  ;18

SAddr.05:  E134, v83.6i, v77.11i   ;03
SAddr.05:  v79.4i, v84.13i   ;03
SAddr.05:  v82.8i, v86.17i   ;04
SAddr.05:  v80.2i, v85.15i   ;04
SAddr.05:  w00.3i   ;18

SAddr.06:  E35, v83.2i, v77.15i ;03
SAddr.06:  v85.8i, v84.17i   ;03
SAddr.06:  v82.4i, v87.13i   ;04
SAddr.06:  v86.6i, v80.11i   ;04
SAddr.06:  w00.1i   ;18

SDI.00':   u02.2i, u03.2i, u04.2i  ;13
SDI.00':   u01.2i
SDI.00':   u06.2i, u07.2i, u08.2i  ;14
SDI.00':   u05.2i
SDI.00':   #R81.2i  ;18
SDI.00':   #TP088.1i   ;20

SDI.00: E96, v95.9i ;15

SDI.00z':  v95.8o   ;15
SDI.00z':  #R81.1o  ;18

SDI.01':   u10.2i, u11.2i, u12.2i  ;13
SDI.01':   u09.2i
SDI.01':   u14.2i, u15.2i, u16.2i  ;14
SDI.01':   u13.2i
SDI.01':   #R82.2i  ;18
SDI.01':   #TP087.1i   ;20

SDI.01: E196, v95.5i   ;15

SDI.01z':  v95.6o   ;15
SDI.01z':  #R82.1o  ;18

SDI.02':   u18.2i, u19.2i, u20.2i  ;13
SDI.02':   u17.2i
SDI.02':   u22.2i, u23.2i, u24.2i  ;14
SDI.02':   u21.2i
SDI.02':   #R83.2i  ;18
SDI.02':   #TP086.1i   ;20

SDI.02: E95, v95.11i   ;15

SDI.02z':  v95.10o  ;15
SDI.02z':  #R83.1o  ;18

SDI.03':   u26.2i, u27.2i, u28.2i  ;13
SDI.03':   u25.2i
SDI.03':   u30.2i, u31.2i, u32.2i  ;14
SDI.03':   u29.2i
SDI.03':   #R84.2i  ;18
SDI.03':   #TP085.1i   ;20

SDI.03: E195, v95.3i   ;15

SDI.03z':  v95.4o   ;15
SDI.03z':  #R84.1o  ;18

SDI.04':   u34.2i, u35.2i, u36.2i  ;13
SDI.04':   u33.2i
SDI.04':   u38.2i, u39.2i, u40.2i  ;14
SDI.04':   u37.2i
SDI.04':   #R85.2i  ;18
SDI.04':   #TP084.1i   ;20

SDI.04: E94, v95.13i   ;15

SDI.04z':  v95.12o  ;15
SDI.04z':  #R85.1o  ;18

SDI.05':   u42.2i, u43.2i, u44.2i  ;13
SDI.05':   u41.2i
SDI.05':   u46.2i, u47.2i, u48.2i  ;14
SDI.05':   u45.2i
SDI.05':   #R86.2i  ;18
SDI.05':   #TP083.1i   ;20

SDI.05: E194, v95.1i   ;15

SDI.05z':  v95.2o   ;15
SDI.05z':  #R86.1o  ;18

SDI.06':   u50.2i, u51.2i, u52.2i  ;13
SDI.06':   u49.2i
SDI.06':   u54.2i, u55.2i, u56.2i  ;14
SDI.06':   u53.2i
SDI.06':   #R87.2i  ;18
SDI.06':   #TP082.1i   ;20

SDI.06: E93, v96.9i ;15

SDI.06z':  v96.8o   ;15
SDI.06z':  #R87.1o  ;18

SDI.07':   u58.2i, u59.2i, u60.2i  ;13
SDI.07':   u57.2i
SDI.07':   u62.2i, u63.2i, u64.2i  ;14
SDI.07':   u61.2i
SDI.07':   #R88.2i  ;18
SDI.07':   #TP081.1i   ;20

SDI.07: E193, v96.5i   ;15

SDI.07z':  v96.6o   ;15
SDI.07z':  #R88.1o  ;18

SDI.08':   u66.2i, u67.2i, u68.2i  ;13
SDI.08':   u65.2i
SDI.08':   u70.2i, u71.2i, u72.2i  ;14
SDI.08':   u69.2i
SDI.08':   #R89.2i  ;18
SDI.08':   #TP096.1i   ;20
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SDI.08: E92, v96.11i   ;15

SDI.08z':  v96.10o  ;15
SDI.08z':  #R89.1o  ;18

SDI.09':   u74.2i, u75.2i, u76.2i  ;13
SDI.09':   u73.2i
SDI.09':   u78.2i, u79.2i, u80.2i  ;14
SDI.09':   u77.2i
SDI.09':   #R90.2i  ;18
SDI.09':   #TP095.1i   ;20

SDI.09: E192, v96.3i   ;15

SDI.09z':  v96.4o   ;15
SDI.09z':  #R90.1o  ;18

SDI.10':   u82.2i, u83.2i, u84.2i  ;13
SDI.10':   u81.2i
SDI.10':   u86.2i, u87.2i, u88.2i  ;14
SDI.10':   u85.2i
SDI.10':   #R91.2i  ;18
SDI.10':   #TP094.1i   ;20

SDI.10: E91, v96.13i   ;15

SDI.10z':  v96.12o  ;15
SDI.10z':  #R91.1o  ;18

SDI.11':   u90.2i, u91.2i, u92.2i  ;13
SDI.11':   u89.2i
SDI.11':   u94.2i, u95.2i, u96.2i  ;14
SDI.11':   u93.2i
SDI.11':   #R92.2i  ;18
SDI.11':   #TP093.1i   ;20

SDI.11: E191, v96.1i   ;15

SDI.11z':  v96.2o   ;15
SDI.11z':  #R92.1o  ;18

SDI.12':   u98.2i, u99.2i, v00.2i  ;13
SDI.12':   u97.2i
SDI.12':   v02.2i, v03.2i, v04.2i  ;14
SDI.12':   v01.2i
SDI.12':   #R93.2i  ;18
SDI.12':   #TP092.1i   ;20

SDI.12: E89, v97.9i ;15

SDI.12z':  v97.8o   ;15
SDI.12z':  #R93.1o  ;18

SDI.13':   v06.2i, v07.2i, v08.2i  ;13
SDI.13':   v05.2i
SDI.13':   v10.2i, v11.2i, v12.2i  ;14
SDI.13':   v09.2i
SDI.13':   #R94.2i  ;18

SDI.13':   #TP091.1i   ;20

SDI.13: E189, v97.5i   ;15

SDI.13z':  v97.6o   ;15
SDI.13z':  #R94.1o  ;18

SDI.14':   v14.2i, v15.2i, v16.2i  ;13
SDI.14':   v13.2i
SDI.14':   v18.2i, v19.2i, v20.2i  ;14
SDI.14':   v17.2i
SDI.14':   #R95.2i  ;18
SDI.14':   #TP090.1i   ;20

SDI.14: E88, v97.11i   ;15

SDI.14z':  v97.10o  ;15
SDI.14z':  #R95.1o  ;18

SDI.15':   v22.2i, v23.2i, v24.2i  ;13
SDI.15':   v21.2i
SDI.15':   v26.2i, v27.2i, v28.2i  ;14
SDI.15':   v25.2i
SDI.15':   #R96.2i  ;18
SDI.15':   #TP089.1i   ;20

SDI.15: E188, v97.3i   ;15

SDI.15z':  v97.4o   ;15
SDI.15z':  #R96.1o  ;18

SDI.16':   v30.2i, v31.2i, v32.2i  ;13
SDI.16':   v29.2i
SDI.16':   v34.2i, v35.2i, v36.2i  ;14
SDI.16':   v33.2i
SDI.16':   #R97.2i  ;18
SDI.16':   #TP102.1i   ;20

SDI.16: E87, v97.13i   ;15

SDI.16z':  v97.12o  ;15
SDI.16z':  #R97.1o  ;18

SDI.17':   v38.2i, v39.2i, v40.2i  ;13
SDI.17':   v37.2i
SDI.17':   v42.2i, v43.2i, v44.2i  ;14
SDI.17':   v41.2i
SDI.17':   #R98.2i  ;18
SDI.17':   #TP101.1i   ;20

SDI.17: E187, v97.1i   ;15

SDI.17z':  v97.2o   ;15
SDI.17z':  #R98.1o  ;18

SDI.18':   v46.2i, v47.2i, v48.2i  ;13
SDI.18':   v45.2i
SDI.18':   v50.2i, v51.2i, v52.2i  ;14
SDI.18':   v49.2i
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SDI.18':   #R99.2i  ;18
SDI.18':   #TP100.1i   ;20

SDI.18: E86, v98.9i ;15

SDI.18z':  v98.8o   ;15
SDI.18z':  #R99.1o  ;18

SDI.19':   v54.2i, v55.2i, v56.2i  ;13
SDI.19':   v53.2i
SDI.19':   v58.2i, v59.2i, v60.2i  ;14
SDI.19':   v57.2i
SDI.19':   #R100.2i ;18
SDI.19':   #TP099.1i   ;20

SDI.19: E186, v98.5i   ;15

SDI.19z':  v98.6o   ;15
SDI.19z':  #R100.1o ;18

SDI.20':   v62.2i, v63.2i, v64.2i  ;13
SDI.20':   v61.2i
SDI.20':   v66.2i, v67.2i, v68.2i  ;14
SDI.20':   v65.2i
SDI.20':   #R101.2i ;18
SDI.20':   #TP098.1i   ;20

SDI.20: E85, v98.11i   ;15

SDI.20z':  v98.10o  ;15
SDI.20z':  #R101.1o ;18

SDI.21':   v70.2i, v71.2i, v72.2i  ;13
SDI.21':   v69.2i
SDI.21':   v74.2i, v75.2i, v76.2i  ;14
SDI.21':   v73.2i
SDI.21':   #R102.2i ;18
SDI.21':   #TP097.1i   ;20

SDI.21: E185, v98.3i   ;15

SDI.21z':  v98.4o   ;15
SDI.21z':  #R102.1o ;18

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SDO.03: w02.5o, E119   ;16

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SDO.08: w01.18o, E23   ;16

SDO.09: w01.3o, E123   ;16

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SDO.12: w01.14o, E25   ;16

SDO.13: w01.7o, E125   ;16

SDO.14: w01.12o, E26   ;16

SDO.15: w01.9o, E126   ;16

SDO.16: v92.18o, E27   ;16

SDO.17: v92.3o, E127   ;16

SDO.18: v92.16o, E28   ;16

SDO.19: v92.5o, E128   ;16

SDO.20: v92.14o, E29   ;16

SDO.21: v92.7o, E129   ;16

SelA:   v88.8o, v78.10i   ;02

SelB:   v88.6o, v78.4i ;02

SelC:   v89.8o, v78.13i   ;02

SelD:   v89.6o, v78.1i ;02

SelE:   v91.8o, v81.10i   ;02

SelF:   v91.6o, v81.4i ;02

SelG:   v91.11o, v81.13i  ;02

SelH:   v91.3o, v81.1i ;02

VCC:    #C35.1i, #C39.1i, #C67.1i  ;23
VCC:    #C71.1i, #C98.1i, #C125.1i
VCC:    #C127.1i, #C129.1i, #C181.1i
VCC:    #C182.1i, #C183.1i, #C184.1i
VCC:    #C185.1i, #C186.1i, #C188.1i
VCC:    #C189.1i, #C190.1i, #C191.1i
VCC:    #C192.1i, #C195.1i, #C196.1i
VCC:    #C197.1i, #C198.1i, #C194.1i
VCC:    #C199.1i, #C200.1i, #C201.1i

Write': E138, v90.5i   ;03
Write': w00.6i   ;18

WriteA':   u01.3i   ;05
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WriteA':   u09.3i   ;05
WriteA':   u17.3i   ;05
WriteA':   u25.3i   ;05
WriteA':   u33.3i   ;05
WriteA':   u41.3i   ;05
WriteA':   u49.3i   ;05
WriteA':   u57.3i   ;05
WriteA':   u65.3i   ;05
WriteA':   u73.3i   ;05
WriteA':   u81.3i   ;05
WriteA':   u89.3i   ;05
WriteA':   u97.3i   ;05
WriteA':   v05.3i   ;05
WriteA':   v13.3i   ;05
WriteA':   v21.3i   ;05
WriteA':   v29.3i   ;05
WriteA':   v37.3i   ;05
WriteA':   v45.3i   ;05
WriteA':   v53.3i   ;05
WriteA':   v61.3i   ;05
WriteA':   v69.3i   ;05
WriteA':   #R9.2i   ;17
WriteA':   #TP016.1i   ;20

WriteAz':  v77.3o   ;03
WriteAz':  #R9.1o   ;17

WriteB':   u02.3i   ;06
WriteB':   u10.3i   ;06
WriteB':   u18.3i   ;06
WriteB':   u26.3i   ;06
WriteB':   u34.3i   ;06
WriteB':   u42.3i   ;06
WriteB':   u50.3i   ;06
WriteB':   u58.3i   ;06
WriteB':   u66.3i   ;06
WriteB':   u74.3i   ;06
WriteB':   u82.3i   ;06
WriteB':   u90.3i   ;06
WriteB':   u98.3i   ;06
WriteB':   v06.3i   ;06
WriteB':   v14.3i   ;06
WriteB':   v22.3i   ;06
WriteB':   v30.3i   ;06
WriteB':   v38.3i   ;06
WriteB':   v46.3i   ;06
WriteB':   v54.3i   ;06
WriteB':   v62.3i   ;06
WriteB':   v70.3i   ;06
WriteB':   #R19.2i  ;17
WriteB':   #TP022.1i   ;20

WriteBz':  v84.12o  ;03
WriteBz':  #R19.1o  ;17

WriteC':   u03.3i   ;07
WriteC':   u11.3i   ;07
WriteC':   u19.3i   ;07
WriteC':   u27.3i   ;07
WriteC':   u35.3i   ;07
WriteC':   u43.3i   ;07
WriteC':   u51.3i   ;07
WriteC':   u59.3i   ;07
WriteC':   u67.3i   ;07
WriteC':   u75.3i   ;07
WriteC':   u83.3i   ;07
WriteC':   u91.3i   ;07
WriteC':   u99.3i   ;07
WriteC':   v07.3i   ;07
WriteC':   v15.3i   ;07
WriteC':   v23.3i   ;07
WriteC':   v31.3i   ;07
WriteC':   v39.3i   ;07
WriteC':   v47.3i   ;07
WriteC':   v55.3i   ;07
WriteC':   v63.3i   ;07
WriteC':   v71.3i   ;07
WriteC':   #R29.2i  ;17
WriteC':   #TP028.1i   ;20

WriteCz':  v79.9o   ;03
WriteCz':  #R29.1o  ;17

WriteD':   u04.3i   ;08
WriteD':   u12.3i   ;08
WriteD':   u20.3i   ;08
WriteD':   u28.3i   ;08
WriteD':   u36.3i   ;08
WriteD':   u44.3i   ;08
WriteD':   u52.3i   ;08
WriteD':   u60.3i   ;08
WriteD':   u68.3i   ;08
WriteD':   u76.3i   ;08
WriteD':   u84.3i   ;08
WriteD':   u92.3i   ;08
WriteD':   v00.3i   ;08
WriteD':   v08.3i   ;08
WriteD':   v16.3i   ;08
WriteD':   v24.3i   ;08
WriteD':   v32.3i   ;08
WriteD':   v40.3i   ;08
WriteD':   v48.3i   ;08
WriteD':   v56.3i   ;08
WriteD':   v64.3i   ;08
WriteD':   v72.3i   ;08
WriteD':   #R39.2i  ;17
WriteD':   #TP034.1i   ;20

WriteDz':  v85.14o  ;03
WriteDz':  #R39.1o  ;17

WriteE':   u05.3i   ;09
WriteE':   u13.3i   ;09
WriteE':   u21.3i   ;09
WriteE':   u29.3i   ;09
WriteE':   u37.3i   ;09
WriteE':   u69.3i   ;09
WriteE':   v01.3i   ;09
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WriteE':   v33.3i   ;09
WriteE':   v65.3i   ;09
WriteE':   v73.3i   ;09
WriteE':   v41.3i   ;09
WriteE':   v09.3i   ;09
WriteE':   u77.3i   ;09
WriteE':   u45.3i   ;09
WriteE':   u53.3i   ;09
WriteE':   u85.3i   ;09
WriteE':   v17.3i   ;09
WriteE':   v49.3i   ;09
WriteE':   v57.3i   ;09
WriteE':   v25.3i   ;09
WriteE':   u93.3i   ;09
WriteE':   u61.3i   ;09
WriteE':   #R49.2i  ;17
WriteE':   #TP056.1i   ;20

WriteEz':  v80.7o   ;04
WriteEz':  #R49.1o  ;17

WriteF':   u06.3i   ;10
WriteF':   u38.3i   ;10
WriteF':   u70.3i   ;10
WriteF':   v02.3i   ;10
WriteF':   v34.3i   ;10
WriteF':   v66.3i   ;10
WriteF':   v74.3i   ;10
WriteF':   v42.3i   ;10
WriteF':   v10.3i   ;10
WriteF':   u78.3i   ;10
WriteF':   u46.3i   ;10
WriteF':   u14.3i   ;10
WriteF':   u22.3i   ;10
WriteF':   u54.3i   ;10
WriteF':   u86.3i   ;10
WriteF':   v18.3i   ;10
WriteF':   v50.3i   ;10
WriteF':   v58.3i   ;10
WriteF':   v26.3i   ;10
WriteF':   u94.3i   ;10
WriteF':   u62.3i   ;10
WriteF':   u30.3i   ;10
WriteF':   #R59.2i  ;17
WriteF':   #TP062.1i   ;20

WriteFz':  v86.16o  ;04
WriteFz':  #R59.1o  ;17

WriteG':   v59.3i   ;11
WriteG':   v27.3i   ;11
WriteG':   u95.3i   ;11
WriteG':   u63.3i   ;11
WriteG':   u31.3i   ;11
WriteG':   u23.3i   ;11
WriteG':   u15.3i   ;11
WriteG':   u07.3i   ;11
WriteG':   u39.3i   ;11
WriteG':   u71.3i   ;11

WriteG':   v03.3i   ;11
WriteG':   v35.3i   ;11
WriteG':   v67.3i   ;11
WriteG':   v75.3i   ;11
WriteG':   v43.3i   ;11
WriteG':   v11.3i   ;11
WriteG':   u79.3i   ;11
WriteG':   u47.3i   ;11
WriteG':   u55.3i   ;11
WriteG':   u87.3i   ;11
WriteG':   v19.3i   ;11
WriteG':   v51.3i   ;11
WriteG':   #R69.2i  ;17
WriteG':   #TP068.1i   ;20

WriteGz':  v87.5o   ;04
WriteGz':  #R69.1o  ;17

WriteH':   u08.3i   ;12
WriteH':   u40.3i   ;12
WriteH':   u72.3i   ;12
WriteH':   v04.3i   ;12
WriteH':   v36.3i   ;12
WriteH':   v68.3i   ;12
WriteH':   v76.3i   ;12
WriteH':   v44.3i   ;12
WriteH':   v12.3i   ;12
WriteH':   u80.3i   ;12
WriteH':   u48.3i   ;12
WriteH':   u16.3i   ;12
WriteH':   u24.3i   ;12
WriteH':   u56.3i   ;12
WriteH':   u88.3i   ;12
WriteH':   v20.3i   ;12
WriteH':   v52.3i   ;12
WriteH':   v60.3i   ;12
WriteH':   v28.3i   ;12
WriteH':   u96.3i   ;12
WriteH':   u64.3i   ;12
WriteH':   u32.3i   ;12
WriteH':   #R79.2i  ;17
WriteH':   #TP074.1i   ;20

WriteHz':  v82.18o  ;04
WriteHz':  #R79.1o  ;17

ZGND:   E90, E80, E70, E60, E40, E30  ;19
ZGND:   E20, E10, E110, E120, E130
ZGND:   E140, E160, E170, E180, E190
ZGND:   #C193.2i, #C164.2i, #C107.2i
ZGND:   #C42.2i, #C202.2i, #C203.2i
ZGND:   #C204.2i, #C41.1i, #C187.1i
ZGND:   #CR1.1o  ;19

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ZM5V:   #F1.2o, #C41.2i, #C187.2i  ;19
ZM5V:   #C86.1i, #C88.1i, #C90.1i  ;21
ZM5V:   #C91.1i, #C93.1i, #C95.1i
ZM5V:   #C97.1i, #C100.1i, #C102.1i
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ZM5V:   #C110.1i, #C112.1i, #C114.1i
ZM5V:   #C117.1i, #C119.1i, #C121.1i
ZM5V:   #C123.1i, #C124.1i, #C43.1i
ZM5V:   #C45.1i, #C47.1i, #C49.1i
ZM5V:   #C52.1i, #C54.1i, #C56.1i
ZM5V:   #C58.1i, #C59.1i, #C61.1i
ZM5V:   #C63.1i, #C65.1i, #C68.1i
ZM5V:   #C70.1i, #C72.1i, #C74.1i
ZM5V:   #C75.1i, #C77.1i, #C79.1i
ZM5V:   #C84.1i, #C2.1i, #C4.1i
ZM5V:   #C6.1i, #C8.1i, #C9.1i
ZM5V:   #C11.1i, #C13.1i, #C15.1i
ZM5V:   #C18.1i, #C20.1i, #C22.1i
ZM5V:   #C24.1i, #C25.1i, #C27.1i
ZM5V:   #C29.1i, #C31.1i, #C34.1i
ZM5V:   #C36.1i, #C38.1i, #C40.1i
ZM5V:   #C126.1i, #C128.1i, #C130.1i
ZM5V:   #C133.1i, #C135.1i, #C137.1i
ZM5V:   #C139.1i, #C140.1i, #C142.1i
ZM5V:   #C144.1i, #C146.1i, #C149.1i
ZM5V:   #C151.1i, #C153.1i, #C155.1i
ZM5V:   #C156.1i, #C158.1i, #C160.1i
ZM5V:   #C162.1i, #C166.1i
ZM5V:   #C81.1i, #C183.1i, #C170.1i   ;23
ZM5V:   #C172.1i, #C173.1i, #C175.1i
ZM5V:   #C177.1i, #C179.1i

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ZP12V:  #C96.1i, #C99.1i, #C101.1i
ZP12V:  #C103.1i, #C105.1i
ZP12V:  #C109.1i, #C111.1i
ZP12V:  #C113.1i, #C115.1i
ZP12V:  #C116.1i, #C118.1i
ZP12V:  #C120.1i, #C122.1i
ZP12V:  #C131.1i, #C132.1i
ZP12V:  #C134.1i, #C136.1i, #C46.1i
ZP12V:  #C48.1i, #C50.1i, #C51.1i
ZP12V:  #C53.1i, #C55.1i, #C57.1i
ZP12V:  #C60.1i, #C62.1i, #C64.1i
ZP12V:  #C66.1i, #C69.1i, #C73.1i
ZP12V:  #C76.1i, #C78.1i, #C80.1i
ZP12V:  #C82.1i, #C83.1i, #C85.1i
ZP12V:  #C87.1i, #C1.1i, #C3.1i
ZP12V:  #C5.1i, #C7.1i, #C180.1i
ZP12V:  #C10.1i, #C12.1i, #C14.1i
ZP12V:  #C16.1i, #C17.1i, #C19.1i
ZP12V:  #C21.1i, #C23.1i, #C26.1i
ZP12V:  #C28.1i, #C30.1i, #C32.1i
ZP12V:  #C33.1i, #C37.1i, #C44.1i
ZP12V:  #C138.1i, #C141.1i
ZP12V:  #C143.1i, #C145.1i
ZP12V:  #C147.1i, #C148.1i
ZP12V:  #C150.1i, #C152.1i
ZP12V:  #C154.1i, #C157.1i
ZP12V:  #C159.1i, #C161.1i
ZP12V:  #C163.1i, #C165.1i

ZP12V:  #C167.1i, #C169.1i
ZP12V:  #C171.1i, #C174.1i
ZP12V:  #C176.1i, #C178.1i

ZP5V:   #R111.1i, #R109.1i, #R107.1i  ;18
ZP5V:   #R105.1i, #R103.1i
ZP5V:   #F2.2o, #C203.1i, #C202.1i ;19
ZP5V:   #C204.1i
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XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11186	SHEET REV.
	TITLE SCHEMATIC, MSC	A4	SHEET 51 OF	B