8. RS232C Controller
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8. RS232C Controller

The RS232C controller provides a channel for communication between the Dove machine and external devices like print servers or printers. Figure 8.1 illustrates the RS232C controller as it applies to the overall IOP board.

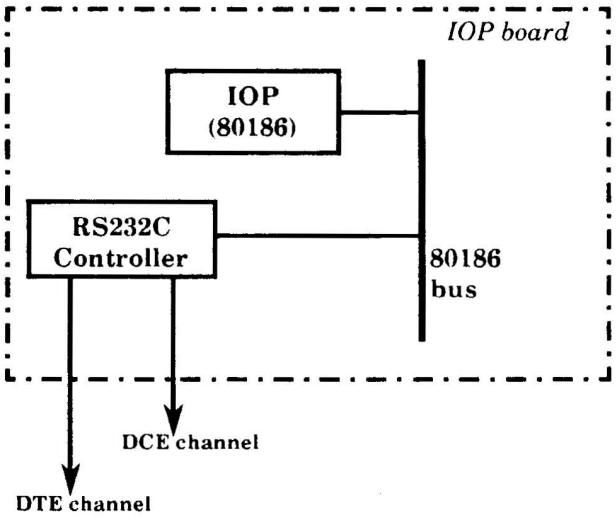

Figure 8.1. RS232C block diagram

8.1 Hardware

The RS232C controller consists of the following components:

- Serial controller
- System interface
- Two serial channels

8.1.1 Serial Controller

The RS232C controller consists of an integrated multi-protocol Intel 8274 serial controller (MPSC) and an Intel 8254 timer. The 8274 chip supports RS232C requirements directly and provides parity and CRC generation and checking. Two bytes of buffering are provided in the controller. The 8254 chip provides the timing function for the system.

8.1.1.1. Controller

Figure 8.2 illustrates the pins and signals of the serial controller. Table 8.1 lists the pins by name and number and explains their function in the controller system.

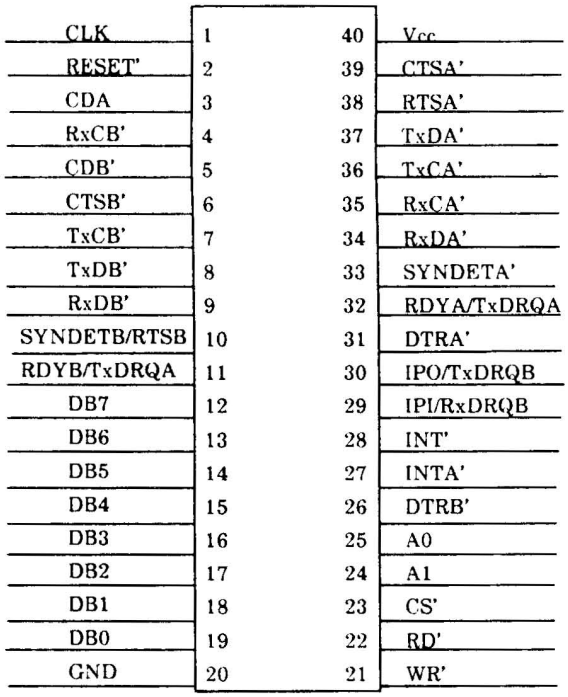

Figure 8.2. 8274 serial controller pins and signals

Table 8.1. 8274 Serial Controller Pin Assignments

Symbol	Pin #	Type	Name and Function
CLK	1	I	**Clock:** System clock, TTL compatible.
RESET'	2	I	**Reset:** A low signal on this pin forces the MPSC to an idle state. TxDA and TxDB are forced high. The modem interface output signals are forced high. The MPSC will remain idle until the control registers are initialized. Reset must be true for one complete clock cycle.
CDA'	3	I	**Carrier Detect (Channel A):** This interface signal is supplied by the modem to indicate that a data carrier signal has been detected and that a valid data signal is present on the RxDA line. If the auto enable control is set, then the 8274 will not enable the serial receiver until CDA' has been activated.
RxCB'	4	I	**Receive Clock (Channel B):** The serial data are shifted into the receive data input (RxDB') on the rising edge of the receive clock.
CDB'	5	I	**Carrier Detect (Channel B):** This interface signal is supplied by the modem to indicate that a data carrier signal has been detected and that a valid data signal is present on the RxDB line. If the auto enable control is set, then the 8274 will not enable the serial receiver until CDB' has been activated.
CTSB'	6	I	**Clear to Send (Channel B):** This interface signal is supplied by the modem in response to an active RTS' signal. CTS' indicates that the data terminal/computer equipment is permitted to transmit data. In addition, if the auto enable control is set, then the 8274 will not transmit data bytes until CTS' has been activated.
TxCB'	7	I	**Transmit Clock (Channel B):** The serial data is shifted out from the transmit data output (TxDB) on the falling edge of the transmit clock.

- more -

Table 8.1. 8274 Serial Controller Pin Assignments (continued)

Symbol	Pin #	Type	Name and Function
TxDB'	8	O	**Transmit Data (Channel B):** This pin transmits serial data to the communications channel (Channel B).
RxDB'	9	I	**Receive Data (Channel B):** This pin receives serial data from the communications channel (Channel B).
SYNDETB/ RTSB	10	I/O	**Synchronous Detection (Channel B):** This pin is used in byte synchronous mode either as an internal sync detect (output) or as a means to force external synchronization (input). In SDLC mode, this pin is an output indicating flag detection. In asynchronous mode it is a general purpose input (Channel B). Request To Send (Channel B): General purpose output, generally used to signal that Channel B is ready to send data. SYNDETB' or RTSB' selection is done by WR2; D7 (Channel A).
DB7-DB0	12 - 19	I/O	**Data Bus:** The Data Bus lines are bidirectional three-state lines which interface with the system's Data Bus.
CTSA'	39		**Clear to Send (Channel A):** This interface signal is supplied by the modem in response to an active RTS' signal. CTS' indicates that the data terminal/computer equipment is permitted to transmit data. In addition, if the auto enable control is set, then the 8274 will not transmit data bytes until CTS' has been activated.
RTSA'	38	O	**Request to Send (Channel A):** General purpose output commonly used to signal that Channel A is ready to send data.
TxDA	37	O	**Transmit Data (Channel A):** This pin transmits serial data to the communications channel (Channel A).
TxCA'	36	I	**Transmit Clock (Channel A):** The serial data is shifted out from the transmit data output (TxDA) on the falling edge of the transmit clock.
RxCA'	35	I	**Receive Clock (Channel A):** The serial data is shifted into the receive data input (TxDA) on the rising edge of the receive clock.
RxDA'	34	I	**Receive Data (Channel A):** This pin receives serial data from the communications channel (Channel A).
DTRA'	31	O	**Data Terminal Ready (Channel A):** General purpose output.
IPI/RxDRQB	29	I/O	**Interrupt Priority In/Receiver DMA Request (Channel B):** In modes 0 and 1, IPI' is Interrupt Priority In. A low on IPI' means that no higher priority device is being serviced by the controlling processor's interrupt service routine. In mode 2 this pin is RxDRQB and is used to request a DMA cycle for a receive operation (Channel B). In interrupt mode, this pin must be tied low.
INT'	28	O	**Interrupt:** The interrupt signal indicates that the highest priority internal interrupt requires service (open collector). Priority can be resolved via an external interrupt controller or a daisy-chain scheme.
INTA'	27	I	**Interrupt Acknowledge:** This interrupt acknowledge signal allows the highest priority interrupting device to generate an interrupt vector. This pin must be pulled high (inactive) in non-vector mode.
DTRB'	26	O	**Data Terminal Ready (Channel B):** General purpose output.
A0	25	I	**Address:** This line selects Channel A or B during data or command transfers. A low selects Channel A.
A1	24	I	**Address:** This line selects between data or command information transfer. A low selects data transfer.
CS'	23	I	**Chip Select:** This signal selects the MSPC and enables reading from or writing into its registers.
RD'	22	I	**Read:** Read controls a data byte or status byte transfer from the MPSC to the CPU.
WR'	21	I	**Write:** Write controls transfer of data or commands to the MPSC.

Pin 20 = GND
Pin 40 = Vcc (+5 V power supply)
Pins 11, 30, 32, and 33 are not used.

8.1.1.2. Timer

The serial controller contains a 24-pin chip that provides the internal timing for the RS232C subsystem.

Table 8.2 lists the appropriate time constants that should be used to initialize the 8254 in order to achieve a desired baud rate. Because the 8254 input is driven by a fixed system clock, there is usually a small error between the exact clock frequency required for a given baud rate and the clock frequency produced by the 8254. The amount of expected error is also shown in Table 8.2.

Table 8.2. Baud Rate Constants

Baud Rate	Time Constant (Hex)	Error
9600	26 (001AH)	0.16 %
7200	35 (0023H)	0.79%
4800	52 (0034H)	0.16%
3600	69 (0045H)	0.64%
2400	104 (0068H)	0.16%
2000	125 (007DH)	0%
1800	139 (008BH)	0.08%
1200	208 (00D0H)	0.16%
600	417 (01A1H)	0.08%
300	833 (0341H)	0.04%
150	1667 (0683H)	0.02%
134.5	1859 (0743H)	0.01%
110	2272 (0BE0H)	0.03%
75	3333 (0D05H)	0.01%
50	5000 (1388H)	0%

Figure 8.3 illustrates the pins and signals of the 8254 timer. Table 8.3 lists the pins and explains their function.

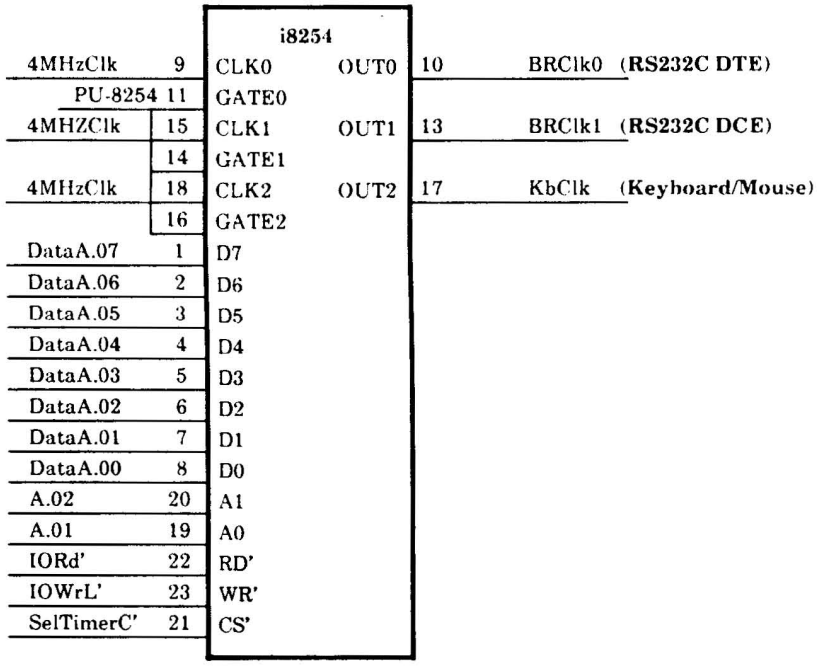

Figure 8.3. 8254 timer pins and signals

Table 8.3. 8254 Timer Pin Assignments

Symbol	Pin #	Type	Name and Function
A1-A0	19,20	I	**Address:** Used to select one of the three counters or the control word register for read or write operations. Normally connected to the system address bus. A1 A0 Selects 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
Clk0	9	I	**Clock 0:** 4 MHz clock from Counter 0.
CLK1	15	I	**Clock 1:** 4 MHz clock from Counter 1.
CLK2	18	I	**Clock 2:** 4 MHz clock from Counter 2.
CS'	21	I	**Chip Select:** A low on this input enables the 8254 to respond to RD' and WR' signals. RD' and WR' are ignored otherwise.
D7-D0	1-8	I/O	**Data:** Bi-directional three-state data bus lines, connected to system data bus.
Gate0	11	I	**Gate 0:** High.
Gate1	14	I	**Gate 1:** High.
Gate2	16	I	**Gate2:** High.
OUT0	10	O	**Output 0:** Output of Counter 0 to RS232C DTE.
OUT1	13	O	**Output 1:** Output of Counter 1 to RS232C DCE.
OUT2	17	O	**Output 2:** Output of Counter 2 to Keyboard/Mouse.
RD'	22	I	**Read Control:** Low during CPU read operations.
WR'	23	I	**Write Control:** Low during CPU write operations.

Pin 12 is Ground

Pin 24 is Vcc (+5 V power supply connection)

8.1.2 Interfaces

The 8274 is an interrupt-driven device that operates in vectored and nonvectored mode. Only nonvectored mode may be used in this design. Reset must be true for one complete system clock cycle for proper interrupt reset (250 ns). Wr' signal must be greater than 250 ns. One wait state is necessary to satisfy tRR, tWW, and tRD set-up and hold requirements. The leading edge of RD' sets the in-service latch. The CPU should read RR2 of Channel B to determine which internal source requested service.

8.1.2.1. System Interface Signals

Figure 8.4 illustrates how the serial controller interfaces to the system. Table 8.4 briefly summarizes the signals (described in Table 8.1).

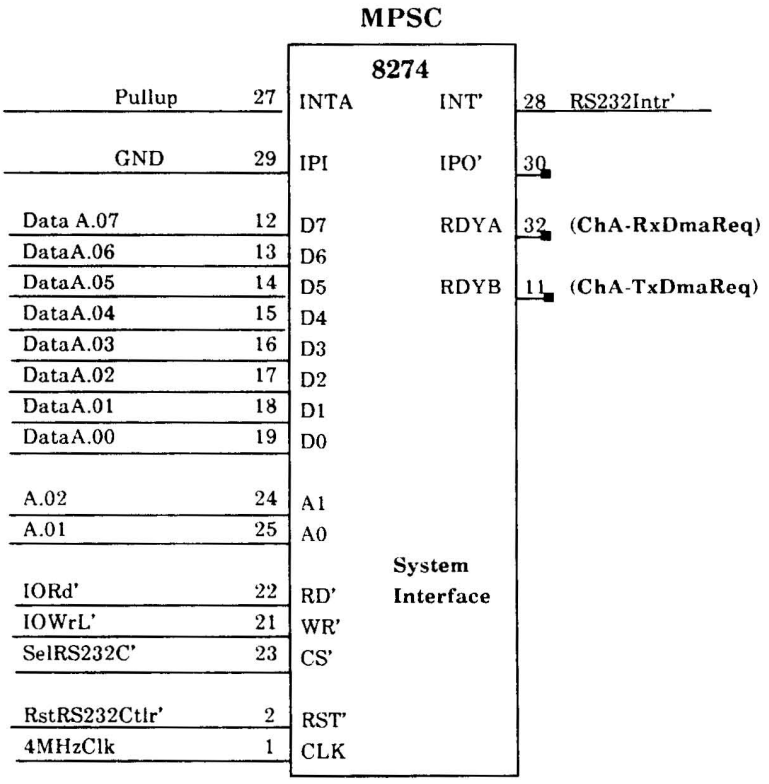

Figure 8.4. RS232C system interface pins and signals

Table 8.4. System Interface Pin Assignments

Symbol	Pin #	Type	Name and Function
INTA	27	I	Allows the 8274 to generate an interrupt vector when the CAS lines decode to "4" (100). For polling, INTA' = H.
IPI	29	I	Indicates to the 8274 that the current interrupt acknowledge cycle is intended for the 8274. Refer also to text.
D7-D0	12-19	I/O	Three-state data lines used by the 80186 to communicate with the 8274.
INT'	28	O	Indicates that an interrupt condition has been encountered in the 8274.
A1	24	I	Selects between data (0) or command (1) registers during an access cycle to the 8274.
A0	25	I	Selects between channel A (0) or channel B (1) registers during an access cycle to the 8274.
RD'	22	I	Indicates that the current access cycle is a read cycle.
WR'	21	I	Indicates that the current access cycle is a write cycle.
CS'	23	I	Enables the 8274 for the current access cycle.
RST'	2	I	Resets the 8274 when driven to 0.
CLK	1	I	4 MHz clock used by the 8274 as its internal system clock.

Pins 11, 30, and 32 are not used.

8.1.2.2. 8274 Interface Ports

The 8274 interface has two ports: Channel A and Channel B. Channel A port is configured as a DTE port; Channel B is configured as a DCE port. The DTE port connects to communication equipment for remote and standalone workstations. The DCE port is primarily for local printers, and usually operates in asynchronous mode as a TTY port. Synchronous operation is possible, however, through the DTE port.

Figure 8.5 illustrates how the 8274 serial controller interfaces to the RS232C channel A DTE port.

Figure 8.6 illustrates the same for the RS232C channel B DCE port.

The 8274 signals are described in Table 8.1.

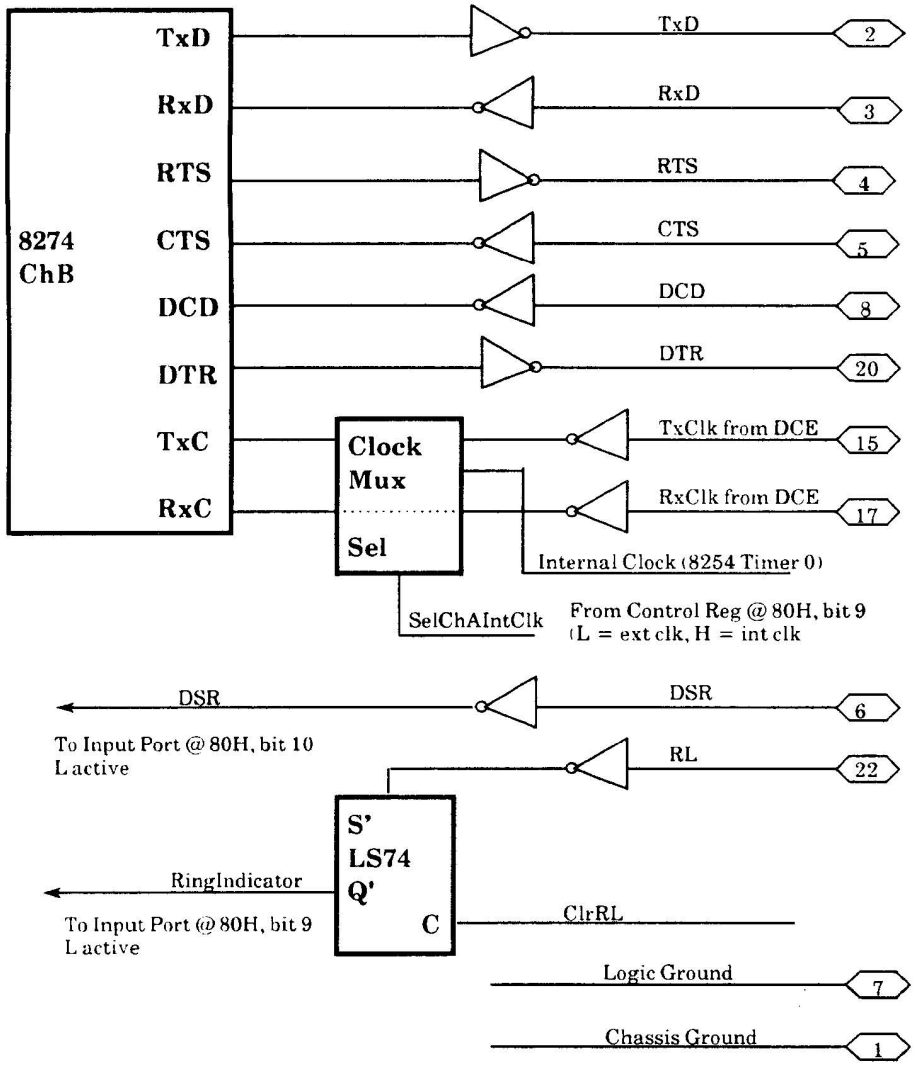

Figure 8.5. RS232C channel A DTE port

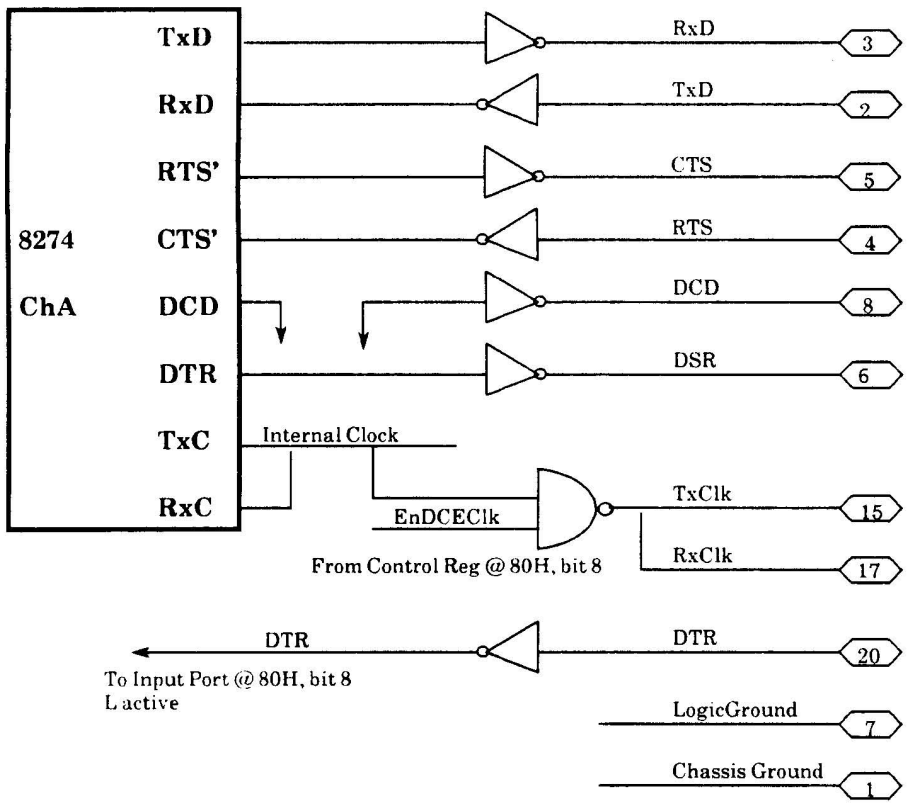

Figure 8.6. RS232C channel B DCE port

8.1.2.3. Interface Connectors

The RS232C interface uses a 25-pin DB type connector. Typically, DTE uses a male connector, and DCE uses a female connector. RS232C signal names are written to and read from the DTE.

Table 8.5 summarizes the interface signals that are available on the connectors. The direction of flow for signals between a DCE and a DTE port is also listed.

Table 8.5. Interface Signals

Connector Pin No	Signal Name	Direction of Flow	Signal Type	Active Level (nominal)
1	GND Chassis Ground	DTE-DCE		
2	TxD Transmitted Data	DTE→DCE	Data	-12v
3	RxD Received Data	DTE←DCE	Data	-12v
4	RTS Request to Send	DTE→DCE	Control	+12v
5	CTS Clear To Send	DTE←DCE	Control	+12v
6	DSR Data Set Ready	DTE←DCE	Control	+12v
7	SG Signal Ground	DTE-DCE		
8	DCD Data Carrier Detect	DTE←DCE	Control	+12v
15	TxC Transmitter Clock	DTE←DCE	Timing	
17	RxC Receiver Clock	DTE←DCE	Timing	
20	DTR Data Terminal Ready	DTE→DCE	Control	+12v
22	RI Ring Indicator	DTE←DCE	Control	+12v

8.1.3 Serial Channels

The ports provide two independent full duplex channels; the channels are illustrated in Figure 8.6. Asynchronous, byte-and bit-synchronous transfers at data rates up to 9600 bps are possible. Byte-synchronous protocols include IBM Bisync; bit-synchronous protocols will include SDLC/HDLC.

Both channels provide asynchronous, byte-synchronous and bit-synchronous operations up to 9600 Baud. Both channels are interrupt-driven.

Signal voltages on the interface lines are standard RS232 levels. There are two types of signals: data signals and control signals. Data signals are TxD and RxD. All other signals are control signals.

8.2 Theory of Operations

DMA resources are not available to the 8274, which is an interrupt-driven device.

Figure 8.7 illustrates the data paths of the RS232C controller. The circled number is the sequence number, as described in the following outline of the 8274 acknowledge procedure.

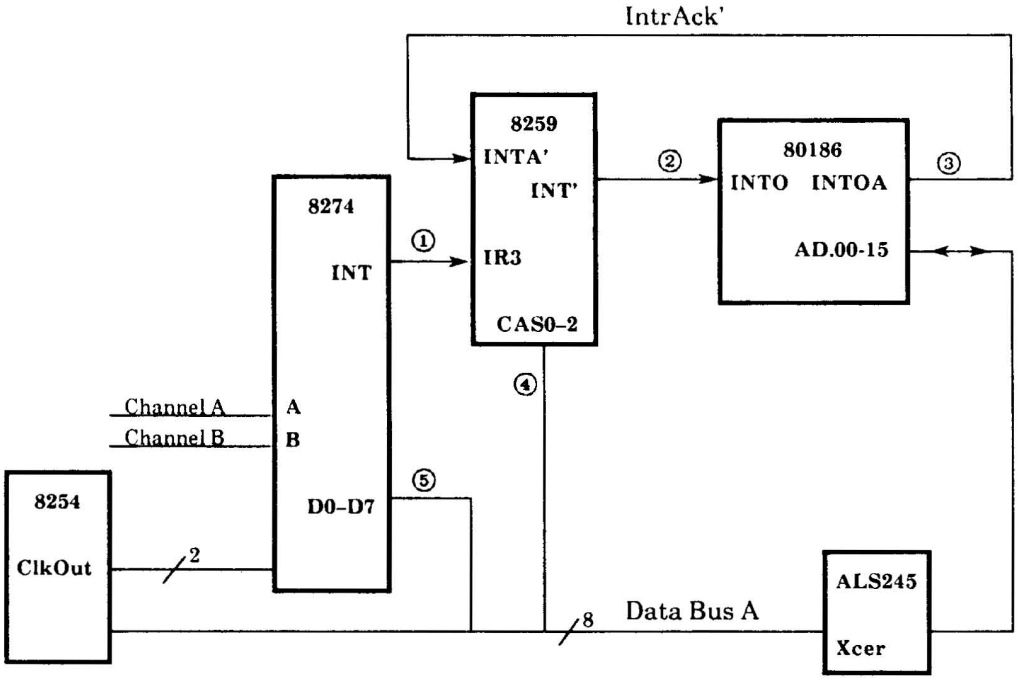

Figure 8.7. RS232C controller data paths

1) When an internal interrupt condition is sensed by the 8274, the 8274 sends an interrupt request to the master interrupt controller 8259.

2) If the interrupt request meets the conditions of that time, then the 8259 sends an interrupt to the 80186 microprocessor.

3) When the 80186 is able to service the interrupt, the 80186 responds with two contiguous interrupt acknowledge cycles.

4) The master 8259 delivers the interrupt vector on the data bus during the second INTA cycle. The 80186 then processes the interrupt vector to obtain the address of the interrupt service routine in memory. The 80186 will begin execution at that location.

Figure 8.8 illustrates timing for the acknowledge operation.

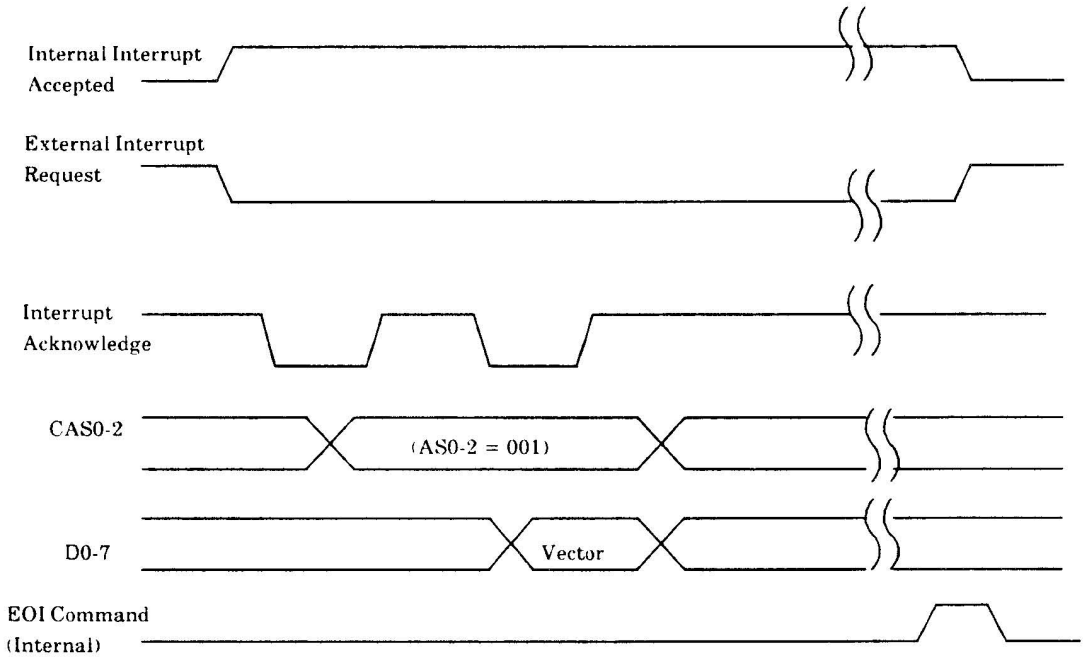

Figure 8.8. Timing for 8274 interrupt acknowledge

8.3 Programmer Interface: Registers

This section describes the IOP registers that affect RS232C operation, the 8274 serial controller registers and the 8254 timer registers.

8.3.1 External Registers

The IOP control and reset registers contain bits for RS232C operation.

The DTE port (CHA) has a ring indicator whose output (active high) may be obtained at bit 9 of the input register 80H. The ring indicator may be reset by an "IN" instruction to address A0H.

Also available at the input register are Channel A DSR signal state (active low) on bit 10 and the Channel B DTR signal (active low) on bit 8.

The DTE channel may use an internal receive and transmit clock from the 8254, or external clocks from the interface connector (SDLL). Bit 9 of the control register (80H) determines which clock is used, as follows:

0 = external clocks
1 = internal clock

The transmit and receive clock of the DCE port may be enabled or disabled from the interface connector by bit 8 of the control register (80H), as follows:

0 = drive is disabled, and pins 15 and 17 are held at an RS232C high level; that is, 12 V.

1 = clock driver enabled; drives the DCE clock onto pins 15 and 17 or to the DCE connector.

8.3.2 8274 Serial Controller Registers

The serial controller registers appear as eight I/O registers to the 80186. Each register is accessed by reading from or writing to a physical register location. Table 8.6 lists the register locations.

Table 8.6. Serial Controller Registers

Register	R/W	Address
Channel A Receive Data	R	40H
Channel A Transmit Data	W	40H
Channel B Receive Data	R	42H
Channel B Transmit Data	W	42H
Channel A Status	R	44H
Channel A Command	W	44H
Channel B Status	R	46H
Channel B Command	W	46H

To access a given register, the lower three bits of WR0 must be set to indicate which register will be read from or written to next. For example, to read RR3 or write WR3, xxxxx011 must be written to WR0; when the 8274 is reset, WR0 will point to 0, and the first access will read RR0 or write WR0.

Each channel of the serial controller has eight write registers for commands and three read registers for status.

8.3.2.1. Write Registers

Write registers on the 8274 should be initialized prior to use, as their reset states are not stable. Write register 4 (WR4) must be the first register initialized. Write xxxxx100 initializes WR4.

In addition, the 8254 should be initialized to provide the proper transmit or receive clock for the desired baud rate (refer to Table 8.2).

Tables 8.7 - 8.15 list the bit assignments for the write registers.

Table 8.7. Write Register 0 (WR0)

Bit	Assignment
D0-D2	Command/Status register pointer.
D5-D3	Command 000 Null code 001 Send abort (SDLC) 010 Reset EXT/Status interrupts 011 Channel reset 100 Enable interrupt on next Rx character 101 Reset TxINT/DMA pending 110 Error reset 111 End of interrupt
D6-D7	Reset 00 Null code 01 Reset Rx CRC checker 10 Reset Tx CRC generator 11 Reset Tx Underrun/EOM latch

Table 8.8. Write Register 1 (WR1)

Bit	Assignment
D0	Ext interrupt enable
D1	TxInterrupt/DMA enable
D2	Status affects vector Channel B only (null code Channel A) 1 Variable vector 0 Fixed vector
D3-D4	Set interrupt 00 RxINT/DMA disable 01 RxInt on first char or special condition. 10 Int on all Rx char (parity affects vector) or special condition. 11 Int on all Rx char (parity does not affect vector) or special condition.
D5	1 Wait on Rx 0 Wait on Tx
D6	Must be 0
D7	Wait enable 1 Enable 0 Disable

Table 8.9. Write Register 2 (WR2): Channel A

Bit	Assignment
D1-D0	Interrupt/DMA 00 Both interrupt 01 A DMA, B INT 10 Both DMA 11 Illegal
D2	Priority 1 Priority RxA, RxB, TxA, TxB, EXTA, EXTB 0 Priority RxA, TxA, RxB, TxB, EXTA, EXTB
D4-D3	Mode 00 8085 Mode 1 01 8085 Mode 2 10 8086/88 Mode 11 ILLEGAL
D5	Specify Interrupt type 1 Vectored Interrupt 0 Non-Vectored Interrupt
D6	Must be 0
D7	Pin select 1 Pin 10 SYNDET' 0 Pin 10 RTS'

Table 8.10. Write Register 2 (WR2): Channel B

Bit	Assignment
D0-D7	All assigned as interrupt vectors.

Table 8.11. Write Register 3 (WR3): Channel B

Bit	Assignment
D0	Rx Enable
D1	Sync char load inhibit
D2	Addr Srch Mode (SLDC)
D3	Rx CRC enable
D4	Enter Hunt Mode
D5	Auto enables
D6-D7	Bits/Char 00 Rx 5 bits/char 01 Rx 7 bIts/char 10 Rx 6 bits/char 11 Rx 8 bits/char

Table 8.12. Write Register 4 (WR4)

Bit	Assignment
D0	Parity 1 Enable parity 0 Disable parity
D1	Even/Odd parity 1 Even parity 0 Odd parity
D2-D3	Sync Modes 00 Enable Sync Modes 01 1 Stop bit 10 1.5 Stop bits 11 2 Stop bits
D4-D5	Sync 00 8 bit Sync char 01 16 bit Sync char 10 SDLC/HLDC Mode (01111110) flag 11 External Sync Mode
D6-D7	Clock 00 X1 clock 01 X16 clock 10 X32 clock 11 X64 clock

Table 8.13. Write Register 5 (WR5)

Bit	Assignment
D0	Tx CRC enable
D1	RTS
D2	SDLC/CRC-16 (CRC Mode)
D3	Tx enable
D4	Send break
D5-D6	Transmit character length 00 Tx 5 bits or less/char 01 Tx7 bits/char 10 Tx 6 bits/char 11 Tx 8 bits/char

Table 8.14. Write Register 6 (WR6)

Bit	Assignment
D0-7	Least significant sync byte (address in SLDC/HLDC Mode)

Table 8.15. Write Register 7 (WR7)

Bit	Assignment
D0-7	Most significant sync byte. (Must be 01111110 in SDLC/HDLC Mode.)

8.3.2.2. Read Registers

Tables 8.16 - 8.18 list the bit assignments for the three read registers.

Table 8.16. Read Register 0 (RR0)

Bit	Assignment
D0	Rx char available
D1	Int pending (ChA only)
D2	Tx buffer empty
D3	Carrier detect
D4	Sync/Hunt
D5	CTS
D6	Tx Underrun/EOM
D7	Break/Abort

Table 8.17. Read Register 1 (RR1): Special Receive Condition Mode

Bit	Assignment		
D0	All sent		
D1-D3		I Field Bits Previous Byte	I Field Bits 2nd Previous Byte
	000	2	8
	001	0	6
	010	0	4
	011	0	8
	100	0	3
	101	0	7
	110	0	5
	111	1	8
D4	Parity error		
D5	Rx overrun error		
D6	CRC/Framing error		
D7	End of frame(SDLC/HLDC Mode)		

Table 8.18. Read Register 2 (RR2)

Bit	Assignment
D0-D7	Interrupt vectors or status affects vector Mode. Contains interrupt vector programmed into WR2. If status affects vector Mode is selected (WR1: D2), then the register contains the modified vector.

8.3.3 8254 Timer Registers

Table 8.19 summarizes the read and write operation for the 8254 timer.

Table 8.19. 8254 Timer Read/Write Operations

CS'	RD'	WR'	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 1
0	0	1	0	1	Read from Counter 1