Appendix A.

Daybreak Display Controller Chip

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Daybreak Display Controller Chip

The Daybreak Display Controller (DDC) is a CMOS LSI chip designed for use in the Daybreak system. Appendix A reprints information about the chip, including:

- Software differences between DCM gate array display controller and DCM/DDC standard cell display controller
- Chip functional and timing specification

DCM board schematics with DDC are contained in Appendix B (printed separately).

Software Differences

This section is reprinted verbatim from a memo titled "DCM/DDC soft. differences," dated 6-Dec-85.

Software differences between DCM (gate array display cntrl) and DCM/DDC (standard cell display contrl):

REV C: added lines 10 and 11

1. Contents of horizontal and vertical control stores (proms) are different. This means DCM and DCM/DDC control stores are not interchangeable. A new Xerox part# number is being specified for DCM/DDC CS proms.
2. Contents of DCM/DDC horizontal and vertical control stores can be read by diagnostic routines. Contents of DCM control stores cannot be read.
3. Contents of DCM/DDC cursor buffer can be read by diagnostic routines. Contents of DCM cursor buffer cannot be read.
3. Gate array displays border registers in the following sequence: low, high, low, etc., whereas standard cell displays them high, low, high, etc.
   Fix, switch programmed values of border registers.
4. Cursor line number low: DCM; 6 bits wide (LSB)
   DCM/DDC; 8 bits wide (LSB)
5. Cursor line number high: DCM; 4 bits wide (MSB)
   DCM/DDC; 2 bits wide (MSB)
6. Cursor offset register of DCM/DDC contains a control bit (bit 7) called NCURSOR. A "0" in this bit enables the cursor while a "1" will disable cursor from display; default value is zero. DCM does not implement this function.

7. A "0" written to bit 1 (video enable bit) of DCM/DDC display control register (EC80) does not disable cursor on the screen. In order to completely blank out display monitor, two steps are required: disable video enable bit and NCURSOR bit. DCM video enable bit completely enable/disables data to screen.

8. DCM: video disabled, no vertical interrupts
   DCM/DDC: video disabled, vertical interrupts still enabled.
   Solution: Display handler disregards vertical interrupts whenever video disabled.

9. Display size/controller type status port – ECCC – bit 1
   DCM: always "1"
   DCM/DDC: always "0"

10. Standard cell DCC does not support cursor and data mixing function "F." I believe this mixing function is never used, but if it is, there are other ways to implement it (e.g., use function "C.")

11. Standard cell DCC does not support reading of status information.

Miscellaneous

1. All address decoding of registers, control stores, and cursor buffers are same between DCM and DCM/DDC.

Appendix A.

DDC Chip Functional & Timing Specification

DDC CHIP

I. INTRODUCTION

The Daybreak Display Controller (DDC) is a CMOS LSI chip designed for use in the Daybreak System. It is based on the Xerox CMOS-III Technology, and is intended to be used in both the 15 inch and the 19 inch black and white display system, running at a maximum clock frequency of 16 MHZ (64 MHZ pixel rate). It has a total of 88 input and output pins (including power and ground pin), and is currently housed in a 119 pin ceramic pin-grid package. It implements both the cursor and the border functions. A total of 16 cursor mixing functions are provided. It can handle a maximum of 2048 pixels (including horizontal sync) in the X dimension and a maximum of 1024 lines (including the vertical sync) in the Y dimension for the display. It can work in either interlaced mode or non-interlaced mode.

The DDC has 2 clock inputs, MC and RAWCLK, and they are asynchronous to each other. MC is 4 times slower than the dot-rate of the monitor and can go as high as 16 MHZ. Rawclk is designed for 16 MHZ. The chip is not guaranteed to work with MC greater than 14.2 MHZ and Rawclk slower than 16 MHZ - 5% in the worst case of memory performance.

II. THE INTERFACE PORTS

The DDC chip is designed to be used in an environment as depicted in Fig. 1.0. It consists of 4 separate I/O ports: 1) The System Interface Port, 2) The Control Store Port, 3) The Memory Controller Interface Port, 4) The Display Monitor Port. Figure 1.1 shows the corresponding interface ports of the chip.

2.1 THE SYSTEM INTERFACE PORT

This is a bi-directional asynchronous port to mainly interface with the 8086 system bus. Through the 8086 system bus, all necessary chip configurations can be programmed, such as: the bit-map start address, number of quadwords per Scan line, border information, cursor patterns and location, interlaced or non-interlaced, scan line length, bit map starting location, border pattern etc. The control store for DDC is also downloaded via this port.

Fig. 2.0 shows the 8086 system bus read/write timing into the chip, while Fig. 2.1 shows the direct read/write timing thru the chip to the control store memory.

2.2 THE CONTROL STORE PORT

This port interfaces with the local control store memory. Decoded addresses and data thru the 8086 system bus are transfered via this port and are written into the control store memory asynochronously with respect to the MC clock. Ten unidirectional address lines CSAØ to 9, four bidirectional data bus CSDØ to 3 together with the 3 control lines, namely NVCS (vertical control store memory select), NHCS (horizontal control store memory select) and the NCSWR (control store write enable) constitute this port. The Direct read/write timing from the system bus via this port is as shown in Figure 2.1. During the normal operation, the control store program is read into the chip via this port to be executed.

The timing for reading the control store during normal operations is shown in Fig. 2.2. The read of the control store is synchronous with the internal word clock (WC) of the DDC chip. WC is generated by MC divided by 4.

2.3 THE MEMORY INTERFACE PORT

This port interfaces solely with the memory controller to obtain the bit map data to be displayed. The DDC chip requests the bit-map data by lowering it's request signal (NCREQ) and at the same time sends out the corresponding address to the memory controller.

The memory controller, in response, sends back 4 consecutive acknowledge signals (NCXACK) along with 4 data words each 16 bits wide. The DDC uses the rising edge of NCXACK to strobe in the data. All signals in this port are synchronized to RAWCLK.

The timing for this port is shown in Figure 2.3.

2.4 THE DISPLAY MONITOR PORT

This port is a unidirectional interface between the DDC and the Display Monitor. Four video data output bits along with the vertical sync and the horizontal sync pulse are sent out at the rising edge of the MC clock to the Display Monitor. The maximum Output rate of the video data is at 16 MHZ per nibble, which translates to 64 MHZ pixel clock rate. Figure 2.4 shows the DDC video output timing. The video data is serialized externally to the chip, with the video data bit VID3 as the first and the VIDØ as the last video data to be sent to the monitor for display.

III. FUNCTIONAL PIN DEFINITIONS

Fig. 3.0 shows the pin assignment and both top and bottom view of the Daybreak Display controller (DDC) chip. The DDC chip is currently housed in a 119 pin ceramic pin-grid package. There are a total of 88 pins used, out of which thirty-six are input pins (including power and ground pins), forty are output pins and the rest are Bidirectional I/O pins.

3.1 CLOCK/RESET PINS

3.1.1 MC (CLOCK INPUT)

The MC clock pin receives an external input clock of 25% duty cycle (25% high, 75% low) T^2L signal and converts it into CMOS Level within the chip to be used by the internal logic. It also generates two divide down internal clock signals, namely BC (divided by 2) and WC (divided by 4) used by the internal chip logic.

3.1.2 NWC (CLOCK OUTPUT)

Inverted version of the internal clock signal WC (MC divided by four). Its main function is for testing the chip.

3.1.3 RAWCLK (CLOCK INPUT)

This clock signal is only used by the FIFO section in the DDC chip. The request signal NCXREQ and the address generated to the memory controller are in sync to this clock signal.

3.1.4. NHRST (INPUT - LOW TRUE RESET SIGNAL)

This signal will reset the "video" bit in the Display Control Register inside the DDC chip to zero, which blanks out all the video data output to the display monitor. It will at the same time disable the NCREQ signal from requesting any bit-map data from the memory controller. However, the DDC chip will still be fetching the control store data at a random fashion before the control store is properly initialized. The NHRST signal has no effect in resetting any internal data latches to a known state, nor will it tri-state any I/O signals of the DDC chip.

3.2 SYSTEM INTERFACE PORT PINS

3.2.1 NCS (INPUT - ACTIVE LOW CHIP SELECT)

A low on this pin enables I/O read/write communication between the DDC chip and the external system processor.

3.2.2 AAØØ THROUGH AA10 (INPUT ADDRESS PINS 0 TO 10)

These eleven pins point to either internal DDC registers or to external control store RAM.

3.2.3 NIOW (INPUT - ACTIVE LOW WRITE STROKE)

The system processor envokes the write strobe in conjunction with the chip select and address to deliver data to the internal location or to the external control store memory specified by the address.

3.2.4 NIOR (INPUT - ACTIVE LOW READ STROKE)

The system processor envokes the read strobe in conjunction with the chip select and address to access the internal cursor RAM contents or the control store memory contents. (other Internal Registers are not readable)

3.2.5 NVRET (OUTPUT - ACTIVE LOW VERTICAL RETRACE LINE)

This signal is the inverted version of the EOF (End of Field). Low for one scan line period.

3.2.6 DBØ THROUGH DB7 (BI-DIRECTIONAL - DATA PIN ØTO 7)

The data pins are used to provide the data for I/O transfers to and from the DDC chip. It is also used in conjuction with the Control Store Port of the DDC chip via its CSDØ:3 data bus for I/O transfer to and from the external control store memory.

3.3. THE CONTROL STORE PORT PINS

3.3.1 NVCS (OUTPUT - ACTIVE LOW VERTICAL CONTROL STORE MEMORY SELECT)

A Low on this pin enables I/O read/write communication between the DDC chip and the vertical control store memory.

3.3.2 NHCS (OUTPUT - ACTIVE LOW HORIZONTAL CONTROL STORE MEMORY SELECT)

A Low on this pin enables I/O read/write communication between the DDC chip and the horizontal control store memory.

3.3.3 CSA0 THRU CSA9 (OUTPUT ADDRESS PIN 0 TO 9)

These ten pins address the Control Store memory.

3.3.4 NCSWR (OUTPUT - LOW WRITE AND HIGH READ)

A Low on the signal will enable the write operation to the control store memory, while a high will read out the content of the control store memory. The signal stays high during normal operation.

3.3.5 CSD0 THRU CSD3 (BI-DIRECTION - DATA PIN 0 TO 3)

The data pins are the datapath for transfers between the DDC chip and the control store memory.

3.4 THE MEMORY INTERFACE PORT PINS

3.4.1 NCXREQ (OUTPUT - LOW TRUE REQUEST PIN)

A low on this signal indicates the DDC chip is requesting bit-map data from the external memory controller.

3.4.2 NCXACK (INPUT - LOW TRUE ACKNOWLEDGE PIN)

A high to low transition on this pin indicates that the bit-map data request by the DDC chip is accepted, and the bit-map data is valid on the data bus. The DDC chip uses the rising edge of this signal to latch in the data on the data bus.

3.4.3 CA03 THRU CA20 (OUTPUT - ADDRESS PIN 3 TO 20)

These eighteen address pins, generated by the DDC chip point to the current location of bitmap data. (The first address of a 4 word group)

3.4.4. CD00 THRU CD15 (INPUT - DATA PIN 0 TO 15)

These sixteen data pins are used to provide the bit-map data from the memory controller to the DDC chip.

3.5 THE DISPLAY MONITOR PORT PINS

3.5.1 VSYNC (OUTPUT SIGNAL)

This is the vertical sync pulse sent from the DDC chip to the display monitor. It is synchronized with the MC clock signal and is sent out at the rising edge of the MC clock.

3.5.2 HSYNC (OUTPUT SIGNAL)

This is the horizontal sync pulse sent from the DDC chip to the display monitor. It is synchronized and sent out at the rising edge of the MC clock.

3.5.3 VID0 THRU VID3 (OUTPUT - DATA PIN 0 TO 3)

These four output data pins carry the video display data from the DDC chip to the display monitor. It is synchronized and sent out at the rising edge of the MC clock.

3.6 VDD AND GND (INPUT PINS)

There is only one VDD and one ground pin for the DDC chip. VDD supplies 5 volts to the chip.

IV. SOFTWARE PROCEDURES AND PROGRAMMING

4.0 DESCRIPTION OF THE DDC CONTROL WORD ADDRESS AND FORMAT

Fig. 4.0 shows the DDC's relative control word address and format. It also includes a table showing the mixing function between the cursor and the bit-map data.

4.0.1 VERTICAL CONTROL STORE

The Vertical Control Store defines the characteristic of the scan lines to be displayed. Each control word in the vertical control store defines a whole scan line. It has a maximum capacity of up to 1024 vertical control word. The address for the vertical control store is E800to EBFF. The 5 MSB's of the 20 bit address line coming from the system bus are decoded externally as NCS comes into the DDC chip. The remaining 11 address lines come directly to the DDC chip. (It is assumed that throughout the remaining of the writing). As illustrated in Fig 4.0, only the lower nibble of the data byte constitute the control word. The definition of the Vertical Control word is as follows:

BITØ - VSYNC: a 1 in this bit will generate a line length of vertical sync.

BIT1 - VBLANK: a 1 in this bit will blank the whole line

BIT2 - VPIC: a 1 in this bit defines a picture line while a Ø defines the whole line as border.

BIT3 - EOF: a 1 in this bit generates the END OF FIELD signal, and causes a retace to the beginning of the next scanning field.

EOF indicates it is the last control word of a field (either even or odd)

4.0.2 HORIZONTAL CONTROL STORE

The horizontal control store defines a region in a scan line. Each horizontal control word in the horizontal control store defines a 16 bit region in a scan line. Current DDC chip design has a maximum capacity of up to 128 horizontal control words, and controls up to 128 words or 2048 pixels in a scan line. The address for the horizontal control store is ECØØ to EC7F. In a similar manner to the vertical control store, only the lower nibble of the data byte constitutes the control word.

The definition of the horizontal control word is as follows:

BITØ - HSYNC: a 1 in this bit will generate a 16 - pixel wide (4 MC clock period) horizontal sync within a scan line.

BIT1 - HBLANK: a 1 in this bit will blank out a 16 - pixel wide region within a scan line.

BIT2 - HPIC: a 1 in this bit will define a picture word within a scan line, while a Ødefine a border word.

BIT3 - VCLK: a 1 in this bit will generate a vertical clock pulse (4 MC Period)

There should be a total of exactly 3 VCLK's programmed in the horizontal control store. Labeled VCLK #2, VCLK #3 and VCLK

#1. See Fig. 4.1 and Fig. 4.2 for the programming example of horizontal control store.

VCLK #2 and VCLK #3 define the transition edge of the VSYNC signal, while VCLK #1 defines the last control word of the horizontal control store. VCLK #1 also signals a vertical control store fetch in the next cycle. The VCLK's should never be programmed in consecutive words. (In the gate array version VCLK#1 is the second last control word instead of the last control word)

4.0.3 DISPLAY CONTROL REGISTER

The address for the Display Control register inside the DDC is EC8Ø. It is a 8-bit Register. The representation of its corresponding functions are as follows:

BITØ - NINTL: A 1 in this bit sets the display is in non-interlace mode, and a Øsets it in interlace mode.

BIT1 - VIDEO: A 1 in this bit enables the display, while a Ø will blank out the display. During the reset time (i.e. NHRST = LOW), this bit is reset to zero, and the display monitor is blanked out. It is important to set this bit back to 1 to enable the video display before proceeding on with the normal operation.

BIT2 - UNUSED

BIT3 - DPIC: A 1 in this bit is the normal mode while a Ø forces the display to be an all border pattern.

BIT4-7 - BFØ:BF3 These 4 bits define the mixing function between the cursor and the bit map data.
See Fig. 4.Ø for the corresponding mixing function.

4.0.4 BORDER PATTERN LOW REGISTER

This 8 bit register defines the low border pattern. The address for writing into this register inside the DDC chip is EC81. The display for the whole screen is arranged in such a way that 2 lines of border pattern high alternates with 2 lines of border pattern low, with the border pattern high at the top of the screen.

4.0.5 BORDER PATTERN HIGH REGISTER

This 8 bit register defines the high border pattern. The address for this internal register is EC82.

4.0.6 CURSOR X HIGH REGISTER

This 8 bit register holds the cursor's location in the X-dimension. The address of this internal register is EC83.

4.0.7 CURSOR X LOW REGISTER

The lower nibble (bit 3 to bit Ø) of this register holds the cursor's bit-OFFSET Position from the location specifed by the cursor X High Register. For example, if bit3:Ø = 1111, it specifies that the cursor's location will be shifted right 15 bit in the X-dimension from the location specify by the address in the cursor X High Register.

Bit 7 of this Register also contains a control BIT called NCURSOR. A Ø in this bit enables the cursor while a 1 will disable the cursor from display. The address for this internal register is EC84.

4.0.8 CURSOR Y LOW REGISTER

This register holds the Lower 8 bits of the cursor's location in the Y-dimension. The address for this internal register is EC85.

4.0.9 CURSOR Y HIGH REGISTER

This register holds the 2 high bits of the cursor's location in the Y-dimension. Together with the lower 8 bits in the cursor Y Low Register, it forms the entire 10 bit address of the cursor's location in the Y-dimension. The address for this internal register is EC86.

4.0.10 QUADWORDS PER LINE REGISTER

Bit 5 to bit Ø of this Register holds the number of quadwords per scan line. This is used for different size display screens. The address for this internal register is EC88.

4.0.11 BIT MAP START ADDRESS LOW REGISTER

This internal register holds the low byte of the Bit Map data's starting address. The address for this internal register is EC89.

4.0.12 BIT MAP START ADDRESS HIGH REGISTER

This internal register holds the high byte of the bit map data's starting address. The address for this internal register is EC8A.

4.0.13 CURSOR BUFFER

This cursor buffer is 32 bytes deep in the DDC chip. The writing in of the cursor pattern is specified in the Intel byte format. See Fig. 4.3 for the format. The address for the cursor buffer is from ED00 to ED1F.

4.0.14 SOFTWARE RESET

The software reset will reset the chip and align the display to the beginning of the first scan line. The address for the software reset is ED6Ø to ED7F.

4.1 DATA FORMAT FOR MEMORY DATA AND CURSOR DATA

Fig 4.3 shows both the memory bit-map data and the cursor data format. They are both specified in the Intel format.

4.2 PROGRAMMING THE CONTROL STORE

Fig. 4.1 and Fig 4.2 show two programming examples of the Control Store. One is for the 15 inch black and white display and the other is for the 19 inch B/W display. Notice in the horizontal control store, as mentioned before, there are exactly three VCLKs programmed, and that the VCLK #1 defines the last control word of the horizontal control store. For the vertical control store, EOF defines the last control word in both the interlace and the non-interlace cases. Each count in the horizontal control store represents a duration of 4 MC clock period. The HSYNC, for instance, in the horizontal control store is programmed a total of 10 counts which represents a 40 MC clock period.

DDC chip D.C. characteristics

All pins are T^2L compatible with the exception of MC input.

VIL = 0.8v	VIH = 2V
VOL = 0.4v	VOH = 2.4V

MC Input:

VIL = 0.8V	VIH = 4.0V

All output and I/O pins with the exception of HSYNC, VSYNC and VIDØ:3 can sink 3MA @ 0.4V and source 0.2MA @ 2.4V. The output signals HSYNC, VSYNC and VIDØ:3 can sink 2MA @ 0.4V and source 200uA @ 2.4V.

All input capacitance CI = 18pf.

All output and I/O pins with the exception of HSYNC, VSYNC and VIDØ:3 output pins can drive 40pf of external output capacitance.

HSYNC, VSYNC and VIDØ:3 output pins can drive 12pf of external output capacitance.

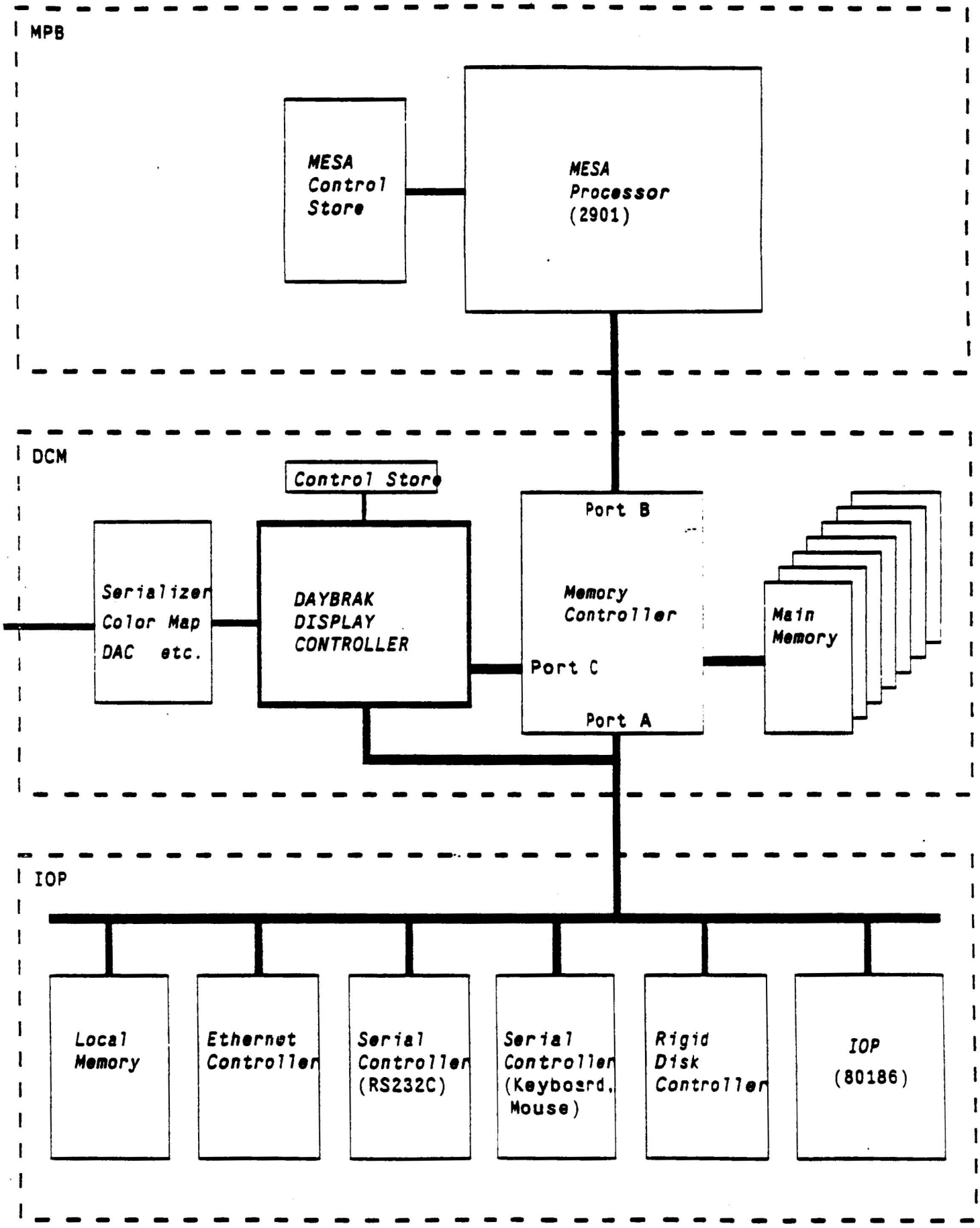
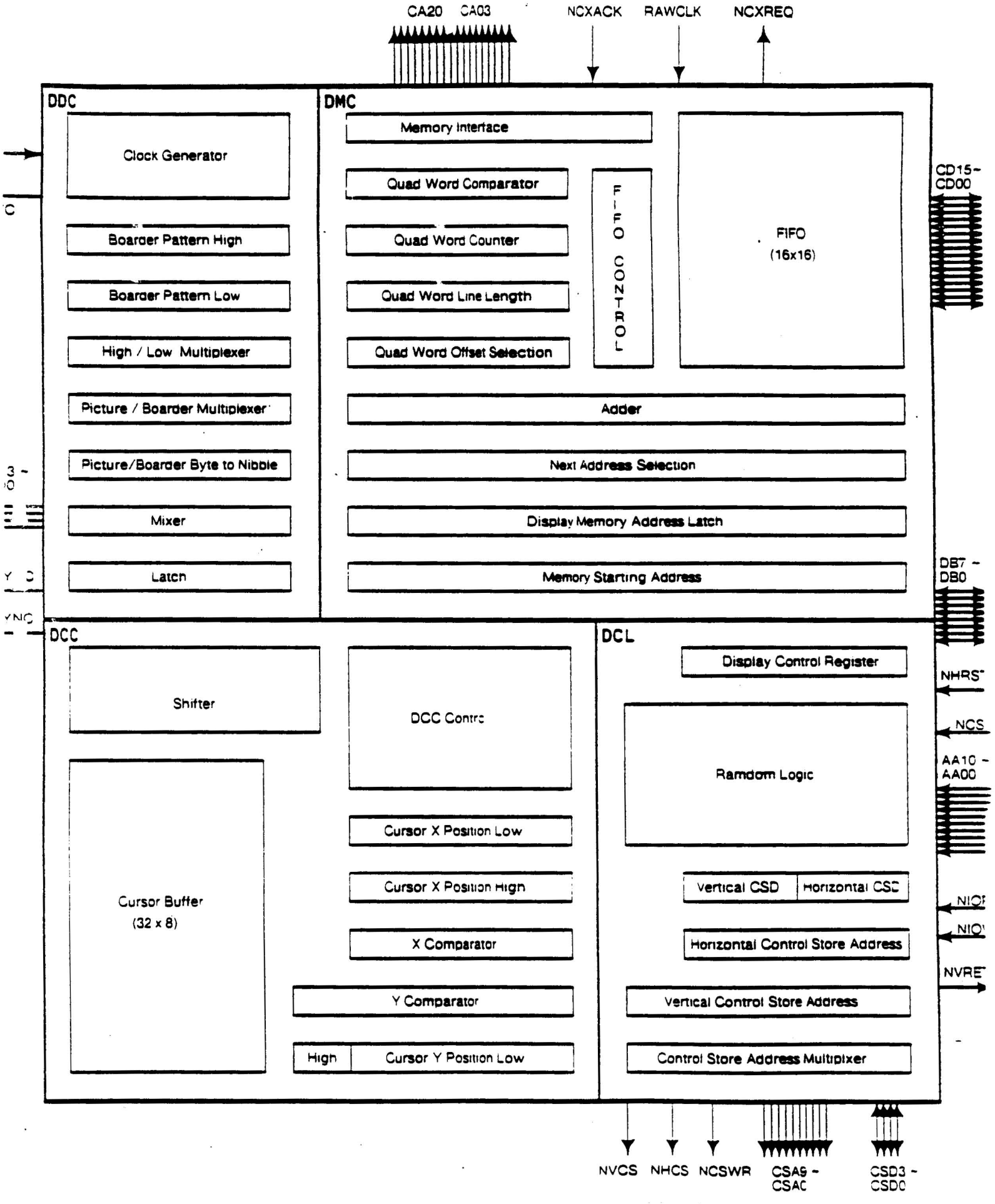

MPB
MESA Control Store
MESA Processor (2901)
DCM
Control Store
Serializer Color Map DAC etc.
DAYBRAK DISPLAY CONTROLLER
Port B
Memory Controller
Port C
Port A
Main Memory
IOP
Local Memory
Ethernet Controller
Serial Controller (RS232C)
Serial Controller (Keyboard, Mouse)
Rigid Disk Controller
IOP (80186)

FIGURE 1.0


CA20 CA03
NCXACK
RAWCLK
NCXREQ
DDC
Clock Generator
Boarder Pattern High
Boarder Pattern Low
High / Low Multiplexer
Picture / Boarder Multiplexer
Picture/Boarder Byte to Nibble
Mixer
Latch
DMC
Memory Interface
Quad Word Comparator
Quad Word Counter
Quad Word Line Length
Quad Word Offset Selection
FIFO CONTROL
FIFO
(16x16)
Adder
Next Address Selection
Display Memory Address Latch
Memory Starting Address
CD15 - CD00
DB7 - DB0
DCC
Shifter
DCC Contrc
Cursor Buffer
(32 x 8)
Cursor X Position Low
Cursor X Position High
X Comparator
Y Comparator
High
Cursor Y Position Low
DCL
Display Control Register
Ramdom Logic
Vertical CSD
Horizontal CSC
Horizontal Control Store Address
Vertical Control Store Address
Control Store Address Multiplxer
NHRS
NCS
AA10 - AA00
NVRE
NVCS
NHCS
NCSWR
CSA9 - CSA0
CSD3 - CSD0

SYSTEM INTERFACE PORT TIMING REQUIREMENT

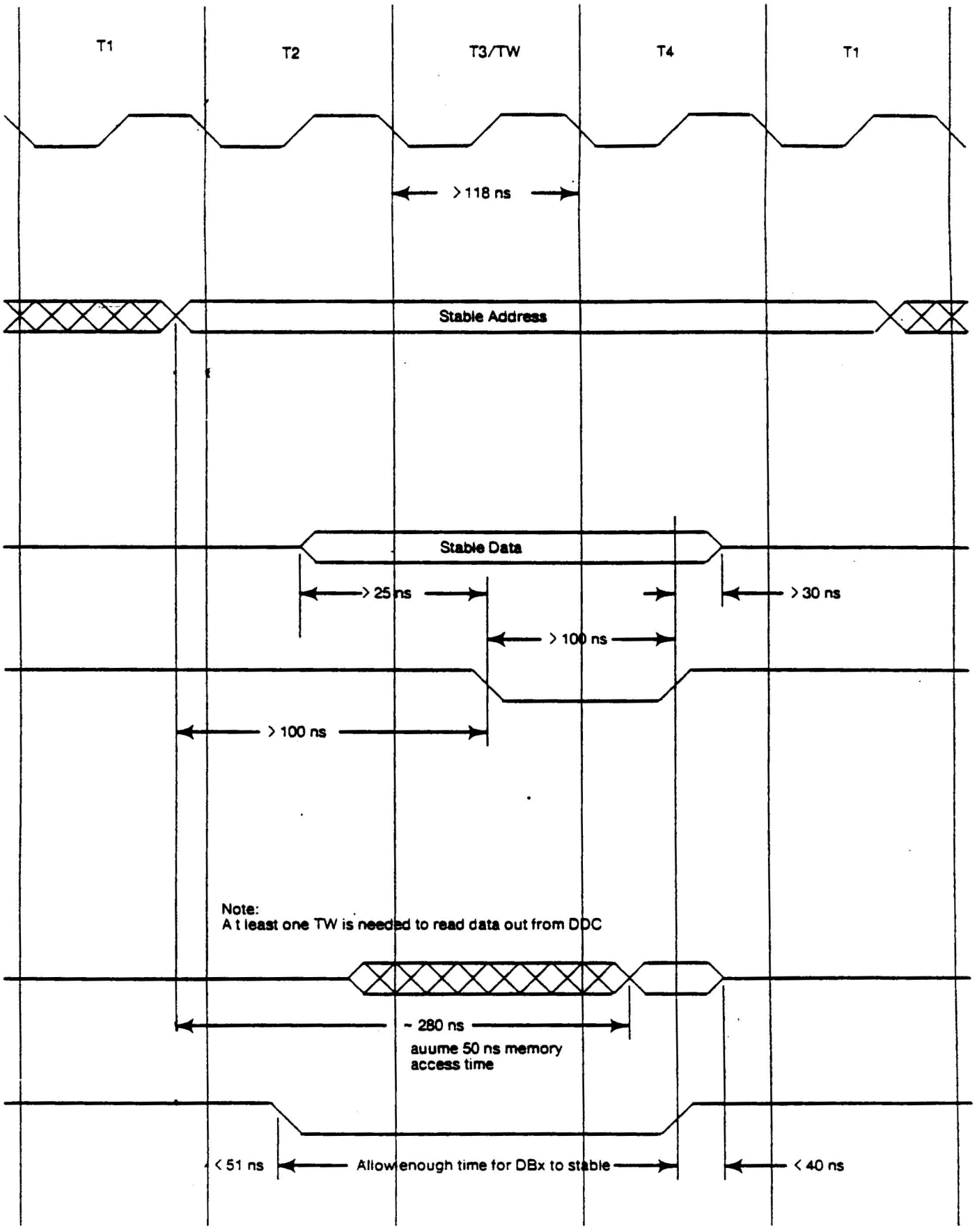


FIGURE 2.0

DIRECT READ/WRITE OF CONTROL STORE THROUGH SYSTEM INTERFACE PORT

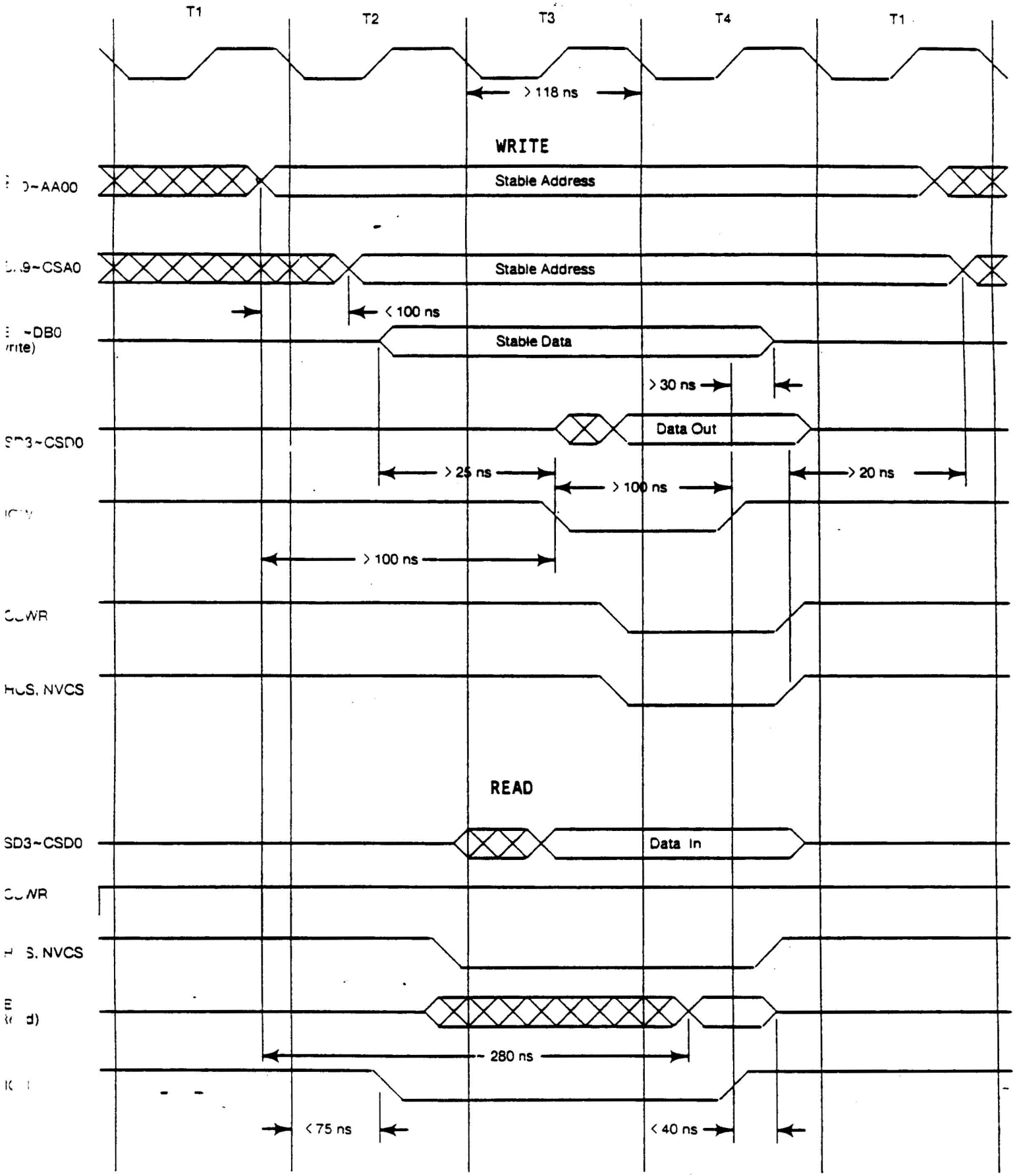


FIGURE 2.1

[DDCCSDTiming1.sil 4/3/85]

DDC READ OF CONTROL STORE DURING NORMAL OPERATION

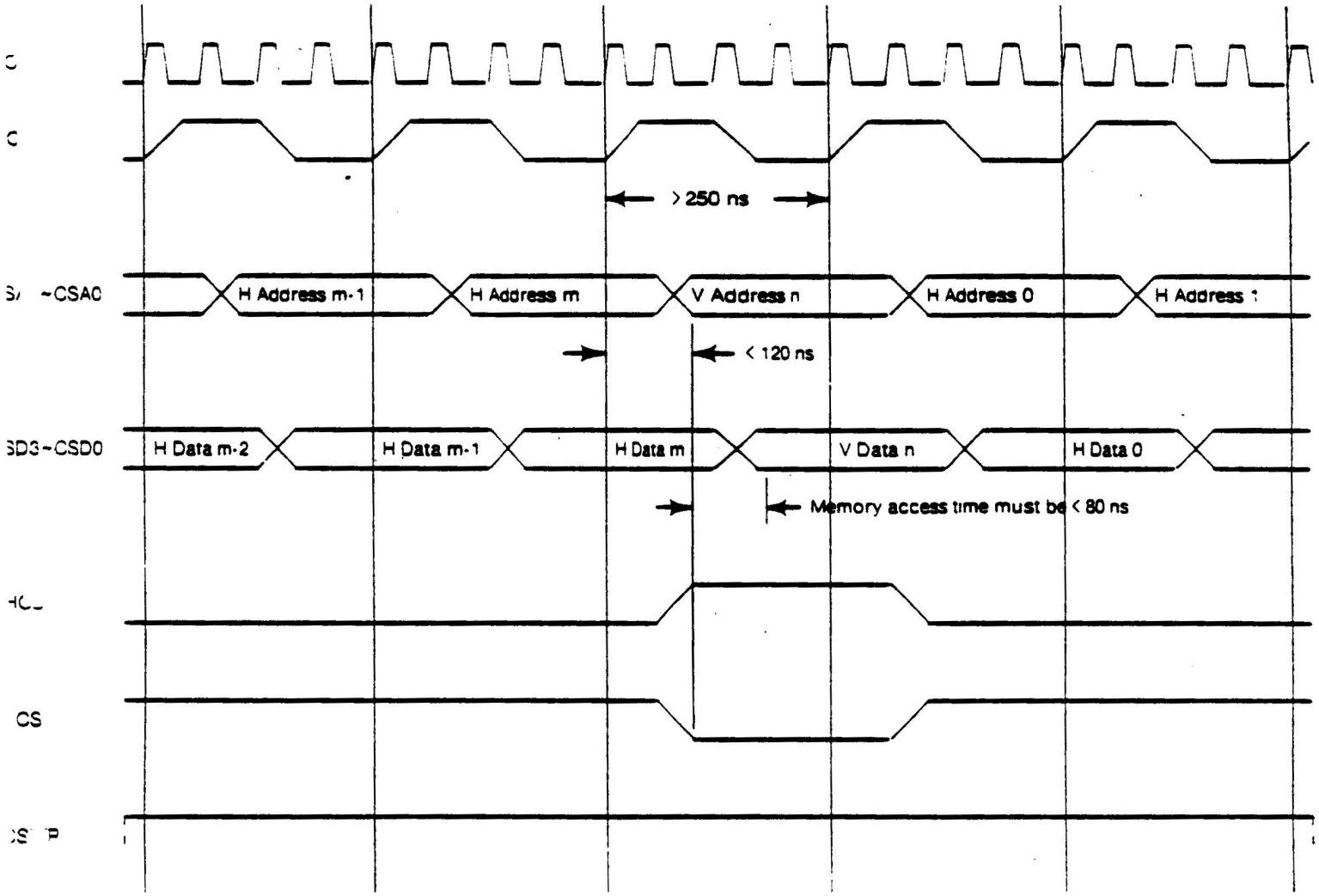
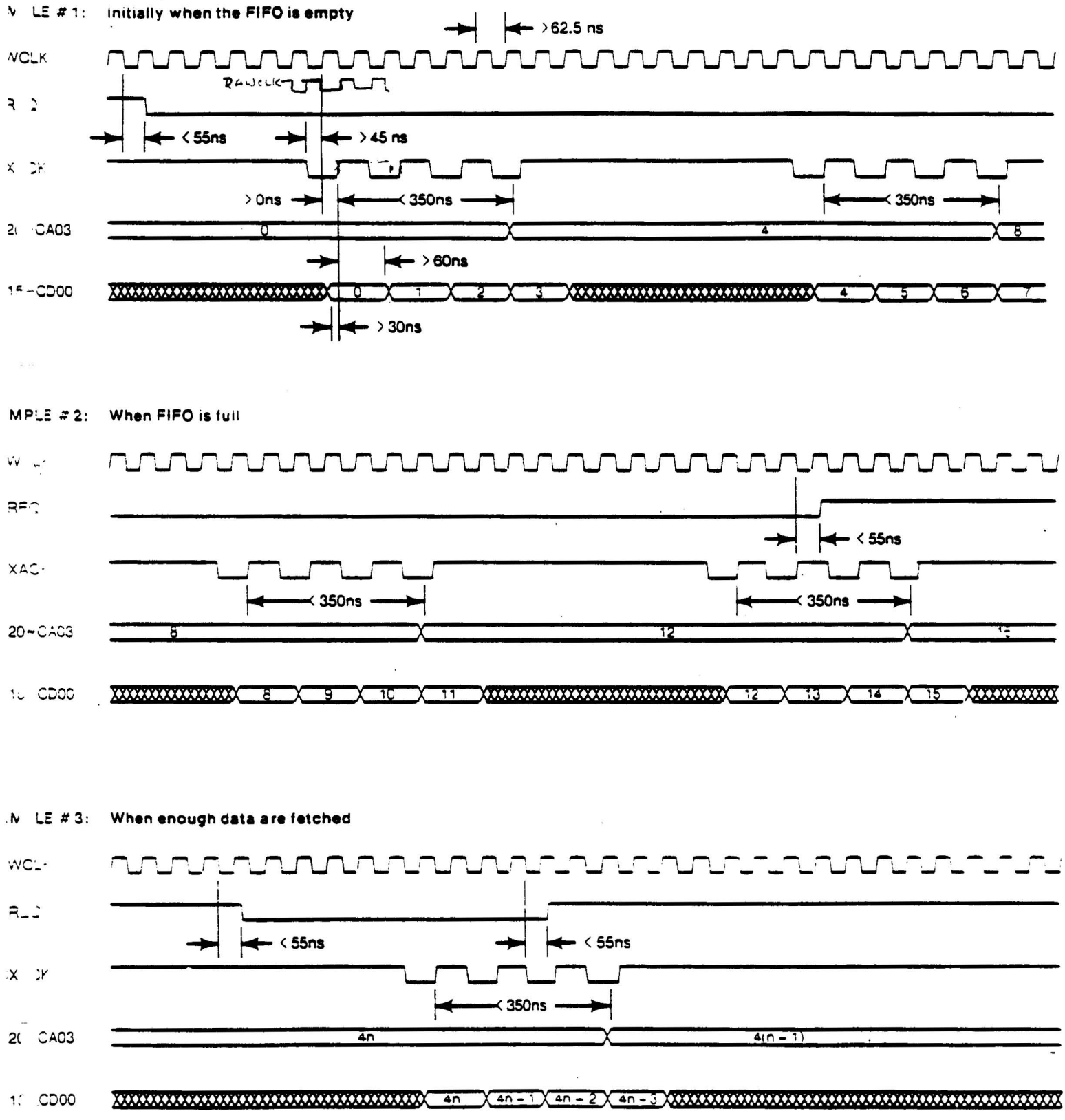


FIGURE 2.2

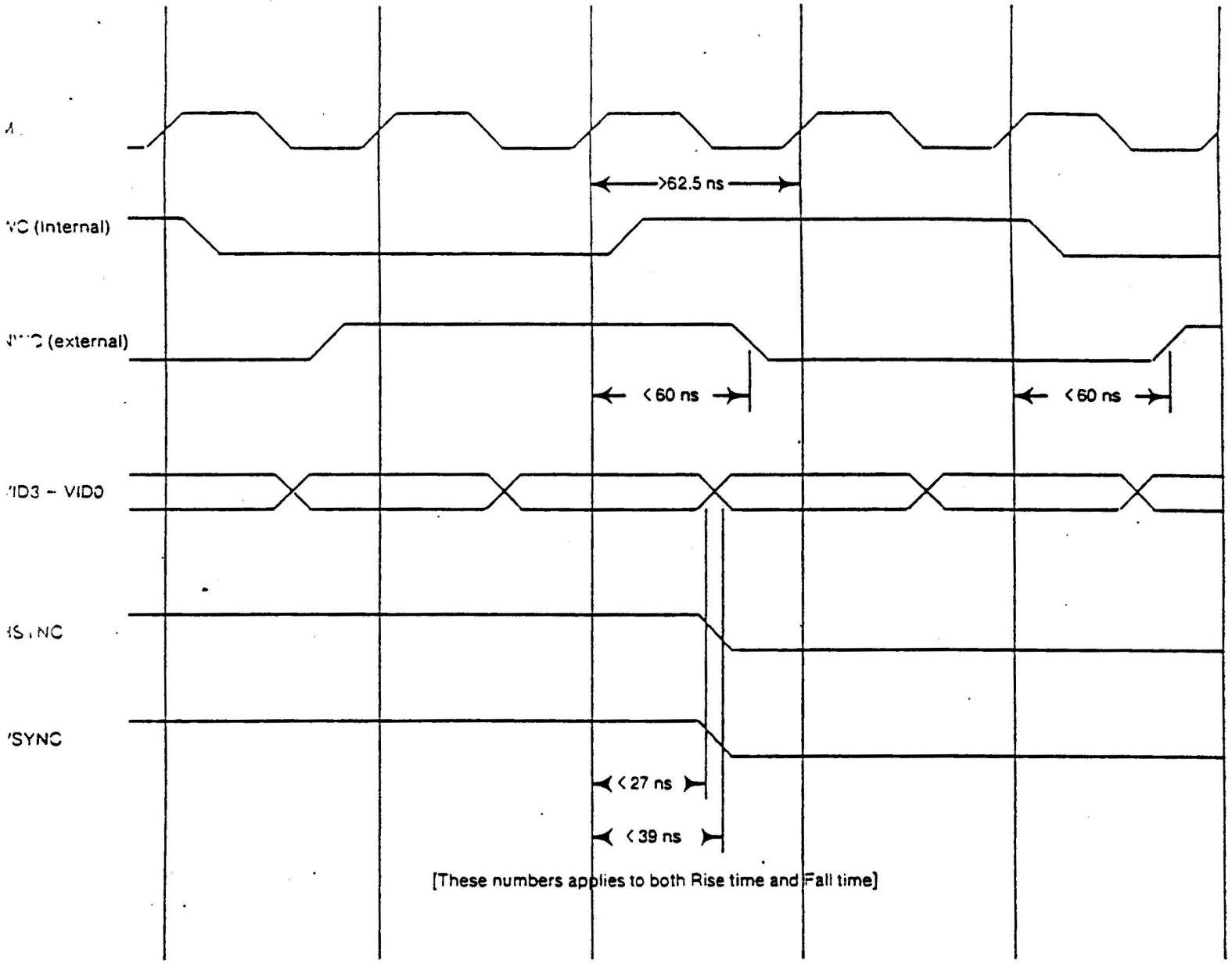
DDC MEMORY INTERFACE TIMING



Refresh Cycle are Shown here

FIGURE 2.3

DDC VIDEO OUTPUT TIMING



[These numbers applies to both Rise time and Fall time]

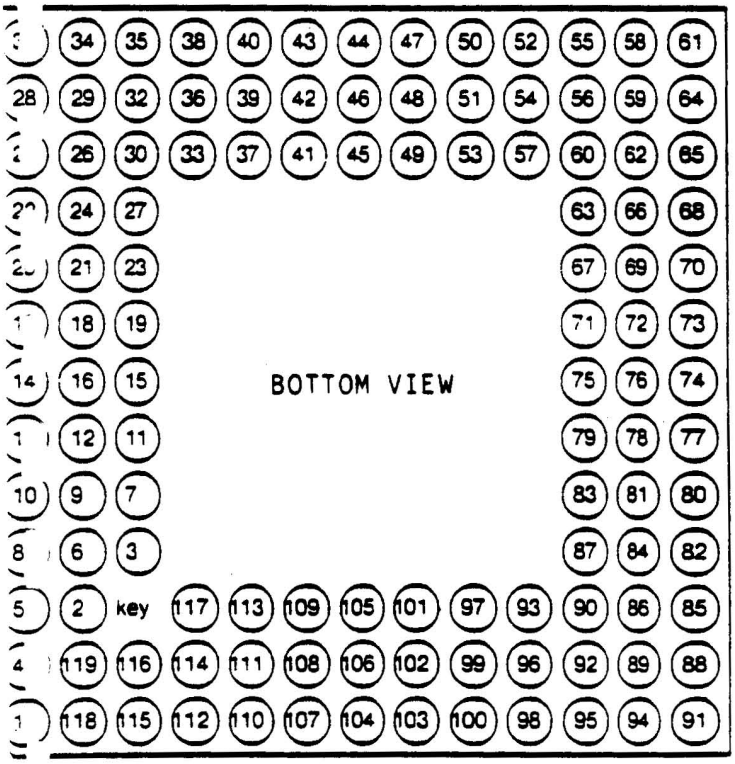
Maximum rise time or Fall time is 12 ns

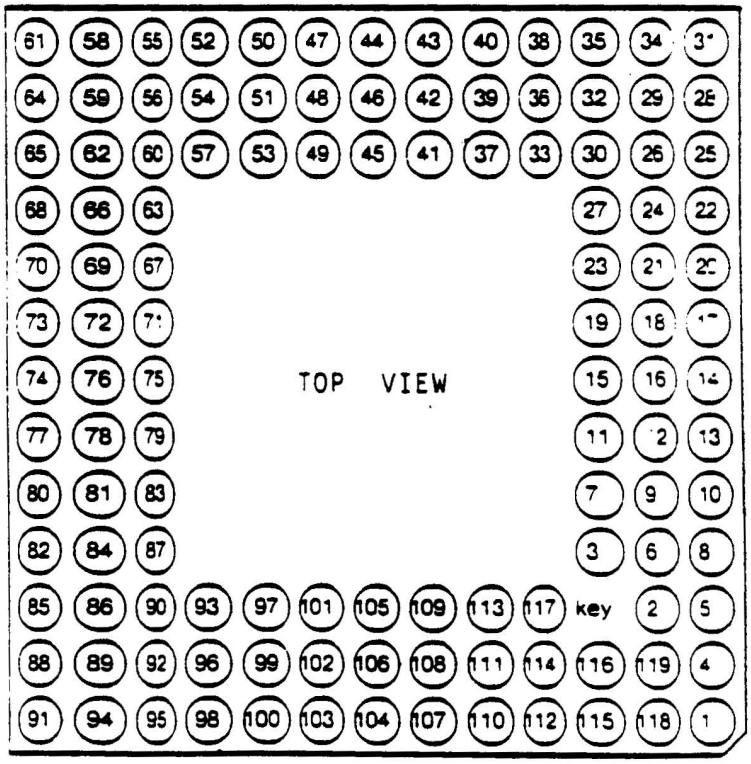
Rise time is mesured from o.8V to 2.0V

Fall time is mesured from 2.0V to 0.8V

DISPLAY CONTROLLER PIN ASSIGNMENT

PIN #	SIGNAL NAME	TYPE	PIN #	SIGNAL NAME	TYPE	PIN #	SIGNAL NAME	TYPE	PIN #	SIGNAL NAME	TYPE
			31			61			91		
2			32			62			92		
			33			63			93		
			34			64			94		
5	NCXACK	I	35	NWC	O	65	CSD2	I/O	95	DB2	I/O
	RAWCLK	I	36	MC	I	66	CSD1	I/O	96	DB3	I/O
	NCREQ	O	37	HSYNC	O	67	CSD0	I/O	97	DB4	I/O
8	CA03	O	38	VSYNC	O	68	NVRET	O	98	DB5	I/O
9	CA04	O	39	VID0	O	69	NIOR	I	99	DB6	I/O
0	CA05	O	40	VID1	O	70	NIOW	I	100	DB7	I/O
11	CA06	O	41	VID2	O	71	AA00	I	101	CD15	I
12	CA07	O	42	VID3	O	72	AA01	I	102	CD14	I
3	CA08	O	43	NCSWR	O	73	AA02	I	103	CD13	I
14	CA09	O	44	NVCS	O	74	AA03	I	104	CD12	I
15	VDD	I	45	NHCS	O	75	AA04	I	105	CD11	I
6	CA10	O	46	CSA9	O	76	GND	I	106	CD10	I
7	CA11	O	47	CSA8	O	77	AA05	I	107	CD09	I
18	CA12	O	48	CSA7	O	78	AA06	I	108	CD08	I
9	CA13	O	49	CSA6	O	79	AA07	I	109	CD07	I
0	CA14	O	50	CSA5	O	80	AA08	I	110	CD06	I
21	CA15	O	51	CSA4	O	81	AA09	I	111	CD05	I
2	CA16	O	52	CSA3	O	82	AA10	I	112	CD04	I
3	CA17	O	53	CSA2	O	83	NCS	I	113	CD03	I
24	CA18	O	54	CSA1	O	84	NHRST	I	114	CD02	I
5	CA19	O	55	CSA0	O	85	DB0	I/O	115	CD01	I
6	CA20	O	56	CSD3	I/O	86	DB1	I/O	116	CD00	I
27			57			87			117		
28			58			88			118		
9			59			89			119		
30			60			90			key		





DDC CONTROL WORDS ADDRESS AND FORMAT

			bit 7							bit 0
tical Control Store	R/W	E800 ~ EBFF					EOF	VPIC	VBLANK	VSYNC
izontal Control Store	R/W	EC00 ~ EC7F					VCLK	HPIC	HBLANK	HSYNC
y Control Register	W	EC80	BF3	BF2	BF1	BF0	DPIC		VIDEO	NINTL
r Pattern Low	W	EC81	Border Pattern Low							
r Pattern High	W	EC82	Border Pattern High							
X High	W	EC83	Cursor X High							
sor X Low	W	EC84	NCURSOR				Cursor X Low			
sor Y Low	W	EC85	Cursor Y Low							
Y High	W	EC86							Cursor Y Low	
ords Per Line	W	EC88					Quadwords Per Line			
Start Address Low	W	EC89	CA12	CA11	CA10	CA09	CA08	CA07	CA06	CA05
Start Address High	W	EC8A	CA20	CA19	CA18	CA17	CA16	CA15	CA14	CA13
sor Buffer	R/W	ED00 ~ ED1F	Cursor Byte							
ware Reset		ED60 ~ ED7F								

~ BF0 Mixing Function
= End Of Field
K Blank Word
C 1 = Picture Word 0 = Border Word
Horizontal Sync
URSOR 1 = Disable Cursor 0 = Enable Cursor
T 1 = Non-Interlace 0 = Interlace
A..K Blank Line
K Vertical Clock
E Enable Bitmap display
C 1 = Picture Line 0 = Border Line
Vertical Sync

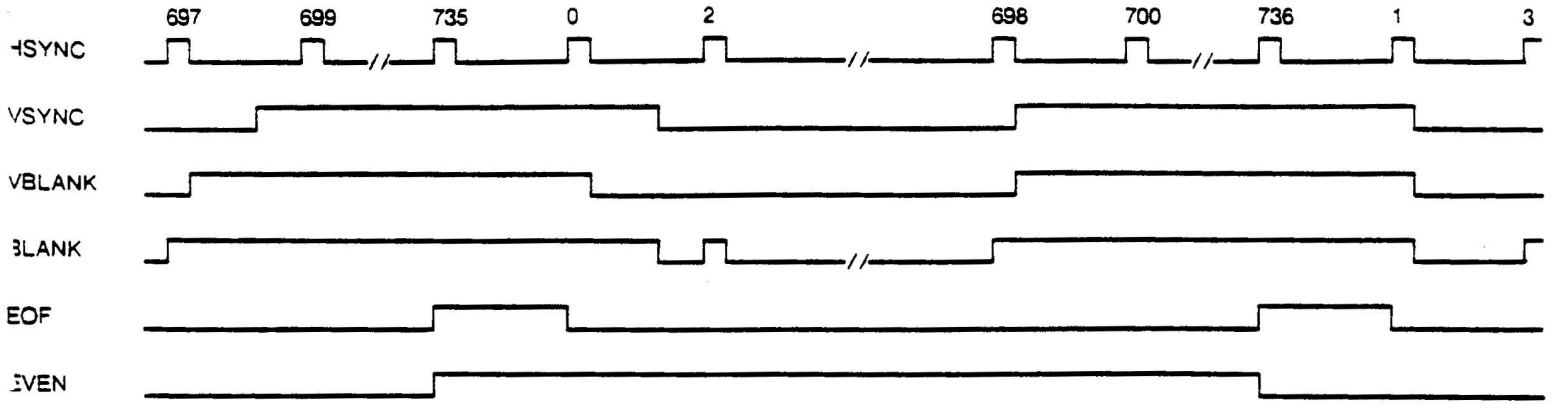
Mixing Function

F	RESULT	BG
0	0	1
1	V' • C'	0
2	V' • C	1
3	V'	0
4	V • C'	0
5	C'	1
6	V ⊞ C	0
7	V' + C'	1

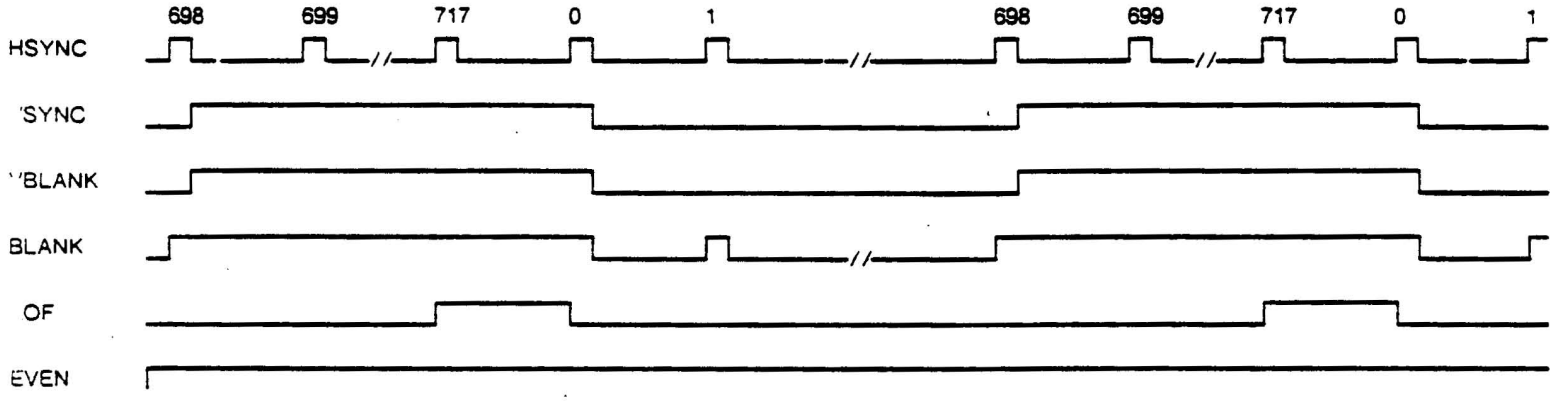
F	RESULT	BG
8	V • C	1
9	V' ⊞ C	0
A	C	0
B	V' + C	0
C	V	0
D	V + C'	1
E	V + C	0
F	1	1

F BF3 ~ BF0
BG Cursor Background
V Bitmap
C Cursor
• AND
+ OR
⊞ Exclusive OR

15 INCH DISPLAY WITH INTERLACE



15 INCH DISPLAY WITHOUT INTERLACE



EXAMPLE:

orizontal Control Store

Address (D)	Code (H)	Count (D)	Comment
0~8	3	9	HSync, HBlank
	B	1	HSync, HBlank, VClk # 2
10~11	0	2	Border
12~43	4	32	Picture
44	C	1	Picture, VClk # 3
45~63	4	19	Picture
64~65	0	2	Border
66~67	2	2	HBlank, Border
68	A	1	HBlank, Border, VCLK # 1

Vertical Control Store

Interlace

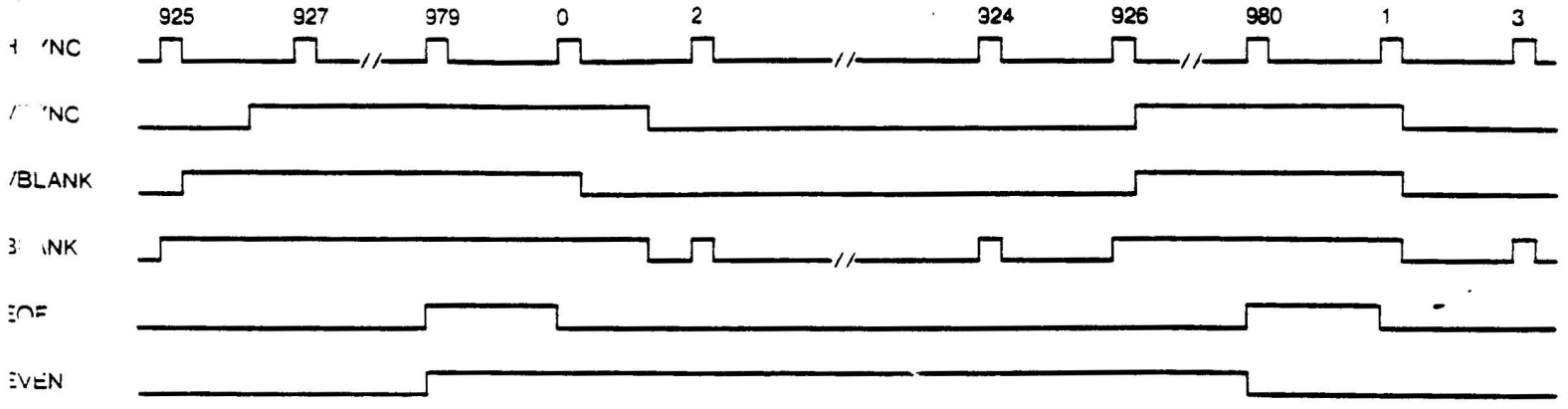
Address (D)	Code (H)	Count (D)	Comment
0~31	0	32	Top Border
32~664	4	633	Bit Map
665~696	0	32	Bottom Border
697~734	3	38	Vsync, VBlank
735~736	B	2	Vsync, VBlank, EOF

Non-Interlace

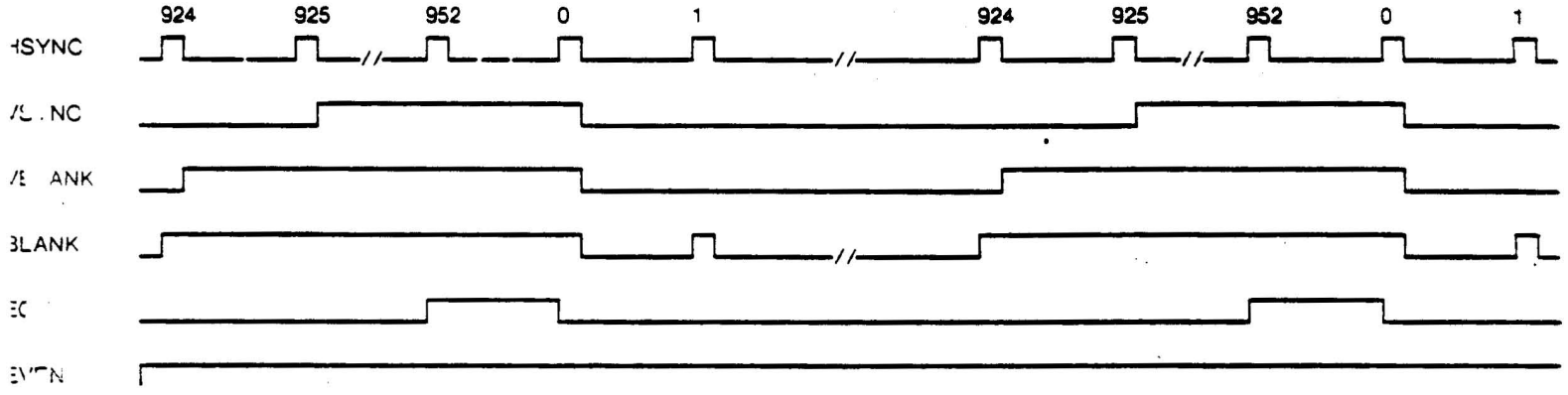
Address (D)	Code (H)	Count (D)	Comment
0~31	0	32	Top Border
32~665	4	634	Bit Map
666~697	0	32	Bottom Border
698~716	3	19	Vsync, VBlank
717	B	1	Vsync, VBlank, EO

FIGURE 4.1

19 INCH DISPLAY WITH INTERLACE



19 INCH DISPLAY WITHOUT INTERLACE



EXAMPLE:

Horizontal Control Store

Address (D)	Code (H)	Count (D)	Comment
0-14	3	15	HSync, HBlank
15	B	1	HSync, HBlank, VClk # 2
16-17	0	2	Border
18-64	4	47	Picture
65	C	1	Picture, VClk # 3
66-89	4	24	Picture
90-91	0	2	Border
92	2	1	HBlank, Border
93	A	1	HBlank, Border, VCLK # 1

Vertical Control Store

Interlace

Address (D)	Code (H)	Count (D)	Comment
0-31	0	32	Top Border
32-892	4	861	Bit Map
893-924	0	32	Bottom Border
925-978	3	54	Vsync, VBlank
979-980	B	2	Vsync, VBlank, EOF

Non-Interlace

Address (D)	Code (H)	Count (D)	Comment
0-31	0	32	Top Border
32-891	4	860	Bit Map
892-923	0	32	Bottom Border
924	2	1	VBlank, Border
925-951	3	27	Vsync, VBlank
952	B	1	Vsync, VBlank, EOF

FIGURE 4.2