P-50

OPERATION & MAINTENANCE PROGRAMS

HAGAN/CSD
TRAINING DEPARTMENT

Westinghouse Electric Corporation

TABLE OF CONTENTS

BOOTSTRAP (S3A)

I. Purpose

To load the binary loader into core.

II. Description of Operation

A. Place the tape "BINARY LOADER, BOOTSTRAP FORMAT" under the reader; turn the reader on.

1. When using the high speed reader, place the ON/OFF switch in the ON position.

2. When using the ASR set, the turn-on procedure is as follows:

a. Set ASR switch to OFF position.

b. Put machine in WRITE mode; depress the Master Clear button.

c. Using the probe, load the S-Register with the location.

d. Using the probe, load the X-Register with the contents of the location; depress the Start button.

e. Repeat c and d until all three words below have been entered:

Location	Contents
00000_8	00101_8
00101_8	37740_8
00102_8	$340**_8$

The two asterisks above denote the output channel number of the ASR set.

f. Put machine in INSTRUCTION STEP mode; depress the Master Clear and Start buttons.

B. Load the bootstrap manually (1); or use the bootstrap card (2).

1. Manual Load

a. Put machine in WRITE mode; depress the Master Clear button.

b. Using the probe, load the S-Register with the location.

c. Using the probe, load the X-Register with the contents of the location; depress the Start button.

d. Repeat b and c until all the words on the program listing (locations $0-27_8$) have been entered.

2. Bootstrap Card Load

   a. Connect the bootstrap card to the proper main frame plug.

   b. Put machine in WRITE mode; depress the Master Clear button.

   c. Using the probe, carefully trace the path on the bootstrap card crossing all exposed conductors in sequence.

   d. Remove the bootstrap card from the main frame p ug.

C. Verify that location 25_8 of the bootstrap program contains the proper input command to reference the selected reader.

D. Put machine in RUN mode; depress the Master Clear and Start buttons.

III. Run Time

In less than one minute, with lockout set, the bootstrap program will read in the binary loader and transfer to its starting location.

IV. Storage

Number of locations used: 27_8 ($1-27_8$).

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 512632

```
                        BOOTSTRAP

                        PROGRAM LIBRARY
                        PROGRAM NO.   P-50  53A


WIRED BOOTSTRAP FOR THE P-50 SERIES COMPUTER


A. OPERATING INSTRUCTIONS:
 1. CONNECT THE BOOTSTRAP CARD TO PROPER PLUG ON MAIN FRAME.

 2. VERIFY THAT THE READER AND LOCATION 25 (OCTAL) OF THE
BOOTSTRAP PROGRAM WILL REFER TO THE SAME CHANNEL.

 3. SELECT WRITE MODE AND MASTER CLEAR.

 4. USING A GROUNDED PROBE, CAREFULLY TRACE PATH ON BOOT-
STRAP CARD, CROSSING ALL EXPOSED CONDUCTORS IN SEQUENCE.
(THE BOOTSTRAP ALSO MAY BE LOADED MANUALLY.)

 5. REMOVE BOOTSTRAP CARD FROM MAIN FRAME PLUG.

 6. PLACE THE TAPE OF THE BINARY LOADER, BOOTSTRAP FORMAT,
IN READER AND TURN READER ON.  (IF THE ASR READER IS USED,
PLACE SWITCH ON LINE.  IF THE ASR SET IS NOT TURNED ON,
EXECUTE AN OUTPUT INSTRUCTION TO THE ASR SET WHILE IN SINGLE
STEP WITH THE ACCUMULATOR CONTAINING THE TURN-ON CHR-37740.)

 7. SELECT RUN MODE, MASTER CLEAR, AND START.

 8. WITH LOCKOUT SET , THE BOOTSTRAP PROGRAM WILL READ IN
THE BINARY LOADER AND TRANSFER TO THE FIRST LOCATION OF IT.

 9. FOR THE REMAINDER OF THE START UP PROCEDURE, SEE THE
BOOTSTRAPPED BINARY LOADER DESCRIPTION.
```

EJE

B. BOOTSTRAP FORMAT:

FIRST WORD OF THE TAPE IS THE LAST LOCATION PLUS ONE OF THE PROGRAM.

THE FOLLOWING WORDS ON THE TAPE ARE STORED IN DECENDING ORDER.

EACH WORD IS COMPOSED OF TWO SEVEN-BIT CHARACTERS IN REVERSE ORDER.

THE FIRST CHARACTER, WHICH IS THE LOW ORDER SEVEN BITS, IS DENOTED BY A PUNCH IN TAPE CHANNEL 8.

BLANK TAPE IS IGNORED WHEN LOOKING FOR FIRST CHARACTER.

THE SECOND CHARACTER, WHICH IS THE HIGH ORDER SEVEN BITS, IS DENOTED BY A NON-PUNCH IN TAPE CHANNEL 8.

IF A WORD CONTAINS TWO PUNCHES IN TAPE CHANNEL 8, CONTROL IS TRANSFERRED TO THE BEGINNING OF THE LOADED PROGRAM.

C. TIME DELAY

LOCKOUT AND A TIME DELAY REPLACE THE READER INTERRUPT.

THE TIME DELAY IS (3+3) * 4.5USEC * 6209 = .167SECONDS

THE SLOWEST READER IS ASSUMED TO BE FASTER THAN SIX CHARACTERS PER SECOND.

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 512632

```
103                                 EJE
104                                     WIRED BOOTSTRAP FOR THE P-50 SERIES COMPUTER
105
106
107                 00000           ORG PC                                                  S    (S)
110     00000       00020           OCT READC       READ A CHARACTER AND IGNORE.            00   00020
111     00001       00001   STORAG  OCT L               STORAGE INDEX, FIRST WORD HERE.     01   00001
112     00002  10 0 040     2HALF   ADD TEMP        COMBINE FIRST CHARACTER WITH FIRST.     02   10040
113     00003  14 0 101     TIMCON  LSH ACC             PLACE BITS IN PROPER POSITION,      03   14101
114     00004  37 1 001             STL STORAG,I    STORE COMPLETE WORD IN CORE,            04   37401
115     00005  01 0 001             DCR STORAG          DECREASE STORAGE INDEX BY ONE.      05   01001
116     00006  36 0 020     1HALF   RJP READC       GET FIRST CHARACTER OF WORD,            06   36020
117     00007  20 0 005             ZJP L-1             IGNORE BLANK FIRST CHARACTERS,      07   20005
120     00010  02 0 101             CMB ACC         CLEAR TAPE CHANNEL 8.                   10   02101
121     00011  14 0 101             LSH ACC             SHIFT FIRST CHARACTER TO LOW END.   11   14101
122     00012  14 0 027             LSH SHIFT7      THE SHIFT IS PERFORMED SEVEN TIMES.     12   14027
123     00013  27 0 010             PJP L-2             IS THE SHIFTING OPERATION DONE?     13   27010
124     00014  37 0 040             STL TEMP        STORE SHIFTED FIRST CHARACTER,          14   37040
125     00015  36 0 020             RJP READC           GET SECOND CHARACTER OF WORD.       15   36020
126     00016  21 0 001             EJP 2HALF       IF BIT 13(TAPE CH.8) OFF, FORM WORD.    16   21001
127     00017  24 1 001             JMP STORAG,I        IF ON, TRANSFER TO PROGRAM.         17   24401
130     00020      00005   READC   ...     1HALF-1 FIRST TIME, RETURN TO GET FIRST CHR.    20   00005
131     00021  01 0 100             DCR TIMDLY          DECREMENT TIME DELAY.               21   01100
132     00022  27 0 020             PJP L-1         DELAY UNTIL TIME DELAY IS NEGATIVE,     22   27020
133     00023  32 0 003             ENL TIMCON          TIMCON = (3+3)*4.5*6209 = .167SEC.  23   32003
134     00024  37 0 100             STL TIMDLY      RESET DELAY WITH TIME DELAY CONSTANT.   24   37100
135     00025  30 0 000             INT **              INPUT ONE EIGHT-BIT CHAR.(6-13).    25   300** 40 A
136     00026  24 1 020             RTN             RETURN WITH CHARACTER INPUTED.          26   24420
137     00027      20100   SHIFT7  OCT 20100           FLAG FOR SHIFTING SEVEN TIMES.      27   20100
140                00040   TEMP    EQU 32          TEMPORARY STORAGE FOR FIRST CHR.
141                00100   TIMDLY  EQU 64              TIME DELAY, AUTOMATICALLY RESET.
142                00000           END
```

DATE 4/27/65, TIME 2/50/39 P.M.

PROJECT NO. 5-0053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512632

STARTED 4/27/65, 2/50/00 P.M.
COMPLETED 4/27/65, 2/50/38 P.M.
NUMBER OF INPUT RECORDS 98.
NUMBER OF OUTPUT RECORDS 98.
NUMBER OF BINARY RECORDS 27.

BOOTSTRAPPED BINARY LOADER (S4A)

I. Purpose

To load P-50 binary tapes into core with both latitudinal (parity) and longitudinal (checksum) error checking.

II. Description of Operation

A. Read in the "Binary Loader, Bootstrap Format" paper tape using the bootstrap. (See Bootstrap Description for details.)

B. Enter the following parameters if necessary:

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat 2 and 3 until all the desired parameters have been entered.

Location	Preset	Description
X7750	300XX	Input command to access same reader as used by bootstrap. (XX denotes reader channel.)
X7766	00007	Standard High Speed Reader Interrupt Location.
X7767	00010	Standard ASR Reader Interrupt Location.
X7771	X7601	Address, minus one, where control is transferred when a stop code is read.

(X is 0, 1, 2 or 3 depending on which bay the binary loader is in.)

C. Read in the desired binary tape using the bootstrapped binary loader.

1. Place the binary tape under the paper tape reader. If the ASR reader is used, the binary loader assumes that it has already been turned on by the computer. (See turn on procedure in Bootstrap description.)

2. Place machine in RUN mode.

3. Depress the Master Clear button.

4. Depress the Start button.

5. If no errors are detected, the tape will be input up to and including the stop or transfer code.

D. Normal Completion

1. If the tape contains a stop code at the end of the tape, the computer will either stop with the S-Register (bits 0-7) set to 202_8 or will transfer

automatically to the TØP program in the P-50 Executives, depending on whether location X7771 was preset to X7601 or 401.

2. If the tape contains a transfer code at the end of the tape, the computer will transfer control to the specified transfer location.

E. Error Stop

If the error checking procedure finds an error, the computer wi stop with the S-Register (bits 0-7) set to either of the following:

1. S-Register (0-7) = 4: Parity Error

2. S-Register (0-7) = 5: Checksum Error

To reread the binary tape, replace it under the reader at the beginning of the tape and depress the Start button.

F. Using the Binary Loader after a Time Lapse

To read in binary tapes after other programs have been executed, the following procedure must be followed. (This assumes that the bootstrapped binary loader remains in core.)

1. Put machine in WRITE mode; depress Master Clear button.

2. Using the probe, load the X-Register with the starting location of the bootstrapped binary loader (X7602, where X = 0, 1, 2, or 3 depending on which bay the loader is in); depress the Start button.

3. Execute Step C of this section.

III. Program Comments

A. When the bootstrap program transfers control to the binary loader, the input command used by the bootstrap is stored in location X7750, thus the loader is preset to use the same reader as the bootstrap.

B. The loader assumes that the reader interrupt location is either 7_8 or 10_8.

C. The input of a stop code on the binary tape will either result in a stop with the P-Register set to X7602 or a transfer to the executives, depending on how location X7771 is preset.

D. The above three items may be changed as indicated in Section II. B.

E. The bootstrapped binary loader does not load any interrupt locations until it is completely finished so that it cannot be interrupted during the loading process. Because of this precaution, the loader will not function properly when an attempt is made to load into core locations 7475_8 to 7777_8 or when binary tapes are loaded consecutively in bay zero. (This is no restriction since the programmer's console will perform these functions once the executives are entered. Also, a binary loader in the binary form may be entered in this manner.)

F. The bootstrapped binary loader will not load correctly into its particular area of core ($X7600_8 - X7777_8$), where X = 0, 1, 2, or 3 depending on which bay the loader is in.

G. A transfer to location zero or location 37777_8 is interpreted as a stop code. Attempted storage into location zero is ignored.

H. Tapes containing the bootstrapped binary loader in the bootstrap format are available from the Program Library for all four bays of core; tapes containing the binary loader in the binary form are also available for all four bays of core.

IV. Storage

Number of locations used: 200_8 (X7600-X7777).

V. Run Time

The bootstrapped binary loader runs at the speed of the reader.

PROJECT NO, 530053 PROGRAMMER E.E. O,HARE TAPE NUMBER 512633

BOOTSTRAPPED BINARY LOADER

PROGRAM LIBRARY
PROGRAM NO. P-50 S4A

1. READ IN BINARY LOADER, BOOTSTRAP FORMAT, USING THE BOOTSTRAP PROGRAM (SEE BOOTSTRAP DESCRIPTION).

2. AFTER THE BOOTSTRAP PROGRAM TRANSFERS TO THE BINARY LOADER, THE BINARY LOADER WILL STOP WITH THE S-REGISTER (BITS 0-7) SET TO A (202).

3. PLACE BINARY TAPE TO BE LOADED IN SAME INPUT DEVICE AS USED BY THE BOOTSTRAP PROGRAM (THE FORMAT OF A BINARY TAPE IS DESCRIBED IN THE PROGRAMMER,S CONSOLE WRITEUP).

4. PLACE MACHINE IN RUN MODE, PUSH MASTER CLEAR BUTTON, AND THEN PUSH THE START BUTTON.

5. IF BINARY TAPE CONTAINS A STOP CODE AT THE END, THE PROGRAM WILL EITHER STOP WITH THE S-REGISTER (BITS 0-7) SET TO A (202) OR TRANSFER TO THE P-50 EXECUTIVES, DEPENDING ON HOW THE BINARY LOADER WAS PRESET.

IF BINARY TAPE CONTAINS A TRANSFER CODE AT THE END, THE PROGRAM WILL TRANSFER TO THAT LOCATION SPECIFIED BY THE TRANSFER CODE.

6. IF A PARITY ERROR (ODD PARITY CHECKING) OCCURS, THE PROGRAM WILL STOP WITH THE S-REGISTER(BITS 0-7) SET TO A (4).

IF A CHECKSUM ERROR (14 BIT SUM ON WORDS) OCCURS, THE PROGRAM WILL STOP WITH THE S-REGISTER(BITS 0-7) SET TO A (5).

TO RESTART ON EITHER OF THE ABOVE TWO ERRORS, DEPRESS MASTER CLEAR BUTTON AND THEN DEPRESS START BUTTON, AFTER REPOSITIONING TAPE IN INPUT DEVICE.

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512633

```
                                EJE
                                     7. TO RESTART, SET THE P-REGISTER TO X7602, WHERE (X)
                                   IS EITHER 0, 1, 2, OR 3 DEPENDING ON WHICH BAY OF CORE
                                   THE BINARY LOADER HAS BEEN ASSEMBLED FOR.

                          ******   N.B. *** THE BINARY LOADER USES THE SAME INPUT DEVICE AS THE
                          ******   BOOTSTRAP, ASSUMES THAT THE INPUT DEVICE'S INTERRUPT IS
                          ******   EITHER AT LOCATION SEVEN OR TEN (OCTAL), AND WILL NOT LOAD
                          ******   CORE LOCATIONS 7475 TO 7777 (OCTAL) PROPERLY.
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 512633

```
 61                                  EJE
 62                                      BOOTSTRAPPED BINARY LOADER FOR THE P-50 SERIES COMPUTER
 63
 64
 65                                  UNL
 66                          A       HED THE FOLLOWING ARE PROGRAM PARAMETERS:
 67                  00000   BAY     EQU 0                   BAY OF CORE WHERE BINARY LOADER WILL BE
 70                  00000   STPND   EQU 0                   STOP INDEX: 0-STOP; 1-TRANSFER TO EXECS.
 71                  00007   HSRLO   EQU 7                   HIGH SPEED READER INTERRUPT LOCATION
 72                  00010   ASRLO   BEQU 10                 ASR SET READER INTERRUPT LOCATION
 73                  00025   RCHLO   BEQU 25                 INPUT DEVICE,S CHANNEL LOC. FROM BOOTSTRAP
 74
 75                  00402   STPEX   BEQU 402                STOP FOR EXECUTIVES (TOP ROUTINE)
 76                  07602   STPBL   BEQU BAY*10000+7602     STOP FOR BINARY LOADER
 77                                  RPT STPND
101                                  DLE STPND
102                 07602   STP     EQU STPBL               STOP IN BINARY LOADER (S-REGISTER = 7202)
103
104
105                 07600   BINLD   BORG BAY*10000+7600
106   07600  32 1 370                ENL RDCHL,I             GET CORRECT READER CHANNEL FROM BOOTSTRAP
107   07601  37 0 350                STL INCOM               STORE INPUT COMMAND IN BINARY LOADER
110   07602  00 0 202                STP L                   NORMAL STOP FOR BINARY LOADER: S-REG=7202
111
112   07603  32 0 365  /START        ENL ACC)                NORMAL START FOR BINARY LOADER
113   07604  37 0 375                STL COUNT
114   07605  32 0 364  /             BENL 23400)             STORE IGNORE INTERRUPTS (CLJ ,I = 23400)
115   07606  37 1 375                STL COUNT,I                IN ALL THE INTERRUPT LOCATIONS
116   07607  01 0 375                DCR COUNT
117   07610  27 0 205                PJP L-2
120
121   07611  23 0 211                CLJ L+1                 CLEAR INITIAL LOCKOUT
122   07612  32 0 363  /             ENL RDRTN-1)
123   07613  37 1 362  /             STL ACC+1               STORE READER INTERRUPT RETURN
124   07614  32 0 361  /             BENL 23400+ACC+1)       READER INTERRUPT COMMAND (CLJ ACC+1,I)
125   07615  37 1 366                STL HSRIL,I
126   07616  37 1 367                STL ASRIL,I             STORE IN READER INTERRUPT LOCATIONS
127   07617  36 0 347                RJP INPUT               IGNORE FIRST GARBAGE CHARACTER
```

```
130                                  EJE
131   07620  36 0 276    NBNBK     RJP IBNWD          GET FIRST WORD OF NEXT BINARY BLOCK
132   07621  05 0 376              EDR TORCS          CHECK FOR A TRANSFER OR STOP CODE
133   07622  21 0 223              EJP L+2
134   07623  22 0 250              SLJ STPTR          WORD IS A TRANSFER OR STOP CODE
135
136   07624  37 0 373              STL CKSUM          STORE AS FIRST WORD OF CHECKSUM
137   07625  10 0 360  ✓           ADD ACC+2)         MOVE ORIGIN ABOVE INTERRUPT LOCATIONS
140   07626  37 0 374              STL ORIGN          STORE CURRENT ORIGIN STATEMENT
141   07627  12 0 357  ✓          BAND 30000)
142   07630  20 0 232              ZJP NBNWD+1        ORIGIN STATEMENT IS IN BAY ZERO
143   07631  32 0 373              ENL CKSUM          ORIGIN NOT IN BAY ZERO; USE ACTUAL ORIGIN
144   07632  37 0 374    NBNWD     STL ORIGN          STORE CURRENT ORIGIN STATEMENT
145   07633  36 0 276              RJP IBNWD          GET CONTENTS OF CURRENT ORIGIN STATEMENT
146   07634  01 0 376              DCR TORCS
147   07635  21 0 236              EJP L+2
150   07636  37 1 374              STL ORIGN,I        WORD IS NOT A CHECKSUM; STORE CONTENTS
151   07637  10 0 373              ADD CKSUM
152   07640  37 0 373              STL CKSUM          PLACE WORD IN CHECKSUM AND STORE
153   07641  32 0 374              ENL ORIGN
154   07642  10 0 356  ✓           ADD 1)             INCREASE ORIGN BY ONE
155   07643  01 0 376              DCR TORCS
156   07644  21 0 231              EJP NBNWD          WORD IS NOT A CHECKSUM; GET NEXT WORD
157   07645  32 0 373              ENL CKSUM          WORD IS A CHECKSUM
160   07646  20 0 217              ZJP NBNBK          BINARY BUFFER CORRECT, PROCEED WITH NEXT
161   07647  00 0 005              STP 5              CHECKSUM ERROR; S-REGISTER SET TO A FIVE
162   07650  24 0 202              JMP START          RESTART BINARY LOADER
```

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512633

```
163                                EJE
164   07651   32 1 365   STPTR     ENL ACC              RESTORE ZERO DESIGNATOR
165   07652   20 0 254              ZJP L+3              TRANSFER CODE WAS A STOP CODE (+0 OR -0)
166   07653   11 0 356              SUB 1)               DECREMENT TRANSFER BY ONE
167   07654   24 0 255              JMP L+2              TRANSFER TO TRANSFER LOCATION
170   07655   32 0 371              ENL STOP             TRANSFER TO A  STOP OR P-50 EXECS.
171   07656   37 0 374              STL ORIGN            STORE TRANSFER
172
173   07657   32 0 360              ENL ACC+2)
174   07660   37 0 376              STL SCORE            SET SHIFTED CORE INDEX
175   07661   32 0 356              ENL 1)
176   07662   37 0 375              STL CORE             SET CORE INDEX
177   07663   32 0 376   CYCLE      ENL SCORE
200   07664   10 0 356              ADD 1)               INCREMENT SHIFTED CORE INDEX BY ONE
201   07665   37 0 376              STL SCORE            (NOTE:ONE CANNOT LOAD INTO 00000)
202   07666   32 1 376              ENL SCORE,I
203   07667   37 1 375              STL CORE,I           SHIFT CONTENTS OF CORE DOWN TO PROPER LOC.
204   07670   32 0 375              ENL CORE
205   07671   10 0 356              ADD 1)               INCREMENT CORE INDEX BY ONE
206   07672   37 0 375              STL CORE
207   07673   11 0 355   ✓        8SUB 7600-ACC-2)      MOVE BAY ZERO DOWN TO INTERRUPT LOCS.
210   07674   20 1 374              ZJP ORIGN,I          TERMINATE BINARY LOADER WITH LOCKOUT SET
211   07675   24 0 262              JMP CYCLE            SHIFT ALL WORD IN BAY ZERO DOWN
```

```
212                                EJE
213   07676      00000   IBNWD  ...
214   07677   05 0 354   J      EDR *0)          INPUT A BINARY WORD OF THREE CHARACTERS
215                               CLEAR OVERFLOW DESIGNATOR
216
217   07700   32 0 354           ENL *0)          THE FOLLOWING CONSTANT (00000) IS USED TO
220                               INITIALIZE THREE INDICATORS.  THEIR
221                               INITIALIZATION AND USE ARE EXPLAINED BELOW
222
223                               THE PARTY INDICATOR IS INITIALY SET TO
224   07701   37 0 375           STL PARTY        AN EVEN NUMBER.  IT COUNTS THE NUMBER
225                               OF BITS IN A CHARACTER AND THEN IT IS
226                               TESTED TO ASCERTAIN      IF THE
227                               CHARACTER HAD CORRECT ODD PARITY.
230
231                               THE 10R3F INDICATOR IS USED TO ASCERTAIN
232                               WHICH CHARACTER (1,2, OR 3) OF THE WORD
233                               IS BEING PROCESSED.  THE INDICATOR IS
234                               SET INITIALLY     TO 34 (OCTAL) AND IS
235                               SHIFTED WHEN THE THIRD CHARACTER IS BEING
236                               CHECKED.  THE INDICATOR IS TESTED BY
237                               USING THE DESIGNATORS AS SHOWN BELOW:
240
241   07702   06 0 372           SDR 10R3F          10R3F      E Z P O C
242                               INITIALLY: 1 1 1 0 0
243                               1ST SHIFT: 0 1 1 1 0
244                               2ND SHIFT: 0 0 1 1 1
245                               3RD SHIFT: 0 0 0 1 1
246
247                               IT IS THE FIRST CHARACTER WHEN THE 10R3F
250                               IS PLACED IN THE DESIGNATOR AND THE
251                               OVERFLOW DESIGNATOR IS NOT SET.  IT IS
252                               THE THIRD CHARACTER WHEN A CARRY IS
253                               PROPAGATED BY A RIGHT SHIFT ON THE 10R3F.
254
255                               THE TORCS INDICATOR INITIALLY SETS BITS 0
256   07703   06 0 376           SDR TORCS        AND 13 TO A ZERO AND BIT 4 TO AN ONE.
257                               IF A WORD IS A TRANSFER (OR STOP CODE),
260                               BIT 4 IS SET TO A ZERO.  IF A WORD IS A
                                  CHECKSUM, BIT 13 IS SET TO AN ONE.
```

PROJECT NO. 530053 PROGRAMMER E.E. O,HARE TAPE NUMBER 512633

```
261                                    EJE
262   07704   37 0 377   LOOP    STL WORD        SAVE PARTIAL WORD GENERATED THUS FAR
263   07705   36 0 347           RJP INPUT       INPUT ONE CHARACTER
264   07706   32 1 365           ENL ACC         RESET DESIGNATORS
265   07707   20 0 304           ZJP L-2         IGNORE BLANK TAPE
266   07710   27 0 312           PJP CKCSB
267   07711   01 0 375           DCR PARTY       PARITY BIT (TAPE CHANNEL 8) SET
270   07712   02 1 365           CMB ACC         STRIP OFF PARITY BIT
271
272   07713   14 1 365   CKCSB   LSH ACC         CHECK FOR CHECKSUM BIT (TAPE CHANNEL 7)
273   07714   27 0 317           PJP CKTRB
274   07715   01 0 375           DCR PARTY       CHECKSUM BIT SET
275   07716   02 1 365           CMB ACC         STRIP OFF CHECKSUM BIT
276   07717   03 0 376           SMB TORCS       SET CHECKSUM FLAG (BIT 13=1 AND BIT 0=0)
277
300   07720   14 1 365   CKTRB   LSH ACC         CHECK FOR TRANSFER BIT (TAPE CHANNEL 6)
301   07721   27 0 326           PJP CKBTS
302   07722   01 0 375           DCR PARTY       TAPE CHANNEL 6 SET
303   07723   05 0 372           EDR 10R3F       CHECK WHETHER FIRST CHARACTER OF WORD
304   07724   26 0 326           OJP CKBTS       NO, IT IS NOT
305   07725   02 1 365           CMB ACC         TRANSFER CODE, STRIP OFF BIT
306   07726   16 0 376           RSH TORCS       SET TRANSFER FLAG (BIT 4=0; EVEN DESIGNTR)
```

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512633

```
307                                 EJE
310   07727  05 0 353  JCKBTS  EDR 5)          CHECK REST OF BITS (TAPE CHANNEL 1-5)
311   07730  06 0 347          SDR SHFT5       SET SHIFT FLAG TO SHIFT FIVE TIMES
312   07731  13 0 377          EOR WORD        (OR) PARTIAL WORD GENERATED THUS FAR
313   07732  14 1 365  SHIFT   LSH ACC
314   07733  27 0 334          PJP L+2
315   07734  01 0 375          DCR PARTY       BIT SET, DECREMENT PARITY INDICATOR
316   07735  01 0 347          DCR SHFT5
317   07736  27 0 331          PJP SHIFT
320
321   07737  01 0 375          DCR PARTY       TEST FOR ODD PARITY
322   07740  21 0 342          EJP NOPER
323   07741  00 0 004          STP 4           PARITY ERROR: S-REGISTER SET TO A FOUR
324   07742  24 0 202          JMP START       RESTART BINARY LOADER
325
326   07743  14 1 365  NOPER   LSH ACC         POSITION BINARY WORD: 1:0-1, 2:0-7, 3:0-13
327   07744  16 0 372          RSH 10R3F       CHECK WHETHER THIRD CHARACTER OF WORD
330   07745  25 1 276          CJP IBNWD,I     RETURN WITH BINARY WORD IN ACCUMULATOR
331   07746  24 0 303          JMP LOOP        GET NEXT CHARACTER
332
333   07747     00000  INPUT   ...
334             07747  SHFT5   SYN INPUT       COUNTER FOR SHIFTING FIVE TIMES
335   07750  30 0 000  INCOM   INT **          INPUT ONE CHR ON SAME CHA. AS BOOTSTRAP
336   07751  01 1 354          DCR PC          WAIT FOR INTERRUPT
337   07752  24 1 347  RDRTN   RTN             INTERRUPT RETURN
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 512633

```
      340                              EJE
      341                              GEN
            07753       00005          WRD
            07754       00000          WRD
            07755       07475          WRD
            07756       00001          WRD
            07757       30000          WRD
            07760       00103          WRD
            07761       23502          WRD
            07762       00102          WRD
            07763       07751          WRD
            07764       23400          WRD
            07765       00101          WRD
```

```
342                                    THE FOLLOWING MAY BE PROGRAM INPUTS
343   07766     00007   HSRIL  OCT HSRLO          HIGH SPEED READER INTERRUPT LOCATION
344   07767     00010   ASRIL  OCT ASRLO          ASR SET READER INTERRUPT LOCATION
345   07770     00025   RDCHL  OCT RCHLO          READER CHANNEL LOCATION FROM BOOTSTRAP
346   07771     07601   STOP   OCT STP-1          BINARY LOADER,S TRANSFER ON STOP CODE
347
350             07772   1OR3F  SYN STOP+1         FIRST OR THIRD CHARACTER FLAG
351             07773   CKSUM  SYN STOP+2         CHECKSUM LOCATION
352             07774   ORIGN  SYN STOP+3         NEXT LOCATION TO STORE A BINARY WORD
353             07775   PARTY  SYN STOP+4         PARITY INDEX COUNTER
354             07776   TORCS  SYN STOP+5         TRANSFER OR CHECKSUM FLAG
355             07777   WORD   SYN STOP+6         TEMPORARY STORAGE FOR PARTIAL RESULT
356             07775   COUNT  SYN PARTY          COUNTER FOR STORING IGNORE INTERRUPTS
357             07775   CORE   SYN PARTY          CORE INDEX
360             07776   SCORE  SYN TORCS          SHIFTED CORE INDEX
361             00000          END
```

PROJECT NO. 530053 PROGRAMMER E.E. O,HARE TAPE NUMBER 512633

STARTED 4/27/65. 2/51/00 P.M.
COMPLETED 4/27/65. 2/54/03 P.M.
NUMBER OF INPUT RECORDS 241.
NUMBER OF OUTPUT RECORDS 251.
NUMBER OF BINARY RECORDS 125.

COMMAND EXECUTE TEST (D9A)

I. Purpose of Test

To verify the proper operation of each instruction, except input and output, of the P-50 repertoire.

II. Description of Test

The program consists of an initialization routine which executes, stops and checks four instructions (EDR, JMP, ZJP, RJP); twenty-five routines which test the arithmetic and/or logic of each instruction; seventeen subroutines which verify the proper designator settings; and a number of error routines which display the invalid instructions.

As each instruction is tested and verified, it is added to the working repertoire of instructions.

During initialization each of four instructions is executed individually. If it functions properly a "Stop Check" occurs, if it fails, an "Error Stop" occurs (see Stop Summary). Each stop enters the designators with the operation code of the instruction tested and places the stop number in the S-Register (bits 7-0). The "Stop Check" verifies the proper operation of the instruction.

Following initialization there is a brief build-up of the working repertoire of instructions (ENL, SUB, STL). Later on these instructions are tested more extensively.

The core of the program tests each instruction individually, assuming only the working repertoire.

The designator subroutines check the designator settings after the execution of each instruction.

III. Description of Operation

A. Read in the binary tape of the Command Execute Test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of binary loader (X7602); depress the Start button.

3. Put machine in Run mode; depress the Master Clear button.

4. Place binary tape under the tape reader.

5. Turn the reader on.

6. Depress the Start button.

7. After the test has been read in, it will transfer to its starting location and begin.

B. The test should stop four times with the designator and S-Register set as follows:

Designator	S-Register (bits 7-0)
5	1
24	2
20	3
36	4

When the stop occurs check the Designator and S-Register for the proper setting. If the settings are correct, depress the Start button. After the four Stop Checks the program will run continuously.

C. If four bays of core are not present, Stop 5 will occur once for each absent bay. See the Stop Summary.

D. If another stop occurs one of the instructions is not working. Check the Stop Summary for the description of the stop and the location of the test routine in which it occurred. See the program listing for further explanation.

If a stop other than those specified occurs, a portion of the test has either been loaded incorrectly or destroyed.

To continue testing, depress the Start button. However, unless the malfunction of the instruction in error has been corrected, the remainder of the test may not work properly.

IV. Storage

Number of locations used: 2414_8 (5001_8 - 7414_8).

STOP SUMMARY

--COLUMN--	--COLUMN CONTENT--
STOP	STOP NUMBER IN THE S-REGISTER (BITS 7-0) WHICH COINCIDES WITH AN ERROR NUMBER ON THE PROGRAM LISTING. FOR EXAMPLE, STOP 210 = ERR210.
DESIGNATOR	OPERATION CODE OF THE INSTRUCTION BEING TESTED.
MNEMONIC	MNEMONIC OF THE INSTRUCTION BEING TESTED.
TEST	PROGRAM TEST NUMBER IN WHICH THE ERROR OCCURRED.
LOCATION	LOCATION OF THE TEST ROUTINE.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
1	5	EDR	1	5001	CHECK STOP, SHOULD OCCUR
2	24	JMP	2	5003	CHECK STOP, SHOULD OCCUR
3	20	ZJP	3	5006	CHECK STOP, SHOULD OCCUR
4	36	RJP	4	5016	CHECK STOP, SHOULD OCCUR
5	1	STL	7	5042	STL INTO BAY 1 DID NOT WORK
5	2	STL	7	5053	STL INTO BAY 2 DID NOT WORK
5	3	STL	7	5064	STL INTO BAY 3 DID NOT WORK
10	1	DCR	8A	5134	CONTINUOUSLY DCR THE NUMBER IN ONE LOCATION AND SUBTRACT ONE FROM THE NUMBER IN ANOTHER LOCATION, BOTH DID NOT REACH ZERO AT THE SAME TIME
11	1	DCR	21	7165	DCR NEGATIVE NUMBER SET THE POSITIVE INDICATOR
		DCR	23	7215	DCR NEGATIVE NUMBER SET THE POSITIVE INDICATOR
12	1	DCR	21	7165	DCR NEGATIVE NUMBER SET THE OVERFLOW INDICATOR
		DCR	23	7215	DCR NEGATIVE NUMBER SET THE OVERFLOW INDICATOR
13	1	DCR	20	6547	DCR POSITIVE NUMBER DID NOT SET THE OVERFLOW INDICATOR
		DCR	22	6577	DCR POSITIVE NUMBER DID NOT SET THE OVERFLOW INDICATOR
14	1	DCR	20	6547	DCR POSITIVE NUMBER SET THE ZERO INDICATOR
		DCR	21	7165	DCR NEGATIVE NUMBER SET THE ZERO INDICATOR
		DCR	22	6577	DCR POSITIVE NUMBER SET THE ZERO INDICATOR
		DCR	23	7215	DCR NEGATIVE NUMBER SET THE ZERO INDICATOR
15	1	DCR	20	6547	DCR POSITIVE NUMBER DID NOT SET END AROUND CARRY INDICATOR
		DCR	21	7165	DCR NEGATIVE NUMBER DID NOT SET END AROUND CARRY INDICATOR
		DCR	22	6577	DCR POSITIVE NUMBER DID NOT SET END AROUND CARRY INDICATOR
		DCR	23	7215	DCR NEGATIVE NUMBER DID NOT SET END AROUND CARRY INDICATOR
16	1	DCR	20	6547	DCR POSITIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
		DCR	22	6577	DCR POSITIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
20	2	CMB	13	5434	CMB NEGATIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
23	2	CMB	20	6546	CMB NEGATIVE NUMBER CLEARED THE OVERFLOW INDICATOR
		CMB	22	6576	CMB NEGATIVE NUMBER CLEARED THE OVERFLOW INDICATOR
24	2	CMB	20	6546	CMB NEGATIVE NUMBER SET THE ZERO INDICATOR
		CMB	22	6576	CMB NEGATIVE NUMBER SET THE ZERO INDICATOR
25	2	CMB	20	6546	CMB NEGATIVE NUMBER SET THE END AROUND CARRY INDICATOR
		CMB	22	6576	CMB NEGATIVE NUMBER SET THE END AROUND CARRY INDICATOR
26	2	CMB	20	6546	CMB NEGATIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
		CMB	22	6576	CMB NEGATIVE NUMBER DID NOT SET THE POSITIVE INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23, IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
30	3	SMB	12	5422	SMB NUMBER SET THE POSITIVE INDICATOR
31	3	SMB	13	5434	SMB NUMBER SET THE POSITIVE INDICATOR
33	3	SMB	21	7164	SMB POSITIVE NUMBER CLEARED THE OVERFLOW INDICATOR
		SMB	23	7214	SMB POSITIVE NUMBER CLEARED THE OVERFLOW INDICATOR
34	3	SMB	21	7164	SMB POSITIVE NUMBER SET THE ZERO INDICATOR
		SMB	23	7214	SMB POSITIVE NUMBER SET THE ZERO INDICATOR
35	3	SMB	21	7164	SMB POSITIVE NUMBER SET THE END AROUND CARRY INDICATOR
		SMB	23	7214	SMB POSITIVE NUMBER SET THE END AROUND CARRY INDICATOR
36	3	SMB	21	7164	SMB POSITIVE NUMBER SET THE POSITIVE INDICATOR
		SMB	23	7214	SMB POSITIVE NUMBER SET THE POSITIVE INDICATOR
60	6	SDR	10	5162	SDR IN ACCUMULATOR; SUBTRACT REAL VALUE, ZERO INDICATOR NOT SET
70	7	SDR	10	5162	SDR IN ACCUMULATOR; SUBTRACT REAL VALUE, ZERO INDICATOR NOT SET
100	10	ADD	15A	5526	ADD POSITIVE ZERO TO POSITIVE ZERO; RESULT WAS NOT POSITIVE ZERO
101	10	ADD	15A	5526	ADD NEGATIVE ZERO TO POSITIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
102	10	ADD	15A	5526	ADD POSITIVE ZERO TO NEGATIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
103	10	ADD	15A	5526	ADD NEGATIVE ZERO TO NEGATIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
104	10	ADD	15A	5526	ADD NEGATIVE NUMBER TO POSITIVE NUMBER; RESULT WAS NOT NEGATIVE ZERO
105	10	ADD	15A	5526	ADD POSITIVE NUMBER TO NEGATIVE NUMBER; RESULT WAS NOT NEGATIVE ZERO
106	10	ADD	15B	5566	ERROR IN THE ADDER TEST, SEE THE PROGRAM LISTING
110	11	SUB	6	5025	SUB A NUMBER FROM ITSELF, RESULT WAS NOT ZERO
111	11	SUB	8	5075	SUB POSITIVE ZERO FROM POSITIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
112	11	SUB	8	5075	SUB NEGATIVE ZERO FROM POSITIVE ZERO; RESULT WAS NOT POSITIVE ZERO
113	11	SUB	8	5075	SUB POSITIVE ZERO FROM NEGATIVE ZERO; RESULT WAS NOT NEGATIVE ZERO

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23. IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
114	11	SUB	8	5075	SUB NEGATIVE ZERO FROM NEGATIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
115	11	SUB	8	5075	SUB POSITIVE NUMBER FROM SAME POSITIVE NUMBER RESULT WAS NOT NEGATIVE ZERO
116	11	SUB	8	5075	SUB NEGATIVE NUMBER FROM SAME NEGATIVE NUMBER RESULT WAS NOT NEGATIVE ZERO
120	12	AND	14A	5451	AND POSITIVE ZERO WITH POSITIVE ZERO; RESULT WAS NOT POSITIVE ZERO
121	12	AND	14A	5451	AND POSITIVE ZERO WITH NEGATIVE ZERO; RESULT WAS NOT POSITIVE ZERO
122	12	AND	14A	5451	AND NEGATIVE ZERO WITH POSITIVE ZERO; RESULT WAS NOT POSITIVE ZERO
123	12	AND	14A	5451	AND NEGATIVE ZERO WITH NEGATIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
130	13	EOR	14B	5500	EOR POSITIVE ZERO WITH POSITIVE ZERO; RESULT WAS NOT POSITIVE ZERO
131	13	EOR	14B	5500	EOR POSITIVE ZERO WITH NEGATIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
132	13	EOR	14B	5500	EOR NEGATIVE ZERO WITH POSITIVE ZERO; RESULT WAS NOT NEGATIVE ZERO
133	13	EOR	14B	5500	EOR NEGATIVE ZERO WITH NEGATIVE ZERO; RESULT WAS NOT POSITIVE ZERO
140	14	LSH	17	5625	LSH NEGATIVE ALTERNATE ONES TWICE RESULT WAS NOT NEGATIVE ALTERNATEONES
141	14	LSH	17A	5637	LSH NEGATIVE ZERO, RESULT WAS NOT NEGATIVE ZERO
142	14	LSH	17A	5637	LSH POSITIVE ZERO, RESULT WAS NOT POSITIVE ZERO
143	14	LSH	24	6214	LSH ALTERNATE ONES DID NOT SET THE OVERFLOW INDICATOR
144	14	LSH	24	6214	LSH ALTERNATE ONES SET THE EVEN INDICATOR
145	14	LSH	24	6214	LSH ALTERNATE ONES SET THE ZERO INDICATOR
146	14	LSH	24	6214	LSH POSITIVE ALTERNATE ONES SET THE POSITIVE OR SET THE END AROUND CARRY INDICATOR OR LSH NEGATIVE ALTERNATE ONES CLEARED THE POSITIVE OR THE END AROUND CARRY INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23. IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
151	15	LSH	17B	5652	LSH POSITIVE ZERO, RESULT WAS NOT POSITIVE ZERO
152	15	LSH	17B	5652	LSH NEGATIVE ZERO, RESULT WAS NOT NEGATIVE ZERO
153	16	RSH	21	7164	RSH NEGATIVE NUMBER SET THE END AROUND CARRY INDICATOR
		RSH	23	7214	RSH NEGATIVE NUMBER SET THE END AROUND CARRY INDICATOR
154	16	RSH	21	7164	RSH NEGATIVE NUMBER SET THE POSITIVE INDICATOR
		RSH	23	7214	RSH NEGATIVE NUMBER SET THE POSITIVE INDICATOR
155	16	RSH	21	7164	RSH NEGATIVE NUMBER WITH BITS 1-0 SET TO ZERO SET THE EVEN INDICATOR
		RSH	23	7214	RSH NEGATIVE NUMBER WITH BITS 1-0 SET TO ZERO SET THE EVEN INDICATOR
156	16	RSH	21	7164	RSH NEGATIVE NUMBER CLEARED OVERFLOW INDICATOR
		RSH	23	7214	RSH NEGATIVE NUMBER CLEARED OVERFLOW INDICATOR
157	16	RSH	21	7164	RSH NEGATIVE NUMBER SET ZERO INDICATOR
		RSH	23	7214	RSH NEGATIVE NUMBER SET ZERO INDICATOR
160	16	RSH	18	6044	RSH NEGATIVE ALTERNATE ONES; SEE THE PROGRAM LISTING
161	16	RSH	18	6044	RSH POSITIVE ALTERNATE ONES; SEE THE PROGRAM LISTING
162	16	RSH	18A	6074	RSH POSITIVE ZERO, RESULT WAS NOT POSITIVE ZERO
163	16	RSH	18A	6074	RSH POSITIVE ONE, RESULT WAS NOT POSITIVE ZERO
164	16	RSH	18A	6074	RSH NEGATIVE ZERO, RESULT WAS NOT NEGATIVE ZERO
165	16	RSH	18A	6074	RSH NEGATIVE ONE, RESULT WAS NOT NEGATIVE ZERO
171	17	RSH	18B	6122	RSH POSITIVE ZERO, RESULT WAS NOT POSITIVE ZERO
172	17	RSH	18B	6122	RSH POSITIVE ONE, RESULT WAS NOT POSITIVE ZERO
173	17	RSH	18B	6122	RSH NEGATIVE ZERO, RESULT WAS NOT NEGATIVE ZERO
174	17	RSH	18B	6122	RSH NEGATIVE ONE, RESULT WAS NOT NEGATIVE ZERO
175	16	RSH	20	6546	RSH POSITIVE NUMBER SET THE END AROUND CARRY INDICATOR
			22	6576	RSH POSITIVE NUMBER SET THE END AROUND CARRY INDICATOR
176	16	RSH	20	6546	RSH POSITIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
			22	6576	RSH POSITIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
177	16	RSH	20	6546	RSH POSITIVE NUMBER WITH BITS 1-0 SET TO ZERO DID NOT SET THE EVEN INDICATOR
			22	6576	RSH POSITIVE NUMBER WITH BITS 1-0 SET TO ZERO DID NOT SET THE EVEN INDICATOR
200	20	ZJP	3	5006	WITH THE ZERO INDICATOR SET, ZJP DID NOT OCCUR
201	20	ZJP	10	5162	WITH THE ZERO INDICATOR SET, ZJP DID NOT OCCUR
202	20	ZJP	DSIGCK	6605	EDR ZERO SET THE ZERO INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23. IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
303	10	SUB	20	6542	SUB NEGATIVE NUMBER WITH RESULT POSITIVE; DID NOT SET THE POSITIVE INDICATOR
		ADD	22	6572	ADD TWO POSITIVE NUMBERS WITH RESULT POSITIVE; DID NOT SET THE POSITIVE INDICATOR
304	10	SUB	20	6542	SUB NEGATIVE NUMBER WITH RESULT POSITIVE; DID NOT SET THE EVEN INDICATOR
		SUB	21	7160	SUB POSITIVE NUMBER WITH RESULT NEGATIVE; DID NOT SET THE EVEN INDICATOR
		ADD	22	6572	ADD TWO POSITIVE NUMBER WITH RESULT POSITIVE; DID NOT SET THE EVEN INDICATOR
		ADD	23	7210	ADD TWO NEGATIVE NUMBER WITH RESULT NEGATIVE; DID NOT SET THE EVEN INDICATOR
305	10	SUB	21	7160	SUB POSITIVE NUMBER WITH RESULT NEGATIVE; SET THE POSITIVE INDICATOR
		ADD	23	7210	ADD TWO NEGATIVE NUMBER WITH RESULT NEGATIVE; SET THE POSITIVE INDICATOR
306	10	SUB	21	7160	SUB POSITIVE NUMBER WITH RESULT NEGATIVE; DID NOT SET END AROUND CARRY INDICATOR
		ADD	23	7210	ADD TWO NEGATIVE NUMBER WITH RESULT NEGATIVE; DID NOT SET END AROUND CARRY INDICATOR
307	10	SUB	20	6544	SUB NEGATIVE NUMBER FROM POSITIVE WITH RESULT NEGATIVE DID NOT SET THE OVERFLOW INDICATOR
		SUB	21	7162	SUB POSITIVE NUMBER FROM NEGATIVE WITH RESULT POSITIVE; DID NOT SET OVERFLOW INDICATOR
		ADD	22	6574	ADD TWO POSITIVE NUMBERS WITH RESULT NEGATIVE DID NOT SET OVERFLOW INDICATOR
		ADD	23	7213	ADD TWO NEGATIVE NUMBERS WITH RESULT POSITIVE; DID NOT SET OVERFLOW INDICATOR
310	10	SUB	20	6544	SUB NEGATIVE NUMBER FROM POSITIVE WITH RESULT NEGATIVE SET THE POSITIVE INDICATOR
		ADD	22	6574	ADD TWO POSITIVE NUMBERS WITH RESULT NEGATIVE SET THE POSITIVE INDICATOR
311	10	SUB	20	6544	SUB NEGATIVE NUMBER FROM POSITIVE WITH RESULT NEGATIVE SET THE ZERO INDICATOR
		SUB	21	7162	SUB POSITIVE NUMBER FROM NEGATIVE WITH RESULT POSITIVE; SET THE ZERO INDICATOR
		ADD	22	6574	ADD TWO POSITIVE NUMBERS WITH RESULT NEGATIVE SET THE ZERO INDICATOR
		ADD	23	7213	ADD TWO NEGATIVE NUMBERS WITH RESULT POSITIVE; SET THE ZERO INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23. IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
210	21	EJP	19	6153	EDR ZERO SET THE EVEN INDICATOR
211	21	EJP	19	6153	WITH THE EVEN INDICATOR SET, EJP DID NOT OCCUR
221	22	SLJ	25	6236	SLJ, BUT JUMP DID NOT OCCUR
231	23	CLJ	25	6240	CLJ, BUT JUMP DID NOT OCCUR
240	24	JMP	2	5003	JMP DID NOT OCCUR
250	25	CJP	16	5606	EDR ZERO SET THE END AROUND CARRY INDICATOR
251	25	CJP	16	5606	WITH THE END AROUND CARRY INDICATOR SET; CJP DID NOT OCCUR
260	26	OJP	19A	6170	EDR ZERO SET THE OVERFLOW INDICATOR
261	26	OJP	19A	6170	WITH THE OVERFLOW INDICATOR SET, OJP DID NOT OCCUR
270	27	PJP	11	5230	EDR ZERO SET THE POSITIVE INDICATOR
271	27	PJP	11	5230	WITH THE POSITIVE INDICATOR SET, PJP DID NOT OCCUR
300	10	SUB	20	6542	SUB NEGATIVE NUMBER WITH RESULT POSITIVE; SET THE OVERFLOW INDICATOR
		SUB	21	7160	SUB POSITIVE NUMBER WITH RESULT NEGATIVE; SET THE OVERFLOW INDICATOR
		ADD	22	6572	ADD TWO POSITIVE NUMBER WITH RESULT POSITIVE; SET THE OVERFLOW INDICATOR
		ADD	23	7210	ADD TWO NEGATIVE NUMBER WITH RESULT NEGATIVE; SET THE OVERFLOW INDICATOR
301	10	SUB	20	6542	SUB NEGATIVE NUMBER WITH RESULT POSITIVE; SET THE ZERO INDICATOR
		SUB	21	7160	SUB POSITIVE NUMBER WITH RESULT NEGATIVE; SET THE ZERO INDICATOR
		ADD	22	6572	ADD TWO POSITIVE NUMBERS WITH RESULT POSITIVE; SET THE ZERO INDICATOR
		ADD	23	7210	ADD TWO NEGATIVE NUMBERS WITH RESULT NEGATIVE; SET THE ZERO INDICATOR
302	10	SUB	20	6542	SUB NEGATIVE NUMBER WITH RESULT POSITIVE; SET THE END AROUND CARRY INDICATOR
		ADD	22	6572	ADD TWO POSITIVE NUMBERS WITH RESULT POSITIVE; SET THE END AROUND CARRY INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23. IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
351	12	AND	20	6546	AND POSITIVE NUMBER; DID NOT SET THE END AROUND CARRY INDICATOR
		AND	21	7164	AND NEGATIVE NUMBER; DID NOT SET THE END AROUND CARRY INDICATOR
		AND	22	6576	AND POSITIVE NUMBER; DID NOT SET THE END AROUND CARRY INDICATOR
		AND	23	7214	AND NEGATIVE NUMBER; DID NOT SET THE END AROUND CARRY INDICATOR
352	12	AND	20	6546	AND POSITIVE NUMBER; SET THE ZERO INDICATOR
		AND	21	7164	AND NEGATIVE NUMBER; SET THE ZERO INDICATOR
		AND	22	6576	AND POSITIVE NUMBER; SET THE ZERO INDICATOR
		AND	23	7214	AND NEGATIVE NUMBER; SET THE ZERO INDICATOR
353	12	AND	20	6546	AND POSITIVE NUMBER WITH BIT 0 SET TO ZERO; DID NOT SET THE EVEN INDICATOR
		AND	22	6576	AND POSITIVE NUMBER WITH BIT 0 SET TO ZERO; DID NOT SET THE EVEN INDICATOR
354	12	AND	20	6546	AND POSITIVE NUMBER WITH BIT 13 SET TO ONE; DID NOT SET POSITIVE INDICATOR
		AND	22	6576	AND POSITIVE NUMBER WITH BIT 13 SET TO ONE; DID NOT SET THE POSITIVE INDICATOR
355	12	AND	21	7164	AND NEGATIVE NUMBER WITH BIT 13 SET TO ONE; SET THE POSITIVE INDICATOR
		AND	23	7214	AND NEGATIVE NUMBER WITH BIT 13 SET TO ONE; SET THE POSITIVE INDICATOR
356	12	AND	21	7164	AND NEGATIVE NUMBER WITH BIT 0 SET TO ZERO; SET THE EVEN INDICATOR
		AND	23	7214	AND NEGATIVE NUMBER WITH BIT 0 SET TO ZERO; SET THE EVEN INDICATOR
357	13	EOR	20	6552	EOR POSITIVE NUMBER; CLEAR THE OVERFLOW INDICATOR
360	13	EOR	20	6552	EOR POSITIVE NUMBER WITH ALL ONES SET THE POSITIVE INDICATOR
361	13	EOR	20	6552	EOR POSITIVE NUMBER WITH ALL ONES; SET THE ZERO INDICATOR
		EOR	21	7170	EOR NEGATIVE NUMBER WITH ALL ONES; SET THE ZERO INDICATOR
362	13	EOR	21	7170	EOR NEGATIVE NUMBER; SET THE OVERFLOW INDICATOR
363	13	EOR	21	7170	EOR NEGATIVE NUMBER WITH ALL ONES DID NOT SET THE POSITIVE INDICATOR

CHECK LOCATION TEST (6604); IF STOP INVOLVES TESTS 20-23, IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
312	10	SUB	20	6544	SUB NEGATIVE NUMBER FROM POSITIVE WITH RESULT NEGATIVE SET THE END AROUND CARRY INDICATOR
		ADD	22	6574	ADD TWO POSITIVE NUMBERS WITH RESULT NEGATIVE SET THE END AROUND CARRY INDICATOR
313	10	SUB	21	7162	SUB POSITIVE NUMBER FROM NEGATIVE WITH RESULT POSITIVE; DID NOT SET THE POSITIVE INDICATOR
		ADD	23	7213	ADD TWO NEGATIVE NUMBERS WITH RESULT POSITIVE; DID NOT SET THE POSITIVE INDICATOR
314	10	SUB	21	7162	SUB POSITIVE NUMBER FROM NEGATIVE WITH RESULT POSITIVE; DID NOT SET END AROUND CARRY INDICATOR
		ADD	23	7213	ADD TWO NEGATIVE NUMBERS WITH RESULT POSITIVE; DID NOT SET END AROUND CARRY INDICATOR
320	32	ENL	5	5017	ENL WITH ZERO, THE ZERO INDICATOR NOT SET
321	32	ENL	20	6540	ENL POSITIVE NUMBER SET THE OVERFLOW INDICATOR
		ENL	22	6570	ENL POSITIVE NUMBER SET THE OVERFLOW INDICATOR
322	32	ENL	20	6540	ENL POSITIVE NUMBER SET THE ZERO INDICATOR
		ENL	22	6570	ENL POSITIVE NUMBER SET THE ZERO INDICATOR
323	32	ENL	20	6540	ENL POSITIVE NUMBER SET THE END AROUND CARRY INDICATOR
		ENL	22	6570	ENL POSITIVE NUMBER SET THE END AROUND CARRY INDICATOR
324	32	ENL	20	6540	ENL POSITIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
		ENL	22	6570	ENL POSITIVE NUMBER DID NOT SET THE POSITIVE INDICATOR
330	33	ENL	5	5022	ENL WITH ZERO; THE ZERO INDICATOR NOT SET
334	32	ENL	21	7157	ENL NEGATIVE NUMBER SET THE OVERFLOW INDICATOR
		ENL	23	7206	ENL NEGATIVE NUMBER SET THE OVERFLOW INDICATOR
335	32	ENL	21	7157	ENL NEGATIVE NUMBER SET END AROUND CARRY INDICATOR
		ENL	23	7206	ENL NEGATIVE NUMBER SET END AROUND CARRY INDICATOR
336	32	ENL	21	7157	ENL NEGATIVE NUMBER SET THE ZERO INDICATOR
		ENL	23	7206	ENL NEGATIVE NUMBER SET THE ZERO INDICATOR
337	32	ENL	21	7157	ENL NEGATIVE NUMBER SET THE POSITIVE INDICATOR
		ENL	23	7206	ENL NEGATIVE NUMBER SET THE POSITIVE INDICATOR
350	12	AND	20	6546	AND POSITIVE NUMBER; CLEAR THE OVERFLOW INDICATOR
		AND	21	7164	AND NEGATIVE NUMBER; CLEAR THE OVERFLOW INDICATOR
		AND	22	6576	AND POSITIVE NUMBER; CLEAR THE OVERFLOW INDICATOR
		AND	23	7214	AND NEGATIVE NUMBER; CLEAR THE OVERFLOW INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23, IT CONTAINS THE TEST NUMBER.

STOP	DESIGNATOR	MNEMONIC	TEST	LOCATION	DESCRIPTION OF STOP
370	37	STL	7	5035	STL A NUMBER; SUBTRACT IT; THE ZERO INDICATOR NOT SET
371	37	STL	9	5145	STL A NUMBER; SUBTRACT IT; THE ZERO INDICATOR NOT SET
372	37	STL	21	7172	STL POSITIVE NUMBER, SET THE OVERFLOW INDICATOR
373	37	STL	20	6554	STL NEGATIVE NUMBER; CLEAR THE OVERFLOW INDICATOR
374	37	STL	20	6554	STL NEGATIVE NUMBER, SET THE ZERO INDICATOR
		STL	21	7172	STL POSITIVE NUMBER, SET THE ZERO INDICATOR
375	37	STL	20	6554	STL NEGATIVE NUMBER; SET END THE AROUND CARRY INDICATOR
		STL	21	7172	STL POSITIVE NUMBER; SET END THE AROUND CARRY INDICATOR
376	37	STL	20	6554	STL NEGATIVE NUMBER; SET POSITIVE INDICATOR
377	37	STL	21	7172	STL POSITIVE NUMBER; DID NOT SET THE POSITIVE INDICATOR

CHECK LOCATION TEST (6604) IF STOP INVOLVES TESTS 20-23. IT CONTAINS THE TEST NUMBER.

PROJECT NO. 550050 PROGRAMMER J.S. PHILLIPPI APE NUMBER 345116

```
 1                                    COMMAND EXECUTE TEST
 2
 3                                    PROGRAM LIBRARY
 4                                    PROGRAM NO.  P-50 D9A
 5
 6
 7                                    DECREMENT COUNTER MACRO
10                    DSK     MAC INDEx,TEST,LOOP
11                            DCR INDEX
12                            JP TEST
13                            JMP LOOP
14                            TER
15                                   ERROR STOP MACRO
16                                   ERR ABC WHERE ABC IS SOME NUMBER REFERS TO STOP ABC
17                                   S-REGISTER CONTAINS ABC
20                                   DESIGNATOR CONTAINS AB  (IN MOST CASES)
21                    ERR     MAC A1,A2,JUMP
22                            EDR A1
23                            STP A2
24                            JMP JUMP
25                            TER
26                    MNE     VFD 5,1,8
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
27                          EJE
30                                IF A STOP IS DESIRED AFTER ONE CYCLE: DO THE FOLLOWING
31
32                                SINCE THERE IS A TRANSFER CODE AT THE END OF THE TAPE,
33                                THE TEST WILL BEGIN IMMEDIATELY AFTER IT IS READ IN
34                                HOWEVER, AFTER ONE INSTRUCTION HAS BEEN EXECUTED, THE
35                                MACHINE WILL STOP WITH THE S-REGISTER (BITS 7-0) SET
36                                TO 1.  THIS IS THE FIRST CHECK STOP OF THE TEST
37
40                                1.  WHEN STOP 1 OCCURS, DEPRESS THE STOP BUTTON.
41                                2.  PUT THE MACHINE IN WRITE MODE.
42                                3.  DEPRESS THE MASTER CLEAR BUTTON.
43                                4.  USING THE PROBE, LOAD THE S-REGISTER WITH 6244.
44                                5.  USING THE PROBE, LOAD THE X-REGISTER WITH 6.
45                                6.  DEPRESS THE START BUTTON.
46                                7.  DEPRESS THE MASTER CLEAR BUTTON.
47                                8.  USING THE PROBE, LOAD THE X-REGISTER WITH THE
50                                    STARTING LOCATION OF THE TEST, 5000.
51                                9.  DEPRESS THE START BUTTON.
52                                10. PUT THE MACHINE IN RUN MODE.
53                                11.DEPRESS THE MASTER CLEAR BUTTON.
54                                12. DEPRESS THE START BUTTON.
55                                13. THE TEST SHOULD RUN THROUGH ONE CYCLE, STOPPING
56                                    AT THE FOUR CHECK STOPS AND CONTINUING.
57                                14. WHEN ONE CYCLE IS COMPLETE, THE MACHINE WILL STOP
60                                    WITH THE S-REGISTER (BITS 7-0) SET TO 6.
61                                15. ONE CYCLE RUNS FOR 14 SECONDS.
62
63
64                                TO RESTORE THE CONTINUOUS CYCLING OF THE TEST, DO
65                                THE FOLOWING:
66                                1.  DEPRESS THE STOP BUTTON.
67                                2.  PUT THE MACHINE IN WRITE MODE.
70                                3.  DEPRESS THE MASTER CLEAR BUTTON.
71                                4.  USING THE PROBE, LOAD THE S-REGISTER WITH 6244.
72                                5.  USING THE PROBE, LOAD THE X-REGISTER WITH 24745.
73                                6.  DEPRESS THE START BUTTON.
74                                7.  DEPRESS THE MASTER CLEAR BUTTON.
75                                8.  USING THE PROBE, LOAD THE X-REGISTER WITH THE
76                                    STARTING LOCATION OF THE TEST, 5000.
```

PRO_E:T NO. 530053 PROGRAMMER _.E. PHILLIPPI TAPE NUMBER 345116

```
   77
  100
  101
  102
  103
  104
```

9. DEPRESS THE START BUTTON.
10. PUT THE MACHINE IN RUN MODE.
11. DEPRESS THE MASTER CLEAR BUTTON.
12. DEPRESS THE START BUTTON.
13. THE TEST WILL RUN CONTINUOUSLY AFTER STOPPING AT THE CHECK STOPS.

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
105                              EJE
106                                        INITIALLY THE PROGRAM STOPS AT 4 CHECK STOPS
107
110
111              05001          8ORG 5001
112                                        TEST 01  EDR
113
114                                        ENTER DESIGNATOR WITH A NUMBER N, N=5, AND STOP
115                                        S-REGISTER IS 1
116                                        IF DESIGNATOR IS N, ASSUME EDR WORKS
117                                        IF DESIGNATOR IS NOT N
120                                              1. CHECK LOCATION 5377  SHOULD BE 5
121                                              2. IF LOCATION IS 5, EDR DOES NOT WORK
122                                              3. IF LOCATION IS NOT 5, MAKE IT 5 AND RESTART
123   05001   05 0 377  /TEST018EDR 5)
124   05002      04001           HNE 4,,1
125
126
127                                        TEST 02  JMP
130
131                                        JUMP AND STOP
132                                        DESIGNATOR IS 24
133                                        IF S-REGISTER IS 2, ASSUME JMP WORKS
134                                        IF S-REGISTER IS 240, JUMP DID NOT OCCUR
135                                              COMPARE LOCATION 5003 WITH LISTING
136   05003   24 0 010    TEST02 JMP L+6
137   05004   05 0 376          8EDR 24)
140   05005   00 0 240          8STP 240
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
141                                EJE
142                                                TEST 03  ZJP
143
144                                                ENTER DESIGNATOR WITH ZERO INDICATOR AND ZERO JUMP
145                                                DESIGNATOR IS 20
146                                                IF S-REGISTER IS 3, ASSUME ZJP WORKS
147                                                IF S-REGISTER IS 200, JUMP DID NOT OCCUR
150                                                     CHECK LOCATION 5375  SHOULD BE 10-ZERO INDICATOR
151   05006  05 0 375  /TEST03BEDR 10)
152   05007  20 0 013           ZJP L+5
153   05010  24 0 267           JMP ERR200
154   05011  05 0 376         BEDR 24)
155   05012     04002           HNE 4,,2
156   05013  24 0 005           JMP TEST03
157   05014  05 0 374  /       BEDR 20)
160   05015     04003           HNE 4,,3
161
162
163                                                TEST 04  RJP
164
165                                                RETURN JUMP AND STOP
166                                                DESIGNATOR IS 36
167                                                IF S-REGISTER IS 4, ASSUME RJP WORKS
170                                                IF STOP DOES NOT OCCUR, JUMP DID NOT OCCUR
171                                                     CHECK LOCATION 5016 COMPARE WITH LISTING
172   05016  36 0 255   TEST04 RJP STOPCK
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
173                                 EJE
174                                                 TEST 05  ENL
175
176                                                 ENTER ACCUMULATOR WITH ZERO AND ZERO JUMP
177                                                 IF STOP OCCURS
200                                                       1. S-REGISTER IS 320
201                                                       2. DESIGNATOR IS 32
202                                                       3. CHECK ACCUMULATOR 101 SHOULD BE ZERO
203                                                       4. CHECK LOCATION 5373  SHOULD BE ZERO
204                                                          IF LOCATION IS ZERO, ENL DOES NOT WORK
205   05017  32 0 373  /TEST05 ENL 0)
206   05020  20 0 021         ZJP L+2
207   05021  24 0 272         JMP ERR320
210                                                        ENL (33)
211   05022     33373         @ANE 33,,373
212   05023  20 0 024         ZJP TEST06
213   05024  24 0 325         JMP ERR330
214
215
216                                                 TEST 06  SUP
217
220                                                 ENTER ACCUMULATOR WITH SOME NUMBER N. SUBTRACT N. ZJP
221                                                 IF STOP OCCURS
222                                                       1. S-REGISTER IS 110
223                                                       2. DESIGNATOR IS 11
224                                                       3. CHECK ACCUMULATOR 101 SHOULD BE ZERO
225                                                          IF ACCUMULATOR NOT ZERO, SUB DOES NOT WORK
226   05025  32 0 372  /TEST06@ENL 21476)
227   05026  11 1 371  /       SUB ACC
230   05027  20 0 030         ZJP L+2
231   05030  24 0 275         JMP ERR110
232   05031  32 0 370  /      @ENL 16301)
233   05032  11 1 371         SUB ACC
234   05033  20 0 034         ZJP TEST07
235   05034  24 0 275         JMP ERR110
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
236                                EJE
237                                          TEST 07  STL
238
241                                          ENTER ACCUMULATOR WITH SOME NUMBER N, STORE N IN Y
242                                          SUBTRACT Y, ZERO JUMP
243                                          IF STOP OCCURS
244                                                1. S-REGISTER IS 370
245                                                2. DESIGNATOR IS 3?
246                                                3. CHECK ACCUMULATOR SHOULD BE ZERO
247                                                4. CHECK LOCATIONS 5367  5263  SHOULD BE EQUAL
250                                                   IF NOT EQUAL STL DOES NOT WORK
251   05035  32 0 367  JTEST07BENL 37776)
252   05036  37 0 263           STL TEMP
253   05037  11 0 263           SUB TEMP
254   05040  20 0 041           ZJP TEST7A
255   05041  24 0 300           JMP ERR370
```

PROJECT NO. 538053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
256                                    EJE
257                                                TEST 7A  STL
258
261                                                SIMILAR TO TEST 07
262                                                STORE N IN THREE OTHER BAYS OF CORE
263                                                IF STOP OCCURS S REGISTER IS 5
264                                                      1. DESIGNATOR IS 1
265                                                         BAY 1 DOES NOT EXIST OR
266                                                         N STORED INCORRECTLY IN Y  Y IS 17776
267                                                         Y AND LOCATION 5372 SHOULD BE EQUAL
270                                                      2. DESIGNATOR IS 2
271                                                         BAY 2 DOES NOT EXIST OR
272                                                         N STORED INCORRECTLY IN Y  Y IS 27776
273                                                         Y AND LOCATION 5370 SHOULD BE EQUAL
274                                                      3. DESIGNATOR IS 3
275                                                         BAY 3 DOES NOT EXIST OR
276                                                         N STORED INCORRECTLY IN Y  Y IS 37776
277                                                         Y AND LOCATION 5372 SHOULD BE EQUAL
300   05042  32 0 372   TEST7A BENL 21476)
301   05043  37 1 366  J        BSTL 17776),I
302   05044  32 0 374           BENL 20)
303   05045  37 1 365  J        BSTL 7776),I
304   05046  32 1 366           BENL 17776),I
305   05047  11 0 372           BSUB 21476)
306   05050  20 0 052            ZJP L+3
307   05051  05 0 364  J         EDR 1)
310   05052     04005            RNE 4,,5
311   05053  32 0 370           BENL 16301)
312   05054  37 1 363  J        BSTL 27776),I
313   05055  32 0 374           BENL 20)
314   05056  37 1 365           BSTL 7776),I
315   05057  32 1 363           BENL 27776),I
316   05060  11 0 370           BSUB 16301)
317   05061  20 0 063            ZJP L+3
320   05062  05 0 362  J         EDR 2)
321   05063     04005            RNE 4,,5
322   05064  32 0 372           BENL 21476)
323   05065  37 1 367           BSTL 37776),I
324   05066  32 0 374           BENL 20)
325   05067  37 1 365           BSTL 7776),I
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
326   05070  32 1 367          8ENL 37776),I
327   05071  11 0 372          8SUB 21476)
330   05072  20 0 074           ZJP TEST08
331   05073  05 0 361  J        EDR 3)
332   05074     04005           MNE 4,,5
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
333                                    EJE
334                                              TEST 8  SUB
335
336                                                      ACC      Y      RESULT      ERROR
337
340   05075   32 0 373    TEST08 ENL 0)                *0       *0       -0          111
341   05076   11 0 373           SUB 0)
342   05077   20 0 100           ZJP L+2
343   05100   24 0 330           JMP ERR111
344   05101   27 0 077           PJP L-1
345   05102   32 0 373           ENL 0)                *0       -0       *0          112
346   05103   11 0 360  J        SUB -0)
347   05104   20 0 105           ZJP L+2
350   05105   24 0 377           JMP ERR112
351   05106   27 0 107           PJP L+2
352   05107   24 0 104           JMP L-2
353   05110   32 0 360           ENL -0)               -0       *0       -0          113
354   05111   11 0 373           SUB 0)
355   05112   20 0 113           ZJP L+2
356   05113   24 1 357  J        JMP ERR113
357   05114   27 0 112           PJP L-1
360   05115   32 0 360           ENL -0)               -0       -0       -0          114
361   05116   11 0 360           SUB -0)
362   05117   20 0 120           ZJP L+2
363   05120   24 1 356  J        JMP ERR114
364   05121   27 0 117           PJP L-1
365   05122   32 0 355  J        8ENL 12525)           *N       *N       -0          115
366   05123   11 0 355           8SUB 12525)
367   05124   20 0 125           ZJP L+2
370   05125   24 1 354  J        JMP ERR115
371   05126   27 0 124           PJP L-1
372   05127   32 0 353  J        8ENL 25252)           -N       -N       -0          116
373   05130   11 0 353           8SUB 25252)
374   05131   20 0 132           ZJP L+2
375   05132   24 1 352  J        JMP ERR116
376   05133   27 0 131           PJP L-1
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
377                                 EJE
400                                                 TEST 8A DCR
401
402                                                 CHECK DECREMENT WITH SUBTRACT
403                                                 ENTER ACCUMULATOR WITH N, STORE N IN Y
404                                                 SUBTRACT 1 AND DECREMENT Y CONTINUOUSLY
405                                                 JUMP WHEN ACCUMULATOR ZERO
406                                                 IF STOP OCCURS
407                                                       1. S-REGISTER IS 10
410                                                       2. DESIGNATOR IS 1
411                                                       3. CHECK ACCUMULATOR 101  SHOULD BE ZERO
412                                                       4. CHECK LOCATION 5263  SHOULD BE ZERO
413                                                          IF NOT ZERO DCR DOES NOT WORK
414   05134   32 0 367   TEST8AENL 37776)
415   05135   37 0 263          STL TEMP
416   05136   20 0 141          ZJP L+4
417   05137   01 0 263          DCR TEMP
420   05140   11 0 364          SUB 1)
421   05141   24 0 135          JMP L-3
422   05142   32 0 263          ENL TEMP
423   05143   20 0 144          ZJP TEST09
424   05144   24 0 303          JMP ERR010
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI APE NUMBER 345116

```
                                    EJE
                                                TEST 09  STL
                                                SAME AS TEST 07 ONLY MORE EXHAUSTIVE
                                                TESTS 10000 NUMBERS
                                                IF STOP OCCURS
                                                      1. S-REGISTER IS 371
                                                      2. DESIGNATOR IS 37
                                                      3. CHECK ACCUMULATOR 101  SHOULD BE ZERO
                                                      4. CHECK LOCATIONS  5263  5264  SHOULD BE EQUAL
                                                         IF NOT EQUAL  STL DOES NOT WORK
05145  32 0 351  JTEST09BENL 10000)
05146  37 8 266          STL INDEX
05147  32 0 350  J       BENL 20000)
05150  37 8 263          STL TEMP
05151  32 0 263   JMP09A ENL TEMP
05152  37 0 264          STL TEMPA
05153  11 0 264          SUB TEMPA
05154  20 0 155          ZJP L+2
05155  24 0 306          JMP ERR371
05156  01 0 263          DCR TEMP
05157  01 0 266          DCR INDEX
05160  20 0 161          ZJP TEST10
05161  24 0 150          JMP JMP09A
```

```
455                                 EJE
456                                                 TEST 10  SDR
457
460                                                 ENTER DESIGNATOR WITH N=37-30,17-10  (ZERO INDICATOR)
461                                                 ZERO JUMP TO STORE DESIGNATOR IN Y
462                                                 ENTER ACCUMULATOR WITH Y, SUBTRACT N, ZERO JUMP
463                                                 IF STOP OCCURS
464                                                       1. S-REGISTER IS 201
465                                                          DESIGNATOR IS 20
466                                                          CHECK INITIALIZER  5346  SHOULD BE 37
467                                                          CHECK COUNTERS  5362 IS 2    5375 IS 10
470                                                        N LOCATION  5263  HAS RANGE 37-30,  17-10
471                                                             THIS IS ZERO INDICATOR (BIT 3)
472                                                       2. S-REGISTER IS 60
473                                                          DESIGNATOR IS 6
474                                                        CHECK LOCATIONS  5262  5263  SHOULD BE EQUAL
475                                                         IF NOT EQUAL SDR DOES NOT WORK
476   05162  36 0 201   TEST10 RJP A1
477   05163  06 0 262          SDR SAVE
500   05164  32 0 262          ENL SAVE
501   05165  11 0 263          SUB TEMP
502   05166  20 0 167          ZJP L+2
503   05167  24 0 311          JMP ERR060
504   05170  36 0 214          RJP A2
505   05171  36 0 201          RJP A1
506                                                  SDR (7)
507   05172     07262          BMNE 7,,262
510   05173  32 0 262          ENL SAVE
511   05174  11 0 263          SUB TEMP
512   05175  20 0 176          ZJP L+2
513   05176  24 1 347  J       JMP ERR070
514   05177  36 0 214          RJP A2
515   05200  24 0 227          JMP TEST11
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
516                                    EJE
517   05201      00000    A1          ...
520   05202   32 0 346    J          8ENL 37)
521   05203   37 0 263               STL TEMP
522   05204   32 0 362               8ENL 2)
523   05205   37 0 261               STL INDEXB
524   05206   32 0 375    JMP10A     8ENL 10)
525   05207   37 0 267               STL INDEXA
526   05210   05 0 263    JMP10B     EDR TEMP
527   05211   20 0 212               ZJP L+2
530   05212   24 0 314               JMP ERR201
531   05213   24 1 201               RTN
532   05214      00000    A2          ...
533   05215   01 0 263               DCR TEMP
534                                  DSK INDEXA,JMP10C,JMP10B
534   05216   01 0 267               DCR INDEXA
534   05217   20 0 220               ZJP JMP10C
534   05220   24 0 207               JMP JMP10B
535   05221   32 0 263    JMP10C     ENL TEMP
536   05222   11 0 375               8SUB 10)
537   05223   37 0 263               STL TEMP
540                                  DSK INDEXB,RTN,JMP10A
540   05224   01 0 261               DCR INDEXB
540   05225   20 0 226               ZJP RTN
540   05226   24 0 205               JMP JMP10A
541   05227   24 1 214    RTN        RTN
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
542                                EJE
543                                          TEST 11  PJP
544
545                                          ENTER DESIGNATOR WITH POSITIVE INDICATORS AND PJP
546                                          IF STOP OCCURS DESIGNATOR IS 27
547                                                1. S-REGISTER IS 270
550                                                   INITIAL CHECK - ENTER DESIGNATOR WITH ZERO
551                                                   AND POSITIVE JUMP TO STOP
552                                                   CHECK LOCATION 5373  SHOULD BE ZERO
553                                                   IF ZERO, PJP OCCURS WITHOUT PROPER INDICATOR
554                                                2. S-REGISTER IS 271
555                                                  CHECK INITIALIZER  5345  SHOULD BE 77
556                                                  CHECK COUNTERS  5344  IS 7  5343  IS 4
557                                                  POSITIVE INDICATOR (BIT 2)  5863
560                                                   IF BIT 2 ON  PJP DOES NOT WORK
561   05230  05 0 373   TEST11 EDR 0)
562   05231  27 0 322          PJP ERR270
563   05232  32 0 345  J      8ENL 77)
564   05233  37 0 263          STL TEMP
565   05234  32 0 344  J       ENL 7)
566   05235  37 0 261          STL INDEXB
567   05236  32 0 343  JJMP11A ENL 4)
570   05237  37 0 267          STL INDEXA
571   05240  05 0 263   JMP11B EDR TEMP
572   05241  27 0 242          PJP L+2
573   05242  24 0 317          JMP ERR271
574   05243  01 0 263          DCR TEMP
575                             DSK INDEXA,JMP11C,JMP11B
576   05244  01 0 267          DCR INDEXA
575   05245  20 0 246          ZJP JMP11C
575   05246  24 0 237          JMP JMP11B
576   05247  32 0 263   JMP11C ENL TEMP
577   05250  11 0 343          SUB 4)
600   05251  37 0 263          STL TEMP
601                             DSK INDEXB,TEST12,JMP11A
601   05252  01 0 261          DCR INDEXB
601   05253  20 1 342  J       ZJP TEST12
601   05254  24 0 235          JMP JMP11A
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
602                                     EJE
603   05255       00000   STOPCK ,,,
604   05256  05 0 341  /       8EDR 36)
605   05257       04004             MNE 4,,4
606   05260  24 1 255             RTN
607
610   05261       00000   INDEXB OCT 0
611   05262       00000   SAVE   OCT 0
612   05263       00000   TEMP   OCT 0
613   05264       00000   TEMPA  OCT 0
614   05265       00000   TEMPB  OCT 0
615   05266       00000   INDEX  OCT 0
616   05267       00000   INDEXA OCT 0
617                       ERR2008ERR 20),200,TEST04
617   05270  05 0 374             EDR 20)
617   05271  00 0 200             STP 200
617   05272  24 0 015             JMP TEST04
620                       ERR3208ERR 32),320,TEST06
620   05273  05 0 340  /       EDR 32)
620   05274  00 0 320             STP 320
620   05275  24 0 024             JMP TEST06
621                       ERR1108ERR 11),110,TEST07
621   05276  05 0 337  /       EDR 11)
621   05277  00 0 110             STP 110
621   05300  24 0 034             JMP TEST07
622                       ERR3708ERR 37),370,TEST7A
622   05301  05 0 346             EDR 37)
622   05302  00 0 370             STP 370
622   05303  24 0 041             JMP TEST7A
623                       ERR0108ERR 1),10,TEST09
623   05304  05 0 364             EDR 1)
623   05305  00 0 010             STP 10
623   05306  24 0 144             JMP TEST09
624                       ERR3718ERR 37),371,TEST10
624   05307  05 0 346             EDR 37)
624   05310  00 0 371             STP 371
624   05311  24 0 161             JMP TEST10
625                       ERR0608ERR 6),60,TEST11
625   05312  05 0 336  /       EDR 6)
625   05313  00 0 060             STP 60
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
625   05314  24 0 227          JMP TEST11
626                        ERR2018ERR 20),201,TEST11
626   05315  05 0 374          EDR 20)
626   05316  00 0 201          STP 201
626   05317  24 0 227          JMP TEST11
627                        ERR2718ERR 27),271,TEST12
627   05320  05 0 335  ✓       EDR 27)
627   05321  00 0 271          STP 271
627   05322  24 1 342          JMP TEST12
630                        ERR2708ERR 27),270,TEST12
630   05323  05 0 335          EDR 27)
630   05324  00 0 270          STP 270
630   05325  24 1 342          JMP TEST12
631                        ERR3308ERR 33),330,TEST06
631   05326  05 0 334  ✓       EDR 33)
631   05327  00 0 330          STP 330
631   05330  24 0 024          JMP TEST06
632                        ERR1118ERR 11),111,TEST09
632   05331  05 0 337          EDR 11)
632   05332  00 0 111          STP 111
632   05333  24 0 144          JMP TEST09
      05334     00033          WRD
      05335     00027          WRD
      05336     00006          WRD
      05337     00011          WRD
      05340     00032          WRD
      05341     00036          WRD
      05342     05421          WRD
      05343     00004          WRD
      05344     00007          WRD
      05345     00077          WRD
      05346     00037          WRD
      05347     05416          WRD
      05350     20000          WRD
      05351     10000          WRD
      05352     05413          WRD
      05353     25252          WRD
      05354     05410          WRD
      05355     12525          WRD
      05356     05405          WRD
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

05357	05402	WRD
05360	37777	WRD
05361	00003	WRD
05362	00002	WRD
05363	27776	WRD
05364	00001	WRD
05365	07776	WRD
05366	17776	WRD
05367	37776	WRD
05370	16301	WRD
05371	00101	WRD
05372	21476	WRD
05373	00000	WRD
05374	00020	WRD
05375	00010	WRD
05376	00024	WRD
05377	00005	WRD

PROJECT NO. 530053 PROGRAMMER J.E. [illegible] TAPE NUMBER 345116

```
633                                ERR1128ERR 11),112,TEST09
633   05400   05 0 377  /              EDR 11)
633   05401   00 0 112                 STP 112
633   05402   24 1 375  /              JMP TEST09
634                                ERR1138ERR 11),113,TEST09
634   05403   05 0 377                 EDR 11)
634   05404   00 0 113                 STP 113
634   05405   24 1 376                 JMP TEST09
635                                ERR1148ERR 11),,114,TEST09
635   05406   05 0 377                 EDR 11)
635   05407   00 0 114                 STP 114
635   05410   24 1 376                 JMP TEST09
636                                ERR1158ERR 11),115,TEST09
636   05411   05 0 377                 EDR 11)
636   05412   00 0 115                 STP 115
636   05413   24 1 376                 JMP TEST09
637                                ERR1168ERR 11),116,TEST09
637   05414   05 0 377                 EDR 11)
637   05415   00 0 116                 STP 116
637   05416   24 1 376                 JMP TEST09
640                                ERR0708ERR 07),070,TEST11
640   05417   05 0 375  /              EDR 07)
640   05420   00 0 070                 STP 070
640   05421   24 1 374  /              JMP TEST11
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
641                                     EJE
642                                                 TEST 12  SMB
643
644                                                 ENTER ACCUMULATOR WITH NUMBER N (20000-1)
645                                                 SET MOST SIGNIFICANT BIT OF N, POSITIVE JUMP
646                                                 IF STOP OCCURS
647                                                       1, S-REGISTER IS 30
650                                                       2, DESIGNATOR IS 3
651                                                       3, CHECK ACCUMULATOR 101 SHOULD BE NEGATIVE
652                                                          IF POSITIVE SMB DOES NOT WORK
653   05422   32 0 373  JTEST12ENL 20000)
654   05423   37 1 372  J       STL TEMP
655   05424   37 1 371  J       STL INDEX
656   05425   32 1 372    JMP12A ENL TEMP
657   05426   03 1 370  J       SMB ACC
660   05427   27 0 267          PJP ERR030
661   05430   01 1 372          DCR TEMP
662                             DSK INDEX,TEST13,JMP12A
662   05431   01 1 371          DCR INDEX
662   05432   20 0 033          ZJP TEST13
662   05433   24 0 024          JMP JMP12A
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
663                                 EJE
664                                             TEST 13  CMB
665
666                                             SET MOST SIGNIFICANT BIT OF NUMBER N, IF POSITIVE STOP
667                                             CLEAR MOST SIGNIFICANT BIT OF N, POSITIVE JUMP
670                                             IF STOP OCCURS
671                                                   1. S-REGISTER IS 31
672                                                      DESIGNATOR IS 3
673                                                     CHECK LOCATION  5263  SHOULD BE NEGATIVE
674                                                      IF POSITIVE SMB DOES NOT WORK
675                                                   2. S-REGISTER IS 20
676                                                      DESIGNATOR IS 2
677                                                     CHECK LOCATION  5263  SHOULD BE POSITIVE
700                                                      IF NEGATIVE CMB DOES NOT WORK
701   05434   32 0 367  JTEST13BENL 30000)
702   05435   37 1 372          STL TEMP
703   05436   32 0 373         BENL 20000)
704   05437   37 1 371          STL INDEX
705   05440   03 1 372   JMP13A SMB TEMP
706   05441   27 0 275          PJP ERR031
707   05442   02 1 372          CMB TEMP
710   05443   27 0 044          PJP L+2
711   05444   24 0 272          JMP ERR020
712   05445   01 1 372          DCR TEMP
713                             DSK INDEX,TST14A,JMP13A
713   05446   01 1 371          DCR INDEX
713   05447   20 0 050          ZJP TST14A
713   05450   24 0 037          JMP JMP13A
```

```
714                                     SUBR
715                                             TEST 14A   ADD
716
717                                                          ACC      Y      RESULT      ERROR
720
721   05451   32 0 156  JTST14A  SNL 0)                    +0      +0       +0          120
722   05452   12 0 357           AND 0)
723   05453   20 0 0             SZJP L+2
724   05454   24 0 3             JMP ERR120
725   05455   27 0 0             SKP L+2
726   05456   24 0 3             JMP L-2
727   05457   32 0 36            SNL 0)                    +0      -0       +0          121
730   05460   12 0 36            AND -0)
731   05461   20 0 0             SZJP L+2
732   05462   24 0 3             JMP ERR121
733   05463   27 0 0             SKP L+2
734   05464   24 0 3             JMP L-2
735   05465   32 0 3             SNL -0)                   -0      +0       +0          122
736   05466   12 0 3             AND 0)
737   05467   20 0 0             SZJP L+2
740   05470   24 0 3             JMP ERR122
741   05471   27 0 0             SKP L+2
742   05472   24 0 0             JMP L-2
743   05473   32 0 3             SNL -0)                   -0      -0       -0          123
744   05474   12 0 3             AND -0)
745   05475   20 0 0             SZJP L+2
746   05476   24 0 3             JMP ERR123
747   05477   27 0 0             SKP L-1
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
 750                                    EJE
 751                                              TEST 148   EOR
 752
 753                                                        ACC      Y      RESULT      ERROR
 754
 755   05500   32 0 366   TST148 ENL 0)                     +0      +0       +0          130
 756   05501   13 0 366          EOR 0)
 757   05502   20 0 103          ZJP L+2
 760   05503   24 0 314          JMP ERR130
 761   05504   27 0 105          PJP L+2
 762   05505   24 0 102          JMP L-2
 763   05506   32 0 366          ENL 0)                    +0      -0       -0          131
 764   05507   13 0 365          EOR -0)
 765   05510   20 0 111          ZJP L+2
 766   05511   24 0 317          JMP ERR131
 767   05512   27 0 110          PJP L-1
 770   05513   32 0 365          ENL -0)                   -0      +0       -0          132
 771   05514   13 0 366          EOR 0)
 772   05515   20 0 116          ZJP L+2
 773   05516   24 0 322          JMP ERR132
 774   05517   27 0 115          PJP L-1
 775   05520   32 0 365          ENL -0)                   -0      -0       +0          133
 776   05521   13 0 365          EOR -0)
 777   05522   20 0 123          ZJP L+2
1000   05523   24 0 325          JMP ERR133
1001   05524   27 0 125          PJP L+2
1002   05525   24 0 122          JMP L-2
```

PROJECT NO. 530053 PROGRAMMER L.E. PHILLIPPI TAPE NUMBER 345116

```
1003                                    EJE
1004                                              TEST 15  ADD
1005
1006                                                        ACC      Y      RESULT      ERROR
1007
1010   05526   32 0 366    TST15A ENL 0)                    +0      +0       +0          100
1011   05527   10 0 366           ADD 0)
1012   05530   20 0 151           ZJP L+2
1013   05531   24 0 330           JMP ERR100
1014   05532   27 0 153           PJP L+2
1015   05533   24 0 330           JMP L-2
1016   05534   32 0 366           ENL 0)                    +0      -0       -0          101
1017   05535   10 0 365           ADD -0)
1020   05536   20 0 157           ZJP L+2
1021   05537   24 0 331           JMP ERR101
1022   05540   27 0 156           PJP L-1
1023   05541   32 0 365           ENL -0)                   -0      +0       -0          102
1024   05542   10 0 366           ADD 0)
1025   05543   20 0 144           ZJP L+2
1026   05544   24 0 332           JMP ERR102
1027   05545   27 0 143           PJP L-1
1030   05546   32 0 365           ENL -0)                   -0      -0       -0          103
1031   05547   10 0 365           ADD -0)
1032   05550   20 0 151           ZJP L+2
1033   05551   24 1 364    J      JMP ERR103
1034   05552   27 0 150           PJP L-1
1035   05553   32 0 363    J      8ENL 12525)               +N      -N       -0          104
1036   05554   10 0 362    J      8ADD 25252)
1037   05555   20 0 156           ZJP L+2
1040   05556   24 1 361    J      JMP ERR104
1041   05557   27 0 155           PJP L-1
1042   05560   32 0 362           8ENL 25252)               -N      +N       -0          105
1043   05561   10 0 363           8ADD 12525)
1044   05562   20 0 163           ZJP L+2
1045   05563   24 1 360    J      JMP ERR105
1046   05564   27 0 162           PJP L-1
```

```
1047                                    EJE
1050   05565     07414   T              UCT TABLE
1051
1052                                                TEST 15B ADD
1053
1054                                                ADDER TEST
1055
1056                                                00000 + 37776 = 37776        12525 + 12525 = 25252
1057                                                00001 + 37777 = 00001        25252 + 25252 = 12525
1060                                                37775 + 00000 = 37775        00002 + 00001 = 00003
1061                                                37777 + 00002 = 00002        37776 + 37775 = 37774
1062                                                IF STOP OCCURS
1063                                                      1. S-REGISTER IS 102
1064                                                      2. DESIGNATOR IS 10
1065                                                      3. LOCATION  5624  IS ADDRESS A OF SUM
1066                                                         A+2 AND A+1 ARE THE NUMBERS ADDED
1067                                                         CHECK LISTING FOR CORRECT VALUES
1070                                                      4. IF VALUES ARE WRONG, ADD DOES NOT WORK
1071   05566   32 0 165   TST15B ENL T
1072   05567   37 0 224          STL TAB
1073   05570   32 0 357   J      ENL 8)
1074   05571   37 1 371          STL INDEX
1075   05572   32 1 224   JMP15C ENL TAB,I
1076   05573   01 0 224          DCR TAB
1077   05574   10 1 224          ADD TAB,I
1100   05575   01 0 224          DCR TAB
1101   05576   13 1 224          EOR TAB,I
1102   05577   27 0 200          PJP L+2
1103   05600   24 0 201          JMP L+2
1104   05601   20 0 202          ZJP L+2
1105   05602   24 1 356   J      JMP ERR106
1106   05603   01 0 224          DCR TAB
1107   05604   01 1 371          DCR INDEX
1110   05605   27 0 171          PJP JMP15C
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
1111                                    EJE
1112                                                TEST 16  CJP
1113
1114                                                ENTER DESIGNATOR WITH CARRY INDICATORS AND CARRY JUMP
1115                                                IF STOP OCCURS DESIGNATOR IS 25
1116                                                      1, S-REGISTER IS 250
1117                                                         INITIAL CHECK - ENTER DESIGNATOR WITH ZERO
1120                                                         AND CARRY JUMP TO ERROR STOP
1121                                                       CHECK LOCATION  5766  SHOULD BE ZERO
1122                                                        IF ZERO, CJP OCCURS WITHOUT PROPER INDICATOR
1123                                                      2, S-REGISTER IS 251
1124                                                       CHECK INITIALIZER  5754  SHOULD BE 77
1125                                                       CHECK COUNTER  5753  SHOULD BE 32
1126                                                       CARRY INDICATOR (BIT 0)  5263
1127                                                        IF BIT 0 IS ON CJP DOES NOT WORK
1130   05606  05 0 366   TEST16 EDR 0)
1131   05607  25 1 355  J       CJP ERR250
1132   05610  32 0 354  J      BENL 77)
1133   05611  37 1 372          STL TEMP
1134   05612  32 0 353  J       ENL 32)
1135   05613  37 1 371          STL INDEX
1136   05614  05 1 372   JMP16A EDR TEMP
1137   05615  25 0 216          CJP L+2
1140   05616  24 1 352  J       JMP ERR251
1141   05617  01 1 372          DCR TEMP
1142   05620  01 1 372          DCR TEMP
1143                             DSK INDEX,TEST17,JMP16A
1143   05621  01 1 371          DCR INDEX
1143   05622  20 0 224          CJP TEST17
1143   05623  24 0 213          JMP JMP16A
1144   05624     00000   TAB     OCT 0
```

PROJECT NO. 530053 PROGRAMMER J E. PHILLIPPI TAPE NUMBER 345116

```
1145                                EJE
1146                                          TEST 17  LSH
1147
1150                                          LEFT SHIFT NUMBER N, N=25252, END AROUND CARRY JUMP TO
1151                                          LEFT SHIFT N, N=12525, RESULT IS 25252
1152                                          IF STOP OCCURS
1153                                                1. S-REGISTER IS 140
1154                                                2. DESIGNATOR IS 14
1155                                                3. CHECK LOCATION  5762  SHOULD BE 25252
1156                                                4. CHECK M  5263  SHOULD BE 25252
1157                                                   IF NOT LSH DOES NOT WORK
1160   05625  32 0 351  JTEST178ENL 10000)
1161   05626  37 1 371          STL INDEX
1162   05627  32 0 362         8ENL 25252)
1163   05630  37 1 372          STL TEMP
1164   05631  14 1 372   JMP17A LSH TEMP
1165   05632  25 0 230          CJP JMP17A
1166   05633  32 1 372          ENL TEMP
1167   05634  11 0 362         8SUB 25252)
1170   05635  20 0 236          ZJP L+2
1171   05636  24 1 350  J        JMP ERR140
```

```
1172                                    EJE
1173                                            TEST 17A   LSH (14)
1174
1175                                                        Y      RESULT      ERROR
1176
1177   05637  32 0 365    TST17A ENL -0)                   -0       -0          141
1200   05640  14 1 370           LSH ACC
1201   05641  20 0 242           ZJP L+2
1202   05642  24 1 347  J        JMP ERR141
1203   05643  27 0 241           PJP L-1
1204   05644  32 0 366           ENL 0)                   +0       +0          142
1205   05645  14 1 370           LSH ACC
1206   05646  20 0 247           ZJP L+2
1207   05647  24 1 345  J        JMP ERR142
1210   05650  27 0 251           PJP L+2
1211   05651  24 0 246           JMP L-2
1212                                            TEST 17B   LSH (15)
1213
1214                                                        Y      RESULT      ERROR
1215
1216   05652  32 0 366    TST17B ENL 0)                   +0       +0          151
1217   05653     15770           BMNE 15,1,370
1220   05654  20 0 255           ZJP L+2
1221   05655  24 1 345  J        JMP ERR151
1222   05656  27 0 257           PJP L+2
1223   05657  24 0 254           JMP L-2
1224   05660  32 0 365           ENL -0)                  -0       -0          152
1225   05661     15770           BMNE 15,1,370
1226   05662  20 0 263           ZJP L+2
1227   05663  24 1 344  J        JMP ERR152
1230   05664  27 0 262           PJP L-1
1231                              DSK INDEX,TEST18,JMP17A
1231   05665  01 1 371           DCR INDEX
1231   05666  20 1 343  J        ZJP TEST18
1231   05667  24 0 230           JMP JMP17A
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
1232                                    EJE
1233                                ERR0308ERR 3),30,TEST13
1233   05670   05 0 342  ✓              EDR 3)
1233   05671   00 0 030                  STP 30
1233   05672   24 0 033                  JMP TEST13
1234                                ERR0208ERR 2),20,TST14A
1234   05673   05 0 341  ✓              EDR 2)
1234   05674   00 0 020                  STP 20
1234   05675   24 0 050                  JMP TST14A
1235                                ERR0318ERR 3),31,TST14A
1235   05676   05 0 342                  EDR 3)
1235   05677   00 0 031                  STP 31
1235   05700   24 0 050                  JMP TST14A
1236                                ERR1208ERR 12),120,TST15A
1236   05701   05 0 340  ✓              EDR 12)
1236   05702   00 0 120                  STP 120
1236   05703   24 0 125                  JMP TST15A
1237                                ERR1218ERR 12),121,TST15A
1237   05704   05 0 340                  EDR 12)
1237   05705   00 0 121                  STP 121
1237   05706   24 0 125                  JMP TST15A
1240                                ERR1228ERR 12),122,TST15A
1240   05707   05 0 340                  EDR 12)
1240   05710   00 0 122                  STP 122
1240   05711   24 0 125                  JMP TST15A
1241                                ERR1238ERR 12),123,TST15A
1241   05712   05 0 340                  EDR 12)
1241   05713   00 0 123                  STP 123
1241   05714   24 0 125                  JMP TST15A
1242                                ERR1308ERR 13),130,TST15A
1242   05715   05 0 337  ✓              EDR 13)
1242   05716   00 0 130                  STP 130
1242   05717   24 0 125                  JMP TST15A
1243                                ERR1318ERR 13),131,TST15A
1243   05720   05 0 337                  EDR 13)
1243   05721   00 0 131                  STP 131
1243   05722   24 0 125                  JMP TST15A
1244                                ERR1328ERR 13),132,TST15A
1244   05723   05 0 337                  EDR 13)
1244   05724   00 0 132                  STP 132
```

PROJECT NO 530053 PROGRAMMER J E. PHILLIPPI TAPE NUMBER 345116

```
1244   05725  24 0 125          JMP TST15A
1245                        ERR1538ERR 13),1,TST15A
1245   05726  05 0 337          EDR 13)
1245   05727  00 0 133          STP 133
1245   05730  24 0 125          JMP TST15A
1246                        ERR1008ERR 10),100,TST15B
1246   05731  05 0 357          EDR 10)
1246   05732  00 0 100          STP 100
1246   05733  24 0 165          JMP TST15B
1247                        ERR1018ERR 10),101,TST15B
1247   05734  05 0 357          EDR 10)
1247   05735  00 0 101          STP 101
1247   05736  24 0 165          JMP TST15B
       05737      00013         WRD
       05740      00012         WRD
       05741      00002         WRD
       05742      00003         WRD
       05743      06043         WRD
       05744      06027         WRD
       05745      06024         WRD
       05746      06021         WRD
       05747      06016         WRD
       05750      06040         WRD
       05751      10000         WRD
       05752      06032         WRD
       05753      00040         WRD
       05754      00077         WRD
       05755      06035         WRD
       05756      06013         WRD
       05757      00010         WRD
       05760      06010         WRD
       05761      06005         WRD
       05762      25252         WRD
       05763      12525         WRD
       05764      06002         WRD
       05765      37777         WRD
       05766      00000         WRD
       05767      30000         WRD
       05770      00101         WRD
       05771      05266         WRD
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

05772	05263	WRD
05773	20000	WRD
05774	05227	WRD
05775	00007	WRD
05776	05144	WRD
05777	00011	WRD

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPS[illegible] NUMBER 345116

```
1250                          ERR1028ERR 10),102,TST15B
1250    06000  05 0 377  J          EDR 10)
1250    06001  00 0 102             STP 102
1250    06002  24 1 376  J          JMP TST15B
1251                          ERR1038ERR 10),103,TST15B
1251    06003  05 0 377             EDR 10)
1251    06004  00 0 103             STP 103
1251    06005  24 1 376             JMP TST15
1252                          ERR1048ERR 10),104,TST15B
1252    06006  05 0 377             EDR 10)
1252    06007  00 0 104             STP 104
1252    06010  24 1 376             JMP TST15B
1253                          ERR1058ERR 10,)105,TST15B
1253    06011  05 1 377             EDR 10
1253    06012  00 0 102  J          STP )105
1253    06013  24 1 376             JMP TST15B
1254                          ERR1068ERR 10),106,TST15
1254    06014  05 0 377             EDR 10)
1254    06015  00 0 106             STP 106
1254    06016  24 1 374  J          JMP TEST16
1255                          ERR1418ERR 14),141,TST17B
1255    06017  05 0 373  J          EDR 14)
1255    06020  00 0 141             STP 141
1255    06021  24 1 372  J          JMP TST17B
1256                          ERR1428ERR 14),142,TST17B
1256    06022  05 0 373             EDR 14)
1256    06023  00 0 142             STP 142
1256    06024  24 1 372             JMP TST17B
1257                          ERR1518ERR 15),151,TEST18
1257    06025  05 0 371  J          EDR 15)
1257    06026  00 0 151             STP 151
1257    06027  24 0 043             JMP TEST18
1260                          ERR1528ERR 15),152,TEST18
1260    06030  05 0 371             EDR 15)
1260    06031  00 0 152             STP 152
1260    06032  24 0 043             JMP TEST18
1261                          ERR2518ERR 25),251,TEST17
1261    06033  05 0 370  J          EDR 25)
1261    06034  00 0 251             STP 251
1261    06035  24 1 367  J          JMP TEST17
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
1262                          ERR2508ERR 25),250,TEST17
1262    06036  05 0 370              EDR 25)
1262    06037  00 0 250              STP 250
1262    06040  24 1 367              JMP TEST17
1263                          ERR1408ERR 14),140,TEST18
1263    06041  05 0 373              EDR 14)
1263    06042  00 0 140              STP 140
1263    06043  24 0 043              JMP TEST18
```

```
1264                                    SUB
1265                                                TEST 8  RSH
1266
1267                                                RIGHT SHIFT NUMBER N, N=25252, (32525) LEFT SHIFT
1270                                                (25253), LOGICAL AND WITH 37776 (25252), SUBTRACT N
1271                                                IF STOP OCCURS
1272                                                      1. S-REGISTER IS 160
1273                                                      2. DESIGNATOR IS 16
1274                                                      3. CHECK LOCATION  6363  SHOULD BE 25252
1275                                                      4. CHECK LOCATION  6361  SHOULD BE 37776
1276                                                      5. CHECK LOCATION  5263  SHOULD BE 25253
1277                                                         ACCUMULATOR SHOULD BE ZERO
1300                                                      6. RSH DOES NOT WORK
1301    06044   32 0 366  JTEST188ENL 10000)
1302    06045   37 1 365  J       STL INDEXA
1303    06046   37 1 364  J       STL INDEXB
1304    06047   32 0 363  J      8ENL 25252)
1305    06050   37 1 362  J       STL TEMP
1306    06051   16 1 362    JMP18A RSH TEMP
1307    06052   14 1 362           LSH TEMP
1310    06053   32 1 362           ENL TEMP
1311    06054   12 0 361  J      8AND 37776)
1312    06055   11 0 363           8SUB 25252)
1313    06056   20 0 057           ZJP L+2
1314    06057   24 0 274           JMP ERR160
1315                               DSK INDEXA,JMP18B,JMP18A
1315    06060   01 1 365           DCR INDEXA
1315    06061   20 0 062           ZJP JMP18B
1315    06062   24 0 050           JMP JMP18A
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
1316                                    EJE
1317                                                SIMILARLY, RIGHT SHIFT N, N=12525
1320                                                      IF STOP OCCURS
1321                                                      1. S-REGISTER IS 161
1322                                                      2. CHECK LOCATION  6360  SHOULD BE 12525
1323                                                      3. CHECK LOCATION  6357  SHOULD BE 1
1324                                                      4. CHECK LOCATION  5263  SHOULD BE 12524
1325                                                         ACCUMULATOR SHOULD BE ZERO
1326                                                      5. RSH DOES NOT WORK
1327   06063   32 0 360  JJMP1888ENL 12525)
1330   06064   37 1 362          SIL TEMP
1331   06065   16 1 362   JMP18C RSH TEMP
1332   06066   14 1 362          LSH TEMP
1333   06067   32 1 362          ENL TEMP
1334   06070   13 0 357  J       EOR 1)
1335   06071   11 0 360         BSUB 12525)
1336   06072   20 0 073          ZJP L+2
1337   06073   24 0 277          JMP ERR161
```

PROJECT NO. 530853 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
1340                                    EJE
1341                                              TEST 18A   RSH (16)
1342
1343                                                          Y      RESULT      ERROR
1344
1345   06074   32 0 3?5    TST18A ENL 0)                     +0       +0          162
1346   06075   16 1 356  ✓        RSH ACC
1347   06076   20 0 077            ZJP L+2
1350   06077   24 0 244            JMP ERR162
1351   06100   27 0 101            PJP L+2
1352   06101   24 0 076            JMP L-2
1353   06102   32 0 357            ENL 1)                    +1       +0          163
1354   06103   16 1 356            RSH ACC
1355   06104   20 0 105            ZJP L+2
1356   06105   24 0 247            JMP ERR163
1357   06106   27 0 107            PJP L+2
1360   06107   24 0 104            JMP L-2
1361   06110   32 0 355  ✓        ENL -0)                   -0       -0          164
1362   06111   16 1 356            RSH ACC
1363   06112   20 0 113            ZJP L+2
1364   06113   24 0 252            JMP ERR164
1365   06114   27 0 112            PJP L-1
1366   06115   32 0 361            ENL -1)                   -1       -0          165
1367   06116   16 1 356            RSH ACC
1370   06117   20 0 120            ZJP L+2
1371   06120   24 0 255            JMP ERR165
1372   06121   27 0 117            PJP L-1
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
1373                                EJE
1374                                        TEST 18B   RSH (17)
1375
1376                                                    Y      RESULT      ERROR
1377
1400   06122  32 0 375   TST18B ENL 0)                 +0       +0          171
1401   06123     17756          BMNE 17,1,356
1402   06124  20 0 125           ZJP L+2
1403   06125  24 0 260           JMP ERR171
1404   06126  27 0 127           PJP L+2
1405   06127  24 0 124           JMP L-2
1406   06130  32 0 357           ENL 1)                 +1       +0          172
1407   06131     17756          BMNE 17,1,356
1410   06132  20 0 133           ZJP L+2
1411   06133  24 0 263           JMP ERR172
1412   06134  27 0 135           PJP L+2
1413   06135  24 0 132           JMP L-2
1414   06136  32 0 355           ENL -0)                -0       -0          173
1415   06137     17756          BMNE 17,1,356
1416   06140  20 0 141           ZJP L+2
1417   06141  24 0 266           JMP ERR173
1420   06142  27 0 140           PJP L-1
1421   06143  32 0 361           ENL -1)                -1       -0          174
1422   06144     17756          BMNE 17,1,356
1423   06145  20 0 146           ZJP L+2
1424   06146  24 0 271           JMP ERR174
1425   06147  27 0 145           PJP L-1
1426                              DSK INDEXB,TEST19,JMP18C
1426   06150  01 1 364           DCR INDEXB
1426   06151  20 0 152           ZJP TEST19
1426   06152  24 0 064           JMP JMP18C
```

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```
1427                                    EJE
1430                                                TEST 19  EJP
1431
1432                                                ENTER DESIGNATOR WITH EVEN INDICATORS AND EVEN JUMP
1433                                                IF STOP OCCURS DESIGNATOR IS 21
1434                                                      1. S-REGISTER IS 210
1435                                                         INITIAL CHECK - ENTER DESIGNATOR WITH ZERO
1436                                                         AND EVEN JUMP TO ERROR STOP
1437                                                        CHECK LOCATION  6375  SHOULD BE ZERO
1440                                                         IF ZERO, EJP OCCURS WITHOUT PROPER INDICATOR
1441                                                      2. S-REGISTER IS 211
1442                                                        CHECK INITIALIZER  6352  SHOULD BE 37
1443                                                        CHECK COUNTER  6354  IS 16
1444                                                        EVEN INDICATOR (BIT 4)  5263
1445                                                         IF BIT 4 ON EJP DOES NOT WORK
1446   06153  05 0 375   TEST19 EDR 0)
1447   06154  21 0 302          EJP ERR210
1450   06155  32 0 354  ✓       ENL 16)
1451   06156  37 1 353  ✓       STL INDEX
1452   06157  32 0 352  ✓      8ENL 37)
1453   06160  37 1 362          STL TEMP
1454   06161  05 1 362   JMP19A EDR TEMP
1455   06162  21 0 163          EJP L+2
1456   06163  24 0 305          JMP ERR211
1457   06164  01 1 362          DCR TEMP
1460                             DSK INDEX,TST19A,JMP19A
1460   06165  01 1 353          DCR INDEX
1460   06166  20 0 167          ZJP TST19A
1460   06167  24 0 160          JMP JMP19A
```

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```
1461                                    EJE
1462                                                TEST 19A OJP
1463
1464                                                ENTER DESIGNATOR WITH OVERFLOW INDICATOR AND OJP
1465                                                IF STOP OCCURS DESIGNATOR IS 26
1466                                                      1. S-REGISTER IS 260
1467                                                         INITIAL CHECK - ENTER DESIGNATOR WITH ZERO
1470                                                         AND OVERFLOW JUMP TO ERROR STOP
1471                                                       CHECK LOCATION  6375  SHOULD BE ZERO
1472                                                         IF ZERO, OJP OCCURS WITHOUT PROPER INDICATOR
1473                                                      2. S=REGISTER IS 261
1474                                                       CHECK INITIALIZER  6352  SHOULD BE 37
1475                                                       CHECK COUNTERS  6377  IS 8   6351 IS 2
1476                                                       OVERFLOW INDICATOR  (+IT 1)  5263
1477                                                         IF BIT 1 ON  OJP DOES NOT WORK
1500   06170   05 0 375   TST19A EDR 0)
1501   06171   26 0 310         OJP ERR260
1502   06172   32 0 377         ENL 8)
1503   06173   37 1 364         STL INDEXB
1504   06174   32 0 352        8ENL 37)
1505   06175   37 1 362         STL TEMP
1506   06176   32 0 351  JUMP19B ENL 2)
1507   06177   37 1 365         STL INDEXA
1510   06200   05 1 362   JMP19C EDR TEMP
1511   06201   26 0 202         OJP L+2
1512   06202   24 0 313         JMP ERR261
1513   06203   01 1 362         DCR TEMP
1514   06204   01 1 365         DCR INDEXA
1515   06205   27 0 177         PJP JMP19C
1516   06206   32 1 362         ENL TEMP
1517   06207   11 0 351         SUB 2)
1520   06210   37 1 362         STL TEMP
1521   06211   01 1 364         DCR INDEXB
1522   06212   27 0 175         PJP JMP19B
1523   06213   24 1 350  J      JMP TEST20
```

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```
1524                                    EJE
1525                                                TEST 24
1526
1527                                                CHECK DESIGNATOR SETTINGS BY LEFT SHIFT ALTERNATE ONES-
1530                                                      OVERFLOW IS SET
1531                                                      EVEN NOT SET
1532                                                      ZERO NOT SET
1533                                                      IF CARRY THEN ALSO POSITIVE SET OR NOT SET
1534                                                IF STOP OCCURS
1535                                                        CHECK LOCATION  6363  SHOULD BE 25252
1536   06214  32 0 366   TEST248ENL 10000)
1537   06215  37 1 3[illegible]        STL INDEX
1540   06216  36 1 34[illegible]  ✓     RJP DSIGCK
1541   06217  32 0 363              BENL 25252)
1542   06220  14 1 356   JMP24A LSH ACC
1543   06221  26 0 [illegible]          OJP L+2
1544   06222  24 0 327                  JMP ERR143
1545   06223  21 0 321                  EJP ERR144
1546   06224  20 0 316                  ZJP ERR145
1547   06225  25 0 226                  CJP L+2
1550   06226  24 0 230                  JMP L+3
1551   06227  27 0 230                  PJP L+2
1552   06230  24 0 324                  JMP ERR146
1553                                    DSK INDEX,TEST25,JMP24A
1553   06231  01 1 353                  DCR INDEX
1553   06232  20 0 233                  ZJP TEST25
1553   06233  24 0 217                  JMP JMP24A
```

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```
1554                                    EJE
1555                                                TEST 25  CLJ-SLJ
1556
1557                                                SET LOCKOUT AND JUMP, CLEAR LOCKOUT AND JUMP
1560                                                IF STOP OCCURS JUMPS DID NOT OCCUR
1561                                                      1. S-REGISTER IS 221   SLJ DOES NOT WORK
1562                                                      2. S-REGISTER IS 231   CLJ DOES NOT WORK
1563   06234  32 0 346  JTEST25 ENL 3)
1564   06235  37 1 353           STL INDEX
1565   06236  22 0 237   JMP25A SLJ L+2
1566   06237  24 0 332           JMP ERR221
1567   06240  23 0 241           CLJ L+2
1570   06241  24 0 335           JMP ERR231
1571   06242  01 1 353           DCR INDEX
1572   06243  27 0 235           PJP JMP25A
1573   06244  24 1 345  JEND     JMP TEST08
```

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```
1574                                    EJE
1575                                ERR1628ERR 16),162,TEST19
1575   06245   05 0 344  ✓              EDR 16)
1575   06246   00 0 162                 STP 162
1575   06247   24 0 152                 JMP TEST19
1576                                ERR1638ERR 16),163,TEST19
1576   06250   05 0 344                 EDR 16)
1576   06251   00 0 163                 STP 163
1576   06252   24 0 152                 JMP TEST19
1577                                ERR1648ERR 16),164,TEST19
1577   06253   05 0 344                 EDR 16)
1577   06254   00 0 164                 STP 164
1577   06255   24 0 152                 JMP TEST19
1600                                ERR1658ERR 16),165,TEST19
1600   06256   05 0 344                 EDR 16)
1600   06257   00 0 165                 STP 165
1600   06260   24 0 152                 JMP TEST19
1601                                ERR1718ERR 17),171,TEST19
1601   06261   05 0 343  ✓              EDR 17)
1601   06262   00 0 171                 STP 171
1601   06263   24 0 152                 JMP TEST19
1602                                ERR1728ERR 17),172,TEST19
1602   06264   05 0 343                 EDR 17)
1602   06265   00 0 172                 STP 172
1602   06266   24 0 152                 JMP TEST19
1603                                ERR1738ERR 17),173,TEST19
1603   06267   05 0 343                 EDR 17)
1603   06270   00 0 173                 STP 173
1603   06271   24 0 152                 JMP TEST19
1604                                ERR1748ERR 17),174,TEST19
1604   06272   05 0 343                 EDR 17)
1604   06273   00 0 174                 STP 174
1604   06274   24 0 152                 JMP TEST19
1605                                ERR1608ERR 16),160,TEST19
1605   06275   05 0 344                 EDR 16)
1605   06276   00 0 160                 STP 160
1605   06277   24 0 152                 JMP TEST19
1606                                ERR1618ERR 16),161,TEST19
1606   06300   05 0 344                 EDR 16)
1606   06301   00 0 161                 STP 161
```

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```
1606   06302  24 0 152          JMP TEST19
1607                          ERR2108ERR 21),210,TST19A
1607   06303  05 0 342  /       EDR 21)
1607   06304  00 0 210          STP 210
1607   06305  24 0 167          JMP TST19A
1610                          ERR2118ERR 21),211,TST19A
1610   06306  05 0 342          EDR 21)
1610   06307  00 0 211          STP 211
1610   06310  24 0 167          JMP TST19A
1611                          ERR2608ERR 26),260,TEST20
1611   06311  05 0 341  /       EDR 26)
1611   06312  00 0 260          STP 260
1611   06313  24 1 350          JMP TEST20
1612                          ERR2618ERR 26),261,TEST20
1612   06314  05 0 341          EDR 26)
1612   06315  00 0 261          STP 261
1612   06316  24 1 350          JMP TEST20
1613                          ERR1458ERR 14),145,TEST25
1613   06317  05 0 373          EDR 14)
1613   06320  00 0 145          STP 145
1613   06321  24 0 233          JMP TEST25
1614                          ERR1448ERR 14),144,TEST25
1614   06322  05 0 373          EDR 14)
1614   06323  00 0 144          STP 144
1614   06324  24 0 233          JMP TEST25
1615                          ERR1468ERR 14),146,TEST25
1615   06325  05 0 373          EDR 14)
1615   06326  00 0 146          STP 146
1615   06327  24 0 233          JMP TEST25
1616                          ERR1438ERR 14),143,TEST25
1616   06330  05 0 373          EDR 14)
1616   06331  00 0 143          STP 143
1616   06332  24 0 233          JMP TEST25
1617                          ERR2218ERR 22),221,END
1617   06333  05 0 340  /       EDR 22)
1617   06334  00 0 221          STP 221
1617   06335  24 0 243          JMP END
1620                          ERR2318ERR 23),231,END
       06336  24 0 377          SKP
       06337     00023          WRD
```

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06340	00022	WRD
06341	00026	WRD
06342	00021	WRD
06343	00017	WRD
06344	00016	WRD
06345	05074	WRD
06346	00003	WRD
06347	06805	WRD
06350	06526	WRD
06351	00002	WRD
06352	00037	WRD
06353	05266	WRD
06354	00020	WRD
06355	37777	WRD
06356	00101	WRD
06357	00001	WRD
06360	12525	WRD
06361	37776	WRD
06362	05263	WRD
06363	25252	WRD
06364	05261	WRD
06365	05267	WRD
06366	10000	WRD
06367	05624	WRD
06370	00025	WRD
06371	00015	WRD
06372	05651	WRD
06373	00014	WRD
06374	05605	WRD
06375	00000	WRD
06376	05565	WRD
06377	00010	WRD

PROJECT NO. 530053 PROGRAMMER J. E. PHILLIPPI TAPE NUMBER 345116

```
1620   06400  05 0 377 /        EDR 23.
1620   06401  00 0 231          STP 231
1620   06402  24 1 376 .        JMP END
1621                     ERR2028ERR 20),202,TEST20
1621   06403  05 0 376 /        EDR 20)
1621   06404  00 0 202          STP 202
1621   06405  24 0 126          JMP TEST20
1622                     ERR3218ERR 32),321,TEST24
1622   06406  05 0 374 /        EDR 32)
1622   06407  00 0 321          STP 321
1622   06410  24 1 373 /        JMP TEST24
1623                     ERR3228ERR 32),322,TEST24
1623   06411  05 0 374          EDR 32)
1623   06412  00 0 322          STP 322
1623   06413  24 1 373          JMP TEST24
1624                     ERR3238ERR 32),323,TEST24
1624   06414  05 0 374          EDR 32)
1624   06415  00 0 323          STP 323
1624   06416  24 1 373          JMP TEST24
1625                     ERR3248ERR 32),324,TEST24
1625   06417  05 0 374          EDR 32)
1625   06420  00 0 324          STP 324
1625   06421  24 1 373          JMP TEST24
1626                     ERR3128ERR 10),312,TEST24
1626   06422  05 0 372 /        EDR 10)
1626   06423  00 0 312          STP 312
1626   06424  24 1 373          JMP TEST24
1627                     ERR3028ERR 10),302,TEST24
1627   06425  05 0 372          EDR 10)
1627   06426  00 0 302          STP 302
1627   06427  24 1 373          JMP TEST24
1630                     ERR3108ERR 10),310,TEST24
1630   06430  05 0 372          EDR 10)
1630   06431  00 0 310          STP 310
1630   06432  24 1 373          JMP TEST24
1631                     ERR3038ERR 10),303,TEST24
1631   06433  05 0 372          EDR 10)
1631   06434  00 0 303          STP 303
1631   06435  24 1 373          JMP TEST24
1632                     ERR0238ERR 2),023,TEST24
```

```
1632   06436  05 0 371  ✓        EDR 2)
1632   06437  00 0 023           STP 023
1632   06440  24 1 373           JMP TEST24
1633                     ERR0248ERR 2),024,TEST24
1633   06441  05 0 371           EDR 2)
1633   06442  00 0 024           STP 024
1633   06443  24 1 373           JMP TEST24
1634                     ERR0258ERR 2),025,TEST24
1634   06444  05 0 371           EDR 2)
1634   06445  00 0 025           STP 025
1634   06446  24 1 373           JMP TEST24
1635                     ERR0268ERR 2),026,TEST24
1635   06447  05 0 371           EDR 2)
1635   06450  00 0 026           STP 026
1635   06451  24 1 373           JMP TEST24
1636                     ERR3508ERR 12),350,TEST24
1636   06452  05 0 370  ✓        EDR 12)
1636   06453  00 0 350           STP 350
1636   06454  24 1 373           JMP TEST24
1637                     ERR3528ERR 12),352,TEST24
1637   06455  05 0 370           EDR 12)
1637   06456  00 0 352           STP 352
1637   06457  24 1 373           JMP TEST24
1640                     ERR3518ERR 12),351,TEST24
1640   06460  05 0 370           EDR 12)
1640   06461  00 0 351           STP 351
1640   06462  24 1 373           JMP TEST24
1641                     ERR3548ERR 12),354,TEST24
1641   06463  05 0 370           EDR 12)
1641   06464  00 0 354           STP 354
1641   06465  24 1 373           JMP TEST24
1642                     ERR3538ERR 12),353,TEST24
1642   06466  05 0 370           EDR 12)
1642   06467  00 0 353           STP 353
1642   06470  24 1 373           JMP TEST24
1643                     ERR1758ERR 16),175,TEST24
1643   06471  05 0 367  ✓        EDR 16)
1643   06472  00 0 175           STP 175
1643   06473  24 1 373           JMP TEST24
1644                     ERR1768ERR 16),176,TEST24
```

```
1644   06474  05 0 367          EDR 16)
1644   06475  00 0 176          STP 176
1644   06476  24 1 373          JMP TEST24
1645                       ERR1778ERR 16),177,TEST24
1645   06477  05 0 367          EDR 16)
1645   06500  00 0 177          STP 177
1645   06501  24 1 373          JMP TEST24
1646                       ERR0138ERR 1),013,TEST24
1646   06502  05 0 366    J     EDR 1)
1646   06503  00 0 013          STP 013
1646   06504  24 1 373          JMP TEST24
1647                       ERR0148ERR 1),014,TEST24
1647   06505  05 0 366          EDR 1)
1647   06506  00 0 014          STP 014
1647   06507  24 1 373          JMP TEST24
1650                       ERR0158ERR 1),015,TEST24
1650   06510  05 0 366          EDR 1)
1650   06511  00 0 015          STP 015
1650   06512  24 1 373          JMP TEST24
1651                       ERR0168ERR 1),016,TEST24
1651   06513  05 0 366          EDR 1)
1651   06514  00 0 016          STP 016
1651   06515  24 1 373          JMP TEST24
1652                       ERR3578ERR 13),357,TEST24
1652   06516  05 0 365    J     EDR 13)
1652   06517  00 0 357          STP 357
1652   06520  24 1 373          JMP TEST24
1653                       ERR3618ERR 13),361,TEST24
1653   06521  05 0 365          EDR 13)
1653   06522  00 0 361          STP 361
1653   06523  24 1 373          JMP TEST24
1654                       ERR3608ERR 13),360,TEST24
1654   06524  05 0 365          EDR 13)
1654   06525  00 0 360          STP 360
1654   06526  24 1 373          JMP TEST24
```

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```
1655                                    EJE
1656                                                TEST 20
1657
1660                                                CHECK DESIGNATOR SETTINGS AFTER EXECUTION OF EACH
1661                                                INSTRUCTION IN THE SEQUENCE FOLLOWING JMP20A
1662                                                RETURN JUMP TO THE CHECK ROUTINES
1663   06527  32 0 375    TEST20ENL 20)
1664   06530  37 0 204          STL TEST
1665   06531  32 0 364  J       8ENL 2524)
1666   06532  37 1 363  J       STL INDEX
1667   06533  32 0 362  J       8ENL 7777)
1670   06534  37 1 361  J       STL TEMPA
1671   06535  13 0 360  J       8EOR 37777)
1672   06536  37 1 357  J       STL TEMPB
1673                                                DSIGCK CLEARS THE DESIGNATOR AND CHECKS THE JUMPS
1674                                                TEMPA ALWAYS POSITIVE  7777-5253
1675                                                TEMPB ALWAYS NEGATIVE - COMPLEMENT OF TEMPA
1676                                                TEMPA - TEMPB = POSITIVE # - TEMPB = NEGATIVE #
1677   06537  36 0 205   JMP20A RJP DSIGCK
1700   06540  32 1 361          ENL TEMPA
1701   06541  36 0 216          RJP J2022A
1702   06542  11 1 357          SUB TEMPB
1703   06543  36 0 225          RJP J2022B
1704   06544  11 1 357          SUB TEMPB
1705   06545  36 0 236          RJP J2022C
1706   06546  36 0 245          RJP J2022D
1707   06547  01 1 361          DCR TEMPA
1710   06550  36 0 301          RJP J2022E
1711   06551  32 1 361          ENL TEMPA
1712   06552  13 0 360          8EOR 37777)
1713   06553  36 0 312          RJP J2022F
1714   06554  37 1 357          STL TEMPB
1715   06555  36 0 320          RJP J2022G
1716                             DSK INDEX,TEST21,JMP20A
1716   06556  01 1 363          DCR INDEX
1716   06557  20 1 356  J       ZJP TEST21
1716   06560  24 0 136          JMP JMP20A
```

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```
1717                                    EJE
1720                                                TEST 22
1721
1722                                                CHECK DESIGNATOR SETTINGS AFTER EXECUTION OF EACH
1723                                                INSTRUCTION IN THE SEQUENCE FOLLOWING  JMP22A
1724                                                RETURN JUMP TO THE CHECK ROUTINES
1725   06561   32 0 355  J'ES'22BENL 22)
1726   06562   37 0 204          STL TEST
1727   06563   32 0 364         8ENL 2524)
1730   06564   37 1 363          STL INDEX
1731   06565   32 0 362         8ENL 7777)
1732   06566   37 1 354  J       STL TEMP
1733                                                DSIGCK CLEARS THE DESIGNATOR AND CHECKS THE JUMPS
1734                                                TEMP ALWAYS POSITIVE  7777->253
1735                                                TEMP + TEMP = POSITIVE # + TEMP = NEGATIVE #
1736   06567   36 0 205   JMP22A MJP DSIGCK
1737   06570   32 1 354          ENL TEMP
1740   06571   36 0 216          MJP J2022A
1741   06572   10 1 354          ADD TEMP
1742   06573   36 0 225          MJP J2022B
1743   06574   10 1 354          ADD TEMP
1744   06575   36 0 236          MJP J2022C
1745   06576   36 0 245          MJP J2022D
1746   06577   01 1 354          DCR TEMP
1747   06600   36 0 301          MJP J2022E
1750                             DSK INDEX,TEST23,JMP22A
1750   06601   01 1 363          DCR INDEX
1750   06602   20 1 353  J       ZJP TEST23
1750   06603   24 0 166          JMP JMP22A
```

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```
1751                                    EJE
1752   06604      00000    TEST        OCT
1753                                                DSIGCK CLEARS THE DESIGNATOR AND CHECKS THE JUMPS
1754   06605      00000    DSIGCK      ...
1755   06606   05 0 215                EDR ZERO
1756   06607   26 1 352 J              OJP ERR260
1757   06610   20 0 002                ZJP ERR202
1760   06611   21 1 351 J              EJP ERR210
1761   06612   27 1 350 J              PJP ERR270
1762   06613   25 1 347 J              CJP ERR250
1763   06614   24 1 205                RTN
1764   06615      00000    ZERO        OCT 0
1765                                                FOLLOWING ARE SUBROUTINES FOR TESTS 20, 22
1766                                                ENL POSITIVE NUMBER
1767   06616      00000    J2022A      ...
1770   06617   26 0 005                OJP ERR321
1771   06620   20 0 010                ZJP ERR322
1772   06621   25 0 013                CJP ERR323
1773   06622   27 0 223                PJP L+2
1774   06623   24 0 016                JMP ERR324
1775   06624   24 1 216                RTN
1776                                                ADD/SUB  POS/NEG #    RESULT  POSITIVE
1777   06625      00000    J2022B      ..
2000   06626   26 1 346 J              OJP ERR300
2001   06627   20 1 345 J              ZJP ERR301
2002   06630   25 0 024                CJP ERR302
2003   06631   27 0 232                PJP L+2
2004   06632   24 0 032                JMP ERR303
2005   06633   21 0 234                EJP L+2
2006   06634   24 1 344 J              JMP ERR304
2007   06635   24 1 225                RTN
2010                                                ADD/SUB  POS/NEG #    RESULT  NEGATIVE
2011   06636      00000    J2022C      .
2012   06637   26 0 240                OJP L+2
2013   06640   24 1 343 J              JMP ERR307
2014   06641   27 0 027                PJP ERR310
2015   06642   20 1 342 J              ZJP ERR311
2016   06643   25 0 021                CJP ERR312
2017   06644   24 1 236                RTN
2020   06645      00000    J2022D      ...
```

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```
2021  06646  02 1 341  /        CMB ACC
2022  06647  26 0 250           OJP L+2
2023  06650  24 0 035           JMP ERR023
2024  06651  27 0 252           PJP L+2
2025  06652  24 0 046           JMP ERR026
2026  06653  20 0 040           ZJP ERR024
2027  06654  25 0 043           CJP ERR025
2030  06655  12 0 340  /        8AND 37774)
2031  06656  26 0 257           OJP L+2
2032  06657  24 0 051           JMP ERR350
2033  06660  25 0 261           CJP L+2
2034  06661  24 0 057           JMP ERR351
2035  06662  20 0 054           ZJP ERR352
2036  06663  21 0 264           EJP L+2
2037  06664  24 0 065           JMP ERR353
2040  06665  27 0 266           PJP L+2
2041  06666  24 0 062           JMP ERR354
2042  06667  16 1 341           RSH ACC
2043  06670  27 0 271           PJP L+2
2044  06671  24 0 073           JMP ERR176
2045  06672  26 0 273           OJP L+2
2046  06673  24 1 337  /        JMP ERR156
2047  06674  20 1 336  /        ZJP ERR157
2050  06675  25 0 070           CJP ERR175
2051  06676  21 0 277           EJP L+2
2052  06677  24 0 076           JMP ERR177
2053  06700  24 1 245           RTN
2054                                    DCR POSITIVE NUMBER
2055  06701      00000   J2022E  ...
2056  06702  26 0 303           OJP L+2
2057  06703  24 0 101           JMP ERR013
2060  06704  27 0 305           PJP L+2
2061  06705  24 0 112           JMP ERR016
2062  06706  25 0 307           CJP L+2
2063  06707  24 0 107           JMP ERR015
2064  06710  20 0 104           ZJP ERR014
2065  06711  24 1 301           RTN
2066                                    COMPLEMENT POSITIVE #
2067  06712      00000   J2022F  ...
2070  06713  26 0 314           OJP L+2
```

```
2071   06714  24 0 115            JMP ERR357
2072   06715  27 0 123            PJP ERR360
2073   06716  20 0 120            ZJP ERR361
2074   06717  24 1 312            RTN
2075                                       STL NEGATIVE NUMBER
2076   06720      00000   J2022G  ..
2077   06721  26 0 322            OJP L+2
2100   06722  24 1 335  J         JMP ERR373
2101   06723  27 1 334  J         PJP ERR376
2102   06724  20 1 333  J         ZJP ERR374
2103   06725  25 1 332  J         CJP ERR375
2104   06726  24 1 320            RTN
2105                     ERR0338ERR 03),33,TEST24
2105   06727  05 0 331  J         EDR 03)
       06730  24 0 377            SKP
       06731      00003           WRD
       06732      07136           WRD
       06733      07133           WRD
       06734      07141           WRD
       06735      07130           WRD
       06736      07117           WRD
       06737      07114           WRD
       06740      37774           WRD
       06741      00101           WRD
       06742      07053           WRD
       06743      07042           WRD
       06744      07072           WRD
       06745      07056           WRD
       06746      07050           WRD
       06747      06035           WRD
       06750      05322           WRD
       06751      06302           WRD
       06752      06310           WRD
       06753      07176           WRD
       06754      05263           WRD
       06755      00022           WRD
       06756      07144           WRD
       06757      05265           WRD
       06760      37777           WRD
       06761      05264           WRD
```

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06762	07777	WRD
06763	05266	WRD
06764	02524	WRD
06765	00013	WRD
06766	00001	WRD
06767	00016	WRD
06770	00012	WRD
06771	00002	WRD
06772	00010	WRD
06773	06213	WRD
06774	00032	WRD
06775	00020	WRD
06776	06243	WRD
06777	00023	WRD

```
2103   07000  00 0 033          STP 33
2104   07001  24 1 364          JMP *-*
2105                        ERR0334ERR 03,334,*-24
2106   07002  05 0 360          EDR 03)
2107   07003  00 0 034          STP 34
2108   07004  24 1 364          JMP *-*
2109                        ERR0355ERR 03,335,*-24
2110   07005  05 0 360          EDR 03)
2111   07006  00 0 035          STP 35
2112   07007  24 1 364          JMP *-*
2113                        ERR0365ERR 03,336,*-24
2114   07010  05 0 360          EDR 03)
2115   07011  00 0 036          STP 36
2116   07012  24 1 364          JMP *-*
2117                        ERR0110ERR 01,11,*-24
2118   07013  05 0 362          EDR 01)
2119   07014  00 0 011          STP 11
2120   07015  24 1 364          JMP *-*
2121                        ERR0120ERR 01,12,*-24
2122   07016  05 0 362          EDR 01)
2123   07017  00 0 012          STP 12
2124   07020  24 1 364          JMP *-*
2125                        ERR3720ERR 37,372,*-24
2126   07021  05 0 361          EDR 37)
2127   07022  00 0 372          STP 372
2128   07023  24 1 364          JMP *-*
2129                        ERR3770ERR 37,377,*-24
2130   07024  05 0 361          EDR 37)
2131   07025  00 0 377          STP 377
2132   07026  24 1 364          JMP *-*
2133                        ERR3340ERR 32,334,*-24
2134   07027  05 0 360          EDR 32)
2135   07030  00 0 334          STP 334
2136   07031  24 1 364          JMP *-*
2137                        ERR3350ERR 32,335,*-24
2138   07032  05 0 360          EDR 32)
2139   07033  00 0 335          STP 335
2140   07034  24 1 364          JMP *-*
2141                        ERR3360ERR 32,336,*-24
2142   07035  05 0 360          EDR 32)
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

```
2117   07036  00 0 336          STP 336
2117   07037  24 1 364          JMP TEST24
2120                        ERR3378ERR 32),337,TEST24
2120   07040  05 0 360          EDR 32)
2120   07041  00 0 337          STP 337
2120   07042  24 1 364          JMP TEST24
2121                        ERR3078ERR 10),307,TEST24
2121   07043  05 0 357          EDR 10)
2121   07044  00 0 307          STP 307
2121   07045  24 1 364          JMP TEST24
2122                        ERR3138ERR 10),313,TEST24
2122   07046  05 0 357          EDR 10)
2122   07047  00 0 313          STP 313
2122   07050  24 1 364          JMP TEST24
2123                        ERR3008ERR 10),300,TEST24
2123   07051  05 0 357          EDR 10)
2123   07052  00 0 300          STP 300
2123   07053  24 1 364          JMP TEST24
2124                        ERR3118ERR 10),311,TEST24
2124   07054  05 0 357          EDR 10)
2124   07055  00 0 311          STP 311
2124   07056  24 1 364          JMP TEST24
2125                        ERR3018ERR 10),301,TEST24
2125   07057  05 0 357          EDR 10)
2125   07060  00 0 301          STP 301
2125   07061  24 1 364          JMP TEST24
2126                        ERR3148ERR 10),314,TEST24
2126   07062  05 0 357          EDR 10)
2126   07063  00 0 314          STP 314
2126   07064  24 1 364          JMP TEST24
2127                        ERR3068ERR 10),306,TEST24
2127   07065  05 0 357          EDR 10)
2127   07066  00 0 306          STP 306
2127   07067  24 1 364          JMP TEST24
2130                        ERR3058ERR 10),305,TEST24
2130   07070  05 0 357          EDR 10)
2130   07071  00 0 305          STP 305
2130   07072  24 1 364          JMP TEST24
2131                        ERR3048ERR 10),304,TEST24
2131   07073  05 0 357          EDR 10)
```

PROJECT NO. 530053 PROGRAMMER J E PHILLIPPI TAPE NUMBER 345116

```
2131   07074  00 0 304          STP 304
2131   07075  24 1 364          JMP TEST24
2132                        ERR3638ERR 13),363,TEST24
2132   07076  05 0 356  ✓       EDR 13)
2132   07077  00 0 363          STP 363
2132   07100  24 1 364          JMP TEST24
2133                        ERR3628ERR 13),362,TEST24
2133   07101  05 0 356          EDR 13)
2133   07102  00 0 362          STP 362
2133   07103  24 1 364          JMP TEST24
2134                        ERR1538ERR 16),153,TEST24
2134   07104  05 0 355  ✓       EDR 16)
2134   07105  00 0 153          STP 153
2134   07106  24 1 364          JMP TEST24
2135                        ERR1548ERR 16),154,TEST24
2135   07107  05 0 355          EDR 16)
2135   07110  00 0 154          STP 154
2135   07111  24 1 364          JMP TEST24
2136                        ERR1558ERR 16),155,TEST24
2136   07112  05 0 355          EDR 16)
2136   07113  00 0 155          STP 155
2136   07114  24 1 364          JMP TEST24
2137                        ERR1568ERR 16),156,TEST24
2137   07115  05 0 355          EDR 16)
2137   07116  00 0 156          STP 156
2137   07117  24 1 364          JMP TEST24
2140                        ERR1578ERR 16),157,TEST24
2140   07120  05 0 355          EDR 16)
2140   07121  00 0 157          STP 157
2140   07122  24 1 364          JMP TEST24
2141                        ERR3558ERR 12),355,TEST24
2141   07123  05 0 354  ✓       EDR 12)
2141   07124  00 0 355          STP 355
2141   07125  24 1 364          JMP TEST24
2142                        ERR3568ERR 12),356,TEST24
2142   07126  05 0 354          EDR 12)
2142   07127  00 0 356          STP 356
2142   07130  24 1 364          JMP TEST24
2143                        ERR3738ERR 37) 373,TEST24
2143   07131  05 0 361          EDR 37)
```

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```
2143   07132  00 0 373          STP 373
2143   07133  24 1 364          JMP TEST24
2144                       ERR3748ERR 371,374,TEST24
2144   07134  05 0 361          EDR 371
2144   07135  00 0 374          STP 374
2144   07136  24 1 364          JMP TEST24
2145                       ERR3758ERR 371,375,TEST24
2145   07137  05 0 361          EDR 371
2145   07140  00 0 375          STP 375
2145   07141  24 1 364          JMP TEST24
2146                       ERR3768ERR 371,376,TEST24
2146   07142  05 0 361          EDR 371
2146   07143  00 0 376          STP 376
2146   07144  24 1 364          JMP TEST24
```

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```
2147                                    EJE
2150                                                TEST 21
2151
2152                                                CHECK DESIGNATOR SETTINGS AFTER EXECUTION OF EACH
2153                                                INSTRUCTION IN THE SEQUENCE FOLLOWING  JMP21A
2154                                                RETURN JUMP TO THE CHECK ROUTINES
2155   07145   32 0 353  JTEST218ENL 21)
2156   07146   37 1 352  J       STL TEST
2157   07147   32 0 351  J      8ENL 2524)
2160   07150   37 1 350  J       STL INDEX
2161   07151   32 0 347  J      8ENL 32524)
2162   07152   37 1 346  J       STL TEMPA
2163   07153   13 0 345  J      8EOR 37777)
2164   07154   37 1 344  J       STL TEMPB
2165                                                DSIGCK CLEARS THE DESIGNATOR AND CHECKS THE JUMPS
2166                                                TEMPA ALWAYS NEGATIVE  32524 - 30000
2167                                                TEMPA ALWAYS POSITIVE - COMPLEMENT TEMPA
2170                                                TEMPA - TEMPB = NEGATIVE # - TEMPB = POSITIVE #
2171   07155   36 1 343  JJMP21A RJP DSIGCK
2172   07156   32 1 346          ENL TEMPA
2173   07157   36 0 222          RJP J213AA
2174   07160   11 1 344          SUB TEMPB
2175   07161   36 0 230          RJP J213BB
2176   07162   11 1 344          SUB TEMPB
2177   07163   36 0 241          RJP J213CC
2200   07164   36 0 252          RJP J213DD
2201   07165   01 1 346          DCR TEMPA
2202   07166   36 0 302          RJP J213EE
2203   07167   32 1 346          ENL TEMPA
2204   07170   13 0 345         8EOR 37777)
2205   07171   36 0 311          RJP J213FF
2206   07172   37 1 344          STL TEMPB
2207   07173   36 0 317          RJP J213GG
2210                              DSK INDEX,TEST22,JMP21A
2210   07174   01 1 350          DCR INDEX
2210   07175   20 1 342  J       ZJP TEST22
2210   07176   24 0 154          JMP JMP21A
```

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```
2211                                EJE
2212                                                TEST 23
2213
2214                                                CHECK DESIGNATOR SETTINGS AFTER EXECUTION OF EACH
2215                                                INSTRUCTION IN THE SEQUENCE FOLLOWING  JMP23A
2216                                                RETURN JUMP TO THE CHECK ROUTINES
2217   07177   32 0 341  JTEST23 ENL 23)
2220   07200   37 1 352          STL TEST
2221   07201   32 0 351         8ENL 2524)
2222   07202   37 1 350          STL INDEX
2223   07203   32 0 347         8ENL 32524)
2224   07204   37 1 340  J       STL TEMP
2225                                                DSIGCK CLEARS THE DESIGNATOR AND CHECKS THE JUMPS
2226                                                TEMP ALWAYS NEGATIVE  32524 - 30000
2227                                                TEMP + TEMP = NEGATIVE # + TEMP = POSITIVE #
2230   07205   36 1 343   JMP23A RJP DSIGCK
2231   07206   32 1 340          ENL TEMP
2232   07207   36 0 222          RJP J213AA
2233   07210   10 1 340          ADD TEMP
2234   07211   36 0 230          RJP J213BB
2235   07212   10 1 340          ADD TEMP
2236   07213   36 0 241          RJP J213CC
2237   07214   36 0 252          RJP J213DD
2240   07215   01 1 340          DCR TEMP
2241   07216   36 0 302          RJP J213EE
2242                             DSK INDEX,TEST24,JMP23A
2242   07217   01 1 350          DCR INDEX
2242   07220   20 1 364          ZJP TEST24
2242   07221   24 0 204          JMP JMP23A
```

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```
2243                                    EJE
2244                                                FOLLOWING ARE SUBROUTINES FOR TESTS 21, 23
2245                                                ENL NEGATIVE #
2246   07222      00000   J213AA
2247   07223  26 0 026            OJP ERR334
2250   07224  25 0 031            CJP ERR335
2251   07225  20 0 034            ZJP ERR336
2252   07226  27 0 037            PJP ERR337
2253   07227  24 1 222            RTN
2254                                                ADD/SUB  NEG/POS #   RESULT NEGATIVE
2255   07230      00000   J213BB ...
2256   07231  26 0 050            OJP ERR300
2257   07232  27 0 067            PJP ERR305
2260   07233  25 0 234            CJP L+2
2261   07234  24 0 064            JMP ERR306
2262   07235  20 0 056            ZJP ERR301
2263   07236  21 0 237            EJP L+2
2264   07237  24 0 072            JMP ERR304
2265   07240  24 1 230            RTN
2266                                                ADD/SUB  NEG/POS #   RESULT POSITIVE
2267   07241      00000   J213CC ...
2270   07242  26 0 243            OJP L+2
2271   07243  24 0 042            JMP ERR307
2272   07244  27 0 245            PJP L+2
2273   07245  24 0 045            JMP ERR313
2274   07246  20 0 053            ZJP ERR311
2275   07247  25 0 250            CJP L+2
2276   07250  24 0 061            JMP ERR314
2277   07251  24 1 241            RTN
2300   07252      00000   J213DD ...
2301   07253  03 1 337  /         SMB ACC
2302   07254  26 0 255            OJP L+2
2303   07255  24 1 336  /         JMP ERR033
2304   07256  27 0 007            PJP ERR036
2305   07257  20 0 001            ZJP ERR034
2306   07260  25 0 004            CJP ERR035
2307   07261  12 0 335  /        8AND 37774)
2310   07262  26 0 263            OJP L+2
2311   07263  24 1 334  /         JMP ERR350
2312   07264  27 0 122            PJP ERR355
```

```
2313   07265  20 1 333  /        ZJP ERR352
2314   07266  25 0 267           CJP L+2
2315   07267  24 1 332  /        JMP ERR351
2316   07270  21 0 125           EJP ERR356
2317   07271  16 1 337           RSH ACC
2320   07272  27 0 106           PJP ERR154
2321   07273  25 0 103           CJP ERR153
2322   07274  26 0 275           OJP L+2
2323   07275  24 0 114           JMP ERR156
2324   07276  21 0 111           EJP ERR155
2325   07277  20 0 117           ZJP ERR157
2326   07300  05 1 331  /        EDR ZERO
2327   07301  24 1 252           RTN
2330                                        DCR NEGATIVE #
2331   07302     00000   J213EE  ...
2332   07303  26 0 015           OJP ERR012
2333   07304  20 1 330  /        ZJP ERR014
2334   07305  25 0 306           CJP L+2
2335   07306  24 1 327  /        JMP ERR015
2336   07307  27 0 012           PJP ERR011
2337   07310  24 1 302           RTN
2340                                        COMPLEMENT NEGATIVE #
2341   07311     00000   J213FF  ...
2342   07312  26 0 100           OJP ERR362
2343   07313  27 0 314           PJP L+2
2344   07314  24 0 075           JMP ERR363
2345   07315  20 1 326  /        ZJP ERR361
2346   07316  24 1 311           RTN
2347                                        STL POSITIVE #
2350   07317     00000   J213GG  ...
2351   07320  26 0 020           OJP ERR372
2352   07321  25 0 136           CJP ERR375
2353   07322  20 0 133           ZJP ERR374
2354   07323  27 0 324           PJP L+2
2355   07324  24 0 023           JMP ERR377
2356   07325  24 1 317           RTN
2357                              GEN
       07326     06520           WRD
       07327     06507           WRD
       07330     06504           WRD
```

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07331	06615	WRD
07332	06457	WRD
07333	06454	WRD
07334	06451	WRD
07335	37774	WRD
07336	06726	WRD
07337	00101	WRD
07340	05263	WRD
07341	00023	WRD
07342	06560	WRD
07343	06605	WRD
07344	05265	WRD
07345	37777	WRD
07346	05264	WRD
07347	32524	WRD
07350	05266	WRD
07351	02524	WRD
07352	06604	WRD
07353	00021	WRD
07354	00012	WRD
07355	00016	WRD
07356	00013	WRD
07357	00010	WRD
07360	00032	WRD
07361	00037	WRD
07362	00001	WRD
07363	00003	WRD
07364	06213	WRD

```
2360                                                    ADDER TEST TABLE
2361    07365     37774          OCT 37774,37775,37776
        07366     37775
        07367     37776
2362    07370     00003          OCT 00003,00001,00002,12525,25252,25252,25252,12525,12525,00002
        07371     00001
        07372     00002
        07373     12525
        07374     25252
        07375     25252
        07376     25252
        07377     12525
        07400     12525
        07401     00002
2363    07402     00002          OCT 00002,37777,37775,00000,37775,00001,37777,00001,37776,37776
        07403     37777
        07404     37775
        07405     00000
        07406     37775
        07407     00001
        07410     37777
        07411     00001
        07412     37776
        07413     37776
2364    07414     00000    TABLE OCT 00000
2365              05001          END TEST01
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 345116

STARTED 3/22/65.11/26/00 A.M.
COMPLETED 3/22/65.11/33/16 A.M.
NUMBER OF INPUT RECORDS 1269.
NUMBER OF OUTPUT RECORDS 1886.
NUMBER OF BINARY RECORDS 1295.

CORE CROSSTALK TEST (D10A)

I. Purpose of Test

To clear any half-set cores and to check core for crosstalk interference.

II. Description of Test

The test is divided into two parts:

In part one the following sequence is executed: (TØPLØC = highest numbered core location.)

> Store positive zero at location TØPLØC, check, store negative zero (37777_8) at location TØPLØC, check, store positive zero at location TØPLØC, check; repeat this procedure for locations TØPLØC-1, TØPLØC-2, ..., LASTLØ+1, where LASTLØ (152_8) is the last location of the core crosstalk program.

In part two the following sequence is executed:

> Store negative zero (37777_8) in location TØPLØC for an arbitrary number of times, check to see that all core locations in the same bay as this location are positive zero; repeat this procedure for locations TØPLØC-1, TØPLØC-2, ..., LASTLØ+1.

Provision has been made to vary the highest core location (TØPLØC) from the end of the crosstalk test (LASTLØ+1 = 153_8) up to and including 37777_8. Errors will occur if TØPLØC is a number for which no core bay exists. Since the program does not communicate with any I/O devices it needs no interrupts. Thus the program is to be run under lockout.

The first part of the program unsets any half-set cores that may have occurred before testing. After this part is finished, part two checks for crosstalk interference. The number of cycles of this test may be varied from 1 to 8191 times, or if desired, the test may be run continuously.

III. Operation of Test

A. Read in the binary tape of the Core Crosstalk test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Preset	Description
136_8	TØPLØC	37577_8	Highest core location to be tested.
137_8	NØCYCL	0	Number of cycles to be done.

C. Start the test.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the test (0_8), depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Depress the Start button.

D. If an error is encountered, the test will stop with the S-Register set as follows:

Part One Error:

S-Register (0-7)	Description
001	First positive zero stored or read incorrectly.
002	First positive zero stored or read as negative number.
003	Negative zero stored or read incorrectly.
004	Negative zero stored or read as positive number.
005	Second positive zero stored or read incorrectly.
006	Second positive zero stored or read as negative number.

Location ADDRES (140_8) will contain the address of the error. Thus contents of the contents of ADDRES may be inspected if half-set cores are not suspected.

Part Two Error:

S-Register (0-7)	Description
007	Disturbed location not zero.

Location ADDRES (140_8) contains the address of the location where storage actually took place; location LØCNDX (141_8) contains the address of the disturbed location.

To continue testing, depress the Start button.

E. If the number of cycles becomes equal to NØCYCL, the program is terminated with the S-Register (bits 7-0) containing 010_8. If NØCYCL equals a positive zero, the program runs continuously.

F. Proper operation of the core is verified by the absence of computer stops (except, of course, stop 010).

G. The program may be restarted by pushing the Start button.

IV. Storage

Number of locations used: 152_8 ($1-152_8$).

ROJECT NO, 530053 PROGRAMMER E,E O,HARE TAPE NUMBER 345045

```
 1                                          CORE CROSSTALK TEST
 2
 3                                          PROGRAM LIBRARY
 4                                          PROGRAM NO,  P-50 D10A
 5
 6
 7                                     THE FOLLOWING ARE PROGRAM PARAMETERS:
10            37577   HIADRS8EQU 37577              HIGHEST ADDRESS   TO BE CHECKED
11            00000   TIMES 8EQU 0                  NO OF CYCLES TO BE COMPLETED
12
13                                               NOTE WELL!  THIS PROGRAM MUST SKIP BY THE ACC,
14            00001          ORG PC+1                PROGRAM IS TO BE RUN UNDER LOCKOUT
15   00001  32 0 137  START  ENL NOCYCL
16   00002  37 0 143         STL CNTR          RESET NO, OF CYCLES COUNTER
17   00003  32 0 136  PART1  ENL TOPLOC              UNSET HALFSET CORES TEST
20   00004  37 0 140         STL ADDRES              STORE ADDRESS INDEX
21   00005  11 0 152         SUB END
22   00006  37 0 142         STL COUNT               STORE NUMBER OF ADDRESSES INDEX
23   00007  32 0 151  JLOOP1 ENL +0)
24   00010  37 1 140         STL ADDRES,I            WRITE POS, ZERO IN -ITH CORE LOCATION
25   00011  32 1 140         ENL ADDRES,I            READ -ITH CORE LOCATION
26   00012  20 0 014         ZJP 10CCT
27   00013  00 0 001         STP 1                   NOT ZERO, STOP 1
30   00014  24 0 016         JMP 20CCT               PROCEED
31   00015  27 0 016  10CCT  PJP 20CCT
32   00016  00 0 002         STP 2                   NOT POS, ZERO, STOP2
33   00017  32 0 150  J20CCT ENL -0)
34   00020  37 1 140         STL ADDRES,I            WRITE NEG, ZERO IN -ITH CORE LOCATION
35   00021  32 1 140         ENL ADDRES,I            READ -ITH CORE LOCATION
36   00022  27 0 025         PJP 30CCT
37   00023  20 0 026         ZJP 40CCT
40   00024  00 0 003         STP 3                   NOT NEG ZERO, STOP 3
41   00025  24 0 026         JMP 40CCT
42   00026  00 0 004  30CCT  STP 4                   NOT NEG, NUMBER, STOP 4
43   00027  32 0 151  40CCT  ENL +0)
44   00030  37 1 140         STL ADDRES,I            WRITE POS, ZERO IN -ITH CORE LOCATION
45   00031  32 1 140         ENL ADDRES,I            READ -ITH CORE LOCATION
46   00032  20 0 034         ZJP 50CCT
47   00033  00 0 005         STP 5                   NOT ZERO, STOP 5
50   00034  24 0 136         JMP 60CCT               PROCEED
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE APE NUMBER 345045

```
51   00035  27 0 036   50CCT  PJP 60CC!
52   00036  00 0 006          STP 6              NOT POS, ZERO, STOP 6
53   00037  01 0 140   60CCT  DCR ADDRES         DECREMENT ADDRESS INDEX
54   00040  01 0 142          DCR COUNT          DECREMENT COUNT
55   00041  20 0 042          ZJP CCTALK         CHECK CROSSTALK
56   00042  24 0 006          JMP LOOP1          WRITE-READ TEST NEXT CORE LOCATION
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345045

```
 57                                    EJE                    CROSSTALK TEST
 60   00043  32 0 136   CCTALK ENL TOPLOC
 61   00044  37 0 140          STL ADDRES                      STORE ADDRESS INDEX
 62   00045  32 0 147   JPART2 ENL 100)
 63   00046  37 0 142          STL COUNT
 64   00047  32 0 150          ENL -0)
 65   00050  37 1 140   /0CCT  STL ADDRES,I                    WRITE NEG ZERO 100 TIMES (ARBITRARY VALUE)
 66   00051  01 0 142          UCR COUNT                       TO SET UP FAVORABLE CONDITIONS FOR
 67   00052  27 0 047          PJP 70CCT                       CROSSTALK BETWEEN CORE LOCATIONS
 70
 71   00053  32 0 140          ENL ADDRES
 72   00054  13 0 136          EOR TOPLOC                      FIND COMMON BAY BITS
 73   00055  12 0 146   J      BAND 30000)
 74   00056  20 0 071          ZJP 100CCT                      ADDRESS AND TOPLOC IN SAME BAY
 75   00057  32 0 140          ENL ADDRES                      ADDRESS IS IN A LOWER BAY THAN TOPLOC
 76   00060  12 0 146          BAND 30000)
 77   00061  13 0 145   J      BEOR 7777)                      SET LOCNDX  TO HIGHEST BAY LOCATION IN
100   00062  37 0 141          STL LOCNDX                        WHICH ADDRESS IS IN
101   00063  12 0 146          BAND 30000)
102   00064  20 0 066          ZJP 80CCT                       LOCNDX IS IN BAY ZERO
103   00065  32 0 145          BENL 7777)                      LOCNDX IS NOT IN BAY ZERO. SET COUNT TO
104   00066  24 0 103          JMP 105CCT                        4096 DECIMAL (ONE BAY)
105   00067  32 0 145   80CCT  BENL 7777)
106   00070  11 0 152   90CCT  SUB END                         SET COUNT TO 4096 MINUS NO  OF
107   00071  24 0 104          JMP 110CCT                        INSTRUCTION IN TEST
110   00072  32 0 136   100CCT ENL TOPLOC
111   00073  37 0 141          STL LOCNDX                      SET LOCATION INDEX TO TOP LOCATION
112   00074  12 0 146          BAND 30000)
113   00075  06 0 142          SDR COUNT                       STORE BAY ZERO INDICATOR
114   00076  32 0 136          ENL TOPLOC
115   00077  12 0 145          BAND 7777)                      SET COUNT TO TOPLOC, IF NOT IN BAY ZERO
116   00100  24 0 101          JMP 103CCT              SKIP PAST ACCUMULATOR LOCATION
117   00101      C0000         OCT ***                       ACCUMULATOR LOCATION
120   00102  05 0 142   103CCT EOR COUNT              TOP LOCATION IN BAY ZERO. SET COUNT TO
121   00103  20 0 067          ZJP 90CCT                       TOPLOC MINUS NO. OF INS. IN TEST
122   00104  10 0 144   J105CCT ADD 1)
123   00105  37 0 142   110CCT S L COUN                        STORE NO. OF WORDS TO BE CHECKED
```

```
      124                              EJE                  CHECK WHETHER CROSSTALK HAS OCCURRED
      125
      126                                                   (LOOP2) IS THE DOMINANT LOOP IN THAT THE
      127                                                   TIME TO EXECUTE ALL THE OTHER INSTRUCTIONS
      130                                                   IS NEGLIGIBLE COMPARED TO THIS LOOP.  THE
      131                                                   TOTAL NUMBER OF MACHINE CYCLES IS 16. IF
      132                                                   A MAXIMUM OF 4096 WORDS ARE CHECKED (IT IS
      133                                                   ASSUMED THAT THERE IS NO CROSSTALK BETWEEN
      134                                                   BAYS) FOR EACH BAY, THEN THE MAXIMUM TIME
      135                                                   FOR ONE COMPLETE CYCLE TO CHECK ALL THAT
      136                                                   WAS REQUESTED WOULD BE:
      137
      140                                                      TIME =  (16)*(4.5US)*(4096)*NOWORDS
      141
      142                                                      TIME = .0048*NOWORDS  MINUTES/CYCLE
      143
      144                                                   IF NOWORDS IS 4096:
      145                                                      TIME = 19.2 MIN/CYCLE
      146
      147                                                   IF NOWORDS IS 16384:
      150                                                      TIME = 76.8 MIN/CYCLE
      151
      152                                                   THIS TIME FORMULA MAY BE USED TO OBTAIN
      153                                                   A ROUGH APPROXIMATION OF THE LENGTH OF
      154                                                   A CYCLE, SINCE SIMPLIFICATIONS HAVE BEEN
      155                                                   MADE TO OBTAIN SAID FORMULA.
      156
      157   00106  32 0 150            ENL -0)              INITIALIZE FOR CARRY JUMP
      160   00107  10 1 141   LOOP2    ADD LOCNDX,I         CHECK LOCATION
      161   00110  25 0 130            CJP 120CCT           LOCATION HAS CHANGED, NOT POS, ZERO
      162   00111  01 0 141   120CCT   DCM LOCNDX           LOCATION OKAY
      163   00112  01 0 142            DCR COUNT
      164   00113  27 0 106            PJP LOOP2            CHECK NEXT LOCATION
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345045

```
165                                     EJE                     RESET AND SETUP FOR NEXT CROSSTALK TRY
166    00114   32 0 151                 ENL *01
167    00115   37 1 140                 STL ADDRES,I            RESTORE CONTENTS OF TRIED CROSSTALK ADRESS
170    00116   01 0 140                 DCR ADDRES              DECREMENT ADDRESS
171    00117   32 0 140                 ENL ADDRES
172    00120   11 0 152                 SUB END
173    00121   20 0 122                 ZJP 130CCT              ALL ADDRESSES HAVE BEEN TESTED
174    00122   24 0 044                 JMP PART2               TRY NEXT ADDRESS FOR CROSSTALK
175
176    00123   32 0 143   130CCT ENL CNTR
177    00124   20 0 002                 ZJP PART1               REPEAT TEST CONTINUOUSLY
200    00125   01 0 143                 DCR CNTR
201    00126   27 0 002                 PJP PART1               REPEAT TEST FOR NUMBER OF CYCLES
202    00127   00 0 010                 STP 8                   TEST FINISHED. NO. OF CYCLES COMPLETED
203    00130   24 0 000                 JMP START         REPEAT PROGRAM
204
205    00131   32 0 140   140CCT ENL ADDRES
206    00132   11 0 141                 SUB LOCNDX
207    00133   20 0 110                 ZJP 120CCT              ERROR OKAY. CHECK WAS ON ADDRESS
210    00134   00 0 007                 STP 7                   CROSSTALK ERROR. CHECK ADDRESS AND
211    00135   24 0 110                 JMP 120CCT              LOCNDX, AND CONTINUE IF DESIRED
212
213
214                                     THE FOLLOWING MAY BE PROGRAM INPUTS:
215    00136     37577    TOPLOC OCT HIADRS                    TOP LOCATION
216    00137     00000    NOCYCL OCT TIMES                     NUMBER OF CYCLES
217
220    00140     00000    ADDRES OCT
221    00141     00000    LOCNDX OCT
222    00142     00000    COUNT  OCT
223    00143     00000    CNTR   OCT
224                                     BEN
       00144     00001            WRD
       00145     07777            WRD
       00146     30000            WRD
       00147     00144            WRD
       00150     37777            WRD
       00151     00000            WRD
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345045

```
225   00152     00152   END     OCT LASTLO
226             00152   LASTLO  SYN L-1              LAST LOCATION
227             00000           END
```

DATE 3/22/65. TIME 10/46/16 A.M.

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345045

STARTED 3/22/65.10/45/00 A.M.
COMPLETED 3/22/65.10/46/18 A.M.
NUMBER OF INPUT RECORDS 151.
NUMBER OF OUTPUT RECORDS 157.
NUMBER OF BINARY RECORDS 109.

WORST CASE CORE PATTERN TEST (D11A)

I. Purpose of Test

To generate the worst case core pattern in all specified bays of core, and to check that this pattern has been successfully generated.

II. Description of Test

The program stores the desired pattern throughout core, from the highest location specified (HIADR) down to the lowest location specified (LØADR). LØADR may vary from the end of the worst case core program (371_8) to the physical end of core (7777_8 for 4K core, 37777_8 for 16K core, etc.). HIADR may vary from LØADR to the physical end of core. The pattern has been derived from the manufacturer's specifications of the core any may be deducted from the program listing. Provision has also been made to store the complement (plus zero for minus zero and vice versa) of the worst case core pattern if so desired.

Once the pattern has been stored, each core location between HIADR and LØADR is checked to verify that it is either plus or minus zero. Core locations are checked from the highest to the lowest core location. One pass through this limit is designated as a cycle. The number of cycles may be varied from 1 to 8191, or if desired, the test may run continuously.

If an error occurs, that is, a core location does not contain plus or minus zero, the core location and the contents of that particular location are printed out on the ASR typewriter. The correct value is then attempted to be stored in this location and the checking proceeds. A control on the number of errors printed may be changed from 1 to 8191 lines.

All interrupts are ignored except the one corresponding to the ASR typewriter. The interrupt location and the channel number of the ASR typewriter must be changed to correspond with the existing hardware setup.

III. Operation of Test

A. Read in the binary tape of the Worst Case Core Pattern test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Place the binary tape under the tape reader.

5. Turn the reader on.

6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Preset	Description
317_8	ASRCHA	1	ASR typewriter channel
320_8	INTLØC	11_8	ASR interrupt location
321_8	IND	0	If non-zero, complement pattern
322_8	HIADR	37577_8	Highest core location to be tested
323_8	LØADR	371_8	Lowest core location to be tested
324_8	NØCYCL	0	Number of cycles to execute
325_8	PRTCNT	1000_{10}	Number of error printouts allowed

C. Start the Test

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the test (101_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Depress the Start button.

D. Any errors encountered will be printed on the ASR typewriter. An example of such a printout is:

27753 37773

Thus location 27753_8 has dropped bit two. The ASR set is turned on at the start of each printout and off at the end of it.

If the number of error printouts becomes equal to PRTCNT, the program is terminated with the S-Register (bits 7-0) containing two (2).

E. If the number of cycles becomes equal to NØCYCL, the program is terminated with the S-Register (bits 7-0) containing one (1). If NØCYCL equals a positive zero, the program runs continuously.

F. Proper operation of the core is verified by the absence of printout on the ASR typewriter.

G. The program may be restarted by pushing the Start button.

IV. Storage

Number of locations used: 267_8 (102 - 371).

JECT NO. 530853 PROGRAMMER E.E. O,HARE TAPE NUMBER 345066

```
                                        WORST CASE CORE PATTERN TEST

                                        PROGRAM LIBRARY
                                        PROGRAM NO.  P-50 B11A


                                    THE FOLLOWING ARE PROGRAM PARAMETERS:
            00001   ASROCH EQU 1                    ASR OUTPUT CHANNEL
            00011   ASRCLOBEQU 11                   ASR OUTPUT INTERRUPT COMPLETION LOCATION
            00000   PATYPE EQU 0                    PATTERN TYPE: NORMAL=0; COMPLEMENTED=NON-0
            37577   HIADRSBEQU 37577                HIGHEST CORE ADDRESS TO BE INCLUDED IN TST
            01750   NOLINE EQU 1000                 MAXIMUM NUMBER OF LINES TO BE PRINTED
            00000   TIMES BEQU 0                    NUMBER OF TEST CYCES REQUESTED:+0=INFINITE

                        UNL
            00102       UNG ACC+1
00102   32 0 370 JWCCOREBENL 100)                   START OF WORST CASE CORE PROGRAM-INITILIZE
00103   37 0 334        STL TEMP1
00104   32 0 367 /      BENL 23403)
00105   37 1 334        STL TEMP1,I                 STORE IGNORE INTERRUPTS (CLJ ,I)
00106   01 0 334        DCR TEMP1                     IN ALL THE INTERRUPT LOCATIONS
00107   27 0 104        PJP L-2

00110   32 0 322        ENL HIADR
00111   37 0 333        STL PSEUDP                  PSEUDO-PROGRAM COUNTER INDEX.
00112   11 0 323        SUB LOADR
00113   10 0 366 /      ADD 1)
00114   37 0 332        STL COUNT                   NO. OF LOCATIONS TO BE USED IN TEST
00115   32 0 317        ENL ASRCHA
00116   10 0 365 /      BADD 34000)
00117   37 0 314        STL OUTCOM                  COMPUTE AND STORE OUTPUT COMMAND
00120   32 0 354        ENL CLKOUT
00121   37 0 201        STL TVECTR                  STORE TRANSFER VECTOR TO CLEAR LOCKOUT
00122   32 0 356        ENL INTINS
00123   37 1 320        STL INTLOC,I                STORE INTERRUPT INSTRUCTION
00124   32 0 324        ENL NOCYCL                  RESTORE COUNTERS
00125   37 0 326        STL CTR1
00126   32 0 325        ENL PRTCNT
00127   37 0 327        STL CTR2
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345066

```
                                                    TEST X-PART OF MATRIX: BITS 00-05
                                                    DETERMINE WHETHER A +0 OR -0 SHOULD BE

                                                    STORED IN THE LOC. NOW BEING CONSIDERED

                                                    THE ALGORITHM BY WHICH THIS IS DONE
                                                    IS BRIEFLY DESCRIBED BY THE REMARKS
                                                    THAT FOLLOW

                                          NOMENCLATURE
                                                X = 0, 1, 2, 3, 4, 5, 6, OR 7
                                                Y = 0, 1, 2, OR 3
                                                F = FOUR OR FIVE
                                                S = SIX OR SEVEN
                                                ODD * ODD   = EVEN
                                                ODD * EVEN  = ODD
                                                EVEN * EVEN = EVEN

                                       IF A LOCATION IS EVEN IN THE SENSE USED BELOW AND IND = 0,
                                                ALL ONES WILL BE STORED IN THE LOCATION.

                                       IF A LOCATION IS ODD IN THE SENSE USED BELOW AND IND = 0,
                                                ALL ZEROS WILL BE STORED IN THE LOCATION.

                                       IF IND IS NOT ZERO, THE REVERSE OF THE ABOVE IS TRUE

00130   32 0 345    TESTX   ENL 002000
00131   37 0 331            STL CHKLOC
00132   32 0 321            ENL IND
00133   20 0 134            ZJP L+2
00134   01 0 331            DCR CHKLOC
00135   32 0 333            ENL PSEUDP
00136   12 0 340            AND 000010
00137   20 0 140            ZJP L+2
00140   01 0 331            DCR CHKLOC
00141   32 0 333            ENL PSEUDP
00142   12 0 341            AND 000020
00143   20 0 144            ZJP L+2
00144   01 0 331            DCR CHKLOC
```

OJECT NO. 530053 PROGRAMMER E E O.HARE TAPE NUMBER 345066

```
121                                                  XX0X, XX3X, XX4X, AND XX7X ARE EVEN
122                                                  XX1X, XX2X, XX5X, AND XX6X ARE ODD
123
124   00145   32 0 333          ENL PSEUDP
125   00146   12 0 337          AND 000004
126   00147   20 0 150          ZJP L+2
127   00150   24 0 154          JMP TESTY
130   00151   32 0 333          ENL PSEUDP
131   00152   12 0 336          AND 000002
132   00153   20 0 154          ZJP TESTY
133   00154   01 0 331          DCR CHKLOC
134
135                                                  XXX0, XXX1, XXX4, XXX5, XXX6, AND XXX7 ARE EVEN
136                                                  XXX2 AND XXX3 ARE ODD
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345066

```
137                                 EJE                 TEST Y-PART OF MATRIX: BITS 06-11
140   00155  32 0 333   TESTY      ENL PSEUDP
141   00156  12 0 343              AND 000400
142   00157  20 0 167              ZJP NOTBT8
143   00160  32 0 333              ENL PSEUDP
144   00161  12 0 342              AND 000200
145   00162  20 0 163              ZJP L+2
146   00163  01 0 331              DCR CHKLOC
147   00164  32 0 333              ENL PSEUDP
150   00165  12 0 344              AND 001000
151   00166  20 0 167              ZJP L+2
152   00167  01 0 331              DCR CHKLOC
153   00170  32 0 333   NOTBT8     ENL PSEUDP
154   00171  12 0 345              AND 002000
155   00172  20 0 173              ZJP DONE
156   00173  01 0 331              DCR CHKLOC
157
160                                       0YXX, 1YXX, 4YXX, AND 5YXX ARE EVEN
161                                       2YXX, 3YXX, 6YXX, AND 7YXX ARE ODD
162
163                                       0FXX, 1SXX, 2SXX, 3FXX, 4FXX
164                                       5SXX, 6SXX, AND 7FXX ARE EVEN
165
166                                       0SXX, 1FXX, 2FXX, 3SXX, 4SXX,
167                                       5FXX, 6FXX, AND 7SXX ARE ODD
```

```
170                                 EJE                 STORE WORST CASE CORE PATTERN
171   00174   32 0 335    DONE      ENL ZERO            TESTING OF LOCATION IS DONE
172   00175   01 0 331              DCR CHKLOC
173   00176   21 0 177              EJP L+2             STORE +0 OR -0  IN THE LOCATION BEING
174   00177   32 0 346              ENL MZERO           TESTED AS DETERMINED BY THE TESTX AND
175   00200   37 1 333              STL PSEUDP,I        TESTY  ROUTINES
176   00201      00000    TVECTR    OCT **              IF ALL LOCS HAVE BEEN TESTED, GO TO CONTIN
177   00202   01 0 333              DCR PSEUDP          IF NOT, COME HERE AND DCR PSEUDO-P INDEX
200   00203   01 0 332              DCR COUNT           DECREMENT COUNT
201   00204   20 0 205              ZJP L+2
202   00205   24 0 127              JMP TESTX           TEST NEXT LOCATION
203   00206   32 0 355              ENL CONJMP
204   00207   37 0 201              STL TVECTR          REPLACE TRANSFER VECTOR WITH CONTINUE JUMP
```

PROJECT NO. 530053 PROGRAMMER E.E. O,HARE TAPE NUMBER 345066

```
205                                    EJE                 CHECK WORST CASE CORE PATTERN
206   00210  32 0 322   CHECK  ENL HIADR
207   00211  37 0 333          STL PSEUDP                  INITIALIZE PSEUDO-PROGRAM COUNTER INDEX
210   00212  11 0 323          SUB LOADR
211   00213  10 0 366          ADD 1)
212   00214  37 0 332          STL COUNT                   INITIALIZE NO. OF LOCATIONS COUNT
213
214   00215  32 1 333   CHKLOP ENL PSEUDP,I               CHECK LOCATION
215   00216  20 0 223          ZJP CONTIN
216   00217  36 0 237          RJP PRTERR                  LOCATION IN ERROR, NOT +0 OR -0
217   00220  01 0 327          DCR CTR2                    DECREMENT PRINT COUNT
220   00221  27 0 127          PJP TESTX                   RESTORE THIS LOCATION PROPERLY
221   00222  00 0 002          STP 2                       LINES PRINTED HAVE EXCEEDED LIMIT ---STOP
222   00223  24 0 101          JMP WCCORE                  REPEAT PROGRAM
223
224   00224  01 0 333   CONTIN DCR PSEUDP                  DECREMENT PSEUDO-P INDEX
225   00225  01 0 332          DCR COUNT                   DECREMENT COUNT INDEX
226   00226  20 0 227          ZJP CHKCYL
227   00227  24 0 214          JMP CHKLOP                  CHECK NEXT LOCATION
230
231   00230  32 0 326   CHKCYL ENL CTR1                    BRING NUMBER OF CYCLES YET TO BE DONE
232   00231  20 0 233          ZJP CINFIT
233   00232  01 0 326          DCR CTR1                    DECREMENT NUMBER OF CYCLES
234   00233  24 0 207          JMP CHECK                   BEGIN ANOTHER SERIES OF CHECKS
235
236   00234  27 0 207   CINFIT PJP CHECK                  +0, CHECK CORE INFINITELY
237   00235  00 0 001          STP 1                       -0, TEST COMPLETED---STOP
240   00236  24 0 101          JMP WCCORE                  REPEAT PROGRAM
```

```
241                                     EJE                     PRINT THE ERROR
242   00237       00000   PRTERR  ...
243   00240  32 0 364  /          ENL 12)
244   00241  37 0 350              STL CNT                 NUMBER OF TURN ON CHARS TO OUTPUT
245   00242  32 0 353              ENL ASRON
246   00243  36 0 313   10WCC      RJP OUT                 TURN ON ASR SET IN PRESCRIBED MANNER
247   00244  01 0 350              DCR CNT
250   00245  27 0 242              PJP 10WCC
251   00246  32 0 350              ENL CR
252   00247  36 0 313              RJP OUT                 PRINT A CARRIAGE RETURN
253   00250  32 0 347              ENL LF
254   00251  36 0 313              RJP OUT                 PRINT A LINE FEED
255   00252  32 0 333              ENL PSEUDP
256   00253  36 0 267              RJP UNPACK              UNPACK AND PRINT LOCATION WHICH IS IN ERR
257   00254  32 0 363  /          ENL 3)
260   00255  37 0 350              STL CNT
261   00256  32 0 351              ENL SPACE
262   00257  36 0 313   20WCC      RJP OUT                 PRINT THREE SPACES
263   00260  01 0 350              DCR CNT
264   00261  27 0 256              PJP 20WCC
265   00262  32 1 333              ENL PSEUDP,I
266   00263  36 0 267              RJP UNPACK              UNPACK AND PRINT CONTENTS OF LOCATION
267   00264  32 0 352              ENL ASROFF
270   00265  36 0 313              RJP OUT                 TURN OFF ASR SET
271   00266  24 1 237              RTN
```

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 345066

```
272                                 EJE             UNPACK THE NUMBER AND OUTPUT
273   00267     00000   UNPACK      ...
274                                 RPT 4
275   00270  14 0 101               LSH ACC          SHIFT NUMBER INTO CORRECT INITIAL POSITION
276   00274  37 0 334               STL TEMP1
277   00275  32 0 362  J            ENL 5)
300   00276  37 0 330               STL CNT          SET DIGIT COUNT
301   00277  32 0 361  J            8ENL 140)
302   00300  24 0 301               JMP 40WCC        FIRST DIGIT IS EITHER 0-3
303   00301  32 0 360  J30WCC       8ENL 340)        OTHER DIGITS ARE 0-7
304                     40WCC       RPT 3
305   00302  14 0 334               LSH TEMP1
306   00305  12 0 334               AND TEMP1        GET DIGIT FROM NUMBER, IN CORRECT POSITION
307   00306  10 0 357  J            8ADD 13000)      FORM CORRESPONDING ASR OUTPUT CODE
310   00307  36 0 313               RJP OUT          PRINT DIGIT
311   00310  01 0 330               DCR CNT          DECREMENT DIGIT COUNT
312   00311  27 0 300               PJP 30WCC        GET NEXT DIGIT
313   00312  24 1 267               RTN
314
315   00313     00000   OUT         ...
316   00314  34 0 000   OUTCOM      OUT **           OUTPUT CHARACTER
317   00315  01 0 000               DCR PC           WAIT FOR INTERRUPT
320   00316  24 1 313   INTRTN      RTN              INTERRUPT RETURN
```

```
321                                    EJE                    CONSTANTS AND DATA
322                                                 THE FOLLOWING MAY BE MADE PROGRAM INPUTS!
323   00317      00001    ASRCHA OCT ASROCH          ASR OUTPUT CHANNEL NUMBER
324   00320      00011    INTLOC OCT ASROLO          ASR INTERRUPT LOCATION
325   00321      00000    IND    OCT PATYPE          COMPLEMENT INDICATOR
326   00322      37577    HIADR  OCT HIADRS          HIGHEST CORE ADDRESS TO BE CHECKED
327   00323      00371    LOADR  OCT END             LOWEST  CORE ADDRESS TO BE CHECKED
330   00324      00000    NOCYCL OCT TIMES           NO OF TEST CYCLES REQUESTED! +0=INFINITE
331   00325      01750    PRTCNT OCT NOLINE          PRINT COUNTER, MAXIMUM NO. OF LINES
332
333   00326      00000    CTR1   OCT
334   00327      00000    CTR2   OCT
335   00330      00000    CNT    OCT
336   00331      00000    CHKLOC OCT
337   00332      00000    COUNT  OCT
340   00333      00000    PSEUDP OCT
341   00334      00000    TEMP1  OCT
342   00335      00000    ZERO   OCT
343   00336      00002    000002 OCT 2
344   00337      00004    000004 OCT 4
345   00340      00010    000010 OCT 10
346   00341      00020    000020 OCT 20
347   00342      00200    000200 OCT 200
350   00343      00400    000400 OCT 400
351   00344      01000    001000 OCT 1000
352   00345      02000    002000 OCT 2000
353   00346      37777    MZERO  OCT -0
354   00347      10500    LF     OCT 21200/2
355   00350      10640    CR     OCT 21500/2
356   00351      12000    SPACE  OCT 24000/2
357   00352      17741    ASROFF OCT 17741
360   00353      37740    ASRON  OCT 37740
361   00354   23 0 201    CLKOUT CLJ TVECTR+1
362   00355   23 0 223    CONJMP CLJ CONTIN
363   00356   23 0 315    INTINS CLJ INTRTN
364                                GEN
      00357      13000           WRD
      00360      00340           WRD
      00361      00140           WRD
      00362      00005           WRD
```

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 345066

00363	00003	WRD
00364	00014	WRD
00365	34000	WRD
00366	00001	WRD
00367	23400	WRD
00370	00100	WRD

PROJECT NO. 930053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345066

```
      365              00371   END     SYN L                   FIRST LOCATION AVAILABLE FOR TESTING
      366              00000           END
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 345066

STARTED 3/22/65.11/02/00 A.M.
COMPLETED 3/22/65.11/03/47 A.M.
NUMBER OF INPUT RECORDS 246.
NUMBER OF OUTPUT RECORDS 256.
NUMBER OF BINARY RECORDS 186.

ADDER TEST (D12A)

I. Purpose of Test

To thoroughly test the adder by performing the following eight additions:

1. 00000 + 37776 = 37776
2. 00001 + 37777 = 00001
3. 37775 + 00000 = 37775
4. 37777 + 00002 = 00002
5. 12525 + 12525 = 25252
6. 25252 + 25252 = 12525
7. 00002 + 00001 = 00003
8. 37776 + 37775 = 37774

II. Description of Test

This test continuously performs the eight additions listed above and checks the sums.

III. Description of Operation

A. Read in the binary tape of the Adder test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.
7. After the tape has read in, the machine will transfer to the starting location of the test and begin.

B. The test runs continuously unless an error occurs.

C. When an error is encountered, the machine stops with the S-Register (bits 7-0) set as follows:

S-Register	Description
1	00000 + 37776 = 37776
2	00001 + 37777 = 00001
3	37775 + 00000 = 37775
4	37777 + 00002 = 00002
5	12525 + 12525 = 25252
6	25252 + 25252 = 12525
7	00002 + 00001 = 00003
10	37776 + 37775 = 37774

IV. Storage

Number of locations used: 103_8 (1001-1103)

PROJECT NO. 530053 PROGRAMMER L.M. MAYS TAPE NUMBER 345077

```
                                        ADDER TEST

                                        PROGRAM LIBRARY
                                        PROGRAM NO. P-50  D12A

                  01001                 ORG 513
01001   32 0 074  START   ENL ONEONE
01002   18 0 075          ADD ONETWO
01003   13 0 075          EOR ONETWO
01004   27 0 005          PJP L+2
01005   24 0 006          JMP L+2
01006   20 0 007          ZJP 2NDSUM
01007   00 0 001          STP 1
01010   32 0 076  2NDSUM  ENL TWOONE
01011   18 0 077          ADD TWOTWO
01012   13 0 076          EOR TWOONE
01013   27 0 014          PJP L+2
01014   24 0 015          JMP L+2
01015   20 0 016          ZJP 3RDSUM
01016   00 0 002          STP 2
01017   32 0 100  3RDSUM  ENL 3ONE
01020   18 0 074          ADD 3TWO
01021   13 0 100          EOR 3ONE
01022   27 0 023          PJP L+2
01023   24 0 024          JMP L+2
01024   20 0 025          ZJP 4THSUM
01025   00 0 003          STP 3
01026   32 0 077  4THSUM  ENL 4ONE
01027   18 0 101          ADD 4TWO
01030   13 0 101          EOR 4TWO
01031   27 0 032          PJP L+2
01032   24 0 033          JMP L+2
01033   20 0 034          ZJP 5THSUM
01034   00 0 004          STP 4
```

PROJECT NO. 530053 PROGRAMMER L.M. MAYS TAPE NUMBER 345077

```
 44                                      EJE
 45   01035  32 0 102   5THSUM ENL 5ONE
 46   01036  10 0 102          ADD 5TWO
 47   01037  13 0 103          EOR 6ONE
 50   01040  27 0 041          PJP L+2
 51   01041  24 0 042          JMP L+2
 52   01042  20 0 043          ZJP 6THSUM
 53   01043  00 0 005          STP 5
 54   01044  32 0 103   6THSUM ENL 6ONE
 55   01045  10 0 103          ADD 6TWO
 56   01046  13 0 102          EOR 5ONE
 57   01047  27 0 050          PJP L+2
 60   01050  24 0 051          JMP L+2
 61   01051  20 0 052          ZJP 7THSUM
 62   01052  00 0 006          STP 6
 63   01053  32 0 101   7THSUM ENL 7ONE
 64   01054  10 0 076          ADD 7TWO
 65   01055  13 0 072          EOR 03
 66   01056  27 0 057          PJP L+2
 67   01057  24 0 060          JMP L+2
 70   01060  20 0 061          ZJP 8THSUM
 71   01061  00 0 007          STP 7
 72   01062  32 0 075   8THSUM ENL 8ONE
 73   01063  10 0 100          ADD 8TWO
 74   01064  13 0 073          EOR 037774
 75   01065  27 0 066          PJP L+2
 76   01066  24 0 067          JMP L+2
 77   01067  20 0 000          ZJP START
100   01070  00 0 010          STP 8
101   01071  24 0 000          JMP START
```

PROJECT NO. 530053 PROGRAMMER L.M. MAYS TAPE NUMBER 345077

```
102                                    EJE
103  01072      00003     03          DEC 3
104  01073      37774     037774      OCT 37774
105  01074      00000     ONEONE      OCT 0
106  01075      37776     ONETWO      OCT 37776
107  01076      00001     TWOONE      OCT 1
110  01077      37777     TWOTWO      OCT 37777
111  01100      37775     3ONE        OCT 37775
112             01074     3TWO        SYN ONEONE
113             01077     4ONE        SYN TWOTWO
114  01101      00002     4TWO        OCT 2
115  01102      12525     5ONE        OCT 12525
116             01102     5TWO        SYN 5ONE
117  01103      25252     6ONE        OCT 25252
120             01103     6TWO        SYN 6ONE
121             01101     7ONE        SYN 4TWO
122             01076     7TWO        SYN TWOONE
123             01075     8ONE        SYN ONETWO
124             01100     8TWO        SYN 3ONE
125             01081                 END START
```

PROJECT NO. 530053 PROGRAMMER L.M. MAYS TAPE NUMBER 345077

STARTED 3/22/65.11/11/00 A.M.
COMPLETED 3/22/65.11/11/56 A.M.
NUMBER OF INPUT RECORDS 85.
NUMBER OF OUTPUT RECORDS 85.
NUMBER OF BINARY RECORDS 78.

735 SELECTRIC TYPEWRITER TEST (D13A)

I. Purpose of Test

To verify the proper operation of the 735 Selectric logging typewriter.

II. Description of Test

The program prints a set of characters twice per line on the 735 Selectric typewriter. This set includes all the alphanumeric and special characters. A sample printout of one half of a line follows:

ABCDEFGHIJKLMNOPQRSTUVWXYZ 1234567890-,/.='!;*)(+¢:°?±_#$@%&"

The 735 typewriter is placed in the lower case mode at the beginning and at the end of each half line. The number of lines printed may be varied from one to 8191 lines.

All interrupts are ignored except the one corresponding to the 735 typewriter which is being tested. The interrupt location and the channel number of the 735 typewriter must be changed to correspond to the existing hardware setup.

III. Description of Operation

A. Read in the binary tape of the 735 Selectric Typewriter test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.

B. Enter the test parameters

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the S-Register with the parameter location.
3. Using the probe, load the X-Register with the parameter constant; depress the Start button.
4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Preset	Description
152_8	735CHA	53_8	735 output channel number
153_8	INTLØC	13_8	735 interrupt location
154_8	NUMLIN	100_{10}	Number of lines to be printed

C. Start the test

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the test (101_8); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Depress the Start button.

D. The program will print the number of lines designated by NUMLIM and then stop with the S-Register (bits 7-0) containing a one.

E. Proper operation is verified by visual inspection of the 735 printout with the sample printout given above.

F. The program may be restarted by depressing the Start button.

IV. Storage

Number of locations used: $166_8 (102_8 - 267_8)$

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 535441

```
                                        735 SELECTRIC TYPEWRITER TEST

                                        PROGRAM LIBRARY
                                        PROGRAM NO.   D13A


                                    THE FOLLOWING ARE PROGRAM PARAMETERS:
            00053   7350CH8EQU 53               735 OUTPUT CHANNEL
            00013   7351RT8EQU 13               735 INTERRUPT LOCATION
            00144   TIMES  EQU 100              NUMBER OF LINES TO BE PRINTED


                     UNL
            00102    ORG ACC+1                  TYPE THE ENTIRE SET OF CHARS TWICE/LINE
00102  32 0 267  J     8ENL 100)
00103  37 0 155         STL CHRCNT
00104  32 0 266  J     8ENL 23400)               STORE IGNORE INTERRUPT (CLJ .I) IN ALL
00105  37 1 155  10TT   STL CHRCNT,I               THE INTERRUPT LOCATIONS
00106  01 0 155         DCR CHRCNT
00107  27 0 104         PJP 10TT
00110  32 0 152         ENL 735CHA
00111  10 0 265  J     8ADD 34000)
00112  37 0 140         STL OUTC04                 STORE PROPER CHANNEL IN OUTPUT COMMAND
00113  37 0 115         STL L+2
00114  32 0 164         ENL LOWERC                 PUT TYPEWRITER IN LOWER CASE
00115  34 0 000         OUT **
00116  32 0 160         ENL DELAY
00117  37 0 157         STL LINECT                 DELAY AT LEAST 60 MILLISECONDS
00120  01 0 157         DCR LINECT                   UNTIL LOWER CASE IS OUTPUT
00121  27 0 117         PJP LOOP                   REASON:NO INTERRUPT IF IT IS IN LOWER CASE
00122  32 0 163         ENL ITIMS
00123  37 1 153         STL 10TT,I                 STORE INTERRUPT INSTRUCTION
00124  32 0 154  START  ENL NUMLIN
00125  37 0 157         STL LINECT                 SET MAXIMUM NUMBER OF LINES TO BE TYPED

00126  32 0 264  LOOP   ENL 3)
00127  37 0 1[illegible]  STL FIELD                STORE NO. OF FIELDS/LINE (2 PLUS CR FIELD)
00130  32 0 243         ENL CR
00131  23 0 1[illegible]  [illegible]              OUTPUT CARRIAGE RETURN TO START
00132  32 0 1[illegible]  NFIELD ENL NUMCHS
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 535441

```
 51   00133  37 0 155          STL CHRCNT          STORE NO. OF CHARACTERS TO OUTPUT IN FIELD
 52   00134  32 0 162          ENL ENLTAB
 53   00135  37 0 136          STL BRINGC          STORE CHARACTER BRING INSTRUCTION
 54   00136     00000  BRINGC  OCT **              BRING A CHARACTER
 55   00137  01 0 136          DCR BRINGC          DECREMENT CHARACTER BRING INSTRUCTION
 56   00140  34 0 000  OUTCOM  OUT **              OUTPUT CHARACTER
 57   00141  01 0 000          DCR PC              WAIT FOR THE INTERRUPT
 60   00142  01 0 155  INTRTN  DCR CHRCNT
 61   00143  27 0 135          PJP BRINGC          GET NEXT CHARACTER
 62   00144  01 0 156          DCR FIELD
 63   00145  27 0 131          PJP NFIELD          FIELD FINISHED, GET NEXT FIELD
 64   00146  01 0 157          DCR LINECT
 65   00147  27 0 125          PJP LOOP            PRINT NEXT LINE
 66   00150  00 0 001          STP 1               NO. OF LINES REQUESTED HAVE BEEN PRINTED
 67   00151  24 0 123          JMP START
 70
 71
 72                            THE FOLLOWING MAY BE PROGRAM INPUTS:
 73   00152     00053  735CHA  OCT 7350CH          735 OUTPUT CHANNEL
 74   00153     00013  INTLOC  OCT 735IRT          735 INTERRUPT LOCATION
 75   00154     00144  NUMLIN  OCT TIMES           NO. OF LINES TO PRINT; IF ZERO RUN ALWAYS
 76
 77   00155     37777  CHRCNT  OCT -
100   00156     37777  FIELD   OCT -
101   00157     37777  LINECT  OCT -
102   00160     07640  DELAY   DEC 4000
103   00161     00077  NOCHRS  OCT STRTAB-ENDTAB+1
104   00162  32 0 262  ENLTAB  ENL STRTAB
105   00163  23 0 141  INTINS  CLJ INTRTN
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 535441

```
106                              EJE                    TABLE OF CODES FOR THE 735 SELECTRIC
107                       735    VFD 6,5,3
110                       ENDTAB EQU L
111    00164      00010   LOWERC 735 ,1,                LOWER CASE
112    00165      16000          735 28,,               QUOTES
113    00166      36400          735 61,,               AMPERSAND
114    00167      36000          735 60,,               %
115    00170      35000          735 58,,               @
116    00171      32400          735 53,,               $
117    00172      35400          735 59,,               #
120    00173      00200          735 ,16,               UNDER LINE
121    00174      37400          735 63,,               PLUS OR MINUS
122    00175      02400          735 5,,                ?
123    00176      17000          735 30,,               DEGREE SIGN
124    00177      06400          735 13,,               !
125    00200      34000          735 56,,               CENT SIGN
126    00201      05000          735 10,,               +
127    00202      30000          735 48,,               (
130    00203      32000          735 52,,               )
131    00204      34400          735 57,,               *
132    00205      00020          735 ,2,                U.C.
133    00206      06400          735 13,,               !
134    00207      17000          735 30,,               EXCLAMATION
135    00210      16000          735 28,,               APOSTROPHE
136    00211      05000          735 10,,               =
137    00212      15000          735 26,,               .
140    00213      02400          735 5,,                /
141    00214      04400          735 9,,                ,
142    00215      00200          735 ,16,               -
143    00216      32000          735 52,,               0
144    00217      30000          735 48,,               9
145    00220      34400          735 57,,               8
146    00221      36400          735 61,,               7
147    00222      34000          735 56,,               6
150    00223      36000          735 60,,               5
151    00224      32400          735 53,,               4
152    00225      35400          735 59,,               3
153    00226      35000          735 58,,               2
154    00227      37000          735 62,,               1
155    00230      00000          735 0,,                SPACE
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 535441

```
      156   00231     37000           735 62,.              Z
      157   00232     02000           735 4,.               Y
      160   00233     27400           735 47,.              X
      161   00234     10000           735 16,.              W
      162   00235     15400           735 27,.              V
      163   00236     25400           735 43,.              U
      164   00237     27000           735 46,.              T
      165   00240     12000           735 20,.              S
      166   00241     16400           735 29,.              R
      167   00242     04000           735 8,.               Q
      170   00243     06000           735 12,.              P
      171   00244     12400           735 21,.              O
      172   00245     25000           735 42,.              N
      173   00246     17400           735 31,.              M
      174   00247     22400           735 37,.              L
      175   00250     24000           735 40,.              K
      176   00251     07000           735 14,.              J
      177   00252     14000           735 24,.              I
      200   00253     22000           735 36,.              H
      201   00254     07400           735 15,.              G
      202   00255     05400           735 11,.              F
      203   00256     26000           735 44,.              E
      204   00257     26400           735 45,.              D
      205   00260     24400           735 41,.              C
      206   00261     20000           735 32,.              B
      207   00262     14400           735 25,.              A
      210             00262   STRTAB  EQU L-1
      211   00263     00040   CR      735 ,4,               CARRIAGE RETURN
            00264     00003           WRD
            00265     34000           WRD
            00266     23400           WRD
            00267     00100           WRD
      212             00000           END
```

PROJECT NO. 538053 PROGRAMMER E.E. O.HARE TAPE NUMBER 535441

STARTED 5/04/64. 6/57/00 A.M.
COMPLETED 5/04/64. 6/57/49 A.M.
NUMBER OF INPUT RECORDS 138.
NUMBER OF OUTPUT RECORDS 142.
NUMBER OF BINARY RECORDS 121.

EXTENDED CORE MEMORY TEST
P50 COMPUTER D14A

I. PURPOSE OF TEST

To extensively read and write into extended core and to check for crosstalk interference.

II. DESCRIPTION OF TEST

The test program reads and writes into extended core locations HIADR (highest address) through LØADR (lowest address) inclusive.

The test consists of three parts. In the first part, each extended core location is written and read individually, starting with location HIADR. The pattern is as follows: 37777_8 (all ones) is written into HIADR, then HIADR is read and the value checked, then 00000_8 (all zeros) is written and read, then 25252_8, and finally 12525_8. Following this, location HIADR-1 is written and read in the same manner, and then the remaining extended core locations, down to LØADR.

The second part is executed after the first. In this section all extended core locations are written with an alternating pattern; then all the locations are read and checked. The pattern is as follows: 37777_8, 00000_8, 37777_8, 00000_8, ... is stored in locations HIADR through LOADR, then the locations are read and checked; then 00000_8, 37777_8, 00000_8, 37777_8... is stored and checked; then 25252_8, 12525_8, 25252_8, 12525_8, and finally 12525_8, 25252_8, 12525_8, 25252_8 ....

In the third part, two location counters are initialized: C2 to HIADR, C3 to LØADR (or one, if LØADR is zero). Positive zero is output to the extended core location whose address is contained in C2; negative zero is output to location C3. Both locations are then read and their contents verified. The address in C2 is decremented; the address in C3 is incremented. The test recycles, using the new address until address C3 contains HIADR+1.

After part three is executed, the test decrements a NTIMES counter. If the counter is positive or if it is set so the test runs indefinitely, parts one, two, and three are again executed. If the test is set to run a fixed number of cycles, the computer will stop when the cycle counter is zero.

If an error occurs during the first or third parts, the location in error and the correct pattern are printed on the programmer's console ASR set. If an error occurs during the second part, the pattern (the value stored in HIADR) is printed. The computer stops after the error printout.

All interrupts are ignored except the one corresponding to the ASR typewriter.

III. OPERATION OF TEST

A. Read in the binary tape of the Extended Core Memory Test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (7602_8, 17602_8, 27602_8, or 37602_8); depress the Start Button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Place the binary tape under the tape reader; turn the reader on.

5. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat Steps 2 and 3 until all the following parameters have been entered;

Location		Preset	Description
6571_8	ADRCH	00070_8	Ext. Core address select channel
6575_8	ØUTCH	00077_8	Ext. Core output channel
6576_8	INTCH	00062_8	Ext. Core input channel
6577_8	ASRØC	00015_8	ASR output channel
6600_8	INTLØC	00011_8	ASR output interrupt location
6601_8	HIADR	37777_8	Highest Ext. Core loc. to test
6602_8	LØADR	00000	Lowest Ext. Core loc. to test
6603_8	NTIMES	00000	No. of cycles (+0 for infinite no.)

C. Start the test

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the test (6377_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Depress the Start button.

D. Errors

1. If an error occurs during part one, a message of the form below will be printed on the ASR set:

E1 Pxxxxx Lyyyyy

where "xxxxx" is the correct pattern (37777, 00000, 25252, or 12525) and "yyyyy" is the location in error. This location in extended core can then be examined to determine the exact error.

2. If an error occurs during part two, a message of the form below will be printed on the ASR set:

E2 Pxxxxx

where "xxxxx" is the pattern stored in location HIADR. The extended core S-Register will contain the address minus one (1) of the last location read.

3. If an error occurs during part three, the message is as follows:

E3 Pxxxxx Lyyyyy

where "xxxxx" is the correct pattern (00000, or 37777) and "yyyyy" is the location in error.

4. After any of the above error printouts, the computer will stop with the S-Register, bits 0-7, containing 002. If the Start button on the P-50 computer is depressed, part one, two, or three will be restarted, depending in which part the last error occurred.

E. Normal stop

When the number of cycles, NTIMES, have been executed (NTIMES $\neq$ +0), the computer will stop with the S-Register, bits 0-7, containing 001. The test may be restarted by depressing the Start button.

IV. STORAGE

Number of locations used: 560_8 (6400_8-7157_8).

V. RUN TIME

Recommended run time: 2 hours.

```
                                        EXTENDED CORE MEMORY TEST     PROGRAM NO. P-50 D14A

                                              THE FOLLOWING ARE PROGRAM PARAMETERS
                                              SEE LISTING, LOCATIONS 6574-6603
                00070   ADRCHN8EQU 70                 ADDRESS OUTPUT CHANNEL     OES
                00077   OUTCHN8EQU 77                 DATA OUTPUT CHANNEL        OEZ
                00062   INTCHN8EQU 62                 DATA INPUT CHANNEL         IEZ
                00015   ASROCH8EQU 15                 ASR OUTPUT CHANNEL
                00011   ASRINT8EQU 11                 ASR OUTPUT COMPLETE INTERRUPT LOCATION
                37777   HIADRS8EQU 37777              HIGHEST EXTENDED CORE ADDRESS TO TEST
                00000   LOADRS EQU 0                  LOWEST  EXTENDED CORE ADDRESS TO TEST
                00000   TIMES  EQU 0                  NO, TEST CYCLES (ZERO = INDEFINITE)


                06400          8ORG 6400              LOCKOUT SET
06400   32 0 361  JP1    8ENL 100)
06401   37 0 204          STL I1
06402   32 0 360  J       8ENL 23400)
06403   37 1 204          STL I1,I                   STORE CLJ 0,I IN ALL INTERRUPT LOCATIONS
06404   01 0 204          DCR I1
06405   27 0 002          PJP L-2
06406   23 0 006          CLJ L+1
06407   32 0 177          ENL ASROC
06410   10 0 357  J       8ADD 34000)
06411   37 0 315          STL OUTCUM
06412   32 0 207          ENL INTINS
06413   37 1 200          STL INTLOC,I
06414   32 0 210          ENL INTADD
06415   37 1 356  J       8STL 202
06416   32 0 174          ENL ADRCH
06417   10 0 357          8ADD 34000)
06420   37 0 214          STL A01
06421   37 0 220          STL A02
06422   37 0 231          STL A03
06423   37 0 242          STL A04
06424   37 0 322          STL A05
06425   37 0 326          STL A06
06426   37 0 335          STL A07
06427   32 0 175          ENL OUTCH
```

EXTENDED CORE MEMORY TEST

```
 51   06430  10 0 357          8ADD 34000)
 52   06431  37 0 216           STL 001
 53   06432  37 0 233           STL 002
 54   06433  37 0 235           STL 003
 55   06434  37 0 324           STL 004
 56   06435  37 0 330           STL 005
 57   06436  32 0 176           ENL INTCH
 60   06437  10 0 355 ✓         8ADD 30000)
 61   06440  37 0 221           STL I01
 62   06441  37 0 243           STL I02
 63   06442  37 0 251           STL I03
 64   06443  37 0 336           STL I04
 65
 66                                        TEST BEGINNING
 67
 70   06444  32 0 203  P11      ENL NTIMES
 71   06445  37 0 206           STL C1
 72
 73                                        PART ONE
 74
 75   06446  32 0 201  P12      ENL HIADR
 76   06447  37 0 205           STL PSEUDP
 77   06450  32 0 354 ✓P2       ENL -0)                    ALL ONES
100   06451  36 0 211           RJP S01
101   06452  27 0 377           PJP ERROR1
102   06453  20 0 054           ZJP L+2
103   06454  24 0 377           JMP ERROR1
104   06455  32 0 353 ✓         ENL +0)                    ALL ZEROS
105   06456  36 0 211           RJP S01
106   06457  20 0 060           ZJP L+2
107   06460  24 0 377           JMP ERROR1
110   06461  27 0 062           PJP L+2
111   06462  24 0 377           JMP ERROR1
112   06463  32 0 352 ✓         8ENL 25252)
113   06464  36 0 211           RJP S01
114   06465  13 0 351 ✓         8EOR 12525)
115   06466  27 0 377           PJP ERROR1
116   06467  20 0 070           ZJP L+2
117   06470  24 0 377           JMP ERROR1
120   06471  32 0 351          8ENL 12525)
```

EXTENDED CORE MEMORY TEST

```
      121   06472  36 0 211          RJP S01
      122   06473  13 0 351         8EOR 12525)
      123   06474  20 0 075          ZJP L+2
      124   06475  24 0 377          JMP ERROR1
      125   06476  27 0 077          PJP L+2
      126   06477  24 0 377          JMP ERROR1
      127
      130
      131   06500  32 0 205   P3     ENL PSEUDP
      132   06501  11 0 202          SUB LOADR
      133   06502  20 0 110          ZJP P4
      134   06503  01 0 205          DCR PSEUDP
      135   06504  20 0 105          ZJP L+2
      136   06505  24 0 047          JMP P2
      137   06506  32 0 353          ENL +0)
      140   06507  37 0 205          STL PSEUDP
      141   06510  24 0 047          JMP P2
      142
      143                                    PART TWO
      144
      145   06511  32 0 201   P4     ENL HIADR
      146   06512  11 0 202          SUB LOADR
      147   06513  37 0 205          STL PSEUDP
      150   06514  21 0 115          EJP L+2
      151   06515  24 0 116          JMP L+2
      152   06516  01 0 205          DCR PSEUDP
      153   06517  16 0 205          RSH PSEUDP
      154   06520  02 0 205          CMB PSEUDP
      155   06521  32 0 354          ENL -0)              ALL ONES--ALL ZEROS
      156   06522  36 0 223          RJP S02
      157   06523  32 0 353          ENL +0)              ALL ZEROS--ALL ONES
      160   06524  36 0 223          RJP S02
      161   06525  32 0 352         8ENL 25252)           25252--12525
      162   06526  36 0 223          RJP S02
      163   06527  32 0 351         8ENL 12525)           12525-25252
      164   06530  36 0 223          RJP S02
      165
      166                                    PART THREE
      167
      170   06531  32 0 201   P41    ENL HIADR
```

EXTENDED CORE MEMORY TEST

```
171   06532  37 0 263          STL C2
172   06533  32 0 202          ENL LOADH
173   06534  20 0 135          ZJP L+2
174   06535  24 0 136          JMP L+2
175   06536  32 0 350    /     ENL 1)
176   06537  37 0 264          STL C3
177
200   06540  36 0 320    P42   RJP S05
201   06541  32 0 264          ENL C3
202   06542  37 0 205          STL PSEUDP
203   06543  32 0 353          ENL +0)
204   06544  36 0 332          RJP S06
205   06545  32 0 263          ENL C2
206   06546  37 0 205          STL PSEUDP
207   06547  32 0 354          ENL -0)
210   06550  36 0 332          RJP S05
211
212   06551  32 0 264    P43   ENL C3
213   06552  13 0 201          EOR HIADH
214   06553  20 0 163          ZJP P49
215   06554  32 0 264          ENL C3
216   06555  10 0 350          ADD 1)
217   06556  37 0 264          STL C3
220   06557  01 0 263          DCR C2
221   06560  32 0 263          ENL C2
222   06561  13 0 264          EOR C3
223   06562  20 0 150          ZJP P43
224   06563  24 0 137          JMP P42
225
226
227                                     END OF ONE CYCLE
230   06564  32 0 206    P49   ENL C1
231   06565  20 0 171          ZJP P6              TEST FOR POS./NEG.
232   06566  01 0 206    P5    DCR C1
233   06567  27 0 045          PJP P12
234   06570  00 0 001          STP 1               NO. CYCLES COMPLETED
235   06571  23 0 043          CLJ P11
236   06572  27 0 045    P6    PJP P12
237   06573  24 0 165          JMP P5
```

```
      240                                    EJE
      241
      242
      243                                        THE FOLLOWING MAY BE PROGRAM INPUTS
      244   06574      00070    ADRCH   OCT ADRCHN
      245   06575      00077    OUTCH   OCT OUTCHN
      246   06576      00062    INTCH   OCT INTCHN
      247   06577      00015    ASROC   OCT ASROCH
      250   06600      00011    INTLOC  OCT ASRINT
      251   06601      37777    HIADR   OCT HIADRS
      252   06602      00000    LOADR   OCT LOADRS
      253   06603      00000    NTIMES  OCT TIMES
      254
      255
      256
      257   06604      00000    I1      OCT
      260   06605      00000    PSEUDP  OCT
      261   06606      00000    C1      OCT
I     262   06607   23 1 202    INTINS  CLJ 202,1
      263   06610      06716    INTADD  OCT INTRTN-1
```

```
264                                         EJE
265
266   06611      00000   S01     ...                 WRITE/READ ONE LOCATION
267   06612   37 0 262           STL PATTRN
270   06613   32 0 205           ENL PSEUDP
271   06614   34 0 070   A01     OUT ADRCHN
272   06615   32 0 262           ENL PATTRN
273   06616   34 0 077   001     OUT OUTCHN
274   06617   32 0 205           ENL PSEUDP
275   06620   34 0 070   A02     OUT ADRCHN
276   06621   30 0 062   I01     INT INTCHN
277   06622   24 1 211           RTN
300
301
302                                                 WRITE ALTERNATING PATTERN IN ALL TEST LOCATION
303   06623      00000   S02     ...
304   06624   37 0 262           STL PATTRN
305   06625   32 0 205           ENL PSEUDP
306   06626   37 0 263           STL C1
307   06627   37 0 264           STL C3
310   06630   32 0 201           ENL HIADR
311   06631   34 0 070   A03     OUT ADRCHN
312   06632   32 0 262   1S02    ENL PATTRN
313   06633   34 0 077   002     OUT OUTCHN
314   06634   13 0 264           EOR C3
315   06635   34 0 077   003     OUT OUTCHN
316   06636   01 0 263           DCR C2
317   06637   27 0 231           PJP 1S02
320   06640   20 0 231           ZJP 1S02
321   06641   32 0 201           ENL HIADR
322   06642   34 0 070   A04     OUT ADRCHN
323   06643   30 0 062   I02     INT INTCHN
324   06644   13 0 262           EOR PATTRN
325   06645   27 0 246           PJP L+2
326   06646   24 1 347   J       JMP ERROR2
327   06647   20 0 250           ZJP L+2
330   06650   24 1 347           JMP ERROR2
331   06651   30 0 062   I03     INT INTCHN
332   06652   13 0 262           EOR PATTRN
333   06653   27 1 347           PJP ERROR2
```

EXTENDED CORE MEMORY TEST

```
334   06654  20 0 255          ZJP L+2
335   06655  24 1 347          JMP ERROR2
336   06656  01 0 264          DCR C3
337   06657  27 0 242          PJP I02
340   06660  20 0 242          ZJP I02
341   06661  24 1 223          RTN
342   06662      00000  PATTRN OCT
343   06663      00000  C2     OCT
344   06664      00000  C3     OCT
345
346
347                                                    PRINT BUFFER
350   06665      00000  S03    ...
351   06666  32 0 346  /       ENL 12)
352   06667  37 0 307          STL CNT
353   06670  32 0 310  03L1    ENL ASRON
354   06671  36 0 314          RJP OUT
355   06672  01 0 307          DCR CNT
356   06673  27 0 267          PJP 03L1
357   06674  32 0 345  /       ENL OUTBF)
360   06675  37 0 312          STL BUF
361   06676  32 1 312  03L2    ENL BUF,I
362   06677  36 0 314          RJP OUT
363   06700  01 0 312          DCR BUF
364   06701  01 0 313          DCR BUFC
365   06702  27 0 275          PJP 03L2
366   06703  32 0 311          ENL ASROF
367   06704  36 0 314          RJP OUT
370   06705  00 0 002          STP 2
371   06706  23 1 265          CLJ S03,I
372   06707      00000  CNT    OCT
373   06710      37740  ASRON  OCT 37740
374   06711      17741  ASROF  OCT 17741
375   06712      00000  BUF    OCT
376   06713      00000  BUFC   OCT
377
400
401                                                    OUTPUT
402   06714      00000  OUT    ...
403   06715  34 0 015  OUTCOM OUT ASROCH
```

```
404   06716  01 1 353          DCH PC
405   06717  24 1 314   INTRTN RTN
406
407
410                                        WRITE FOR PART THREE
411   06720     00000   S05     ...
412   06721  52 0 264           ENL C3
413   06722  54 0 070   A05     OUT ADRCHN
414   06723  52 0 353           ENL +0)
415   06724  54 0 077   004     OUT OUTCHN
416   06725  52 0 263           ENL C2
417   06726  54 0 070   A06     OUT ADRCHN
420   06727  52 0 354           ENL -0)
421   06730  54 0 077   005     OUT OUTCHN
422   06731  24 1 320           RTN
423
424
425
426   06732     00000   S06     ...          READ/CHECK FOR PART THREE
427   06733  57 0 262           STL PATTRN
430   06734  52 0 265           ENL PSEUDP
431   06735  54 0 070   A07     OUT ADRCHN
432   06736  56 0 062   I04     INT INTCHN
433   06737  13 0 262           EOR PATTRN
434   06740  27 0 341           SKP L+2
435   06741  24 1 344           JMP ERRORS
436   06742  25 1 332           JSP S06,I
437   06743  24 1 344           JMP ERRORS
      06744     07014           WRD
      06745     07155           WRD
      06746     00014           WRD
      06747     07002           WRD
      06750     00001           WRD
      06751     12525           WRD
      06752     25252           WRD
      06753     00000           WRD
      06754     37777           WRD
      06755     30000           WRD
      06756     00202           WRD
      06757     34000           WRD
```

EXTENDED CORE MEMORY TEST

```
            06760     23400          WHD
            06761     00100          WHD
```

EXTENDED CORE MEMORY TEST

```
440                 07000          ORG 7000
441
442
443
444   07000  32 0 061   ERROR1 ENL ASR1              E1  PXXXXX  LXXXXX
445   07001  36 0 074          RJP S07
446   07002  24 1 157 J        JMP P12
447
450
451
452   07003  32 0 062   ERROR2 ENL ASR2              E2  PXXXXX
453   07004  37 0 132          STL OUTBF-3
454   07005  32 0 156 J        ENL PBUF)
455   07006  37 0 072          STL TBUF
456   07007  32 1 155 J        ENL PATTRN
457   07010  36 0 020          RJP S04
460   07011  32 0 154 J        ENL 12)
461   07012  37 1 153 J        STL BUFC
462   07013  36 1 152 J        RJP S03
463   07014  24 1 151 J        JMP P4
464
465
466
467   07015  32 0 063   ERRJR3 ENL ASR3              E3  PXXXXX  LXXXXX
470   07016  36 0 074          RJP S07
471   07017  24 1 150 J        JMP P41
472
473
474
475                                        UNPACK 5-DIGIT NUMBER FOR PRINTOUT
476   07020      00000   S04   ...
477   07021  37 0 073          STL 04T1
500   07022  12 0 147 J        BAND 30000)
501   07023  16 1 146 J        RSH ACC
502   07024  02 1 146          CMB ACC
503                            RPT 6
504   07025  16 1 146          RSH ACC
      07026  16 1 146
      07027  16 1 146
      07030  16 1 146
```

EXTENDED CORE MEMORY TEST

```
            07031  16 1 146
            07032  16 1 146
     505    07033  36 0 064          RJP S04A
     506    07034  12 0 145  J       &AND 7000)
     507                             RPT 4
     510    07035  16 1 146          RSH ACC
            07036  16 1 146
            07037  16 1 146
            07040  16 1 146
     511    07041  36 0 064          RJP S04A
     512    07042  12 0 144  J       &AND 700)
     513    07043  16 1 146          RSH ACC
     514    07044  36 0 064          RJP S04A
     515    07045  12 0 143  J       &AND 70)
     516                             RPT 2
     517    07046  14 1 146          LSH ACC
            07047  14 1 146
     520    07050  36 0 064          RJP S04A
     521    07051  12 0 142  J       &AND 7)
     522                             RPT 5
     523    07052  14 1 146          LSH ACC
            07053  14 1 146
            07054  14 1 146
            07055  14 1 146
            07056  14 1 146
     524    07057  36 0 064          RJP S04A
     525    07060  24 1 020          RTN
     526    07061     33040  ASR1   OCT 26100/2+20000      33040
     527    07062     33100  ASR2   OCT 26200/2+20000      33100
     530    07063     33140  ASR3   OCT 26300/2+20000      33140
     531
     532                                        CONVERT DIGIT TO ASCII CODE
     533    07064     00000  S04A   ...
     534    07065  10 0 136          ADD ASR0
     535    07066  37 1 072          STL TBUF,I
     536    07067  01 0 072          DCR TBUF
     537    07070  32 0 073          ENL 04T1
     540    07071  24 1 064          RTN
     541    07072     00000  TBUF   OCT
     542    07073     00000  04T1   OCT
```

EXTENDED CORE MEMORY TEST

```
543
544
545                                                    USED BY ERROR1 AND ERHOH3
546   07074      00000   S07     ...
547   07075   37 0 132           STL OUTBF-3
550   07076   32 0 141  /        ENL LBUF)
551   07077   37 0 072           STL TBUF
552   07100   32 1 140  /        ENL PSEUDP
553   07101   36 0 020           RJP S04
554   07102   32 0 156           ENL PBUF)
555   07103   37 0 072           STL TBUF
556   07104   32 1 155           ENL PATTRN
557   07105   36 0 020           RJP S04
560   07106   32 0 137  /        ENL 20)
561   07107   37 1 153           STL BUFC
562   07110   36 1 152           RJP S03
563   07111   24 1 074           RTN
564
565
566                                                          PRINT BUFFER
567   07112      00000           OCT                            X
570   07113      00000           OCT                            X
571   07114      00000           OCT                            X
572   07115      00000           OCT                            X
573   07116      00000   LBUF    OCT                            X
574   07117      34600           OCT 31400/2+20000              L
575   07120      32000           OCT 24000/2+20000              SP
576   07121      32000           OCT 24000/2+20000              SP
577   07122      00000           OCT                            X
600   07123      00000           OCT                            X
601   07124      00000           OCT                            X
602   07125      00000           OCT                            X
603   07126      00000   PBUF    OCT                            X
604   07127      35000           OCT 32000/2+20000              P
605   07130      32000           OCT 24000/2+20000              SP
606   07131      32000           OCT 24000/2+20000              SP
607   07132      00000           OCT                            1 OR 2      261/262
610   07133      34240           OCT 30500/2+20000              E
611   07134      30500           OCT 21200/2+20000              LP
612   07135      30640   OUTBF   OCT 21500/2+20000              CR
```

EXTENDED CORE MEMORY TEST

```
      613   07136     33000    ASR0    OCT 26000/2+20000       33000
            07137     00024             WRD
            07140     06605             WRD
            07141     07116             WRD
            07142     00007             WRD
            07143     00070             WRD
            07144     00700             WRD
            07145     07000             WRD
            07146     00101             WRD
            07147     30000             WRD
            07150     06530             WRD
            07151     06510             WRD
            07152     06665             WRD
            07153     06713             WRD
            07154     00014             WRD
            07155     06662             WRD
            07156     07126             WRD
            07157     06445             WRD
      614               00000             END
```

ASR PUNCH-READER TEST (D15A)

I. Purpose of Test

To verify the proper operation of the ASR punch and reader.

II. Description of Test

The program reads characters in ASCII code through the ASR reader until two terminating characters (minus sign and rub out) are read. Due to the mechanical design of the ASR set, the characters being read are also printed and punched at the same time.

After the terminating characters have been received, the entire character set that has been read and stored is punched and printed. Thus for both the read cycle and the punch cycle, a print record is generated. Errors may then be detected by visual inspection of these two print records. Inspection of the tape records punched may also be done, noting that there are two tape records for the read cycle (the ASR set punches as it reads) and one tape record for the punch cycle.

If more than 147 characters are input as a character set, all characters after the 147th character are ignored until the terminating characters are received. The number of read/punch cycles may be varied from 1 to 8191 times or the test may be set to run continuously. At the beginning of the test the ASR set is turned on in the prescribed manner by the test program, and when the number of cycles has been completed, the ASR set is turned off.

All interrupts are ignored while the test program is running except the ones corresponding to the ASR set which is being tested. The interrupts and channel numbers of the ASR set which are used in the test program must correspond with the existing hardware setup.

The minus sign is the terminating character which actually signals the end of the character set being read or punched. However, on the read cycle, the rub-out character (all ones) must follow the minus sign in order to clear the ASR buffer register for the output to follow.

III. Description of Operation

A. Punch an ASCII character set tape on the ASR punch, off-line mode, via the ASR keyboard. The tape must end with a minus sign and a rub-out character (all ones). A suggested character set is a carriage return, line feed, followed by:

ABCDEFGHIJKLMNOPQRSTUVWXYZ 0123456789!"#$%&'()*=: /;

and terminated by the rub-out character. Turn the ASR punch off and place the ASR switch in the OFF position after the character set is punched.

B. Read in the binary tape of the ASR Punch-Reader test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.

C. Enter the Test Parameters.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the S-Register with the parameter location.
3. Using the probe, load the X-Register with the parameter constant; depress the Start button.
4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Preset	Description
213_8	ASRILØ	10_8	ASR Input Interrupt Location
214_8	ASRØLØ	11_8	ASR Output Interrupt Location
215_8	ASRICH	1	ASR Input Channel
216_8	ASRØCH	0	ASR Output Channel
217_8	NUMTIM	100_{10}	Number of cycles to read and punch ($1-8191_{10}$, or zero).

D. Start the Test.

1. Put the beginning of the tape containing the character set from the ASR punch under the ASR reader and turn the ASR punch on.
2. Put machine in WRITE mode; depress the Master Clear button.
3. Using the probe, load the X-Register with the starting location of the test (101_8); depress the Start button.
4. Put machine in RUN mode; depress the Master Clear button.
5. Depress the Start button.

E. Normal Completion

1. The program will print and punch twice the number of records designated by NUMTIM and then stop with the S-Register (bits 0-7) containing one (1). If NUMTIM is equal to zero, the test will run continuously.
2. Proper operation is verified by visual inspection of the ASR printout from the initial character set. Note that turning the ASR off and on may punch a few rub-out characters on the tape. These should be ignored while checking the tape.
3. The program may be restarted by depressing the Master Clear and Start buttons.

F. Error Stop

1. If bits 0-5 of an input word are non-zero, the program will stop with the S-Register (bits 0-7) containing a two (2).
2. The accumulator may be examined to ascertain what illegal character was input. (Note: The reader inputs to bits 6-13 of the accumulator.)
3. The program may be restarted by executing steps 4 and 5 in Section III. D.

IV. Storage

Number of locations used: 362_8 (102_8-463_8).

PROJECT NO. 538053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512641

```
 1                                        ASR PUNCH-READER TEST
 2
 3                                        PROGRAM LIBRARY
 4                                        PROGRAM NO.   P-50  D15A
 5
 6
 7                                THE FOLLOWING ARE PROGRAM PARAMETERS:
10            00010   ASRIRT8EQU 10                 ASR INPUT INTERRUPT LOCATION
11            00011   ASRORT8EQU 11                 ASR OUTPUT INTERRUPT LOCATION
12            00001   ASRICN EQU 1                  ASR INPUT CHANNEL NUMBER
13            00000   ASROCN EQU 0                  ASR OUTPUT CHANNEL NUMBER
14            00144   TIMES  EQU 100                NUMBER OF LINES TO BE READ OR PUNCHED
15
16                          UNL
17            00102   ASRPRT ORG ACC+1
20  00102  32 0 226  /      8ENL 100)
21  00103  37 0 227          STL CHRSTO
22  00104  32 0 225  /      8ENL 23400)             STORE IGNORE INTERRUPTS (CLO ,I) IN ALL
23  00105  37 1 227   10ASRT STL CHRSTO,I             THE INTERRUPT LOCATIONS
24  00106  01 0 227          DCR CHRSTO
25  00107  27 0 104          PJP 10ASRT
26  00110  23 0 110          CLO L+1                 CLEAR LOCKOUT
27  00111  32 0 215          ENL ASRICH
30  00112  10 0 224  /      8ADD 30000)
31  00113  37 0 210          STL INTCOM              STORE PROPER CHANNEL IN INPUT COMMAND
32  00114  32 0 216          ENL ASROCH
33  00115  10 0 223  /      8ADD 34000)
34  00116  37 0 204          STL OUTCOM              STORE PROPER CHANNEL IN OUTPUT COMMAND
35  00117  32 0 217          ENL NUMTIM
36  00120  37 0 230          STL COUNT               SET MAXIMUM NUMBER OF LINES TO BE READ
37  00121  32 0 232          ENL OUTINS
40  00122  37 1 214          STL ASROLD,I            STORE OUTPUT INTERRUPT INSTRUCTION
41  00123  32 0 231          ENL INTINS
42  00124  37 1 213          STL ASRILD,I            STORE INPUT INTERRUPT INSTRUCTION
43  00125  32 0 222  /       ENL 12)
44  00126  37 0 227          STL CHRSTO
45  00127  32 0 237          ENL TURNON
46  00130  36 0 203   20ASRT RJP OUTONE              TURN ON ASR SET IN PRESCRIBED MANNER
47  00131  01 0 227          DCR CHRSTO
50  00132  27 0 127          PJP 20ASRT
```

PROJECT NO. 530353 PROGRAMMER E.E. O'HARE TAPE NUMBER 512641

```
 51                                    EJE
 52   00133  32 0 233   START  ENL STORAG
 53   00134  37 0 227          STL CHRSTO          SET CHARACTER STORAGE INDEX
 54   00135  36 0 207          RJP INTONE          IGNORE FIRST CHARACTER
 55   00136  36 0 207   INPUT  RJP INTONE          INPUT A CHARACTER
 56   00137  37 1 227          STL CHRSTO,I        STORE CHARACTER INPUT
 57   00140  12 0 221   J      BAND 77)            CHECK FOR ILLEGAL BITS SET (8-5)
 60   00141  20 0 146          ZJP CKMINS
 61   00142  32 1 227          ENL CHRSTO,I        BRING ILLEGAL CHARACTER TO ACCUMULATOR
 62   00143  00 0 002          STP 2               STOP WITH S-REGISTER SET TO A TWO
 63   00144  12 0 220   J      BAND 37700)
 64   00145  37 1 227          STL CHRSTO,I        STRIP OFF ILLEGAL BITS
 65   00146  23 0 147          CLJ L+2             CLEAR LOCKOUT ON A STOP
 66   00147  32 1 227   CKMINS ENL CHRSTO,I        CHECK FOR A MINUS SIGN
 67   00150  11 0 235          SUB MINUS
 70   00151  20 0 156          ZJP RESET           IT IS, EXIT TO OUTPUT
 71   00152  32 0 227          ENL CHRSTO
 72   00153  11 0 234          SUB LIMIT
 73   00154  20 0 135          ZJP INPUT           MAXIMUM NUMBER OF CHRS HAVE BEEN INPUT
 74   00155  01 0 227          DCR CHRSTO          DECREMENT CHARACTER STORAGE INDEX
 75   00156  24 0 135          JMP INPUT
 76   00157  32 0 233   RESET  ENL STORAG
 77   00160  37 0 227          STL CHRSTO          RESET CHARACTER STORAGE INDEX
100   00161  32 1 227   OUTPUT ENL CHRSTO,I
101   00162  16 0 101          RSH ACC             BRING CHARACTER AND SHIFT INTO POSITION
102   00163  36 0 203          RJP OUTONE          OUTPUT ONE CHARACTER
103   00164  32 1 227          ENL CHRSTO,I
104   00165  11 0 235          SUB MINUS
105   00166  20 0 170          ZJP RUBOUT          CHARACTER IS A MINUS SIGN, TEST COUNTER
106   00167  01 0 227          DCR CHRSTO          DECREMENT CHARACTER STORAGE INDEX
107   00170  24 0 160          JMP OUTPUT          OUTPUT NEXT CHARACTER
110   00171  32 0 237   RUBOUT ENL TURNON
111   00172  36 0 203          RJP OUTONE          OUTPUT A RUBOUT CHARACTER
112   00173  32 0 230          ENL COUNT
113   00174  20 0 132          ZJP START           IF COUNT IS ZERO, READ AND PUNCH CONTINUOS
114   00175  01 0 230          DCR COUNT           DECREMENT COUNTER
115   00176  27 0 132          PJP START           CONTINUE READING AND PUNCHING
116   00177  32 0 236          ENL TURNOF
117   00200  36 0 203          RJP OUTONE          TURN OFF ASR SET AND STOF WITH S-REG = 1
120   00201  00 0 001          STP 1
```

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512641

```
121   00202  24 0 101          JMP ASRPRT          REPEAT
122
123   00203      00000  OUTONE ...
124   00204  34 0 000   OUTCOM OUT **              OUTPUT A CHARACTER
125   00205  01 0 000          DCR PC              WAIT FOR INTERRUPT
126   00206  24 1 203   OPTRTN RTN                 INTERRUPT RETURN
127
130   00207      00000  INTONE ...
131   00210  30 0 000   INTCOM INT **              INPUT A CHARACTER
132   00211  01 0 000          DCR PC              WAIT FOR INTERRUPT
133   00212  24 1 207   IPTRTN RTN                 INTERRUPT RETURN
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 512641

```
134                                 EJE
135
136                                     THE FOLLOWING MAY BE PROGRAM INPUTS:
137   00213     00010   ASRILO OCT ASRIRT          ASR INPUT INTERRUPT LOCATION
140   00214     00011   ASROLO OCT ASRORT          ASR OUTPUT INTERRUPT LOCATION
141   00215     00001   ASRICH OCT ASRICN          ASR INPUT CHANNEL
142   00216     00000   ASROCH OCT ASROCN          ASR OUTPUT CHANNEL
143   00217     00144   NUMTIM OCT TIMES           NUMBER OF LINES TO BE READ OR PUNCHED
144
145                                 GEN
      00220     37700           WRD
      00221     00077           WRD
      00222     00014           WRD
      00223     34000           WRD
      00224     30000           WRD
      00225     23400           WRD
      00226     00100           WRD
```

PROJECT NO. 530053 PROGRAMMER E.E. O.HARE TAPE NUMBER 512641

```
146   00227      00000   CHRSTO OCT                  CHARACTER STORAGE INDEX
147   00230      00000   COUNT  OCT                  COUNTER FOR NUMBER OF LINES
150   00231  23 0 211    INTINS CLJ IPTRTN           INPUT INTERRUPT INSTRUCTION
151   00232  23 0 205    OUTINS CLJ OPTRTN           OUTPUT INTERRUPT INSTRUCTION
152   00233      00463   STORAG DEC BUFFER+147       BEGINNING OF BUFFER INDEX
153   00234      00240   LIMIT  DEC BUFFER           END OF BUFFER INDEX
154   00235      25500   MINUS  OCT 25500            ASR MINUS SIGN CODE
155   00236      17741   TURNOF OCT 17741            ASR TURN OFF CODE
156   00237      37740   TURNON OCT 37740            ASR TURN ON  CODE
157              00240   BUFFER SYN L                BUFFER STORAGE FOR CHARACTERS
160              00000          END
```

DATE 4/27/65. TIME 2/57/55 P.M.

PROJECT NO. 530053 PROGRAMMER E.E. O'HARE TAPE NUMBER 512641

STARTED 4/27/65. 2/57/08 P.M.
COMPLETED 4/27/65. 2/57/55 P.M.
NUMBER OF INPUT RECORDS 112.
NUMBER OF OUTPUT RECORDS 119.
NUMBER OF BINARY RECORDS 97.

HIGH SPEED PUNCH-READER TEST (D16A)

I. Purpose of Test

To verify the proper operation of the high speed punch and reader.

II. Description of Test

The test program begins by punching 12 blank characters (leader) and 255 data characters. After this paper tape has been punched, it should be placed in the high speed reader.

The program then reads the paper tape that has been punched and compares each character to the character used as data. If a character input is not the same as the data character, a punch or reader error has occurred and the program stops.

After reading the paper tape, the program repeats the punch cycle and the read cycle until both cycles has been performed eight times. (This number can be modified.) After eight times, the program stops.

All interrupts other than the punch and reader interrupts are ignored while the test is in progress. Interrupts and channel numbers used in the test program must correspond with the existing hardware setup.

III. Description of Operation

A. Read in the binary tape of the high speed punch-reader test using the bootstrapped binary loader.

1. Put machine in Write mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (7602_8, 17602_8, 27602_8, or 37602_8); depress the Start button.

3. Put machine in Run mode; depress the Master Clear button.

4. Place the binary tape under the tape reader.

5. Turn the reader on.

6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in Write mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter value; depress the Start button.

4. Repeat 2 and 3 until all the following parameters have been entered:

Location:	Preset:	Description:
174_8	PCHLØC 6	Punch Interrupt Location
175_8	RDRLØC 22_8	Reader Interrupt Location
176_8	PCHCHA 50_8	Punch Channel
177_8	RDRCHA 64_8	Reader Channel
200_8	NUMTIM 10_8	Number punch-reader cycles

NOTE: If zero is entered as the number of punch-reader cycles (location 200_8), the test will run continuously.

C. Start the Test

1. Put machine in Write mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the test (101_8); depress the Start button.
3. Put machine in Run mode; depress the Master Clear button.
4. Depress the Start button.

D. Normal Execution

1. After the punch completes one punch cycle, place the paper tape under the high speed reader; turn the reader on.
2. After the proper number of punch-reader cycles have been completed (location 200_8), the machine will stop with the S-Register (bits 0-7) containing one (1). If location 200_8 is zero, the test runs continuously.
3. The test may be restarted after a one stop by depressing the Master Clear and Start buttons.

E. Error Stop

1. If a character is mispunched or misread, the machine will stop with the S-Register (bits 0-7) containing two (2).
2. The accumulator (location 101_8) may be examined to ascertain what character was input. (Note that the reader inputs to bits 6-13 of the accumulator.)
3. The program may be restarted after a two stop by putting the machine in the Run mode and depressing the Master Clear and Start buttons.

IV. Storage

Number of locations used: 532_8 (102_8 - 633_8)

V. Run Time

Program runs at the speed of the high speed reader and punch.

Recommended Run Time: 25 minutes

HIGH SPEED PUNCH-READER TEST PROGRAM NO, P-50 D16A

```
 1                                                  HIGH SPEED PUNCH -READER TEST
 2
 3                                                  PROGRAM LIBRARY
 4                                                  PROGRAM NO, P-50 D16A
 5
 6
 7
10                                          THE FOLLOWING ARE PROGRAM PARAMETERS:
11              00006   PCHIRTB EQU 6               PUNCH  INTERRUPT LOCATION
12              00022   RDRIRTB EQU 22              READER INTERRUPT LOCATION
13              00050   PCHCHNB EQU 50              PUNCH CHANNEL NUMBER
14              00064   RDRCHNB EQU 64              READER CHANNEL NUMBER
15              00010   TIMES   EQU 8               NO, OF CYCLES TO BE READ OR PUNCHED
16
17                        UNL
20              00102   PNRUTT  ORG ACC+1
21   00102  32 0 217  /       BENL 100)
22   00103  37 0 203           STL BUFFER
23   00104  32 0 216  /       BENL 25400)          STORE IGNORE INTERRUPTS (CLJ ,I) IN ALL
24   00105  37 1 203   10RPT   STL BUFFER,I           THE INTERRUPT LOCATIONS
25   00106  01 0 203           DCR BUFFER
26   00107  27 0 104           PJP 10RPT
27   00110  23 0 110           CLJ L+1             RELEASE LOCKOUT
30   00111  32 0 177           ENL RDRCHA
31   00112  10 0 215  /       BADD 30000)
32   00113  37 0 153           STL INTCOM          STORE PROPER CHANNEL IN INPUT COMMAND
33   00114  32 0 176           ENL PCHCHA
34   00115  10 0 214  /       BADD 34000)
35   00116  37 0 142           STL OUTCOM          STORE PROPER CHANNEL IN OUTPUT COMMAND
36   00117  32 0 200           ENL NUMTIM
37   00120  37 0 204           STL COUNT           SET MAXIMUM NUMBER OF LINES TO BE READ
40   00121  32 0 213  /       ENL 1)
41   00122  37 0 205           STL FTIMFG          SET FIRST TIME FLAG TO IGNORE FIRST CHA
42   00123  32 0 202           ENL RDRINS
43   00124  37 1 175           STL RDRLOC,I        STORE READER INTERRUPT LOCATION
44   00125  32 0 201           ENL PCHINS
45   00126  37 1 174           STL PCHLOC,I        STORE PUNCH INTERRUPT LOCATION
```

HIGH SPEED PUNCH-READER TEST PROGRAM NO, P-50 D16A

```
 46                                    EJE
 47   00127  32 0 212  /CYCLE  ENL DATA+NBLNKS+OFF+1)
 50   00130  37 0 206           STL LENGTH          NUMBER OF CHARACTERS TO BE PUNCHED
 51   00131  32 0 211  /        ENL BASE+DATA+NBLNKS)
 52   00132  37 0 203           STL BUFFER          START OF PUNCH BUFFER
 53   00133  01 0 206   PCHRTN  DCR LENGTH
 54   00134  20 0 143           ZJP RESET           ONE PUNCH CYCLE DONE, GO TO READ CYCLE
 55   00135  01 0 203           DCR BUFFER
 56   00136  32 1 203           ENL BUFFER,I        ENTER CHARACTER
 57   00137  16 0 101           RSH ACC             POSITION CHARACTER
 60   00140  25 0 141           CJP OUTCOM          TURN OFF CHAR - DO NOT SET FEED BIT
 61   00141  03 0 101           SMB ACC             SET FEED BIT (BIT 13)
 62   00142  34 0 000   OUTCOM  OUT **             OUTPUT CHARACTER
 63   00143  01 0 000           DCR PC              WAIT FOR INTERRUPT
 64
 65   00144  32 0 210  /RESET   ENL DATA+1)
 66   00145  37 0 206           STL LENGTH          NUMBER OF CHARACTERS TO BE READ
 67   00146  32 0 207  /        ENL BASE+DATA)
 70   00147  37 0 203           STL BUFFER          START OF READER BUFFER
 71   00150  01 0 206   RDRLOP  DCR LENGTH
 72   00151  20 0 165           ZJP CNTEST          ONE READ CYCLE DONE, TEST COUNTER
 73   00152  01 0 203           DCR BUFFER          DECREMENT BUFFER INDEX
 74   00153  30 0 000   INTCOM  INT **             INPUT A CHARACTER
 75   00154  01 0 000           DCR PC              WAIT FOR INTERRUPT
 76   00155  01 0 205   RDRRTN  DCR FTIMFG
 77   00156  20 0 126           ZJP CYCLE           IGNORE FIRST GARBAGE CHARACTER
100   00157  37 0 205           STL FTIMFG          UNSET FIRST TIME FLAG
101   00160  11 1 203           SUB BUFFER,I
102   00161  20 0 147           ZJP RDRLOP          CHARACTER CHECKS WITH BUFFER CHARACTER
103   00162  10 1 203           ADD BUFFER,I
104   00163  20 0 152           ZJP INTCOM          CHARACTER IS A BLANK, IGNORE IT
105   00164  00 0 002           STP 2               CHARACTER DOES NOT CHECK WITH BUFFER CHR
106   00165  23 0 147           CLJ RDRLOP          CONTINUE CHECKING AFTER VISUAL INSPECTION
```

```
107                                     EJE
110   00166  32 0 204   CNTEST ENL COUNT
111   00167  20 0 126          ZJP CYCLE          IF NUMBER OF TIMES IS ZERO, TEST FOREVER
112   00170  01 0 204          DCR COUNT
113   00171  27 0 126          PJP CYCLE          REPEAT PUNCH AND READ CYCLE
114   00172  00 0 001          STP 1              DESIRED NUMBER OF CYCLES HAS BEEN COMPLETD
115   00173  24 0 101          JMP PNRDTT         RESTART TEST
116
117
120                                     THE FOLLOWING MAY BE PROGRAM INPUTS:
121   00174      00006   PCHLOC OCT PCHIRT         PUNCH  INTERRUPT LOCATION
122   00175      00022   RDRLOC OCT RDRIRT         READER INTERRUPT LOCATION
123   00176      00050   PCHCHA OCT PCHCHN         PUNCH  CHANNEL
124   00177      00064   RDRCHA OCT RDRCHN         READER CHANNEL
125   00200      00010   NUMTIM OCT TIMES          NUMBER OF CYCLES TO BE READ OR PUNCHED
126
127   00201  23 0 132   PCHINS CLJ PCHRIN         PUNCH  INTERRUPT INSTRUCTION
130   00202  23 0 154   RDRINS CLJ RDRRIN         READER INTERRUPT INSTRUCTION
131   00203      00000   BUFFER OCT                START OF PUNCH OR READER BUFFER
132   00204      00000   COUNT  OCT                NUMBER OF CYCLES COUNTER
133   00205      00000   FTIMFG OCT                FIRST TIME FLAG TO IGNORE GARBAGE CHAR
134   00206      00000   LENGTH OCT                LENGTH OF PUNCH OR READER BUFFER
135                                     GEN
      00207      00620          WRD
      00210      00400          WRD
      00211      00634          WRD
      00212      00415          WRD
      00213      00001          WRD
      00214      34000          WRD
      00215      30000          WRD
      00216      23400          WRD
      00217      00100          WRD
```

HIGH SPEED PUNCH-READER TEST PROGRAM NO, P-50 D16A

```
136                 00014   NBLNKS  EQU 12              NUMBER OF BLANKS FOR PUNCH TO WARM UP
137                 00377   DATA    EQU 255             NUMBER OF DATA CHRS TO BE READ OR PUNCHED
140                 00001   OFF     EQU 1               NUMBER OF TURN-OFF CHRS FOR PUNCH
141                                                     DATA BUFFER FOR PUNCH AND READER
142                                 RPT OFF
143   00220         00003           OCT 3               TURN OFF PUNCH  (BIT 0 = 1)
144
145                         BASE    RPT DATA
146   00221         00100           OCT L+1-BASE*100    DATA: 00000001,00000010,...,11111111(5-12)
147
150                                 RPT NBLNKS
151   00620         00000           OCT 0               TURN ON PUNCH AND PUNCH BLANK
152                 00000           END
```

MARK II ANALOG INPUT STATISTICAL TEST (D17B)

I. Purpose of Test

To read a variable number of analog points and print the test results on an ASR set.

II. Description of Test

From one to four vidars can be checked, with the following restrictions:

Test 1 vidar	Vidar #1 will be tested
Test 2 vidars	Vidars #1, #2 will be tested
Test 3 vidars	Vidars #1, #2, #3 will be tested

A maximum of 14 pounts per vidar can be checked.

The first 20 values and their frequency are recorded for each point. After every point has been read CYCLES (specified in initialization) times, the results are printed on the document device. If the span adjustment feature is selected, the span values are also printed on the document device.

The test can be operated with or without span adjustment. The last point specified for each vidar will be taken as the span calibrate point if this option is selected. This point must be short circuited for proper operation of span adjustment. Span point settings are printed every 8 readings if the span print option is selected. When the test has gone through the number of scan cycles specified by CYCLES, the data collected in the tables is output in the format below.

Col. 1	Col. 2	Col. 3	Col. 4	
00100	00100	00077	00077	The four columns are the span
00100	00100	00077	00077	point settings for the 4 vidars
00100	00100	00077	00077	being tested. Column 1 is for
00100	00100	00077	00077	vidar #4, column 2 is for vidar
00100	00100	00077	00077	#3, column 3 is for vidar #2, and
00100	00100	00077	00077	column 4 is for vidar #1.
00100	00100	00077	00077	
00100	00100	00077	00077	
10007	00033	17457	00001	Column 1 contains the reading
10010	00021			taken. No conversion is done and
10006	00020			the readings are the actual inputs.
10011	00003			
10005	00001			
10007	00041	17457	00002	Column 2 contains the frequency
10006	00022			at which each reading occurred.
10005	00001			
10010	00012			
10011	00002			
10007	00045	17357	00004	Column 3 contains the word and
10010	00017			channel address together with the
10006	00011			gain at which the point was read.
10005	00001			
10011	00002			
00002	00047	17357	00010	Column 4 contains the bit address.
00003	00025			
00001	00004			

Col. 1	Col. 2	Col. 3	Col. 4	
10010	00013	27257	00020	All numbers are octal. When more than one vidar is being tested, the readings for the highest numbered vidar are printed out first.
10005	00015			
10007	00017			
10004	00011			
10006	00017			
10003	00001			

III. Description of Operation

A. Read in the binary tape of the Analog Statistics Test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (7602_8, 17602_8, 27602_8, 37602_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Place the binary tape under the tape reader.

5. Turn on reader.

6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Preset	Description
100_8	ANLINT	2	Analog conversion complete interrupt Loc.
401_8	NUMTST	4	No. vidars to be tested
402_8	TYPCHN	0	Document device output channel
403_8	ASRINT	11_8	Document device output complete int. Loc.
404_8	VDRADR	14_{10}	No. points per vidar to be tested
405_8	CYCLES	100_8	No. cycles before printout
406_8	CYCTIM	10_{10}	Tenths sec. delay between scans
407_8	SPNSET	0	Zero to adjust span
410_8	SPNPRT	0	Zero to print span adjustment
411_8-427_8	ADRTB1	0	Gain, word, channel select control words for vidar no. 1
430-446	ADRTB2	0	Gain, word, channel select control words for vidar no. 2
447-465	ADRTB3	0	Gain, word, channel select control words for vidar no. 3
466-504	ADRTB4	0	Gain, word, channel select control words for vidar no. 4

Location		Preset	Description
505-523	BITAB1	0	Bit select control words for vidar no. 1
524-542	BITAB2	0	Bit select control words for vidar no. 2
543-561	BITAB3	0	Bit select control words for vidar no. 3
562-600	BITAB4	0	Bit select control words for vidar no. 4

The format for the gain, word, channel select control words is as follows:

Bits 13, 12	gain	Bit 13 = 1	50 mv	Bit 12 = 1	5 volts
Bits 11-6	word				
Bits 5-0	channel				

The bit select control words contain one bit set.

C. Start the test.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-register with the starting location of the test (600_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button; depress the Start button.

D. The test runs continuously, reading each point the desired number of times and printing out the data.

IV. Storage

The program uses 7140_8 locations (400_8-7537_8).

V. Run Time

Recommended run time: 4 hours.

```
        1                                   PROGRAM TITLE: P-50 MARK II ANALOG STATISTICAL TEST (D17B-1)
        2
        3                                   DATE: JUNE 1,1966
        4
        5                                   SOURCE COMPUTER: P-500, SYSTEMS LAB, NESAP 50/500
        6                                   OBJECT COMPUTER: P-50 MARK II SERIES
        7
       10                                   PROGRAMMER: C.VETTER
       11
       12                                   ABSTRACT: THIS PROGRAM IS A REVISION OF D17B, IN D17B-1
       13                                             THE ANALOG CONVERSION COMPLETE INTERRUPT
       14                                             INITIATES THE INPUT AFTER ALL VALUES HAVE BEEN
       15                                             STORED.  IN D17B NO VALUES ARE STORED UNTIL
       16                                             THE ANALOG CONVERSION COMPLETE INTERRUPT IS
       17                                             RECEIVED.  SEE DESCRIPTION OF SAME CODE NUMBER
       20                                             AVAILABLE FROM C.S.D. DRAFTING SECTION.
       21
       22                                   CODING: NOT STNDRD1 - REVISION OF D17A PROGRAMMED ORIGINALLY
       23                                           PRIOR TO STNDRD1.
```

```
                                EJE ASSEMBLY PARAMETERS

                                                THE FOLLOWING MAY BE CHANGED AT RUN TIME
00002   ANINT   EQU 2           ANALOG CONVERSION COMPLETE INTERRUPT LOCATION
00004   NUMVDR  EQU 4           MAXIMUM NO. VIDARS TO BE TESTED
00000   DOCOUT  EQU 0           DOCUMENT DEVICE OUTPUT CHANNEL
00011   DOCINT  EQU 11          DOCUMENT DEVICE OUTPUT COMPLETE INTERRUPT LOCATION
                                THE FOLLOWING MAY NOT BE CHANGED EXCEPT BY REASSEMBLY
00001   ASR     EQU 1           ASR=1 TO OUTPUT ON ASR SET, =0 TO OUTPUT ON SELECTRIC
00400   ORIGIN  EQU 400         PROGRAM ORIGIN
00016   VDRCH1  EQU 16          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 1
00036   VDRCH2  EQU 36          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 2
00056   VDRCH3  EQU 56          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 3
00076   VDRCH4  EQU 76          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 4
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
42                                  EJE
43                                  UNL
44              00400               ORG ORIGIN
45                                          THE FOLLOWING ARE INPUTS AT RUN TIME
46   00400      00002   ANLINT OCT  ANINT  ANALOG CONVERSION COMPLETE INTERRUPT LOCATION
47   00401      00004   NUMTST OCT  NUMVDR NUMBER OF VIDARS TO BE TESTED
50   00402      00000   TYPCHN OCT  DOCOUT DOCUMENT DEVICE OUTPUT CHANNEL
51   00403      00011   ASRINT OCT  DOCINT DOCUMENT DEVICE OUTPUT COMPLETE INTERRUPT LOCATION
52   00404      00016   VDRADR DEC  14     NUMBER OF POINTS PER VIDAR TO BE READ
53   00405      00100   CYCLES OCT  100    NUMBER OF READINGS PER POINT BEFORE PRINTOUT
54   00406      00012   CYCTIM DEC  10     CYCTIM*1/10 SEC. = TIME DELAY BEFORE NEXT READING OF
55                                                              ALL POINTS
56   00407      00000   SPNSET OCT         ZERO TO ADJUST SPAN,NON-ZERO TO SKIP SPAN ADJUST
57   00410      00000   SPNPRT OCT         ZERO TO PRINT  SPAN,NON-ZERO TO SKIP SPAN PRINT
60                          ADRTB1 RPT 15  WORD CHANNEL SELECT FOR VIDAR NO. 1
61   00411      00000          OCT
62                          ADRTB2 RPT 15  WORD CHANNEL SELECT FOR VIDAR NO. 2
63   00430      00000          OCT
64                          ADRTB3 RPT 15  WORD CHANNEL SELECT FOR VIDAR NO. 3
65   00447      00000          OCT
66                          ADRTB4 RPT 15  WORD CHANNEL SELECT FOR VIDAR NO. 4
67   00466      00000          OCT
70                          BITAB1 RPT 15  BIT SELECT FOR VIDAR NO. 1
71   00505      00000          OCT
72                          BITAB2 RPT 15  BIT SELECT FOR VIDAR NO. 2
73   00524      00000          OCT
74                          BITAB3 RPT 15  BIT SELECT FOR VIDAR NO. 3
75   00543      00000          OCT
76                          BITAB4 RPT 15  BIT SELECT FOR VIDAR NO. 4
77   00562      00000          OCT
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
100                                     EJE PROGRAM CONTROL
101
102   00601  22 0 201                   SLJ L+1             SET LOCKOUT
103   00602  36 1 376  J                RJP RESTRT          INITIALIZE PROGRAM
104   00603  36 0 223  ANALOG           RJP OUTANI          INPUT DATA,OUTPUT MULTIPLEXER ADDRESS
105   00604  16 0 352                   RSH IND
106   00605  27 0 216                   PJP FIRST           FIRST TIME - IGNORE INPUT
107   00606  24 0 206  1STCHG           JMP L+1             REPLACEABLE DURING INITIALIZATION
110                                     DLE 4-NUMVDR*2      STORE VALUES READ
111   00607  32 0 353                   ENL SAVE4
112   00610  36 1 375  J                RJP STORE
113   00611  32 0 354                   ENL SAVE3
114   00612  36 1 375                   RJP STORE
115   00613  32 0 355                   ENL SAVE2
116   00614  36 1 375                   RJP STORE
117   00615  32 0 356                   ENL SAVE1
120   00616  36 1 375                   RJP STORE
121   00617  03 0 352  FIRST            SMB IND
122   00620  16 0 351                   RSH ANT             WAIT FOR INTERRUPT
123   00621  27 0 202                   PJP ANALOG          RECYCLE
124   00622  24 0 217                   JMP L-2
```

```
125                                 EJE
126                                          THIS SUBROUTINE IS ENTERED AFTER ALL PREVIOUS
127                                          DATA HAS BEEN STORED AND THE ANALOG CONVERSION
130                                          COMPLETE INTERRUPT IS RECEIVED, IT INPUTS DATA
131                                          CURRENTLY ON THE DATA LINES AND STORES IT IN
132                                          TEMPORARY LOCATIONS FOR EACH VIDAR, IT THEN
133                                          OUTPUTS SPAN AND GAIN AND MULTIPLEXER ADDRESS
134                                          FOR NEXT POINTS.
135
136   00623      00000   OUTANI ...
137   00624   03 0 351           SMB ANT
140   00625   24 0 225   2NDCHG  JMP L+1          REPLACEABLE DURING INITIALIZATION
141                              DLE 4-NUMVDR*2    INPUT CURRENT DATA AND STORE TEMPORARILY
142   00626   30 0 076           INP VDRCH4
143   00627   37 0 353           STL SAVE4
144   00630   30 0 056           INP VDRCH3
145   00631   37 0 354           STL SAVE3
146   00632   30 0 036           INP VDRCH2
147   00633   37 0 355           STL SAVE2
150   00634   30 0 016           INP VDRCH1
151   00635   37 0 356           STL SAVE1
152   00636   32 0 374   /       BENL 200)         OUTPUT SPAN AND GAIN FOR NEXT POINTS
153   00637   24 0 237   3RDCHG  JMP L+1          REPLACABLE DURING INITIALIZATION
154                              DLE 4-NUMVDR           RESET SPAN
155   00640   34 0 076           OUT VDRCH4
156   00641   34 0 056           OUT VDRCH3
157   00642   34 0 036           OUT VDRCH2
160   00643   34 0 016           OUT VDRCH1
161                              DLE 4-NUMVDR*4         PICK UP GAIN
162   00644   32 0 307           ENL LADR4
163   00645   12 0 373   /       BAND 377)
164   00646   10 0 372   /       BADD 32000)
165   00647   37 0 265           STL GAIN4
166   00650   32 0 311           ENL LADR3
167   00651   12 0 373           BAND 377)
170   00652   10 0 372           BADD 32000)
171   00653   37 0 271           STL GAIN3
172   00654   32 0 313           ENL LADR2
173   00655   12 0 373           BAND 377)
174   00656   10 0 372           BADD 32000)
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
      175   00657  37 0 275           STL GAIN2
      176   00660  32 0 315           ENL LADR1
      177   00661  12 0 373          8AND 377)
      200   00662  10 0 372          8ADD 32000)
      201   00663  37 0 301           STL GAIN1
      202   00664  24 0 264  4THCHG   JMP L+1          REPLACEABLE DURING INITIALIZATION
      203                             DLE 4-NUMVDR*4          OUTPUT SPAN AND GAIN
      204   00665  32 0 066  GAIN4    ENL ADRTB4
      205   00666  12 0 371  /        8AND 30000)
      206   00667  10 1 370  /         ADD SPWRD4
      207   00670  34 0 076           OUT VDRCH4
      210   00671  32 0 047  GAIN3    ENL ADRTB3
      211   00672  12 0 371          8AND 30000)
      212   00673  10 1 367  /         ADD SPWRD3
      213   00674  34 0 056           OUT VDRCH3
      214   00675  32 0 030  GAIN2    ENL ADRTB2
      215   00676  12 0 371          8AND 30000)
      216   00677  10 1 366  /         ADD SPWRD2
      217   00700  34 0 036           OUT VDRCH2
      220   00701  32 0 011  GAIN1    ENL ADRTB1
      221   00702  12 0 371          8AND 30000)
      222   00703  10 1 365  /         ADD SPWRD1
      223   00704  34 0 016           OUT VDRCH1
      224   00705  24 0 305  5THCHG   JMP L+1          REPLACEABLE DURING INITIALIZATION
      225                             DLE 4-NUMVDR*2  OUTPUT MULTIPLEXER ADDRESSES FOR NEXT POINTS
      226   00706  32 0 162           ENL BITAB4
      227   00707  34 1 066  LADR4    OUT ADRTB4,I
      230   00710  32 0 143           ENL BITAB3
      231   00711  34 1 047  LADR3    OUT ADRTB3,I
      232   00712  32 0 124           ENL BITAB2
      233   00713  34 1 030  LADR2    OUT ADRTB2,I
      234   00714  32 0 105           ENL BITAB1
      235   00715  34 1 011  LADR1    OUT ADRTB1,I
      236   00716  32 0 364  /        8ENL 400)          OUTPUT TO TRIGGER ANALOG CONVERSION
      237   00717  34 0 016           OUT VDRCH1
      240                             DLE 4-NUMVDR*6  UPDATE POINT ADDRESSES
      241   00720  32 0 306           ENL LADR4-1
      242   00721  10 0 363  /         ADD 1)
      243   00722  37 0 306           STL LADR4-1
      244   00723  32 0 307           ENL LADR4
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

```
245   00724   10 0 363            ADD 1)
246   00725   37 0 307            STL LADR4
247   00726   32 0 310            ENL LADR3-1
250   00727   10 0 363            ADD 1)
251   00730   37 0 310            STL LADR3-1
252   00731   32 0 311            ENL LADR3
253   00732   10 0 363            ADD 1)
254   00733   37 0 311            STL LADR3
255   00734   32 0 312            ENL LADR2-1
256   00735   10 0 363            ADD 1)
257   00736   37 0 312            STL LADR2-1
260   00737   32 0 313            ENL LADR2
261   00740   10 0 363            ADD 1)
262   00741   37 0 313            STL LADR2
263   00742   32 0 314            ENL LADR1-1
264   00743   10 0 363            ADD 1)
265   00744   37 0 314            STL LADR1-1
266   00745   32 0 315            ENL LADR1
267   00746   10 0 363            ADD 1)
270   00747   37 0 315            STL LADR1
271   00750   24 1 223            RTN
272
273   00751       00000   ANT     OCT
274   00752       00000   IND     OCT
275                               DLE 4-NUMVDR
276   00753       00000   SAVE4   OCT
277   00754       00000   SAVE3   OCT
300   00755       00000   SAVE2   OCT
301   00756       00000   SAVE1   OCT
302                               DLE 4-NUMVDR
303   00757   32 0 163    BITFX4  ENL BITAB4+1
304   00760   32 0 144    BITFX3  ENL BITAB3+1
305   00761   32 0 125    BITFX2  ENL BITAB2+1
306   00762   32 0 106    BITFX1  ENL BITAB1+1
```

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P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

307

		EJE
00763	00001	WRD
00764	00400	WRD
00765	02162	WRD
00766	02161	WRD
00767	02160	WRD
00770	02157	WRD
00771	30000	WRD
00772	32000	WRD
00773	00377	WRD
00774	00200	WRD
00775	01400	WRD
00776	01000	WRD

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

```
310                 01000           ORG ORIGIN+256
311                                         THIS SUBROUTINE INITIALIZES THE INTERRUPTS AND
312                                         THE TEST PROGRAM TO START OR RESTART THE TEST.
313   01000       00000   RESTRT ...
314   01001   32 1 370 /          ENL TYPCHN
315   01002   10 0 367 /        &ADD 3400U)
316   01003   37 1 366 /          STL OUT+1           INITIALIZE DOCUMENT DEVICE OUTPUT CHANNEL
317   01004   32 1 365 /          ENL ASRINT
320   01005   37 0 276            STL TYPINT          INITIALIZE DOCUMENT DEVICE INTERRUPT LOCATION
321   01006   32 1 364 /          ENL ANLINT
322   01007   37 0 272            STL INTLUC          INITIALIZE ANALOG CONVERSION COMPLETE INT. LOC.
323   01010   32 0 363 /        &ENL 100)             STORE IGNORE INTERRUPTS IN ALL LOCATIONS
324   01011   37 0 273            STL LSTINT
325   01012   32 0 271            ENL CLJ01
326   01013   37 1 273            STL LSTINT,I
327   01014   01 0 273            DCR LSTINT
330   01015   27 0 012            PJP L-2
331   01016   23 0 016            CLJ L+1             CLEAR LOCKOUT
332   01017   32 0 276            ENL TYPINT          STORE TYPER INTERRUPT JUMP LOCATION
333   01020   10 0 362 /          ADD 65)
334   01021   37 0 274            STL RND
335   01022   32 0 361 /          ENL INTRIN-1)
336   01023   37 1 274            STL RND,I
337   01024   32 0 271            ENL CLJ01           STORE JUMP IN TYPER INTERRUPT LOCATION
340   01025   10 0 276            ADD TYPINT
341   01026   10 0 362            ADD 65)
342   01027   37 1 276            STL TYPINT,I
343   01030   32 0 272            ENL INTLUC          STORE ANALOG INTERRUPT JUMP LOCATION
344   01031   10 0 362            ADD 65)
345   01032   37 0 274            STL RND
346   01033   32 0 360 /          ENL ANLNT)
347   01034   37 1 274            STL RND,I
350   01035   32 0 270            ENL RJPINS          STORE RETURN JUMP IN ANALOG INTERRUPT LOCATION
351   01036   10 0 272            ADD INTLUC
352   01037   10 0 362            ADD 65)
353   01040   37 1 272            STL INTLUC,I
354   01041   32 1 357 /          ENL CYCLES          NO. CYCLES BEFORE PRINTOUT
355   01042   37 1 356 /          STL PRTOUT
356   01043   32 0 355 /          ENL 8)              INITIALIZE CYCLE COUNT FOR SPAN ADJUST
357   01044   37 1 354 /          STL SPNCNT
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

```
360   01045  32 1 353  /      ENL NUMTST        CALCULATE TOTAL NO. POINTS TO BE TESTED
361   01046  37 0 274         STL RND
362   01047  32 0 352  /      ENL 0)
363   01050  10 1 351  /      ADD VDRADR
364   01051  01 0 274         DCR RND
365   01052  27 0 047         PJP L-2
366   01053  37 1 350  /      STL TOTADR
367   01054  37 1 347  /      STL FINCNT
370   01055  32 1 353         ENL NUMTST        MODIFY CONSTANT 20DCR
371   01056  01 1 362         DCR ACC
372   01057  37 0 274         STL RND
373   01060  14 1 352         LSH ACC
374   01061  14 1 362         LSH ACC
375   01062  10 0 274         ADD RND
376   01063  14 1 362         LSH ACC
377   01064  14 1 362         LSH ACC
400   01065  37 1 346  /      STL 20DCR
401   01066  32 0 352         ENL 0)            INITIALIZE SPAN ADJUST WORDS TO ZERO
402                           DLE 4-NUMVDR
403   01067  37 1 345  /      STL SPAN4
404   01070  37 1 344  /      STL SPAN3
405   01071  37 1 343  /      STL SPAN2
406   01072  37 1 342  /      STL SPAN1
407   01073  32 0 275         ENL SPINIT        SET INITIAL SPAN VALUE
410                           DLE 4-NUMVDR
411   01074  37 1 341  /      STL SPWRD4
412   01075  37 1 340  /      STL SPWRD3
413   01076  37 1 337  /      STL SPWRD2
414   01077  37 1 336  /      STL SPWRD1
415   01100  03 1 335  /      SMB ANT           CLEAR ANALOG INTERRUPT INDICATOR
416   01101  02 1 334  /      CMB IND           SET FIRST READ INDICATOR
417                           DLE 4-NUMVDR*10   STORE FIRST POINT AND BIT ADDRESS FOLLOWING LAST
420   01102  32 1 351         ENL VDRADR
421   01103  10 0 333  /      ADD ADRTB4)
422   01104  37 0 274         STL RND
423   01105  32 1 333         ENL ADRTB4
424   01106  37 1 274         STL RND,I
425   01107  32 1 351         ENL VDRADR
426   01110  10 0 332  /      ADD BITAB4)
427   01111  37 0 274         STL RND
```

```
430   01112  32 1 332          ENL BITAB4
431   01113  37 1 274          STL RND,I
432   01114  32 1 351          ENL VDRADR
433   01115  10 0 331  /       ADD ADRTB3)
434   01116  37 0 274          STL RND
435   01117  32 1 331          ENL ADRTB3
436   01120  37 1 274          STL RND,I
437   01121  32 1 351          ENL VDRADR
440   01122  10 0 330  /       ADD BITAB3)
441   01123  37 0 274          STL RND
442   01124  32 1 330          ENL BITAB3
443   01125  37 1 274          STL RND,I
444   01126  32 1 351          ENL VDRADR
445   01127  10 0 327  /       ADD ADRTB2)
446   01130  37 0 274          STL RND
447   01131  32 1 327          ENL ADRTB2
450   01132  37 1 274          STL RND,I
451   01133  32 1 351          ENL VDRADR
452   01134  10 0 326  /       ADD BITAB2)
453   01135  37 0 274          STL RND
454   01136  32 1 326          ENL BITAB2
455   01137  37 1 274          STL RND,I
456   01140  32 1 351          ENL VDRADR
457   01141  10 0 325  /       ADD ADRTB1)
460   01142  37 0 274          STL RND
461   01143  32 1 325          ENL ADRTB1
462   01144  37 1 274          STL RND,I
463   01145  32 1 351          ENL VDRADR
464   01146  10 0 324  /       ADD BITAB1)
465   01147  37 0 274          STL RND
466   01150  32 1 324          ENL BITAB1
467   01151  37 1 274          STL RND,I
470   01152  56 1 323  /       RJP REINIT        REINITIALIZE TABLE POINTERS
471   01153  56 1 322  /       RJP CLTAB         STORE ZEROS IN TABLES
472                            DLE 4-NUMVDR*2
473   01154  01 1 321  /       DCR LADR4
474   01155  01 1 320  /       DCR LADR4-1
475   01156  01 1 317  /       DCR LADR3
476   01157  01 1 316  /       DCR LADR3-1
477   01160  01 1 315  /       DCR LADR2
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
500   01161   01 1 314  ✓      DCR LADR2-1
501   01162   01 1 313  ✓      DCR LADR1
502   01163   01 1 312  ✓      DCR LADR1-1
503   01164   32 1 353         ENL NUMTST        1ST CHANGE - IN CONTROL SECTION
504   01165   13 1 311  ✓      EOR ALONES
505   01166   10 0 310  ✓      ADD NUMVDR)
506   01167   14 1 362         LSH ACC
507   01170   10 0 307  ✓      ADD 1STCHG)
510   01171   12 0 306  ✓     8AND 377)
511   01172   10 0 305  ✓     8ADD 24000)
512   01173   37 1 307         STL 1STCHG
513   01174   32 1 353         ENL NUMTST        2ND CHANGE - IN OUTANI
514   01175   13 1 311         EOR ALONES
515   01176   10 0 310         ADD NUMVDR)
516   01177   14 1 362         LSH ACC
517   01200   10 0 304  ✓      ADD 2NDCHG)
520   01201   12 0 306        8AND 377)
521   01202   10 0 305        8ADD 24000)
522   01203   37 1 304         STL 2NDCHG
523   01204   32 1 353         ENL NUMTST        3RD CHANGE - IN OUTANI
524   01205   13 1 311         EOR ALONES
525   01206   10 0 310         ADD NUMVDR)
526   01207   10 0 303  ✓      ADD 3RDCHG)
527   01210   12 0 306        8AND 377)
530   01211   10 0 305        8ADD 24000)
531   01212   37 1 303         STL 3RDCHG
532   01213   32 1 353         ENL NUMTST        4TH CHANGE - IN OUTANI
533   01214   13 1 311         EOR ALONES
534   01215   10 0 310         ADD NUMVDR)
535   01216   14 1 362         LSH ACC
536   01217   14 1 362         LSH ACC
537   01220   10 0 302  ✓      ADD 4THCHG)
540   01221   12 0 306        8AND 377)
541   01222   10 0 305        8ADD 24000)
542   01223   37 1 302         STL 4THCHG
543   01224   32 1 353         ENL NUMTST        5TH CHANGE - IN OUTANI
544   01225   13 1 311         EOR ALONES
545   01226   10 0 310         ADD NUMVDR)
546   01227   14 1 362         LSH ACC
547   01230   10 0 301  ✓      ADD 5THCHG)
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
      550   01231  12 0 306          BAND 377)
      551   01232  10 0 305          BADD 24000)
      552   01233  37 1 301           STL 5THCHG
      553   01234  32 1 353           ENL NUMTST        6TH CHANGE - IN ADJSPN
      554   01235  13 1 311           EOR ALONES
      555   01236  10 0 310           ADD NUMVDR)
      556   01237  37 0 274           STL RND
      557   01240  14 1 362           LSH ACC
      560   01241  10 0 274           ADD RND
      561   01242  14 1 362           LSH ACC
      562   01243  10 0 274           ADD RND
      563   01244  10 0 300  J        ADD 6THCHG)
      564   01245  12 0 306          BAND 377)
      565   01246  10 0 305          BADD 24000)
      566   01247  37 1 300           STL 6THCHG
      567   01250  32 1 353           ENL NUMTST        7TH CHANGE - IN ADJSPN
      570   01251  13 1 311           EOR ALONES
      571   01252  10 0 310           ADD NUMVDR)
      572   01253  37 0 274           STL RND
      573   01254  14 1 362           LSH ACC
      574   01255  10 0 274           ADD RND
      575   01256  10 0 277  J        ADD 7THCHG)
      576   01257  12 0 306          BAND 377)
      577   01260  10 0 305          BADD 24000)
      600   01261  37 1 277           STL 7THCHG
      601   01262  24 1 000           RTN
      602
      603   01263     00000   ANLNT  ...               ANALOG INTERRUPT ROUTINE
      604   01264  06 0 274          SDR RND
      605   01265  02 1 335          CMB ANT
      606   01266  05 0 274          EDR RND
      607   01267  23 1 263          CLJ ANLNT,I
      610
I     611   01270  36 1 000  RJPINS RJP ,I
I     612   01271  23 1 000  CLJ0I  CLJ ,I
      613   01272     00002  INTLOC OCT ANINT
      614   01273     00100  LSTINT OCT 100
      615   01274     00000  RND    OCT
      616   01275     00100  SPINIT OCT 100
      617   01276     00011  TYPINT OCT DOCINT
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
      620                                EJE
            01277      02133            WRD
            01300      02042            WRD
            01301      00705            WRD
            01302      00664            WRD
            01303      00637            WRD
            01304      00625            WRD
            01305      24000            WRD
            01306      00377            WRD
            01307      00606            WRD
            01310      00004            WRD
            01311      02150            WRD
            01312      00714            WRD
            01313      00715            WRD
            01314      00712            WRD
            01315      00713            WRD
            01316      00710            WRD
            01317      00711            WRD
            01320      00706            WRD
            01321      00707            WRD
            01322      01720            WRD
            01323      01655            WRD
            01324      00505            WRD
            01325      00411            WRD
            01326      00524            WRD
            01327      00430            WRD
            01330      00543            WRD
            01331      00447            WRD
            01332      00562            WRD
            01333      00466            WRD
            01334      00752            WRD
            01335      00751            WRD
            01336      02162            WRD
            01337      02161            WRD
            01340      02160            WRD
            01341      02157            WRD
            01342      02155            WRD
            01343      02154            WRD
            01344      02153            WRD
            01345      02152            WRD
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

01346	01647	WRD
01347	01462	WRD
01350	01467	WRD
01351	00404	WRD
01352	00000	WRD
01353	00401	WRD
01354	02156	WRD
01355	00010	WRD
01356	01464	WRD
01357	00405	WRD
01360	01263	WRD
01361	02423	WRD
01362	00101	WRD
01363	00100	WRD
01364	00400	WRD
01365	00403	WRD
01366	02421	WRD
01367	34000	WRD
01370	00402	WRD

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

```
621                 01400           ORG ORIGIN+512
622                                         THIS SUBROUTINE UPDATES THE STATISTICS TABLES
623                                         AFTER EACH CONVERSION, IF POINTS HAVE BEEN READ
624                                         CYCLES TIMES,PROGRAM GOES TO PRINT ROUTINE.
625
626   01400       00000   STORE   ...
627   01401   37  0 063            STL INPSAV          SAVE VALUE READ
630   01402   32  1 317            ENL LNORDG,I        NUMBER OF READINGS ALREADY STORED
631   01403   11  0 060            SUB D20
632   01404   37  0 066            STL REMCNT
633   01405   32  1 317            ENL LNORDG,I
634   01406   37  0 065            STL RDGCNT
635   01407   20  0 022            ZJP 1STSTR          FIRST READING OF A POINT
636   01410   32  0 063   COMPAR   ENL INPSAV          HAS VALUE ALREADY BEEN STORED ?
637   01411   13  1 315            EOR LREDNG,I
640   01412   27  0 013            PJP L+2
641   01413   24  0 014            JMP L+2
642   01414   20  0 025            ZJP SAVE            YES
643   01415   01  0 315            DCR LREDNG          NO
644   01416   01  0 313            DCR LFREQ
645   01417   01  0 065            DCR RDGCNT
646   01420   27  0 007            PJP COMPAR
647   01421   32  0 066            ENL REMCNT
650   01422   20  0 042            ZJP NOROOM          NO ROOM FOR ADDITIONAL VALUES
651   01423   32  0 061   1STSTR   ENL ONE             NEW VALUE TO BE STORED
652   01424   10  1 317            ADD LNORDG,I
653   01425   37  1 317            STL LNORDG,I
654   01426   32  0 061   SAVE     ENL ONE             INCREMENT FREQUENCY
655   01427   10  1 313            ADD LFREQ,I
656   01430   37  1 313            STL LFREQ,I
657   01431   32  0 063            ENL INPSAV          STORE VALUE
660   01432   37  1 315            STL LREDNG,I
661   01433   32  0 066            ENL REMCNT
662   01434   11  0 065            SUB RDGCNT
663   01435   37  0 066            STL REMCNT
664   01436   10  0 315            ADD LREDNG          ADJUST READING TABLE START TO NEXT VIDAR
665   01437   37  0 315            STL LREDNG
666   01440   32  0 066            ENL REMCNT
667   01441   10  0 313            ADD LFREQ           ADJUST FREQUENCY TABLE START TO NEXT VIDAR
670   01442   37  0 313            STL LFREQ
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
671   01443  01 0 317   NOROOM DCR LNORDG      NO ROOM FOR ADDITIONAL VALUES
672   01444  01 0 062          DCR FINCNT
673   01445  27 0 046          PJP L+2
674   01446  24 0 047          JMP L+2
675   01447  24 1 000          RTN
676   01450  36 1 366  J       RJP ADJSPN      RECORD SPAN CALIBRATE POINT READINGS
677   01451  36 0 255          RJP REINIT      INITIALIZE TABLE POINTERS
700   01452  32 0 067          ENL TOTADR
701   01453  37 0 062          STL FINCNT      TOTAL NUMBER OF POINTS TO BE TESTED
702   01454  01 0 064          DCR PRTOUT
703   01455  27 0 056          PJP L+2
704   01456  36 0 070          RJP PRINT
705   01457  24 1 000          RTN
706
707   01460     00024  D20     DEC 20
710   01461     00001  ONE     OCT 1
711   01462     00000  FINCNT  OCT
712   01463     00000  INPSAV  OCT
713   01464     00000  PRTOUT  OCT
714   01465     00000  RDGCNT  OCT
715   01466     00000  REMCNT  OCT
716   01467     00000  TOTADR  OCT
```

```
717                                     EJE
720                                             THIS SUBROUTINE PRINTS OUT THE ACCUMULATED DATA
721                                             FROM THE TABLES,THEN REINITIALIZES PROGRAM.
722
723   01470       00000   PRINT   ...
724   01471   22  0 071           SLJ L+1             SET LOCKOUT
725   01472   32  1 365   /       ENL CYCLES          INITIALIZE CYCLE COUNT
726   01473   37  0 064           STL PRTOUT
727   01474   36  1 364   /       RJP CARRTN          OUTPUT CARRIAGE RETURN
730   01475   32  1 363   /       ENL NUMTST          NUMBER OF VIDARS BEING TESTED
731   01476   37  0 254           STL VDRCNT
732   01477   02  0 251           CMB FRST            SET FIRST LINE INDICATOR
733   01500   32  1 362  /VIDRD   ENL VDRADR          NUMBER OF POINTS/VIDAR BEING TESTED
734   01501   37  0 252           STL SINGCT
735   01502   32  0 361   /       ENL ADRTB-1)
736   01503   10  0 254           ADD VDRCNT
737   01504   37  0 253           STL TEMP
740   01505   32  1 253           ENL TEMP,I          GAIN,WORD,CHANNEL OF READINGS
741   01506   37  0 245           STL ADRES
742   01507   32  0 360   /       ENL BITAB-1)
743   01510   10  0 254           ADD VDRCNT
744   01511   37  0 253           STL TEMP
745   01512   32  1 253           ENL TEMP,I          BIT OF READINGS
746   01513   37  0 246           STL BIT
747   01514   32  1 317   PNTRD   ENL LNORDG,I        NUMBER OF READINGS AT THIS POINT
750   01515   37  0 065           STL RDGCNT
751   01516   32  0 060           ENL D20
752   01517   11  1 317           SUB LNORDG,I        NUMBER OF UNUSED READING LOCATIONS
753   01520   37  0 250           STL EMPTY
754   01521   32  0 317           ENL LNORDG          STARTING LOCATION OF NO. OF READINGS POINTER
755   01522   11  1 363           SUB NUMTST
756   01523   37  0 317           STL LNORDG
757   01524   32  1 315   VALFND  ENL LREDNG,I        VALUE
760   01525   36  1 357   /       RJP OUTPUT
761   01526   36  1 356   /       RJP SPACER
762   01527   32  1 313           ENL LFREQ,I         FREQUENCY
763   01530   36  1 357           RJP OUTPUT
764   01531   16  0 251           RSB FRST
765   01532   27  0 134           RJP ADRFND
766   01533   36  1 354           RJP CARRTN
```

```
  767   01534  24 0 156          JMP NEXT
  770   01535  56 1 356  ADRFND  RJP SPACER
  771   01536  03 0 251          SMB FRST          CLEAR FIRST LINE INDICATOR
  772   01537  32 1 245          ENL ADRES,I       GAIN,WORD,CHANNEL
  773   01540  56 1 357          RJP OUTPUT
  774   01541  32 1 355  J       ENL SPACE
  775   01542  56 1 354  J       RJP OUT
  776   01543  56 1 356          RJP SPACER
  777   01544  32 1 246          ENL BIT,I         BIT
 1000   01545  56 1 357          RJP OUTPUT
 1001   01546  32 1 355          ENL SPACE
 1002   01547  56 1 354          RJP OUT
 1003   01550  56 1 364          RJP CARRIN
 1004   01551  32 0 245          ENL ADRES
 1005   01552  10 0 353  J       ADD 1)
 1006   01553  37 0 245          STL ADRES
 1007   01554  32 0 246          ENL BIT
 1010   01555  10 0 353          ADD 1)
 1011   01556  37 0 246          STL BIT
 1012   01557  01 0 315  NEXT    DCR LREDNG
 1013   01560  01 0 313          DCR LFREQ
 1014   01561  01 0 065          DCR RDGCNT
 1015   01562  20 0 163          ZJP CRTN
 1016   01563  24 0 123          JMP VALFND
 1017   01564  56 1 364  CRTN    RJP CARRIN
 1020   01565  32 0 315          ENL LREDNG        ADJUST READING TABLE TO NEXT POINT OF VIDAR
 1021   01566  11 0 250          SUB EMPTY
 1022   01567  11 0 247          SUB 20DCR
 1023   01570  37 0 315          STL LREDNG
 1024   01571  32 0 313          ENL LFREQ         ADJUST FREQUENCY TABLE TO NEXT POINT OF VIDAR
 1025   01572  11 0 250          SUB EMPTY
 1026   01573  11 0 247          SUB 20DCR
 1027   01574  37 0 313          STL LFREQ
 1030   01575  02 0 251          CMB FRST          SET FIRST LINE INDICATOR
 1031   01576  01 0 062          DCR FINCNT
 1032   01577  20 0 227          ZJP OUTFIN        OUTPUT FOR ALL VIDARS FINISHED
 1033   01600  01 0 252          DCR SINGCT
 1034   01601  27 0 113          RJP PNTRD         PRINT DATA FOR NEXT POINT OF VIDAR
 1035   01602  56 0 255          RJP REINIT        INITIALIZE VALUE AND FREQUENCY POINTERS
 1036   01603  01 0 254          DCR VDRCNT
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
1037   01604   32 1 363          ENL NUMTST
1040   01605   11 0 254          SUB VDRCNT
1041   01606   37 0 253          STL TEMP
1042   01607   32 0 317          ENL LNORDG
1043   01610   11 0 253          SUB TEMP
1044   01611   37 0 317          STL LNORDG      INITIALIZE NUMBER OF READINGS POINTER
1045   01612   32 0 253          ENL TEMP
1046   01613   14 1 352  /       LSH ACC
1047   01614   14 1 352          LSH ACC
1050   01615   10 0 253          ADD TEMP
1051   01616   14 1 352          LSH ACC
1052   01617   14 1 352          LSH ACC
1053   01620   37 0 253          STL TEMP        *20
1054   01621   32 0 315          ENL LREDNG
1055   01622   11 0 253          SUB TEMP
1056   01623   37 0 315          STL LREDNG      SET READING POINTER FOR NEXT VIDAR
1057   01624   32 0 313          ENL LFREQ
1060   01625   11 0 253          SUB TEMP
1061   01626   37 0 313          STL LFREQ       SET FREQUENCY POINTER FOR NEXT VIDAR
1062   01627   24 0 077          JMP VIDRD       PRINT DATA FOR NEXT VIDAR
1063   01630   36 0 255  OUTFIN  RJP REINIT      OUTPUT FOR ALL VIDARS FINISHED
1064   01631   36 0 320          RJP CLTAB       CLEAR FREQUENCY TABLE TO ZERO
1065   01632   32 0 067          ENL TOTADR
1066   01633   37 0 062          STL FINCNT
1067   01634   24 1 070          RTN
1070
1071   01635      00411  ADRTB   OCT ADRTB1
1072   01636      00430          OCT ADRTB2
1073   01637      00447          OCT ADRTB3
1074   01640      00466          OCT ADRTB4
1075   01641      00505  BITAB   OCT BITAB1
1076   01642      00524          OCT BITAB2
1077   01643      00543          OCT BITAB3
1100   01644      00562          OCT BITAB4
1101   01645      00000  ADRES   OCT
1102   01646      00000  BIT     OCT
1103   01647      00074  20DCR   DEC NUMVDR-1*20
1104   01650      00000  EMPTY   OCT
1105   01651      00000  FRST    OCT
1106   01652      00000  SINGCT  OCT
```

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P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

1107	01653	00000	TEMP	OCT
1110	01654	00000	VDRCNT	OCT

```
     1111                                    EJE
     1112                                              THIS SUBROUTINE GOES TO TIMER,THEN REINITIALIZES
     1113                                              PROGRAM TO START READING FIRST POINT ON EACH VIDAR.
     1114
     1115   01655      00000    REINIT ...
     1116   01656  36 1 351  /          RJP TIMER          TIME DELAY
     1117                               DLE 4-NUMVDR*4     INITIALIZE OUTPUT COMMANDS
     1120   01657  32 0 306            ENL ADRFX4
     1121   01660  37 1 350  /         STL LADR4
     1122   01661  32 1 347  /         ENL BITFX4
     1123   01662  37 1 346  /         STL LADR4-1
     1124   01663  32 0 307            ENL ADRFX3
     1125   01664  37 1 345  /         STL LADR3
     1126   01665  32 1 344  /         ENL BITFX3
     1127   01666  37 1 343  /         STL LADR3-1
     1130   01667  32 0 310            ENL ADRFX2
     1131   01670  37 1 342  /         STL LADR2
     1132   01671  32 1 341  /         ENL BITFX2
     1133   01672  37 1 340  /         STL LADR2-1
     1134   01673  32 0 311            ENL ADRFX1
     1135   01674  37 1 337  /         STL LADR1
     1136   01675  32 1 336  /         ENL BITFX1
     1137   01676  37 1 335  /         STL LADR1-1
     1140   01677  32 0 312            ENL FRQFIX         INITIALIZE LOCATION OF FREQUENCY TABLE
     1141   01700  37 0 313            STL LFREQ
     1142   01701  32 0 314            ENL NORFIX         INITIALIZE LOCATION OF NUMBER OF READINGS
     1143   01702  37 0 317            STL LNORDG
     1144   01703  32 0 316            ENL RDGFIX         INITIALIZE LOCATION OF VALUE TABLE
     1145   01704  37 0 315            STL LREDNG
     1146   01705  24 1 255            RTN
     1147
     1150                               DLE 4-NUMVDR
I    1151   01706  34 1 067   ADRFX4 OUT ADRTB4+1,I
I    1152   01707  34 1 050   ADRFX3 OUT ADRTB3+1,I
I    1153   01710  34 1 031   ADRFX2 OUT ADRTB2+1,I
I    1154   01711  34 1 012   ADRFX1 OUT ADRTB1+1,I
     1155   01712      07107   FRQFIX UCT FRQNCY
     1156   01713      07107   LFREQ  UCT FRQNCY
     1157   01714      02605   NORFIX UCT NORDG
     1160   01715      02605   LREDNG UCT NORDG
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

1161	01716	04746	RDGFIX OCT READING
1162	01717	04746	LNORDG OCT READING

```
1163                                    EJE
1164                                              THIS SUBROUTINE CLEARS ALL ENTRIES IN FREQUENCY
1165                                              TABLE,VALUE TABLE,NO, READINGS TABLE TO ZERO.
1166
1167   01720       00000    CLTAB   ...
1170   01721   32  1 334    JCLR    ENL ZERO
1171   01722   37  1 315            STL LFREQ,I
1172   01723   32  0 315            ENL LFREQ
1173   01724   13  1 335    J       EOR BGNTB
1174   01725   20  0 327            ZJP L+3
1175   01726   01  0 315            DCR LFREQ
1176   01727   24  0 320            JMP CLR
1177   01730   32  0 312            ENL FROFIX
1200   01731   37  0 315            STL LFREQ
1201   01732   24  1 320            RTN
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

1202

EJE

01733	02473	HKD
01734	02467	HKD
01735	00714	HKD
01736	00762	HKD
01737	00715	HKD
01740	00712	HKD
01741	00761	HKD
01742	00713	HKD
01743	00710	HKD
01744	00760	HKD
01745	00711	HKD
01746	00706	HKD
01747	00757	HKD
01750	00707	HKD
01751	02400	HKD
01752	00101	HKD
01753	00001	HKD
01754	02420	HKD
01755	02511	HKD
01756	02451	HKD
01757	02425	HKD
01760	01640	HKD
01761	01634	HKD
01762	00404	HKD
01763	00401	HKD
01764	02461	HKD
01765	00405	HKD
01766	02000	HKD

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

```
1203                02000           ORG ORIGIN+768
1204                                        THIS SUBROUTINE AVERAGES 8 READINGS FROM THE SPAN
1205                                        POINT AND ADJUSTS THE SPAN SETTING ACCORDING
1206                                        TO THIS AVERAGE. IT PRINTS SPAN SETTINGS IF
1207                                        DESIRED.
1210
1211   02000      00000   ADJSPN ...,
1212   02001  32 1 177  /        ENL SPNSET
1213   02002  20 0 003           ZJP L+2
1214   02003  24 1 000           RTN
1215   02004  03 0 151           SMB SIND            SET SPAN ADJUST INDICATOR
1216                              DLE 4-NUMVDR*6      ADD READINGS TO SPAN CHECK WORD
1217   02005  32 1 176  /        ENL SAVE4
1220   02006  27 0 007           PJP L+2
1221   02007  11 0 175  /        SUB 1)
1222   02010  13 0 150           EOR ALONES
1223   02011  10 0 152           ADD SPAN4
1224   02012  37 0 152           STL SPAN4
1225   02013  32 1 174  /        ENL SAVE3
1226   02014  27 0 015           PJP L+2
1227   02015  11 0 175           SUB 1)
1230   02016  13 0 150           EOR ALONES
1231   02017  10 0 153           ADD SPAN3
1232   02020  37 0 153           STL SPAN3
1233   02021  32 1 173  /        ENL SAVE2
1234   02022  27 0 023           PJP L+2
1235   02023  11 0 175           SUB 1)
1236   02024  13 0 150           EOR ALONES
1237   02025  10 0 154           ADD SPAN2
1240   02026  37 0 154           STL SPAN2
1241   02027  32 1 172  /        ENL SAVE1
1242   02030  27 0 031           PJP L+2
1243   02031  11 0 175           SUB 1)
1244   02032  13 0 150           EOR ALONES
1245   02033  10 0 155           ADD SPAN1
1246   02034  37 0 155           STL SPAN1
1247   02035  01 0 156           DCR SPNCNT          ADJUST SPAN EVERY 8 READINGS
1250   02036  20 0 037           ZJP L+2
1251   02037  24 1 000           RTN
1252   02040  32 0 171  /        ENL 8)
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
1253   02041  37 0 156          STL SPNCNT
1254   02042  24 0 042  6THCHG  JMP L+1           REPLACEABLE DURING INITIALIZATION
1255                             DLE 4-NUMVDR*7    CHECK FOR SPAN ADJUST ON EACH VIDAR
1256   02043  16 0 152          RSH SPAN4
1257   02044  16 0 152          RSH SPAN4
1260   02045  16 0 152          RSH SPAN4
1261   02046  16 0 152          RSH SPAN4
1262   02047  16 0 152          RSH SPAN4
1263   02050  20 0 051          ZJP L+2
1264   02051  02 0 053          CMB L+2
1265   02052  16 0 153          RSH SPAN3
1266   02053  16 0 153          RSH SPAN3
1267   02054  16 0 153          RSH SPAN3
1270   02055  16 0 153          RSH SPAN3
1271   02056  16 0 153          RSH SPAN3
1272   02057  20 0 060          ZJP L+2
1273   02060  02 0 151          CMB SIND
1274   02061  16 0 154          RSH SPAN2
1275   02062  16 0 154          RSH SPAN2
1276   02063  16 0 154          RSH SPAN2
1277   02064  16 0 154          RSH SPAN2
1300   02065  16 0 154          RSH SPAN2
1301   02066  20 0 067          ZJP L+2
1302   02067  02 0 151          CMB SIND
1303   02070  16 0 155          RSH SPAN1
1304   02071  16 0 155          RSH SPAN1
1305   02072  16 0 155          RSH SPAN1
1306   02073  16 0 155          RSH SPAN1
1307   02074  16 0 155          RSH SPAN1
1310   02075  20 0 076          ZJP L+2
1311   02076  02 0 151          CMB SIND
1312   02077  16 0 151          RSH SIND          CHECK SPAN ADJUST INDICATOR
1313   02100  27 0 101          PJP L+2
1314   02101  24 0 121          JMP SOUT          NO SPAN ADJUSTMENT NEEDED
1315                             DLE 4-NUMVDR*4    MODIFY SPAN WORDS
1316   02102  32 0 152          ENL SPAN4
1317   02103  10 0 157          ADD SPWRD4
1320   02104  12 0 170  ✓       BAND 177)
1321   02105  37 0 157          STL SPWRD4
1322   02106  32 0 153          ENL SPAN3
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
1323   02107  10 0 160          ADD SPWRD3
1324   02110  12 0 170         8AND 177)
1325   02111  37 0 160          STL SPWRD3
1326   02112  32 0 154          ENL SPAN2
1327   02113  10 0 161          ADD SPWRD2
1330   02114  12 0 170         8AND 177)
1331   02115  37 0 161          STL SPWRD2
1332   02116  32 0 155          ENL SPAN1
1333   02117  10 0 162          ADD SPWRD1
1334   02120  12 0 170         8AND 177)
1335   02121  37 0 162          STL SPWRD1
1336   02122  32 0 157  /SOUT    ENL 0)
1337                             DLE 4-NUMVDR
1340   02123  37 0 152          STL SPAN4
1341   02124  37 0 153          STL SPAN3
1342   02125  37 0 154          STL SPAN2
1343   02126  37 0 155          STL SPAN1
1344   02127  32 1 166  /       ENL SPNPRT
1345   02130  20 0 131          JMP L+2
1346   02131  24 1 000          RTN                    DO NOT PRINT SPAN SETTINGS
1347   02132  36 1 165  /       RJP CARRTN
1350   02133  24 0 133   7THCHG JMP L+1                REPLACEABLE DURING INITIALIZATION
1351                             DLE 4-NUMVDR*3         PRINT SPAN SETTINGS
1352   02134  32 0 157          ENL SPWRD4
1353   02135  36 1 164  /       RJP OUTPUT
1354   02136  36 1 163  /       RJP SPACER
1355   02137  32 0 160          ENL SPWRD3
1356   02140  36 1 164          RJP OUTPUT
1357   02141  36 1 163          RJP SPACER
1360   02142  32 0 161          ENL SPWRD2
1361   02143  36 1 164          RJP OUTPUT
1362   02144  36 1 163          RJP SPACER
1363   02145  32 0 162          ENL SPWRD1
1364   02146  36 1 164          RJP OUTPUT
1365   02147  24 1 000          RTN
1366
1367   02150      37777  ALONES OCT 37777
1370   02151      00000  SIND   OCT
1371                             DLE 4-NUMVDR
1372   02152      00000  SPAN4  OCT
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
1373   02153     00000   SPAN3   OCT
1374   02154     00000   SPAN2   OCT
1375   02155     00000   SPAN1   OCT
1376   02156     00000   SPNCNT  OCT
1377                     DLE  4-NUMVDR
1400   02157     00000   SPWRD4  OCT
1401   02160     00000   SPWRD3  OCT
1402   02161     00000   SPWRD2  OCT
1403   02162     00000   SPWRD1  OCT
```

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P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
     1404
                                        EJE
           02163      02451            NKD
           02164      02425            NKD
           02165      02461            NKD
           02166      00410            NKD
           02167      00000            NKD
           02170      00177            NKD
           02171      00010            NKD
           02172      00756            NKD
           02173      00755            NKD
           02174      00754            NKD
           02175      00001            NKD
           02176      00753            NKD
           02177      00407            NKD
```

```
1405                 02400          UKS ORIGIN+1024
1406                                       THIS SUBROUTINE IS ENTERED BETWEEN SUCCESSIVE
1407                                       READINGS OF THE LIST OF POINTS, IT DELAYS
1410                                       CYCTIM*1/10 SECOND,THEN RETURNS.
1411
1412   02400          00000   TIMER  ...
1413   02401  32 1 115  ✓       ENL CYCTIM
1414   02402  20 0 013          ZJP NOTD
1415   02403  37 0 017          STL T2
1416   02404  32 0 114  ✓       ENL 4000)
1417   02405  37 0 016          STL T1
1420   02406  32 0 016   TNTH   ENL T1
1421   02407  37 0 015          STL DCNT
1422   02410  01 0 015          DCR DCNT          1/10 SECOND DELAY
1423   02411  27 0 007          PJP L-1
1424   02412  01 0 017          DCR T2
1425   02413  27 0 005          PJP TNTH
1426   02414  24 1 000   NOTD   RTN
1427
1430   02415          00000   DCNT   OCT
1431   02416          07640   T1     DEC 4000
1432   02417          00000   T2     OCT
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D178-1)

```
1433                                    EJE
1434                                                THIS SUBROUTINE OUTPUTS 1 CHARACTER TO THE
1435                                                DOCUMENT DEVICE
1436
1437   02420      00000   OUT     ...
1440   02421   54 0 000           OUT DOCOUT
1441   02422   23 0 022           CLJ L+1          CLEAR LOCKOUT
1442   02423   01 1 113 ✓         DCR PC           WAIT FOR INTERRUPT
1443   02424   24 1 020   INTRTN  RTN
1444
1445                                                THIS SUBROUTINE OUTPUTS THE 2 OCTAL DIGITS
1446                                                OF THE ACCUMULATOR TO THE DOCUMENT DEVICE BY
1447                                                USING OUT...
1450
1451   02425      00000   OUTPUT  ...
1452   02426   57 0 077           STL OUTSAV
1453   02427   52 0 071           ENL D5
1454   02430   57 0 074           STL CNT
1455   02431   14 0 077           LSH OUTSAV
1456   02432   14 0 077           LSH OUTSAV
1457   02433   52 0 077           ENL OUTSAV
1460   02434   12 0 070           AND 2BITS
1461   02435   10 0 075   OTLOP   ADD LCODE        FIND CHARACTER OUTPUT CODE
1462   02436   57 0 076           STL LOOKUP
1463   02437   52 1 076           ENL LOOKUP,I
1464   02440   56 0 020           RJP OUT          OUTPUT CHARACTER
1465   02441   14 0 077           LSH OUTSAV
1466   02442   14 0 077           LSH OUTSAV
1467   02443   14 0 077           LSH OUTSAV
1470   02444   52 0 077           ENL OUTSAV
1471   02445   12 0 072           AND 3BITS
1472   02446   01 0 074           DCR CNT
1473   02447   27 0 034           PJP OTLOP
1474   02450   24 1 025           RTN
1475
1476                                                THIS SUBROUTINE OUTPUTS 3 SPACES TO THE
1477                                                DOCUMENT DEVICE BY USING OUT...
1500
1501   02451      00000   SPACER  ...
1502   02452   32 0 070           ENL D3
```

```
1503   02453  37 0 074          STL CNT
1504   02454  32 0 111          ENL SPACE        PICK UP CHARACTER OUTPUT CODE
1505   02455  36 0 020          RJP OUT          OUTPUT CHARACTER
1506   02456  01 0 074          DCR CNT
1507   02457  27 0 053          PJP L-3
1510   02460  24 1 051          RTN
1511                                      THIS SUBROUTINE OUTPUTS A CARRIAGE RETURN
1512                                      AND LINE FEED TO THE DOCUMENT DEVICE.
1513
1514   02461      00000  CARRTN ...
1515   02462  32 0 110          ENL CARRGE       CARRIAGE RETURN
1516   02463  36 0 020          RJP OUT
1517                             DLE 1-ASR*2
1520   02464  32 0 112          ENL LF           LINE FEED
1521   02465  36 0 020          RJP OUT
1522   02466  24 1 061          RTN
1523
1524   02467      00000  ZERO   OCT 0
1525   02470      00003  D3     DEC 3
1526   02471      00005  D5     DEC 5
1527              02470  2BITS  SYN D3
1530   02472      00007  3BITS  OCT 7
1531   02473      02516  BGNTB  OCT TABEND
1532   02474      00000  CNT    OCT
1533   02475      02500  LCODE  OCT CODE
1534   02476      00000  LOOKUP OCT
1535   02477      00000  OUTSAV OCT
1536                             DLE 3*ASR        SELECTRIC CODE TABLE
1542                      CAD    VFD 1,2,3,3,5
1543                             DLE 1-ASR*11     ASR CODE TABLE
1544   02500      03000  CODE   CAD 0,0,6,0,0
1545   02501      13040         CAD 0,2,6,1,0
1546   02502      13100         CAD 0,2,6,2,0
1547   02503      03140         CAD 0,0,6,3,0
1550   02504      13200         CAD 0,2,6,4,0
1551   02505      03240         CAD 0,0,6,5,0
1552   02506      03300         CAD 0,0,6,6,0
1553   02507      13340         CAD 0,2,6,7,0
1554   02510      10640  CARRGE CAD 0,2,1,5,0
1555   02511      12000  SPACE  CAD 0,2,4,0,0
```

```
P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

     1556   02512     00500   LF      CAD 0,0,1,2,0
     1557                             GEN
            02513     00000           WRD
            02514     07640           WRD
            02515     00406           WRD
```

P-50 MARK II ANALOG INPUT STATISTICAL TEST (D17B-1)

```
1560                            TABEND RPT NUMVDR*14
1561    02516       00000              OCT
1562                02605       NORDG  SYN L-1
1563                04746       REDING SYN 14*20*NUMVDR*NORDG*1
1564                07107       FRQNCY SYN 14*20*NUMVDR*REDING*1
1565                00000              END
```

ANALOG INPUT SCANNER TEST (D18B)

I. Purpose of Test

To read a variable number of analog points on up to four vidars and to print each input point which results in an out-of-limits reading.

II. Description of Test

The program reads an analog point on each vidar, then checks to see if the values are within the allowed tolerance. If a value is out-of-limits, a message in the following format will be printed on the ASR set, and the program continues.

READING IS aaaaa AT POINT bbcc ddddd

where aaaaa = actual reading
bbcc ddddd = analog point
bb is the word
cc is the channel
ddddd is the bit (one bit set).

Bits 0-13 of each word specified at initialization are checked. After all points have been read CYCLES (specified at initialization) times, the following message is printed on the ASR set, and the program restarts.

ANALOG SCANNER TEST COMPLETE

III. Description of Operation

A. Read in the binary tape of the Analog Scanner Test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (7602_8, 17602_8, 27602_8, or 37602_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Place the binary tape under the tape reader.

5. Turn on reader.

6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Preset	Description
6000_8	ANLINT	2	Analog conversion complete interrupt location
6001_8	NUMTST	4	No. vidars to be tested
6002_8	ASRCHN	0	ASR output channel
6003_8	ASRINT	11_8	ASR output complete interrupt location
6004_8	MAXCHN	77_8	Last output channel to be used
6005_8	SPNSEL	20100_8	Span select and gain
6006_8	SPNRST	200_8	Span reset
6007_8	VALUE	0	Desired bit value of points read
6010_8	DEV	5	Allowable deviation from value
6011_8	NØPTS	32_{10}	Maximum no. words to be read on any vidar
6012_8	CYCLES	100_8	No. cycles before end message
7177_8	CTR1	0	No. words to be read on vidar 1
7200_8-7237_8	VIDAR1	0	Words to be read on vidar 1 Word no. in bits 11-6
7240_8	CTR2	0	No. words to be read on vidar 2
7241_8-7300_8	VIDAR2	0	Words to be read on vidar 2
7301_8	CTR3	0	No. words to be read on vidar 3
7302_8-7341_8	VIDAR3	0	Words to be read on vidar 3
7342_8	CTR4	0	No. words to be read on vidar 4
7343_8-7402_8	VIDAR4	0	Words to be read on vidar 4

C. Start the test.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the test (6012_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button; depress the Start button.

D. The test runs continuously, scanning each point and printing out-of-limits errors.

VI. Storage

The program uses 1403_8 locations. (6000_8-7402_8)

V. Run Time

Recommended run time: 1/2 hour.

```
        1                               PROGRAM TITLE: P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)
        2
        3                               DATE: MARCH 1,1966
        4
        5                               SOURCE COMPUTER: P-500, SYSTEMS LAB, WESAP 50/500
        6                               OBJECT COMPUTER: P-50 MARK II SERIES
        7
       10                               PROGRAMMER: C,VETTER
       11
       12                               ABSTRACT: SEE DESCRIPTION OF SAME CODE NUMBER AVAILABLE
       13                                         FROM C,S,D, CHIEF DRAFTSMAN,
       14
       15                               CODING: NOT STNDRD1 - REVISION OF D18A PROGRAMMED ORIGINALLY
       16                                       PRIOR TO STNDRD1,
```

```
                                EJE ASSEMBLY PARAMETERS

                                                THE FOLLOWING MAY BE CHANGED AT RUN TIME
00002   ANINT   EQU 2           ANALOG CONVERSION COMPLETE INTERRUPT LOCATION
00004   NUMVDR  EQU 4           MAXIMUM NO. VIDARS TO BE TESTED
00000   DOCOUT  EQU 0           DOCUMENT DEVICE OUTPUT CHANNEL
00011   DOCINT8 EQU 11          DOCUMENT DEVICE OUTPUT COMPLETE INTERRUPT LOCATION
                                THE FOLLOWING MAY NOT BE CHANGED EXCEPT BY REASSEMBLY
06000   ORIGIN8 EQU 6000        PROGRAM ORIGIN
00016   VDRCH18 EQU 16          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 1
00036   VDRCH28 EQU 36          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 2
00056   VDRCH38 EQU 56          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 3
00076   VDRCH48 EQU 76          SPAN AND GAIN AND INPUT CHANNEL FOR VIDAR 4
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
34                                  EJE
35                                  UNL
36                06000             ORG ORIGIN
37                                          THE FOLLOWING ARE INPUTS AT RUN TIME
40    06000       00002   ANLINT OCT ANINT   ANALOG INPUT CONVERSION COMPLETE INTERRUPT LOCATION
41    06001       00004   NUMTST OCT NUMVDR  NUMBER OF VIDARS TO BE TESTED
42    06002       00000   ASRCHN OCT DOCOUT  ASR OUTPUT CHANNEL
43    06003       00011   ASRINT OCT DOCINT  ASR OUTPUT COMPLETE INTERRUPT LOCATION
44    06004       00077   MAXCHN OCT 77      LAST OUTPUT CHANNEL TO BE USED
45    06005       20100   SPNSEL OCT 20100   SPAN SELECT AND GAIN
46    06006       00200   SPNRST OCT 200     SPAN RESET
47    06007       00000   VALUE  OCT         DESIRED BIT VALUE OF POINTS READ
50    06010       00005   DEV    OCT 5       ALLOWABLE DEVIATION FROM VALUE
51    06011       00040   NOPTS  DEC 32      MAXIMUM NO. WORDS TO BE READ ON ANY VIDAR
52    06012       00100   CYCLES OCT 100     NO. CYCLES BEFORE PRINTOUT OF END MESSAGE
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
 53                                        EJE
 54                                                  SET INTERRUPTS
 55   06013  22 0 013                      SLJ L+1          SET LOCKOUT
 56   06014  32 0 377  /                  BENL 100)         STORE IGNORE INTERRUPTS IN ALL LOCATIONS
 57   06015  37 0 312                      STL LSTINT
 60   06016  32 0 224                      ENL CLJ01
 61   06017  37 1 312                      STL LSTINT,I
 62   06020  01 0 312                      DCR LSTINT
 63   06021  27 0 016                      PJP L-2
 64   06022  23 0 022                      CLJ L+1          CLEAR LOCKOUT
 65   06023  32 0 000   SETINT ENL ANLINT                   STORE ANALOG INTERRUPT
 66   06024  10 0 376  /                   ADD 65)
 67   06025  37 0 322                      STL TEMP
 70   06026  13 0 320                      EOR RJPX
 71   06027  37 1 000                      STL ANLINT,I
 72   06030  32 0 375  /                   ENL INTRTN)
 73   06031  37 1 322                      STL TEMP,I
 74   06032  32 0 003                      ENL ASRINT       STORE ASR INTERRUPT
 75   06033  10 0 376                      ADD 65)
 76   06034  37 0 322                      STL TEMP
 77   06035  13 0 320                      EOR RJPX
100   06036  37 1 003                      STL ASRINT,I
101   06037  32 0 374  /                   ENL ASRIN)
102   06040  37 1 322                      STL TEMP,I
103                                                 SET ASR CHANNEL
104   06041  32 0 002   SETCHN ENL ASRCHN
105   06042  13 0 317                      EOR OUTX
106   06043  37 1 373  /                   STL OASR
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
      107                                    EJE
      110                                              SET JUMPS
      111   06044   32 0 001    SETJMP ENL NUMTST        IN PRETEST
      112   06045   13 0 372  J       8EOR 37777)
      113   06046   10 0 371  J        ADD NUMVDR)
      114   06047   10 0 370  J        ADD GSPN)
      115   06050   12 0 367  J       8AND 377)
      116   06051   10 0 366  J       8ADD 24000)
      117   06052   37 0 072           STL GSPN
      120   06053   32 0 001           ENL NUMTST        IN OUTINT
      121   06054   13 0 372          8EOR 37777)
      122   06055   10 0 371           ADD NUMVDR)
      123   06056   14 1 376           LSH ACC
      124   06057   14 1 376           LSH ACC
      125   06060   10 0 365  J        ADD OUTINT)
      126   06061   12 0 367          8AND 377)
      127   06062   10 0 366          8ADD 24000)
      130   06063   37 0 115           STL OUTINT
```

```
131                                     EJE
132                                                 PRETEST:  OUTPUT GAIN AND SPAN SELECT
133   06064  32 0 006   PRETST ENL SPNRST
134   06065  34 0 016    OA    OUT VDRCH1
135   06066  32 0 364  J       ENL 100)
136   06067  01 1 376          DCR ACC
137   06070  27 0 066          PJP L-1
140   06071  32 0 005          ENL SPNSEL
141   06072  24 0 072   GSPN   JMP L+1           REPLACEABLE DURING INITIALIZATION
142   06073  34 0 076    OB    OUT VDRCH4
143   06074  34 0 056    OC    OUT VDRCH3
144   06075  34 0 036    OD    OUT VDRCH2
145   06076  34 0 016    OE    OUT VDRCH1
146                                                 BEGIN TEST
147   06077  36 1 363  JANITST RJP INITL           INITIALIZE
150   06100  02 0 250   SETUP  CMB IGNORE          SET FIRST READING INDICATOR
151   06101  03 0 246          SMB END             CLEAR END OF CYCLE INDICATOR
152   06102  32 0 011          ENL NOPTS           STORE NUMBER OF POINTS TO BE READ
153   06103  37 0 251          STL INDEX
154   06104  32 0 012          ENL CYCLES
155   06105  37 0 245          STL CYCNT
156   06106  32 0 007          ENL VALUE
157   06107  11 0 010          SUB DEV
160   06110  11 0 362  J       SUB 1)
161   06111  37 0 311          STL LOLIM           LOW LIMIT
162   06112  32 0 007          ENL VALUE
163   06113  10 0 010          ADD DEV
164   06114  37 0 247          STL HILIM           HIGH LIMIT
165                                                 OUTPUT - INPUT ROUTINE
166   06115  24 0 115  OUTINT JMP L+1              REPLACEABLE DURING INITIALIZATION
167   06116  30 0 076   IA     INT VDRCH4
170   06117  37 0 313          STL NVAL4
171   06120  32 0 222          ENL BIT
172   06121  34 1 305          OUT LOC4,I
173   06122  30 0 056   IB     INT VDRCH3
174   06123  37 0 314          STL NVAL3
175   06124  32 0 222          ENL BIT
176   06125  34 1 306          OUT LOC3,I
177   06126  30 0 036   IC     INT VDRCH2
200   06127  37 0 315          STL NVAL2
```

```
P-50 MARK II ANALOG INPUT SCANNER TEST (D188)

      201   06130  32 0 222            ENL BIT
      202   06131  34 1 307            OUT LOC2,I
      203   06132  30 0 016    ID      INT VDRCH1
      204   06133  37 0 316            STL NVAL1
      205   06134  32 0 222            ENL BIT
      206   06135  34 1 310            OUT LOC1,I
      207   06136  32 0 361  JTRIGERBENL 400)
      210   06137  34 0 016            OUT VDRCH1
```

```
211                                     EJE
212                                                 CHECK FOR READING WITHIN LIMITS
213   06140   32 0 250   CKLIM   ENL IGNORE
214   06141   27 0 162           PJP ENTLOC         IGNORE THESE READINGS
215   06142   32 0 360   /       ENL NVAL1)
216   06143   37 0 323           STL VAL
217   06144   32 0 357   /       ENL INTPT1)
220   06145   37 0 252           STL INT
221   06146   32 0 001           ENL NUMTST
222   06147   37 0 244           STL COUNT
223   06150   32 1 323   LIMIT   ENL VAL,I          CHECK READING
224   06151   11 0 311           SUB LOLIM
225   06152   27 0 153           PJP L+2
226   06153   24 0 323           JMP LIMERR
227   06154   32 1 323           ENL VAL,I
230   06155   11 0 247           SUB HILIM
231   06156   27 0 323           PJP LIMERR
232   06157   01 0 252   DCRLIM  DCR INT            DECREMENT COUNTERS TO CHECK NEXT VIDAR
233   06160   01 0 323           DCR VAL
234   06161   01 0 244           DCR COUNT
235   06162   27 0 147           PJP LIMIT
236   06163   32 0 310   ENTLOC  ENL LOC1           STORE WORD,CHANNEL,BIT FOR LIMERR
237   06164   37 0 256           STL INTPT1
240   06165   32 0 307           ENL LOC2
241   06166   37 0 255           STL INTPT2
242   06167   32 0 306           ENL LOC3
243   06170   37 0 254           STL INTPT3
244   06171   32 0 305           ENL LOC4
245   06172   37 0 253           STL INTPT4
246   06173   32 0 222           ENL BIT
247   06174   37 0 223           STL BITSV
250   06175   03 0 250           SMB IGNORE
251   06176   32 0 246           ENL END
252   06177   27 0 207           PJP ENDRT
253   06200   24 1 356   /       JMP INCRMT         INCREMENT POINT ADDRESSES
254   06201   01 0 245    CBA    DCR CYCNT
255   06202   27 0 203           PJP ABC
256   06203   02 0 246           CMB END
257                                                 WAIT FOR INTERRUPT
260   06204   32 0 221   ABC     ENL AFLAG
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D188)

```
      261   06205  27 0 203          PJP L-1
      262   06206  02 0 221          CMB AFLAG
      263   06207  24 0 114          JMP OUTINT
      264                                    END ROUTINE
      265   06210  03 0 246  ENDRT    SMB END
      266   06211  36 1 355  J        RJP OTRCU
      267   06212     06225          OCT COMPLT
      270   06213  24 0 076          JMP ANITST
      271                                    ANALOG INTERRUPT RETURN
      272   06214     00000  INTRTN ...
      273   06215  06 0 321          SDR SAVE
      274   06216  03 0 221          SMB AFLAG
      275   06217  05 0 321          EDR SAVE
      276   06220  23 1 214          CLJ INTRTN,I
      277
      300   06221     00000  AFLAG   OCT
      301   06222     00001  BIT     OCT 1
      302   06223     00000  BITSV   OCT
I     303   06224  23 1 000  CLJOI   CLJ ,I
      304   06225     02145  COMPLT  BCD 14ANALOG SCANNER TEST COMPLETE
      305   06243     01477          OCT 1477
      306   06244     00000  COUNT   OCT
      307   06245     00000  CYCNT   OCT
      310   06246     20000  END     OCT 20000
      311   06247     00000  HILIM   OCT
      312   06250     00000  IGNORE  OCT
      313   06251     00000  INDEX   OCT
      314   06252     00000  INT     OCT
      315   06253     00000  INTPT4  OCT
      316   06254     00000  INTPT3  OCT
      317   06255     00000  INTPT2  OCT
      320   06256     00000  INTPT1  OCT
      321   06257     05125  LIMFOR  BCD 05READING IS     X
      322   06264     06060          OCT 6060
      323   06265     00000  M       OCT
      324   06266     00000  MI      OCT
      325   06267     00000  LOA     OCT ,6060
      326   06271     02163          BCD 05AT POINT      X
      327   06276     00000  MIX     OCT
      330   06277     00000  LOX     OCT ,6060
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
      331   06301      00000   HHB     OCT
      332   06302      00000   HIB     OCT
      333   06303      00000   LOB     OCT ,1477
      334   06305      00000   LOC4    OCT
      335   06306      00000   LOC3    OCT
      336   06307      00000   LOC2    OCT
      337   06310      00000   LOC1    OCT
      340   06311      00000   LOLIM   OCT
      341   06312      00000   LSTINT  OCT
      342   06313      00000   NVAL4   OCT
      343   06314      00000   NVAL3   OCT
      344   06315      00000   NVAL2   OCT
      345   06316      00000   NVAL1   OCT
      346   06317   34 0 000   OUTX    OUT
I     347   06320   36 1 000   RJPX    RJP ,I
      350   06321      00000   SAVE    OCT
      351   06322      00000   TEMP    OCT
      352   06323      00000   VAL     OCT
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
353                                     EJE
354                                                     LIMIT ERROR
355   06324   32 1 323    LIMERR ENL  VAL,I
356   06325   36 1 354  /        RJP  CNVTA
357   06326   37 0 267           STL  LOA
360   06327   36 1 353  /        RJP  CNVTB
361   06330   37 0 266           STL  HI
362   06331   32 0 321           ENL  SAVE
363   06332   14 1 376           LSH  ACC
364   06333   14 1 376           LSH  ACC
365   06334   12 0 352  /        AND  3)
366   06335   10 0 351  /       BADD  6000)
367   06336   37 0 265           STL  H
370   06337   32 1 252           ENL  INT,I
371   06340   36 1 354           RJP  CNVTA
372   06341   37 0 277           STL  LOX
373   06342   36 1 353           RJP  CNVTB
374   06343   37 0 276           STL  HIX
375   06344   32 0 223           ENL  BITSV
376   06345   36 1 354           RJP  CNVTA
377   06346   37 0 303           STL  LOB
400   06347   36 1 353           RJP  CNVTB
      06350      24377           SKP
      06351      06000           WRD
      06352      00003           WRD
      06353      06603           WRD
      06354      06570           WRD
      06355      07000           WRD
      06356      06411           WRD
      06357      06256           WRD
      06360      06316           WRD
      06361      00400           WRD
      06362      00001           WRD
      06363      06530           WRD
      06364      00144           WRD
      06365      06115           WRD
      06366      24000           WRD
      06367      00377           WRD
      06370      06072           WRD
      06371      00004           WRD
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
06372     37777          WRD
06373     07041          WRD
06374     07056          WRD
06375     06214          WRD
06376     00101          WRD
06377     00100          WRD
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
401   06400   37 1 267  ✓      STL HIB
402   06401   32 1 266  ✓      ENL SAVE
403   06402   14 1 265  ✓      LSH ACC
404   06403   14 1 265         LSH ACC
405   06404   12 0 264  ✓      AND 3)
406   06405   10 0 263  ✓     8ADD 6000)
407   06406   37 1 262  ✓      STL HHB
410   06407   36 1 261  ✓      RJP OTRCD
411   06410      06257         OCT LIMFUR
412   06411   24 1 260  ✓      JMP DCRLIM
```

```
413                                    EJE
414                                                INCREMENT POINT ADDRESS
415   06412  32 0 257  /INCRMT ENL LOC1)
416   06413  37 0 233         STL LOC
417   06414  32 1 256  /      ENL NUMTST
420   06415  37 1 255  /      STL COUNT
421   06416  02 0 122         CMB ADDR
422   06417  32 1 254  /      ENL BIT
423   06420  27 0 021         PJP L+2
424   06421  03 0 122         SMB ADDR
425   06422  14 1 254         LSH BIT
426   06423  32 0 122         ENL ADDR
427   06424  27 1 253  /      PJP ABC
430   06425  32 1 252  /INCCHN ENL MAXCHN        INCREMENT CHANNEL
431   06426  11 1 127         SUB CHNLNO,I
432   06427  20 0 040         ZJP CH3
433   06430  01 0 127         DCR CHNLNO
434   06431  32 1 233   CH2   ENL LOC,I
435   06432  12 0 251  /      BAND 37700)
436   06433  10 1 127         ADD CHNLNO,I
437   06434  37 1 233         STL LOC,I
440   06435  01 0 233         DCR LOC
441   06436  01 1 255         DCR COUNT
442   06437  27 0 030         PJP CH2
443   06440  24 1 253         JMP ABC
444   06441  32 0 250  /CH3   ENL CHAN1)
445   06442  37 0 127         STL CHNLNO
446   06443  32 1 255   INCWRD ENL COUNT         INCREMENT WORD
447   06444  11 1 256         SUB NUMTST
450   06445  10 0 247  /      ADD 1)
451   06446  27 0 054         PJP R1
452   06447  10 0 247         ADD 1)
453   06450  27 0 063         PJP R2
454   06451  10 0 247         ADD 1)
455   06452  27 0 072         PJP R3
456   06453  10 0 247         ADD 1)
457   06454  27 0 101         PJP R4
460   06455  01 0 224   R1    DCR COUNT1
461   06456  27 0 060         PJP L+3
462   06457  32 1 246  /      ENL CTR1
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D188)

```
463   06460   37 0 224          STL COUNT1
464   06461   32 0 232          ENL LIM1
465   06462   10 0 224          ADD COUNT1
466   06463   24 0 107          JMP R5
467   06464   01 0 223   R2     DCR COUNT2
470   06465   27 0 067          PJP L+3
471   06466   32 1 245   /      ENL CTR2
472   06467   37 0 223          STL COUNT2
473   06470   32 0 231          ENL LIM2
474   06471   10 0 223          ADD COUNT2
475   06472   24 0 107          JMP R5
476   06473   01 0 222   R3     DCR COUNT3
477   06474   27 0 076          PJP L+3
500   06475   32 1 244   /      ENL CTR3
501   06476   37 0 222          STL COUNT3
502   06477   32 0 230          ENL LIM3
503   06500   10 0 222          ADD COUNT3
504   06501   24 0 107          JMP R5
505   06502   01 0 221   R4     DCR COUNT4
506   06503   27 0 105          PJP L+3
507   06504   32 1 243   /      ENL CTR4
510   06505   37 0 221          STL COUNT4
511   06506   32 0 227          ENL LIM4
512   06507   10 0 221          ADD COUNT4
513   06510   37 0 122   R5     STL ADDR
514   06511   32 1 122          ENL ADDR,I
515   06512   10 1 127          ADD CHNLNO,I
516   06513   37 1 233          STL LOC,I
517   06514   01 0 233          DCR LOC
520   06515   01 1 255          DCR COUNT
521   06516   27 0 042          PJP INCWRD
522   06517   01 1 242   /      DCR INDEX
523   06520   27 1 253          PJP ABC
524   06521   24 1 241   /      JMP CBA
525
526   06522       00000   ADDR   OCT
527   06523       00077   CHAN4  OCT 77
530   06524       00017   CHAN3  OCT 17
531   06525       00037   CHAN2  OCT 37
532   06526       00057   CHAN1  OCT 57
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
      533   06527      00000   CHNLNO OCT
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
534                                     EJE
535                                                 INITIALIZE
536   06530       00000   INITL   ...
537   06531   32 1 256            ENL NUMTST
540   06532   37 1 242            STL INDEX
541   06533   32 0 240  /         ENL LIM1)
542   06534   37 0 226            STL LIM
543   06535   32 0 257            ENL LOC1)
544   06536   37 0 233            STL LOC
545   06537   32 0 250            ENL CHAN1)
546   06540   37 0 127            STL CHNLNO
547   06541   32 0 247            ENL 1)
550   06542   37 1 254            STL BIT
551   06543   32 1 226    I1      ENL LIM,I
552   06544   37 0 225            STL CNT
553   06545   10 1 225            ADD CNT,I
554   06546   37 0 122            STL ADDR
555   06547   32 1 122            ENL ADDR,I
556   06550   10 1 127            ADD CHNLNO,I
557   06551   37 1 233            STL LOC,I
560   06552   01 1 242            DCR INDEX
561   06553   20 0 156            ZJP I2
562   06554   01 0 226            DCR LIM
563   06555   01 0 233            DCR LOC
564   06556   24 0 142            JMP I1
565   06557   32 1 246    I2      ENL CTR1
566   06560   37 0 224            STL COUNT1
567   06561   32 1 245            ENL CTR2
570   06562   37 0 223            STL COUNT2
571   06563   32 1 244            ENL CTR3
572   06564   37 0 222            STL COUNT3
573   06565   32 1 243            ENL CTR4
574   06566   37 0 221            STL COUNT4
575   06567   24 1 130            RTN
```

```
576                                     EJE
577                                                 CONVERT 2 LOW ORDER DIGITS OF ACCUMULATOR
600    06570        00000    CNVTA   ...
601    06571  37 1 266          STL   SAVE
602    06572  12 0 237  /     BAND   7)
603    06573  37 1 236  /      STL   TEMP
604    06574  32 1 266          ENL   SAVE
605    06575  12 0 235  /     BAND   70)
606    06576  14 1 265          LSH   ACC
607    06577  14 1 265          LSH   ACC
610    06600  14 1 265          LSH   ACC
611    06601  10 1 236          ADD   TEMP
612    06602  24 1 170          RTN
613                                                 CONVERT 2 HIGH ORDER DIGITS OF ACCUMULATOR
614    06603        00000    CNVTB   ...
615    06604  32 1 266          ENL   SAVE
616    06605  12 0 234  /     BAND   700)
617    06606  16 1 265          RSH   ACC
620    06607  16 1 265          RSH   ACC
621    06610  16 1 265          RSH   ACC
622    06611  37 1 236          STL   TEMP
623    06612  32 1 266          ENL   SAVE
624    06613  12 0 261          BAND  7000)
625    06614  10 1 236          ADD   TEMP
626    06615  16 1 265          RSH   ACC
627    06616  16 1 265          RSH   ACC
630    06617  16 1 265          RSH   ACC
631    06620  24 1 203          RTN
632
633    06621        00000    COUNT4  OCT
634    06622        00000    COUNT3  OCT
635    06623        00000    COUNT2  OCT
636    06624        00000    COUNT1  OCT
637    06625        00000    CNT     OCT
640    06626        00000    LIM     OCT
641    06627        07342    LIM4    OCT   VIDAM4-1
642    06630        07301    LIM3    OCT   VIDAM3-1
643    06631        07240    LIM2    OCT   VIDAM2-1
644    06632        07177    LIM1    OCT   VIDAM1-1
645    06633        00000    LOC     OCT
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
      646                                EJE
            06634      00700            WRD
            06635      00070            WRD
            06636      06322            WRD
            06637      00007            WRD
            06640      06632            WRD
            06641      06200            WRD
            06642      06251            WRD
            06643      07342            WRD
            06644      07301            WRD
            06645      07240            WRD
            06646      07177            WRD
            06647      00001            WRD
            06650      06526            WRD
            06651      37700            WRD
            06652      06004            WRD
            06653      06203            WRD
            06654      06222            WRD
            06655      06244            WRD
            06656      06001            WRD
            06657      06310            WRD
            06660      06156            WRD
            06661      07000            WRD
            06662      06301            WRD
            06663      06000            WRD
            06664      00003            WRD
            06665      00101            WRD
            06666      06321            WRD
            06667      06302            WRD
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
647                 07000             ORG ORIGIN+512
650    07000        00000   OTRCD     ...        PRINT RECORD TERMINATED BY 77 CODE
651    07001  32 0 000               ENL OTRCD
652    07002  10 0 076  /            ADD 1)
653    07003  37 0 000               STL OTRCD
654    07004  32 1 000               ENL OTRCD,I
655    07005  37 0 065               STL OTADS
656    07006  03 0 066               SMB OTIND
657    07007  32 1 065   OTLOP      ENL OTADS,I
660    07010  16 0 066               RSH OTIND
661    07011  27 0 017               PJP SECND
662    07012  16 1 075  /            RSH ACC
663    07013  16 1 075               RSH ACC
664    07014  16 1 075               RSH ACC
665    07015  16 1 075               RSH ACC
666    07016  16 1 075               RSH ACC
667    07017  16 1 075               RSH ACC
670    07020  12 0 074  /SECND      BAND 77)
671    07021  11 0 074               BSUB 77)
672    07022  20 1 000               ZJP OTRCD,I
673    07023  10 0 074               BADD 77)
674    07024  27 0 025               PJP L+2
675    07025  32 0 073  /            ENL 0)
676    07026  36 0 035               MJP OT1
677    07027  32 0 065               ENL OTADS
700    07030  10 0 076               ADD 1)
701    07031  16 0 066               RSH OTIND
702    07032  27 0 004               PJP OTLOP-2
703    07033  02 0 066               CMB OTIND
704    07034  24 0 006               JMP OTLOP
705
706    07035        00000   OT1       ...
707    07036  10 0 072  /            ADD TBL)
710    07037  37 0 063               STL ADS
711    07040  32 1 063               ENL ADS,I
712    07041  34 0 000   OASR        OUT
713    07042  32 0 064               ENL MFLAG          WAIT FOR INTERRUPT
714    07043  27 0 041               PJP L-1
715    07044  02 0 064               CMB MFLAG
716    07045  32 0 063               ENL ADS
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
717   07046  11 0 071  /       @SUB TBL+14)
720   07047  20 0 052            /JP LFD
721   07050  32 0 073            ENL 0)
722   07051  37 0 063            STL ADS
723   07052  24 1 035            JMP OT1,I
724   07053  32 0 070  /LFD      @ENL 30500)
725   07054  37 0 063            STL ADS
726   07055  24 0 040            JMP OT1+4
727                                        ASR INTERRUPT RETURN
730   07056      00000   ASRIN   ...
731   07057  06 1 067  /         SDR SAVE
732   07060  03 0 064            SMB MFLAG
733   07061  05 1 067            EDR SAVE
734   07062  23 1 056            CLJ ASRIN,I
735
736   07063      00000   ADS     OCT
737   07064      00000   MFLAG   OCT
740   07065      00000   OTADS   OCT
741   07066      00000   OTIND   OCT
742                              GEN
      07067      06321           WRD
      07070      30500           WRD
      07071      07113           WRD
      07072      07077           WRD
      07073      00000           WRD
      07074      00077           WRD
      07075      00101           WRD
      07076      00001           WRD
```

P-50 MARK II ANALOG INPUT SCANNER TEST (D18B)

```
 743                                                    TELETYPE MODEL 35 CODE
 744                          COD     VFD 1,2,3,3,5
 745   07077     23000        TBL     COD 1,0,6,0,      0       00
 746   07100     33040                COD 1,2,6,1,      1       01
 747   07101     33100                COD 1,2,6,2,      2       02
 750   07102     23140                COD 1,0,6,3,      3       03
 751   07103     33200                COD 1,2,6,4,      4       04
 752   07104     23240                COD 1,0,6,5,      5       05
 753   07105     23300                COD 1,0,6,6,      6       06
 754   07106     33340                COD 1,2,6,7,      7       07
 755   07107     33400                COD 1,2,7,0,      8       10
 756   07110     23440                COD 1,0,7,1,      9       11
 757   07111     35700                COD 1,3,3,6,      0       12
 760   07112     33640                COD 1,2,7,5,      =       13
 761   07113     30640                COD 1,2,1,5,      CR      14
 762   07114     23500                COD 1,0,7,2,      :       15
 763   07115     33700                COD 1,2,7,6,      >       16
 764   07116     22040                COD 1,0,4,1,      EXCLM   17
 765   07117     22540                COD 1,0,5,3,      +       20
 766   07120     24040                COD 1,1,0,1,      A       21
 767   07121     24100                COD 1,1,0,2,      B       22
 770   07122     34140                COD 1,3,0,3,      C       23
 771   07123     24200                COD 1,1,0,4,      D       24
 772   07124     34240                COD 1,3,0,5,      E       25
 773   07125     34300                COD 1,3,0,6,      F       26
 774   07126     24340                COD 1,1,0,7,      G       27
 775   07127     24400                COD 1,1,1,0,      H       30
 776   07130     34440                COD 1,3,1,1,      I       31
 777   07131     23740                COD 1,0,7,7,      ?       32
1000   07132     22700                COD 1,0,5,6,      .       33
1001   07133     32440                COD 1,2,5,1,      )       34
1002   07134     35540                COD 1,3,3,3,      [       35
1003   07135     23600                COD 1,0,7,4,      <       36
1004   07136     32140                COD 1,2,4,3,      #       37
1005   07137     22640                COD 1,0,5,5,      -       40
1006   07140     34500                COD 1,3,1,2,      J       41
1007   07141     24540                COD 1,1,1,3,      K       42
1010   07142     34600                COD 1,3,1,4,      L       43
1011   07143     24640                COD 1,1,1,5,      M       44
1012   07144     24700                COD 1,1,1,6,      N       45
```

```
1013   07145    34740          COD 1,3,1,7,     O      46
1014   07146    25000          COD 1,1,2,0,     P      47
1015   07147    35040          COD 1,3,2,1,     Q      50
1016   07150    35100          COD 1,3,2,2,     R      51
1017   07151    25740          COD 1,1,3,7,     -      52
1020   07152    22200          COD 1,0,4,4,     $      53
1021   07153    32500          COD 1,2,5,2,     *      54
1022   07154    35640          COD 1,3,3,5,     )      55
1023   07155    33540          COD 1,2,7,3,     (      56
1024   07156    34000          COD 1,3,0,0,     0      57
1025   07157    32000          COD 1,2,4,0,     SPACE  60
1026   07160    32740          COD 1,2,5,7,     /      61
1027   07161    25140          COD 1,1,2,3,     S      62
1030   07162    35200          COD 1,3,2,4,     T      63
1031   07163    25240          COD 1,1,2,5,     U      64
1032   07164    25300          COD 1,1,2,6,     V      65
1033   07165    35340          COD 1,3,2,7,     W      66
1034   07166    35400          COD 1,3,3,0,     X      67
1035   07167    25440          COD 1,1,3,1,     Y      70
1036   07170    25500          COD 1,1,3,2,     Z      71
1037   07171    32240          COD 1,2,4,5,     %      72
1040   07172    32600          COD 1,2,5,4,     .      73
1041   07173    22400          COD 1,0,5,0,     (      74
1042   07174    32300          COD 1,2,4,6,     AMP    75
1043   07175    25600          COD 1,1,3,4,     \      76
1044   07176    20500          COD 1,0,1,2,     L FEED 77
1045
1046   07177    00000   CTR1   OCT
1047                    VIDAR1 RPT 32
1050   07200    00000          OCT
1051   07240    00000   CTR2   OCT
1052                    VIDAR2 RPT 32
1053   07241    00000          OCT
1054   07301    00000   CTR3   OCT
1055                    VIDAR3 RPT 32
1056   07302    00000          OCT
1057   07342    00000   CTR4   OCT
1060                    VIDAR4 RPT 32
1061   07343    00000          OCT
1062            00000          END
```

CONTACT CLOSURE OUTPUT VS. CONTACT CLOSURE INPUT TEST (D19A)

I. Purpose of Test

To test up to eight contact closure output registers against the same number of contact closure input registers without the use of the P-50 Executives. Various patterns are set on the registers and the registers are then checked for proper operation. This test is for multiplexed CCI. See V for non-multiplexed modifications.

II. Description of Test

The program assumes that n contact output registers are tied to n contact input registers (where n ranges from 1 to 8). Various patterns are output to the contact outputs; after each change, all the contact inputs are checked to verify that the desired changes (and no more) took place.

The pattern of output is as follows:

00000,37777,.....,00000,37777,(Sequence of 14)
00001,00002,.....,10000,20000,(Sequence of 14)
20000,30000,.....,37776,37777,(Sequence of 14)
12525,25252,.....,12525,25252,(Sequence of 14)

III. Description of Operation

A. Read in the binary tape of the Contact Closure Output vs. Contact Closure Input test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Place the binary tape under the tape reader.

5. Turn the reader on.

6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat 2 and 3 until all the following parameters have been entered.

Location		Description
6000_8-6007_8	CWDS	Contact closure output (CCO) control words, one for each register. Each control word contains the word (bits 13-6) and the set channel (bits 5-0) for a particular output. The registers are assigned numbers 0-7 corresponding to locations 6000_8-6007_8.
6010_8-6017_8	IBF	Contact closure input (CCI) control words, one for each register. Each control word contains a one in the bit position corresponding to the register number. For example, a one in bit 4 (20_8) of the control word refers to register 4. Note, one and only one bit of a control word can be set. The registers are assigned numbers 0-7 corresponding to locations 6010_8-6017_8.
6020_8	NCCØ	Number of registers to be tested.
6021_8	CCØI	Contact closure output (CCO) completion interrupt location.
6022_8	ØRI	Contact closure input (CCI) cycle completion interrupt location.
6023_8	IRI	Contact closure input (CCI) input request interrupt location.
6024_8	ASRI	ASR output completion interrupt location.
6025_8	CCIØUT	Output command to contact closure input (CCI) address channel. For example, if the channel is 42_8, the command is 34042_8 (ØUT 42_8).
6026_8	CCIINT	Input command from contact closure input (CCI) read channel. For example, if the channel is 43_8, the command is 30043_8 (INT 43_8).
6027_8	ØUTASR	Output command to ASR output channel. For example, if the channel is 44_8, the command is 34044_8 (ØUT 44_8).

C. Start the test.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the test (6027_8); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Clear the lockout and hit flip-flop using the probe; depress the Start button.

D. Test runs continuously, printing out a completion message on the ASR set after five runs.

CCØ-CCI TEST COMPLETED

E. When an error occurs a message is printed out on the ASR set, and the test continues. The error message format is:

CCØ-CCI REGISTER a SHOULD BE bbbb BUT IS cccc.

where

a = Register number
bbbb = Pattern that should be there
cccc = Pattern which is there

IV. Storage

Number of locations used: 1052_8 (6000_8-7051_8).

V. Non-Multiplexed CCI Modification to D19A

It should be pointed out here that CCI can be multiplexed or non-multiplexed. The program listed in D19A is for multiplexed CCI; if non-multiplexed CCI's are used, the program must be modified as follows:

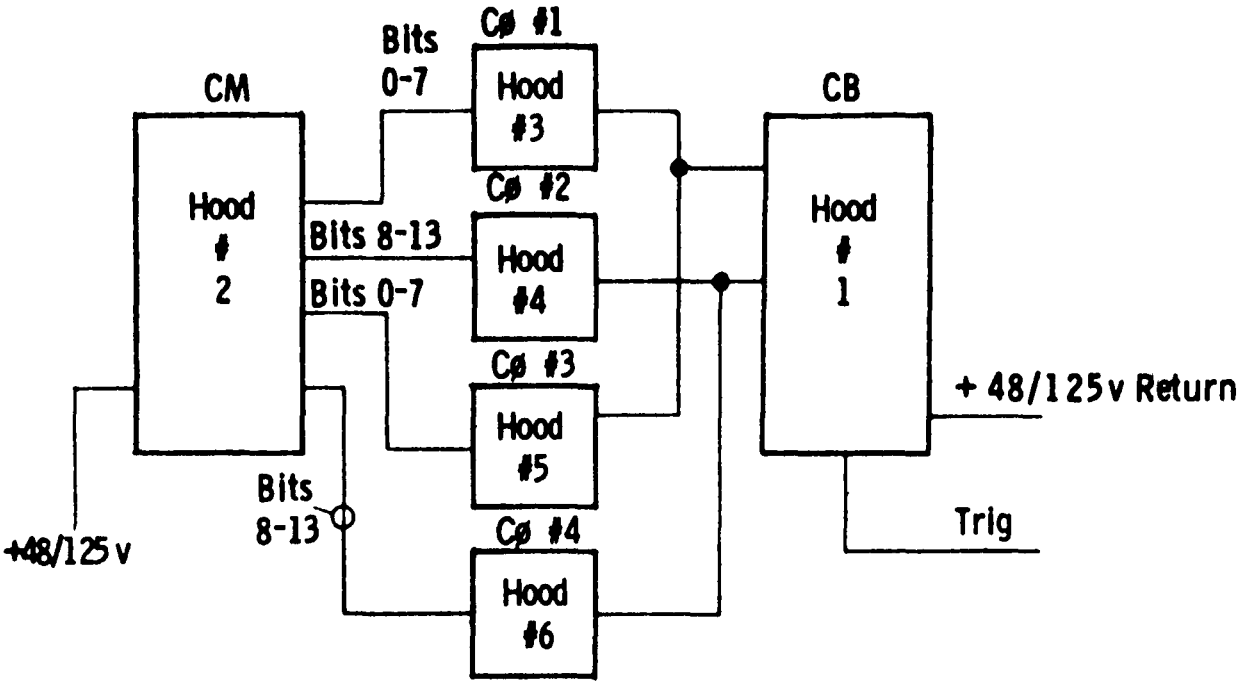
Location	Initial Contents	New Content
6635	32631	300 XX*
6636	10342	23631

*Input channel number

VI. Test Cables

A. Multiplexed CCI Vs. CCØ Cable

Drawing 775A055, sheets 1 to 6 show the connections for multiplexed CCI vs. CCØ. This cable allows the user to check up to 28 CCØ points. Figure 1 below shows a block diagram of the connectors.



MPLX. CCI VS. CCØ TEST CABLE
Figure 1

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR MCI-CCØ TEST
DWG 775 A 055 SUB. 1 2 3 4 FINISH CHART

FROM Hood #2 TERM	COLOR	TO Hood #3 TERM	REMARKS
X35	BLK	X6	CCØ B.0 - CM (EVEN BIT)
X34	WH./BLK	X10	ARM B.1
X33	BRN	X14	B.2
X32	WH/BRN	X22	B.3
X31	RED	X26	B.4
X30	WH/RED	X30	B.5
X29	GRN	X34	B.6
	WH/GRN		
~~X1~~	~~GRA~~	~~X1*~~	~~CB(2) TRIG R~~
~~X2~~	~~WH/GRA~~	~~X2*~~	~~CB(2) TRIG~~

FROM Hood #3 TERM	COLOR	TO Hood #1 TERM	REMARKS
X8	BLK	X35	CCØ B.0
X12	WH/BLK	X33	N.Ø. B.1
X16	BRN	X31	B.2
X23	WH/BRN	X29	B.3
X27	RED	X27	B.4
X31	WH/RED	X25	B.5
X35	GRN	X23	B.6
	WH/GRN		
~~X1*~~	~~GRA~~	~~X16~~	~~CB(2) TRIG R~~
~~X2*~~	~~WH/GRA~~	~~X16~~	~~CB(2) TRIG~~

SHEET 1 OF 6 775A055

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR MCI-CCØ TEST
DWG 775A055 SUB 1 2 3 4 FINISH CHART

FROM Hood #2 TERM	COLOR	TO Hood #4 TERM	REMARKS
X28	BLK	X6	CCØ B.7 - CM (EVEN BIT)
X27	WH./BLK	X10	ARM B.8
X26	BRN	X14	B.9
X25	WH/BRN	X22	B.10
X24	RED	X26	B.11
X23	WH/RED	X30	B.12
X22	GRN	X34	B.13
	WH/GRN		

FROM Hood #4 TERM	COLOR	TO Hood #1 TERM	REMARKS
X8	BLK	X21	CCØ B.7
X12	WH/BLK	X13	N.C. B.8
X16	BRN	X11	B.9
X23	WH/BRN	X9	B.10
X27	RED	X7	B.11
X31	WH/RED	X5	B.12
X35	GRN	X3	B.13
	WH/GRN		

SHEET 2 OF 6 775A055

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR MCI-CCØ TEST
DWG 775A055 SUB XXX4

FINISH CHART

FROM Hood #2 TERM	COLOR	TO Hood #5 TERM	REMARKS
X16	BLK	X6	CCØ B.0 - CM (odd bit)
X15	WH./BLK	X10	ARM B.1
X14	BRN	X14	B.2
X13	WH/BRN	X22	B.3
X12	RED	X26	B.4
X11	WH/RED	X30	B.5
X10	GRN	X34	B.6
	WH/GRN		

FROM Hood #5 TERM	COLOR	TO Hood #1 TERM	REMARKS
X8	BLK	X34	CCØ B.0
X12	WH/BLK	X32	N.C. B.1
X16	BRN	X30	B.2
X23	WH/BRN	X28	B.3
X27	RED	X26	B.4
X31	WH/RED	X24	B.5
X35	GRN	X22	B.6
	WH/GRN		

SHEET 3 OF 6

775A055

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST

TEST CABLE FOR MCI-CCØ TEST

DWG 775 A055 SUB. #7 #4 FINISH CHART

FROM Hood #2 TERM	COLOR	TO Hood #6 TERM	REMARKS
X9	BLK	X6	CCØ B.7 - CM (ODD BIT)
X8	WH./BLK	X10	ARM B.8
X7	BRN	X14	B.9
X6	WH/BRN	X22	B.10
X5	RED	X26	B.11
X4	WH/RED	X30	B.12
X3	GRN	X34	B.13
	WH/GRN		

FROM Hood #6 TERM	COLOR	TO Hood #1 TERM	REMARKS
X8	BLK	X20	CCØ B.7
X12	WH/BLK	X14	N.Ø. B.8
X16	BRN	X12	B.9
X23	WH/BRN	X10	B.10
X27	RED	X8	B.11
X31	WH/RED	X6	B.12
X34	GRN	X4	B.13
	WH/GRN		

SHEET 4 OF 6

775 A055

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR MCI-CB TEST

DWG 775A055 SUB. 1 2 3 4 FINISH CHART

FROM Hood #2 PIN	COLOR	TO POWER SUPPLY	REMARKS	FROM Hood #1 PIN	COLOR	TO POWER SUPPLY	REMARKS
X18	ORANGE	BUS	+48V	X19	BLUE	BUS	48V RET.

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR MCT-CB TEST

DWG 775A055 SUB. X224 FINISH CHART

FROM Hood #1 PIN	COLOR	TO RS. SW. PIN	REMARKS	FROM	COLOR	TO	REMARKS
X17	BLACK	X17	CB (n) TRIG. R				
X18	RED	X18	CB (n) TRIG.				

SHEET 6 OF 6 775A055

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST

TEST CABLE FOR CØ - CB TEST

DWG 775A053 SUB. 1 FINISH CHART

FROM C01	COLOR	TO CB	REMARKS
X8	Black	X35	CB1 B00
X12	White/Bk	X33	B01
X16	Brown	X31	B02
X23	White/Bn	X29	B03
X27	Red	X27	B04
X31	White/Red	X25	B05
X35	Orange	X23	B06
X6	White/O	SPLICE	+48V
X1 *	Yellow	X21	B07
X2 *	White/Y	X13	B08
X3 *	Green	X11	B09
X4 *	White/Gn	X9	B10
X17 *	Blue	X7	B11
X18 *	White/Bu	X5	B12
X19 *	Gray	X3	B13
	White/Gy		

FROM	COLOR	TO	REMARKS

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST

TEST CABLE FOR C∅-CB TEST

DWG 775A053 SUB. 1 FINISH CHART

FROM C01	COLOR	TO C02	REMARKS
	Black		
	White/Bk		
	Brown		
	White/Bn		
	Red		
	White/Red		
	Orange		
X34	White/O	X6	+48V
X1 *	Yellow	X8	CB1 B07
X2 *	White/Y	X12	B08
X3 *	Green	X16	B09
X4 *	White/Gn	X23	B10
X17 *	Blue	X27	B11
X18 *	White/Bu	X31	B12
X19 *	Gray	X35	B13
	White/Gy		

FROM	COLOR	TO	REMARKS

SHEET 2 OF 5 775A053

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR CØ-CB TEST

DWG 775A053 SUB. 1 FINISH CHART

FROM C01	COLOR	TO C01	REMARKS	FROM	COLOR	TO	REMARKS
X7	RED	X10					
X11	↑	X14					
X15	|	X21					
X22	|	X25					
X26	↓	X29					
X30	RED	X33					

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR CØ-CB TEST

DWG. 775A053 SUB. 1 FINISH CHART

FROM CO2	COLOR	TO CO2	REMARKS	FROM	COLOR	TO	REMARKS
X7	RED	X10					
X11	↑	X16					
X15	|	X21					
X22	|	X25					
X26	↓	X29					
X30	RED	X33					

SHEET 4 OF 5 775A053

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR CØ-CB TEST

DWG. 775A053 SUB. 1 FINISH CHART

FROM CB	COLOR	TO Power Supply	REMARKS
SPLICE	RED	BUS	+48V
X19	BLACK	BUS	48V RET.

FROM	COLOR	TO	REMARKS

SHEET 5 OF 5 775A053

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
 1                                          CCO VS OCI TEST
 2
 3                                          PROGRAM LIBRARY
 4                                          PROGRAM NO.   P-50  D19A
 5
 6
 7              00173          BORG 173
18   00173      06721           OCT ASRIN,IRINT,ORINT,INTCCO
     00174      06643
     00175      06650
     00176      06503
11              06000          BORG 6000
12                                         CONTACT CLOSURE OUTPUT CONTROL WORDS
13                        CWDS   RPT 8
14   06000      00000           OCT
     06001      00000
     06002      00000
     06003      00000
     06004      00000
     06005      00000
     06006      00000
     06007      00000
15                                         CONTACT CLOSURE INPUT CONTROL WORDS
16                        IBF    RPT 8
17   06010      00000           OCT
     06011      00000
     06012      00000
     06013      00000
     06014      00000
     06015      00000
     06016      00000
     06017      00000
20   06020      00000   NCCO    OCT
21   06021      00012   CCOI    BOCT 12            CCO COMPLETE
22   06022      00005   ORI     BOCT 5             CCI OUTPUT REQ
23   06023      00004   IRI     BOCT 4             CCI INPUT REQ
24   06024      00011   ASRI    BOCT 11            ASR COMPLETE
25   06025  34 0 000   CCIOUT  BOUT               CCI ADDRESS CHAN
26   06026  30 0 000   CCIINT  BINT               CCI DATA
27   06027  34 0 044   OUTASR  BOUT 44            ASR OUTPUT CHAN
```

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
39                                      EJE
31                                          SET UP CHANNELS AND INTERRUPTS
32   06030   32 0 204    SETUP      ENL RJ176
33   06031   37 1 021               STL CCOI,I
34   06032   32 0 203               ENL RJ175
35   06033   37 1 022               STL ORI,I
36   06034   32 0 202               ENL RJ174
37   06035   37 1 023               STL IRI,I
40   06036   32 0 201               ENL RJ173
41   06037   37 1 024               STL ASRI,I
42   06040   32 0 025               ENL CCIOUT
43   06041   37 1 366   J           STL IRINT-2
44   06042   32 0 026               ENL CCIINT
45   06043   37 1 365   J           STL IRINT+1
46   06044   32 0 027               ENL OUTASR
47   06045   37 1 364   J           STL ASRIN-2
```

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
 50                                    EJE
 51   06046  32 0 363  JCCOCCI ENL 56)
 52   06047  37 0 164          STL T1
 53   06050  32 0 020          ENL NCCO
 54   06051  11 0 362  J       SUB 1)
 55   06052  37 0 200          STL NCCOM1
 56   06053  32 0 361  J       ENL PTRNS+55)
 57   06054  37 0 206          STL PATRN
 60   06055  32 1 206          ENL PATRN,I
 61   06056  37 0 166          STL T3
 62   06057  32 0 360  J       ENL 3)
 63   06060  37 0 207          STL FRSTID
 64   06061  32 0 200          ENL NCCOM1
 65   06062  37 0 072          STL ACW+1
 66   06063  37 0 120          STL CAWC+1
 67   06064  32 0 020          ENL NCCO
 70   06065  37 0 165          STL T2
 71   06066  32 1 206   CCOLOP ENL PATRN,I
 72   06067  13 0 166          EOR T3
 73   06070  37 0 166          STL T3
 74   06071  36 1 357  JACW     RJP ACWR
 75   06072     00000          OCT
 76   06073  01 0 072          DCR L-1
 77   06074  01 0 165          DCR T2
100   06075  27 0 065          PJP CCOLOP
101   06076  01 0 207          DCR FRSTID
102   06077  27 0 101          PJP L+3
103   06100  32 1 206          ENL PATRN,I
104   06101  24 0 102          JMP L+2
105   06102  32 0 356  J       ENL 0)
106   06103  37 0 166          STL T3
107   06104  13 1 206          EOR PATRN,I
110   06105  37 0 167          STL T4
111   06106  32 0 355  J       ENL 100)
112   06107  37 0 354  J       STL 101)
113   06110  01 0 354          DCR 101)
114   06111  27 0 107          PJP L-1
115   06112  32 0 020          ENL NCCO
116   06113  37 0 165          STL T2
117   06114  32 1 206   CCILOP ENL PATRN,I
```

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
120   06115  13 0 167          EOR T4
121   06116  37 0 167          STL T4
122   06117  36 1 353  /CAWC   RJP CAW
123   06120     00000          OCT
124   06121  01 0 120          DCR L-1
125   06122  37 0 171          STL T6
126   06123  13 0 167          EOR T4
127   06124  27 0 126          PJP L+3
130   06125  36 0 210          RJP ERROR
131   06126  24 0 130          JMP L+3
132   06127  20 0 130          ZJP L+2
133   06130  24 0 124          JMP L-3
134   06131  01 0 165          DCR T2
135   06132  27 0 113          PJP CCILOP
136   06133  01 0 207          DCR FRSTID
137   06134  27 0 060          PJP CCOLOP-5
140   06135  01 0 206          DCR PATRN
141   06136  01 0 164          DCR T1
142   06137  27 0 054          PJP CCCCCI+7
143   06140  01 0 205          DCR CYCNT
144   06141  27 0 045          PJP CCOCCI
145   06142  32 0 352  /       ENL 5)
146   06143  37 0 205          STL CYCNT
147                             PRINT END OF CYCLE
150   06144  36 1 351  /       RJP OTRCD
151   06145     06147          OCT COIFMT
152   06146  24 0 045          JMP CCOCCI
153   06147     02323  COIFMT  BCD 12CCU-CCI TEST COMPLETED
      06150     04640
      06151     02323
      06152     03160
      06153     06325
      06154     06263
      06155     06023
      06156     04644
      06157     04743
      06160     02563
      06161     02524
      06162     01460
154   06163     01477          OCT 1477
```

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```
155                                    EJE
156   06164     00000    T1      OCT
157   06165     00000    T2      OCT
160   06166     00000    T3      OCT
161   06167     00000    T4      OCT
162   06170     00000    T5      OCT
163   06171     00000    T6      OCT
164   06172     00000    T7      OCT
165   06173     00000    T8      OCT
166   06174     00000    T9      OCT
167   06175     00000    T10     OCT
170   06176     00000    T11     OCT
171   06177     06000    T12     OCT  6000
172   06200     00000    NCCOM1  OCT
173   06201     36573    RJ173   OCT  36573
174   06202     36574    RJ174   OCT  36574
175   06203     36575    RJ175   OCT  36575
176   06204     36576    RJ176   OCT  36576
177   06205     00005    CYCNT   OCT  5
200   06206     06430    PATRN   DEC  PTRNS+55
201   06207     00003    FRSTID  OCT  3
```

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```
202                                    EJE
203   06210      00000   ERROR   ...
204   06211  32 0 350  /         ENL WAS)
205   06212  36 0 265            RJP SUPZ
206   06213  32 0 167            ENL T4
207   06214  37 0 171            STL T6
210   06215  32 0 347  /         ENL SHBE)
211   06216  36 0 265            RJP SUPZ
212   06217  32 0 120            ENL CAWC+1
213   06220  10 0 362            ADD 1)
214   06221  27 0 222            PJP L+2
215   06222  13 0 346  /         EOR -)
216   06223  37 0 171            STL T6
217   06224  32 0 345  /         ENL REG)
220   06225  36 0 265            RJP SUPZ
221   06226  36 1 351            RJP OTRCD
222   06227      06231            OCT ERCOIF
223   06230  24 1 210   RTNN    RTN
224   06231      02323   ERCOIF  BCD 08CCU-CCI REGISTER X
      06232      04640
      06233      02323
      06234      03160
      06235      05125
      06236      02731
      06237      06263
      06240      02551
225   06241      00000   REG     OCT ,,
      06242      00000
      06243      00000
226   06244      06062           BCD 05 SHOULD BE
      06245      03046
      06246      06443
      06247      02460
      06250      02225
227   06251      00000   SHBE    OCT ,,
      06252      00000
      06253      00000
230   06254      06022           BCD 04 BUT IS X
      06255      06463
      06256      06031
```

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```
          06257     06260
     231  06260     00000   WAS     OCT ,,
          06261     00000
          06262     00000
     232  06263     03314           OCT 3314,7777
          06264     07777
```

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```
233                                    EJE
234   06265      00000    SUPZ    ...
235   06266  37 0 172             STL T7
236   06267  03 0 173             SMB T8
237   06270  03 0 176             SMB T11
240   06271  32 0 360             ENL 3)
241   06272  37 0 174             STL T9
242   06273  32 0 352             ENL 5)
243   06274  37 0 175             STL T10
244   06275  24 0 276             JMP L+2
245   06276  14 0 171   LOOP      LSH T6
246   06277  14 0 171             LSH T6
247   06300  14 0 171             LSH T6
250   06301  32 0 171             ENL T6
251   06302  12 0 174             AND T9
252   06303  20 0 305             ZJP L+3
253   06304  02 0 173             CMB T8
254   06305  24 0 310             JMP L+4
255   06306  16 0 173             RSH T8
256   06307  27 0 310             PJP L+2
257   06310  32 0 344   J         @ENL 60)
260   06311  16 0 176             RSH T11
261   06312  27 0 327             PJP FRSCH
262   06313  13 0 177             EOR T12
263   06314  37 1 172             STL T7,I
264   06315  32 0 172             ENL T7
265   06316  10 0 362             ADD 1)
266   06317  37 0 172             STL T7
267   06320  02 0 176             CMB T11
270   06321  32 0 343   JFORS     ENL 7)
271   06322  37 0 174             STL T9
272   06323  01 0 175             DCR T10
273   06324  27 0 275             PJP LOOP
274   06325  32 0 342   J         @ENL 6000)
275   06326  37 0 177             STL T12
276   06327  24 1 265             RTN
277   06330  14 1 341   JFRSCH    LSH ACC
300   06331  14 1 341             LSH ACC
301   06332  14 1 341             LSH ACC
302   06333  14 1 341             LSH ACC
```

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```
303    06334  14 1 341          LSH ACC
304    06335  14 1 341          LSH ACC
305    06336  37 0 177          STL T12
306    06337  03 0 176          SMB T11
307    06340  24 0 320          JMP FORS
310                              GEN
              06341     00101   WRD
              06342     06000   WRD
              06343     00007   WRD
              06344     00060   WRD
              06345     06241   WRD
              06346     37777   WRD
              06347     06251   WRD
              06350     06260   WRD
              06351     06654   WRD
              06352     00005   WRD
              06353     06631   WRD
              06354     00145   WRD
              06355     00144   WRD
              06356     00000   WRD
              06357     06457   WRD
              06360     00003   WRD
              06361     06430   WRD
              06362     00001   WRD
              06363     00070   WRD
              06364     06717   WRD
              06365     06644   WRD
              06366     06641   WRD
```

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```
P     311                          PTRNS  RPT 7
      312   06367     25252               OCT 25252,12525
            06370     12525
            06371     25252
            06372     12525
            06373     25252
            06374     12525
            06375     25252
            06376     12525
            06377     25252
            06400     12525
            06401     25252
            06402     12525
            06403     25252
            06404     12525
      313   06405     37777               OCT 37777,37776,37774,37770,37760,37740,37700,37600,37400,37000
            06406     37776
            06407     37774
            06410     37770
            06411     37760
            06412     37740
            06413     37700
            06414     37600
            06415     37400
            06416     37000
      314   06417     36000               OCT 36000,34000,30000,20000
            06420     34000
            06421     30000
            06422     20000
      315   06423     20000               OCT 20000,10000,4000,2000,1000,400,200,100,40,20,10,4,2,1
            06424     10000
            06425     04000
            06426     02000
            06427     01000
            06430     00400
            06431     00200
            06432     00100
            06433     00040
            06434     00020
            06435     00010
```

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```
            06436     00004
            06437     00002
            06440     00001
316
317         06441     37777          HPT 7
            06442     37777          OCT 37777,37777
            06443     37777
            06444     37777
            06445     37777
            06446     37777
            06447     37777
            06450     37777
            06451     37777
            06452     37777
            06453     37777
            06454     37777
            06455     37777
            06456     37777
```

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
320                                     EJE
321                                         ROUTINE TO SIMULATE ACW WITHOUT EXECUTIVES.
322   06457      00000    ACWR    ...
323   06460   37 0 115             STL DATA
324   06461   32 0 057             ENL ACWR
325   06462   10 0 140  J          ADD 1)
326   06463   37 0 057             STL ACWR
327   06464   32 1 057             ENL ACWR,I
330   06465   37 0 116             STL REGA
331   06466   10 0 137  J          ADD CWDS)
332   06467   37 0 117             STL CWD
333   06470   32 1 117             ENL CWD,I
334   06471   37 0 120             STL CHWD
335   06472   32 0 116             ENL REGA
336   06473   10 0 136  J          ADD BUF)
337   06474   37 0 117             STL CWD
340   06475   32 0 135  J          ENL 2)
341   06476   37 0 121             STL IFLG
342   06477   32 0 115             ENL DATA
343   06500   37 1 117             STL CWD,I
344   06501   34 1 120   OUTC      OUT CHWD,I
345   06502   01 1 134  J          DCR PC
346   06503      00000    INTCCO  ...
347   06504   32 0 121             ENL IFLG
350   06505   20 0 121             ZJP STOP
351   06506   01 0 121             DCR IFLG
352   06507   20 0 113             ZJP L+5
353   06510   01 0 120             DCR CHWD
354   06511   32 1 117             ENL CWD,I
355   06512   13 0 133  J          EOR -)
356   06513   23 0 100             CLJ OUTC
357   06514   23 1 057             CLJ ACWR,I
```

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```
      360                                    EJE
      361   06515      00000    DATA    OCT
      362   06516      00000    REGA    OCT
      363   06517      00000    CWD     OCT
      364   06520      00000    CHWD    OCT
      365   06521      00000    IFLG    OCT
      366   06522   00 0 077    STOP    BSTP 77
      367                      BUF     HPT 8
      370   06523      00000           OCT
            06524      00000
            06525      00000
            06526      00000
            06527      00000
            06530      00000
            06531      00000
            06532      00000
      371                              GEN
            06533      37777           WRD
            06534      00000           WRD
            06535      00002           WRD
            06536      06523           WRD
            06537      06000           WRD
            06540      00001           WRD
```

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
372                                        ROUTINES FOR SBO AND SBZ WITHOUT EXECUTIVES.
373   06541      00000   SBO     ...
374   06542  32 0 351  /         ENL -)
375   06543  37 0 210            STL MASK
376   06544  32 0 141            ENL SBO
377   06545  24 0 151            JMP SBZ+4
400   06546      00000   SBZ     ...
401   06547  32 0 350  /         ENL 0)
402   06550  37 0 210            STL MASK
403   06551  32 0 146            ENL SBZ
404   06552  10 0 347  /         ADD 1)
405   06553  37 0 146            STL SBZ
406   06554  32 1 146            ENL SBZ,I
407   06555  12 0 346  /        8AND 17)
410   06556  37 0 211            STL BIT
411   06557  32 1 146            ENL SBZ,I
412   06560  16 1 345  /         RSH ACC
413   06561  16 1 345            RSH ACC
414   06562  16 1 345            RSH ACC
415   06563  16 1 345            RSH ACC
416   06564  37 0 202            STL ACWC+1
417   06565  10 0 344  /         ADD BUF)
420   06566  37 0 212            STL INIT
421   06567  32 0 211            ENL BIT
422   06570  10 0 343  /         ADD MAST)
423   06571  37 0 211            STL BIT
424   06572  32 1 211            ENL BIT,I
425   06573  37 0 211            STL BIT
426   06574  32 0 210            ENL MASK
427   06575  27 0 203            PJP SBZA
430   06576  13 0 211            EOR BIT
431   06577  12 0 212            AND INIT
432   06600  13 0 211            EOR BIT
433   06601  36 0 057   ACWC     RJP ACWR
434   06602      00000            OCT
435   06603  24 1 146            RTN
436   06604  32 0 351   SBZA     ENL -)
437   06605  13 0 211            EOR BIT
440   06606  12 0 212            AND INIT
441   06607  24 0 200            JMP ACWC
```

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```
442   06610   00000   MASK   OCT
443   06611   00000   BIT    OCT
444   06612   00000   INIT   OCT
445   06613   00001   MAST   OCT 1,2,4,10,20,40,100,200,400,1000,2000,4000,10000,20000
      06614   00002
      06615   00004
      06616   00010
      06617   00020
      06620   00040
      06621   00100
      06622   00200
      06623   00400
      06624   01000
      06625   02000
      06626   04000
      06627   10000
      06630   20000
```

```
446                                     EJE
447   06631       00000   CAW
450   06632   32  0 251               ENL  CAW
451   06633   10  0 347               ADD  1)
452   06634   37  0 251               STL  CAW
453   06635   32  1 251               ENL  CAW,I
454   06636   10  0 342   J           ADD  (WF)
455   06637   37  0 253               STL  TEMP
456   06640   32  1 253               ENL  TEMP,I
457   06641   34  0 000               OCT
460   06642   01  1 350               DCR  PC
461   06643       00000   IRINT
462   06644   30  0 000               INT
463   06645   37  0 253               STL  TEMP
464   06646   23  0 246               CLJ  L+1
465   06647   01  1 350               DCR  PC
466   06650       00000   ORINT
467   06651   32  0 253               ENL  TEMP
470   06652   23  1 251               CLJ  CAW,I
471   06653       00000   TEMP        OCT
```

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```
472                                     EJE
473   06654      00000   OTRCD          .          PRINT RECORD TERMINATED BY 77 CODE
474   06655  32 0 254                   ENL OTRCD
475   06656  10 0 347                   ADD 1)
476   06657  37 0 254                   STL OTRCD
477   06660  32 1 254                   ENL OTRCD.I
500   06661  37 0 311                   STL OTADS
501   06662  03 0 312                   SMB OTIND
502   06663  32 1 311   OTLOP           ENL OTADS.I
503   06664  16 0 312                   RSH OTIND
504   06665  27 0 273                   PJP SECND
505   06666  16 1 345                   RSH ACC
506   06667  16 1 345                   RSH ACC
507   06670  16 1 345                   RSH ACC
510   06671  16 1 345                   RSH ACC
511   06672  16 1 345                   RSH ACC
512   06673  16 1 345                   RSH ACC
513   06674  12 0 341   JSECND          8AND 77)
514   06675  11 0 341                   8SUB 77)
515   06676  20 1 254                   ZJP OTRCD.I
516   06677  10 0 341                   8ADD 77)
517   06700  27 0 301                   PJP L+2
520   06701  32 0 350                   ENL 0)
521   06702  36 0 313                   RJP OT1
522   06703  32 0 311                   ENL OTADS
523   06704  10 0 347                   ADD 1)
524   06705  16 0 312                   RSH OTIND
525   06706  27 0 260                   PJP OTLOP-2
526   06707  02 0 312                   CMB OTIND
527   06710  24 0 262                   JMP OTLOP
530   06711      00000   OTADS          OCT
531   06712      00000   OTIND          OCT
```

```
532                                     EJE
533    06713        00000    OT1        ...
534    06714   10 0 340  J             ADD TBL)
535    06715   37 0 335                 STL ADS
536    06716   32 1 335                 ENL ADS,1
537    06717   34 0 000                 OUT
540    06720   01 1 350                 UCR PC
541    06721        00000    ASRIN      ...
542    06722   32 0 335                 ENL ADS
543    06723   20 0 330                 ZJP !GNORA
544    06724   11 0 337  J              BSUB TBL+14)
545    06725   20 0 331                 ZJP LFD
546    06726   32 0 350                 ENL 0)
547    06727   37 0 335                 STL ADS
550    06730   23 1 313                 CLJ OT1,I
551    06731   23 1 321    IGNORA       CLJ ASRIN,I
552    06732   32 0 336  JLFD          BENL 30500)
553    06733   37 0 335                 STL ADS
554    06734   23 0 316                 CLJ OT1+4
555    06735        00000    ADS        OCT
556                                     GEN
       06736        30500              WRD
       06737        06766              WRD
       06740        06752              WRD
       06741        00077              WRD
       06742        06010              WRD
       06743        06613              WRD
       06744        06523              WRD
       06745        00101              WRD
       06746        00017              WRD
       06747        00001              WRD
       06750        00000              WRD
       06751        37777              WRD
```

```
      557                          COD    VFD 1,8,5
      560                          CDE    MAC A,B,C,D,E,F,G,H
      561                                 COD 1,A,
      562                                 COD 1,B,
      563                                 COD 1,C,
      564                                 COD 1,D,
      565                                 COD 1,E,
      566                                 COD 1,F,
      567                                 COD 1,G,
      570                                 COD 1,H,
      571                                 TER
      572                          TBL    8CDE 260,261,262,263,264,265,266,267
      572   06752      33000              COD 1,260,
      572   06753      33040              COD 1,261,
      572   06754      33100              COD 1,262,
      572   06755      33140              COD 1,263,
      572   06756      33200              COD 1,264,
      572   06757      33240              COD 1,265,
      572   06760      33300              COD 1,266,
      572   06761      33340              COD 1,267,
      573                                 8CDE 270,271,336,275,215,272,276,241
      573   06762      33400              COD 1,270,
      573   06763      33440              COD 1,271,
      573   06764      35700              COD 1,336,
      573   06765      33640              COD 1,275,
      573   06766      30640              COD 1,215,
      573   06767      33500              COD 1,272,
      573   06770      33700              COD 1,276,
      573   06771      32040              COD 1,241,
      574                                 8CDE 253,301,302,303,304,305,306,307
      574   06772      32540              COD 1,253,
      574   06773      34040              COD 1,301,
      574   06774      34100              COD 1,302,
      574   06775      34140              COD 1,303,
      574   06776      34200              COD 1,304,
      574   06777      34240              COD 1,305,
      574   07000      34300              COD 1,306,
      574   07001      34340              COD 1,307,
      575                                 8CDE 310,311,277,256,251,333,274,243
      575   07002      34400              COD 1,310,
```

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```
575   07003    34440        COD 1.311.
575   07004    33740        COD 1.277.
575   07005    32700        COD 1.256.
575   07006    32440        COD 1.251.
575   07007    35540        COD 1.333.
575   07010    33600        COD 1.274.
575   07011    32140        COD 1.243.
576                         8CDE 255,312,313,314,315,316,317,320
576   07012    32640        COD 1.255.
576   07013    34500        COD 1.312.
576   07014    34540        COD 1.313.
576   07015    34600        COD 1.314.
576   07016    34640        COD 1.315.
576   07017    34700        COD 1.316.
576   07020    34740        COD 1.317.
576   07021    35000        COD 1.320.
577                         8CDE 321,322,337,244,252,335,273,300
577   07022    35040        COD 1.321.
577   07023    35100        COD 1.322.
577   07024    35740        COD 1.337.
577   07025    32200        COD 1.244.
577   07026    32500        COD 1.252.
577   07027    35640        COD 1.335.
577   07030    33540        COD 1.273.
577   07031    34000        COD 1.300.
600                         8CDE 240,257,323,324,325,326,327,330
600   07032    32000        COD 1.240.
600   07033    32740        COD 1.257.
600   07034    35140        COD 1.323.
600   07035    35200        COD 1.324.
600   07036    35240        COD 1.325.
600   07037    35300        COD 1.326.
600   07040    35340        COD 1.327.
600   07041    35400        COD 1.330.
601                         8CDE 331,332.245,254,250,246,334,212
601   07042    35440        COD 1.331.
601   07043    35500        COD 1.332.
601   07044    32240        COD 1.245.
601   07045    32600        COD 1.254.
601   07046    32400        COD 1.250.
```

DATE 4/15/65. TIME 2/44/07 A.M.

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

```
601   07047   32300        COD 1.246.
601   07050   35600        COD 1.334.
601   07051   30500        COD 1.212.
602           00000        END
```

PROJECT NO. 530053 PROGRAMMER D. HEYING TAPE NUMBER 447514

STARTED 10/10/65. 2/52/00 A.M.
COMPLETED 4/14/65. 2/44/07 A.M.
NUMBER OF INPUT RECORDS 386.
NUMBER OF OUTPUT RECORDS 610.
NUMBER OF BINARY RECORDS 563.

CONTACT CLOSURE OUTPUT VS. PROCESS INTERRUPT TEST (D20.

I. Purpose of Test

To check up to four words of process interrupts by connecting them to the same number of contact closure output words.

II. Description of Test

The program consists of four parts.

In part one, initialization, all contacts are opened and the corresponding interrupt images are cleared to positive zero.

In part two, the following sequence is executed: close a contact, check for an interrupt (one and only one interrupt should occur); open the same contact, check for an interrupt (no interrupt should occur). All contacts are tested.

In part three the following sequence is executed: close a contact, check for an interrupt (one and only one interrupt should occur); repeat until all contacts are closed.

In part four the following sequence is executed: open a contact check for an interrupt (no interrupt should occur); close a contact, check for an interrupt (one and only one interrupt should occur). All contacts are tested.

III. Description of Operation

A. Read in the binary tape of the Contact Closure Output vs. Process Interrupt test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (X7602); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.

B. Enter the test parameters.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the S-Register with the parameter location.
3. Using the probe, load the X-Register with the parameter constant; depress the Start button.
4. Repeat 2 and 2 until all the following parameters have been entered.

Location		Description
5400_8	CCØ	Contact closure output (CCØ) completion interrupt location.
5401_8	ASR	ASR output completion interrupt location
5402_8	ASRCHN	ASR output channel number

Location		Description
5403_8	CØN	Number of contacts which are connected to process interrupts; the maximum number is 56_{10}. Bit 0 of first CCØ word is connected to first process interrupt, Bit 1 to second, etc.
5404_8	PRI	Location of first process interrupt which is connected to a contact closure output (CCØ). The process interrupts are assigned sequentially to the CCØ's.
5405_8 - 5410_8	CWDS	Contact closure output (CCØ) control words, one for each register. Each control word contains the word (bits 13-6) and the set channel (bits 5-0) for a particular output.

C. Start the test

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the test (5410_8); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Clear lockout and hit flip-flops using the probe; depress the Start button.

D. Test runs continuously, printing out the following completion message on the ASR set after ten runs (one cycle).

CCØ-PRI TEST COMPLETE

E. When an error occurs a message is printed out on the ASR set, and the test continues. The error message format is:

CCØINT IS aa SHOULD BE bb

where

aa = interrupt* which occurred (octal number)
bb = interrupt* which should have occurred (octal number)

IV. Storage

Number of locations used: 2052_8 (5400_8 - 7451_8)

V. CCØ vs. Interrupt Test Cable

Drawing 775A054 shows the connections for the CCØ vs. Interrupt Test Cable.

Note: This test will not check interrupts 0-17 (core location 1-20).

* The interrupt numbers assigned sequentially, beginning with one, to the process interrupts used for the test. That is, the first process interrupt used is one (01), the second is two (02), etc.

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST

TEST CABLE FOR CO-4IF TEST

DWG 775A054 SUB. 1 FINISH CHART

FROM CO1	COLOR	TO 4IF	REMARKS	FROM	COLOR	TO	REMARKS
X8	Black	X35	CD (N) B00				
X7	White/Bk	X34	B00R				
X12	Brown	X33	B01				
X11	White/Br	X32	B01R				
X16	Red	X31	B02				
X15	White/Red	X30	B02R				
X23	Orange	X29	B03				
X22	White/O	X28	B03R				
X27	Yellow	X27	B04				
X26	White/Y	X26	B04R				
X31	Green	X25	B05				
X30	White/Gn	X24	B05R				
X35	Blue	X23	B06				
X34	White/Bu	X22	B06R				
X19*	Gray	X21	B07				
X18*	White/Gy	X20	B07R				

SHEET 1 OF 2 775A054

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

TITLE PRODAC 50/550 CABLE WIRING LIST
TEST CABLE FOR CO-4IF TEST

DWG 775A054 SUB. 1 FINISH CHART

FROM C01	COLOR	TO C02	REMARKS	FROM	COLOR	TO	REMARKS
X19*	BLACK	X8					
X18*	RED	X7					

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
 1                                          CCO VS PROCESS INTERRUPT TEST
 2
 3                                          PROGRAM LIBRARY
 4                                          PROGRAM NO.   P-50  020A
 5
 6
 7              05400           BORG 5400
10                      STC     MAC
11                              ENL L-1
12                              STL CONTAT
13                              TER
14                      RTC     MAC SBOSBZ
15                              ENL CONTAT
16                              STL SBOSBZ+1
17                              TER
20                      ITR     MAC N
21                              ...
22                              SDR TEMPX
23                              DCR TABLE-N
24                              EDR TEMPX
25                              CLJ L-4,1
26                              TER
27    05400     00000   CCO     OCT         CCO INTERRUPT NUMBER
30    05401     00000   ASR     OCT         ASR INTERRUPT NUMBER
31    05402     00000   ASRCHN  OCT         ASR CHANNEL NUMBER
32    05403     00000   CON     OCT               NUMBER OF CONTACTS
33    05404     00000   FRI     OCT               FIRST PROCESS INTERRUPT
34                      CONS    RPT 4
35    05405     00000           OCT
      05406     00000
      05407     00000
      05410     00000
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
 36                                      EJE
 37   05411  32 0 002    SETUP  ENL ASRCHN
 40   05412  13 0 364  J        8EOR 34000)
 41   05413  37 1 363  J         STL OUT
 42   05414  32 0 001            ENL ASR
 43   05415  10 0 362  J         ADD 65)
 44   05416  37 0 255            STL TEMP
 45   05417  13 0 361  J        8EOR 36400)
 46   05420  37 1 001            STL ASR,I
 47   05421  32 0 360  J         ENL ASRIN)
 50   05422  37 1 255            STL TEMP,I
 51   05423  32 0 000            ENL CCO
 52   05424  10 0 362            ADD 65)
 53   05425  37 0 255            STL TEMP
 54   05426  13 0 361           8EOR 36400)
 55   05427  37 1 000            STL CCO,I
 56   05430  32 0 357  J         ENL INTCCO)
 57   05431  37 1 255            STL TEMP,I
 60   05432  32 0 003    START  ENL CON
 61   05433  10 1 356  J         ADD SS1
 62   05434  37 0 255            STL TEMP
 63   05435  32 0 355  J         ENL LASTAD)
 64   05436  37 1 354  J         STL LAST
 65   05437  32 0 004            ENL PRI
 66   05440  37 0 253    AA      STL INDEX
 67   05441  10 0 362           8ADD 101)
 70   05442  37 0 254            STL JUMP
 71   05443  13 0 361           8EOR 36400)
 72   05444  37 1 253            STL INDEX,I
 73   05445  32 1 354            ENL LAST
 74   05446  37 1 254            STL JUMP,I
 75   05447  01 1 354            DCR LAST
 76   05450  01 1 354            DCR LAST
 77   05451  01 1 354            DCR LAST
100   05452  01 1 354            DCR LAST
101   05453  01 1 354            DCR LAST
102   05454  32 0 253            ENL INDEX
103   05455  10 1 356            ADD SS1
104   05456  01 0 255            DCR TEMP
105   05457  27 0 037            PJP AA
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512.06

```
106   05460   32 0 353  JCC      ENL 10)
107   05461   37 1 352  J        STL CTR
110   05462   36 0 267   BB      RJP INITLX
111                               RTC SBZC
111   05463   32 0 256           ENL CONTAT
111   05464   37 0 070           STL SBZ0+1
112   05465   32 0 256           ENL CONTAT
113   05466   37 0 070           STL SBZ0+1
114   05467   36 1 351  JSBZ0    RJP SBZ
115   05470       00000          OCT
116                               STC
116   05471   32 0 070           ENL L-1
116   05472   37 0 256           STL CONTAT
117   05473   32 0 353  J        ENL 10000)
120   05474   01 1 362           DCR ACC
121   05475   27 0 073           RJP L-2
122   05476   32 1 347  J        ENL SS0
123   05477   37 1 257           STL ITABX,I
124   05500   36 1 346  J        RJP ICRCON
125   05501   01 0 257           DCR ITABX
126   05502   01 1 345  J        DCR INDEXX
127   05503   27 0 062           RJP BB+1
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
130                                        EJE
131   05504  36 0 267   TEST1  RJP INITLX
132                              RTC SB01
132   05505  32 0 256           ENL CONTAT
132   05506  37 0 112           STL SB01+1
133                              RTC SBZ1
133   05507  32 0 256           ENL CONTAT
133   05510  37 0 130           STL SBZ1+1
134   05511  36 1 344  /SB01     RJP SB0
135   05512     00000           OCT
136                              STC
136   05513  32 0 112           ENL L-1
136   05514  37 0 256           STL CONTAT
137   05515  32 0 350   WAITA BENL 10000)
140   05516  01 1 362           DCR ACC
141   05517  27 0 115           PJP L-1
142   05520  32 1 257           ENL ITABX,I
143   05521  10 1 356           ADD SS1
144   05522  37 1 257           STL ITABX,I
145   05523  27 0 124           PJP L+2
146   05524  24 0 125           JMP L+2
147   05525  36 0 240           RJP ERR1
150   05526  36 0 277           RJP ZINTCK
151   05527  36 1 351   SBZ1    RJP SBZ
152   05530     00000           OCT
153   05531  32 0 350   WAITB BENL 10000)
154   05532  01 1 362           DCR ACC
155   05533  27 0 131           PJP L-1
156   05534  32 1 257           ENL ITABX,I
157   05535  20 0 136           ZJP L+2
160   05536  36 1 343  /        RJP ERR2
161   05537  03 1 342  /        SMB FLAG
162   05540  36 0 277           RJP ZINTCK
163   05541  36 1 346           RJP ICRCUN
164   05542  01 0 257           DCR ITABX
165   05543  01 1 345           DCR INDEXX
166   05544  27 0 104           PJP TEST1+1
```

```
167                                     EJE
170   05545   36 0 267    TEST2   RJP INITLX
171                                     RTC S802
171   05546   32 0 256                  ENL CONTAT
171   05547   37 0 151                  STL S802+1
172   05550   36 1 344    S802    RJP S80
173   05551       00000               OCT
174                                     STC
174   05552   32 0 151                  ENL L-1
174   05553   37 0 256                  STL CONTAT
175   05554   32 0 350    WAITC 8ENL 10000)
176   05555   01 1 362                  DCR ACC
177   05556   27 0 154                  PJP L-1
200   05557   32 1 257                  ENL ITABX,I
201   05560   10 1 356                  ADD SS1
202   05561   37 1 257                  STL ITABX,I
203   05562   27 0 163                  PJP L+2
204   05563   24 0 164                  JMP L+2
205   05564   36 0 240                  RJP ERR1
206   05565   36 0 277                  RJP ZINTCK
207   05566   36 1 346                  RJP ICRCON
210   05567   01 0 257                  DCR ITABX
211   05570   01 1 345                  DCR INDEXX
212   05571   27 0 145                  PJP TEST2+1
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
213                                     EJE
214   05572  36 0 267   TEST3  RJP INITLX
215                                     RTC SB03
215   05573  32 0 256                   ENL CONTAT
215   05574  37 0 214                   STL SB03+1
216                                     RTC SBZ3
216   05575  32 0 256                   ENL CONTAT
216   05576  37 0 200                   STL SBZ3+1
217   05577  36 1 351   SBZ3   RJP SBZ
220   05600      00000                  OCT
221                                     STC
221   05601  32 0 200                   ENL L-1
221   05602  37 0 256                   STL CONTAT
222   05603  32 0 350   WAITD BENL 10000)
223   05604  01 1 362                   DCR ACC
224   05605  27 0 203                   PJP L-1
225   05606  32 1 257                   ENL ITABX,I
226   05607  20 0 210                   ZJP L+2
227   05610  36 1 343                   RJP ERR2
230   05611  03 1 342                   SMB FLAG
231   05612  36 0 277                   RJP ZINTCK
232   05613  36 1 344   SB03   RJP SB0
233   05614      00000                  OCT
234   05615  32 0 350   WAITE BENL 10000)
235   05616  01 1 362                   DCR ACC
236   05617  27 0 215                   PJP L-1
237   05620  32 1 257                   ENL ITABX,I
240   05621  10 1 356                   ADD SS1
241   05622  37 1 257                   STL ITABX,I
242   05623  27 0 224                   PJP L+2
243   05624  24 0 225                   JMP L+2
244   05625  36 0 240                   RJP ERR1
245   05626  36 0 277                   RJP ZINTCK
246   05627  36 1 346                   RJP ICRCON
247   05630  01 0 257                   DCR ITABX
250   05631  01 1 345                   DCR INDEXX
251   05632  27 0 172                   PJP TEST3+1
252   05633  01 1 352                   DCR CTR
253   05634  27 0 061                   PJP BR
254   05635  36 1 341   J               RJP OTHCH
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
255   05636      07374            OCT COMPLT
256   05637  24 0 057             JMP CC
257
260   05640      00000   ERR1     ...
261   05641  32 1 340   J         ENL TT
262   05642  11 0 257             SUB ITABX
263   05643  36 1 337   J         RJP CNVTA
264   05644  37 1 336   J         STL INTR
265   05645  32 1 347             ENL SS0
266   05646  37 1 335   J         STL INTW
267   05647  37 1 257             STL ITABX.I
270   05650  36 1 341             RJP OTRCD
271   05651      07356            OCT FORMAT
272   05652  24 1 240             RTN
273   05653      00000   INDEX    OCT
274   05654      00000   JUMP     OCT
275   05655      00000   TEMP     OCT
276   05656      00000   CONTAT   OCT
277   05657      00000   ITABX    OCT
300   05660      00000   ITAB     OCT
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
301                                     EJE
302   05661      00000   INITAL ...
303   05662  32 1 334  J         ENL T
304   05663  37 0 260            STL ITAB
305   05664  32 0 003            ENL CON
306   05665  37 0 253            STL INDEX
307   05666  24 1 261            RTN
310   05667      00000   INITLX ...
311   05670  32 1 334            ENL T
312   05671  37 0 257            STL ITABX
313   05672  32 0 003            ENL CON
314   05673  37 1 345            STL INDEXX
315   05674  32 1 333  J         ENL SSX
316   05675  37 0 256            STL CONTAT
317   05676  24 1 267            RTN
320   05677      00000   ZINTCK ...
321   05700  36 0 261            MJP INITAL
322   05701  32 1 260            ENL ITAB,I
323   05702  20 0 305            ZJP ZXX
324   05703  10 1 356            ADD SS1
325   05704  37 1 260            STL ITAB,I
326   05705  24 0 312            JMP ERR3
327   05706  01 0 260   ZXX      DCR ITAB
330   05707  01 0 253            DCR INDEX
331   05710  27 0 300            PJP ZINTCK+2
332   05711  02 1 342            CMB FLAG
333   05712  24 1 277            RTN
334   05713  32 1 342   ERR3     ENL FLAG
335   05714  27 0 317            PJP L+4
336   05715  32 1 347            ENL SS0
337   05716  37 1 336            STL INTR
340   05717  24 0 323            JMP L+5
341   05720  32 1 340            ENL TT
342   05721  11 0 257            SUB ITABX
343   05722  36 1 337            MJP CNVTA
344   05723  37 1 336            STL INTR
345   05724  32 1 340            ENL TT
346   05725  11 0 260            SUB ITAB
347   05726  36 1 337            MJP CNVTA
350   05727  37 1 335            STL INTW
```

PROJECT NO. 530053 PROGRAMMER J.S. PHILLIPPI TAPE NUMBER 512606

```
351   05730  36 1 341          RJP OTRCD
352   05731     07356          OCT FORMAT
353   05732  24 0 277          JMP ZINTCK+1
      05733     07346          WRD
      05734     06070          WRD
      05735     07363          WRD
      05736     07372          WRD
      05737     06525          WRD
      05740     06071          WRD
      05741     07000          WRD
      05742     07344          WRD
      05743     07424          WRD
      05744     07236          WRD
      05745     07345          WRD
      05746     07410          WRD
      05747     07517          WRD
      05750     10000          WRD
      05751     07343          WRD
      05752     07343          WRD
      05753     00012          WRD
      05754     07355          WRD
      05755     06523          WRD
      05756     07350          WRD
      05757     07206          WRD
      05760     07045          WRD
      05761     16400          WRD
      05762     00001          WRD
      05763     07343          WRD
      05764     34000          WRD
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
354                 06000          8ORG 6000
355                                 RPT 55
356     06000       00000           OCT
        06001       00000
        06002       00000
        06003       00000
        06004       00000
        06005       00000
        06006       00000
        06007       00000
        06010       00000
        06011       00000
        06012       00000
        06013       00000
        06014       00000
        06015       00000
        06016       00000
        06017       00000
        06020       00000
        06021       00000
        06022       00000
        06023       00000
        06024       00000
        06025       00000
        06026       00000
        06027       00000
        06030       00000
        06031       00000
        06032       00000
        06033       00000
        06034       00000
        06035       00000
        06036       00000
        06037       00000
        06040       00000
        06041       00000
        06042       00000
        06043       00000
        06044       00000
        06045       00000
```

```
          06046     00000
          06047     00000
          06050     00000
          06051     00000
          06052     00000
          06053     00000
          06054     00000
          06055     00000
          06056     00000
          06057     00000
          06060     00000
          06061     00000
          06062     00000
          06063     00000
          06064     00000
          06065     00000
          06066     00000
     357  06067     00000    TABLE  OCT
     358  06070     06067            OCT TABLE
     359  06071     06070            OCT TABLE+1
     361  06072     00001    TEMPX   OCT
     363  06073     00004            OCT
     364  06074     00001            OCT
     365                             ITR 55
     365  06075     00001            ...
     365  06076  06 0 072            SDR TEMPX
     365  06077  01 0 001            DCR TABLE-55
     365  06100  05 0 072            EDR TEMPX
     365  06101  23 1 035            CLJ L-4,1
     366                             ITR 54
     366  06102     00000            ...
     366  06103  06 0 072            SDR TEMPX
     366  06104  01 0 001            DCR TABLE-54
     366  06105  05 0 072            EDR TEMPX
     366  06106  23 1 102            CLJ L-4,1
     367                             ITR 53
     367  06107     00000            ...
     367  06110  06 0 072            SDR TEMPX
     367  06111  01 0 002            DCR TABLE-53
     367  06112  05 0 072            EDR TEMPX
```

```
367   06113  23 1 107          CLJ L-4.1
370                            ITR 52
370   06114     00000          ...
370   06115  06 0 072          SDR TEMPX
370   06116  01 0 003          DCR TABLE-52
370   06117  05 0 072          EDR TEMPX
370   06120  23 1 114          CLJ L-4.1
371                            ITR 51
371   06121     00000          ...
371   06122  06 0 072          SDR TEMPX
371   06123  01 0 004          DCR TABLE-51
371   06124  05 0 072          EDR TEMPX
371   06125  23 1 121          CLJ L-4.1
372                            ITR 50
372   06126     00000          ...
372   06127  06 0 072          SDR TEMPX
372   06130  01 0 005          DCR TABLE-50
372   06131  05 0 072          EDR TEMPX
372   06132  23 1 126          CLJ L-4.1
373                            ITR 49
373   06133     00000          ...
373   06134  06 0 072          SDR TEMPX
373   06135  01 0 006          DCR TABLE-49
373   06136  05 0 072          EDR TEMPX
373   06137  23 1 133          CLJ L-4.1
374                            ITR 48
374   06140     00000          ...
374   06141  06 0 072          SDR TEMPX
374   06142  01 0 007          DCR TABLE-48
374   06143  05 0 072          EDR TEMPX
374   06144  23 1 140          CLJ L-4.1
375                            ITR 47
375   06145     00000          ...
375   06146  06 0 072          SDR TEMPX
375   06147  01 0 010          DCR TABLE-47
375   06150  05 0 072          EDR TEMPX
375   06151  23 1 145          CLJ L-4.1
376                            ITR 46
376   06152     00000          ...
376   06153  06 0 072          SDR TEMPX
```

```
376   06154  01 0 011          DCR TABLE-46
376   06155  05 0 072          EDR TEMPX
376   06156  23 1 152          CLJ L-4,I
377                            ITR 45
377   06157     00000          ...
377   06160  06 0 072          SDR TEMPX
377   06161  01 0 012          DCR TABLE-45
377   06162  05 0 072          EDR TEMPX
377   06163  23 1 157          CLJ L-4,I
400                            ITR 44
400   06164     00000          ...
400   06165  06 0 072          SDR TEMPX
400   06166  01 0 013          DCR TABLE-44
400   06167  05 0 072          EDR TEMPX
400   06170  23 1 164          CLJ L-4,I
401                            ITR 43
401   06171     00000          ...
401   06172  06 0 072          SDR TEMPX
401   06173  01 0 014          DCR TABLE-43
401   06174  05 0 072          EDR TEMPX
401   06175  23 1 171          CLJ L-4,I
402                            ITR 42
402   06176     00000          ...
402   06177  06 0 072          SDR TEMPX
402   06200  01 0 015          DCR TABLE-42
402   06201  05 0 072          EDR TEMPX
402   06202  23 1 176          CLJ L-4,I
402                            ITR 41
403   06203     00000          ...
403   06204  06 0 072          SDR TEMPX
403   06205  01 0 016          DCR TABLE-41
403   06206  05 0 072          EDR TEMPX
403   06207  23 1 203          CLJ L-4,I
404                            ITR 40
404   06210     00000          ...
404   06211  06 0 072          SDR TEMPX
404   06212  01 0 017          DCR TABLE-40
404   06213  05 0 072          EDR TEMPX
404   06214  23 1 210          CLJ L-4,I
405                            ITR 39
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
405   06215      00000          ...
405   06216   06 0 072          SDR TEMPX
405   06217   01 0 020          DCR TABLE-39
405   06220   05 0 072          EDR TEMPX
405   06221   23 1 215          CLJ L-4,I
406                             ITR 38
406   06222      00000          ...
406   06223   06 0 072          SDR TEMPX
406   06224   01 0 021          DCR TABLE-38
406   06225   05 0 072          EDR TEMPX
406   06226   23 1 222          CLJ L-4,I
407                             ITR 37
407   06227      00000          ...
407   06230   06 0 072          SDR TEMPX
407   06231   01 0 022          DCR TABLE-37
407   06232   05 0 072          EDR TEMPX
407   06233   23 1 227          CLJ L-4,I
410                             ITR 36
410   06234      00000          ...
410   06235   06 0 072          SDR TEMPX
410   06236   01 0 023          DCR TABLE-36
410   06237   05 0 072          EDR TEMPX
410   06240   23 1 234          CLJ L-4,I
411                             ITR 35
411   06241      00000          ...
411   06242   06 0 072          SDR TEMPX
411   06243   01 0 024          DCR TABLE-35
411   06244   05 0 072          EDR TEMPX
411   06245   23 1 241          CLJ L-4,I
412                             ITR 34
412   06246      00000          ...
412   06247   06 0 072          SDR TEMPX
412   06250   01 0 025          DCR TABLE-34
412   06251   05 0 072          EDR TEMPX
412   06252   23 1 246          CLJ L-4,I
413                             ITR 33
413   06253      00000          ...
413   06254   06 0 072          SDR TEMPX
413   06255   01 0 026          DCR TABLE-33
413   06256   05 0 072          EDR TEMPX
```

```
413   06257  23 1 253          CLJ L-4,I
414                            ITR 32
414   06260      00000         ...
414   06261  06 0 072          SDR TEMPX
414   06262  01 0 027          DCR TABLE-32
414   06263  05 0 072          EDR TEMPX
414   06264  23 1 260          CLJ L-4,I
415                            ITR 31
415   06265      00000         ...
415   06266  06 0 072          SDR TEMPX
415   06267  01 0 030          DCR TABLE-31
415   06270  05 0 072          EDR TEMPX
415   06271  23 1 265          CLJ L-4,I
416                            ITR 30
416   06272      00000         ...
416   06273  06 0 072          SDR TEMPX
416   06274  01 0 031          DCR TABLE-30
416   06275  05 0 072          EDR TEMPX
416   06276  23 1 272          CLJ L-4,I
417                            ITR 29
417   06277      00000         ...
417   06300  06 0 072          SDR TEMPX
417   06301  01 0 032          DCR TABLE-29
417   06302  05 0 072          EDR TEMPX
417   06303  23 1 277          CLJ L-4,I
420                            ITR 28
420   06304      00000         ...
420   06305  06 0 072          SDR TEMPX
420   06306  01 0 033          DCR TABLE-28
420   06307  05 0 072          EDR TEMPX
420   06310  23 1 304          CLJ L-4,I
421                            ITR 27
421   06311      00000         ...
421   06312  06 0 072          SDR TEMPX
421   06313  01 0 034          DCR TABLE-27
421   06314  05 0 072          EDR TEMPX
421   06315  23 1 311          CLJ L-4,I
422                            ITR 26
422   06316      00000         ...
422   06317  06 0 072          SDR TEMPX
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
422   06320  01 0 035          DCR TABLE-26
422   06321  05 0 072          EDR TEMPX
422   06322  23 1 316          CLJ L-4,I
423                            ITR 25
423   06323     00000          ...
423   06324  06 0 072          SDR TEMPX
423   06325  01 0 036          DCR TABLE-25
423   06326  05 0 072          EDR TEMPX
423   06327  23 1 323          CLJ L-4,I
424                            ITR 24
424   06330     00000          ...
424   06331  06 0 072          SDR TEMPX
424   06332  01 0 037          DCR TABLE-24
424   06333  05 0 072          EDR TEMPX
424   06334  23 1 330          CLJ L-4,I
425                            ITR 23
425   06335     00000          ...
425   06336  06 0 072          SDR TEMPX
425   06337  01 0 040          DCR TABLE-23
425   06340  05 0 072          EDR TEMPX
425   06341  23 1 335          CLJ L-4,I
426                            ITR 22
426   06342     00000          ...
426   06343  06 0 072          SDR TEMPX
426   06344  01 0 041          DCR TABLE-22
426   06345  05 0 072          EDR TEMPX
426   06346  23 1 342          CLJ L-4,I
427                            ITR 21
427   06347     00000          ...
427   06350  06 0 072          SDR TEMPX
427   06351  01 0 042          DCR TABLE-21
427   06352  05 0 072          EDR TEMPX
427   06353  23 1 347          CLJ L-4,I
430                            ITR 20
430   06354     00000          ...
430   06355  06 0 072          SDR TEMPX
430   06356  01 0 043          DCR TABLE-20
430   06357  05 0 072          EDR TEMPX
430   06360  23 1 354          CLJ L-4,I
431                            ITR 19
```

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```
431   06361      00000          ...
431   06362   06 0 072          SDR TEMPX
431   06363   01 0 044          DCR TABLE-19
431   06364   05 0 072          EDR TEMPX
431   06365   23 1 361          CLJ L-4,1
432                             ITR 18
432   06366      00000          ...
432   06367   06 0 072          SDR TEMPX
432   06370   01 0 045          DCR TABLE-18
432   06371   05 0 072          EDR TEMPX
432   06372   23 1 366          CLJ L-4,1
433                             ITR 17
433   06373      00000          ...
433   06374   06 0 072          SDR TEMPX
433   06375   01 0 046          DCR TABLE-17
433   06376   05 0 072          EDR TEMPX
433   06377   23 1 373          CLJ L-4,1
434                             ITR 16
434   06400      00000          ...
434   06401   06 1 166  J       SDR TEMPX
434   06402   01 1 165  J       DCR TABLE-16
434   06403   05 1 166          EDR TEMPX
434   06404   23 1 000          CLJ L-4,1
435                             ITR 15
435   06405      00000          ...
435   06406   06 1 166          SDR TEMPX
435   06407   01 1 164  J       DCR TABLE-15
435   06410   05 1 166          EDR TEMPX
435   06411   23 1 005          CLJ L-4,1
436                             ITR 14
436   06412      00000          ...
436   06413   06 1 166          SDR TEMPX
436   06414   01 1 163  J       DCR TABLE-14
436   06415   05 1 166          EDR TEMPX
436   06416   23 1 012          CLJ L-4,1
437                             ITR 13
437   06417      00000          ...
437   06420   06 1 166          SDR TEMPX
437   06421   01 1 162  J       DCR TABLE-13
437   06422   05 1 166          EDR TEMPX
```

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```
437   06423  23 1 017          CLJ L-4,I
440                             ITR 12
440   06424      00000         ...
440   06425  06 1 166          SDR TEMPX
440   06426  01 1 161  J       DCR TABLE-12
440   06427  05 1 166          EDR TEMPX
440   06430  23 1 024          CLJ L-4,I
441                             ITR 11
441   06431      00000         ...
441   06432  06 1 166          SDR TEMPX
441   06433  01 1 160  J       DCR TABLE-11
441   06434  05 1 166          EDR TEMPX
441   06435  23 1 031          CLJ L-4,I
442                             ITR 10
442   06436      00000         ...
442   06437  06 1 166          SDR TEMPX
442   06440  01 1 157  J       DCR TABLE-10
442   06441  05 1 166          EDR TEMPX
442   06442  23 1 036          CLJ L-4,I
443                             ITR 9
443   06443      00000         ...
443   06444  06 1 166          SDR TEMPX
443   06445  01 1 156  J       DCR TABLE-9
443   06446  05 1 166          EDR TEMPX
443   06447  23 1 043          CLJ L-4,I
444                             ITR 8
444   06450      00000         ...
444   06451  06 1 166          SDR TEMPX
444   06452  01 1 155  J       DCR TABLE-8
444   06453  05 1 166          EDR TEMPX
444   06454  23 1 050          CLJ L-4,I
445                             ITR 7
445   06455      00000         ...
445   06456  06 1 166          SDR TEMPX
445   06457  01 1 154  J       DCR TABLE-7
445   06460  05 1 166          EDR TEMPX
445   06461  23 1 055          CLJ L-4,I
446                             ITR 6
446   06462      00000         ...
446   06463  06 1 166          SDR TEMPX
```

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```
446   06464  01 1 153  J        DCR TABLE-6
446   06465  05 1 166           EDR TEMPX
446   06466  23 1 062           CLJ L-4,I
447                             ITR 5
447   06467     00000           ...
447   06470  06 1 166           SDR TEMPX
447   06471  01 1 152  J        DCR TABLE-5
447   06472  05 1 166           EDR TEMPX
447   06473  23 1 067           CLJ L-4,I
450                             ITR 4
450   06474     00000           ...
450   06475  06 1 166           SDR TEMPX
450   06476  01 1 151  J        DCR TABLE-4
450   06477  05 1 166           EDR TEMPX
450   06500  23 1 074           CLJ L-4,I
451                             ITR 3
451   06501     00000           ...
451   06502  06 1 166           SDR TEMPX
451   06503  01 1 150  J        DCR TABLE-3
451   06504  05 1 166           EDR TEMPX
451   06505  23 1 101           CLJ L-4,I
452                             ITR 2
452   06506     00000           ...
452   06507  06 1 166           SDR TEMPX
452   06510  01 1 147  J        DCR TABLE-2
452   06511  05 1 166           EDR TEMPX
452   06512  23 1 106           CLJ L-4,I
453                             ITR 1
453   06513     00000           ...
453   06514  06 1 166           SDR TEMPX
453   06515  01 1 146  J        DCR TABLE-1
453   06516  05 1 166           EDR TEMPX
453   06517  23 1 113           CLJ L-4,I
454                    LASTAD   ITR 0
454   06520     00000           ...
454   06521  06 1 166           SDR TEMPX
454   06522  01 1 145  J        DCR TABLE-0
454   06523  05 1 166           EDR TEMPX
454   06524  23 1 120           CLJ L-4,I
```

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```
455                                        EJE
456    06525      00000    CNVTA  ...
457    06526   37 1 144    J       STL SAVE
460    06527   12 0 143    J      8AND 7)
461    06530   37 1 142    J       STL TEMP
462    06531   32 1 144            ENL SAVE
463    06532   12 0 141    J      8AND 70)
464    06533   14 1 140    J       LSH ACC
465    06534   14 1 140            LSH ACC
466    06535   14 1 140            LSH ACC
467    06536   10 1 142            ADD TEMP
470    06537   24 1 125            RTN
       06540      00101            WRD
       06541      00070            WRD
       06542      05655            WRD
       06543      00007            WRD
       06544      07354            WRD
       06545      06067            WRD
       06546      06066            WRD
       06547      06065            WRD
       06550      06064            WRD
       06551      06063            WRD
       06552      06062            WRD
       06553      06061            WRD
       06554      06060            WRD
       06555      06057            WRD
       06556      06056            WRD
       06557      06055            WRD
       06560      06054            WRD
       06561      06053            WRD
       06562      06052            WRD
       06563      06051            WRD
       06564      06050            WRD
       06565      06047            WRD
       06566      06072            WRD
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
471                 07000           8ORG 7000
472     07000       00000   OTRCD   ...         PRINT RECORD TERMINATED BY 77 CODE
473     07001   32  0 000           ENL OTRCD
474     07002   10  0 342   J       ADD 1)
475     07003   37  0 000           STL OTRCD
476     07004   32  1 000           ENL OTRCD.I
477     07005   37  0 035           STL OTADS
500     07006   03  0 036           SMB OTIND
501     07007   32  1 035   OTLOP   ENL OTADS.I
502     07010   16  0 036           RSH OTIND
503     07011   27  0 017           PJP SECND
504     07012   16  1 341   J       RSH ACC
505     07013   16  1 341           RSH ACC
506     07014   16  1 341           RSH ACC
507     07015   16  1 341           RSH ACC
510     07016   16  1 341           RSH ACC
511     07017   16  1 341           RSH ACC
512     07020   12  0 341   JSECND  8AND 77)
513     07021   11  0 340           8SUB 77)
514     07022   20  1 000           ZJP OTRCD.I
515     07023   10  0 340           8ADD 77)
516     07024   27  0 025           PJP L+2
517     07025   32  0 337   J       ENL 0)
520     07026   36  0 037           RJP OT1
521     07027   32  0 035           ENL OTADS
522     07030   10  0 342           ADD 1)
523     07031   16  0 036           RSH OTIND
524     07032   27  0 004           PJP OTLOP-2
525     07033   02  0 036           CMB OTIND
526     07034   24  0 006           JMP OTLOP
527     07035       00000   OTADS   OCT
530     07036       00000   OTIND   OCT
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
531                                     EJE
532   07037       00000   OT1           ...
533   07040   10  0 336   J             ADD TBL)
534   07041   37  0 061                 STL ADS
535   07042   32  1 061                 ENL ADS,I
536   07043   34  0 000   OUT           OUT
537   07044   01  1 337                 DCR PC
540   07045       00000   ASRIN         ...
541   07046   32  0 061                 ENL ADS
542   07047   20  0 054                 ZJP IGNORA
543   07050   11  0 335   J             8SUB TBL+14)
544   07051   20  0 055                 ZJP LFD
545   07052   32  0 337                 ENL 0)
546   07053   37  0 061                 STL ADS
547   07054   23  1 037                 CLJ OT1,I
550   07055   23  1 045   IGNORA        CLJ ASRIN,I
551   07056   32  0 334   JLFD          8ENL 30500)
552   07057   37  0 061                 STL ADS
553   07060   23  0 042                 CLJ OT1+4
554   07061       00000   ADS           OCT
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
555                                 EJE
556                          COD    VFD 1,8,5
557                          CDE    MAC A,B,C,D,E,F,G,H
560                                 COD 1,A,
561                                 COD 1,B,
562                                 COD 1,C,
563                                 COD 1,D,
564                                 COD 1,E,
565                                 COD 1,F,
566                                 COD 1,G,
567                                 COD 1,H,
570                                 TER
571                          TBL    8CDE 260,261,262,263,264,265,266,267
571    07062      33000             COD 1,260,
571    07063      33040             COD 1,261,
571    07064      33100             COD 1,262,
571    07065      33140             COD 1,263,
571    07066      33200             COD 1,264,
571    07067      33240             COD 1,265,
571    07070      33300             COD 1,266,
571    07071      33340             COD 1,267,
572                                 8CDE 270,271,336,275,215,272,276,241
572    07072      33400             COD 1,270,
572    07073      33440             COD 1,271,
572    07074      33700             COD 1,336,
572    07075      33640             COD 1,275,
572    07076      33640             COD 1,215,
572    07077      33500             COD 1,272,
572    07100      33700             COD 1,276,
572    07101      32040             COD 1,241,
573                                 8CDE 253,301,302,303,304,305,306,307
573    07102      32540             COD 1,253,
573    07103      34040             COD 1,301,
573    07104      34100             COD 1,302,
573    07105      34140             COD 1,303,
573    07106      34200             COD 1,304,
573    07107      34240             COD 1,305,
573    07110      34300             COD 1,306,
573    07111      34340             COD 1,307,
574                                 8CDE 310,311,277,256,251,333,274,243
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
574    07112     34400          COD 1.310.
574    07113     34440          COD 1.311.
574    07114     33740          COD 1.277.
574    07115     32700          COD 1.256.
574    07116     32440          COD 1.251.
574    07117     35540          COD 1.333.
574    07120     33600          COD 1.274.
574    07121     32140          COD 1.243.
575                             8CDE 255,312,313,314,315,316,317,320
575    07122     32640          COD 1.255.
575    07123     34500          COD 1.312.
575    07124     34540          COD 1.313.
575    07125     34600          COD 1.314.
575    07126     34640          COD 1.315.
575    07127     34700          COD 1.316.
575    07130     34740          COD 1.317.
575    07131     35000          COD 1.320.
576                             8CDE 321,322,337,244,252,335,273,300
576    07132     35040          COD 1.321.
576    07133     35100          COD 1.322.
576    07134     35740          COD 1.337.
576    07135     32200          COD 1.244.
576    07136     32500          COD 1.252.
576    07137     35640          COD 1.335.
576    07140     33540          COD 1.273.
576    07141     34000          COD 1.300.
577                             8CDE 240,257,323,324,325,326,327,330
577    07142     32000          COD 1.240.
577    07143     32740          COD 1.257.
577    07144     35140          COD 1.323.
577    07145     35200          COD 1.324.
577    07146     35240          COD 1.325.
577    07147     35300          COD 1.326.
577    07150     35340          COD 1.327.
577    07151     35400          COD 1.330.
600                             8CDE 331,332,245,254,250,246,334,212
600    07152     35440          COD 1.331.
600    07153     35500          COD 1.332.
600    07154     32240          COD 1.245.
600    07155     32600          COD 1.254.
```

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600	07156	32400	COD 1,250.
600	07157	32300	COD 1,246.
600	07160	35500	COD 1,334.
600	07161	30600	COD 1,212.

PROJECT NO. 530853 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
601                                    EJE
602                                        ROUTINE TO SIMULATE ACH WITHOUT EXECUTIVES.
603   07162      00000    ACHR    ...
604   07163   37 0 220            STL DATA
605   07164   32 0 162            ENL ACHR
606   07165   10 0 342            ADD 1)
607   07166   37 0 162            STL ACHR
610   07167   32 1 162            ENL ACHR,I
611   07170   37 0 221            STL REG
612   07171   10 0 333  J         ADD CWDS)
613   07172   37 0 222            STL CWD
614   07173   32 1 222            ENL CWD,I
615   07174   37 0 223            STL CHWD
616   07175   32 0 221            ENL REG
617   07176   10 0 332  J         ADD BUF)
620   07177   37 0 222            STL CWD
621   07200   32 0 331  J         ENL 2)
622   07201   37 0 224            STL IFLG
623   07202   32 0 220            ENL DATA
624   07203   37 1 222            STL CWD,I
625   07204   34 1 223   OUTC     OUT CHWD,I
626   07205   01 1 337            DCR PC
627   07206      00000   INTCCO  ...
630   07207   32 0 224            ENL IFLG
631   07210   20 0 224            ZJP STOP
632   07211   01 0 224            DCR IFLG
633   07212   20 0 216            ZJP L+5
634   07213   01 0 223            DCR CHWD
635   07214   32 1 222            ENL CWD,I
636   07215   13 0 330  J        8EOR 37777)
637   07216   23 0 203             CLJ OUTC
640   07217   23 1 162             CLJ ACHR,I
641   07220      00000   DATA    OCT
642   07221      00000   REG     OCT
643   07222      00000   CWD     OCT
644   07223      00000   CHWD    OCT
645   07224      00000   IFLG    OCT
646   07225   00 0 077   STOP    8STP 77
647                      BUF     RPT 8
650   07226      00000           OCT
```

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07227	00000
07230	00000
07231	00000
07232	00000
07233	00000
07234	00000
07235	00000

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
651                                     EJE
652                                         ROUTINES FOR SBO AND SBZ WITHOUT EXECUTIVES.
653   07236       00000   SBO       ...
654   07237  32 0 330                ENL -)
655   07240  37 0 305                STL MASK
656   07241  32 0 236                ENL SBO
657   07242  24 0 246                JMP SBZ+4
660   07243       00000   SBZ       ...
661   07244  32 0 337                ENL 0)
662   07245  37 0 305                STL MASK
663   07246  32 0 243                ENL SBZ
664   07247  10 0 342                ADD 1)
665   07250  37 0 243                STL SBZ
666   07251  32 1 243                ENL SBZ,I
667   07252  12 0 327  J             BAND 17)
670   07253  37 0 306                STL BIT
671   07254  32 1 243                ENL SBZ,I
672   07255  16 1 341                RSH ACC
673   07256  16 1 341                RSH ACC
674   07257  16 1 341                RSH ACC
675   07260  16 1 341                RSH ACC
676   07261  37 0 277                STL ACWC+1
677   07262  10 0 332                ADD BUF)
700   07263  37 0 307                STL INIT
701   07264  32 0 306                ENL BIT
702   07265  10 0 326  J             ADD MAST)
703   07266  37 0 306                STL BIT
704   07267  32 1 306                ENL BIT,I
705   07270  37 0 306                STL BIT
706   07271  32 0 305                ENL MASK
707   07272  27 0 300                PJP SBZX
710   07273  13 0 306                EOR BIT
711   07274  12 1 307                AND INIT,I
712   07275  13 0 306                EOR BIT
713   07276  36 0 162   ACWC        RJP ACWR
714   07277       00000               OCT
715   07300  24 1 243                HTN
716   07301  32 0 330   SBZX        ENL -)
717   07302  13 0 306                EOR BIT
720   07303  12 1 307                AND INIT,I
```

```
      721   07304  24 0 275          JMP ACWC
      722   07305      00000   MASK   OCT
      723   07306      00000   BIT    OCT
      724   07307      00000   INIT   OCT
      725   07310      00001   MAST   OCT 1,2,4,10,20,40,100,200,400,1000,2000,4000,10000,20000
            07311      00002
            07312      00004
            07313      00010
            07314      00020
            07315      00040
            07316      00100
            07317      00200
            07320      00400
            07321      01000
            07322      02000
            07323      04000
            07324      10000
            07325      20000
      726                          GEN
            07326      07310      WRD
            07327      00017      WRD
            07330      37777      WRD
            07331      00002      WRD
            07332      07226      WRD
            07333      05405      WRD
            07334      30500      WRD
            07335      07076      WRD
            07336      07062      WRD
            07337      00000      WRD
            07340      00077      WRD
            07341      00101      WRD
            07342      00001      WRD
```

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

```
727   07343   00000   CTR     OCT
730   07344   00000   FLAG    OCT
731   07345   00000   INDEXX  OCT
732   07346   00000   SSX     OCT                  FIRST CONTACT
733   07347   00000   SS0     OCT 0
734   07350   00001   SS1     OCT 1
735   07351   00002   SS2     OCT 2
736   07352   00015   SS15    OCT 15
737   07353   00017   SS17    OCT 17
740   07354   00000   SAVE    OCT
741   07355   00000   LAST    OCT
742   07356   02323   FORMAT  BCD 05CCOINT IS      X
      07357   04631
      07360   04563
      07361   06031
      07362   06260
743   07363   00000   INTW    OCT
744   07364   06060           OCT 6060
745   07365   06230           BCD 05SHOULD BE      X
      07366   04664
      07367   04324
      07370   06022
      07371   02560
746   07372   00000   INTR    OCT .1477
      07373   01477
747   07374   02323   COMPLT  BCD 11CCO-PRI TEST COMPLETE     X
      07375   04640
      07376   04751
      07377   03160
      07400   06325
      07401   06263
      07402   06023
      07403   04644
      07404   04743
      07405   02563
      07406   02560
750   07407   01477           OCT 1477
```

```
      751                                    EJE
      752   07410      00000   ICRCON ...
      753   07411   32 1 051  J        ENL CONTAT
      754   07412   10 1 050  J        ADD SS1
      755   07413   37 1 051           STL CONTAT
      756   07414   12 1 047  J        AND SS17
      757   07415   11 1 046  J        SUB SS15
      760   07416   27 0 017           PJP ICRWRD
      761   07417   24 1 010           RTN
      762   07420   32 1 045  JICRWRD  ENL SS2
      763   07421   10 1 051           ADD CONTAT
      764   07422   37 1 051           STL CONTAT
      765   07423   24 1 010           RTN
      766   07424      00000   ERR2    ...
      767   07425   32 1 044  J        ENL TT
      770   07426   11 1 043  J        SUB ITABX
      771   07427   36 1 042  J        RJP CNVTA
      772   07430   37 1 041  J        STL INT+
      773   07431   32 1 040  J        ENL SS0
      774   07432   37 1 037  J        STL INTR
      775   07433   36 1 036  J        RJP OTRCD
      776   07434      07356           OCT FORMAT
      777   07435   24 1 024           RTN
            07436      07000           WRD
            07437      07372           WRD
            07440      07347           WRD
            07441      07363           WRD
            07442      06525           WRD
            07443      05657           WRD
            07444      06071           WRD
            07445      07351           WRD
            07446      07352           WRD
            07447      07353           WRD
            07450      07350           WRD
            07451      05656           WRD
     1000              00000           END
```

DATE 4/27/65, TIME 2/32/31 P.M.

PROJECT NO. 530053 PROGRAMMER J.E. PHILLIPPI TAPE NUMBER 512606

STARTED 4/27/65, 2/30/00 P.M.
COMPLETED 4/27/65, 2/32/31 P.M.
NUMBER OF INPUT RECORDS 512.
NUMBER OF OUTPUT RECORDS 1046.
NUMBER OF BINARY RECORDS 925.

P-50 CCI TEST WITHOUT CABLES D37A

I. Purpose of Test

To perform a simple "go-no go" test on the multiplexed and/or non-multiplexed contact closure input registers.

II. Description of Test

The program will test up to fourteen multiplexed CCI registers and up to fourteen non-multiplexed CCI registers per run.

Non-multiplexed CCI registers are tested if NØNMUL is not zero; multiplexed CCI registers are tested if MLTPLX is not zero. (NØNMUL and MLTPLX are input parameters.)

When a register is read, if the contents are zero, the test continues. If the contents are nonzero, the bit pattern output to select the register (multiplexed) or the input channel (non-multiplexed) and the reading are printed in binary; the test continues.

III. Description of Operation

A. Read in the binary tape of the test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (76028, 176028, 276028, or 376028); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.

B. Enter the test parameters

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the S-Register with the parameter location.
3. Using the probe, load the X-Register with the parameter constant; depress the Start button.
4. Repeat steps 2 and 3 until all parameters needed have been entered.

Location	Parameter	Description
200_8	NØNMUL	Number of non-multiplexed CCI registers to be tested ($0-14_{10}$).
201_8	MLTPLX	Number of multiplexed CCI registers to be tested ($0-14_{10}$).
202_8	One bit set	Bit to output to select register 16_8
203_8		Bit to output to select register 15_8
.		.
.		.
.		.
.		.
216_8		Bit to output to select register 2_8
217_8		Bit to output to select register 1_8
220_8	Input Channel	Input channel, non-multiplexed register 16_8
221_8		Input channel, non-multiplexed register 15_8
.		.
.		.
.		.
234_8		Input channel, non-multiplexed register 2
235_8		Input channel, non-multiplexed register 1
265_8	340XX	XX is multiplexed CCI address select channel
270_8	300XX	XX is multiplexed CCI input channel
of CCI input request interrupt	24276_8	Transfer for multiplexed CCI input request interrupt
of CCI cycle complete interrupt	24271_8	Transfer for multiplexed CCI cycle complete interrupt
of logger interrupt	24734_8	Transfer for ASR or Selectric completion interrupt
335_8	340XX	XX is ASR or Selectric output channel

(Load following only if Selectric logger is used; do not load if ASR set is used for printout.)

Location	Parameter	Description
337_8	37410_8	Selectric code for "1"
340_8	05400_8	Used to get code for "0"
341_8	00110_8	Selectric code for space
342_8	00050_8	Selectric code for carriage return
343_8	00110_8	Selectric code for space

C. Start the Test

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the test (237_8); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Depress the Start button.

D. The test runs continuously. When a register is read and the contents are not zero, the following printout occurs:

xxxxxxxxxxxxxx yyyyyyyyyyyyyy

where x...x is the bit pattern output (for a multiplexed CCI register) or x...x is the input channel (for a non-multiplexed CCI register) and y...y is the register contents.

IV. Storage

Number of locations used: 161_8 (200_8-360_8)

```
                                        P-50 CCI TEST WITHOUT CABLES                    P-50 D37A
                                          TESTS MULTIPLEXED AND/OR NON-MULTIPLEXED CCI
            00200           BOMG 200

00200       00000   NONMUL  DEC         NUMBER NON-MULTIPLEXED CCI REGISTERS TO BE TESTED
                                        UP TO 14 NON MULTIPLEXED REGISTERS PER RUN CAN BE
                                        TESTED

00201       00000   MLTPLX  DEC        NUMBER MULTIPLEXED CCI REGISTERS TO BE TESTED
                                        UP TO 14 MULTIPLEXED REGISTERS PER RUN CAN BE TESTED
                            HPT 14
00202       00000           OCT
00203       00000
00204       00000
00205       00000
00206       00000
00207       00000
00210       00000
00211       00000
00212       00000
00213       00000
00214       00000
00215       00000
00216       00000
00217       00000
            00217   MULTAB  SYN L-1     THIS LOCATION CONTAINS THE BIT NUMBER OF THE
                                        FIRST MULTIPLEXED CCI REGISTER TO BE READ.  BIT
                                        NUMBERS FOR SUCCEEDING MULTIPLEXED CCI REGISTERS
                                        ARE PLACED IN SEQUENTIALLY DESCENDING LOCATIONS.
                                        ALL MULTIPLEXED REGISTERS MUST BE ON THE SAME CHANNEL

                            HPT 14
00220       00000           OCT
00221       00000
00222       00000
00223       00000
00224       00000
00225       00000
00226       00000
00227       00000
```

P-50 MULTIPLEXED AND NON-MULTIPLEXED CCI TEST WITHOUT CABLES

```
            00230     00000
            00231     00000
            00232     00000
            00233     00000
            00234     00000
            00235     00000
      25              00235   NONTAB SYN L-1    THIS LOCATION CONTAINS THE INPUT CHANNEL NUMBER OF THE
      26                                        FIRST NON-MULTIPLEXED CCI REGISTER TO BE TESTED.
      27                                        CHANNEL NUMBERS FOR SUCCEEDING NON-MULTIPLEXED
      30                                        CCI REGISTERS ARE PLACED IN SEQUENTIALLY DESCENDING
      31                                        LOCATIONS.
```

P-50 MULTIPLEXED AND NON-MULTIPLEXED CCI TEST WITHOUT CABLES

```
32                                      EJE
33
34    00236   32 0 235    INS1    ENL NONTAB
35    00237   30 0 000    BLKINT  INT **
36
37    00240   32 0 200    NONSTR  ENL NONMUL        NON-MULTIPLEXED START LOCATION
40    00241   20 0 256            ZJP MULSTR
41    00242   37 0 353            STL NONCNT
42    00243   32 0 235    RESTR1  ENL NONTAB
43    00244   01 0 243            DCR L-1
44    00245   37 0 356            STL PRTLOC
45    00246   10 0 237            ADD BLKINT
46    00247   37 0 250            STL L+1
47    00250   30 0 000            INT **      ** IS NON-MULTIPLEXED INPUT CHANNEL
50    00251   20 0 252            ZJP N
51    00252   36 0 303            RJP PRINT
52    00253   01 0 353    N       DCR NONCNT
53    00254   27 0 242            PJP RESTR1
54    00255   32 0 236            ENL INS1
55    00256   37 0 243            STL RESTR1
56
```

P-50 MULTIPLEXED AND NON-MULTIPLEXED CCI TEST WITHOUT CABLES

```
 57                                    EJE
 60                                        BEGINNING OF MULTIPLEXED CCI TEST.
 61
 62   00257  32 0 201   MULSTR ENL MLTPLX        START OF MULTIPLEX TEST
 63   00260  20 0 237          ZJP NONSTR
 64   00261  37 0 354          STL MLTCNT
 65   00262  32 0 217   RESTR2 ENL MULTAB
 66   00263  01 0 262          DCR L-1
 67   00264  37 0 356          STL PRTLUC
 70   00265  34 0 000          OUT **       ** IS MULTIPLEX ADDRESS SELECT CHANNEL
 71   00266  23 0 266   INWATE CLJ L+1
 72   00267  01 0 000          DCR PC
 73   00270  30 0 000   OUTINT INT **       ** IS MULTIPLEXED INPUT CHANNEL NUMBER
 74                                        OUTINT IS ADDRESS COMPLETE INTERRUPT ENTRY
 75   00271  24 0 265          JMP INWATE
 76   00272  37 0 355   ININT  STL PRTLUC-1
 77   00273  20 0 274          ZJP M
100   00274  36 0 303          NJP PRINT
101   00275  01 0 354   M      DCR MLTCNT
102   00276  27 0 261          PJP RESTR2
103   00277  32 0 302          ENL INS2
104   00300  37 0 262          STL RESTR2
105   00301  24 0 237          JMP NONSTR
106   00302  32 0 217   INS2   ENL MULTAB
```

P-50 MULTIPLEXED AND NON-MULTIPLEXED CCI TEST WITHOUT CABLES

```
107                                     EJE
110                                         PRINT SUBROUTINE
111   00303       00000   PRINT     ...
112   00304  37 0 355                STL PRTLOC-1
113   00305  32 0 344                ENL TWO
114   00306  37 0 357                STL CNT1
115   00307  32 0 345                ENL IN2
116   00310  37 0 314                STL R2
117   00311  32 0 346   L2           ENL FORTEN
120   00312  37 0 360                STL CNT2
121   00313  32 0 337   L1           ENL ONECHR
122   00314  14 0 356   R2           LSH PRTLOC
123   00315  25 0 316                CJP L+2
124   00316  11 0 340                SUB FORTY
125   00317  36 0 334                RJP OUT
126   00320  01 0 360                DCR CNT2
127   00321  27 0 312                PJP L1
130   00322  01 0 314                DCR R2
131   00323  32 0 343                ENL SPACE
132   00324  36 0 334                RJP OUT
133   00325  01 0 357                DCR CNT1
134   00326  27 0 310                PJP L2
135   00327  32 0 342                ENL CARRGE
136   00330  36 0 334                RJP OUT
137   00331  32 0 341                ENL LF
140   00332  36 0 334                RJP OUT
141   00333  24 1 303                RTN
142   00334       00000   OUT       ...
143   00335  34 0 000                OUT **          ASR OR LOGGER CHANNEL NO,
144   00336  24 0 265                JMP INWATE
145   00337       13040   ONECHR    OCT 13040       FOR SELECTRIC OUTPUT USE OCT 37410
146   00340       00040   FORTY     OCT 40          FOR SELECTRIC OUTPUT USE OCT 5400
147   00341       10500   LF        OCT 10500       FOR SELECTRIC OUTPUT USE OCT 110
150   00342       10640   CARRGE    OCT 10640       FOR SELECTRIC OUTPUT USE OCT 50
151   00343       12000   SPACE     OCT 12000       FOR SELECTRIC OUTPUT USE OCT 110
152   00344       00002   TWO       OCT 2
153   00345  14 0 356     IN2       LSH PRTLOC
154   00346       00016   FORTEN    DEC 14
155               00353   NONCNT    SYN L+4
156               00354   MLTCNT    SYN NONCNT+1
```

```
      157              00356   PRTLOC SYN MLTCNT+2
      160              00357   CNT1   SYN PRTLOC+1
      161              00360   CNT2   SYN CNT1+1
      162              00000          END
```

INTERRUPT TEST WITHOUT CABLES D38A

I. Purpose of Test

To perform a simple "go-no go" test on one to sixteen interrupts.

II. Description of Test

Up to sixteen interrupts may be tested by storing transfer commands in sixteen interrupt locations.

The test prints the relative interrupt number in binary when an interrupt occurs. The printout format is "000000000XXXXX", where XXXXX is 00000_2 - 10000_2.

III. Description of Operation

A. Read in the binary tape of the test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the binary loader (7602_8, 17602_8, 27602_8, or 37602_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Place the binary tape under the tape reader.

5. Turn the reader on.

6. Depress the Start button.

B. Enter the test parameters

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the S-Register with the parameter location.

3. Using the probe, load the X-Register with the parameter constant; depress the Start button.

4. Repeat steps 2 and 3 until all parameters needed have been entered.

Location	Parameter	Description
of 1st interrupt	36 257	Transfer for 1st interrupt
of 2nd interrupt	36 264	Transfer for 2nd interrupt
of 3rd interrupt	36 271	Transfer for 3rd interrupt
of 4th interrupt	36 276	Transfer for 4th interrupt
of 5th interrupt	36 303	Transfer for 5th interrupt
of 6th interrupt	36 310	Transfer for 6th interrupt
of 7th interrupt	36 315	Transfer for 7th interrupt
of 8th interrupt	36 322	Transfer for 8th interrupt
of 9th interrupt	36 327	Transfer for 9th interrupt
of 10th interrupt	36 334	Transfer for 10th interrupt
of 11th interrupt	36 341	Transfer for 11th interrupt
of 12th interrupt	36 346	Transfer for 12th interrupt

Location	Parameter	Description
of 13th interrupt	36 353	Transfer for 13th interrupt
of 14th interrupt	36 360	Transfer for 14th interrupt
of 15th interrupt	36 365	Transfer for 15th interrupt
of 16th interrupt	36 372	Transfer for 16th interrupt
of logger interrupt	24 637	Transfer for ASR or Selectric logger
240_8	34 0XX	ASR or Selectric output channel

(Load following only if Selectric logger is used; do not load if ASR set is used for printout.)

244_8	37410_8	Output Code for "1"
245_8	05400_8	Output Code for "0"
246_8	00050_8	Output Code for carriage return
247_8	00110_8	Output Code for space
250_8	00110_8	Output Code for space

C. Start the test

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the test (203_8); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Depress the Start button.

D. The test runs continuously, printing the relative number ($1\text{-}16_{10}$) of any interrupt which occurs.

IV. Storage

Number of locations used: 177_8 (200_8 - 376_8)

P-50 INTERRUPT TEST WITHOUT CABLES

```
 1                                          P-50 INTERRUPT TEST WITHOUT CABLES                P-50 D38A
 2            00200              BORG 200
 3
 4   00200    00000   SAVE   ...          THIS ROUTINE IS ENTERED WITH A NUMBER IDENTIFYING THE
 5                                         INTERRUPT IN THE ACCUMULATOR.THIS NUMBER IS PRINTED
 6                                         ON EITHER ASR OR SELECTRIC TYPER.
 7   00201  01 0 243          DCR MARKER
10   00202  37 1 243          STL MARKER,I
11   00203  23 1 200          CLJ SAVE,I
12   00204  32 0 256 JSTART   ENL TABLE)
13   00205  11 0 243          SUB MARKER
14   00206  20 0 235          ZJP DONE
15   00207  32 1 243          ENL MARKER,I
16   00210  27 0 214          PJP ENDONE
17   00211  32 0 243          ENL MARKER
20   00212  10 0 255 J        ADD 1)
21   00213  37 0 243          STL MARKER
22   00214  22 0 203          SLJ START
23   00215  37 0 253 ENDONE   STL TABLE
24   00216  03 1 243          SMB MARKER,I
25   00217  32 0 254          ENL 14
26   00220  37 0 377          STL CNT
27   00221  32 0 244 L1       ENL ONECHR
30   00222  14 0 253          LSH TABLE
31   00223  25 0 224          CJP L+2
32   00224  11 0 245          SUB ZERCHR
33   00225  36 0 237          RJP OUT
34   00226  01 0 377          DCR CNT
35   00227  27 0 220          PJP L1
36   00230  32 0 246          ENL CARRGE
37   00231  36 0 237          RJP OUT
40   00232  32 0 250          ENL LF
41   00233  36 0 237          RJP OUT
42   00234  23 0 234 DONE     CLJ L+1
43   00235  32 0 256          ENL TABLE)
44   00236  22 0 203          SLJ START
45   00237    00000 OUT      ...
46   00240  34 0 000          OUT **              TYPER OUTPUT CHANNEL
47   00241  23 0 241          CLJ L+1
50   00242  01 0 000          DCR PC
```

```
51    00243    00253   MARKER OCT TABLE
52    00244    13040   ONECHR OCT 13040        FOR SELECTRIC OUTPUT USE OCT 37410
53    00245    00040   ZERCHR OCT 40           FOR SELECTRIC OUTPUT USE OCT 5400
54    00246    10640   CARRGE OCT 10640        FOR SELECTRIC OUTPUT USE OCT 50
55    00247    12000   SPACE  OCT 12000        FOR SELECTRIC OUTPUT USE OCT 110
56    00250    10500   LF     OCT 10500        FOR SELECTRIC OUTPUT USE OCT 110
57    00251    20000          OCT 20000
60    00252    20000          OCT 20000
61    00253    20000   TABLE  OCT 20000
62             00377   CNT    BEQU 377
63                             GEN
      00254    00016          WRD
      00255    00001          WRD
      00256    00253          WRD
```

```
 64
 65                                                  FIRST INTERRUPT SUBROUTINE
 66   00257      00000   1INT    ...
 67   00260  32  0 263          ENL ONE
 70   00261  36  0 200          RJP SAVE
 71   00262  24  1 257          RTN
 72   00263      00001   ONE     DEC 1               INTERRUPT NUMBER
 73
 74                                                  SECOND INTERRUPT SUBROUTINE
 75   00264      00000   2INT    ...
 76   00265  32  0 270          ENL TWO
 77   00266  36  0 200          RJP SAVE
100   00267  24  1 264          RTN
101   00270      00002   TWO     DEC 2               INTERRUPT NUMBER
102
103                                                  THIRD INTERRUPT  SUBROUTINE
104   00271      00000   3INT    ...
105   00272  32  0 275          ENL THREE
106   00273  36  0 200          RJP SAVE
107   00274  24  1 271          RTN
110   00275      00003   THREE   DEC 3               INTERRUPT NUMBER
111
112                                                  FOURTH INTERRUPT SUBROUTINE
113   00276      00000   4INT    ...
114   00277  32  0 302          ENL FOUR
115   00300  36  0 200          RJP SAVE
116   00301  24  1 276          RTN
117   00302      00004   FOUR    DEC 4               INTERRUPT NUMBER
120
121                                                  FIFTH INTERRUPT SUBROUTINE
122   00303      00000   5INT    ...
123   00304  32  0 307          ENL FIVE
124   00305  36  0 200          RJP SAVE
125   00306  24  1 303          RTN
126   00307      00005   FIVE    DEC 5               INTERRUPT NUMBER
127
130                                                  SIXTH INTERRUPT SUBROUTINE
131   00310      00000   6INT    ...
132   00311  32  0 314          ENL SIX
133   00312  36  0 200          RJP SAVE
```

P-50 INTERRUPT TEST WITHOUT CABLES

```
134   00313  24 1 310          RTN
135   00314     00006   SIX     DEC 6       INTERRUPT NUMBER
136
137                             SEVENTH INTERRUPT SUBROUTINE
140   00315     00000   7INT    ...
141   00316  32 0 321          ENL SEVEN
142   00317  36 0 200          RJP SAVE
143   00320  24 1 315          RTN
144   00321     00007   SEVEN   DEC 7       INTERRUPT NUMBER
145
146                             EIGHTH INTERRUPT SUBROUTINE
147   00322     00000   8INT    ...
150   00323  32 0 326          ENL EIGHT
151   00324  36 0 200          RJP SAVE
152   00325  24 1 322          RTN
153   00326     00010   EIGHT   DEC 8       INTERRUPT NUMBER
154
155                             NINTH INTERRUPT SUBROUTINE
156   00327     00000   9INT    ...
157   00330  32 0 333          ENL NINE
160   00331  36 0 200          RJP SAVE
161   00332  24 1 327          RTN
162   00333     00011   NINE    DEC 9       INTERRUPT NUMBER
163
164                             TENTH INTERRUPT SUBROUTINE
165   00334     00000   10INT   ...
166   00335  32 0 340          ENL TEN
167   00336  36 0 200          RJP SAVE
170   00337  24 1 334          RTN
171   00340     00012   TEN     DEC 10      INTERRUPT NUMBER
172
173                             ELEVENTH INTERRUPT SUBROUTINE
174   00341     00000   11INT   ...
175   00342  32 0 345          ENL ELEVEN
176   00343  36 0 200          RJP SAVE
177   00344  24 1 341          RTN
200   00345     00013   ELEVEN  DEC 11      INTERRUPT NUMBER
201
202                             TWELFTH INTERRUPT SUBROUTINE
203   00346     00000   12INT   ...
```

P-50 INTERRUPT TEST WITHOUT CABLES

```
204   00347  32 0 352          ENL TWELVE
205   00350  36 0 200          RJP SAVE
206   00351  24 1 346          RTN
207   00352     00014  TWELVE  DEC 12      INTERRUPT NUMBER
210
211                             THIRTEENTH INTERRUPT SUBROUTINE
212   00353     00000  13INT   ...
213   00354  32 0 357          ENL THRTEN
214   00355  36 0 200          RJP SAVE
215   00356  24 1 353          RTN
216   00357     00015  THRTEN  DEC 13      INTERRUPT NUMBER
217
220                             FOURTEENTH INTERRUPT SUBROUTINE
221   00360     00000  14INT   ...
222   00361  32 0 364          ENL FORTEN
223   00362  36 0 200          RJP SAVE
224   00363  24 1 360          RTN
225   00364     00016  FORTEN  DEC 14      INTERRUPT NUMBER
226
227                             FIFTEENTH INTERRUPT SUBROUTINE
230   00365     00000  15INT   ...
231   00366  32 0 371          ENL FIFTEN
232   00367  36 0 200          RJP SAVE
233   00370  24 1 365          RTN
234   00371     00017  FIFTEN  DEC 15      INTERRUPT NUMBER
235
236                             SIXTEENTH INTERRUPT SUBROUTINE
237   00372     00000  16INT   ...
240   00373  32 0 376          ENL SIXTEN
241   00374  36 0 200          RJP SAVE
242   00375  24 1 372          RTN
243   00376     00020  SIXTEN  DEC 16      INTERRUPT NUMBER
244               00000          END
```

P-50 CCØ TEST WITHOUT CABLES D39A

I. Purpose of Test

To perform a simple "go-no go" test on one to sixty-three CCØ registers.

II. Description of Test

All contacts are set to one; then, the program delays one second, and all contacts are set to zero. After another delay of one second the cycle is repeated.

Contacts are set to one by an output of 37777_8 on each multiplexer address with set channel. Contacts are set to zero by an output of 37777_8 on each multiplexer address with reset channel. Time delays are program loops.

III. Description of Operation

A. Read in the binary tape of the test using the bootstrapped binary loader.

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the X-Register with the starting location of the binary loader (7602_8, 17602_8, 27602_8, or 37602_8); depress the Start button.
3. Put machine in RUN mode; depress the Master Clear button.
4. Place the binary tape under the tape reader.
5. Turn the reader on.
6. Depress the Start button.

B. Enter the test parameters

1. Put machine in WRITE mode; depress the Master Clear button.
2. Using the probe, load the S-Register with the parameter location.
3. Using the probe, load the X-Register with the parameter constant; depress the Start button.
4. Repeat steps 2 and 3 until all parameters needed have been entered.

Location	Parameter	Description
of CCØ completion interrupt	24311_8	Transfer for CCØ interrupt
200_8	N	Number of CCØ registers is N ($1-77_8$)
277_8 ↓ $277-N+1$	Multiplexer Addresses	The multiplexer addresses for the CCØ registers to be tested start in location 277_8 and are stored sequentially in descending locations. The lowest location is 201_8. A multiplexer address contains the set channel in bits 0-5 and the word in bits 6-11. The reset channel is assumed to be one less than the set channel.

C. Start the Test

1. Put machine in WRITE mode; depress the Master Clear button.

2. Using the probe, load the X-Register with the starting location of the test (277_8); depress the Start button.

3. Put machine in RUN mode; depress the Master Clear button.

4. Depress the Start button.

D. The test runs continuously.

IV. Storage

Number of locations used: 161_8 (200_8-360_8)

P-50 CCO TEST WITHOUT CABLES

```
                                                P-50 CCO TEST WITHOUT CABLES                    P-50 D39A
                    00200           BORG 200
00200   00000   NUMREG DEC                  THE NUMBER OF CCO REGISTERS TO BE TESTED IS
                                            STORED IN THIS LOCATION
                        RPT 63
00201   00000           OCT
00202   00000
00203   00000
00204   00000
00205   00000
00206   00000
00207   00000
00210   00000
00211   00000
00212   00000
00213   00000
00214   00000
00215   00000
00216   00000
00217   00000
00220   00000
00221   00000
00222   00000
00223   00000
00224   00000
00225   00000
00226   00000
00227   00000
00230   00000
00231   00000
00232   00000
00233   00000
00234   00000
00235   00000
00236   00000
00237   00000
00240   00000
00241   00000
00242   00000
00243   00000
```

P-50 CCO TEST WITHOUT CABLES

```
            00244     00000
            00245     00000
            00246     00000
            00247     00000
            00250     00000
            00251     00000
            00252     00000
            00253     00000
            00254     00000
            00255     00000
            00256     00000
            00257     00000
            00260     00000
            00261     00000
            00262     00000
            00263     00000
            00264     00000
            00265     00000
            00266     00000
            00267     00000
            00270     00000
            00271     00000
            00272     00000
            00273     00000
            00274     00000
            00275     00000
            00276     00000
            00277     00000
  7                   00277   ADDR    SYN L-1         THIS IS THE BEGINNING LOCATION FOR THE
 10                                                  CCO REGISTER ADDRESSES.
 11                                                  THE ADDRESS FOR THE FIRST REGISTER IS STORED
 12                                                  IN LOCATION ADDR.  SUCCEEDING ADDRESSES ARE
 13                                                  STORED SEQUENTIALLY IN DECREASING LOCATIONS.
 14                                                  BITS 0-5 OF AN ADDRESS CONTAIN THE SET CHANNEL
 15                                                  BITS 6-11 OF AN ADDRESS CONTAIN THE WORD.
 16                                                  UP TO 63 ADDRESSES MAY BE ENTERED.
 17                                                  PARTS OF THE ADDRESS TABLE NOT BEING USED DO
 20                                                  NOT HAVE TO BE CLEARED.
 21
```

```
22                                  EJE
23                                      FIELD CCO TEST
24
25                                      THIS TEST SETS ALL CONTACT OUTPUTS IN SYSTEM TO 1,
26                                      WAITS ONE SECOND,
27                                      THEN SETS ALL CONTACT OUTPUTS TO ZERO AND RESTARTS
30
31
32   00300  62 0 351   START   ENL TWO
33   00301  37 0 357           STL RESET
34   00302  62 0 353   1LOP    ENL OUTIT
35   00303  37 0 307           STL OTCOM
36   00304  62 0 200           ENL NUMREG
37   00305  37 0 356           STL REGCNT
40   00306  62 0 350           ENL MINUS
41   00307  64 1 277   OTCOM   OUT ADDR,I
42   00310  23 0 310           CLJ L+1
43   00311  01 0 000           DCR PC
44   00312  01 0 307   INTRPT  DCR OTCOM       INTERRUPT RETURN
45   00313  01 0 356           DCR REGCNT      NEG AFTER LAST REGISTER IS OUTPUT
46   00314  27 0 306           PJP OTCOM
47   00315  62 0 352           ENL TIMCNT
50   00316  01 0 101   DCR     DCR ACC         ONE SECOND TIME DELAY
51   00317  24 0 317           JMP L+1
52   00320  24 0 320           JMP L+1
53   00321  24 0 321           JMP L+1
54   00322  24 0 322           JMP L+1
55   00323  24 0 323           JMP L+1
56   00324  24 0 324           JMP L+1
57   00325  27 0 315           PJP DCR
60   00326  62 0 200           ENL NUMREG
61   00327  37 0 356           STL REGCNT
62   00330  62 0 355           ENL BEGADR
63   00331  37 0 360           STL FIXADR
64   00332  01 0 357           DCR RESET
65   00333  27 0 342           PJP CLEAR
66   00334  62 1 360   LOP2    ENL FIXADR,I
67   00335  10 0 354           ADD ONE
70   00336  37 1 360           STL FIXADR,I
71   00337  01 0 360           DCR FIXADR
```

P-50 CCO TEST WITHOUT CABLES

```
 72   00340  01 0 356          DCR REGCNT
 73   00341  27 0 333          PJP LOP2
 74   00342  24 0 277          JMP START
 75   00343  01 1 360  CLEAR   DCR FIXADR,I
 76   00344  01 0 360          DCR FIXADR
 77   00345  01 0 356          DCR REGCNT
100   00346  27 0 342          PJP L-3
101   00347  24 0 301          JMP 1LOP
102   00350     37777  MINUS   OCT 37777
103   00351     00002  TWO     OCT 2
104   00352     17777  TIMCNT  OCT 17777
105   00353  34 1 277  OUTIT   OUT ADDR,I
106   00354     00001  ONE     OCT 1
107   00355     00277  BEGADR  OCT ADDR
110
111
112
113               00356  REGCNT  SYN BEGADR+1
114               00357  RESET   SYN REGCNT+1
115               00360  FIXADR  SYN RESET+1
116               00000          END
```

PRODAC 50 PROGRAMMER'S CONSOLE PACKAGE

I. Introduction

The programmer's console programs facilitate communication with the P-50 computer. The package provides a means of loading programs, executing programs, loading constants or instructions, and dumping areas of main and extended core memory. Core locations may be dumped in binary on tape or in octal on the keyboard.

The programmer's console operates within the priority structure of the X50F executive system for all of its functions, and its calling priority is established for a particular system when the executive system is initialized. Note that this programmer's console is included with standard executive system X50F only.

Before initiating a programmer's console function, the ASR punch and reader should be turned off. Then to gain the computer's attention, the Attention Interrupt Button is depressed. The attention interrupt will have any one of two or four effects depending upon the initialization of MPCOPT -- the message writer option for the programmer's console.

a) If neither the programmer's console nor the device 0 program is currently running, the programmer's console programs will be put into the bidding state.

b) If the programmer's console is not currently running but the device 0 program is running, the flag PCFLG will be set and the programmer's console programs will be suspended.

c) If the programmmer's console is currently running and the device 0 program is not running; the programmer's console programs will exit to TOPLOP and the ASR set will be turned off.

d) If the programmer's console is suspended and the device 0 program is running, the flag PCFLG will be cleared and the programmer's console programs will be turned off.

When the programmer's console programs are permitted to run by the executive system, the ASR set will be turned on and input from the ASR set will be requested. Input consists of a two-letter mnemonic followed either by a space and up to four constants or by a return. If more than two letters precede the space (or the return), only the last two will be considered. The resulting two-letter mnemonic is then compared to the defined mnemonics. If it is not found equal to any, "ERR 1" will be printed and the programmer's console will exit to TOPLOP and the ASR set will be turned off.

If the two-letter mnemoic is found equal to a defined mnemonic, a transfer to the proper program will be set up, and if a space followed the mnemonic code, any constants preceding the return will be input. The number of constants will depend on the function being initiated. Constants must be entered in octal or decimal; a plus or minus sign at the beginning of a constant specifies it to be a decimal number; unsigned integers are

considered to be in octal. Constants are terminated by a slash (/) or by a return. Decimal and octal constants may both appear on the same line of input. If a character is input other than an octal or decimal constant "ERR" will be printed and the programmer's console will exit to TOPLOP and the ASR set will be turned off.

If the correction character left parenthesis "(" is encountered, all digits following the last slash or the space are ignored.

If more than four constants are entered before a return, "ERR 2" will be printed and the programmer's console programs will exit to TOPLOP and the ASR set will be turned off. If more or less constants are specified than are required by the function being initiated, "ERR 2" will also be printed and the programmer's console will be turned off.

When a return has been input to the programmer's console, the transfer to the requested programmer's console program is put into effect with the number of constants in the accumulator (zero when a return followed the mnemonic code) and with the constants stored in the order that they were input in CON1, ..., CON4. A line feed may precede the return; this character is always ignored on input. When the programmer's console program completes the activity requested, further constants may be required. These are entered in the same manner as the initial constants--that is, in decimal or octal, separated by slashes, and terminated with a return.

II. Programmer's Console Programs

This programmer's console package contains eleven defined functions: Binary Load, Binary Punch from Main Memory, Binary Punch from Extended Memory, Check Tape, Set Limits for Main Memory, Set Limits for Extended Memory, Numeric Load into Main Memory, Numeric Load into Extended Memory, Octal Dump from Main Memory, Octal Dump from Extended Memory, Run on Machine. Provision for more programs to fit specific installations has been made in that there is room for ten more mnemonics to be defined and ten more transfer locations to be inserted.

The defined programmer's console functions are described below. In input examples, ␣ represents space and) represents return.

A. Binary Load

Mnemonic code:	BL
Number on constants:	zero

When this function is initiated, a binary tape in the standard P-50 binary format will be loaded through the programmer's console tape reader into main or extended core. The binary load function is controlled by control words on the binary tape so that no constants are input. (See section on Binary Tape Format).

If any constants are input, the message "ERR 2" will be printed and the programmer's console will be turned off. If a character with even parity is detected on the binary tape, "ERR 4" will be printed; if the check-sum on the tape does not compare to the sum of the words on the tape, "ERR 5" will be printed. If either of these errors occurs, the ASR set will be turned off following the printing of the appropriate message.

B. Binary Punch

1. Binary Punch from Main Memory

Mnemonic code:	BP
Number on constants:	0, 1, 2

2. Binary Punch from Extended Memory

Mnemonic code:	XP
Number of constants:	0, 1, 2

The mnemonic code determines whether main memory (BP) or extended memory (XP) will be referenced. Each is a separate function.

Depending upon the number of constants which are input, a core area or core location, a transfer code, or a stop code will be punched in binary by the programmer's console punch. Two constants designate a core area or location; one constant specifies a transfer code and the main memory transfer location, no constant results in a stop code.

If two constants are input and the first is not less than or equal to the second, "ERR 3" will be printed and the programmer's console will be turned off.

When using this function with a high speed punch, the turning on and off of the punch will be done via programming.

When the punch on the ASR set is used, it must be turned on and off manually. Since input from the keyboard will be punched on tape if the punch is turned on, in addition to the binary output requested, the following procedure is recommended:

1. Turn punch off.
2. Depress Attention Interrupt Button.
3. Type on keyboard: BR␣XX/XX↵ or XP␣XX/XX↵
4. Turn punch on--leader will be punched followed by requested area in binary.
5. Turn punch off.
6. Type on keyboard: (XX/XX↵ (another area), or (XX↵ (transfer code) or (↵ (stop code). Always begin with the correction character "(".
7. Turn punch on--leader will be punched followed by an area in binary, or a transfer code or stop code.
8. Turn punch off and continue.

Examples: To obtain a binary tape of a program currently located in main memory locations 600_8 - 723_8 and of another program in location 1012_{10} - 1244_{10} and to put a transfer to location 610_8 at the end of the tape, the following should be executed:

```
BP↓600/723↵
(+1012/+1244↵
(610↵
```

To obtain a binary tape containg the contents of extended core locations 600_8 - 723_8 and 1012_{10} - 1244_{10}, and terminated with a stop code, the following should be executed:

```
XR↓600/723↵
(+1012/+1244↵
↵
```

C. Check Tape

Mnemonic code:	CT
Number of constants:	zero

A binary tape in the standard P-50 binary format will be compared, word by word, to the contents of the proper area of either main or extended core. If any discrepancies occur, the core location, the contents of the tape and the contents of core will be printed in the octal dump format. An "A" will precede an extended core address. The process will continue until the end of the tape. The tape will be parity checked and checksum checked at the same time.

If any constants are input following the function code, "ERR 2" will be printed and the programmer's console will be turned off. If a parity error is detected, "ERR 5" will be printed. These errors both turn off the programmer's console programs and the ASR set.

Example:

```
   CT↵
    762  23200  32301
   1102      1  37777
A   466  37777  37775
A20215  20001  20133
```

The first word following the location is the contents of the tape; the second is the contents of core.

When the programmer's console reader is used for this function rather than a high speed reader, the printing of one discrepancy will alter the I/O sequence and further input will be incorrect. Thus, this function should be used with the ASR reader only to verify that a tape has been punched correctly.

D. Set Limits

1. Set Limits for Main Memory

Mnemonic code:	LM
Number of constants:	2

2. Set Limits for Extended Memory

Mnemonic code:	XM
Number of constants:	2

When either of the set limit functions is called for, two constants should be entered prior to the first return. These constants define the core area or location usable by the numeric load functions.

If the first or both constants are zero (0) the limits are set to zero and the entire core is protected. (The limits are initially set to zero). If the first constant is not less than or equal to the second constant, "ERR 3" will be printed and the programmer's console will be turned off.

Examples:

To set limits in Main Memory to the core area 10000_8 through 10100_8, the following should be executed:

LM␣10000/10100␤

To set limits in extended memory to one location 7000_8, the following should be executed:

XM␣7000/7000␤

E. Numeric Load

1. Numeric Load into Main Memory

Mnemonic code:	NL
Number of constants:	zero

2. Numeric Load into Extended Memory

Mnemonic code:	XL
Number of constants:	zero

When either of the numeric load functions is called for, no constants should be entered prior to the first return. Successive constants separated by returns designated the locations to be modified and octal or decimal data. Both functions are terminated by the right parenthesis ")".

If an attempt is made to enter data without first specifying the beginning location, "ERR 3" will be printed and the programmer's console and ASR set will be turned off.

If an attempt is made to enter data into a location outside the core limits, "ERR 7" will be printed and the programmer's console and ASR set will be turned off.

Input:	Location:	Contents:	Comment:
NL↵ or XL↵			Calling Sequence for Main or Extended Memory Loading
=1022↵			Origin in octal
24026↵	1022	24026	JMP instruction entered in octal
+17↵	1023	00021	Decimal Data
+27↵	1024	00033	Decimal Data
21↵	1025	00021	Octal Data
33↵	1026	00033	Octal Data
=+600↵			New Origin in decimal
10073↵	1130	10073	ADD instruction entered in octal
↵	1131		Do not change this location
379(37073↵	1132	37073	STL instruction entered in octal, correction character used
)			Terminal character

The correction character "(" may be used with this function. However, if an error occurs when typing the origin, note that the equals character which was input is not ignored.

Error:	=10782
Correct:	=10782(10772
Incorrect:	=10782(=10772

F. Octal Dump

1. Octal Dump from Main Memory

Mnemonic code:	ØD
Number of constants:	1, 2

2. Octal Dump from Extended Memory

Mnemonic code:	XD
Number of constants:	1, 2

Depending upon the number of constants which are specified, these programs will print the contents of a core area or a location in octal. If two constants are given, the contents of the core area so defined will be output 8 words per line with the address of the first word at the beginning of each line. An "A" precedes the address of the first word for extended core dumps. If one constant is specified, the address which was input and the contents of the location will be printed. A return alone (no constants) signifies the end of request.

If two constants are specified and the first is not less than or equal to the second, "ERR 3" will be printed and the programmer's console and ASR set will be turned off.

Examples:

```
OD +210/+220↵
322   32015  11014  27216  20371  32015  27212  32014
332   27216  20216      3
465/472↵
465    1012   1053   1064     33     14     62
↵
XD +503/+514↵
A 767    20777    21031   1072   10100   10267   10777   16000   30010
A 777    1777    37224    2030  16553
1047↵
A 1047    32602
↵
```

G. Run on Machine

Mnemonic code:	RN
Number of constants:	1

This function transfers control to the location specified. If exactly one constant is not input, "ERR 2" will be printed and the programmer's console and ASR set will be turned off.

The program thus initiated can be terminated manually depressing the attention interrupt button or turned off by having it exit to EXIT in the attention interrupt routine. Note that all references to the running sublevel in this program must be for the programmer's console sublevel.

III. Key to Error Printouts

ERR 1	Mnemonic error
ERR 2	Constant error
ERR 3	Format error
ERR 4	Parity error
ERR 5	Checksum error
ERR 6	Illegal character
ERR 7	Out of limits

IV. ASCII-BCD Code Table

BCD	Character	ASCII	BCD	Character	ASCII
00	0	060	40	-	055
01	1	261	41	J	312
02	2	262	42	K	113
03	3	063	43	L	314
04	4	264	44	M	115
05	5	065	45	N	116
06	6	066	46	Ø	317
07	7	267	47	P	120
10	8	270	50	Q	321
11	9	071	51	R	322
12	↑	336	52	←	137
13	=	275	53	$	044
14	Return	215	54	*	252
15	:	072	55	]	335
16	>	276	56	;	273
17	!	041	57	@	300
20	+	053	60	Space	240
21	A	101	61	/	257
22	B	102	62	S	123
23	C	303	63	T	324
24	D	104	64	U	125
25	E	305	65	V	126
26	F	306	66	W	327
27	G	107	67	X	330
30	H	110	70	Y	131
31	I	311	71	Z	132
32	?	077	72	%	245
33	.	056	73	,	254
34	)	251	74	(	050
35	[	333	75	&	246
36	<	074	76	\	134
37	#	243	77	Line Feed	012

V. Binary Tape Format

On a binary tape, one word consists of three characters. Each character contains eight levels; levels one through six contain data unless the word is a control word. Each character is punched in odd parity and the parity bit when preset appears in the eight level.

A Prodac 50 word in core contains 14 bits; the correspondence between a core word and a word on the binary tape is as follows:

Bits 12-13	Character 1, levels 1-2
Bits 6-11	Character 2, levels 1-6
Bits 0-5	Character 3, levels 1-6

A punch in the seventh level of the first character of a word indicates that the word is checksum.

Levels 3-4 of the first character of a word are always zero; they are ignored. Levels 5-6 define a control word--the first word on a binary tape and the first word following a checksum are control words.

The following describes the differences among the control words and their effects when loaded through the binary loader:

A. Load Main Memory Word. Zeros in the fifth and sixth levels of the first character of a control word define a load main memory word. Subsequent data will be stored directly into successive locations in main memory starting at the location specified by the data in character 1, levels 1-2, and characters 2 and 3, levels 1-6.

B. Load Extended Memory Word. A zero in level six and a one in level five of the first character define a load extended memory word. Subsequent data will be stored directly into successive locations in extended core starting at the location specified by the data in character 1, levels 1-2, and characters 2 and 3, levels 1-6.

C. Transfer Control Word. A one punched in level six and a zero in level five of the first character of a control word define a transfer control word. Machine control will be transferred to the location specified in the remaining data levels (not all ones).

D. Load Stop Word. This control word consists of a punch in level six of the first character, zero in level 5, and all ones punched in the remaining data levels. Machine control is transferred to the priority executive, thus terminating the loading process.

APRIL, 1969

P-50
PRINTED CIRCUIT
CARD DESCRIPTIONS

HAGAN/CSD
TRAINING DEPARTMENT

Westinghouse Electric Corporation

TABLE OF CONTENTS

SECTION I MAIN FRAME

TABLE OF CONTENTS (Continued)

SECTION II INPUT/OUTPUT

AUTOMATIC RESET 1AR3

A. GENERAL DESCRIPTION

The Automatic Restart Card contains circuits to provide the following functions:

1. Detect whether the central processor was running or stopped when the low voltage sensor applied a clamp to the memory subsystem.

2. Automatically restart the central processor upon resumption of power if the machine had stopped prior to the clamping of the memory.

B. CIRCUIT OPERATION

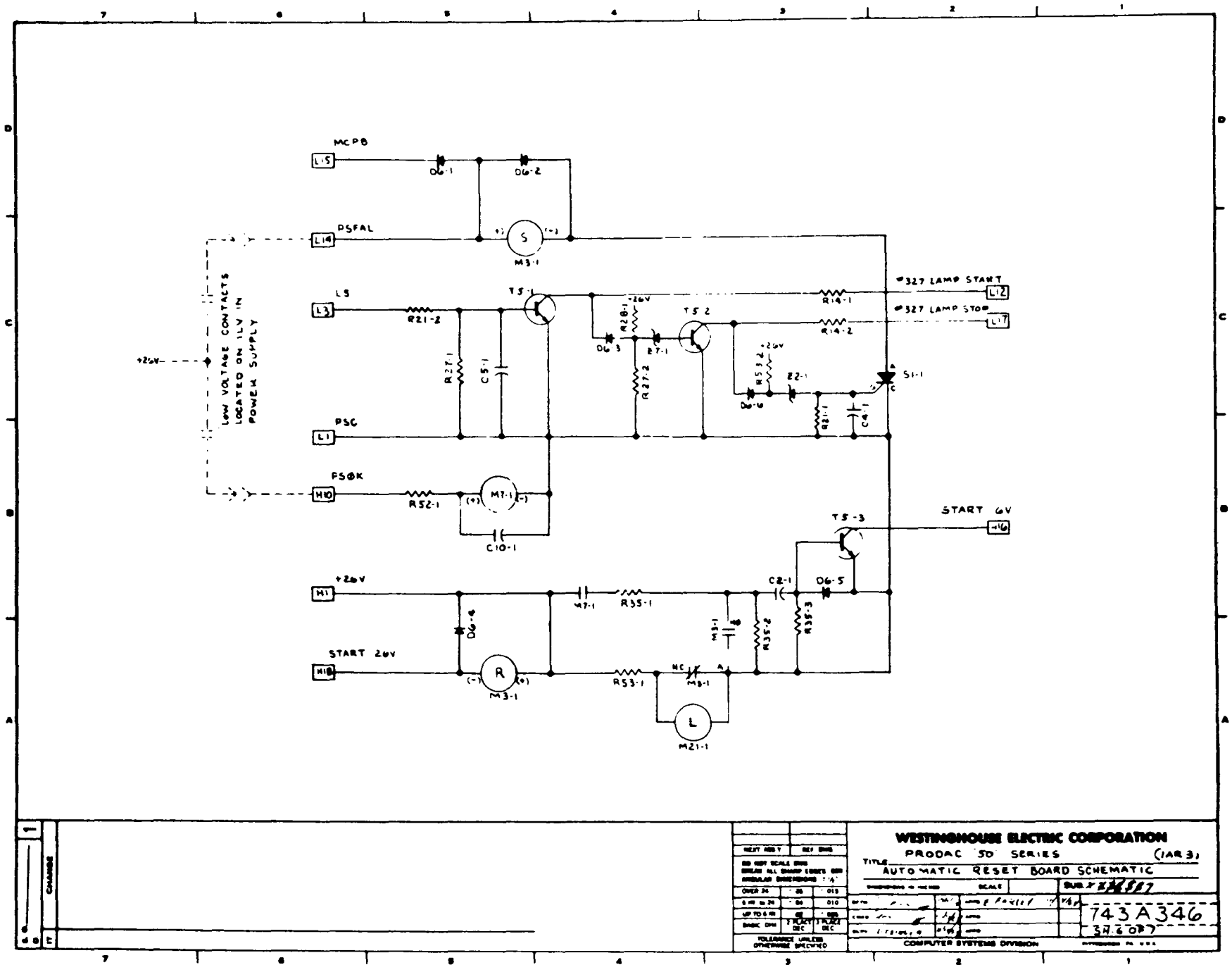
Drawing 743A346 shows the run detection circuit. Pin L3 goes to the final tap of the delay line timing chain. With the central processor running, pulses periodically appear at this point and are filtered to provide base drive for transistor T5-1. T5-1 conducts turning on the lamp in the "start" pushbutton and also removing the base drive from transistor T5-2. With T5-2 cutoff, gate drive is provided to the SCR, S1-1, which serves as the run detector.

If the power supply fault contacts close providing +26 to pin L14, while S1-1 has gate drive, a current is circulated in the set coil of the bistable relay M3-1. The setting of M3-1 signifies that the central processor was not stopped when the fault occurred. Upon power resumption auto restart is inhibited by the NØ contacts of relay M3-1 and the auto restart fault lamp M21-1 will be on. M3-1 is reset by manual starting.

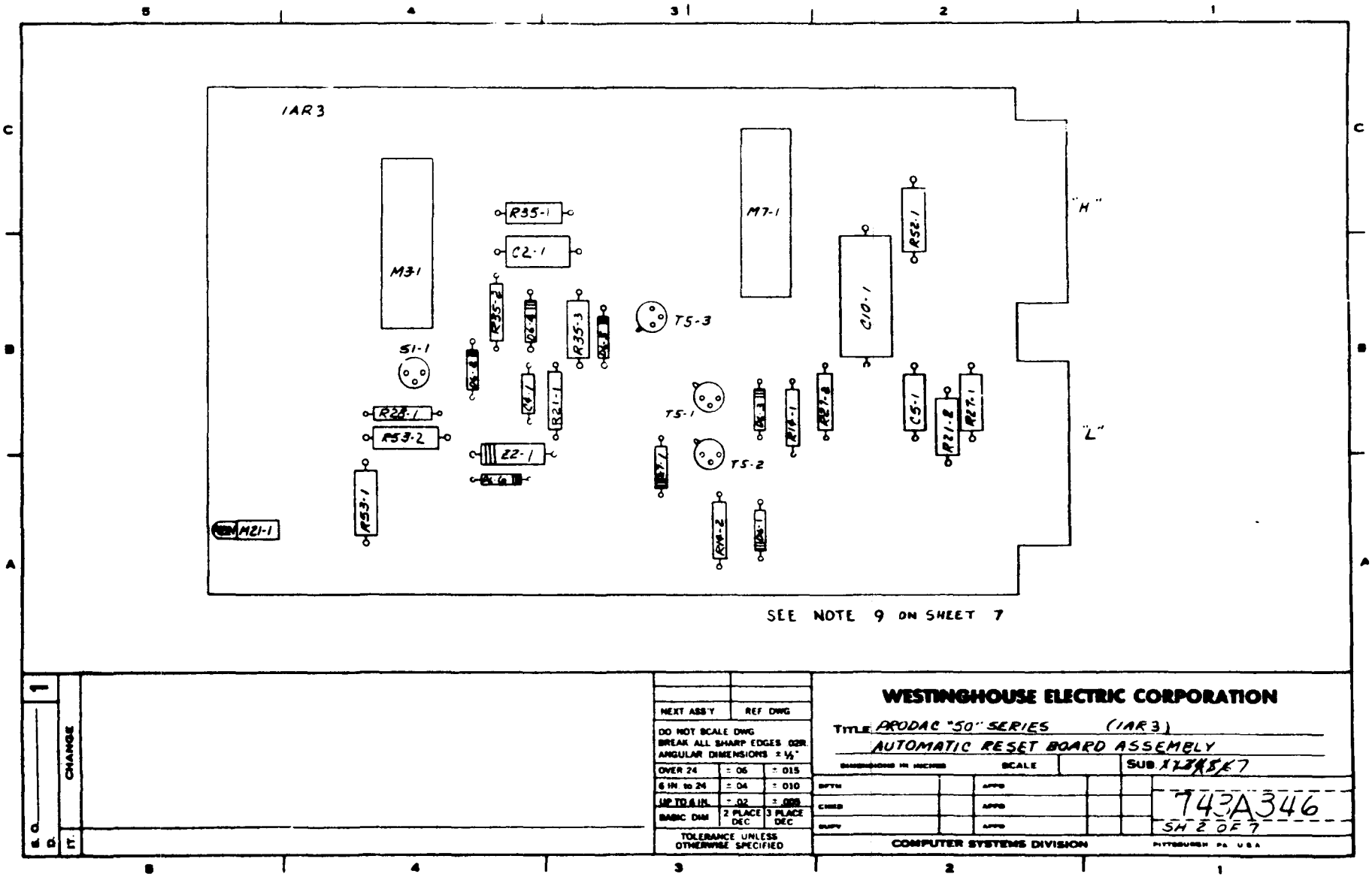
If, however, in response to the power supply failure interrupt, the central processor completed its tasks and stopped prior to the closing of the power supply fault contacts, base drive would be removed from T5-1 which in turn would cause T5-2 to conduct, turning on the stop lamp.

This removes the gate drive from S1-1. Now when +26 is applied to pin L14 by the power supply fault contact, S1-1 does not conduct and relay M3-1 is not set. The Master Clear relay is picked, keeping the processor in a cleared state as power is removed.

The auto restarting circuit is also located on the automatic reset card. As power is resumed after an outage, the low voltage contacts are still in the power supply fault position and the positive supply is connected to pin L14. This in turn holds the central processor in the master cleared state until a voltage sufficient for running is obtained. Then the low voltage contacts transfer to the PSØK state - applying the positive supply to pin H10. This energizes relay M7-1 which provides a short time delay. When the contacts of relay M7-1 close, a positive step is applied to the capacitor C2-1, provided that the auto restart fault relay M3-1 had not been set. This step is differentiated to provide base drive for transistor T5-3. T5-3 conducts for a short period of time starting the central processor by grounding pin H16.



WESTINGHOUSE ELECTRIC CORPORATION			
PRODAC 50 SERIES		(IAR 3)	
TITLE AUTOMATIC RESET BOARD SCHEMATIC			
SCALE		SIZE D	743A346
COMPUTER SYSTEMS DIVISION			3M6087



NEXT ASS'Y	REF DWG	
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°		
OVER 24	± .06	± .015
6 IN to 24	± .04	± .010
UP TO 6 IN.	± .02	± .005
BASIC DIM	2 PLACE DEC	3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED		

E.C.O.	IT	CHANGE	
1			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC "50" SERIES (1AR3)
AUTOMATIC RESET BOARD ASSEMBLY

DIMENSIONS IN INCHES | SCALE | SUB 1 7 8 E 7

DRTN		APPD	
CHKD		APPD	
SUPV		APPD	

743A346
SH 2 OF 7

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA U.S.A.

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BIT CARD 2BC1 3BC1 2BC2 4BC1

A. GENERAL DESCRIPTION

The bit card contains the Z, X, and S registers, and adder circuitry for one of 14 bits. In addition the bit card provides:

1. Core sense amplifying gate
2. Peripheral input gate
3. S → Z gate
4. X → Z gate
5. $\overrightarrow{Z}$ → X gate
6. Z → X gate
7. $\overline{Z}$ → X gate
8. Adder to S gate
9. Adder to inhibit timing
10. Output buffer

Figure 3-8 is a block diagram of the card as used.

B. CIRCUIT OPERATION

Dual NAND A is connected as a flip-flop and is used as the S register; in like manner Dual NAND C is used in the Z register, and Dual NAND D is used in the X register.

The adder circuitry is composed of Dual NAND's E, F, H, and K.

H11 and K11 form the carry chain (C-OUT).

NAND's H5 and K5 form the Sum of Z and X when $\overline{EOR}$ and $\overline{AND}$ inputs are logical "one's".

NAND's H5 and K5 form the AND of Z and X when $\overline{AND}$ is a "zero" and $\overline{EOR}$ is a "one".

H5 and K5 form the Exclusive OR of Z and X when $\overline{AND}$ is a "one".

Diodes D1-2 and D1-3 form decode for Sum equal to a Positive Zero.

S to Z Gate consists of modified NAND B11 which is used as an inverter.

X to Z Gate consists of modified NAND B12 which is used as an inverter.

$\overrightarrow{Z}$ to X Gate consists of modified NAND J12 and an input from Z register.

Z to X Gate consists of modified NAND G12 and an input from the Z register.

Z to X Gate consists of modified NAND G5 and a complemented input from the Z register.

Adder to S Gate consists of NAND F5; this allows the sum of X and Z to be gated to the S register.

Adder to Inhibit Timing consists of NAND F11. Diode D1-6 forms a decode for SUM equal to Negative Zero.

Output Buffer consists of modified NAND J11; this is used to buffer X register output data to peripheral driver cards.

Refer to the circuit in the upper left hand corner of schematic 743A300.

This circuit accommodates inputs from core memory (pins L18 and L17) and from other inputs on pin L15.

Transistor T8-1 is usually biased off. When the sense preamp output voltage exceeds 0.5 volt, T8-1 conducts. This provides base drive for T1-1 to set the Z register flip-flop if strobe is a "one".

This circuit is also used to accommodate input data (pin L15).

An input voltage of 4.5 volts minimum from any one of the digital buffer cards causes the Z register flip-flop to be set by turning on transistor T1-1 if input strobe is a "one".

Lamp Driver: The 3 volts, 15 ma indicators are driven from a saturating transistor which drives the lamp through a high impedance to limit inrush current and improve bulb life.

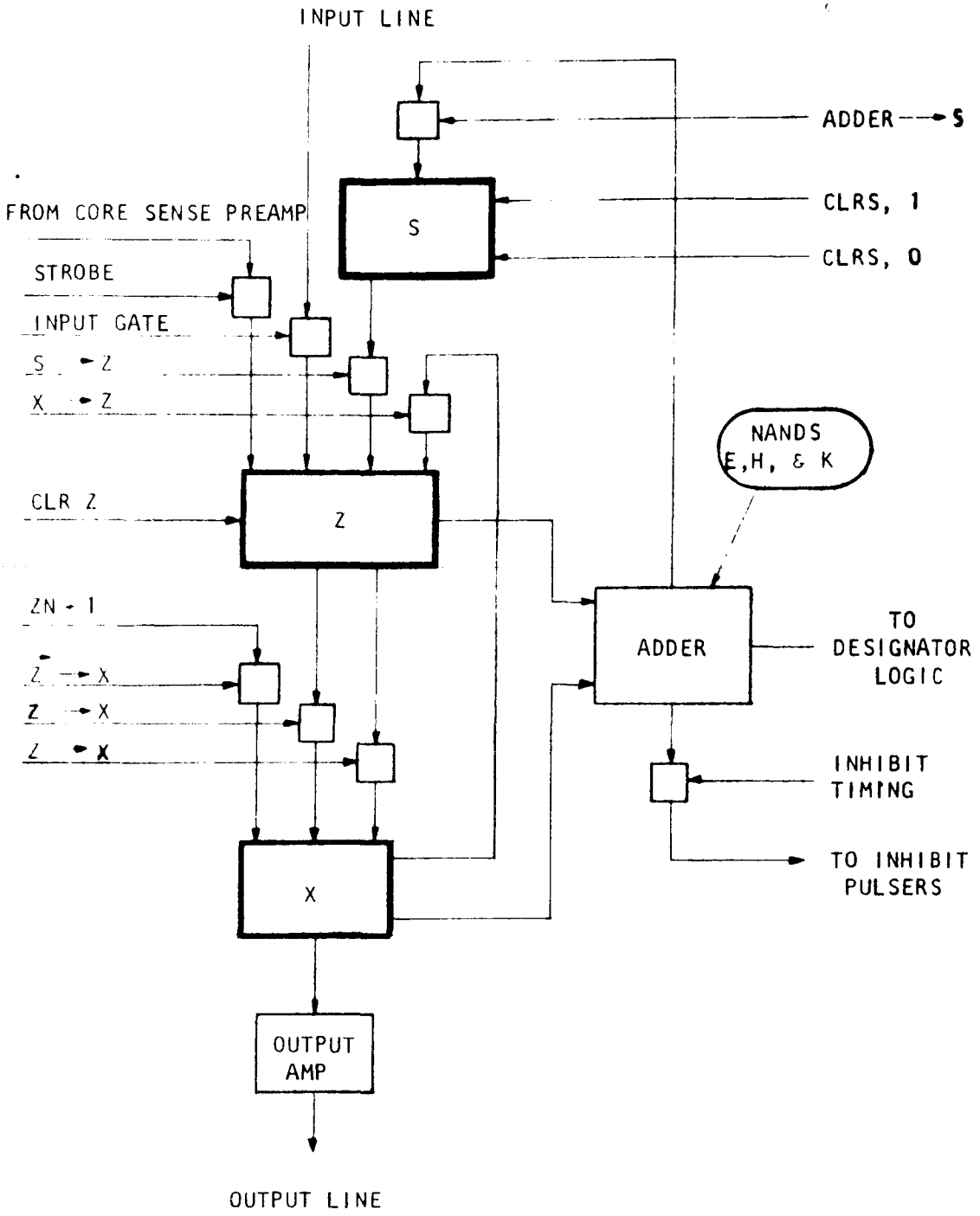
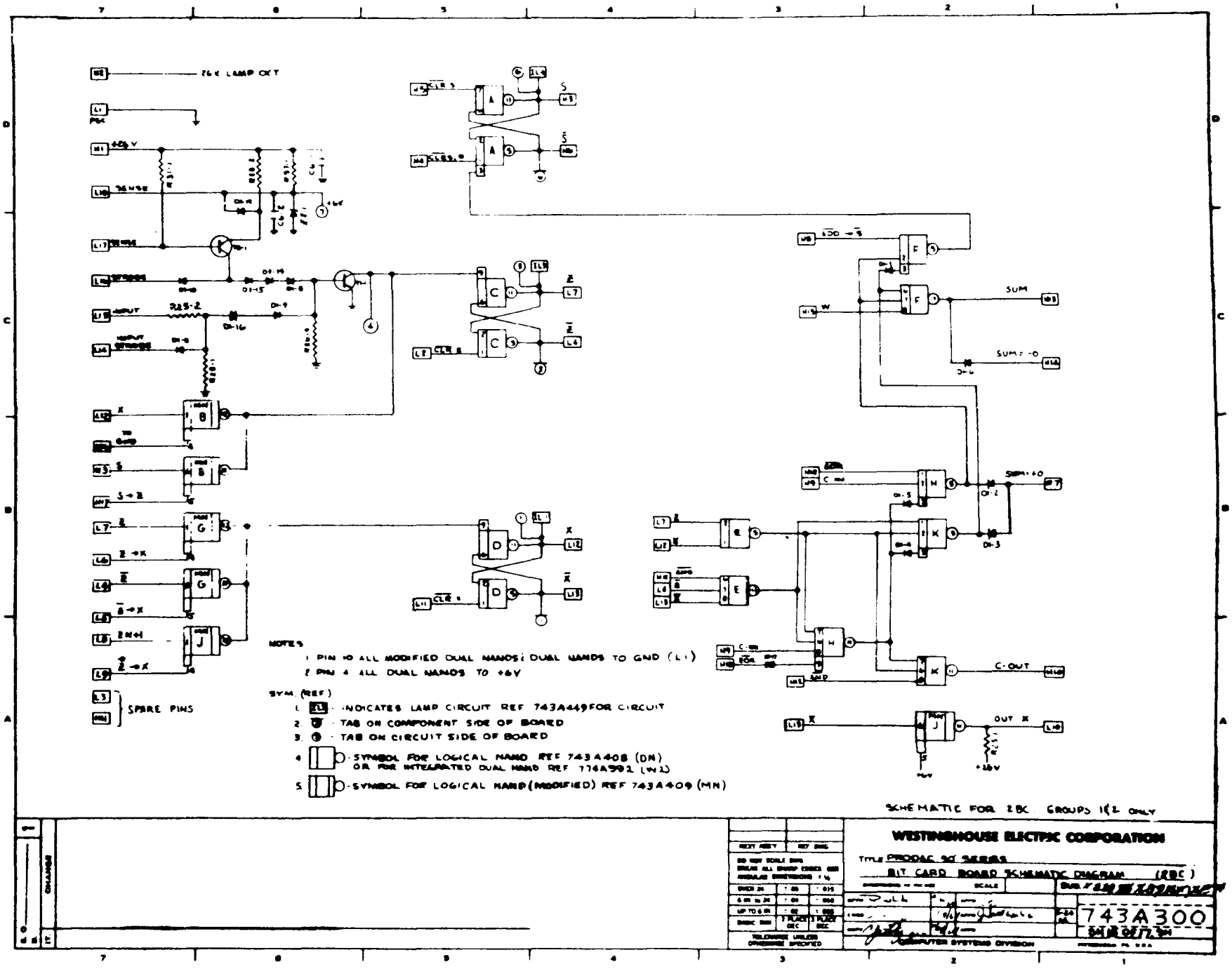
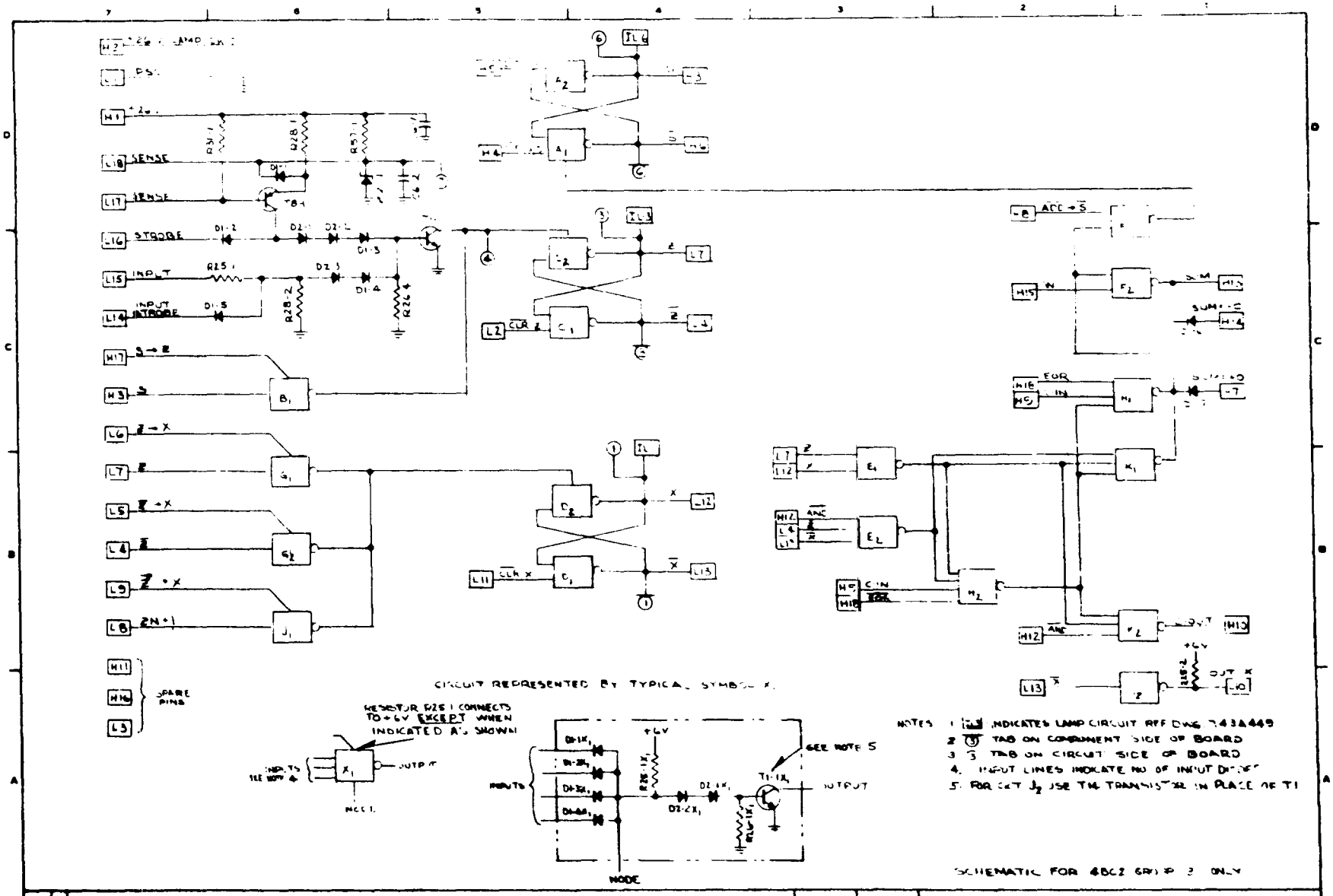

INPUT LINE
ADDER → S
FROM CORE SENSE PREAMP
S
CLRS, 1
CLRS, 0
STROBE
INPUT GATE
S → Z
X → Z
NANDS E,H, & K
CLR Z
Z
ZN + 1
Z → X
Z → X
Z → X
ADDER
TO DESIGNATOR LOGIC
INHIBIT TIMING
TO INHIBIT PULSERS
X
OUTPUT AMP
OUTPUT LINE

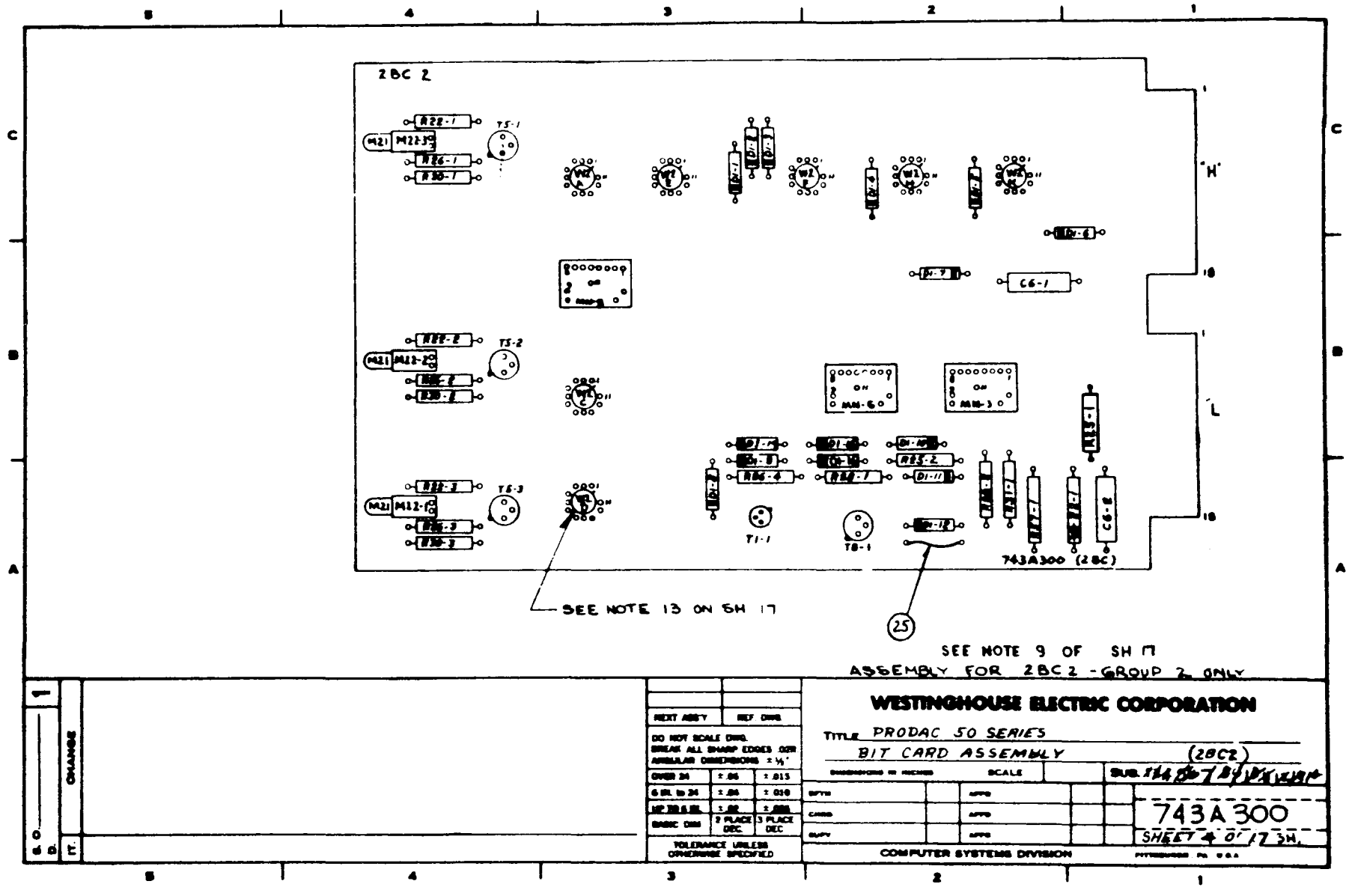
Figure 3-8.

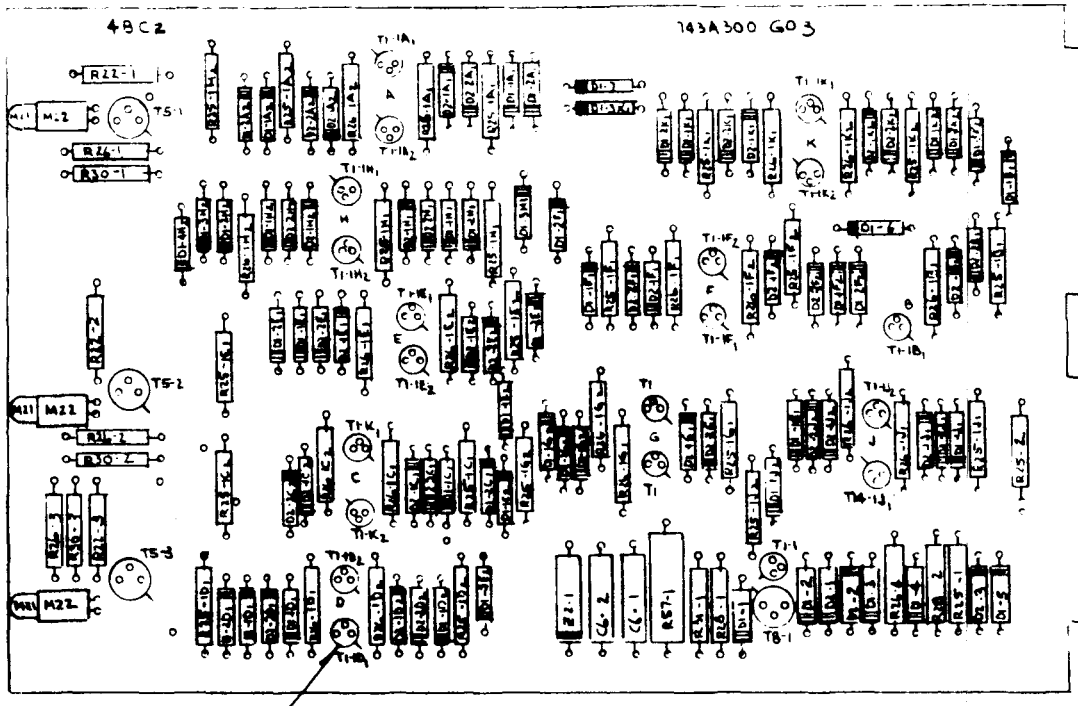

+6V LAMP OUT
SUM
SUM-1-0
C-OUT
OUT X
SPARE PINS
NOTES
1. PIN 10 ALL MODIFIED DUAL NANDS; DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6V
SYM (REF)
1. INDICATES LAMP CIRCUIT REF 743A449 FOR CIRCUIT
2. TAB ON COMPONENT SIDE OF BOARD
3. TAB ON CIRCUIT SIDE OF BOARD
4. SYMBOL FOR LOGICAL NAND REF 743A408 (DN) OR FOR INTEGRATED DUAL NAND REF 774A592 (WJ)
5. SYMBOL FOR LOGICAL NAND (MODIFIED) REF 743A409 (MN)
SCHEMATIC FOR EBC GROUPS 1&2 ONLY
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
BIT CARD BOARD SCHEMATIC DIAGRAM (EBC)
743A300
COMPUTER SYSTEMS DIVISION

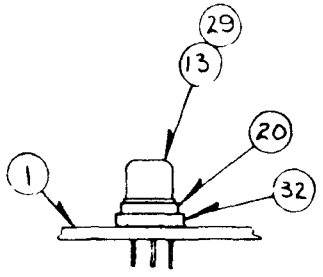


NOTES
1. INDICATES LAMP CIRCUIT REF DWG 743A449
2. TAB ON COMPONENT SIDE OF BOARD
3. TAB ON CIRCUIT SIDE OF BOARD
4. INPUT LINES INDICATE NO OF INPUT DIODES
5. FOR CKT J_2 USE THE TRANSISTOR IN PLACE OF T1

WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES (48C2)
BIT CARD SCHEMATIC
743A300
SHEET 8 OF 17
COMPUTER SYSTEMS DIVISION


2BC 2
SEE NOTE 13 ON SH 17
25
SEE NOTE 9 OF SH 17
ASSEMBLY FOR 2BC2 - GROUP 2 ONLY
743A300 (2BC)
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES
BIT CARD ASSEMBLY (2BC2)
743A300
SHEET 4 OF 17 SH.
COMPUTER SYSTEMS DIVISION





DETAILED ASSEMBLY OF TRANSISTORS (TYPE TO-18 CASE ONLY) & PADS (ITS. 20 & 32) TO BOARD

ASSEMBLY FOR 4BC2- GROUP 3

1	CHANGE		
S.O.			
IT.			

NEXT ASS'Y	REF DWG
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°	
OVER 24	± .06 ± .01S
6 IN. to 24	± .04 ± .010
UP TO 6 IN.	± .02 ± .005
BASIC DIM	2 PLACE DEC 3 PLACE DEC.
TOLERANCE UNLESS OTHERWISE SPECIFIED	

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES (4BC2)
BIT CARD ASSEMBLY

DIMENSIONS IN INCHES | SCALE | SUB. XXXXXX

DRTN		APPD	
CHKD		APPD	
SUPV		APPD	

743A300
SH 5 OF 17

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA. U.S.A.

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CORE PULSER CARD 2CP1 - 3CP1

A. GENERAL DESCRIPTION

This card is used to provide pulse amplifiers driving the X and Y half-select lines or to drive the inhibit lines of the core stack. (See Figure 3-9).

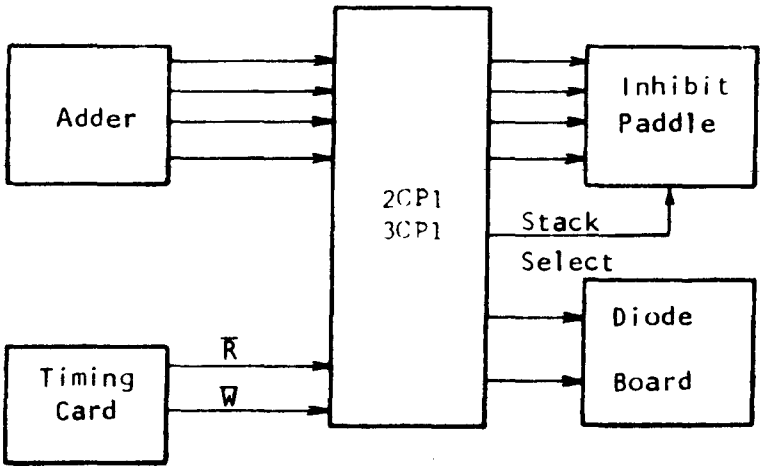


Figure 3-9.

B. CIRCUIT OPERATION

1. The card contains six pulsers and one stack select amplifier. Four of the six pulsers are inhibit pulsers, one is a Read (or Inhibit) pulser, the other a Write (or Inhibit) pulser.

2. The circuit diagram of the core pulser card is shown on schematic 743A315. The card receives inputs from the adder and timer cards. Its outputs are used to provide pulse amplification to inhibit lines on to the half-select lines.

Since this board has six identical pulser circuits, the circuit in the upper left of schematic 743A315, will be discussed here.

Signals will be defined as a "1" (positive voltage) or a "0" (zero voltage).

If both the stack select (SEL) and input pulse (pin L3) are at a "1" level, transistor T1-1 will conduct and this will block transistors T6-1 and T2-1.

If now the input goes to ground ("0" level), and the output transistor (T1-8) of the stack select amplifier is conducting, transistor T1-1 will be blocked for a maximum duration determined by capacitor C4-1 and resistors R26-1, R34-1, and R26-2. Under normal operating conditions, the actual duration is determined by the length of the Input or Stack Select pulse.

If a stack select pulse (SEL) is not present (logical "1") and there is an input pulse (logical "0"), enough current will be supplied through resistor R52-1 to keep transistor T1-1 conducting.

Should a stack select pulse saturate (drive into heavy conduction) the output transistor (T1-8 of the stack select amplifier) sufficient base drive will be provided through resistor R34-1 to keep T1-1 conducting.

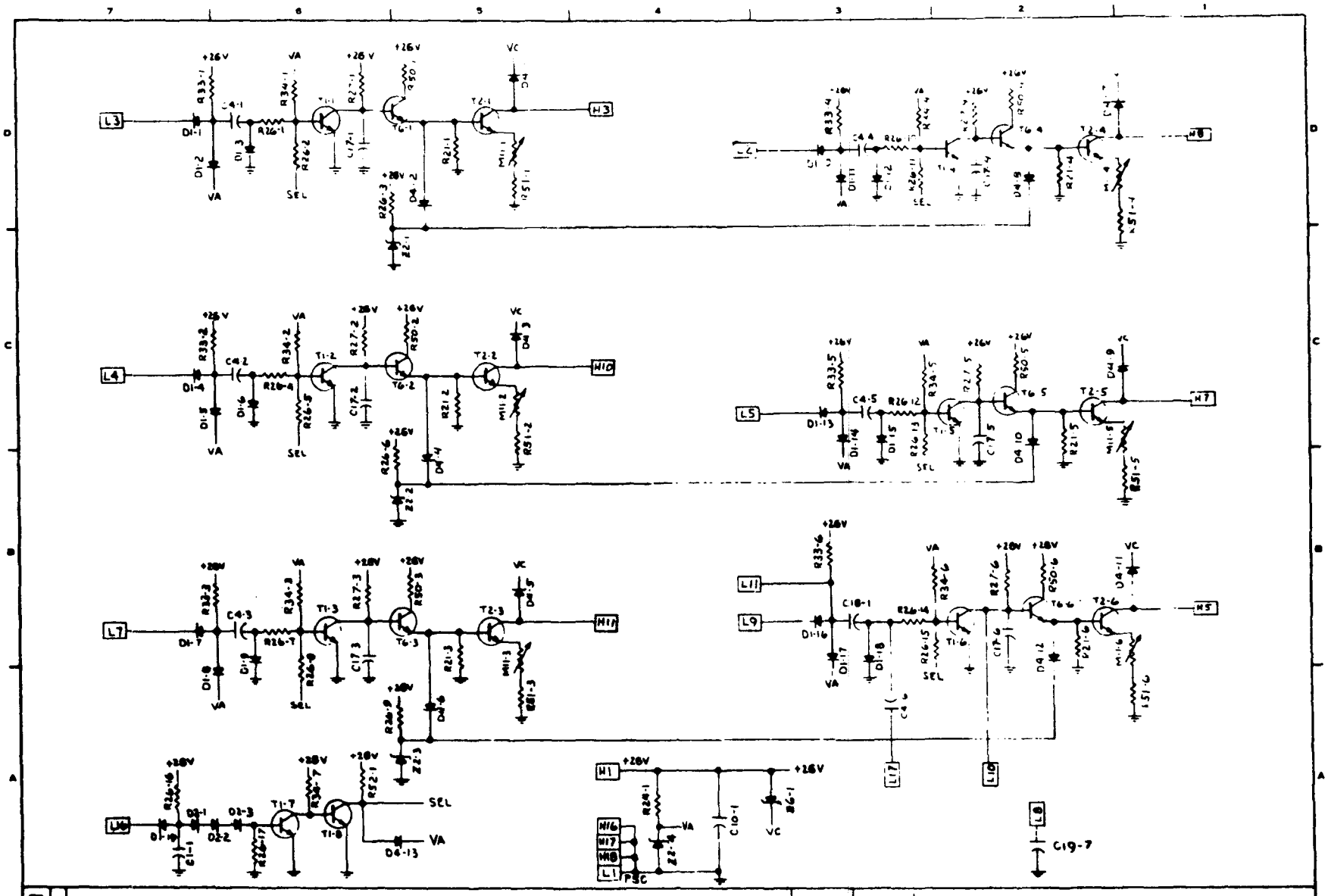
When transistor T2-1 is not blocked, it acts as a current source. The current is determined by zener diode Z2-1, resistor R51-1 and the setting of potentiometer M11-1. The cathode of diode D4-1 is connected to a 22 volt zener (Z6-1) to limit any excessive inductive feedback.

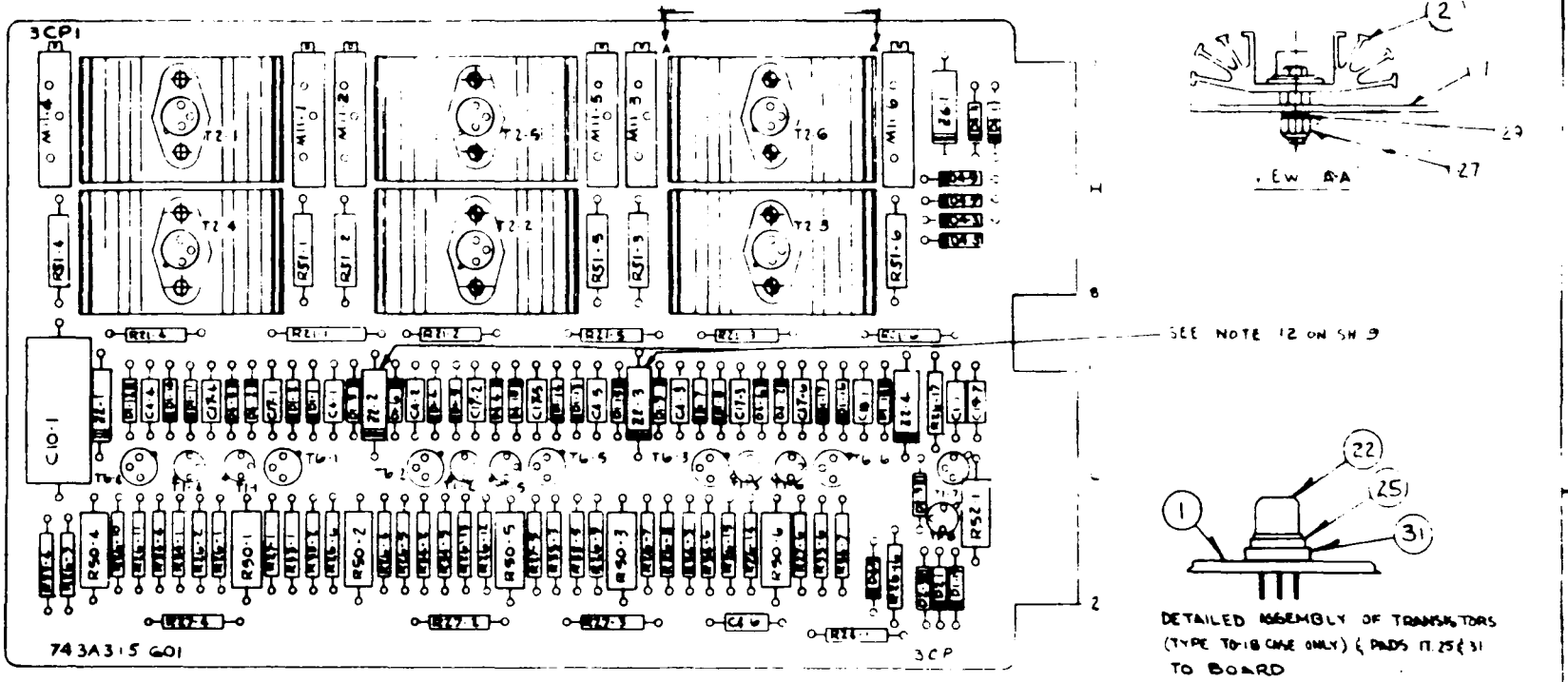
Capacitor C4-1 determines the maximum output pulse under fault conditions (that is with no Input Pulse or Stack Select Pulse).

Capacitor C17-1 controls the rate of rise of the current in the output stage to reduce inductive overshoot and feedback.

The potentiometers on the card are used to adjust currents through a 300 to 400 milliampere range.

The location of the potentiometer on the card are as shown on the module layout drawing.


L3
H3
L6
H6
L4
H10
L5
H7
L7
H11
L11
L9
H5
L12
L10
L8
C19-7
H1
H16
H17
H18
L1
PSC
SEL
VA
D4-13
+26V
VA
VC
WESTINGHOUSE ELECTRIC CORPORATION
COMPUTER SYSTEMS DIVISION
743A315



NEXT ASS'Y		REF DWG	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ±½°			
OVER 24	± 06	± 015	
6 IN. to 24	± 04	± 010	
UP TO 6 IN.	± 02	± 005	
BASIC DIM	2 PLACE DEC	3 PLACE DEC	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES (3CP1)
CORE PULSER CARD ASS'Y.

SCALE 1:1

743A315
SH. 3 OF 9

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA U.S.A.

DESIGNATOR CARD 2DC1

A. GENERAL DESCRIPTION

The 2DC1 card is used to provide the following functions.

1. A five bit designator register
2. A gating designator decode logic for setting designator
3. A gate for designator to the Z register bits 0-4
4. A gate for bits 0-4 of the Z register to the designator
5. A decode for non-conditional jumps and designator jump
6. A decode for return jump instructions

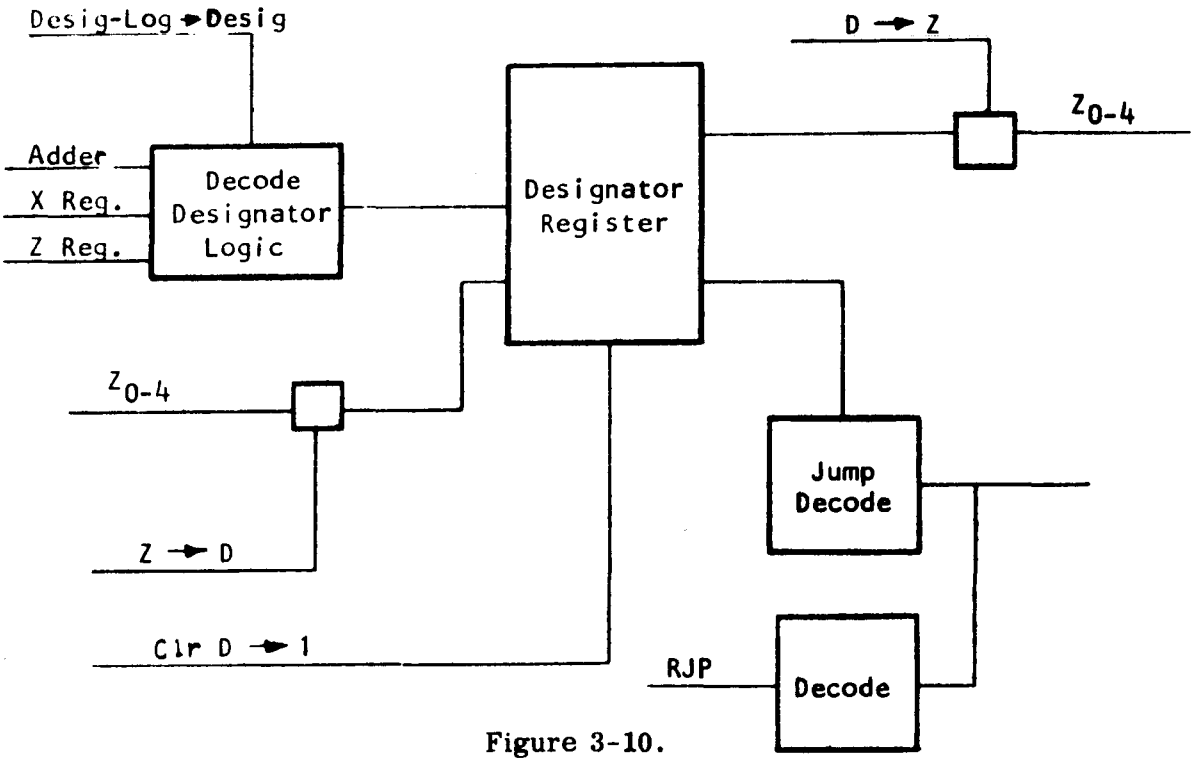


Figure 3-10.

B. CIRCUIT OPERATION

1. Five Bit Designator Register - This consists of NAND circuits A, B, C, D, E and five indicator driver circuits. The register is cleared to "zeroes" (the lights off) before gating the designator logic. The Overflow Designator is not cleared except by master clear or Enter Designator instruction. The register is cleared to "ones" (all lights on) before gating the Z Register.

2. Designator Decode Logic Gate - This consists of NAND circuits F, G, H, J, K, and U5.
   a) F11 (output of F NAND, pin 11) sets the Even Designator when the Adder Output is Positive and Even.

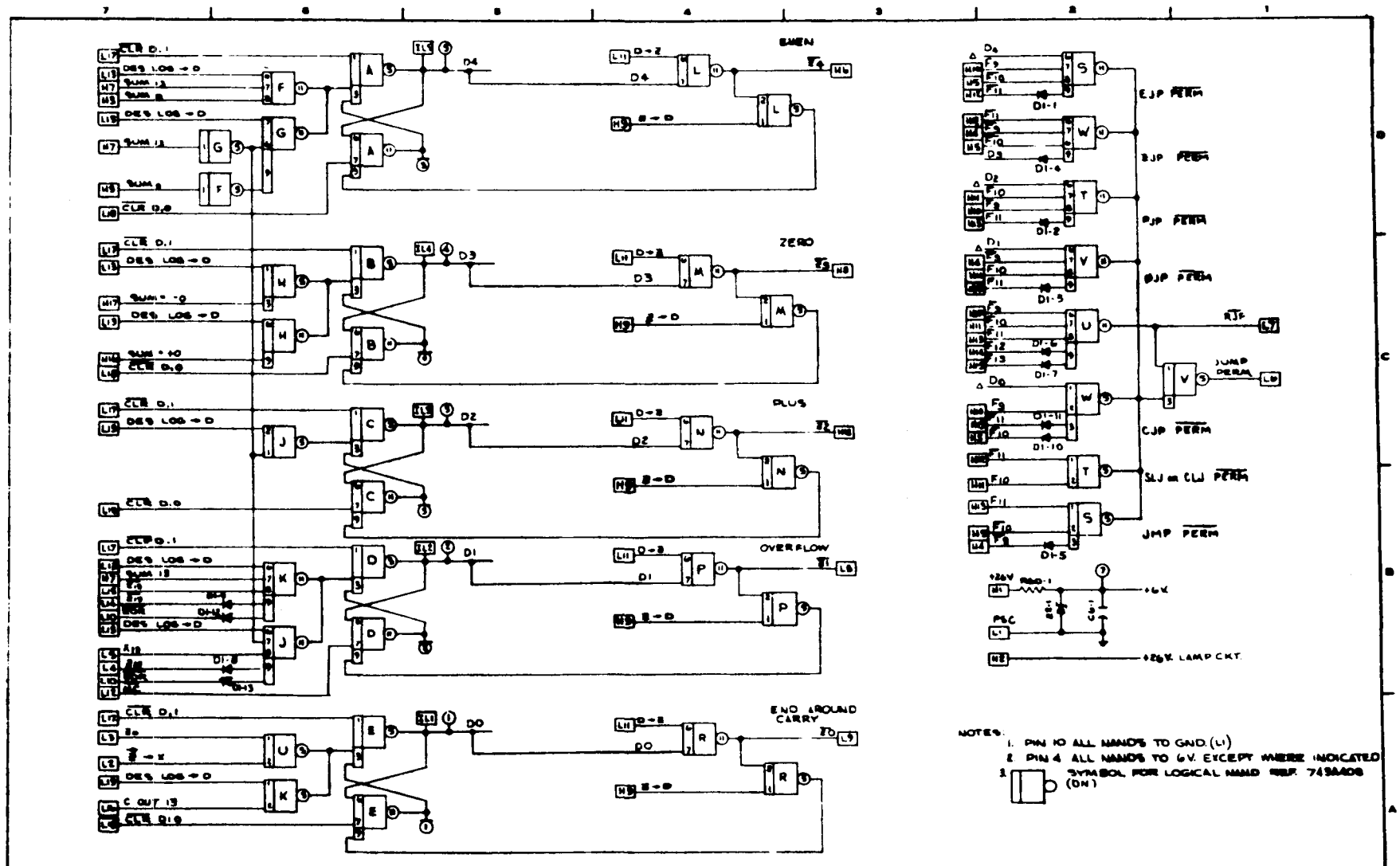
b) F5, G5, G11 set the Even Designator when the Adder Output is Negative and Even. (In reality Bit 13 and Bit 0 are compared, if they are the same, the number is even.)
c) H5 sets the Zero Designator (IL4) when the Adder Output is a negative zero.
d) H11 Sets the Zero Designator when the Adder Output is Positive Zero. The Decode Diodes of the NAND are located on the Bit Cards.
e) J5 Sets the Positive Designator when the Adder Output is Positive.
f) K11 Sets the Overflow Designator when X and Z are positive and Sum is Negative. It is inhibited on an EOR Instruction.
g) J11 Sets the Overflow Designator when X and Z are negative and the Sum is Positive. It is inhibited on an EOR Instruction.
h) K5 Sets the End Around Carry Designator when there is a Carry-Out on Bit Thirteen.
i) U5 Sets the End Around Carry Designator when a "One" is Shifted Off on a RSH Instruction.

3. Designator to Z Register Gate
   Consists of NAND L11, M11, N11, P11, R11
   Setting of Z register is accomplished by clamping the Output of the compliment side of the Flip-Flops.

4. Z Register to Designator Gate
   Consists of NAND L5, M5, N5, P5, R5
   Setting of the Designators is accomplished by clearing them to "One's" and setting "Zero's" from the compliment side of the Z Register.

5. Jump permissive Decode
   Consists of NAND S, T, U11, V, W
   a) S11 decodes EJP Instruction and Even Designator
   b) W11 decodes ZJP Instruction and Zero Designator
   c) T11 decodes PJP Instruction and Positive Designator
   d) V11 decodes OJP Instruction and Overflow Designator
   e) W5 decodes CJP Instruction and End Around Carry Designator
   f) T5 decodes SLJ or CLJ Instruction
   g) S5 decodes JMP Instruction
   h) U11 decodes RJP Instruction
   i) V5 is used as a Logic Inverter

6. Return Jump Decode
   Consists of NAND U11.
   This also forms part of Jump Permissive Decode



WESTINGHOUSE ELECTRIC CORPORATION

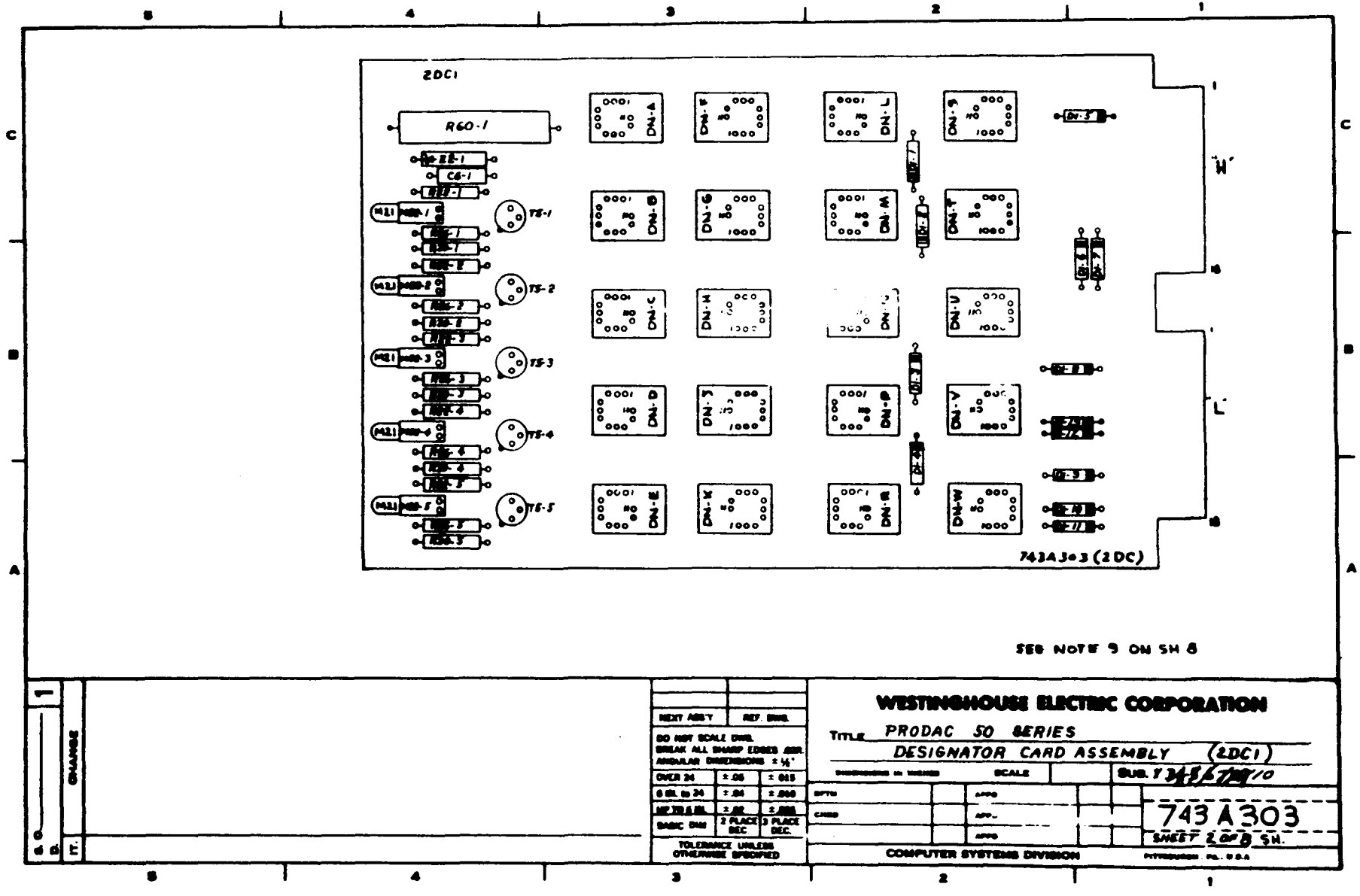
TITLE PRODAC 50 SERIES

DESIGNATOR CARD BOARD SCHEMATIC (2DC)

743A303

SH 7 OF 8 SH

COMPUTER SYSTEMS DIVISION


2DC1
R60-1
C6-1
TS-1
TS-2
TS-3
TS-4
TS-5
743A303 (2DC)
SEE NOTE 9 ON SH 8
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES
DESIGNATOR CARD ASSEMBLY (2DC1)
743A303
SHEET 2 OF 8 SH.
COMPUTER SYSTEMS DIVISION

EXTERNAL INTERRUPT 3EI2

A. GENERAL DESCRIPTION

The EI card is the principal module of the interrupt subsystem. This subsystem is the means of gaining the attention of the computer from either a contact closure or a transistor switch. In response to a contact closure, a temporary core buffer is set, and a "Hit" signal is sent to the interrupt scan card. The computer recognizes the presence of an interrupt and (if not running under interrupt lockout) begins interrogating the interrupt cores. When a core which has been set previously is interrogated, a response voltage is generated, and the computer accesses the appropriate location in core memory corresponding to that interrupt.

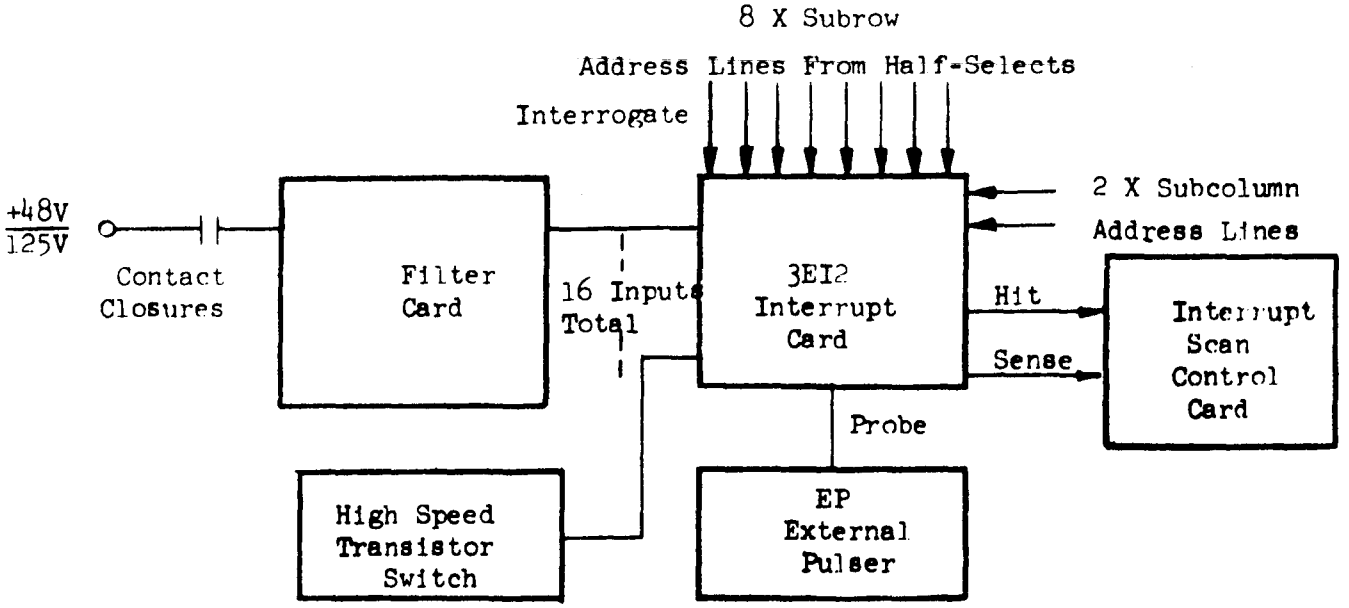


Figure 3-11. Application of EI Interrupt Card

The EI accepts up to 16 interrupt inputs. A maximum of four EI cards can be used per system. Either a filtered contact closure from the process or a high-speed transistor-driven signal from peripheral units and/or other computers can set interrupts. An interrupt core is set when the input voltage exceeds the threshold level of the interrupt circuit and a synchronizing probe pulse is present from an external pulser card. This probe pulse is generated each instruction Sequence III and is inhibited during interrupt scan to prevent simultaneous setting and resetting of interrupt cores. A hit pulse occurs when a core is set and indicates that an interrupt scan should begin if lockout is not set. During interrupt scan, eight X subrow line and two X subcolumn lines from the HS half-select cards route interrogate pulses sequentially to each interrupt core. When an interrogate pulse is passed through a core which has been set, a response voltage called a sense pulse occurs. The address in the S register when the sense pulse occurs indicates the core memory location containing the next instruction.

B. CIRCUIT OPERATION

1. Circuit Specification

Interrupts are to be set from filtered contact closures to 48 volts ±10%. The filtered interrupt rate is 20 per second. Interrupts can be set from a transistor-driven circuit powered from the unregulated (26 volt ± 4 volt) main frame power supply.

Probe pulses occurring once per instruction are typically 4 microseconds in duration. The maximum rate would be 4 microseconds every 9 microseconds. Probe pulse amplitude variation is 14.5 to 17.2 volts worse case.

Interrogate pulses occur every 1.5 microseconds with a 0.9 microsecond duration. Peak current is 0.4 ampere and is supplied through the half-select matrix.

The hit and sense pulse load on the El card is 150 ohms. Amplitude should exceed 1.5 volts for at least 150 nanoseconds.

All circuits should be capable of floating with respect to central processor ground.

2. Circuit Description

Card Block Diagram (Figure 3-12)

This module contains 16 interrupt input circuits. There are five commons available, making three groups of four circuits and two groups of two circuits.

The basic interrupt circuit is shown in Figure 3-13.

An input voltage charges the 0.5 microfarad capacitor. The voltage on the low side of the 0.05 microfarad coupling capacitor follows if the input voltage rise is sufficiently fast. When a threshold determined by the zener breakdown voltage of the Z10 zener and the base emitter drop of the T16 transistor is exceeded at a level of 17.6 to 19.4 volts, the transistor turns on and allows the next probe pulse to be applied across the Shockley diode (S3). The sum of the probe voltage and the voltage on the input capacitor appears across the S3 Shockley diode and should be sufficient to cause the Shockley to fire. The Shockley's firing dumps charge from the input capacitor through the core and saturates it in one direction. This firing path for the Shockley, which is initially through the probe transformer, transfers to the D4 diode, which is a low impedance to ground.

The response voltage when the core is set is the hit pulse. When the core is interrogated, the response voltage called the sense pulse is generated.

To guarantee that the core will be set once and only once for each contact closure (or applied input voltage), the 0.05 microfarad capacitor is charged. It is selected to be one-tenth the filter capacitor so that the input will not be reset to a point where the input voltage can once again produce a voltage excursion sufficient to set the core.

The method chosen for applying the probe pulse only when the input voltage exceeds a threshold minimizes the possibility of the Shockley's undergoing rate firing at too low an input voltage level. Circuit waveforms are shown in Figure 3-14.

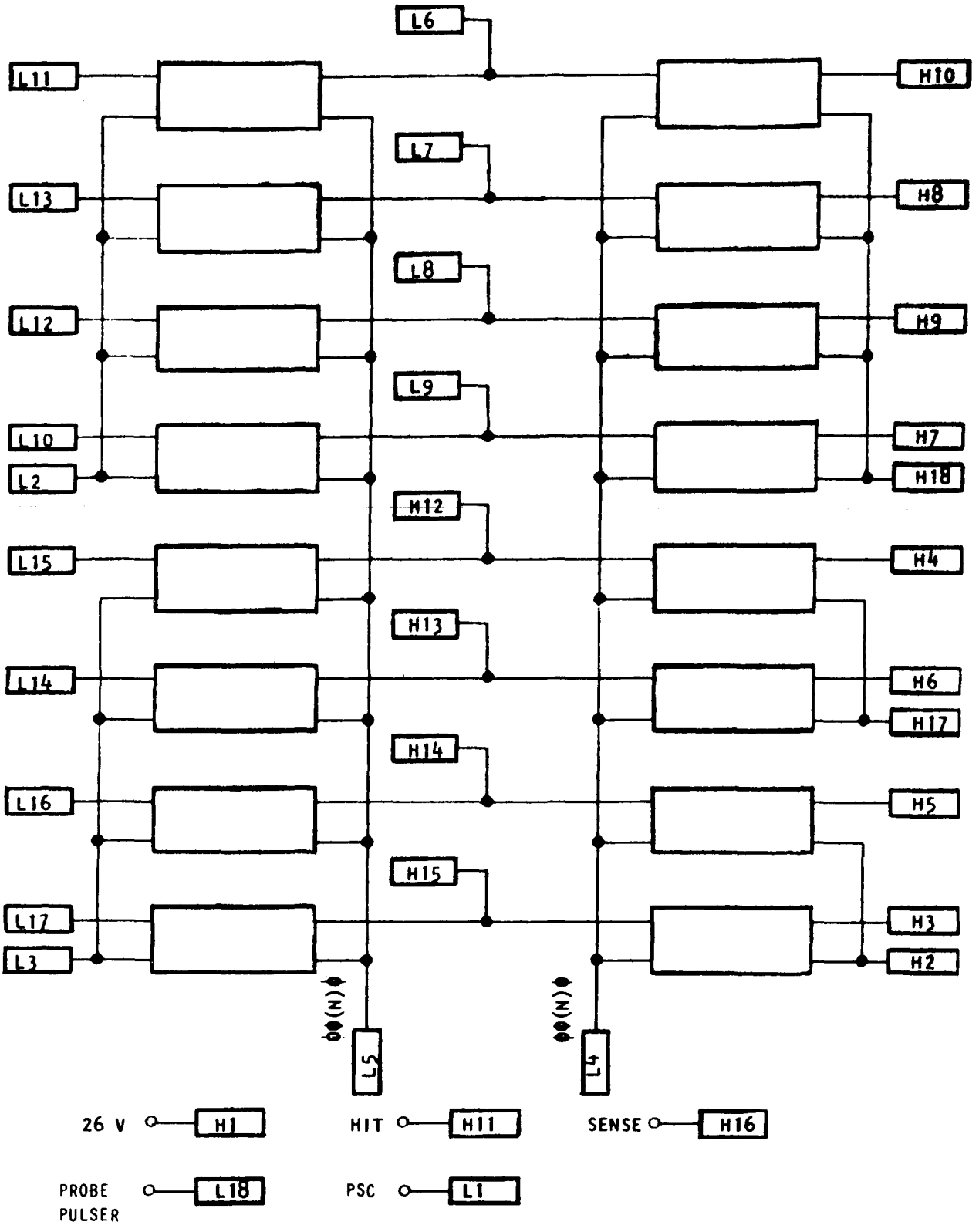


Figure 3-12. EI Card Block Diagram

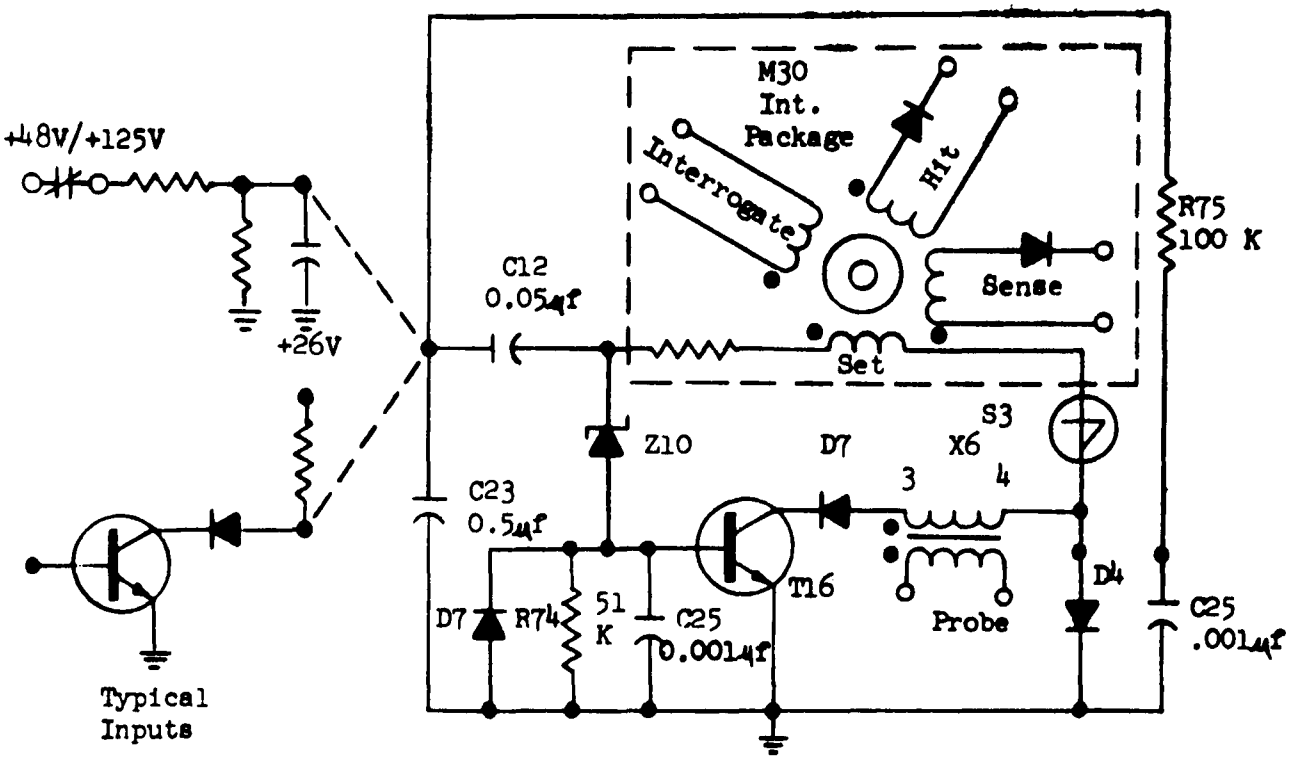


Figure 3-13. Basic Interrupt CKT

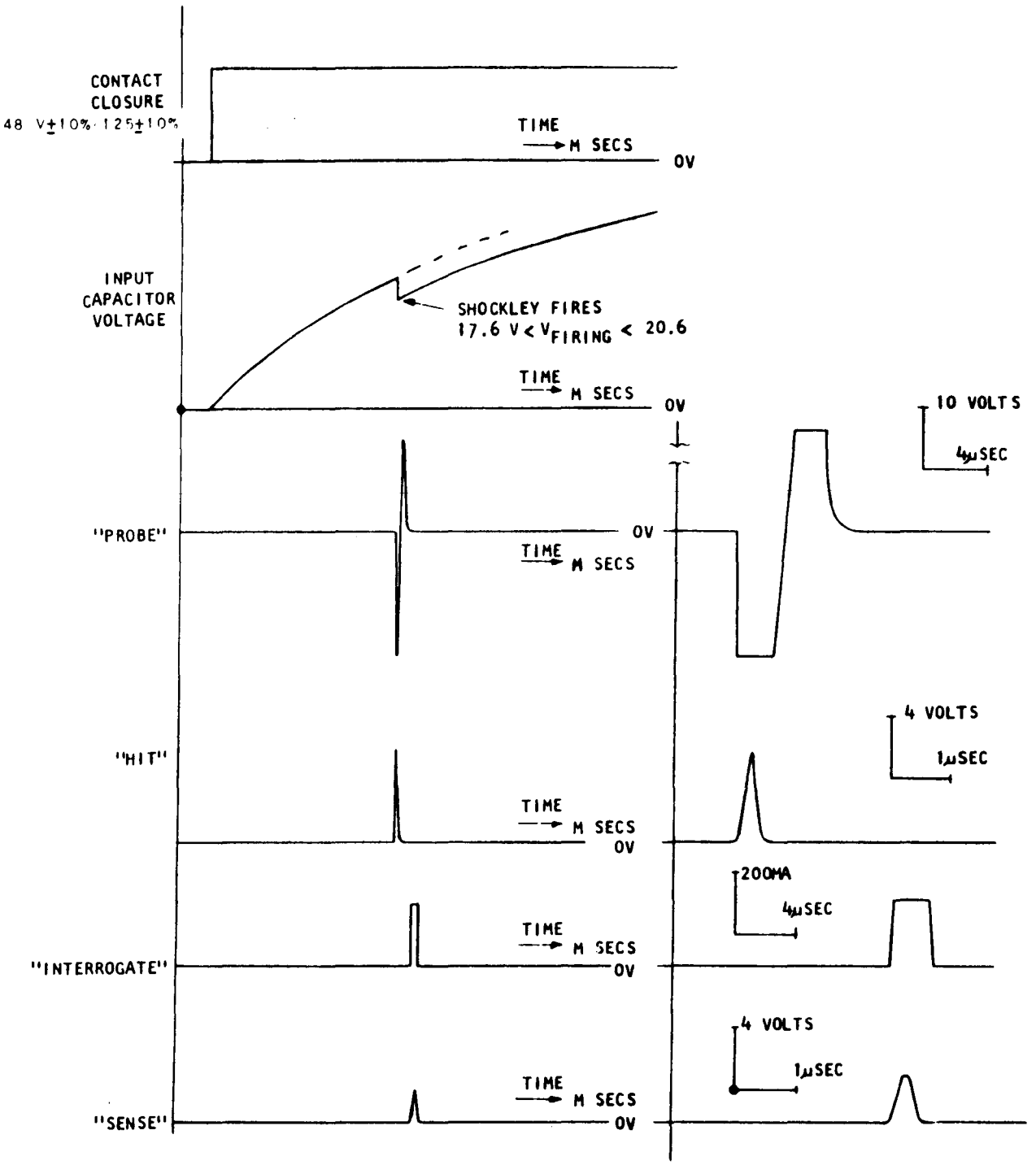

CONTACT
CLOSURE
48 V±10% 125±10%
TIME
M SECS
0V
INPUT
CAPACITOR
VOLTAGE
SHOCKLEY FIRES
17.6 V < V FIRING < 20.6
TIME
M SECS
0V
10 VOLTS
4μSEC
"PROBE"
0V
TIME
M SECS
4 VOLTS
1μSEC
"HIT"
TIME
M SECS
0V
200MA
4μSEC
TIME
M SECS
"INTERROGATE"
0V
4 VOLTS
1μSEC
TIME
M SECS
"SENSE"
0V

Figure 3-14.

3. Interrupt Core Package (Figure 3-15)

This cordwood package contains four buffer cores for the EI interrupt board.

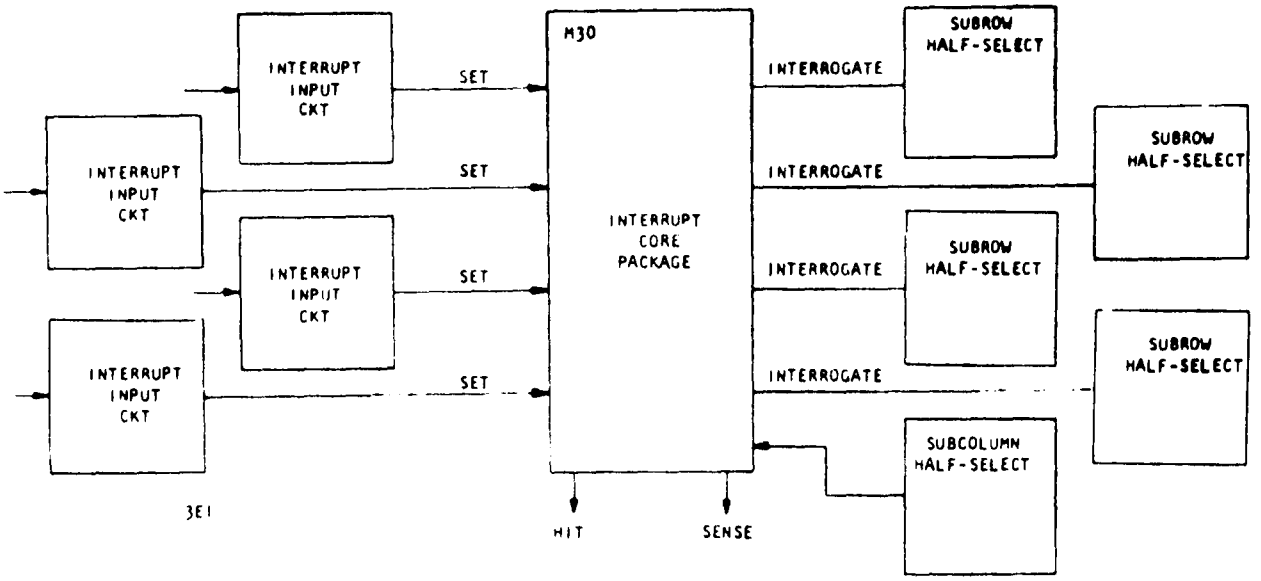


Figure 3-15. Interrupt Core Package

The storage elements within the package are ferrite cores each of which has four windings: A set winding, a hit winding, an interrogate winding, and a sense winding. Whenever an interrupt input signal goes positive, a probe pulse from the computer will cause the 4 layer diode in the interrupt circuit to discharge a capacitor to set the core. A pulse of positive polarity is developed across the hit winding to give an indication that a core has been set and an interrupt scan should be begun. The scan consists of interrogate pulses generated in series. When the core which was previously set is interrogated a positive pulse appears across the sense winding. The sense pulse stops the scan and the computer goes to the core address as determined by the address last used in the interrupt scan.

The interrupt input circuit provides approximately 0.6 ampere through the set winding. The interrogate pulse has a duration of 0.9 microsecond at 0.9 ampere. Hit and sense pulse amplitudes are in the range of 2 to 6 volts.

a) Circuit Description (Figure 3-16)

The square loop core provides the memory and isolation required for the external interrupt system. The output pulse from the interrupt circuit is applied across winding 7-8 through resistor R5, and drives the core to its positive saturation state. A response voltage ("Hit") across winding 1-2 results from the cores being driven to a new saturation state. The "Hit" pulse signals the computer to start a sequential interrogation of all cores.

When the interrogate current pulse is applied to winding 5-6 through the half-select switches, the core is driven back to its negative saturation state. The resulting flux change induces a signal across the "sense" winding 4-3. In the absence of an interrupt input the core is already in its negative saturation state so that very little flux change is produced by an interrogate pulse, and a negligible voltage is induced across the sense winding. Diodes D4-1 and D4-3 provide isolation between the "hit" and "sense" pulses.

b) The duration of the "set" pulse is approximately 2 microseconds. The "interrogate" pulses are 0.9 microsecond long.

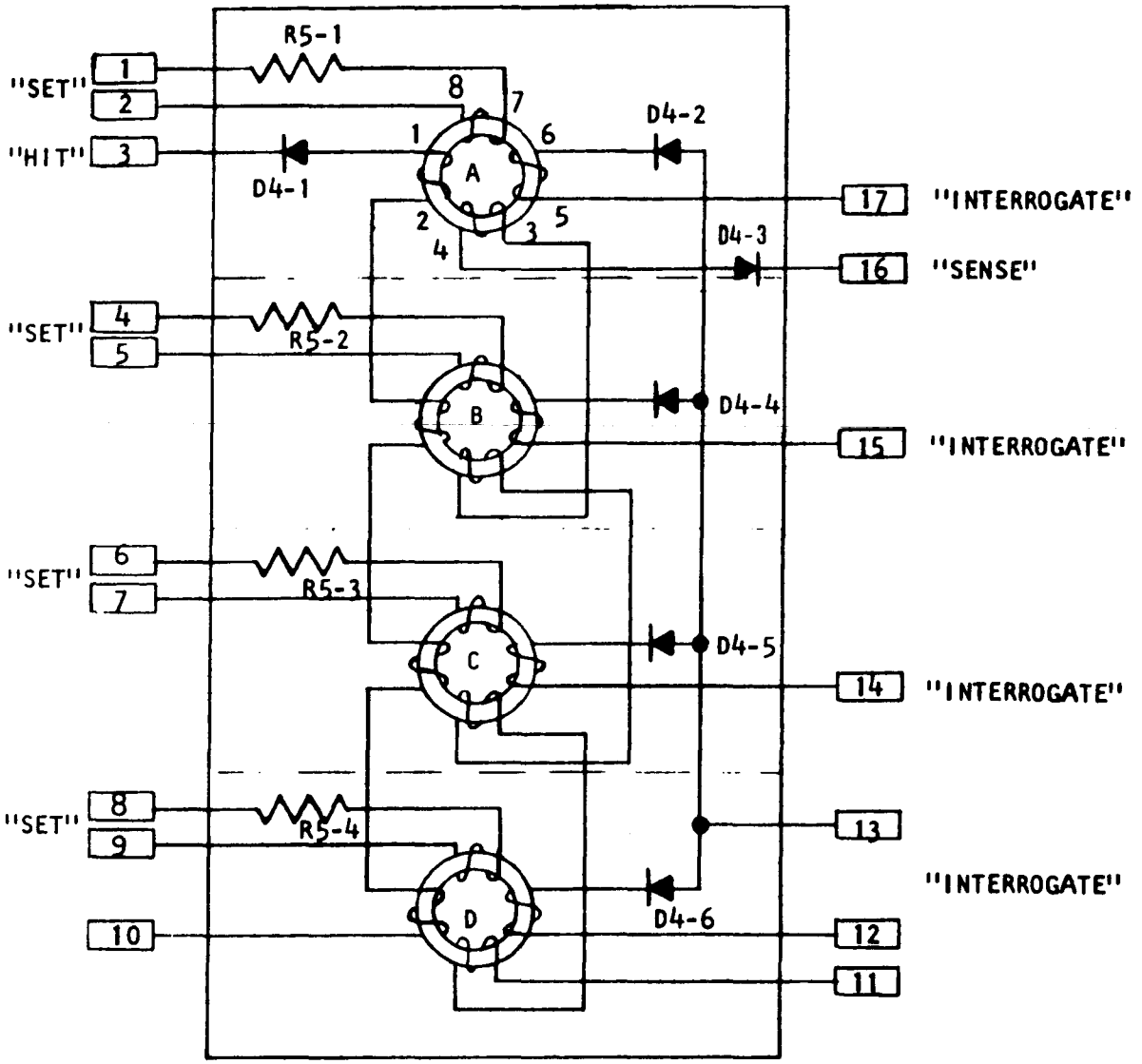
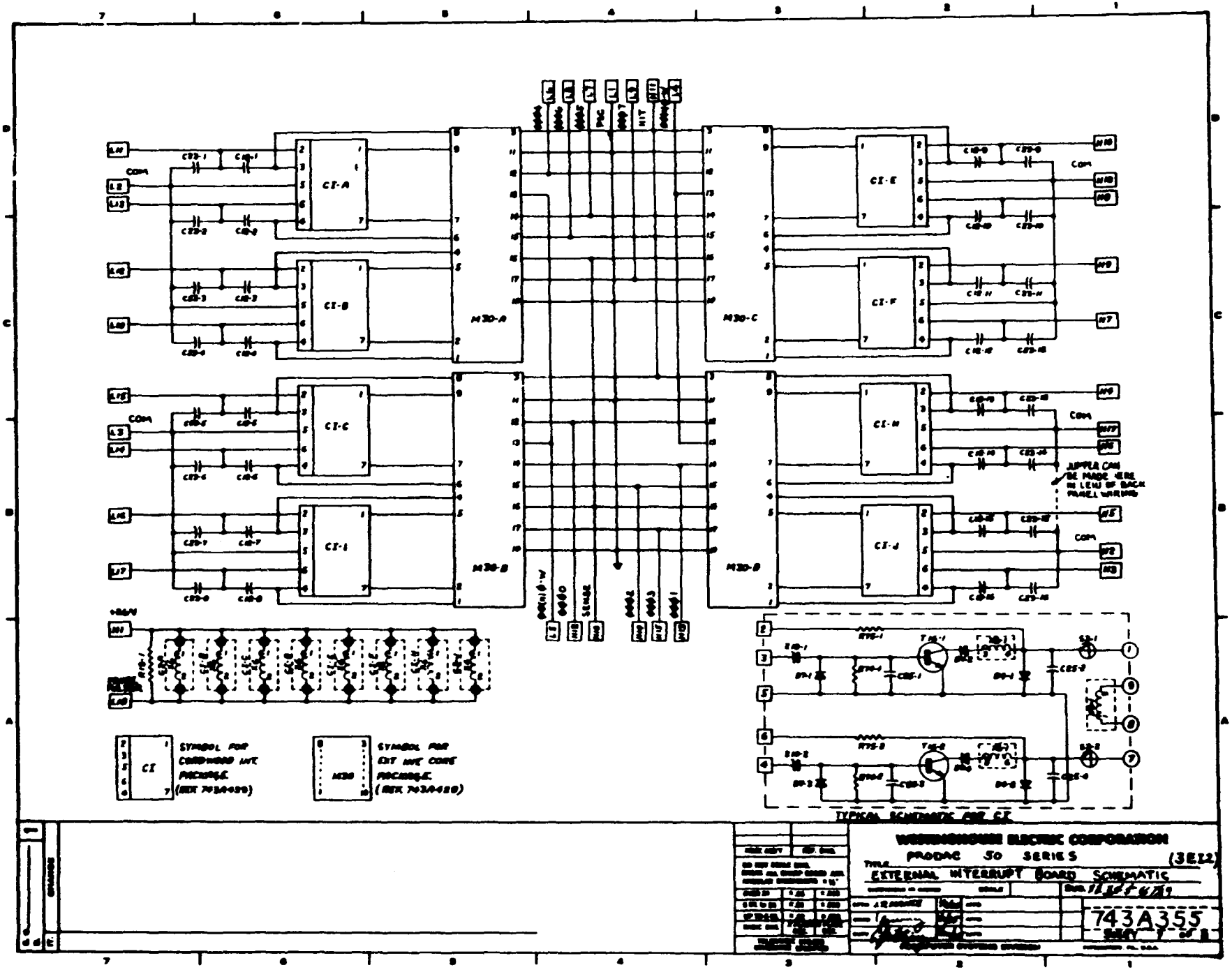
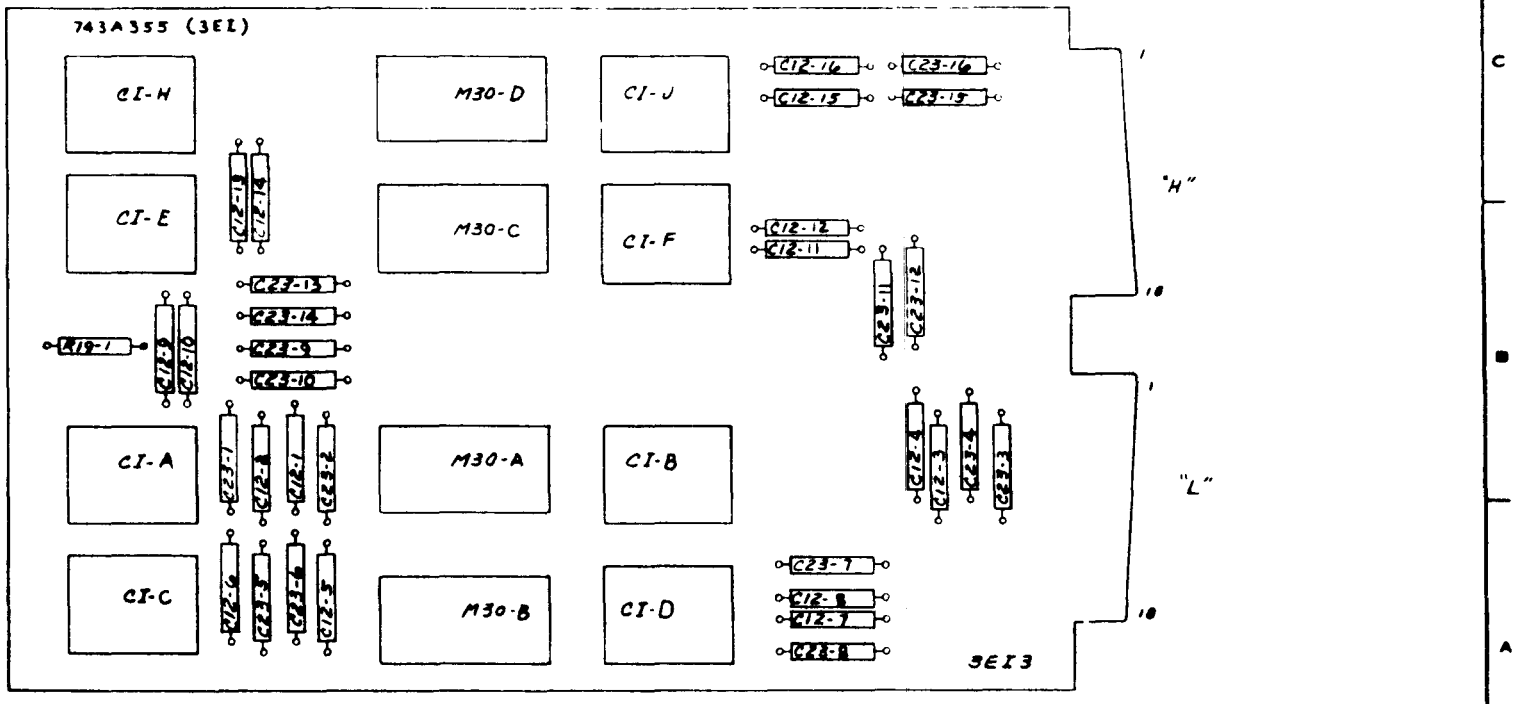

R5-1
"SET"
1
2
"HIT"
3
8
7
1
6
A
2
5
3
4
D4-1
D4-2
D4-3
17
"INTERROGATE"
16
"SENSE"
"SET"
4
5
R5-2
B
D4-4
15
"INTERROGATE"
"SET"
6
7
R5-3
C
D4-5
14
"INTERROGATE"
"SET"
8
9
R5-4
D
D4-6
13
"INTERROGATE"
10
12
11

Figure 3-16.


CI-A
CI-B
CI-C
CI-I
CI-E
CI-F
CI-H
CI-J
M30-A
M30-B
M30-C
M30-D
COM
SYMBOL FOR CARDWARE INT. PRIORITY. (REF 7034-020)
SYMBOL FOR EXT INT CODE PRIORITY. (REF 7034-020)
TYPICAL SCHEMATIC FOR CI
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
(3E12)
EXTERNAL INTERRUPT BOARD SCHEMATIC
743A355



SEE NOTE 9 SH. 8

NEXT ASS'Y		REF DWG	
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN. to 24	± .04	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM	2 PLACE DEC.	3 PLACE DEC.	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

1			
S.O.	CHANGE		
IT.			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC "50" SERIES (3EI2)

EXTERNAL INTERRUPT CARD ASSEMBLY

DIMENSIONS IN INCHES | SCALE | SUB. X 2 3 4 5 6 7 8 9

DRTN		APPD	
CHKD		APPD	
SUPV		APPD	

743A355

SH. 2 OF 8

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA U.S.A.

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EXTERNAL PULSER CARD 1EP3/2EP1

A. GENERAL DESCRIPTION

This card is used to perform a number of operations, namely, Channel, Word, Probe, and Interrogate pulse generation. Two of these operations are performed on each card.

See Figure 3-17 for Block Diagram. The External Pulser receives logic levels and timing pulses from the main-frame control circuitry cards. Pulse energy is supplied to the:

a) External Interrupt pulse transformers,
b) External Interrupt Interrogate matrix,
c) Word peripheral matrix, and
d) Channel peripheral matrix.

B. CIRCUIT OPERATION

1. Circuit Specifications

Logic levels are intended to feed pins H15, H17, and H13. These signals ground to select outputs and hold down 1.4 ma maximum. The "one" signal will be clamped at 2 volts maximum. The timing signals are brought in through capacitive coupled inputs H14 and H16 and also ground to select the outputs. They must hold down 7.7 ma max. and block 7.15 volts in the "one" state. The timing signals are capacitive coupled to guarantee the outputs will not be full "on" continuously in case the inputs are held at ground. The output signal level is intended to be a regulated 18 volt pulse with 400 ma of current limit.

2. Circuit Description

The card block diagram of Figure 3-18 shows the two applications of the External Pulser card. There are two pulser circuits on each card and there are two external pulser cards in the system. The first card contains the interrogate pulser and four of its eight associated half-select transformers. The second card contains the remaining four half-select transformers for the interrogate pulser, the probe pulser, and the channel pulser with all eight of its half-select transformers.

Each pulser circuit consists of an OR gate and an inverting stage which drives the output transistor.

The schematic of the external pulser is shown on Drawing 743A308. The circuit operates in the following way. When all input diodes have a "1" signal, transistor T1-1 is saturated providing base drive for transistor T14-1. Transistor T2-1 is, therefore, blocked. When all input diodes are grounded, transistors T1-1 and T14-1 block and the output transistor T2-1 conducts. The base voltage of T2-1 is clamped, which prevents the transistor from saturating. Transistor T2-1 therefore acts as a current source, the current being adjustable by potentiometer M11-1. The output voltage at the collector is determined by the 18 V zener diode Z13-1 and D4-3 in series with it. Zener diode Z12-1 serves to clamp any inductive flyback voltage. The maximum time duration for which the output transistor can conduct is limited by the time constant of the capacitive coupled input circuit. Any number of input circuits can be connected to the pulser. There are two input circuits for the probe and interrogate pulsers. The word and channel pulsers have three input circuits each.

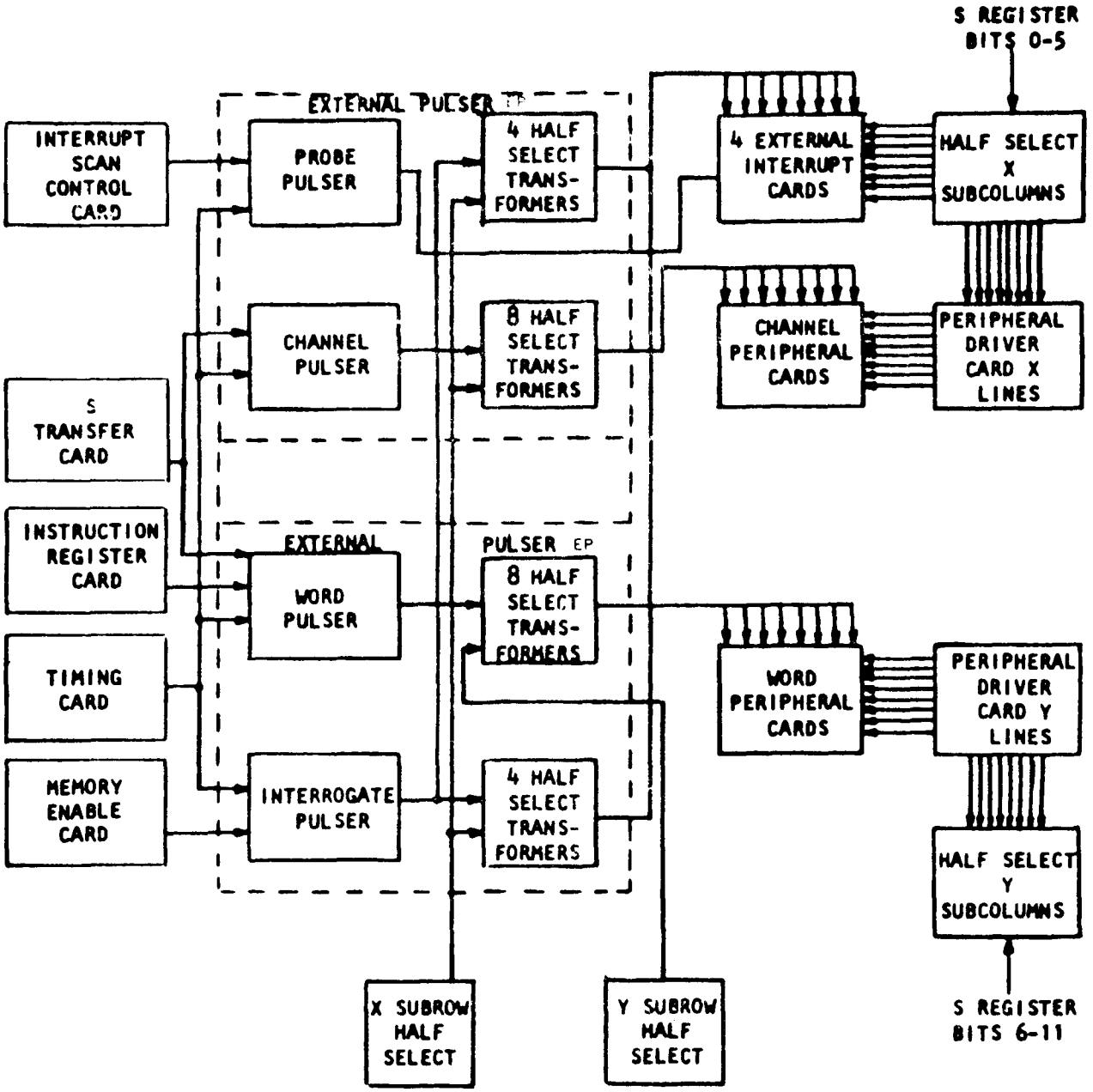

S REGISTER BITS 0-5
EXTERNAL PULSER TP
INTERRUPT SCAN CONTROL CARD
PROBE PULSER
4 HALF SELECT TRANS-FORMERS
4 EXTERNAL INTERRUPT CARDS
HALF SELECT X SUBCOLUMNS
CHANNEL PULSER
8 HALF SELECT TRANS-FORMERS
CHANNEL PERIPHERAL CARDS
PERIPHERAL DRIVER CARD X LINES
S TRANSFER CARD
INSTRUCTION REGISTER CARD
EXTERNAL
PULSER EP
WORD PULSER
8 HALF SELECT TRANS-FORMERS
TIMING CARD
WORD PERIPHERAL CARDS
PERIPHERAL DRIVER CARD Y LINES
MEMORY ENABLE CARD
INTERROGATE PULSER
4 HALF SELECT TRANS-FORMERS
HALF SELECT Y SUBCOLUMNS
X SUBROW HALF SELECT
Y SUBROW HALF SELECT
S REGISTER BITS 6-11

Figure 3-17.

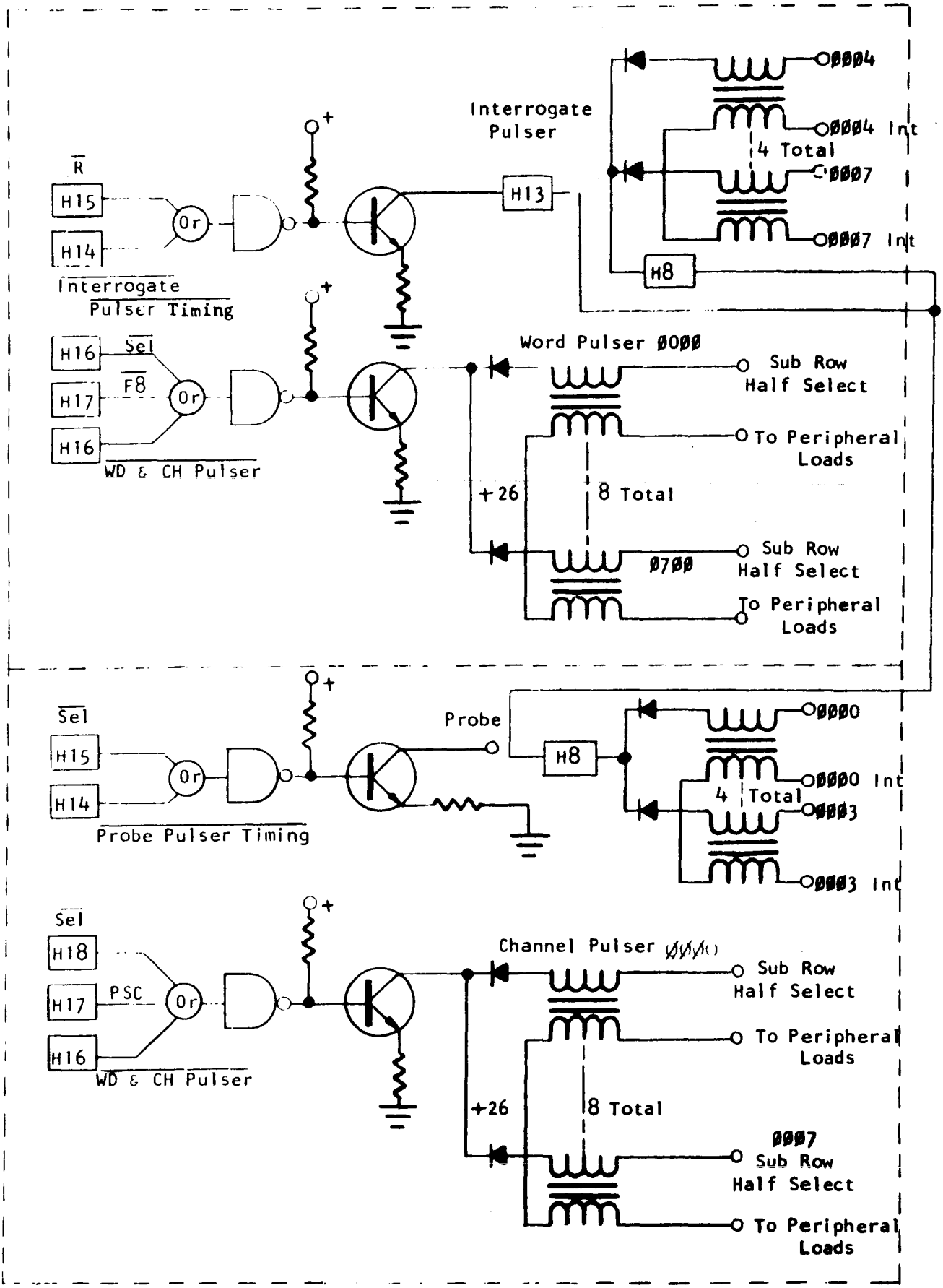
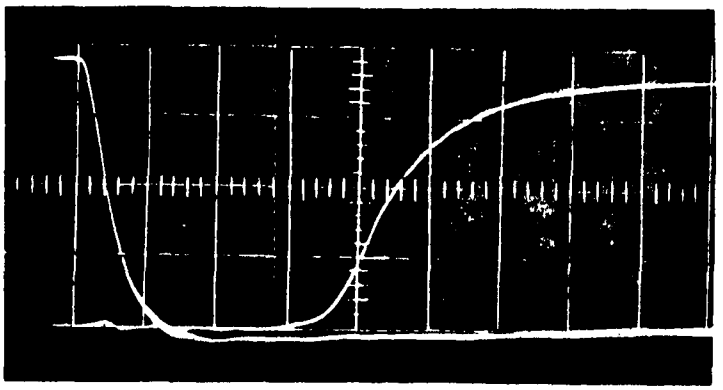

Interrogate Pulser
R
H15
H14
Or
Interrogate Pulser Timing
H13
H8
0004
0004 Int
4 Total
0007
0007 Int
H16
Sel
H17
F8
H16
WD & CH Pulser
Word Pulser 0000
Sub Row Half Select
To Peripheral Loads
+26
8 Total
0700
Sub Row Half Select
To Peripheral Loads
Sel
H15
H14
Probe Pulser Timing
Probe
H8
0000
0000 Int
4 Total
0003
0003 Int
Sel
H18
H17
PSC
H16
WD & CH Pulser
Channel Pulser 0000
Sub Row Half Select
To Peripheral Loads
+26
8 Total
0007
Sub Row Half Select
To Peripheral Loads

Figure 3-18.

3. Timing

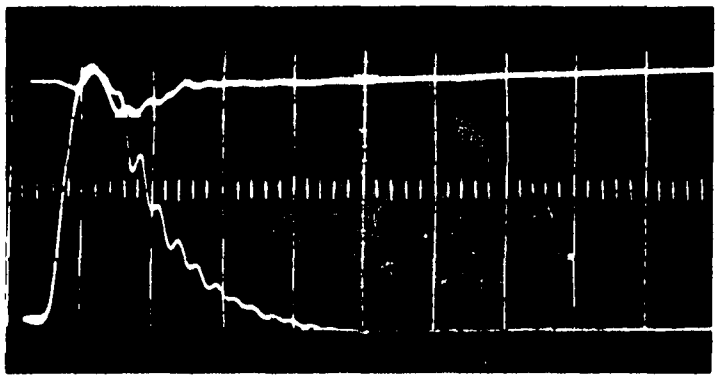
Waveforms in Figure 3-19 show the input to output delay for a 1 microsecond current pulse, typical of the interrogate pulse used in the interrogate scan. Also shown is the delay for a four microsecond voltage pulse as is used in the Word, Channel and Probe pulse applications.



Output Current Rise Time

Input Voltage 2V/cm
Output Current 100 mA/cm

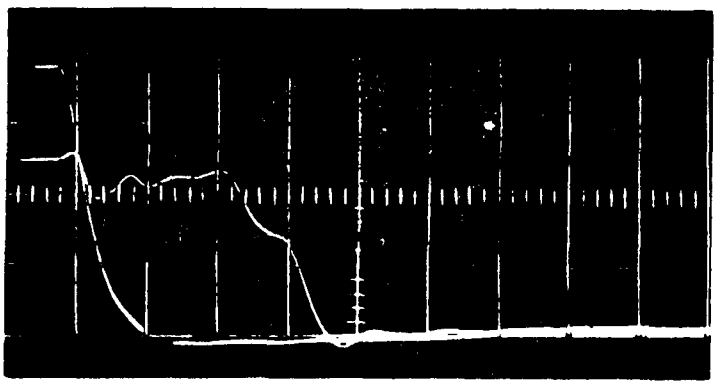
0·1 μs/cm



Output Current Fall Time

Input Voltage 2V/cm
Output Current 100 mA/cm

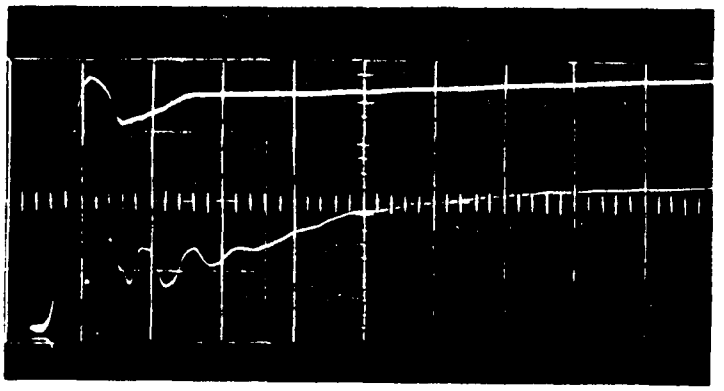
0·1 μs/cm



Output Voltage Fall Time

Input Voltage 2V/cm
Output Voltage (between collector and ground) 5V/cm

0·1 μs/cm

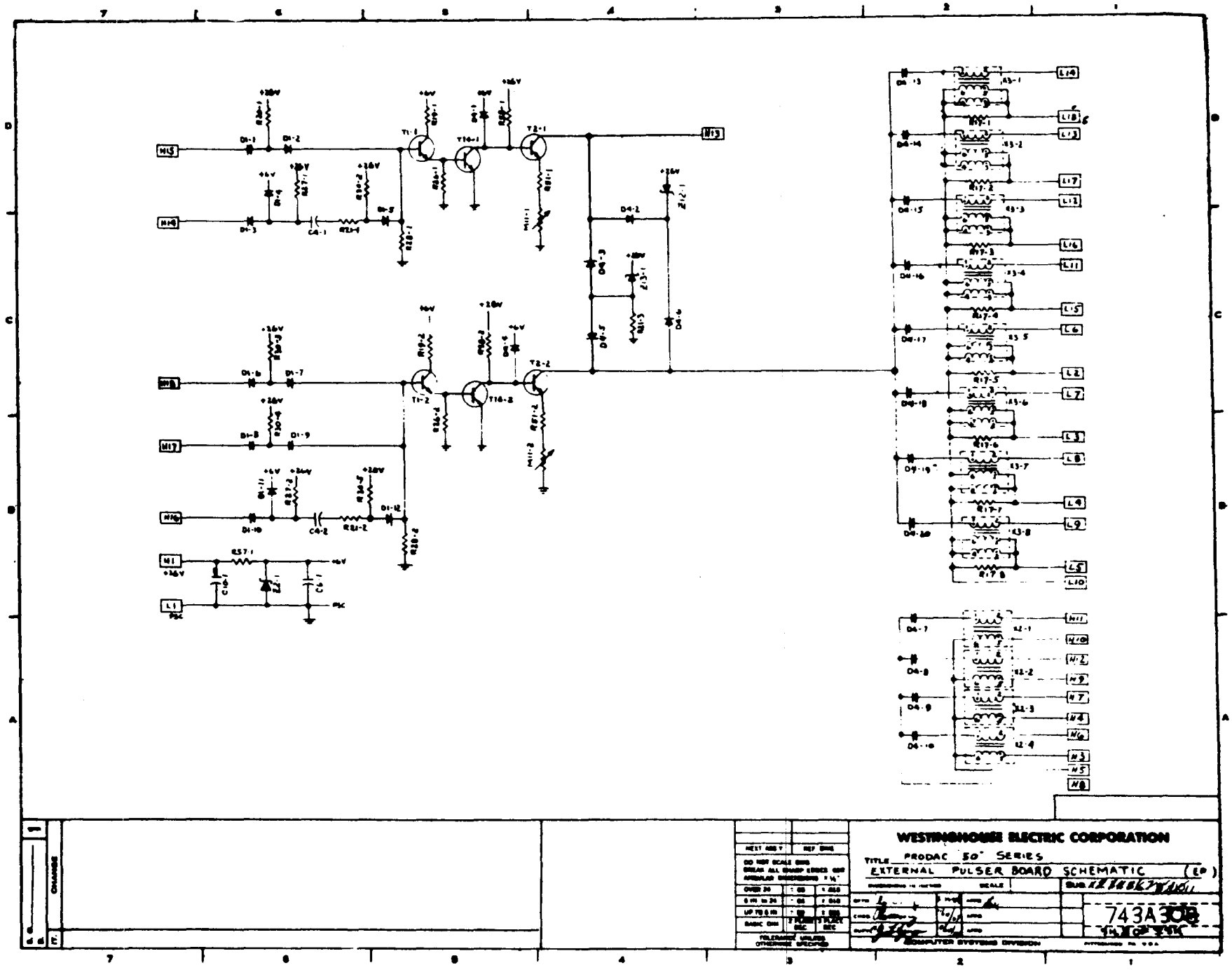


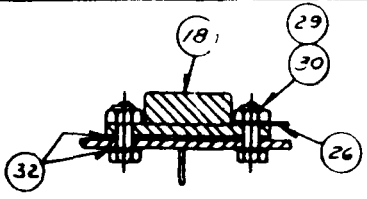
Output Voltage Rise Time

Input Voltage 2V/cm
Output Voltage (between collector and ground) 5V/cm

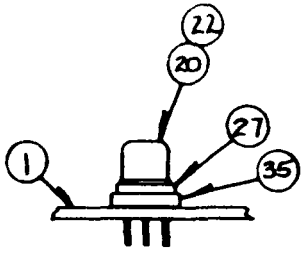
0·1 μs/cm

Figure 3-19.

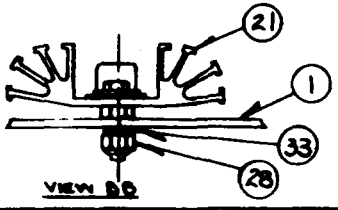

WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES
EXTERNAL PULSER BOARD SCHEMATIC (EP)
743A308



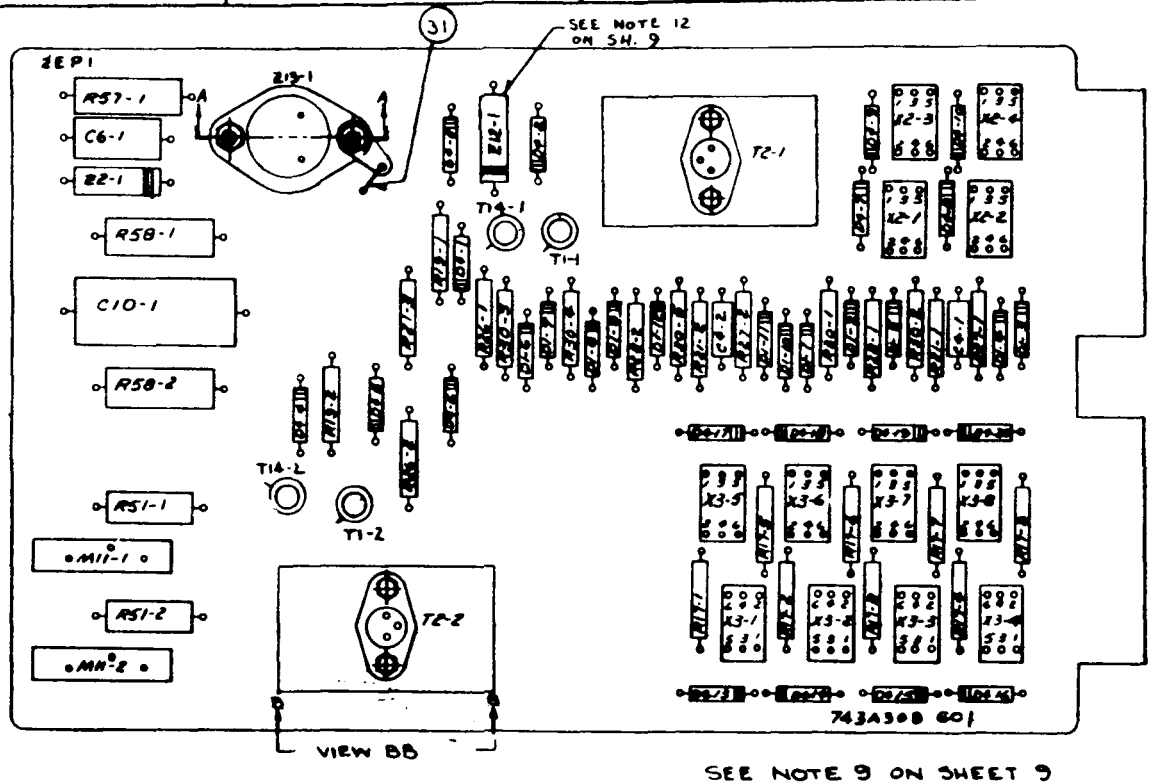
SECTION A-A



DETAILED ASSEMBLY OF T1 & T14 TRANSISTORS TO BOARD



VIEW BB



SEE NOTE 9 ON SHEET 9

ASSEMBLY FOR 2EP1 -GROUP 1 ONLY

NEXT ASSY		REF. DWG.		
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020R ANGULAR DIMENSIONS ± ½°				
OVER 24	± .06	± .015		
6 IN. to 24	± .04	± .010		
UP TO 6 IN.	± .02	± .005		
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.		
TOLERANCE UNLESS OTHERWISE SPECIFIED				

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC "50" SERIES (2EP1)

EXTERNAL PULSER CARD ASSEMBLY

SCALE

DRWN		APPD		SIZE	743A308
CHKD		APPD			SHEET 3 OF 5
SUPV		APPD			

COMPUTER SYSTEMS DIVISION

HALF SELECT CARD 2HS2

A. GENERAL DESCRIPTION

This circuit card is required to provide four subrow and four subcolumn half-select switches. The half-select switches are time-shared by the core memory subsystem., the interrupt subsystem and the input-output subsystem. The subrow half-select switches and the subcolumn half-select switches complete the current paths for the primary and secondary windings of the half-select transformers respectively.

The relationship of the half-select switches to the system is shown in the block diagrams (Figures 3-20, 3-21 and 3-22) that follow.

B. CIRCUIT OPERATION

1. Circuit Specifications

The input to the half-select switches is obtained by decoding the S-register outputs. The decoding is done by means of modified NAND modules. The output state of the subrow half-select switch has to handle 350 mA inductive load plus the transformer losses and damping current across the primary winding of the half-select transformers. The subcolumn half-select switch has to carry a 350 mA inductive load.

2. Circuit Description

This card contains 4 subrow and 4 subcolumn half-select switches. One pair of half-select switches have OR type inputs to allow direct access to core locations assigned to the Accumulator and Program Counter.

a) Subrow Description-Figure 3-23

Signals will be defined as a "1" (positive voltage) and a "0" (zero voltage).

When all four inputs to the circuit are logical "one" 's the output of the NAND gate is a logical "zero". Base drive is therefore provided for transistor T8-1 through resistor R24-1. Transistor T8-1 saturates, providing base drive for transistor T2-1. Transistor T2-1 conducts but is prevented from saturating.

When T2-1 is conducting, a current path is provided for the pulser circuit and therefore current flows through the half-select transformer. Switching delays through the subrow half-select switches are minimized by using a nonsaturating switch as the output stage. Diode D8-1 helps to reverse bias transistor T8-1. Diode D4-1 limits the flyback voltage across the transformer thereby protecting transistor T2-1 from destruction. Diode D7-2 prevents turn-on of transistor T2 when the flyback pulse occurs.

b) Subcolumn Description-Figure 3-24

When all four inputs to the circuit are logical "one" 's the output of the NAND gate is a logical "zero". Transistor T6-1 is, therefore, blocked, transistors T6-2 and T12-1 are conducting.

Diodes D4-8, D4-9, D4-X, D4-Y, D4-10, D4-11 and transistor T12-1 form an a-c switch, so that when transistor T12-1 is conducting, current can flow through the half-select transformer in either direction. When point B is negative with respect to point A, conduction takes place through D4-Y, D4-10, D4-11, T12-1 and D4-9. When point A is negative with respect to B, conduction takes place through D4-10, T12-1, D4-8 and D4-X.

Diode D4-7 is needed for limiting the flyback voltage. Diode D4-5 serves to facilitate fast turn-off of transistor T12-1. Diode D4-6 provides a path for discharging line capacitance. The capacitor C3-1 is needed to delay the turn-off of the subcolumn output transistor until the primary current through the half-select transformer decreases. This is necessary to prevent magnetizing current buildup.

3. Timing

The half-select switches are selected for a duration of 4.2 microseconds; and are unselected for 0.3 microseconds.

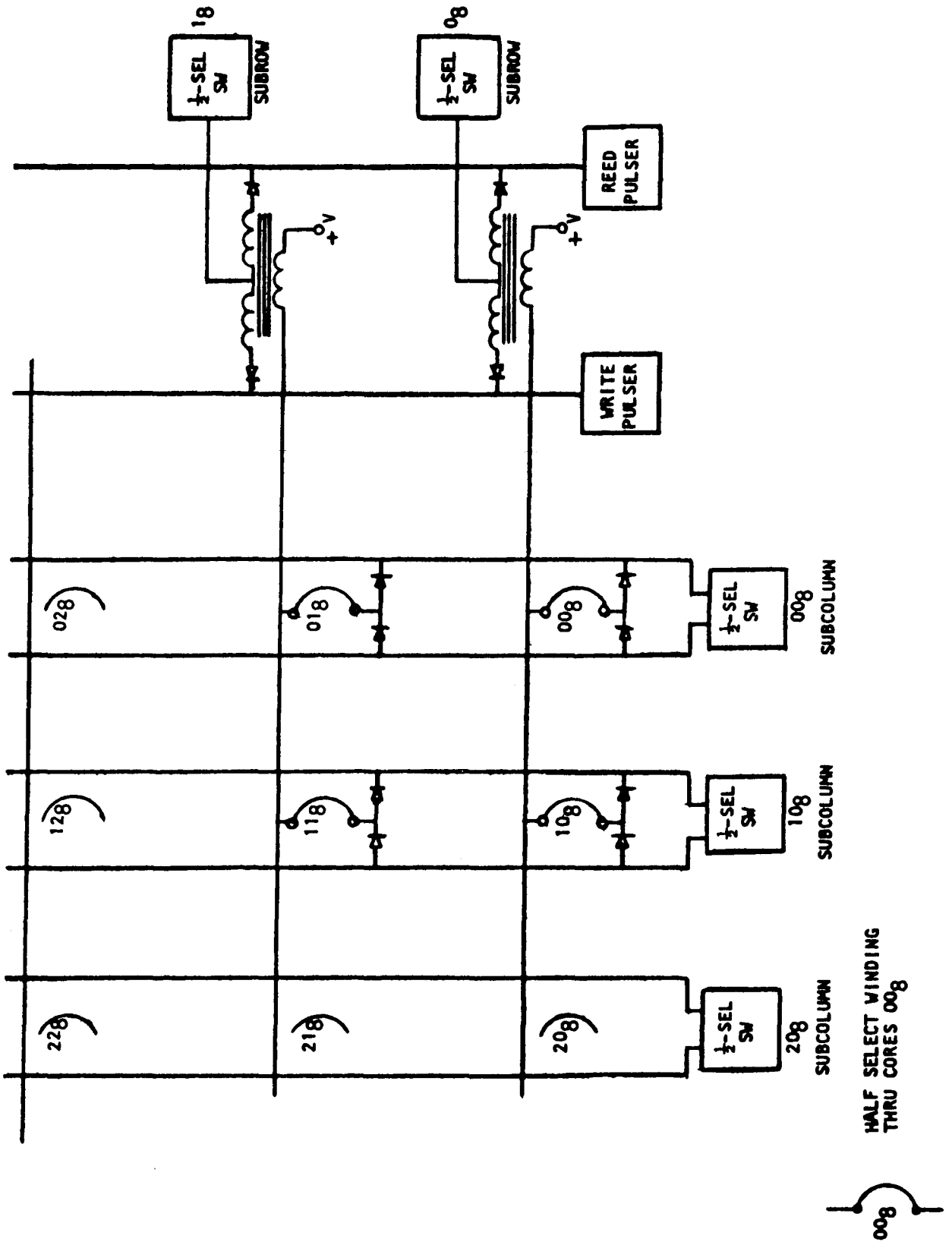


Figure 3-20. PRODAC Half-Select Scheme, Typical Partial View for Least-Significant Half-Address of One Stack

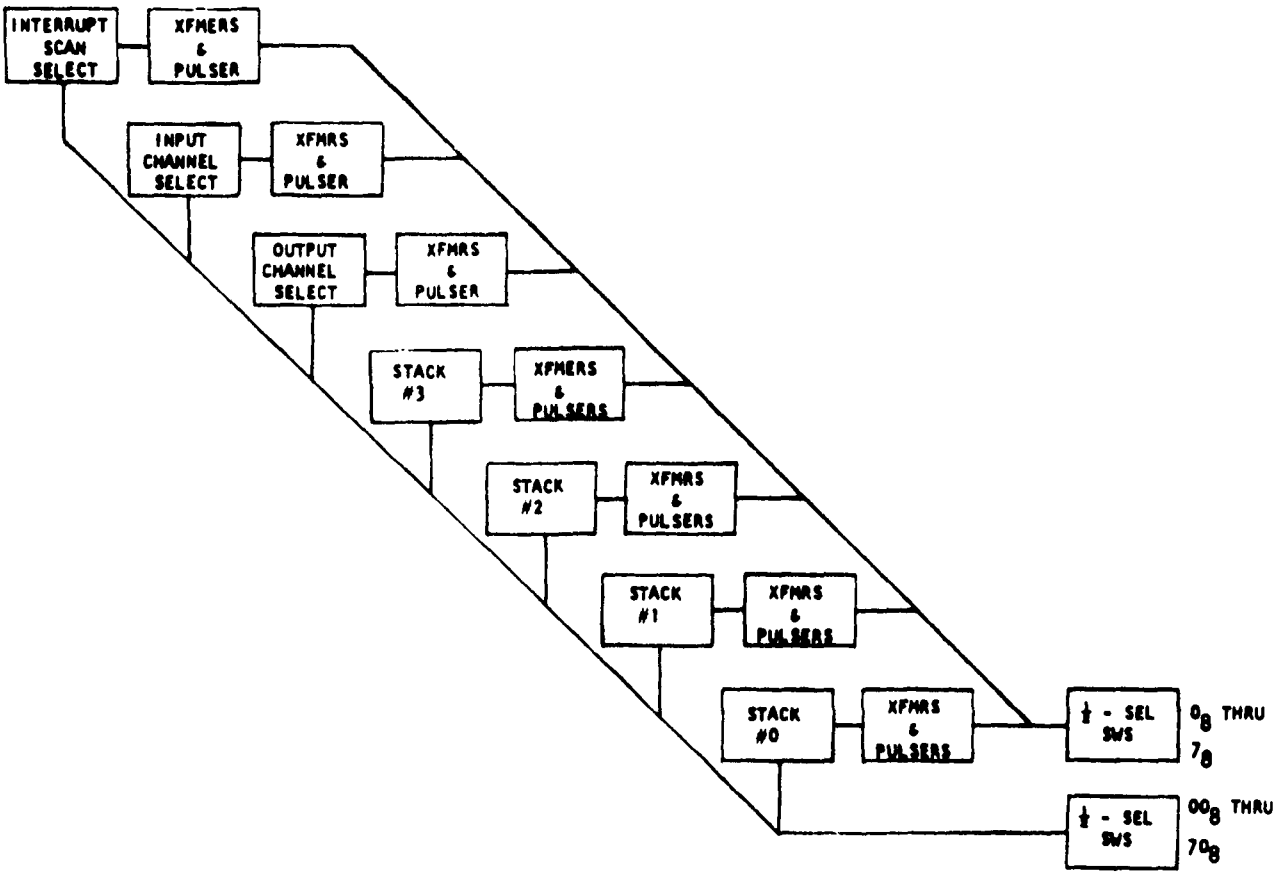


Figure 3-21. PRODAC Half-Select Scheme, Least Significant Half-Address, "X-Axis"

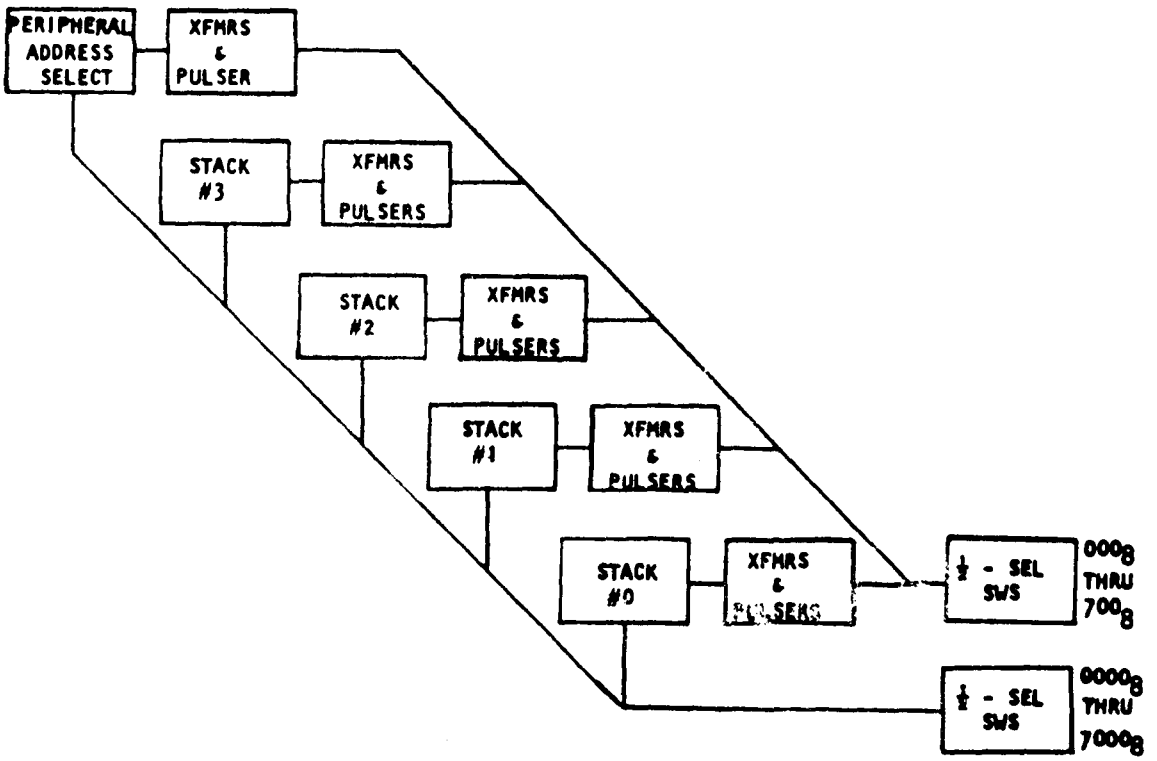


Figure 3-22. PRODAC Half-Select Scheme, Most Significant Half-Address, "Y-Axis"

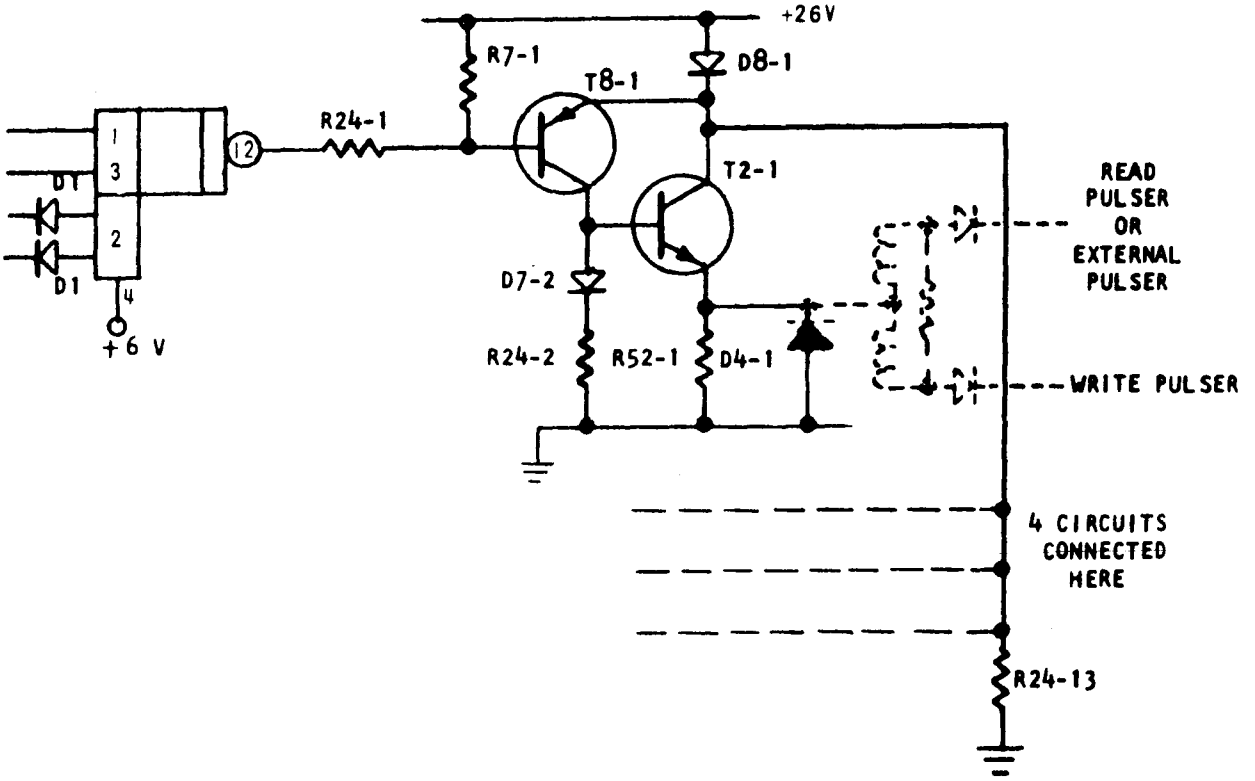


Figure 3-23. Subrow Half-Select Switch

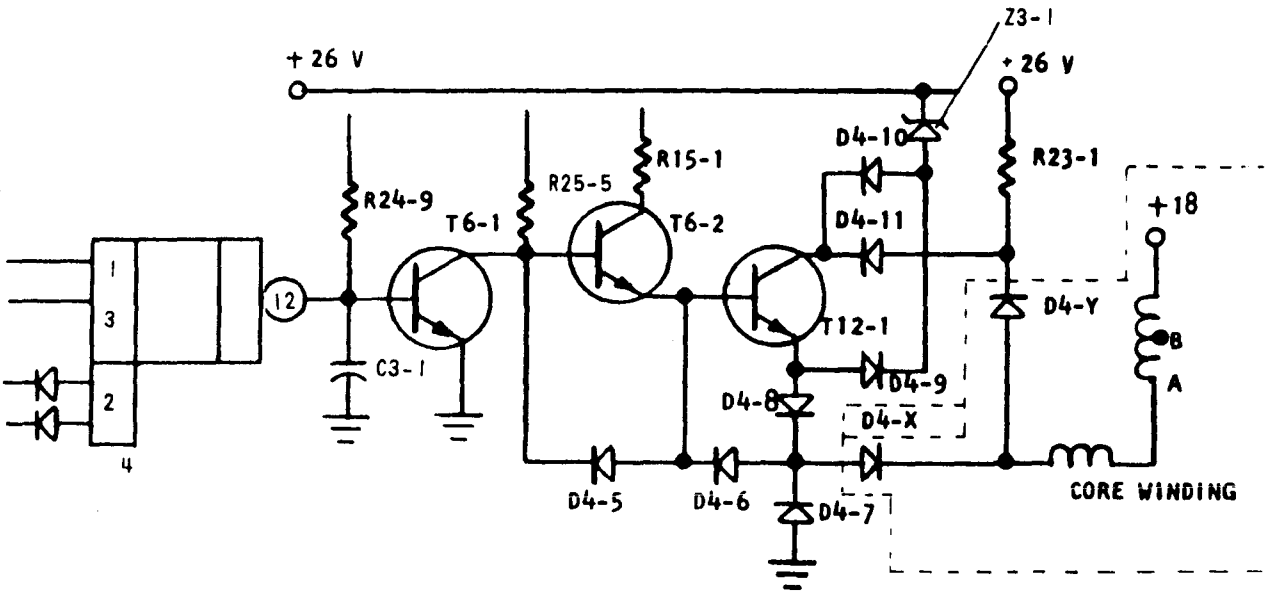
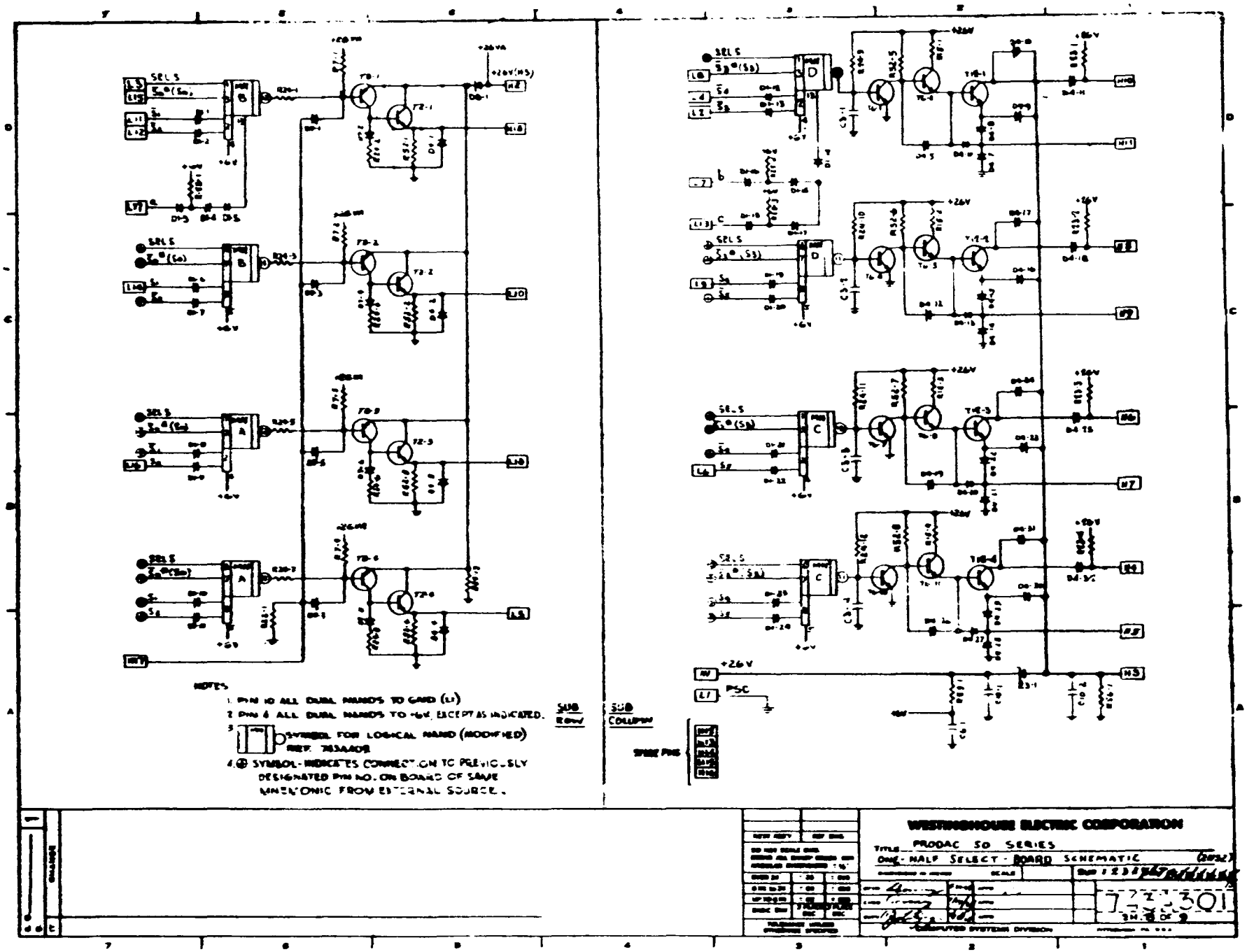
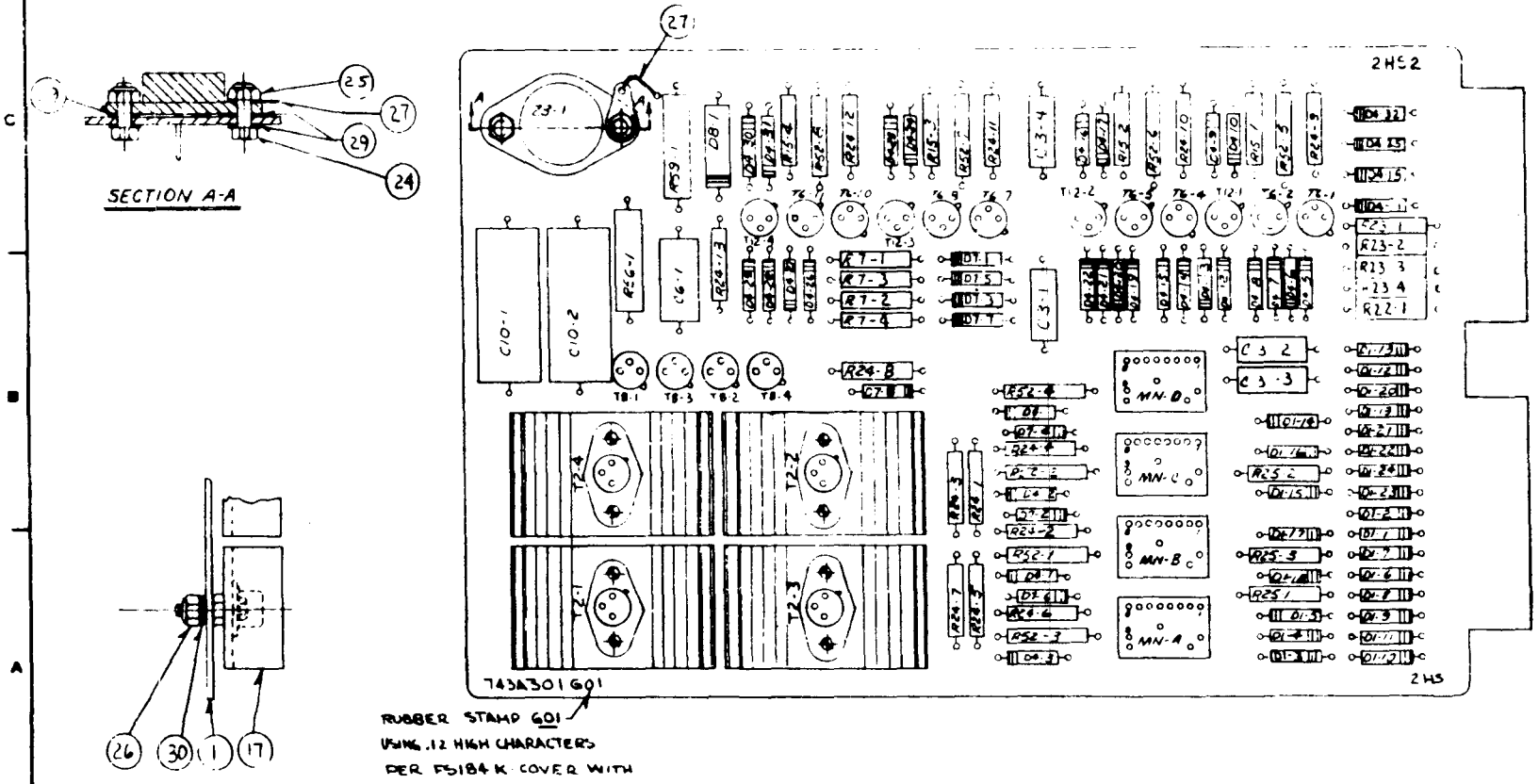


Figure 3-24. Subcolumn Half-Select Switch


NOTES:
1. PIN 10 ALL DUAL NANDS TO GAND (L)
2. PIN 6 ALL DUAL NANDS TO +5V, EXCEPT AS INDICATED.
3. SYMBOL FOR LOGICAL NAND (MODIFIED) REF. 7834A08
4. @ SYMBOL-INDICATES CONNECTION TO PREVIOUSLY DESIGNATED PIN NO. ON BOARD OF SAME MNEMONIC FROM EXTERNAL SOURCE.
SUB ROW
SUB COLUMN
SPARE PINS
+26V
PSC
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
ONE-HALF SELECT-BOARD SCHEMATIC
7733301
SH. 5 OF 9



NEXT ASS'Y		REF DWG	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN. to 24	± .04	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM	2 PLACE DEC	3 PLACE DEC	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
ONE-HALF SELECT ASSEMBLY (2HS2)

DIMENSIONS IN INCHES — SCALE — SUB. 1 2 3 4 5 6 7 8 9 10 11 12

DRWN — APPD
CHKD — APPD
SUPV — APPD

743A301
SH. 3 OF 9

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA U.S.A.

NO.	CHANGE
1	

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INTERRUPT SCAN CONTROL 2IC1

A. GENERAL DESCRIPTION

The 2IC1 card is used to provide:

1. Interrupt Control Logic
2. Probe Pulser Timing
3. Clear S to "Zero" Gate Drive
4. S → Z Gate Drive
5. Clear F to "One" Gate Drive

Figure 3-25 is a block diagram of this card.

B. CIRCUIT DESCRIPTION

Interrupt Control Logic - consists of NANDS A, B, C, D5, E11 and F. Dual NAND B is used as a flip-flop to perform the "Interrupt Lockout" function. Similarly Dual NAND C is a flip-flop for the "Hit" function.

NAND A5 will set "Interrupt Lockout" in Sequence VII of a SLJ (Set Lockout and Jump) instruction.

NAND A11 will clear "Interrupt Lockout" during Sequence VII of a CLJ (Clear Lockout and Jump) instruction.

NAND F5 will set "Interrupt Lockout" when an interrupt core (located elsewhere) is set. The input to F5 must be a minimum 2 volt level from the interrupt core. This will not come in until the core has been interrogated.

NAND F11 will set the "Hit" flip-flop when an interrupt core (again 2 volt minimum level) is set and the core has been probed.

NAND D5 clears the "Hit" flip-flop upon completion of an Interrupt Scan. The diodes on the input D1-2, D1-3, and D1-4 determine the number of interrupts to be scanned.

A look at the table marked "Remove Diodes" (on the schematic) will show which diodes are to be removed (physically). For example, if the system has 16 interrupts, then diodes D1-3 and D1-4 are removed, for 48 interrupts, only diode D1-4 is removed. For 64 interrupts (maximum available) diodes D1-2 and D1-3 are removed.

NAND E11 inhibits one interrupt scan when the conditions for scan (that is when all inputs are logical zero) are not present.

NAND E5 is used for the Probe Pulser Timing signal.

$\overline{\text{Clr S, 0}}$ - consists of NAND H11 and diode D1-26. The S register is master cleared by clamping H11 to ground.

S to Z Gate Drive - consists of NAND G and interrupt sequence. G11 enables the date during Sequence VII.

H5 is used as the gate drive circuit.

$\overline{\text{Clr F, 1}}$ - consists of NAND D11 and diode D1-6. F register will be cleared by clamping D11 to ground through diode D1-6.

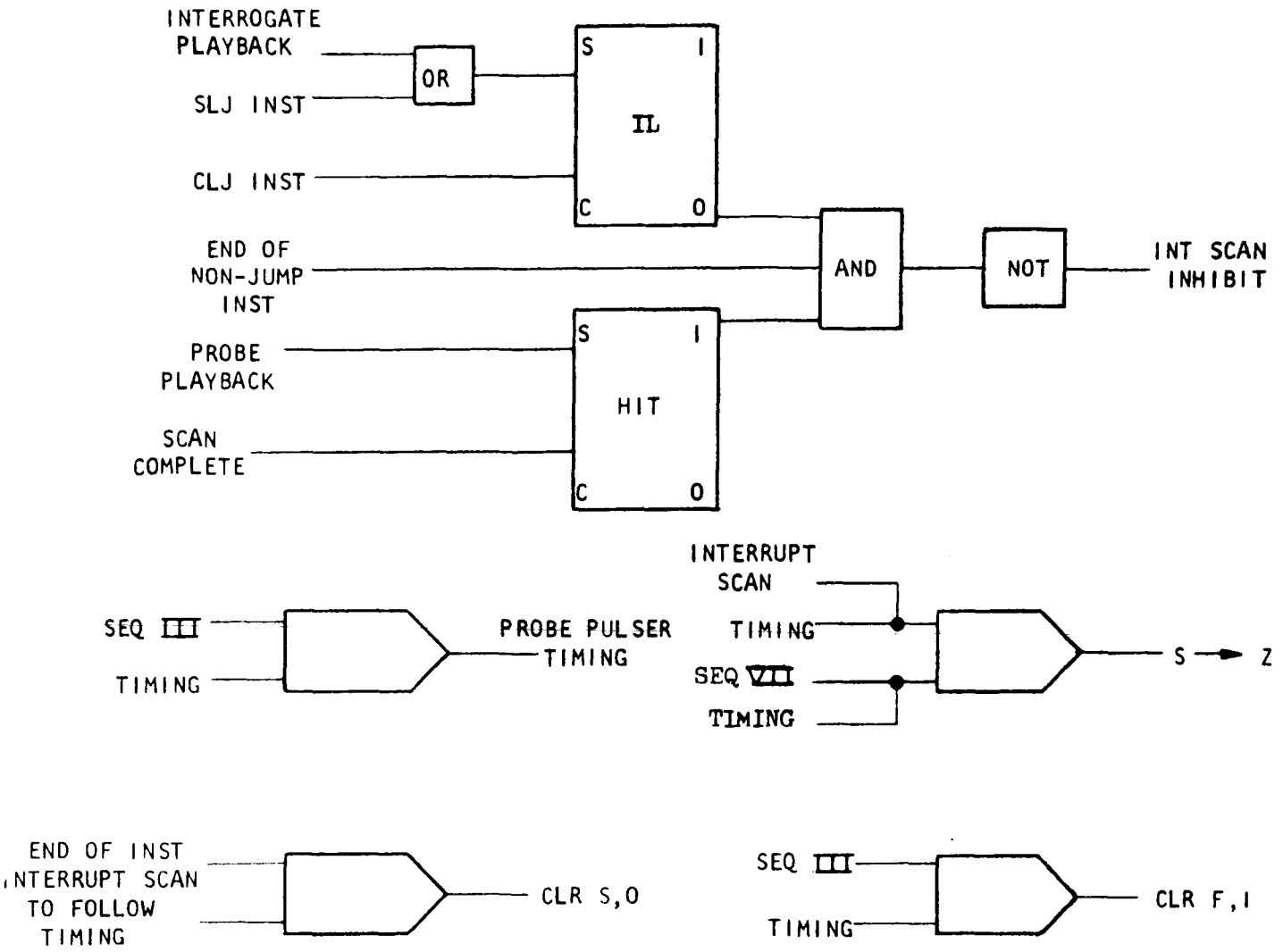
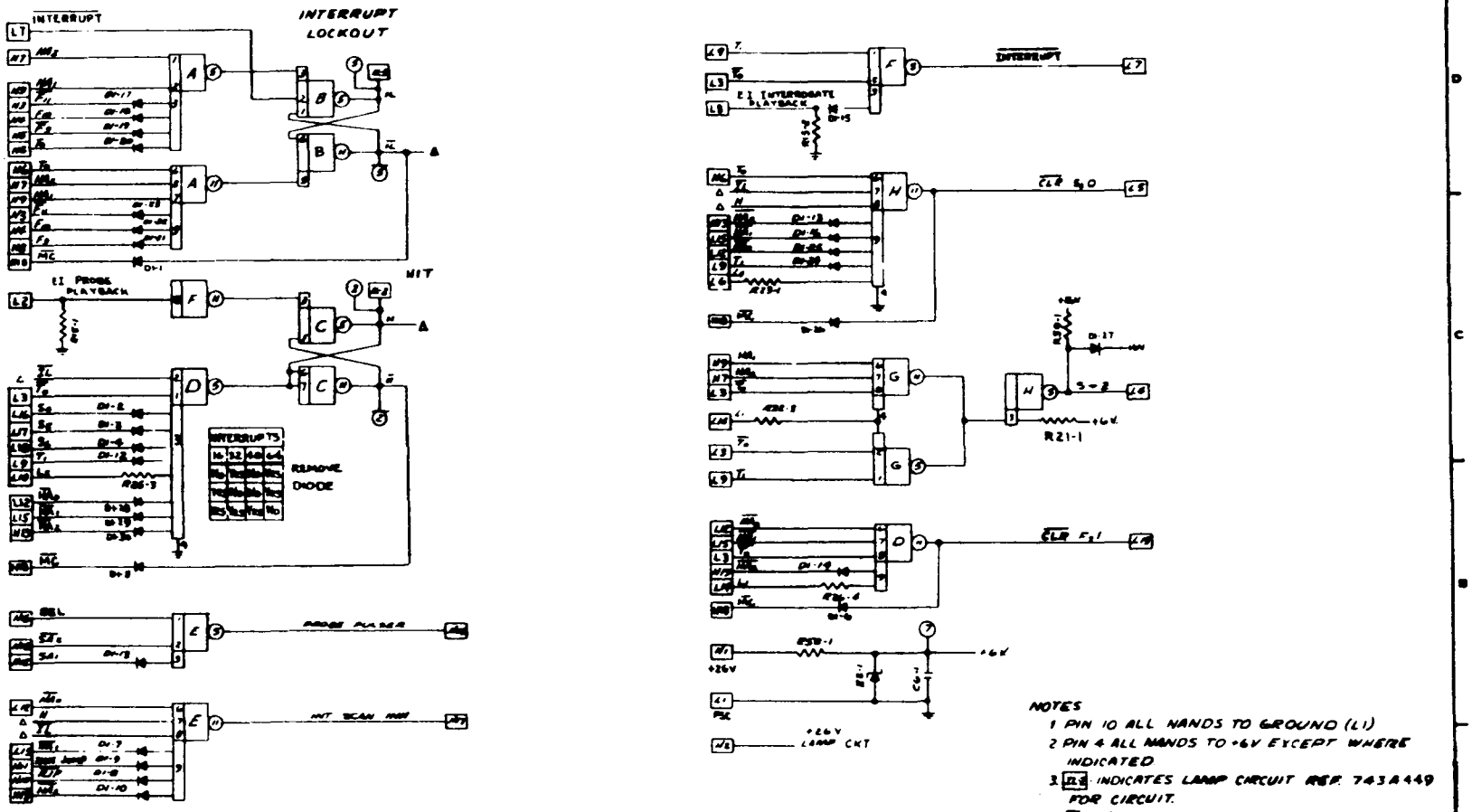

INTERROGATE PLAYBACK
SLJ INST
OR
CLJ INST
S
I
IL
C
O
END OF NON-JUMP INST
AND
NOT
INT SCAN INHIBIT
PROBE PLAYBACK
SCAN COMPLETE
HIT
SEQ III
TIMING
PROBE PULSER TIMING
INTERRUPT SCAN
TIMING
SEQ VII
TIMING
S → Z
END OF INST
INTERRUPT SCAN TO FOLLOW TIMING
CLR S,O
SEQ III
TIMING
CLR F,I

Figure 3-25.



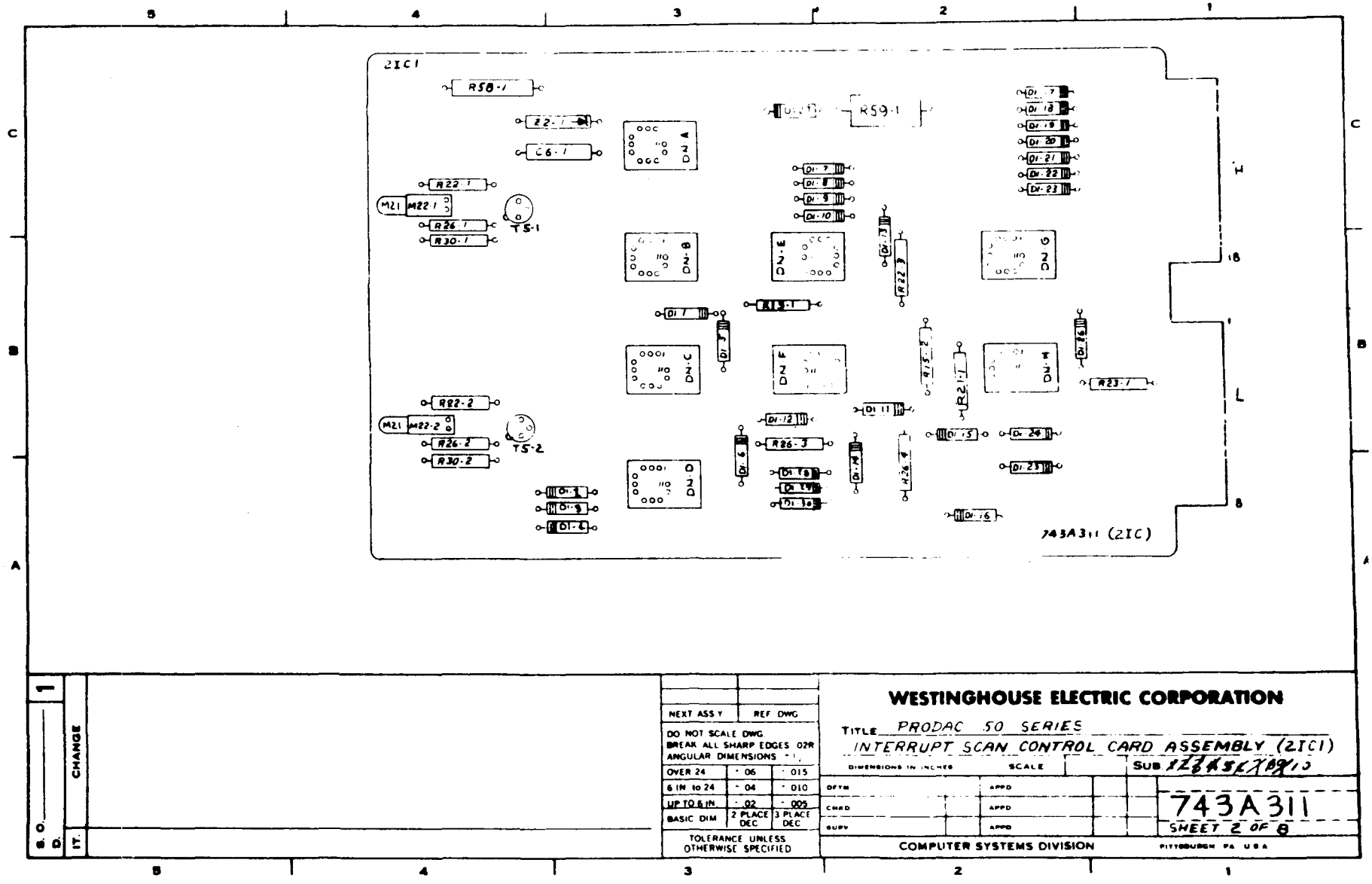
WESTINGHOUSE ELECTRIC CORPORATION

Title PRODAC 50 SERIES
INT SCAN CONTROL BOARD SCHEMATIC (22C1)

Size F 2 348787810

743A311
SH 3 OF 8

COMPUTER SYSTEMS DIVISION



S.O. D.	1	CHANGE	
IT.			

NEXT ASS'Y	REF DWG
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ±1°	

OVER 24	± .06	± .015
6 IN to 24	± .04	± .010
UP TO 6 IN	± .02	± .005
BASIC DIM	2 PLACE DEC	3 PLACE DEC

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
INTERRUPT SCAN CONTROL CARD ASSEMBLY (2IC1)

DIMENSIONS IN INCHES | SCALE | SUB [illegible]

DFTM		APPD
CHKD		APPD
SUPV		APPD

743A311
SHEET 2 OF 8

COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

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INTERRUPT FILTER MODULE 4IF1/4IF2

A. GENERAL DESCRIPTION

This module contains eight filters which condition interrupting plant contacts by removing high frequency noise spiker. The 4IF1 is designed for use with +48 volt inputs and the 4IF2 is designed for +125 volt input signals. The pin assignments on the 4IF module are the same as those used on the faster, isolating 5IF series and therefore, corresponding modules are electrically interchangeable. (Figure 3-26).

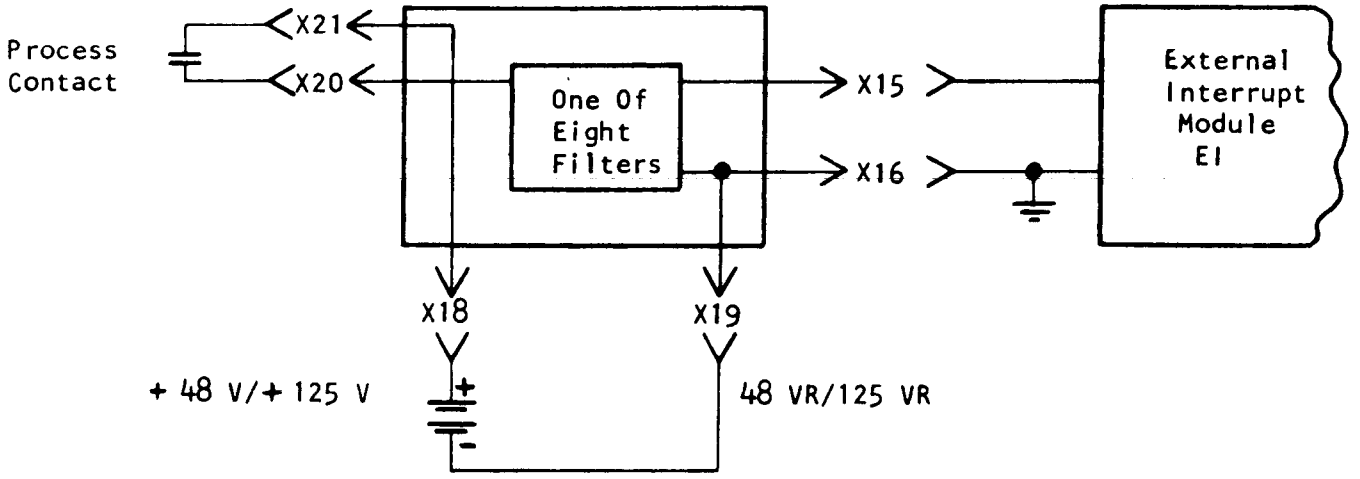


Figure 3-26.

B. CIRCUIT SPECIFICATIONS

1. Input Requirements

The total resistance of the wiring to the process contact plus the contact resistance should not exceed an arbitrary 1000 ohms. With these filters, the filtered interrupt rate is 20 per second.

2. Output Specifications

The output of this card is designed for coupling directly into the 3EI external interrupt module using twisted pair cabling. The 3EI card is within about 25 feet of these filter cards in existing installations.

3. Power Requirements (with all contacts closed)

4IF1 (48V version)
+48 volts ± 10% 15.4 milliamperes ± 11% per card

4IF2 (125V version)
+125 volts ± 10% 15.1 milliamperes ± 11% per card

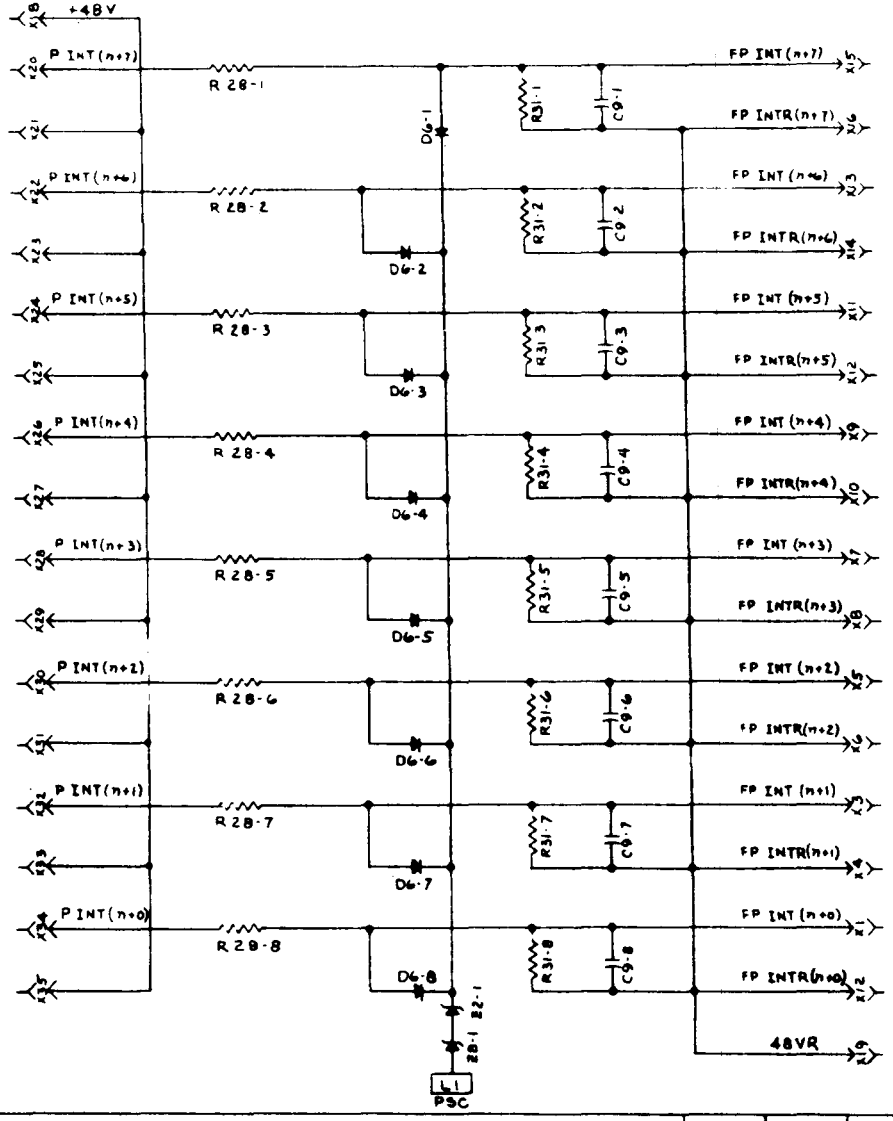
C. CIRCUIT DESCRIPTION

Each filter consists of a voltage divider with a 0.5 mfd capacitor on the output. This capacitor is in parallel with another 0.5 mfd capacitor in each input to the 3EI external interrupt card. In both the 48 and the 125 volt case, the resistors are chosen to give approximately 28-1/2 volts steady state across the capacitor. However, all filter outputs are clamped to a bus connected through a 6.8V and a 20V zener diode to PSC. This limits the voltage input to the 3EI card under worst case condition to about 28 volts and avoids double interrupts.

The voltage divider resistors are 10K and 15K in the 48V case and 51.1K and 15K in the 125V case with the 15K appearing across the 0.5 mfd capacitors. Each divider takes about 2 milliamperes steady state when the contact is closed.

The discharge time constant assuming 1 mfd capacitance total and 15K is 15 milliseconds in both cases. The charging time constant is 11.6 milliseconds for 125V and 6 milliseconds for the 48V version. This assumes negligible contact and lead resistance.

Following the closing of the process contact, the input to the 3EI must rise to +17 volts typically before the interrupt is recognized by the computer. With rated voltages and negligible lead and contact resistance, it will take about 0.92 time constant for the capacitors to charge to 17 volts. This gives 5.5 and 10.7 milliseconds delay for the 48 and 125 volt versions respectively. With maximum lead resistance, these values increase to about 6.1 and 10.9 milliseconds respectively. About 40 milliseconds is needed to discharge the filter on opening of the process contact so that another closure can be recognized. This then gives a maximum rate of about 20 interrupts per second.



NEXT ASS'Y		REF DWG
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020 MAX UNLESS OTHERWISE SPECIFIED		
OVER 24	.06	.015
6 IN to 24	.04	.010
UP TO 6 IN	.02	.005
BASIC DIM	2 PLACE DEC	3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED		

WESTINGHOUSE ELECTRIC CORPORATION

PRODAC 50 SERIES 4IF1

TITLE +48V INTERRUPT FILTER SCHEMATIC

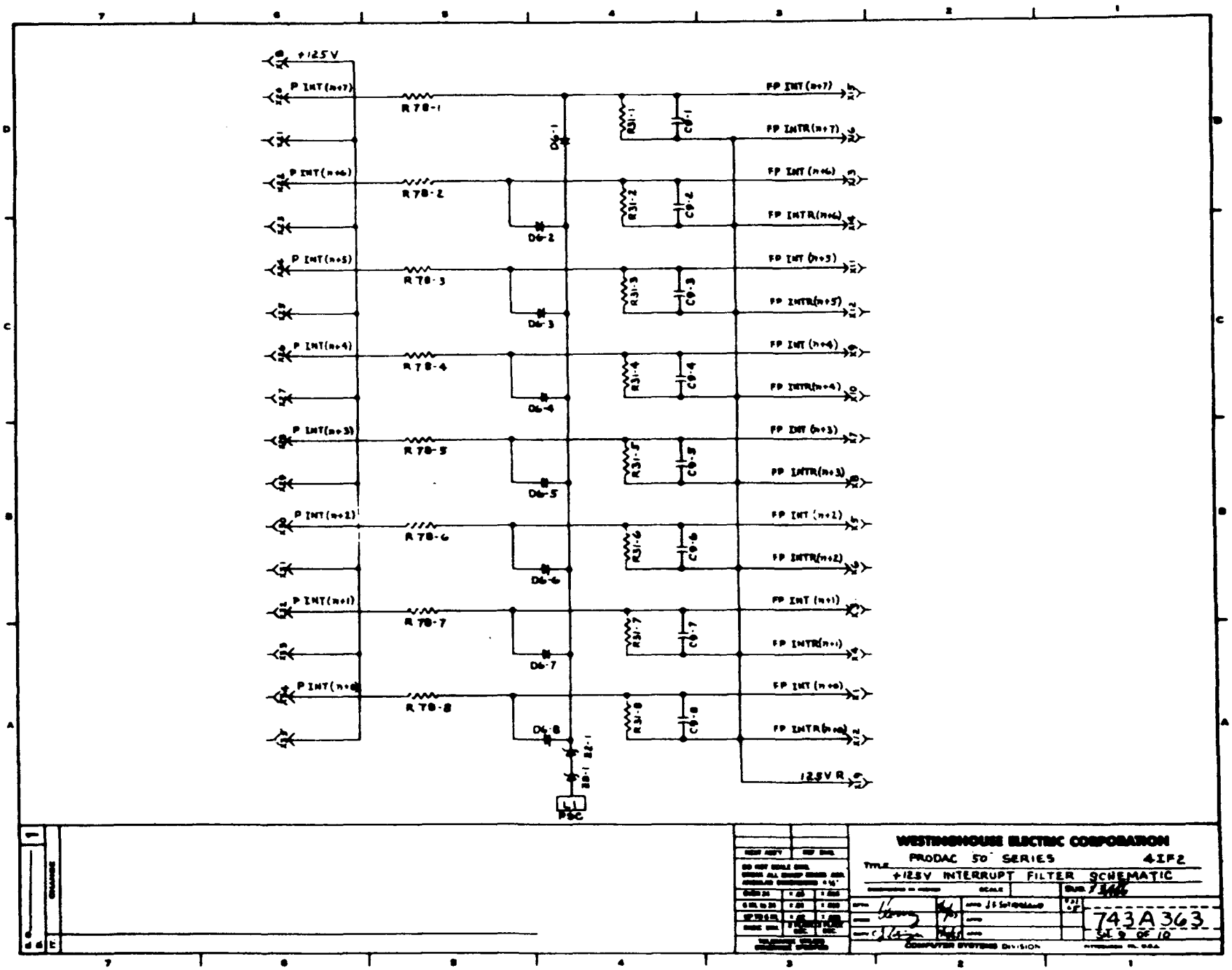
SCALE: SUB 1 3 4 6

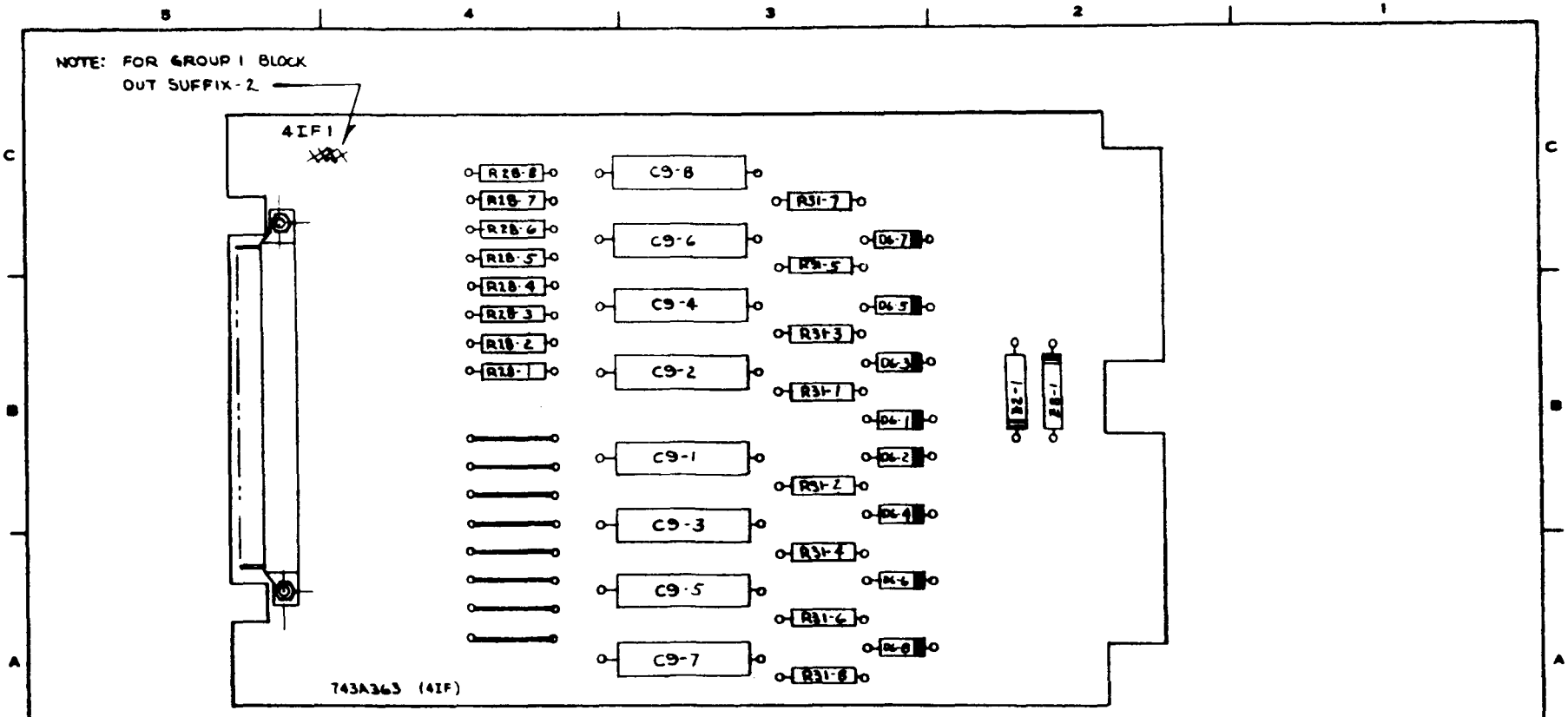
APPD J E SUTHERLAND

COMPUTER SYSTEMS DIVISION

743A363

SH 8 OF 10


+12.5V
P INT(n+7)
P INT(n+6)
P INT(n+5)
P INT(n+4)
P INT(n+3)
P INT(n+2)
P INT(n+1)
P INT(n+0)
R 78-1
R 78-2
R 78-3
R 78-4
R 78-5
R 78-6
R 78-7
R 78-8
D6-1
D6-2
D6-3
D6-4
D6-5
D6-6
D6-7
D6-8
R31-1
R31-2
R31-3
R31-4
R31-5
R31-6
R31-7
R31-8
C9-1
C9-2
C9-3
C9-4
C9-5
C9-6
C9-7
C9-8
FP INT(n+7)
FP INTR(n+7)
FP INT(n+6)
FP INTR(n+6)
FP INT (n+5)
FP INTR(n+5)
FP INT (n+4)
FP INTR(n+4)
FP INT (n+3)
FP INTR(n+3)
FP INT (n+2)
FP INTR(n+2)
FP INT (n+1)
FP INTR(n+1)
FP INT (n+0)
FP INTR(n+0)
12.5V R
P6C
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
4IF2
+12.5V INTERRUPT FILTER SCHEMATIC
743A363
COMPUTER SYSTEMS DIVISION



SEE NOTE 9 SH.10

1	CHANGE		
S.O.			
E.C.			

NEXT ASSY	REF. DWG.	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .030 ANGULAR DIMENSIONS ± ½°		
OVER 24	± .06	± .015
6 IN. to 24	± .04	± .030
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.
TOLERANCE UNLESS DIMENSIONS SPECIFIED		

WESTINGHOUSE ELECTRIC CORPORATION

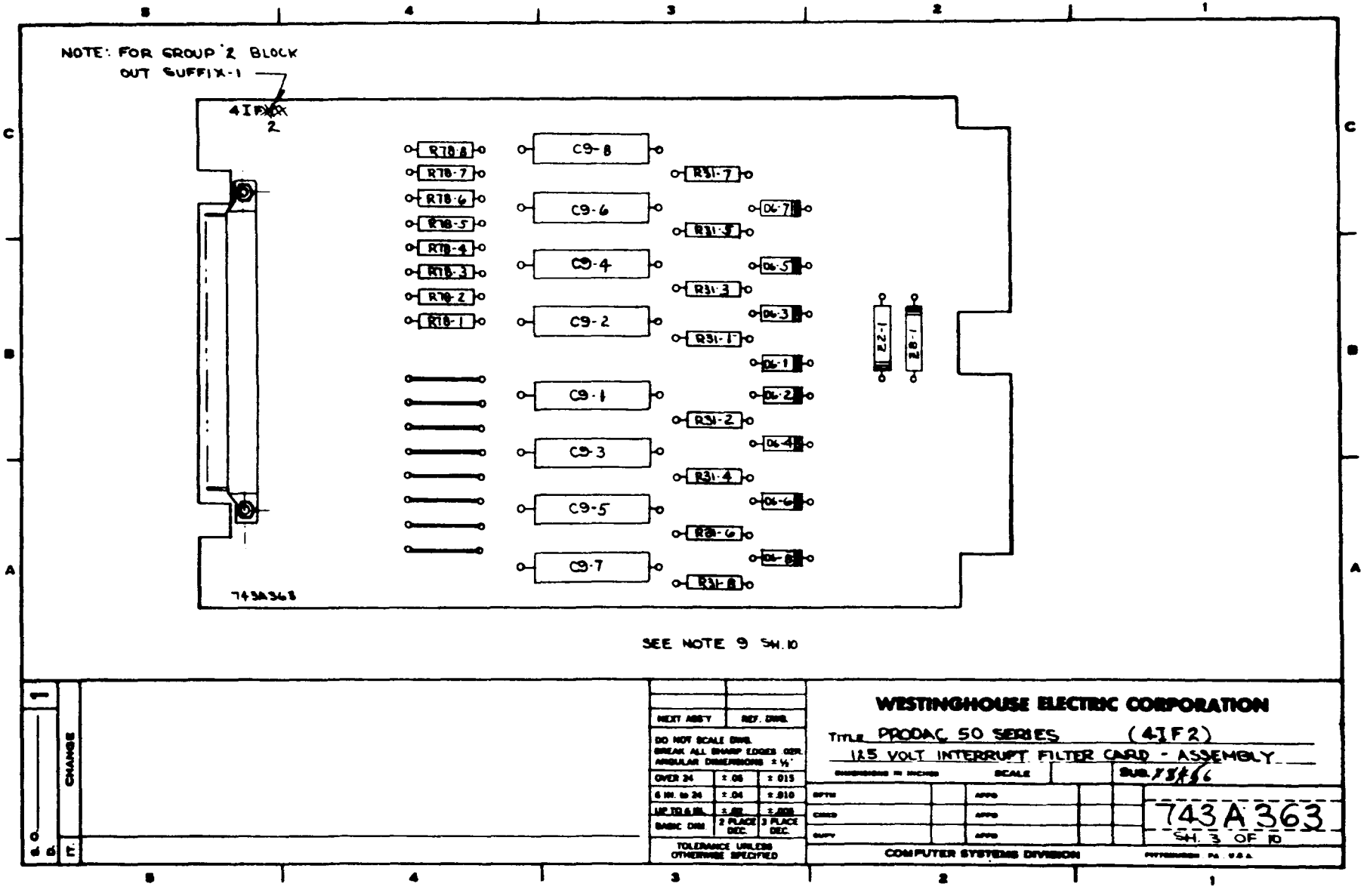
TITLE PRODAC 50 SERIES (4IF1)
48 VOLT INTERRUPT FILTER CARD - ASSEMBLY

DIMENSIONS IN INCHES | SCALE | SUB. 743A386

DRFTR		APPD	
CHKD		APPD	
SUPV		APPD	

743A363
SH 2 OF 10

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA. U.S.A.



1	CHANGE				

NEXT ASSY		REF. DWG.
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020 R. ANGULAR DIMENSIONS ± ½°		
OVER 24	± .06	± .015
6 TO 24	± .04	± .010
UP TO & INCL. 6	± .02	± .005
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.
TOLERANCE UNLESS OTHERWISE SPECIFIED		

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES (4IF2)
115 VOLT INTERRUPT FILTER CARD - ASSEMBLY

DIMENSIONS IN INCHES | SCALE | SUB. 18466

DEPTH		APPD			743A363
CHKD		APPD			SH. 3 OF 10
SUPV		APPD			

COMPUTER SYSTEMS DIVISION — PITTSBURGH, PA. U.S.A.

ISOLATED INTERRUPT FILTER MODULE 5IF1/5IF2

A. GENERAL DESCRIPTION

This module contains eight isolating filters which condition interrupting plant contacts by removing high frequency noise spikes. The 5IF1 is designed for use with +48 volt inputs and the 5IF2 is designed for +125 volt input signals. The pin assignments on the 5IF module are the same as those used on the 4IF series and therefore, corresponding modules are electrically interchangeable. (Figure 3-27).

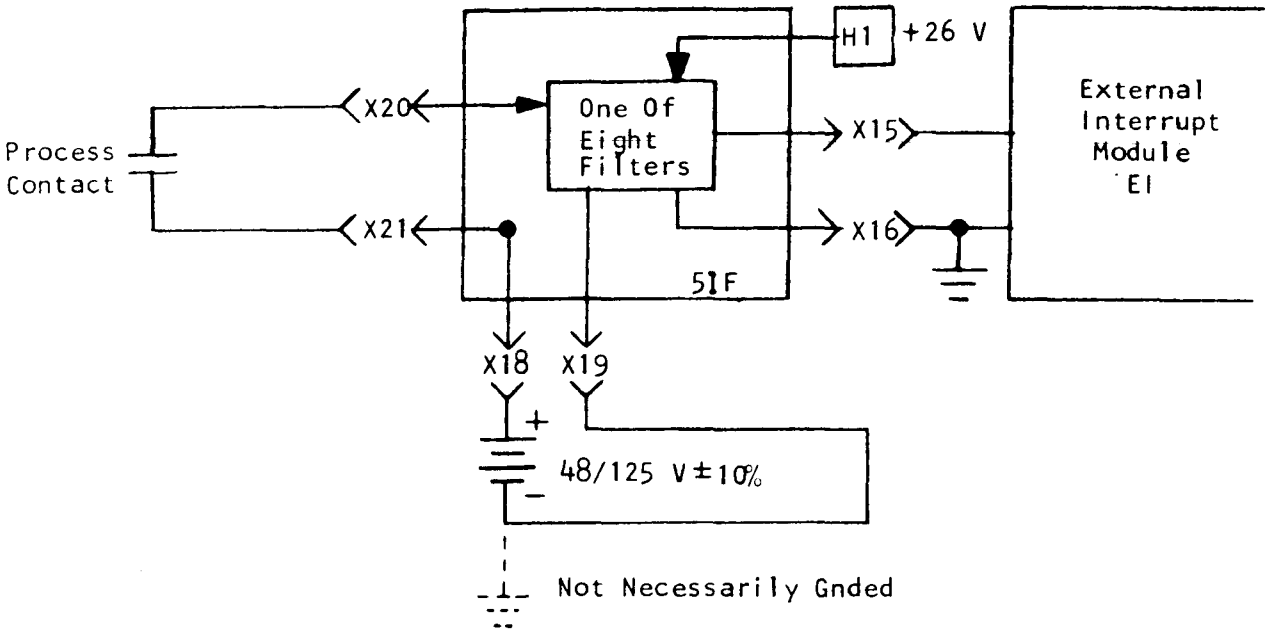


Figure 3-27.

B. CIRCUIT SPECIFICATIONS

1. Input Requirements

The total resistance of the wiring to the process contact plus the contact resistance must not in any case exceed 2000 ohms for a 48 volt system or 7000 ohms in a 125 volt system. When these large lead resistances are allowed, the speed of the system is reduced to 100 operations per second. If the lead resistance is less than 100 ohms then the 5IF filters will follow 200 operations per second. It should be noted that this filter will not block extremely low frequency contact bounce noise below 200 cps.

2. Output Specifications

The output of this card is designed for coupling directly into the 3EI external interrupt module, and therefore it can supply 26 milliamperes from a +26 volt source into the input terminal of the 3EI card. Twisted pair cabling between the 5IF and the 3EI should be less than 25 feet long.

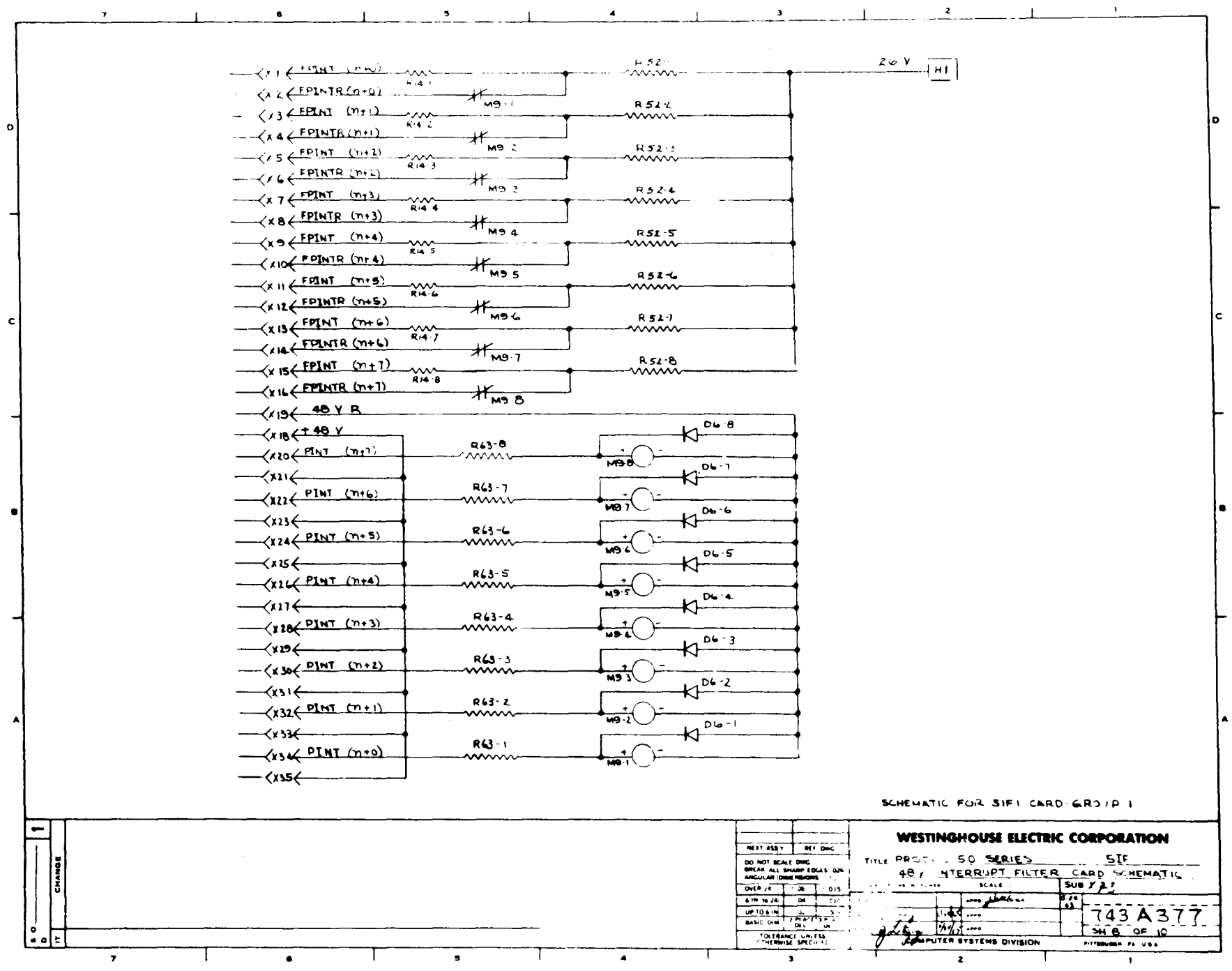
3. Power Requirements

5IF1 (48 volt version)
+48 volts ±10% 145 milliamps per card (worst case)
+26 volts ±10% 208 milliamps per card (worst case)
(note that the above currents are exclusive and the worst cases shown will not occur simultaneously)

5IF2 (125 volt version)
+125 volts ±10% 185 milliamps per card (worst case)
+26 volts ±10% 208 milliamps per card (worst case)
(note that the above currents are exclusive and the worst cases shown will not occur simultaneously)

C. CIRCUIT DESCRIPTION

The individual filter circuits used on the 5IF card use mercury wetted relays for isolation and filtering. The circuits shown on sheets 8 and 9 of drawing 743A377 illustrate the technique used. Series resistors (R63 on 5IF1 and R64 on 5IF2) limit the coil current to 105 excess amp turns of relay drive. This provides a pickup time of 1.7 milliseconds and a drop time of 2.0 milliseconds. Following the opening of the relay contact, the input to the 3EI must rise to +17 volts typically before the interrupt is recognized by the computer. This delay is typically 0.6 milliseconds, but can be as long as 1.3 milliseconds or as short as 0.4 millisecond depending on component tolerances in the 3EI and voltage variations on the +26 volt power supply. The series resistors (R14) on the 5IF card limit the discharge current resulting from the relay contacts closing. Extremely high pulses of current would be generated each time a process interrupt contact opened and de-energized a relay on the 5IF card if the R14 resistors were omitted.



SCHEMATIC FOR SIF1 CARD 6R3 P 1

1	CHANGE	

NEXT ASSY | REF DWG

DO NOT SCALE DWG
BREAK ALL SHARP EDGES .005
ANGULAR DIMENSIONS

OVER /4	.38	.015
6 IN TO 24	.04	.01
UP TO 6 IN	.2	.5
BASIC DIM	DEC	LIN

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

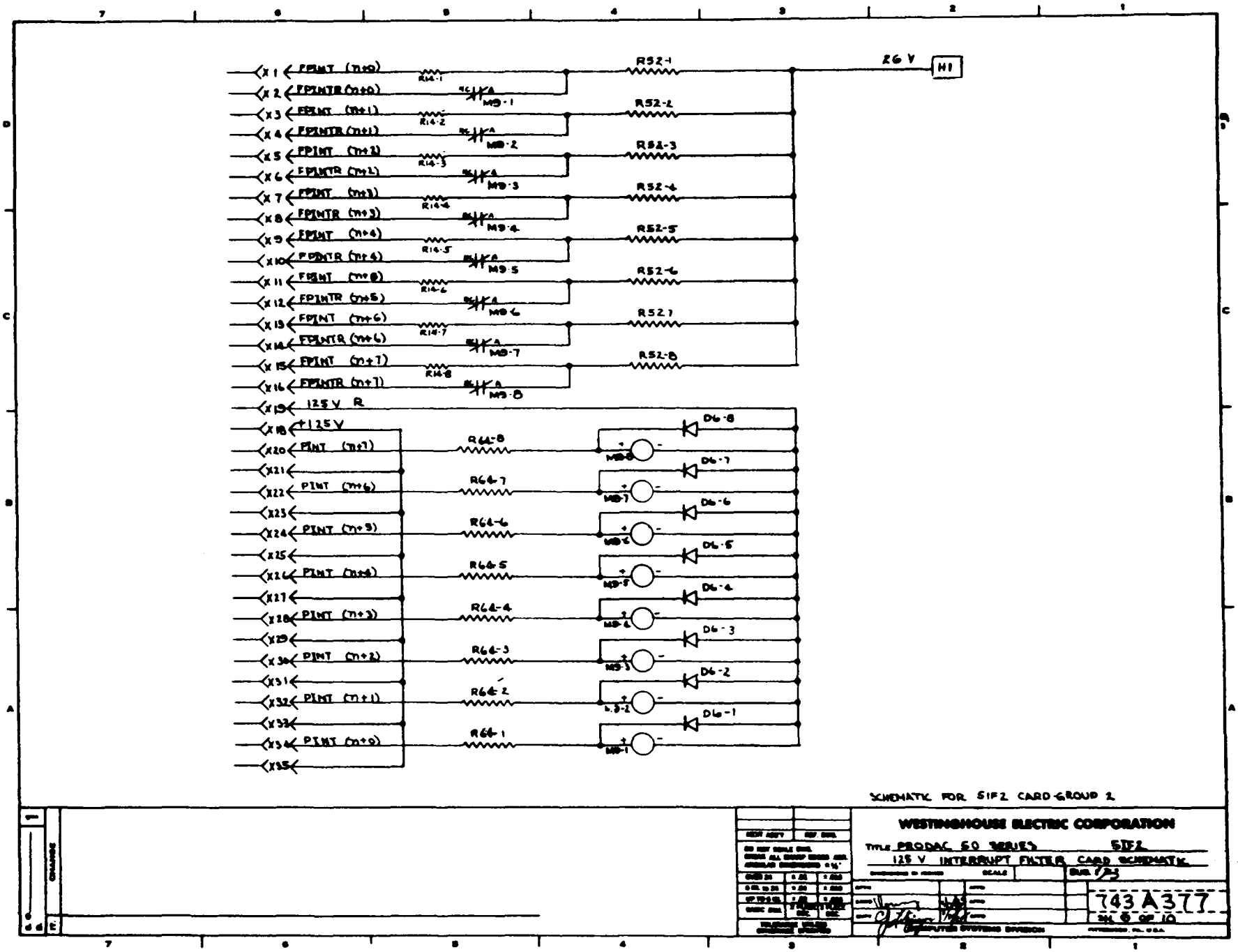
TITLE PROC - 50 SERIES SIF
48 V INTERRUPT FILTER CARD SCHEMATIC

SCALE | SUB 3 2 2

DRWN | DATE 5-26-83
CHKD
APPD

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA U.S.A.

743A377
SH 8 OF 10

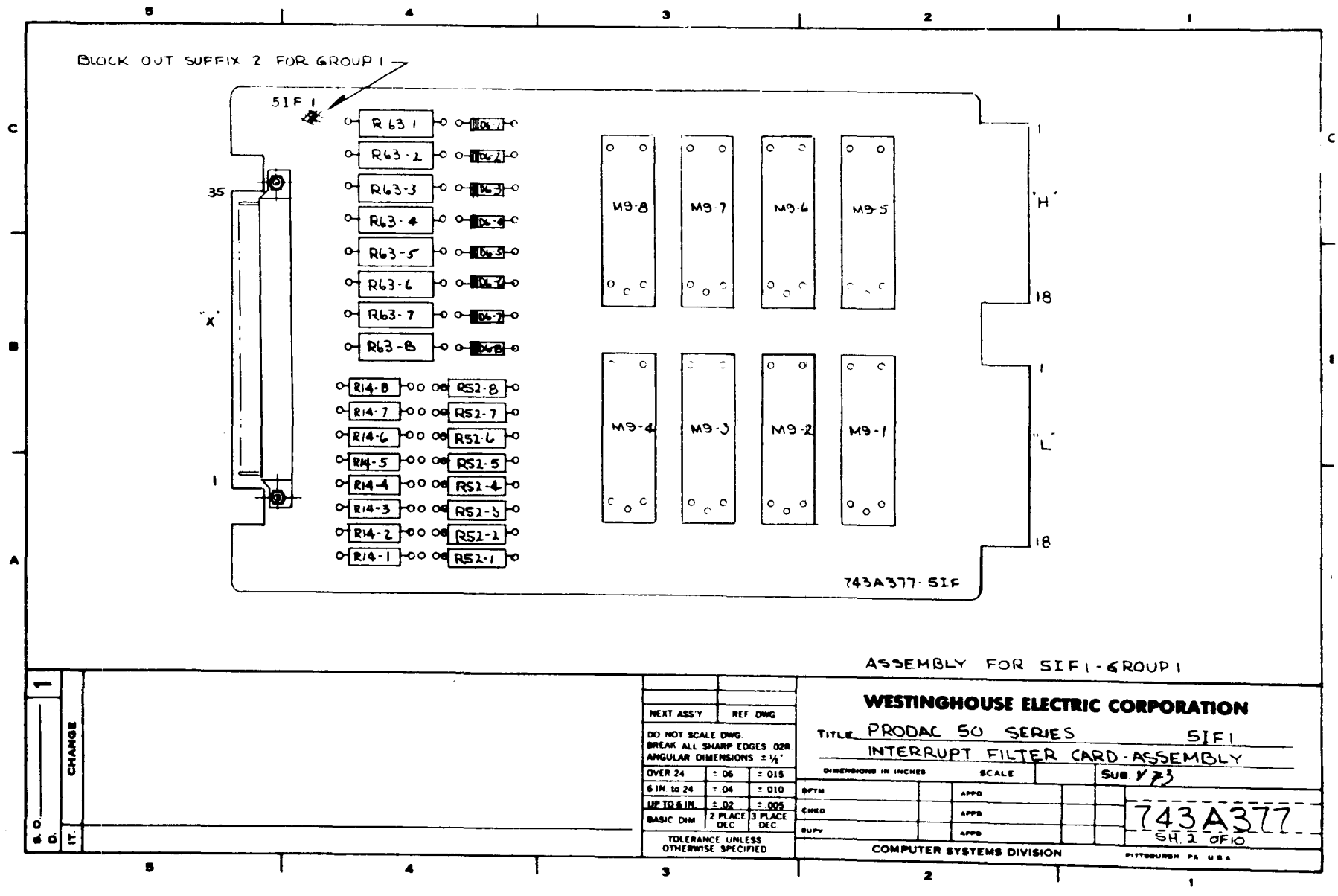


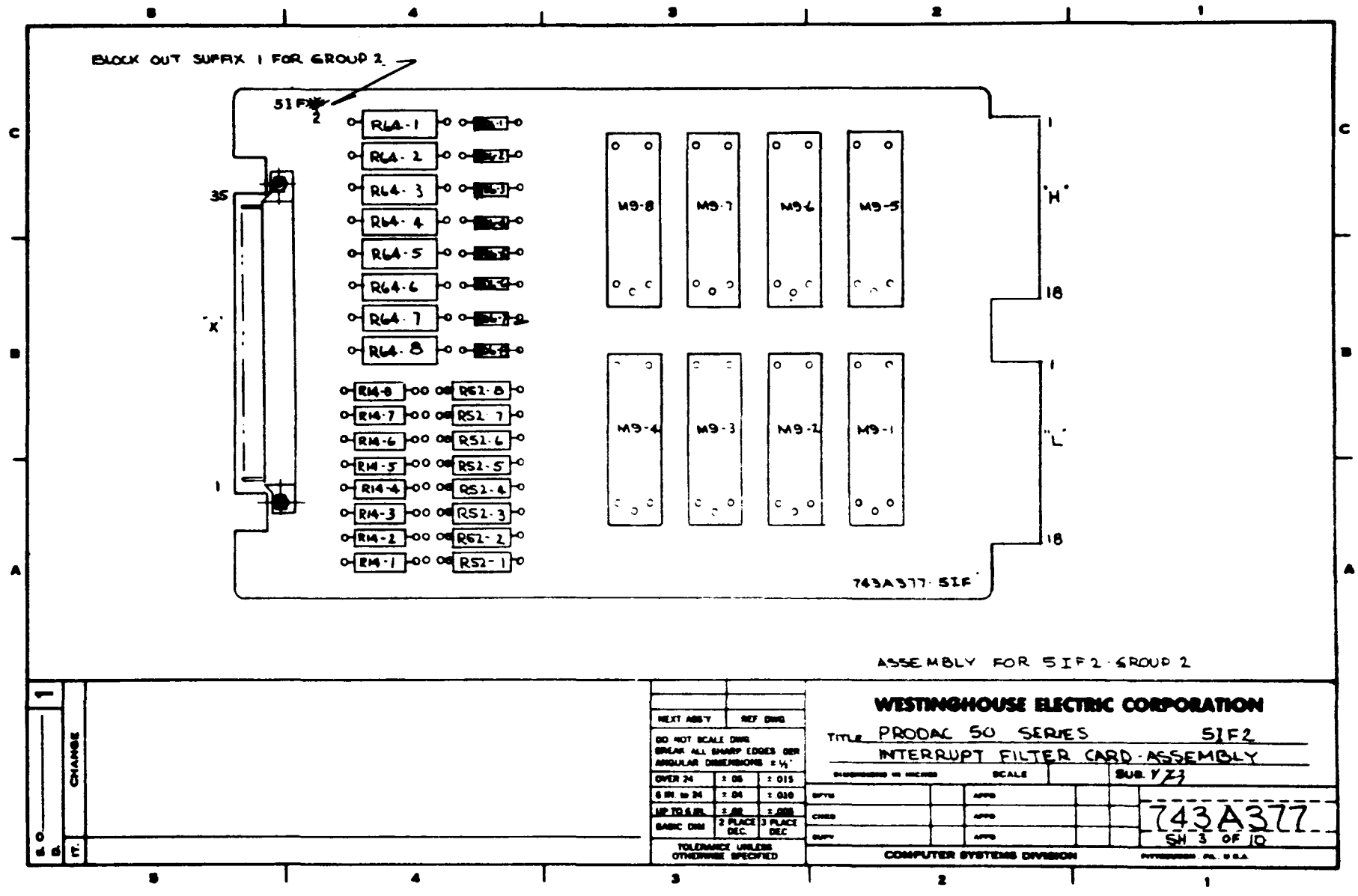
SCHEMATIC FOR SIF2 CARD GROUP 2

WESTINGHOUSE ELECTRIC CORPORATION

Title PRODAC 50 SERIES SIF2
125 V INTERRUPT FILTER CARD SCHEMATIC

743A377


BLOCK OUT SUFFIX 2 FOR GROUP 1
51F1
R63-1
R63-2
R63-3
R63-4
R63-5
R63-6
R63-7
R63-8
R14-8
R14-7
R14-6
R14-5
R14-4
R14-3
R14-2
R14-1
RS2-8
RS2-7
RS2-6
RS2-5
RS2-4
RS2-3
RS2-2
RS2-1
M9-8
M9-7
M9-6
M9-5
M9-4
M9-3
M9-2
M9-1
35
1
"X"
"H"
"L"
743A377-51F
ASSEMBLY FOR 51F1-GROUP 1
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES 51F1
INTERRUPT FILTER CARD-ASSEMBLY
743A377
SH. 2 OF 10
COMPUTER SYSTEMS DIVISION
PITTSBURGH PA U.S.A.


BLOCK OUT SUFFIX 1 FOR GROUP 2
51F
2
35
"X"
1
R64-1
R64-2
R64-3
R64-4
R64-5
R64-6
R64-7
R64-8
R14-8
R14-7
R14-6
R14-5
R14-4
R14-3
R14-2
R14-1
R61-8
R51-7
R51-6
R51-5
R51-4
R51-3
R51-2
R51-1
M9-8
M9-7
M9-6
M9-5
M9-4
M9-3
M9-2
M9-1
1
"H"
18
1
"L"
18
743A377-51F
ASSEMBLY FOR 51F2-GROUP 2
1
CHANGE
E.O.
ECN
NEXT ASS'Y
REF DWG
DO NOT SCALE DWG.
BREAK ALL SHARP EDGES
ANGULAR DIMENSIONS ± ½°
OVER 24 ± .06 ± .015
6 IN. to 24 ± .04 ± .010
UP TO 6 IN. ± .02 ± .005
BASIC DIM 2 PLACE DEC. 3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES 51F2
INTERRUPT FILTER CARD-ASSEMBLY
SCALE
SUB. Y Z 3
DRWN
CHKD
SUPV
APPD
743A377
SH 3 OF 10
COMPUTER SYSTEMS DIVISION

INHIBIT PADDLE BOARD 3IP2

A. GENERAL DESCRIPTION

This circuit board is required to contain the damping resistors for the inhibit windings of the core stack, and the logic elements necessary for selecting core stacks.

The relationship of the Inhibit Paddle Board to the system is shown by the block diagram of Figure 3-28.

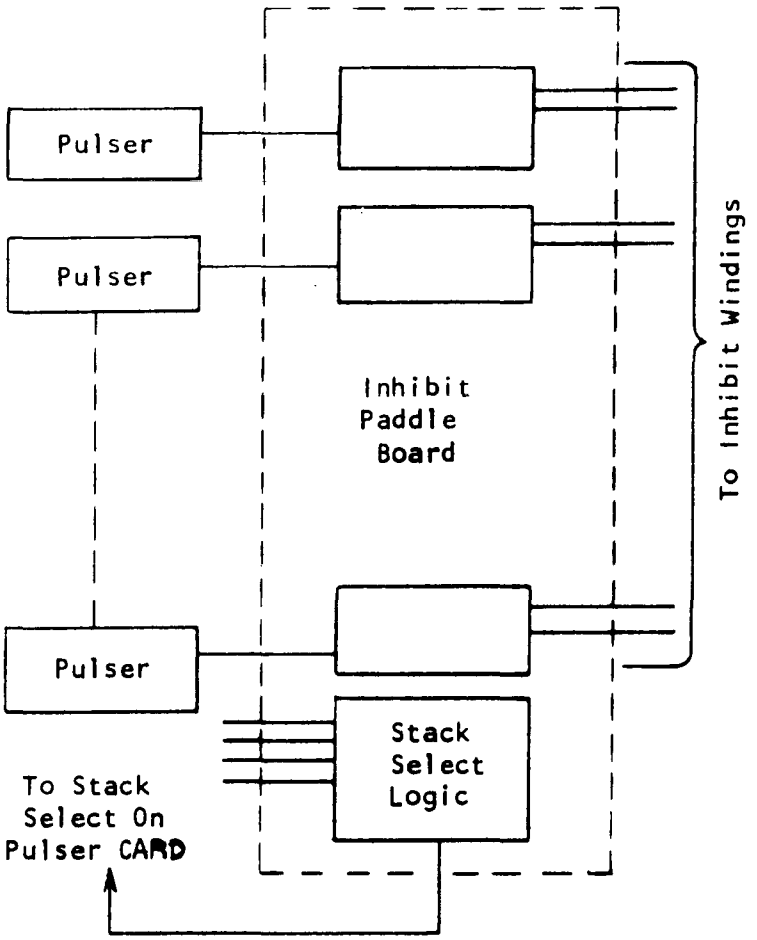


Figure 3-28.

B. CIRCUIT DESCRIPTION

The card contains 14 inhibit input circuits, two logic gates and zener diode power supply. The inhibit input circuit (Figure 3-29) consists of a damp-resistor across the inhibit winding and a diode in series with the inhibit winding. The primary purpose of this diode is to offer protection to the inhibit winding under accidental over-current conditions. Should the current

become excessive, the diode should fail before the winding. In addition to this safety feature the diodes also insure that current will not circulate through the Inhibit winding in the opposite direction.

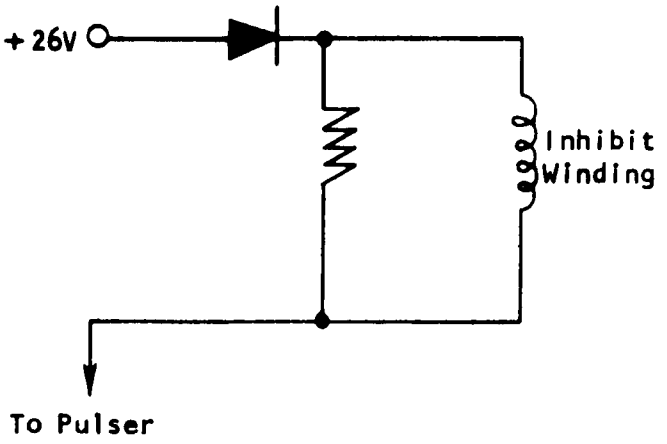
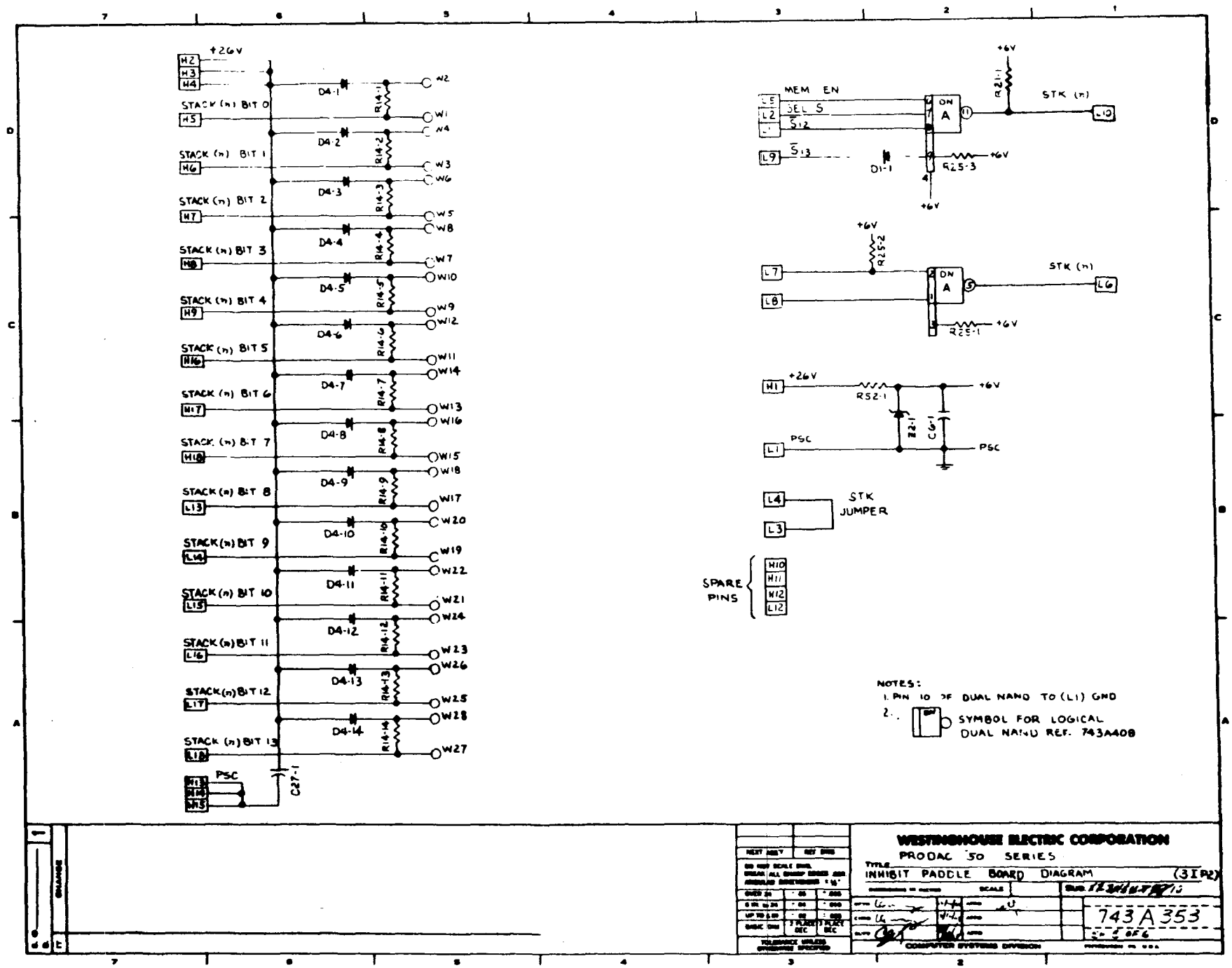
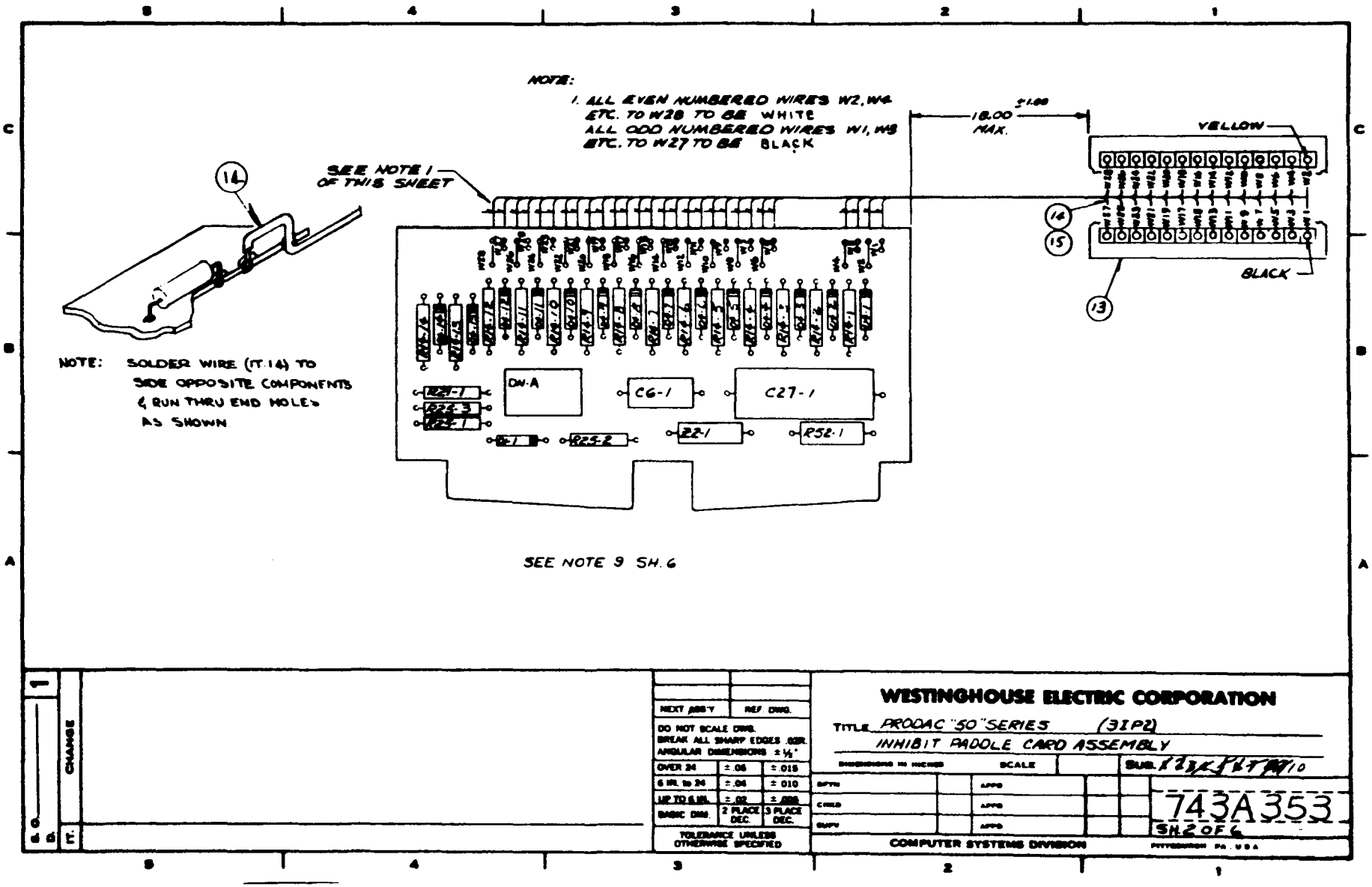


Figure 3-29. Inhibit Input Circuit

The logic elements on this board are two NAND gates in a dual NAND package. One NAND gate is used to decode the last two bits of the S-register together with the memory enable signal. The output of this NAND gate provides the "stack select" signal for the pulser card. The additional NAND gate is provided to enable additional logic operations where more than one stack is used.


+26V
H2
H3
H4
STACK (n) BIT 0
H5
STACK (n) BIT 1
H6
STACK (n) BIT 2
H7
STACK (n) BIT 3
H8
STACK (n) BIT 4
H9
STACK (n) BIT 5
H16
STACK (n) BIT 6
H17
STACK (n) BIT 7
H18
STACK (n) BIT 8
L13
STACK (n) BIT 9
L14
STACK (n) BIT 10
L15
STACK (n) BIT 11
L16
STACK (n) BIT 12
L17
STACK (n) BIT 13
L18
D4-1
D4-2
D4-3
D4-4
D4-5
D4-6
D4-7
D4-8
D4-9
D4-10
D4-11
D4-12
D4-13
D4-14
R14-1
R14-2
R14-3
R14-4
R14-5
R14-6
R14-7
R14-8
R14-9
R14-10
R14-11
R14-12
R14-13
R14-14
W2
W1
W4
W3
W6
W5
W8
W7
W10
W9
W12
W11
W14
W13
W16
W15
W18
W17
W20
W19
W22
W21
W24
W23
W26
W25
W28
W27
PSC
H1
H4
H5
C27-1
MEM EN
L5
SEL S
S12
L2
L9
S13
D1-1
R25-3
+6V
DN A
11
STK (n)
L10
R21-1
L7
L8
R25-2
R25-1
5
L6
H1
RS2-1
R2-1
C6-1
L1
PSC
L4
L3
STK JUMPER
SPARE PINS
H10
H11
H12
L12
NOTES:
1. PIN 10 OF DUAL NAND TO (L1) GND
2. SYMBOL FOR LOGICAL DUAL NAND REF. 743A408
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
TITLE INHIBIT PADDLE BOARD DIAGRAM (3IP2)
743A353
SHEET 5 OF 6



NEXT ASS'Y		REF DWG.	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .03R. ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN. to 24	± .04	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC "50" SERIES (3IP2)
INHIBIT PADDLE CARD ASSEMBLY

DRAWING TO INCHES | SCALE | SIZE B | SHEET 1 OF 1

DRAWN | APPD
CHKD | APPD
SUPV | APPD

743A353
SH 2 OF 6

COMPUTER SYSTEMS DIVISION — PITTSBURGH Pa. U.S.A.

IT.	CHANGE	E.O.
1		

INSTRUCTION REGISTER CARD 2IR1 3IR1

A. GENERAL DESCRIPTION

The Instruction Register Card is used in the central processor to provide the following functions.

1. A Six-Bit Function Register
2. A Gate for Bits 8-13 of the Z Register to the Function Register
3. AND Instruction Decode and Gate Drive
4. EOR Instruction Decode and Gate Drive
5. STP Instruction Decode
6. SMB Instruction Decode
7. CMB Instruction Decode
8. DCR Instruction Decode
9. Decode for Clamping XO to a "One".

Figure 3-30 is a block diagram of the card as used in the central processor.

B. CIRCUIT OPERATION

The card will be described in terms of its usage, refer to the block diagram and schematic.

Six Bit Function Register - consists of NAND's A, B, C, D, E, and F plus six indicator driver circuits. The Register is cleared to "One's" (all lights on). "Zero's" are gated from the Z register. NAND's A, B, C, D, and E have an additional base drive for high fan-out capability.

Z Register Bit 13-8 to Function Register - consists of NAND's G, H, and J. The clear side of Z register is gated to set "Zero's" in the F register. This is done since all "Zero's" are decoded as stop codes.

AND Instruction Decode and Gate Drive - consists of transistors T3-3 and T3-4 plus their associated diodes and resistors. This circuit provides a logical NAND. The only difference between this circuit and a modified NAND, is the amount of current this two-stage amplifier can drive.

EOR Instruction and Gate Drive - consists of transistors T3-1 and T3-2, NAND L5 and associated diodes and resistors, this circuit as above, provides a logical NAND. NAND L5 causes the EOR bus to become a "zero" when the Z register is cleared, this disrupts the Adder carry chain to prevent a sum of "Positive Zero" and "Negative Zero" from equaling "Positive Zero".

STP Instruction Decode - consists of NAND L11 which decodes the STOP Instruction.

SMB Instruction Decode - consists of NAND K5 which clamps output of Z13 to "Zero", thus setting Z13 during SMB Instruction.

CMB Instruction Decode - consists of NAND K11 which clamps output of Z13 to "Zero", thus clearing Z13 during CMB Instruction.

DCR Instruction Decode - consists of NAND M11 which clamps XO to a "Zero" when all other bits in X register are set to "One's" for DCR Instruction.

Clamp XO to One Decode - consists of NAND M5 which clamps XO to a "Zero" forcing XO to a "One" for incrementing the program counter in Sequence III and the S register in Sequence I.

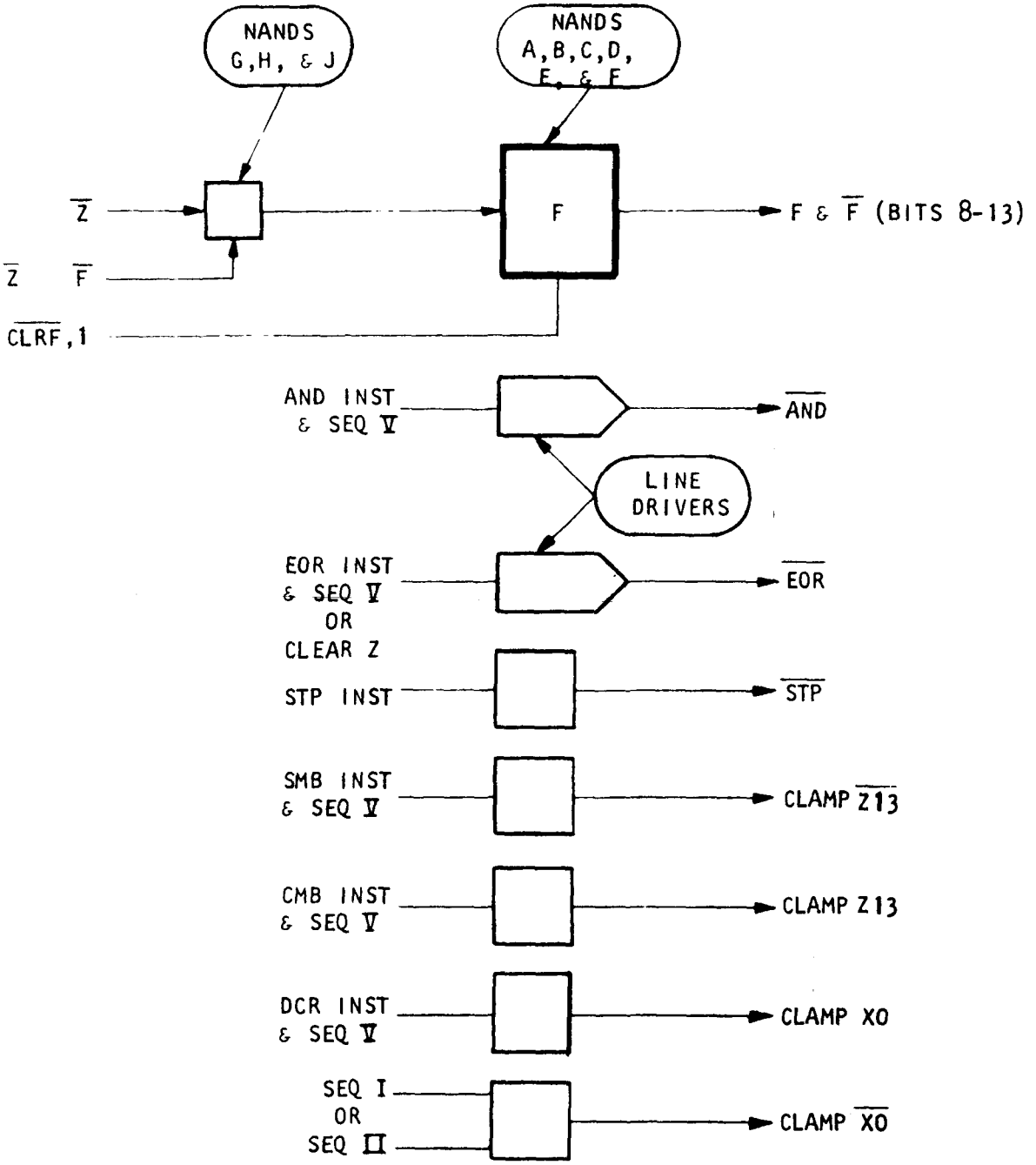
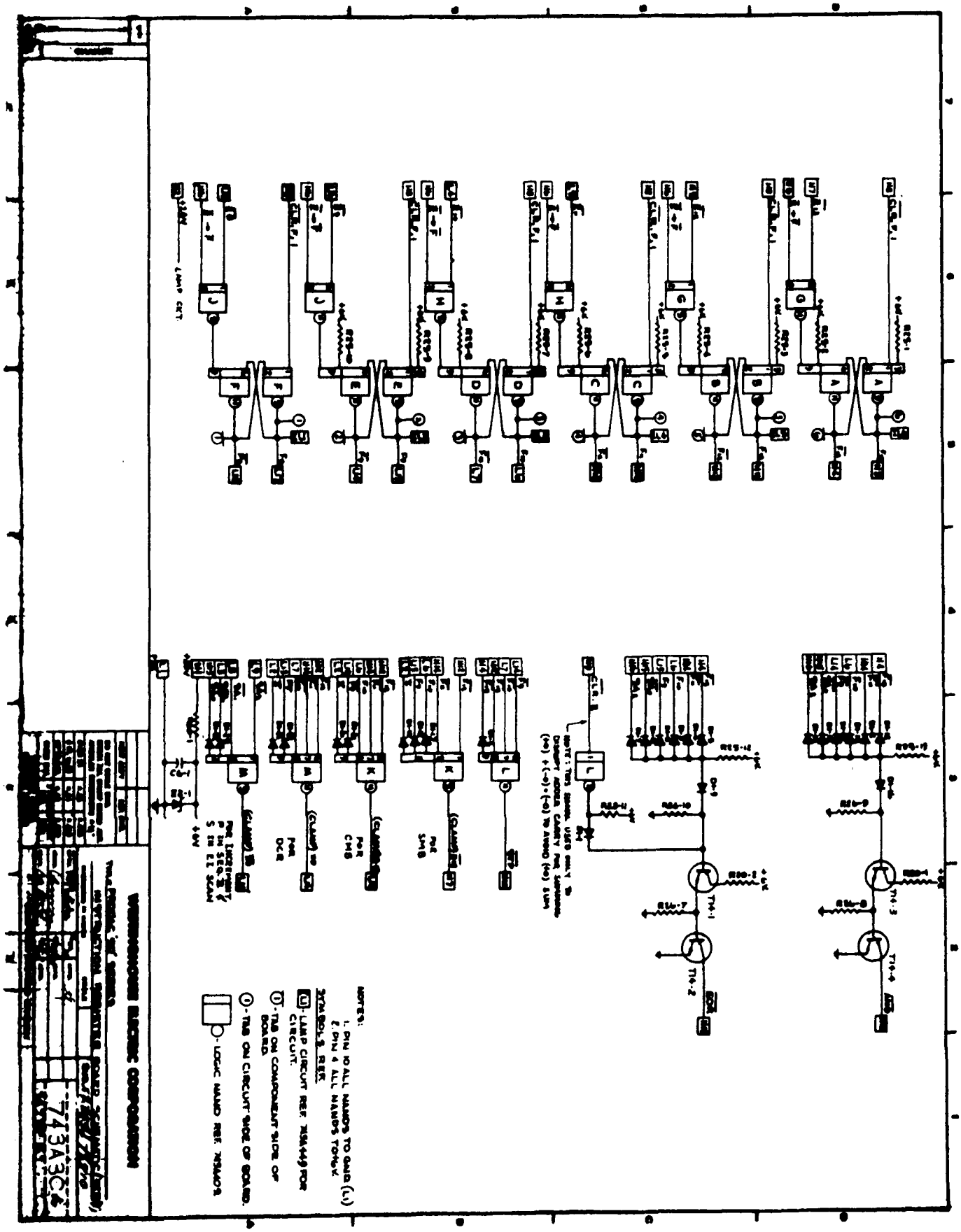
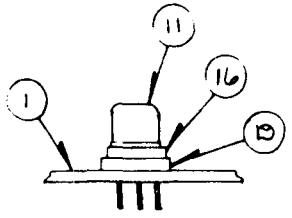
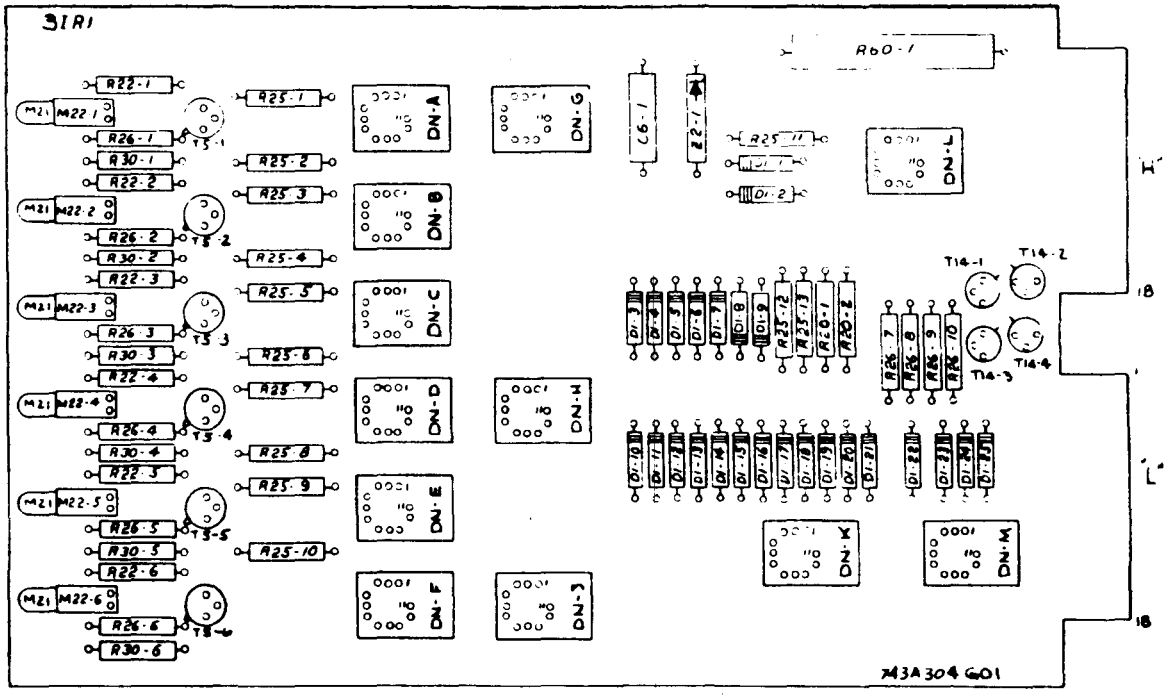

NANDS G,H, & J
NANDS A,B,C,D, E, & F
Z
F
F & F (BITS 8-13)
Z F
CLRF,1
AND INST & SEQ V
AND
LINE DRIVERS
EOR INST & SEQ V OR CLEAR Z
EOR
STP INST
STP
SMB INST & SEQ V
CLAMP Z13
CMB INST & SEQ V
CLAMP Z13
DCR INST & SEQ V
CLAMP XO
SEQ I OR SEQ II
CLAMP XO

Figure 3-30.





DETAILED ASSEMBLY OF TRANSISTORS (TYPE TO-18 CASE ONLY) & PADS (IT. 11 & 13) TO BOARD



SEE NOTE 9 OF SH 8

NEXT ASS'Y	REF DWG				
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°					
OVER 24	± .06	± .015			
6 IN. to 24	± .04	± .010			
UP TO 6 IN.	± .02	± .005			
BASIC DIM	2 PLACE DEC	3 PLACE DEC			
TOLERANCE UNLESS OTHERWISE SPECIFIED					

S.O.	IT	CHANGE			
1					

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
INST REG CARD ASSEMBLY (3IR1)

DIMENSIONS IN INCHES | SCALE | SUB. 1 2 3 4 5 6 7 8 9 10

DRWN		APPD			
CHKD		APPD			
QUPY		APPD			

743A304
SHEET 2 OF 8 SH.

COMPUTER SYSTEMS DIVISION PITTSBURGH PA. U.S.A.

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LOW VOLTAGE SENSOR 3LV2

A. GENERAL DESCRIPTION

The Low Voltage Sensor card contains three separate circuits which perform the following functions:

1. The Low Voltage Detection circuit detects excursions of the +26 voltage bus below safe operating levels and provides a signal to the Central Processor if this happens.

2. The Synchronizer Interrupt circuit acts as a real time clock for program timekeeping purposes.

3. The Dead Computer Switch circuit monitors operation of certain hardware and software functions, and provides contacts available for alarm and control purposes in the event of certain classes of computer malfunction.

B. CIRCUIT OPERATION

1. Circuit Description - Low Voltage Circuit

Drawing 743A340 shows the low voltage detection circuit in the upper center. Input to the circuit is the +26VDC to PSC (i.e., unregulated +26V bus voltage) appearing between x30 and x18-x20. M12-1 is adjusted to turn T8-1 on when the bus voltage drops to 23.6V. T8-1 then turns on T5-2 which grounds the base of T5-3 turning T5-3 OFF. The collector of T5-3 is raised to bus voltage by R53-1, and an external interrupt, PFAL INT, is generated. Also, T5-4 is now turned ON thus grounding the base of T5-3 and holding it OFF. Approximately 6 milliseconds later, relay M7-1 which has been held energized by capacitor C26-1 drops out, and the NC contacts are closed as indicated.

M19-1 is used to precisely set time delay from start of power supply failure interrupt until closing of power supply fault relay contact. This time delay is set between 7.2 and 8.0 ms and compensates for variations in parameters such as relay M7-1 dropout time and current, capacitor C26-1 value, and resistor R52-3 value.

When the relay armature transfers to the NC side, base drive is removed from T5-4 and this transistor turns OFF. This removes the ground from the base of T5-3 and enables the circuit to respond to a +26 voltage bus level above +22.9 volts. R30-1 is a feedback resistor which provides approximately 1.2 volts of hysteresis. Thus T8-1 turns OFF when the +26 voltage bus reaches about 24VDC.

2. Circuit Description - Synchronizer Interrupt

The Synchronizer Interrupt circuit is also located on the Low Voltage Sensor card diagram upper left hand corner. T5-1 is turned ON and OFF 60 times each second by the 6.3VAC 60CPS voltage applied to the transistor's base through R23-1 and D7-1. Since the collector of T5-1 is returned to +26V through R52-2, the collector is alternately at near PSC potential and then +26VDC generating an external interrupt (labeled SYNC INT) used by computer programs for internal timekeeping functions.

R23-1 limits current into the base of T5-1, and diode D7-1 prevents the base-emitter junction from being stressed by a high reverse voltage during negative alternations of the input voltage.

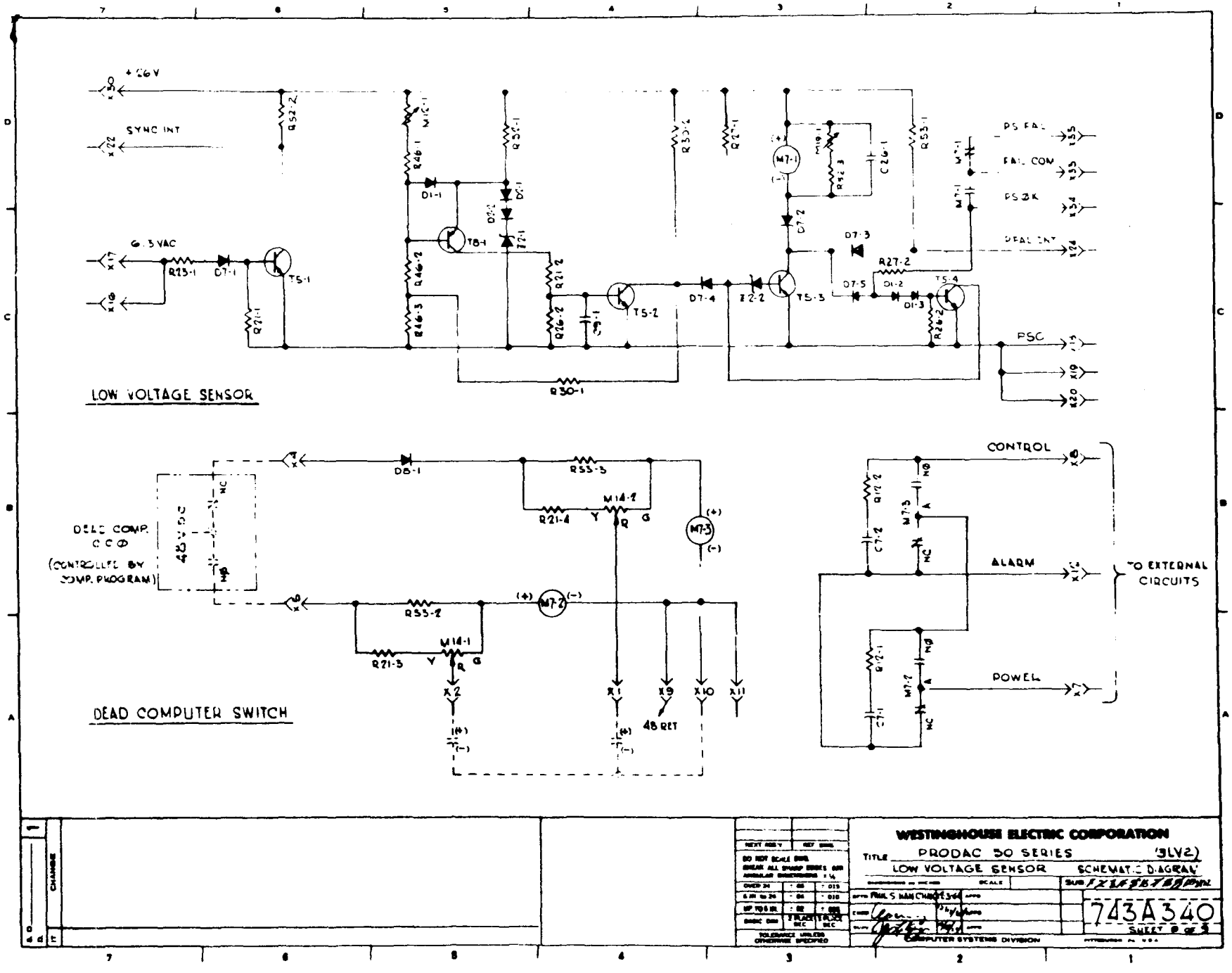
Under certain conditions, it is desirable to have a synchronizer interrupt rate of 120 pulses per second. To achieve this, the 60CPS voltage is rectified in a bridge circuit and the pulse D.C. output is applied to the base of T5-1 for a 120 PPS interrupt rate.

3. Circuit Description - Dead Computer Switch

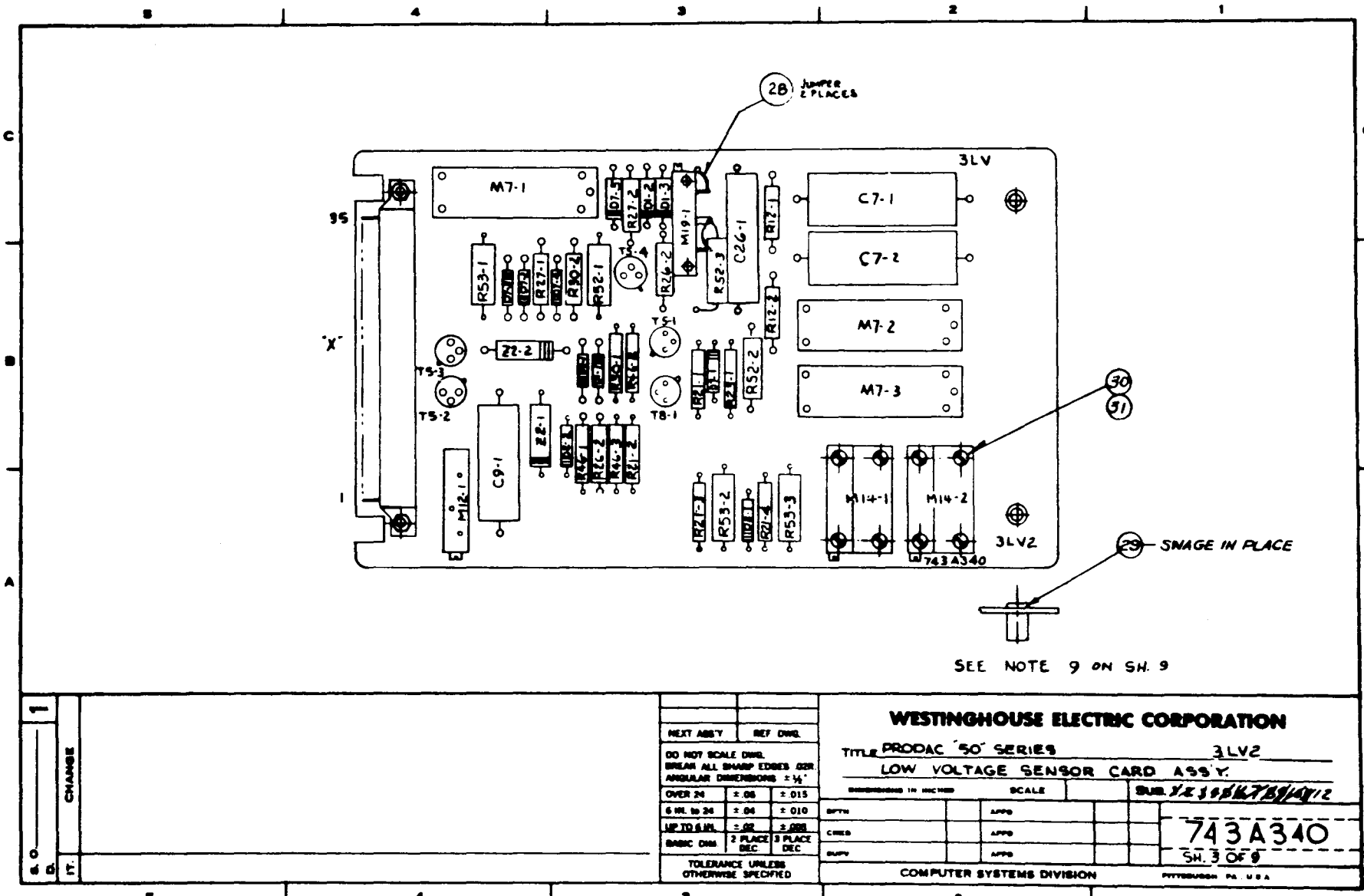
The third functional circuit located on the Low Voltage Sensor card is the Dead Computer Switch. This circuit's output depends on the state of the two relays, M7-2 and M7-3. The relays are single side stable and arranged such that if either relay is in the de-energized state, continuity exists between the POWER connection and the ALARM connection. When both relays are energized, the POWER connection is coupled to the CONTROL output. Power input is furnished by an external source and ALARM and CONTROL functions are determined by the computer user. (Relay contact ratings are identical to CCØ ratings, namely 500 volts maximum, 2 amperes maximum or 100VA maximum. However, large inductive loads must be shunted by suppression diodes.)

+48VDC is applied to the relays alternately by a contact output. Each relay has an external capacitor in parallel with it. This capacitor charges up and holds the relay energized while the CCØ is applying power to the other relay-capacitor combination. If for some reason the Dead Computer Switch CCØ does not return to the other side at the end of the switching internal, the relay will "time out" and close the ALARM circuit.

M14-1 and M14-2 are voltage dividers used to adjust the charge-discharge cycle of the capacitors. This determines what the period of the CCØ switching cycle must be. (Maximum period is 2 seconds or 1 second between contact transfers, and minimum period is 1 second or 0.5 second between contact transfers.) Diode D8-1 is an isolating diode that makes it possible to take an external interrupt from the anode of D8-1 if desired. C7-1 and R12-1, and C7-2 and R12-2 are filters across the relay contacts. These are for contact protection, although as noted above these filters are not adequate protection against large inductive loads. Relay M7 is a single side stable relay with a coil resistance of 675 ohms. "Must operate" voltage is 8.6VDC.



WESTINGHOUSE ELECTRIC CORPORATION			
TITLE PRODAC 50 SERIES (3LV2)			
LOW VOLTAGE SENSOR SCHEMATIC DIAGRAM			
COMPUTER SYSTEMS DIVISION		743A340	SHEET 8 OF 8


28 JUMPER 2 PLACES
3LV
M7-1
C7-1
C7-2
M7-2
M7-3
C26-1
C9-1
M14-1
M14-2
3LV2
743A340
30
31
29 SNAGE IN PLACE
SEE NOTE 9 ON SH. 9
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC "50" SERIES 3LV2
LOW VOLTAGE SENSOR CARD ASS'Y.
743A340
SH. 3 OF 9
COMPUTER SYSTEMS DIVISION

DIODE BOARDS 2MA1, 2MB1

A. GENERAL DESCRIPTION

These two boards are required to contain the blocking diodes and the transformers for the half-select matrix.

The relationship of the diode boards to the system is shown in Figure 3-31.

B. CIRCUIT OPERATION

1. Circuit Specifications

The primary windings of the half-select transformers are driven by the pulsers and the sub-row half-select switches. The secondary windings together with the subcolumn half-select switches provide a current path through the core windings. A damping resistor is placed across the secondary of the transformer to prevent excessive inductive flyback. The sub-column diode matrix is connected directly to the core stack in the manner shown on the drawing. The primary consideration in the grouping of the core windings is the geometry of the printed circuit layout.

2. Circuit Description

The card block diagram is shown in Figure 3-32. Each half-select transformer drives 8 core half-select lines. The subcolumn diodes are connected in groups of eight on each diode board and then connected to the eight subcolumn half-select switches.

3. Diode Identification

Figures 3-33 and 3-34 show the layout of the MA and MB boards which identify the diodes with respect to the X matrix or Y matrix. For example, looking at the MA schematic, the diodes marked X36 are tied to ØØ3ØW and ØØ3ØR. On Figure 3-33, these can be physically located at the upper right hand side of the drawing (and the board itself) by noting the number (36) shown between two lines (these indicate the diodes), and whether it is the read or write diode by the R or W identification.

The figure is broken down into an X matrix or Y matrix by the solid line extending (in stair-case fashion) across the board.

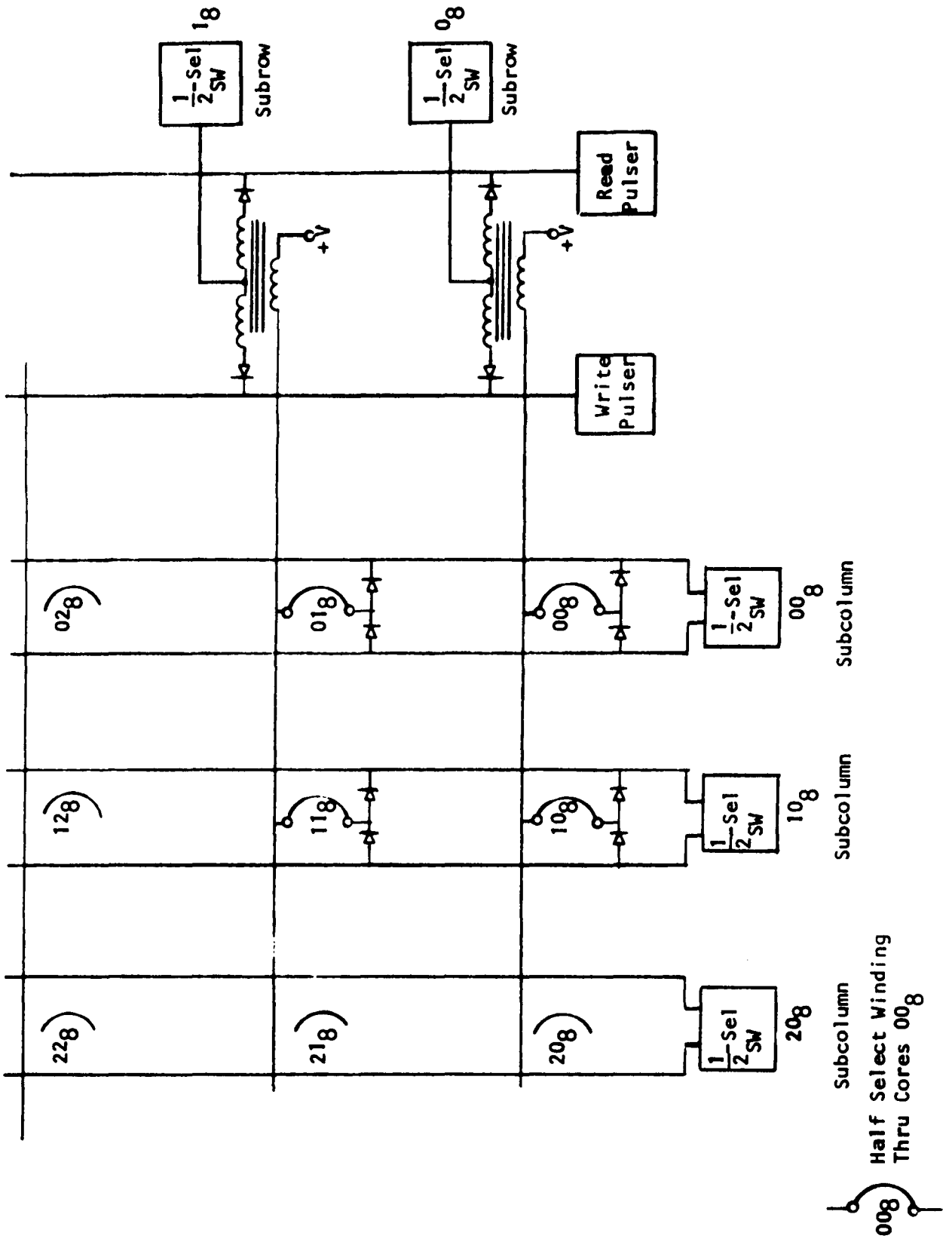


Figure 3-31. PRODAC Half-Select Scheme Typical Partial View for Least-Significant Half-Address of One Stack

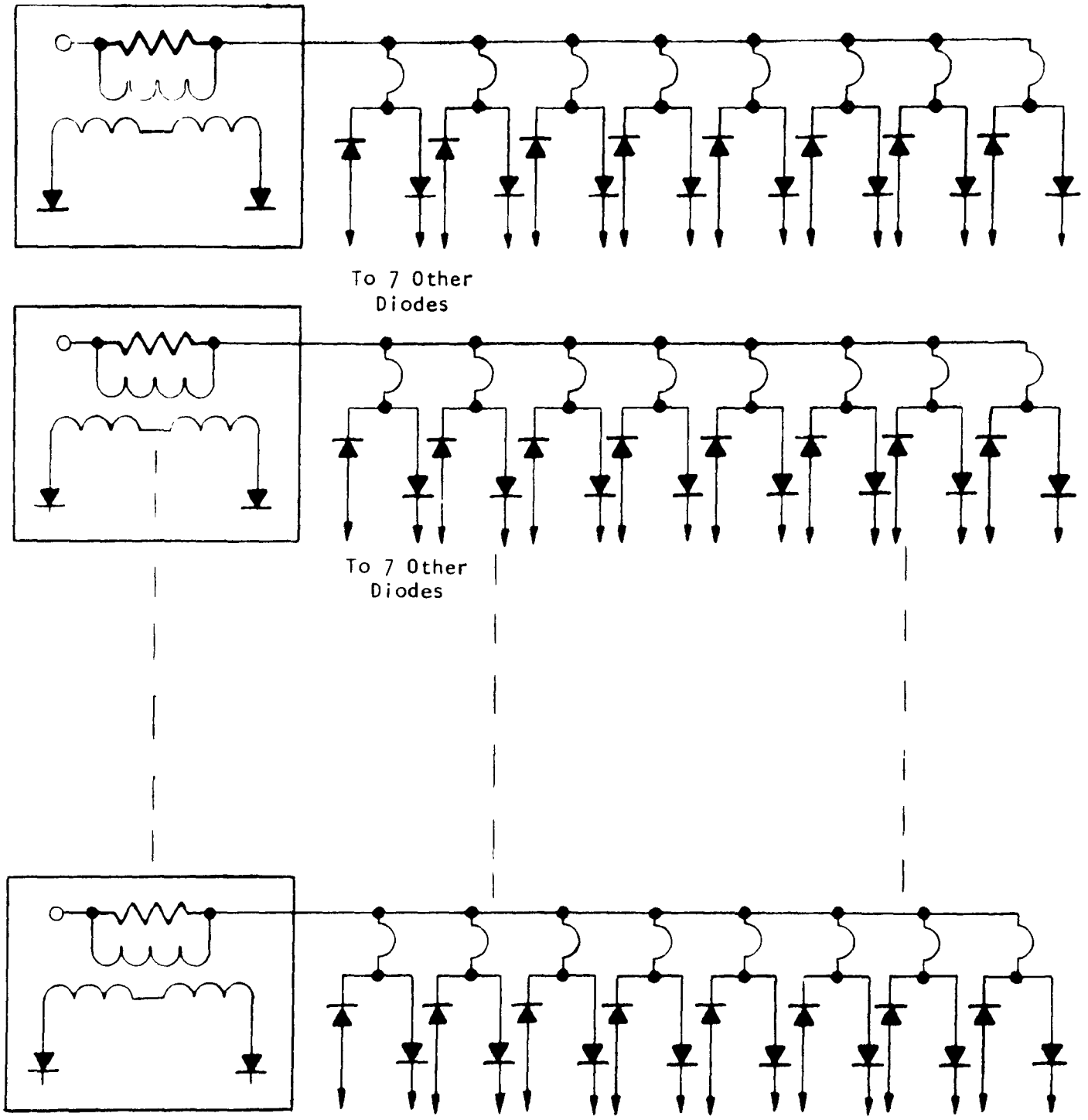


Figure 3-32.

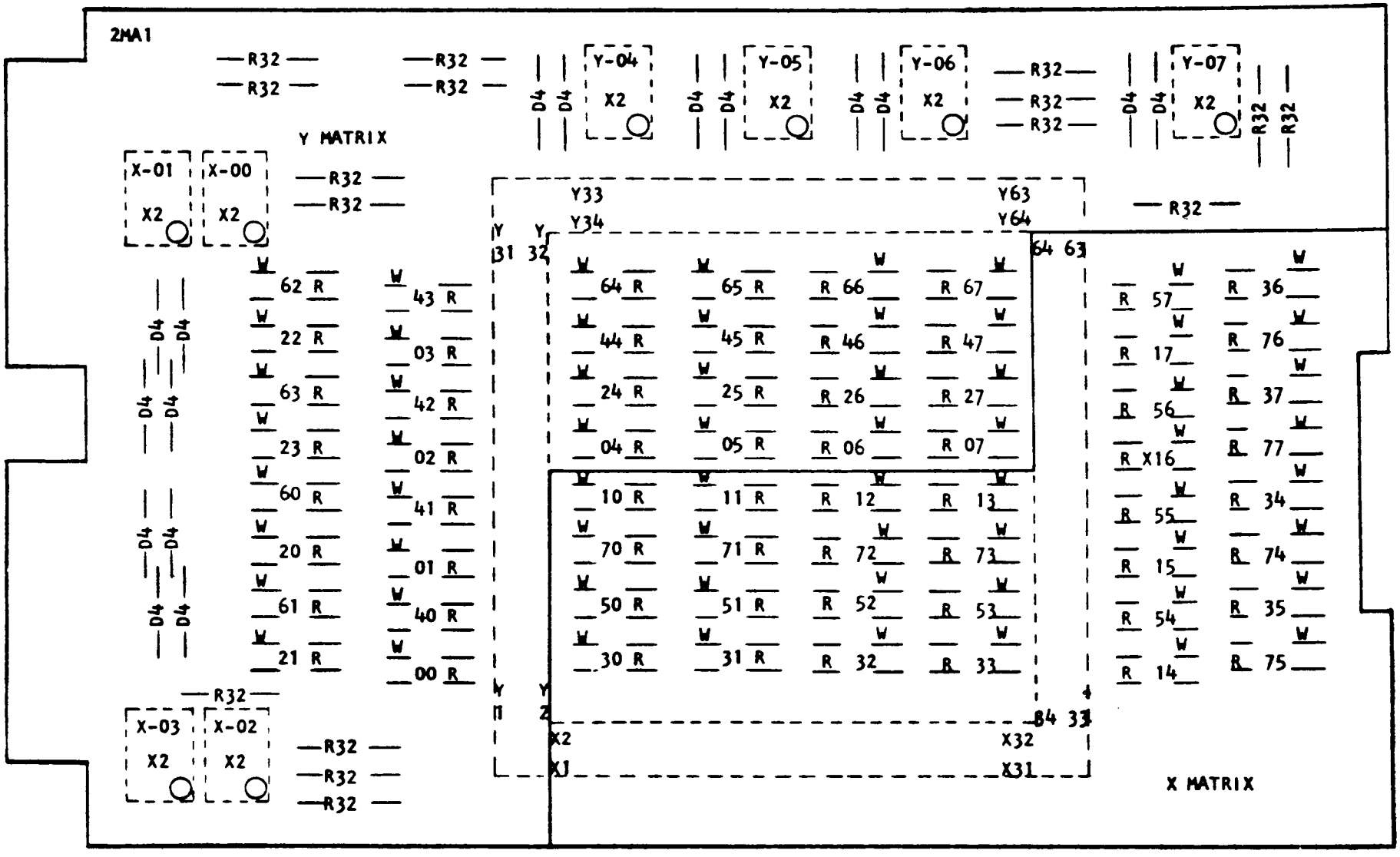


Figure 3-33. Diode Identification - 2MA

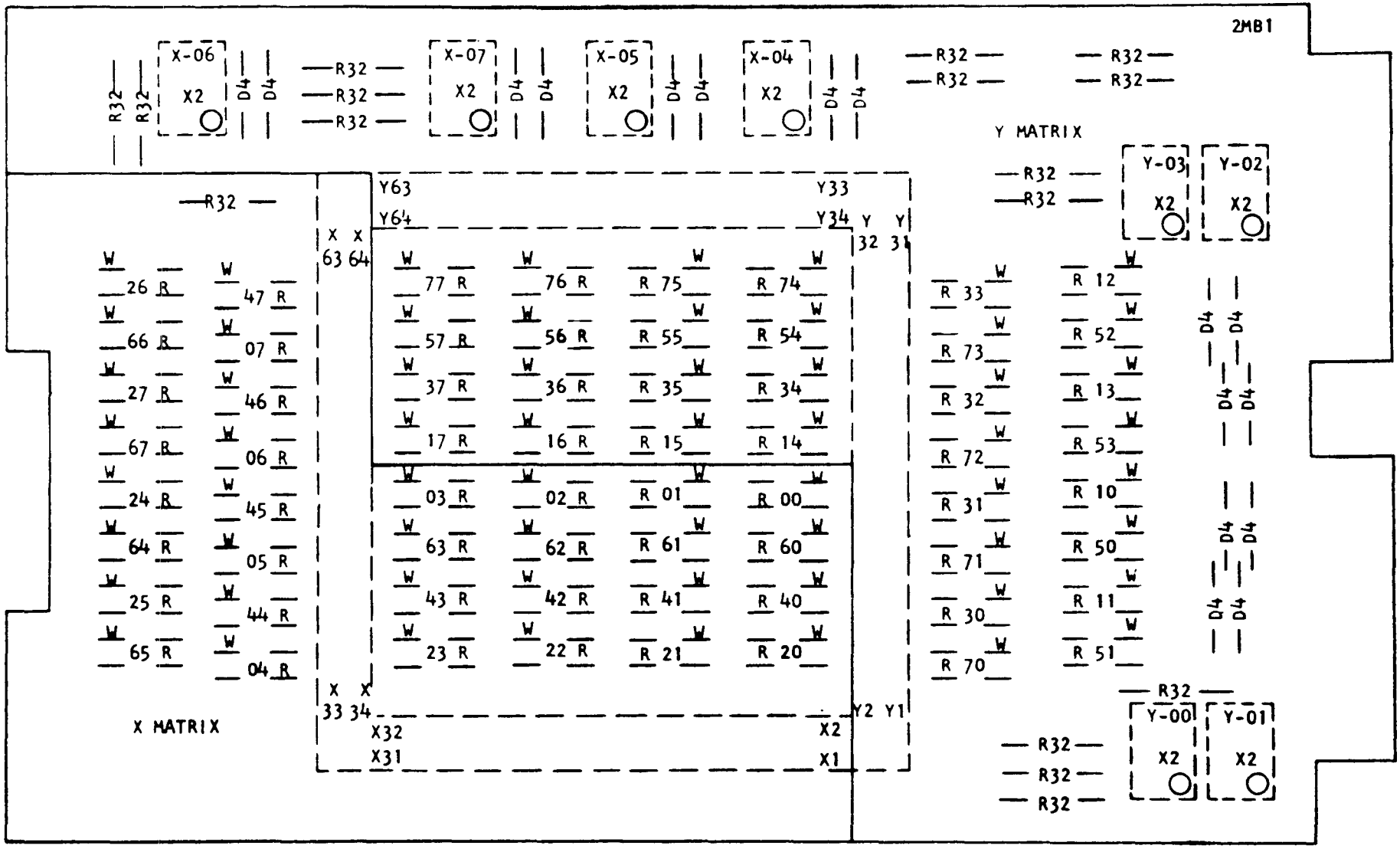
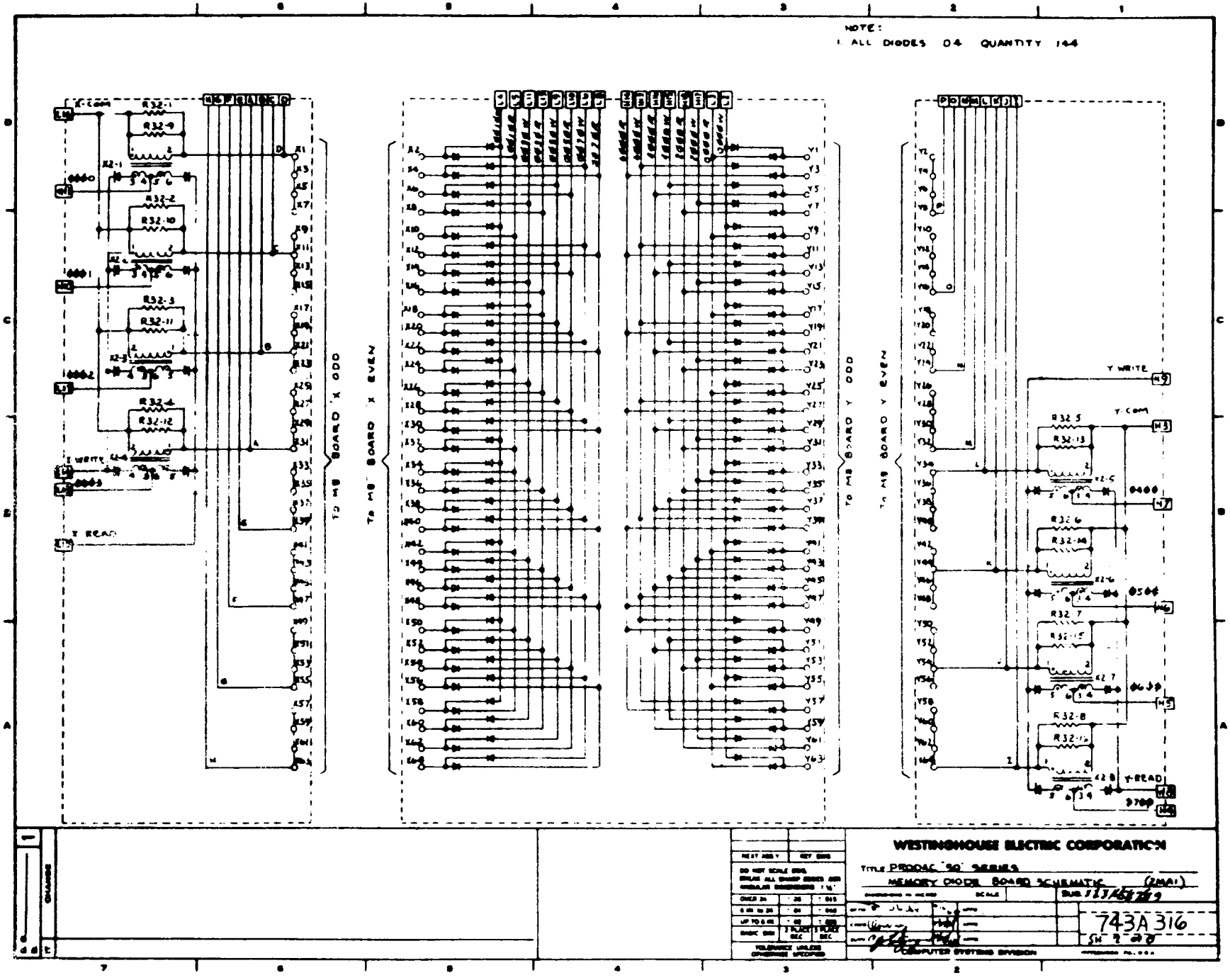
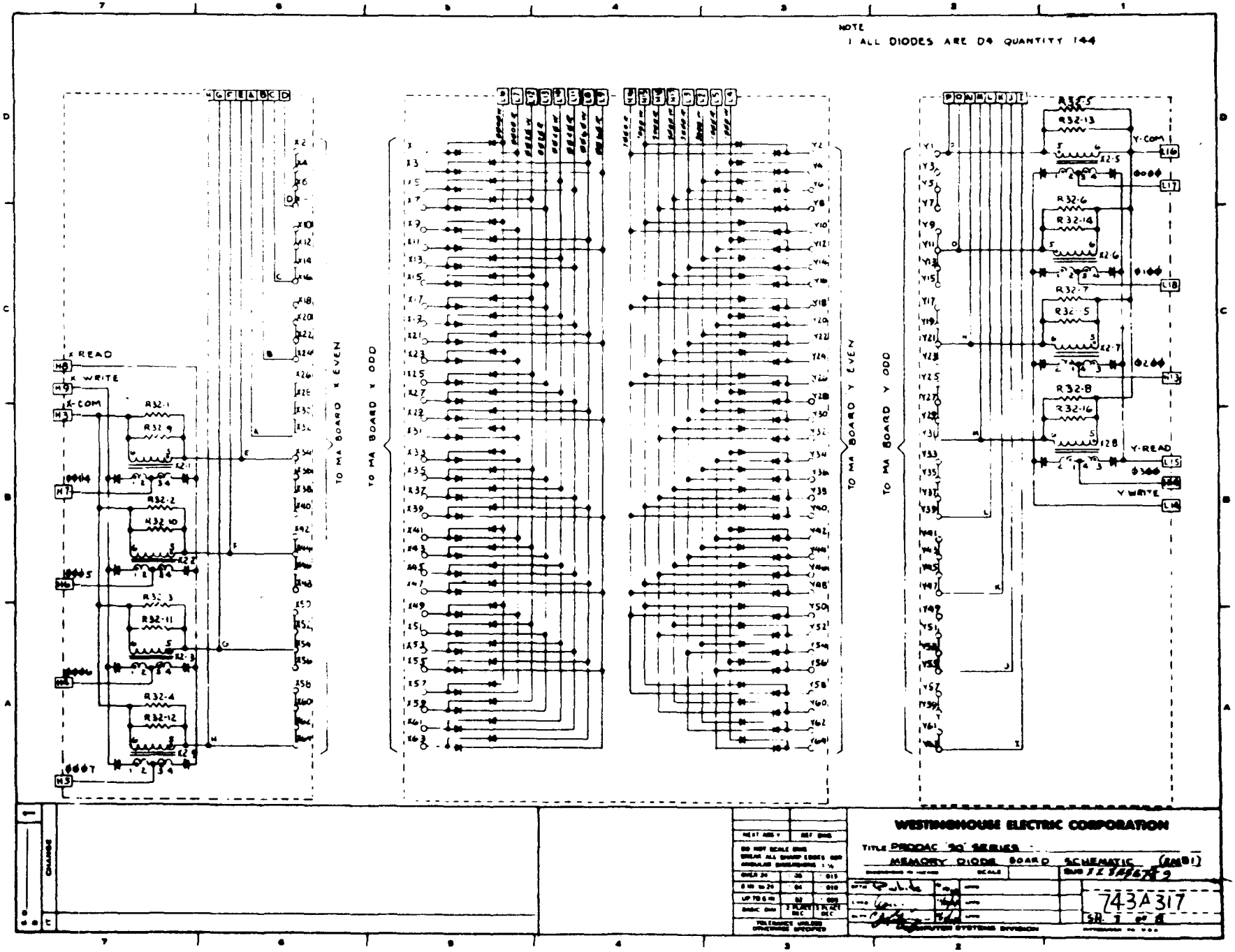
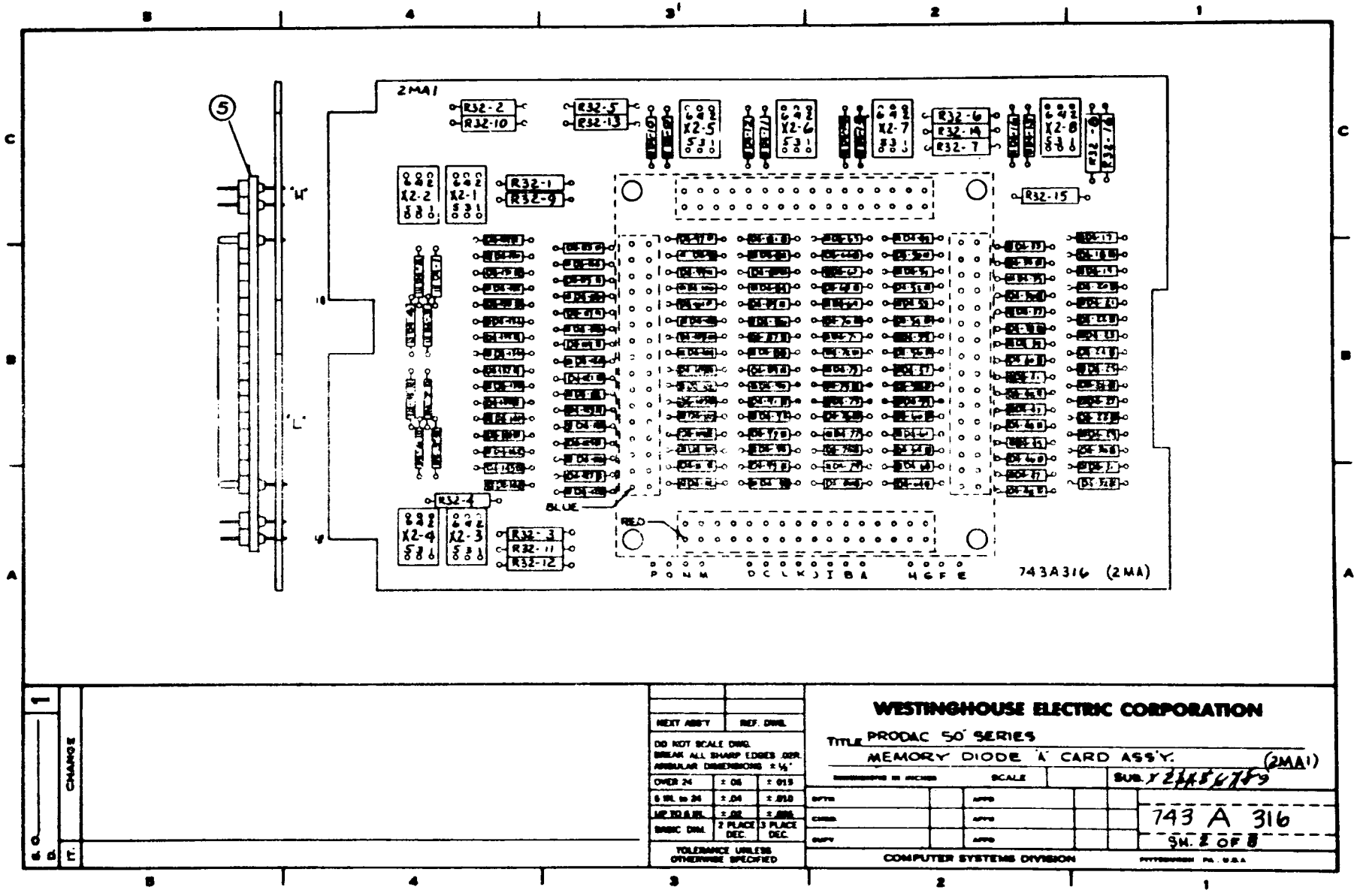
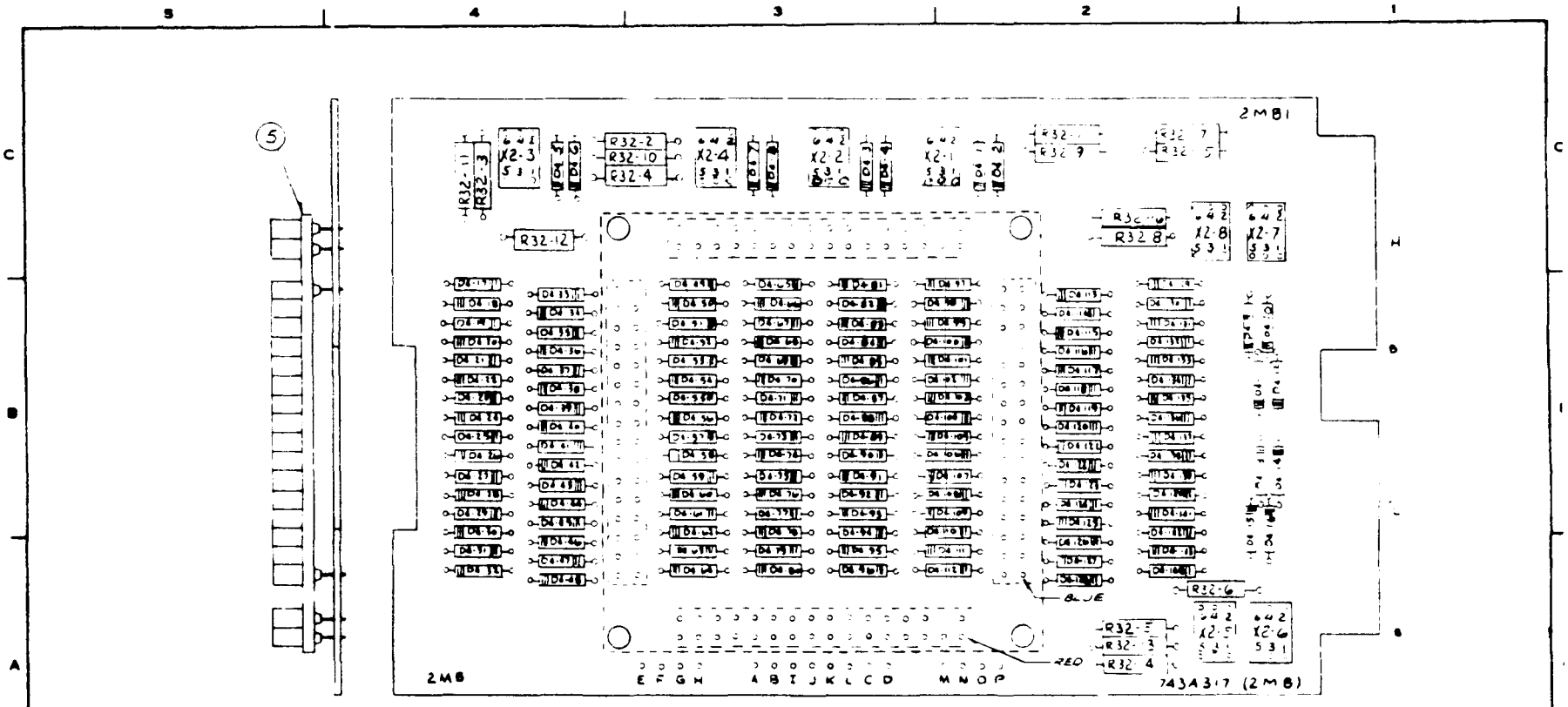


Figure 3-34. Diode Identification - 2MB


NOTE:
1. ALL DIODES 04 QUANTITY 144
X COM
R32-1
R32-9
R32-2
R32-10
R32-3
R32-11
R32-4
R32-12
X WRITE
X READ
TO M8 BOARD X EVEN
TO M8 BOARD X ODD
TO M8 BOARD Y EVEN
TO M8 BOARD Y ODD
Y WRITE
Y COM
R32-5
R32-13
R32-6
R32-14
R32-7
R32-15
R32-8
R32-16
Y READ
WESTINGHOUSE ELECTRIC CORPORATION
Title PRODAC '50' SERIES
MEMORY DIODE BOARD SCHEMATIC (2MAT)
743A316
COMPUTER SYSTEMS DIVISION


NOTE
1 ALL DIODES ARE D9 QUANTITY 144
X READ
X WRITE
X-COM
R32-1
R32-9
R32-2
R32-10
R32-3
R32-11
R32-4
R32-12
TO MA BOARD X EVEN
TO MA BOARD X ODD
TO MA BOARD Y EVEN
TO MA BOARD Y ODD
Y-COM
R32-13
R32-6
R32-14
R32-7
R32-15
R32-8
R32-16
Y-READ
Y WRITE
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 90 SERIES
MEMORY DIODE BOARD SCHEMATIC
743A317


2MA1
R32-2
R32-10
R32-5
R32-13
X2-5
X2-6
X2-7
X2-8
R32-6
R32-14
R32-7
R32-15
X2-2
X2-1
R32-1
R32-9
R32-4
X2-4
X2-3
R32-3
R32-11
R32-12
BLUE
RED
P O N M D C L K J I B A H G F E
743A316 (2MA)
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES
MEMORY DIODE 'A' CARD ASS'Y. (2MA1)
SCALE
SUB. X2345679
743 A 316
SH. 2 OF 8
COMPUTER SYSTEMS DIVISION
NEXT ASS'Y
REF. DWG.
DO NOT SCALE DWG.
BREAK ALL SHARP EDGES .025R.
ANGULAR DIMENSIONS ± ½°
OVER 24 ± .06 ± .015
6 thru 24 ± .04 ± .010
UP TO 6 IN. ± .02 ± .005
BASIC DIM. 2 PLACE DEC. 3 PLACE DEC.
TOLERANCE UNLESS OTHERWISE SPECIFIED
CHANGE
S.O.
E.C.



SEE NOTE 9 SH 8

NEXT ASS'Y		REF DWG	
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN to 24	± .04	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM	2 PLACE DEC	3 PLACE DEC	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
MEMORY DIODE B CARD ASS'Y. (2MB1)

DIMENSIONS IN INCHES | SCALE | SUB X A B 4 5 6 7 8 9

DRWN | APPD
CHKD | APPD
SUPV | APPD

743A317
SH 2 OF 8

COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

1 | CHANGE | 0 | S.O. | IT

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MEMORY ENABLE BOARD 2ME2

A. GENERAL DESCRIPTION

The ME board performs or provides several important functions: memory enable decode and drive, select accumulator decode and drive, select program counter decode and drive, select S register decode and drive, inversion of return jump instruction decode, interrogate pulser timing and core strobe gate drive. (Figure 3-35).

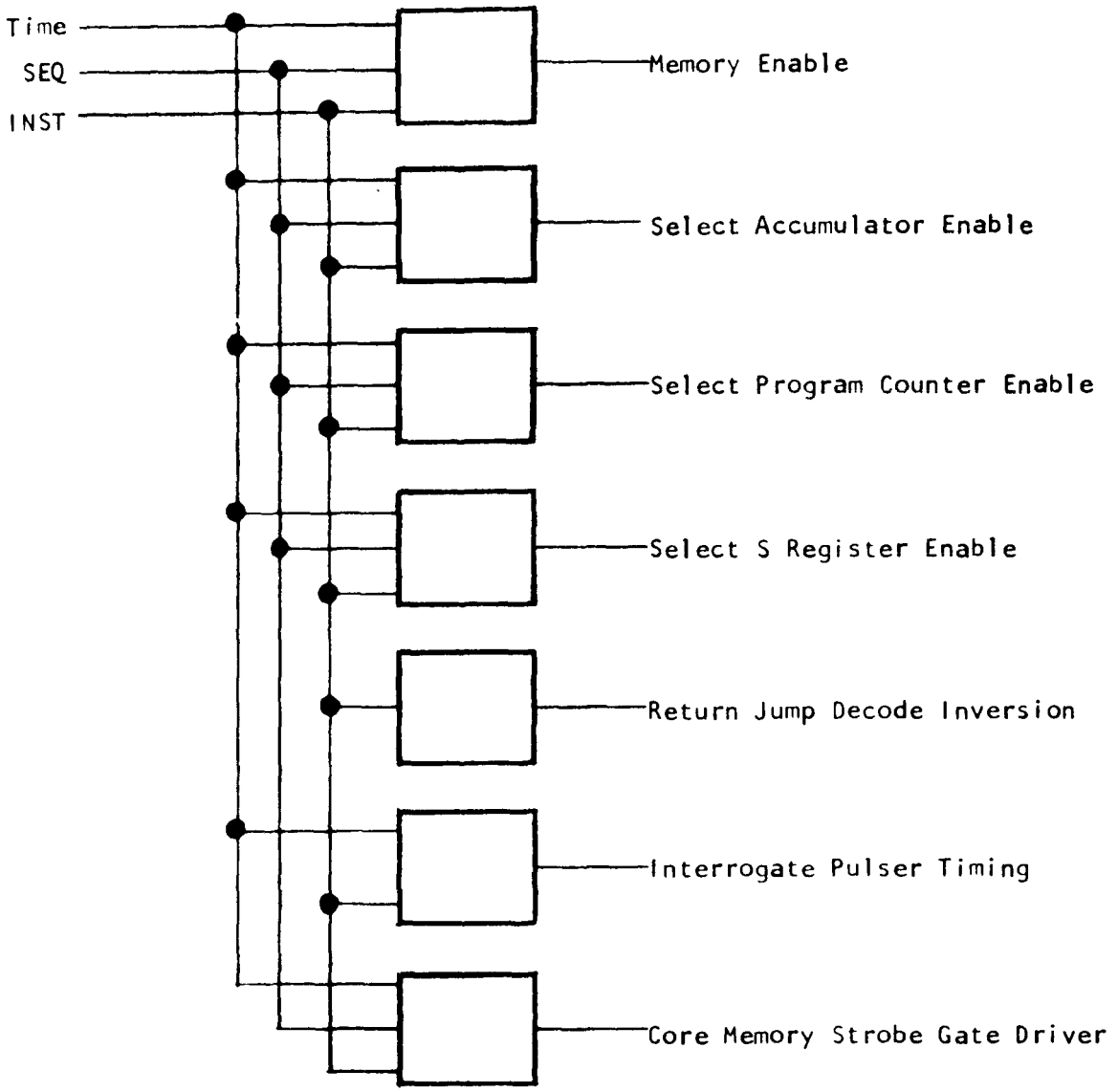


Figure 3-35. Memory Enable Board

B. CIRCUIT DESCRIPTION

Memory Enable Decode Drive: Consists of NAND B-11, E5 and E11. B-11 disables memory during Sequence VI of an output instruction. E5 disables memory during an external interrupt scan. E11 disables memory during Sequence V of an input instruction.

Select Accumulator Decode Drive: (SEL A) Consists of NAND J and L5. J11 selects accumulator during Sequence V of OUT and STL instructions. J5 selects accumulator during Sequence VI of ADD, AND, INP, SUB, EOR, and ENL instructions. L5 is a logic inverter.

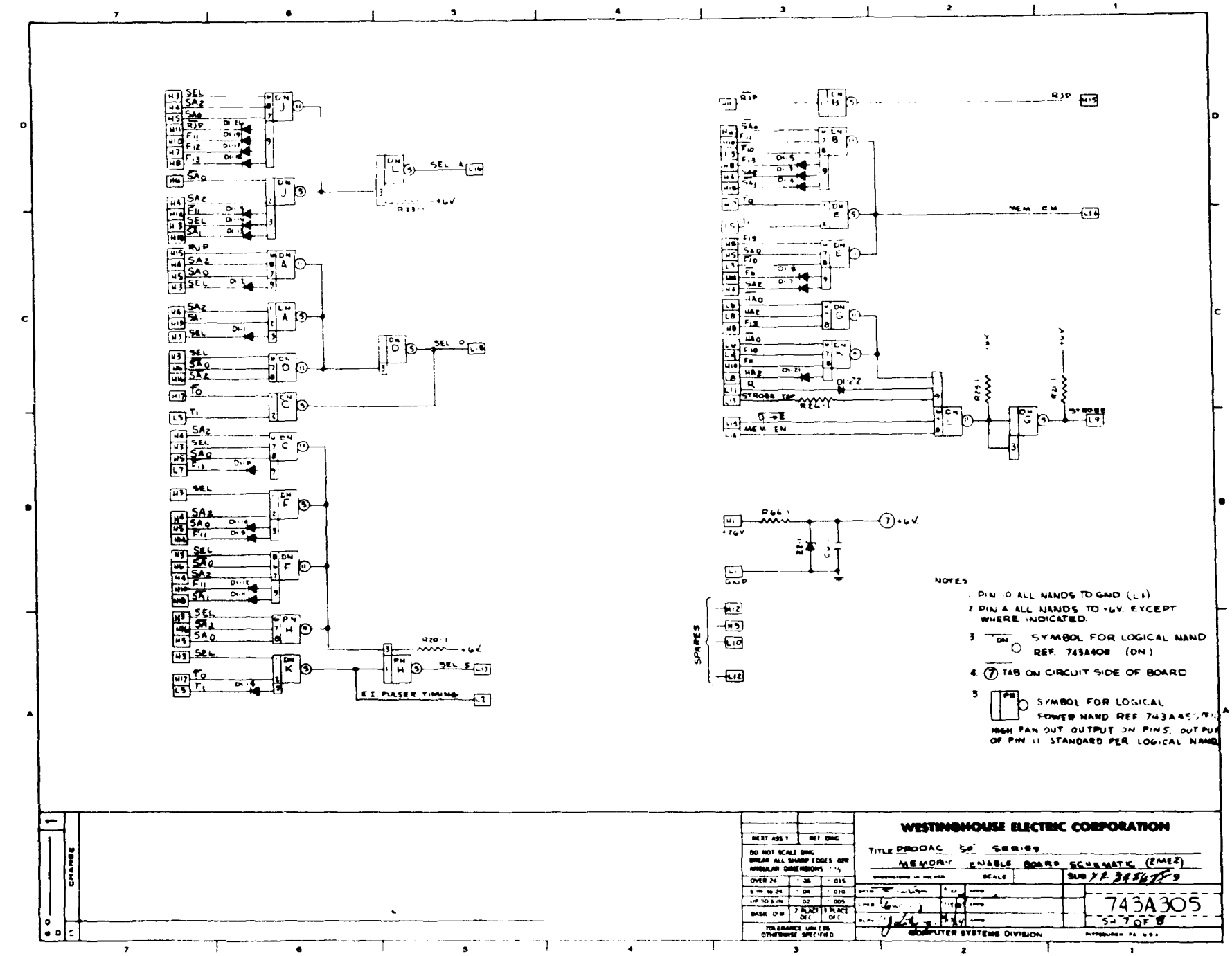
Select Program Counter Decode Drive: (SEL P) Consists of NAND A, D, and C5. A11 selects P (program counter) during Sequence V of an RJP instruction. A5 selects P during Sequence VII. D11 selects P during Sequence II. D5 is a logic inverter. C5 inhibits the selecting of P during an interrupt scan.

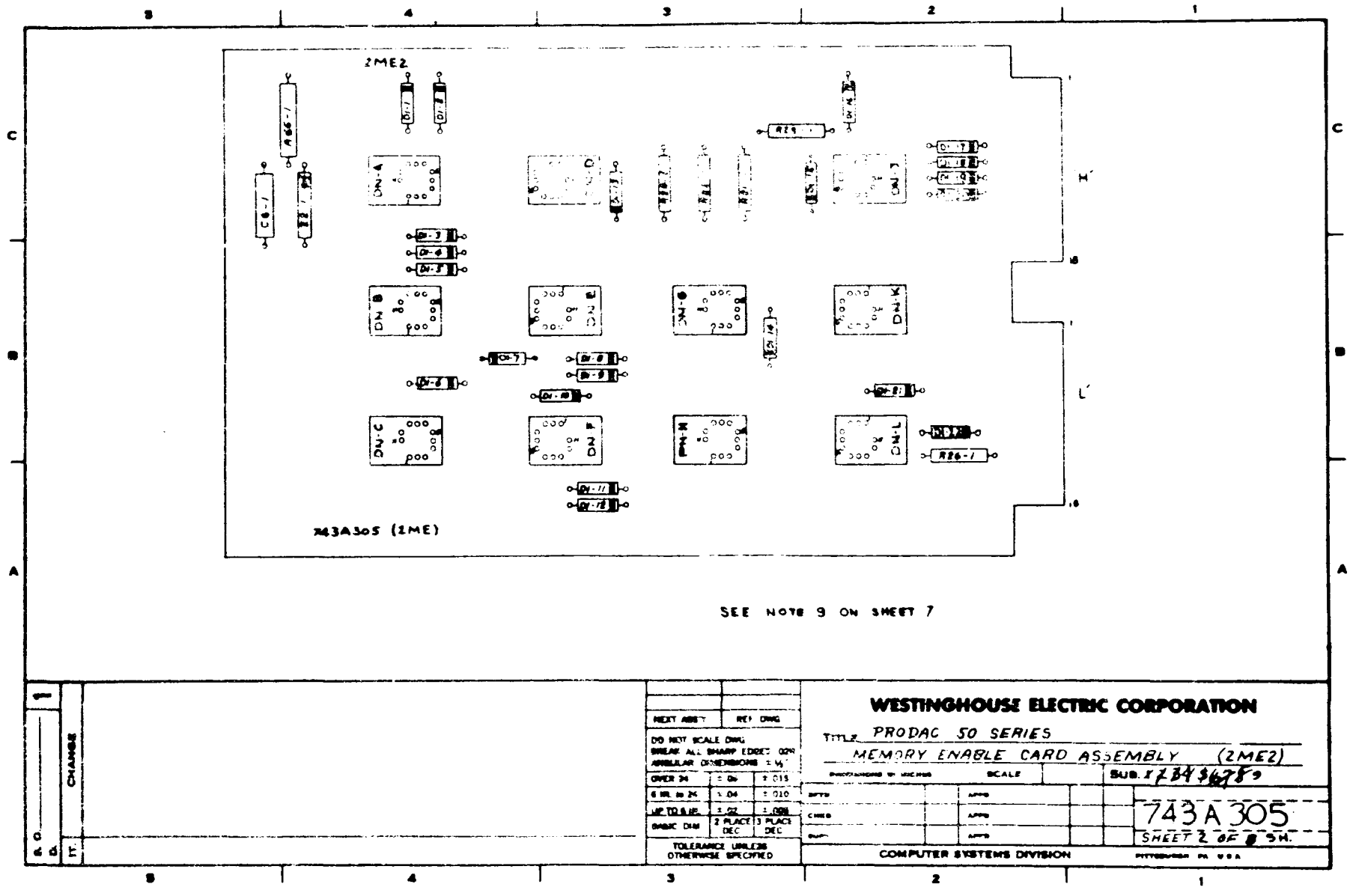
Select S Register Decode Drive: (SEL S) Consists of NAND C11, F, H and K5. C11 and F5 select S during Sequence V of all instructions except OUT, RJP, and STL. F11 selects S during Sequence VI of LSH, RSH, OUT, RJP, and STL instructions. H11 selects S during Sequence III. K5 selects S during an external interrupt scan. H5 is a power logic inverter.

Return Jump Inversion: B5 is a logic inverter.

Interrogate Pulser Timing: Consists of NAND K5. This NAND (K5) also is used to time the external interrupt interrogate pulser.

Core Strobe Gate Driver: Consists of NAND G, K11 and L11. G11 inhibits strobe during Sequence VI of INP, STL, OUT, RJP, and STL instructions. K11 inhibits strobe during Sequence VI of SDR, LSH, RJP, and STL instructions. L11 is a decoding delay line tap amplifier which inhibits strobe when memory is disabled. G5 has extra base drive in order to drive many additional outputs.


SEL A
SEL D
SEL E
EI PULSER TIMING
MEM EN
STROBE
NOTES
1. PIN 10 ALL NANDS TO GND (L1)
2. PIN 4 ALL NANDS TO +6V. EXCEPT WHERE INDICATED.
3. SYMBOL FOR LOGICAL NAND REF. 743A408 (DN)
4. (7) TAB ON CIRCUIT SIDE OF BOARD
SPARES
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES
MEMORY ENABLE BOARD SCHEMATIC (EMEB)
743A305
SH 1 OF 8
COMPUTER SYSTEMS DIVISION


2ME2
743A305 (1ME)
SEE NOTE 9 ON SHEET 7
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES
MEMORY ENABLE CARD ASSEMBLY (2ME2)
SCALE
SIZE B
743A305
SHEET 2 OF 8 SH.
COMPUTER SYSTEMS DIVISION
PITTSBURGH PA U.S.A.
CHANGE
TOLERANCE UNLESS OTHERWISE SPECIFIED

PERIPHERAL DRIVER CARD 2PD1

A. GENERAL DESCRIPTION

The circuits on this card provide isolation between the subcolumn half-select switches and the peripheral equipment. In the absence of the peripheral drivers, cable capacitances would present low impedance paths to the currents in the high speed half-select systems and would cause excessive ringing. Since both the current amplitude and current rise time are critical in the central processor half-select applications, it is desirable to isolate the peripheral cables from the half-select switches. In I/O applications neither the amplitudes nor the rise times of the voltage waveforms are critical.

The relationship of the Peripheral Drivers to the rest of the system is shown in Figure 3-36. The inputs to the Peripheral Drivers are the output lines of the subcolumn half-select lines. The SEL pulse from the timing card and the Word and Channel Pulser timing pulse together enable the peripheral driver circuits. The Peripheral Drivers and the Subrow half-select switches form the input-output half-select matrix.

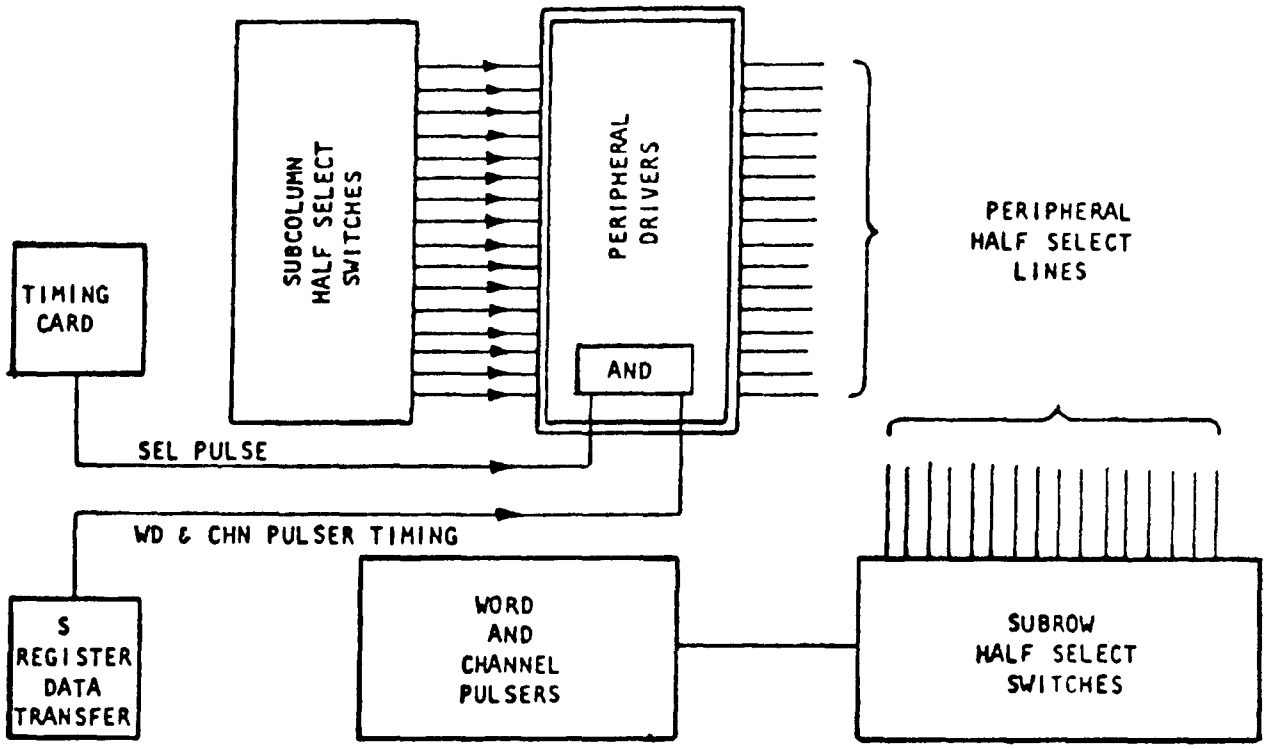


Figure 3-36.

B. CIRCUIT OPERATION

1. Circuit Specification

The inputs to the Peripheral Drivers are obtained at the common collector output stage of the subcolumn half-select switches. The $\overline{SEL}$ and WD & CHN pulser timing inputs are logic levels.

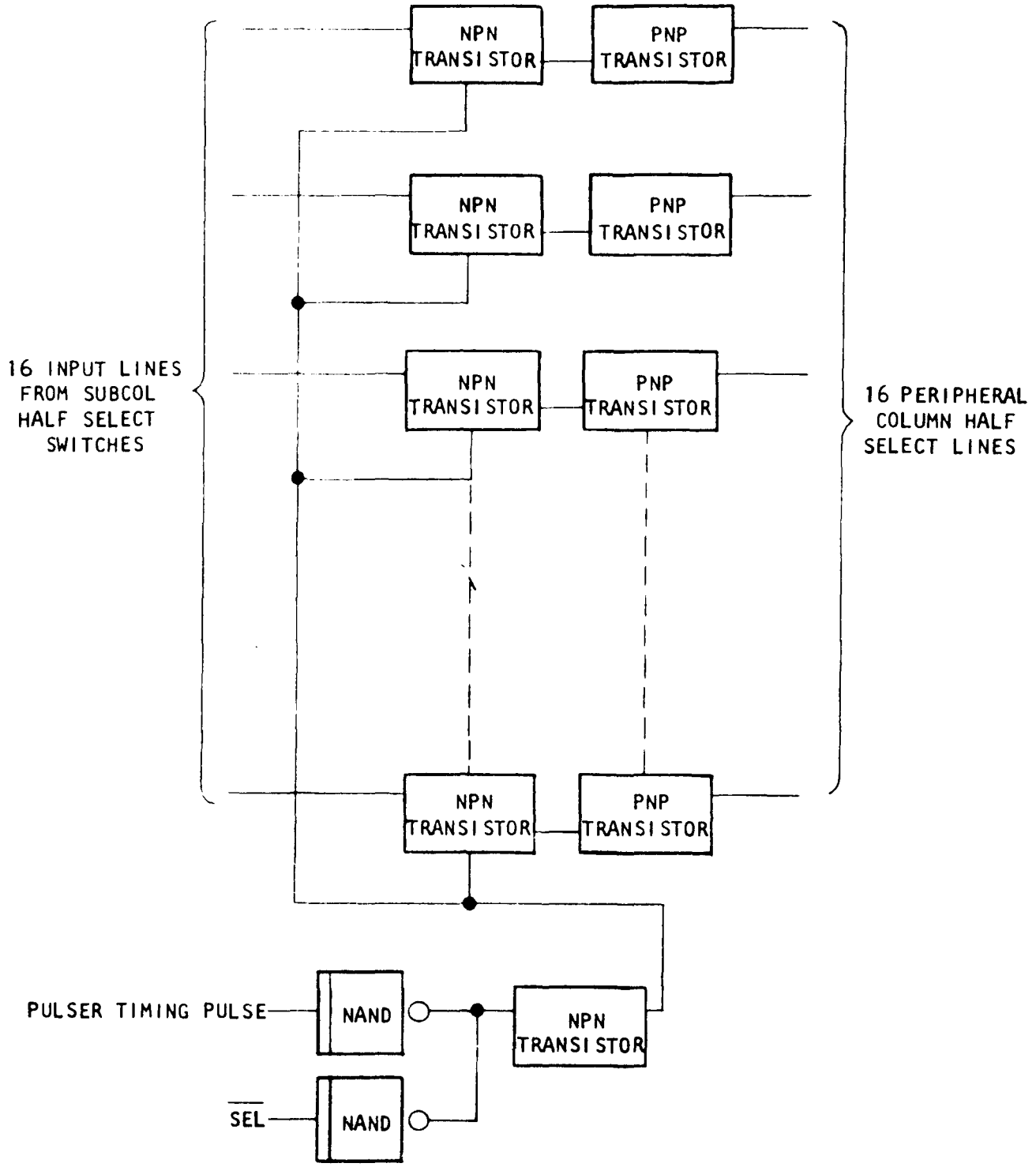


Figure 3-37.

2. Circuit Description

The Card block diagram is shown in Figure 3-37. Corresponding to the 16 subcolumn half-select switches there are 16 Peripheral Driver circuits on the card. Each circuit consists of an output transistor (PNP) that is driven by an NPN stage. The Peripheral Driver circuits are gated by means of a gating transistor that provides the emitter currents for the NPN stages. This gating transistor is driven by the logical sum of $\overline{SEL}$ and the External Pulser timing pulse - WD & CH.

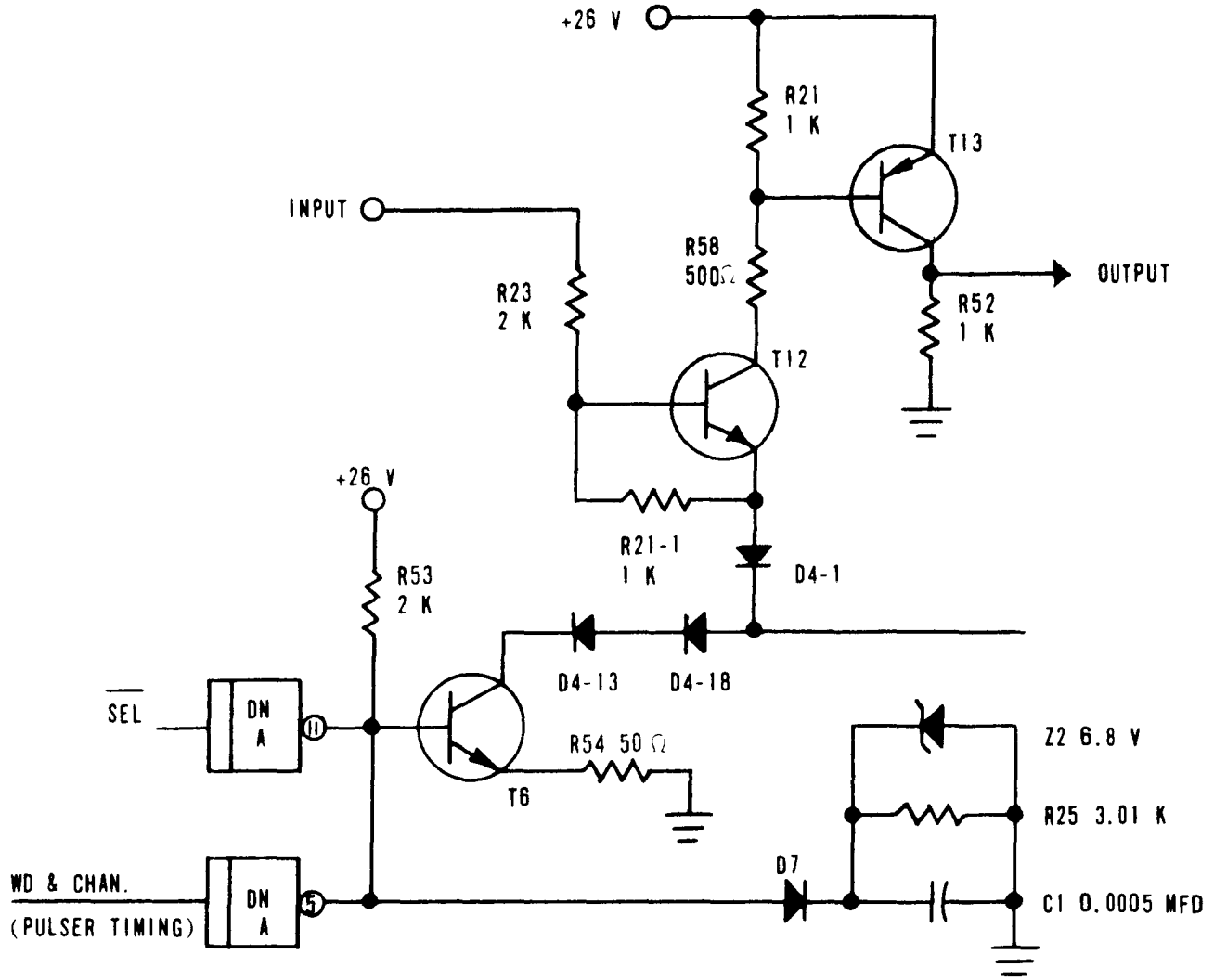
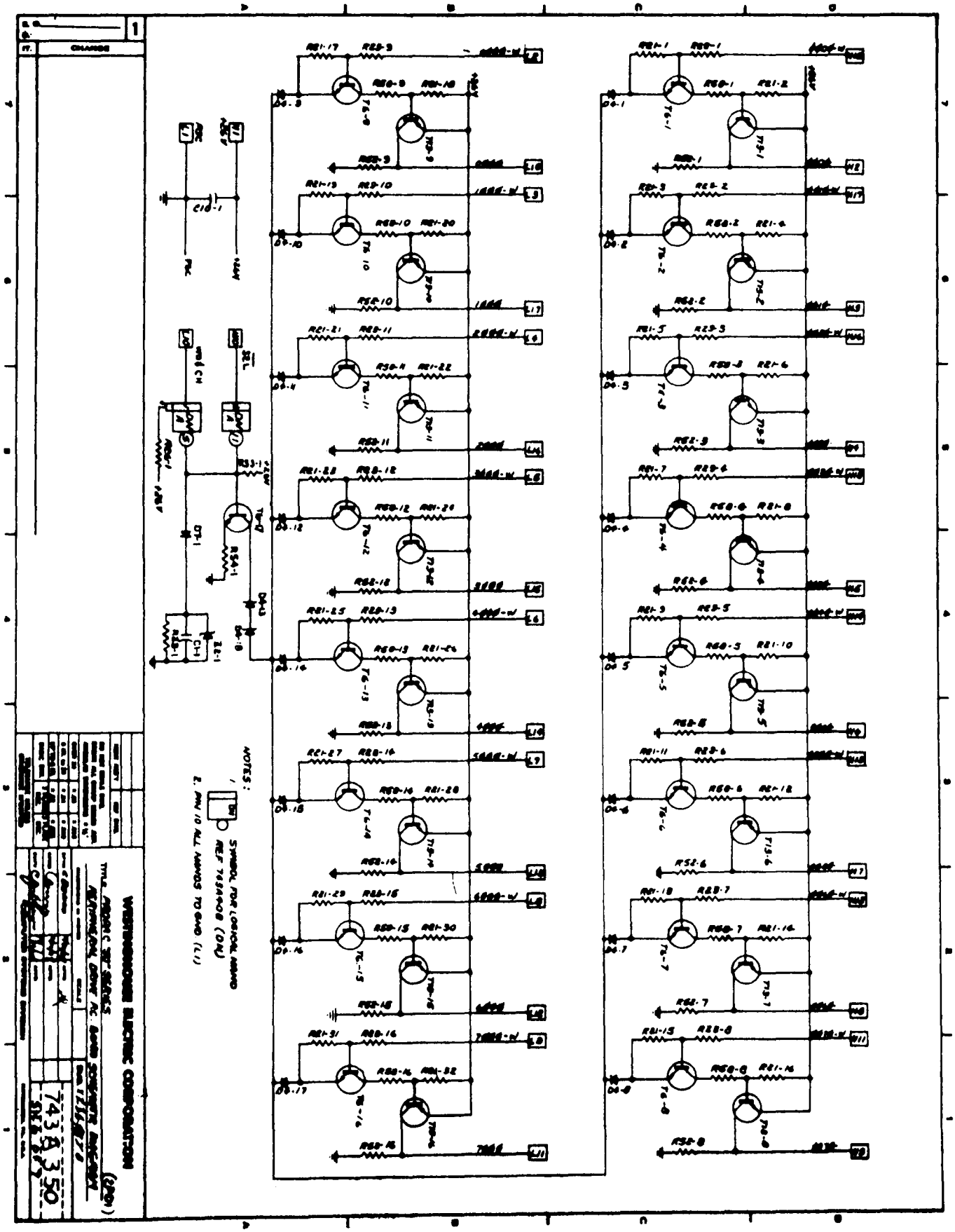
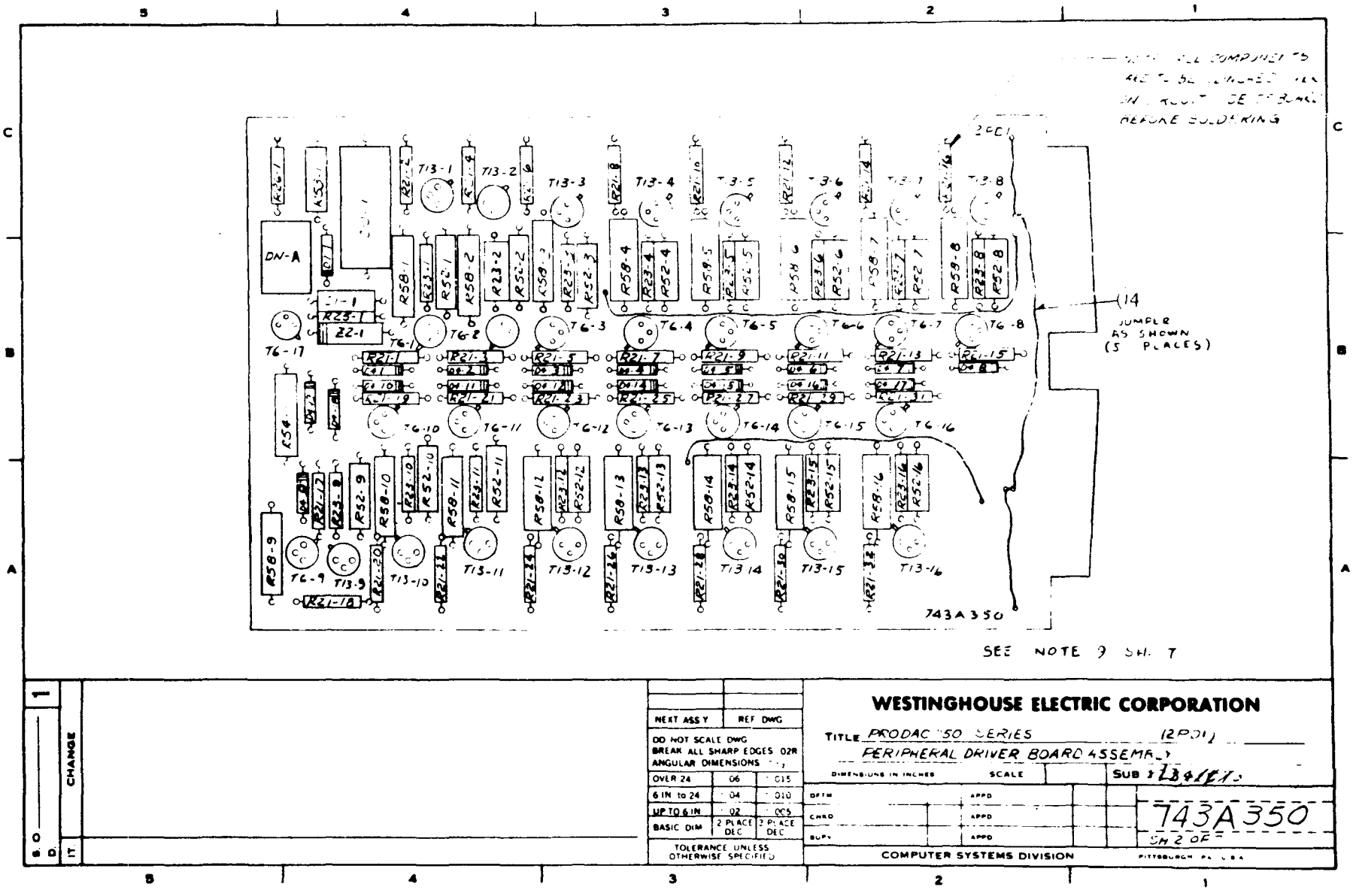


Figure 3-38. Circuit Diagram

The peripheral driver circuit (shown in Figure 3-38) operates in the following manner: When the $\overline{SEL}$ and pulser timing pulses are both zeros, transistor T6 is conducting, so that if there is an input, transistor T12 conducts, saturating transistor T13. Zener diode Z2 limits the base voltage of transistor T6 to ensure operation as a current source initially. Capacitor C1 limits the rate of rise of the emitter current for transistor T6. This is necessary for limiting the rate at which transistor T13 turns on by limiting the rate of rise of its base current. The reason for limiting the turn-on speed of transistor T13 is to avoid loosing signal through cable capacitance.

Diodes D4-13 and D4-18 help to keep transistor T12 blocked when the subcolumn half-select switch feeding the circuit is not conducting. With the subcolumn half-select switch blocked, the input is two diode drops and one collector saturation drop above ground.





1	CHANGE				
S.O.	IT.				

NEXT ASS'Y	REF DWG
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ±°	
OVER 24	.06 .015
6 IN to 24	.04 .010
UP TO 6 IN	.02 .005
BASIC DIM	2 PLACE DEC / 3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED	

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES (2P01)
PERIPHERAL DRIVER BOARD ASSEMBLY

DIMENSIONS IN INCHES | SCALE | SUB 1 2841E12

DFTM APPD
CHKD APPD
SUPV APPD

743A350
SH 2 OF

COMPUTER SYSTEMS DIVISION — PITTSBURGH PA U.S.A.

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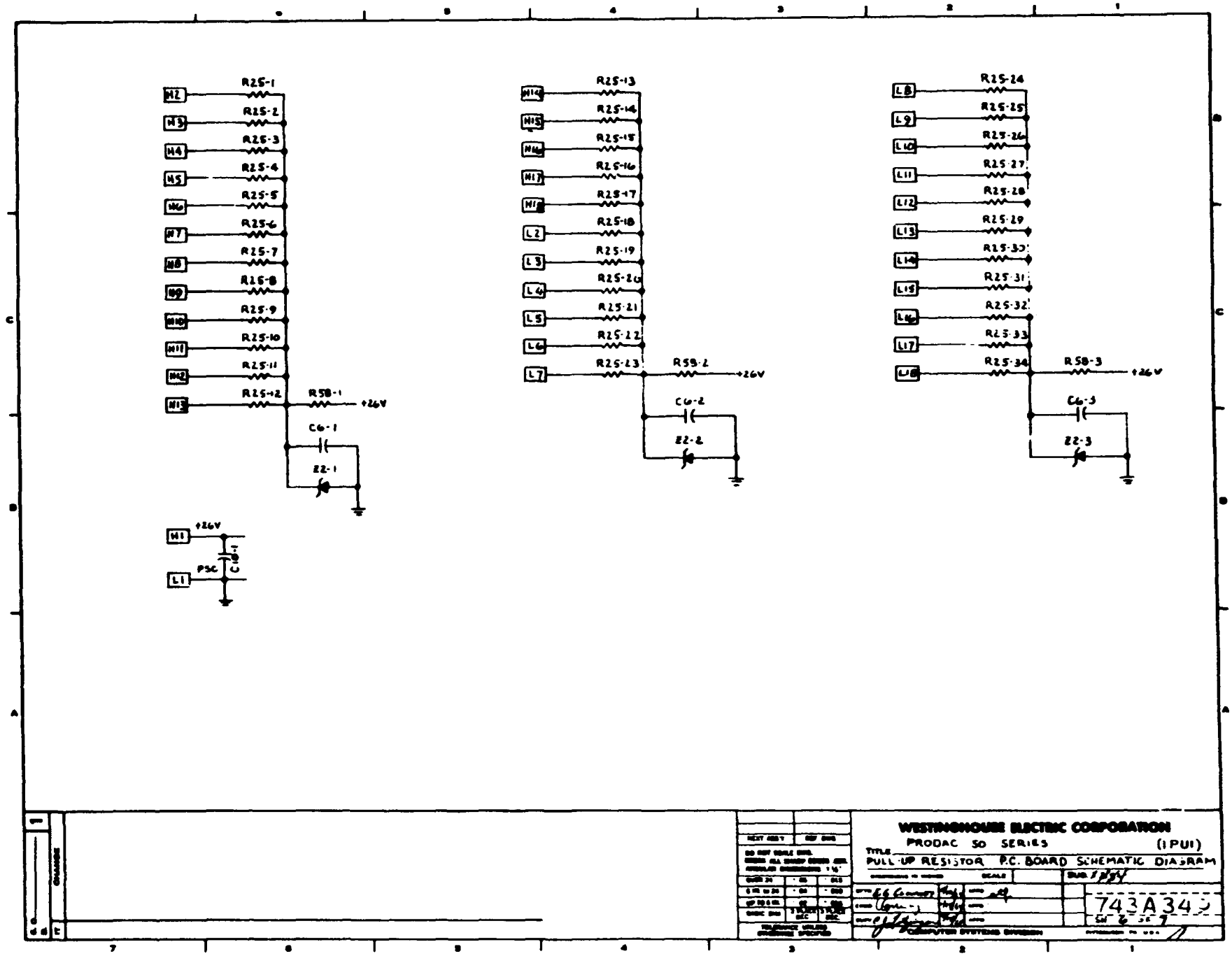
PULL-UP RESISTOR CARD 1PU1

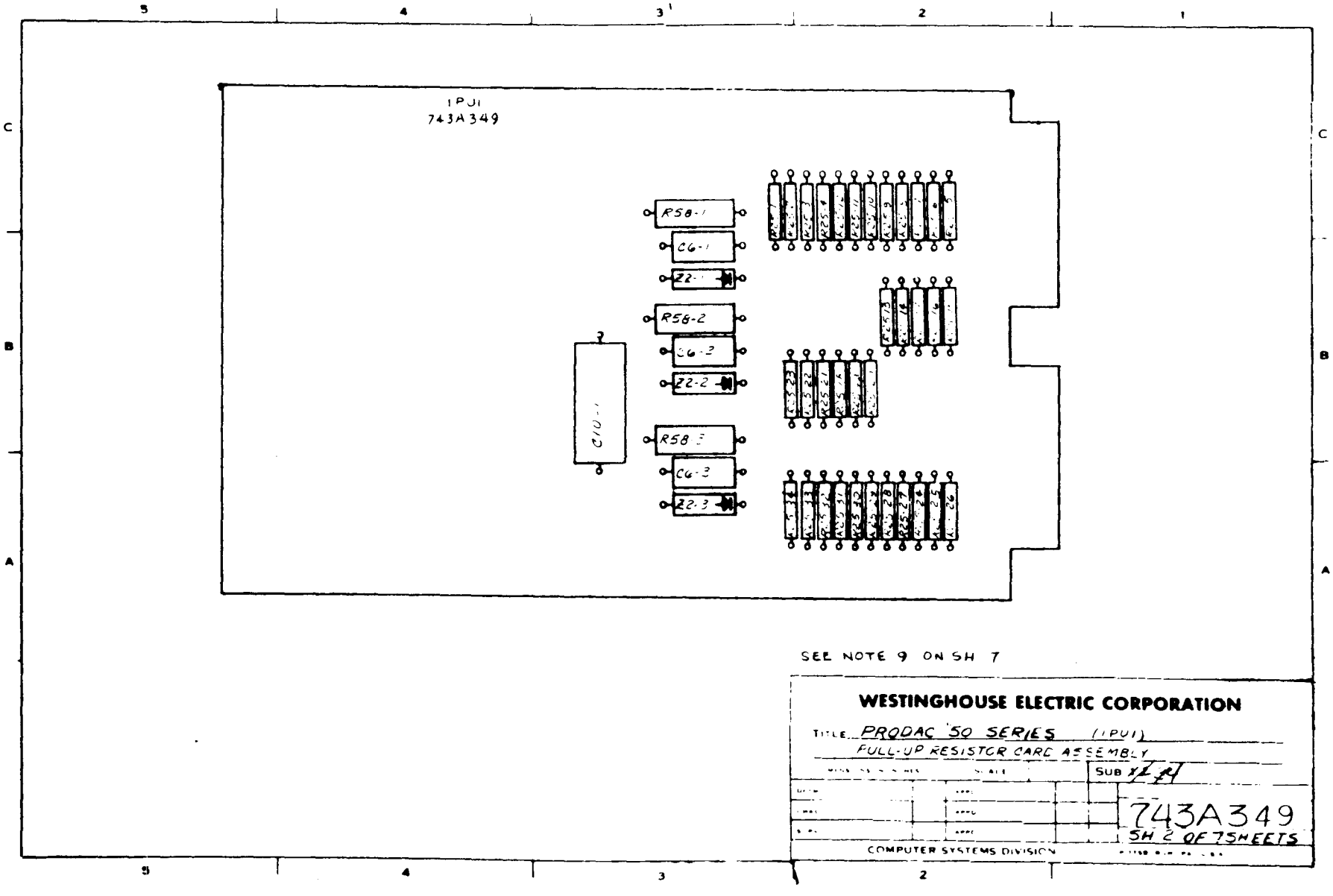
A. GENERAL DESCRIPTION

Resistors are provided for use as additional collector loads for NAND's or modified NAND's where it is desired to improve speed or noise immunity.

B. CIRCUIT DESCRIPTION

This card contains 34 resistors having a 3.01K value, connected to 6.8-volt supplies on the card. Each resistor adds an equivalent loading of one NAND input to the collector to which it is tied.


H2
H3
H4
H5
H6
H7
H8
H9
H10
H11
H12
H13
R25-1
R25-2
R25-3
R25-4
R25-5
R25-6
R25-7
R25-8
R25-9
R25-10
R25-11
R25-12
R58-1
+26V
C6-1
Z2-1
H1
+26V
PSC
C6-4
L1
H14
H15
H16
H17
H18
L2
L3
L4
L5
L6
L7
R25-13
R25-14
R25-15
R25-16
R25-17
R25-18
R25-19
R25-20
R25-21
R25-22
R25-23
R59-2
+26V
C6-2
Z2-2
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
R25-24
R25-25
R25-26
R25-27
R25-28
R25-29
R25-30
R25-31
R25-32
R25-33
R25-34
R58-3
+26V
C6-3
Z2-3
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
(1PUI)
TITLE
PULL-UP RESISTOR P.C. BOARD SCHEMATIC DIAGRAM
743A345
SH 6 OF 7


1PU1
743A349
RSB-1
C6-1
Z2-1
RSB-2
C6-2
Z2-2
RSB-3
C6-3
Z2-3
C1U-1
SEE NOTE 9 ON SH 7
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES (1PU1)
PULL-UP RESISTOR CARD ASSEMBLY
SUB XE 84
743A349
SH 2 OF 75 SHEETS
COMPUTER SYSTEMS DIVISION

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SENSE AMPLIFIER CARD 1SA2 1SA3
2SA1 2SA2

A. GENERAL DESCRIPTION

The circuits on this card are required to provide amplification for the outputs of the core memory sense lines. The amplifiers must have good common mode rejection at high frequencies. Note: There are two sense amplifier card configurations, one for core stacks 0 and 3, the other for 1 and 4. Essentially these are to accommodate left and right hand wiring to the core stacks. Circuits are identical. (Figure 3-39).

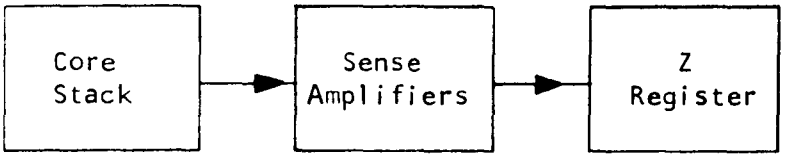


Figure 3-39.

The Sense Amplifier is electrically situated between the sense windings of the core-stack and the input of the Z register. The amplitudes of the sense outputs are too small to set the flip-flops of the Z register. The sense amplifiers provide the necessary amplification.

B. CIRCUIT OPERATION

1. Circuit Specifications

The sense windings of the core stack are shunted by a 100 ohm damping resistor and connected directly to the input of the sense amplifier. The output of the sense amplifier is transformer coupled to a level discriminator on the bit card. The transformer passes the amplified normal mode signal while rejecting the common mode signal.

2. Circuit Description

The sense amplifier card contains 14 amplifier circuits as well as transformer outputs and rectifying circuits, as shown in the card block diagram, Figure 3-40.

Refer to Figure 3-41 and drawing 743A314. The sense amplifier is a two stage, a-c, balanced amplifier. The first stage, consisting of transistors T14-1 and T14-2, provides all the voltage gain of the amplifier. The second stage, consisting of transistors T15-1 and T15-2 acts as a buffer amplifier with unity voltage gain. The output is obtained between the emitters of transistors T15-1 and T15-2. The blocking capacitors C11-1 and C11-15 isolate the d-c emitter currents of T14-1 and T14-2 and T15-1 and T15-2 respectively. This ensures that under quiescent conditions none of the transistors will be blocked, thereby eliminating the need for matching the transistor pairs for base-emitter voltage drop.

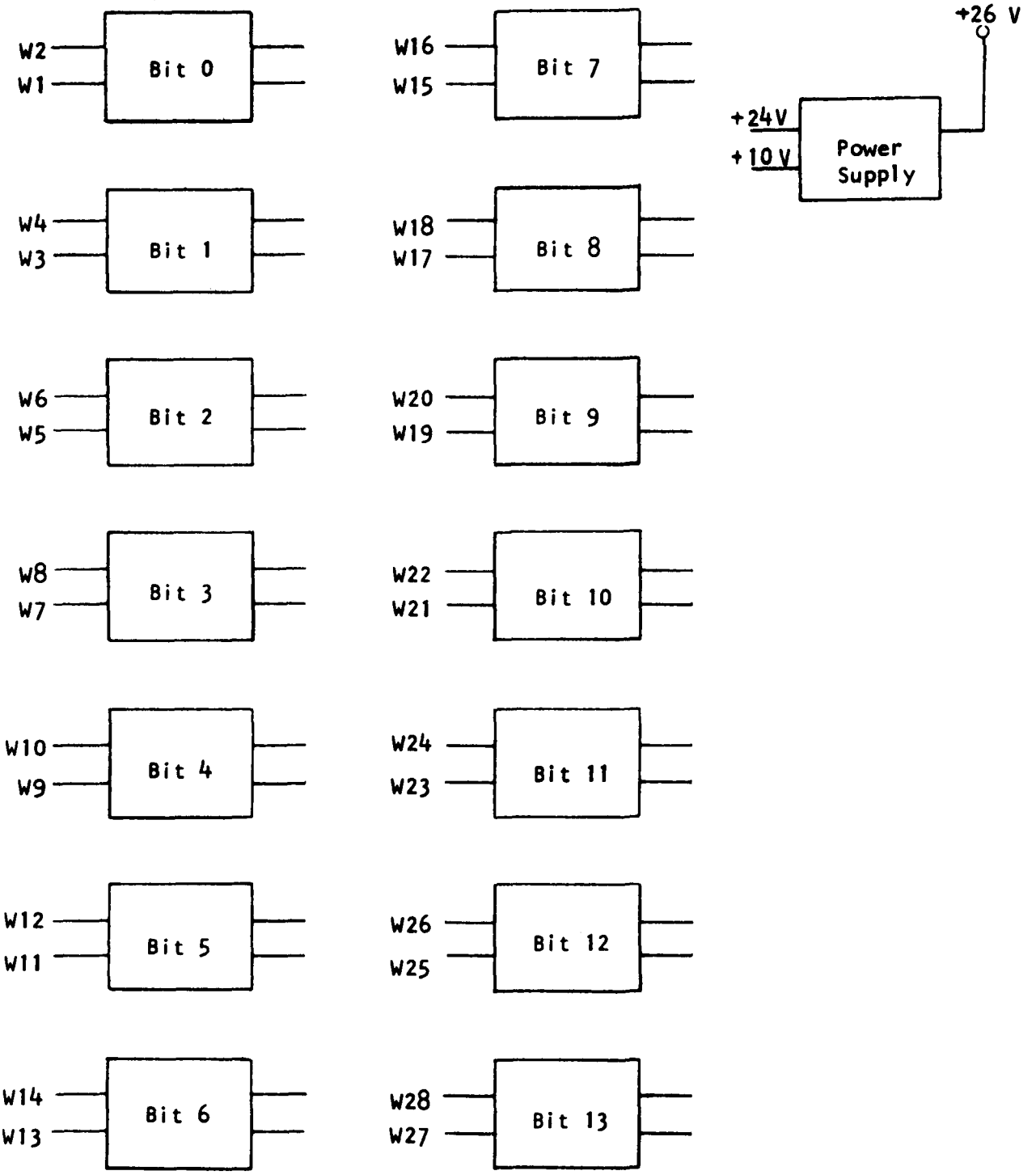

W2
W1
Bit 0
W4
W3
Bit 1
W6
W5
Bit 2
W8
W7
Bit 3
W10
W9
Bit 4
W12
W11
Bit 5
W14
W13
Bit 6
W16
W15
Bit 7
W18
W17
Bit 8
W20
W19
Bit 9
W22
W21
Bit 10
W24
W23
Bit 11
W26
W25
Bit 12
W28
W27
Bit 13
+26 V
+24V
+10V
Power
Supply

Figure 3-40.

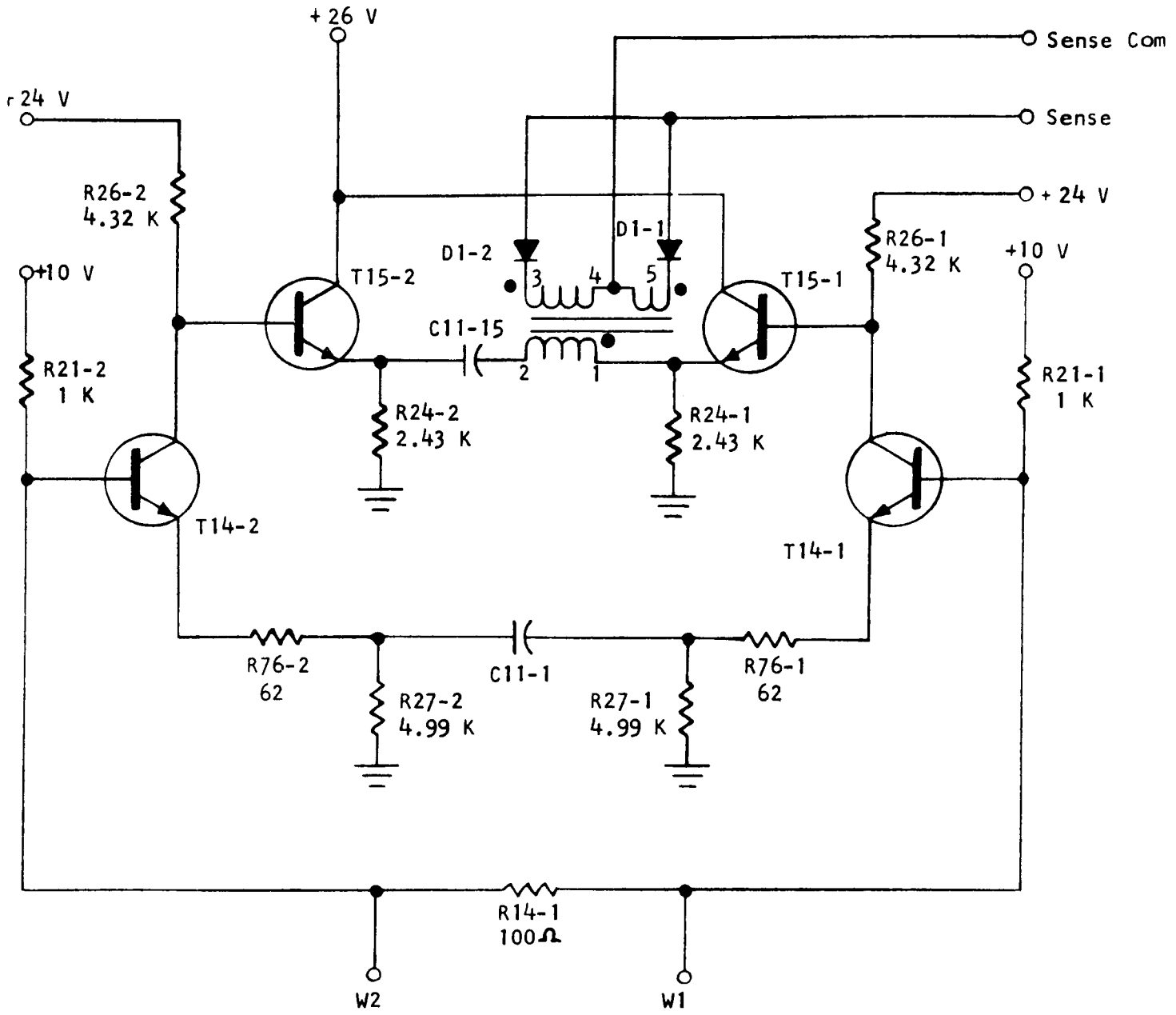
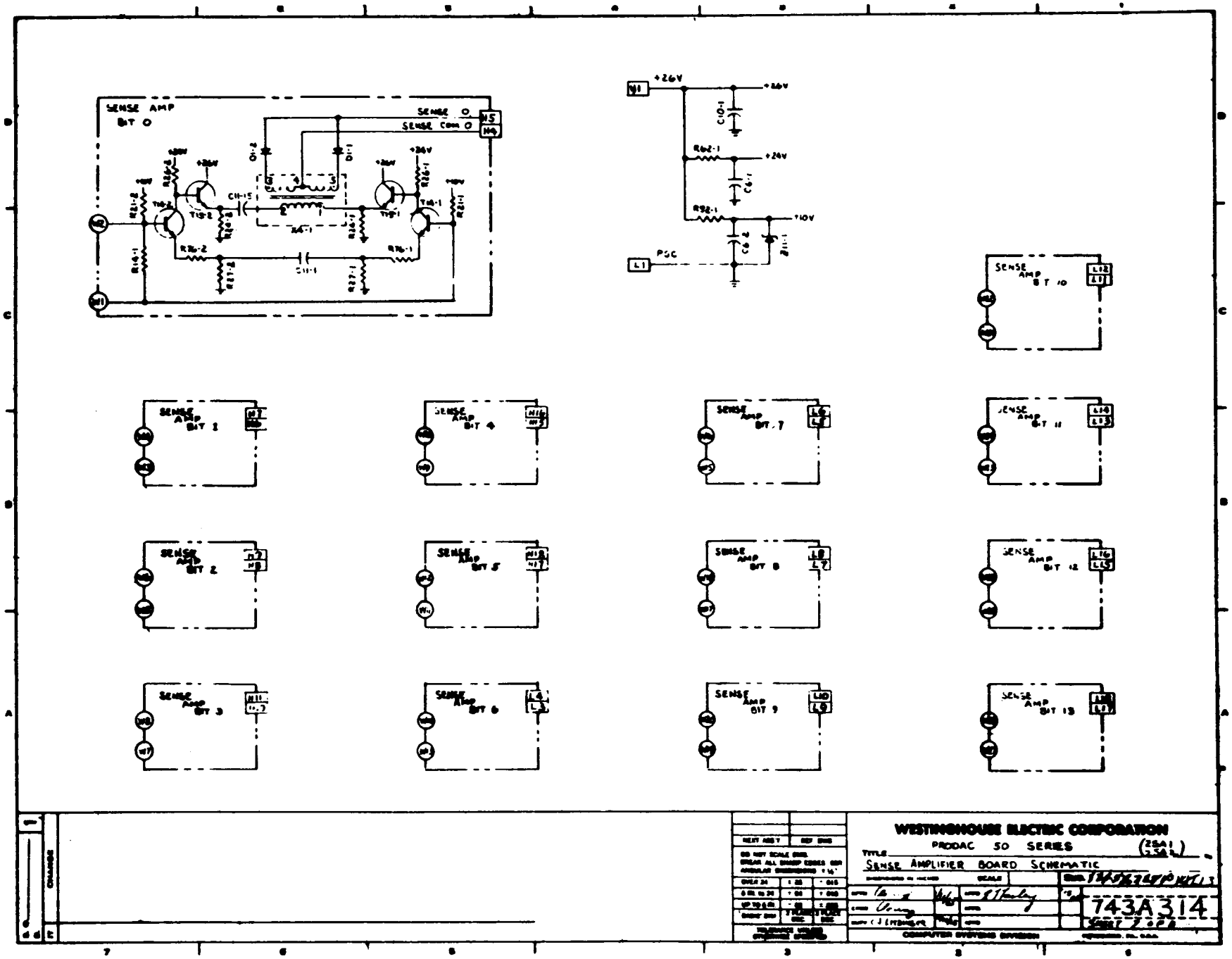
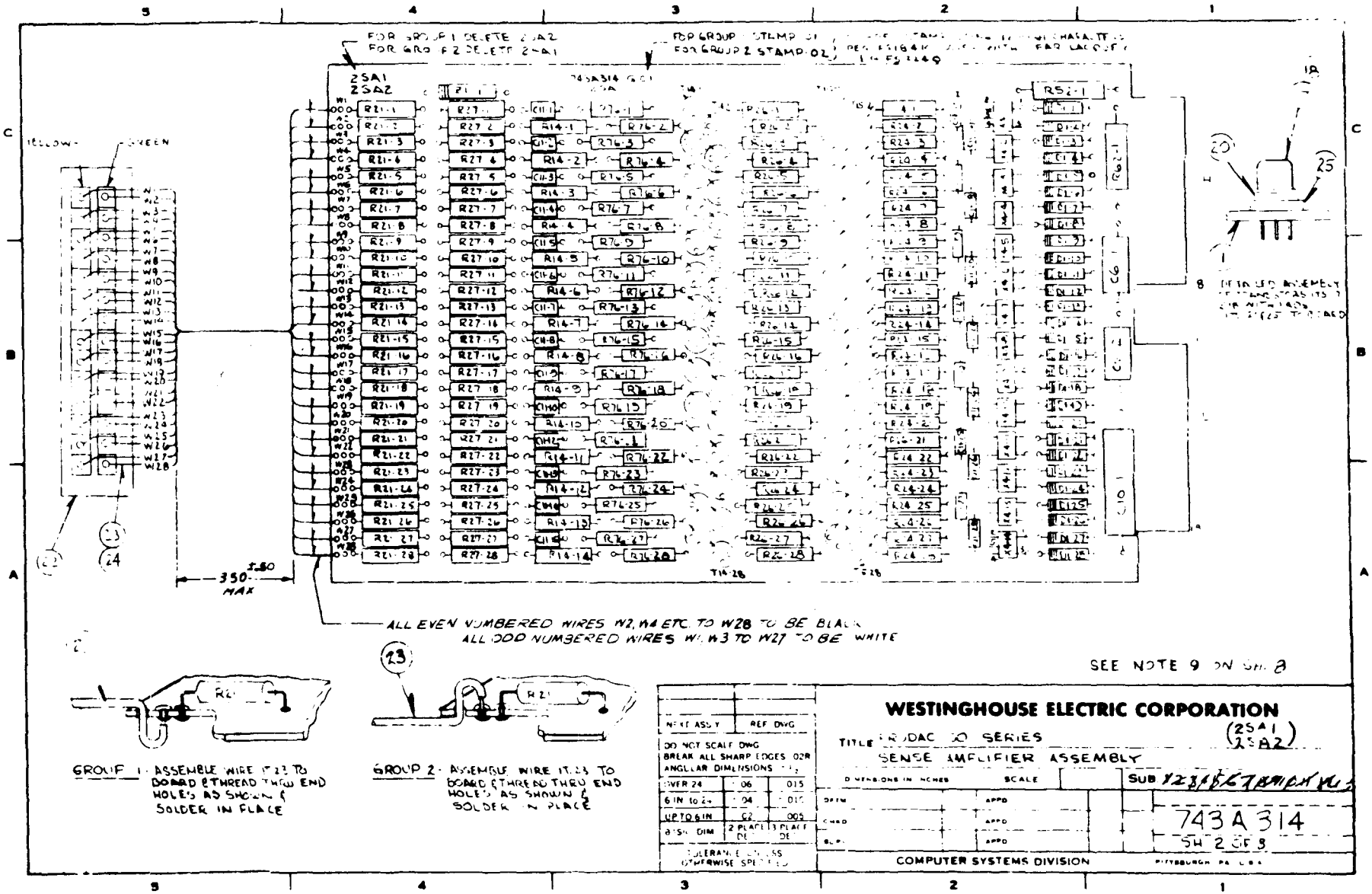

+26 V
Sense Com
r24 V
Sense
R26-2
4.32 K
+24 V
D1-2
D1-1
+10 V
T15-2
T15-1
R26-1
4.32 K
+10 V
3
4
5
C11-15
2
1
R21-2
1 K
R21-1
1 K
R24-2
2.43 K
R24-1
2.43 K
T14-2
T14-1
R76-2
62
C11-1
R76-1
62
R27-2
4.99 K
R27-1
4.99 K
R14-1
100Ω
W2
W1

Figure 3-41.


SENSE AMP BIT 0
SENSE 0
SENSE COM 0
+26V
PSC
SENSE AMP BIT 10
SENSE AMP BIT 1
SENSE AMP BIT 4
SENSE AMP BIT 7
SENSE AMP BIT 11
SENSE AMP BIT 2
SENSE AMP BIT 5
SENSE AMP BIT 8
SENSE AMP BIT 12
SENSE AMP BIT 3
SENSE AMP BIT 6
SENSE AMP BIT 9
SENSE AMP BIT 13
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
SENSE AMPLIFIER BOARD SCHEMATIC
743A314


FOR GROUP 1 DELETE 2SA2
FOR GROUP 2 DELETE 2SA1
FOR GROUP 1 STAMP 01
FOR GROUP 2 STAMP 02
2SA1
2SA2
YELLOW
GREEN
350 MAX
ALL EVEN NUMBERED WIRES W2, W4 ETC. TO W28 TO BE BLACK
ALL ODD NUMBERED WIRES W1, W3 TO W27 TO BE WHITE
SEE NOTE 9 ON SH. 8
GROUP 1 - ASSEMBLE WIRE #23 TO BOARD & THREAD THRU END HOLE AS SHOWN & SOLDER IN PLACE
GROUP 2 - ASSEMBLE WIRE #23 TO BOARD & THREAD THRU END HOLE AS SHOWN & SOLDER IN PLACE
DO NOT SCALE DWG
BREAK ALL SHARP EDGES .02R
ANGULAR DIMENSIONS ±½°
OVER 24 .06 .015
6 IN TO 24 .04 .010
UP TO 6 IN .02 .005
WESTINGHOUSE ELECTRIC CORPORATION
TITLE MODAC 50 SERIES (2SA1 2SA2)
SENSE AMPLIFIER ASSEMBLY
SCALE
SUB
743A314
SH 2 OF 3
COMPUTER SYSTEMS DIVISION
PITTSBURGH PA

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SEQUENCE CONTROL CARD 1SC2

A. GENERAL DESCRIPTION

This card provides a three-bit sequence advance register, a three-bit sequence half-advance register, a sequence half-advance to sequence advance gate, a decoding gate to set half-advance register, a decode of Sequence V, and clamping for manual read core and manual write core.

Figure 3-42 shows in block diagram form the uses of this card.

B. CIRCUIT DESCRIPTION

Block diagram Figure 3-42 is helpful in connection with study of the following block description and also drawing 743A302.

The Sequence Advance Register: Consists of NAND's D, E and F. These have double-base drive for high fanout.

The Sequence Half-Advance Register: Consists of NAND's A, B and C. These also have double-base drive for high fanout.

Sequence Half-Advance to Sequence Register Gate: Consists of NAND's J, K and L. It transfers both sides of the register, thus avoiding clearing before transfer.

Sequence Half-Advance Decoding Gate: Consists of NAND's G, H, N, P and R. (See the sequence flowchart located at the bottom of schematic for sequence rotation.)

R11 sets Sequence III from Sequence II. H5 sets Sequence IV from Sequence III on a non-jump instruction. H11 sets Sequence IV from Sequence III when a jump is to be taken. P11 sets Sequence V from Sequence III. N11 sets Sequence VII from Sequence III. P5 sets Sequence V from Sequence IV. G5 sets Sequence VII from Sequence IV. G11 sets Sequence VI from Sequence V. N5 sets Sequence VII from Sequence VI. R5 decodes a non-jump instruction.

Decode Sequence V: Consists of NAND M. M11 decodes Sequence V. M5 inverts Sequence V.

Manual Read Core Decode: Consists of R25-14 and D7-2 to D7-6. Switch grounding clamps Sequence V of the ENL (Enter Lower) instruction.

Manual Write Core Decode: Consists of R25-13 and D7-1 and D7-7. Switch grounding clamps Sequence VI of the STL (Store Lower) instruction.

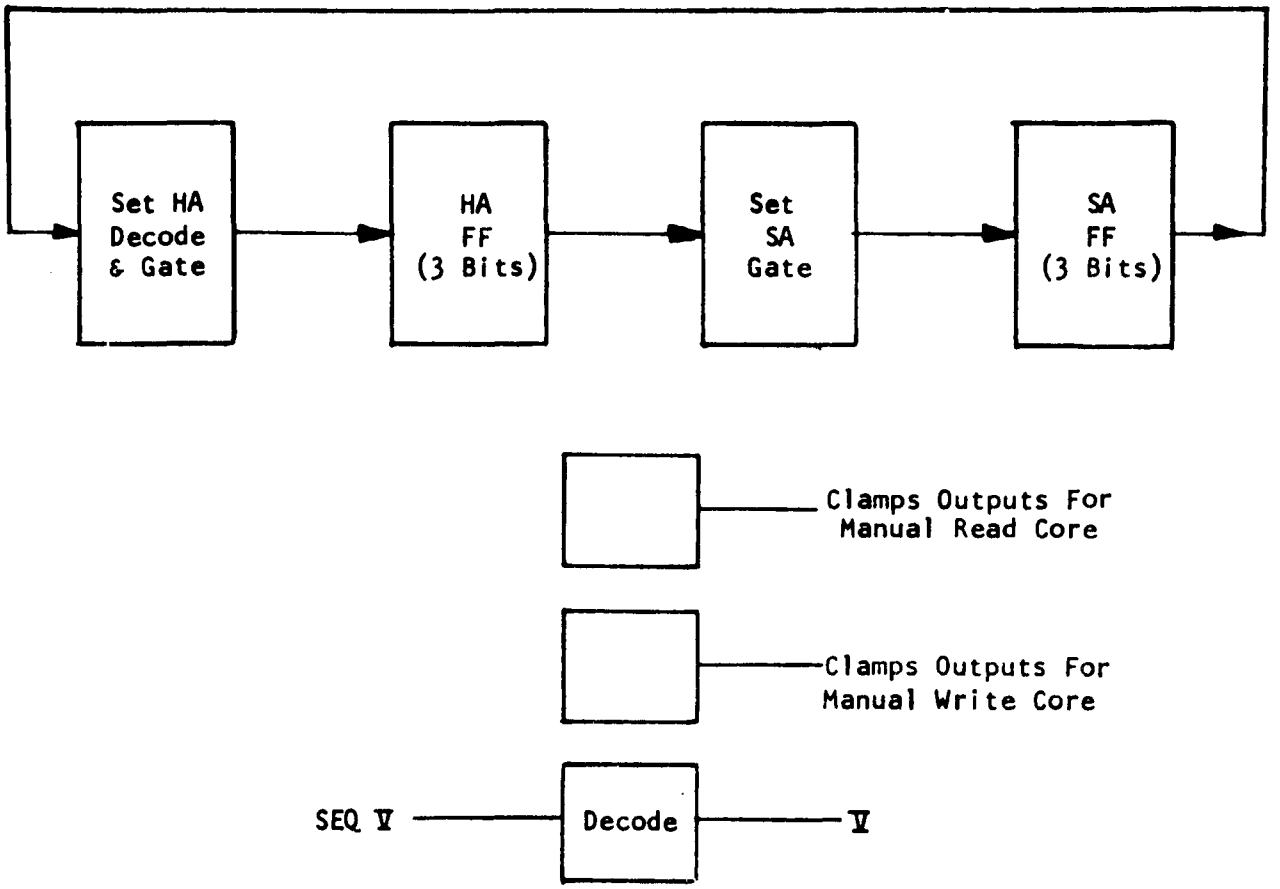
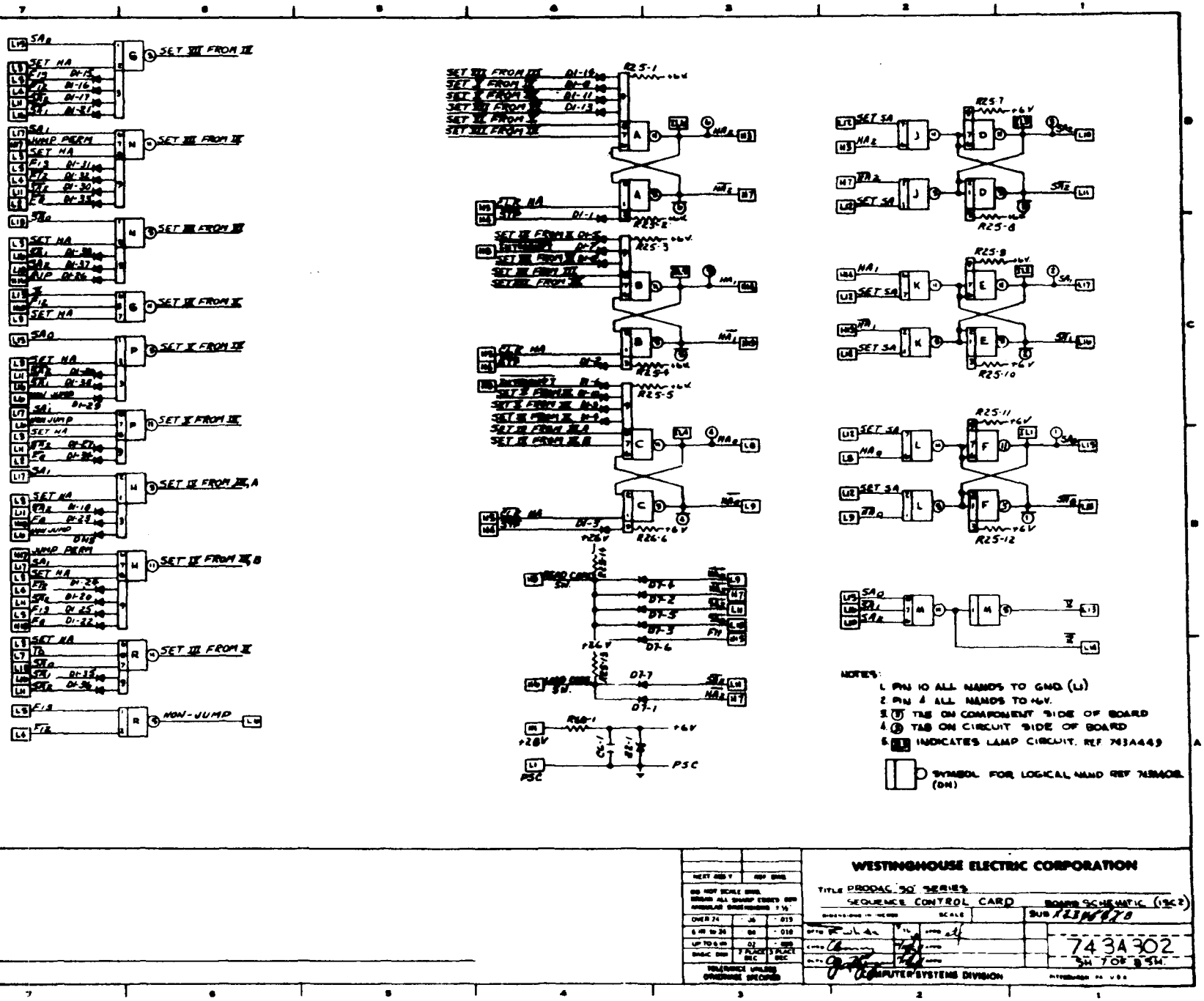

Set HA
Decode
& Gate
HA
FF
(3 Bits)
Set
SA
Gate
SA
FF
(3 Bits)
Clamps Outputs For
Manual Read Core
Clamps Outputs For
Manual Write Core
SEQ V
Decode
V

Figure 3-42.

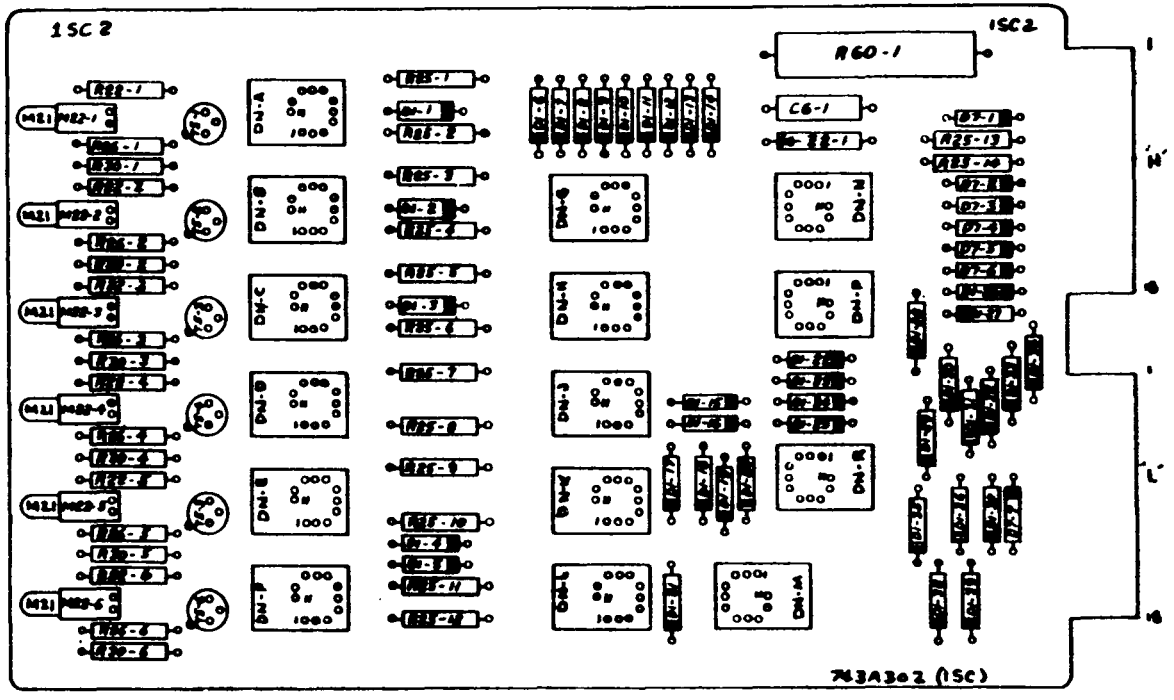


WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
SEQUENCE CONTROL CARD
BOARD SCHEMATIC (1 OF 2)
SUB 743A028

743A302
SH 1 OF 2 SH

COMPUTER SYSTEMS DIVISION



SEE NOTE 9 ON SH 8

1	C.O.			
	IT.			

NEXT ASSY | REF. DWG.

DO NOT SCALE DWG.
BREAK ALL SHARP EDGES .005
ANGULAR DIMENSIONS ±½°

OVER 24	±.05	±.010
6 TO 24	±.01	±.010
TO 6 INCL.	±.02	±.005
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
SEQUENCE ADVANCE CARD ASSEMBLY (1SC2)

DIMENSIONS IN INCHES | SCALE | SUB. Y743A678

DRAWN | APPD
CHKD | APPD
SUPV | APPD

743A302
SHEET 2 OF 8 SH

COMPUTER SYSTEMS DIVISION — PITTSBURGH, PA. U.S.A.

S REGISTER DATA TRANSFER 2ST2

A. GENERAL DESCRIPTION

This card is used to provide:

1. Adder to S gate drive
2. Clear S to "one" gate drive
3. Clear X to "zero" gate drive
4. Input data strobe gate drive
5. Input and output decode for Word and Channel pulsers
6. Instruction step decode
7. Inhibit pulser timing signal

Figure 3-43 shows in block diagram form the uses of this card.

B. CIRCUIT DESCRIPTION

$\overline{ADD} \rightarrow \bar{S}_{0-7}$ consists of NANDs E5 and A11. E5 is used as a decoding delay line tap amplifier, A11 is used as an inverter.

$\overline{ADD} \rightarrow \bar{S}_{8-13}$ consists of NANDs E11 and A5. E11 is used as a decoding delay line tap amplifier, A5 is used as an inverter.

$\overline{CLR}\ S/_{0-7,1}$ consists of NAND G5 which is used as a decoding delay line tap amplifier.

$\overline{CLR}\ S/_{8-13,1}$ consists of NAND G11 which is used as a decoding delay line tap amplifier.

$\overline{CLR}$ X, consists of NAND F5 and diode D1-4. F5 is used as a double drive decoding delay line tap amplifier, D1-4 is used to clamp the output of $\overline{CLR}$ X bus for master clearing the X register. Of special note here, observe that the $\overline{VI}$ logic signal on pin 3 is not diode isolated.

Input Strobe - consists of NAND F11 and D5. F11 is used as a decoding delay line tap amplifier, D5 is used as a double base drive inverter. R21-1 is used as pull-up which helps to improve the rise time of the strobe pulse.

WD and Ch. Pulser Timing - consists of NANDs D11 and B11. D11 is used to decode the Input instruction and sequence V. B11 decodes the Output instruction and sequence VI.

Inst Step - consists of NAND B5 which decodes the cleared, Half Advance at the end of a sequence which indicates the next sequence will be I or II.

Inhibit Pulser Timing - consists of NAND C5 and C11. C5 is used as a decoding delay line tap amplifier except two taps, L2 and L3 are decoded. It provides a zero output over the duration of two delay line tap periods. C11 is used as a double drive decoding gate driver. C11 output signal is similar to the W signal except that it occurs one delay line tap earlier.

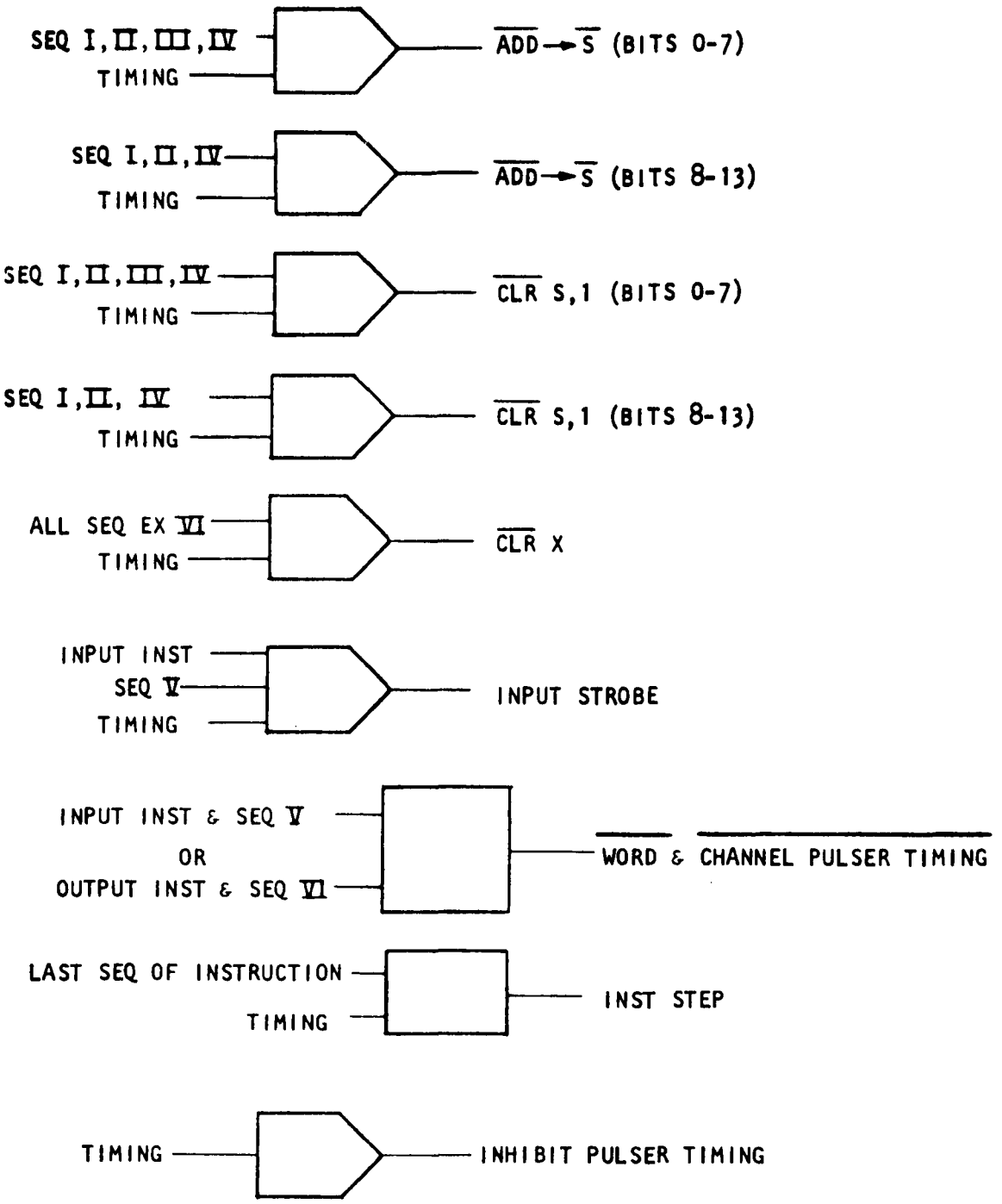
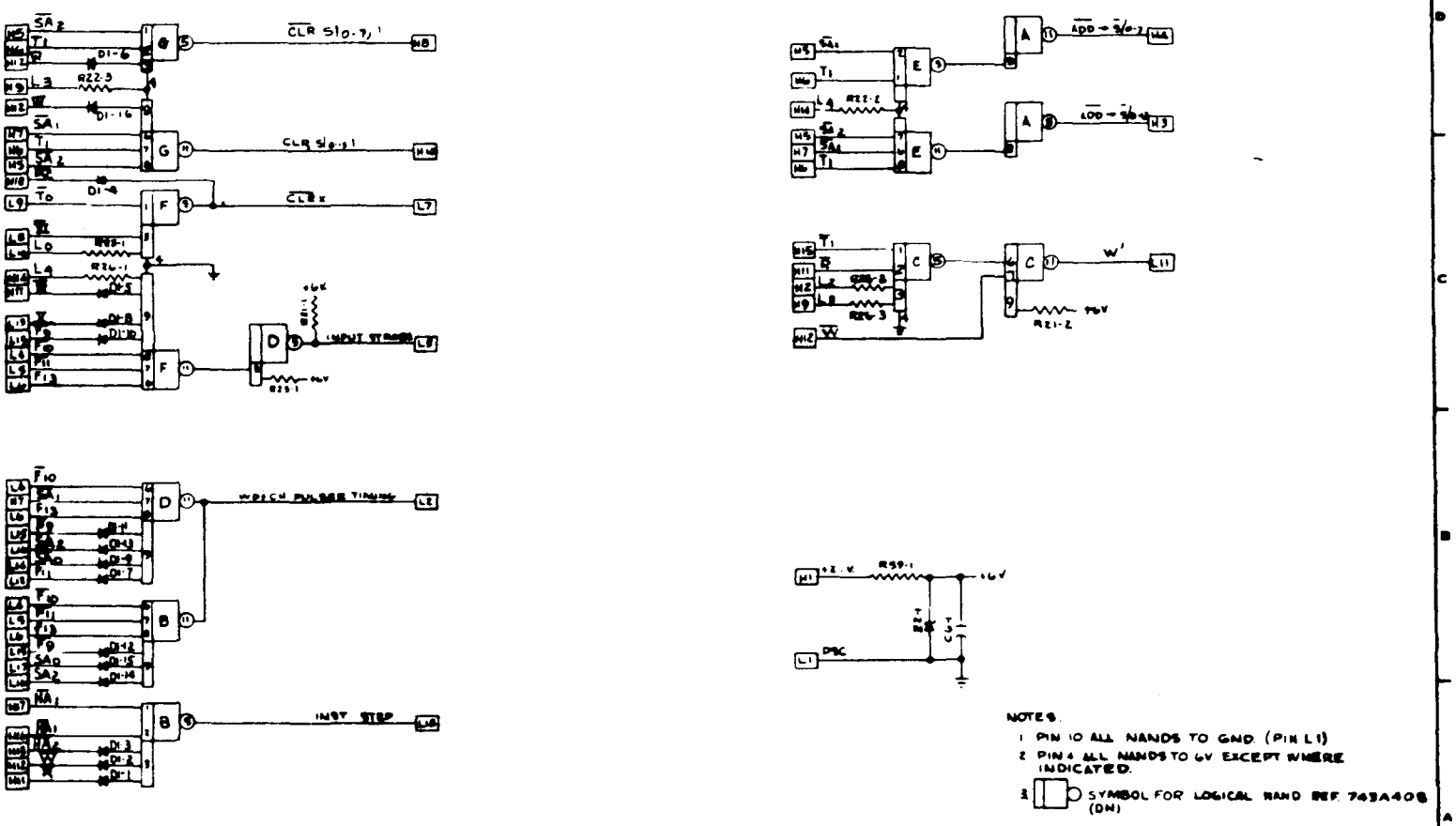

SEQ I, II, III, IV
TIMING
ADD → S (BITS 0-7)
SEQ I, II, IV
TIMING
ADD → S (BITS 8-13)
SEQ I, II, III, IV
TIMING
CLR S,1 (BITS 0-7)
SEQ I, II, IV
TIMING
CLR S,1 (BITS 8-13)
ALL SEQ EX VI
TIMING
CLR X
INPUT INST
SEQ V
TIMING
INPUT STROBE
INPUT INST & SEQ V
OR
OUTPUT INST & SEQ VI
WORD & CHANNEL PULSER TIMING
LAST SEQ OF INSTRUCTION
TIMING
INST STEP
TIMING
INHIBIT PULSER TIMING

Figure 3-43.



WESTINGHOUSE ELECTRIC CORPORATION

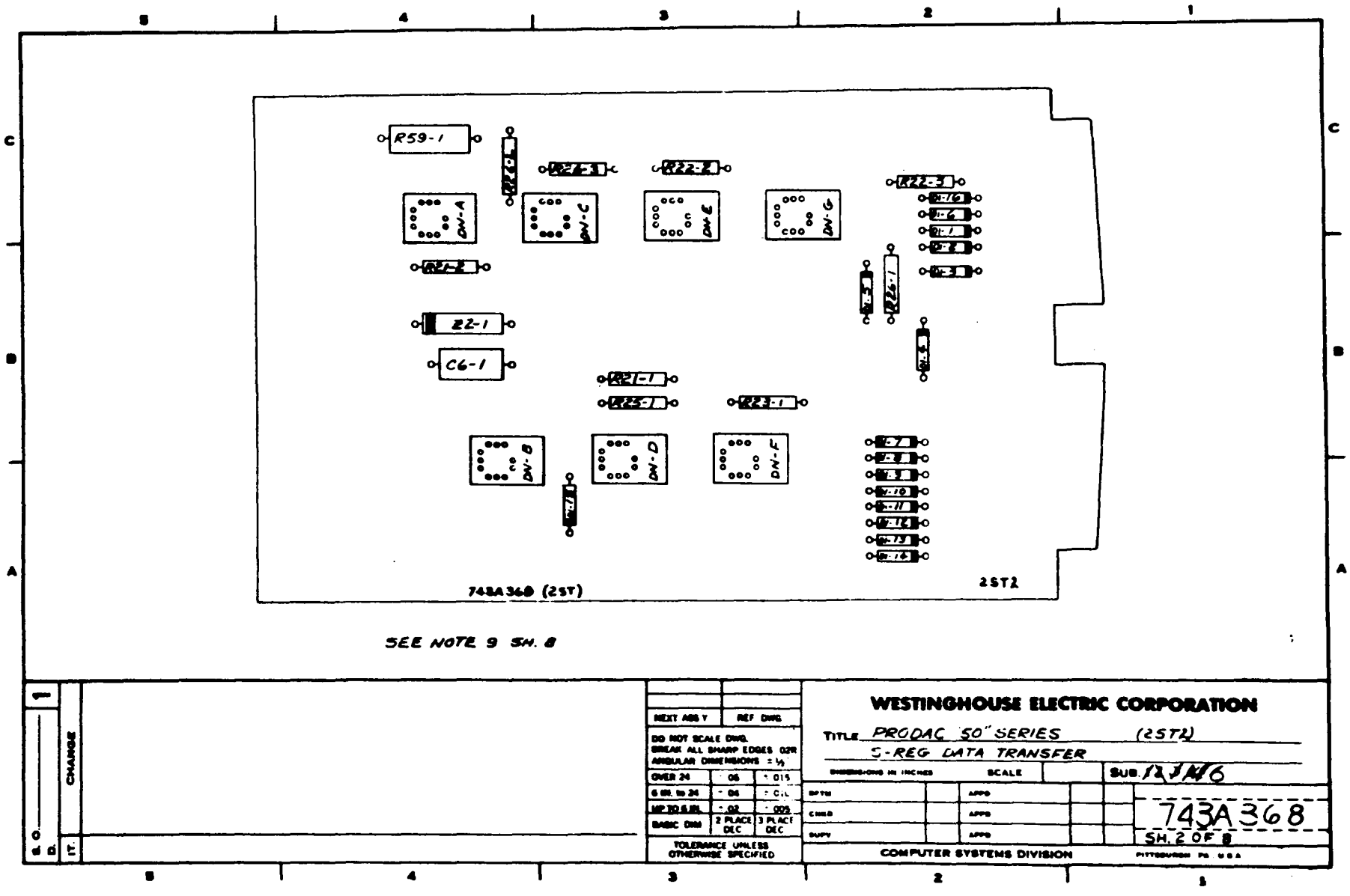
TITLE PRODAC 50 SERIES

3 BUS DATA TRANSFER BOARD SCHEME (3)

743A368

SHEET 1 OF 7

COMPUTER SYSTEMS DIVISION



NEXT ASS'Y	REF DWG		
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½			
OVER 24	± .06	± .015	
6 thru 24	± .04	± .010	
UP TO 6 INCL	± .02	± .005	
BASIC DIM	2 PLACE DEC	3 PLACE DEC	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50" SERIES (2ST2)
5-REG DATA TRANSFER

SCALE | SUB. 13 JAN 6

DRTN | APPD
CHKD | APPD
SUPV | APPD

743A368
SH. 2 OF 8

COMPUTER SYSTEMS DIVISION PITTSBURGH PA. U.S.A.

TIMING CARD 4TC1

A. GENERAL DESCRIPTION

The timing card generates the clock pulses. It provides a delay line timing chain, a two bit register, core read timing, core write timing, the half-select selection timing, a clear Z gate drive, clear and set sequence half-advance gate time, a stop relay, and a master clear relay.

Figure 3-44 is a block diagram of the use of this card in the system.

B. CIRCUIT OPERATION

1. Circuit Specifications

The delay line has a total delay of 1.5 microseconds, three passes are made through the delay line to achieve the basic 4.5 microsecond cycle time.

2. Circuit Description

The delay line is started by a "zero" signal at pin 1 of NAND P flip-flop. This flip-flop is used to prevent contact bounce from the start (external to the board) button from restarting the delay line.

Capacitor C3-1 and resistor R21-7 differentiate the output of P5 to set dual NAND flip-flop N. This provides base drive to transistor T7-1 which drives the delay line directly.

The delay line will sustain itself via dual NAND G12 which acts as a hold off clamp to insure that no multiple pulses occur down the line.

NAND M5 provides restart from the last tap of the delay line.

The delay line may be stopped with a "zero" on the $\overline{STP}$ input on pin 2 of dual NAND M.

This $\overline{STP}$ occurs as a result of a STOP instruction or by depressing the stop (externally mounted) button.

Transistor T7-1 is used as a emitter follower circuit to provide a twelve volt, 300 nanosecond pulse. The pulse width is determined by the first tap of the delay line which generates a level to turn off T7-1. Tap voltages greater than five volts cause switching of the tap amplifiers.

The timing register consists of NAND flip-flops B and C and NAND gates H and J. This register is used to count the cycles and will be $\overline{T0}\cdot\overline{T1}$; $T0\cdot\overline{T1}$; and $T0\cdot T1$.

The core read pulser timing consists of NAND flip-flop D and NAND gates K. The Read pulse (R) is set by $\overline{T0}$ and L1 and stays set until the following L1 time when T0 clears the pulse.

The core write pulser timing consists of NAND flip-flop E and gates NAND L. The Write pulse (W) is set by $T0\cdot\overline{T1}$ and L3 pulse and stays set until the next L3 time when T1 clears the pulse.

Half-Select selection timing consists of NAND F and is set by the first L0 pulse and stays set until the third L3 time when T1 clears W and Sel at the same time.

Clear Z gate driver consists of NAND M11, M11 is used as a decoding delay line tap amplifier. R21-5, R21-6, C6-3 and D1-16 provide a pulse to clear Z when Master Clear (external to the board) is depressed.

Clear sequence half advance gate driver consists of modified NAND G11 which is used as a decoding delay line tap amplifier.

Set sequence half advance gate driver consists of NAND A5 which is used as a logic signal inverter.

Set sequence advance gate driver consists of NAND A11 which is used as a logic signal inverter.

The Stop circuit consists of relay M1-2 and associated components; with this relay closed, the computer will transfer from "run" to "instruction step".

The Master Clear circuit consists of relay M1-1 and associated components; with this relay closed, the computer will stop then master clear the register to preset condition, that is, it will clamp Sel, reset flip-flop P; clamp $\overline{\text{Clr}}$ HA, clamp W, clamp R, set $\overline{\text{T1}}$, set $\overline{\text{T0}}$ and clear Z.

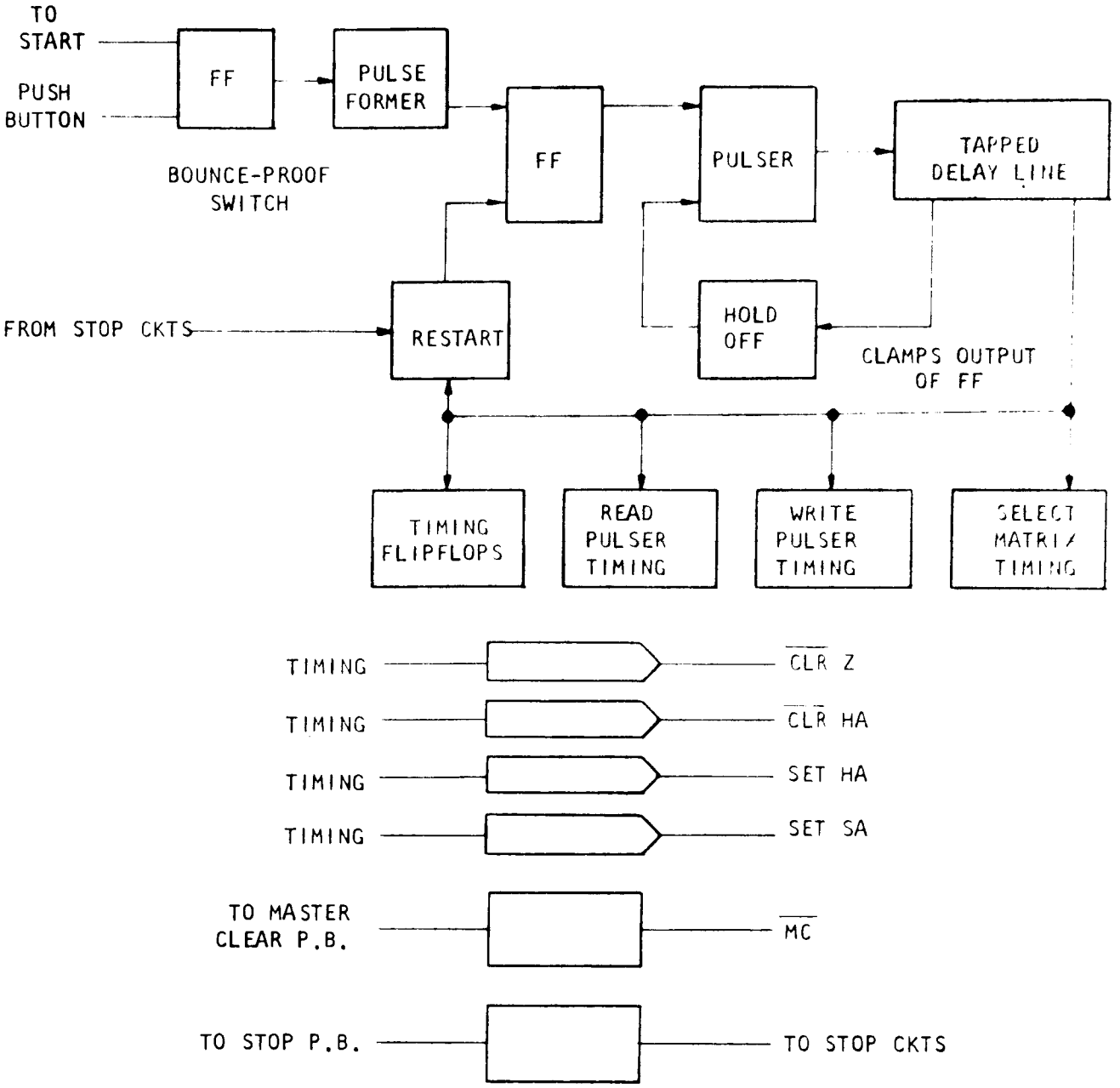
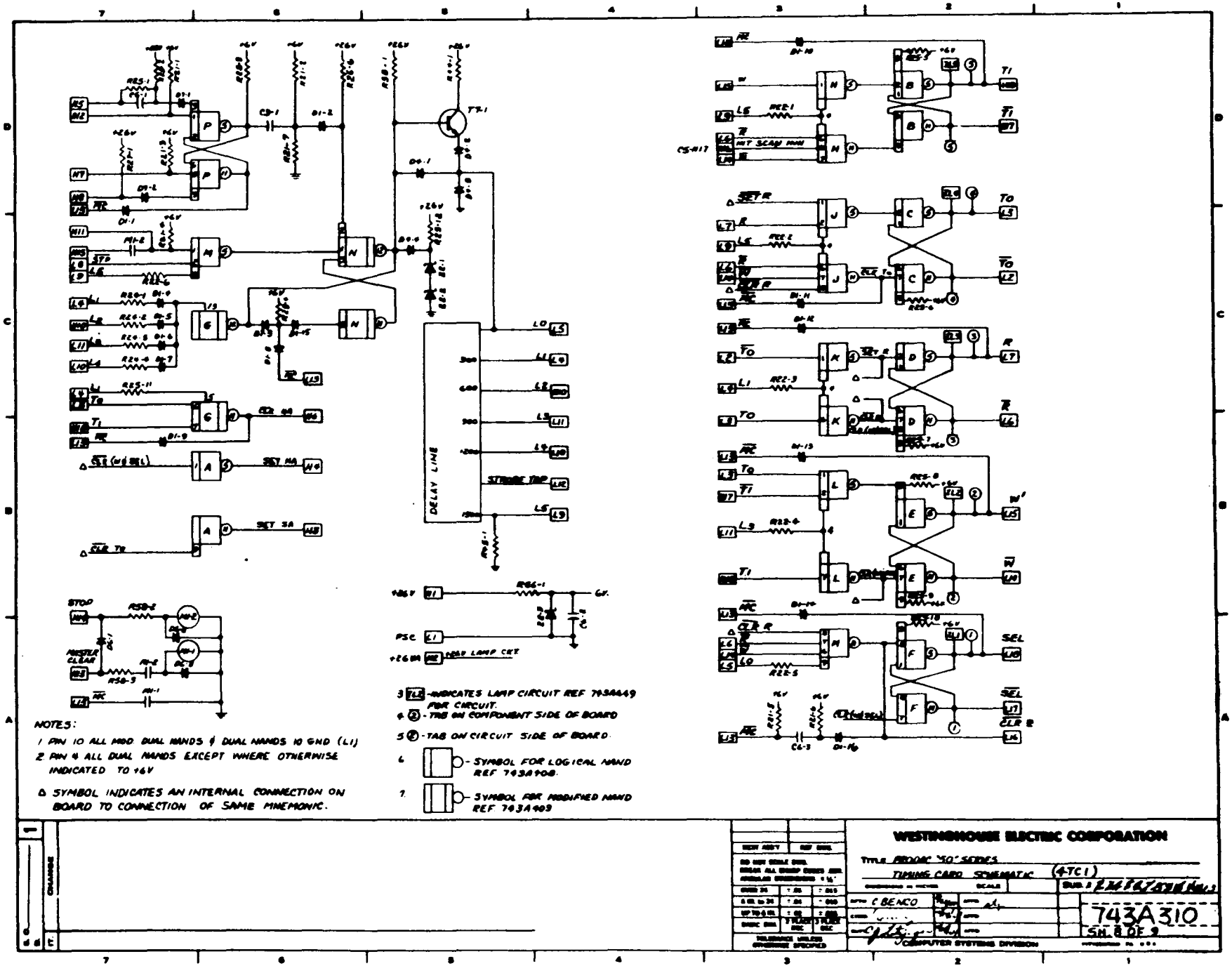

TO START
PUSH BUTTON
FF
PULSE FORMER
BOUNCE-PROOF SWITCH
FF
PULSER
TAPPED DELAY LINE
FROM STOP CKTS
RESTART
HOLD OFF
CLAMPS OUTPUT OF FF
TIMING FLIPFLOPS
READ PULSER TIMING
WRITE PULSER TIMING
SELECT MATRIX TIMING
TIMING
CLR Z
TIMING
CLR HA
TIMING
SET HA
TIMING
SET SA
TO MASTER CLEAR P.B.
MC
TO STOP P.B.
TO STOP CKTS

Figure 3-44.



NOTES:

1. PIN 10 ALL MOD DUAL NANDS & DUAL NANDS 10 GND (LI)
2. PIN 4 ALL DUAL NANDS EXCEPT WHERE OTHERWISE INDICATED TO +6V

Δ SYMBOL INDICATES AN INTERNAL CONNECTION ON BOARD TO CONNECTION OF SAME MNEMONIC.

3 (TL3) -INDICATES LAMP CIRCUIT REF 7934449 FOR CIRCUIT.

4 (B) - TAB ON COMPONENT SIDE OF BOARD

5 (B) - TAB ON CIRCUIT SIDE OF BOARD

6 - SYMBOL FOR LOGICAL NAND REF 743A908.

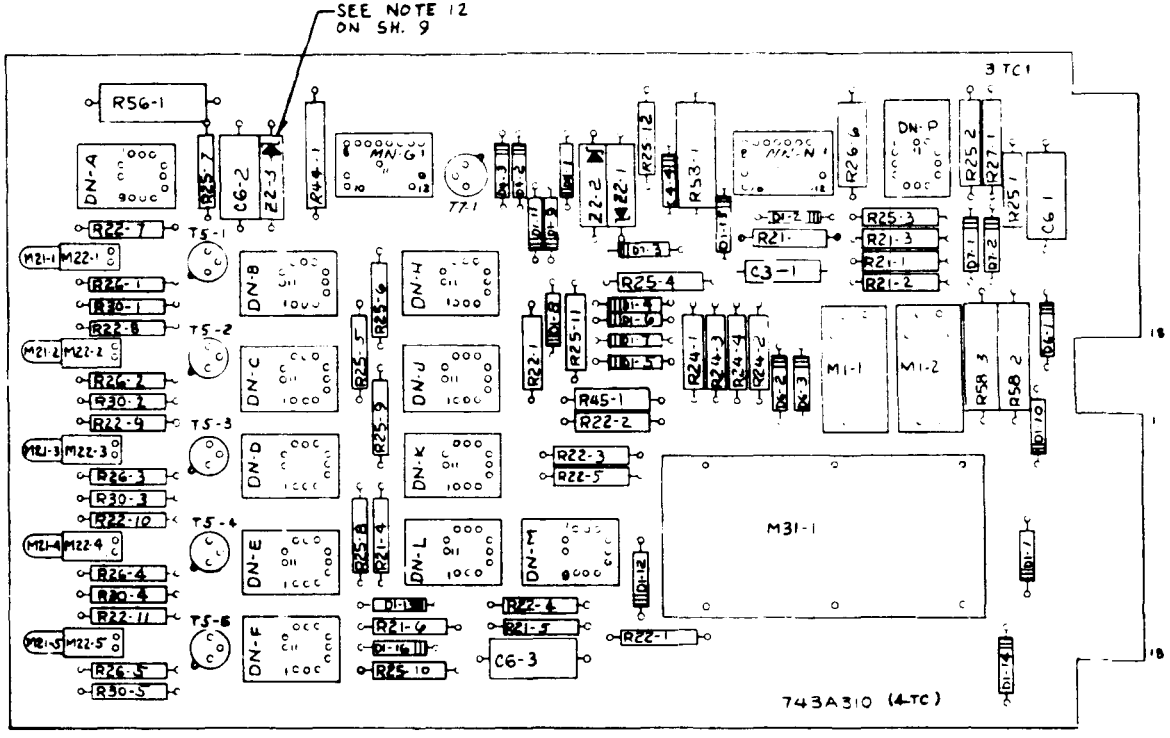
7 - SYMBOL FOR MODIFIED NAND REF 743A909

WESTINGHOUSE ELECTRIC CORPORATION

TITLE: AEGIS "10" SERIES TIMING CARD SCHEMATIC (4TC1)

DWG. # 743A310 SH. 8 OF 9

COMPUTER SYSTEMS DIVISION



1	CHANGE		
S.O.	IT.		

NEXT ASS'Y	REF DWG
DO NOT SCALE DWG BREAK ALL SHARP EDGES .02R ANGULAR DIMENSIONS ± ½°	

OVER 24	± .06	± .015
6 IN. to 24	± .04	± .010
UP TO 6 IN.	± .02	± .005
BASIC DIM	2 PLACE DEC	3 PLACE DEC

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC "50" SERIES
TIMING CARD BOARD ASSEMBLY (4TC1)

DIMENSIONS IN INCHES | SCALE | SUB. X 2345678910MK13

DFTM		APPD
CHKD		APPD
SUPV		APPD

743A310
SH 3 OF 9

COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

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Z TO X TRANSFER CARD 1ZX3

A. GENERAL DESCRIPTION

This card provides these gate drives:

$Z \longrightarrow X$
$Z \longrightarrow X$
$\vec{Z} \longrightarrow X$
$\bar{Z} \longrightarrow \bar{F}$
$Z \longrightarrow D$
$D \longrightarrow Z$

The 1ZX3 card also provides gate drives for designator logic to designator gate, clear designator to "Zero" gate, clear designator to "One" gate; and Sequence VI decode.

Figure 3-45 shows the area of the computer which this card provides.

B. CIRCUIT DESCRIPTION

The accompanying block diagram is helpful in study of the following description of the blocks composing this card.

$Z \longrightarrow X$ Gate Drive: Consists of NAND B, C, R59-1, D1-3. C5 enables $Z \longrightarrow X$ gate drive in Sequence V. B11 inhibits $Z \longrightarrow X$ gate drive in Sequence V during a SUB or DCR instruction. C11 inhibits $Z \longrightarrow X$ gate drive in Sequence V during a RSH instruction. B5 is used in a gate drive circuit.

$\bar{Z} \longrightarrow X$ Gate Drive: Consists of NAND K11, L11, G5, R59-2, D1-2. K11 enables $\bar{Z} \longrightarrow X$ gate drive in Sequence V of DCR instruction. L11 enables $\bar{Z} \longrightarrow X$ gate drive in Sequence V of SUB instruction. G5 is used in a gate drive circuit.

$\vec{Z} \longrightarrow X$ Gate Drive: Consists of NAND F, R59-3 and D1-1. F11 enables $\vec{Z} \longrightarrow X$ gate drive in Sequence V of RSH instruction. F5 is used in a gate drive circuit.

$\bar{Z} \longrightarrow \bar{F}$ Gate Drive: Consists of NAND K5 and L5. K5 enables $\bar{Z} \longrightarrow \bar{F}$ gate drive in Sequence III. L5 is a logic inverter.

$Z \longrightarrow D$ Gate Drive: Consists of NAND A. A11 enables $Z \longrightarrow D$ gate in Sequence V of an EDR instruction. A5 is a logic inverter.

$D \longrightarrow Z$ Gate Drive: Consists of NAND J. J11 enables $D \longrightarrow Z$ gate drive in Sequence V of an SDR instruction. J5 is a logic inverter.

Designator Logic to Designator Gate Drive: Consists of NAND D, E5. E5 enables the designator logic to designator gate in Sequence VI of an instruction which terminates in Sequence VI. D5 is a logic inverter.

Clear D to "Zero" Gate: Consists of NAND H11. H11 clears designator to "Zero" prior to designator logic gating. Master Clear also clamps this gate drive.

Clear D to "One" Gate: Consists of NAND E11. E11 clears designator to "One" prior to gating Z Register to designators in EDR instruction.

Sequence VI Decode: Consists of NAND G11.

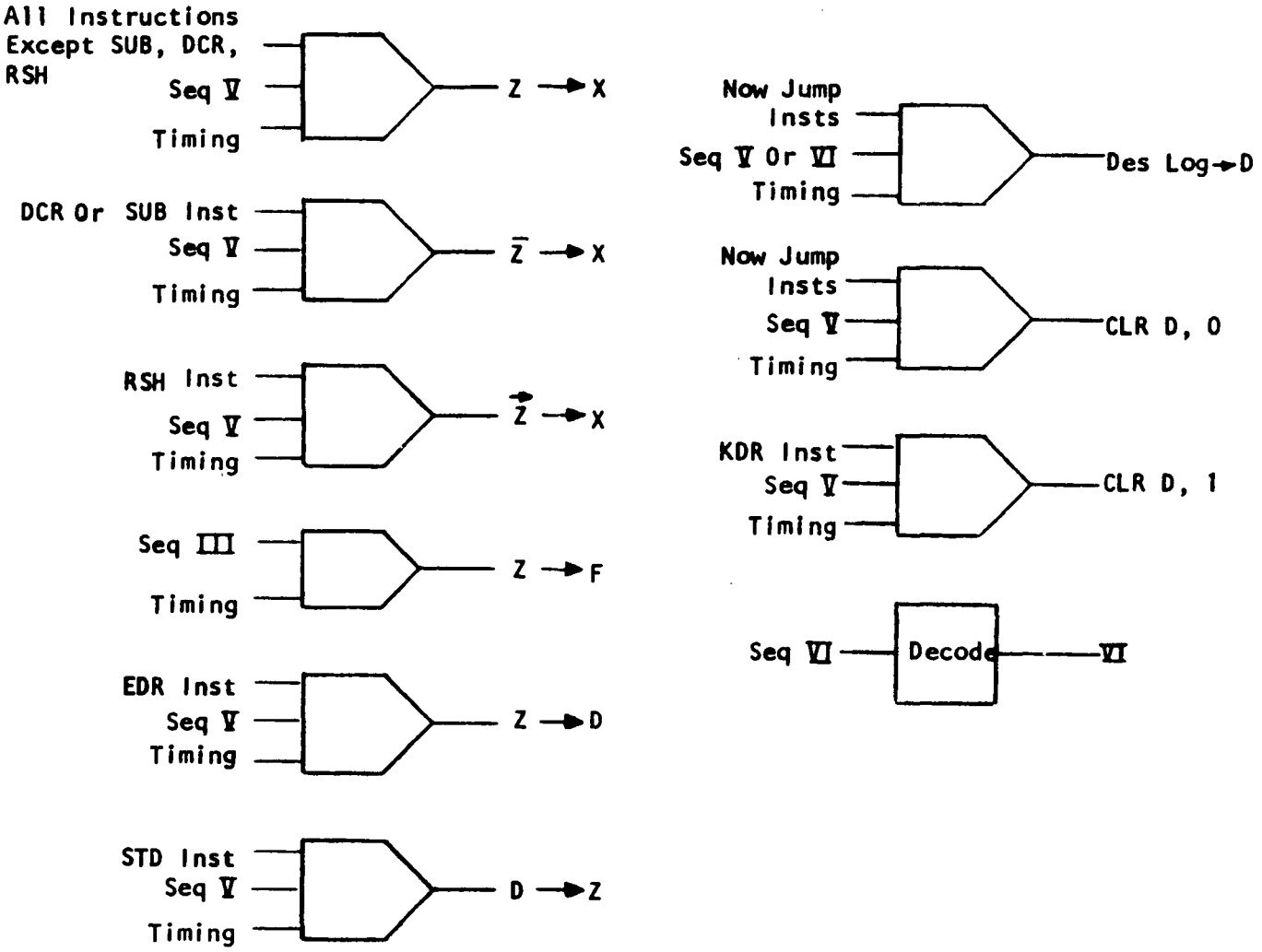
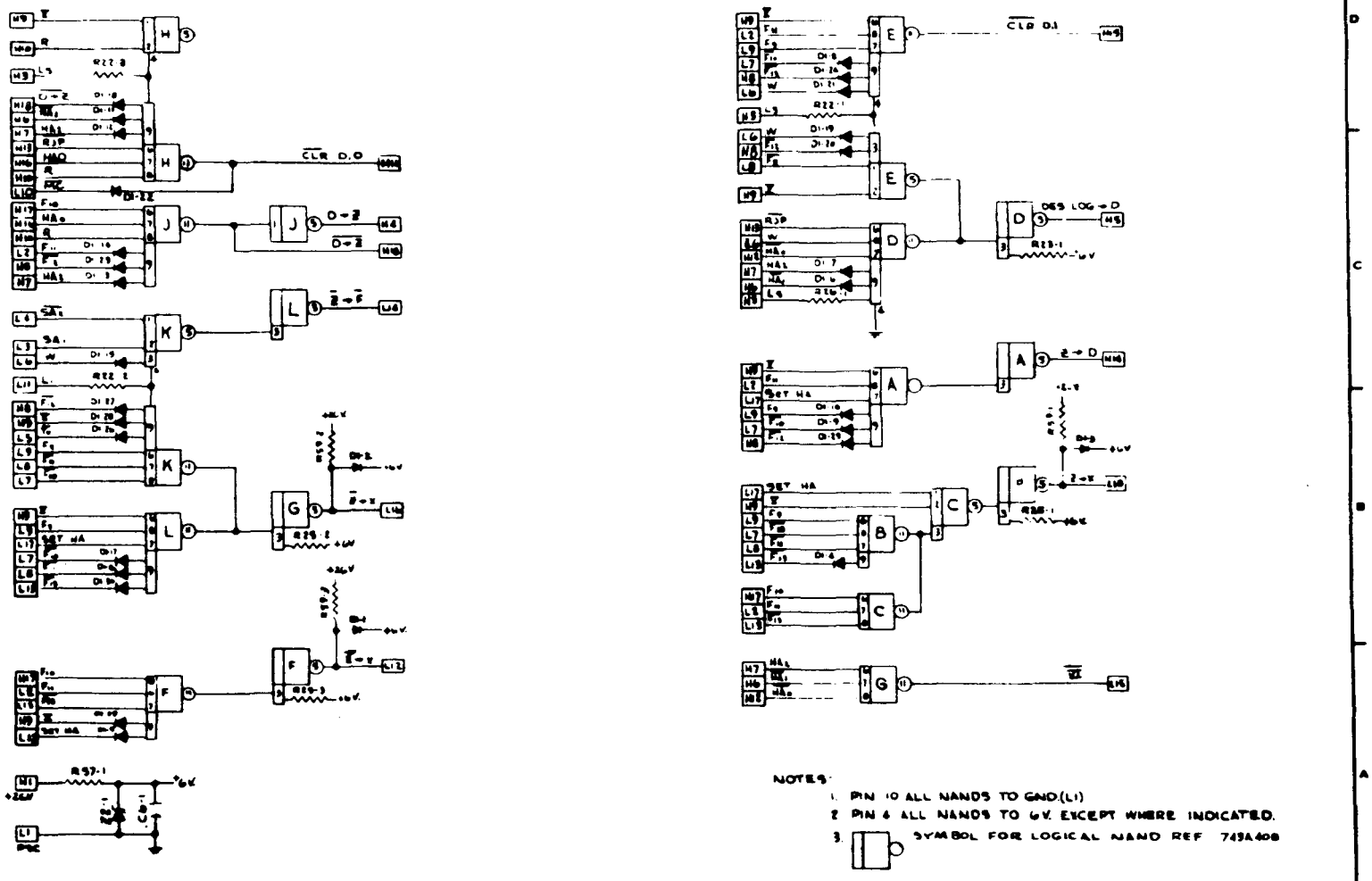


Figure 3-45.

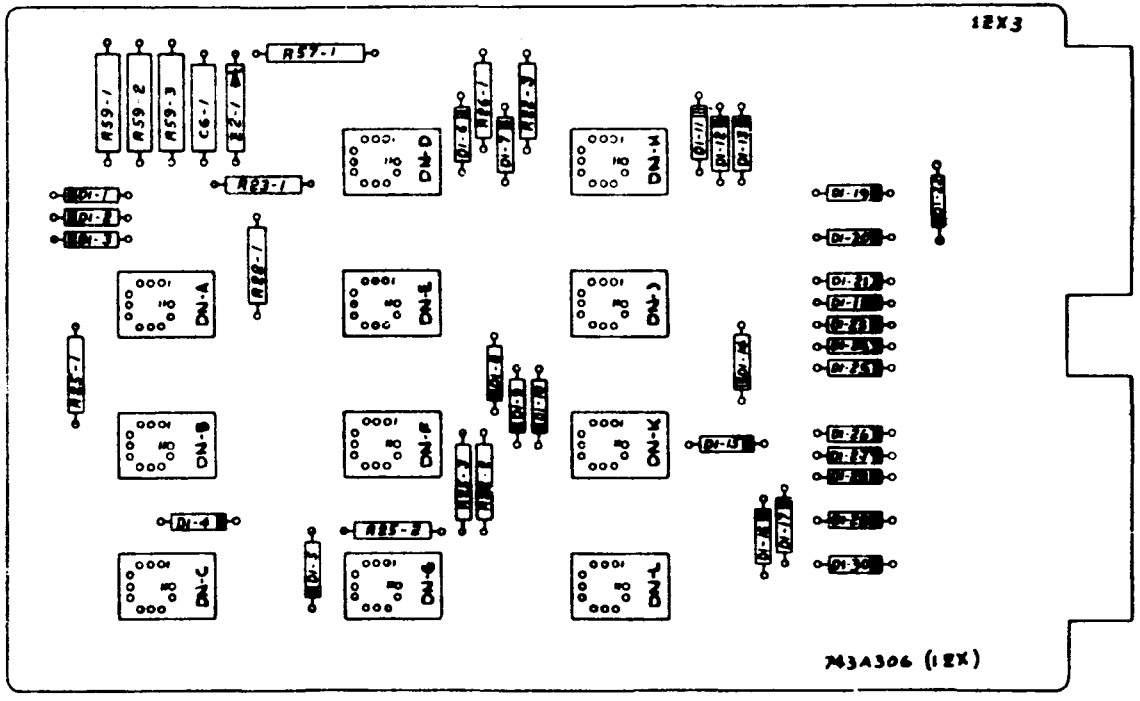


WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
Z → X DATA TRANSFER BOARD SCHEMATIC (REV.)

SIZE D | 743A306 | SH 7 OF 8

COMPUTER SYSTEMS DIVISION



SEE NOTE 9 ON SH.8

NEXT ASS'Y		REF. DWG.	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020R ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN. to 24	± .04	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50 SERIES
Z → X DATA TRANSFER CARD ASSEMBLY (12X3)

SCALE | SUB 1 2 3 4 5 6

743A306
SHEET 2 OF 8

COMPUTER SYSTEMS DIVISION PITTSBURGH PA. U.S.A.

3AC4 - ANALOG CONTROL MODULE

GENERAL DESCRIPTION

This module is used in the Analog Input subsystem to provide proper gating of the output(s) of the voltage-to-frequency converter(s) into the counter(s) (CT module). In addition, the 3AC4 module contains a power supply switch, used to reset the word and channel driver SCR's, and an input by which the Analog Trap (AT module) can open the supply switch. The connection of the 3AC4 module to the Analog Input subsystem is shown in Figure 1.

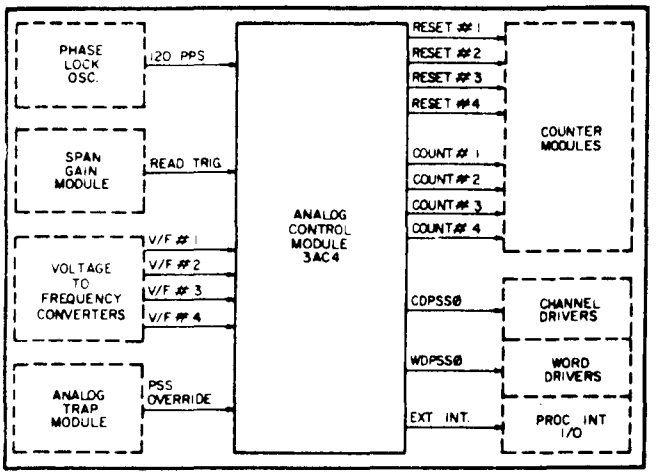


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

- The 120 PPS input requires a 15V, pk-pk, 50% duty cycle, square wave input which is in phase lock with the 60 Hz power line frequency. For 50 Hz power line frequency, the input requirement is 100 PPS instead of 120 PPS. The read trigger input requires 4 μs zero going pulse.

- The V/F (voltage-to-frequency converter) signal requires a logic level positive pulses with a maximum pulse rate of 1 MHz. The power supply switch override input requires a zero voltage level.

Output Capabilities

- Provides logic level "zero" pulse to reset the counters.

- The count signals to the counters are logic level pulses, the frequency and shape is the same as the output of the V/F converter.

- The power supply switch output to the word and channel drivers is normally held to PSC. When the power supply switch triggers this signal goes to +26V (diode coupled) for 1.8 ms.

- The interrupt signal goes from positive (+26V) to near zero to positive and is approximately 1.8 ms in duration.

Power Requirements

Connection to +26V and PSC is required. Power consumption is approximately 350 mA.

CIRCUIT DESCRIPTION

Before discussing the overall operation of the Analog Control circuit, the operation of the following special circuits is described.

NOTE

The following description is for a 60 Hz power line frequency environment. For 50 Hz power line frequency the circuit operation is identical to 60 Hz operation, except the timing pulses are at 100 PPS instead of 120 PPS.

Integrated Circuit Dual NAND - W2

Refer to Figure 2 for schematic and symbol diagrams.

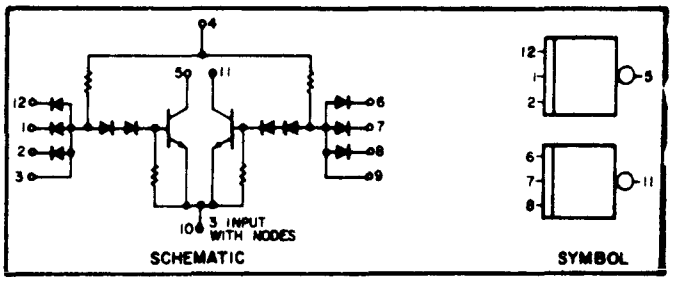


FIGURE 2. IC SCHEMATIC AND SYMBOL

The output transistor can conduct ("zero" state) only if all inputs are high ("one" state) to permit base drive to the output transistor. This is illustrated by the following truth table.

Pin No.			
INPUTS			OUTPUT
12 or 6	1 or 7	2 or 8	5 or 11
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

120 PPS Timing Pulses

Refer to the circuit diagram shown in Figure 3.

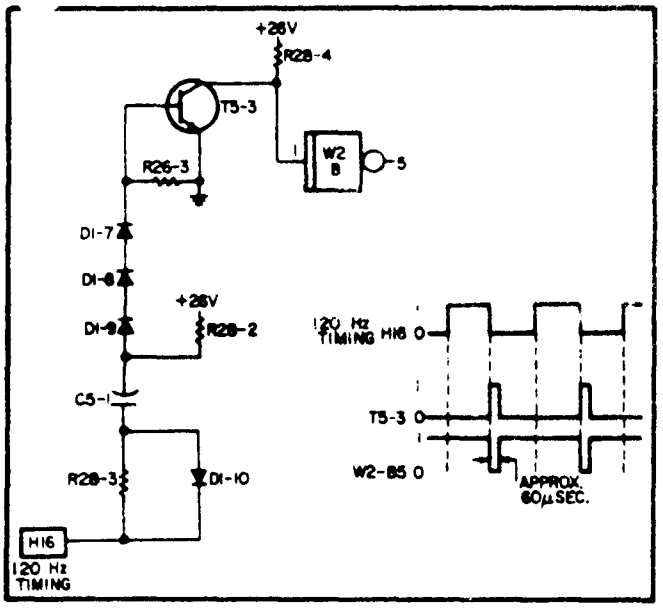


FIGURE 3. 120 PPS TIMING CIRCUIT

Transistor T5-3 is normally conducting due to the base drive supplied by resistor R28-2. The logical "zero" output of T5-3 is inverted to a logical "one" by the integrated circuit module NAND W2-B5. The capacitor C5-1 causes this circuit to differentiate the 120 Hz square wave from the Phase Lock oscillator (PL) module entering Pin H16. The result of differentiation is an approximately 60 μs wide, logical "one" pulse at the output of T5-3 and the complementary pulse at the output of W2-B5. This 120 PPS pulse train is used to sequence the Analog Control module.

Delay Circuit Number One

Refer to Figure 4 for the circuit diagram and Figure 5 for the circuit timing.

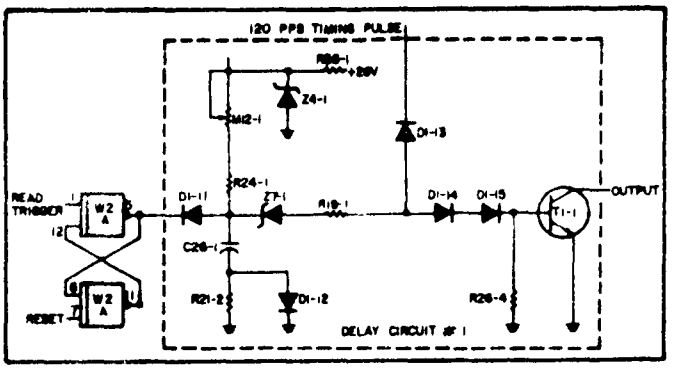


FIGURE 4. NO. 1 DELAY CIRCUIT DIAGRAM

The function of this stage is to provide a minimum time delay between the READ TRIGGER pulse and the first 120 PPS timing pulse used to start the integration period.

Normally, the output of flip-flop W2-A5 is a "zero". Transistor T1-1 is blocking since the cathode of zener diode Z7-1 is near ground. Diode D1-13 is a base drive clamp for transistor T1-1. It permits T1-1 to conduct only at a 120 PPS timing pulse, provided there is base drive through Z7-1.

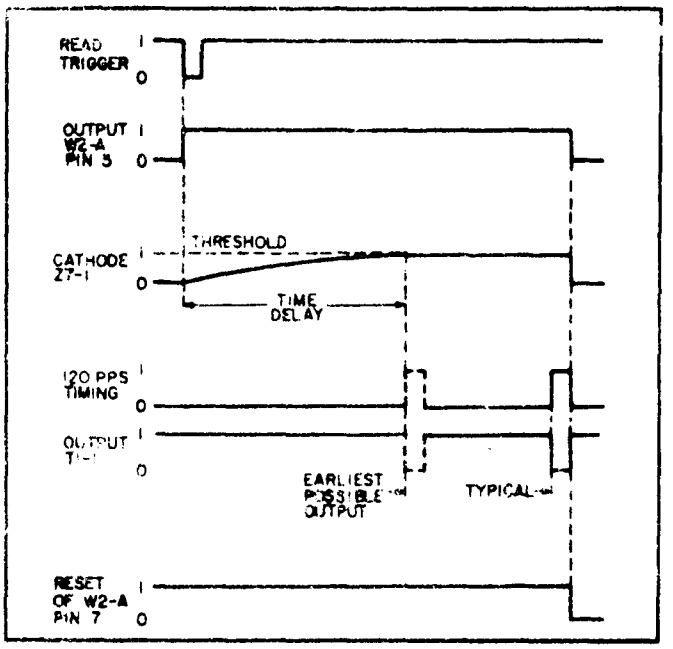


FIGURE 5. NO. 1 DELAY CIRCUIT TIMING

The 4 μs READ TRIGGER pulse starts the time delay by setting flip-flop W2-A5 to a "one". This removes the clamp on capacitor C26-1 which then charges toward the 15V zener supply (Z4-1 and R56-1) through D1-12, R24-1, and M12-1. Potentiometer M12-1 is used to adjust the time delay.

CAUTION

Do not readjust this time delay.

This adjustment is made at the factory and should be readjusted only at the factory due to the difficulties of setup. When the voltage on C26-1 reaches the threshold voltage zener Z7-1 conducts and makes base drive available to transistor T1-1. However, transistor T1-1 continues to block until a 120 PPS timing pulse (a "one" pulse) removes the base drive clamp through diode D1-13. Thus, transistor T1-1 conducts for the duration of the timing pulse.

The delay circuit is reset by a "zero" pulse from the next stage at reset Pin 7 of flip-flop W2-A. Resistor R21-2 is a current limiting resistor for C26-1; it discharges through the output transistor of W2-A5.

Single Stage of Ring Counter

Refer to Figure 6 for the circuit diagram and Figure 7 for the circuit timing.

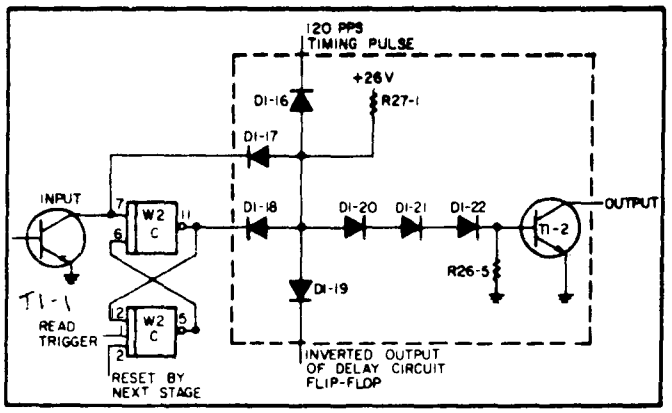


FIGURE 6. RING COUNTER SINGLE STAGE SCHEMATIC

The function of the ring counter single stage is to time $\frac{1}{3}$ cycle of the power line frequency (or one period of the 120 PPS timing pulses) by shifting in a "one" at one timing pulse and shifting the "one" out at the next timing pulse.

W2-C is the memory flip-flop for the timing pulse. Transistor T1-2 and its diodes form a NAND gate which prevents the output of the flip-flop (Pin 11 of W2-C) from setting the next stage when W2-C flip-flop is initially set. Circuit operation is as follows:

Flip-flop W2-C is preset to "zero" (Pin 11) at the beginning of a conversion by the READ TRIGGER pulse. It is set to a "one" by a "zero" at the input (Pin 7) from the previous stage. This input will occur at a timing pulse and the flip-flop W2-C will change state on the leading edge of the timing pulse. Diode D1-17 is connected to the input. When the input is a "zero" this blocks T1-2. Diode D1-19 is connected to the inverted output of the delay circuit flip-flop, which is a "zero" during the delay period. This changes to a "one" at the trailing edge of the timing pulse which enables the ring counter stages. At the next 120 PPS timing pulse transistor T1-2 conducts, thus shifting the "one" to the next stage. Flip-flop W2-C is reset by a "zero" from the next stage at the trailing edge of the timing pulse.

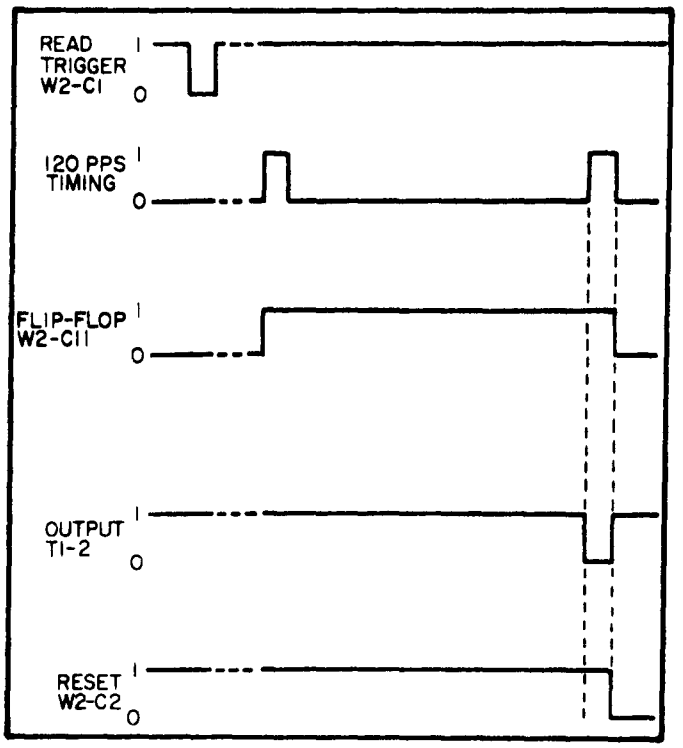


FIGURE 7. RING COUNTER SINGLE STAGE TIMING

Delay Circuit Number Two

Refer to Figure 8 for the circuit diagram and Figure 9 for the circuit timing.

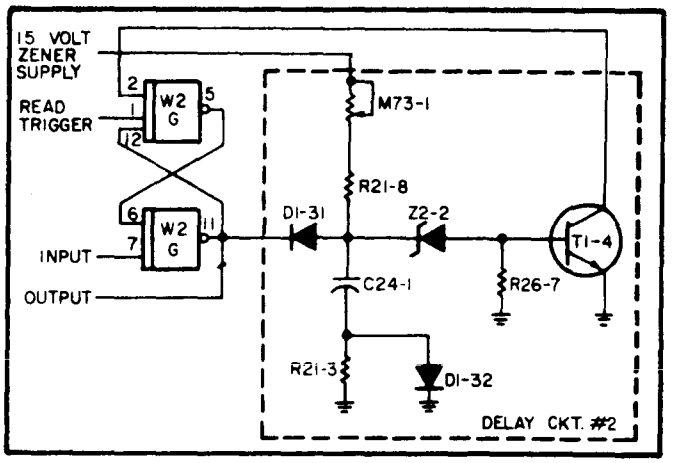


FIGURE 8. NO. 2 DELAY CIRCUIT DIAGRAM

The function of this circuit is to generate, upon pulse command, an output for a fixed time delay.

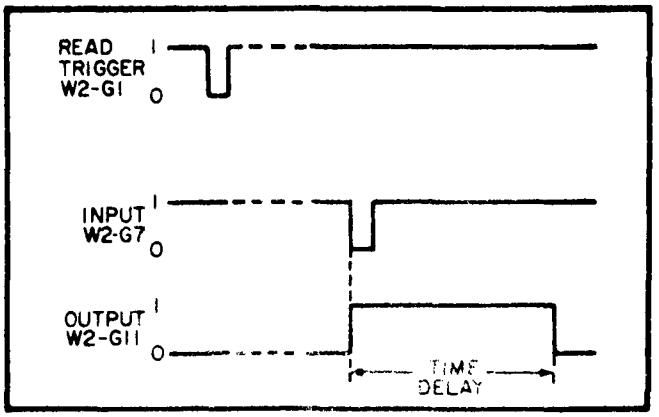


FIGURE 9 NO. 2 DELAY CIRCUIT TIMING

The memory flip-flop W2-G11 is preset at the beginning of a conversion by the READ TRIGGER pulse ("zero" pulse). The output of W2-G11 is therefore a "zero". Transistor T1-4 is blocking. Upon a "zero" pulse input (Pin 7) W2-G11 changes state to an output of "one". This removes the clamp on capacitor C24-1 and permits it to charge toward the 15V zener supply through D1-32, R21-8, and M73-1. Potentiometer M73-1 is used to adjust the time delay. (This adjustment is made at the factory.) When the voltage on C24-1 reaches the zener Z2-2 plus the T1-4 base-emitter voltage, zener Z2-2 conducts and transistor T1-4 is turned on. This action resets flip-flop W2-G11 to a "zero". Resistor R21-3 current limits the discharge of C24-1 through the output transistor of W2-G11.

Power Supply Switch & Analog Completion Interrupt

Refer to Figure 10 for the circuit diagram and Figure 11 for the circuit timing.

The function of this circuit is to supply a ground path for the Word Drivers (WDPSSØ) and the Channel Driver (CDPSSØ), and to generate the Analog Completion Interrupt at the end of the conversion cycle.

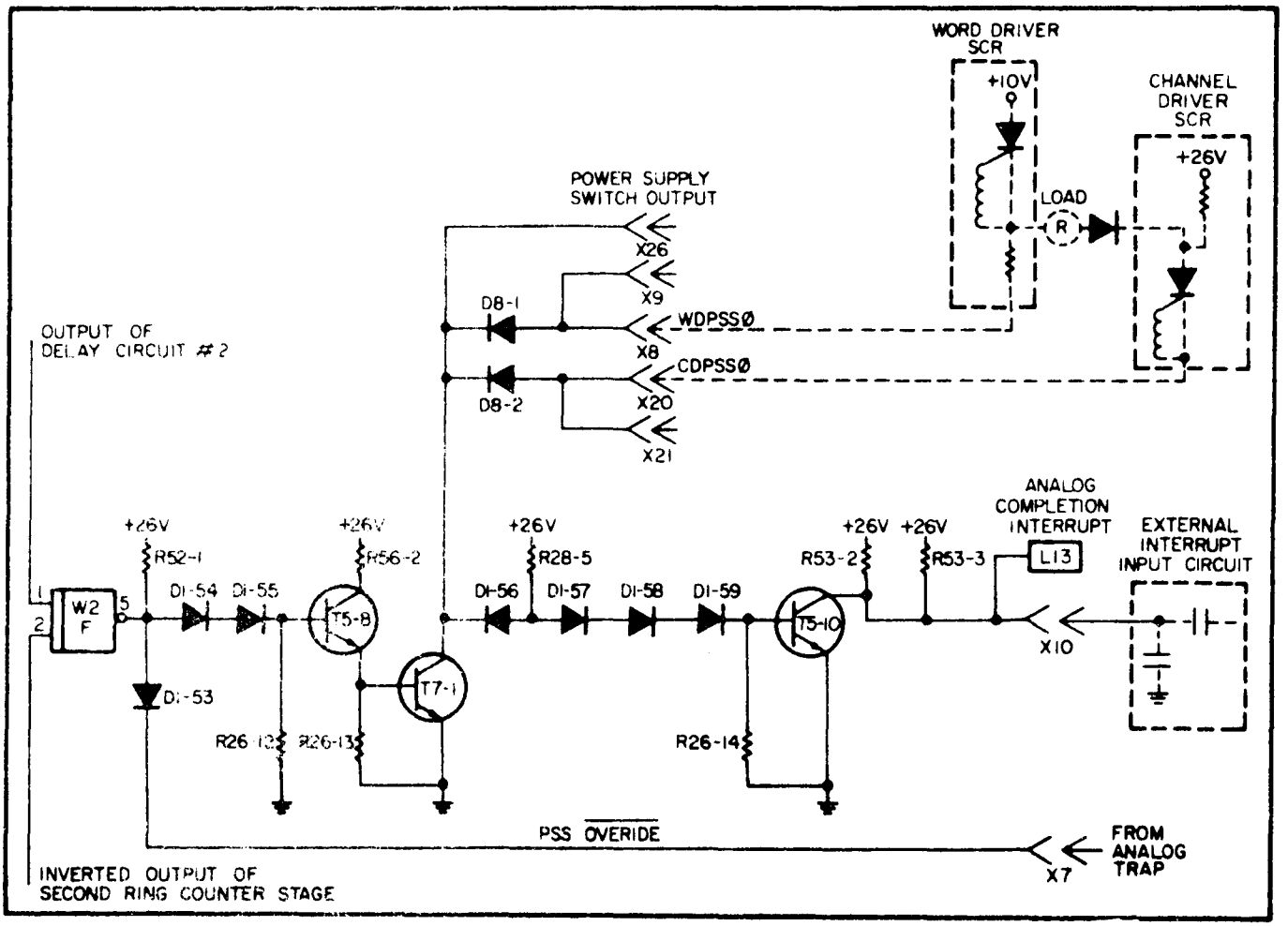


FIGURE 10. PS SWITCH & ANALOG COMPL. INTERRUPT CIRCUIT

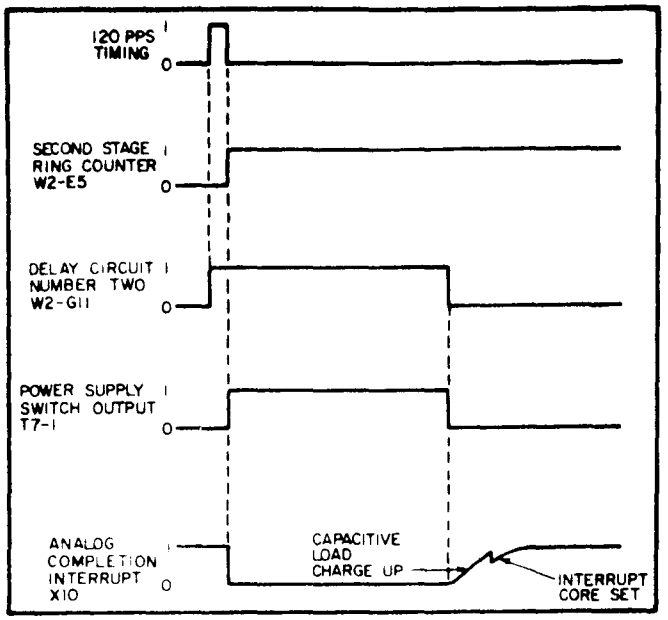


FIGURE 11. PS SWITCH & ANALOG COMPL. INTERRUPT TIMING

Normally, (under steady state conditions), integrated circuit NAND W2-F5 is a "one", thus, transistor T5-8 is conducting and supplying a large base drive to the power supply switch transistor T7-1. Transistor T7-1 is, therefore, normally conducting and providing a ground path to the word and channel drivers. Transistor T5-10 is normally blocking.

When the end of an integration period occurs, the inverted output of the second ring counter stage becomes a "one". Then, for the duration of the "one" output of the delay circuit number two, the output of W2-F5 is a "zero". Therefore, transistor T5-8 and T7-1 are blocking for this period of time. There is sufficient time for the word and channel driver SCR's to turnoff. During this time transistor T5-10 pulls the interrupt signal to ground.

When the output of the delay circuit number two returns to a "zero", transistor T7-1 returns to the conducting state. This action returns transistor T5-10 to the blocking state, thus returning the interrupt signal to + 26V. This positive going pulse is recognized by the process interrupt I/O.

The $\overline{\text{PSS OVERRIDE}}$ connection (Pin X7) from the Analog Trap (AT) module is provided so that upon detection of a multiple point selection, the Analog Trap circuitry can open the power supply switch. A "zero" signal on Pin X7 will open the power supply switch and, therefore, stop the multiple point selection.

AC Module Operation

Refer to the 3AC4 schematic, ㊲ dwg. 743A343. (Fig. 11).

If only the 120 PPS signal is present, it can be seen that no matter what state the flip-flops were in to start, the Analog Control circuitry will come to a stand-still. This occurs when the output of all flip-flops is "zero". In this steady state condition, all flip-flops are reset, which is the same state that exists following the completion of each analog input sequence.

The timing sequence of the Analog Control module is shown in Figure 12.

The sequence begins with the 4 μs READ TRIGGER signal from the span and gain (SB) module, which sets the DELAY CIRCUIT NUMBER ONE-FF via transformer X1-1 and transistor T5-1 and resets all other flip-flops. The DELAY CIRCUIT NUMBER ONE-FF resets all counter modules via transistor T5-2 and times out DELAY CIRCUIT NUMBER ONE for 8 ms to permit sufficient settling time for the point, bus, and guard relays selected and the V/F converter.

The timing sequence (Figure 12) shows three conditions for the READ TRIGGER pulse:

A. For the latest possible READ

B. For the earliest possible READ

C. For a READ which was too late for maximum scan rate (4 ms before timing pulse).

At the next 120 PPS timing pulse leading edge, following the 8.0 ms delay, the first stage ring counter flip-flop W2-C11 is set, which stops the reset of all counters and raises the output of NAND W2-D5 to a "one". The trailing edge of the 120 PPS timing pulse resets the DELAY CIRCUIT NUMBER ONE-FF, which also disables the counter reset and raises the final isolating gate input's to a "one" to enable all isolation gates.

Each V/F converter output is transformer decoupled and isolated from the analog control circuitry via transformers X1-2, X1-3, X1-4, and X1-5. The outputs of the isolating gates to the counters is via transistors T14-1, T14-2, T14-3, and T14-4 for V/F converters numbers 4, 3, 2, and 1 respectively. The isolating gates are enabled for one cycle of the power line frequency.

At the leading edge of the next 120 PPS timing pulse, the second stage ring counter flip-flop W2-E11 is set, which maintains the "one" output of NAND W2-D5. The trailing edge of the 120 PPS timing pulse resets the first stage ring counter flip-flop W2-C11.

At the leading edge of the next 120 PPS timing pulse the DELAY CIRCUIT NUMBER TWO-FF is set and the time delay is started. The trailing edge of the timing pulse resets flip-flops W2-E11 and coincidently closes the isolation gates blocking the V/F output signals and opening the power supply switch.

During the two 120 PPS timing periods the V/F output isolating gates were open for one cycle of the power line frequency. Thus giving the Analog-to-Digital system its noise integration capability.

The power supply switch is opened for 1.8 ms to drop out the Analog Input relays selected. Typically, 0.6 ms following the closing of the power supply switch, the analog completion interrupt is set. With this, the analog conversion cycle is completed.

Note that sufficient time is assured between the opening of the power supply switch and the earliest possible output of the new Analog Input addresses (approximately 100 μs following the setting of the analog completion interrupt) for the previous relays to drop out before the newly addressed relays pick up.

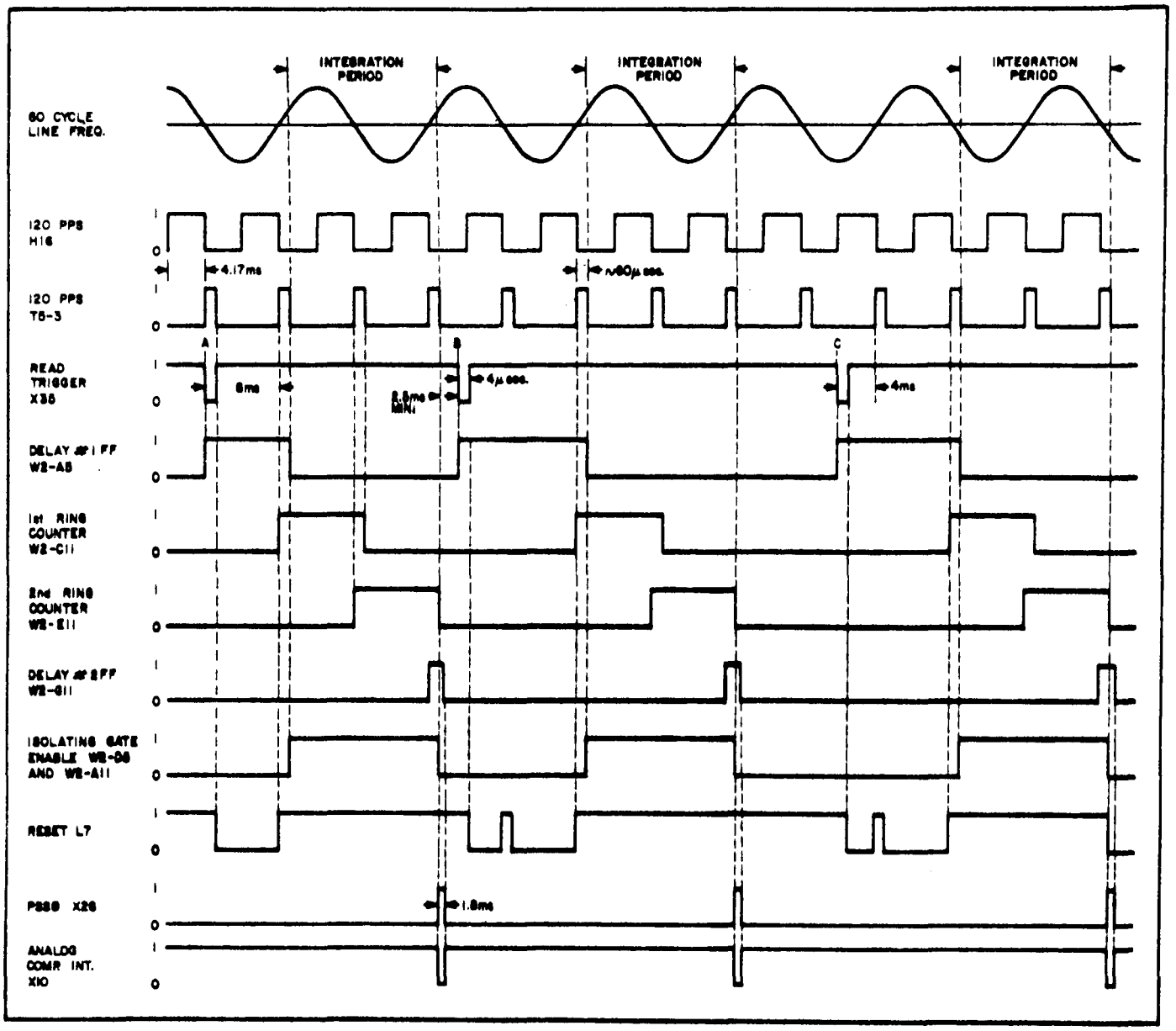


FIGURE 12. ANALOG CONTROL TIMING SEQUENCE

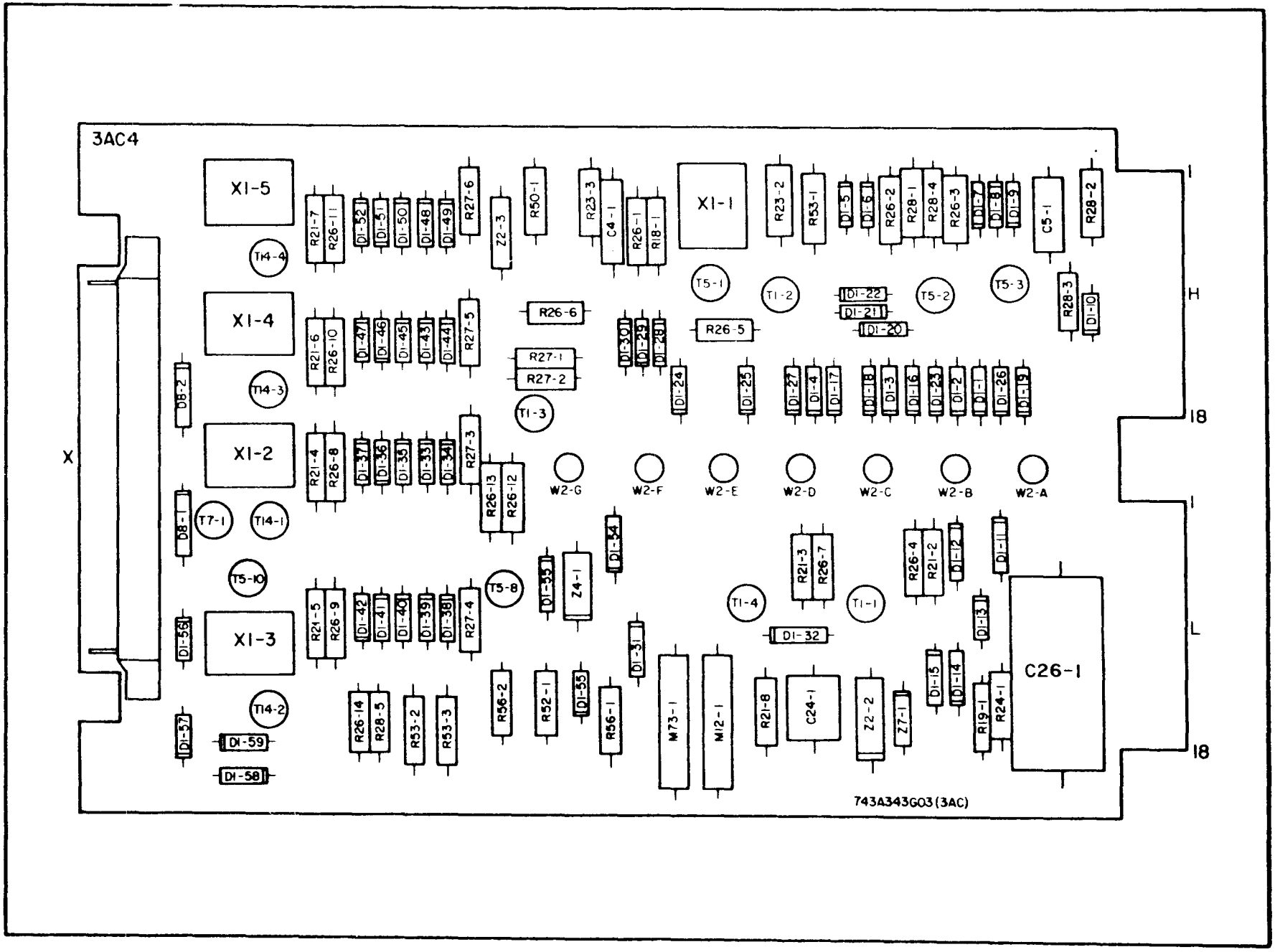


FIGURE 13. 3AC4 ASSEMBLY (REF. DWG. 743A343, SUB 18)

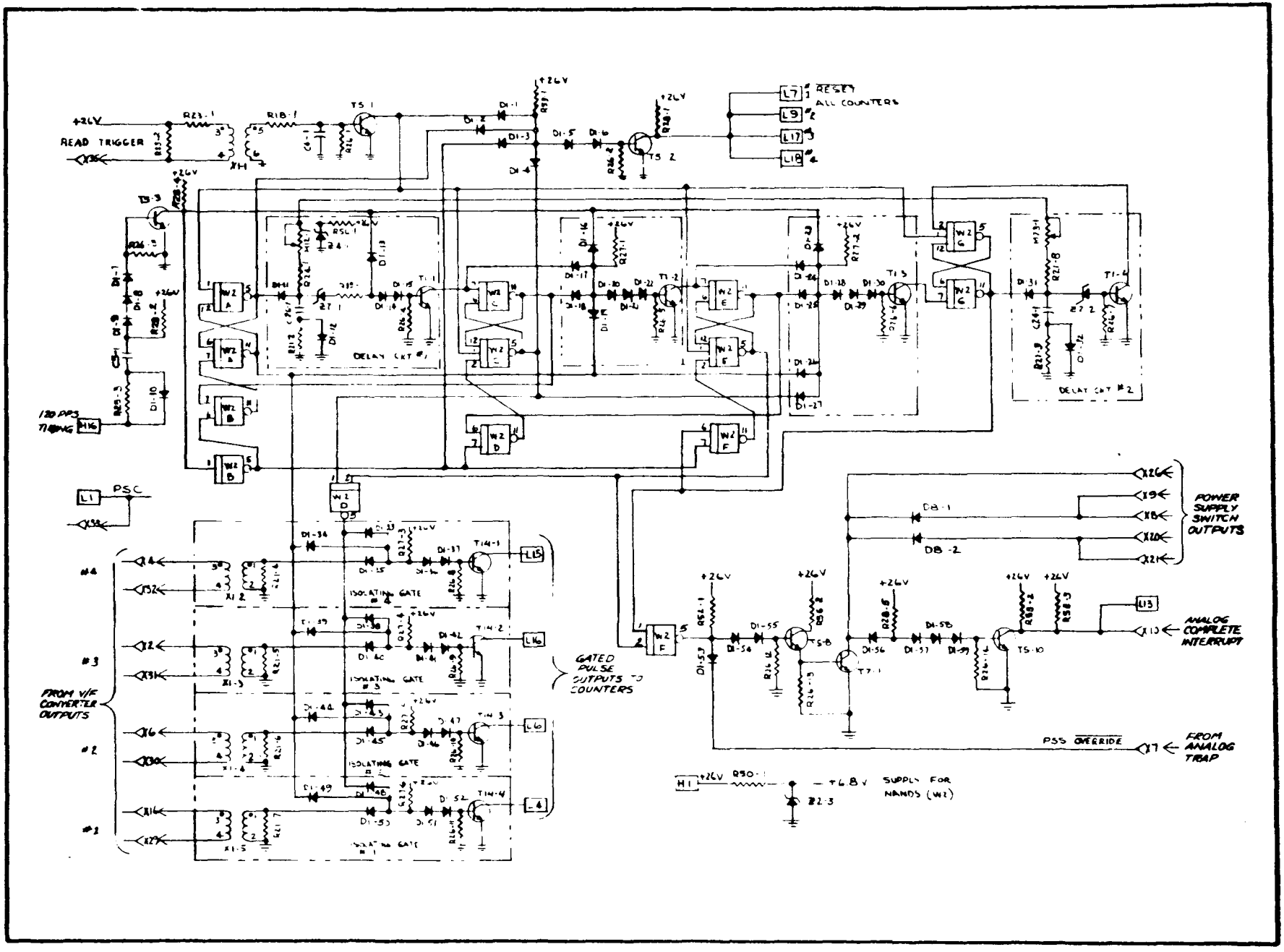


FIGURE 14. 3AC4 SCHEMATIC (REF. DWG. 743A343, SUB 18)

1AO1/1AO3 - 10/11 BIT ANALOG OUTPUT MODULE

GENERAL DESCRIPTION

This card is used to convert binary, digital information into a voltage level. It contains 10 (11 for the 1AO3) mercury-wetted contact, bistable relays which switch resistors in a digital potentiometer to provide 1023 (2047 for the 1AO3) linear steps of voltage output. Each relay has a set and a reset coil. Each coil has a series diode for operation in a matrix and a parallel diode for voltage spike suppression. Resistors are included to provide a suppression ratio of 0.25 (as with a 1-5V output range) and 0.125 (as with a 1-9V output range). With proper cables to an X panel, the card may replace 2 contact-closure output (CO) cards, or it could be switched with contacts or electronic switching. A block diagram of the card is shown in Figure 1.

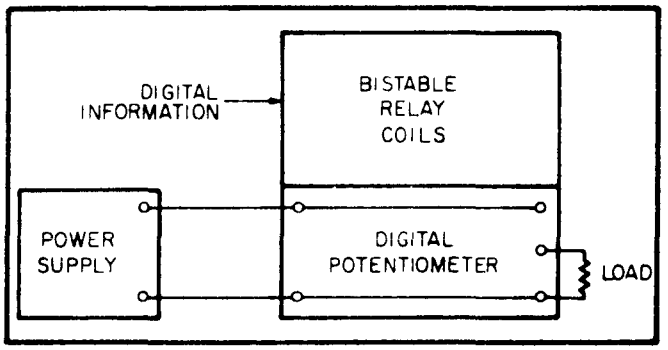


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATION

Input Requirements

Relay Coils

These coils are normally pulsed using word drivers, channel drivers and a power supply switch under program control. If they are switched otherwise the following data can be used:

Type:	Clare HGSM 5235			
Resistance:	675 Ω ± 10% at 25°C			
Turns:	4220			
Must Operate:	6.8 mA (28 A.T. Nominal)			
Must Release:	6.8 mA			
Max voltage at 35°C.	35V			
Max dissipation at 35°C:	1.75W			
Coil rise:	14°C per watt			
Current (mA):	12.7	18.7	30.5	54.2
Operate time(ms):	1.6	1.4	1.3	1.2
Series diode drop:	approx. 0.7V			

Resistor Network

Any changes in the supply voltage to the network will cause the same percentage change in the output. The supply voltage should be regulated to better than that required on the output. The current drawn by the network will vary from 0 to a maximum depending on:

1. The binary number set into the relays.
2. The nature of the load.
3. The zero suppression resistor (R_Z) used, if any.

The maximum load is drawn from the power supply when the conductance of the resistors (including the load) between the output bus and one power terminal equals the conductance of the resistors switched between the output bus and the other power supply terminal. For low resistance loads, this point may not be reached and the maximum current would be drawn when all the relays are set. This would be the case if the load conductance is greater than the conductance of all switched resistors and the zero suppression resistance, if used. For negligible load (high resistance), the supply voltage (E_S) equals the full-scale output voltage (E_H).

To determine the desired input voltage for an appreciable load resistance, we must first define the following:

E_H = Full scale output voltage

I_H = Full scale output current

E_L = Zero scale output voltage

I_L = Zero scale output current

$E_H - E_L$ = SPAN (or $I_H - I_L$ = SPAN)

$s = \frac{E_L}{(E_H - E_L)}$ = suppression ratio or $\frac{I_L}{(I_H - I_L)}$

R_L = Load resistance

$G_L = \frac{1}{R_L}$ = Load conductance

R_z = Zero suppression resistance

$G_z = \frac{1}{R_z}$ = Zero suppression resistance conductance

R_T = Resistance of all switched resistors in parallel (250 Ω)

$G_T = \frac{1}{R_T}$ = Total conductance of the switched resistors (.004 mhos)

For high load resistances (voltage output), the necessary supply voltage can be expressed as:

$$E_S = E_H + \frac{E_H R_T}{R_L (1+s)}$$

For low load resistances (current output), the necessary supply voltage can better be determined as:

$$E_S = I_H R_L + \frac{I_H R_T}{(1+s)}$$

The maximum input voltage, and therefore the output, is limitef by heating in the 500 Ω resistor. The maximum voltage appears across it at approximately midrange, either when it is switched up and all the others down, or vise versa. All the others in parallel approach 500 Ω so that the circuit may be approximated by Figure 6 with $R_A = R_B = 500\ \Omega$.

The 500 Ω resistor is calibrated at 25°C and has a temperature coefficient of ±20 parts per million per °C or ±0.002%/°C. It has a temperature rise of 50°C per watt. To limit its change to less than 0.1%, its dissipation should be limited to 1 watt, giving a maximum voltage of 22.5V across the 500 Ω resistor.

Using this criteria, a graph has been prepared (Fig. 2) showing the output voltage and current ranges that are allowable for the 3 suppression ratios, 0, 0.125, and 0.25 that are available on the card. If other positive suppression ratios, (s), are desired and external resistors are added, the equations for calculating the boundary lines are:

$$E_H = 2\,(22.5)\left(\frac{(1+s)}{(1+2s)}\right)$$

$$E_H = 2\,(22.5)\quad (1+s) \quad - \quad 500\ I_H$$

If a different maximum voltage is to be allowed on the 500 Ω resistor rather than the 22.5V limit set above, the desired voltage would be substituted for the constant 22.5 in the above equations.

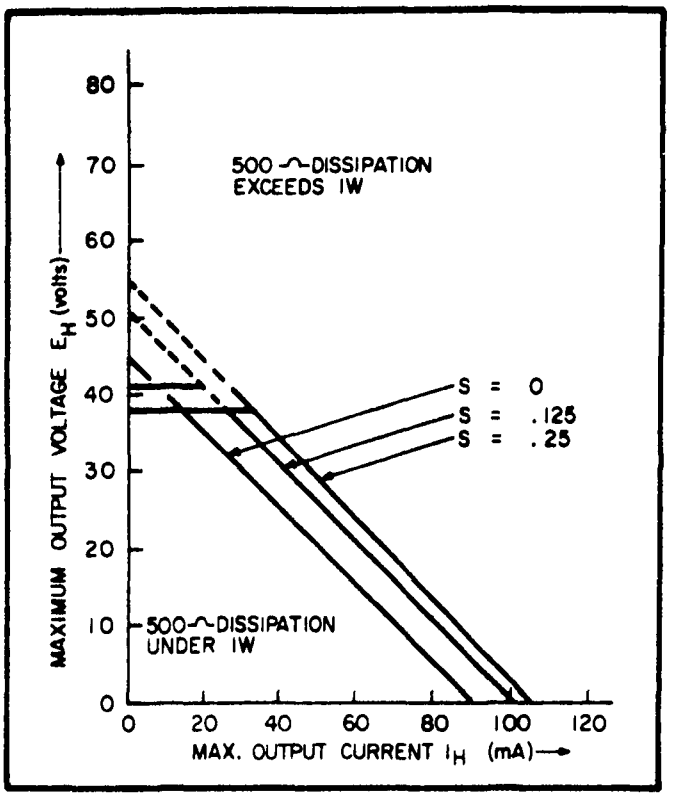


FIGURE 2. OUTPUT VOLTAGE AND CURRENT RANGES

Output Requirements

The maximum output is covered under Input Requirements in determining the input voltages needed to supply a given load. Since the network is simply a voltage divider, one end of the load is connected to the power supply common. All loads fed from one power supply must be capable of being tied to a common.

Power Requirements

The current drawn from the supply varies parabolically with the binary number set into the relays. That is, as the output increases, the power supply current tends to increase, reach a peak, and fall off again. (See Fig. 3 and 4.) In the case of a short circuited load, this degenerates into a straight line and the maximum current drawn is at maximum output and is

$$(1+s)\quad \frac{E_S}{R_T}$$

If the load resistance is less than

$$\frac{R_T}{(1+s)},$$

the inverted parabola never reaches its peak and the maximum supply current also occurs at maximum output

and is

$$\frac{E_S}{R_S + \frac{R_T}{(1+s)}}$$

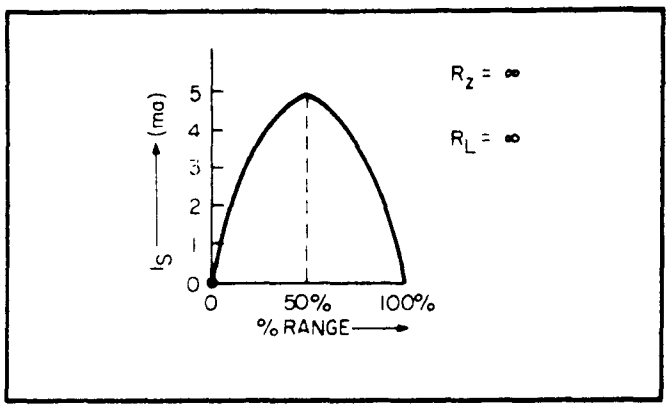


FIGURE 3. SUPPLY CURRENT WITH NO LOAD

If the resistance is greater than

$$\frac{R_T}{(1+s)}$$

the peak of the inverted parabola is reached at an intermediate point where the resistance connected to one power supply terminal equals that connected to the other and the peak current is

$$\frac{E_S\ ((1+s)\ R_L + R_T)}{4R_L R_T}$$

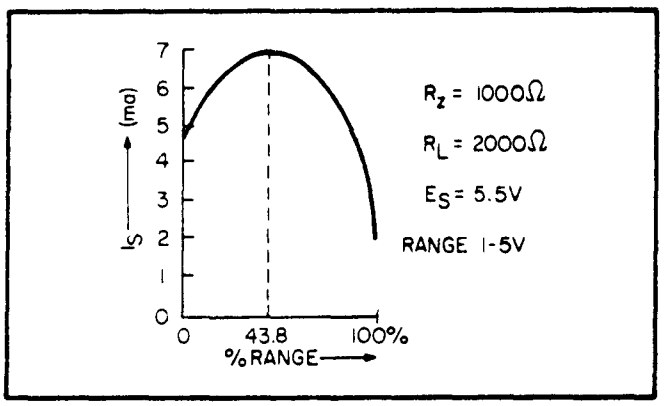


FIGURE 4. SUPPLY CURRENT WITH LOAD AND ZERO SUPPRESSION

CIRCUIT DESCRIPTION

The relay resistor analog output system is in effect, a digital potentiometer. The resistors begin at 500 Ω in the most significant bit and each succeeding one is double the one before it. Thus their conductance is proportional to the worth of the bit they represent. In the typical case, some of the resistors are switched up and others are switched down. Call the parallel resistance of those switched up R_A and those down R_B. (See Fig. 5.) The open circuit output voltage is

$$\frac{R_B}{(R_A + R_B)}\ E_S$$

where E_S is the supply voltage. It is easier to work in terms of conductance G and the output voltage is then expressed as

$$\frac{G_A}{G_A + G_B}\ E_S = \frac{G_A}{G_T}\ E_S$$

Note the numerator is G_A. The denominator is constant (G_T) since it is the sum of the conductances of all the resistors and is approximately 1/250 or 0.004 mhos.

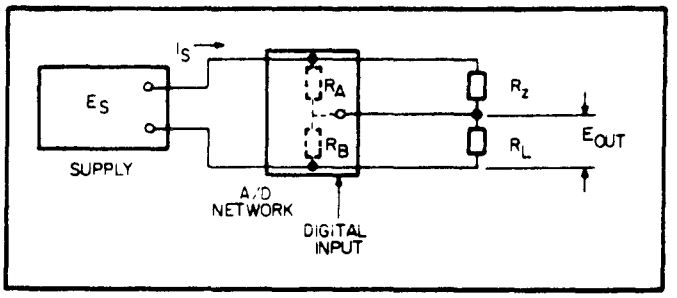


FIGURE 5. LOAD DIAGRAM

Assuming a well regulated power supply, the internal impedance of the supply is negligible and the Thevenin looking-in resistance is simply all the resistors in parallel or approximately 250 Ω. The Thevenin open-circuit voltage is proportional to the binary number set into the relays. With all resistors switched up, the open circuit output voltage is the supply voltage E_S. (See Fig. 6.)

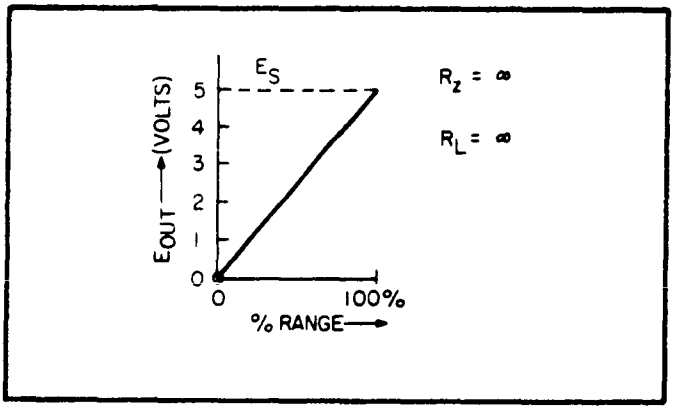


FIGURE 6. OUTPUT WITH NO LOAD

If an appreciable load is added, the full scale output droops but the output remains linear since the Thevenin looking-in resistance remains constant. The supply voltage can be raised (see Input Requirements) to bring the full scale output up as desired. Another way to look at it is to consider the load conductance a constant G_L being added to G_B. The output then is

$$\frac{G_A}{(G_B + G_B + G_L)} E_S = \frac{G_A}{G_T + G_L} E_S$$

where the denominator is fixed for a fixed load. To achieve a positive suppression as, for example, a range of 1-5V, a zero suppression resistor (R_Z) with a conductance G_Z can be added in parallel with R_A. The output is then

$$\frac{G_A + G_Z}{(G_T + G_L + G_Z)} E_S$$

For the low end output $G_A = 0$ and

$$E_{OUT} = \frac{G_Z}{(G_T + G_L + G_Z)} E_S$$

while the high end output is

$$\frac{G_T + G_Z}{(G_T + G_L + G_Z)} E_S$$

since $G_A = G_T$. The difference between these two is called the SPAN. The suppression ratio is the low end value divided by the SPAN, in this case (1/(5-1)) or 0.25. (See Fig. 7.)

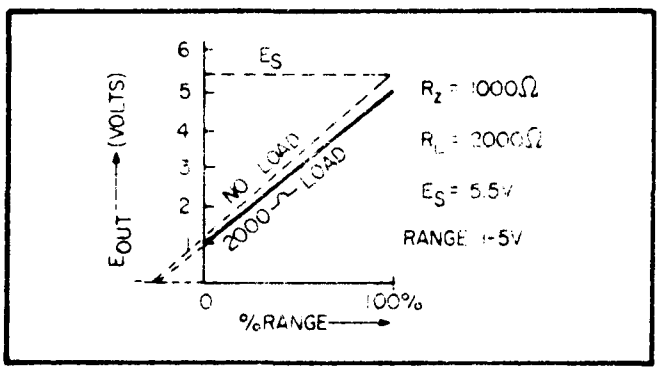


FIGURE 7. OUTPUT WITH LOAD AND ZERO SUPPRESSION

As it turns out, the required zero suppression conductance G_Z is the potentiometer total conductance G_T times the suppression ratio or R_Z

$$R_Z = \frac{R_T}{s} = 250/s$$

In this case, it is 0.004 x 0.25 or 0.001 mhos. The resistor needed is 1000 Ω, regardless of load for s = 0.25. The necessary supply voltage E_S is that needed to give the load voltage plus the drop across G_A and G_Z. At full scale, $G_A = G_T$ and the load voltage is E_H so

$$E_S = E_H + \frac{I_H}{G_Z - G_T}$$

Substituting

$$I_H = \frac{E_H}{R_L} \quad \text{and} \quad G_Z + G_T = (1 + s)(G_T) = \frac{(1+s)}{R_T}$$

we get

$$E_S = E_H + \frac{E_H R_T}{R_L (1+s)}$$

For low resistance loads where the network acts more like a current source it is more convenient to substitute

$$E_H = I_H R_L \quad \text{and} \quad (G_Z + G_T) = \frac{(1+s)}{R_T}$$

as before and use

$$E_S = I_H R_L + \frac{I_H R_T}{(1 + s)}$$

In the sample case (Fig. 5),

$$E_S = 5 + 5 \times \frac{250}{2000\ (1 + 0.25)} = 5.5V$$

Two, zero suppression resistors are furnished on the card and can be jumpered in on the terminal blocks. They are R178-2 (1000 Ω for a 0.125 suppression ratio). Current drawn from the supply varies parabolically with the number set into the relays. For high resistances it is a maximum when the conductance above the output bus equals that below. The maximum supply current is $E_S (1/4)(G_L + G_T + G_Z)$ which may be expressed as

$$E_S \frac{R_T + (1+s) R_L}{4R_T R_L} = E_S \frac{(1+s)}{4R_T} + \frac{1}{4R_L}$$

In the sample case with R_L = 2000 Ω, the maximum supply current is

$$5.5 \times \left(\frac{1.25}{1000} + \frac{1}{2000}\right) = 5.5\ (0.00125 +$$

$$0.000125) = 0.00758\ A$$

As the load resistor is decreased, its conductance G_L

increases and the peak current is drawn from the power supply closer to full scale. When G_L exceeds $G_Z + G_T$, the peak is never reached and the peak current is that drawn at full scale. In terms of resistors, this occurs if

$$R_L < \frac{R_Z R_T}{(R_Z + R_T)}$$

Substituting $R_T = 250$ and $R_Z = 250/s$ gives the criteria:

$$\text{if } R_L < \frac{250}{(1 + s)} ,$$

the maximum power supply current is drawn at full scale and is

$$R_L + \frac{250}{(1 + s)}$$

The percent of full scale at which this occurs is 50

$$\left(1 - s + \frac{R_T}{R_L} \right) \%$$

In the sample case, this is 50

$$\left(1 - 0.25 + \frac{250}{2000} \right) \% = 43.8\%$$

(If this exceeds 100%, the value at full scale must be used as covered above.)

The output increases linearly with the binary number set into the relays. Thus, maximum output is achieved by picking up all relays: and zero scale, by dropping out all relays. Picking up the most significant bit relay, 500 Ω resistor and changes the output by 50% of the span. The next relay gives a 25% change, the next 12.5%, etc. The bit pattern set into the relays must be thought of as a binary fraction with the binary point to the left of the most significant bit furnished on the board. This pattern represents the fractional part of the range to be output. In this way, 100% of full scale is only approximated within 1 step, but the voltage supply is generally adjusted for 100% output with all relays up.

* * *

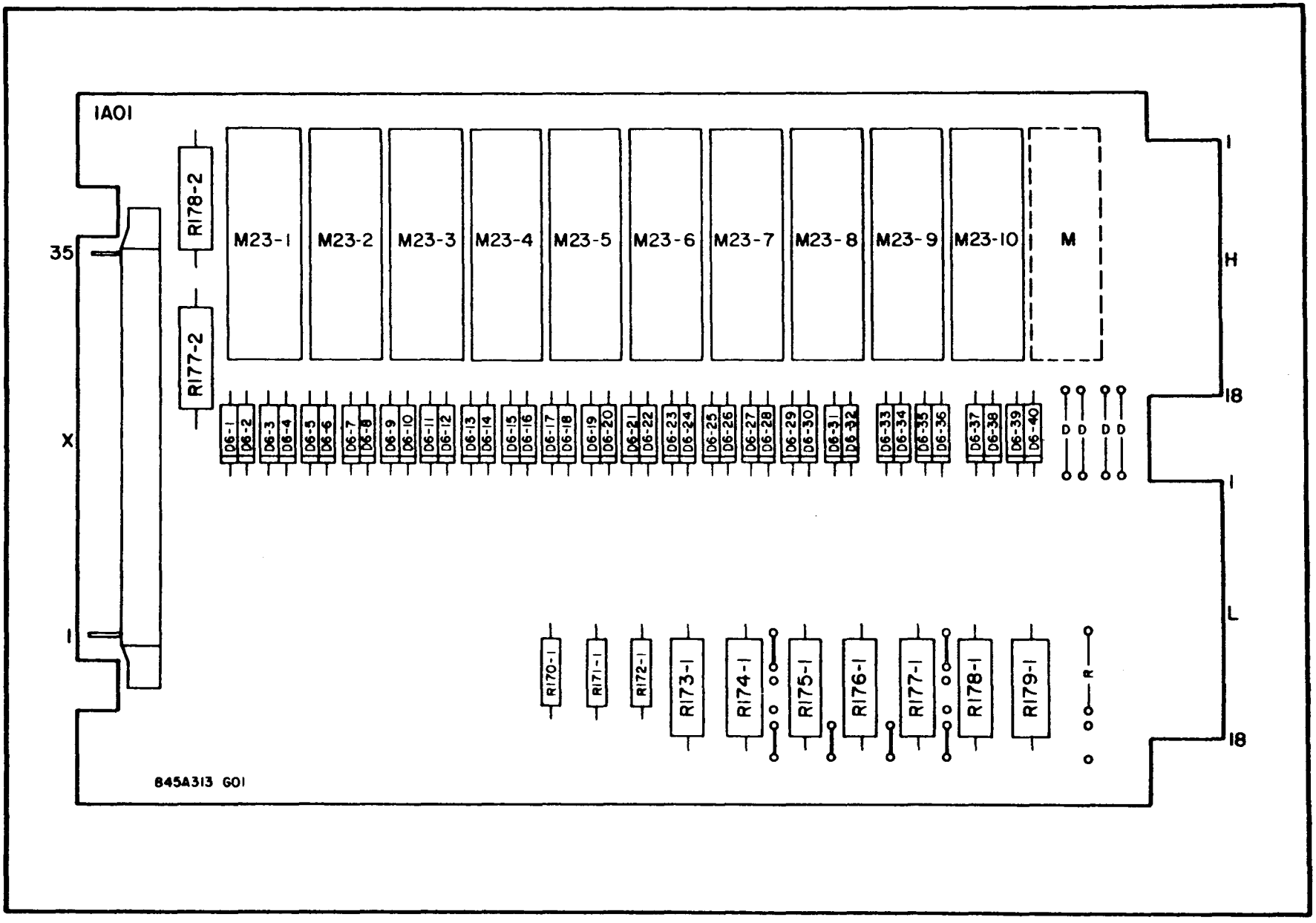


FIGURE 8. 1A01 ASSEMBLY (REF. DWG. 845A313, SUB 3)

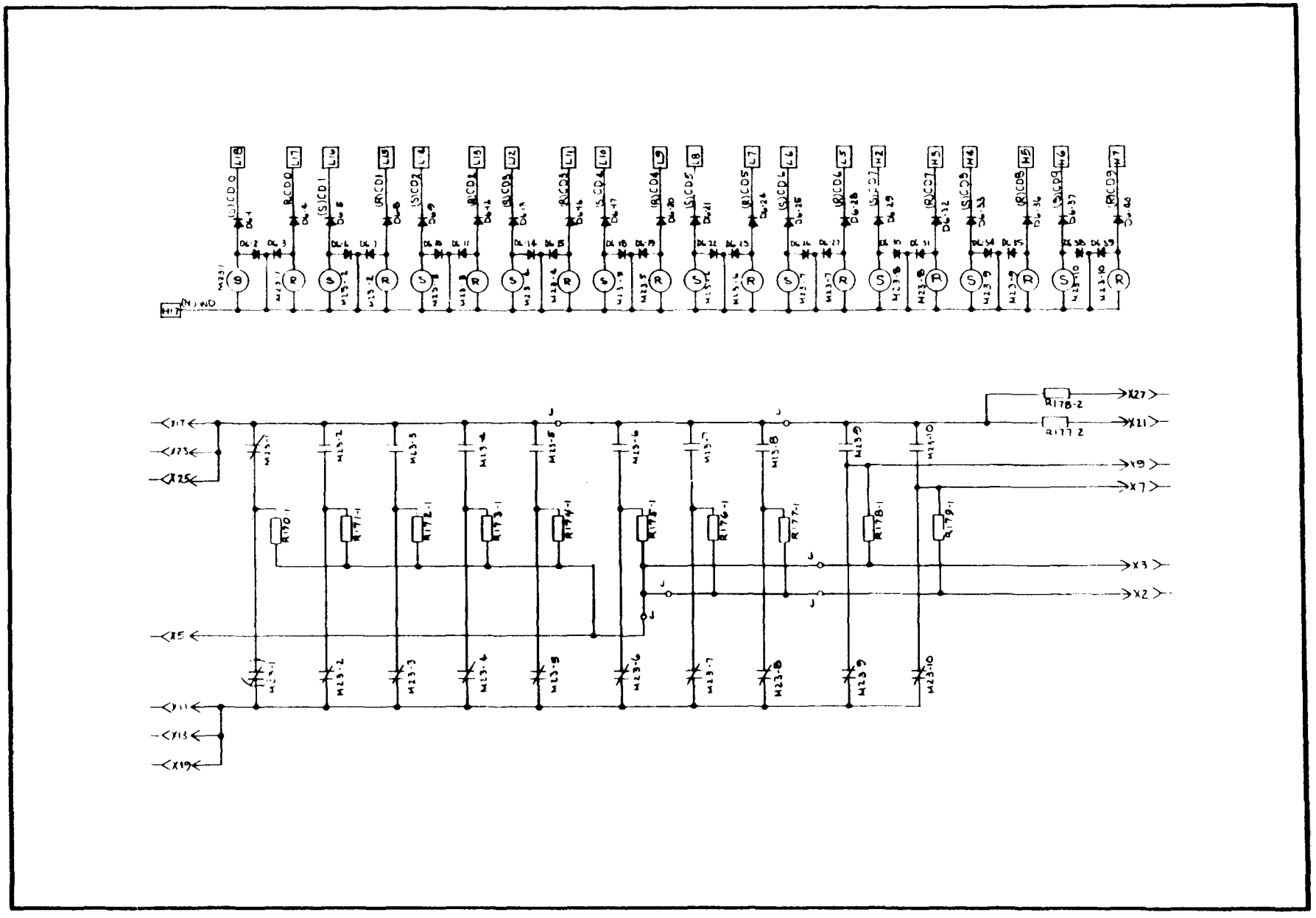


FIGURE 9. 1A01 SCHEMATIC (REF. DWG. 845A313, SUB 3)

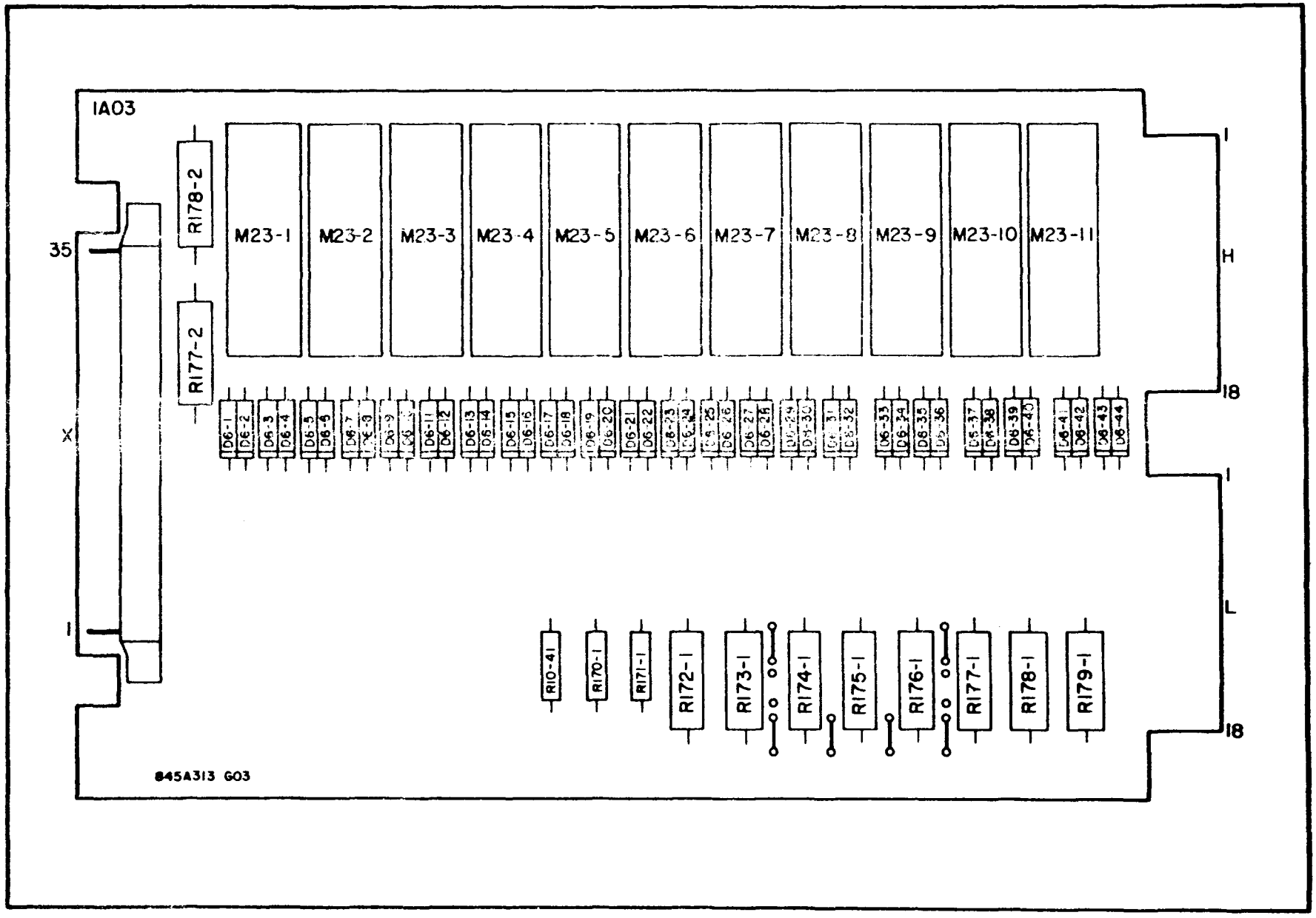


FIGURE 10. 1A03 ASSEMBLY (REF. DWG. 845A313, SUB 3)

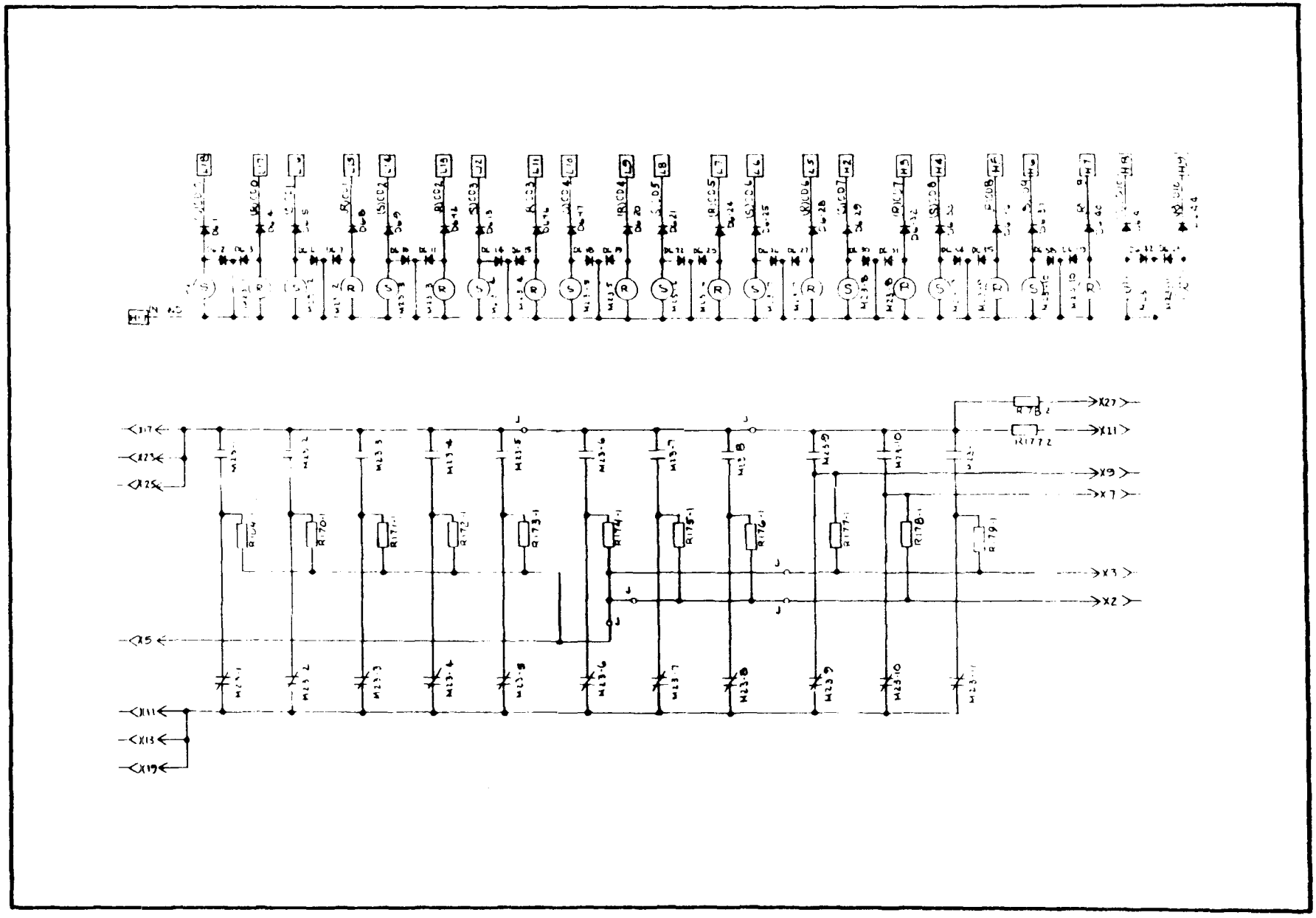


FIGURE 11. 1A03 SCHEMATIC (REF. DWG. 845A313, SUB 3)

1AO2 - 5-BIT REVERSIBLE ANALOG OUTPUT MODULE

GENERAL DESCRIPTION

This card is used to convert binary digital information into a current or voltage level. A typical load is a low resistance, electrically isolated, magnetic amplifier control winding. Using a 25V power supply, two nominal output ranges are available, 10-0-10 mA and 80-0-80 mA.

The card contains 7 mercury-wetted contact, bistable relays, 5 of which switch resistors in a digital potentiometer while the other 2 reverse the polarity of the load. With 5-bit accuracy, 32 linear output levels are available in either direction. With zero output being included for each polarity, 63 discrete output levels are possible. The impedance seen by the load will be constant, regardless of level. This card can be plugged into a contact closure output slot and an 8-pair cable, M110 (originally used with the CB card) will connect its output to 1 terminal block on the "half shells". The same cable used with the CCO's may be used, connecting to suitable terminals on the half shell terminal blocks.

CIRCUIT SPECIFICATION

Input Requirements

Relay Coils

These coils are normally pulsed using word drivers, channel drivers and a power supply switch under program control. If they are switched otherwise the following data can be used:

Type:	Clare HGSM 5235 (1142 for reversing)
Resistance:	675 Ω ± 10% at 25°C
Turns:	4220
Must Operate:	6.8 mA (28 A.T. Nominal)
Must Release:	6.8 mA
Max voltage at 35°C:	35V
Max dissipation at 35°C:	1.75W
Coil rise:	14°C per watt

Current (mA):	12.7	18.7	30.5	54.2
Operate time (msec):	1.6	1.4	1.3	1.2

Series diode drop: approx. 0.7V

Resistor Network

Nominal input voltage is 28Vdc. Any change in input voltage causes the same percentage change in the output current. The maximum current drawn from the power supply when using the 80-0-80 mA range occurs at full-scale output and is 28V/ (326 + R_L) where R_L is the load resistance including line resistance. If R_L = 0, the current is 85.4 mA, which is also the maximum output current. To go to the 10-0-10 mA range, additional resistance is inserted in series with the load and the maximum current is drawn from the supply when the output is about 55% of the full-scale, and is about 31 mA, assuming a short circuited load. Beyond 55%, the current decreases again until at full-scale it is

$$\frac{28}{(256 + 2470)}$$

or about 11 mA, which is the output with zero load (including line) resistance.

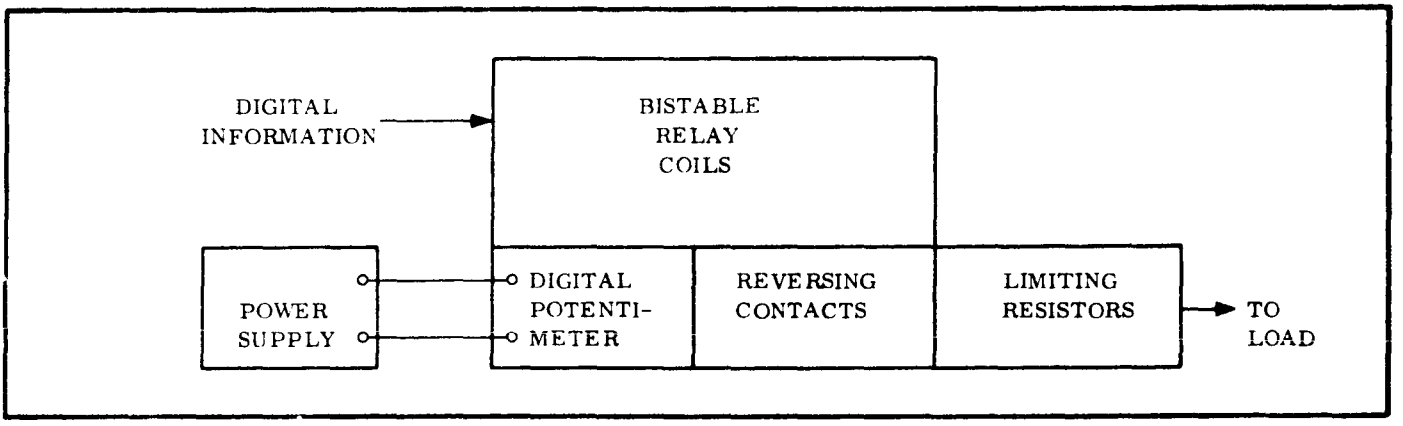


FIGURE 1. BLOCK DIAGRAM

Output Requirements

For the 80-0-80 mA range, the load is connected to X3 (+) and X2 (-). Two, 35 Ω current limiting resistors on the card are in series with the load to avoid damage in case of connection errors. If the power supply has negligible internal impedance, the switched resistors can be considered connected in parallel when calculating the resistance as seen by the load. Thus, the load, which may be a magnetic amplifier winding, will see a constant resistance regardless of the output level. All the switched resistors in parallel equal about 256 Ω. The total resistance as seen by the load is 256 + 2x35 = 326 Ω.

To use the 10-0-10 mA range, additional resistance (2-1200 Ω) is inserted in series with the load when connecting to the 10-0-10 mA output terminals X9 (+) and X7 (-). This raises total resistance seen by the load to about 2730 Ω.

Note the output is linear, that is the steps are even, regardless of load. Also note that a single power supply is used and reversed polarity output is obtained by switching the load leads. This requires the load to be electrically isolated. If it is not, individual isolated power supplies would be needed to supply reversed-polarity output to loads connected to a common.

Other ranges could be achieved by varying the input voltage, adding series load resistance, or connecting the load across X3 and X7 so that only one 1200 Ω resistor would be in series with the load. This would give a looking in resistance of 1491 Ω.

Contact protection is furnished across the reversing contacts which are the bridging type.

Power Requirements

Input and output are generally limited by heating in the 500 Ω resistor which is rated 5W. However, the dissipation must be limited to less than this to avoid board damage. With 120 mA output on the 80-0-80 range, the dissipation would be about 1.8W which has been found safe. If higher outputs are needed, they should be checked experimentally.

On the 80-0-80 range, the voltage needed may be determined as the full load current times (326 + R_L) where R_L is the load resistance. On the 10-0-10 range, use 2656 instead of 326. Nominal voltage is 28V.

Changes in input voltage are reflected directly as output changes. The supply regulation should be as good as, or better than, the desired output stability. With 3% steps, a 1% supply is recommended.

CIRCUIT DESCRIPTION

Five resistors, whose conductance is proportional to the binary bit they represent, are connected to the output bus. Their other ends are switched by relay contacts to either the positive or negative supply terminal which can be considered the output common. The open circuit output voltage is proportional to the conductance switched to positive. Two other relays reverse the load on the output terminals to provide negative output. Two 35 Ω resistors limit the current in the load circuit in case voltage gets connected to it by mistake. Two 1200 Ω resistors limit the output if the nominal 10-0-10 output range is desired.

Note that in outputting binary information to this card, the magnitude of the step must be output to bits 0-4 (7-11) and is always handled as a positive number. Bit 6 (13) can be considered as the sign bit (0 is + and 1 is -), while bit 5 (12) will be its complement. The bit pattern for a positive step 3 is 0100011 while a negative step 3 requires 1000011.

* * *

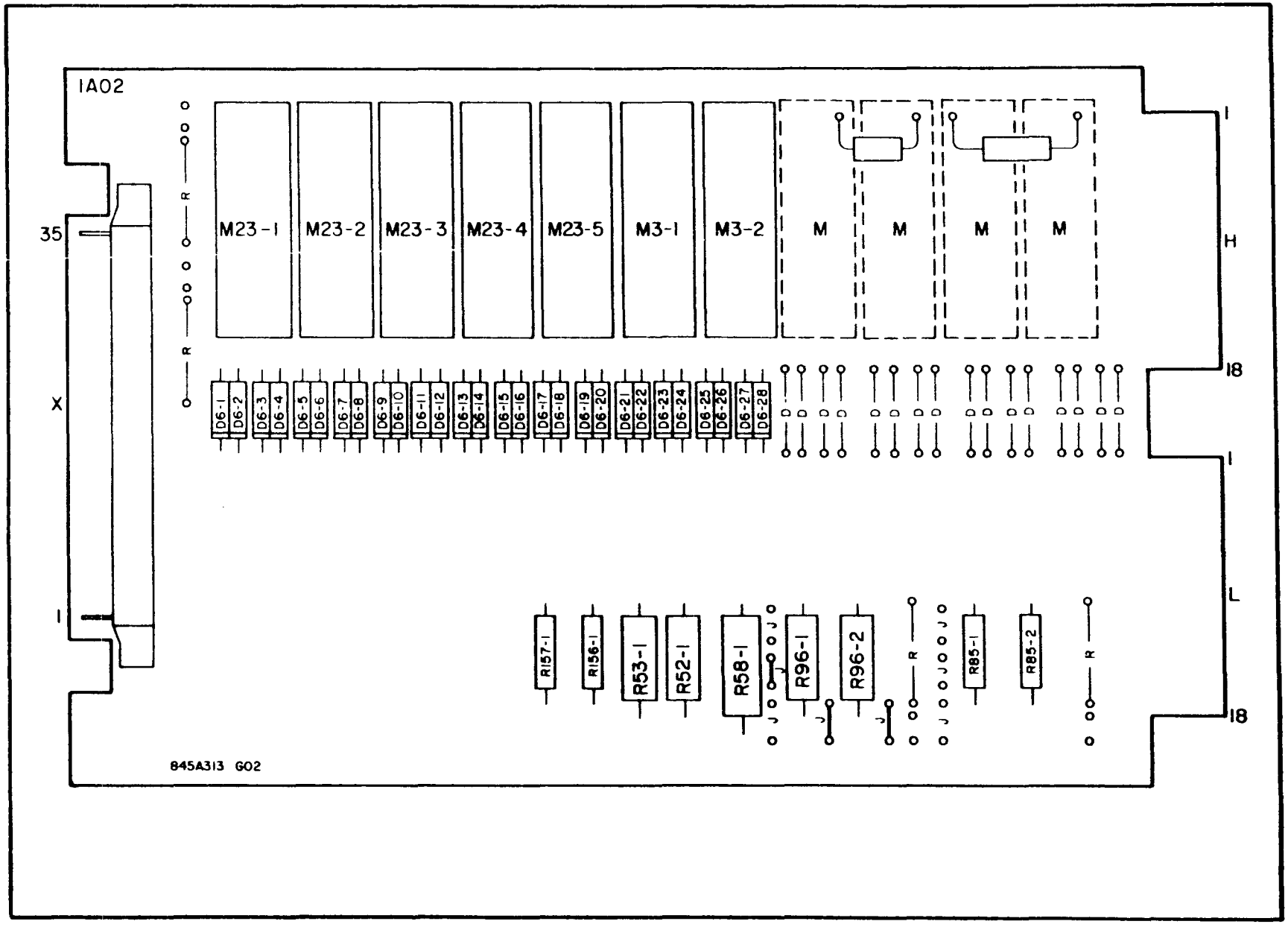


FIGURE 2. 1A02 ASSEMBLY (REF. DWG. 845A313, SUB 3)

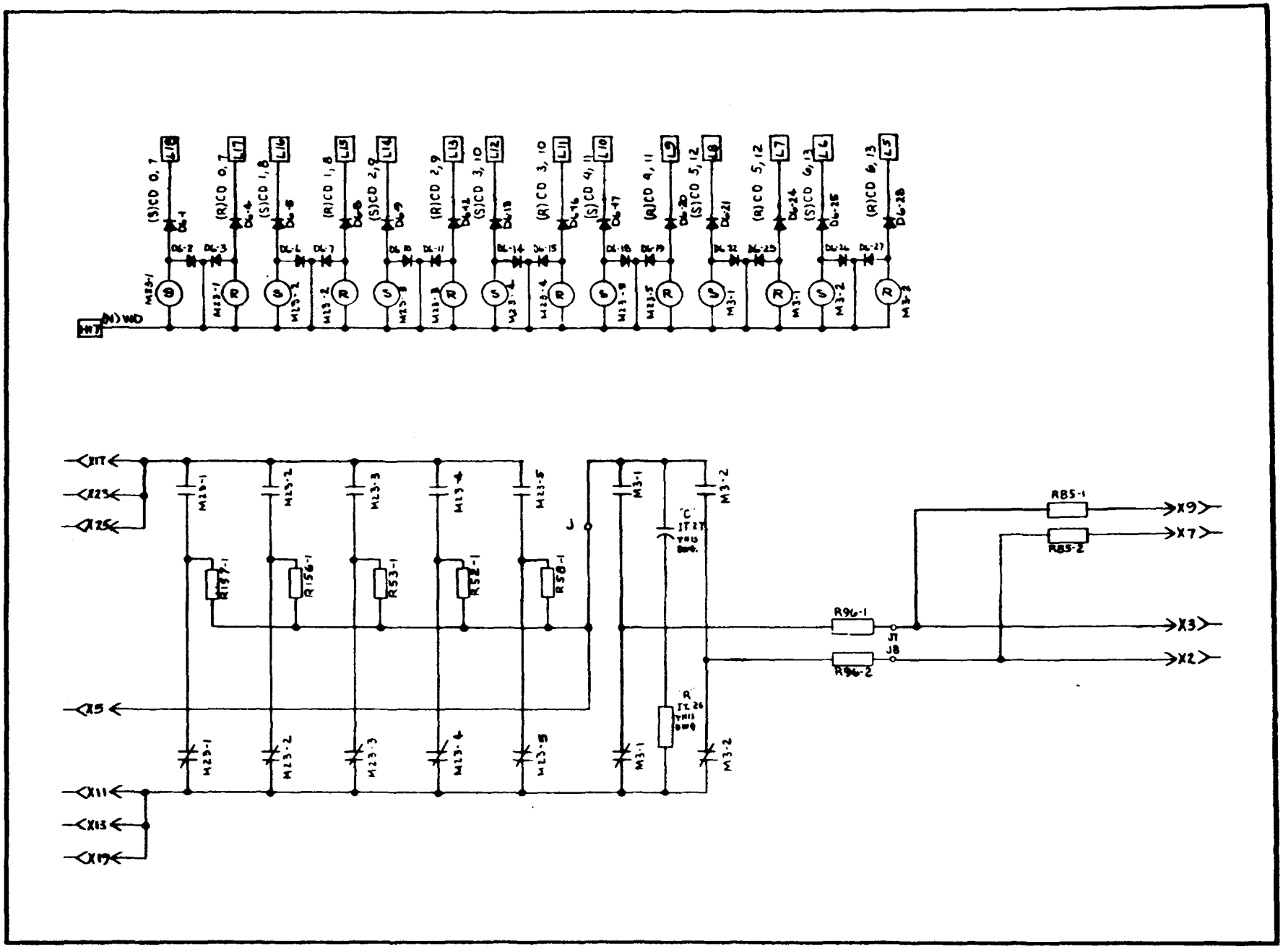


FIGURE 1A02 SCHEMATIC (REF. DWG. 845A313, SUB 3)

4A01 - HIGH SPEED ANALOG OUTPUT

GENERAL DESCRIPTION

The High Speed Analog Output subsystem is comprised of one or more 4AØ1 cards. Each card contains two analog output circuits, and can be used in slots 1 thru 14 of a D-Panel. Each card provides high speed conversion of the digital input from the computer to an analog output. An application block diagram is shown in Figure 1.

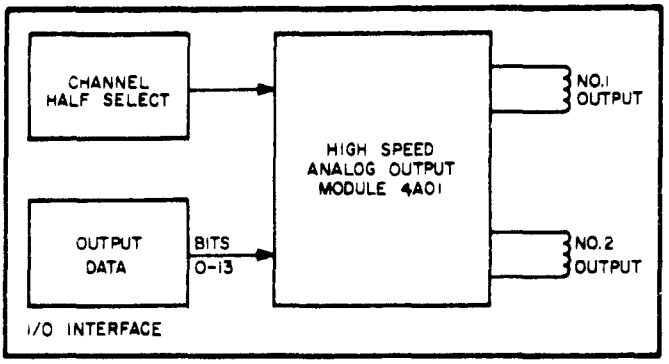


FIGURE 1. APPLICATION BLOCK DIAGRAM

SPECIFICATIONS

Input Requirements

- The half-select input, ØØ (n) Ø and ØØØ (n), requires a minimum 11.0V, 4 μsec pulse.

- The data input (OD13 etc.) require logic level signals of "zero" (1.1V max) and "one" (4.4V min).

Output Requirements

- The load resistance should be less than 20 ohms for current output.

Power Requirements

- + 27V, +10% - 15%, 230 mA
- + 10V, ±0.01%, 30 mA
- - 15V, ±0.01%, 80 mA

Output Range

- -10 to 0 to + 9.844mA, using 6 bits for magnitude (64 steps) and 1 bit for polarity (bit 13 for AØ No. 1, and bit 6 for AØ No 2).

Addressing

- The program would address the cards using the normal direct channel output instruction.

Accuracy

- 0.78% of full scale.

Speed

The time constant of the output amplifier is 50 μsec. The response is 50 μsec + time delay due to programming.

CARD EDGE MNEMONIC BREAKDOWN

Mnemonic	35 Pin ELCO
Control Winding (Pos) of Magnetic Amplifier No. 1	X1
Control Winding (Neg) of Magnetic Amplifier No. 1	X2
Feedback (Connect to X1)	X5
Test Point	X6
Ground	X10
+10V Return	X12
-15V Return	X14
+10V	X16
Control Winding (Neg) of Magnetic Amplifier No. 2	X21
-15V	X24
Test Point	X33
Feedback (Connect to X35)	X34
Control Winding (Pos) of Magnetic Amplifier No. 2	X35

CIRCUIT DESCRIPTION

Each analog output card has two output circuits; where bits 0-6 provide one analog signal (AØ No. 2), and bits 7-13 provide another analog signal (AØ No. 1). The digital-to-analog conversion for one circuit is as follows

Digital Input	Analog Output (mA)
1000000	-10
1010000	-7.5
1100000	-5.0
1110000	-2.5
0000000	0
0010000	+2.5
0100000	+5.0
0110000	+7.5
0111111	+9.844

(bit 13 or bit 6) (bit 7 or bit 0)

The entire output characteristic curve is shown in Figure 2.

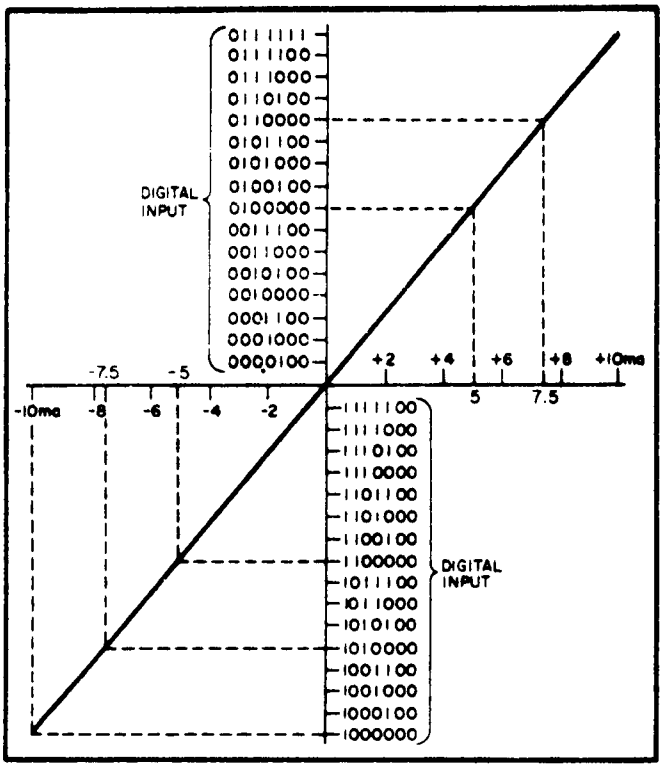


FIGURE 2. OUTPUT CHARACTERISTIC CURVE

Each of the two output circuits can be separated into functional elements as shown in Figure 3

Register Circuit

In the register circuitry (see Fig. 4) a logical "one" is defined as 14.3V and a logical "zero" is +7.5V. Under normal steady-state conditions, no voltages are included in the transformers and signals $\overline{D0}$, $\overline{D1}$, and $\overline{SAMPLE}$ are logical "one's". The NAND flip-flops may be in any state.

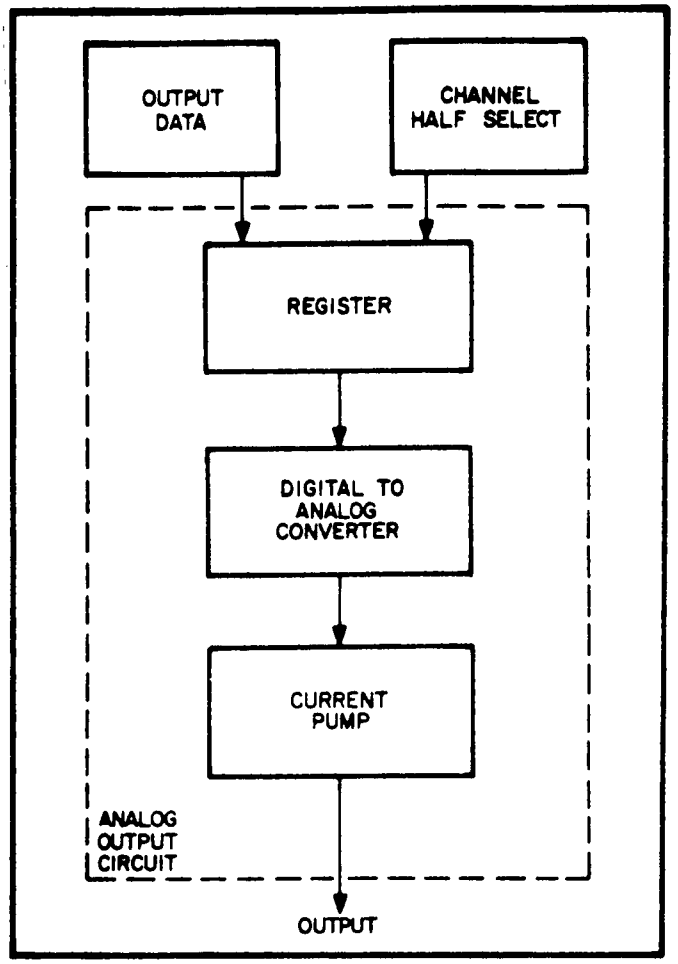


FIGURE 3. OUTPUT CIRCUIT FUNCTIONAL DIAGRAM

When a 4 μsec half-select pulse is applied to terminal L2, transformer X15 is pulsed and capacitor C20 begins charging, thus saturating transistor Q (in a NAND) for the first part (nominal ½) of the 4 μsec. This grounds signal $\overline{SAMPLE}$, tending to turn all the flip-flops off ($\overline{B0}$ and $\overline{B1}$ go to "one's"). Meanwhile, transformers X1 and X2 are being pulsed. If data line ØD00 has a zero on it, winding 1-2 will be shorted and signal $\overline{D0}$ will not deviate far from +14.3V, remaining a logical "one". Therefore, $\overline{SAMPLE}$ going to +7.5V will determine the final state of the flip-flop (0).

If, however, data line OD00 has a "one" on it during the 4 μsec half-select time, a voltage will be induced in winding 5-6 causing signal $\overline{D0}$ to be driven in a negative direction until diode D1-15 conducts, clamping $\overline{D0}$ 1 diode drop below +7.5V, which is a logical "zero". Flip-flop output B0 is at a "one" as well as $\overline{B0}$. However, signal $\overline{SAMPLE}$ will return to a "one" sooner than $\overline{D0}$ (since X15 is capacitively coupled to Q) allowing

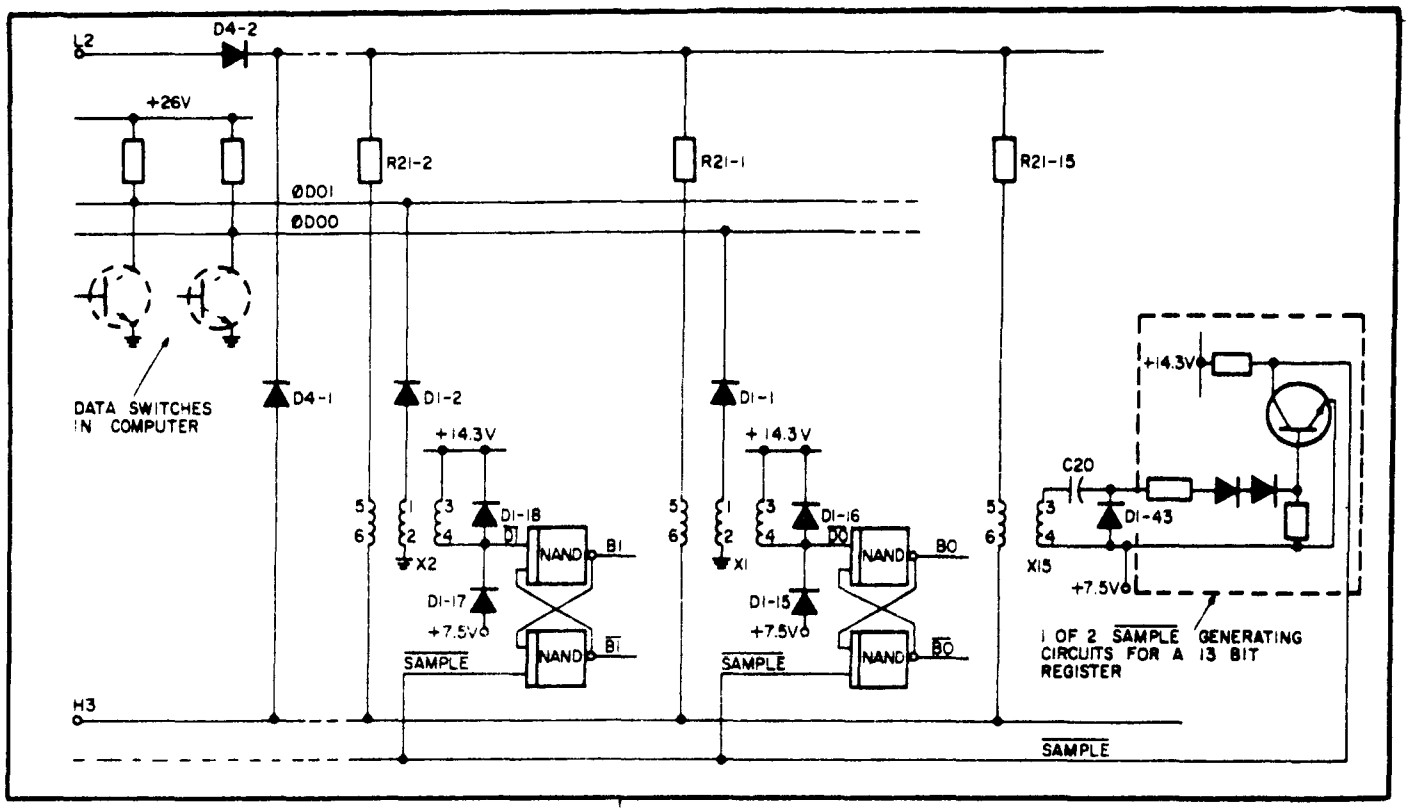


FIGURE 4. REGISTER CIRCUIT

$\overline{B0}$ to go to zero and leaving the flip-flop in the "one" state. The basic criteria is that $\overline{SAMPLE}$ must go to zero long enough to switch the flip-flop off and the $\overline{D}$ signals, if they switch, must remain at zero long enough after $\overline{SAMPLE}$ returns to a "one" to insure the flip-flop staying on.

Digital-to-Analog Converter Circuit

Each digital-to-analog converter (W5) contains:

- one 4-bit buffer amplifier
- one 4-bit ladder switch
- one 4-bit ladder network

The buffer amplifier network, shown in Figure 5, contains four, isolated PNP inverter stages which operate from common emitter and collector supply voltages. When used with a positive emitter supply, it can drive both plus and minus current to a ladder switch network.

Ladder Switch Network

The ladder switch network, shown in Figure 6, consists of four, double-throw analog switches. It is intended to drive the digital-to-analog resistor network. The inputs of the ladder network switch either to +10V or to ground. It is designed to be driven from a plus and minus signal input such as the buffer amplifier.

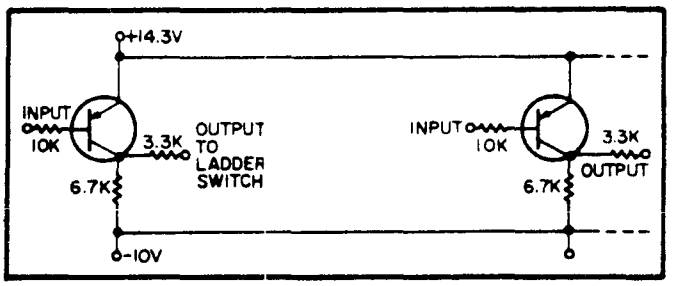


FIGURE 5. BUFFER AMPLIFIER NETWORK

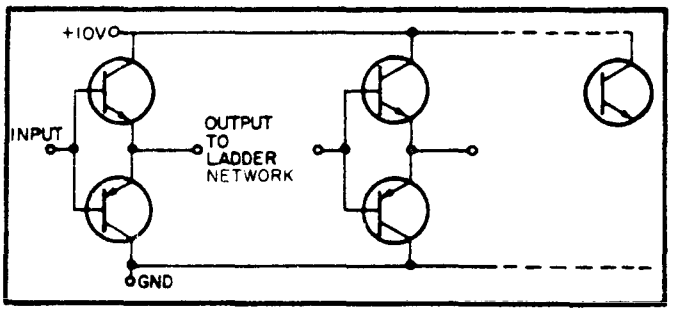


FIGURE 6. LADDER SWITCH NETWORK

4-Bit Ladder Network

The ladder network, shown in Figure 7, is a precision resistor network intended for digital-to-analog conversion. Inputs A, B, C and D are connected to the ladder switch which is switching either to +10V or to ground. The open circuit output voltage is 1/2 the voltage at input A, plus 1/4 the voltage at B, plus 1/8 the voltage at C, and so forth. Thus, the resulting open circuit output voltage is a properly weighted sum of the individual binary bits.

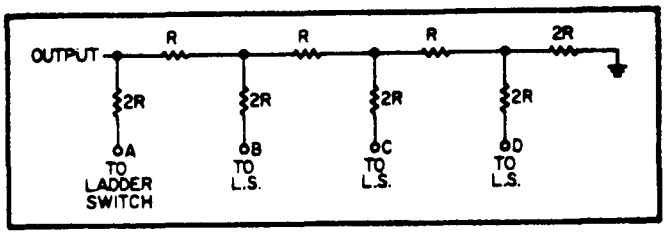


FIGURE 7. LADDER NETWORK

Current Pump

The current pump, shown in Figure 8. consists of an operational amplifier, a current booster circuit (B), and three resistors. It is designed to operate as follows:

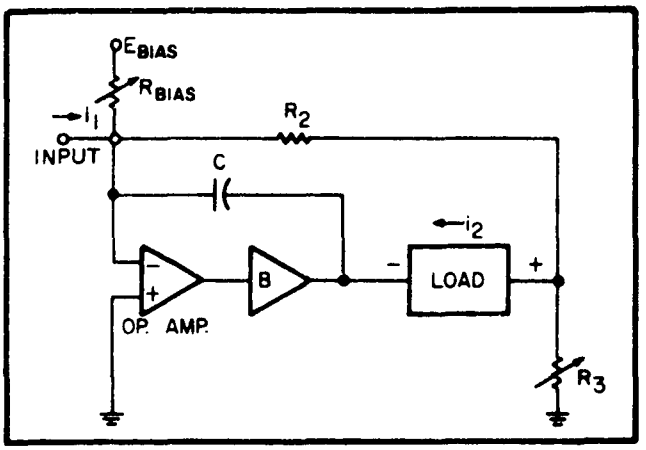


FIGURE 8. CURRENT PUMP DIAGRAM

when $i_1 = 0$,
$i_2 = -10\,mA$:

when $i_1 = 200\,\mu A$,
$i_2 = 0$:

when $i_1 = 400\,\mu A$,
$i_2 = +10\,mA$

R_{bias} can be adjusted for zero offset so that when $i_1 = 200\,\mu A$, $i_2 = 0$. R_3 can be adjusted for full scale so that when $i_1 = 0$, $i_2 = -10\,mA$.

A curve showing the complete input/output current relationship of the current pump is shown in Figure 9.

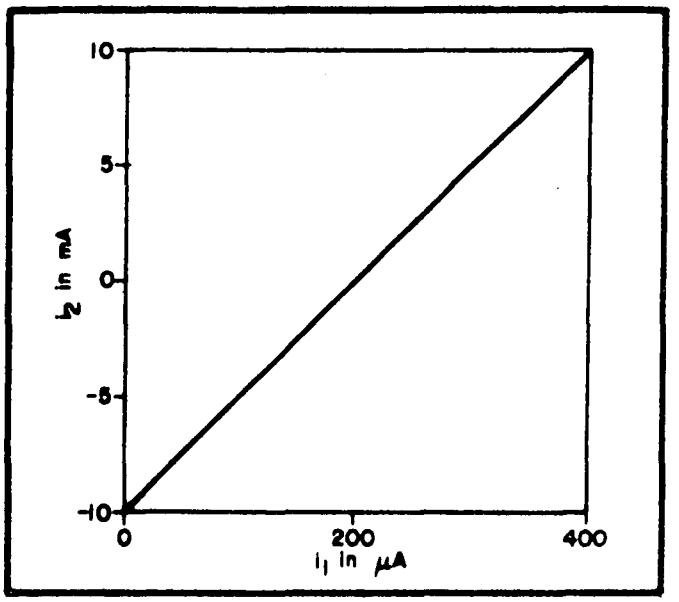


FIGURE 9. CURRENT PUMP INPUT/OUTPUT CURVE

* * *

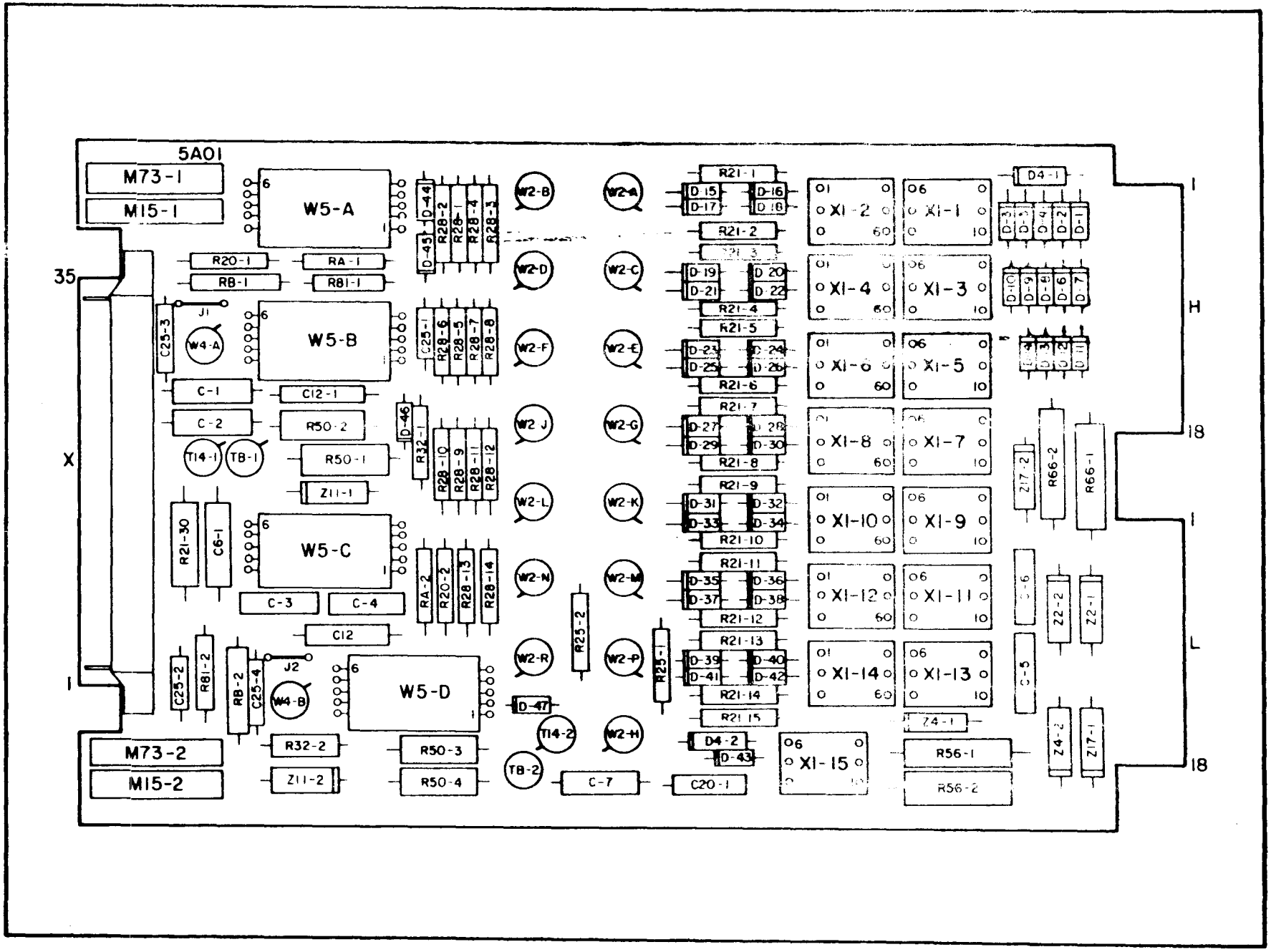
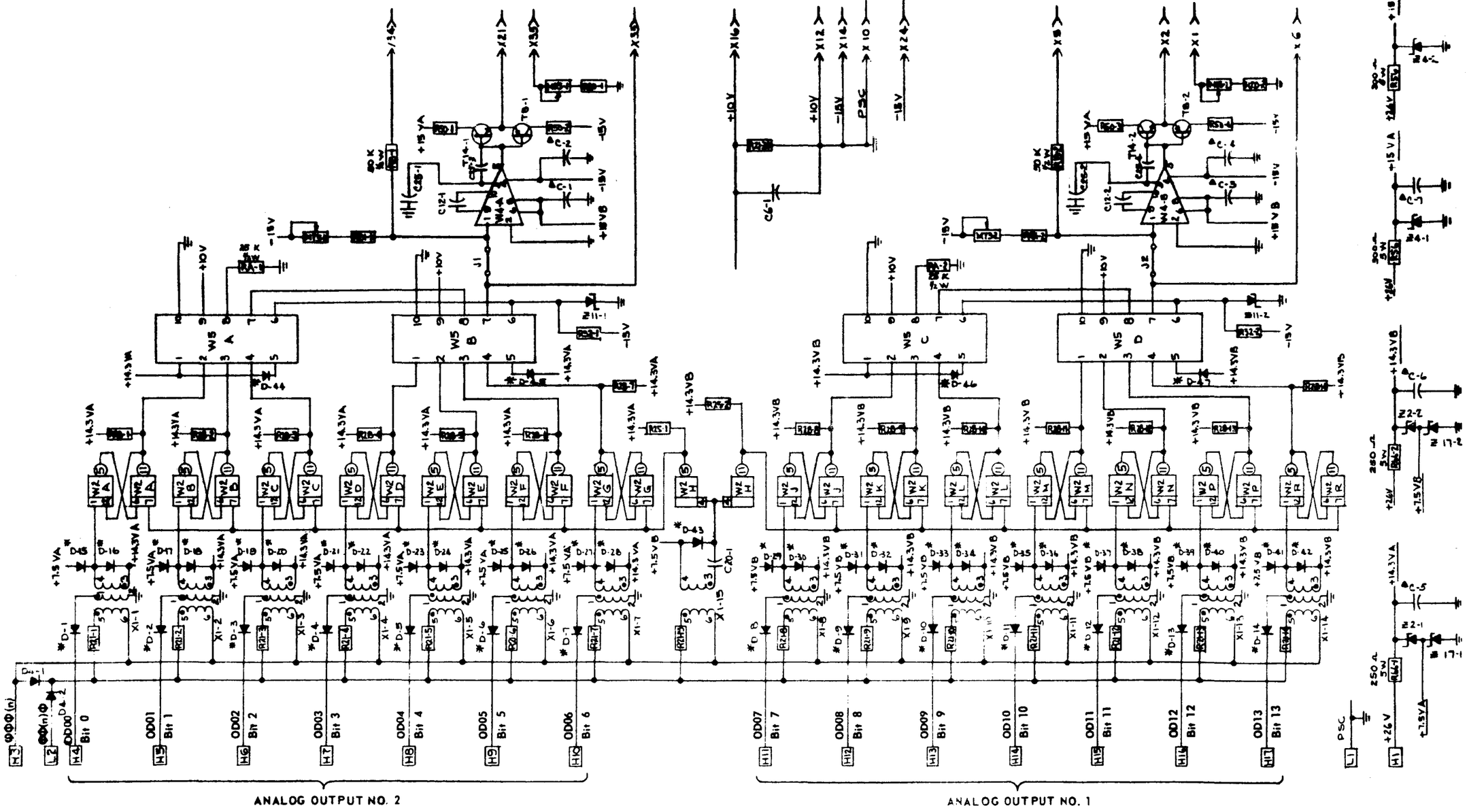


FIGURE 10. 4A01 ASSEMBLY (REF. DWG. 845A338, SUB 2)



NOTES.

1. W2-A,B,C,D,E,F,G - PIN 10 TO +7.5VA — W2-H,J,K,L,M,N,P,R PIN 10 TO +7.5VB
2. W2-A,B,C,D,E,F,G - PIN 6 TO +14.3VA
3. W2-H,J,K,L,M,N,P,R - PIN 6 TO +14.3VB
4. * D-1 THRU D-7 ARE ITEM 19 OF DWG 845A838 (W4-X)
5. ▲ C-1 THRU C-7 ARE ITEM 18 OF DWG 845A838 (W4-X)
6. W4 - REF DWG 669A300
7. W5 - REF DWG. 669A301
8. W2 - REF DWG. 774A992

FIGURE 11. 4A01 SCHEMATIC (REF. DWG. 397D504 SUB 2)

4AP1/4AP2 - ANALOG POINT SELECTION MODULE

GENERAL DESCRIPTION

The Analog Point selection module contains 14 identical relay circuits and one bus-guard relay circuit which are used to connect a selected analog input point to the voltage-to-frequency converter. The 4AP2 card differs from 4AP1 card by having a high output impedance voltage source connected across the PLUS and MINUS busses used for open input circuit detection. An application block diagram of the Analog Point selection card is shown in Figure 1.

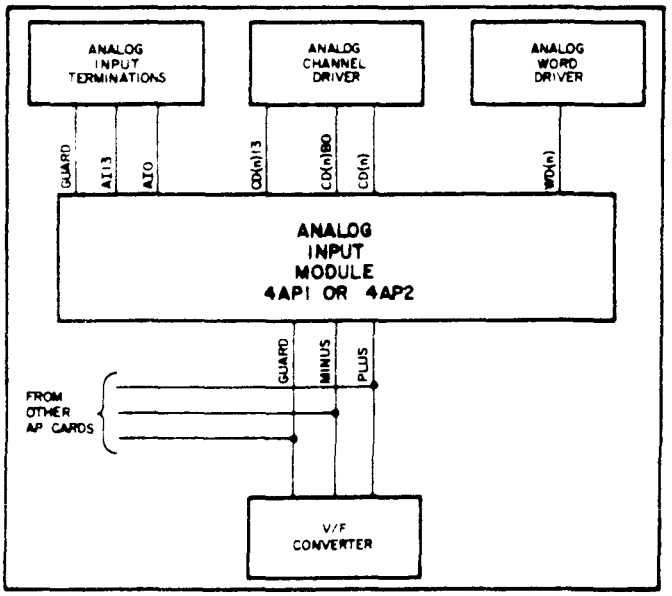


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The word driver input WD (n) requires a conducting path to the + 10 V power supply if the word is selected.

The channel driver input CD (n) requires a conducting path to PSC if the channel is selected, otherwise it is + 26 V.

The channel driver bit inputs, CD (n) bits 0 through 13, require a conducting path to PSC if a bit is selected, otherwise there are + 26 V. The analog inputs are D.C. voltages either in the 0-50 mV range or in the 0-5 V range.

The guard is to be connected to the shield of the analog input signal.

Output Requirements

The PLUS, MINUS and GUARD outputs are physically connected to the selected analog input. These are to be connected through the analog bus to the input of the voltage-to-frequency converter.

Power Requirements

For the 4AP1 module, no connection to any power supply is required. For the 4AP2 module, connections to + 26 V and PSC are required.

CIRCUIT DESCRIPTION

Figure 2 shows the bus and guard relay circuit and one of the 14 input relay circuits. The figure also shows the connections to the analog input subsystem. When word WD (n) is selected the word driver SCR is turned on and provides + 10 V to the common of the relay coils.

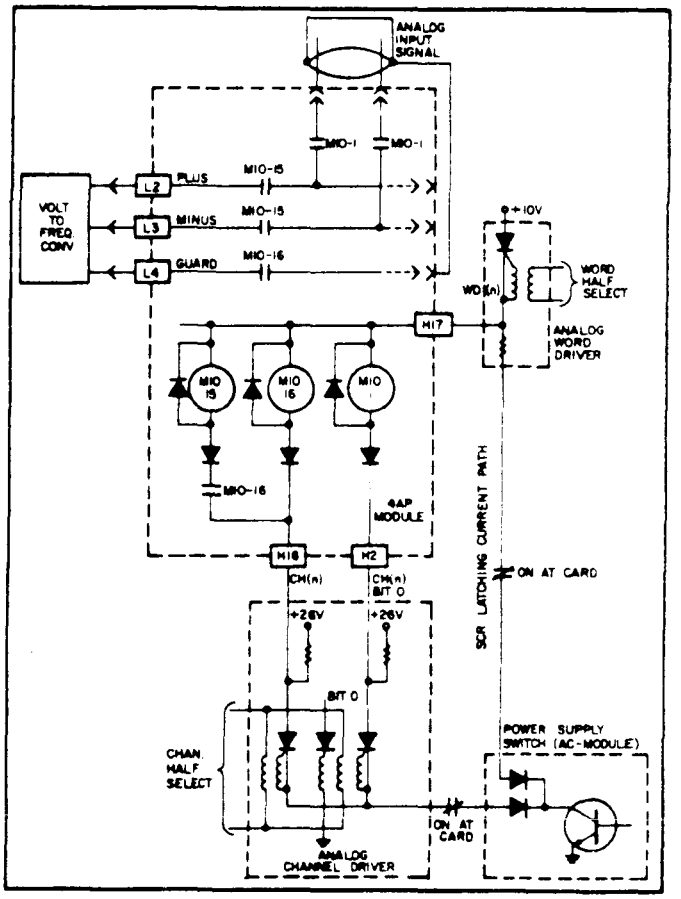


FIGURE 2. BUS, GUARD AND INPUT RELAY CIRCUIT

When channel CH (n) is selected, the channel driver SCR's are turned on (only one bit should be selected out of the 14) which now provide current to PSC through the power supply switch for the guard relay (M10-16) and one of the point relays (M10-1). The guard relay contact, after a small time delay, will then energize the bus relay (M10-15).

Since all the point relays, bus relays and guard relays are mercury-wetted contact type, the input point relay contacts and guard relay contacts will close first, then the bus relay contacts. When the power supply switch opens the SCR's cut off and the relays drop out. The time sequence of operation is shown in Figure 3.

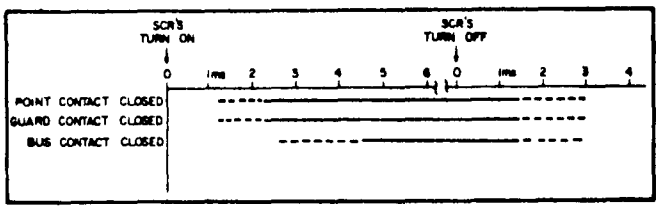


FIGURE 3. SEQUENCE OF OPERATION

The 4AP2 module contains exactly the same circuits as the 4AP1 module, except that a high output impedance voltage source is connected across the PLUS and MINUS busses. This voltage source generates a - 50 mV signal which is recognized by the computer as an open circuit indication.

The voltage source itself (ref. 4AP2 module schematic) consists of an oscillator which is energized by the + 26 Vdc supply. This oscillator is transformer coupled to a rectifier circuit, which is producing the required 50 mVdc signal.

* * *

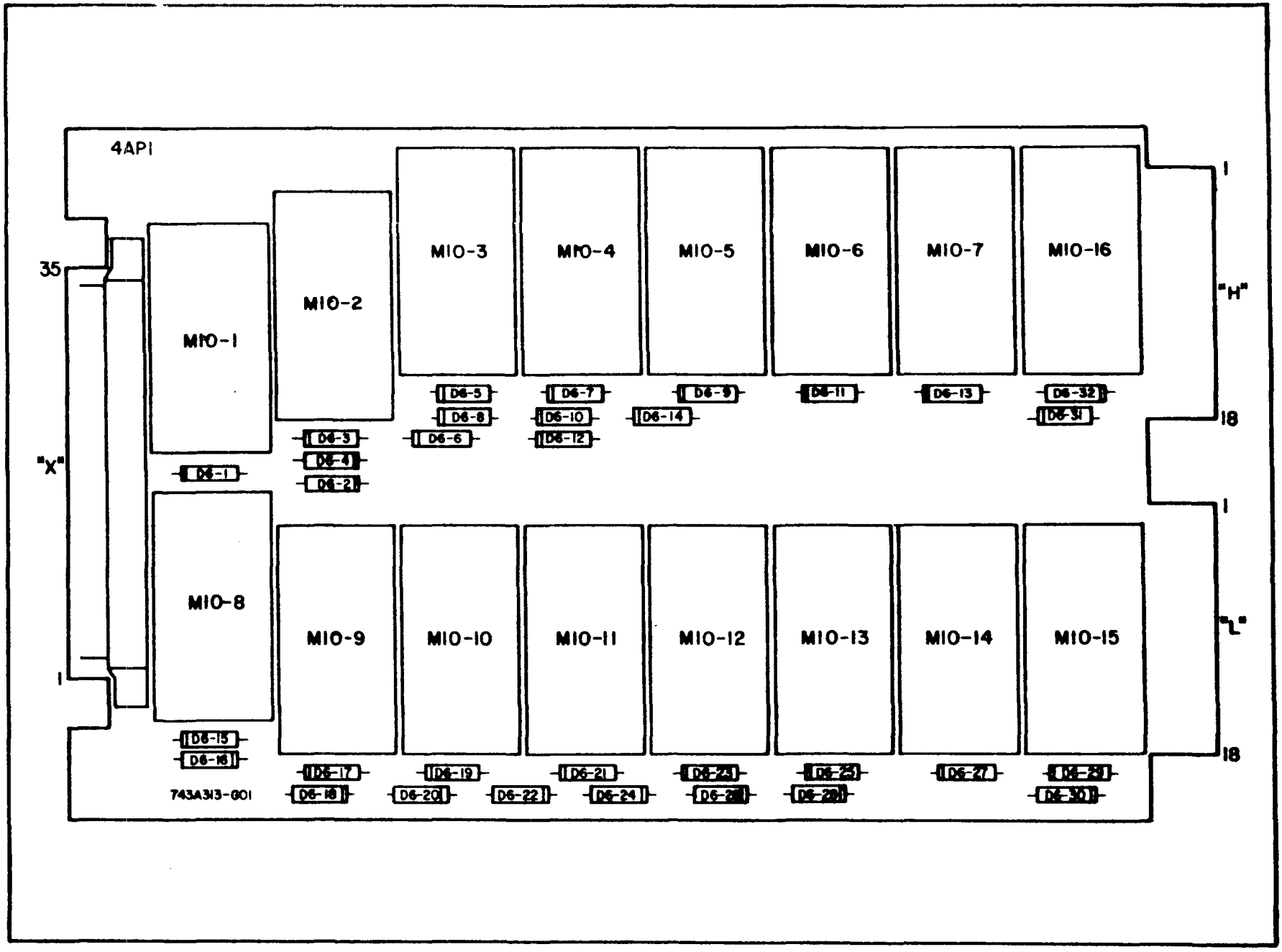


FIGURE 4. 4AP1 ASSEMBLY (REF. DWG. 743A313, SUB 2)

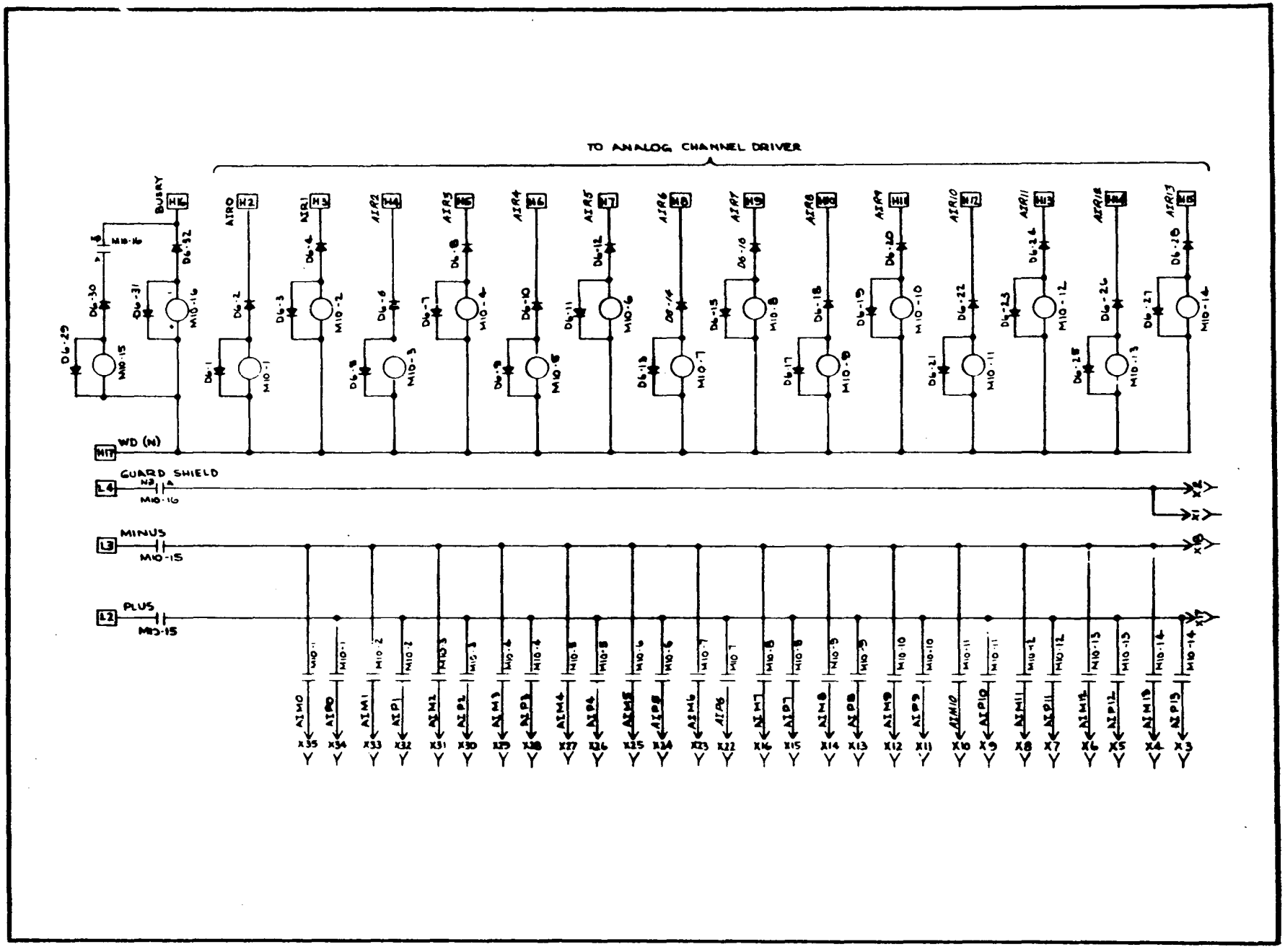


FIGURE 5. 4AP1 SCHEMATIC (REF. DWG. 743A313, SUB 2)

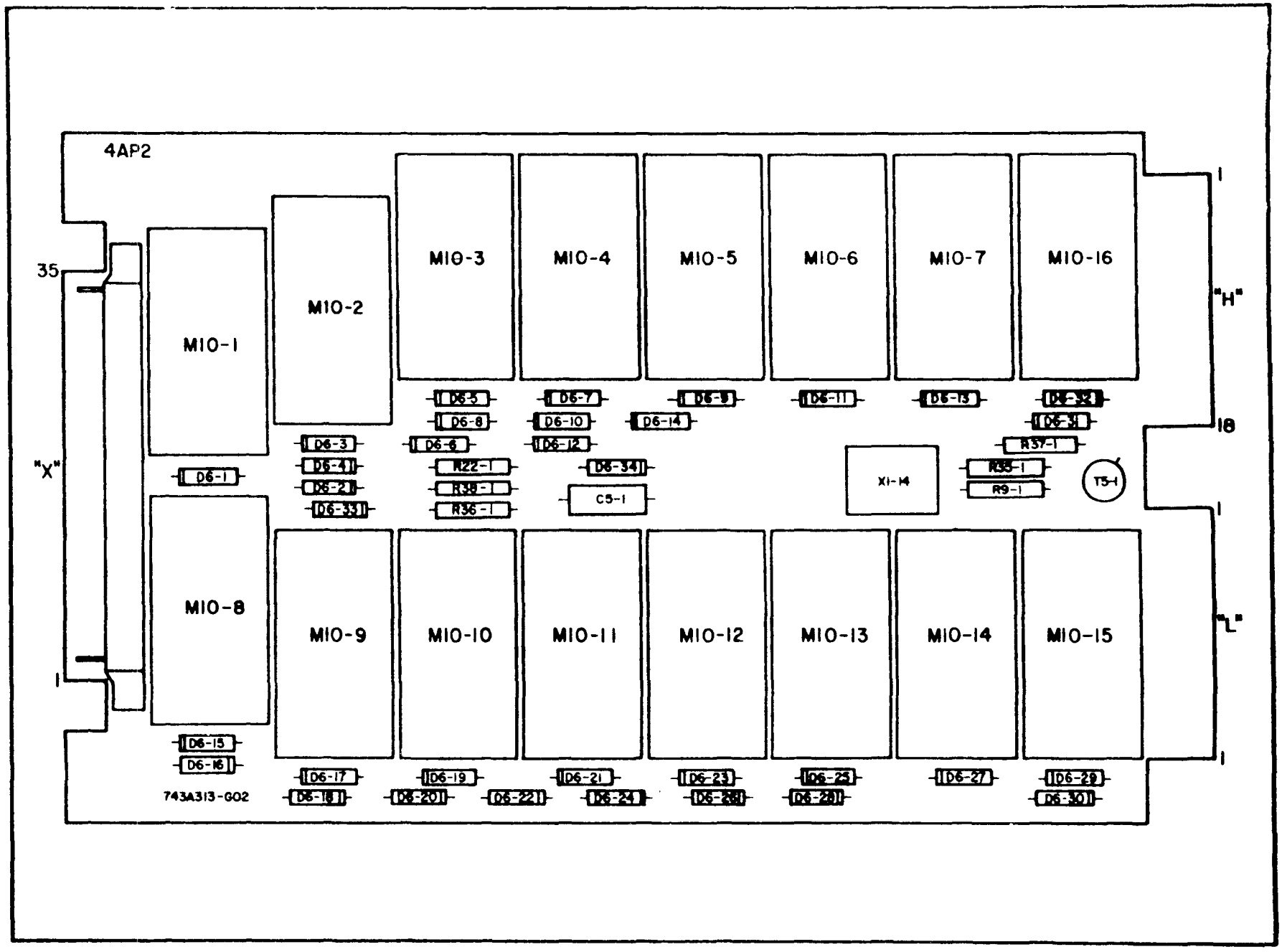


FIGURE 6. 4AP2 ASSEMBLY (REF. DWG. 743A313, SUB 2)

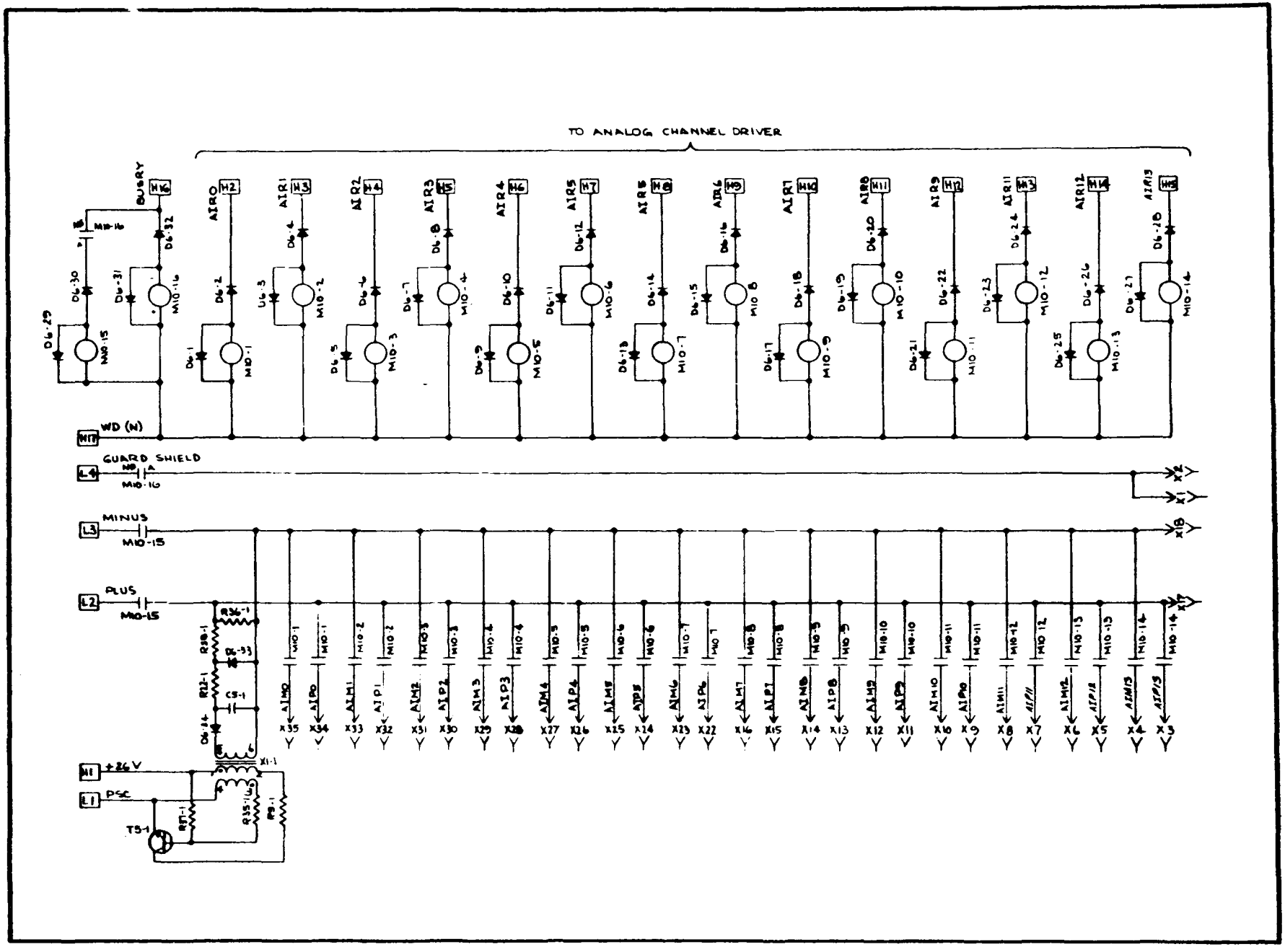


FIGURE 7. 4AP2 SCHEMATIC (REF. DWG. 743A313, SUB 2)

2AT3/2AT1/1SR1 - WORD AND CHANNEL TRAP

GENERAL DESCRIPTION

The basic principle of operation is to sense (as an analog voltage) the state of each word and channel driver. It is expected that one (or less) channel driver and one (or less) word driver per V/F converter, will be conducting at any time. Thus, five detector circuits measure the analog summation of voltages produced by these drivers. Should the expected summations be exceeded, multiplexer disabling and fault interrupt results.

CIRCUIT DESCRIPTION

The only difference between the 2AT3 and 2AT1 is the value of resistors R26-3 and R53-2. However, circuit operation is identical. Resistor-diode summing circuits (1SR1 card) are provided for connection to the respective driver SCR's. This configuration is shown in Figure 1.

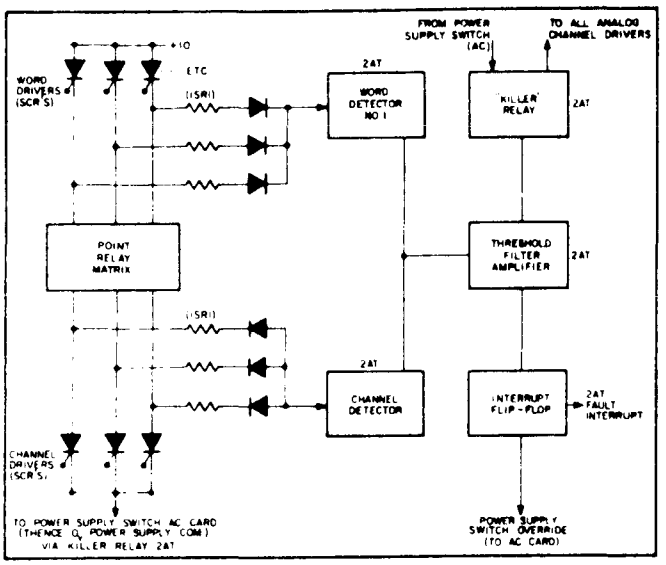


FIGURE 1. WORD AND CHANNEL TRAP CONFIGURATION

The detectors (on 2AT3) monitor current provided by the summing resistor networks, that causes a reaction when any of the five possible currents (channel, word group #1, word group #2, word group #3, or word group #4) exceed a level greater than was expected to be produced by a single conductive SCR. The detectors are emitter-coupled differential amplifiers with paralleled outputs.

Noise rejection is aided by, a zener diode threshold followed by a filter and a common emitter switch amplifier, which further processes and amplifies the detector output signal. This circuit then drives an SCR relay puller that forms a sort of last line of defense by the "KILLER RELAY" which physically interrupts the matrix input current by opening series, normally-closed contacts upon failure detection. Reset of this circuit can occur only upon manual removal of either the 2AT3 card or the AC card, or upon normal power supply switch operation on the AC card.

Normally, failure detection causes a mono-stable multivibrator (on 2AT3) to trip, causing a fault interrupt signal to be initiated and simultaneously generate the power supply switch override signal to the analog control (AC) module. For nominal AC card behavior this signal will disable the power supply switch, again cancelling existing word and channel driver activity.

Since this action is faster than either the point relays or the "KILLER RELAY", all relays are prevented from picking up. However, if the power supply switch is not nominal, the "KILLER RELAY" will operate as described previously.

The estimated maximum tolerable time from trip until Fault Interrupt action (i.e., setting of the corresponding ckt. core) is approximately 1/2 ms.

NOTE

No contact protection is provided for the "KILLER RELAY" and for that reason, because point relay damage may have been sustained whenever the fault was cleared solely by "KILLER RELAY" operation, it is recommended that these contacts be carefully inspected prior to restarting under such conditions. This will be recognized as a complete disabling of the analog multiplexer with the "KILLER RELAY" continuously picked-up.

The effect of either of the modes of failure behavior discussed previously is, unfortunately, related closely to the type of failure and when it occurred in the cycle. It is doubtful if this failure can be adequately predicted. Accordingly, the analog input programs should expect, upon receiving an analog Fault Interrupt, that the previous converted input quantities are suspect, as are subsequent quantities. It is possible for more than one seemingly valid analog completion interrupt to occur incorrectly. It is at this point that the programs should abort current scan operation and, after a delay of more than 35 ms, scanning can be reinitialized.

* * *

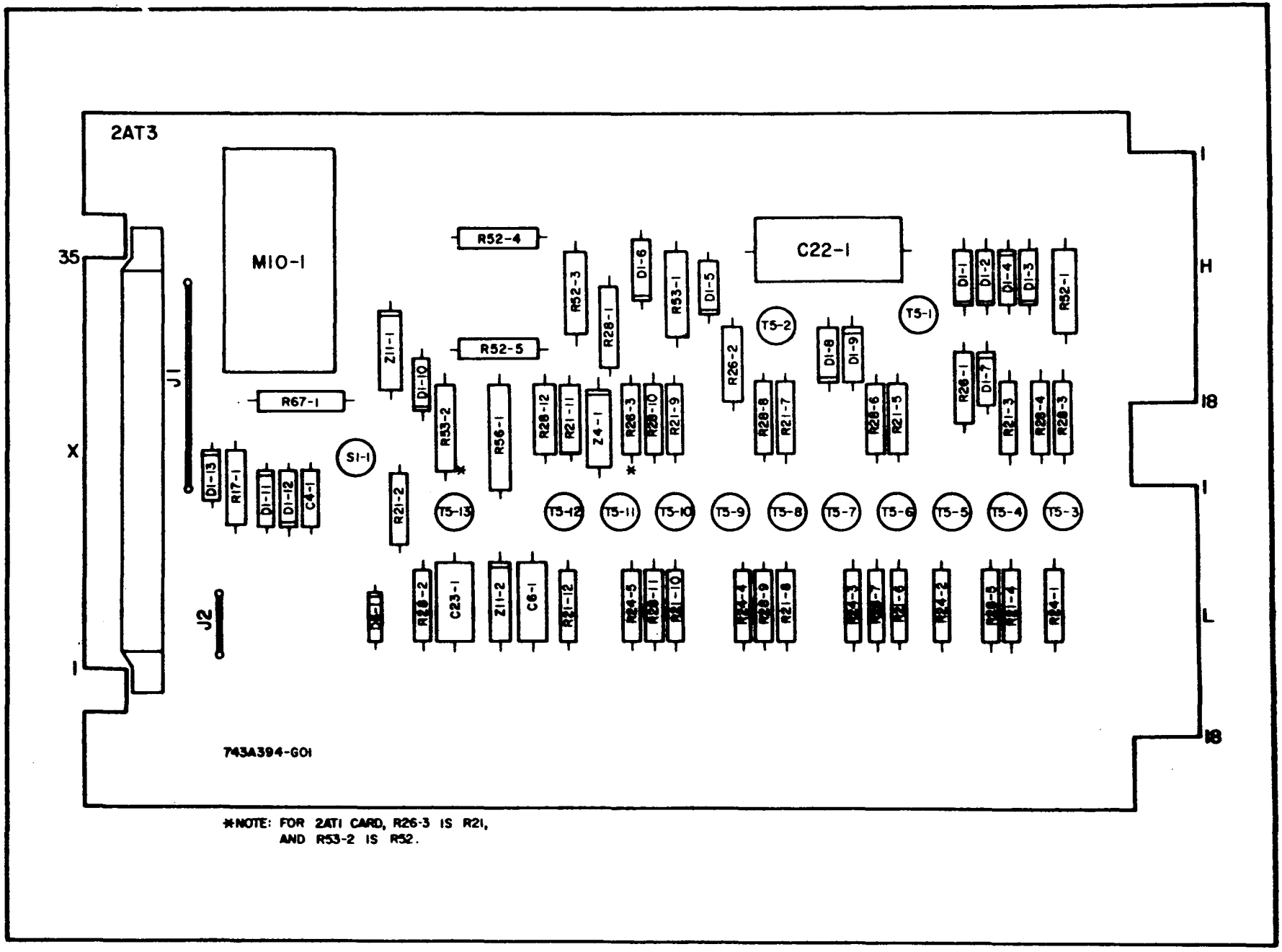


FIGURE 2. 2AT3/2AT1 ASSEMBLY (REF. DWG. 743A394, SUB 6)

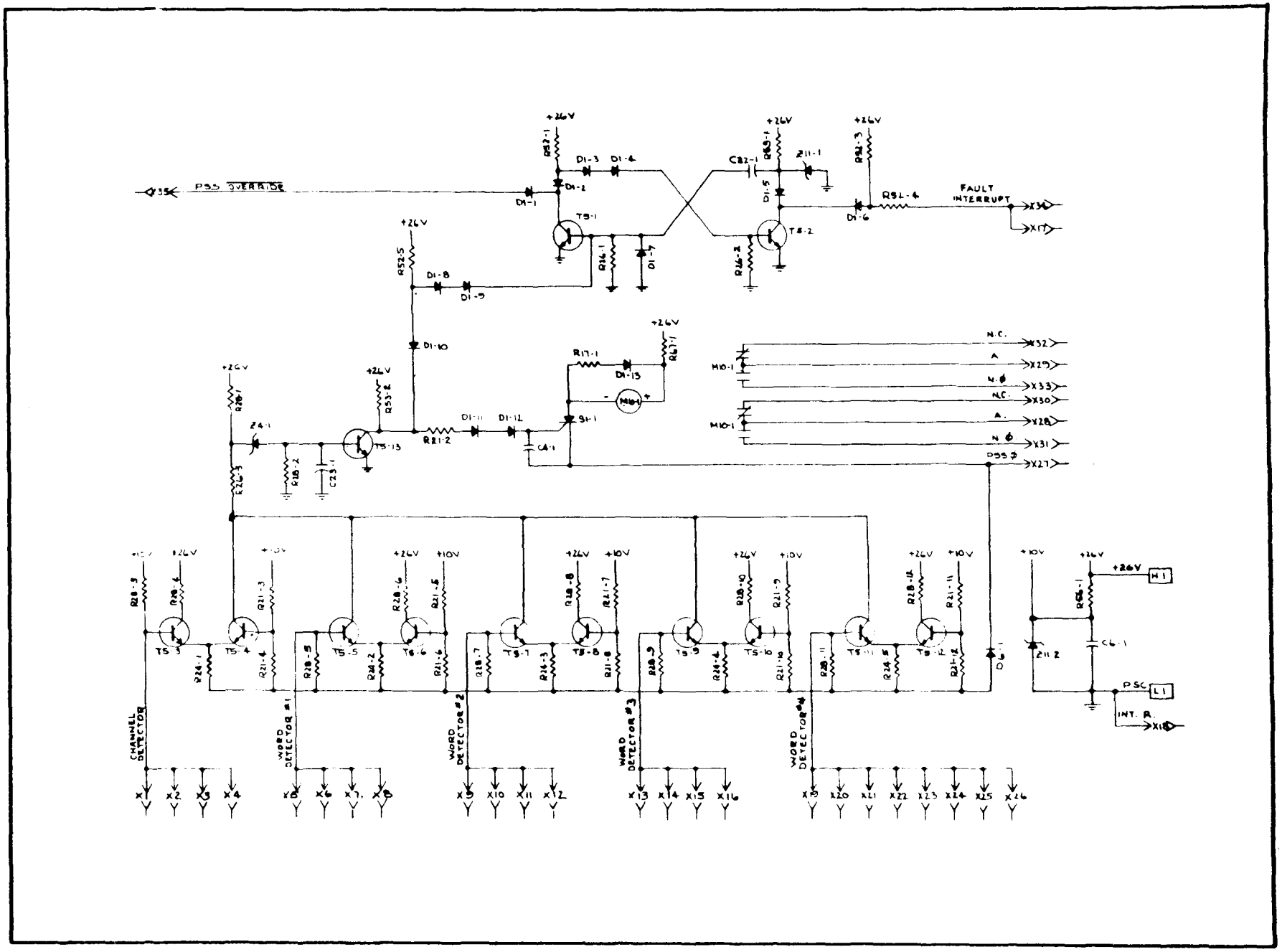


FIGURE 3. 2AT3/2AT1 SCHEMATIC (REF. DWG. 743A394, SUB 6)

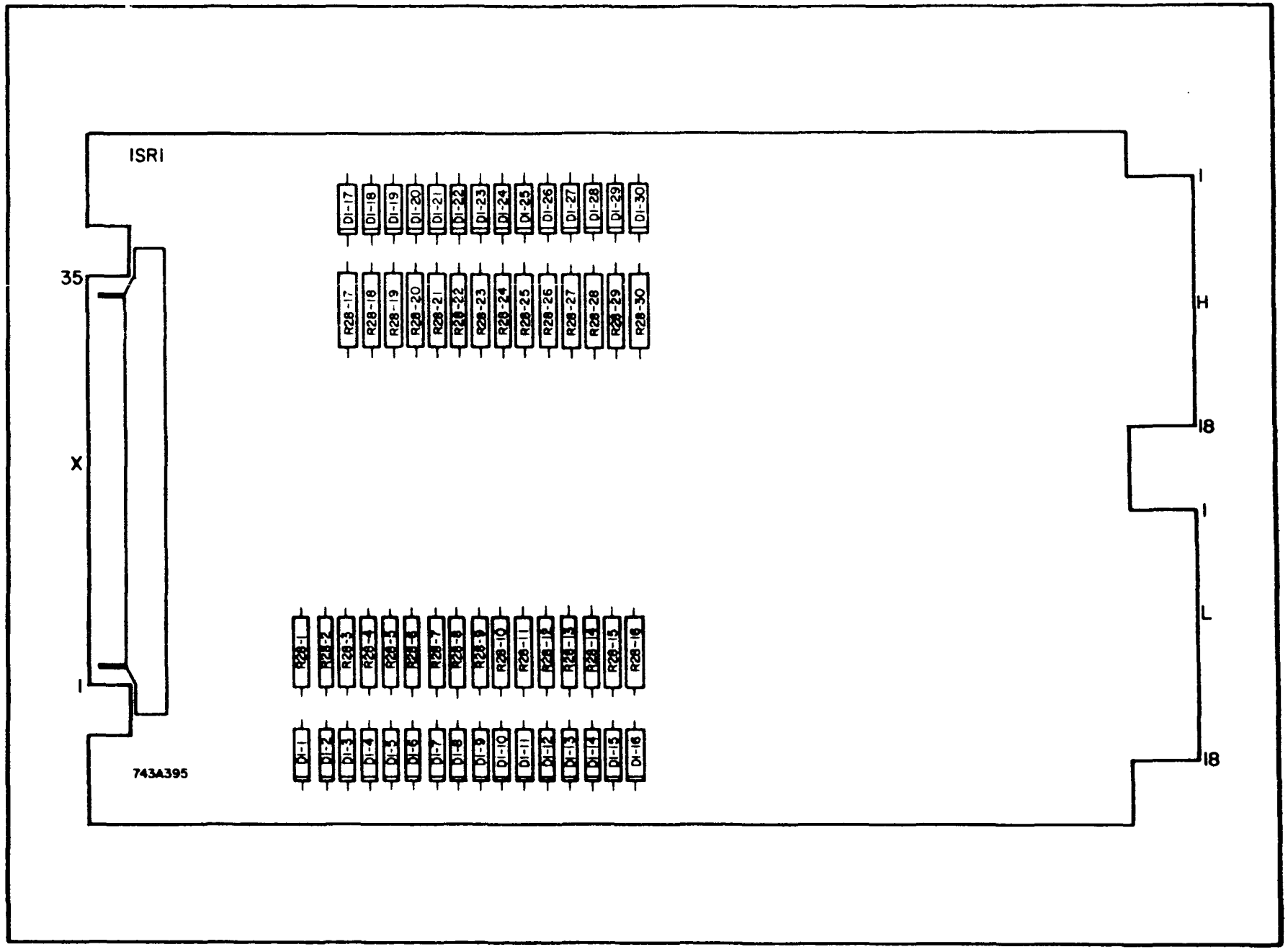


FIGURE 4. 1SR1 ASSEMBLY (REF. DWG. 743A395, SUB 1)

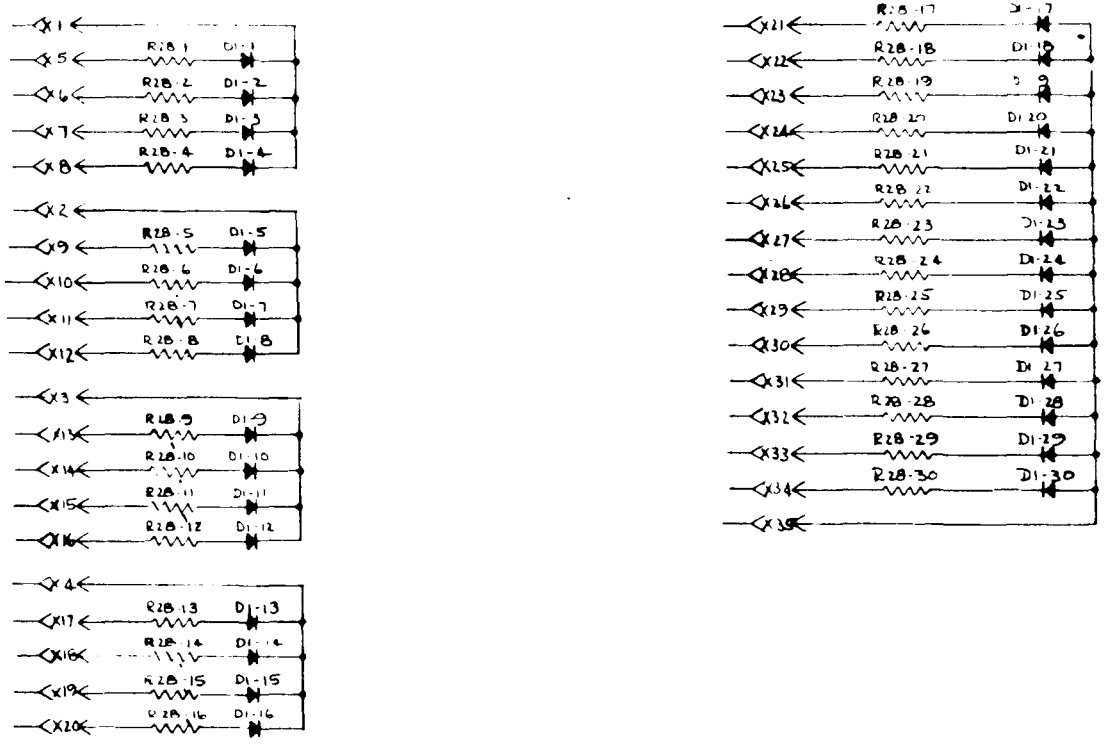
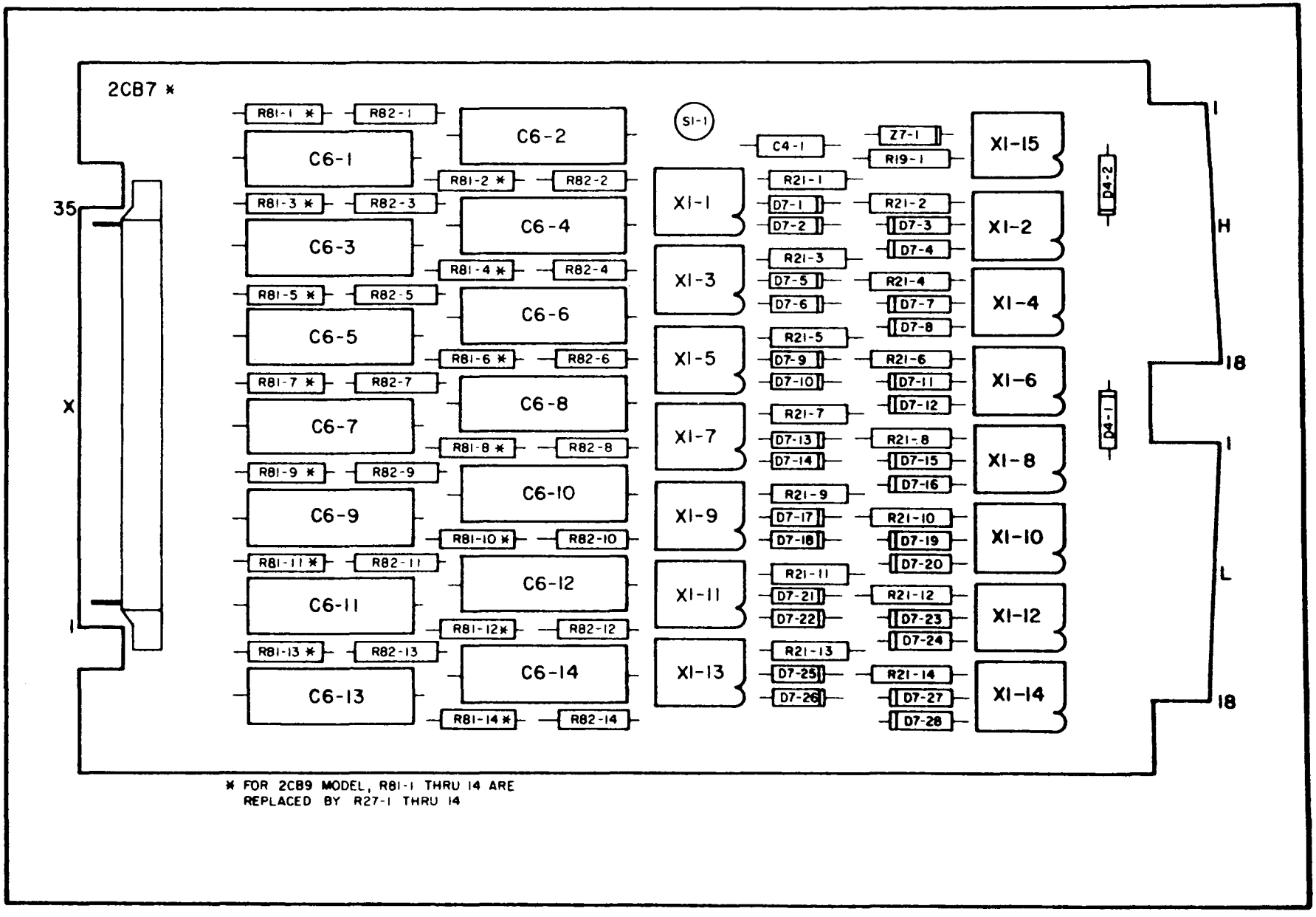


FIGURE 5. 1SR1 SCHEMATIC (REF. DWG. 743A395, SUB 1)



* FOR 2CB9 MODEL, R81-1 THRU 14 ARE REPLACED BY R27-1 THRU 14

FIGURE 9. 2CB7/2CB9 ASSEMBLY (REF. DWG. 743A356, SUB 10)

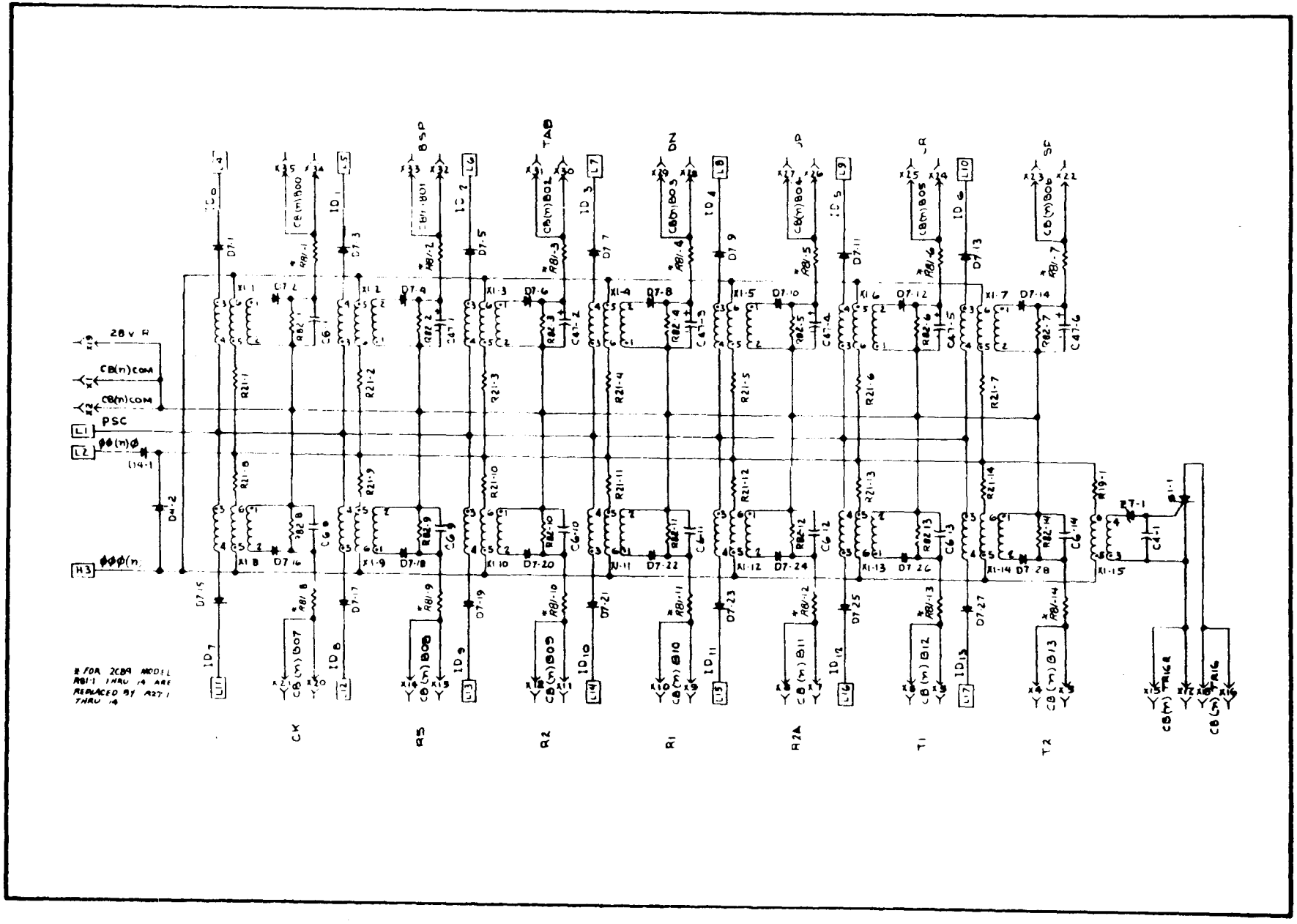


FIGURE 10. 2CB7/2CB9 SCHEMATIC (REF. DWG. 743A356, SUB 10)

CONTACT INPUT BUFFER MODULES

2CB4
2CB5
2CB6
2CB7
2CB8

A. General Description

The module is used to input 14 bits of data from contacts or switches to the I/O interface. The module contains 14 identical transformer isolation circuits and a common trigger output circuit.

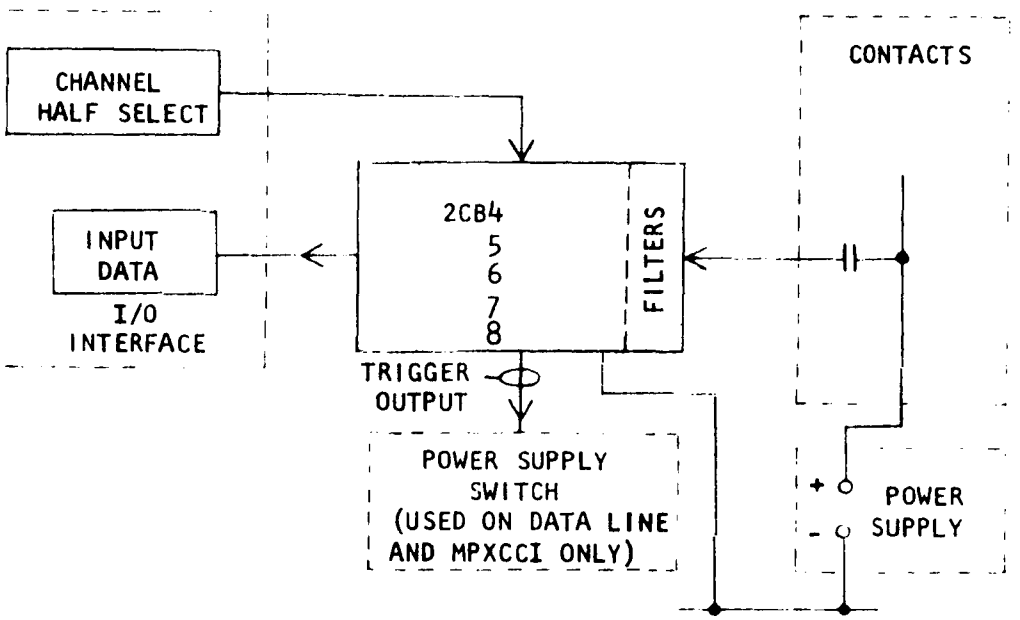


Figure 1

The module type suffix denotes various input filter options to accommodate standard power supply voltages and switching arrangements.

2CB4	48 Volt, standard filter
2CB5	26 Volt, non-filtered
2CB6	125 Volt, standard filter
2CB7	48 Volt, low energy filter
2CB8	26 Volt, data link filter

B. Circuit Specifications

1. Input Requirements

a. Inputs from contacts or switches

The inputs to the module from the contacts or switches are either a d.c. voltage level or zero volts. The presence of the voltage produces a "one" input to the input interface while zero volts produces a "zero" input to the input interface.

The nominal magnitude of the input voltage level at the module and the inrush resistance of each bit of the modules are:

Module Type	Nominal Voltage	Inrush resistance/bit
2CB4	48	13K
2CB5	26	
2CB6	125	43K
2CB7	48	65K
2CB8	26	511

b. Inputs from Channel Half Selects

The half select winding (Row HS and Col HS) require a minimum 11 volt, 4 microsecond pulse.

2. Output

a. Output to I/O interface (input data)

The data output is a minimum 6 volt, 4 microsecond pulse to the I/O interface.

b. Output to power supply switch trigger

The output is clamped at approximately at a one volt level until the power supply switch is reset.

3. Power

The only power connection required by this card is the negative side of the 48 or 125 volt power supply.

C. Circuit Description

1. Data (2CB4, 2CB6 and 2CB7 modules)

Figure 2 illustrates one bit of the 14 bit data buffer register.

Transformer:

Winding 5-6 is primary, N turns
Winding 3-4 is secondary, N turns
Winding 1-2 is tertiary, 2N turns

Filter

Type	RA	RB	CA
2CB4	13K	5K	.5 mfd
2CB6	43K	5K	.5 mfd
2CB7	65K	25K	.1 mfd

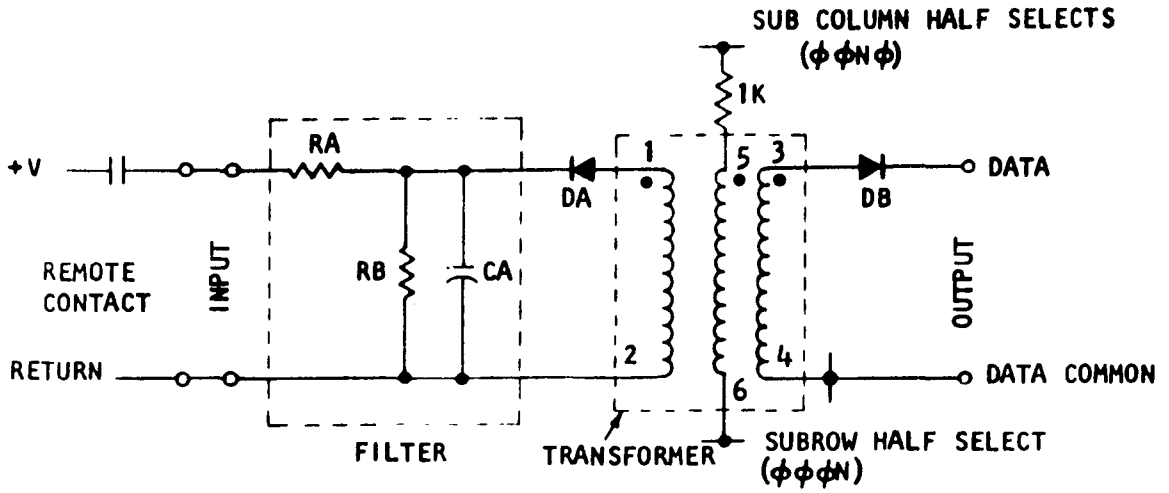


Figure 2

When the remote contact closes, a voltage across capacitor CA will build up as determined by the component values of RA, RB, CA. When the remote contact opens, the voltage across capacitor CA will decay as determined by the component values of RB and CA.

When the channel half select circuits are energized, the transformer primary winding and series 1K resistor will have an applied pulse of about 4 microseconds duration and 12 volts magnitude. The energy available from the primary winding will be "auctioneered" to either the secondary or tertiary windings, depending upon their relative impedances. If the capacitor CA is charged, the tertiary winding appears as a high impedance and most of the pulse energy is available at the secondary winding to supply an output pulse. When the capacitor CA is discharged and acts like a short circuit across the tertiary winding, the pulse energy will be transferred to the tertiary winding and absorbed in charging the capacitor. There will now be sufficient voltage across the secondary winding to produce a "one" signal to the pulse output circuit. The 1K resistor in series with the primary winding provides current limiting. The diode DB prevents a negative pulse output on inductive flyback.

2. Data (2CB5 Module)

Figure 3 illustrates the input portion of one bit of the 14 bit data buffer register. The transformer primary and secondary circuits are the same as shown in Figure 2.

The operation is similar to that described for the 2CB4, 2CB6 and 2CB7 modules except that the impedance on the tertiary winding is dependent upon the state of SCR. When the SCR is blocked, diode DA is reversed biased, the tertiary winding appears as a high impedance, and an output pulse is generated. If the SCR is conducting, the tertiary winding is essentially shorted and no output pulse is generated.

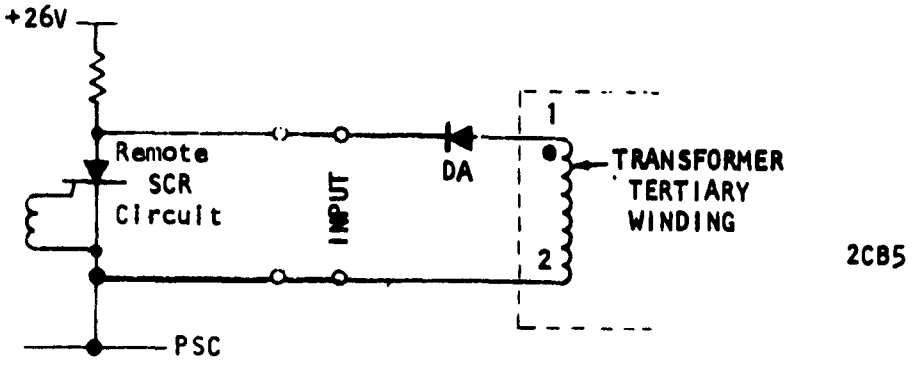


Figure 3

3. Data (2CB8 Module)

Figure 4 illustrates the input portion of one bit of the 14 bit data buffer register. The transformer primary and secondary circuits are the same as shown in Figure 2.

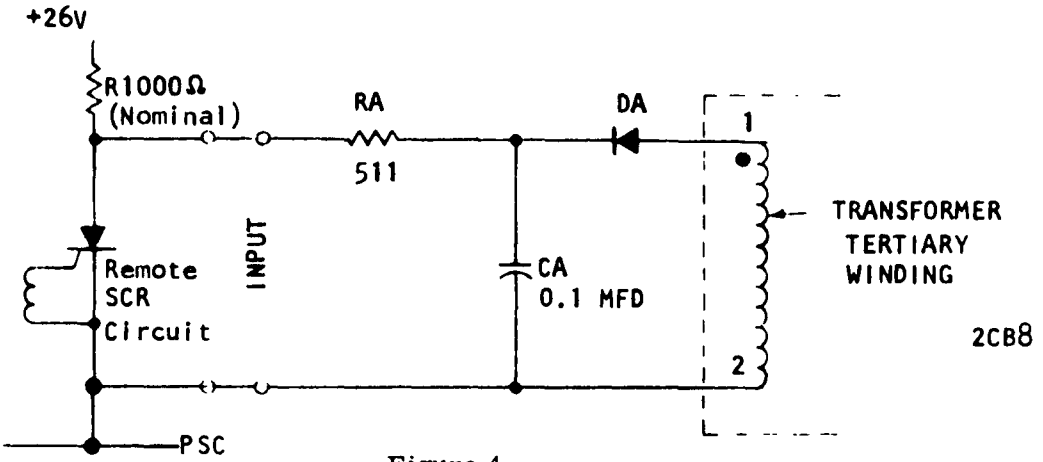


Figure 4

The operation is similar to that described for the 2CB4, 2CB6, and 2CB7 modules. The difference is that the voltage across capacitor CA is controlled by the state of SCR. The time constant for charging the capacitor is influenced by the value of the external resistor R.

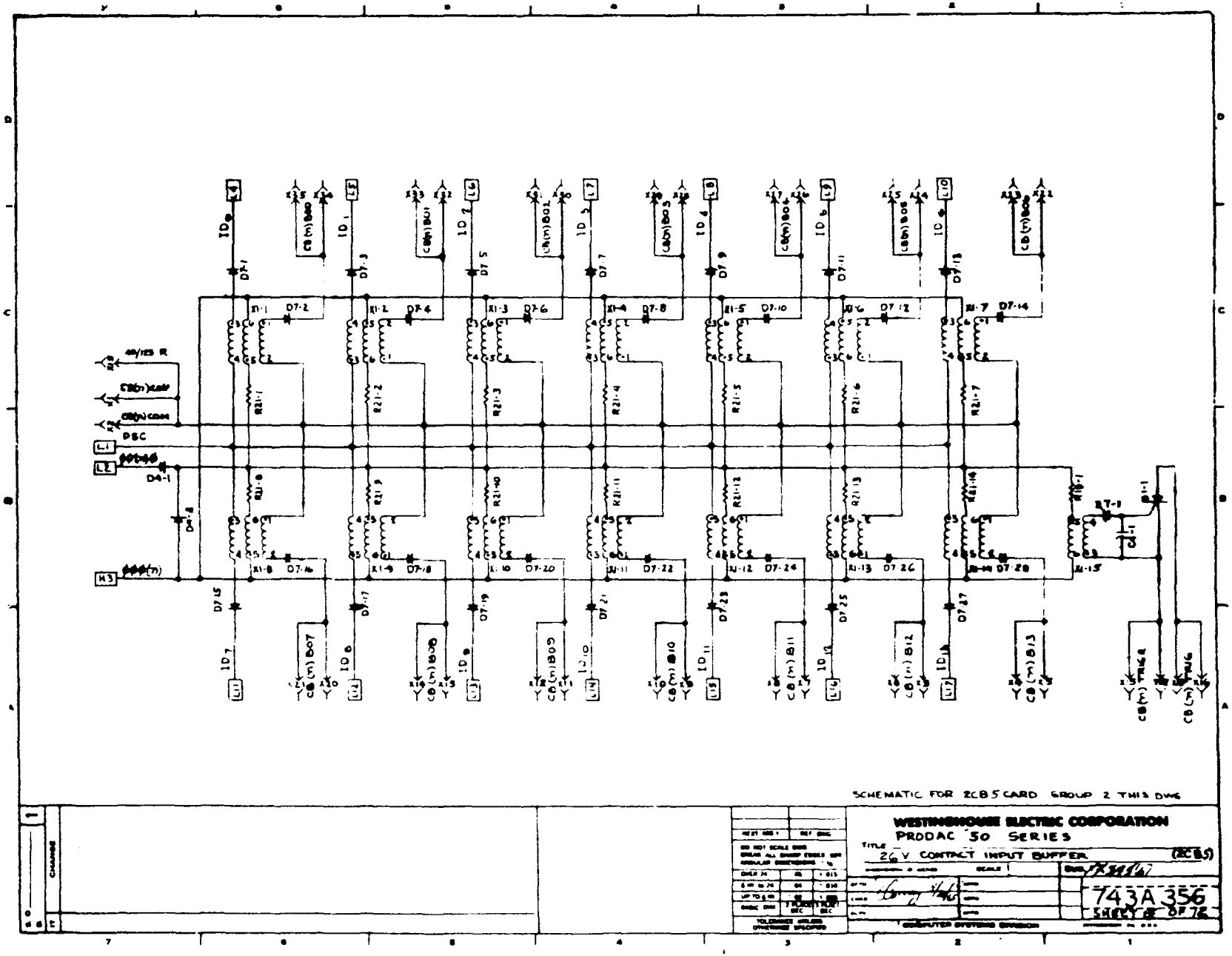
4. Control

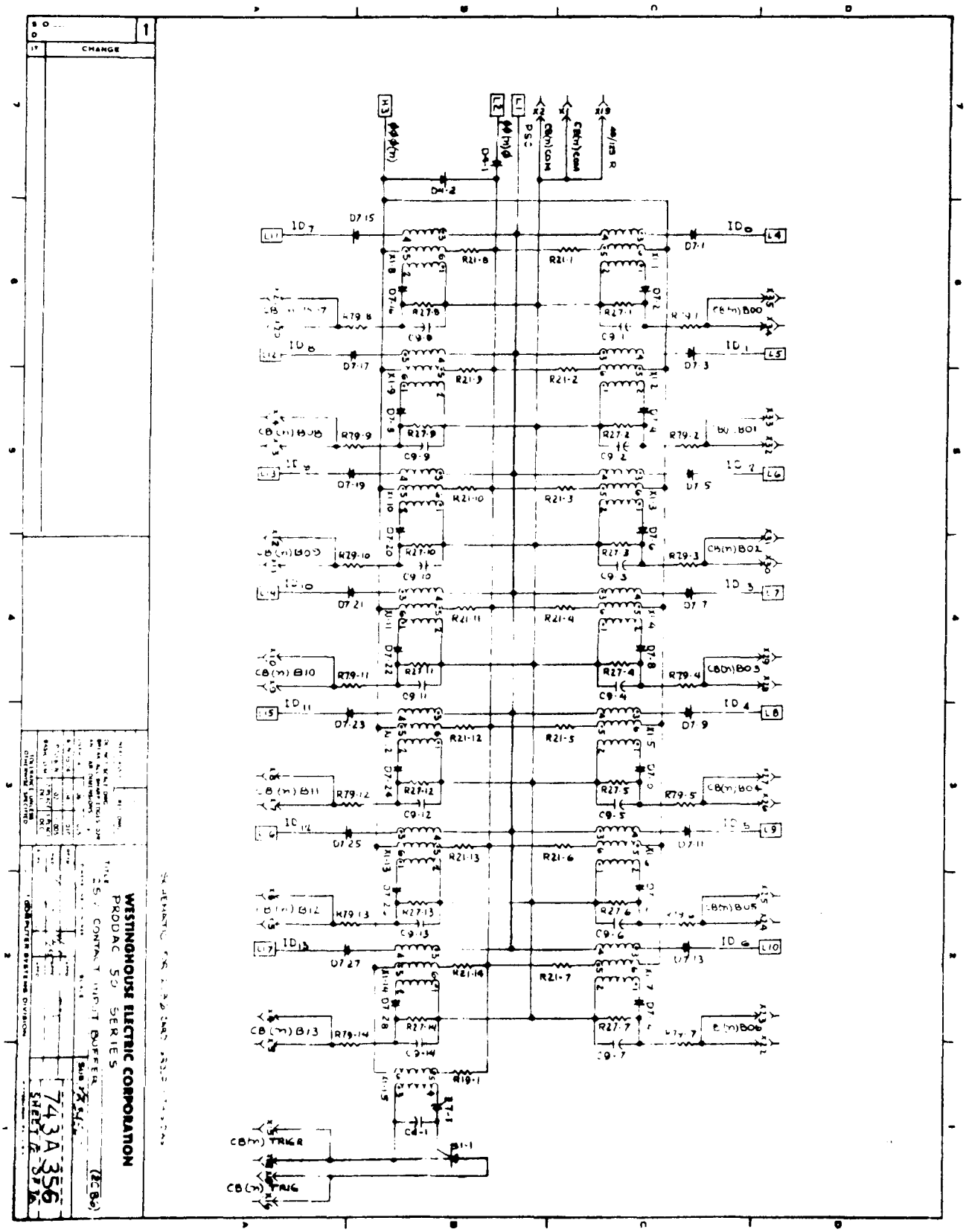
The module contains a transformer isolated SCR used for detection of selection of the module channel half select circuits. When the transformer primary windings are pulsed, the detector SCR turns on. The SCR must be turned off by remote circuits.

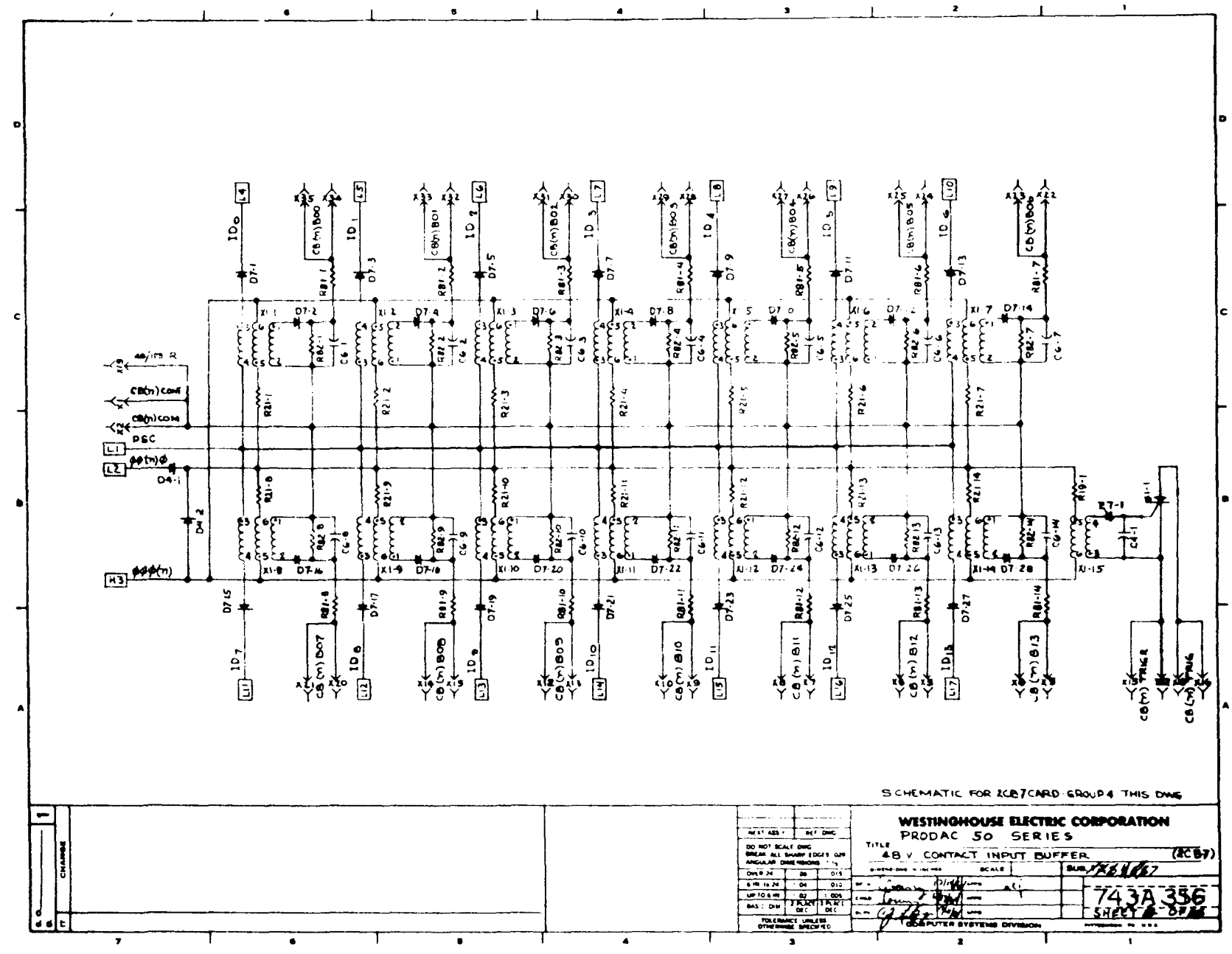
Note that all of the 14 data transformer primary windings and the SCR transformer primary windings are pulsed at the same time.

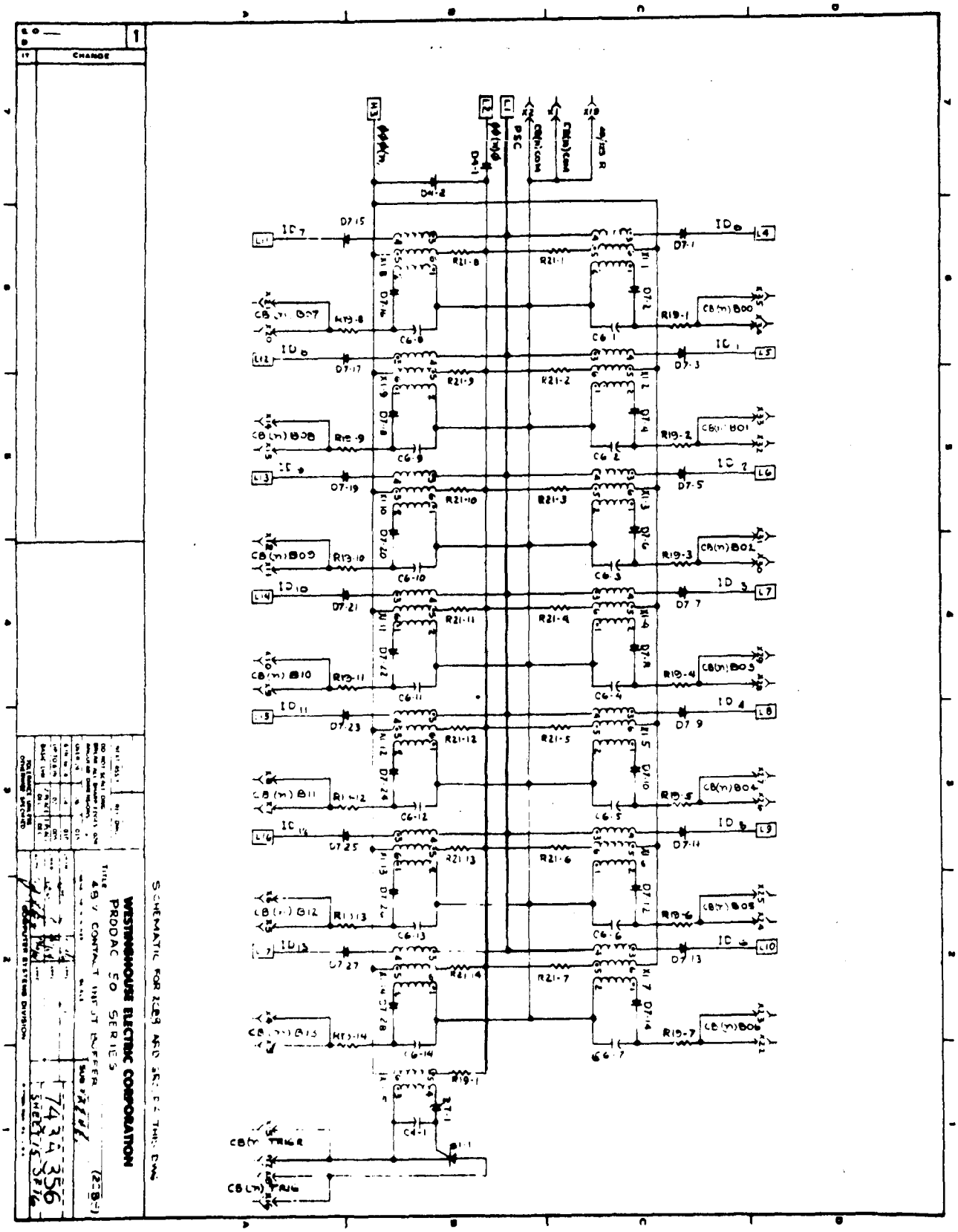
The schematic diagrams for the 2CB series are included with this description.

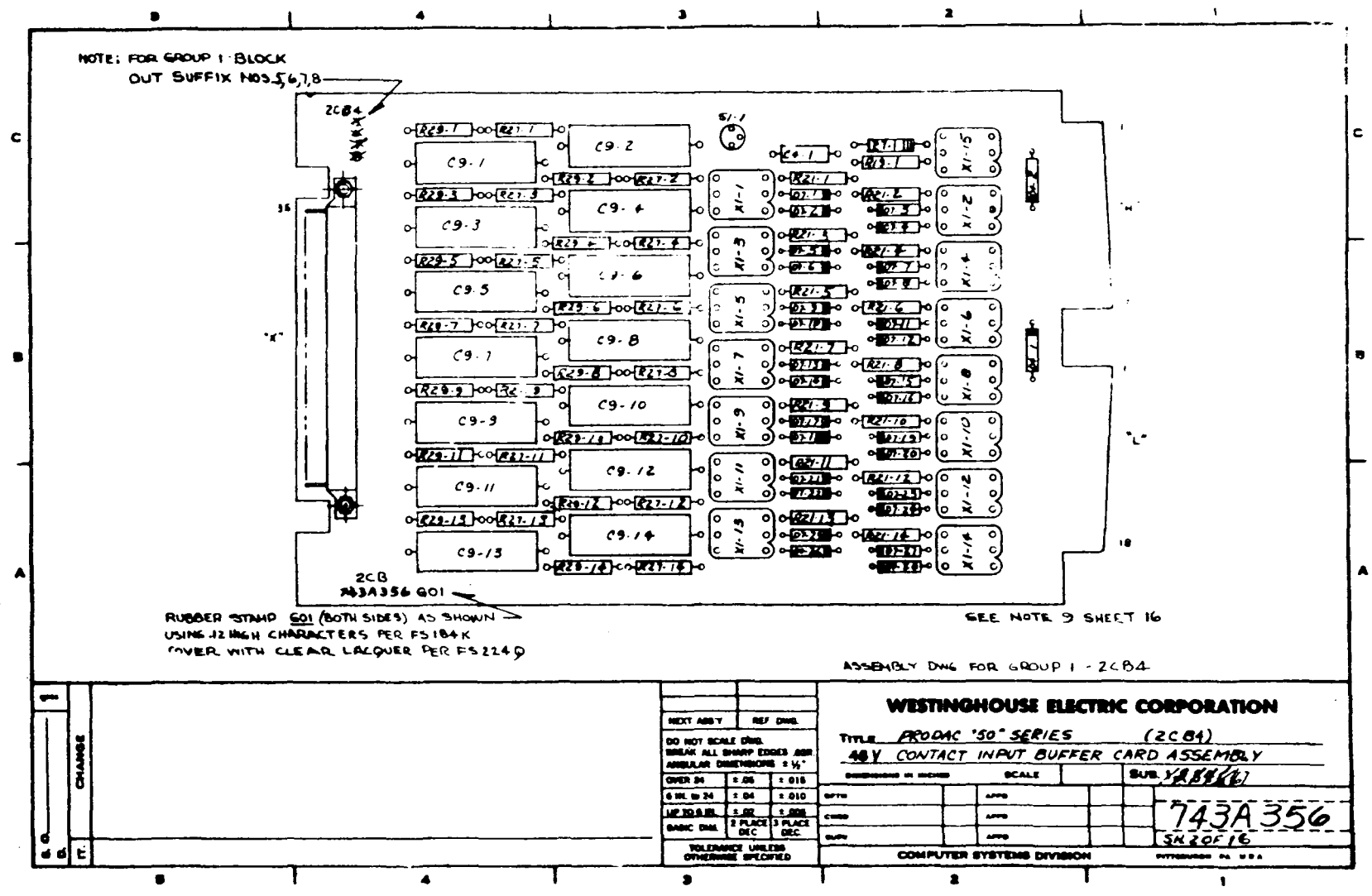
SCHEMATIC FOR ICBM CARD - GROUP I THIS DWG
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
48 V CONTACT INPUT BUFFER
743A358

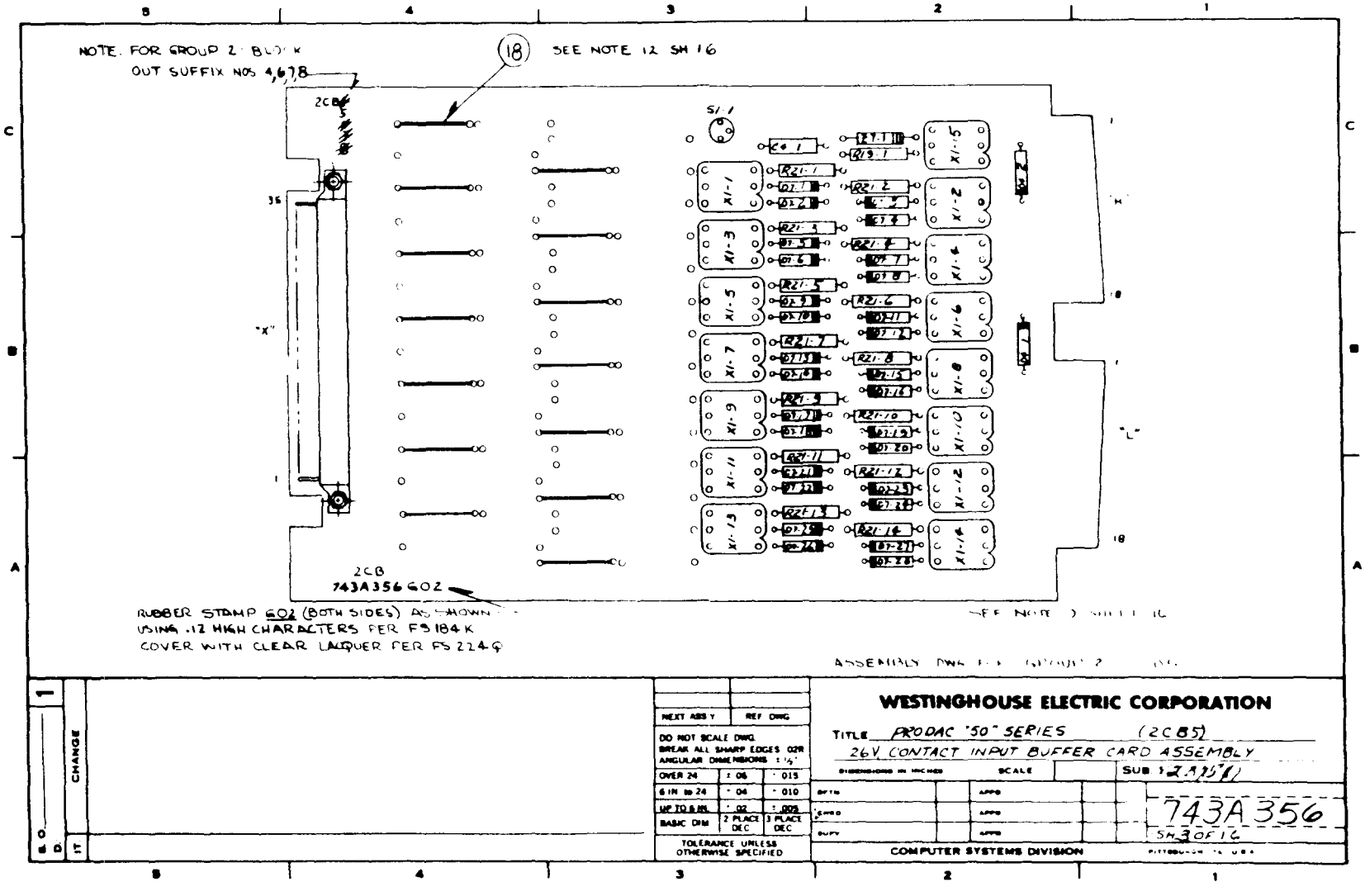

SCHEMATIC FOR 2CB5 CARD GROUP 2 THIS DWG
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
TITLE
20 V CONTACT INPUT BUFFER (2CB5)
743A356
SHEET 18 OF 72

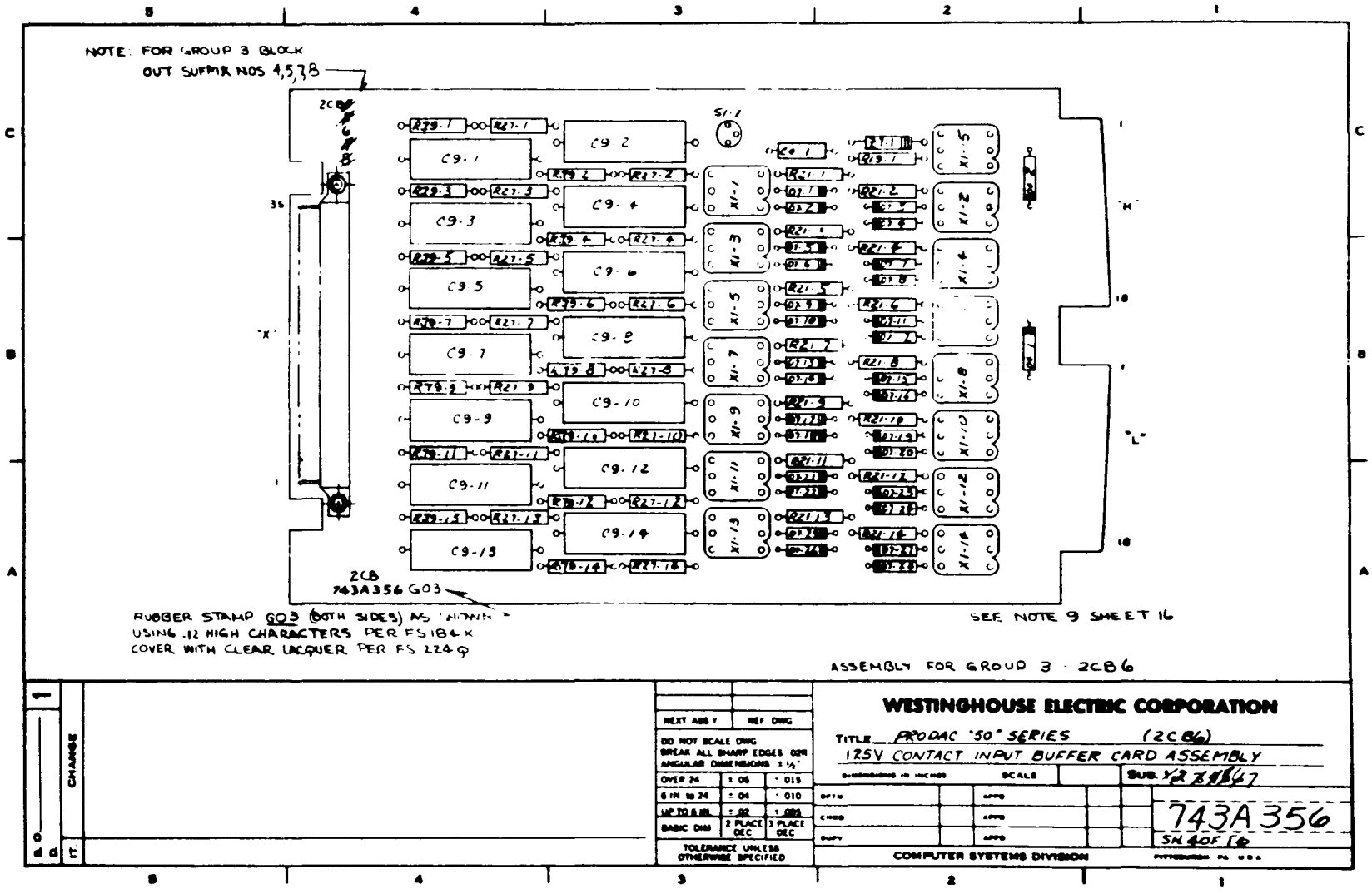

CHANGE
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
743A356
SHEET 2 OF 16

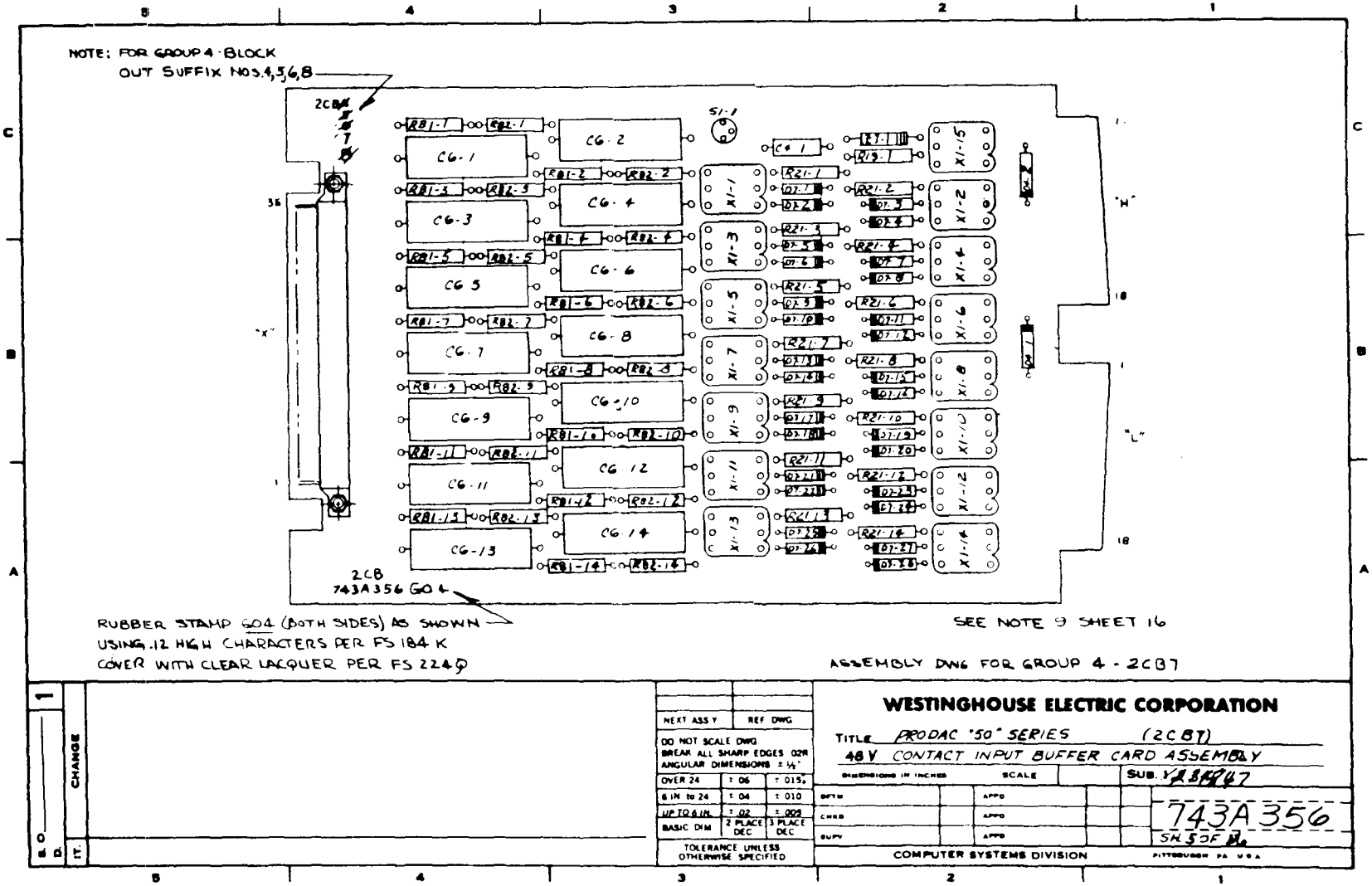

SCHEMATIC FOR 2CB7 CARD GROUP 4 THIS DWG
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
TITLE
48 V CONTACT INPUT BUFFER
(2CB7)
743A356
SHEET 8 OF 8
COMPUTER SYSTEMS DIVISION
CB(n) CONF
CB(n) COM
PSC

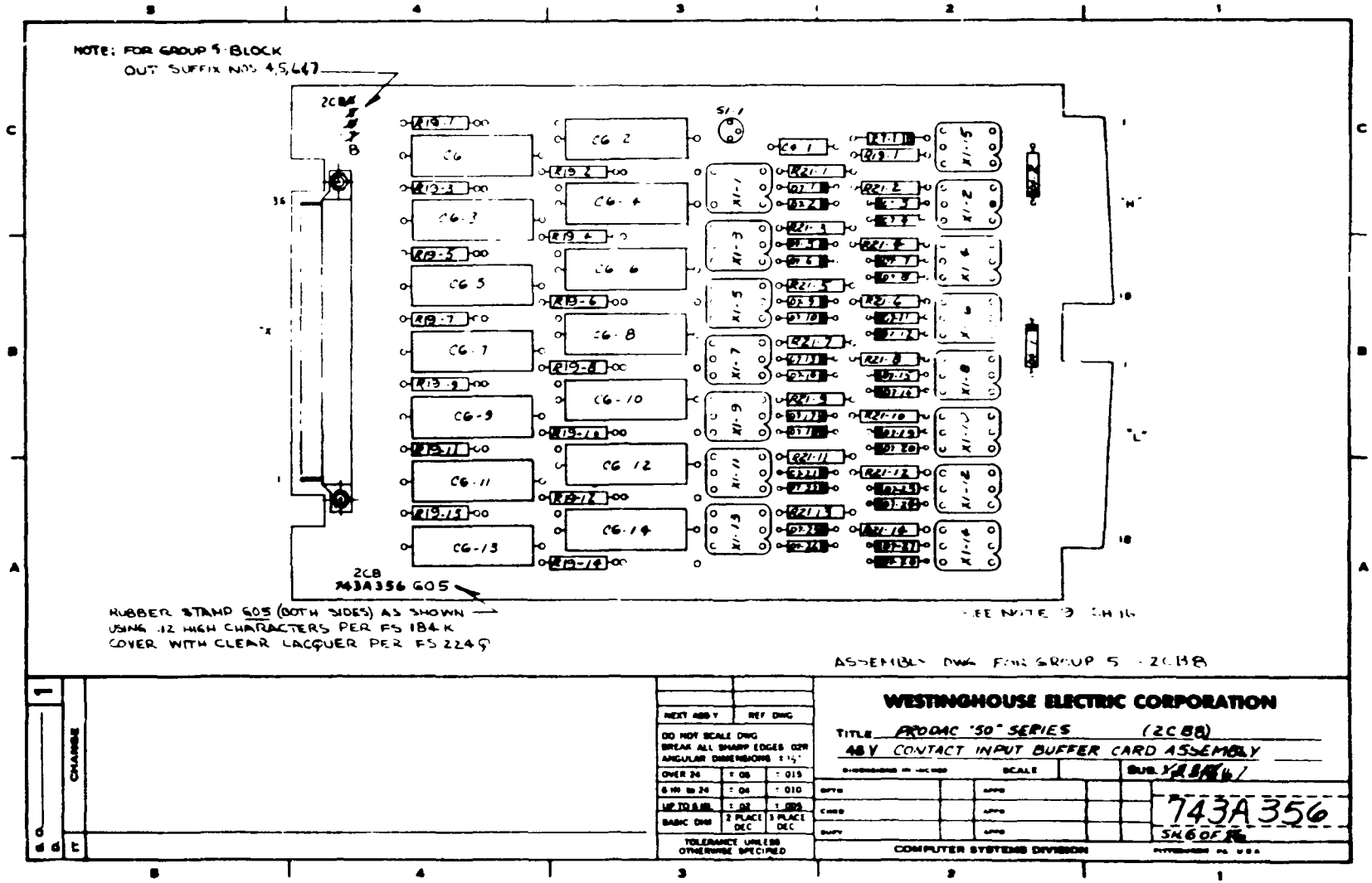

WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
SCHEMATIC FOR
SHEET 15 OF 16
74A4356


NOTE: FOR GROUP 1 BLOCK
OUT SUFFIX NOS. 5,6,7,8
2CB4
S1-1
C9-1
C9-2
C9-3
C9-4
C9-5
C9-6
C9-7
C9-8
C9-9
C9-10
C9-11
C9-12
C9-13
C9-14
X1-1
X1-2
X1-3
X1-4
X1-5
X1-6
X1-7
X1-8
X1-9
X1-10
X1-11
X1-12
X1-13
X1-14
X1-15
2CB
743A356 G01
RUBBER STAMP G01 (BOTH SIDES) AS SHOWN
USING .12 HIGH CHARACTERS PER FS 184 K
COVER WITH CLEAR LACQUER PER FS 224 D
SEE NOTE 9 SHEET 16
ASSEMBLY DWG FOR GROUP 1 - 2CB4
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC "50" SERIES (2CB4)
48 V CONTACT INPUT BUFFER CARD ASSEMBLY
SCALE
SIZE B
743A356
SH 2 OF 16
COMPUTER SYSTEMS DIVISION
CHANGE
NEXT ASS'Y
REF DWG.
DO NOT SCALE DWG.
BREAK ALL SHARP EDGES .005
ANGULAR DIMENSIONS ± ½°
OVER 24 ± .06 ± .015
6 IN. to 24 ± .04 ± .010
UP TO 6 IN. ± .02 ± .005
BASIC DIM. 2 PLACE DEC 3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED


NOTE. FOR GROUP 2 BLOCK
OUT SUFFIX NOS 4,6,7,8
18
SEE NOTE 12 SH 16
2CB
5
35
"X"
2CB
743A356 G02
RUBBER STAMP G02 (BOTH SIDES) AS SHOWN
USING .12 HIGH CHARACTERS PER FS 184 K
COVER WITH CLEAR LACQUER PER FS 224 G
SEE NOTE 1 SHEET 16
ASSEMBLY DWG FOR GROUP 2
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC "50" SERIES (2CB5)
26V CONTACT INPUT BUFFER CARD ASSEMBLY
SUB 1
743A356
SH 3 OF 16
COMPUTER SYSTEMS DIVISION
NEXT ASSY
REF DWG
DO NOT SCALE DWG.
BREAK ALL SHARP EDGES .02R
ANGULAR DIMENSIONS ± ½°
OVER 24 ± .06 .015
6 IN to 24 ± .04 .010
UP TO 6 IN. ± .02 ± .005
BASIC DIM 2 PLACE DEC 3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED
CHANGE
LTR


NOTE: FOR GROUP 3 BLOCK
OUT SUFFIX NOS 4,5,7,8
2CB
743A356 G03
RUBBER STAMP G03 (BOTH SIDES) AS SHOWN
USING .12 HIGH CHARACTERS PER FS1B4K
COVER WITH CLEAR LACQUER PER FS 224g
SEE NOTE 9 SHEET 16
ASSEMBLY FOR GROUP 3 - 2CB6
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC "50" SERIES (2CB6)
125V CONTACT INPUT BUFFER CARD ASSEMBLY
SCALE
SUB 1
743A356
SH 4 OF 16
COMPUTER SYSTEMS DIVISION
NEXT ASSY
REF DWG
DO NOT SCALE DWG
BREAK ALL SHARP EDGES .02R
ANGULAR DIMENSIONS ± ½°
OVER 24 ± .06 ± .015
6 IN to 24 ± .04 ± .010
UP TO 6 IN ± .02 ± .005
BASIC DIM 2 PLACE DEC 3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED
CHANGE
ECO
IT


NOTE: FOR GROUP 4 BLOCK OUT SUFFIX NOS. 4,5,6,8
2CB
CG-1
CG-2
CG-3
CG-4
CG-5
CG-6
CG-7
CG-8
CG-9
CG-10
CG-11
CG-12
CG-13
CG-14
XI-1
XI-3
XI-5
XI-7
XI-9
XI-11
XI-13
XI-15
XI-2
XI-4
XI-6
XI-8
XI-10
XI-12
XI-14
"X"
"H"
"L"
2CB
743A356 G04
RUBBER STAMP G04 (BOTH SIDES) AS SHOWN
USING .12 HIGH CHARACTERS PER FS 184 K
COVER WITH CLEAR LACQUER PER FS 224D
SEE NOTE 9 SHEET 16
ASSEMBLY DWG FOR GROUP 4 - 2CB7
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC "50" SERIES (2CB7)
48 V CONTACT INPUT BUFFER CARD ASSEMBLY
743A356
COMPUTER SYSTEMS DIVISION
PITTSBURGH PA U.S.A.


NOTE: FOR GROUP 5 BLOCK
OUT SUFFIX NOS 4,5,6&7
2CB
S1-1
CG 1
CG 2
CG-3
CG-4
CG 5
CG 6
CG-7
CG-8
CG-9
CG-10
CG-11
CG 12
CG-13
CG-14
2CB
743A356 G05
RUBBER STAMP 605 (BOTH SIDES) AS SHOWN
USING .12 HIGH CHARACTERS PER FS 184K
COVER WITH CLEAR LACQUER PER FS 224S
SEE NOTE 3 SHT 1
ASSEMBLY DWG FOR GROUP 5 - 2CBB
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC "50" SERIES (2CBB)
48 V CONTACT INPUT BUFFER CARD ASSEMBLY
743A356
SHEET OF
COMPUTER SYSTEMS DIVISION

4CD1 - CHANNEL DRIVER MODULE

GENERAL DESCRIPTION

This module (CD) is used to provide a 14 bit channel driver output to the I/O subsystems. It contains 14 identical SCR circuits and one gate triggering circuit. An application block diagram is shown in Figure 1.

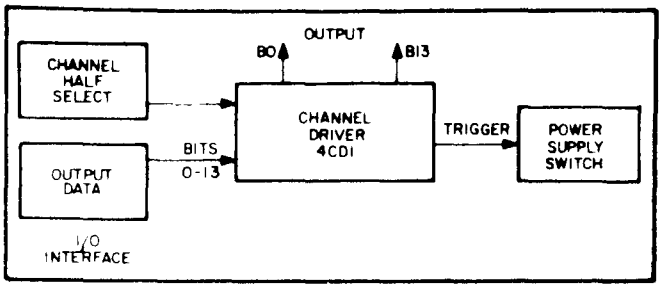


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The half-select inputs, ØØ (n) Ø and ØØØ (n), require a minimum 11 V, 4 μs pulse.

The data inputs (OD13, etc.) require logic level signals of "zero" (1.1 V max.) and "one" (4.4 V min.).

Output Requirements

The driver output (CD (n) B13, etc.) requires a "zero" for selected bit and a "one" for unselected bits.

CD (n) common is normally tied to PSC through the power supply switch, to reset the SCR circuits, this must be opened for a minimum of 150 μs.

Power Requirements

+ 26 V is required for card operation.

CIRCUIT DESCRIPTION

Each of the 14 bits of the channel driver consists of an SCR with a zener diode threshold in the gate circuit and a three winding gate trigger transformer. In addition, there is another SCR on the card which senses the selection of the channel and sends a trigger to the power supply switch (CD (n) TRIG). Figure 2 shows the diagram of one channel SCR and associated circuitry. The connections to the power supply switch are shown in dotted lines.

The operation of the circuit is explained as follows.

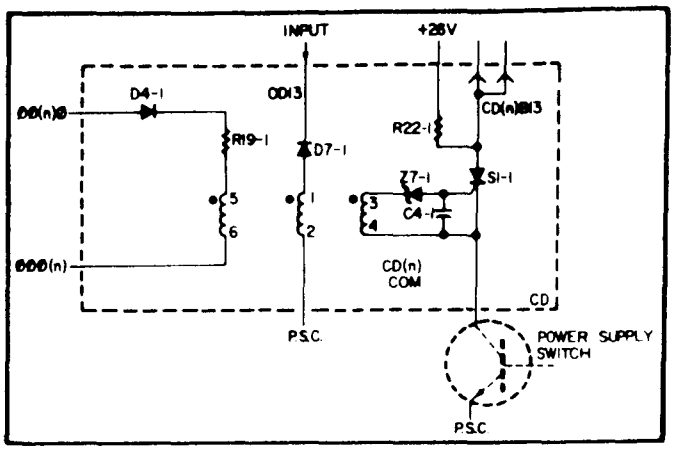


FIGURE 2. ONE CHANNEL SCR CIRCUIT

Initially the output transistor of the power supply switch is saturated (conducting heavily) so that if a positive trigger pulse is applied between the gate and the cathode of S1-1, the SCR will conduct.

The gate circuit consists of zener diode Z7-1 in series with the secondary winding (3-4) of the trigger transformer. The tertiary winding (1-2) of the trigger transformer is connected through diode D7-1. When the input is a logical "one" diode D7-1 is reversed biased, which open circuits the tertiary winding. If the input is a logical "zero", D7-1 is grounded which shorts out the tertiary winding.

It can be seen that when a pulse (channel half-select ØØ (n) Ø and ØØØ (n)) appears across the primary winding (5-6) the logic level of the input line will determine the voltage on the secondary (3-4).

With the input a logical "one", the secondary (3-4) will have a voltage induced in it which triggers S1-1 and drives its output to a logical "zero". This occurs because + 26 V tied to R22-1 will conduct through the power supply switch to PSC.

With the input a logical "zero", no voltage will be induced in the secondary, the SCR will not conduct and therefore the output will remain a logical "one".

The zener diode in the gate circuit is needed since the tertiary winding is never completely short circuited. Losses in diode drop and transistor saturation drop account for a small pulse across the secondary winding when the input is a logical "zero". When the input is a logical "one" and the particular channel is selected, the SCR's will be triggered in response to the half-select pulse. The SCR will remain in the conduction state until the power supply switch turns it off.

* * *

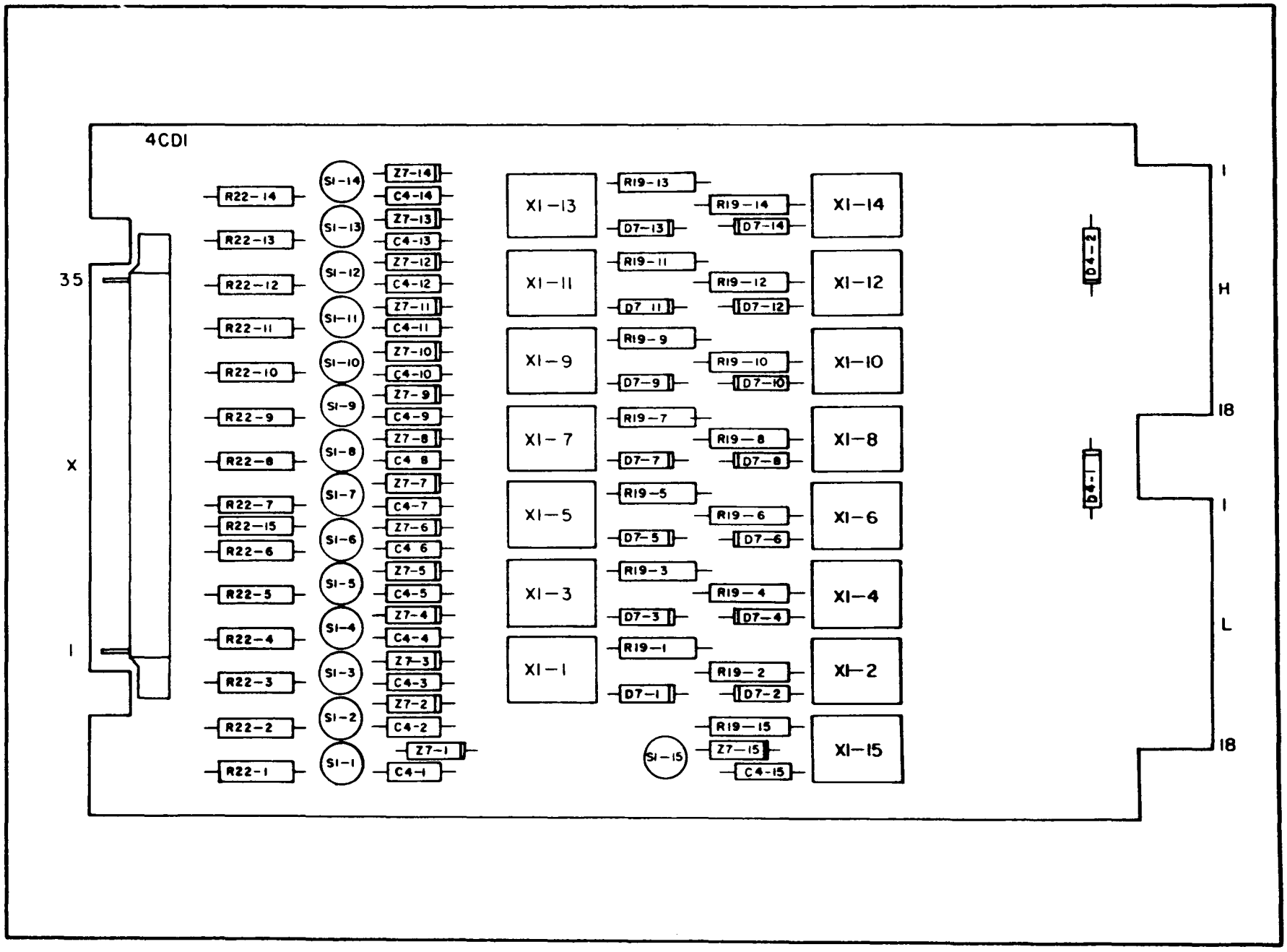


FIGURE 3. 4CD1 ASSEMBLY (REF. DWG. 743A391, SUB 3)

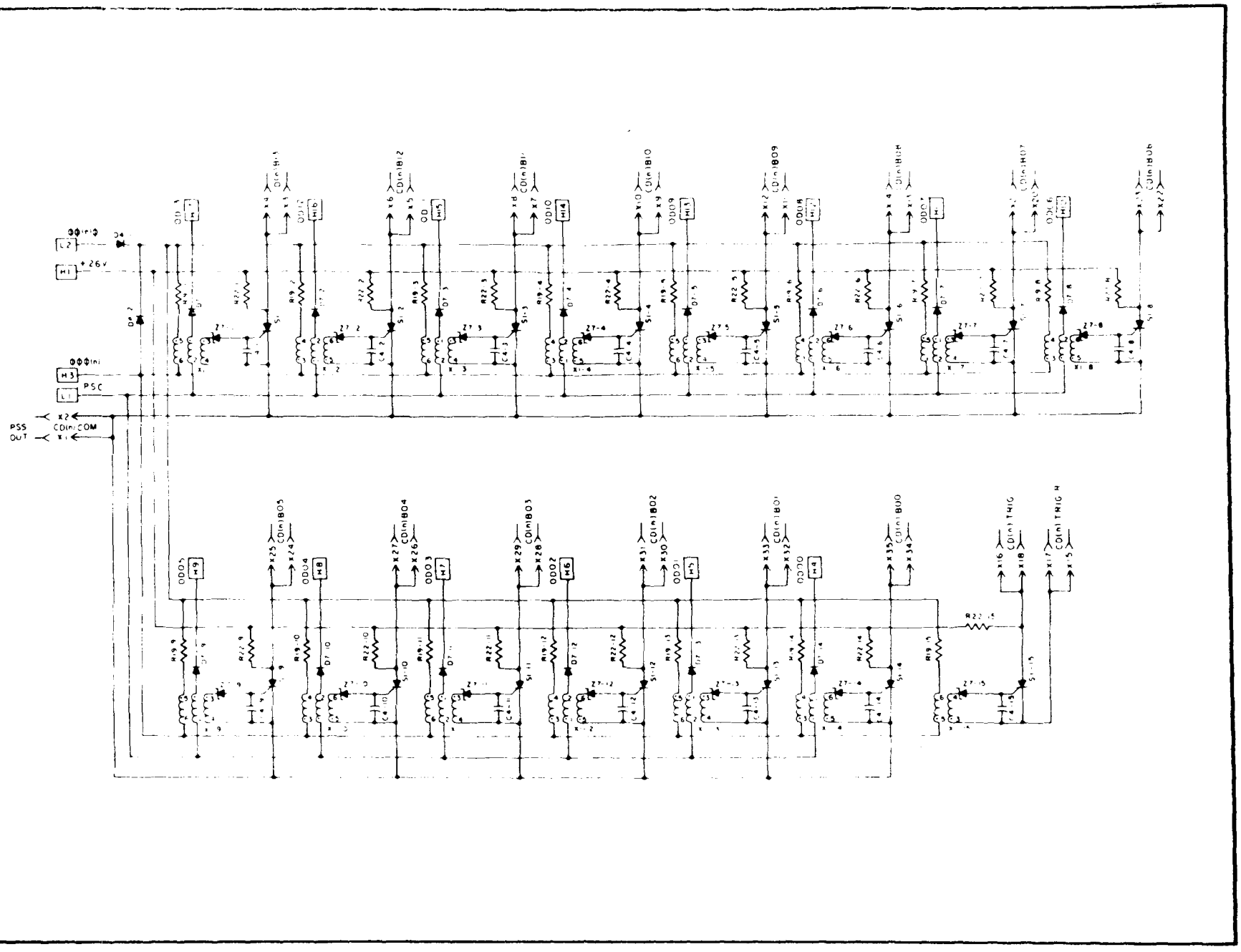


FIGURE 4. 4CD1 SCHEMATIC (REF. DWG. 743A391, SUB 3)

5CL1 - CALIBRATOR MODULE

GENERAL DESCRIPTION

This module is used in the analog input subsystem to provide accurate voltage references for system calibration, RTD measuring circuits for measurement of the thermocouple cold junction temperature, and a power supply switch circuit used in conjunction with the span driver circuits (see SB module). An application block diagram is shown in Figure 1.

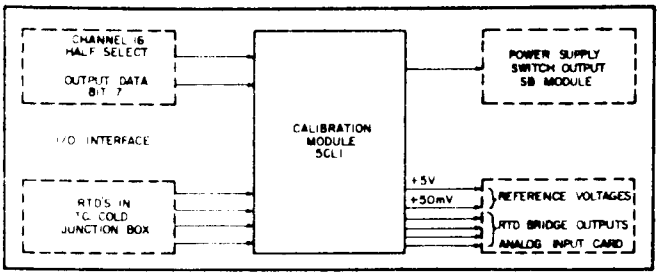


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The channel 16 half-select input requires a minimum 11 V, 4 μs pulse.

Bit 7 input requires a logical "one" if selected and a logical "zero" if not selected.

The RTD inputs require a 100 ohm, 3 wire RTD connection.

Output Capabilities

The reference voltage outputs provide analog voltage signals of:

$$V_2 = 0.03987 \pm 0.01\%$$
$$V_1 = 4.4268 \pm 0.01\%$$

The RTD bridge outputs are 0-50 mV analog signals.

The power supply switch output is normally clamped to PSC.

The maximum current that can be carried by the switch is 850 mA. After the trigger signal, the switch opens for a period of 100 μs. In the non-conducting state the output is at + 26 V.

Power Requirements

Connections to + 26 V and PSC are required.

CIRCUIT DESCRIPTION

Since the 5CL module contains 3 functionally independent circuits, each of these are described separately.

Voltage Reference Circuit

The circuit diagram of the voltage reference circuit is shown in Figure 2.

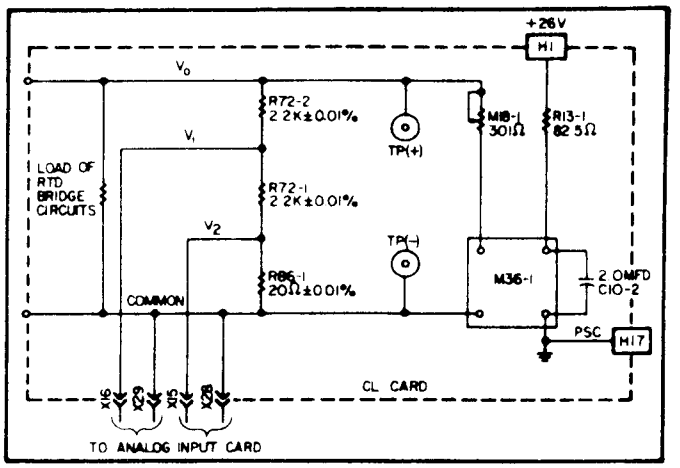


FIGURE 2. VOLTAGE REFERENCE CIRCUIT

The incoming power supply voltage (+ 26 V) is fed to a voltage regulator, M36-1, which is a voltage clipping circuit containing zener diodes. Since the voltage reference divider circuit, R72-1, R72-2 and R86-1, and the load of the RTD bridge circuits constitute a constant load, the voltage V_o (measured between test points TP (+) and TP (-) will be a stable reference voltage. This voltage is adjusted by potentiometer M18-1 to 8.8138V using a standard cell.

The reference voltages, determined by the resistance values of R72-1, R72-2 and R86-1, are V_1 = 4.4268V, V_2 = 0.03987V.

These voltages are used to check the accuracy of the V/F converter.

RTD Bridge Circuits

There are four, identical RTD bridge circuits on the

5CL card. These circuits are used to measure the temperature of the thermocouple cold junction boxes. Since each cold junction box contains 2 RTD's, the 5CL card provides for measurement of 2 cold junction boxes.

The circuit diagram of one RTD bridge circuit is shown in Figure 3.

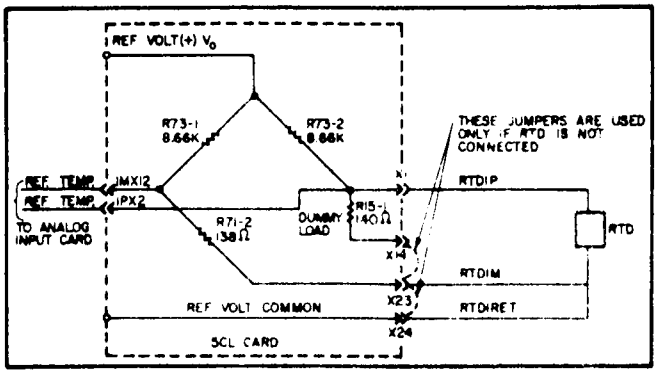


FIGURE 3. RTD BRIDGE CIRCUIT

The same voltage (V) as used for the voltage references is used as supply voltage to the RTD bridges. Since resistors R73-1 and R73-2 are much greater than the RTD resistance, the RTD resistance variation has a negligible effect on the bridge load, so this can be considered constant. If a bridge circuit is not required for RTD measurement, a dummy load R15-1 is connected in place of the RTD. The output of the RTD bridge is connected as an analog input. The bridge output depends on the resistance value of the RTD. For example:

at RTD = 138 ohms, E out = 0V
at RTD = 188 ohms, E out = 50mV

Power Supply Switch

This circuit is a simplified power supply switch for the span driver circuits on the SB card.

Figure 4 shows a simplified schematic of the power supply switch transistor and is normally turned on as long as bit 7 of the span data word is a "zero". Winding 1-2 of X1-1 is shorted and no coupling can occur to winding 5-6 when the channel driver is pulsed. Under these conditions T6-1 is turned off and held off by the clamp at point "A", and T6-2 and T7-1 are turned on. S2-1 at this time will be turned off.

If bit 7 is a "one" and X1-1 is interrogated, point 5 of X1-1 will go positive and turn on T6-1. When T6-1 is turned on, the base of T6-2 forced to ground. T6-2 and T7-1 will turn off and the clamp at point "A" is removed. At the same time, C4 begins to charge, and when it charges sufficiently, S2-1 turns on and forces the base of T6-2 to a positive value so that T6-2 and T7-1 again turn on. As soon as T6-2 turns on, point "A" is again clamped to ground and T6-1 is turned off. The power supply switch T7-1 turns off for a period of time determined by the charge time of C4.

* * *

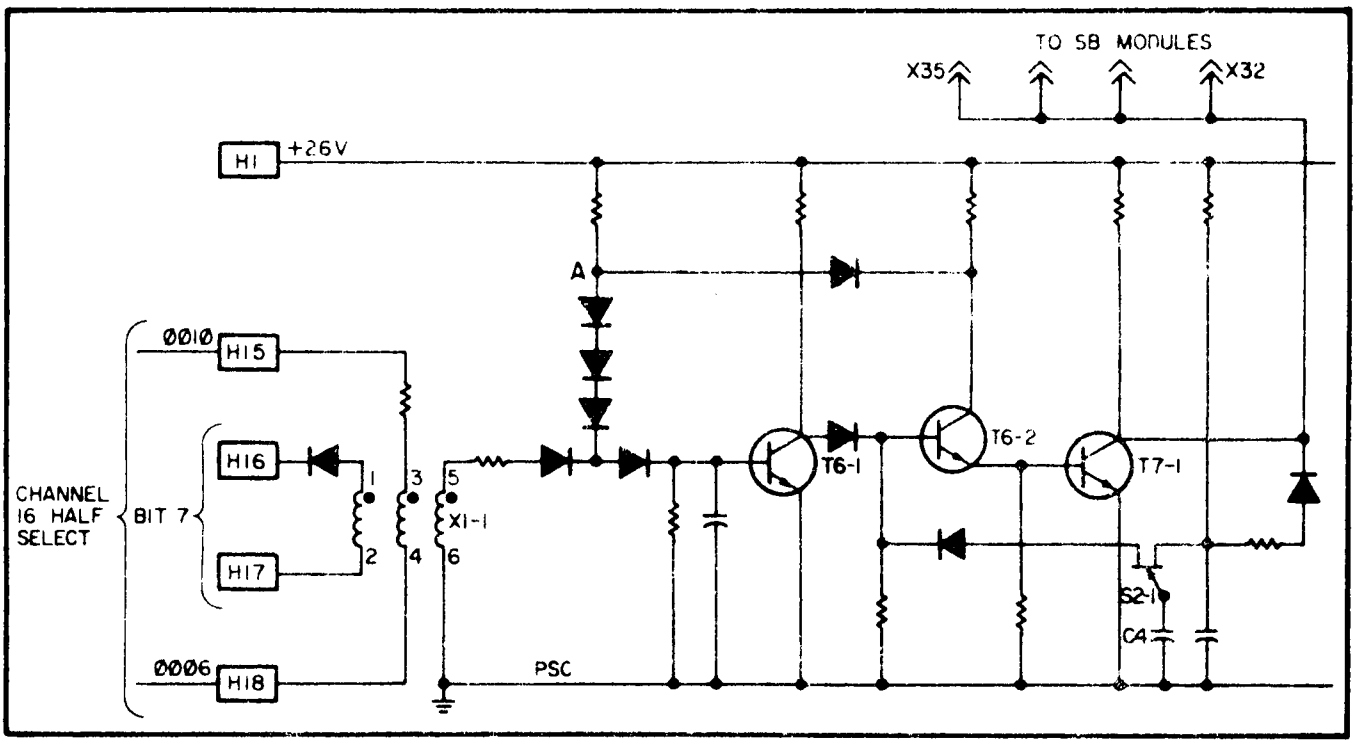


FIGURE 4. POWER SUPPLY SWITCH CIRCUIT

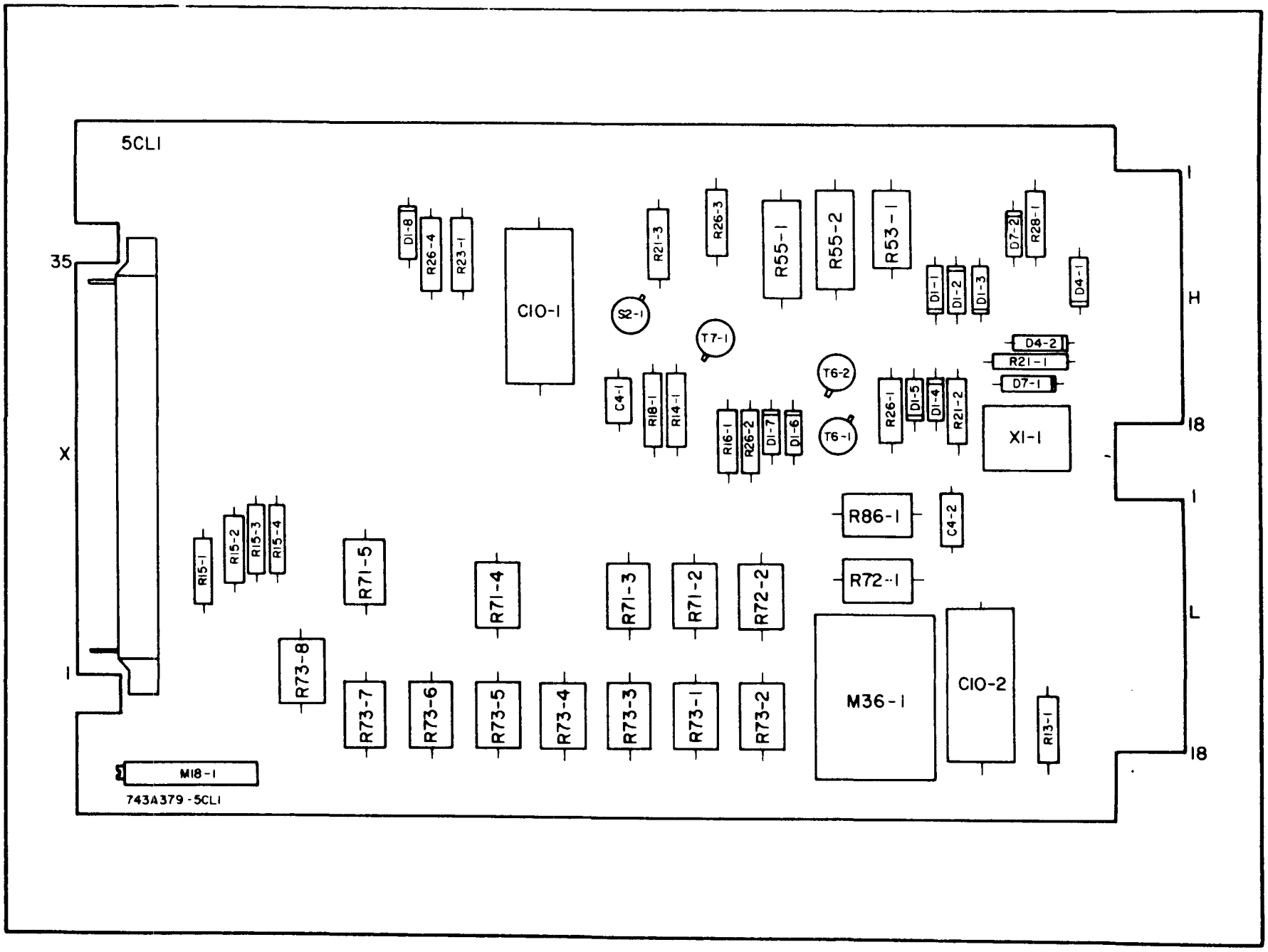
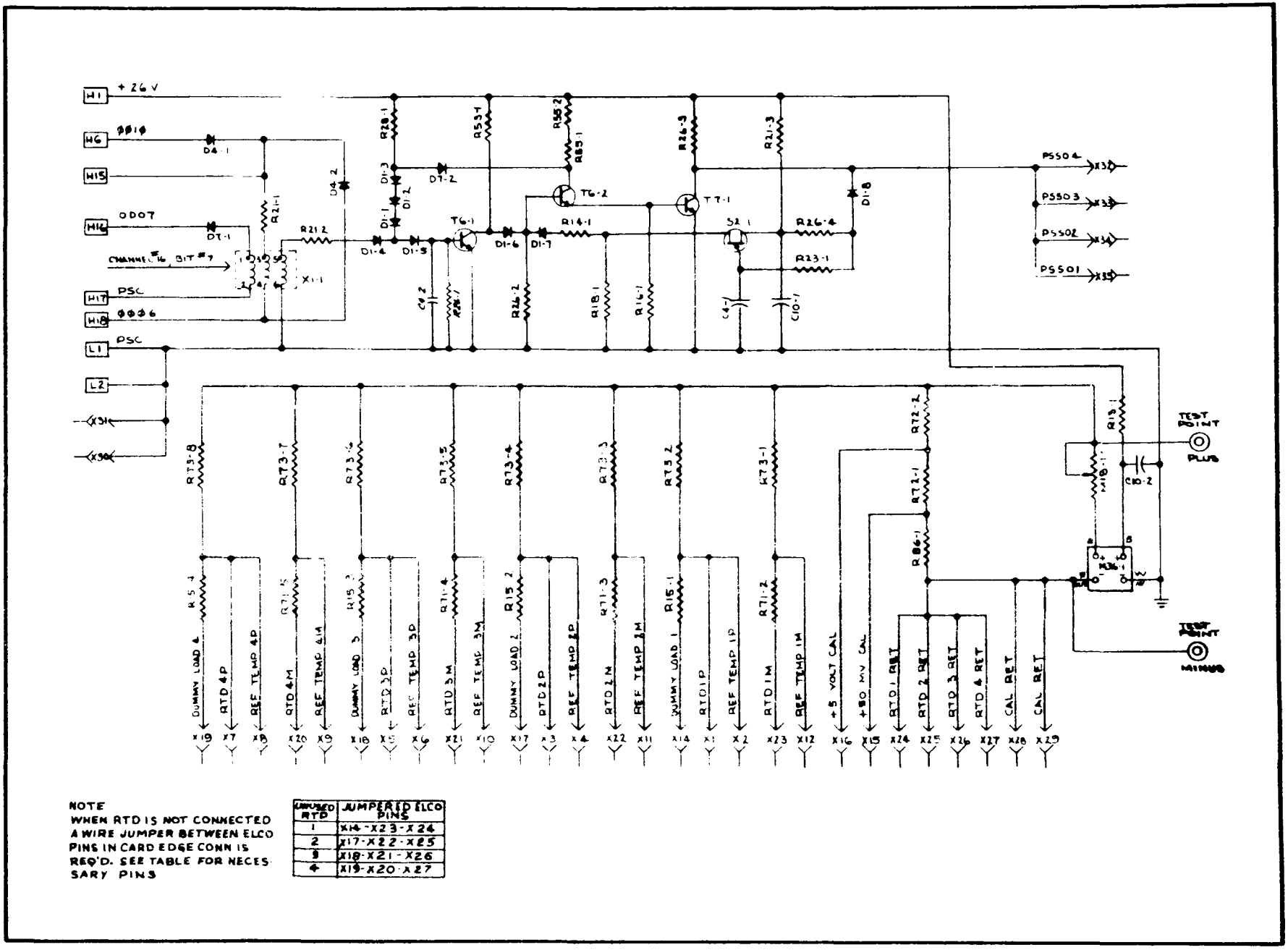


FIGURE 4. 5CL1 ASSEMBLY (REF. DWG. 743A379, SUB 9)



NOTE
WHEN RTD IS NOT CONNECTED A WIRE JUMPER BETWEEN ELCO PINS IN CARD EDGE CONN IS REQ'D. SEE TABLE FOR NECESSARY PINS

UNUSED RTD	JUMPERED ELCO PINS
1	X14 - X23 - X24
2	X17 - X22 - X25
3	X18 - X21 - X26
4	X19 - X20 - X27

FIGURE 5. 5CL1 SCHEMATIC (REF. DWG. 743A379, SUB 9)

3CM2/3CM3 - CONTACT INPUT MULTIPLEX MODULE

GENERAL DESCRIPTION

The 3CM2 and 3CM3 modules are used to multiplex process contacts to the input system. These modules contain two identical relay and diode isolation circuits. An application block diagram is shown in Figure 1.

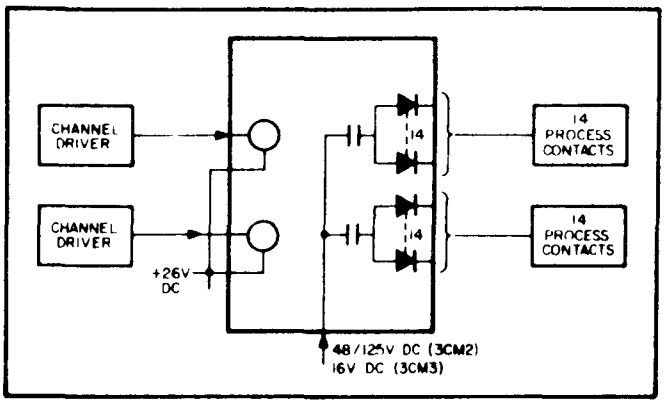


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The coil has a resistance of 675 Ω and has 5200 turns. The minimum requirements for pickup are 8.6V at 11.6 mA. The contacts will close 3 msec after the coil is energized.

Output Requirements

When the contacts close for 3CM2 the 48 or 125Vdc will be presented to the outputs at less than 100 Ω impedance. For 3CM3, 16V will be presented to the outputs at less than 25 Ω.

Power Requirements

- 26Vdc from I/O power supply.
- 16, 48, or 125Vdc from I/O system buss for process contacts.

CIRCUIT DESCRIPTION

When either of the two coils are selected, its contacts will close 3 msec later and this applies the 16, 48, or 125Vdc to the process contacts through the isolation diodes. These diodes are necessary to prevent sneak paths.

* * *

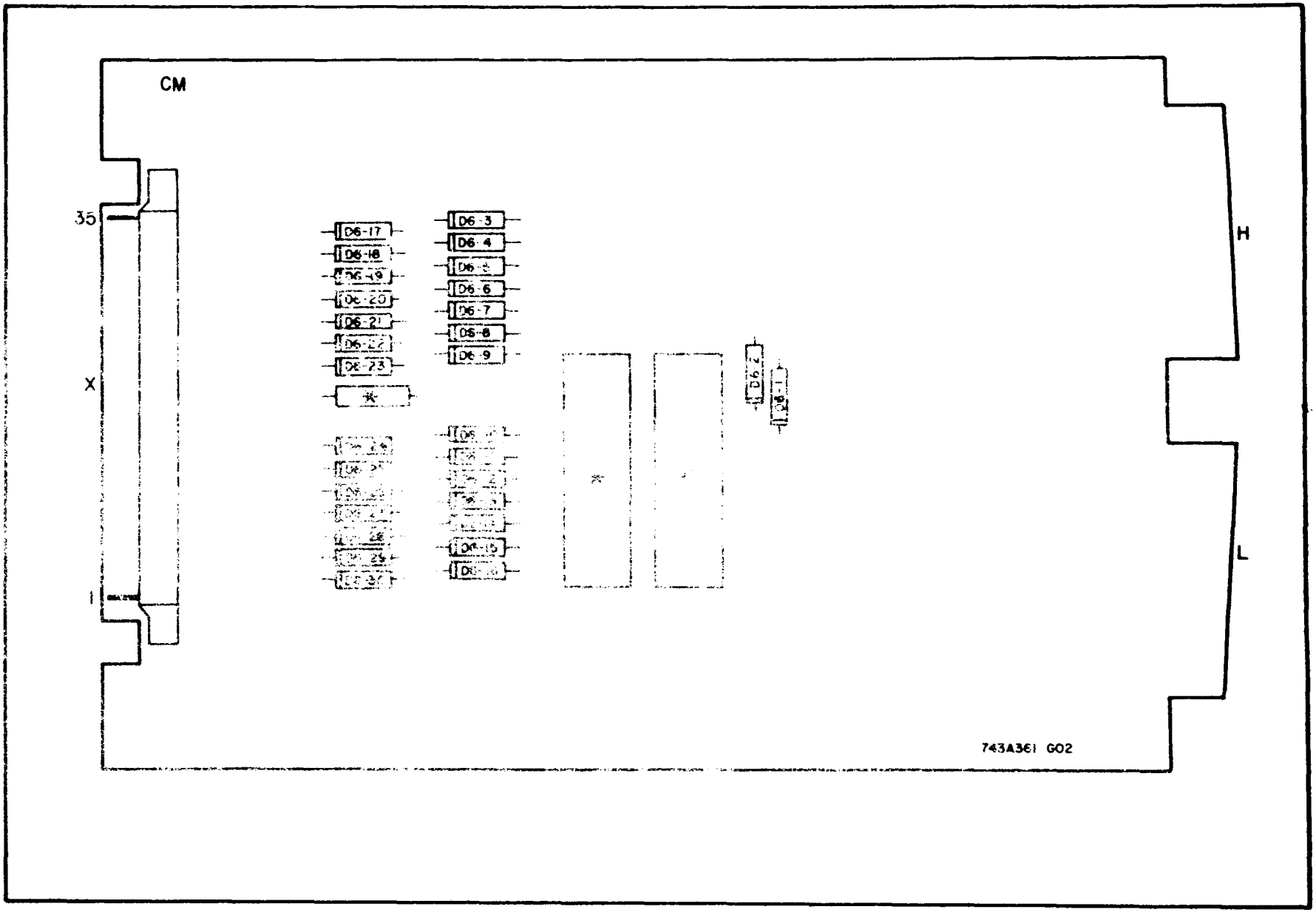


FIGURE 2. 3CM2/3CM3 ASSEMBLY (REF. DWG. 743A361, SUB 9)

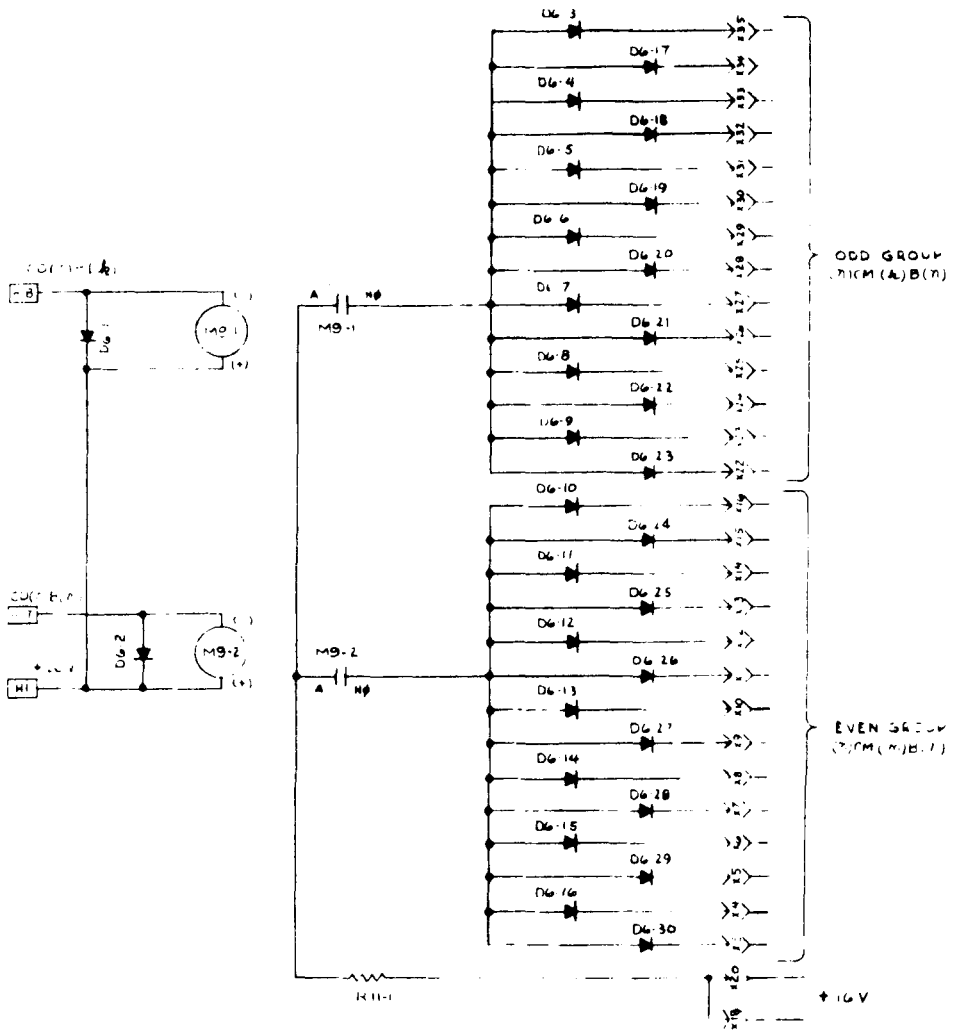


FIGURE 3. 3CM2/3CM3 SCHEMATIC (REF. DWG. 743A361, SUB 9)

2CO1/2CO2 - CONTACT OUTPUT MODULE

GENERAL DESCRIPTION

The 2CO1 module holds the contact output relays used in the CCO subsystem. Each card holds 7 relays, so 2 cards are required for each 14-bit relay register. The card also has 7 suppression diodes, one for each relay, and 7 isolation diodes. Figure 1 shows how contact output modules are used in the CCO subsystem.

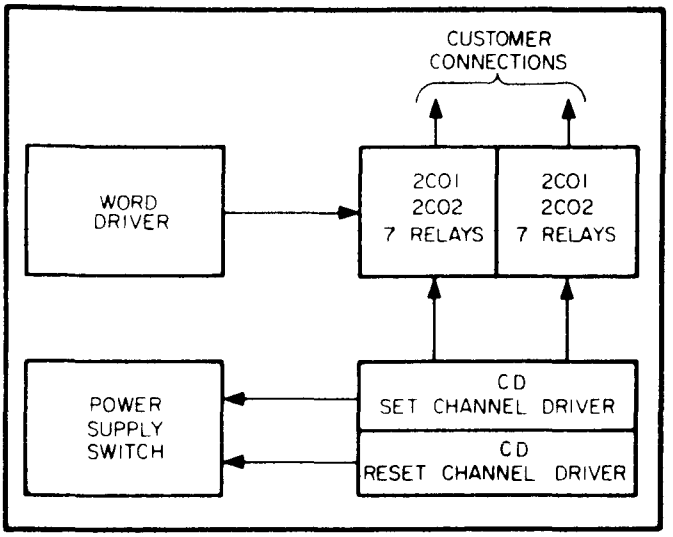


FIGURE 1 APPLICATION BLOCK DIAGRAM

CIRCUIT OPERATION

The relays on the contact output module are long life, bounce free, high speed mercury wetted type. They are magnetically biased for bi-stable operation and have Form D (make before break) contacts with a bridging time of approximately 100 μsec.

The relays are composed of a hermetically sealed, inert gas pressurized switch capsule of glass which is surrounded by a double wound operating coil. The capsule is potted in a high melting point wax and enclosed in a container which has provisions for printed circuit board mounting.

Figure 2 shows the contacts of one CCO relay with the RC contact suppression network. Figure 3 illustrates the range of safe operating loads which can be tolerated without additional, external contact suppression. Reliable, long life operation will result if the current through the contacts just prior to opening, and the peak voltage across the contacts as they open, both lie within the shaded area of Figure 3.

When using CCO relay contacts to control ac devices, a small amount of leakage current due to the RC suppression circuit will be present when the contacts are open.

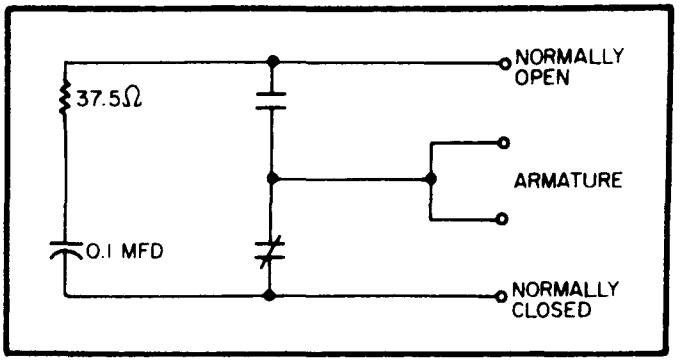


FIGURE 2. RELAY CONTACT SUPPRESSION NETWORK

At 60 Hz the leakage impedance is approximately 26,500 ohms. At higher frequencies the impedance may be calculated using the following formula:

$$Z\ (\text{OHMS}) = \sqrt{R^2 + \left(\frac{1}{\omega C}\right)^2}$$

where: R = 37.5 ohms
C = .1 μFd
ω = 2πf f = frequency

Note that even in a dc circuit the RC network will present a low impedance to high frequency components which may be caused by noise.

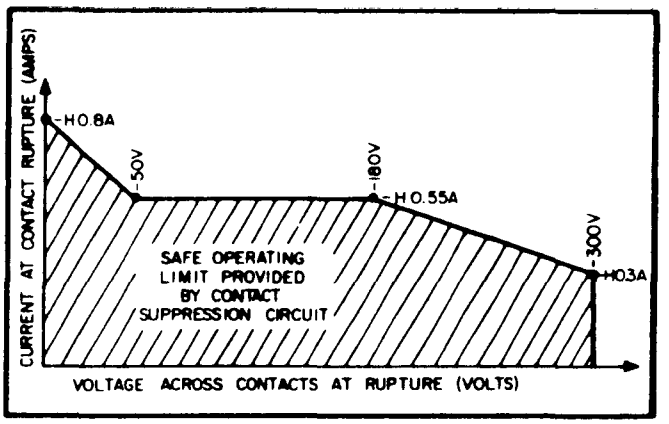


FIGURE 3. RANGE OF SAFE OPERATING LOADS

The 2CO2 module is identical to the 2CO1 module except that the RC contact suppression circuit is not included. This module is not used in the CCO subsystem since the lack of contact protection results in poor contact life. It is used only in computed data link circuitry.

* * *

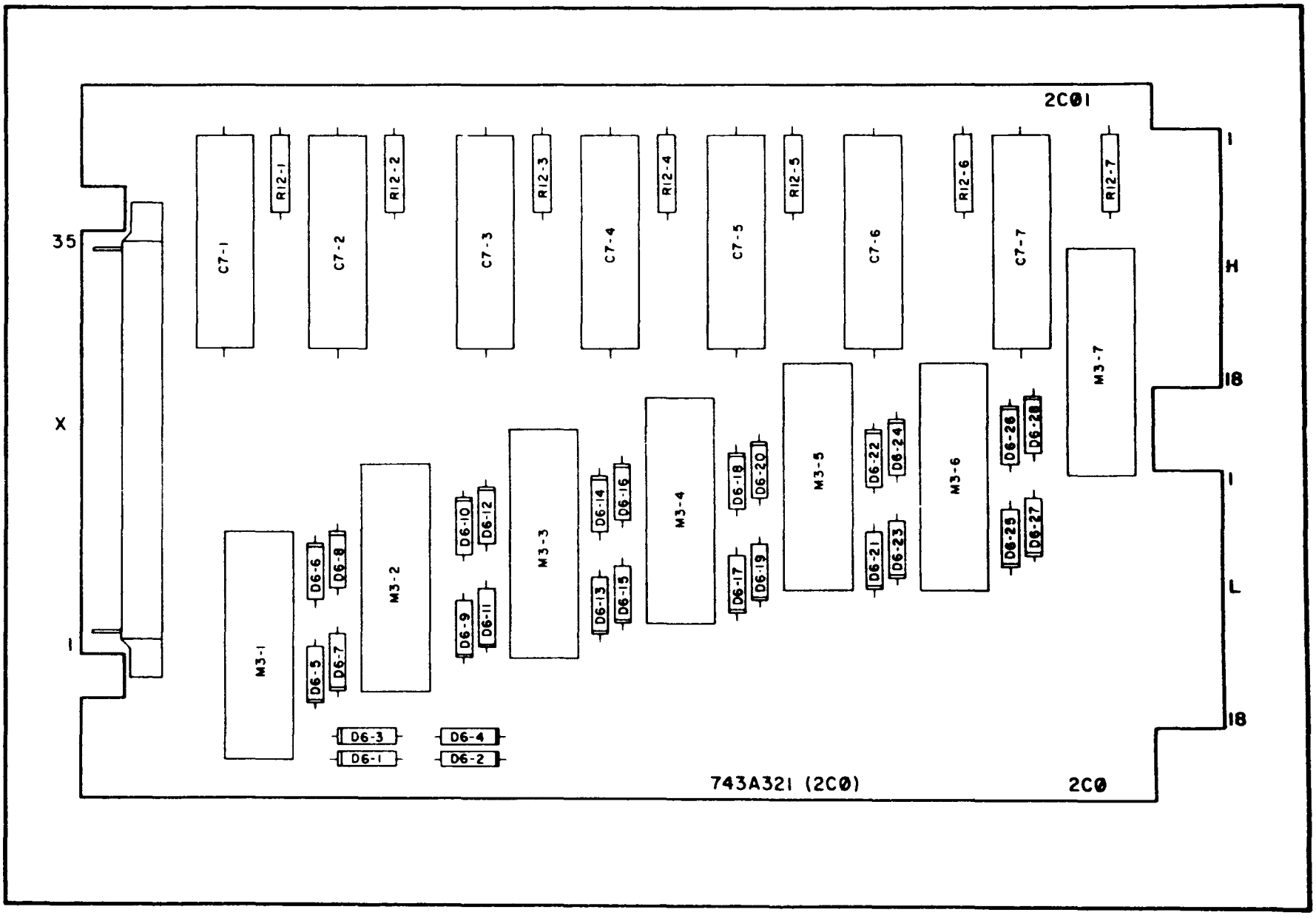


FIGURE 4. 2C01 ASSEMBLY (REF. DWG. 743A321, SUB 9)

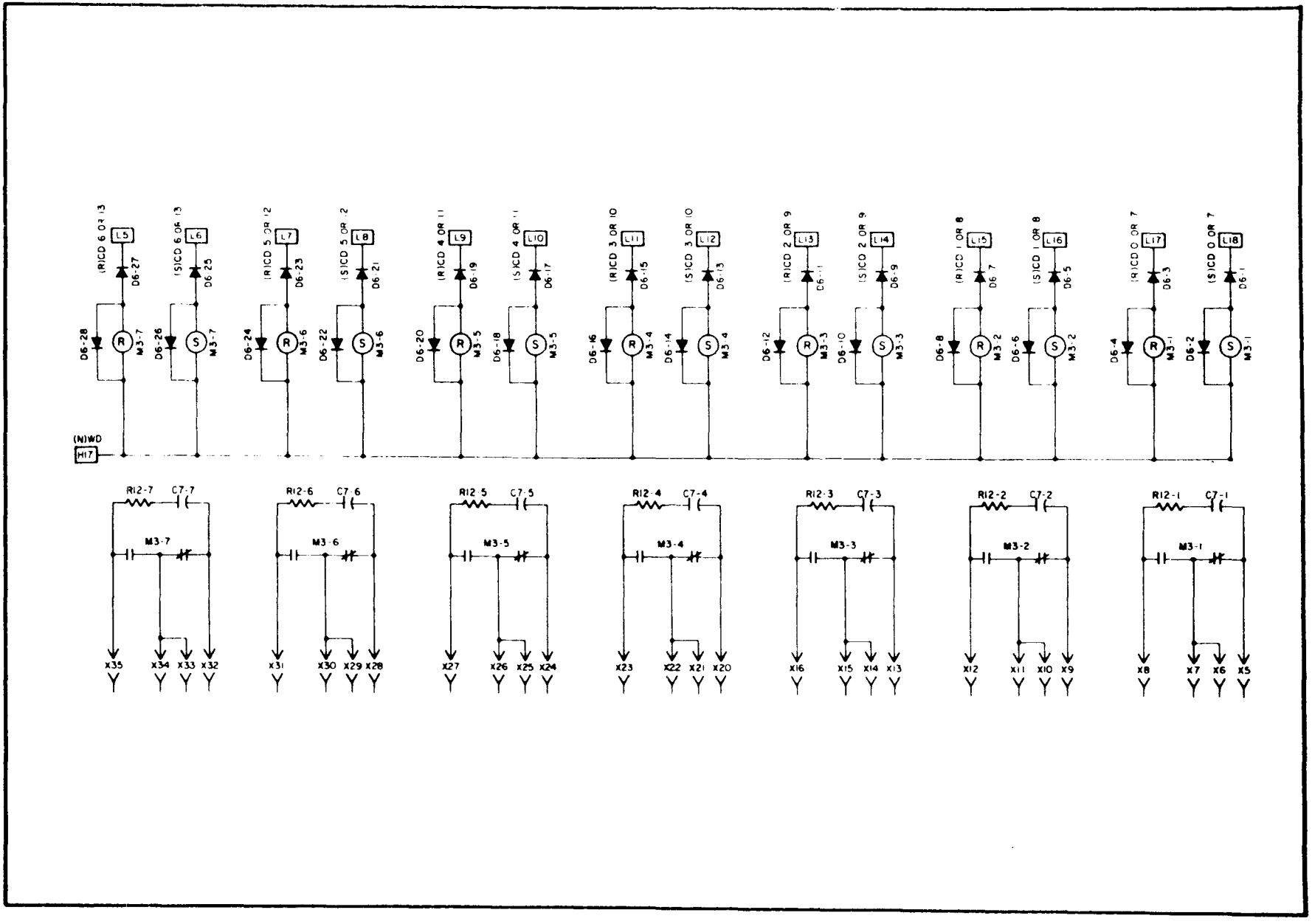


FIGURE 5. 2C01 SCHEMATIC (REF. DWG. 743A321, SUB 9)

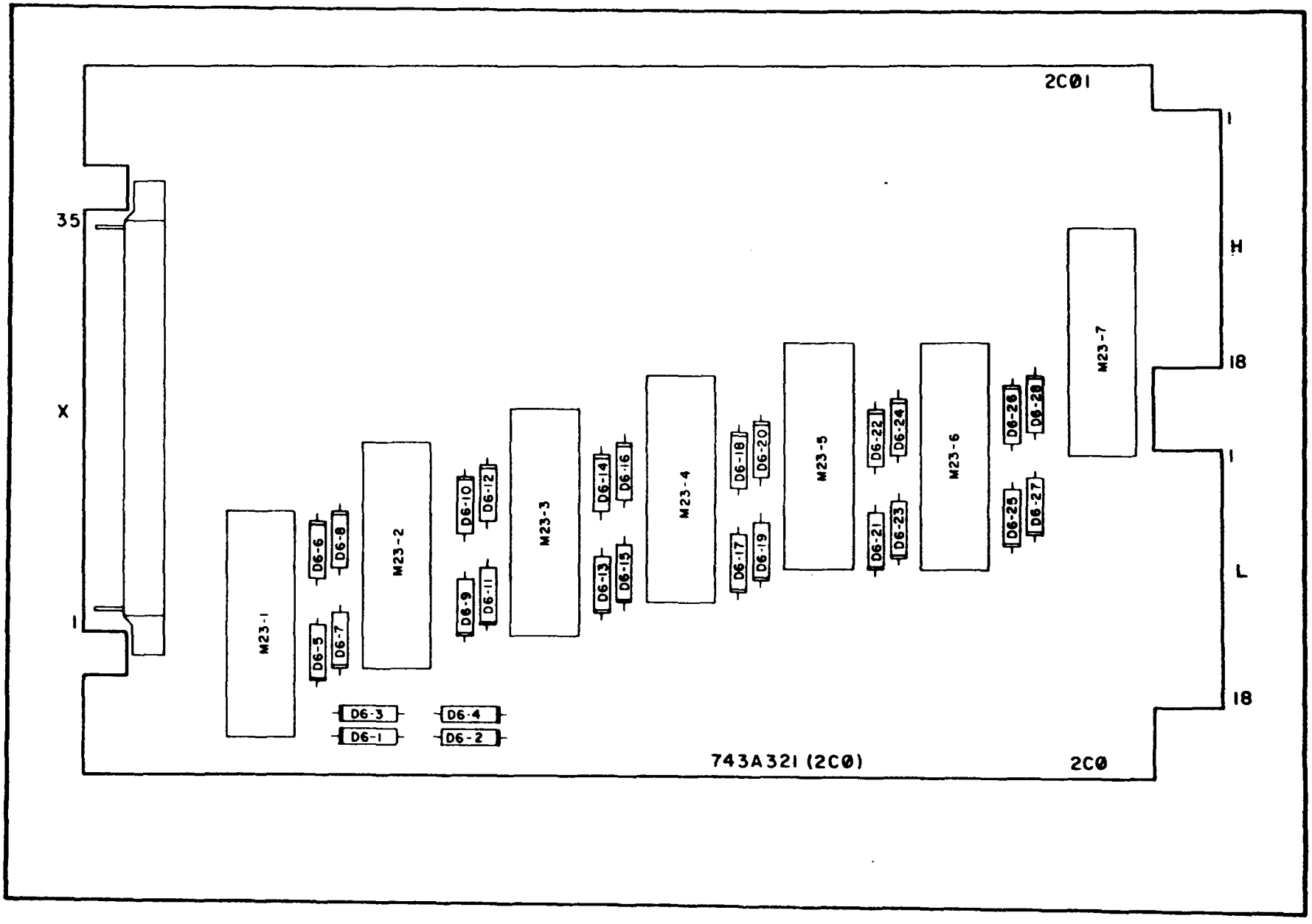


FIGURE 6. 2CO2 ASSEMBLY (REF. DWG. 743A321, SUB 9)

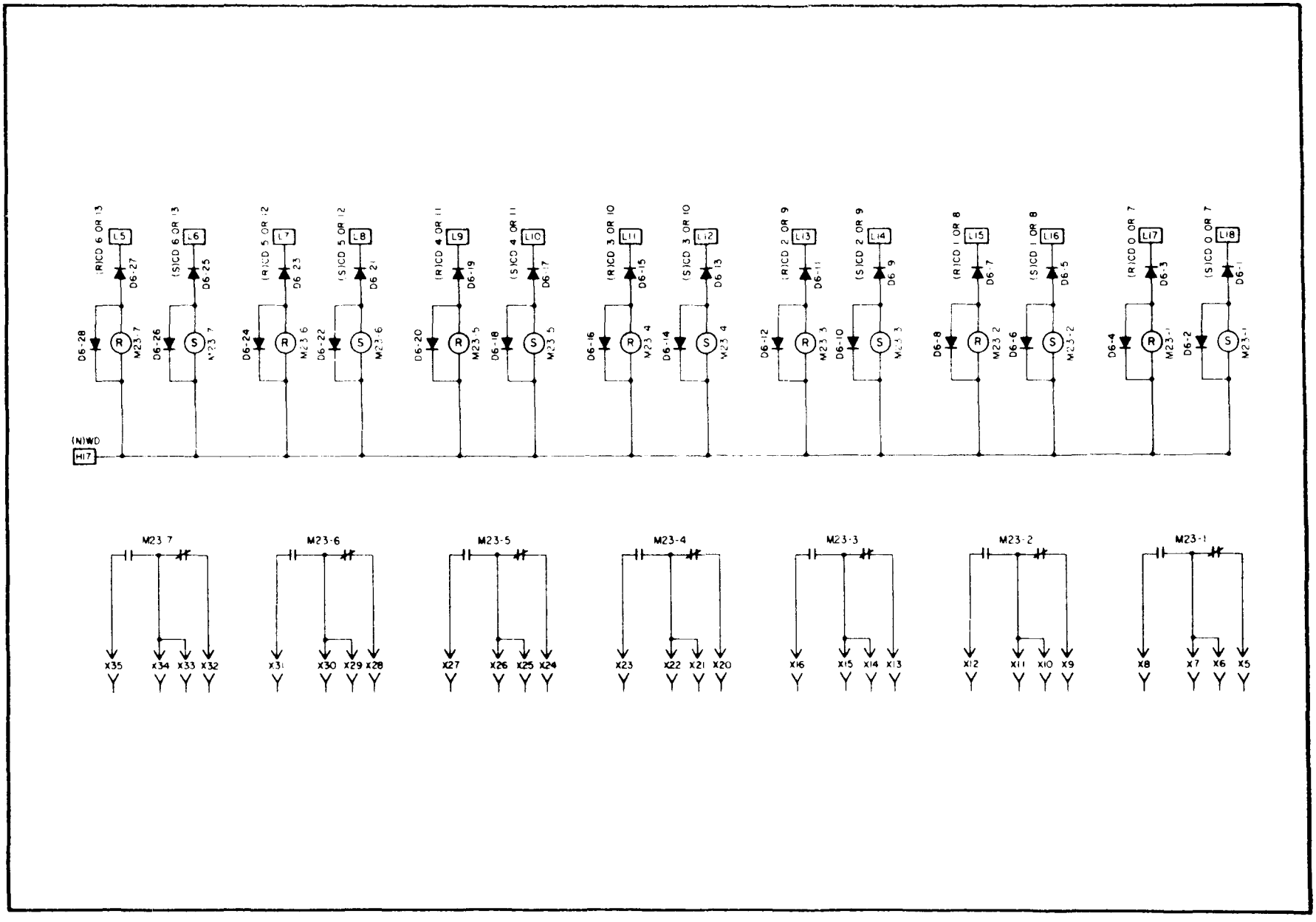


FIGURE 7. 2CO2 SCHEMATIC (REF. DWG. 743A321, SUB 9)

4CT1 - COUNTER MODULE

GENERAL DESCRIPTION

This module is used to provide a 14 bit binary counter with output buffer stages for counting the voltage-to-frequency converter output pulses in the analog input subsystem. The module contains 14 identical counter elements, each being connected to an output buffer. An application block diagram is shown in Figure 1.

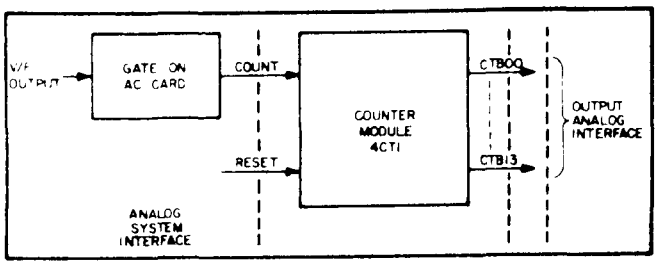


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The input to the counter requires a 0 Pulse (PSC) for advancing the counter. The maximum pulse rate is 1 MHz. The reset input requires a logical "zero" (PSC) for resetting the counter.

Output Capabilities

The output provides a conducting path to PSC for bits which are "zero" and a blocked path to PSC for bits which are "one".

Power Requirements

+26 V, ± 4 V, 450 mA max.

CIRCUIT DESCRIPTION

Each counter stage consists of two NAND gates connected in a flip-flop fashion and a capacitive coupling network (CC). The complement of the output is obtained at Pin 11 of the modified NAND package and is connected to the output buffer stage which is a NAND gate contained in a slow NAND package. The feed-forward signal is obtained at Pin 12 of the modified NAND package and it is fed to the input of the following stage. The input to a counter stage is at Pin 3 of the coupling circuit (CC). The output of the buffer stage goes to the cathode of a coupling diode.

In addition to the counter and buffer stages the card contains zener diode power supplies for the NAND gates in the modified NAND circuits and clamping voltages for the coupling network circuits. In addition to these zener diode supplies, a 6 V unregulated potential divider supply is provided for the NAND gates within the slow NAND packages.

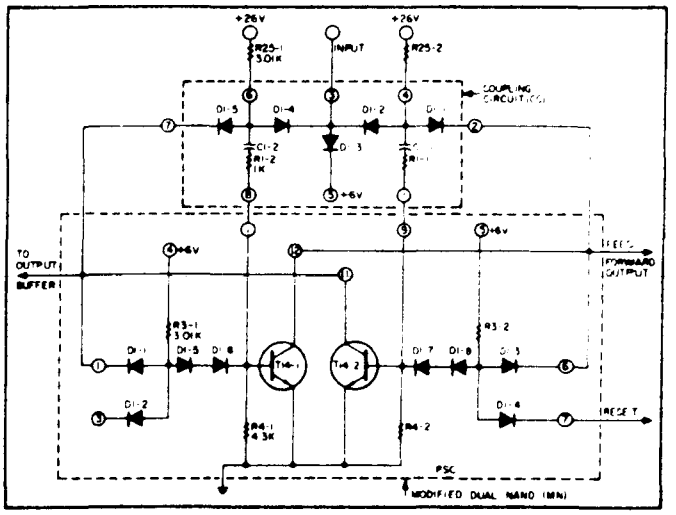


FIGURE 2. COUNTER CIRCUIT - SINGLE STAGE

The circuit diagram of a single stage of the counter is shown in Figure 2. Assume that transistor T14-1 is conducting and transistor T14-2 is blocked. Because of the flip-flop connection, the base of transistor T14-2 is pulled to ground (PSC). The base of transistor T14-1 is at a positive potential, determined by the voltage drop on resistor R4-1, as the current path from + 6 V (Pin 4) to PSC will be through R3-1, D1-5, D1-6 and R4-1.

Capacitor C1-2 will be charged so that its terminal toward the base of transistor T14-1 will be negative with respect to the terminal facing the input to the counter.

* * *

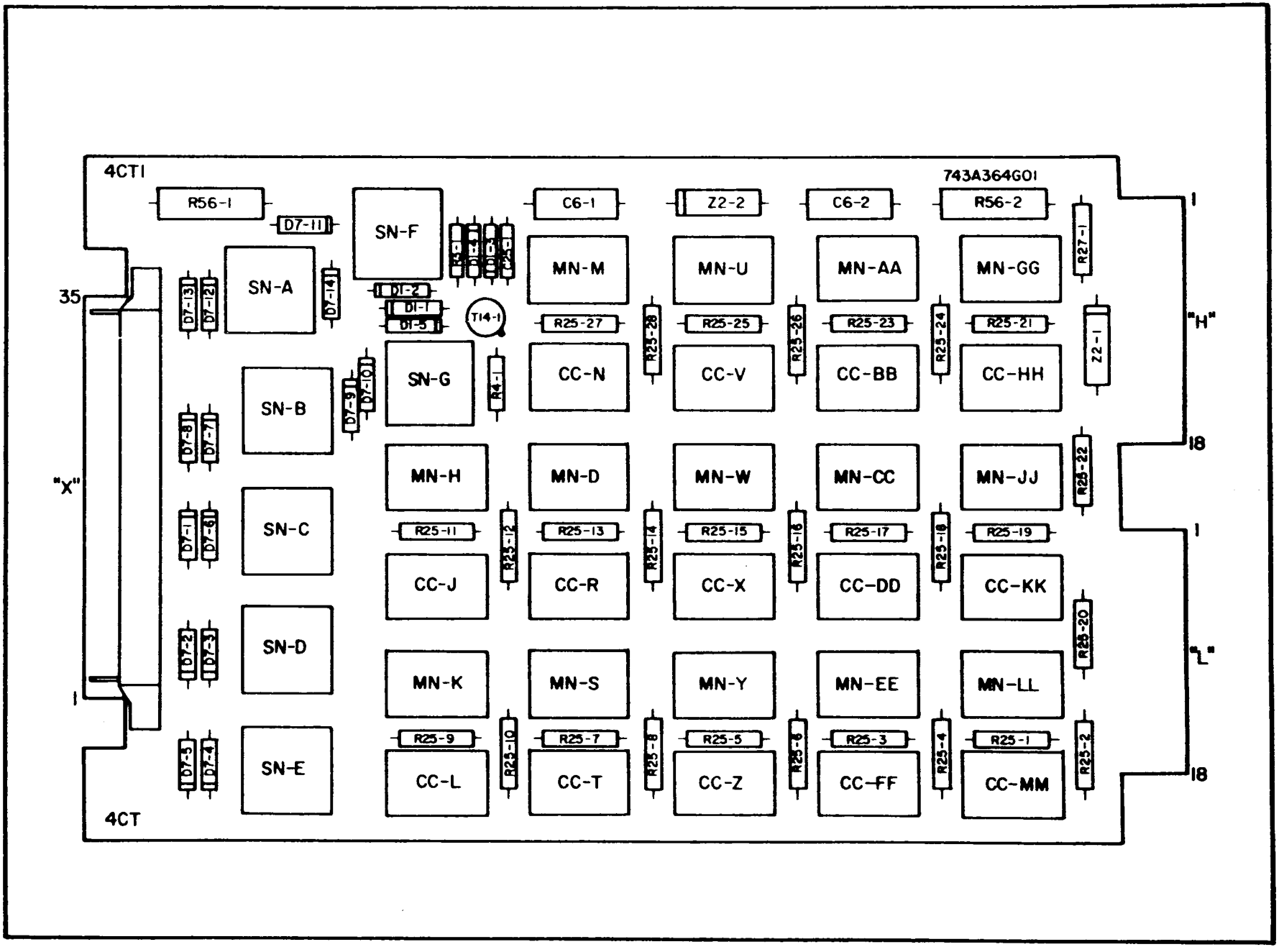


Figure 3. 4CTI Assembly (Ref. Dwg. 743A364, Sub 13)

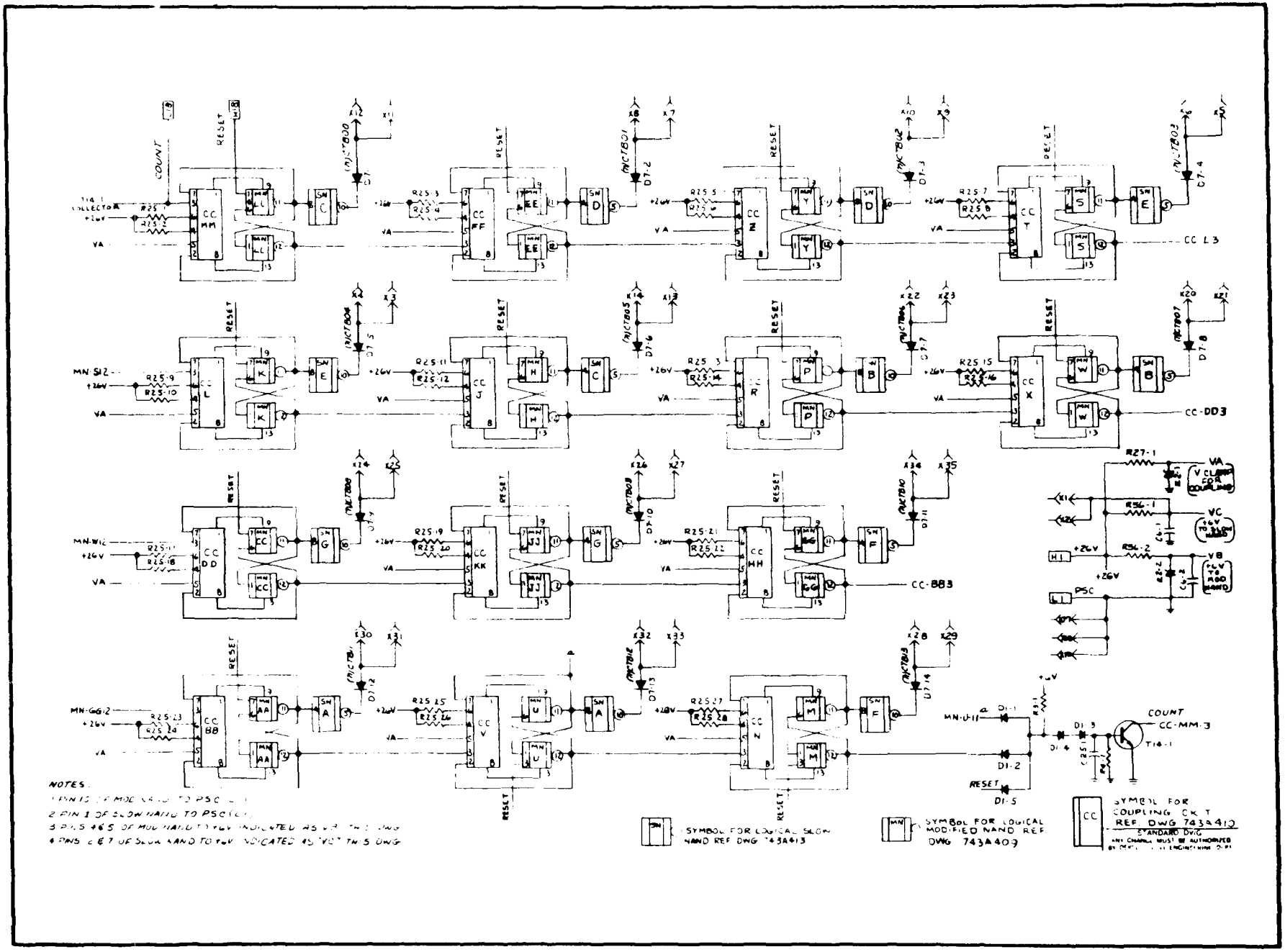


Figure 4. 4CT1 Schematic (Ref. Dwg. 743A364, Sub 13)

4DE1 - DOCUMENT CHANNEL DRIVER

GENERAL DESCRIPTION

The 4DE1 document channel driver card is used as the data buffer between the I/O interface and the paper tape punch interface panel. The module contains nine buffer circuits to hold computer output data and nine current amplifiers to drive the tape punch solenoids. The control circuit on the module synchronizes the transfer of the nine stored data bits to the punch solenoids. The block diagram in Figure 1 shows the application of the 4DE1 card in relation to its associated equipment.

CIRCUIT SPECIFICATIONS

Input Requirements

- Data output from I/O interface; a logic "zero" of 1.1V maximum, and a logic "one" of 4.0V minimum.
- Channel select pulse of 11.0V minimum for 4 μsec.
- Punch feedback trigger pulse of 8.0V minimum peak-to-peak.

Output Capabilities

- Interrupt to computer of +28V dip to 0V for a minimum of 180 μsec.
- Data to tape punch solenoids via a 1A nominal current which energizes the solenoids.
- Motor control via a 28V return signal.

Power Requirements

The 4DE1 card receives power from the +28Vdc, 7A power supply in the punch interface panel.

CARD EDGE MNEMONIC BREAKDOWN

Mnemonic	35 Pin ELCO
Bit 5	X15
Bit 6	X14
Bit 7	X13
Bit 8	X12
Bit 9	X11

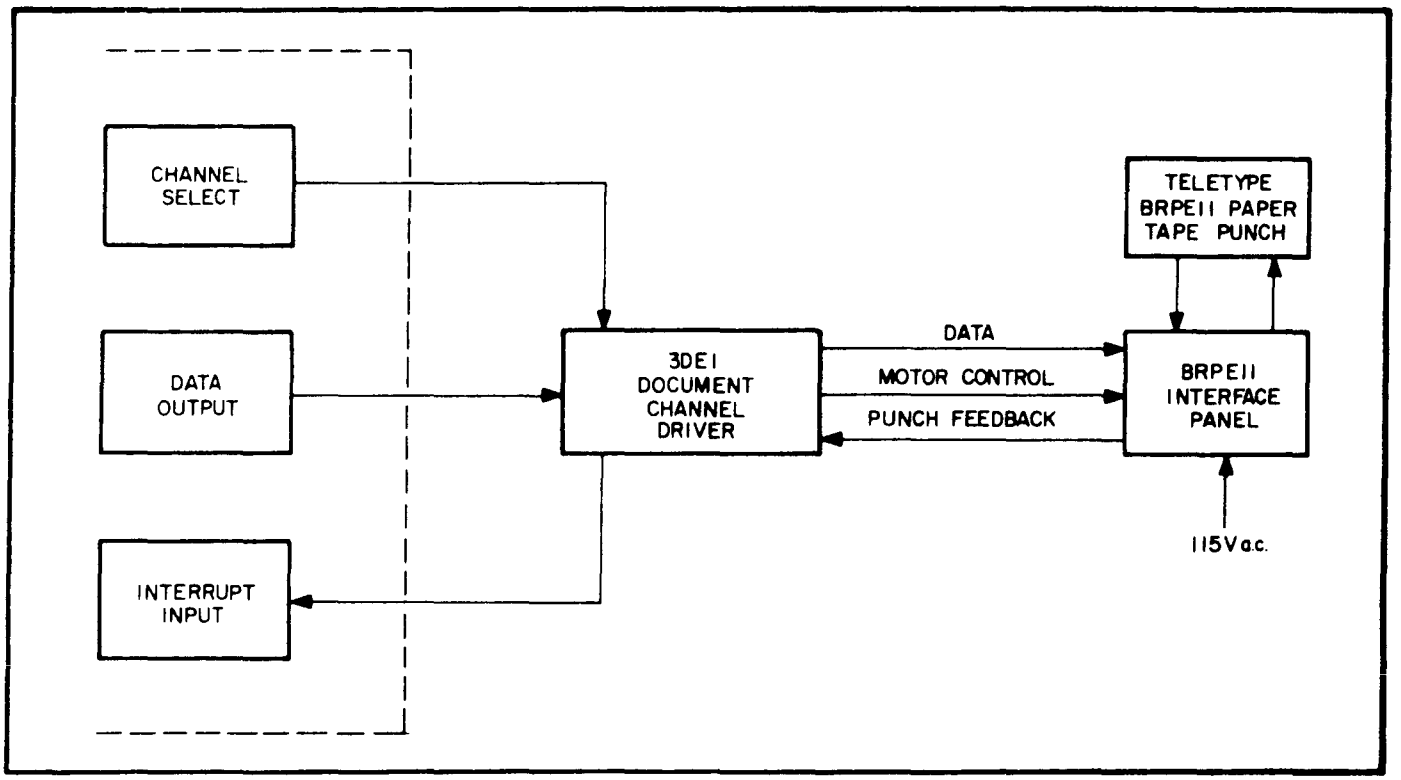


FIGURE 1. APPLICATION BLOCK DIAGRAM

Mnemonic	35 Pin ELCO
Bit 10	X10
Bit 11	X9
Bit 12	X8
Bit 13	X7
TRIG.	X34
TRIG. RTN.	X32
INT.	X17
INT. RTN.	X18
MOTOR ON	X35
+28V	X6
28V RTN	X20

For descriptive purposes the schematic has been divided into 3 circuits which are shown in Figures 2, 3 and 4. The complete schematic (dwg. 845A331, sh. 8) is included as part of this document.

The circuit in Figure 2 contains a pulse shaping network and one memory element. Transistor T24-12 and its base circuitry is the pulse shaping network (network 1) while SCR S1-10, with its gate and cathode circuitry, make up the memory cell. The input to network 1 is the feedback pulse from the tape punch magnetic pickup coil; the output is a current pulse from the collector of transistor T24-12. The inputs to the memory cell are: the current pulse output of network 1, SCR S1-9's gate drive, and transistor T7-1's base drive. The memory cell output is SCR S1-10's anode current.

The quiescent conditions of the circuit in Figure 2 are:

1. SCR S1-9 and SCR S1-10 are in the non-conducting mode.

2. Transistor T7-1 is saturated.

The sequence of events for activating this circuit are:

1. Computer output data sets SCR S1-9 by applying gate drive.

2. "Trigger Input" arrives and sets SCR S1-10 by applying gate drive through transistor T24-12.

3. Transistor T7-1 is switched from saturation to cut off by depriving T7-1 of base drive.

4. SCR S1-9 and SCR S1-10 are switched off by interruption of their current path to ground (T7-1 is cut off for 180 μsec).

During periods when the circuit is not cycled by computer output data, it will ignore incoming "trigger input" pulses.

A second function of this circuit is to prevent data loss by ignoring "trigger input" pulses until the tape punch motor is up to approximately 75 percent speed. Since the minimum voltage input to saturate transistor T24-12 is 3.0V, and the voltage amplitude of the "trigger input" is dependant on the tape motor speed, the circuit acts as a voltage tachometer whose output is zero below 75 percent motor speed and full current above 75 percent motor speed.

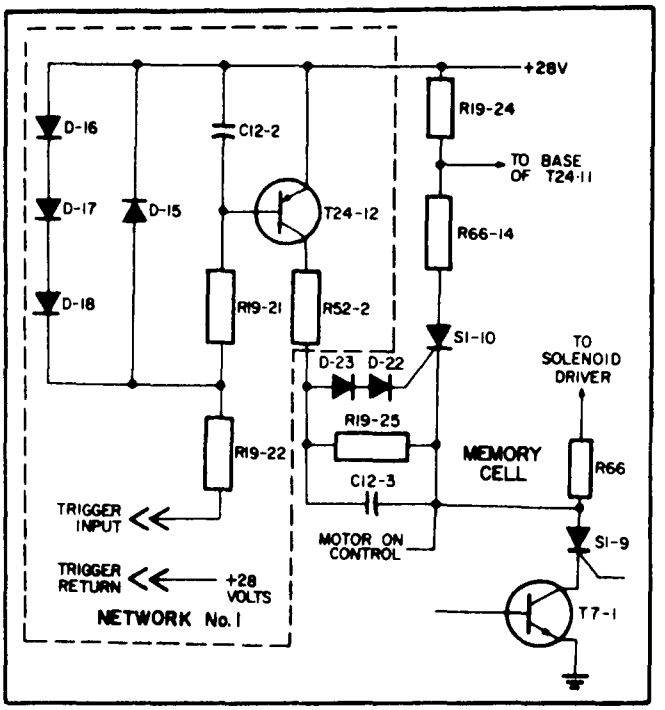


FIGURE 2. PULSE SHAPING NETWORK & 1 MEMORY CELL

Figure 3 shows a unijunction transistor timing circuit used in a time delay configuration. The input to this circuit is current through resistors R66-14 and R19-24; the output is a ground potential on transistor T5-1's collector for approximately 180 μsec.

The quiescent conditions of this circuit are:

1. Transistor T24-11 is cut off.

2. Unijunction transistor S2-1 is non-conducting.

3. Transistor T5-1 is cut off.

The sequence of events for activating this circuit are:

1. Transistor T24-11 is switched from cut off to saturation by base drive current in resistors R66-14 and R19-24.

2. After a time delay of 4.5 msec, unijunction transistor S2-1 saturates for approximately 180 μsec, thus biasing transistor T5-1 into conduction for the same time period.

3. Transistor T24-11 is deprived of its base drive and is cut off.

4. The delay time of 4.5 msec between the input and output is controlled by the RC time constant of capacitor C32-1, resistor R66-12 and potentiometer M12-1. Resistor R30-1, resistor R27-1 and diode D-14 insure that all time delays between input and output are of equal value. Resistors R52-1 and R12-1 provide the correct impedance for the 180 μsec interrupt input signal to the computer. R82 provides a path for the leakage current of T24 during cutoff.

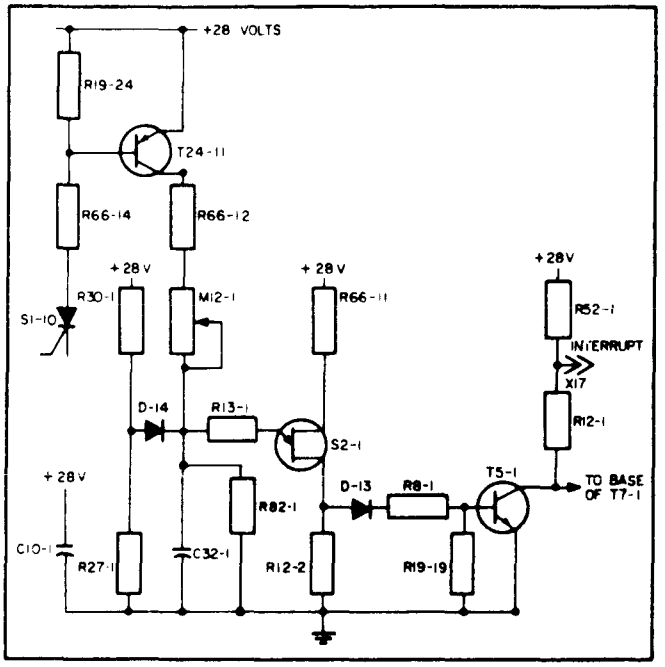


FIGURE 3. UNIJUNCTION TIMINING CIRCUIT

The circuit in Figure 4 consists of three current switches and a data buffer. The circuit holds computer output data, current amplifies it and outputs this data to the tape punch solenoids. Inputs are: a positive 28V on the anode of diode D-21, a ground potential on the anode of diode D-10, and an open circuit across terminals H9 and L1 accompanied by an 11.0V, 4.0 μsec pulse across terminals L2 and H3.

The quiescent conditions of this circuit are:

1. **Transistor T24-10 is saturated.**

2. **Transistor T7-1 is saturated.**

3. **SCR S1-1 is non-conducting.**

4. **Transistor T24-1 is cut off.**

The sequence of events for activating this circuit are:

1. Computer output data sets SCR S1-1.

2. Transistor T24-10 is cut off.

3. Transistor T24-1 is saturated and pulls current through the tape punch solenoids.

4. Transistor T7-1 is cut off interrupting the current path to reset SCR S1-1 and cut off the current to the punch solenoids.

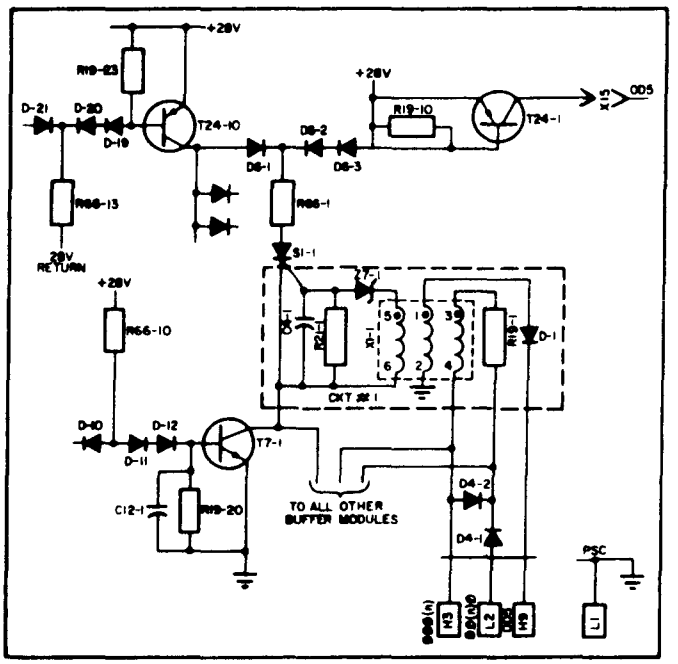


FIGURE 4. CURRENT SWITCHES & DATA BUFFER

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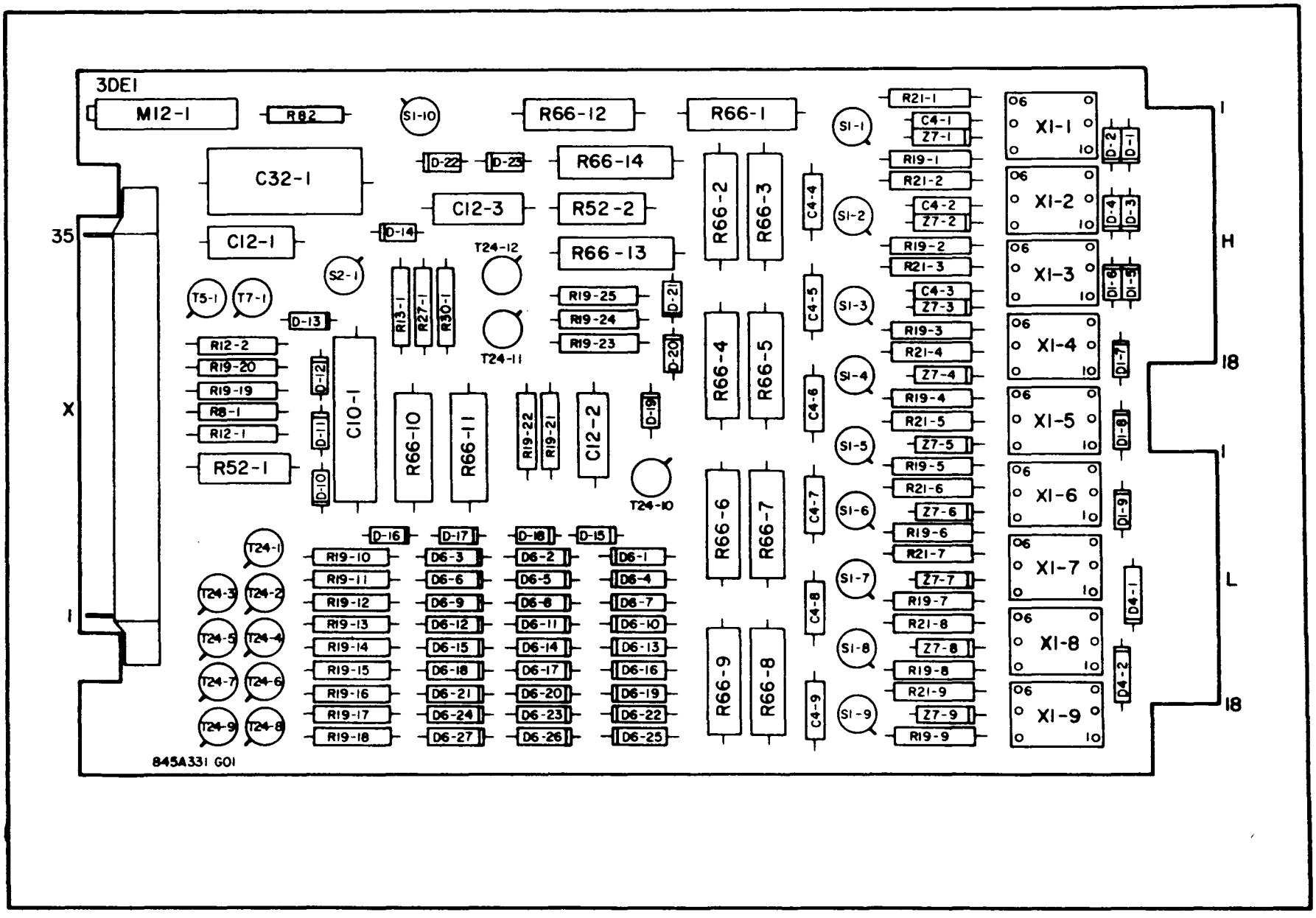


FIGURE 5. 4DE1 ASSEMBLY (REF. DWG. 845A331, SUB 3)

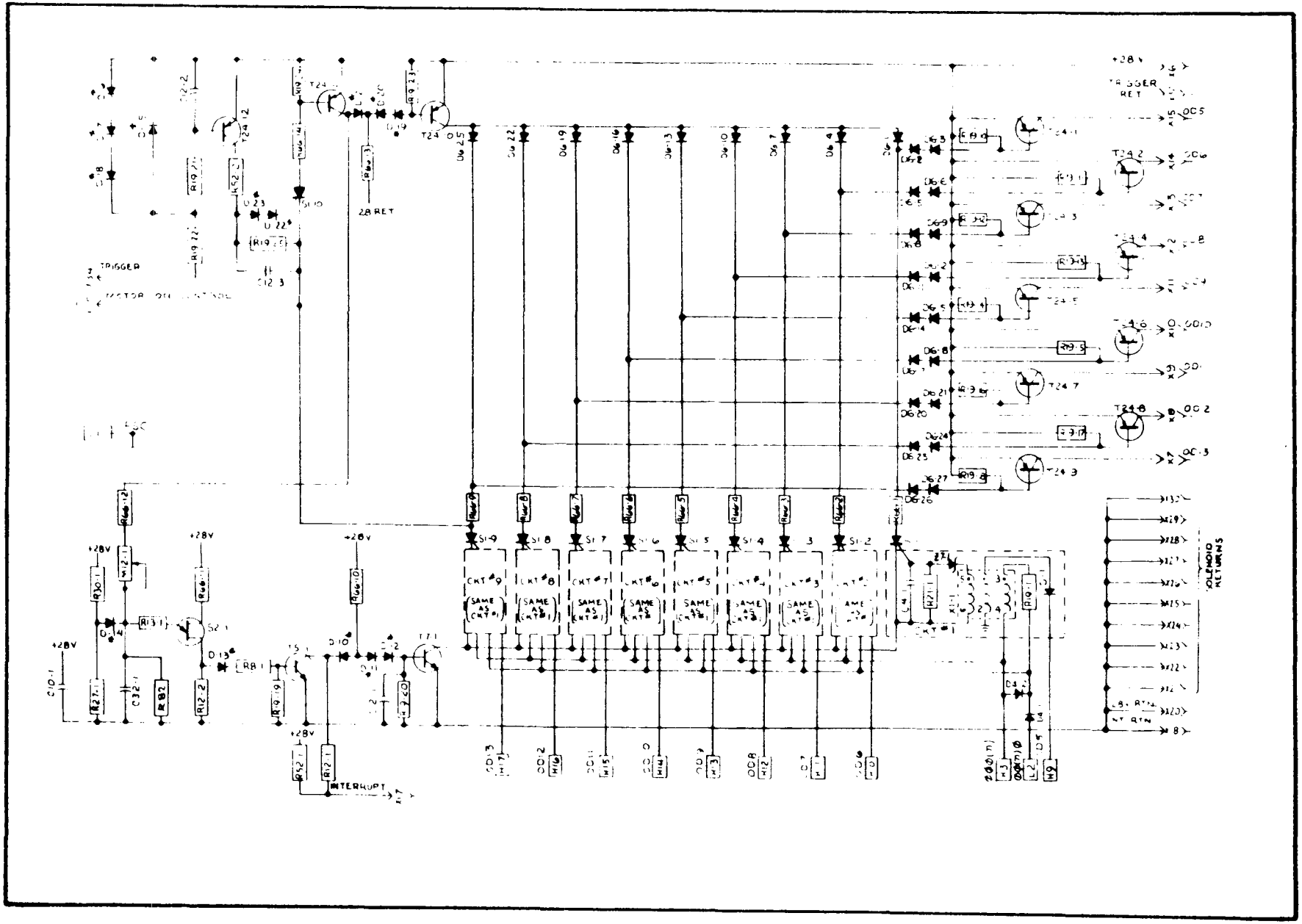


FIGURE 6. 4DE1 SCHEMATIC (REF. DWG. 845A331, SUB 3)

1PL4/1PL5 - PHASE LOCKED OSCILLATOR

GENERAL DESCRIPTION

The phase locked oscillator card is used in the analog input subsystem. Its purpose is to provide a stable 120 cycle square wave output which is locked in phase with the 60 cycle power line frequency. When energized, the phase locked oscillator attains a stable frequency in about 1 min, and follows long term line frequency variations of 58 to 62 Hz (48 to 52 Hz for 1PL5). The 1PL4 card is used for 60 Hz line frequency, and the 1 PL5 for 50 Hz. An application block diagram is shown in Figure 1.

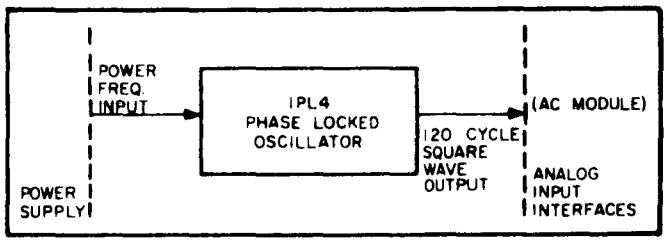


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The power frequency input requires a 6.3V, ± 15% sine wave ac voltage input.

Output Capabilities

The 120 Hz square wave output provides zero volts (PSC) for the negative portion of the pulse and approximately + 15 V for the positive portion of the pulse. The length of the positive portion is equal to the negative portion. The output frequency is phase locked with the power line frequency input.

Power Requirements

Power input is + 26 V, ± 15% dc, 57 mA max.

CIRCUIT DESCRIPTION

The phase locked oscillator circuit can be separated into the functional elements as shown in Figure 2.

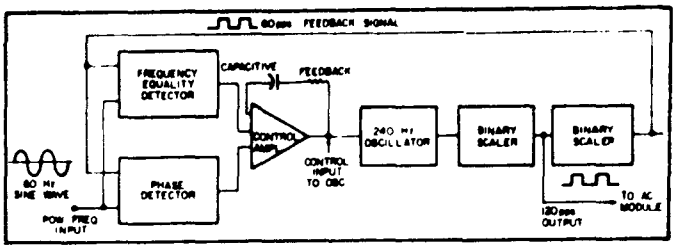


FIGURE 2. PHASE LOCKED OSCILLATOR BLOCK DIAGRAM

These circuit elements are interconnected in a feedback configuration which attempts to maintain the output in a fixed frequency and phase relationship with the 60 Hz input.

The operation of the circuit elements is described in the following:

Unijunction Transistor Oscillator and Binary Scalers

The circuit diagram of the oscillator and scaler circuit is shown in Figure 3.

The oscillator circuit uses a unijunction transistor oscillator. The output frequency is dependent on the control input voltage. An adjustment is provided (potentiometer M13-2) for initial calibration of the oscillator to 240 Hz. (At control input voltage of 7.5V.)

The 240 Hz oscillator output is scaled by a binary scaler which basically is a binary counter stage (flip-flop circuit with capacitive input coupling). The output of this scaler is a 120 Hz square wave signal which is used in the analog input system for timing.

The complement of the output is used to trigger the second binary scaler which further reduces the frequency to 60 Hz. This signal is used as a feedback signal to the frequency equality and phase detectors.

The circuits of the two binary scalers are somewhat different, since the first is triggered by the positive going pulse of the oscillator, while the second is triggered by the negative going transistion of the first scaler.

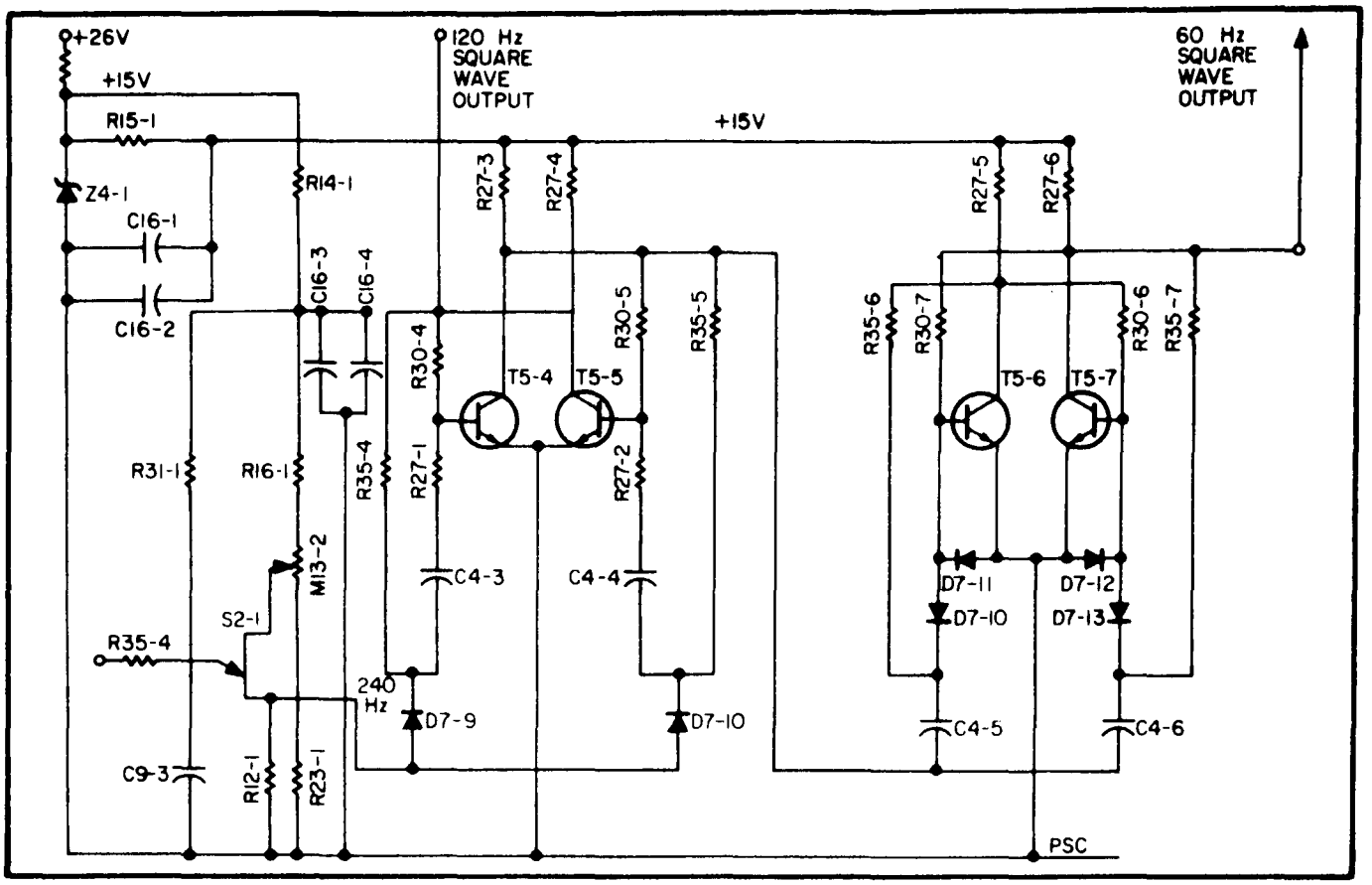


FIGURE 3. OSCILLATOR AND BINARY SCALERS CIRCUIT

Phase and Frequency Equality Detectors

The circuit diagram of these circuits is shown in Figure 4.

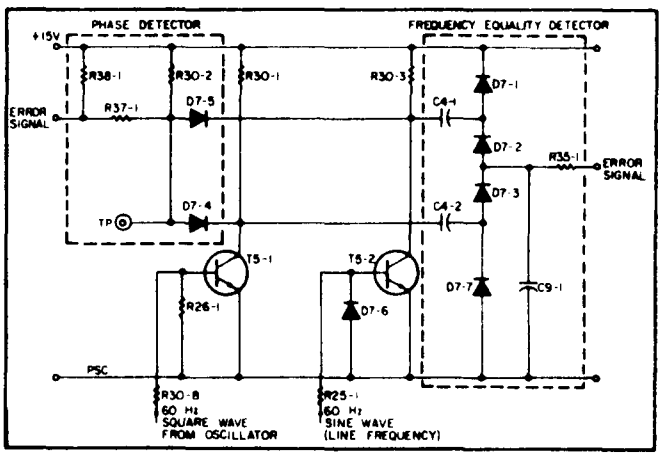


FIGURE 4. PHASE AND FREQUENCY EQUALITY DETECTOR

The output of transistor T5-2 will be square wave corresponding to the power line frequency. The output of transistor T5-1 is also a square wave but this corresponds to the oscillator frequency.

These two square waves are used by both the phase and the frequency equality detectors.

The frequency equality detector utilizes capacitors C4-1 and C4-2 – which are alternately charged and discharged through diode matrix D7-1, D7-2, D7-3 and D7-7 – and will place a charge on capacitor C9-1. The voltage on capacitor C9-1 will be proportional to the frequency difference between the oscillator and the line frequency. When the two frequencies are equal, the voltage on capacitor C9-1 should be half of the supply voltage.

For phase detection, the outputs of the two transistors are fed to a diode AND circuit (diodes D7-5 and D7-4). If the two signals are in phase, the output (on test point TP) will be a 60 Hz square wave. If the two signals are 180° out of phase, the output will be zero. Resistors R38-1 and R37-1 are used to bias the output to the proper [illegible]

Note that after the phase lock oscillator stabilizes, the 60 Hz signal will be 270° out of phase with respect to the 60 Hz line frequency. The wave shape on test point TP therefore will be a square wave pulse with 25% duty cycle.

Control Amplifier

The outputs of both the frequency equality detector and the phase detector are connected to a high gain dc amplifier with capacitive feedback.

The circuit diagram of the amplifier is shown in Figure 5.

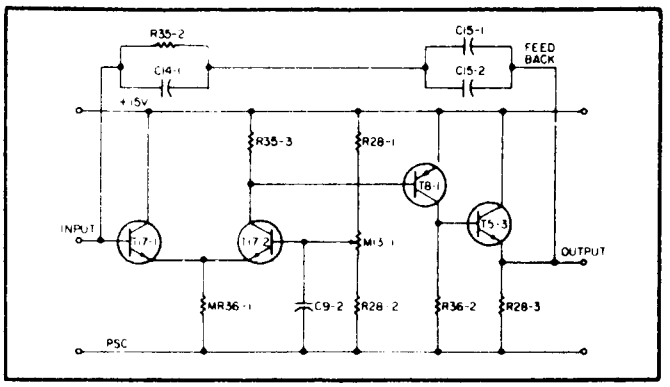


FIGURE 5. CONTROL AMPLIFIER CIRCUIT

The matched pair of transistors T17-1 and T17-2 acts as a difference amplifier. Transistor T8-1 supplies additional gain and T5-3 provides a current gain and low output impedance.

Adjustment for amplifier balance is provided through potentiometer M13-1. (Used during calibration of the 1PL card.)

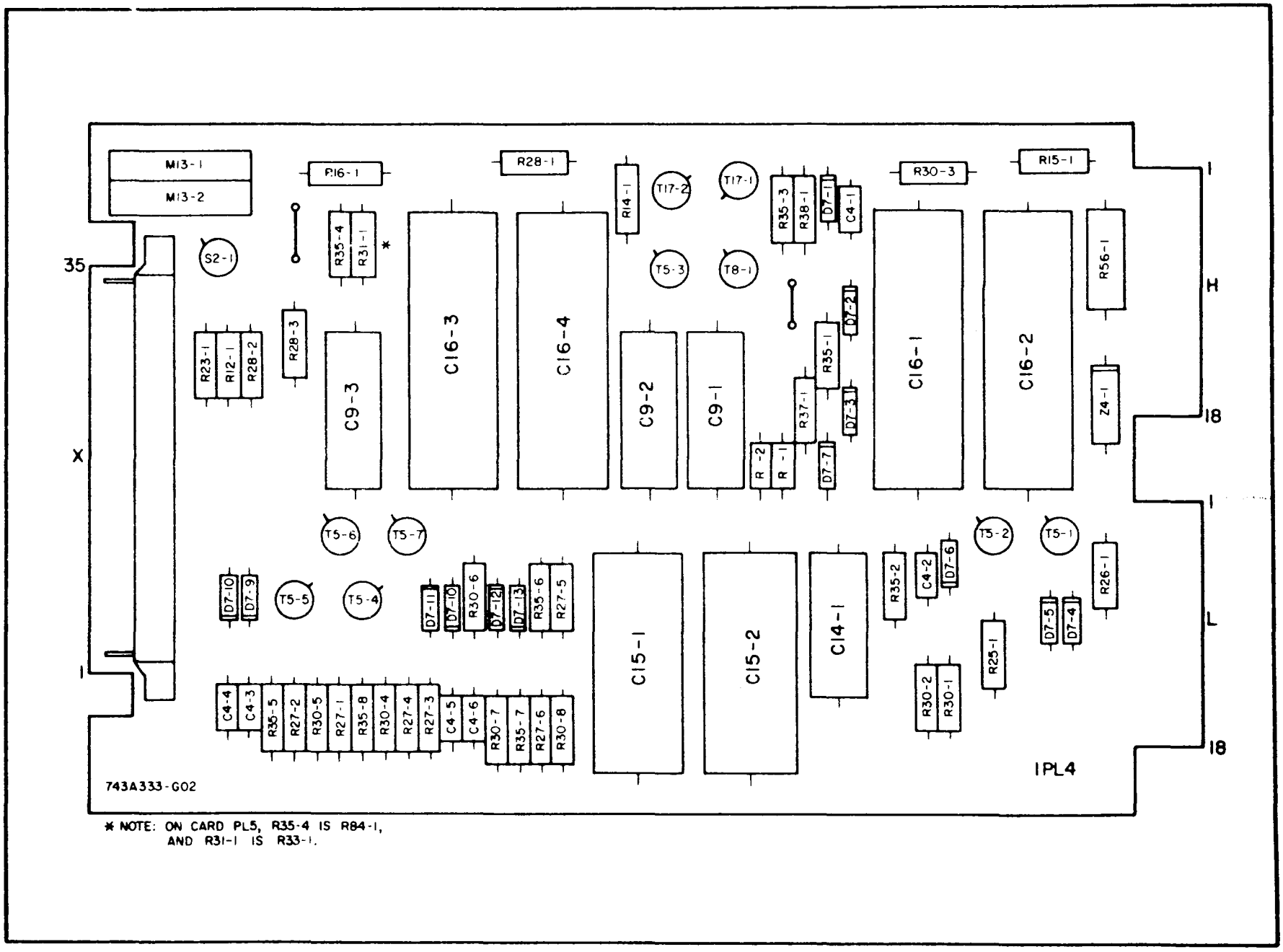
The output of the control amplifier is connected to the control input of the unijunction transistor oscillator.

1PL5 Card – 50 CPS Operation

The operation of the 1PL5 card is identical to that of the 1PL4 card. The only difference is the frequency used The input will accept 48 to 52 Hz (nominal 50 Hz) and the output will be a 100 Hz square wave which is locked in phase with the 50 Hz power line frequency.

The description of the rest of the circuits can likewise be corrected for 50 Hz operation.

* * *



* NOTE: ON CARD PL5, R35-4 IS R84-1, AND R31-1 IS R33-1.

FIGURE 6. 1PL4 1PL5 ASSEMBLY (REF. DWG. 743A333, SUB 14)

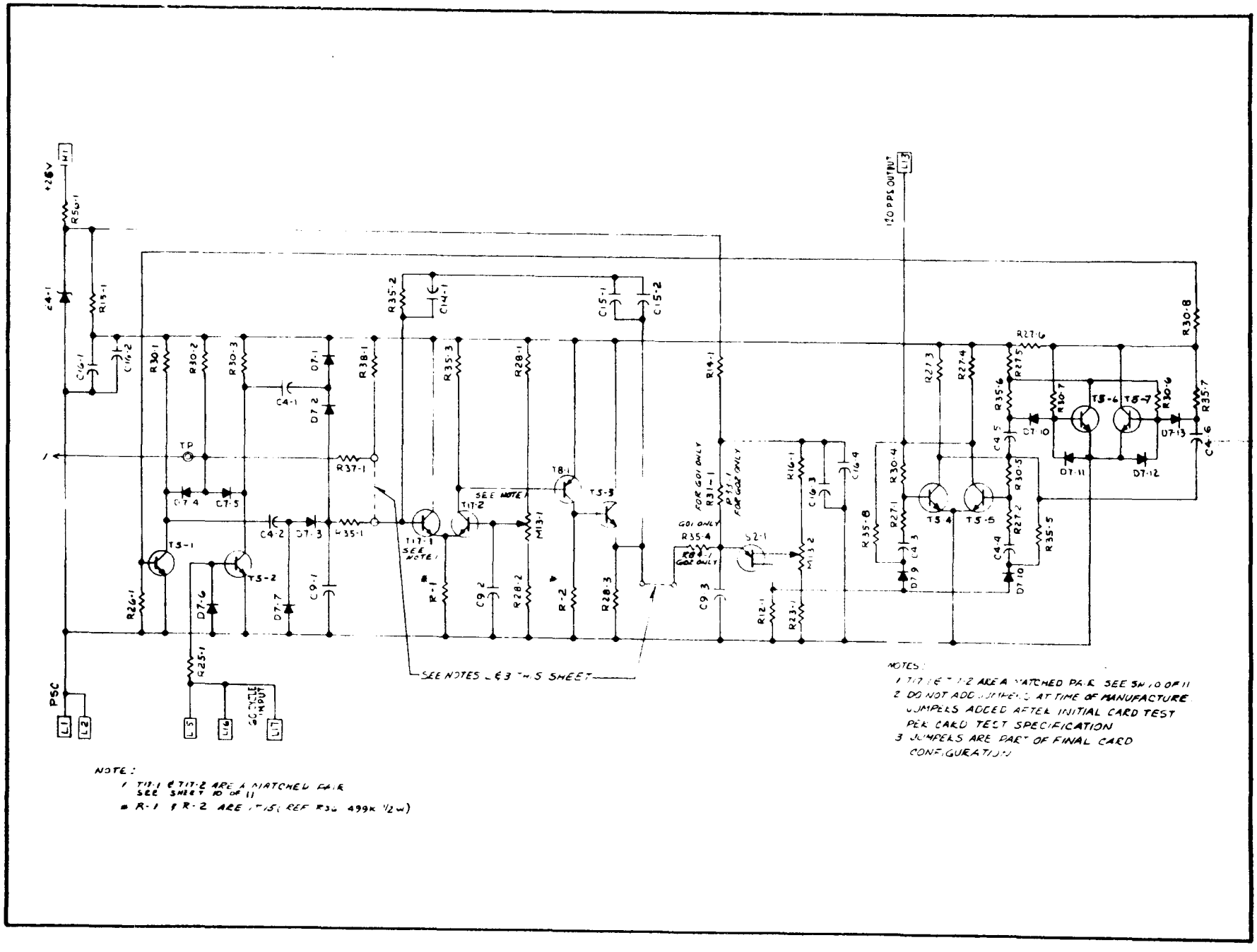


FIGURE 7. 1PL4 1PL5 SCHEMATIC (REF. DWG. 743A333, SUB 14)

2PS1 - POWER SUPPLY SWITCH MODULE

GENERAL DESCRIPTION

The circuits on this module are used to reset SCR's in the input-output subsystem. There are 4 identical circuits on a module.

Figure 1 is a block diagram showing a typical application of the power supply switch.

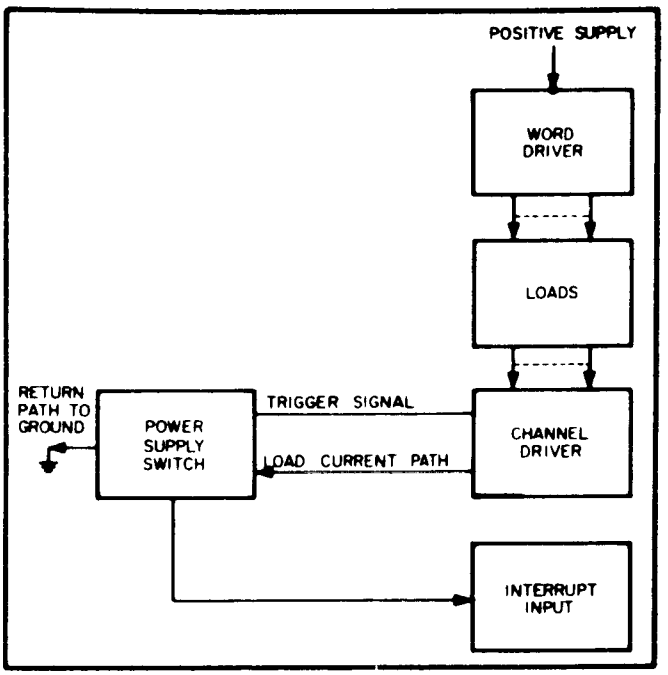


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The power supply switch trigger is clamped at approximately a one volt level until the switch is reset.

Output Capabilities

The maximum current that can be carried by the switch output is 850 mA. The output is in a conducting state when there is no trigger signal. After the trigger signal, there is a time delay of 1 to 9 msec (adjustable) before the output becomes non-conducting and supports 26 V. The non-conducting state lasts 150 to 300 μsec before reverting to conduction again.

The interrupt signal from the power supply switch goes from approximately + 26 V to + 1 V at the time the switch output blocks and back to + 26 V at the time the switch conducts again. The computer detects an interrupt when the positive change in voltage occurs.

Power Requirements

Connections to + 26 V and PSC are required.

CIRCUIT DESCRIPTION

Refer to Figure 2 which is a schematic of one of the 4 identical circuits on the module. The operation of the circuit is described in terms of a channel driver application. With none of the channel drivers selected (i.e., all SCR's are blocked), the base drive of transistor T8-1 is zero, causing it to be blocked. This means that the unijunction transistor S2-1 has no positive supply, and the timing capacitor C10-2 is discharged. Transistor T5-1 has no base drive and is blocked, allowing base drive to be provided to transistor T7-1 which is now in a state to allow conduction.

Assume the channel in Figure 2 has been selected. The detector SCR located on another card (2CB for example) and any number of the channel driver SCR's (such as on a 4CD Card) are turned on. Transistor T7-1 is in a conducting state and provides the current path to ground for the cathodes of the SCR's. The conduction of the detector SCR is the trigger signal which causes base drive to transistor T8-1. Transistor T8-1 turns on, supplying voltage to the unijunction transistor and its timing circuit. After a time delay determined by resistor R18-1, capacitor C10-2, and the adjustment of potentiometer M12-1, unijunction transistor S2-1 breaks down, producing a pulse across resistor R12-1. This causes transistor T5-1 to conduct and transistor T7-1 to block for the approximate duration of the UJT pulse. The blocking of transistor T7-1 reduces the current through the SCR's below the holding value and the SCR's turn off, that is, the SCR's are reset to the blocking state, accomplishing the main function of the power supply switch. The trigger signal is removed when the detector SCR is turned off, causing transistor T8-1 to again block. At the completion of the UJT pulse, transistor T5-1 blocks, and transistor T7-1 returns to its conducting state. The power supply switch has now recovered and is ready for the next selection of the channel.

The interrupt signal is taken from the collector of transistor T5-1. During the UJT pulse, transistor T5-1 is conducting, and the interrupt signal is near zero. At the completion of the UJT pulse, transistor T5-1 blocks, and the external interrupt signal goes to approximately + 26V. The computer recognizes this positive going signal as an interrupt.

The reason for using a unijunction transistor in the timing circuit is because it is stable and does not drift appreciably with temperature or supply voltage. The timing requirements for the power supply switch vary according to its application. The UJT time delay is variable from 1 to 9 msec to accommodate these applications.

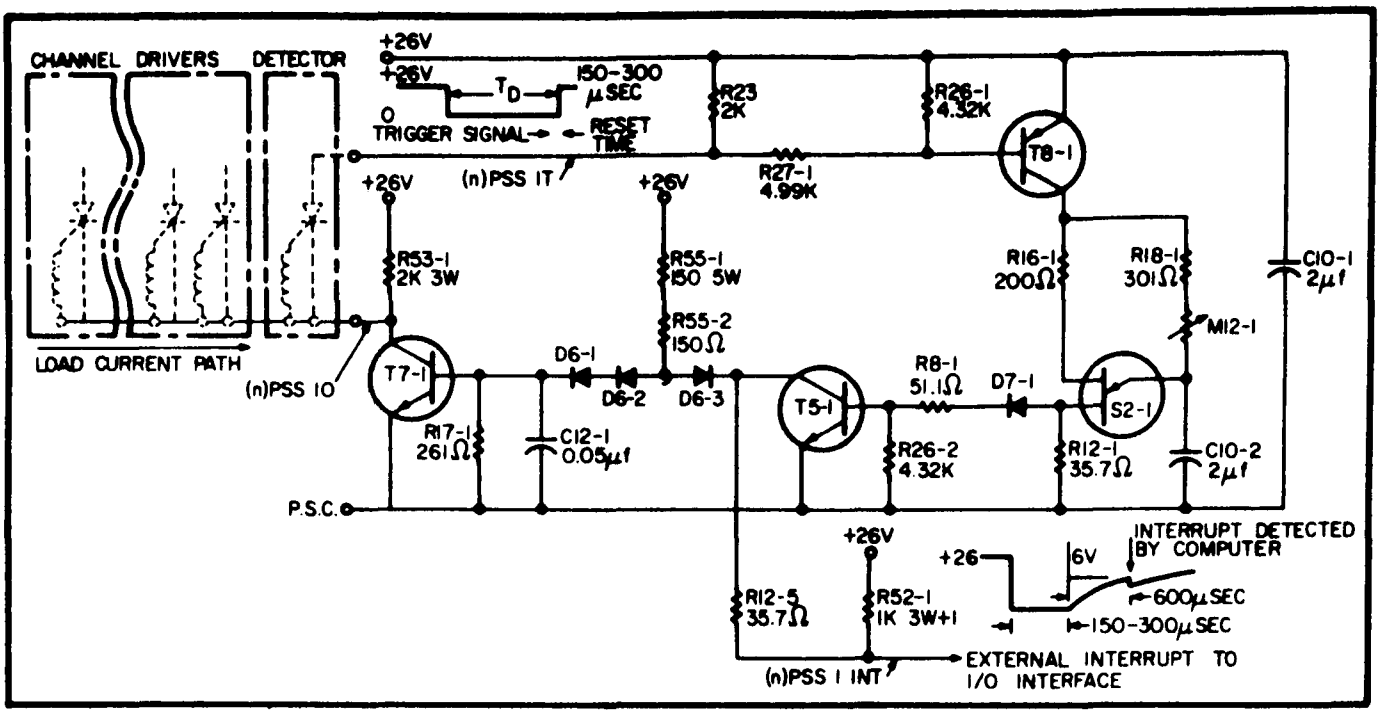


FIGURE 2. ONE POWER SUPPLY SWITCH CIRCUIT

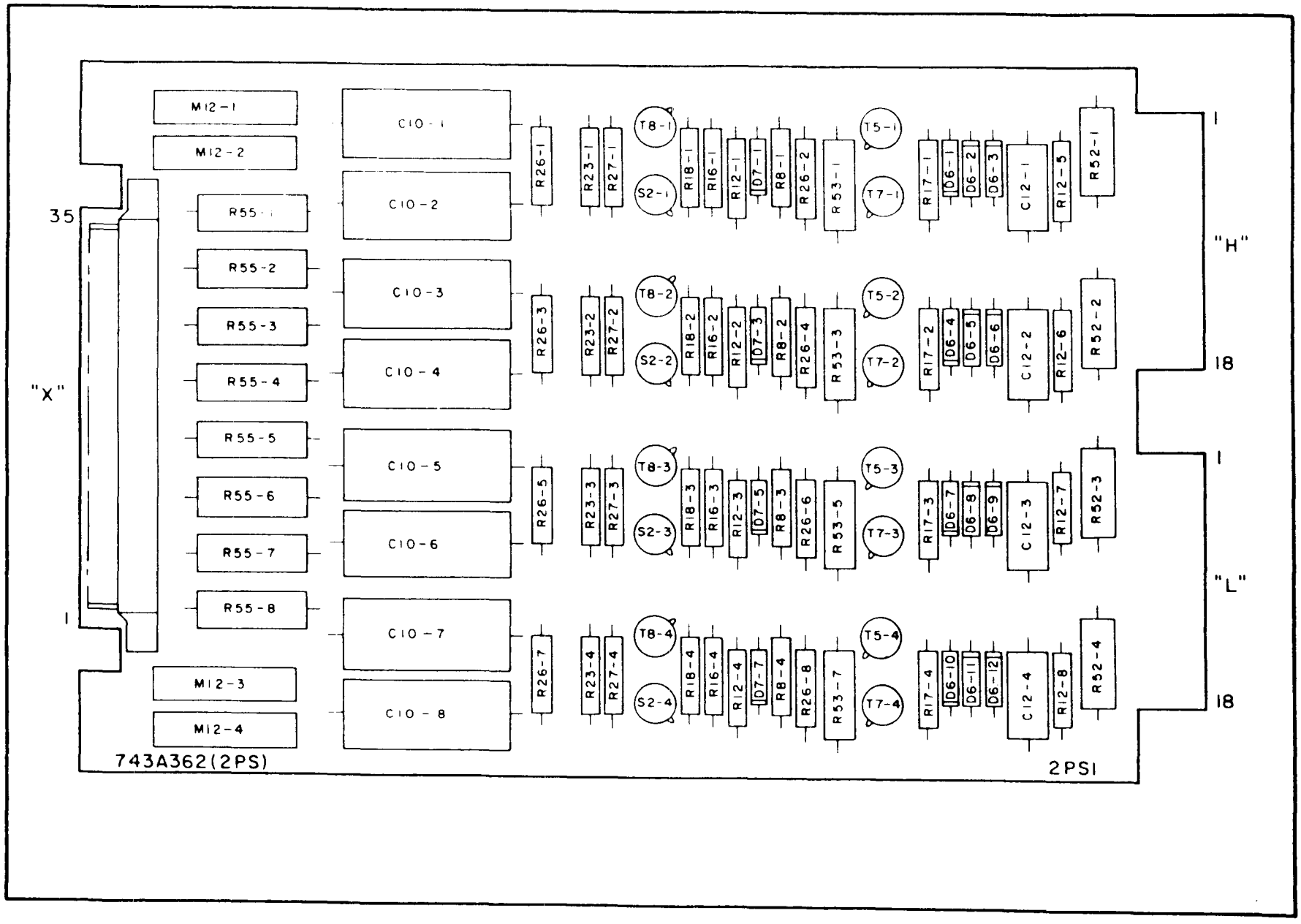


FIGURE 3. 2PS1 ASSEMBLY (REF. DWG. 743A362, SUB 6)

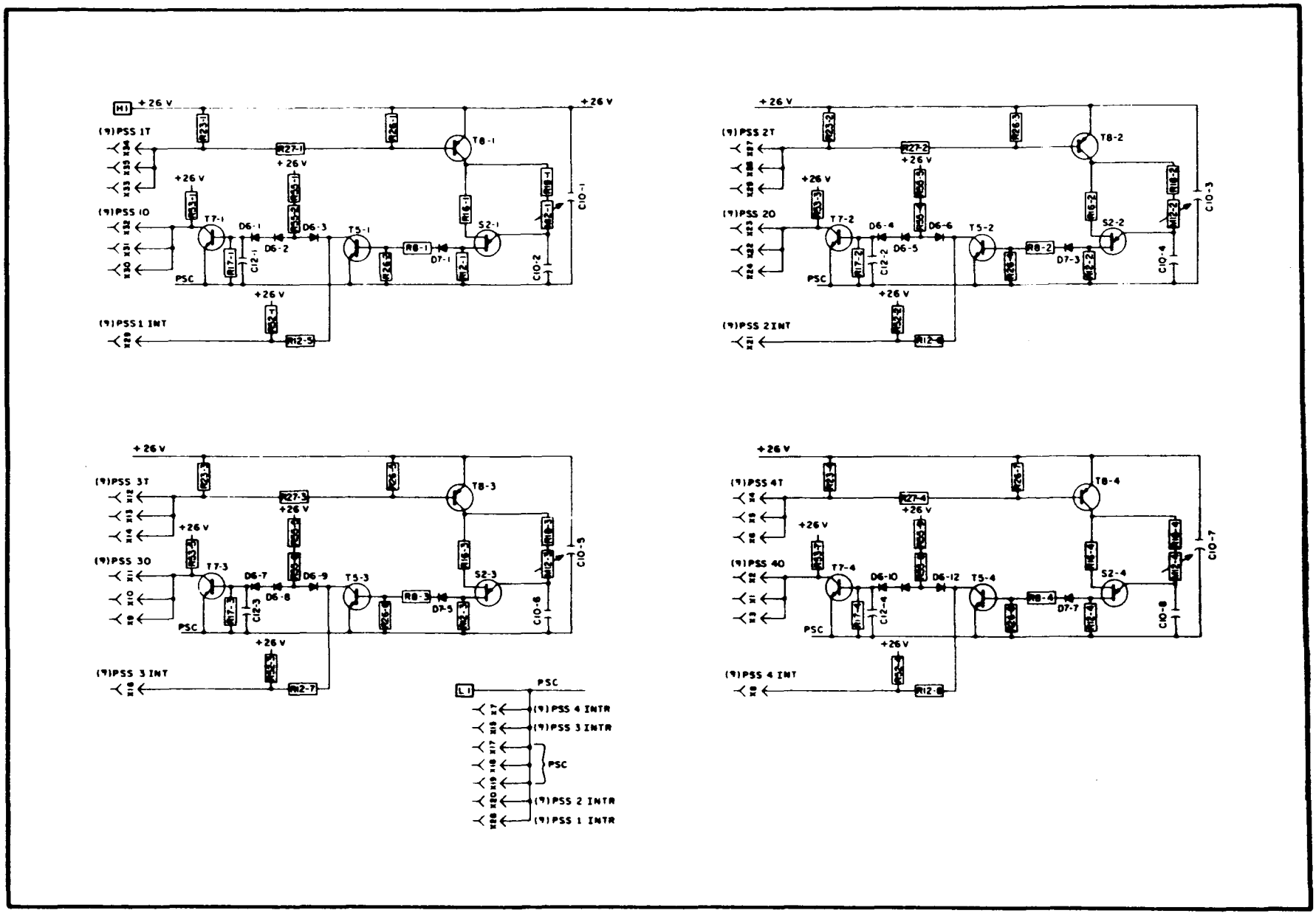


FIGURE 4. 2PS1 SCHEMATIC (REF. DWG. 743A362, SUB 6)

2RB3 - READER BUFFER MODULE

GENERAL DESCRIPTION

The 2RB module serves as a buffer between the CPU and the interface package of the CX Tape Reader. The card contains a data buffer register and control circuitry. An application block diagram is shown in Figure 1.

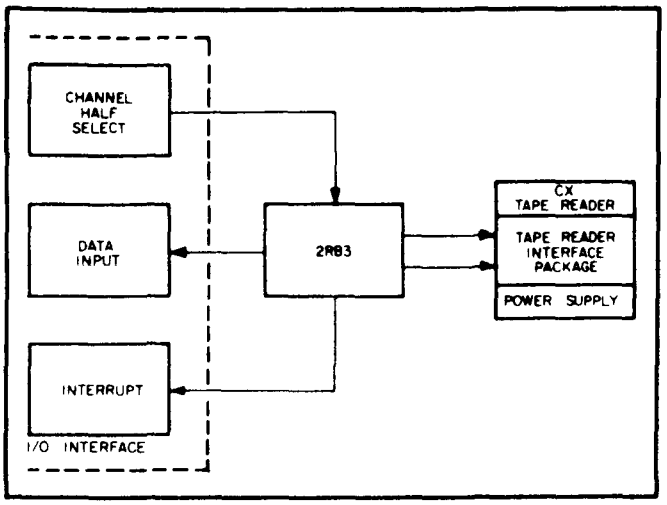


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

- Data input from tape reader interface: Logic "zero"; 1.1V maximum; logic "one", 4.0V minimum.

- Channel half-select requires a minimum 11V, 4 μsec pulse.

Output Requirements

- Data output must be a minimum 6V, 4 μsec pulse.

- Interrupt signal is nominally 26V tied to a 1k pull-up resistor.

Power Requirements

The 2RB requires a 26Vdc from the I/O power supply.

CIRCUIT DESCRIPTION

Refer to the schematic in Figure 4.

Each of the eight identical buffer registers on this card work in the following manner. Refer to upper right hand corner of Figure 4.

Buffer Register

Whenever the tape reader data contact closes (zero voltage on R.D.C.O for example), because of a punched hole in a particular level of the tape, capacitor C9-1 (0.5 mfd) will charge up.

When the computer now addresses the reader channel through the channel half-selects, the data in the buffer register will be transmitted to the computer. This will occur because, with C9-1 charged, winding 1-2 will appear as a high impedance path when the channel half-select pulsed and, therefore, windings 5-6 will have the voltage impressed across it (will present a logical "one" to the computer).

If, however, there is no hole in the tape, C9-1 will not be charged, and when the half-select is pulsed, winding 1-2 will look like a short circuit and there will be no voltage impressed upon winding 5-6 (will present a logical "zero" to the computer).

The register must be cleared once it has been read by the computer; this is done by the Clear Register signal which is common to all 8 bits.

The "U" contact input shown in the schematic is the "Universal" contact in the reader which closes every time a character is read. It is used as a strobe contact.

When the reader advances, the U contact (filtered) closes to PSC and transistor T8-1 conducts for 6 msec, the time which the "U" contact is closed. This causes T5-1 normally blocked, to conduct for a short period of time. When this transistor blocks again, an interrupt (a positive going voltage) is given to the I/O interface, indicating that a character from the tape reader has been read. At the same time, transistor T5-2 blocks and resets the SCR (S1-1).

The computer acknowledges the interrupt by selecting the channel associated with the reader and reading the 8-bit buffer register.

A "dummy" bit is used to indicate this acknowledge from the computer. This is shown on the schematic. The transformer X1-9, when selected with an open primary winding 1-2, will always set the SCR, S1-1. S1-1 may be set since T5-2 is normally conducting except during the interrupt period.

Each time the computer reads the buffer register, it is

necessary to clear the register and "ask" for another character. When S1-1 conducts, transistor T8-2, approximately 25 μsec later, conducts and discharges all capacitors in the buffer register. At the same time a signal is sent to the Reader Advance Circuit to advance the reader.

The Clear Register Switch signal (X12) is not used.

Figure 2 represents the time requirements for this card.

* * *

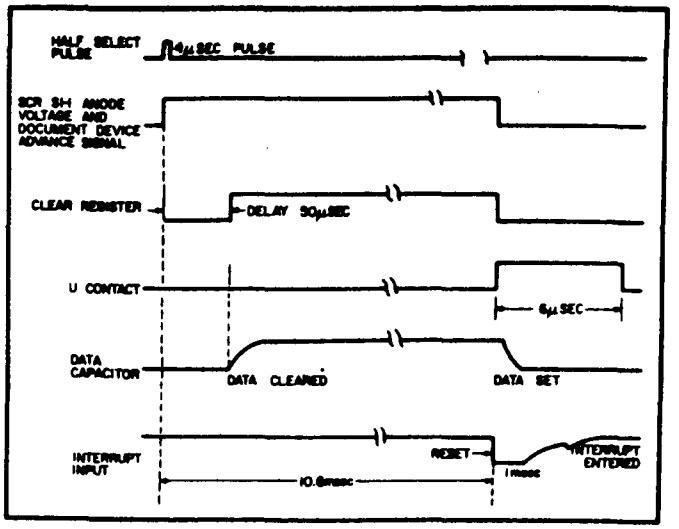


FIGURE 2. CIRCUIT TIMING CHART

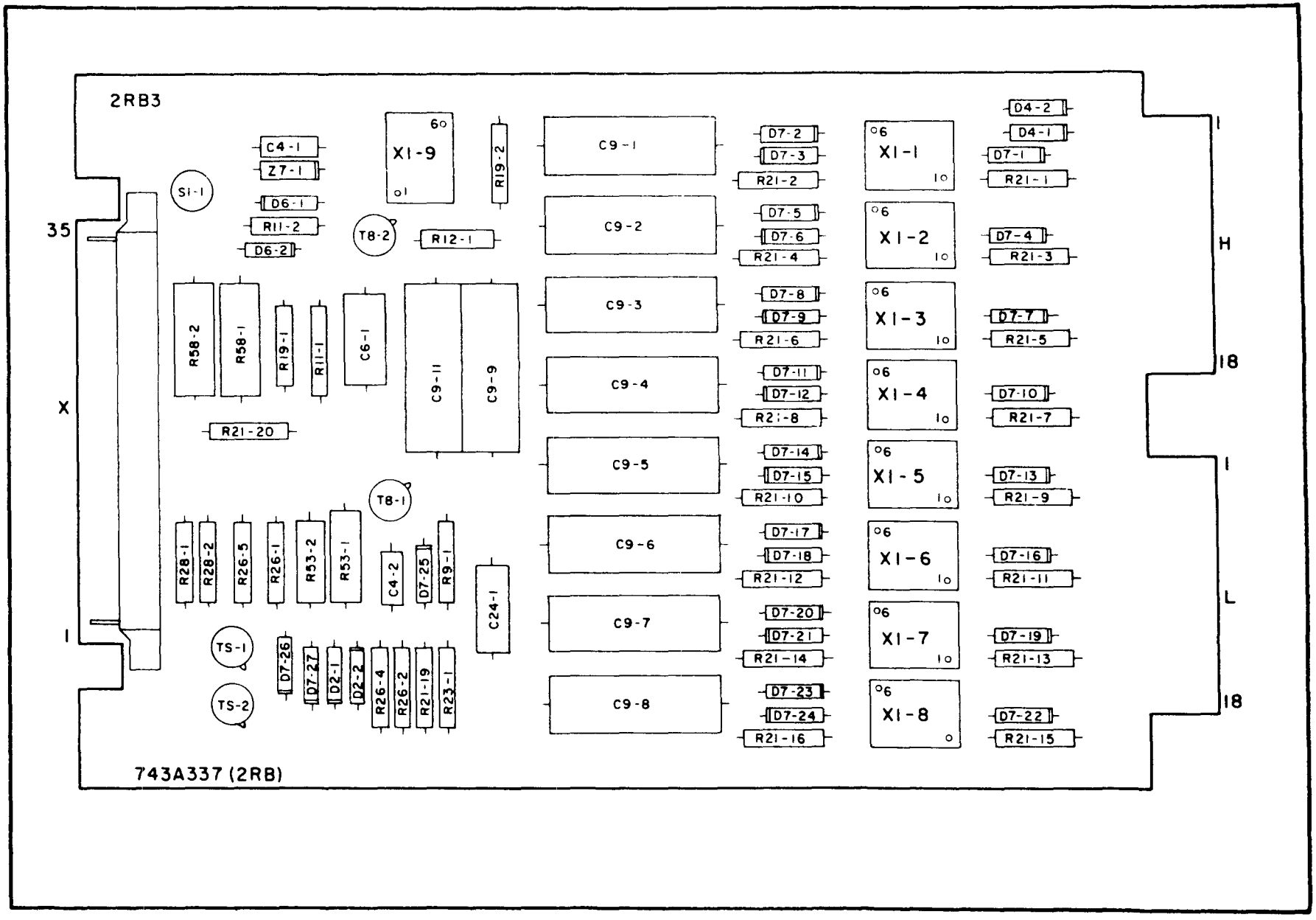


FIGURE 3. 2RB3 ASSEMBLY (REF. DWG. 743A337, SUB 11)

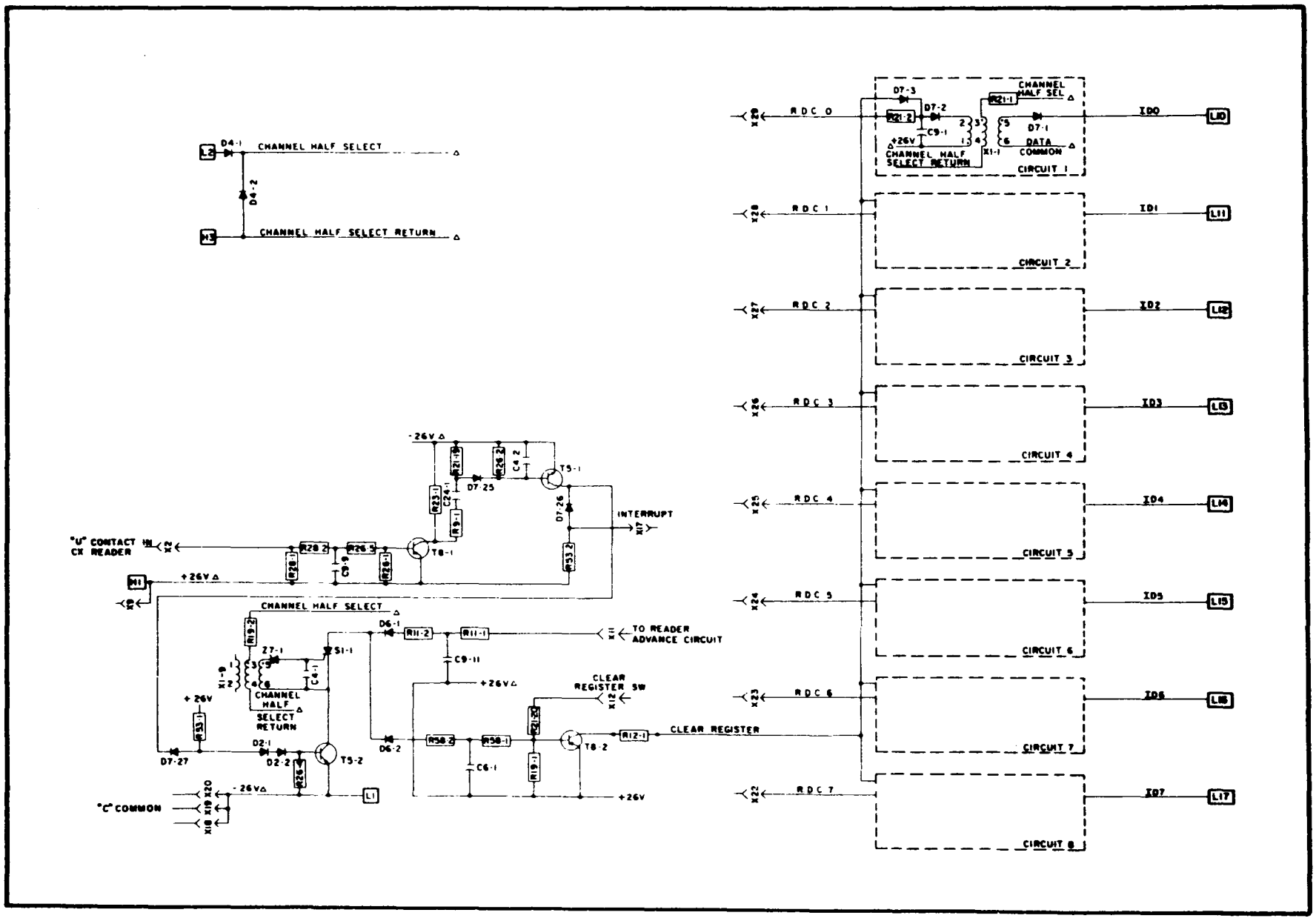


FIGURE 4. 2RB3 SCHEMATIC (REF. DWG. 743A337, SUB 11)

3SB1 - SPAN & GAIN w/INPUT BUFFER

GENERAL DESCRIPTION

This module is used in the analog input subsystem and it performs the following functions:

- Provides addressability by the I/O system through the channel half-select circuit.
- Provides circuits to set the span and gain of the voltage-to-frequency converter.
- Provides transformer isolation between the output of the counters (CT card) and the I/O register.
- Provides a trigger signal to start the analog input cycle.

Figure 1 shows the functional ties of the 3SB module to the analog input subsystem and the I/O interface.

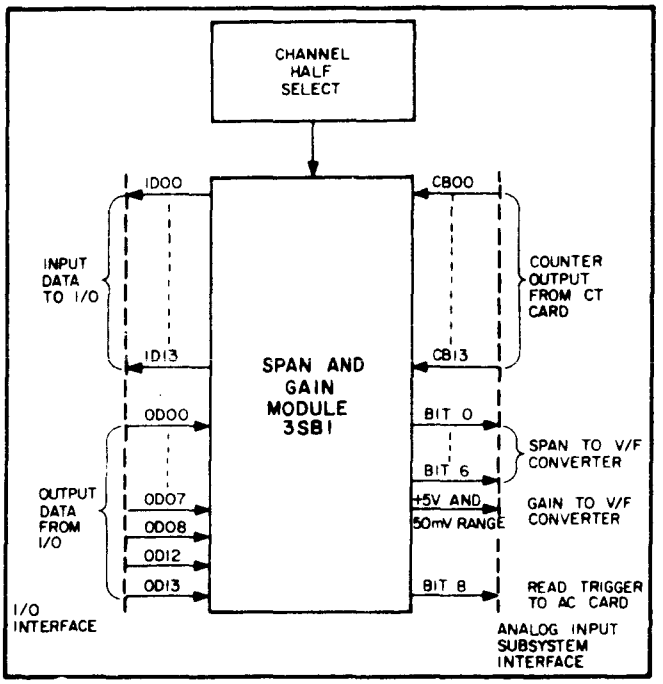


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The channel half-select signal requires a minimum 11 V, 4 μs pulse.

The data input from the counter requires diode-coupled logic-level signal, "zero" (= PSC) for unselected and "one" (= transistor is blocked) for selected bits.

The data inputs from the I/O interface require logic level signals of "zero" (1.1 V max) and "one" (4.4 V min).

Output Requirements

The output to the I/O interface (input data) requires a minimum 6 V, 4 μs pulse.

The span driver output (bits 0 to 6) requires a "zero" for selected bits and "one" (+ 26 V) for unselected bits.

The span driver common is tied to PSC through a power supply switch. To reset the SCR circuits this must be opened for a minimum of 100 μs.

The read trigger output requires a 4 μs grounded (logical "zero") pulse corresponding to the channel half-select pulses.

The gain select requires a logical "zero" if the +5 V range is selected, and a logical "one" (+ 26 V) if the + 50 mV range is selected.

CIRCUIT DESCRIPTION

Since the 3SB module performs 4 different functions, each of these functions is described separately.

Digital Input Buffer

The fourteen bit digital input buffer consists of fourteen identical circuits, each composed of a three winding buffer transformer, a current limiting resistor and an isolating diode. The circuit diagram of one input buffer is shown in Figure 2.

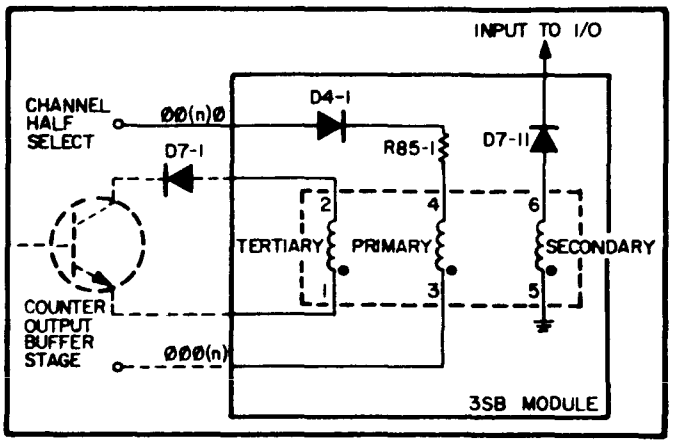


FIGURE 2. ONE INPUT BUFFER CIRCUIT

The circuit operates in the following way. When the transistor representing the output buffer stage of the counter is blocked, diode D7-1 is reversed biased. Most of the primary pulse energy, supplied by the channel half-select circuit (ØØØN), (ØØNØ) is transferred to the secondary winding of the transformer and a pulse is provided to the I/O interface (ID00). When the counter output transistor is saturated, diode D7-1 is grounded (to counter ground) and the tertiary winding of the transformer is short-circuited. Most of the primary pulse energy is now transferred to the tertiary circuit and dissipated in the winding resistance, diode D7-1, and the counter output transistor. The voltage appearing across the secondary winding is not sufficient to provide enough energy to be detected by the I/O interface. Resistor R85-1 provides current limiting and diode D7-11 clamps any inductive flyback voltage.

Span Driver

The span selection consists of seven identical circuits. Each of these circuits consists of an SCR with a zener diode threshold in the gate circuit and a three winding trigger transformer. The circuit diagram of one bit of the span driver is shown in Figure 3.

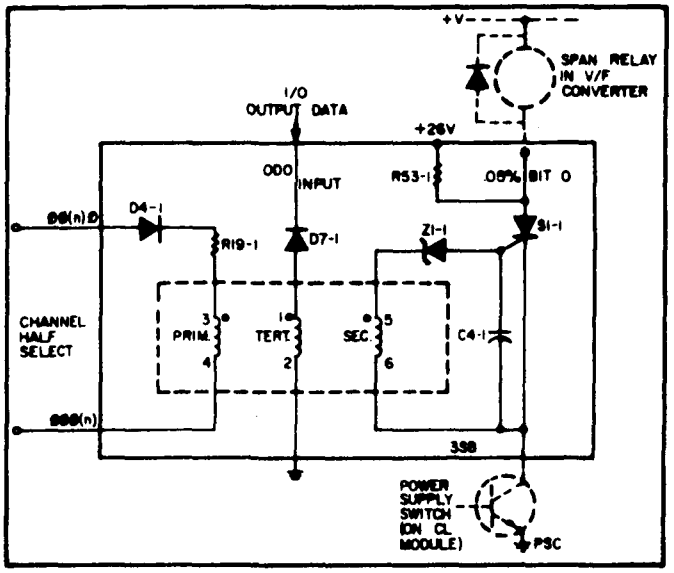


FIGURE 3. ONE BIT OF SPAN DRIVER CIRCUIT

The operation of the circuit is identical to that of a channel driver circuit. Initially the output transistor of the power supply switch is saturated so that if a positive trigger pulse is applied between the gate and the cathode of S1-1, the SCR will conduct. The gate circuit consists of zener diode Z1-1 in series with the secondary winding (5-6) of the trigger transformer. The tertiary winding (1-2) of the trigger transformer is connected through diode D7-1. When the output is a logical "one", diode D7-1 is reversed biased, which open circuits the tertiary winding. If the input is a logical "zero", D7-1 is grounded which shorts out the tertiary winding.

It can be seen that when a pulse (channel half-select ØØ (n) Ø and ØØØ (n)) appears across the primary winding (3-4) the logic level of the input line will determine the voltage on the secondary (5-6).

With the input a logical "one", the secondary (5-6) will have a voltage induced in it which triggers S1-1 and drives its output to a logical "zero". This occurs because the +26 V tied to R53-1 will conduct through the power supply switch to PSC. With the input a logical "zero", no voltage will be induced in the secondary, the SCR will not conduct and therefore the output will remain a logical "one".

The zener diode in the gate circuit is needed since the tertiary winding is never completely short circuited. Losses in diode drop and transistor saturation drop account for a small pulse across the secondary winding when the input is a logical "zero". When the input is a logical "one" and the particular channel is selected, the SCR's will be triggered in response to the half-select pulse. The SCR will remain in the conducting state until the power supply switch turns it off.

The output of the span driver is used to energize the span relays in the voltage-to-frequency converter.

Read Trigger

Bit 8 (ØD8) of the I/O output data is used to generate the read trigger signal. This is accomplished with the circuit shown in Figure 4.

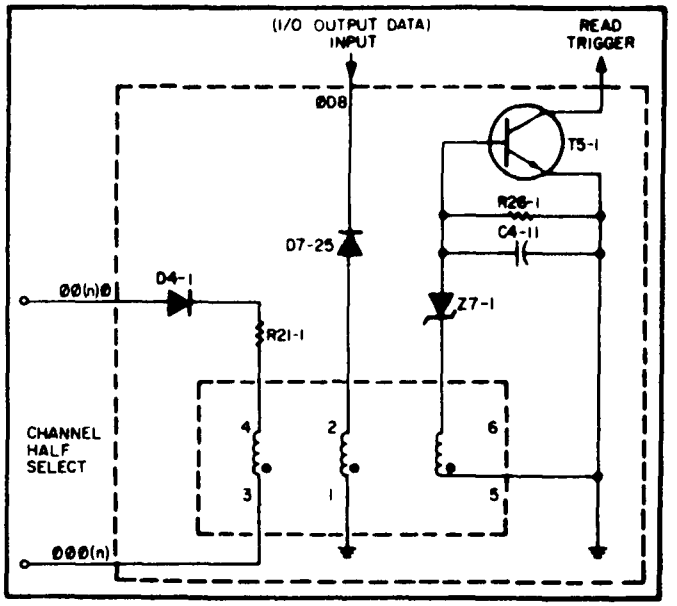


FIGURE 4. READ TRIGGER CIRCUIT

Like the span driver circuit, a pulse will be generated in the secondary winding of the transformer (5-6) by the channel half-select pulse if the input is a logical "one". This pulse will saturate the base to emitter junction of transistor T5-1 and thus, the READ-TRIGGER output will be grounded for approx. the duration of the channel half-select pulse (4 μs).

The zener diode threshold serves the same purpose as described in the span driver description.

Capacitor C4-11 and resistor R26-1 are needed for filtering out noise which may propagate due to the zener capacitance.

Gain Select

Bits 12 and 13 of the I/O output data (ØD12 and ØD13) are used for selection of gain of the voltage to frequency converter. For this purpose, the circuit on the 3SB module consists of two, transistor-diode circuits connected in a flip-flop configuration, coupled to two 3-winding transformers. The circuit diagram is shown in Figure 5.

Assume that transistor T6-2 is conducting. Point 1 is grounded and no base drive is provided to transistor T6-1. But as transistor T6-1 is blocked, base drive is provided to transistor T6-2 through R25-2, D1-8, D1-6, and D1-5. Also +26 V is provided to the gain relay through R25-2 and D1-9. The 50mV range is selected.

If a channel half-select pulse now appears on ØØØ (n) and ØØ (n) Ø and bit 12 (ØD12) is a logical "one", a positive pulse will appear on the secondary winding (5-6) of transformer X1-8 which will turn on transistor T6-1, which in turn will cause T6-2 to be blocked. In this case, no voltage will be provided to the gain relay output. The 5V range is selected.

The flip-flop will change its state again similarly if, on the next half-select pulse, bit 13 (ØD13) is a logical "one".

The flip-flop will not change its state if both bit 12 and bit 13 are logical "zeros".

* * *

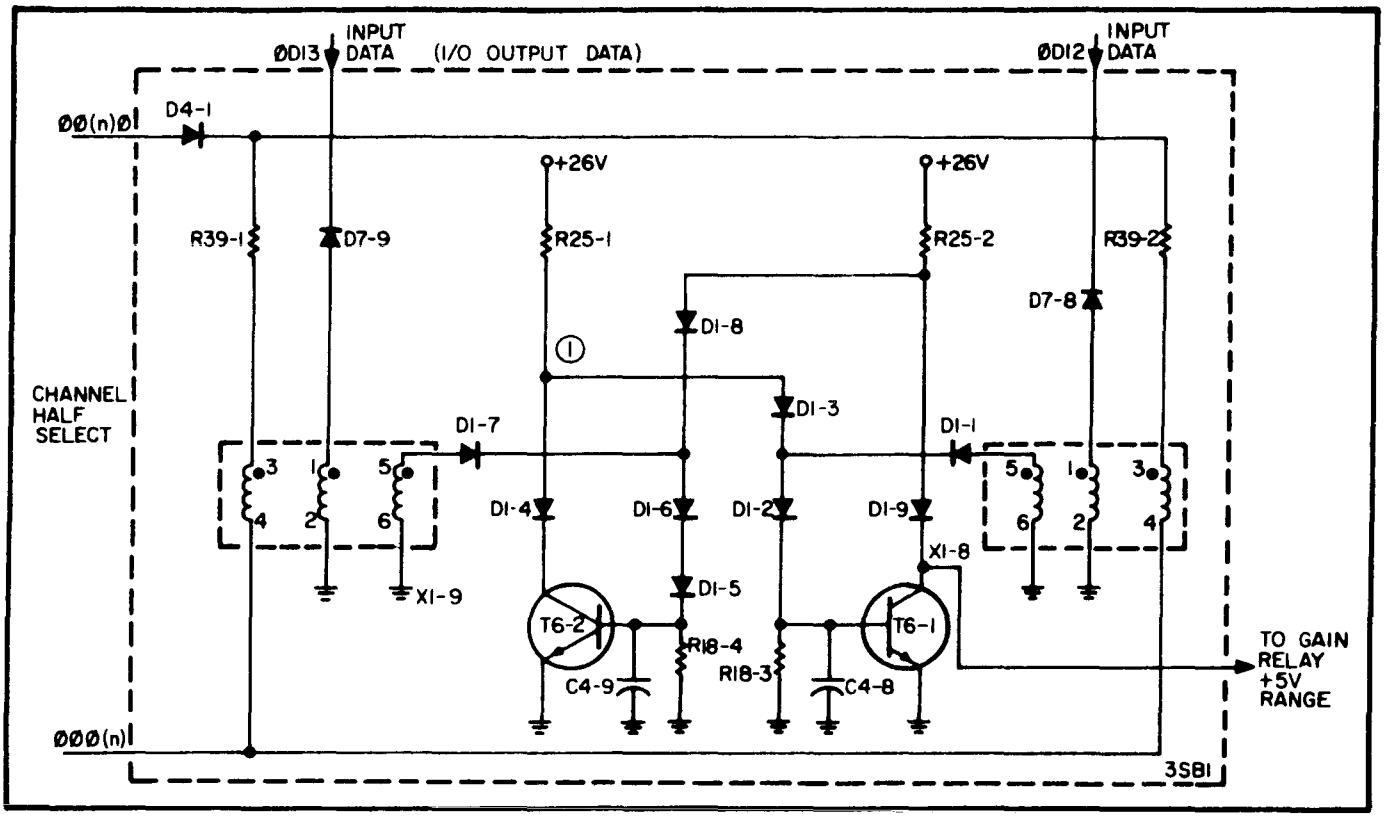


FIGURE 5. GAIN SELECT CIRCUIT

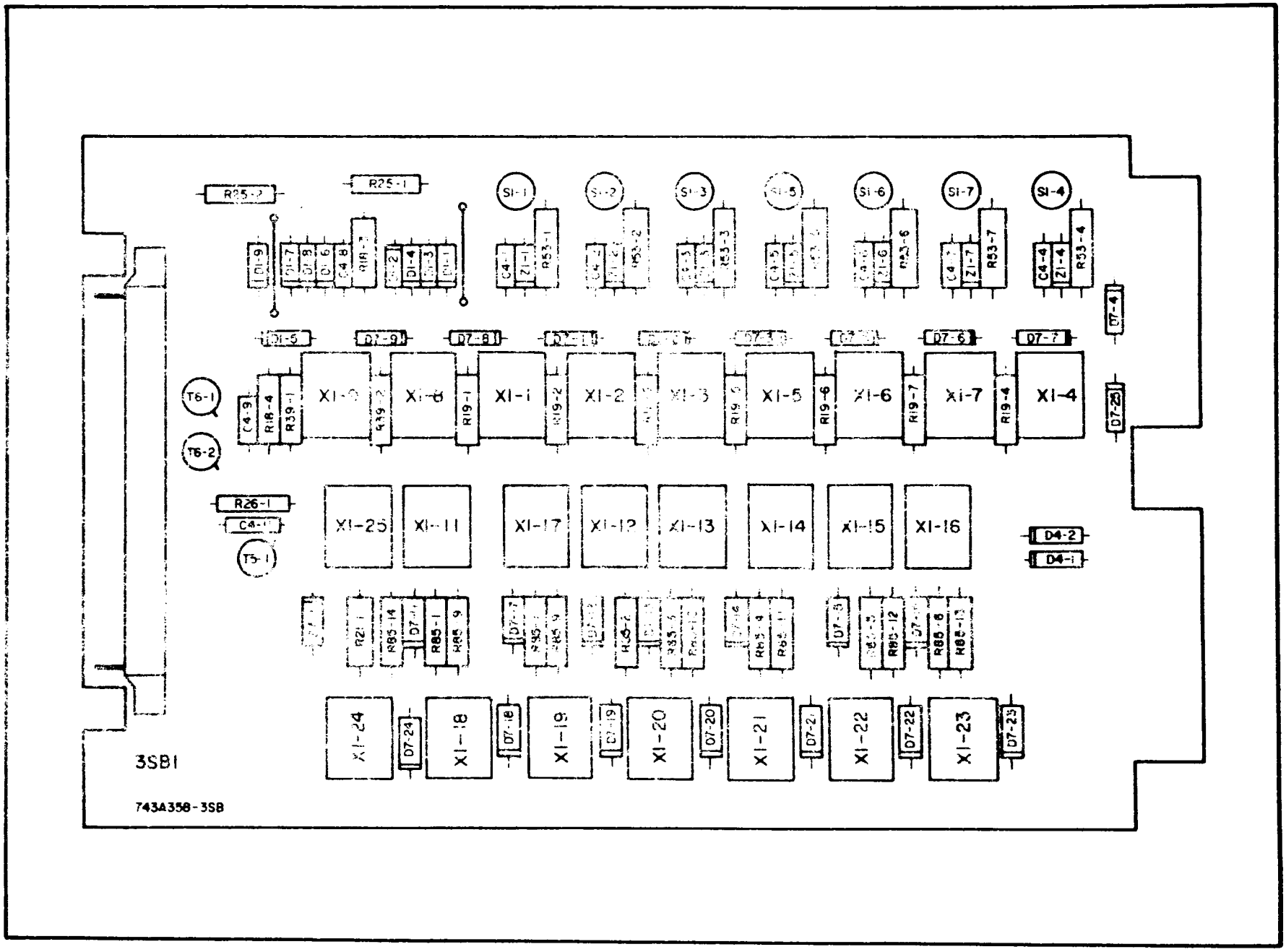


FIGURE 5. 3SB1 ASSEMBLY (REF. DWG. 743A358, SUB 7)

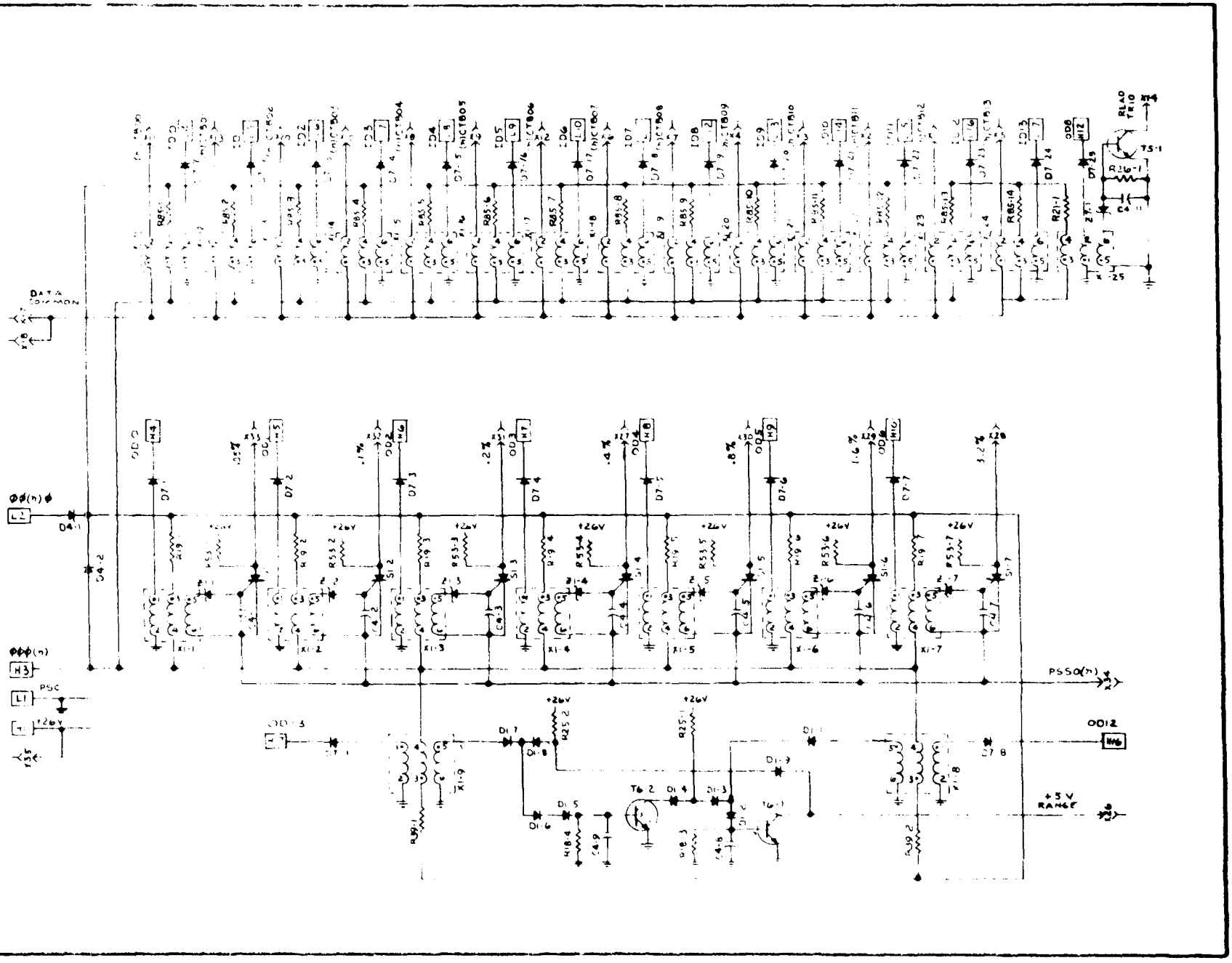


FIGURE 6. 3SB1 SCHEMATIC (REF. DWG. 743A358, SUB 7)

3SI1/3SI2 - SEQUENCE OF EVENTS INTERRUPT CARD

GENERAL DESCRIPTION

The SI card generates a single interrupt when any one of a number of CCI's change state; either from closed to open, or open to closed. The card suffix denotes the following:

Card	Type
3SI1	48V, make or break int.
3SI2	125V, make or break int.

A block diagram showing a typical application of the SI card and power supply switches is shown in Figure 1.

CIRCUIT SPECIFICATIONS

Input Requirements

Inputs must take the form of a switched dc voltage from relay contacts or switches. The presence of a voltage produces a "one" input while zero volts produces a "zero" input.

The nominal magnitude of the input voltage level and in-rush resistance of each bit are:

Module Type	Nominal Voltage	Inrush Resistance/bit
3SI1	48	2.9k
3SI2	125	5.9k

Output Capabilities

Output is to a power supply switch trigger.

The output is clamped at approximately one volt until the power supply switch is reset.

Power Requirements

The negative side of the 48/125V power supply should be connected to the 48/125 RET (X2). The nominal inrush current/bit is 16.5 mA for 48V or 21.2 mA for 125V. A minimum of 6V is required on the anode of the silicon controlled rectifier (X18). The negative side of the plant power supply must be connected to PSC.

CIRCUIT DESCRIPTION

Figure 2 illustrates one bit of the 14 bits on the 3SI1 and 3SI2 cards.

Input resistance for each card is:

Type	Ra	M41 Coil Res.
3SI1	1.5k	1.425k
3SI2	4.5k	1.425k

When the contacts for bit (n) close or open, the relay coil (M41) is energized or de-energized respectively. The coil will not be operated at a frequency greater than 60 Hz. The M41 contacts will momentarily open because

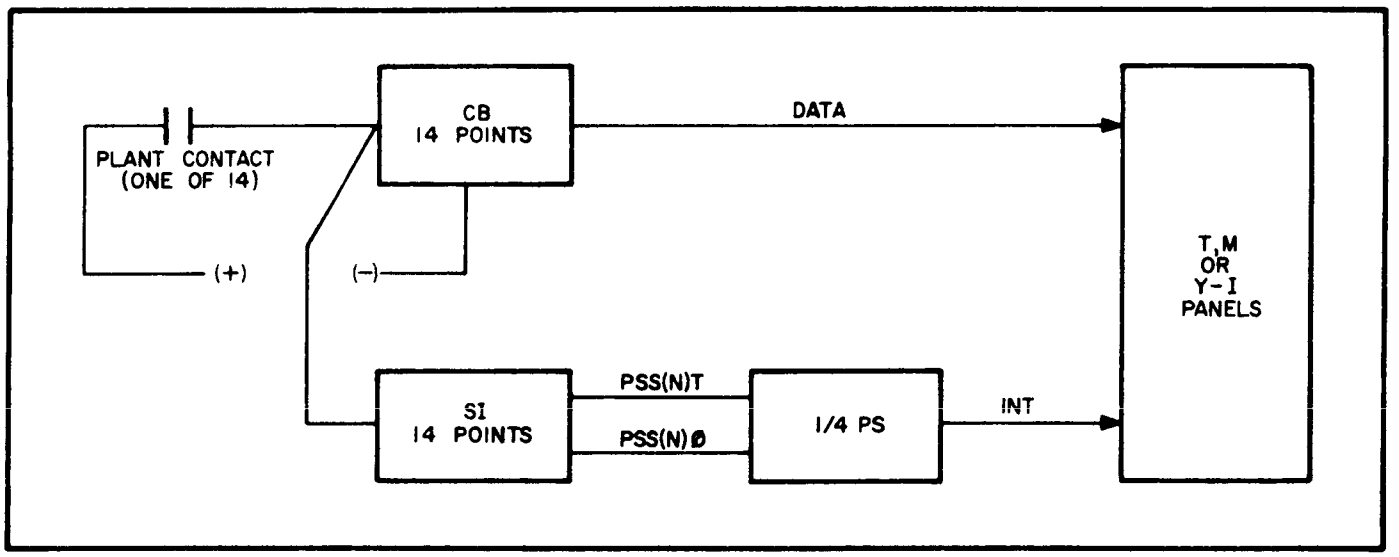


FIGURE 1. APPLICATION BLOCK DIAGRAM

they have "break before make" feature. Therefore the SCR, S1-1 will be triggered and start conducting. S1-1 will be triggered when bit (n) is opened or closed. It will remain conducting until reset by the power supply switch card.

* * *

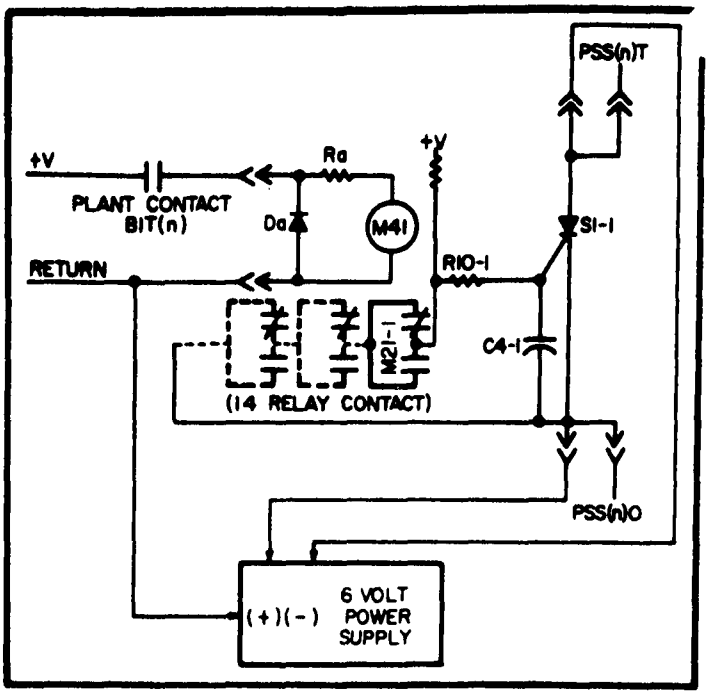


FIGURE 2. ONE BIT CIRCUIT

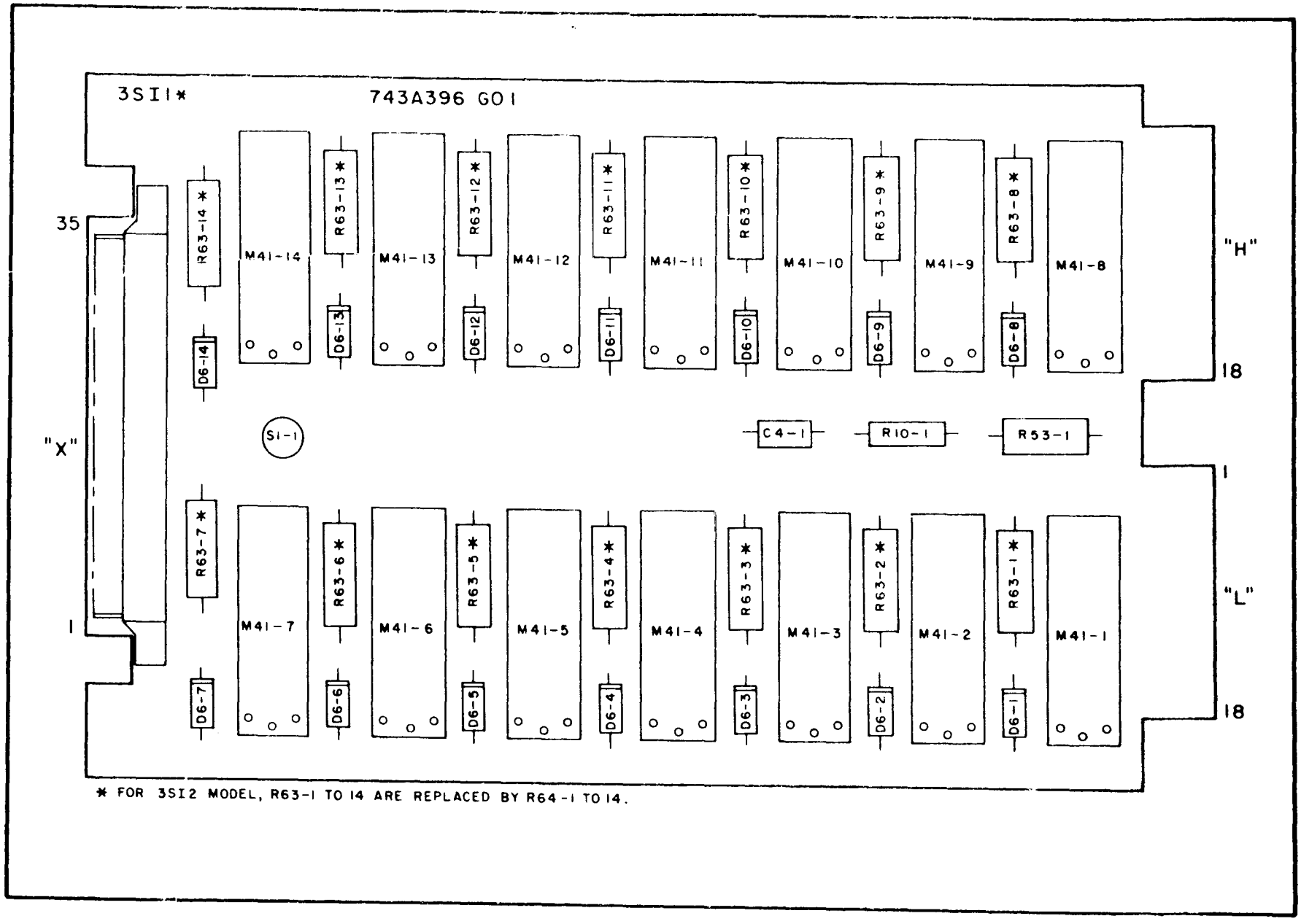


FIGURE 3. 3SII/3SI2 ASSEMBLY (REF. DWG. 743A396, SUB 3)

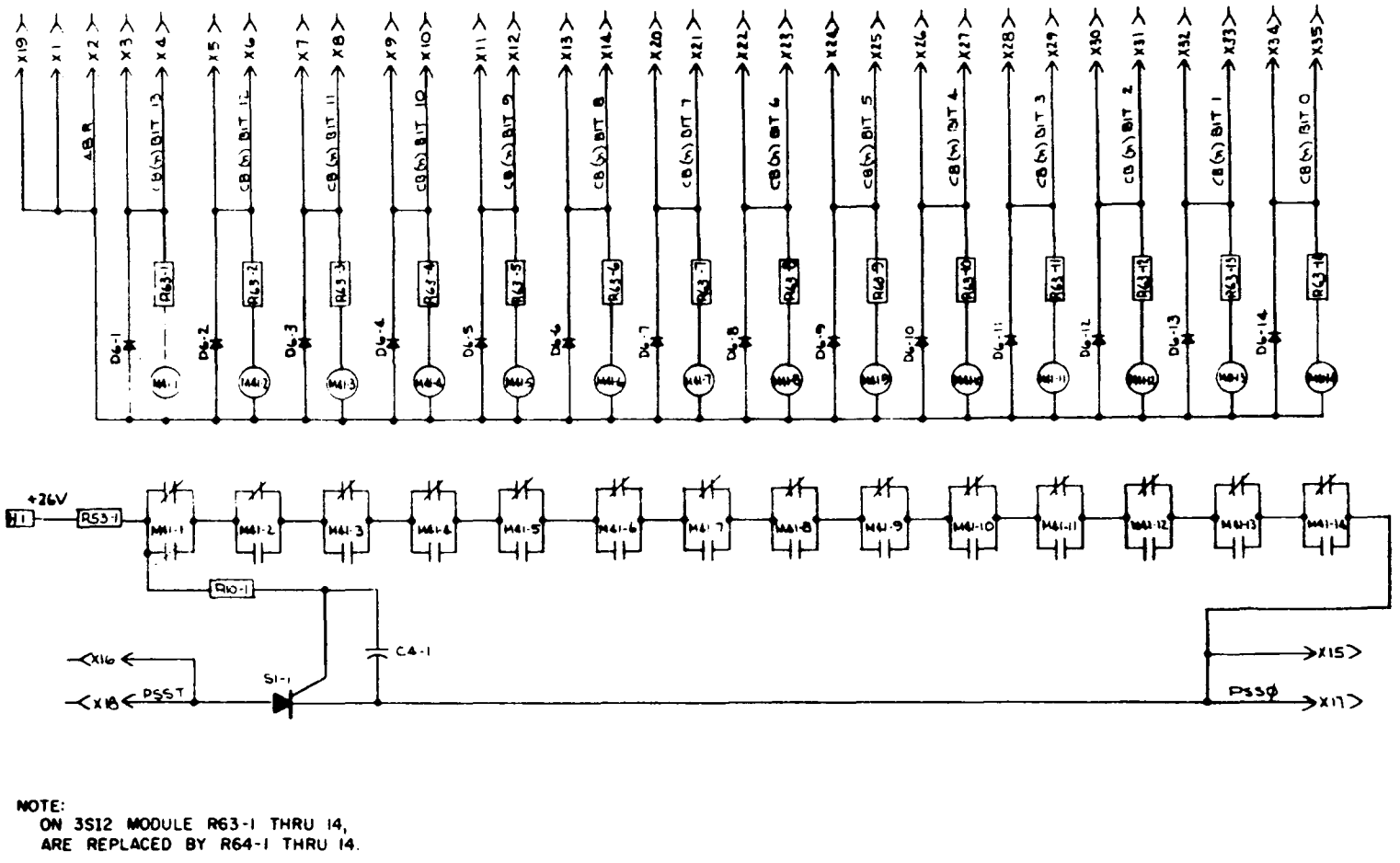


FIGURE 4. 3S11/3S12 SCHEMATIC (REF. DWG. 743A396, SUB 3)

2SL1 - 735 SELECTRIC INTERFACE MODULE

GENERAL DESCRIPTION

The 2SL1 printed circuit module serves as a buffer between the Central Processing Unit, and the interface package of the 735 Selectric typewriter. It contains a data buffer register and control circuitry. An application block diagram is shown in Figure 1.

CIRCUIT SPECIFICATIONS

Signal Requirements

I/O Interface

- Data: logic "zero" - 1.1V maximum; logic "one" - 4.0V minimum.
- I/O Selection: 4.0 μsec pulse, 11V minimum.
- Interrupt Input: nominally 28V tied to a 1k pull up resistor.

735 Interface Package

- Data: zero volts (magnet energized), +28V (magnet de-energized).
- Reset: contact closure, +28V causes reset to occur.

Power Requirements

2SL1 module receives +28V through terminal X1.

CIRCUIT DESCRIPTION

Data Buffer Register

Figure 2 shows one bit of the 14-Bit data buffer register. The Selectric magnet is energized when 4 μsec half-select pulse unloads the data line through the pulse transformer into the associated SCR. When the SCR conducts, the magnet is energized, and the 735 Selectric cycles. This causes the reset contact in the Selectric to close, thus generating a RESET signal. The RESET signal controls the Power Supply Switch located on the SL card. When open, the Power Supply Switch causes the SCR to block and the Selectric magnets to be de-energized.

The outputs of the SCR's which drive the magnets are filtered to prevent rate-of-rise firing of the SCR's. The filter is also used to drop the dc voltage to the magnets from 28Vdc to 24Vdc (their normal operating voltage).

Power Supply Switch Control and Interrupt Circuit

Refer to Figure 3 for the following description.

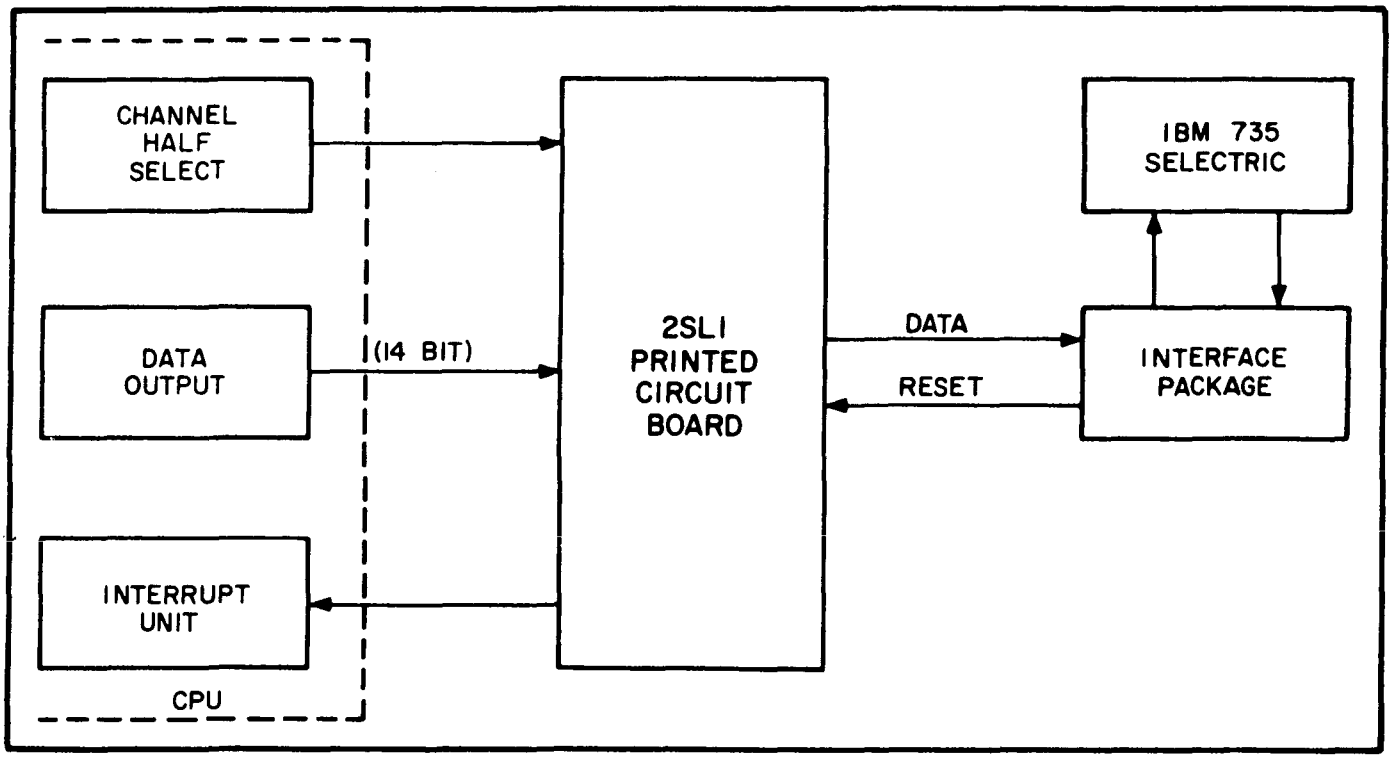


FIGURE 1. APPLICATION BLOCK DIAGRAM

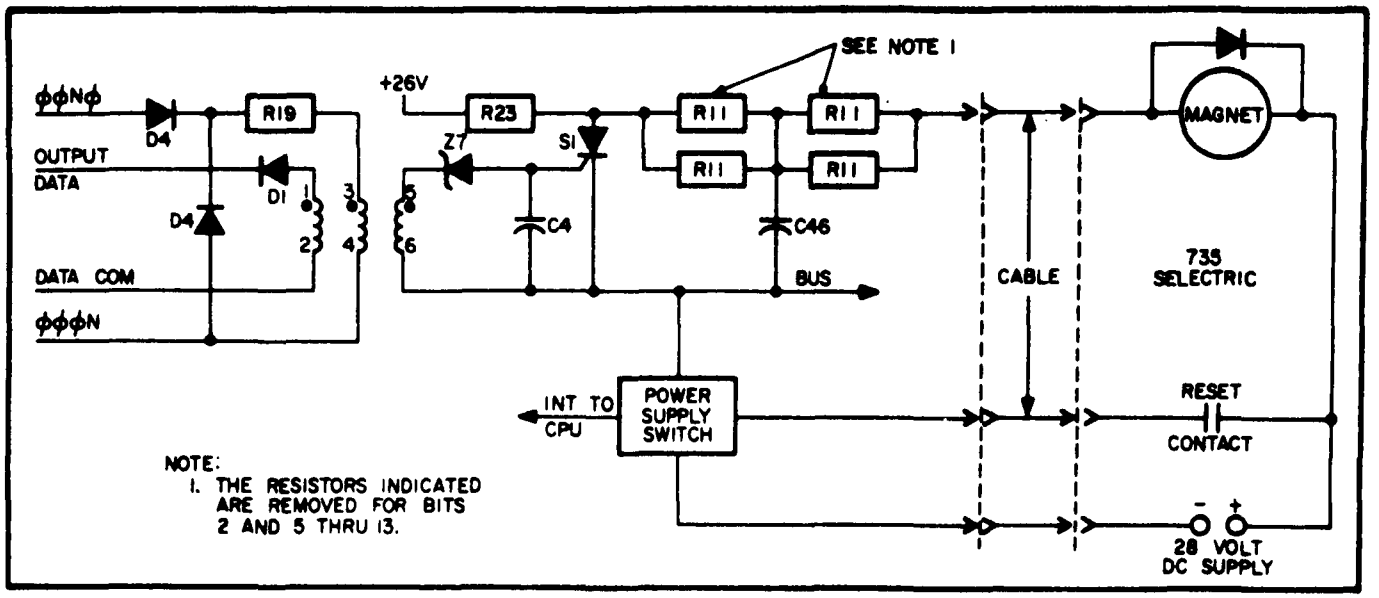


FIGURE 2. ONE BIT OF DATA BUFFER REGISTER

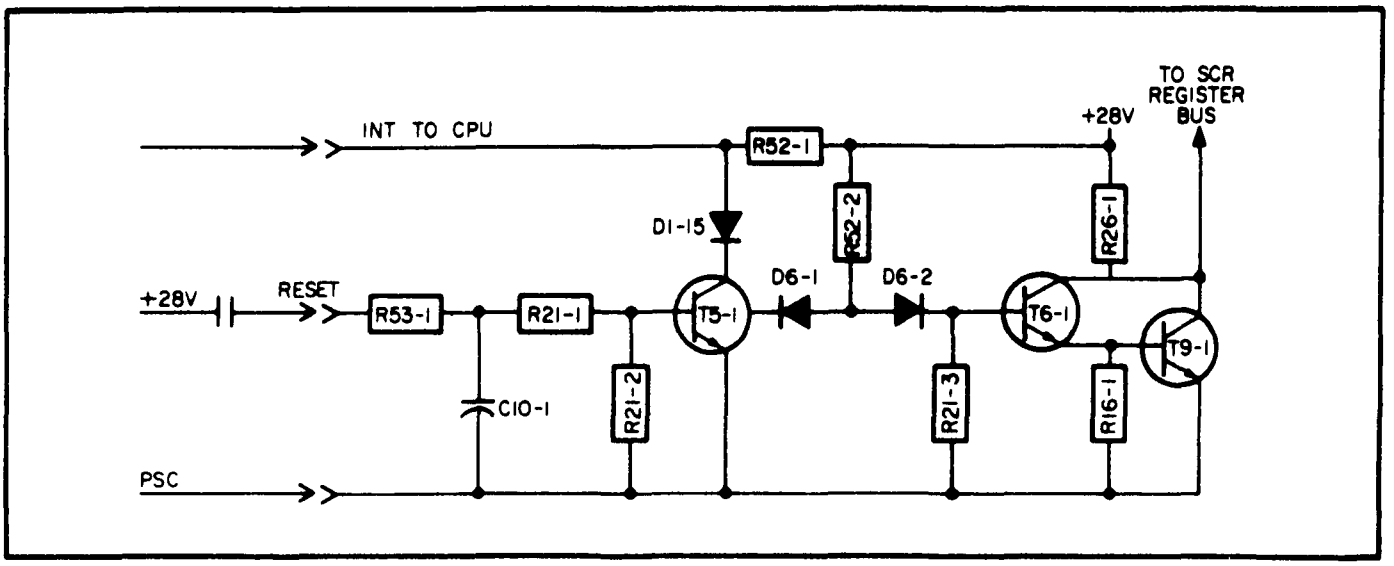


FIGURE 3. POWER SUPPLY SWITCH CONTROL AND INTERRUPT CIRCUIT

Transistor T9-1 is the controlling transistor in the Power Supply Switch which delivers current to the printer magnets if their SCR's are switched on. When this transistor blocks, the SCR's are switched off, and the magnets are de-energized.

In the quiescent state, transistor T9-1 is conducting and transistor T5-1 is normally blocked. The base of T5-1 is controlled by the completion contacts in the printer. Normally these contacts are open, however, when the Selectric cycles, these contacts close and cause transistor T5-1 to conduct. The transistor conducts as long as the completion contact in the Selectric is closed. With T5-1 conducting, T6-1 blocks, thus blocking T9-1. This switches off all the SCR's which were on, thereby clearing the 14-Bit register.

Transistor T5-1 blocks when the completion contacts open. The output of transistor T5-1 is used to interrupt the computer to ask for another character of output. The interrupt occurs when this output has a positive going transition.

* * *

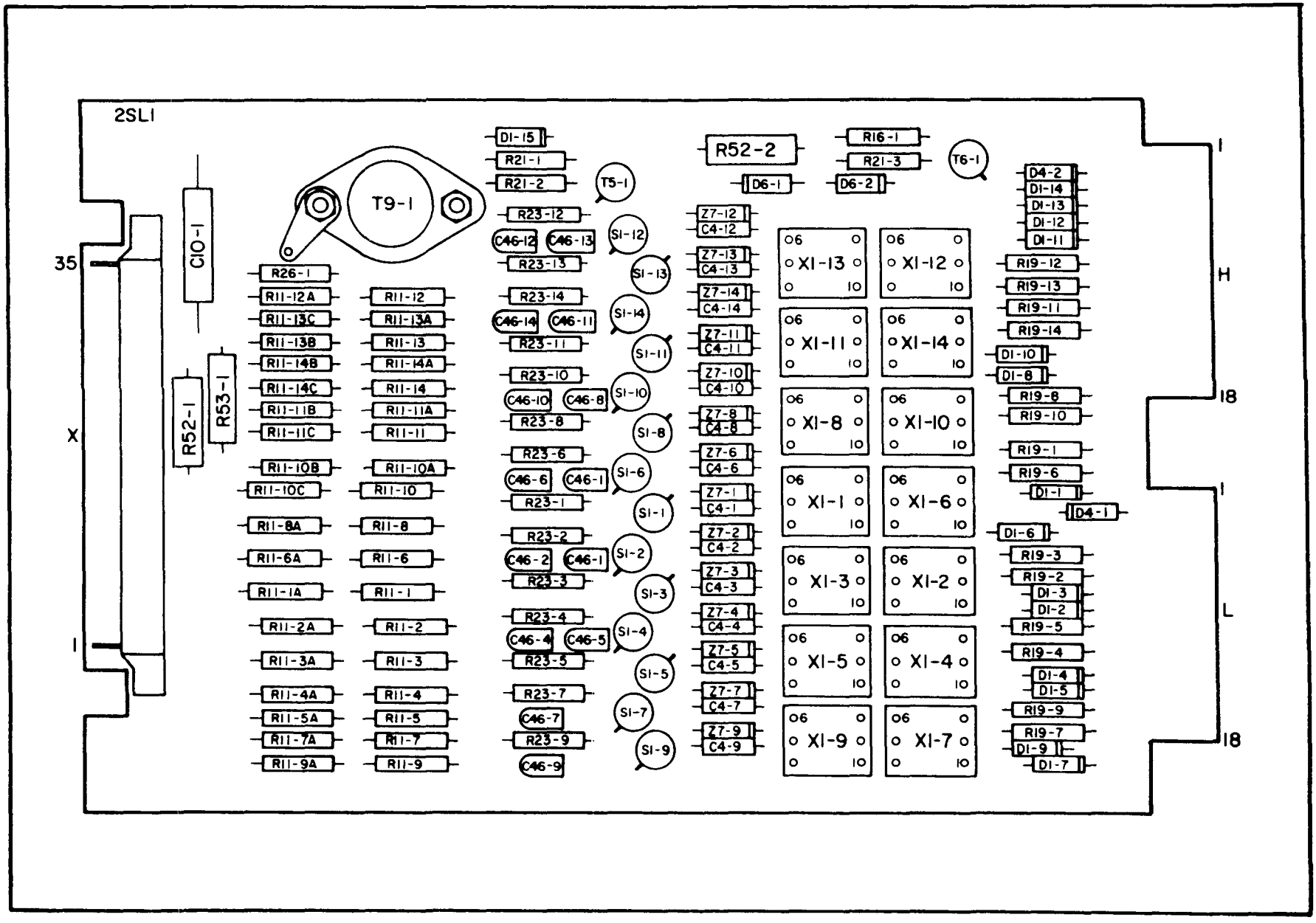


FIGURE 4. 2SL1 ASSEMBLY (REF. DWG. 845A335, SUB 1)

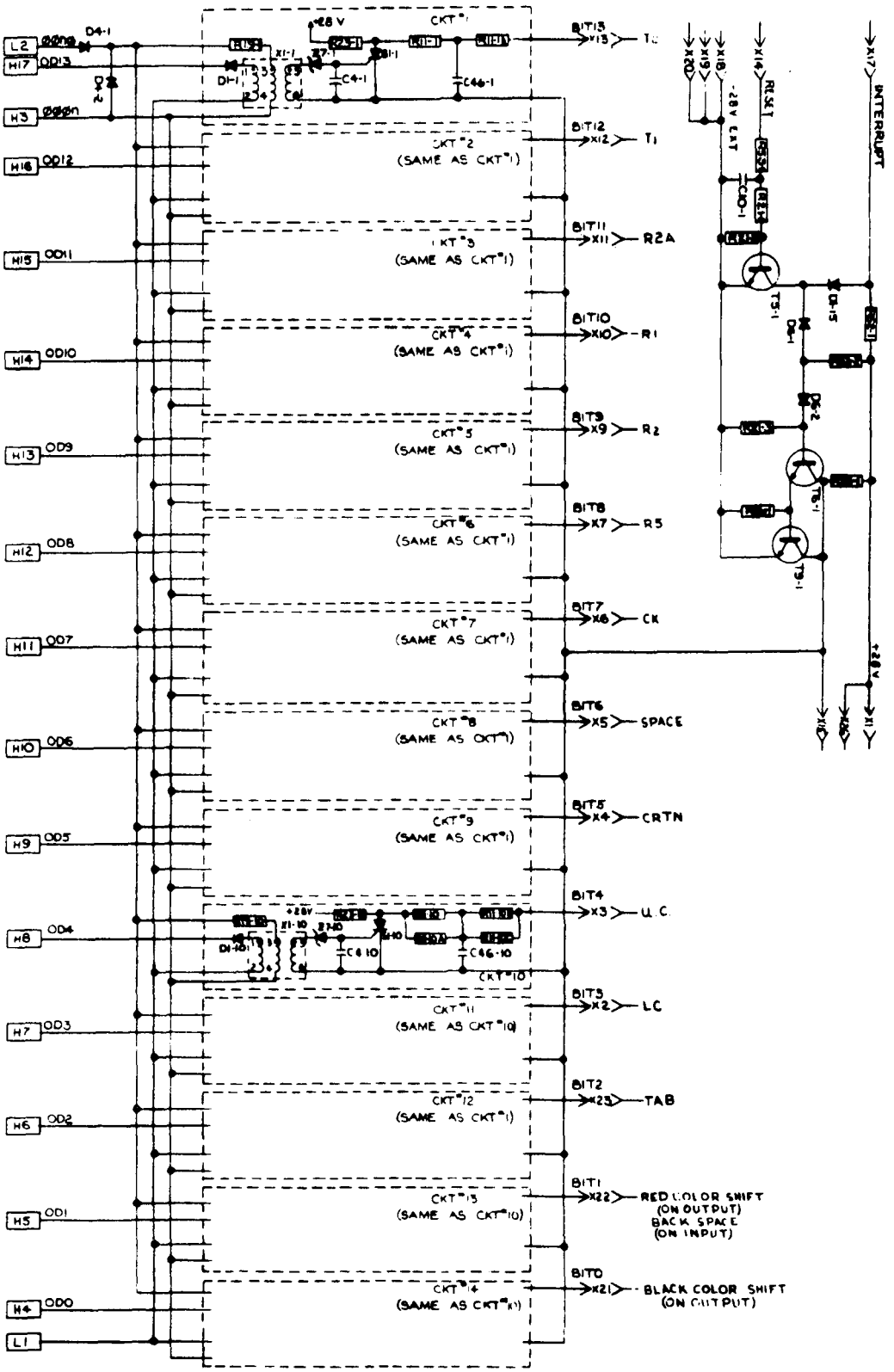


FIGURE 5. 2SL1 SCHEMATIC (REF. DWG. 845A335, SUB 1)

2TN1 - MODEL 35 TELETYPE INPUT MODULE

GENERAL DESCRIPTION

The 2TN1 module is used for control of data transfer between the Model 35 Teletype equipment and the I/O interface. This card contains data input pulse transformers and control circuitry. An application block diagram is shown in Figure 1.

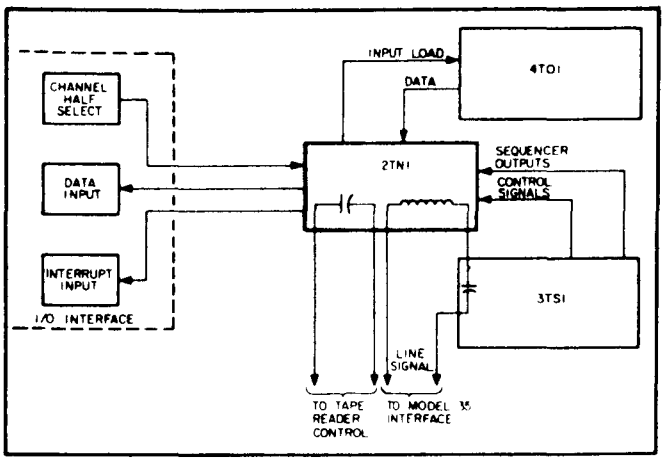


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

I/O Interface

- I/O Selection - 4.0 μsec pulse, 11V minimum.
- Data Input - "one" - 6V minimum, 4.0 μsec pulse.
- Interrupt Input - Interrupt signal is nominally 26V tied to a 1k pull up resistor.

4TO1 Signals

- Data - Logic "zero" - 1.1V maximum, Logic "one" - 4.0V minimum.
- Input Load 200 μsec pulse will set selected SCR.

3TS1 Signals

- Sequencer outputs - zero volts implies logic "zero", positive voltage implies logic "one".
- Control signals - covered in circuit description.

Model 35 Interface

- Mercury Relay Contact used to control tape reader ON/OFF.
- Mercury Relay used to monitor input line current.

Power Requirements

The 2TN1 module receives power from the +26V I/O interface power supply.

CIRCUIT DESCRIPTION

2TN1 card contains the following items:

- The 8 input pulse transformers whose outputs are tied to the I/O interface data input register. The transformer inputs are tied to the 8-bit SCR register on the TO card.
- Line relay used for monitoring serial data from Model 35.
- "Input load" signal used for setting SCR's in data register, (4TO1).
- Tape reader ON/OFF control relay.
- Input interrupt circuit requesting input data be read by I/O interface.
- "Acknowledge" pulse transformer indicating I/O interface has taken previous character.

Figure 2 shows one of the eight pulse transformers used for reading data from the 4TO1 SCR data register to the I/O interface. If the SCR is conducting, winding 1-2 will appear as a short circuit and a small voltage will result across winding 5-6 when the 4.0 μsec channel half-select pulse occurs, this is a logic "zero" to the I/O interface. However, if the SCR is blocked, D1 will be blocked

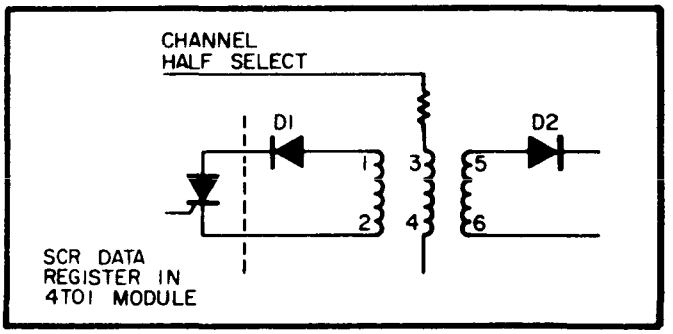


FIGURE 2. PULSE TRANSFORMER CIRCUIT

when channel half-select pulse occurs and a voltage will appear across winding 5-6 and D2 will conduct. This is a logic "one" to the I/O interface.

Figure 3 shows the input mode selection. When the line relay M9-1 is de-energized as a result of a "start" impulse (open line) from the Model 35, SCR S1-1 is set. The relay contacts open and the gate of the SCR is pulsed, turning it on. When S1-1 turns on, transistor T8-1 conducts and generates signals "U" and "Y" which indicate input mode. The signals are +26V.

Figure 4 shows the timing associated with setting the input SCR (S1-1) as a result of "start". Transistor T5-2 remains blocked since "N" is ground at all times other than step 8 of the sequence (STOP). When step 8 of the sequence occurs "N" goes positive, T5-2 conducts. This shunts the S1-1 holding current and the SCR blocks. T8-1 remains on, however, since T5-2 provides the base current to T8-1. Signal pulse "R" occurs about 1.5 msec after "N" and causes T5-2 to block. This generates the interrupt positive transition. Also T8-1 will block and "U" and "Y" signals are inhibited. The same sequence of events will occur when the next "start" occurs.

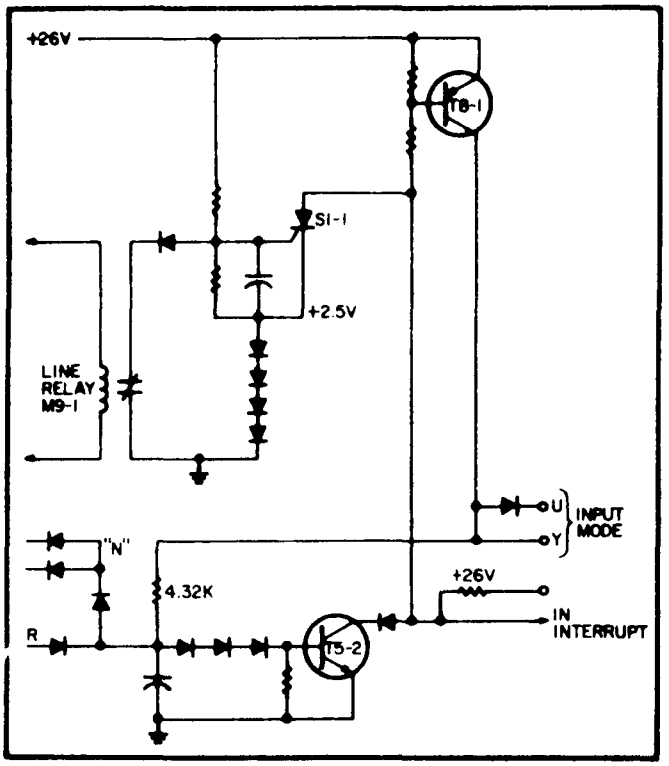


FIGURE 3. INPUT MODE SELECTION CIRCUIT

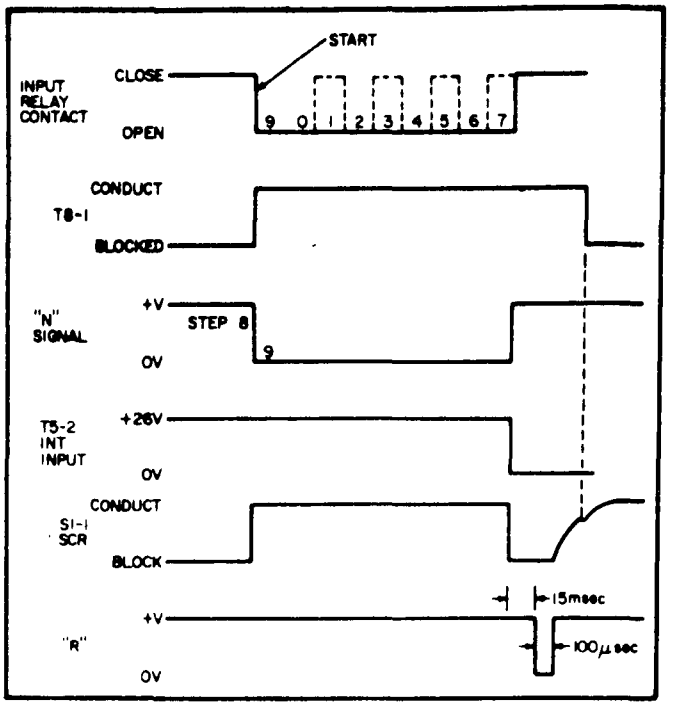


FIGURE 4. CIRCUIT TIMING CHART

The input load signal generation is shown in Figure 5. Input load is the output of transistor T5-5 and is used to set the selected SCR on the 4TO1 card. The input load timing is related to P1 and P2 pulse inputs as shown in Figure 6. Capacitor C23-1 is held discharged by UJT inhibit when the sequencer is not running. When the sequencer is reset and UJT goes positive, C23-1 will be allowed to charge through R28-5 and adjustable potentiometer M17-1. Either P1 or P2 will also discharge C23-1. The charging of C23-1 is shown in Figure 6. Note that P1 occurs first and discharges C23-1, through T5-3, then C23-1 is allowed to charge. When it reaches the required voltage, S2-1 will fire and T5-4 will turn on. This time is adjusted to 6.3 msec after P1 or P2 pulses. At P2 time, C23-1 will again be discharged. When T5-4 turns on, T5-5 blocks since its base current is shunted away by T5-4. The collector of T5-5 will be allowed to go positive if the M-9 mercury contact is opened. If it is closed, then T5-5 will be held at ground and the input load signal will be suppressed.

Figure 7 shows the control of the Tape Reader Relay Contact and the acknowledge signal from the I/O interface as a result of an input interrupt.

Relay M3-1 is a bistable relay which controls the tape reader advance in the Model 35 equipment. Transistor T5-1 will reset or open the tape reader contact while transistor T6-1 is used to set the relay contact closed.

When an input is done on the selected input channel,

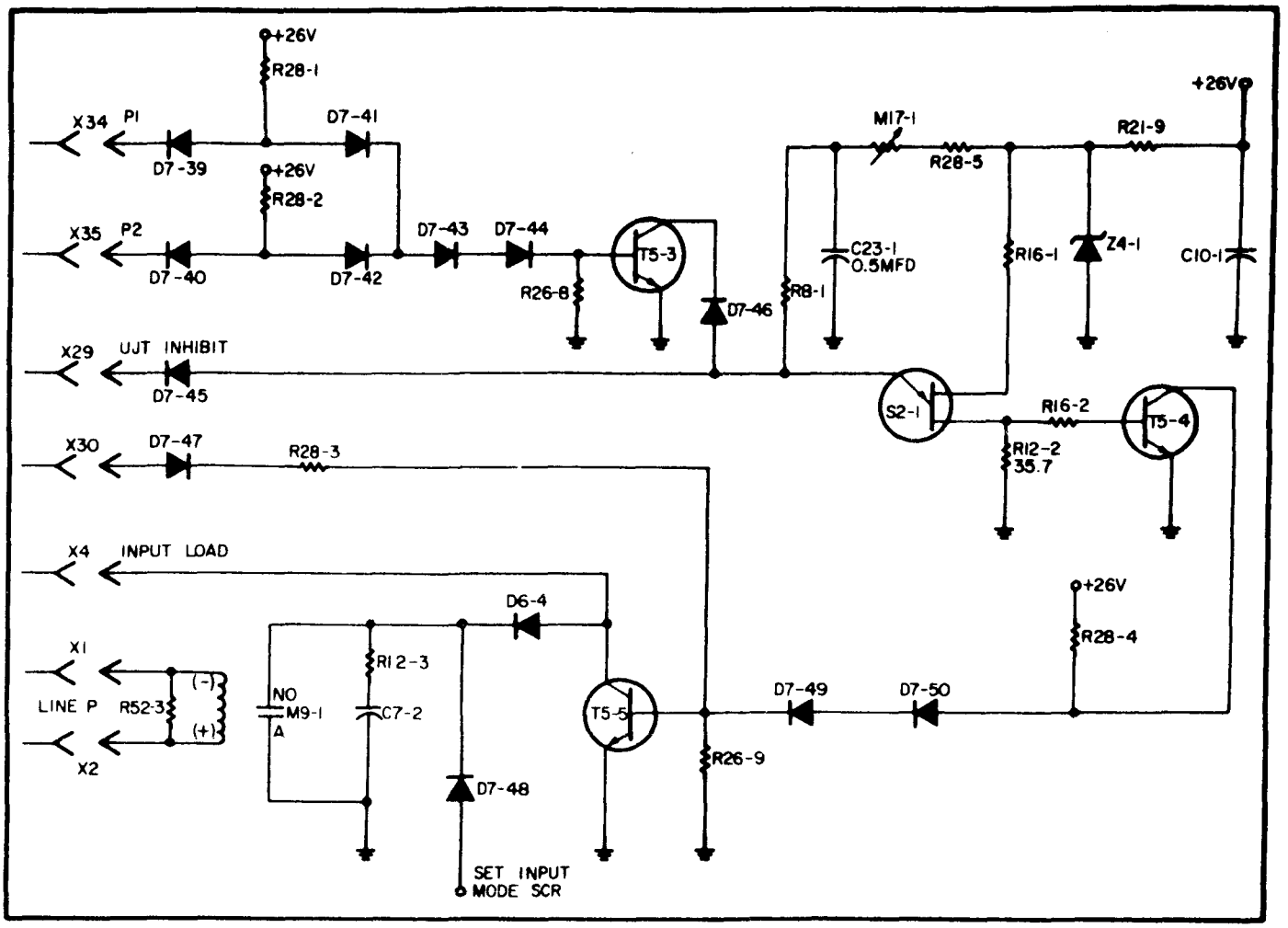


FIGURE 5. INPUT LOAD SIGNAL GENERATION

transformer X1-9 is pulsed with the 4.0 μsec pulse. Since the winding 1-2 is an open circuit, then a positive pulse will be generated from winding 5-6. This pulse will turn on T6-1 and the tape reader contact will be closed. The tape reader will advance and a character will be read. T6-1 conducting shunts base current away from T6-2 and it blocks. This causes T6-1 to be held on via R26-12 and D7-26.

The output of T6-2 is signal "Q" which, when it goes positive, will cause the register reset to occur and signal "R" is generated. Therefore, about 100 μsec after inputting the data, the register is cleared. Also, signal "R" is generated about 1.5 msec after the input command. Signal "R" will shunt the base current of T6-1 and cause it to block. When T6-1 blocks, T6-2 turns on and holds T6-1 off. Signal "Q" goes to ground.

The tape contact is now closed and a new character may be read beginning with Start which enables the sequencer. At step D·$\bar{C}$ of the sequence, the tape reader contact is reset and the reader will stop. When the data is read, the contact is again closed and the data register cleared.

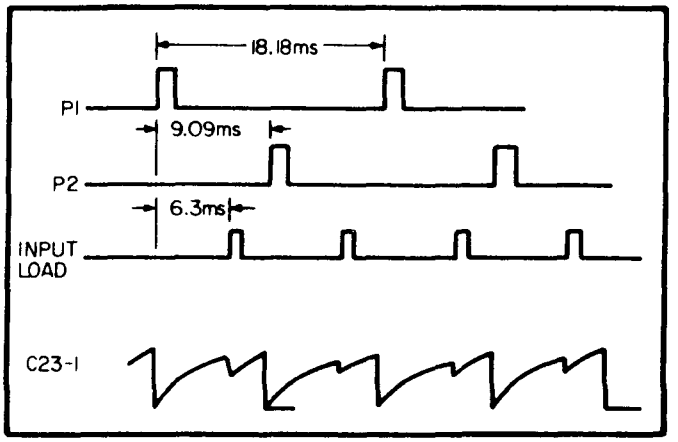


FIGURE 6. INPUT LOAD TIMING

2TN1 Potentiometer Adjustment For Input Load Signal

1. P1 and P2 pulses from TS Card should be connected to TN Card on pins X34 and X35.

2. Connect scope to TN Card at junction of C23-1 and M17-1 and adjust potentiometer to obtain 6.3 msec ramp as shown in Figure 6.

* * *

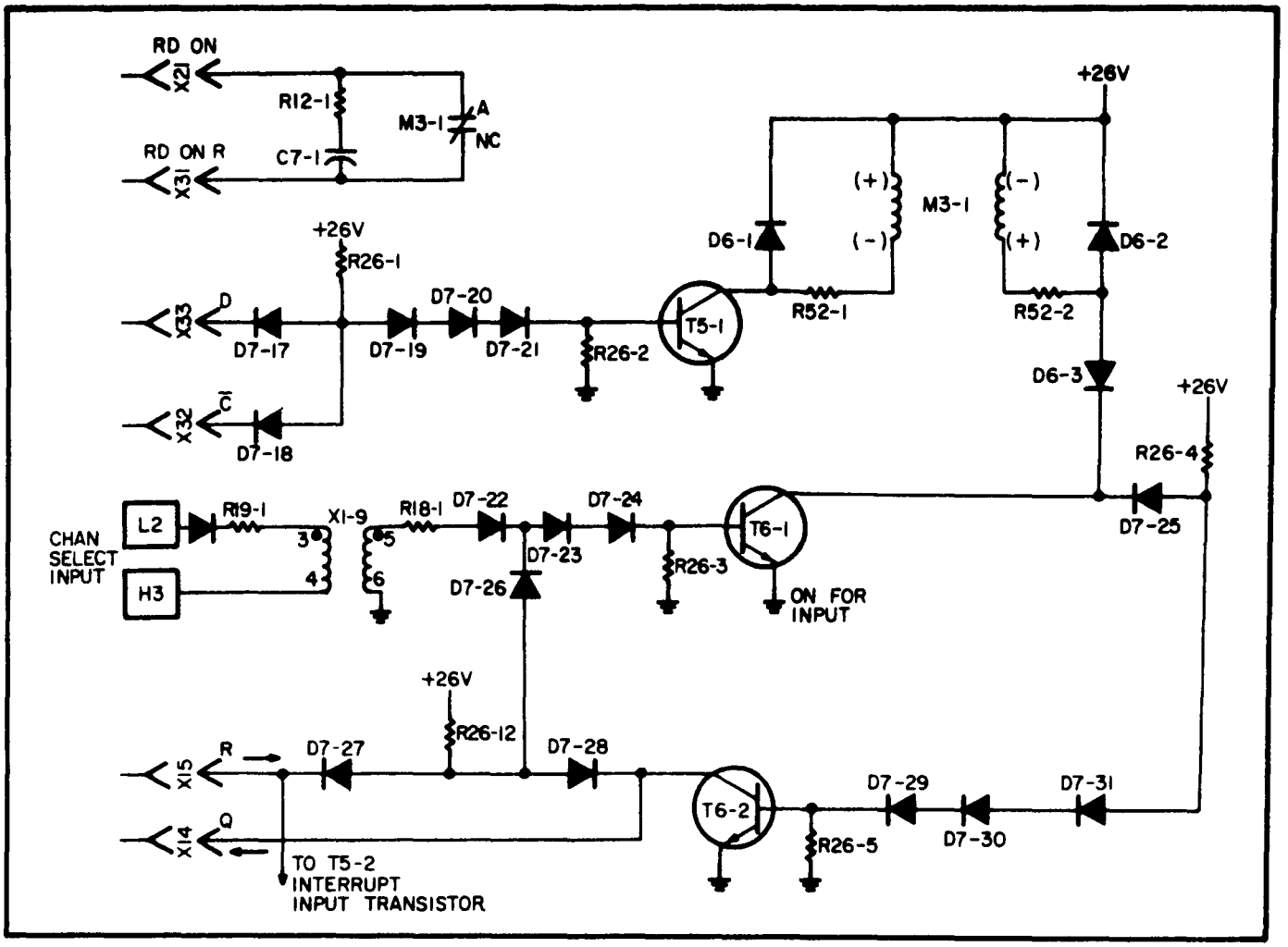


FIGURE 7. RELAY CONTACT CONTROL CIRCUIT

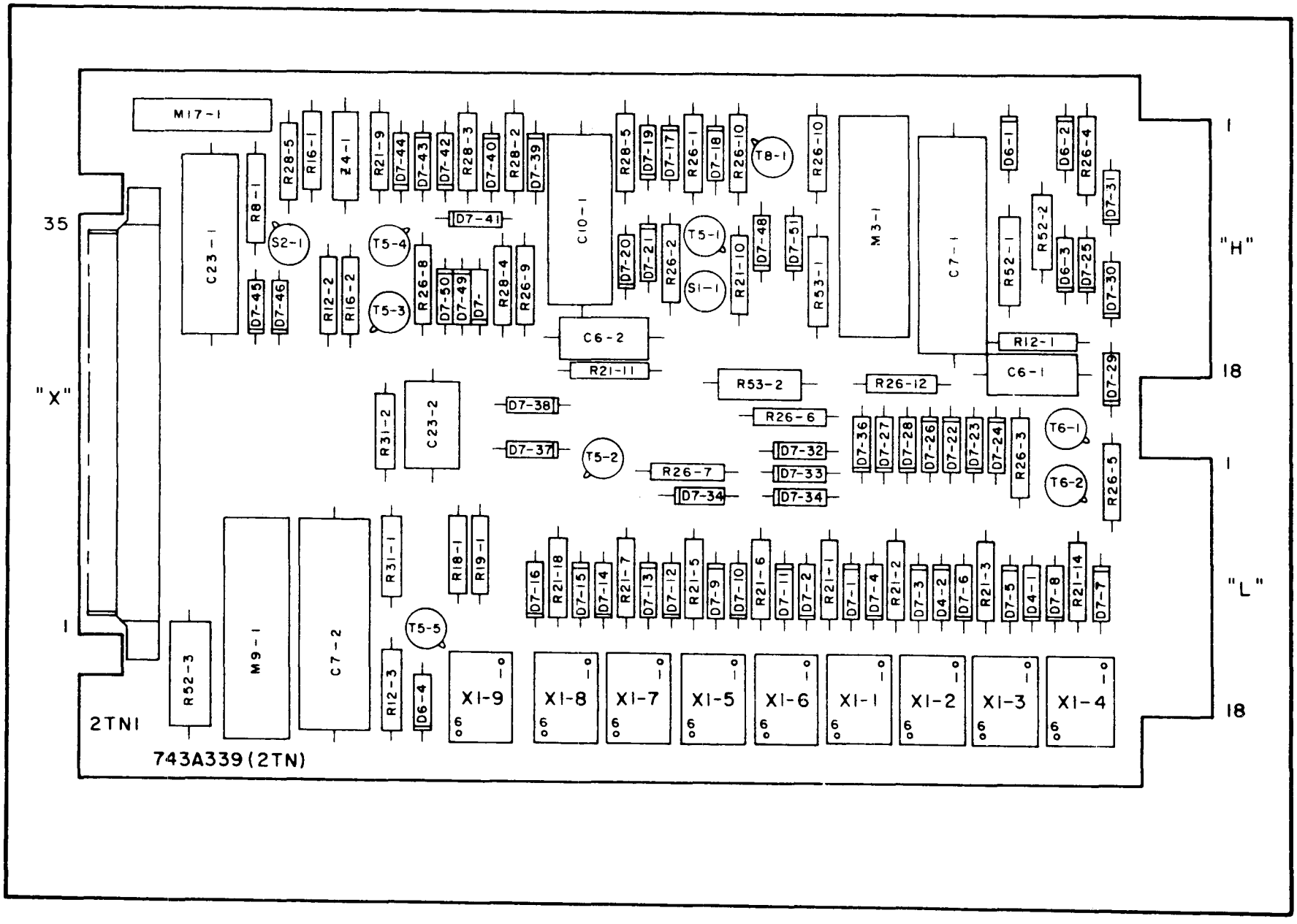


FIGURE 8. 2TN1 ASSEMBLY (REF. DWG. 743A339, SUB 16)

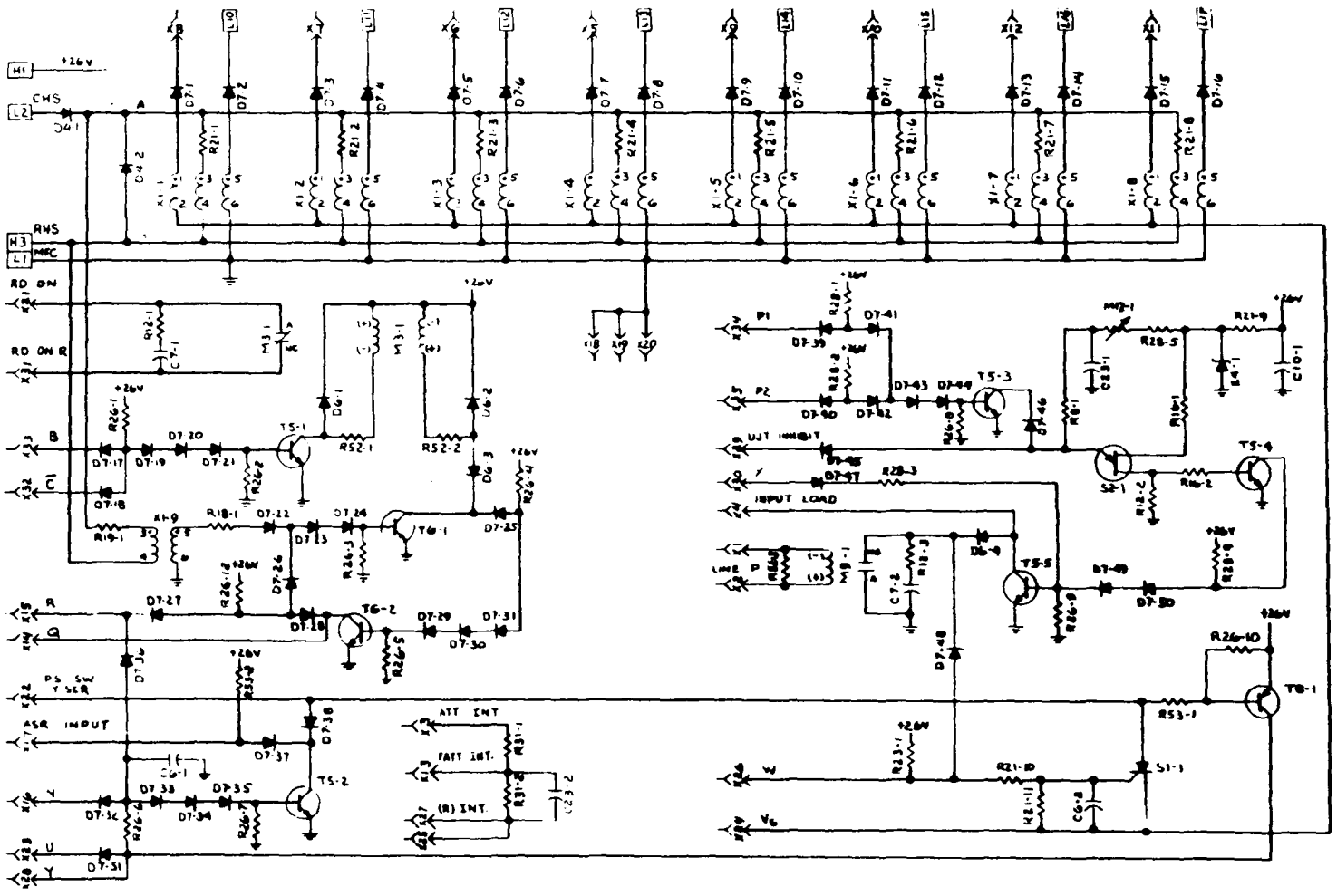


FIGURE 9. 2TN1 SCHEMATIC (REF. DWG. 743A339, SUB 16)

4TO1 - MODEL 35 TELETYPE DATA BUFFER MODULE

GENERAL DESCRIPTION

The 4TO1 module is used as a buffer between the I/O Interface and the Model 35 Teletype equipment for both input and output. The card contains a data buffer register. Figure 1 is an application block diagram of this card.

CIRCUIT SPECIFICATIONS

Input Requirements

I/O Interface

- Data - Logic "0"; 1.1V maximum; Logic "1"; 4.0V minimum.
- Channel half-select - 4.0 μsec pulse, 11V minimum.

3TS1 Signals

- Reset - 0 volts will reset SCR Buffer Register.
- Sequencer Outputs - 0 volts implies "0"; positive voltage "1".
- Output Mode - zero volts implies output mode (M).
- Motor ON/OFF control - zero volts implies turn on motor (L).
- "K" line relay driver input - zero volts-de-energized, + 7.0V-energized.

2TN1 Signals

- Data - Logic "0" - 1.1V maximum; Logic "1" 4.0V minimum.
- Input Load - 200 μsec pulse will set selected SCR.

Power Requirements

The 4TO1 module receives power from the +26V I/O interface power supply.

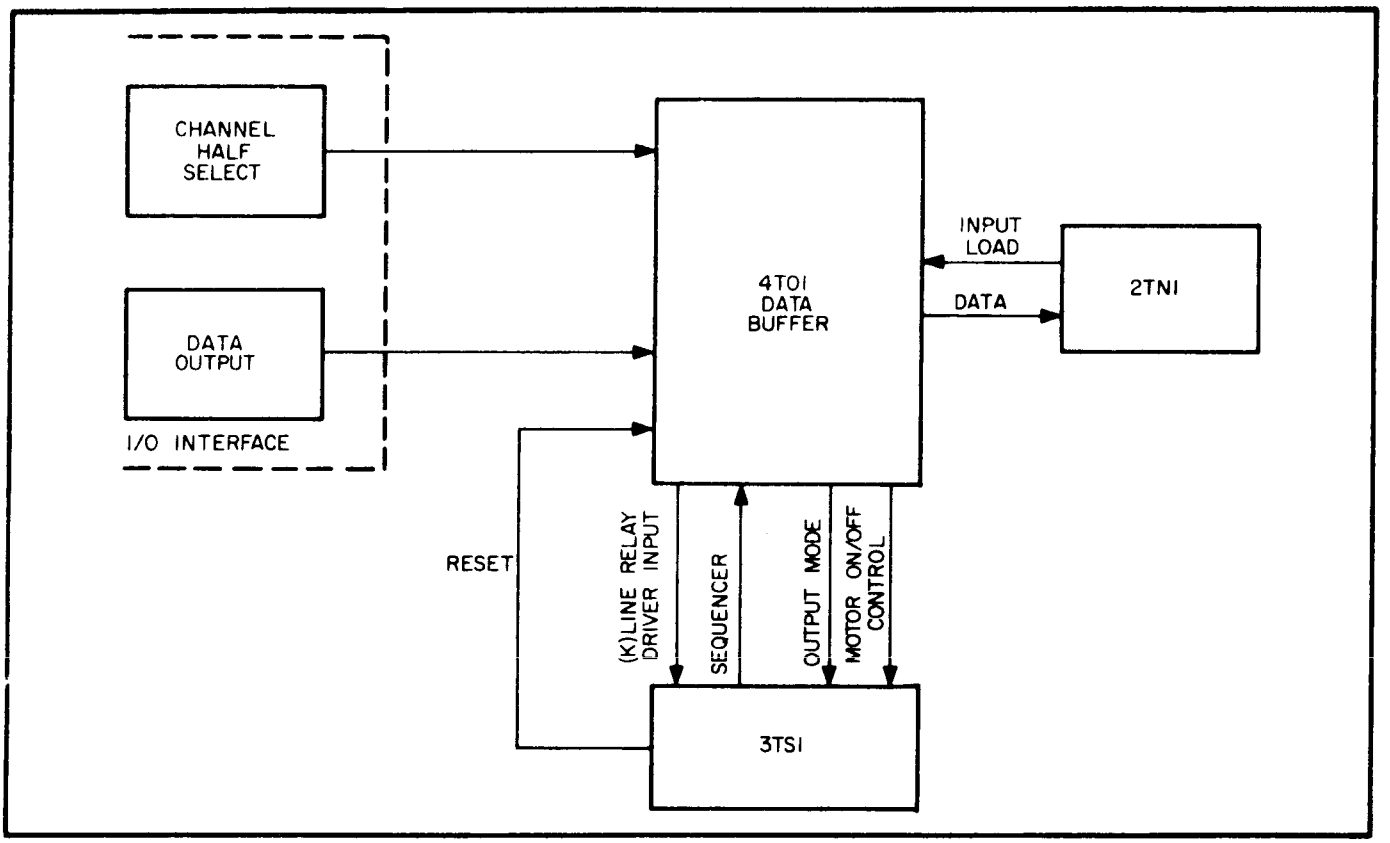


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT DESCRIPTION

The 4TO1 card contains the following:

- The 8-bit data register which stores the 8 bits of data either as output from the computer or as input from the Model 35 equipment.

- Pulse transformers which are connected to the Output Data register.

- Sequencer decoding for the input and output of serial data.

- Output "mode" SCR, signal M, which indicates output mode of operation.

- Motor on/off bistable, which controls motor on/off relay (signal L).

Figure 2 illustrates a typical Data Bit of the 8-bit Buffer register. This data bit may be set by output from the I/O interface or by input from the Model 35 equipment.

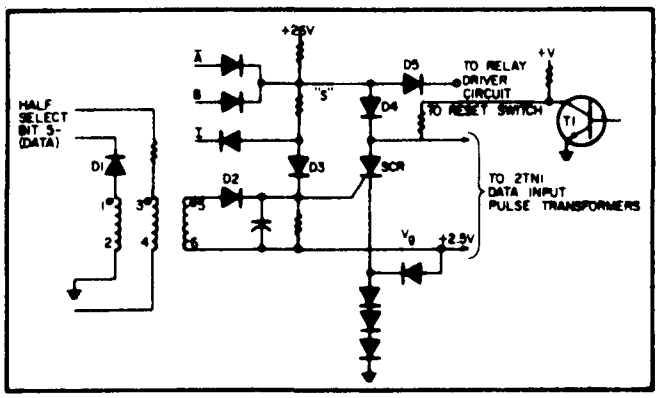


FIGURE 2. ONE BIT CIRCUIT OF 8-BIT DATA REGISTER

If Bit 5, for example, is a logical "0" from the I/O interface, this will cause terminal 1 of the winding 1-2 to be grounded. Since terminal 2 is tied to ground, this winding will appear as a short circuit. If Bit 5 is a logical "1", winding 1-2 will appear to be an open circuit since the series diode is back biased.

I/O interface selects the channel with a 4.0 μsec pulse across winding 3-4 and if winding 1-2 appears as a short circuit, a small voltage will be generated across winding 5-6 and the diode, D-2, will not conduct and the SCR will not be set. If, however, winding 1-2 appears as an open circuit (logical "1"), then, when the channel pulse occurs, sufficient voltage will appear across winding 5-6 so that diode, D-2, will conduct and the SCR will be set. The SCR anode is returned to +26V through resistor R1. This provides holding current for the SCR.

Diode Inputs $\bar{A}$ and B serve to select the SCR during output. $\bar{A}$ and B are sequencer outputs and act as a logical "AND", allowing point "S" to go positive. Signal "I" is the input load signal and is normally at ground. If this signal goes positive when $\bar{A}$ and B are selected, then the SCR is set through diode D-3.

Diode Inputs $\bar{A}$ and B are also used to select the SCR during output. Inputs $\bar{A}$ and B and diode D-4 act as an "AND" gate so that if the SCR is set, point "S" will be held at +2V. If the SCR is blocked, point "S" will be allowed to go more positive. Diode D-5 is the output of this "AND" gate and it is "ORed" together with the other 7 data bits to drive the relay driver circuit.

The anode of the SCR is also connected to pulse transformers for inputting data to the I/O interface. If the SCR is conducting it will appear as a short circuit across winding 1-2. If the SCR is blocked it will appear as an open circuit across winding 1-2 of the input transformer. When the input channel is selected and pulsed, a logical "1" will be stored if the SCR is blocked, and a logical "0" will be stored if the SCR is conducting.

Reset Switch

The outputs of the 8 SCR's which make up the buffer register are connected through holding resistors to a "reset" switch. This switch is a transistor which is blocked as shown in Figure 2. When T1 conducts it will "shunt" the SCR holding current since the voltage drop across the transistor to ground is less than the voltage across the SCR and the 3 series diodes.

Figure 3 shows the motor ON/OFF bistable which is controlled by Bit 13 and Bit 0. If Bit 13 is a logical "one", then a positive pulse will appear across winding 5-6 and the transistor T6-1 will be turned on. This transistor is held on by transistor T6-2 being blocked. Transistor T6-2 will conduct if Bit 0 is a logic "one". When this transistor conducts, it shunts the base current to transistor T6-1 and T6-1 will block. Transistor T6-2 is held on since T6-1 has blocked and the base current to T6-2 is no longer shunted.

The output of T6-1, signal L, drives the mercury wetted motor "ON" relay. This relay is mounted on the TS card.

Also shown in Figure 3 is the "Output Mode" SCR which is set each time the channel is addressed. Note that winding 1-2 is not connected, and as such, will appear as an open circuit when the 4 μsec channel pulse occurs, causing the SCR to be set. Signal "M" is used to indicate that the computer has performed an output.

* * *

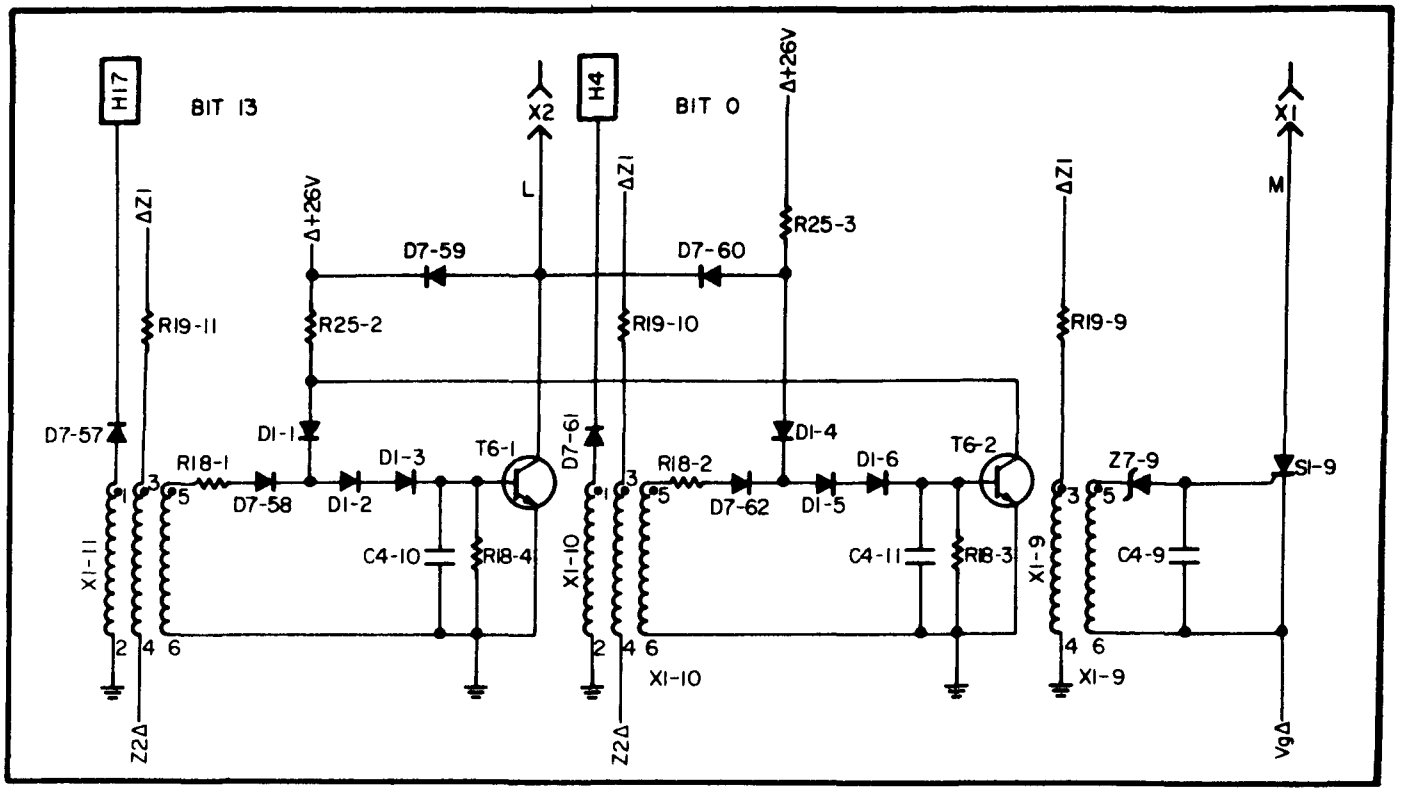


FIGURE 3. MOTOR ON/OFF BISTABLE AND OUTPUT MODE SWITCH

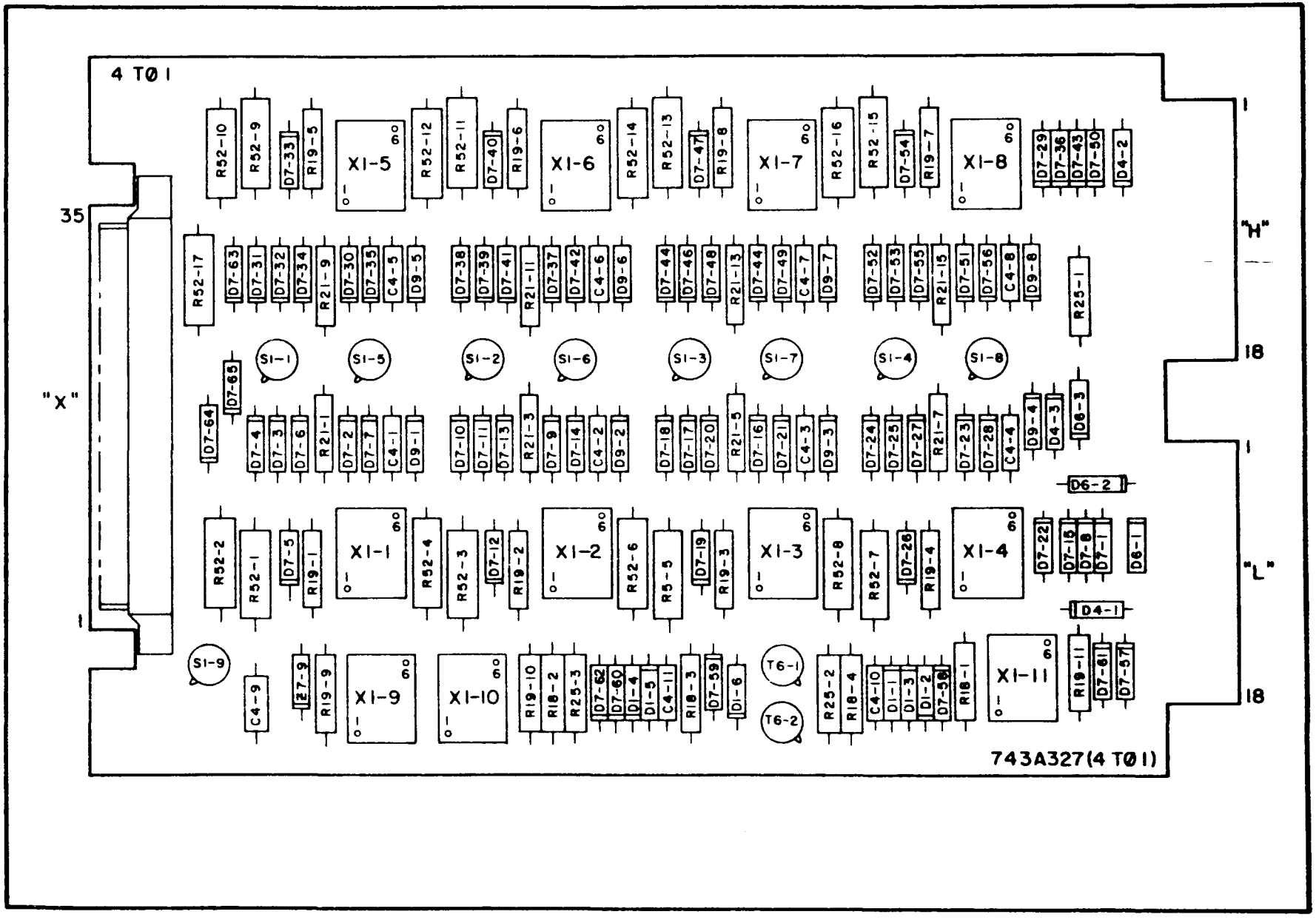


FIGURE 4. 4TO1 ASSEMBLY (REF. DWG. 743A327, SUB 16)

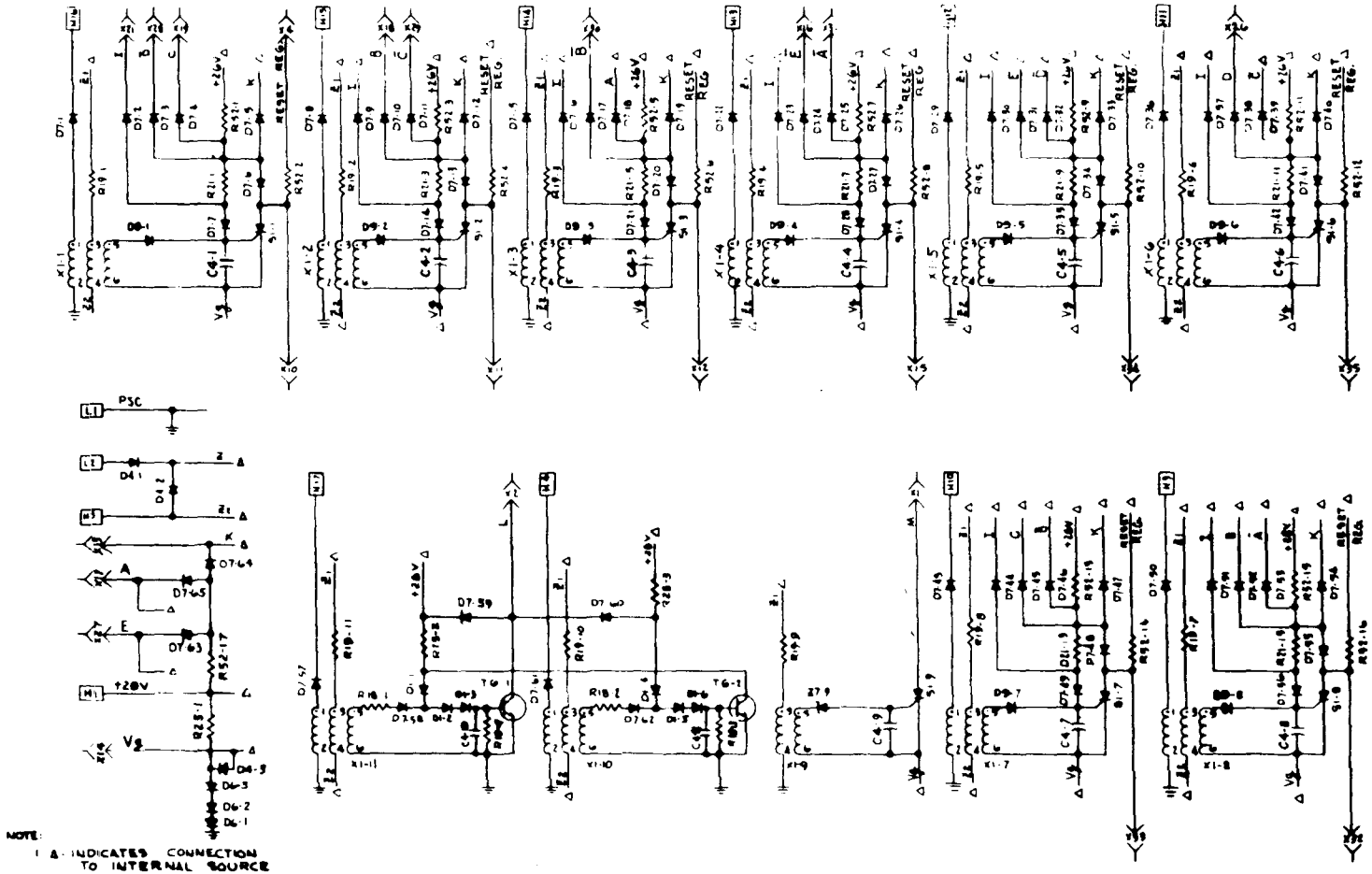


FIGURE 5. 4TO1 SCHEMATIC (REF. DWG. 743A327, SUB 16)

1TP1 - TAPE PUNCH AMPLIFIER AND CONTROL

GENERAL DESCRIPTION

This module is used to accept data input from the 1DE3 buffer and amplify these signals to drive the punch magnets. This module contains buffer amplifiers and control. An application block diagram is shown in Figure 1.

CIRCUIT SPECIFICATIONS

Input Requirements

- Data Input - zero volts input - hole will be punched.

- Magnetic pickup pulse - 4V pulse, 0.5 msec from Tape Punch.

Output Requirements

- Data Output - zero volts output - hole will be punched.

- Reset Pulse - a transition of zero volts to +28 V sent to 1DE3 to cause 4.5 msec delay and initiate interrupt.

Power Requirements

- 1TP1 module receives power from 28Vdc, 8A power supply in the punch interface package.

CIRCUIT DESCRIPTION

A typical amplifier (one of nine) and the associated control is shown in Figure 2.

The requirement of the control circuitry of the 1TP1 card is to accept the magnetic timing pulse from the punch and energize the power transistors associated with each of the selected SCR's in the output register.

In the quiescent state, transistor T4-10 is conducting. Note that this prevents T4-1 through T4-9 from conducting since it holds their bases more positive than the emitters. T4-1 through T4-9 will conduct if T4-10 blocks, allowing their base circuits to go negative. T4-10 is normally conducting because T8-1 is blocked. T8-1 will conduct when T5-2 conducts. T8-1 and T5-2 form a bistable so that if T5-2 is turned on, it in turn biases T8-1 on, which further holds T5-2 on so that the bistable latches "on".

T5-1 is connected to the magnetic pickup and is controlled by this pulse. T5-1, when enabled, turns off turns T5-2 on. Before any action can occur, the feed hole SCR must be selected. This provides an emitter current path for both T5-1 and T5-2. Once the SCR has been turned on, the next magnetic pickup pulse will cause T5-1 to be turned off and T5-2 to turn on; this causes T8-1 to come "on" and T4-10 blocks. The power transistors, T4-1 to T4-9, with their corresponding SCR on, will conduct, and the magnet in the punch will be energized. The magnets will remain energized for as long as the T5-2/T8-1 bistable is latched "ON". This bistable may be reset by opening the feed hole SCR on the 1DE3 card, which removes the emitter current path for transistor T5-2.

When T8-1 conducts due to magnetic pickup pulse its collector goes positive. This positive going signal causes the control on the 1DE3 card to begin timing the length of time that the magnets are energized.

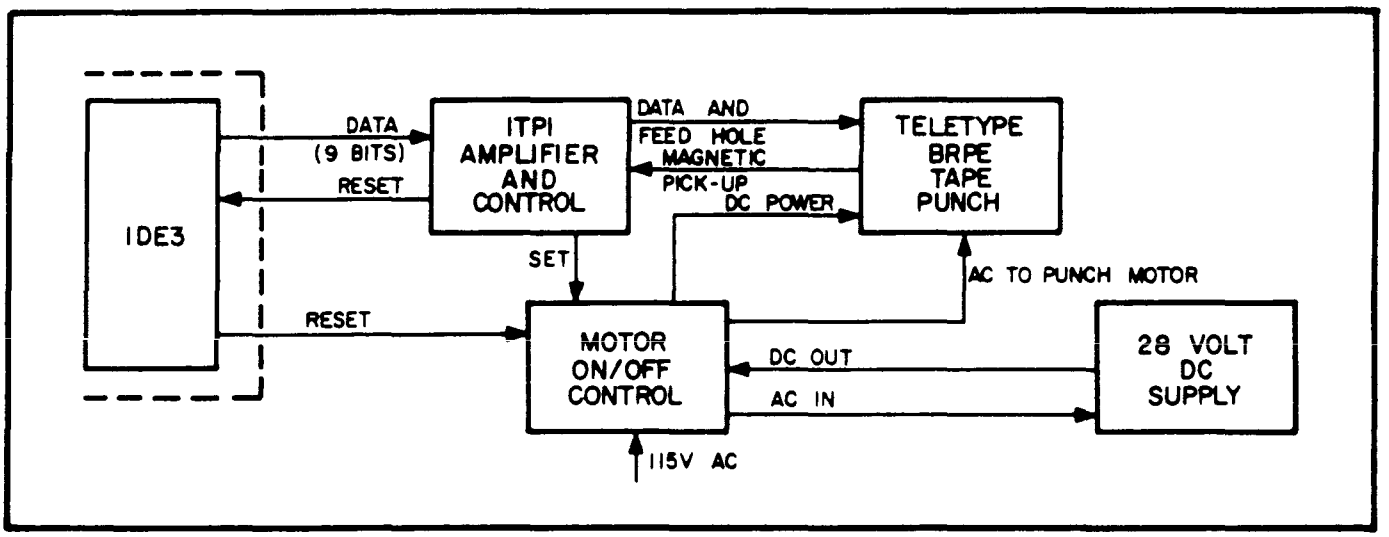


FIGURE 1. APPLICATION BLOCK DIAGRAM

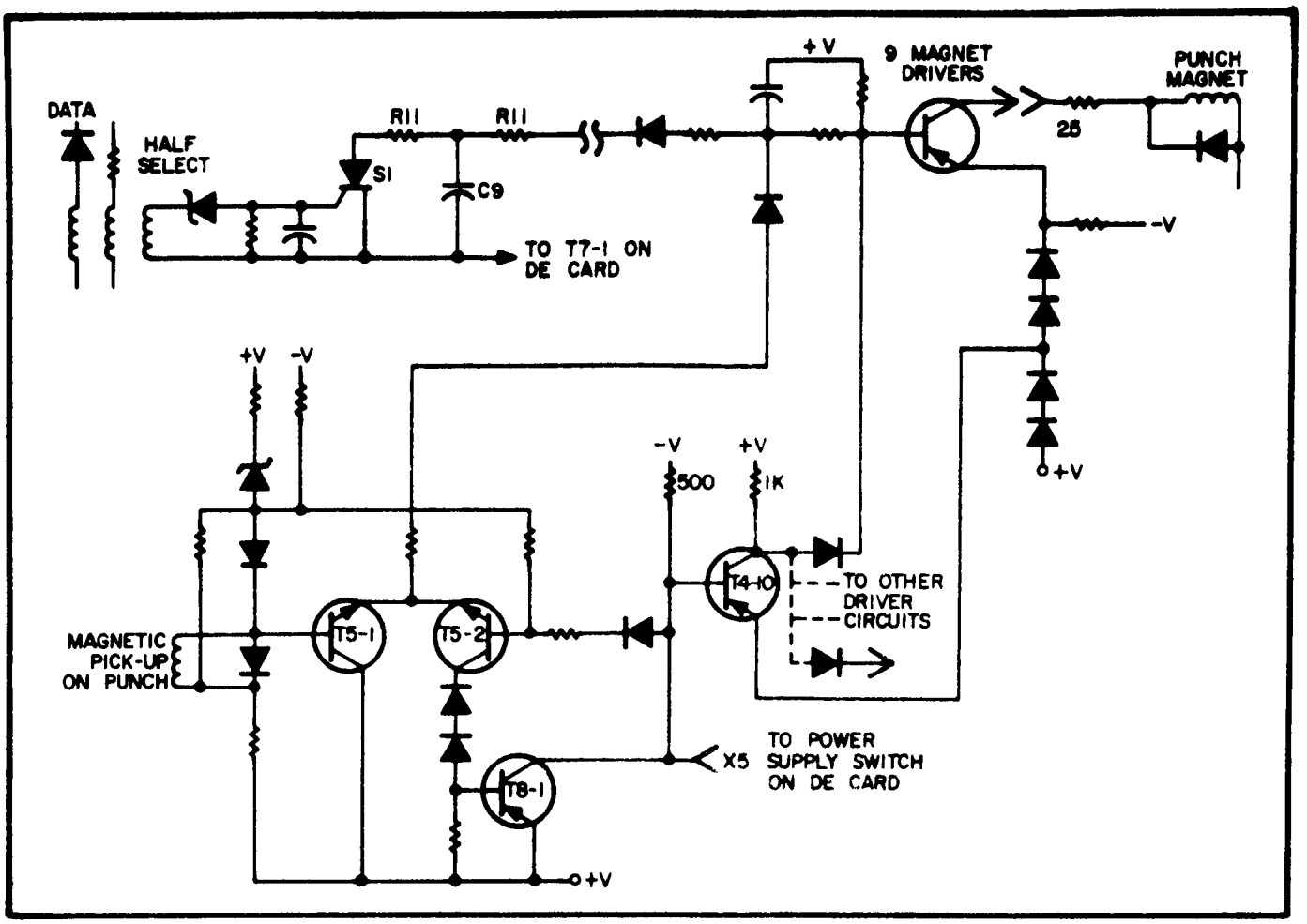


FIGURE 2. TYPICAL BIT AMPLIFIER AND CONTROL CIRCUIT

* * *

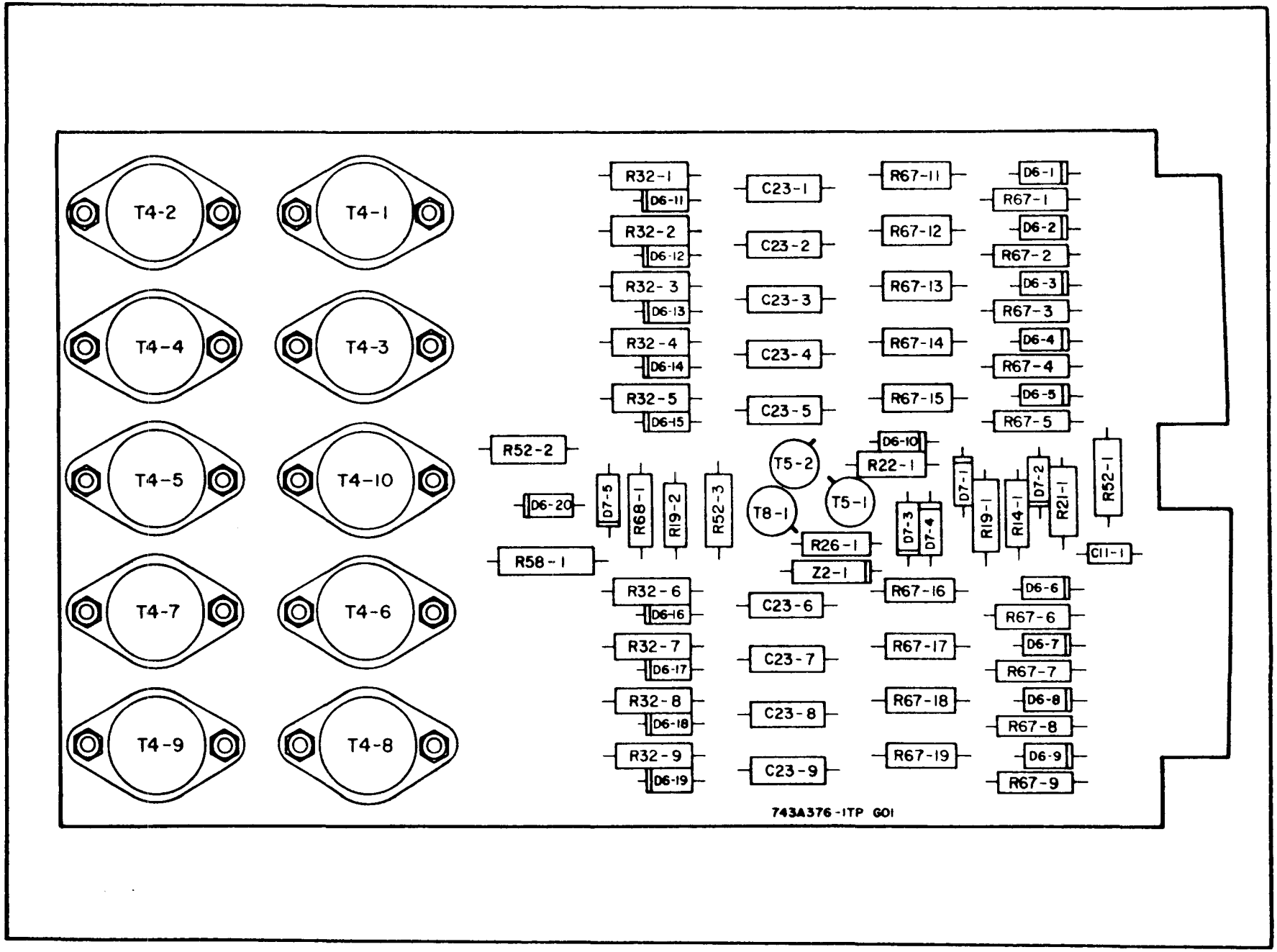


FIGURE 3. 1TP1 ASSEMBLY (REF. DWG. 743A376, SUB 5)

3TS1 - MODEL 35 TELETYPE CONTROL CARD

GENERAL DESCRIPTION

The 3TS1 module is used as control between the Model 35 Teletype equipment and the 4TO1 buffer card. This card contains control and sequence circuitry. An application block diagram is shown in Figure 1.

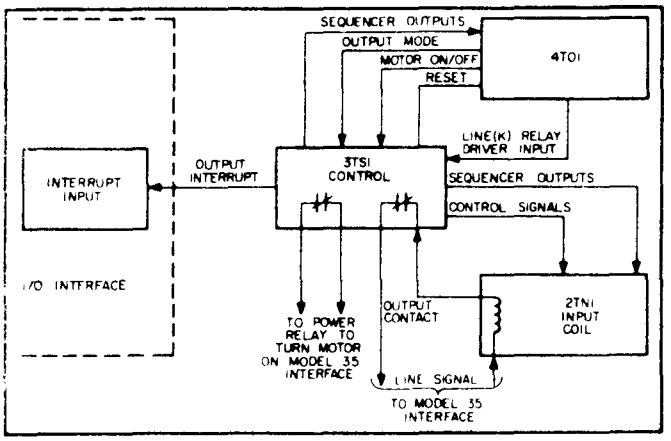


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Signal Requirements

I/O Interface

- Interrupt - The interrupt signal is nominally +6V tied to a 1k pull up resistor.

4TO1 Signals

- Reset - zero volts will reset SCR buffer register.
- Sequence outputs - zero volts implies "zero". +7V implies "one".
- Output Mode - zero volts implies output mode (M).
- Motor ON/OFF control - zero volts implies turn on motor (L).
- "K" line relay driver input - zero volts de-energized, + 7.0V energized.

2TN1 Signals

- Sequencer outputs - zero volts implies "zero" +7V implies "one".
- Control signals - covered in circuit description.

Model 35 Interface

- Mercury Relay contact used to pick power relay to turn on Model 35 equipment.
- Output Contact - opens and closes line to Model 35 equipment.

Power Requirements

The 3TS1 module receives power from the +26V I/O interface power supply.

CIRCUIT DESCRIPTION

3TS1 card contains the following:

- A 5-stage counter used for converting serial to parallel and parallel to serial data.
- A unijunction oscillator (P1 and P2 outputs), which steps the 5-stage counter.
- The register reset circuit used to clear SCR register at the end of data transfer.
- Output interrupt circuit "asking" for new output character in output mode.
- Line contact used for sending serial data to Model 35 equipment.
- "Reset" signal used to reset 5-stage counter at beginning of data transfer.
- Motor on/off mercury relay used to pick motor on/off relay located at the Model 35 equipment.

Figure 2 shows the 5-stage counter using NAND logic to obtain the basic timing of the Model 35 equipment. The timing of the counter is shown in Figure 4. Note that the counter is reset to $E \cdot A$ (step 9). This is defined as "start" to the Model 35 equipment. The counter is stepped along by P1 and P2 pulses which occur alternately every 9.09 msec. The counter will remain in the reset condition until the first P1 pulse occurs and since E is a "one", the A bistable will be reset by $P1 \cdot E$, $P2 \cdot \overline{A}$ will reset bistable B, etc. Figure 4 indicates that by "AND"-ing pairs of these outputs it is possible to have 10 different states. "Stop" is defined as $D \cdot \overline{E}$.

Figure 3 is the unijunction oscillator which generates P1 and P2. In the quiescent state unijunction transistor

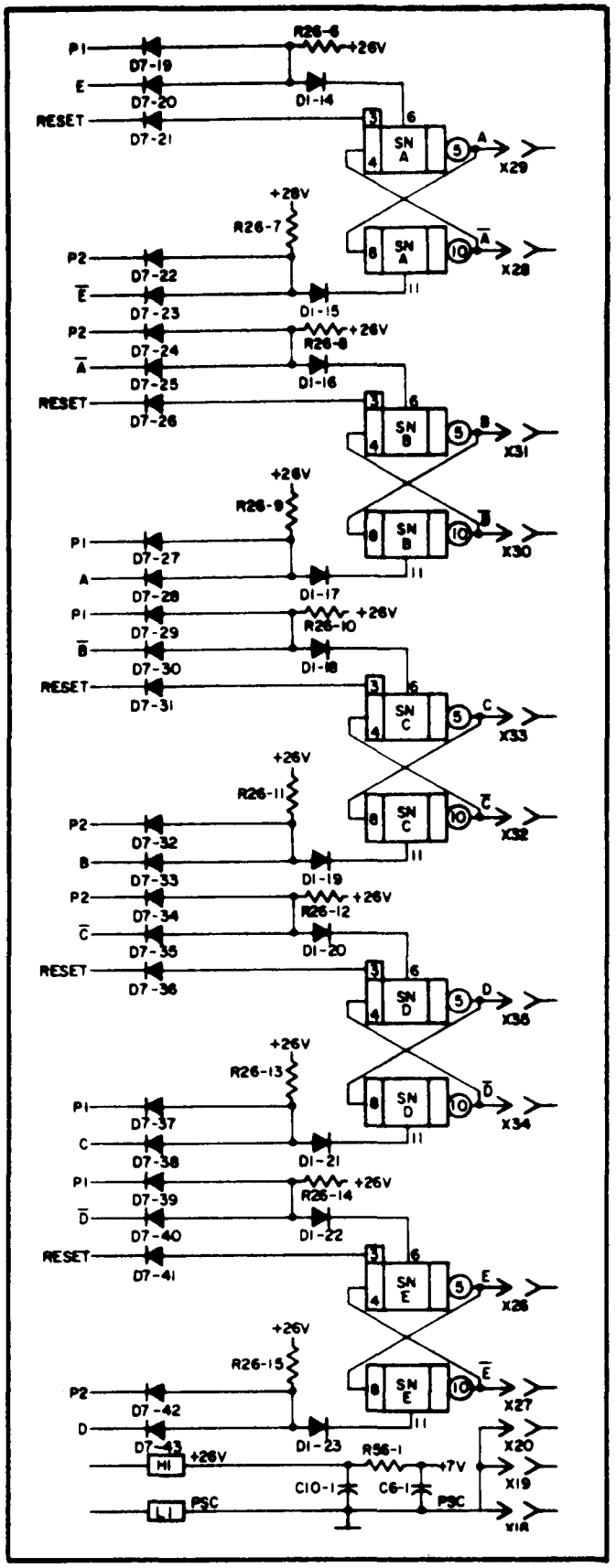


FIGURE 2. 5-STAGE COUNTER CIRCUIT

(UJT) inhibits P1 and P2 by grounding the outputs of the slow NAND (SN-F). When a character is transmitted (input or output) UJT is removed; a reset pulse sets SN-F-10 so that P1 is always first to occur. Zener diode Z4-1 provides an accurate dc voltage from which to adjust P1 and P2.

P1 and P2 are obtained by using two timing capacitor circuits and a diode OR gate to the unijunction emitter (S2-2). The slow NAND flip-flop (SN-F) alternates which timing circuit is used. Each timing capacitor is coupled to a transistor, T5-3 and T5-4. When a timing circuit causes the UJT to fire, its corresponding transistor causes an output pulse to be generated, the flip-flop to change state, and the alternate pulse to be generated at the end of the next period.

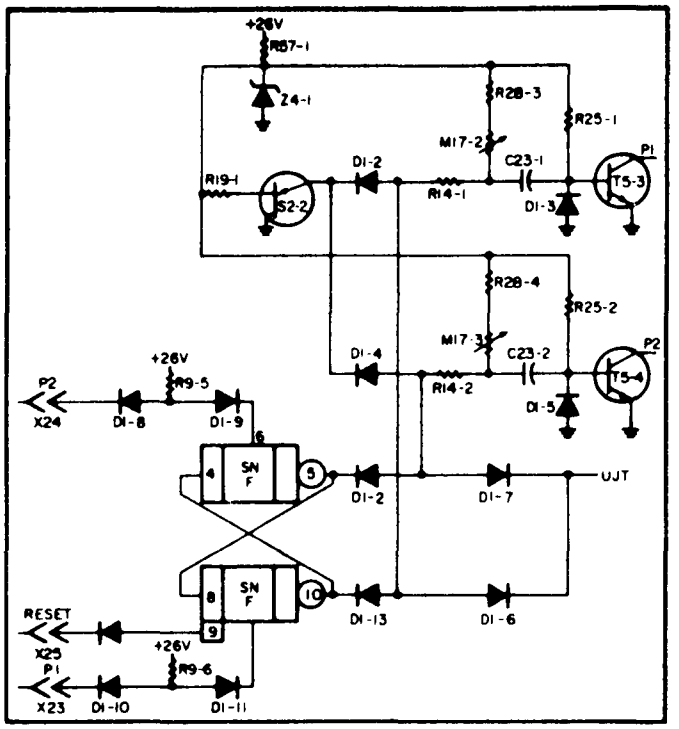


FIGURE 3. UNIJUNCTION OSCILLATOR CIRCUIT

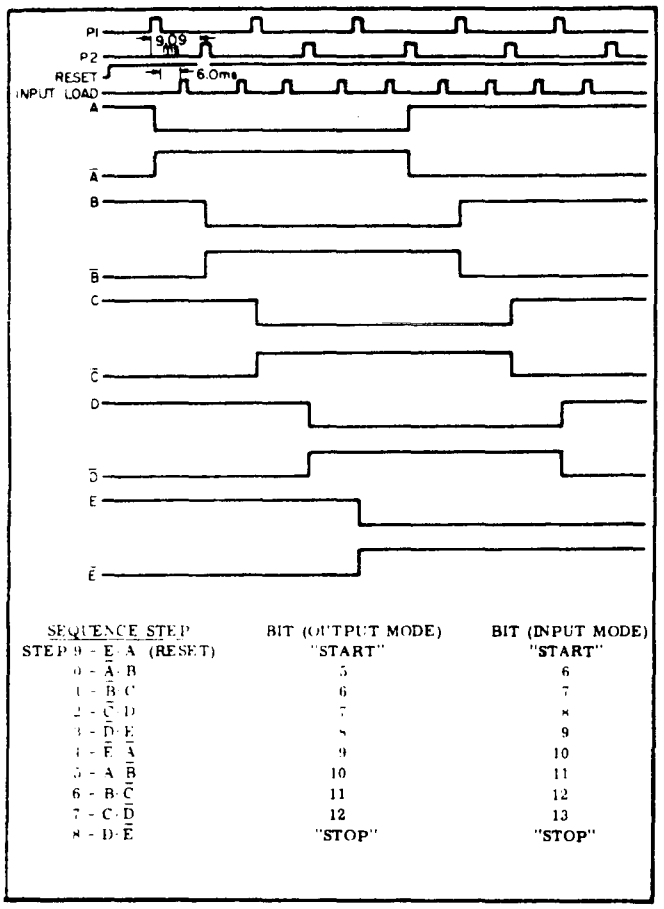
Figure 5 shows the relay driver circuits which control relay M9-1. The normally closed contacts are in series with the line signal to the Model 35 equipment. If the signal "K" is allowed to go more positive than the zener breakdown voltage of Z2-1, then transistor T5-6 will conduct and the relay will be picked up and the line contact will open. The return path for the emitter of T5-6 is through slow NAND SN-H-5 to PSC. This slow NAND will conduct if T8-1 conducts, since T8-1 provides base current to SN-H-5. The input to T8-1 is signal "M" which implies output mode when it is + 26V. Therefore, only when "M" is + 2V (output mode) will the relay driver circuit T5-6 be enabled.

Signal "X" implies output mode when it is a + 26V because T8-1 is conducting.

Reset transistor T5-6 will be pulsed if either "X" or "U" goes positive. "U" will go to positive 26V during the input mode. At the beginning of a data transfer, a reset pulse is generated, and is used to reset the 5-stage counter.

Relay M9-2 will conduct if signal "L" goes to zero volts. The normally open contact will close. This contact is used for turning the Model 35 motor on and off.

Figure 6 shows some additional control and timing required for the Model 35 equipment. In the quiescent state the 5-stage counter is stopped in the $D \cdot \overline{E}$ state so that signal "N" is positive. This causes slow NAND SN-H-10 to conduct and UFT to be zero volts. This signal inhibits the unijunction oscillator as mentioned previously.



SEQUENCE STEP	BIT (OUTPUT MODE)	BIT (INPUT MODE)
STEP 9 - $\overline{E}$ A (RESET)	"START"	"START"
0 - $\overline{A}$ B	5	6
1 - $\overline{B}$ C	6	7
2 - $\overline{C}$ D	7	8
3 - $\overline{D}$ E	8	9
4 - $\overline{E}$ $\overline{A}$	9	10
5 - A $\overline{B}$	10	11
6 - B $\overline{C}$	11	12
7 - C $\overline{D}$	12	13
8 - D $\overline{E}$	"STOP"	"STOP"

FIGURE 4. INPUT OUTPUT SCAN SEQUENCE

The output of SN-G-5 is the output interrupt signal and this slow NAND circuit is enabled only in the output mode, i.e., "X" is positive 26V.

The register reset signal will go to zero volts if either signal "Q" or SN-G-10 goes positive. When this happens T5-5 will conduct and the SCR register on the 4TO1 card will be reset.

Signal "R" will be generated (zero volts) each time sequencer step $\overline{D} \cdot E$ occurs either in the input mode or the output mode. Transistor T5-1 is driven by unijunction transistor S2-1. This transistor has two timing circuits associated with it; one for input (X) and one for input (Y). When $\overline{D} \cdot E$ occurs the base circuit of S2-1 is allowed to go positive depending on which RC timing path is enabled. For the output mode the unijunction S2-1 uses R28-1, M17-1, and C22-1; for the input mode it is R30 and C21-1. For output, "R" will conduct for 100 μsec about 20 msec after $D \cdot \overline{E}$, while for input, this pulse occurs about 1.5 msec after $D \cdot \overline{E}$.

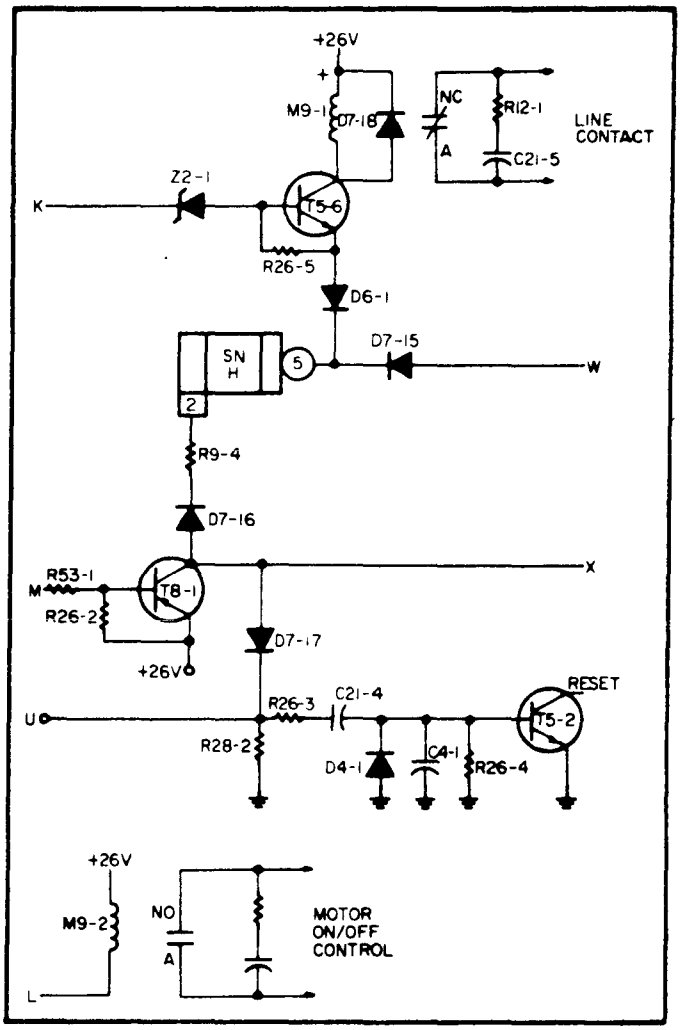


FIGURE 5. RELAY DRIVER CIRCUIT

Refer to Figure 7 which indicates the timing of the control circuitry during the output mode. "N" ($D \cdot \overline{E}$) is at a positive voltage in the quiescent state. When an output occurs, the sequencer is reset to step 9 and the UJT inhibit signal goes positive enabling the sequencer signal "X" to go to 26V. When step 8 of sequencer occurs, unijunction oscillator is inhibited and SN-G-5 output goes to zero volts. This resets the "M" SCR; however,

"X" is still +26V, since SN-G-5 acts to hold in the "X" transistor T8-1. Since "N" is permitted to go positive, the 20 msec time delay will be enabled, after which the 100 μsec "R" signal will occur. This signal blocks SN-G-5, causing "X" (T8-1) to open. Since the slow NAND SN-G-5 blocks, this positive transition causes the interrupt to the I/O interface. Also while SN-G-5 is conducting, this causes the Register Reset signal (T5-5).

The Input mode is similar to the Output mode except that the selected RC network for S2-1 has a time constant of 1.5 msec; i.e., 1.5 msec after step 8 occurs, S2-1 will conduct, causing "R". "R" is now routed to the 2TN1 card which results in an input interrupt to the I/O interface. When the input occurs Signal "Q" goes positive and the SCR register is cleared and another "R" signal is generated. This resets "Q" to zero volts.

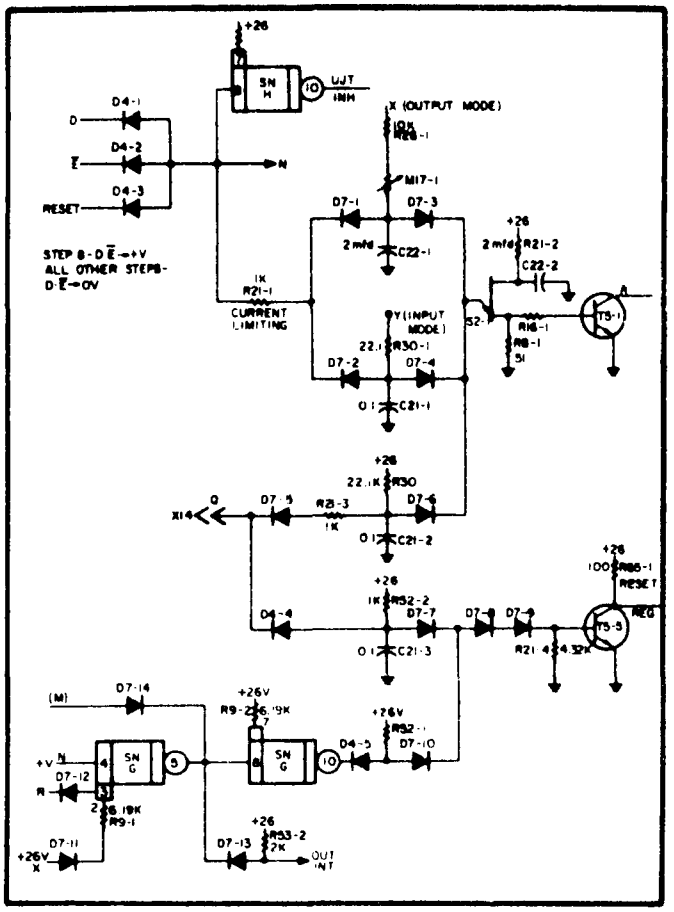


FIGURE 6. CONTROL AND TIMING CIRCUIT

Potentiometer Adjustment

Equipment Required

- 26V to 29V power supply.
- Dual beam scope.
- **Connector setup - 2 Sylvania and 1 Elco with pins made available.**

Adjustment of P1 and P2 on TS Card

1. Connect TS card to Elco and Sylvania connectors.
2. Connect -V to pin L1 on Sylvania.
3. Connect +V to pin H1 on Sylvania.
4. Connect -V to pins 14 and 8 on Elco connector.
5. Connect one channel of scope to Elco X23-(P1).
6. Connect other channel to Elco X24-(P2).
7. Display P1 and P2 trace on scope.
8. Adjust one of two adjacent pots to obtain P2 occurring 9.1 msec after P1.
9. Sync scope on P2 and adjust other adjacent pot to obtain P1 occurring 9.1 msec after P2, shown in "A" of Figure 8.
10. Observe output of "F" NAND on TS card to be 9.1 msec square wave.
11. Observe sequencer outputs "A" through "E" to be sure all NANDS are operating.
12. Observe "Reset" and Elco pin X25.

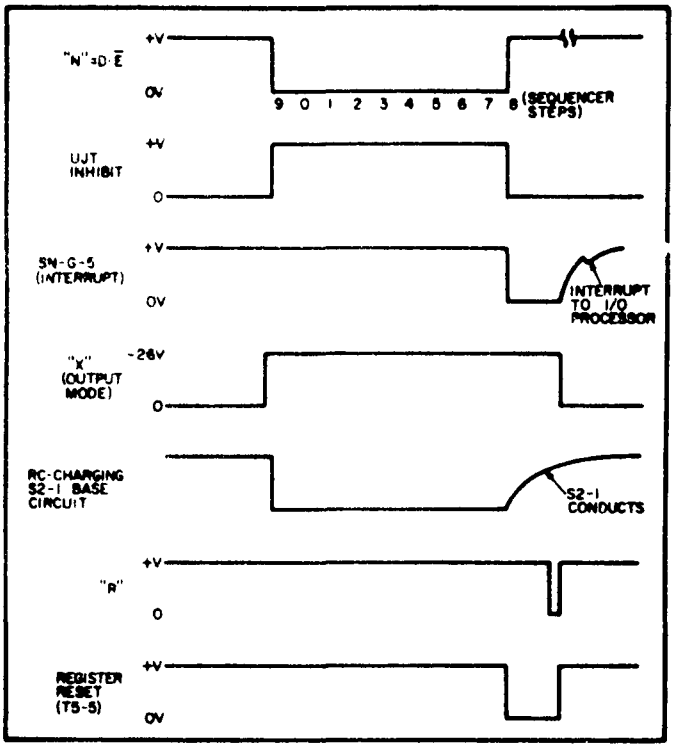


FIGURE 7. OUTPUT MODE TIMING CHART

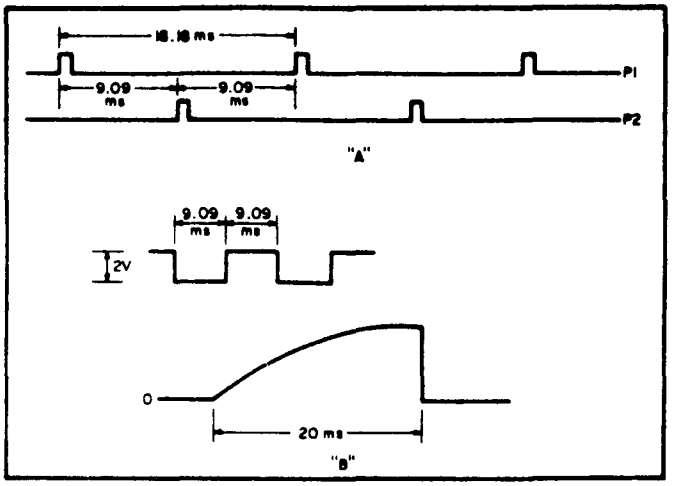


FIGURE 8. POTENTIOMETER ADJUSTMENT TIMING CHART

20 msec Delay (ramp) on TS Card

1. Remove connection X8 to -V.

2. Connect X13, X14, X26, and X34 to X18 (-V).

3. Connect scope to junction of C22-1 and M17-1 and trigger scope positive.

4. Adjust lowest pot (M17-1) on TS card for 20 msec ramp shown in "B" of Figure 8.

* * *

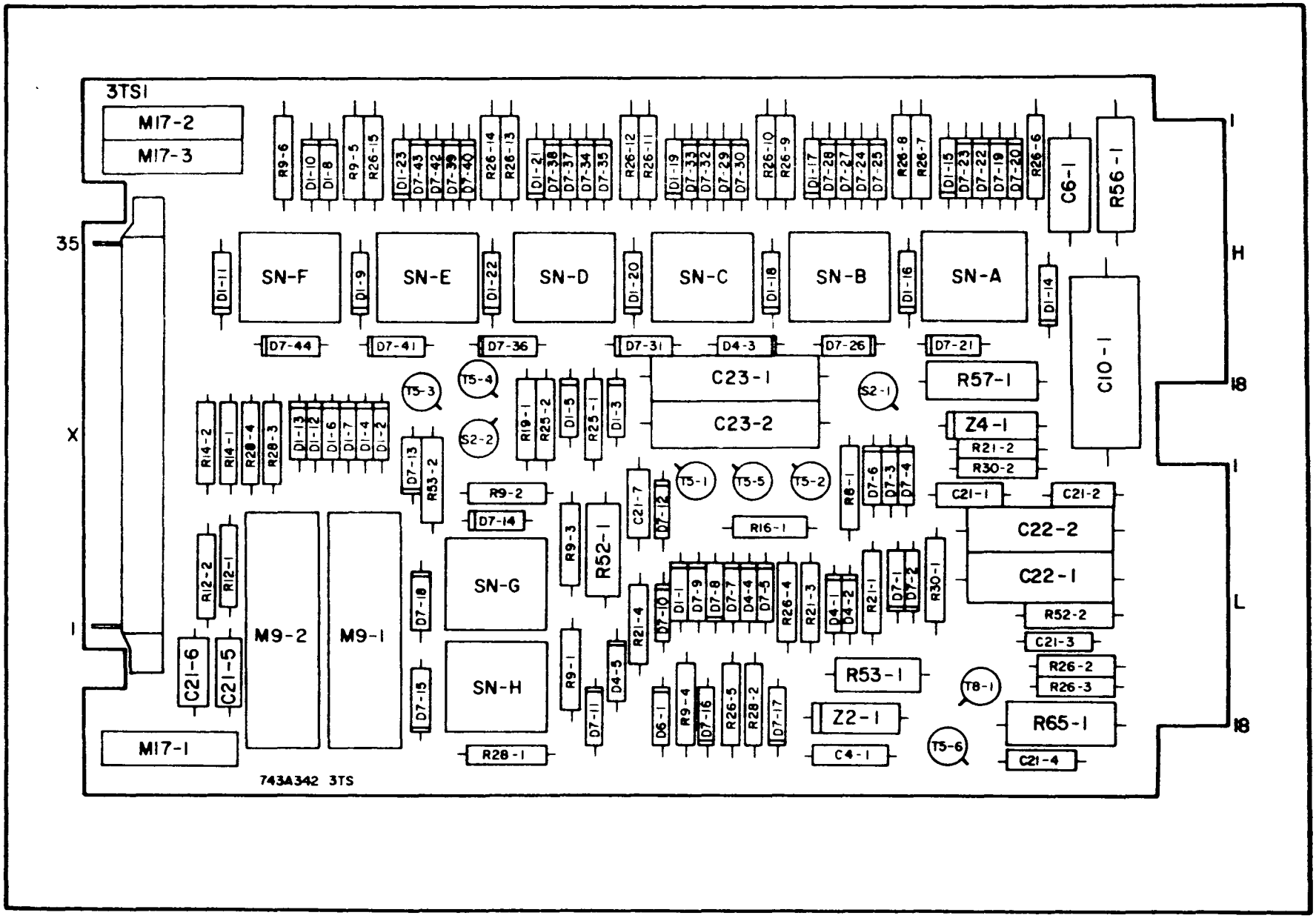


FIGURE 9. 3TS1 ASSEMBLY (REF. DWG. 743A342, SUB 14)

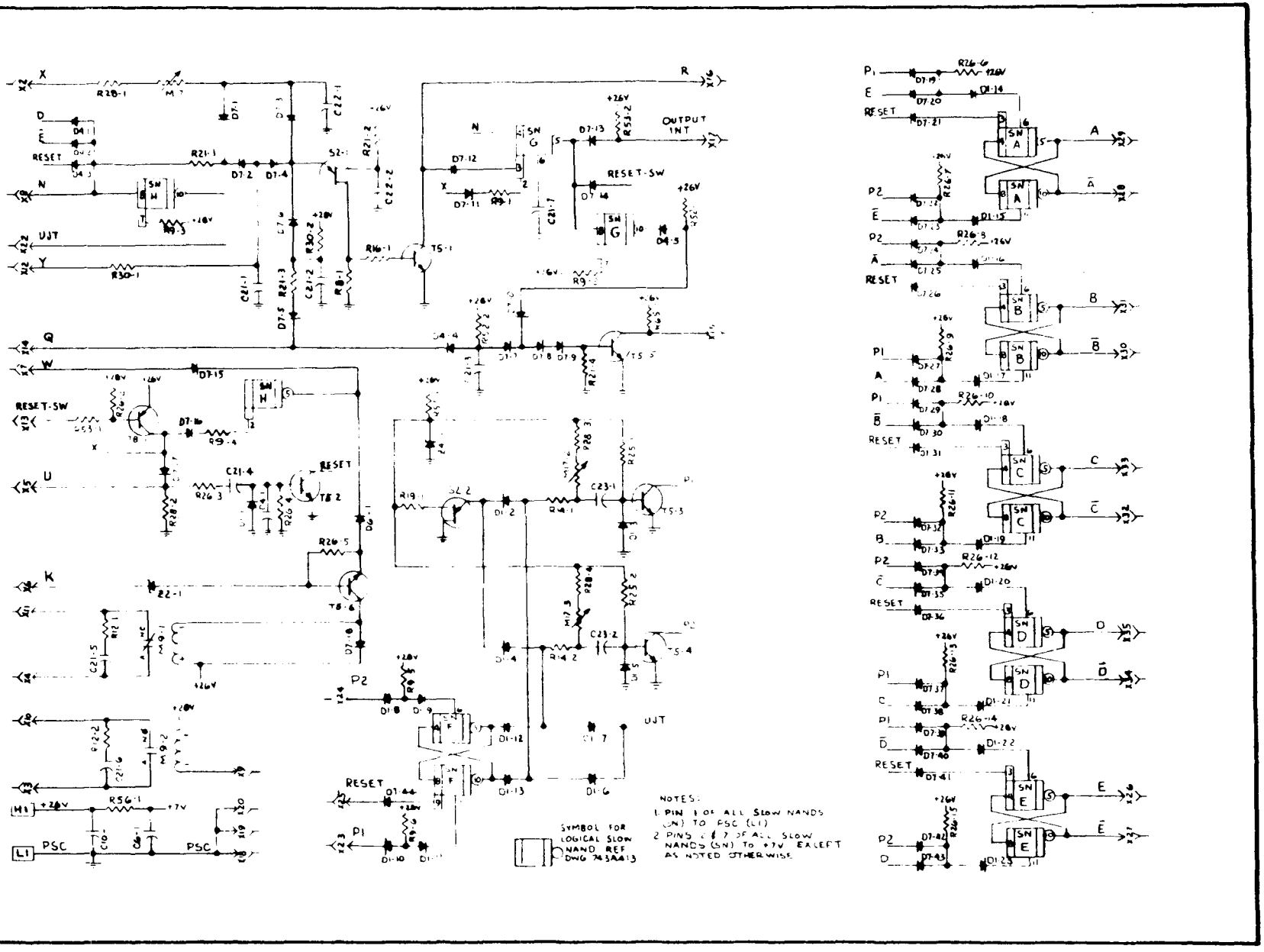


FIGURE 10. 3TS1 SCHEMATIC (REF. DWG. 743A342, SUB 14)

1WD4 - WORD DRIVER MODULE

GENERAL DESCRIPTION

This module is used to provide a 16 bit output to the I/O subsystem. Each bit of the output is designated as a "word". The "word" outputs are used in the I/O subsystem to form a selection matrix with the channel driver(s). An application block diagram is shown in Figure 1.

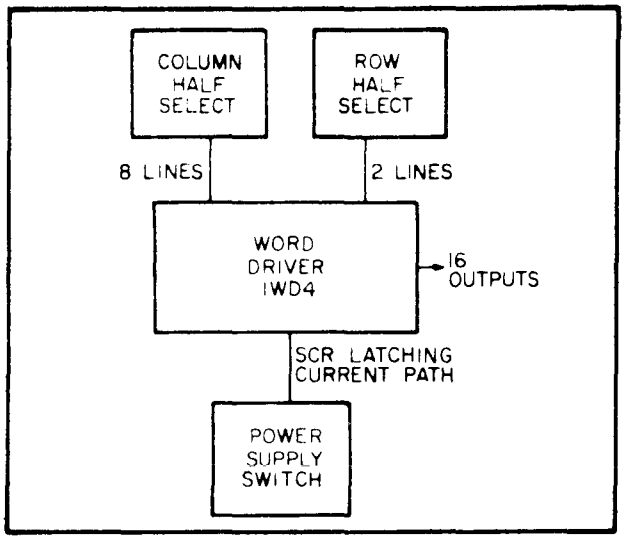


FIGURE 1. APPLICATION BLOCK DIAGRAM

CIRCUIT SPECIFICATIONS

Input Requirements

The half-select input (n) ØØØ and Ø (n) ØØ require a minimum 11 V, 1 μs pulse.

Output Capabilities

The "word" output WD(n) provides a "one" for a selected "word" and a "zero" for unselected words.

WD(n) common is tied to the positive side of the logic power supply.

A current latching circuit is provided for each "word" output which is normally tied to PSC through the power supply switch. To reset the SCR circuits, this must be opened for a minimum of 150 μs.

Power Requirements

Logic level "one" of +10 or +26 V dc is required for card operation.

CIRCUIT DESCRIPTION

Each "word" of the word driver circuit consists of an SCR with a zener diode threshold in the gate circuit and a two-winding gate trigger transformer. Each card contains 16 identical SCR circuits.

Figure 2 shows the schematic diagram of a word SCR and associated circuitry. Dotted lines show the connection to the power supply switch.

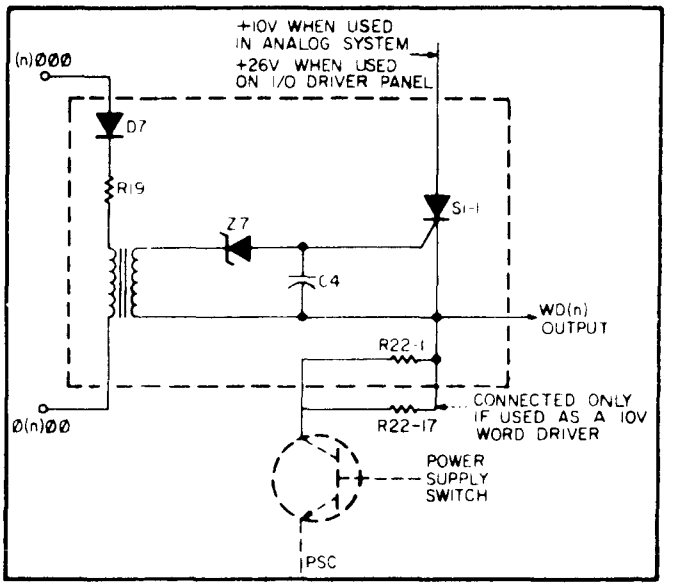


FIGURE 2. WORD SCR SCHEMATIC

Initially, the output transistor of the power supply switch is saturated so that if a positive pulse appears between the gate and the cathode of the SCR (S1-1), the SCR can conduct, since it has sufficient latching current through resistor R22-1 (or R22-1 and R22-17 parallelled if used as a 10 V driver) and the power supply switch.

A particular word driver is selected when a pulse appears across the primary winding of transformer X1-1 (word half-select lines (n) ØØØ and (n) ØØ, which induces a voltage in the secondary winding and this triggers the SCR.

The zener diode threshold prevents erroneous triggering of the SCR by noise in the half-select circuit.

* * *

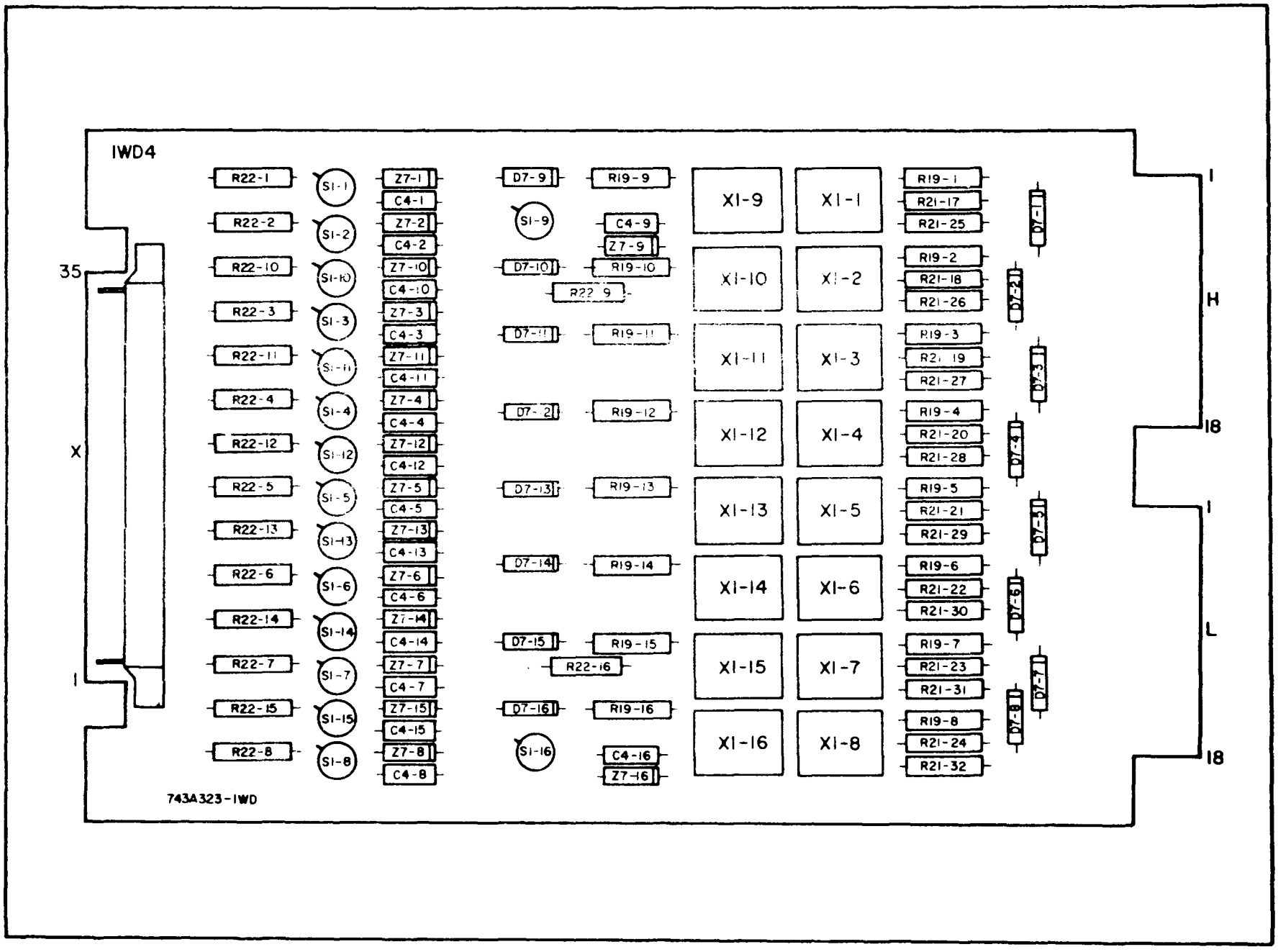


FIGURE 3. 1WD4 ASSEMBLY (REF. DWG. 743A323, SUB 11)

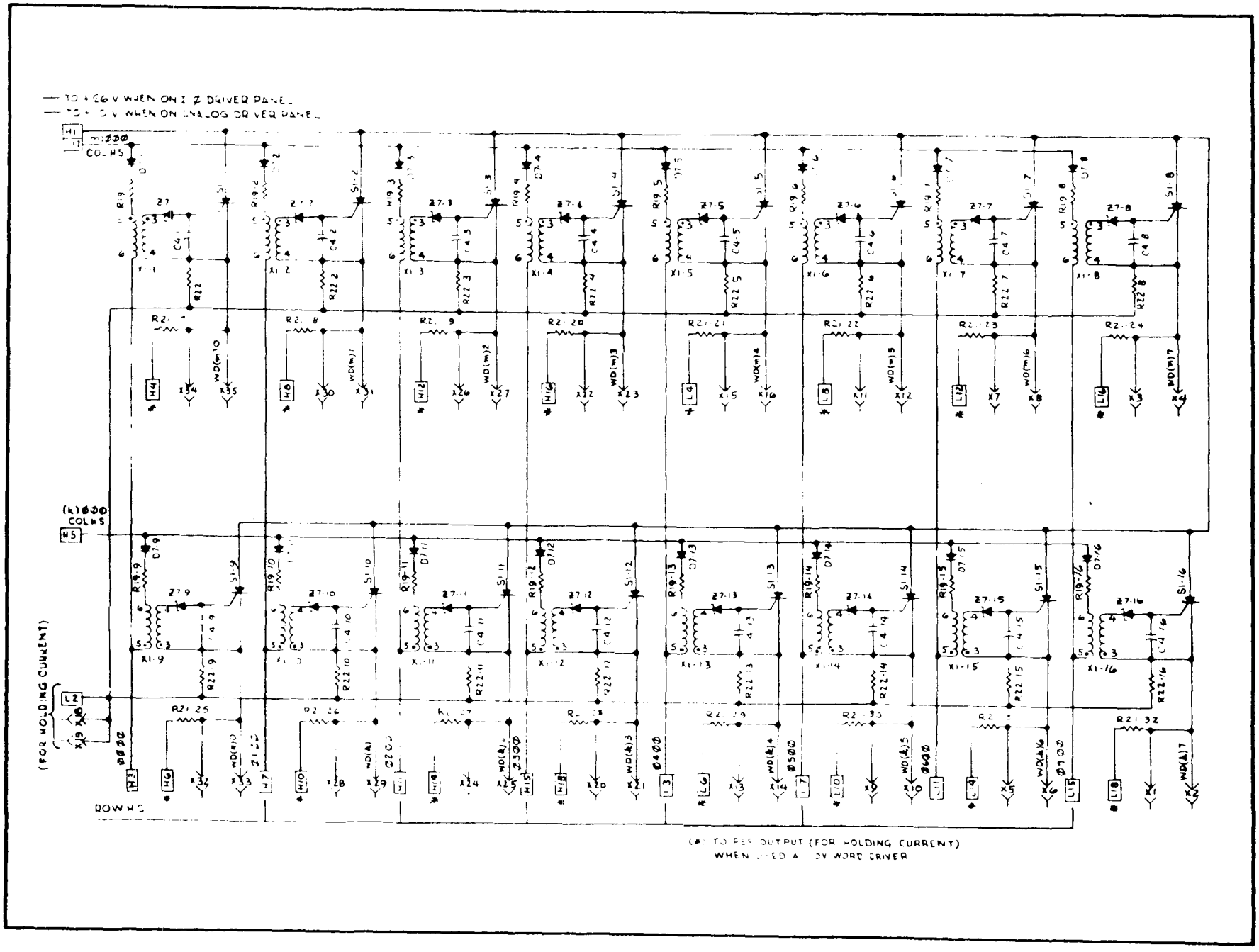


FIGURE 4. 1WD4 SCHEMATIC (REF. DWG. 743A323, SUB 11)

APRIL, 1969

P-50
MAINTENANCE
TRAINING MANUAL

COMPUTER SYSTEMS DIVISION
TRAINING DEPARTMENT

Westinghouse Electric Corporation

I/O A12 OUTPUT

BIT	+	G
0	NN	MM
1	LL	KK
2	JJ	HH
3	EE	DD
4	CC	BB
5	AA	
6	FF	
7		
8		
9		
10		
11		
12		
13		

INPUT A12

BIT	+	G
0	A	B
1	C	D
2	E	F
3	J	K
4	L	M
5	N	P
6	U	T
7	R	S
8	U	V
9	W	X
10	Y	Z
11	a	b
12	c	d
13	e	h

A10

A	0	0	0	0
B				1
C				2
D				3
L				4
M				5
N				6
P				7

NN		0		
MM		1		
LL		2		
KK		3		
CC		4		
BB		5		
AA		6		
Z		7		

TABLE OF CONTENTS

PREFACE

This book is intended to serve a multiple purpose. It is designed as a guide for the person who is interested in learning details of the design, operation and maintenance of the Westinghouse PRODAC 50 Central Processor; and as a reference to specific points or questions which may arise from day to day in working with the P-50.

The book represents the latest available information, as developed by design engineers and other professional personnel of the Westinghouse Computer Systems Division. And it is planned for subsequent modification and/or expansion, as experience grows with this first computing system designed especially for process control. But it is not -- it cannot be -- so detailed that the user can expect to derive the fullest benefit from it by mere reading. Rather, it is aimed at the person who will use it as part of the text material for an intensive training course -- for example, the computer system maintenance man -- which will include substantial classroom and laboratory work, with computers and other training aids.

Such intensive training, conducted by professional Westinghouse computer instructors, naturally enriches and gives added meaning to the printed text. The computer maintenance man, following instruction that includes solving a variety of computer "malfunctions" thoughtfully planned by his instructor to test his new skill and knowledge, will find the book helpful for refresher study or review.

(Such review, when the student is home again and responsible for the smooth operation of the P-50 is important for a reason that one might overlook: The P-50 is designed for great reliability, and malfunctions can be expected rarely. The maintenance man, accordingly, could easily get "rusty" on details of computer construction and operation; how can a man keep "up" on maintenance procedures if he is not called upon for months on end, to concern himself with the computer's operation?)

MAINTAINABILITY

Because this book is likely to be used as a maintenance reference, an added word on the subject of maintainability is appropriate here for the new computer student. Maintainability has been designed into the P-50 in several ways. Careful selection of components is an important factor. Another is wide-tolerance circuit design. A third is success in observing a statistical principle: the fewer the components, the less chance for malfunction. Also important, silicon semiconductors are used exclusively in this system, which makes it possible for the P-50 to tolerate the temperatures and humidity of just about any industrial environment in which men themselves can work.

Ease of maintenance is a feature of the P-50. The circuit cards are large, easy to insert and to plug firmly into place, easy to remove; and the cards are widely separated, and cooled by forced ventilation.

A given circuit card contains functionally related circuits, which simplifies trouble-shooting. As an example, one "bit" or binary digit of each register, data path and adder are on a single card. If trouble should develop in processing of data, you need to determine only which bit is in error in order to locate the defective circuit. You then simply replace that circuit card with a spare.

The checking of "symptoms" is made easy by the fact that all flip-flops have indicators on the ends of their cards.

These and other design features give the P-50 calculated availability of 99.9 per cent.

FIELD SERVICE AND SUPPORT

Through a good many decades, Westinghouse has earned a reputation for efficient, expert electric field service. And the engineers of the Electric Service Division have enhanced this reputation with each new technological change, including atomic reactors, space vehicles, solar engines -- and computers for process control. Throughout the U. S., depending on computer customers' needs and the terms of their orders or contracts, Westinghouse is prepared to supply complete field service for its computer systems -- including installation, startup, checkout, and if necessary maintenance service. The last-named can be on an on-call basis, or part-time, or full-time.

Westinghouse computer training includes general orientation and review of process control computer systems; programming, and maintenance.

GENERAL DESCRIPTION - CENTRAL PROCESSOR

The P-50 central processor consists, functionally speaking, of a control section, an arithmetic section, an input-output (I/O) section, and a core memory section.

It is impossible, however, to identify any one group of logic circuits as comprising one of these sections; a logical portion of one section may also function as parts of other sections. The Z register is an example: It serves as the input-output register for the memory section, one of the inputs to the arithmetic section, and as the input register for the I/O section.

The four sections work together to execute the basic instructions. An understanding of the operation of each section gives one an adequate idea of how the central processor works, and serves as the basis for going on to learn the detailed operation of the P-50 central processor.

Central Processor Characteristics - The P-50 employs a core memory with a capacity of 4K (4096 "words") that is expandable through addition of 4K modules, up to 16K. The word size is 14 "bits" (binary digits). Cycle time is 4.5 microseconds.

The arithmetic used is fixed-point parallel binary, one's complement, negative number. Add time (single word length) is 4 cycles, or 18 microseconds; for indirect addressing, 5 cycles or 22.5 microseconds.

There are 25 one-word, single-address instructions in the basic repertoire, all either directly or indirectly addressable.

The system provides 64 levels of interrupts, with a minimum of 16 lines and increases in 16-line modules.

Clock rate is 3.3 megahertz.

The first step in learning any specific computer system is to become thoroughly familiar with the block diagram and its information flow. Before learning the information flow one must know the individual parts which make up the block diagram. Refer to the computer block diagram (Figure 1-17).

CORE MEMORY

It should be realized that when the core memory is cycled that a fourteen bit word is presented, in parallel, to the input gates of the Z register where it may or may not be placed. At this time in the core cycle the contents of the selected address of memory has been cleared to zero. The output of the adder is then written into this memory location. The specified core memory address may be gotten in one of three ways. If a Select S signal is received, the address will be specified by the fourteen bit word in the S register. If a Select P is received the address will be gotten from the wired in

address circuitry and will be address 00000 octal. If a Select A is received the address will be gotten from the wired in address circuitry and will be address 00101 octal.

HALF SELECTS

The half select (HS) circuitry is used to translate the address into the X and Y drive paths for the core memory. This circuitry will translate the fourteen bit address word in the S register, or the wired in address for the P or A register as determined by the select.

REGISTERS (General)

So far the term register has been thrown around without adequate definition. Well no attempt will be made at this time to do so either, but some reassurance that one is coming will now be given. Registers will be more fully defined and their operation explained shortly. For now it must be realized that a register is a storage device which has been given a special task as described below.

REGISTERS

The P-50 uses registers both internal and external to core memory (see block diagram Figure 1-17).

The internal registers include:

Accumulator or "A" Register

A 14-bit accumulator for the arithmetic unit which stores the results of arithmetic and logical operations.

Program Counter or "P" Register

A 14-bit register which contains the address of the instruction currently being performed. It is incremented -- that is, increased by one -- at the beginning of execution of each instruction.

The external (and visually indicated) registers are:

Address Register or "S" Register

A 14-bit storage location which serves as the embarkation or starting point into the half-select addressing system for all variable addressing, for core memory, process locations, and I/O devices.

Addend Register ("Z" Register)

A 14-bit register most frequently used to receive the output of core memory. By way of sense amplifiers, the "Z" register receives all the words read out of core. In combination with the "X" register, the "Z" register generates an input to the adder, and

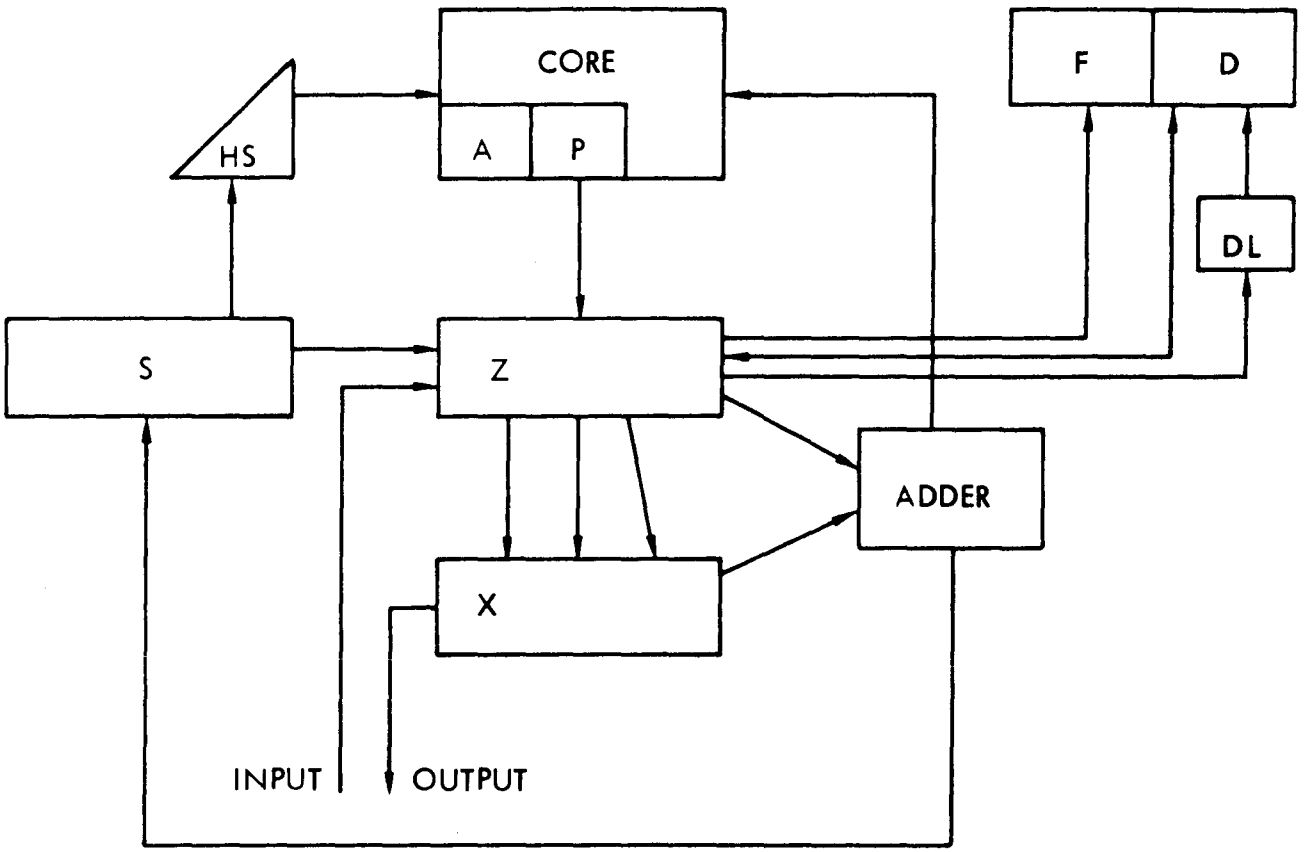


Figure 1-17. Computer Block Diagram

subsequently to any location designated in core memory. The "Z" register also relays the function code and the mode bit (indicating indirect addressing) to the Function ("F") register. In addition, the "Z" register relays to the "S" register, via the adder, the least significant 8 bits of the instruction, which serve as the operand address. Finally, the "Z" register handles all inputs to the central processor.

Augend or "X" Register

This 14-bit register participates in shifting activities as well as handling the complementing instruction. In conjunction with "Z", the "X" register produces input to the adder, such as advancing "P", decrementing a core location or permitting a transfer unchanged. Also it handles all outputs from the central processor.

Function or "F" Register

This is a 6-bit register which receives its information from the "Z" register. Bit positions 9 through 13 in "F" (which are positions 9 through 13 of the instruction) comprise the function code, signalling which of the 25 P-50 instructions is to be performed. Bit 8 is the mode tag, indicating block (direct) or indirect mode.

Designator Register

This is a series of 5 flip-flops provided to store the results of the examination of the last word that has been written into memory. The designator examines each memory operation for:

Zero or not
Positive or negative
Odd or even (for both positive or negative)
End-around carry (which can occur in any addition or subtraction)
Overflow

Generally, all instructions except those used to test the designators will cause these 5 flip-flops to be set appropriately. Testing, by means of the designator jump instructions, may be done immediately after any such operation, at the programmer's option.

* * *

Since the "X", "Z", "S" and "F" registers function only during execution of an instruction, and hold no information between times, their contents may be destroyed between instructions without effect on computation. All information that must be retained between instructions is stored in core memory (that is, in the "A" or "P" registers), with the exception of the designators. Load and Store Designator instructions, called by an interrupt caused by power loss, provide means for bringing designator content into core memory also. Thus power loss or planned shutdowns do not cause a loss of information or computing sequence.

CONTROL SECTION

Referencing Figure 1-17, it can be seen that several transfer paths exist between the various registers. Even though it is not shown on the diagram, all of these transfer paths cannot be enabled at the same time. The transfers should be done only at the proper time and in the proper order. This timing and sequencing of the various commands is the responsibility of the control section.

The control section of the central processor consists of five logic blocks; these are the master clock, cycle counter, the sequencer, the function translator, and the command enables (see Figure 1-18).

The master clock is a tapped LC delay line with a total of six taps which are labeled L0, L1, L2, L3, L4, and L5. These are the main timing of the central processor and govern its operational speed. One pass down the master timing L0 through L5 is considered one cycle.

The cycle counter is a two flip-flop counter which determines which of the master clock cycles is being performed. These cycles are labeled 0, 1, and 2. A group of the three cycles is considered a sequence.

The sequencer consists of two ranks of three flip-flops each. One rank is called the HA or half advance rank and the other rank is called the SA or sequence advance rank. The sequencer tells the central processor which sequence it is performing at the current time and which sequence will be performed next. One must be very careful in that the three flip-flop rank does not contain a binary representation of the sequence. The sequences are labeled one through seven and are represented by Roman numerals.

Sequence I is a one and one half micro second scan sequence. This sequence is used to scan the 64 interrupt words. Sequences II through VII are four and one half micro seconds each. Sequence II is used to update the contents of the P register by one and transfer the updated contents to the S register. Sequence III will call up the instruction and transfer the function code and mode bit to the function register and replace bits 0-7 of the S register with bits 0-7 of the instruction. Sequence IV is the indirect sequence; it

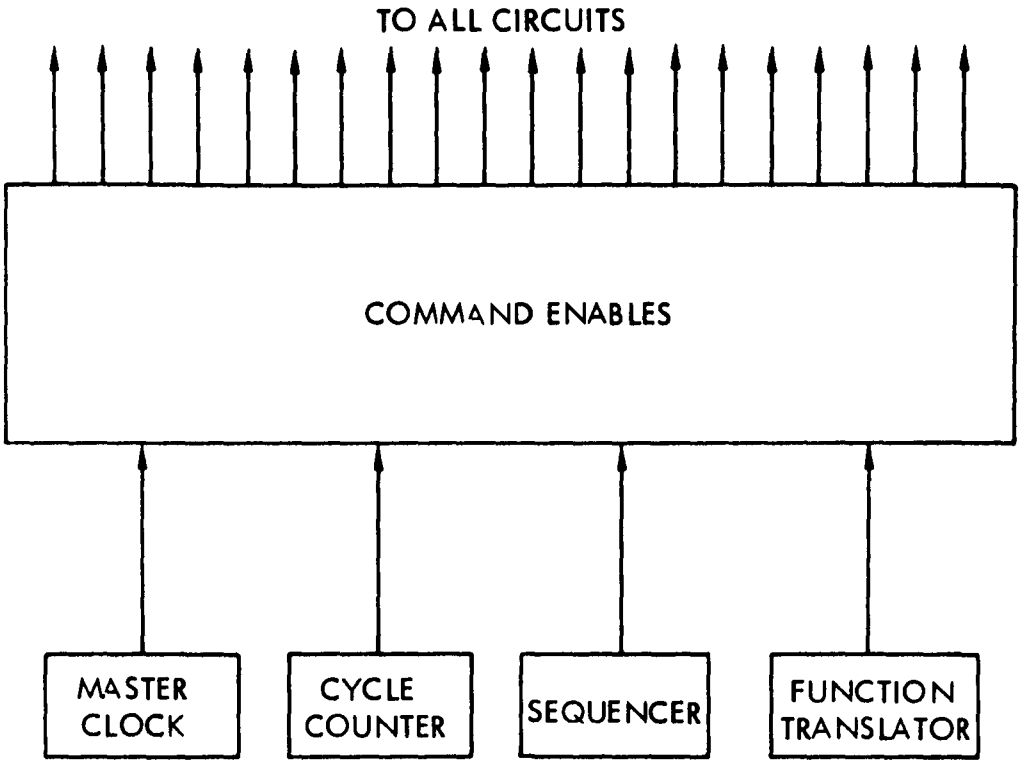

TO ALL CIRCUITS
COMMAND ENABLES
MASTER CLOCK
CYCLE COUNTER
SEQUENCER
FUNCTION TRANSLATOR

Figure 1-18.

will transfer the contents of the memory address specified by the S register into the S register. Sequences V and VI are the arithmetic sequences. They are used to call up the contents of the A register or the operand address, and restore information into the A register or the operand address. Sequence VII is the jump sequence. This sequence is used to transfer, what would normally be the operand address, into the P register.

The function translator is a group of logic circuits which translates the output of the function register and tells the central processor what instruction it is to perform.

The command enables circuit is a group of logics which looks at the output of the master clock, the cycle counter, the sequencer, and the function translator to determine which individual command or group of commands is to be done at that particular instant.

ARITHMETIC SECTION

The arithmetic section of the central processor consists of one logic circuit called the adder and three registers. Two of these registers are the Z register and the X register. These two registers are the two inputs to the adder. The third register in the arithmetic section is the accumulator register (A register), which is located in core memory at address 00101 octal. The arithmetic section does the performance of the arithmetic and logic functions of an instruction. This section is also used for many of the housekeeping type operations like the updating of the P register, and the transferring of information to various registers.

INPUT OUTPUT SECTION

The input output section of the central processor contains many logic circuits. One of these circuits is the translating circuit for the address contained in the S register. This translating circuit is shared with the memory section. This section also contains the circuits for driving a particular channel and a particular word on that channel. The input output section also contains the circuitry for the interrogating of the 64 interrupt word addresses. The input output section receives its address information from the S register, its output data information from the X register and sends its input information to the Z register. This section is the interface between the arithmetic and control section of the central processor and the process itself.

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CORE MEMORY BASIC DESCRIPTION

The core memory section of the central processor consists of the core memory section itself, the input output register for this core memory called the Z register, and the core memory address register called the S register. It can be seen that everything centers around the core memory itself, and in order to understand this section's operation, the basic theory of core storage should be understood.

The storage medium for the core memory is the ferrite core. The core is a small torride of a ferrite material, which exhibits what are called square loop properties. The diameter of this core is about .05 inches (see Figures 1-3 and 1-4). Because of the rectangular shape of the square loop, the core is binary in nature. That is, it has two stable states of flux saturation; one state is a one (point d on the loop) and the other state is a zero (point a on the loop). The core can be saturated to either of these stable states by a magnetic force. The magnetic force is derived from current passing through the drive wires which are threaded through the core. When the core is saturated to the zero or the one state flux density is maximum. When the magnetizing current is removed from the drive windings the core will remain in this magnetic state.

The core memory is a coincident current, random access core memory. In this type of a core memory, magnetizing current required to flip a core from the zero state to the one state or from the one state to the zero state is supplied by two drive windings passing through the core. Each drive winding carries half enough current to flip the core from one state to the other. If one winding is turned on and the other winding is turned off the resultant current is only half enough to flip the core, therefore the core remains in the original state. If both windings are turned on and the current is in a direction which will flip the core, the resultant current is two half drives or a full drive, which is sufficient to flip the core to the other state.

Using this knowledge of the operation of a core memory let us proceed to build a workable core memory section. If we arrange 16 individual cores, in a manner shown in Figure 1-5, we have what is called a core plane. The drive windings mentioned above are placed through the cores in the manner shown. It can be seen that a drive winding for each core passes through three other cores along the same line. One of the half drive windings going through a line of cores is labeled X and the other is labeled Y. If we select any one X line and drive one half enough current through it and select any one Y line and drive one half enough current through it, it can then be seen that all cores along each line will receive one half enough current to flip those cores. At the point where the two lines intersect there is a core which receives one half enough current from the X line and one half enough current from the Y line. Therefore, this is the only core in the plane to receive two half currents, or a full current. This core is said to have been selected and will flip.

Let us assume that this selected core was in the zero state. If we put a current through the drive lines in the read direction (the read direction being defined as the direction required to flip the core to the zero state), it can be seen that since the core was already in the zero state it could not flip. If this core had been in the one state originally, then it would have flipped. When this core flipped, it created a large change in a magnetic flux around the core.

A third winding through the core plane is called a sense winding. This winding passes through every core in the core plane, therefore, the core which flips will induce a voltage onto this sense winding.

If no voltage is induced when we read the core, we assume the core was in the zero state. If a voltage appears on the sense winding when we read the core it is assumed the core was in the one state. The fact of voltage or no voltage on the sense wire is remembered by the Z register. As this type of reading of core memory leaves the core in the zero state it is called destructive readout. The core is now in the zero state and the Z register remembers the original state. We then must write the information back into the core. This is done by reversing the direction of current in the X and Y drive lines. This attempts to flip the core back to the one state. It can be seen now we have a problem. If the core was originally in the one state, it will flip back to the one state, but if the core was originally in the zero state we must stop it from going to the one state. The method chosen to do this is to add an additional winding called an inhibit winding. This winding is placed through all cores of a core plane so that a current passing through it will be in the opposite direction to the write current. This will be a one half current. If we turn on the inhibit winding and both of the write windings at the same time, the inhibit winding will cancel the effect of one of the write windings. There will, therefore, be a resultant of only one half current which will leave the selected core in the zero state. It may now be seen that the inhibit winding will be controlled by the Z register. That is, if a one is detected in the Z register the inhibit winding will not be turned on, but if a zero is detected in the Z register the inhibit current will be turned on to cancel or inhibit the writing of a one in the core.

We now have the ability to address a one bit core memory. If we use the same principle and stack several of these core planes one on top of the other (Figure 1-6), we can make a core memory of as many bits as we choose. If we desire a three bit word length computer we would stack three of these core planes, if we desire a six bit core memory we would stack six of these planes. The number of planes stacked would be governed by the word length of the computer. In Figure 1-6 three core planes are shown one on top of the other. It can be seen in this figure that the X lines and Y lines pass through one line of cores in each core plane. The sense and inhibit lines in this figure are not shown, but they would be restricted to their own core plane. Thus, if we select one X line and one Y line, it can be seen that we will pick one bit in each core plane. We can read the information from the top core plane and send it to the 2^0 position of the Z register. The information from the next core plane down would be sent to the 2^1 position and the next core plane to the 2^2 position and so forth. The inhibit winding for the top plane would get its information from the 2^0 position of the adder*, the next one down the 2^1 position, and so forth. When we drive a particular X and Y line, we will gate the entire word in parallel into the Z register, then on the write cycle (not to be confused with clock cycle) we will turn on the inhibit lines for each bit plane corresponding to zeros at the output of the adder.

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*The P-50 uses the output of the adder instead of Z to determine inhibits.

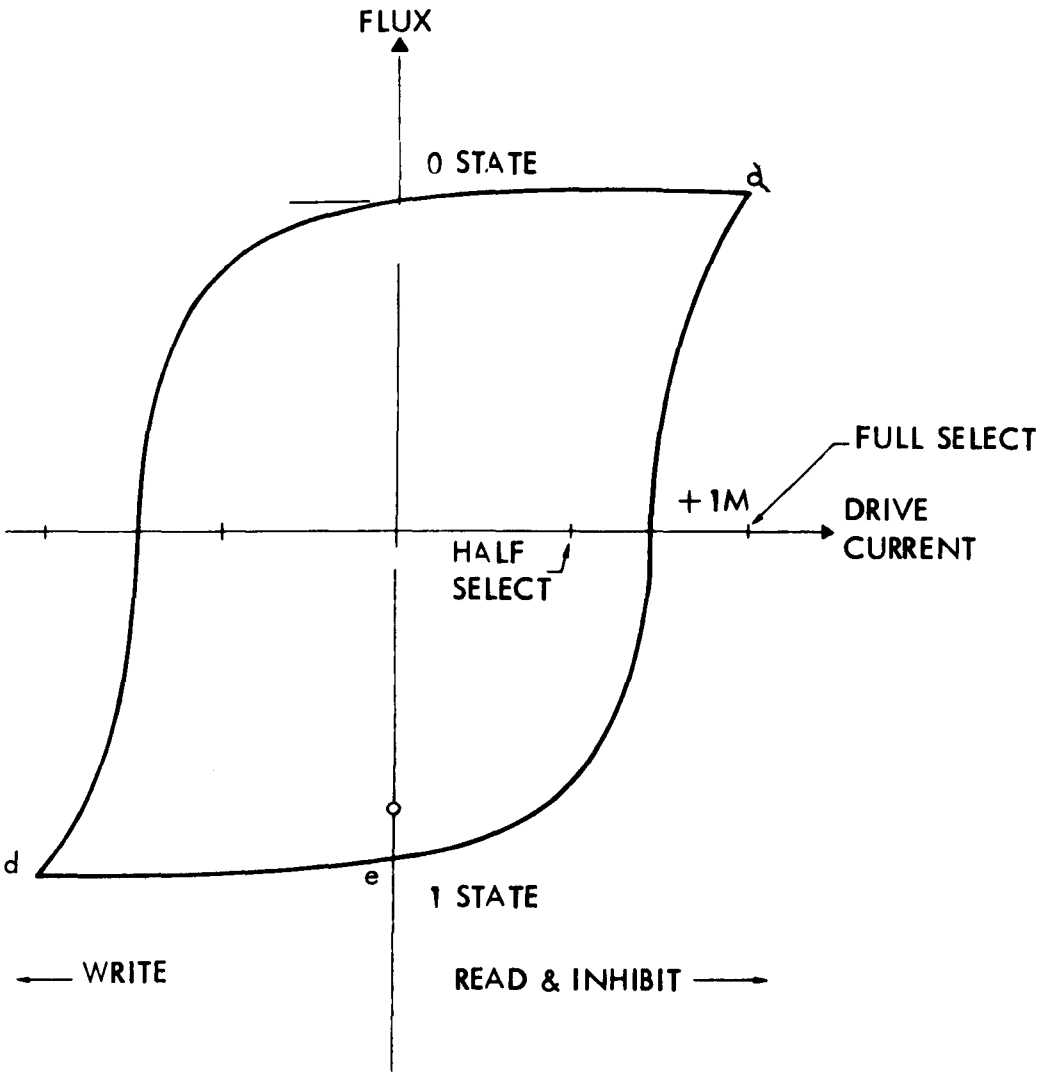

Figure 1-3. Typical Hysteresis Loop

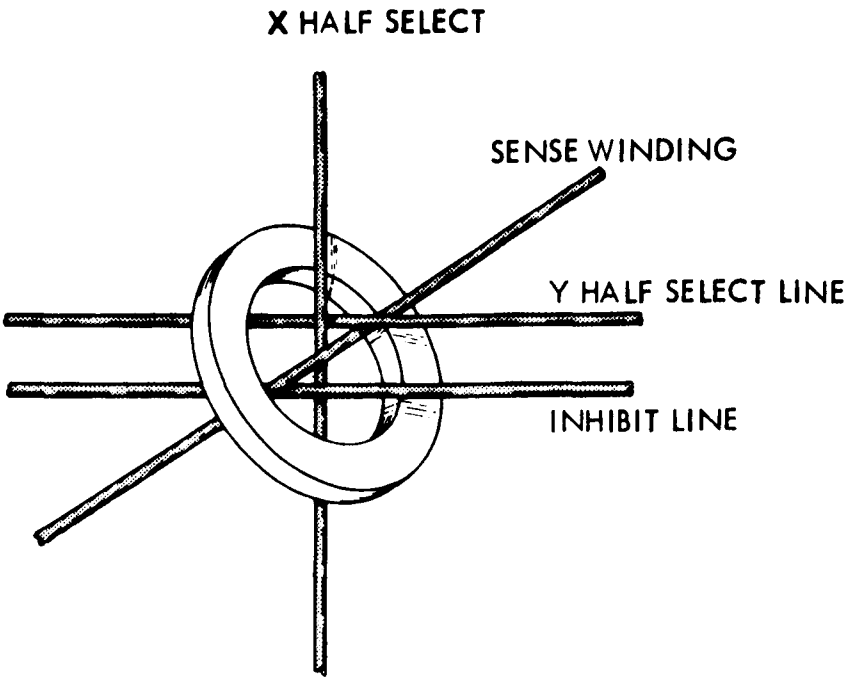

Figure 1-4. Core Windings

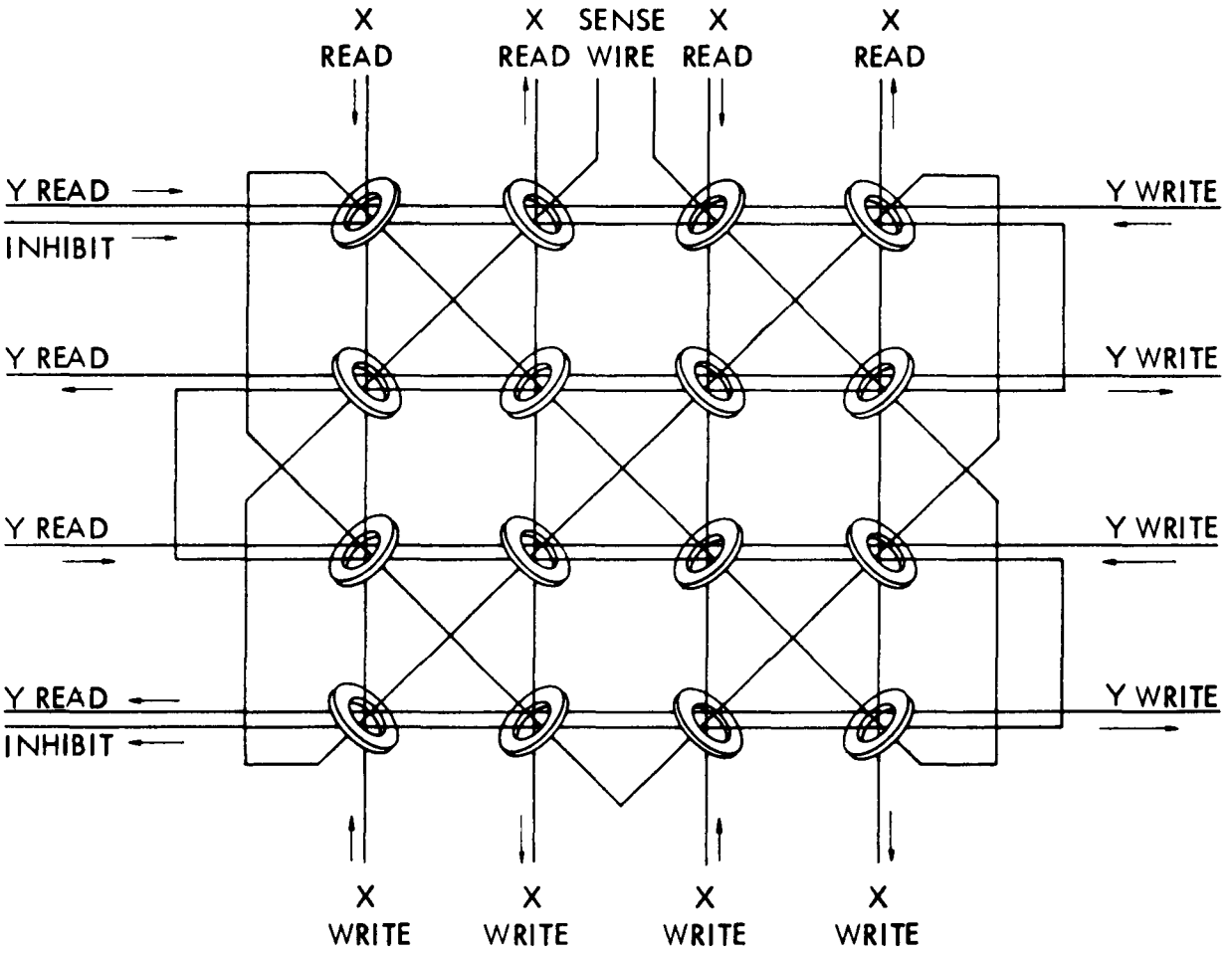

Figure 1-5. Core Plane Wiring

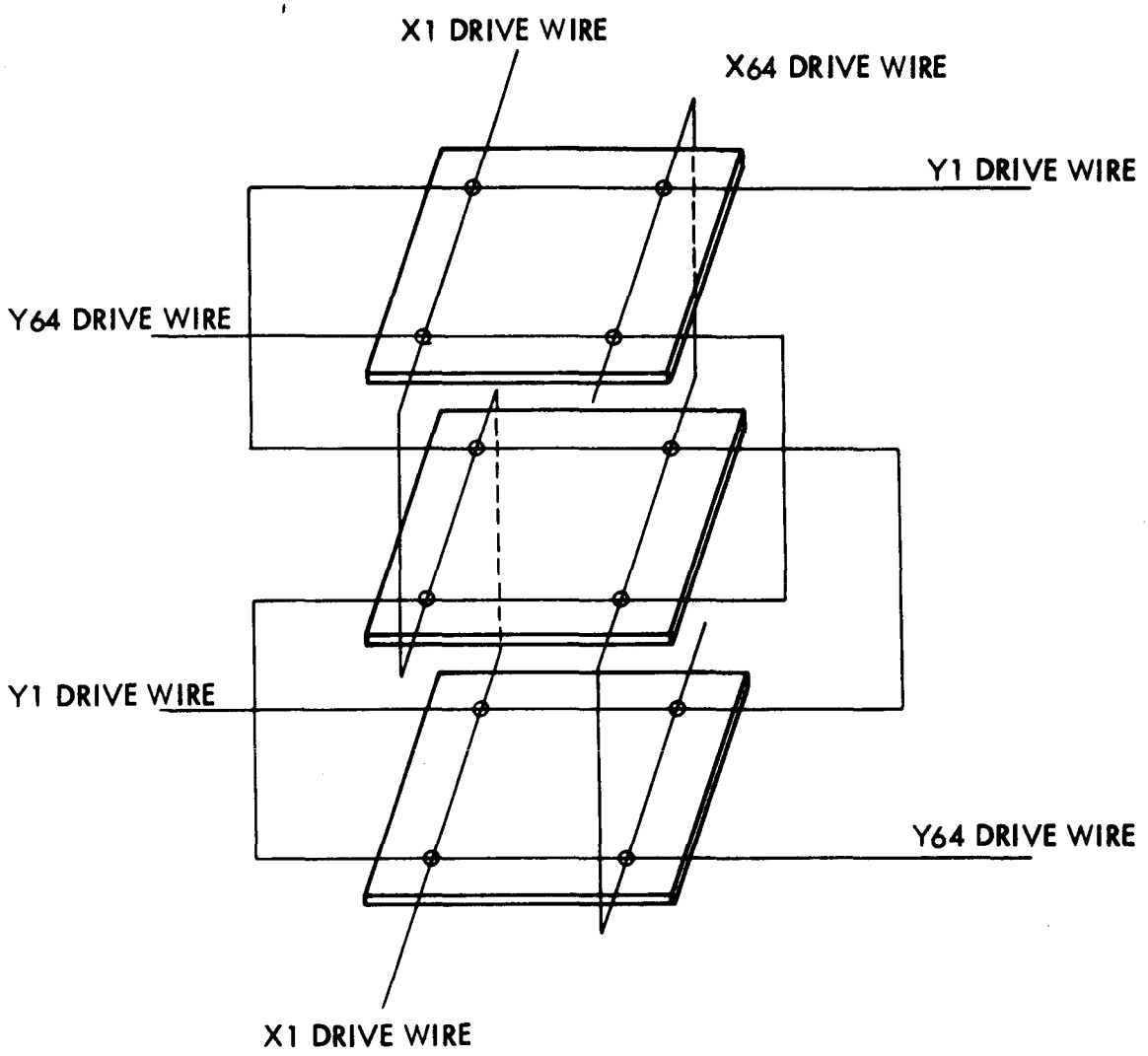

Figure 1-6. Core Stack Drive Wire Configuration

Let us look at a typical read-write cycle. A typical read-write cycle would be to select a particular X and Y line (address select) determined by the translation of the S register. We gate the information from the selected core memory address into the Z register. If we decide to restore the information into the core unchanged, we leave the other input to the adder (the X register) set the zeros. Then we take the output of the adder which would be Z+0, or just Z, and transmit this via the inhibit lines back into the core memory. If we should desire to write new information into core, we select an X and Y line, read the core memory, inhibit the reading of the information into the Z register, place new information into the X register, and transmit the output of the adder, which would then be X+0, or new information plus zero, into the core memory. It can be seen that the difference between a read and a write cycle is what we do with the X and the Z registers. As far as the core memory itself is concerned, there is no difference.

The PRODAC 50 uses 64 X lines, 64 Y lines and 14 bit planes in its core memory, but the basic principle is still the same.

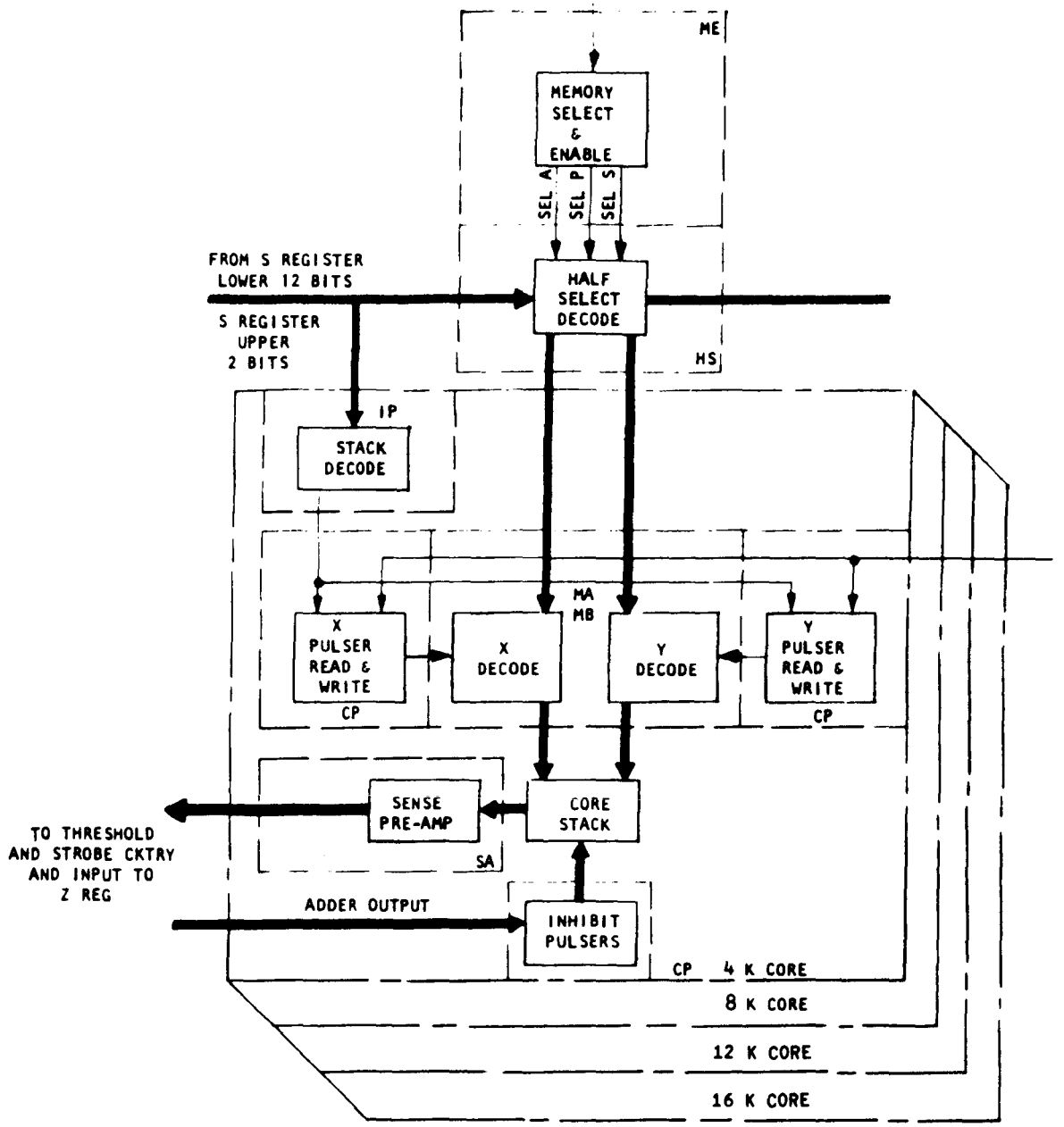

Figure 1-10.

Some locations in core have special significance. Location 00000 is used as the Program Counter and is directly accessible via the half-selects by the SEL P signal. Location 00101 is used as the Accumulator and is accessible by the SEL A signal. At all other times SEL S is used as the timing signal which gates the S register contents to the Half-Select Decode.

ADDRESSING

Half-Selects

The inputs to the half-select switches are the lower 12 bits of the S register and the SEL S signal, or the SEL P, or SEL A signals. The function of the half-select switches is to route current through the core stacks, the Interrupt buffer cores, or the I/O subsystem. The pulse energy is derived from the X Read, X Write, Y Read or Y Write pulsers associated with the selected stacks. (In the case of Interrupt scan selection or I/O subsystem selection, separate pulsers are used). The means whereby the half-select decode operates is the simultaneous selection of a subrow and subcolumn half-select switch. The subrow switch completes the path to the positive supply from the pulser through a half-select transformer. The three X (or Y) subrow bits are the lowest three bits of the X (or Y) part of the address. These bits are decoded to select one of eight X (or Y) half-select transformers. The remaining three X (or Y) bits are associated with the eight subcolumn half-select switches. The eight subcolumn half-select switches connect up to eight loads on any of the eight half-select transformer secondaries. Thus by way of the three subrow bits and three subcolumn bits up to 64 paths can be selected. In the case of the core stack the 64 paths are the 64 half-select lines for X or Y.

The HS card contains four subrow half-select switches and four subcolumn half-select switches. Four HS cards are used in the main frame to provide eight subrow switches for X and eight for Y, and eight subcolumn switches for X and eight for Y.

Diode Boards

In order to route currents through the selected half-select lines, parallel unselected paths must be blocked by blocking diodes. Each path needs two blocking diodes. This is because paths must be blocked for the two directions of current flow corresponding to Read and Write. This means that the 64 X half-select lines and 64 Y half-select lines require 256 diodes. These diodes are mounted on two diode boards, the MA and MB, which are attached to either side of a stack. Also mounted on the two diode boards are the 16 half-select transformers and damping resistors associated with the stack.

Pulsers

The Read, Write, and Inhibit pulsers are associated with a 4096-word stack. The same circuit is used for each of these current pulsers with six circuits located on each CP card. This high-power current pulse source is intended to produce stable currents even when operated from an unregulated supply. Potentiometers for adjusting currents through a 300 milliampere to a 400 milliampere range are provided. The rise times of the current pulses are controlled to give a 0.3 microsecond 10% to 90% rise. The fall is not controlled but drops at nearly the same rate.

The pulsers are the means by which a particular stack is selected. Addressing is a continuing procedure involving the half-select switches, but only that stack will be energized, and therefore selected, whose pulsers are selected. The Stack Select signal is derived from the Inhibit Paddle cards where NANDs decode the upper two bits of the S Register.

Inhibit Paddle Card

The IP Inhibit Paddle Card contains damping resistors for the Inhibit lines. Also on this card are two NANDs which are used to decode the upper two bits of the S register and generate Stack Select signals for the various stacks.

DATA CIRCUITS

Sense Amplifier

An SA Sense Amplifier is associated with each core stack. There are 14 amplifiers on a card corresponding to the 14 sense line pairs. The line itself is terminated in 100 ohms. The amplifier is a balanced differential type with a normal mode gain of about 60 to 5 mc and a common mode rejection at 1 mc of 60 db. Since response voltage signals can be of either polarity, an output transformer and rectifiers are used to created unipolar signals at a new voltage level on the output of each amplifier. The outputs of amplifiers from up to four stacks are paralleled and tied to the bit card where the threshold detector and strobe circuits are located.

Inhibit

The Inhibit pulsers are located on the CP card. Fourteen pulsers are used per core stack. The outputs of the Adder gated by the $\overline{W}$ timing signal are always feeding the data inputs of all the Inhibit pulsers. Only the Inhibit pulsers which are selected by the Stack Select signal will drive Inhibit lines to determine whether a zero or one is restored to a core location.

TIMING CHART

The important signals associated with the Core Memory Subsystem are the Select, Read, Strobe, Write, and Inhibit timing signals. Another time is the gap between Strobe and Write which is allotted to Adder propagation time. The signals for a core sequence are shown in Figure 1-11. All signals are determined by fixed timing taps except Strobe, which can be adjusted over a range of five selectable 50-nanosecond taps. Select P and Select A are not shown but have the same extension as the Select S signal.

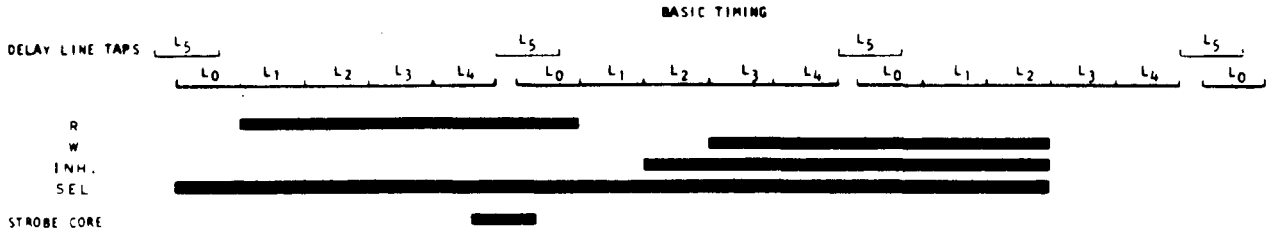

Figure 1-11. Core Memory Subsystem Timing Chart

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REPERTOIRE OF INSTRUCTIONS

COMMAND STRUCTURE

All P-50 instructions may be either directly or indirectly addressed. The bit configuration for each address mode is as follows:

Instruction, Direct Address Mode

13 12 11 10 9	8	7 6 5 4 3 2 1 0	Bit
Function Code	0	Relative Address	Content

In the direct address mode, the 14-bit operand address required to reference a memory cell is generated by the six most significant bits of the program address register and the low-order eight bits of the instruction (the relative address). This imposes the requirement that all instructions which are directly addressed have their operand in the same block of 256 words in which the instruction is located.

Instruction, Indirect Address Mode

13 12 11 10 9	8	7 6 5 4 3 2 1 0	Bit
Function Code	1	Relative Address	Content

Address Defined by P Register and Relative Address

13 12 11 10 9 8 7 6 5 4 3 2 1 0	Bit
Operand Address	Content

In the indirect address mode, the operand address is defined by the contents of the location specified by the six most significant bits of the P Register and the low-order eight bits of the instruction (the relative address).

Input/Output instructions vary slightly from this pattern.

Input/Output Instruction, Direct Address Mode

13 12 11 10 9	8	7 6	5 4 3 2 1 0	Bit
Function Code	0	Not Used	Channel Number	Content

In the direct address mode, used primarily for input, the low-order six bits of the instruction designate the I/O channel.

Input/Output Instruction, Indirect Address Mode

13 12 11 10 9	8	7 6 5 4 3 2 1 0	Bit
Function Code	1	Relative Address	Content

Address Defined by P Register and Relation Address

13 12	11 10 9 8 7 6	5 4 3 2 1 0	Bit
Not Used	Word Select	Channel Number	Content

In the indirect address mode, used mainly for output, the six most significant bits of the program address register and the low-order eight bits of the instruction specify the location of the I/O data word. The I/O data word contains the channel number in the low-order six bits (5-0) and the word number relative to the channel in bits 11-6.

TIMING

The execution of an instruction in the indirect mode occupies 4.5 microseconds more than when the instruction is executed in the direct mode.

DESCRIPTION OF OPERATION

INST.	MNE	CODE	DES	REMARKS
A + (Y) ⟶ A	ADD	10	SET	ADD
A - (Y) ⟶ A	SUB	11	SET	SUBTRACT
(Y) ⟶ A	ENL	32 33	SET	LOAD A
A ⟶ (Y)	STL	37	SET	STORE A
A ⊕ (Y) ⟶ A	EOR	13	SET	SEL. COMPL.
L (A)(Y) ⟶ A	AND	12	SET	LOGICAL PRODUCT OF (A) & (Y)
(Y) R1 ⟶ (Y)	RSH	16 17	SET	END off - SIGN EXT.
(Y) L1 ⟶ (Y)	LSH	14 15	SET	END - AROUND
(Y) - 1 ⟶ (Y)	DCR	01	SET	DECREMENT
SET $(Y)_{13}$	SMB	03	SET	SET MOST SIG. BIT
CLR $(Y)_{13}$	CMB	02	SET	CLR MOST SIG. BIT
(Y_{4-0}) ⟶ DES	EDR	05		LOAD DESIGNATORS
DES ⟶ (Y_{4-0})	SDR	06 07	K	STORE DESIGNATORS
I/O ⟶ A	INT	30 31	SET	INPUT
A ⟶ I/O	OUT	34 35	SET	OUTPUT
Y ⟶ P	JMP	24	K	JUMP
Y ⟶ P	SLJ	22	K	SET LOCKOUT
Y ⟶ P	CLJ	23	K	CLR LOCKOUT

INST.	MNE	CODE	DES	REMARKS
Y ⟶ P if 0 DESIG SET	ZJP	20	K	JUMP ON ZERO
Y ⟶ P if POS DESIG SET	PJP	27	K	JUMP ON POS.
Y ⟶ P if EVEN DESIG SET	EJP	21	K	JUMP ON EVEN
Y ⟶ P if EAC DES SET	CJP	25	K	JUMP ON END AROUND CARRY
Y ⟶ P if OVERFL DES SET	OJP	26	K	JUMP ON OVERFLOW
(P) ⟶ Y, Y ⟶ P	RJP	36	K	RETURN JUMP
STOP	STP	00 04	K	STOP

REPERTOIRE OF INSTRUCTIONS

Mnemonic Code
Octal Code — Description

STP
00,04

STOP

Execution time: 9 microseconds

The computer comes to a stop with the contents of bits 13-8 of the P Register in bits 13-8 of the S Register and the contents of bits 7-0 of the stop instruction in bits 7-0 of the S Register. The mode bit is disregarded and the designators are unchanged.

DCR
01

DECREMENT

Execution time: 13.5 microseconds

A negative one is added to the operand. The appropriate designators are set if an overflow, end-around carry, zero, positive number, and/or even number results; otherwise, all the designators are cleared except the overflow designator.

CMB
02

CLEAR MOST SIGNIFICANT BIT

Execution time: 13.5 microseconds

The sign bit (bit 13) of the operand is cleared to zero and the positive designator is set. The zero and even designators are set or cleared depending on the resultant contents of the operand. The end-around carry designator is cleared, and the overflow designator is unchanged.

SMB
03

SET MOST SIGNIFICANT BIT

Execution time: 13.5 microseconds

The sign bit (bit 13) of the operand is set to one. The even and zero designators are set or cleared depending on the resultant contents of the operand. The positive and end-around carry designators are cleared, and the overflow designator is unchanged.

EDR
05

ENTER DESIGNATORS

Execution time: 13.5 microseconds

Bits 0-4 of the operand replace the contents of the five designators in the following manner:

Bit 4 ⟶ Even designator
Bit 3 ⟶ Zero designator
Bit 2 ⟶ Positive designator
Bit 1 ⟶ Overflow designator
Bit 0 ⟶ End-around carry designator

Only this instruction can clear the overflow designator once it has been set.

SDR
06,07

STORE DESIGNATORS

Execution time: 13.5 microseconds

The five designators are stored in bits 0-4 of the operand. The designators are not changed as a result of this instruction. The storage is as follows:

Even designator ⟶ Bit 4
Zero designator ⟶ Bit 3
Positive designator ⟶ Bit 2
Overflow designator ⟶ Bit 1
End-around carry designator ⟶ Bit 0

$(Y)_{5-13}$ are cleared to zero

ADD
10

ADD ACCUMULATOR

Execution time: 18.0 microseconds

The operand is added to the contents of the accumulator and the result is left in the accumulator. The result is positive zero only if the initial contents of the accumulator and of the operand were both positive zero. The even, zero, positive, and end-around carry designators are set or cleared by the execution of this instruction. The overflow designator will be set if an overflow occurs; otherwise it is unchanged.

SUB
11

SUBTRACT ACCUMULATOR

Execution time: 18.0 microseconds

The operand is complemented and added to the contents of the accumulator (a subtraction, in effect); the result is left in the accumulator. The difference is positive zero only if the initial contents of the accumulator were positive zero and the operand was negative zero. The even, zero, positive, and end-around carry designators are set or cleared by the execution of this instruction. The overflow designator will be set if an overflow occurs; otherwise, it is unchanged.

AND
12

LOGICAL AND

Execution time: 18.0 microseconds

For any bit position of the operand which contains a zero, the corresponding bit position of the accumulator is unconditionally set to zero; all other bit positions of the accumulator remain undisturbed. The effect of this instruction is to compute the bit-by-bit or logical product of the contents of the accumulator and the operand, leaving the result in the accumulator. The even, zero, and positive designators are set or cleared depending on the result in the accumulator. The end-around carry designator is set; the overflow designator is unchanged.

Example:

	(Accumulator)	(Operand)
Initially:	01011	00101
After execution of AND instruction: (Positive designator is set to one; even and zero designators are cleared to zero, and the EAC is set to one.)	00001	00101

EOR
13

EXCLUSIVE OR

Execution time: 18.0 microseconds

For any bit position of the operand which contains a one, the corresponding bit of the accumulator is complemented; all other bit positions of the accumulator remain undisturbed. The even, zero, and positive designators are set or cleared depending on the result in the accumulator. The end-around carry designator is cleared, and the overflow designator is unchanged.

Example:

	(Accumulator)	(Operand)
Initially:	01011	00101
After execution of EOR instruction: (Even and positive designators are set to one; end-around carry and zero designators are cleared to zero.)	01110	00101

LSH
14,15

LEFT SHIFT

Execution time: 18.0 microseconds

Shift the operand to the left one bit position; the high-order bit replaces the low-order bit of the operand. The even, zero, end-around carry, and positive designators are set or cleared depending on the result. The overflow designator is set if the sign of the operand changed as a result of the left shift; otherwise it is unchanged.

For example, the operand = 24505. After LSH, the operand = 11213 with the positive, end-around carry, and overflow designators set to one, all other designators cleared to zero.

RSH
16,17

RIGHT SHIFT

Execution time: 18.0 microseconds

Shift the operand to the right one bit position; the high-order bit is replaced by the original bit. Note that this is an end-off shift and that the low-order bit enters the end-around carry designator. The zero, even, and positive designators are set or cleared depending on the result. The overflow designator is unchanged.

For example, the operand = 24505. After RSH, the operand = 32242 with end-around carry designator set to one, the positive, zero, and even designators cleared to zero.

ZJP
20

*ZERO JUMP

Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump.

If the zero designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. Note that the zero designator will be set by negative zero (all ones) or by positive zero (all zeros). The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

EJP
21

*EVEN JUMP

Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump.

If the even designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. Note that the even designator is set whenever bit 13 and bit 0 of a referenced location are equal. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

SLJ
22

*SET LOCKOUT AND JUMP

Execution time: 13.5 microseconds

Lock out all interrupts and transfer the operand address to the P Register. The designators are not changed as a result of this instruction.

CLJ
23

*CLEAR LOCKOUT AND JUMP

Execution time: 13.5 microseconds

Remove the interrupt lockout and transfer the operand address to the P Register. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following execution of this instruction.

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*Note that when an operand address is transferred to the P Register, the instruction at location operand address plus one is the next instruction to be executed.

JMP 24 *JUMP

Execution time: 13.5 microseconds

Unconditionally transfer the operand address to the P Register. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

CJP 25 *END-AROUND CARRY JUMP

Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump.

If the end-around carry designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

OJP 26 *OVERFLOW JUMP

Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump.

If the overflow designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

PJP 27 *POSITIVE JUMP

Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump.

If the positive designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

INT 30,31 INPUT TO COMPUTER

Execution time: 18.0 microseconds

In the direct mode, data on the input channel specified by bits 0-5 of the instruction are input into the accumulator. In the indirect mode, bits 0-5 of the I/O data word select the input channel and bits 6-11 the word address. The indirect mode should be used with utmost caution; otherwise, conflict with other peripheral devices may occur. The designators are set, cleared, or unchanged as in the ENL instruction.

ENL 32,33 ENTER ACCUMULATOR

Execution time: 18.0 microseconds

Clear the accumulator, then transmit the operand to the accumulator. The even, zero, and positive designators are set or cleared depending on the resultant contents of the accumulator. The end-around carry designator is cleared to zero, and the overflow designator is unchanged.

---

*Note that when an operand address is transferred to the P Register, the instruction at location operand address plus one is the next instruction to be executed.

OUT 34,35 — OUTPUT FROM COMPUTER

Execution time: 18.0 microseconds

If indirectly addressed, the contents of the accumulator are output on the channel selected by bits 0-5 of the I/O data word and the word selected by bits 6-11. In the direct mode, the contents of the accumulator are output on the channel selected by bits 0-5 of the instruction. The designators are set, cleared, or unchanged as in the STL instruction.

RJP 36 — *RETURN JUMP

Execution time: 22.5 microseconds

Store the contents of the P Register in the operand; transfer the operand address to the P Register. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

STL 37 — STORE ACCUMULATOR

Execution time: 18.0 microseconds

Store the contents of the accumulator in the operand. The even, zero, and positive designators are set or cleared, depending on the contents of the accumulator. The end-around carry designator is cleared to zero, and the overflow designator is unchanged.

THE DESIGNATORS

Even Designator

The even designator is affected (set or cleared) by the execution of the following instructions: DCR, CMB, SMB, EDR, ADD, SUB, AND, EOR, LSH, RSH, INT, ENL, OUT, STL.

When the even designator is set by the execution of an instruction other than EDR, it implies that bits 0 and 13 of the result of the instruction are both zero or both one.

Zero Designator

The zero designator is affected (set or cleared) by the execution of the following instructions: DCR, CMB, SMB, EDR, ADD, SUB, AND, EOR, LSH, RSH, INT, ENL, OUT, STL.

When the zero designator is set by the execution of an instruction other than EDR, it implies that the result of the instruction is 00000 or 37777.

Positive Designator

The positive designator is affected (set or cleared) by the execution of the following instructions: DCR, EDR, ADD, SUB, AND, EOR, LSH, RSH, INT, ENL, OUT, STL. The positive designator is always set by the execution of the CMB instruction, always cleared by the execution of the SMB instruction.

When the positive designator is set by the execution of an instruction other than EDR, it implies that bit 13 of the result of the instruction is zero.

*Note that when an operand address is transferred to the P Register, the instruction at location operand address plus one is the next instruction to be executed.

End-Around Carry Designator

The end-around carry designator is affected (set or cleared) by the execution of the following instructions: DCR, EDR, ADD, SUB, LSH, RSH. The end-around carry designator is always cleared when CMB, SMB, EOR, INT, ENL, OUT, and STL instructions are executed. EAC is always set with execution of AND.

When the end-around carry designator is set by the execution of a DCR, ADD, SUB or LSH instruction, it implies that an end-around carry has occurred. When the end-around carry designator is set by the execution of a RSH instruction, it means that the low-order bit of the operand which is shifted off is a one.

Overflow Designator

The overflow designator is set whenever two positive numbers are summed and the result is negative, or two negative numbers are summed and the result is positive. The overflow designator can be set by the execution of the following instructions: DCR, ADD, SUB, LSH. The EDR instruction only can be used to clear the overflow designator.

Designators When Clear

The designators, when clear, indicate the following:

Odd (Even designator)
Non-zero (Zero designator)
Negative (Positive designator)
No end-around carry (End-around carry designator)
No overflow (Overflow designator)

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COMMAND TIMING

Command timing is a list of all commands required to perform a given instruction with respect to order of occurrence.

Before delving into the heart of command timing several things should be established. It is expected that one is familiar with the block diagram including all registers, the various parts of the control section diagram as to why they exist and what they do, and the repertoire of instructions.

Along the left hand margin of command timing is the computer timing with respect to the master clock. The three sets of L0 - L5 which are listed correspond to cycle 0, 1, and 2. The top of the page prior to cycle 0, L0 gives the sequence number and the conditions which must be met for this sequence to be done.

Tracing an instruction through command timing to determine the sequences performed is done as follows. Assume an add instruction is to be done (octal code 10). Start with sequence II. (All instructions start with sequence II.) No conditions are stated for its entrance, therefore we can say and rightfully so that all instructions do sequence II. After an ADD goes through sequence II the computer turns the page to sequence III. No conditions here either so it does sequence III. It then looks at sequence IV. It is not an unsatisfied jump (it is not a jump at all) so the computer says "is the mode bit equal to one?", if yes do sequence IV if not skip sequence IV. After making the decision and either doing or not doing sequence IV the page is turned. Here sequence V is found, but it says this page is only done on an octal code 01, so we turn the page. Can't do this one either. Once past sequence IV we look for the first page with the octal code of the instruction being performed. We finally get to an ADD octal code 10 sequence V. This one we do. Then turn the page and find ADD octal code 10 sequence VI, we do it also. After turning the page again we find SUB octal code 11. As one would find out after turning the balance of the pages all octal codes are placed together in numerical order and in the order performed. That is, because ADD sequence V page is before ADD sequence VI then sequence V must occur before sequence VI. When no more pages can be found for this instruction the computer returns to sequence II to obtain the next instruction.

Prior to looking into the command timing itself some of the terms will be defined. Some of these terms are listed on page 4-7. The following is a more detailed explanation of these and other terms found in the text.

SET READ

The SET READ signal will initiate the reading of the core memory address specified by the select. Remember the core memory location selected is determined by a SELECT S, SELECT P, or SELECT A signal. The reading of a core memory location clears the cores at that address and places their state on the sense winding where it may or may not be gated into the Z register by the READ STROBE command.

The CLEAR READ signal serves only to terminate the read part of the core memory cycle. Because the read operation is a destructive readout the selected memory address will be cleared to zero by the time the clear read command occurs. This location will remain zero until the write operation replaces the original contents or writes new information. If the READ STROBE signal does not occur the information originally in core dies on the sense lines and is lost.

SET WRITE

The SET WRITE signal writes the output of the adder (Z register plus X register) into the memory location determined by the select. This may be the original information in the Z register with the X register cleared. This type of memory cycle is called "read restore". It may be new information in the X register with the Z register cleared (because of no READ STROBE). This type of memory cycle is called "clear write". Or it may be the original information in the Z register and new information in the X register. In which case I don't have the slightest idea what the core memory cycle is called.

READ STROBE

The READ STROBE signal gates the contents of the specified core memory address into the Z register. Contrary to popular belief this is all it does- it does not clear the memory location being read. That is the function of the read and is done whether the READ STROBE is done or not. The READ STROBE is timed to occur at the proper instant to gate this information. It occurs sometime between L4 and L5. For simplicity it is shown to occur at L5. This in no way affects the operation or understanding of command timing.

SET CLAMP

SET CLAMP means to force the specified point to a logical zero. Because the command says SET CLAMP and not just CLAMP it implies that the point is forced to a logical zero and held there. This is exactly what happens. The clamp remains until a CLEAR CLAMP signal occurs. The specified point for the clamp will be one side of a flip-flop (either the cleared or set side). Forcing the cleared side of a flip-flop to a logical zero will set the flip-flop and forcing the set side of a flip-flop to a logical zero will clear it. (re; page 1-43). Remember that just because the clamp is removed or cleared does not mean that the flip-flop will be changed back in its state. For instance when a SET CLAMP $\overline{X0}$ signal occurs the X0 flip-flop will set. When the CLEAR CLAMP $\overline{X0}$ signal occurs the flip-flop will not be cleared; it will only stop being held set.

CLEAR CLAMP

As the above states a CLEAR CLAMP signal removes the forced logical zero from the specified point.

DL

Designator logics (DL) are the logics used to examine the Z register, X register, and adder output when the designators are being set. The command DL → DESIGNATORS means examine these and set the designators accordingly.

IL

Interrupt lockout (IL) is a flip-flop which will prevent the recognition and processing of any interrupt while it is set. The command SET SET IL may sound like a stuttering typewriter but is stated that way for a purpose. If the command were labeled SET IL it would mean that the command occurred only during the tap time specified. But this is not the case; the SET SET IL signal means that the IL flip-flop is held set from that time until the SET IL signal is removed by a CLEAR SET IL. It may be asked now - "if we set the IL flip-flop and hold it set for a period of time why not use SET CLAMP $\overline{\text{IL}}$ and CLEAR CLAMP $\overline{\text{IL}}$". The not so obvious reason is that the $\overline{\text{IL}}$ point is not clamped. That is the cleared side of the IL flip-flop is not held to a logical zero directly. The flip-flop is held set by fully enabling the input gates to the set side for this period of time. Operating in the same manner one will find a SET CLEAR IL and a CLEAR CLEAR IL. The clearing of the CLEAR IL signal does not set the IL flip-flop, and the clearing of the SET IL signal does not clear the IL flip-flop.

HA, SA

These stand for sequence half advance (HA) and sequence advance (SA). HA and SA are flip-flop registers (three each) which are used to handle the advancing form one sequence to another. HA, in basic terms, tells the computer which sequence will be done next and SA tells the computer what sequence is being done now.
Assume the computer is doing sequence II. At cycle 0, L0 HA and SA both contain the value for sequence II. At cycle 2, L1 HA is cleared in preparation for cycle 2, L3 setting it to the next sequence to be done. (Sequence III). The computer now knows that it is doing sequence II (by SA) and that it will do sequence III next (by HA). At cycle 2, L5 SET SA causes HA to be transferred to SA, and the computer now does sequence III. Because of the L5, L0 overlap this time can also be considered cycle 0, L0 of the next sequence (III). Now one may look at HA and say that since HA is still set to sequence III the computer thinks it will do sequence III next. The statement made before that HA tells the computer what sequence will be done next is still true if we realize that the computer only asks during cycle 2, L5 when it wishes to advance SA.

SET I/O PULSE

This signal causes the drive currents to be routed through the input output addressing section of the computer not the core memory section. This is necessary because the same S register and translating circuitry is used for both input output and the core memory.

Note page 4-8. This page is drawn in an altogether different manner than the others. This was done by mistake and has not been changed because it is a very good

way to remind one that sequence I is totally different from the rest. This is about all that will be mentioned about sequence I at this time. It will be covered in detail in the section on interrupts.

Reference sequence III cycle 2, L4. The subscript 0-7 means that only bits 0 through 7 of the S register will be affected, bits 8 through 13 will not be changed. The arrow after ADDER means "is transferred to". ( ) means the contents of the specified register.

Refer to ZJP instruction octal code 20 sequence VII, cycle 0, L1. The (S) means just what it implies. The actual contents of the S register is transferred to the Z register not the contents of the memory location specified by the S register.

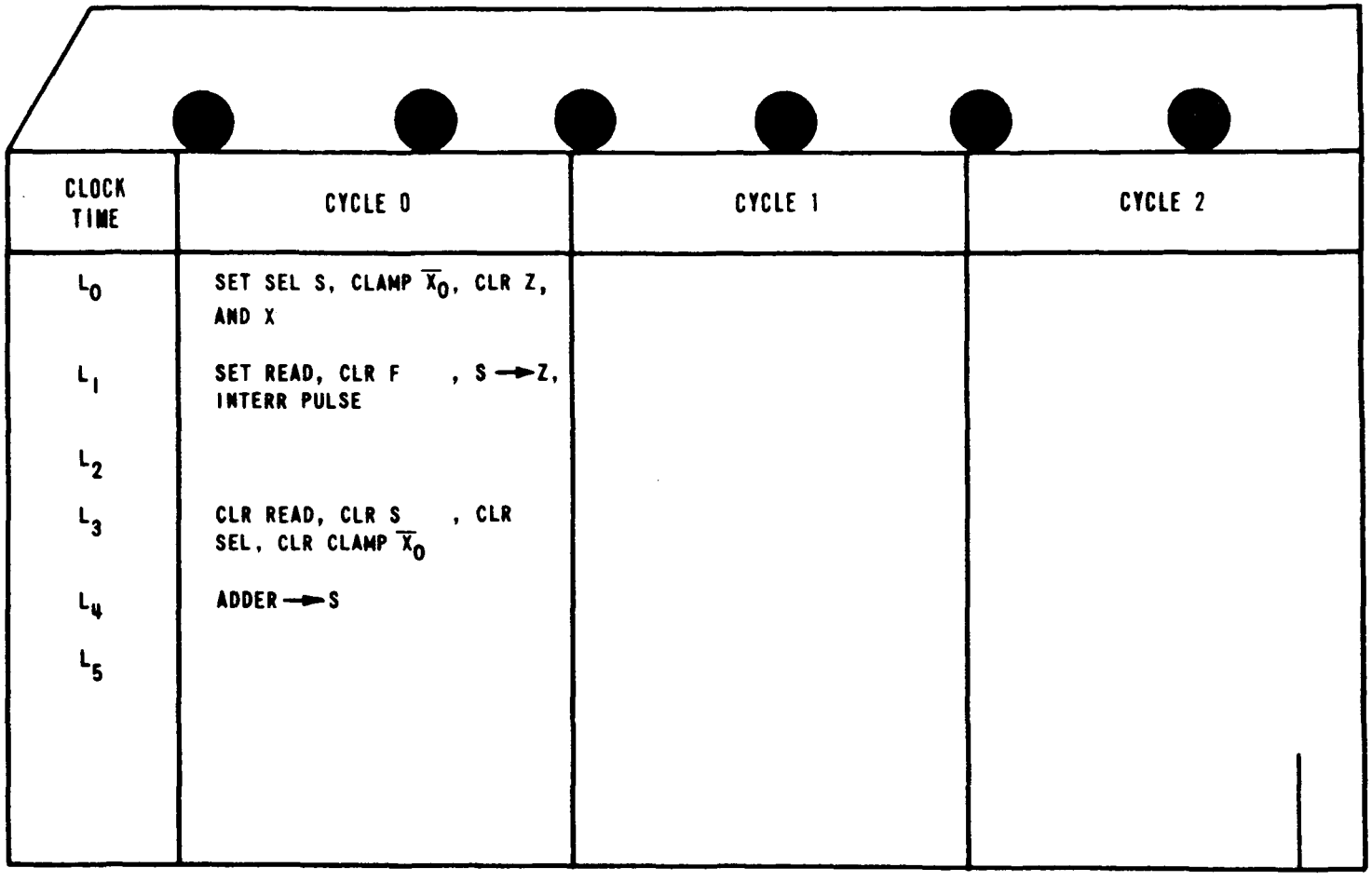
Refer to EDR instruction octal code 05, sequence V, cycle 1, L5. The CLEAR DESIGNATOR TO "1"s command means that all the designator flip-flops will be in the one or set state as a result of this command. This is not the only register which is set to all ones prior to entering, but in this case the computer may stop (if in cycle step re; page 1-71) after the clearing and before the entering. It could be confusing and lead one astray if it said CLEAR DESIGNATORS and all the lights were lit in the designator register. In the other case the computer cannot stop before entering. Therefore only the end result could be seen and could not be confusing.

Figure page 4-6 shows the opposite view of command timing from the sequential list based on the instructions. In this chart the commands and sequences are shown along the left, and three cycles of time along the top. The black bar in the main body of the chart shows that the command or condition exists at the time shown directly above.

Command Sequencing (Timing)

The description that follows contains details of command sequencing of the P-50 computing control system.

Set read-	Initiate the reading of the core memory address specified by the select.
Set write-	Write the output of the adder into the core memory address specified by the select.
Read strobe-	Gate the contents of the core memory address specified by the select, into the Z register.
Set clamp-	Force the specified point to a logical zero until a clear clamp signal is received.
Clear clamp-	Remove the forced logical zero from the specified point.
DL-	Designator logics
IL-	Interrupt lockout
HA-	Sequence half-advance flip-flops
SA-	Sequence advance flip-flops
Set I/O pulse-	Turn on the channel and word drives in the peripheral equipment.



CLOCK TIME	CYCLE 0	CYCLE 1	CYCLE 2
L_0	SET SEL S, CLAMP $\overline{X}_0$, CLR Z, AND X		
L_1	SET READ, CLR F , S → Z, INTERR PULSE		
L_2			
L_3	CLR READ, CLR S , CLR SEL, CLR CLAMP $\overline{X}_0$		
L_4	ADDER → S		
L_5			

SEQUENCE I

SEQUENCE II

L_0	CLEAR Z AND X, SET SELECT "P", SET CLAMP $\overline{XO}$
L_1	CLEAR F, SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR S, CLEAR CLAMP $\overline{XO}$, CLEAR WRITE
L_4	ADDER $\longrightarrow$ S
L_5	SET SA

SEQUENCE III

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA, $(Z)_{8-13} \longrightarrow F$
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR S_{0-7}, CLEAR WRITE
L_4	ADDER $\longrightarrow S_{0-7}$
L_5	SET SA

IF F = 22 OR 23 INTERRUPT LOCKOUT WILL BE SET OR CLEARED DURING L_3 AND L_4 TIME OF CYCLE 2 IF THE MODE BIT = 0.

SEQUENCE IV

(NOTE: This sequence takes place only if the mode bit = 1 and there is no unsatisfied jump.)

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR "S", CLEAR WRITE
L_4	ADDER ⟶ S
L_5	SET SA

IF F = 22 OR 23 INTERRUPT LOCKOUT WILL BE SET OR CLEARED DURING L_3 AND L_4 TIME OF CYCLE 2.

DCR

OCTAL CODE: 01

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S" NOTE: CLAMP X_o SET BY PREVIOUS L_5
L_1	SET READ, $(\bar{Z}) \longrightarrow X$
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATOR
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL $\longrightarrow$ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, $(\bar{Z}) \longrightarrow X$
L_4	
L_5	SET SA, CLEAR CLAMP X_o

CMB

OCTAL CODE: 02

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S" NOTE: CLAMP Z_{13} SET BY PREVIOUS L_5
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATOR
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z) ⟶ X
L_4	
L_5	SET SA, CLEAR CLAMP Z_{13}

SMB

OTAL CODE: 03

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S" NOTE: CLAMP $\overline{Z_{13}}$ SET BY PREVIOUS L_5
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATOR
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z) ⟶ X
L_4	
L_5	SET SA, CLEAR CLAMP $\overline{Z_{13}}$

EDR

OCTAL CODE: 05

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATOR
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	CLEAR DESIGNATOR TO "1" S
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z) $\longrightarrow$ DESIGNATOR, (Z) $\longrightarrow$ X
L_4	
L_5	SET SA

SDR

OCTAL CODE: 06, 07

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ, SET DESIGNATOR $\longrightarrow Z_{0-4}$
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ, CLEAR DESIGNATOR $\longrightarrow Z_{0-4}$
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, $(\vec{Z}) \longrightarrow X$
L_4	
L_5	

ADD

OCTAL CODE: 10

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z)$\longrightarrow$X
L_4	
L_5	SET SA

ADD

OCTAL CODE: 10

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "A"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT A, CLEAR WRITE
L_4	
L_5	SET SA

SUB

OCTAL CODE: 11

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", $(\overline{Z}) \longrightarrow X$, CLEAR WRITE
L_4	
L_5	SET SA

SUB

OCTAL CODE: 11

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "A"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_6	
L_7	CLEAR READ
L_0	
L_1	SET WRITE
L_2	
L_3	DL ⟶ DESIGNATOR
L_4	
L_5	
L_6	
L_7	CLEAR HA
L_0	
L_1	SET HA, CLEAR SELECT "A", CLEAR WRITE
L_2	
L_3	SET SA
L_4	
L_5	

AND

OCTAL CODE: 12

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z) $\longrightarrow$ X
L_4	
L_5	SET SA

AND

OCTAL CODE: 12

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "A", SET AND
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "A", CLEAR WRITE
L_4	
L_5	SET SA, CLEAR AND

EOR

OCTAL CODE: 13

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", (Z) $\longrightarrow$ X, CLEAR WRITE
L_4	
L_5	SET SA

EOR

OCTAL CODE: 13

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "A", SET EOR
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "A", CLEAR WRITE
L_4	
L_5	SET SA, CLEAR EOR

LSH

OCTAL CODE: 14, 15

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z) $\longrightarrow$ X
L_4	
L_5	SET SA

LSH

OCTAL CODE: 14, 15

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE
L_4	
L_5	SET SA

RSH

OCTAL CODE: 16, 17

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, $(\vec{Z}) \longrightarrow X$
L_4	
L_5	SET SA

RSH

OCTAL CODE: 16, 17

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE
L_4	
L_5	SET SA

ZJP

OCTAL CODE: 20

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

EJP

OCTAL CODE: 21

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

SLJ

OCTAL CODE: 22

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	SET SET IL
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA, CLEAR SET IL
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

CLJ

OCTAL CODE: 23

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	SET CLEAR IL
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA, CLEAR CLEAR IL
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

JMP

OCTAL CODE: 24

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

CJP

OCTAL CODE: 25

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

OJP

OCTAL CODE: 26

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S)$\longrightarrow$ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

PJP

OCTAL CODE: 27

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

INT

OCTAL CODE: 30

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S", SET I/O PULSE
L_1	SET READ
L_2	
L_3	
L_4	
L_5	CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	INPUT STROBE
L_5	
L_0	
L_1	CLR HA
L_2	
L_3	SET HA CLEAR SELECT "S", (Z) $\longrightarrow$ X, CLEAR I/O PULSE, CLEAR WRITE
L_4	
L_5	SET SA

INT

OCTAL CODE: 30

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "A"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "A", CLEAR WRITE
L_4	
L_5	SET SA

ENL

OCTAL CODE: 32, 33

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE, (Z) $\longrightarrow$ X
L_4	
L_5	SET SA

ENL

OCTAL CODE: 32, 33

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "A"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "A", CLEAR WRITE
L_4	
L_5	SET SA

OUT

OCTAL CODE: 34

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "A"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "A", CLEAR WRITE, Z ⟶ X
L_4	
L_5	SET SA

OUT

OCTAL CODE: 34

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "S", SET I/O PULSE
L_1	SET READ
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLR HA
L_2	
L_3	SET HA CLEAR I/O PULSE, CLEAR SELECT "S", CLEAR WRITE
L_4	
L_5	SET SA

RJP

OCTAL CODE: 36

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE, (Z)$\longrightarrow$X
L_4	
L_5	SET SA

RJP

OCTAL CODE: 36

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE
L_4	
L_5	SET SA

RJP

OCTAL CODE: 36

SEQUENCE VII

L_0	CLEAR Z AND X, SET SELECT "P"
L_1	SET READ, (S) ⟶ Z
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "P", CLEAR WRITE
L_4	
L_5	SET SA

STL

OCTAL CODE: 37

SEQUENCE V

L_0	CLEAR Z AND X, SET SELECT "A"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	READ STROBE, CLEAR DESIGNATORS
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "A", CLEAR WRITE, (Z)$\longrightarrow$X
L_4	
L_5	SET SA

STL

OCTAL CODE: 37

SEQUENCE VI

L_0	CLEAR Z, SET SELECT "S"
L_1	SET READ
L_2	
L_3	
L_4	
L_5	
L_0	
L_1	CLEAR READ
L_2	
L_3	SET WRITE
L_4	
L_5	DL ⟶ DESIGNATOR
L_0	
L_1	CLEAR HA
L_2	
L_3	SET HA, CLEAR SELECT "S", CLEAR WRITE
L_4	
L_5	SET SA

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DUAL NAND

The dual NAND consists of two NAND circuits which are identical except for the number of input pins (see Figure 1-12). The two NANDS will be designated by the output pin numbers 5 and 11. Side 11 will be discussed and related to side 5 later.

There are three types of inputs. Pins 6, 7 and 8 are internal diode inputs, pin 9 is an external diode input, and pin 4 is a special input which is normally connected to +6V. As many input diodes as desired may be added to pin 9 to increase input capabilities. If a logical one is applied to all used inputs the output on pin 11 will be a logical zero, and conversely if a logical zero is applied to any input pin the output will be a logical one.

The output of the NAND as described has current capabilities of driving a maximum of ten inputs. If it is desired to drive more than this but less than 21, the current capabilities can be increased by adding a resistor from pin 9 to +6V. This in no way changes the previously described operation; it only increases the fan out capability of the circuit.

Some of the circuits require one of the inputs to be from the master clock. Since the master clock taps are +12V instead of +6V, it is necessary to connect this tap through a dropping resistor to pin 9. When this is done pin 4 must be grounded. Since pin 4 is common to both NAND circuits this ground puts a logical zero on the input of circuit 5. To compensate for this a resistor must be placed from pin 3 to +6V. If it is desired to enable both NANDS with the same master clock tap it can be done by connecting a resistor from pin 4 to this tap. Pin 4 would not be connected to +6V in this case. The logical operation of circuit 5 is identical to the operation of circuit 11, except for the change of pin numbers and the lack of the additional internal input diode.

MODIFIED DUAL NAND

The modified dual NAND is similar in operation to the NAND with the exception of a few points (see Figure 1-13). Pins 11 and 12 are the outputs for their respective circuits. Pins 1, 3, 6, and 7 are internal diode inputs and pins 2 and 8 are external diode inputs for their circuits. Pin 13 is used for an additional group of inputs. To accomplish this, an additional circuit, similar to the one between the base of the transistor and the input pins 1, 2, 3, and 4 is connected to pin 13. The operation of pin 9 is the same. Pins 4 and 5 serve the same function as pin 4 in the non-modified dual NAND.

SLOW NAND

The only difference between the modified dual NAND and the slow NAND (Figure 1-14) is the rise time of the circuit. As the name implies the slow NAND has a slower rise time than the modified dual NAND. Otherwise its logic function is identical. Pin numbers differ in the following manner. Pin 1 of the slow NAND corresponds to pin 10 of the modified NAND. 2 to 4, 3 to 2, 4 to 1 & 3, 5 to 12, 6 to 13, 7 to 5, 8 to 6 & 7, 9 to 8, 10 to 11 and pin 11 of the slow NAND to 9 of the modified NAND.

FLIP-FLOP

The logical operation of a flip-flop is as follows: Refer to Figure 1-15. We will start by stating that neither of the B NANDS have all ones in. Therefore, both B NANDS will have a logical one out. Note at this time that the output of A11 is fed back to the input of A5 and the output of A5 to the input of A11. This hookup makes it a flip-flop. We can now see that if pin 2 of A5 and pin 7 of A11 are ones that the logical signal on A5 cannot equal the logical signal on A11. Let's try and see why. If we assume both to be a one, this means that A11 is a one. A11 is connected to A5 pin 1, which would also be a one. If A5 pin 1 is a one and, as we stated, A5 pin 2 was a one, this means that all inputs to A5 are logical ones and the output is then a zero. Also, if we assume both A5 and A11 outputs to be zeros, then the zero on A11 output would be connected to A5 pin 1, which would cause a one at the output of A5. Now that we have seen that A5 and A11 outputs cannot be the same, we can arbitrarily assume some logical signals on them. We will assume A5 output is a zero and A11 output is a one. The one from A11 output is connected to the input pin 1 of A5 which in conjunction with pin 2 will hold the zero at the output of A5, which is connected to input 6 of A11, which holds the one on the output of A11, etc. We can now say that the flip-flop A is in a stable state.

There are only two ways to affect the state of this flip-flop. The first to be discussed is to place a zero on one of the inputs of the side with the logical zero out. If we look at Figure 1-15 again, this means we must put a logical zero on pin 2 of A5 in order to affect the flip-flop. This zero on pin 2 of A5 will cause the output of A5 to go to a logical one. This logical one is then applied to pin 6 of A11 and in conjunction with the one on pin 7 will cause a logical zero out of A11. This zero at the output of A11 is then applied to the input pin 1 of A5 holding the one at the output of A5. Now the input on pin 2 of A5 can go back to a logical one because pin 1 is now taking over. This entire flipping or changing state of the flip-flop from the zero appearing on pin 2 of A5 until it is stable in the flipped state took less than .1usec.

The second method by which the flip-flop can be affected is by placing a ground or logical zero on the output of the side which is a logical one. As one can see from the schematics of the NAND circuit, a logical zero is created by grounding a point through a transistor and it can also be seen that if a logical one and a zero attempt to appear on the same point at the same time, the zero will be the resultant signal. Now, if we have the flip-flop in our original state where A11 output was a logical one and we put a zero at this point, the zero is the resultant. This zero is applied to the input pin 1 of A5 and the circuit will flip as explained above because we have placed a zero on one input of the side which has a zero output.

One of the stable states of the flip-flop will be called the set state and one the cleared state. We will say that the set state is when A5 output is a one. This means that the cleared state is when A11 output is a one. This is just an arbitrary choice of the designer. Either state could be called set or cleared. It can now be seen that if we set the flip-flop that A5 output will be a one and A11 output will be a zero, and if we clear the flip-flop that A5 output will be a zero and A11 output will be a one. Many flip-flops in the system have names such as the R flip-flop, SEL flip-flop, HIT flip-flop, etc. Let us call ours the CAT flip-flop. We will label the output lines of this flip-flop to give an

indication of the flip-flop's state. The label CAT means that this line will be a logical one when the CAT flip-flop is set and the signal $\overline{CAT}$ will mean that this line will be a logical one when the CAT flip-flop is not set or $\overline{CAT}$ means zero implies CAT flip-flop set. This is because CAT and $\overline{CAT}$ must always be opposite.

As we mentioned before, pin 2 of A5 and pin 7 of A11 was one and was to control the state of the CAT flip-flop. Again, referring to Figure 1-15, let us look at B5 and B11. It can be seen that the outputs of these NANDS will determine the state of the CAT flip-flop. A zero on the output of B5 will insure that the CAT flip-flop is set and a zero on the output of B11 will insure that the CAT flip-flop is cleared. Ones at their outputs have no effect. Let us consider what it takes to get a zero at the output of a NAND. The answer is all ones in. Now let us look at the input to B5. Pin 1 will be one when the R flip-flop is set; pin 2 will be a one when the HIT flip-flop is not set (is cleared); and pin 3 will be a one when the SEL flip-flop is set. Thus, we can tell what will set the CAT flip-flop without looking any further than its input gating circuitry. Now let's see what will clear it. The inputs to B11 are as follows: Pin 6 will be a one when the W flip-flop is set; pin 7 will be a logical one during sequence VII; and pin 9 will be a one if a jump condition has been met and we are doing a jump instruction. Of course, I know these last two were not obvious but they do at least point out that a logical label can be of a great assistance and that a logical label does not have to refer to a flip-flop state.

REGISTER TRANSFERS

Figure 1-16 shows two registers of three flip-flops each and associated gating circuitry. Flip-flops A, B, and C are drawn as 3 flip-flops of the X register- bits 2, 1, and 0 respectively. Flip-flops D, E, and F are drawn as 3 flip-flops of the Z register- bits 2, 1, and 0 respectively. NANDS H, J, K, L, and M are the input gating circuitry for the X register. A normal transfer from the Z register to the X register consists of first clearing the X register (putting all the flip-flops in a predetermined state, in our case the cleared state) and then setting those flip-flops with one input gate fully enabled. Therefore the method used here will be for the $\overline{\text{CLR}}$ X signal to go to a logical zero and then one of the signals ($\overline{Z} \rightarrow X$, $\overline{\overline{Z}} \rightarrow X$, or $Z \rightarrow X$) will go to a logical one. For this discussion we will assume that the Z register is set as follows. Flip-flop F set, flip-flop E cleared, and flip-flop D set. This may also be expressed as Z2, $\overline{Z1}$, and Z0 being a logical one. The first part of the transfer will be the clearing of the X register. This is done by putting a logical zero on the $\overline{\text{CLR}}$ X line. This logical zero is placed on one input of the clear side of each flip-flop in the X register. The X register is then in the $\overline{X2}$, $\overline{X1}$, $\overline{X0}$ state. That is $\overline{X2}$, $\overline{X1}$, and $\overline{X0}$ are logical ones. Then one of the transfer signals will go to a logical one. First we will assume that a direct $Z \rightarrow X$ transfer will be done. This means that the $\overline{Z} \rightarrow X$ line will go to a logical one. The others must remain a logical zero and the $\overline{\text{CLR}}$ X must have gone back to a logical one. The logical one from $Z \rightarrow X$ will be presented to one input of each NAND H11, J11, and K11. Now let's look at the other inputs to those NANDS. H11 has its other input a logical one because we originally stated that Z2 was set. J11 has its other input a logical zero and K11 has its other input a logical one. These are also because of the original state of the Z register. H11 and K11 have all used inputs a logical one and therefore their outputs will go to a logical zero.* The output of H11 and K11 going to a logical zero will cause A and C flip-flops to set. (One may also find a flip-flop named for one of its sides. That is the A flip-flop could also be called the X2 flip-flop no matter what its state. One may see it said "the X2 flip-flop cleared or the X2 flip-flop set".) We now have the X2 and X0 flip-flops set. How about the X1 flip-flop. Remember we said that J11 had one input a logical zero because of the Z register. This means that the output of J11 will be a logical one no matter what the other input does. The X1 flip-flop therefore could not be set. We now have the X register in the following state X2, $\overline{X1}$, and X0 a logical one. This is identical to the corresponding bits of the Z register. We have therefore copied into or transferred into the X register the original contents of the Z register. It is important to note that the transfer from one register to another does not change the source register. The Z register being the source register still has its original contents. Review this operation and make sure that you understand it as this is one more of the basic building blocks in understanding the PRODAC 50 computer system.

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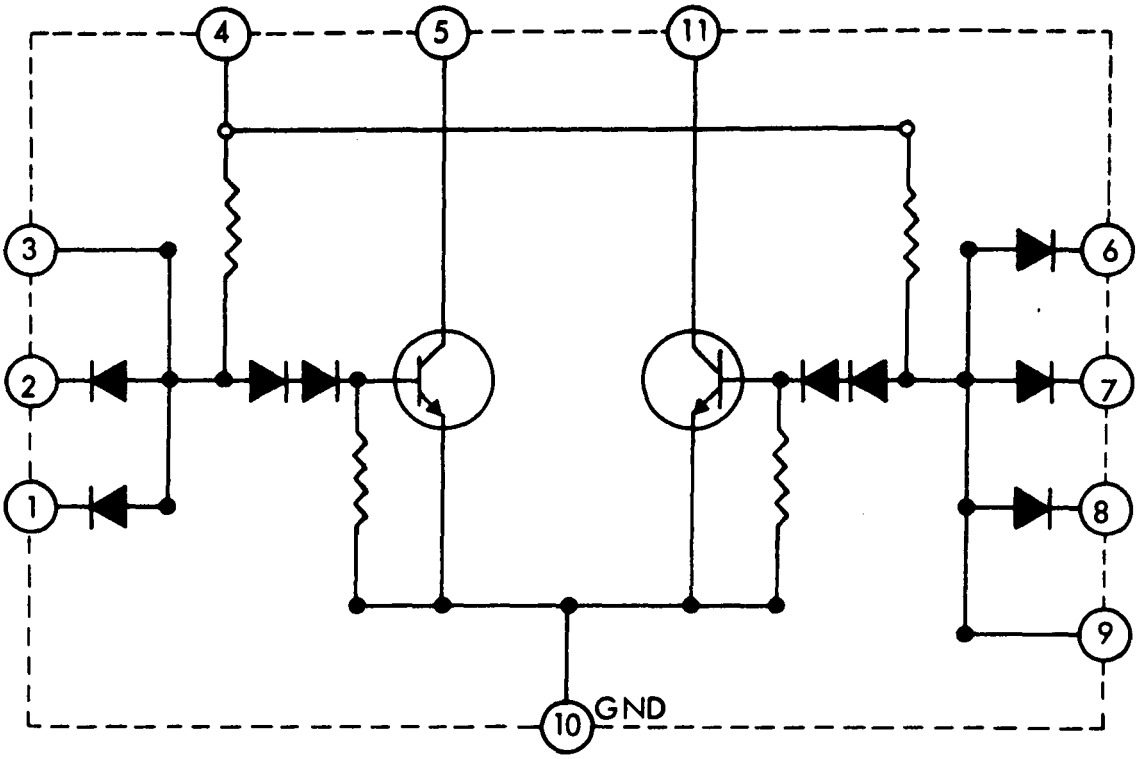
*Remember that a logical one is +6V and a logical zero is 0V or ground. If a logical one and a logical zero are placed at the same point at the same time, the logical zero will be the end result by grounding out the logical one.

Now we will call upon the knowledge gained in the flip-flop and basic transfer write-ups. Again assume the Z register is in the Z2, $\overline{Z1}$, and Z0 state, with the $Z \rightarrow X$ transfer signal back to a logical zero. Make the $\overline{CLR}$ X signal go to a logical zero then back to a logical one. Now let the $\overline{Z} \rightarrow X$ signal go from a logical zero to a logical one and back to a logical zero. While this signal was a logical one note the operation of NANDS H5, J5, and K5. J5 is the only one fully enabled, therefore X1 is the only flip-flop to be set. Note that wherever a flip-flop of Z was set that the corresponding flip-flop of X is cleared and wherever a flip-flop of Z was cleared that the corresponding flip-flop of X is set. This means that we have taken the complement of Z to X. As the name $\overline{Z} \rightarrow X$ implies, transfer the cleared side of Z to the set side of X or made the set side of X the same as the cleared side Z. Review this operation, when it is fully understood, continue on.

Again assume the Z register in the Z2, $\overline{Z1}$, Z0 state. Let the $\overline{CLR}$ X signal go to a logical zero then back to a logical one. Now let the $\overline{Z} \rightarrow X$ signal (Z right shifted to X) go to a logical one and back to a logical zero. Note the end result in the X register. X0 contains what Z1 did. X1 contains what Z2 did. The line labeled "from Z3" means that it comes from the set side of the Z3 flip-flop. (The word "from" will not appear in the logics, it is used now for clarity.) This means that X2 will contain what Z3 did. As an end result the Z register was transferred to the X register displaced one place to the right or right shifted one place. Note that the Z0 flip-flop in this figure goes no place. If you can recall the RSH instruction the state of the Z0 flip-flop will be transferred to the "end around carry designator" flip-flop.



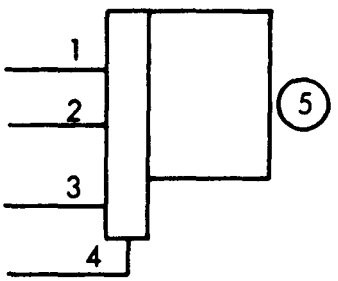
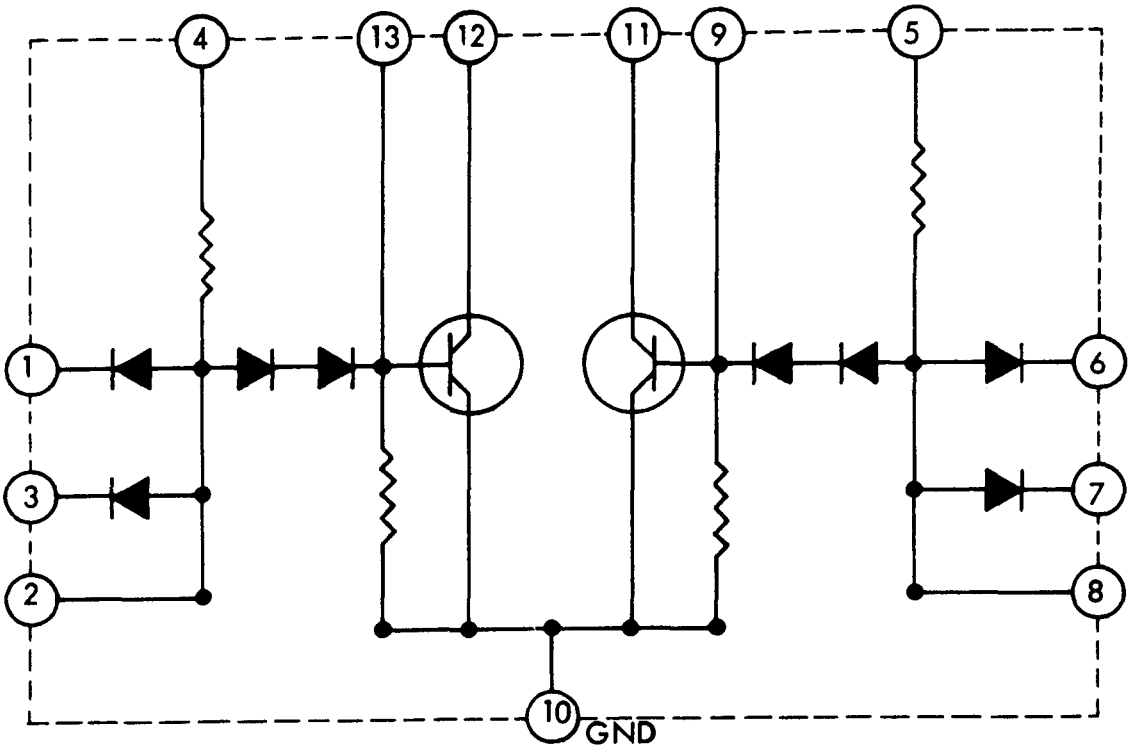


Figure 1-12. Dual NAND



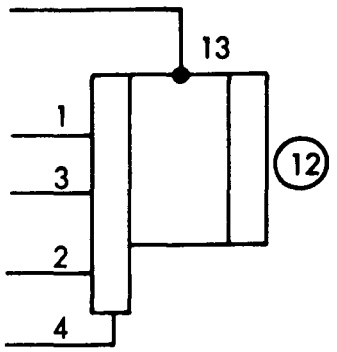


Figure 1-13. Modified Dual NAND

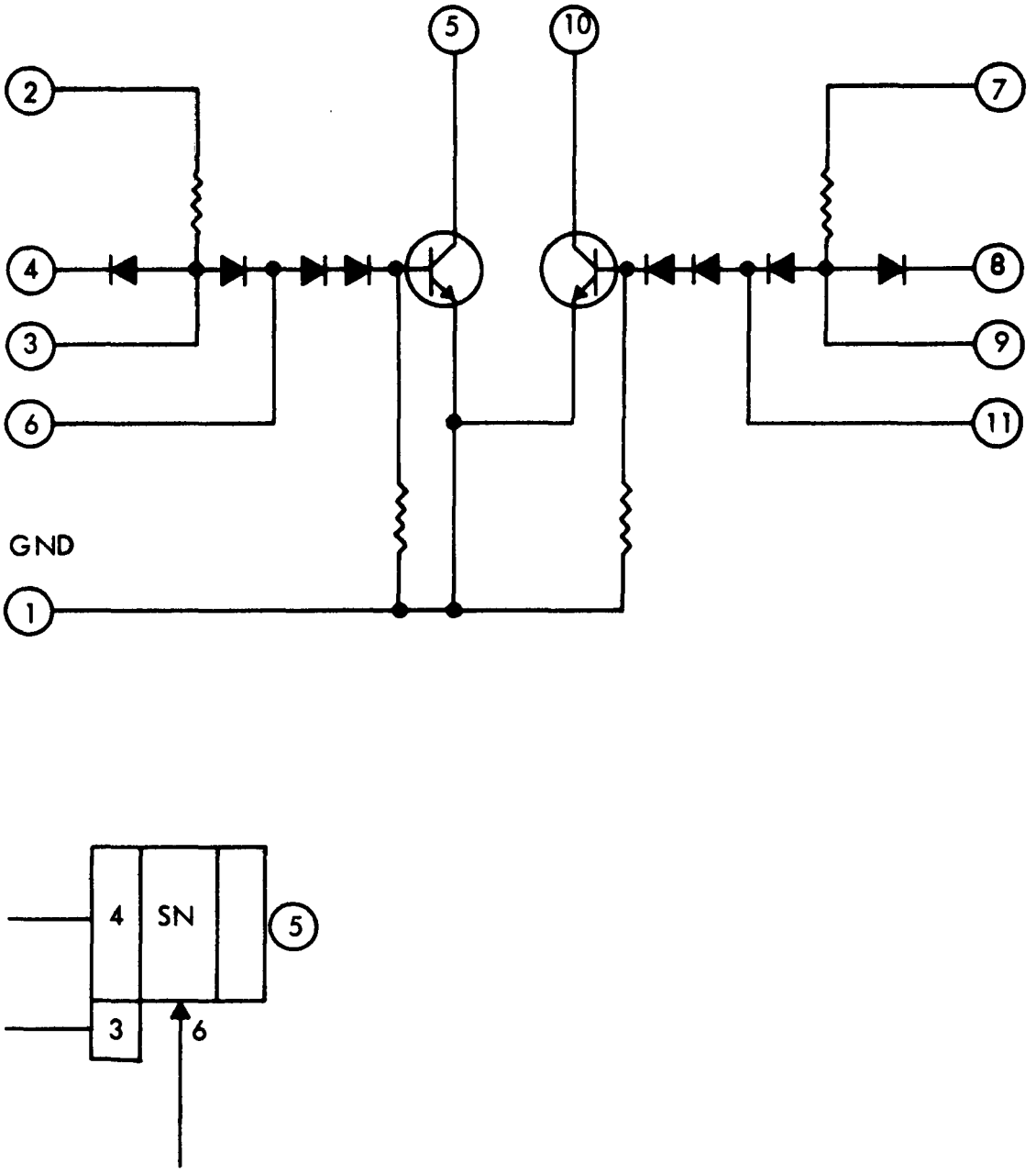


Figure 1-14. Slow NAND

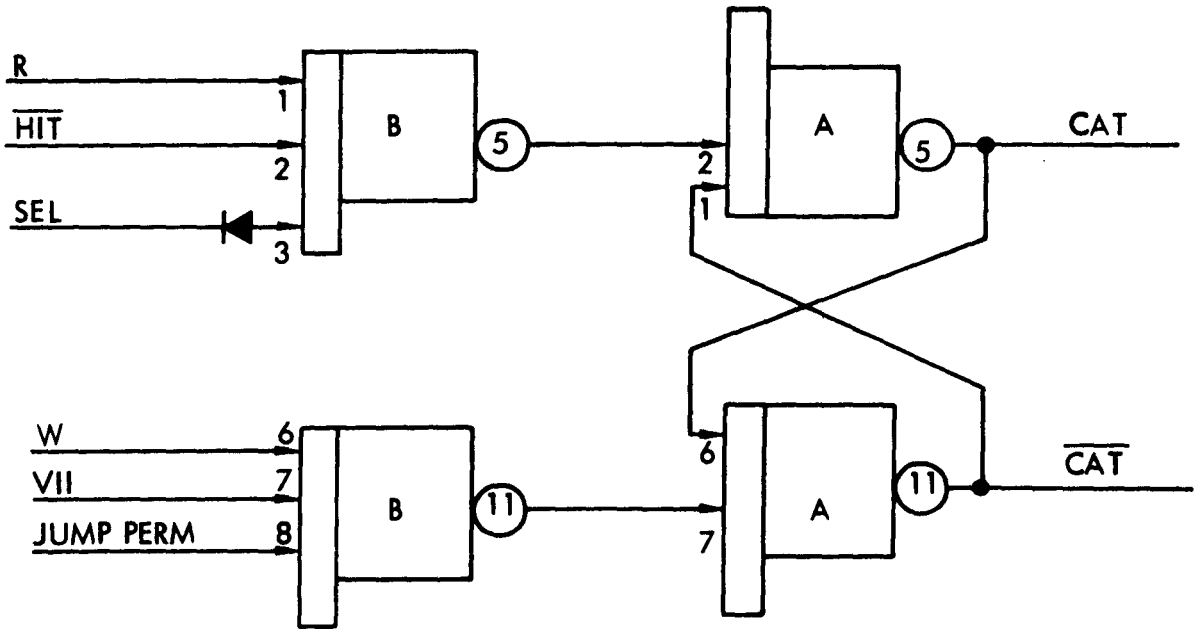


Figure 1-15.

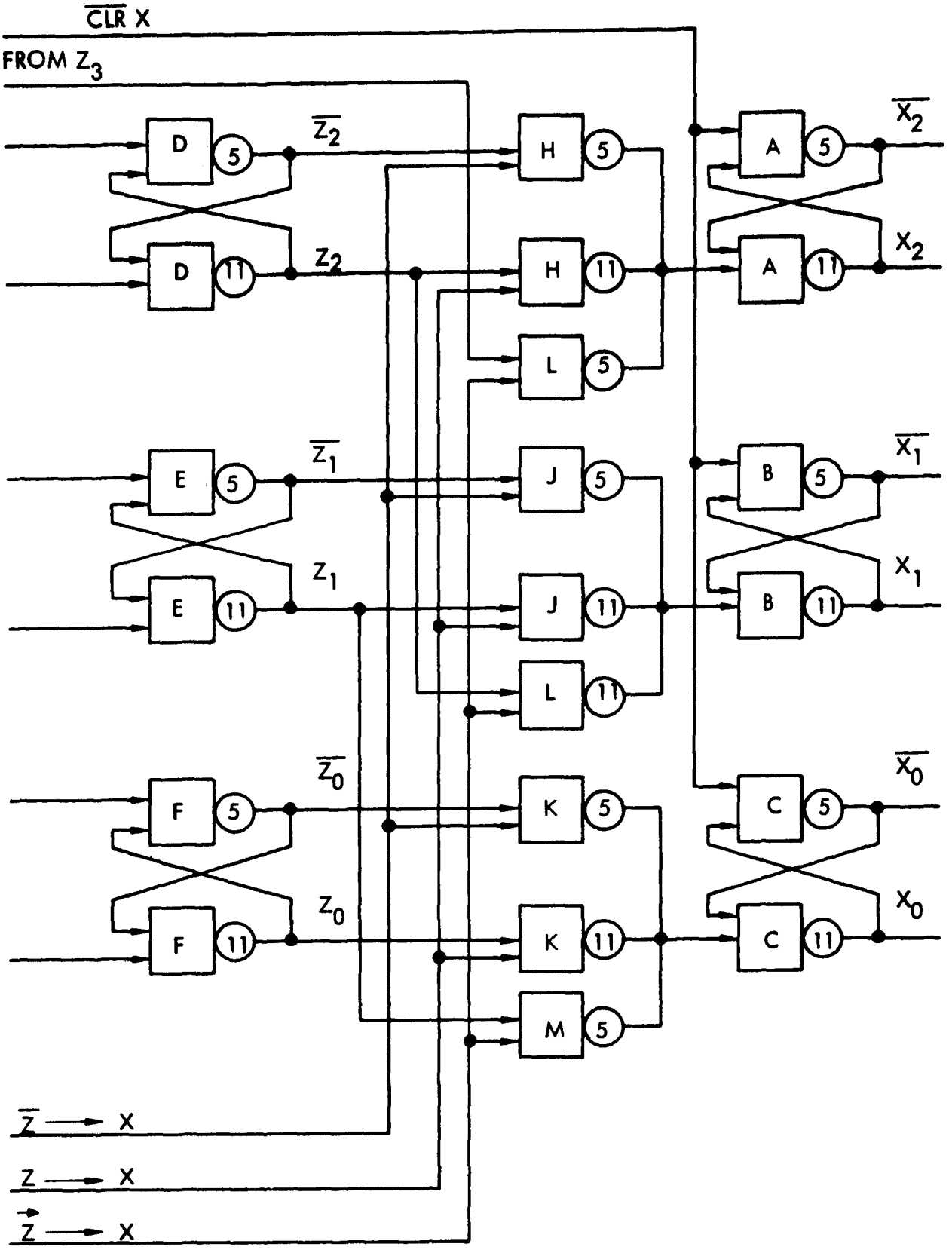

$\overline{CLR}$ X
FROM Z_3
D
5
$\overline{Z_2}$
D
11
Z_2
H
5
H
11
L
5
A
5
$\overline{X_2}$
A
11
X_2
E
5
$\overline{Z_1}$
E
11
Z_1
J
5
J
11
L
11
B
5
$\overline{X_1}$
B
11
X_1
F
5
$\overline{Z_0}$
F
11
Z_0
K
5
K
11
M
5
C
5
$\overline{X_0}$
C
11
X_0
$\overline{Z}$ → X
Z → X
$\vec{Z}$ → X

Figure 1-16.

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1-15. CAPACITOR VALUE CODES

Code	Capacitance	Voltage	Westinghouse Part No.
C1	.0005 μF	50V	742A976H01
C2	.0015 μF	500V	742A976H02
C3	.003 μF	200V	742A976H03
C4	.01 μF	100V	742A976H04
C5	.02 μF	100V	742A976H05
C6	.1 μF	100V	742A976H06
C7	.1 μF	600V	742A976H07
C8	---	---	---
C9	.5 μF	200V	742A976H31
C10	2.0 μF	100V	742A976H09
C11	.1 μF	50V	742A976H10
C12	.05 μF	200V	742A976H11
C13	---	---	---
C14	3 μF	100V	742A976H12
C15	15 μF	100V	742A976H13
C16	250 μF	40V	742A976H14
C17	100 μμF	500V	742A976H15
C18	820 μμF	100V	742A976H16
C19	200 μμF	500V	742A976H17
C20	300 μμF	200V	742A976H18
C21	.1 μF	100V	742A976H06
C22	2 μF	100V	742A976H09
C23	.5 μF	200V	742A976H08
C24	.33 μF	200V	742A976H19
C25	.001 μF	50V	742A976H20
C26	5 μF	100V	742A976H21
C27	10 μF	100V	742A976H22
C28	2000 μF	50V	742A976H23
C29	500 μμF	1kV	669A076H01
C30	10 μF	200V	743A035H04
C31	---	---	---
C32	1.0 μF	200V	669A077H08
C33	30 μF	30V	669A093H02
C34	0.1 μF	200V	669A077H05
C35	30 μF	200V	743A035H03
C36	200 μμF	1kV	669A076H02
C37	0.22 μF	25V	669A094H01
C38	200 μF	125V	669A103H01
C39	100 μF	250V	742A976H25
C40	200 μF	1kV	669A076H05
C41	50 μμF	500V	742A976H26
C42	27 μF	35V	775A436H03
C43	250 μF	50V	742A976H29
C44	10 μμF	100V	742A976H30
C45	4.7 μF	35V	775A436H04
C46	0.47 μF	35V	775A436H05
C47	10.0 μF	50V	742A976H32
C48	0.001 μF	200V	742A976H33
C49	0.01 μF	200V	742A976H34
C50	0.05 μF	200V	742A976H35
C51	0.1 μF	200V	742A976H36
C52	0.5 μF	200V	742A976H08
C53	22 μF	15V	742A976H37

1-16. RESISTOR VALUE CODES

Code	Ohms	Watts	Westinghouse Part No.
R1	1k	1/10	742A969H02
R2	1.5k	1/10	742A969H03
R3	3.01k	1/10	742A969H04
R4	4.32k	1/10	742A969H05
R5	20Ω	1/10	742A969H01
R6	7.68k	1/2	742A971H39
R7	432Ω	1/2	742A971H11
R8	51.1Ω	1/2	742A971H15
R9	6.19k	1/2	742A971H37
R10	20Ω	1/2	742A971H02
R11	10Ω	1/2	742A971H01
R12	35.7Ω	1/2	742A971H03
R13	82.5Ω	1/2	742A971H04
R14	100Ω	1/2	742A971H05
R15	140Ω	1/2	742A971H06
R16	200Ω	1/2	742A971H08
R17	261Ω	1/2	742A971H09
R18	301Ω	1/2	742A971H10
R19	511Ω	1/2	742A971H12
R20	681Ω	1/2	742A971H13
R21	1k	1/2	742A971H30
R22	1.5k	1/2	742A971H31
R23	2k	1/2	742A971H32
R24	2.43k	1/2	742A971H33
R25	3.01k	1/2	742A971H34
R26	4.32k	1/2	742A971H35
R27	4.99k	1/2	742A971H36
R28	10k	1/2	742A971H41
R29	13k	1/2	742A971H43
R30	22.1k	1/2	742A971H47
R31	15k	1/2	742A971H45
R32	150Ω	1/2	742A971H07
R33	18.2k	1/2	742A971H46
R34	8.25k	1/2	742A971H40
R35	100k	1/2	742A971H48
R36	499k	1/2	742A971H49
R37	1.24M	1/2	742A971H70
R38	2.49M	1/2	742A971H71
R39	750Ω	1/2	742A971H14
R40	12.1k	1/2	742A971H42
R41	---	---	---
R42	22M	1/2	742A971H72
R43	13.7k	1/2	742A971H44

Code	Ohms	Watts	Westinghouse Part No.
R44	51Ω	2	743A041H01
R45	100Ω	2	743A041H02
R46	1k	1/2	742A971H30
R47	7.5k	1/2	742A971H38
R48	100Ω	1	742A972H01
R49	10Ω	3	742A973H01
R50	400Ω	3	742A973H03
R51	10Ω	3	742A973H02
R52	1k	3	742A973H04
R53	2k	3	742A973H05
R54	50Ω	5	742A974H01
R55	150Ω	5	742A974H03
R56	300Ω	5	742A974H04
R57	400Ω	5	742A974H05
R58	500Ω	5	742A974H06
R59	700Ω	5	742A974H07
R60	180Ω	10	742A975H01
R61	25Ω	50	---
R62	20Ω	5	742A974H08
R63	1.5k	5	742A974H10
R64	4.5k	5	742A974H11
R65	100Ω	5	742A974H02
R66	250Ω	5	742A974H09
R67	150Ω	3	742A973H06
R68	500Ω	3	742A973H07
R69	---	---	---
R70	40Ω	1/4	742A970H01
R71	138Ω	1/4	742A970H02
R72	2.2k	1/4	742A970H03
R73	8.66k	1/4	742A970H04
R74	51.1k	1/10	742A960H06
R75	100k	1/10	742A969H07
R76	6.19Ω	1/2	742A971H16
R77	2.74k	1/2	742A971H50
R78	51.1k	1/2	742A971H51
R79	43.2k	1/2	742A971H52
R80	249k	1/2	742A971H53
R81	64.9k	1/2	742A971H81
R82	24.9k	1/2	742A971H82
R83	32.4k	1/2	742A971H83
R84	121k	1/2	742A971H84
R85	1.21k	1/2	742A971H85
R86	20Ω, 2PPMC°, ± .01%		651A117H03
R87	20k	1/2	742A971H54
R88	40.2k	1/2	742A971H55
R89	80.6k	1/2	742A971H56
R90	650Ω	3	742A973H10
R91	604Ω	1/2	742A971H17
R92	121Ω	1/2	742A971H18
R93	1Ω, .05%	3	742A973H11
R94	1Ω, 1.0%	3	742A973H12
R95	33Ω	3	742A973H13
R96	35Ω	3	742A973H22
R97	60Ω	3	742A973H15
R98	90Ω	3	742A973H16
R99	49.9k	1/2	742A971H19
R100	45.3k	1/2	742A971H20

Code	Ohms	Watts	Westinghouse Part No.
R101	30.1k	1/2	742A971H21
R102	42.2k	1/2	742A971H22
R103	56.2k	1/2	742A971H23
R104	511k	1/2	742A971H24
R105	2.0M	1	742A972H02
R106	4.99k	1/2	742A971H36
R107	10k	1/2	742A971H41
R108	1k	2	743A041H04
R109	1k	1/2	669A007H02
R110	10k	1/2	669A007H03
R111	12.1k	1/2	669A007H04
R112	1.5k	1/2	669A007H05
R113	30k	1/2	669A007H06
R114	47Ω	1/2	669A007H07
R115	68k	1/2	669A007H08
R116	200k	1/2	669A007H09
R117	4.7k	1/2	669A007H10
R118	15k	1/2	669A007H11
R119	100k	1/2	669A007H12
R120	5.1k	1/2	669A007H13
R121	120k	1/2	669A007H14
R122	1.0M	1/2	669A007H15
R123	240Ω	1/2	669A007H16
R124	51k	1/2	669A007H17
R125	27k	1/2	669A007H18
R126	390k	1/2	669A007H19
R127	150k	1/2	669A007H20
R128	22k	1/2	669A007H21
R129	2.1k	1/2	742A971H25
R130	2.87k	1/2	742A971H26
R131	249k	1/2	742A971H27
R132	470Ω	1/2	669A007H22
R133	200k	1/2	742A971H28
R134	1k	1/2	742A971H30
R135	1.0M	1/2	742A971H29
R136	499k	1/2	742A971H49
R137	100k	1/2	742A971H48
R138	10M	2	669A040H01
R139	24k	1/2	669A007H23
R140	62k	1/2	669A007H24
R141	1.1k	1/2	669A007H25
R142	39k	1/2	669A007H26
R143	20k	1/2	669A007H27
R144	10k	1/2	669A007H03
R145	40.2k	1/2	742A971H55
R146	20k	1/2	742A971H54
R147	4.42k	1/2	742A971H57
R148	27.4k	1/2	742A971H58
R149	300k	1/2	669A007H28
R150	12.1k	1/2	742A971H42
R151	49.9k	1/2	742A971H19
R152	2k	10	742A975H04
R153	162k	1/2	742A971H86
R154	150k	1/2	742A971H87
R155	50Ω	3	742A973H14
R156	4.02k	1/2	742A971H59
R157	8.06k	1/2	742A971H60

Code	Ohms	Watts	Westinghouse Part No.
R158	16k	1/2	669A007H30
R159	32.4k	1/2	742A971H61
R160	255k	1/2	651A114H38
R161	127k	1/2	651A114H37
R162	63.4k	1/2	651A114H35
R163	32k	5	651A116H12
R164	16k	5	651A116H11
R165	8k	5	651A116H10
R166	4k	5	651A116H09
R167	2k	5	651A116H08
R168	1k	5	651A116H07
R169	500Ω	5	651A116H04
R170	255k	1/2	651A114H38
R171	127k	1/2	651A114H37
R172	63.4k	1/2	651A114H35
R173	32k	5	651A116H12
R174	16k	5	651A116H11

1-17. ZENER DIODE VALUE CODES

Code	Volts	Westinghouse Part No.
Z1	4.3V	743A004H01
Z2	6.8V	743A005H01
Z3	8.2V	743A006H01
Z4	15V	743A007H01
Z5	16V	743A008H01
Z6	22V	743A009H01
Z7	2.7V	743A010H01
Z8	20V	743A011H01
Z9	---	---
Z10	18V	742A980H01
Z11	10V	743A002H01
Z12	5.6V	775A057H01
Z13	18V, 50W	743A087H01
Z14	1.5V	669A119H01
Z15	24V	669A089H01
Z16	16V	669A088H01
Z17	7.5V	669A302H01

P 50
LOGIC DIAGRAMS

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LIST OF DRAWINGS

LIST OF DRAWINGS (Cont)

LIST OF DRAWINGS (Cont)

LIST OF DRAWINGS (Cont)

The following notes define the majority of the symbology used with the logic diagrams. (See Figure 4-1.)

NOTE 1. Indicates a connection on this card to another point labeled with the same mnemonic. This signal originates on this card.

NOTE 2. Indicates a connection on this card to another point labeled with the same mnemonic. This signal originates off this card.

NOTE 3. Indicates the operation which takes place when this point is a logical one.

NOTE 4. Indicates the card to which the point goes or from which it comes.

NOTE 5. Indicates the connector and pin to which the point goes or from which it comes.

NOTE 6. Indicates the number of points to which this point is connected.

NOTE 7. Indicates connector and pin. (Connector A12, pin J.)

NOTE 8. Indicates twisted pair cable.

NOTE 9. Indicates the tab number on the wiring side of the board. The tabs are on the outside edge of the board, are equally spaced and labeled 1-7 starting at the bottom.

NOTE 10. Indicates the tab number on the component side of the board.

NOTE 11. Indicates to which indicator logic circuit the point is connected. A logical one at this point turns the indicator on. The indicators are on the outside edge of the board, are equally spaced and are labeled 1-6 starting at the bottom.

NOTE 12. Indicates the connector and pin on this board.

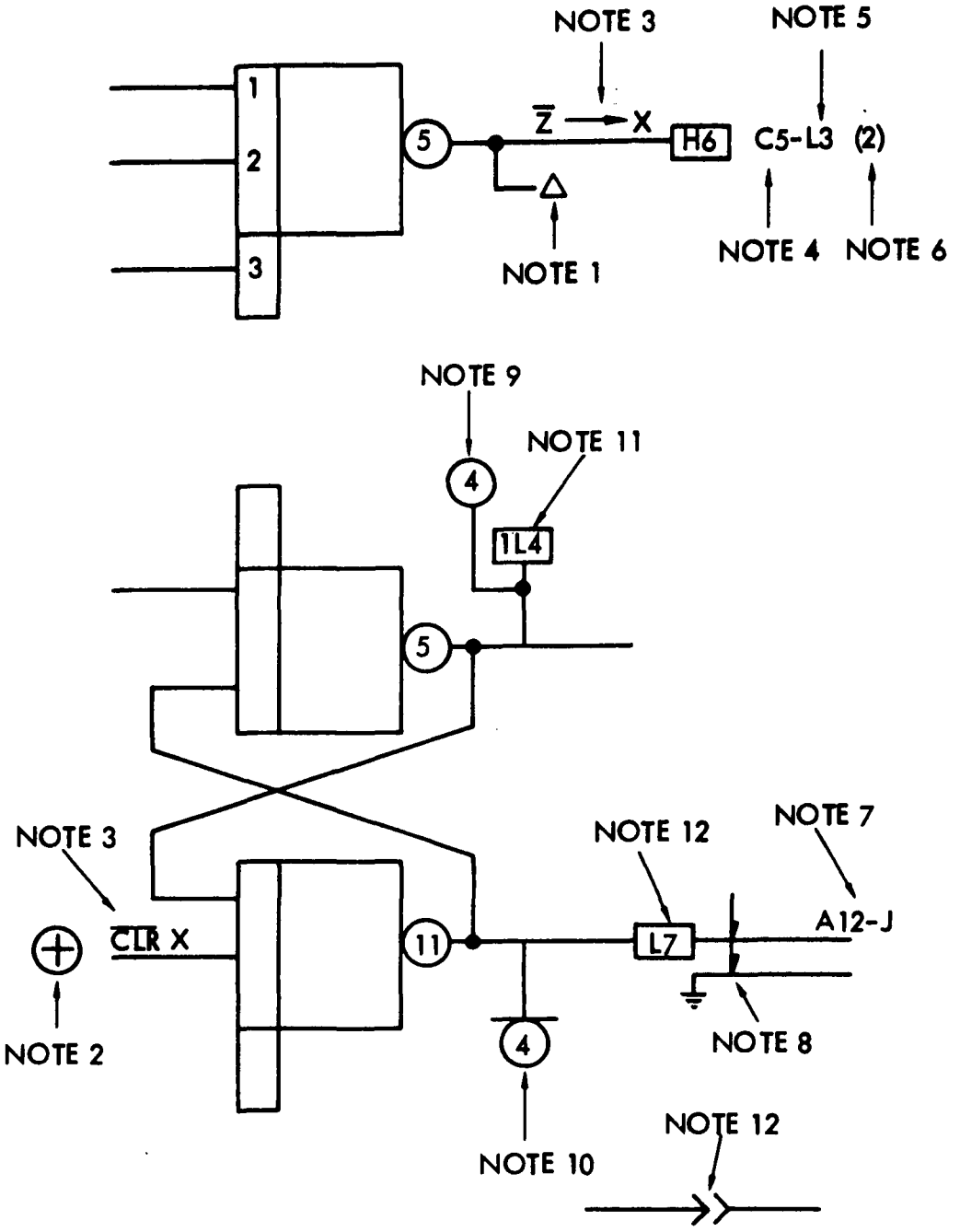
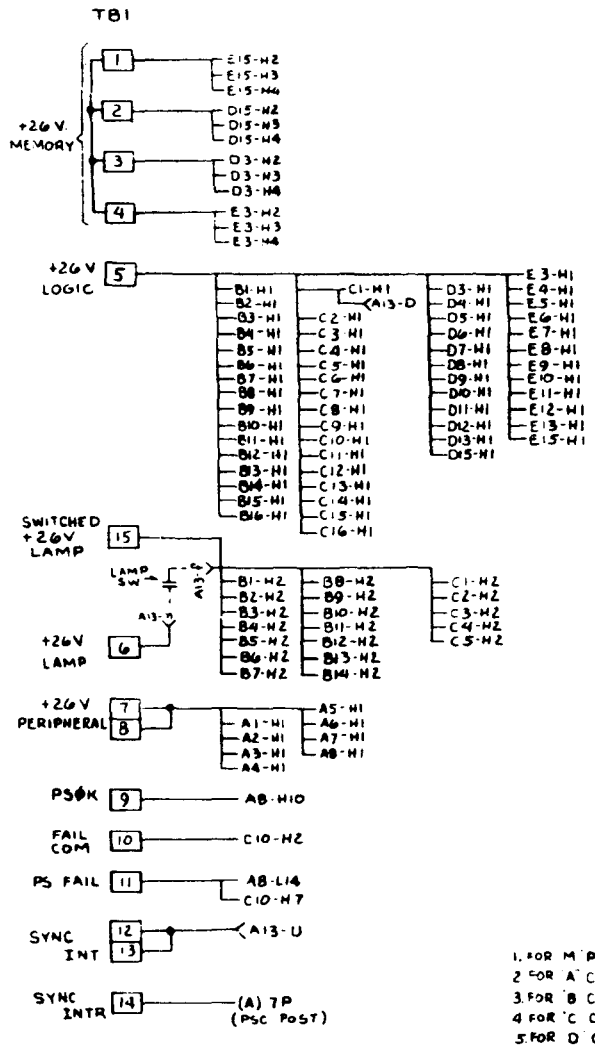

NOTE 3
NOTE 5
1
2
3
5
Z → X
H6
C5-L3 (2)
NOTE 1
NOTE 4
NOTE 6
NOTE 9
NOTE 11
4
1L4
5
NOTE 3
NOTE 12
NOTE 7
CLR X
11
L7
A12-J
NOTE 2
4
NOTE 8
NOTE 10
NOTE 12

Figure 4-1.

M PANEL LOGIC DIAGRAMS

CAGE	SLOT LOCATION	CARD TYPE	REMARKS	LOGIC DIAG DWG. NO.
A	01	2PD		867C218
	02	1PU		867C219
	03	2TM7	CHANNEL 40	
	04		CHANNEL 41	
	05		CHANNEL 42	
	06		CHANNEL 43	
	07		CHANNEL 44	
	08	IAR		867C220
B	01	2DC	BIT 00	867C221
	02	2DC	BIT 01	867C222
	03	2DC	BIT 02	867C223
	04	2DC	BIT 03	867C224
	05	2DC	BIT 04	867C225
	06	2DC	BIT 05	867C226
	07	2DC	BIT 06	867C227
	08	2DC	BIT 07	867C228
	09	2DC	BIT 08	867C229
	10	2DC	BIT 09	867C230
	11	2DC	BIT 10	867C231
	12	2DC	BIT 11	867C232
	13	2DC	BIT 12	867C233
	14	2DC	BIT 13	867C234
	15	2ST		867C235
	16	IAR		867C236
C	01	3TC		867C237
	02	2DC		867C238
	03	1SC		867C239
	04	2EM		867C240
	05	2TC		867C241
	06	2ME		867C242
	07	2HS	X-EVEN	867C243
	08	2HS	X-ODD	867C244
	09	2HS	Y-EVEN	867C245
	10	2HS	Y-ODD	867C246
	11	1EP		867C247
	12	1EP		867C248
	13	3EI	INT 00-17	867C249
	14	3EI	INT 20-37	867C250
	15	3EI	INT 40-57	867C251
	16	3EI	INT 60-77	867C252
D	01	2MB		867C253
	03	3IP	STACK 0	867C254
	04	2MA		867C255
	05	1SA2		867C256
	06	2CP	BIT 0-3	867C257
	07	2CP	BIT 4-7	867C258
	08	2CP	BIT 8-13	867C259
	09	2CP	BIT 8-13	867C260
	10	2CP	BIT 4-7	867C261
	11	2CP	BIT 0-3	867C262
	12	1SA3	STACK 1	867C263
	13	2MB		867C264
	15	3EP		867C265
	16	2MA		867C266
E	01	2MB		867C267
	03	3IP	STACK 2	867C268
	04	2MA		867C269
	05	1SA2		867C270
	06	2CP	BIT 0-3	867C271
	07	2CP	BIT 4-7	867C272
	08	2CP	BIT 8-13	867C273
	09	2CP	BIT 8-13	867C274
	10	2CP	BIT 4-7	867C275
	11	2CP	BIT 0-3	867C276
	12	1SA3	STACK 3	867C277
	13	2MB		867C278
	15	3EP		867C279
	16	2MA		867C280

ASR IN 2'N



1. FOR M PANEL WIRE LIST REF. 743A474
2. FOR A CAGE BUS WIRING REF. 867C141
3. FOR B CAGE BUS WIRING REF. 867C142
4. FOR C CAGE BUS WIRING REF. 867C143
5. FOR D CAGE BUS WIRING REF. 867C144
6. FOR E CAGE BUS WIRING REF. 867C145
7. FOR CONNECTOR (A10 - A16) BREAKDOWN REF. 775A325

CHANGE

NEXT ASSY | REF DWG

DO NOT SCALE DWG. BREAK ALL SHARP EDGES .005 MAXIMUM DIMENSIONS ± ½"

OVER 24	± .06	± .015
6 IN. to 24	± .04	± .010
UP TO 6 IN.	± .02	± .005
BASIC DIM.	2 PLACE DEC	3 PLACE DEC

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

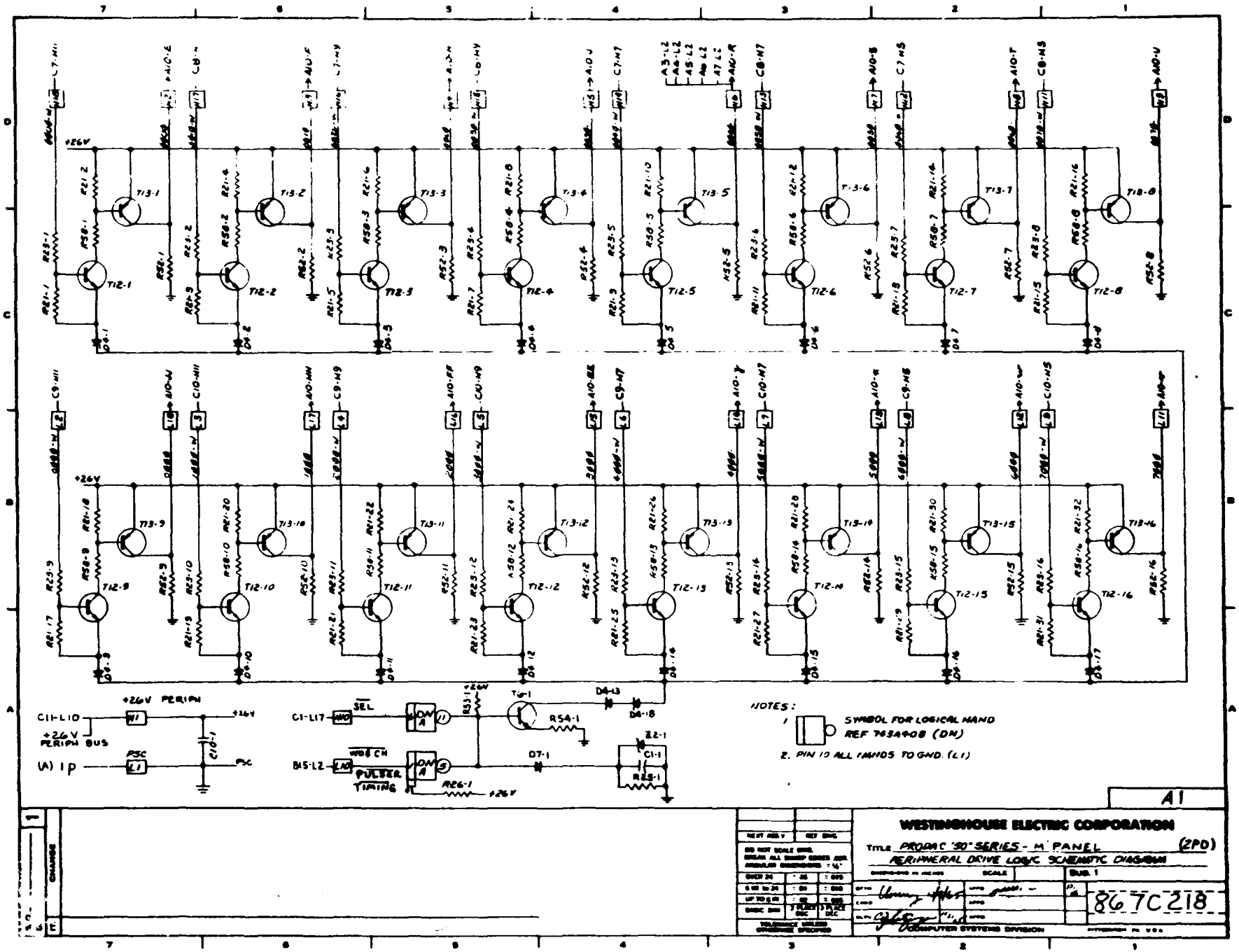
PRODAC 50 SERIES -M PANEL

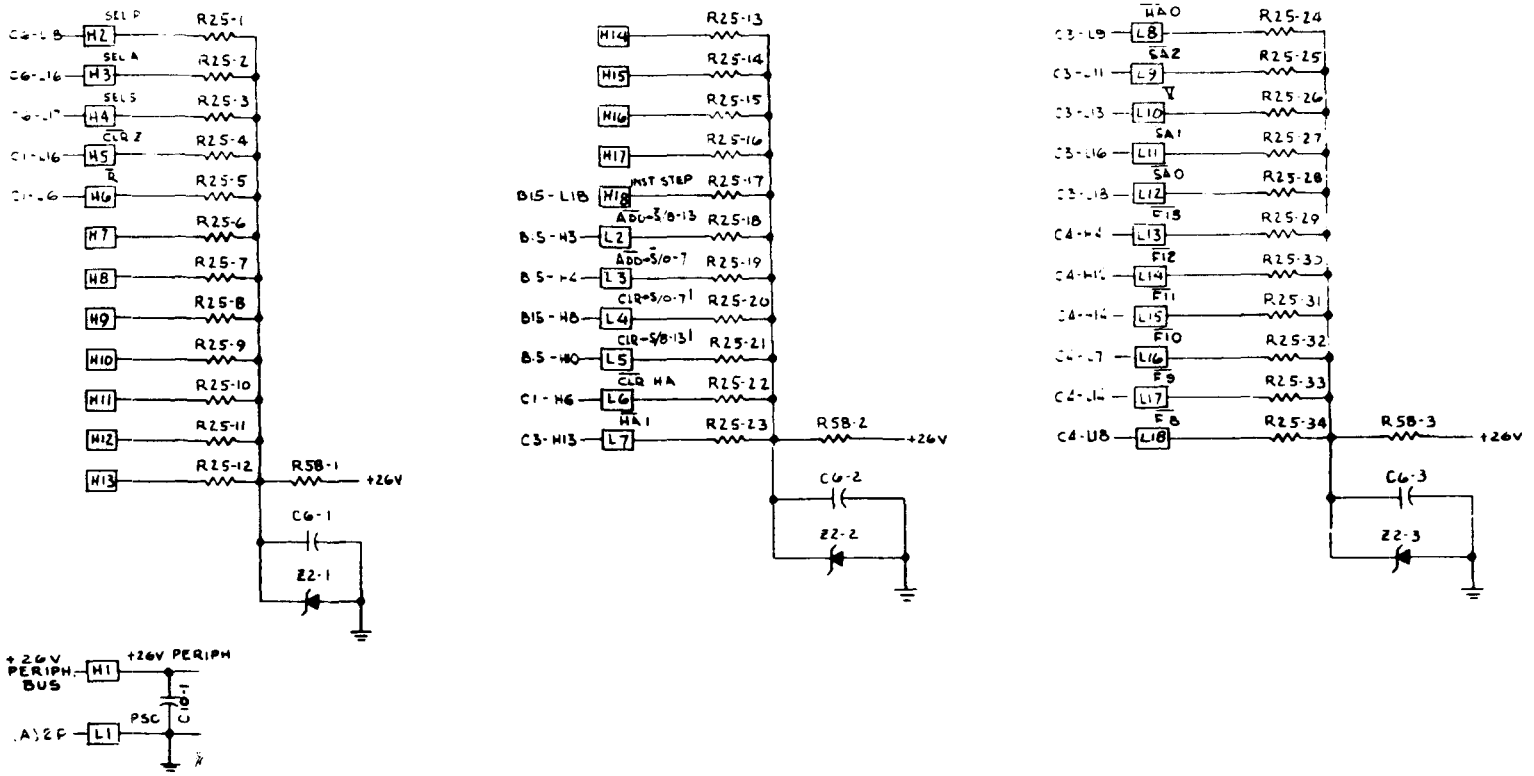
TITLE CARD LISTING & TERM BLOCK ASSIGNMENT

SIZE D | SUB 1

867C217

COMPUTER SYSTEMS DIVISION


+26V
+26V PERIPH
+26V PERIPH BUS
(A) 1p
PSC
SEL
WDB CH
PULSER TIMING
NOTES:
1. SYMBOL FOR LOGICAL NAND REF 7834408 (DN)
2. PIN 10 ALL NANDS TO GND. (L1)
A1
WESTINGHOUSE ELECTRIC CORPORATION
Title PRODAC '50' SERIES - M PANEL (ZPD)
PERIPHERAL DRIVE LOGIC SCHEMATIC DIAGRAM
COMPUTER SYSTEMS DIVISION
86 7C 218



A2

NEXT ASS'Y	REF DWG		
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020 ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN to 24	± .04	± .010	
UP TO 6 IN	± .02	± .005	
BASIC DIM	2 PLACE DEC	3 PLACE DEC	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

PRODAC 50 SERIES-M PANEL (1PU)

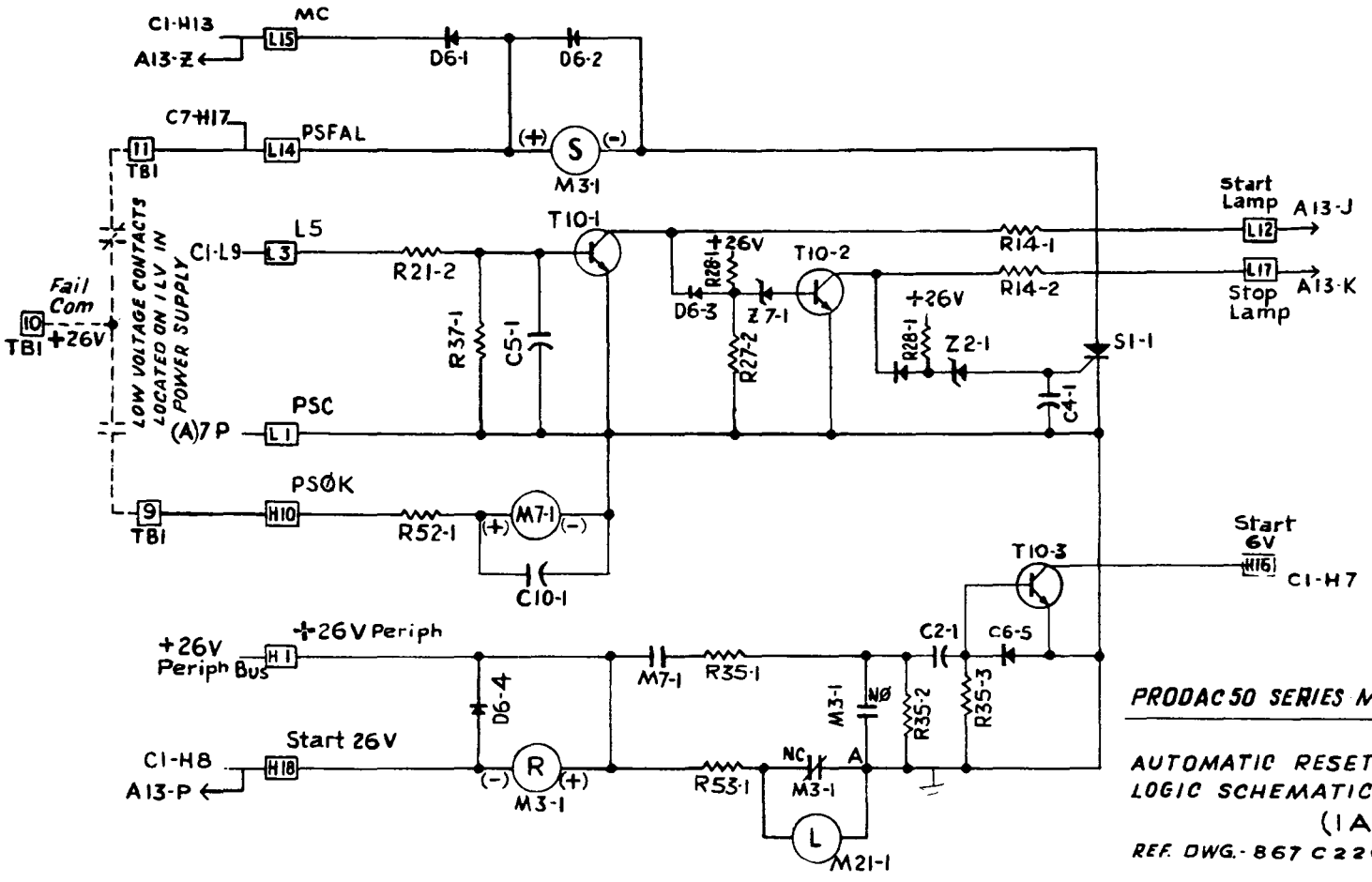
TITLE PULL-UP RESISTOR LOGIC SCHEMATIC DIAGRAM

SCALE | SUB 1

DRWN | APPD | CHKD | APPD | DSGN | APPD

867C219

COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.

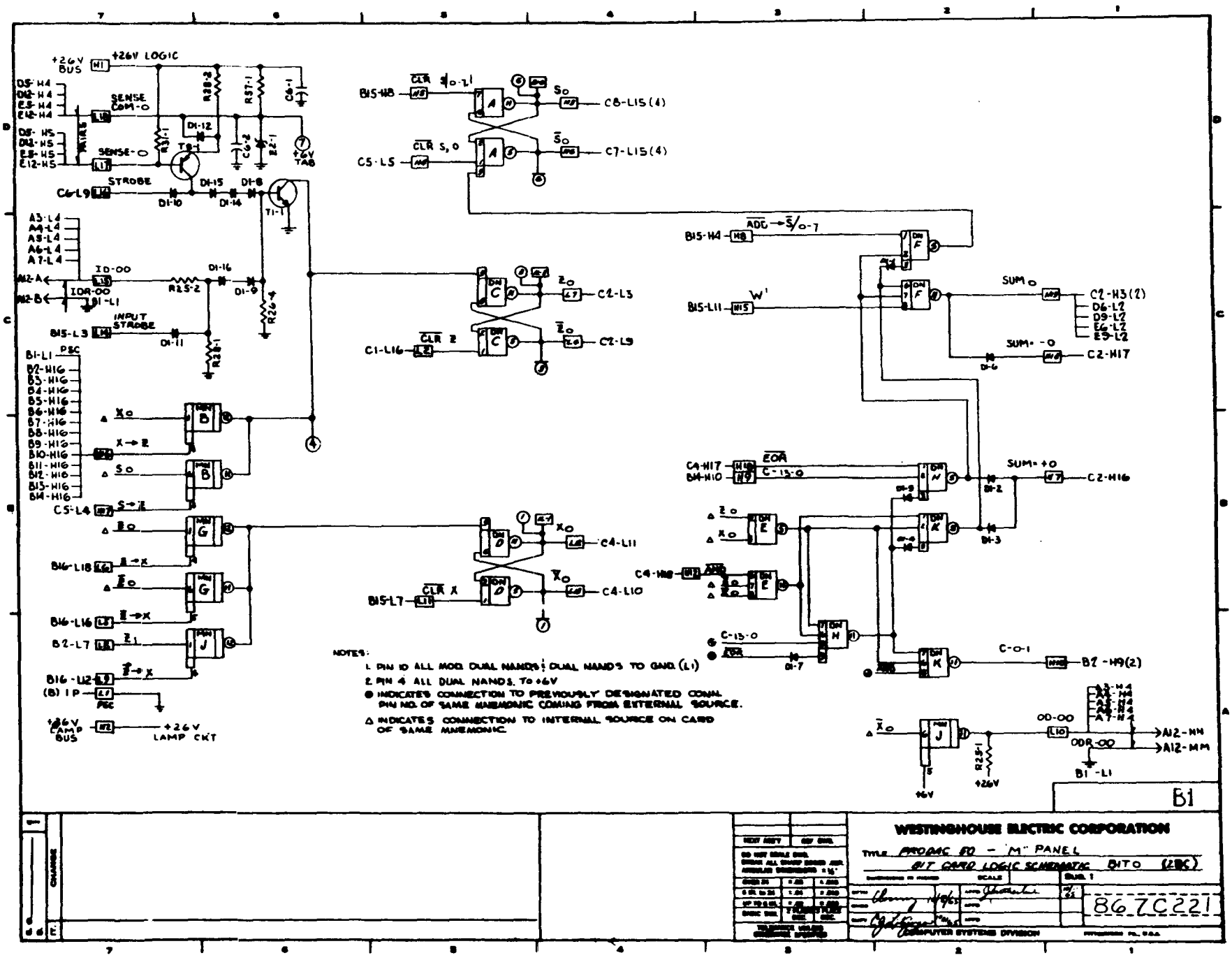


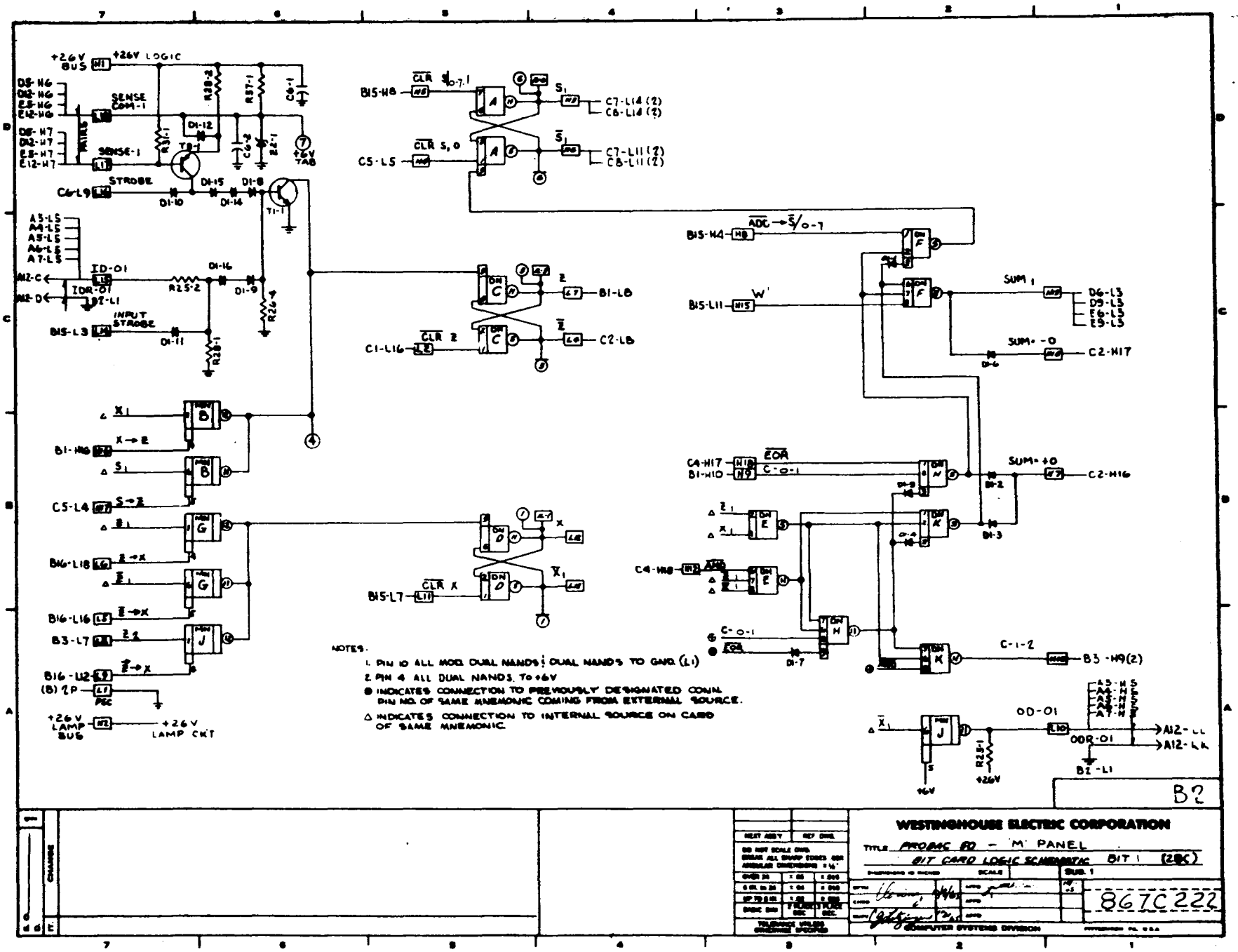
PRODAC 50 SERIES M PANEL

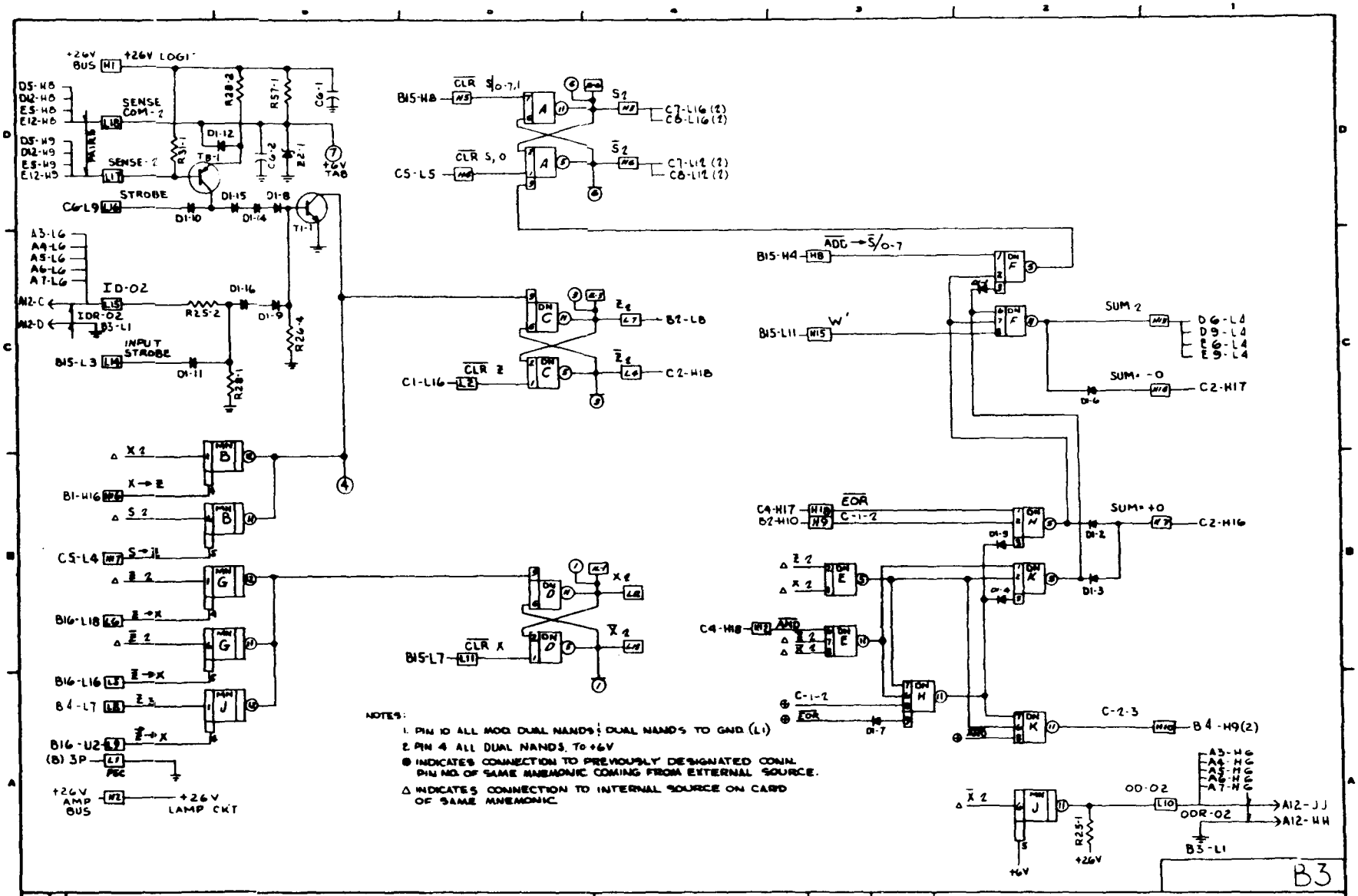
AUTOMATIC RESET LOGIC SCHEMATIC

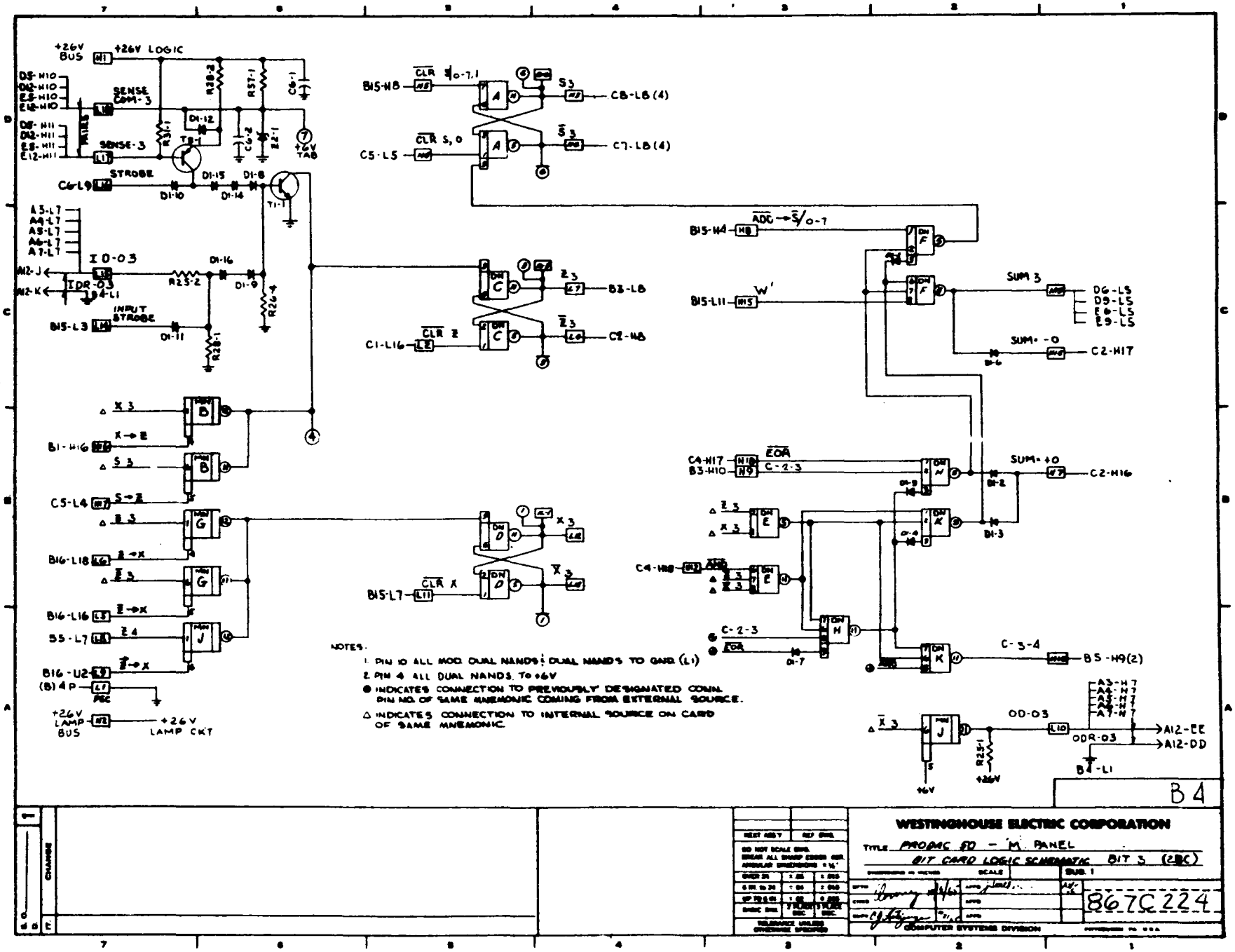
(1AR)-A8

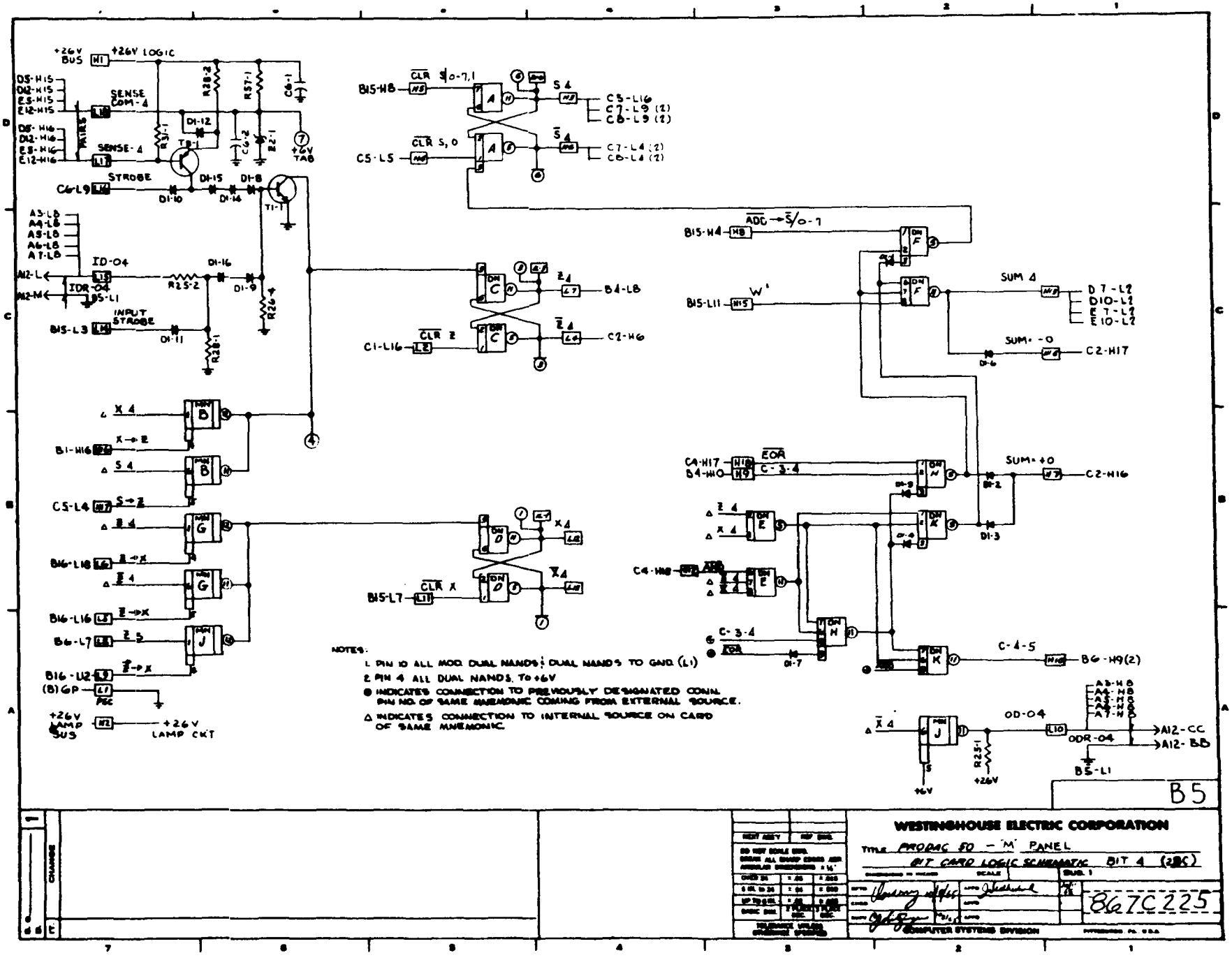
REF. DWG.- 867 C 220

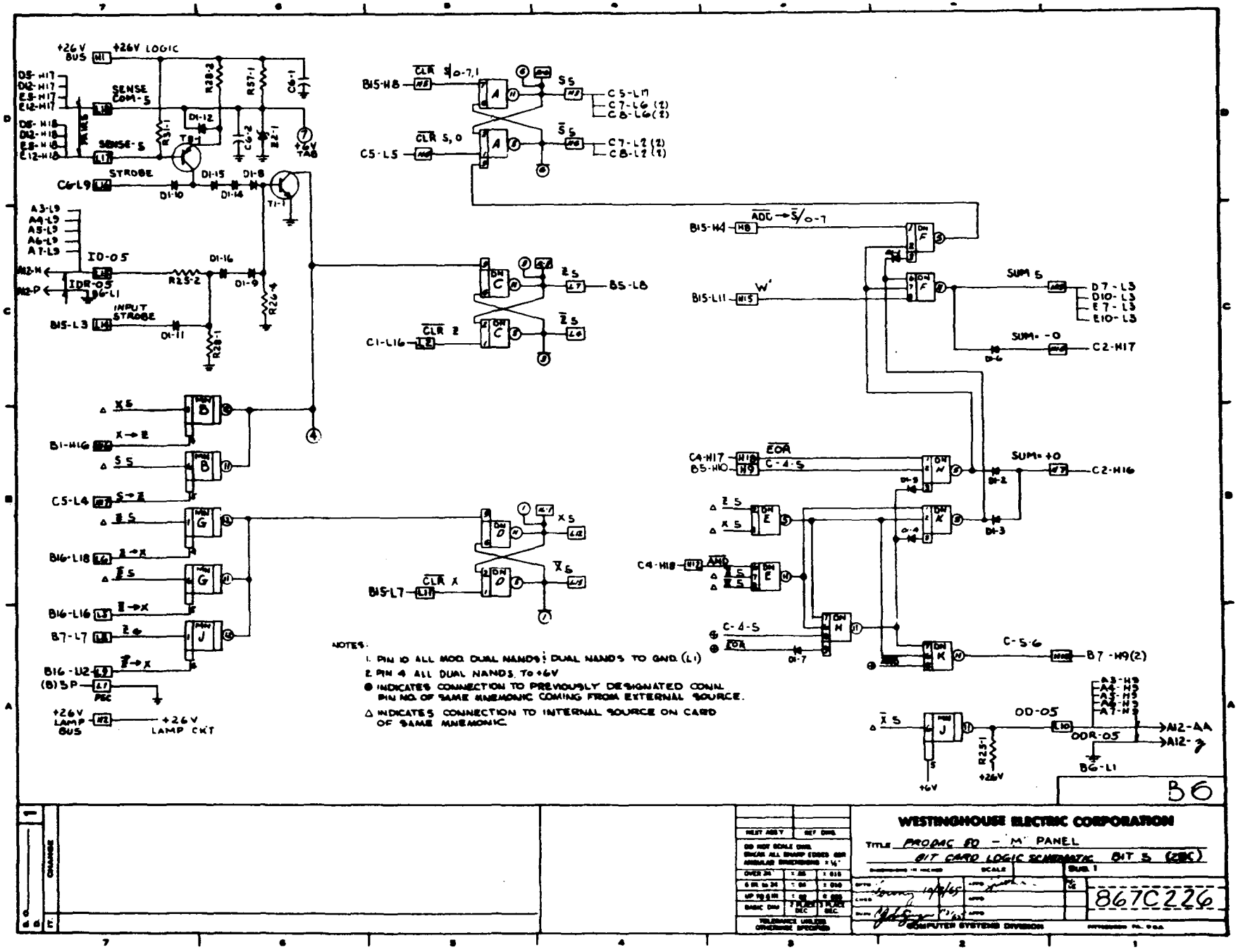

+26V BUS
+26V LOGIC
SENSE COM-0
SENSE-0
STROBE
INPUT STROBE
IDR-00
ID-00
PSC
NOTES:
1. PIN 10 ALL MOD DUAL NANDS & DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC.
+26V LAMP BUS
+26V LAMP CKT
WESTINGHOUSE ELECTRIC CORPORATION
PROAC 60 - M" PANEL
BIT CARD LOGIC SCHEMATIC BIT 0 (LSB)
COMPUTER SYSTEMS DIVISION
867C221
B1


+26V BUS
+26V LOGIC
SENSE COM-1
SENSE-1
STROBE
INPUT STROBE
+26V LAMP BUS
+26V LAMP CKT
CLR S0-7-1
CLR S, 0
CLR Z
CLR X
ADC → S0-7
W'
EOR
C-0-1
C-1-2
SUM-1
SUM-0
SUM-+0
ODR-01
NOTES.
1. PIN 10 ALL MOD. DUAL NANDS; DUAL NAND'S TO GND. (L)
2. PIN 4 ALL DUAL NANDS. To +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC.
B2
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PROBAC 80 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 1 (28K)
867C222
COMPUTER SYSTEMS DIVISION


+26V BUS
+26V LOGIC
SENSE COM-2
SENSE-2
STROBE
INPUT STROBE
ID-02
IDR-02
B5-L1
INPUT STROBE
+26V AMP BUS
+26V LAMP CKT
CLR S0-7,1
CLR S,0
ADD → S0-7
W'
SUM 2
SUM +0
SUM -0
EOR
AND
CLR Z
CLR X
X → Z
Z → X
NOTES:
1. PIN 10 ALL MOD DUAL NANDS; DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS. TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
OD-02
ODR-02
B3-L1
B3
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 2 (2BC)
COMPUTER SYSTEMS DIVISION
867C223


+26V BUS
+26V LOGIC
SENSE COM-3
SENSE-3
STROBE
INPUT STROBE
IO-03
IDR-03
R23-2
R26-4
R26-1
R38-2
R37-1
C6-1
C6-2
Z2-1
T1-1
D1-12
D1-15
D1-8
D1-10
D1-14
D1-16
D1-9
D1-11
+6V TAB
B15-H8
CLR S0-7,1
S3
C8-L8 (4)
C5-L5
CLR S,0
S3
C7-L8 (4)
B15-H4
ADD → S0-7
B15-L11
W'
SUM 3
D6-L5
D9-L5
E6-L5
E9-L5
SUM - 0
C2-H17
C1-L16
CLR Z
Z3
B3-L8
C2-H8
X 3
X→Z
S 3
S→Z
B 3
B→X
Z 3
Z→X
Z 4
Z→X
B1-H16
C5-L4
B16-L18
B16-L16
B5-L7
B16-U2
(B) 4 P
+26V LAMP BUS
+26 V LAMP CKT
CLR X
X3
B15-L7
C4-H17
B3-H10
EQR
C-2-3
SUM - 0
C2-H16
C-3-4
B5-H9(2)
OD-03
ODR-03
A3-H7
A4-H7
A5-H7
A6-H7
A7-H7
A12-EE
A12-DD
B7-L1
R29-1
+26V
+6V
B4
NOTES:
1. PIN 10 ALL MOD. DUAL NANDS ; DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PROMIC 80 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 5 (2BC)
SUB. 1
867C224
COMPUTER SYSTEMS DIVISION


+26V BUS
+26V LOGIC
SENSE COM-4
SENSE-4
STROBE
INPUT STROBE
ID-04
IDR-04
BS-L1
CLR S0-7,1
CLR S,0
CLR Σ
CLR X
ADD → S0-7
W'
EOR
C-3-4
SUM 4
SUM-0
SUM-+0
C-4-5
OD-04
ODR-04
+26V LAMP SUS
+26V LAMP CKT
NOTES:
1. PIN 10 ALL MOD. DUAL NANDS; DUAL NANDS TO GND. (L1)
2. PIN 4 ALL DUAL NANDS. TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
B5
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 - 'M' PANEL
BIT CARD LOGIC SCHEMATIC BIT 4 (2BS)
8677C225
COMPUTER SYSTEMS DIVISION



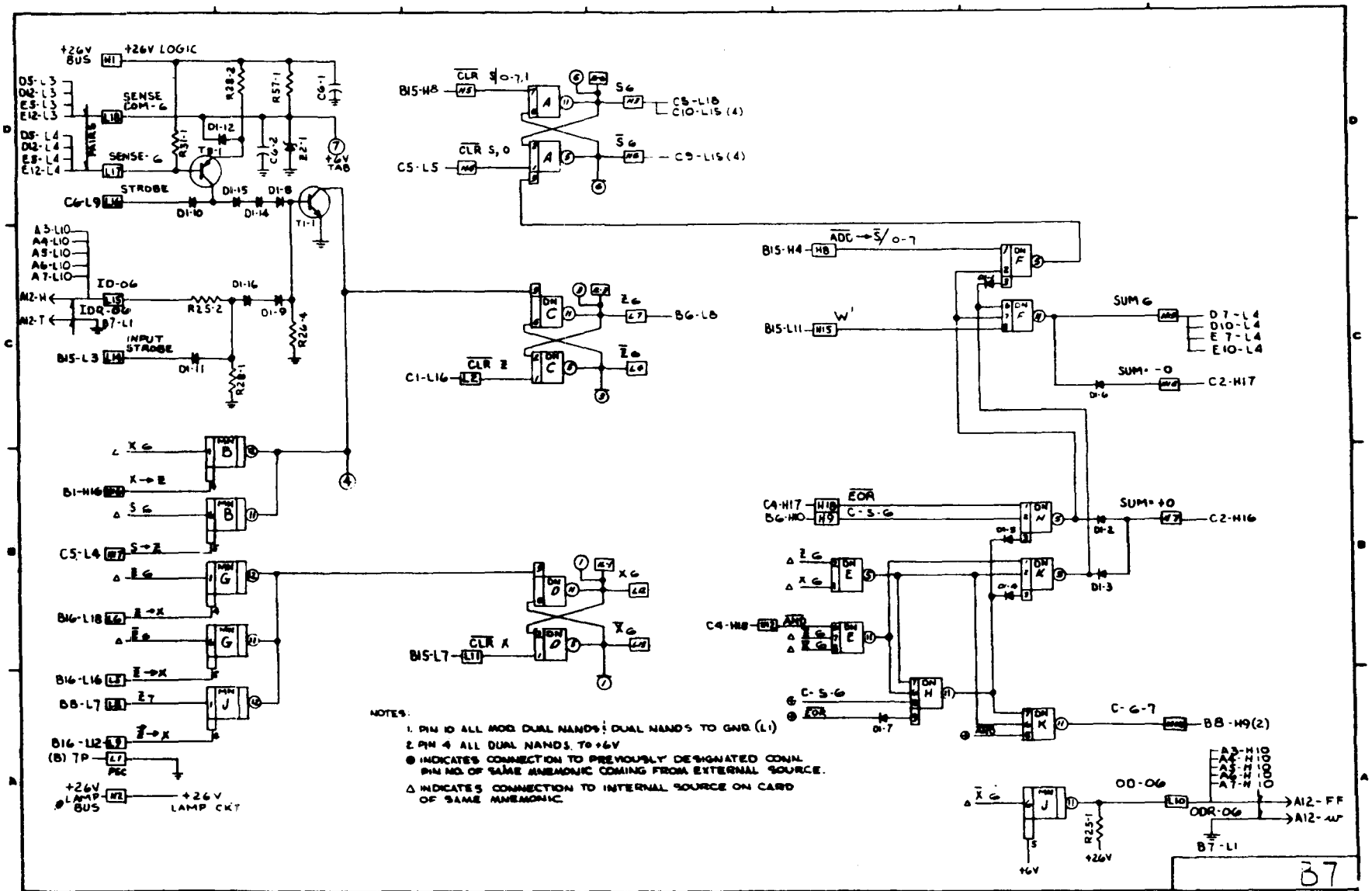
B6

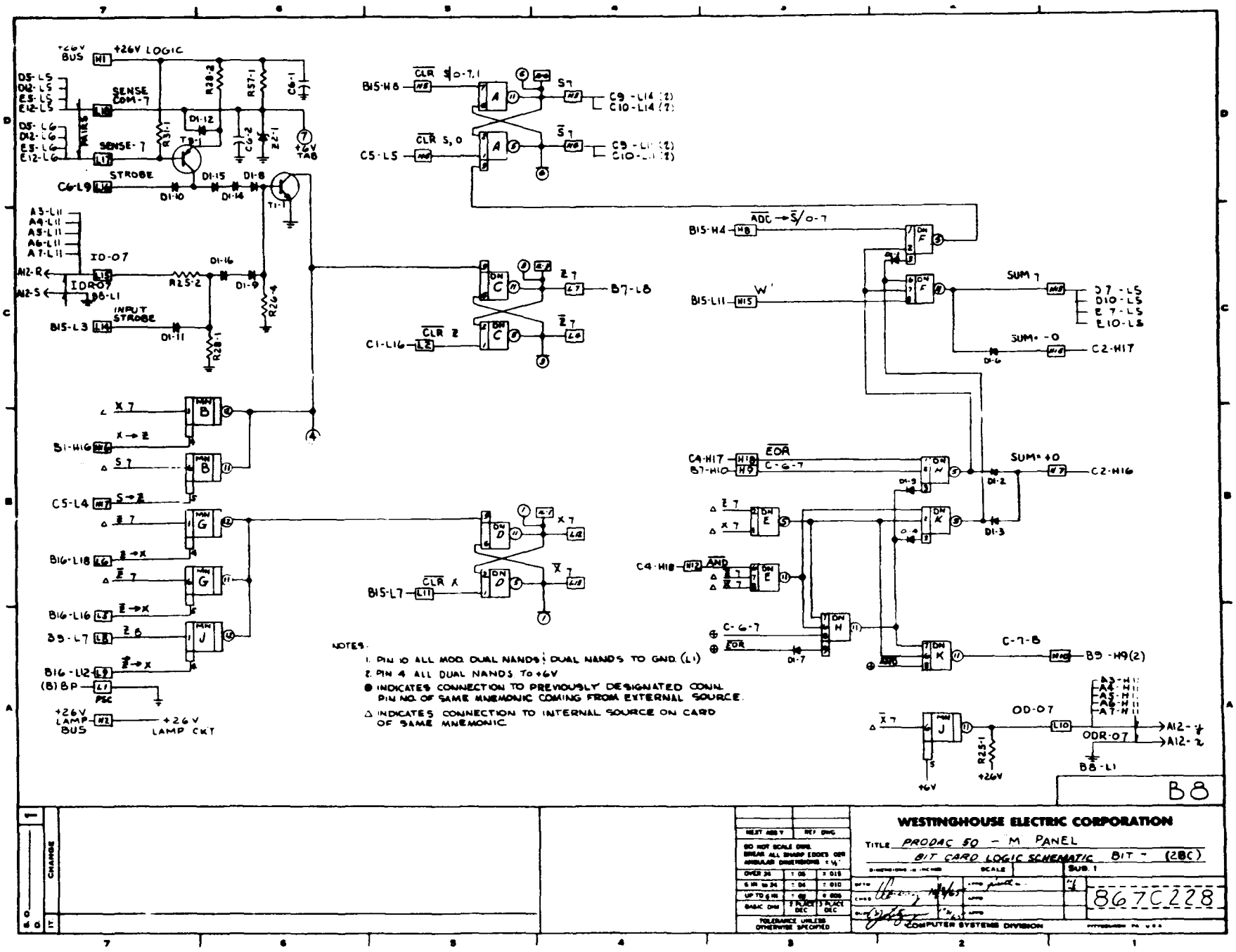
WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 80 - 'M' PANEL
BIT CARD LOGIC SCHEMATIC BIT 5 (28K)

867C226

COMPUTER SYSTEMS DIVISION


+26V BUS
+26V LOGIC
SENSE COM-G
SENSE-G
STROBE
INPUT STROBE
IDR-06
ID-06
CLR S 0-7,1
CLR S,0
CLR Z
CLR X
ADC → S 0-7
W'
EOR
SUM G
SUM -0
SUM +0
C-S-G
C-G-7
00-06
ODR-06
+26V LAMP BUS
+26V LAMP CKT
(B) TP
PSC
NOTES:
1. PIN 10 ALL MOD. DUAL NANDS; DUAL NANDS TO GND. (L1)
2. PIN 4 ALL DUAL NANDS, TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC.
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 6 (2BC)
SCALE
SHT 1
867C227
COMPUTER SYSTEMS DIVISION



WESTINGHOUSE ELECTRIC CORPORATION

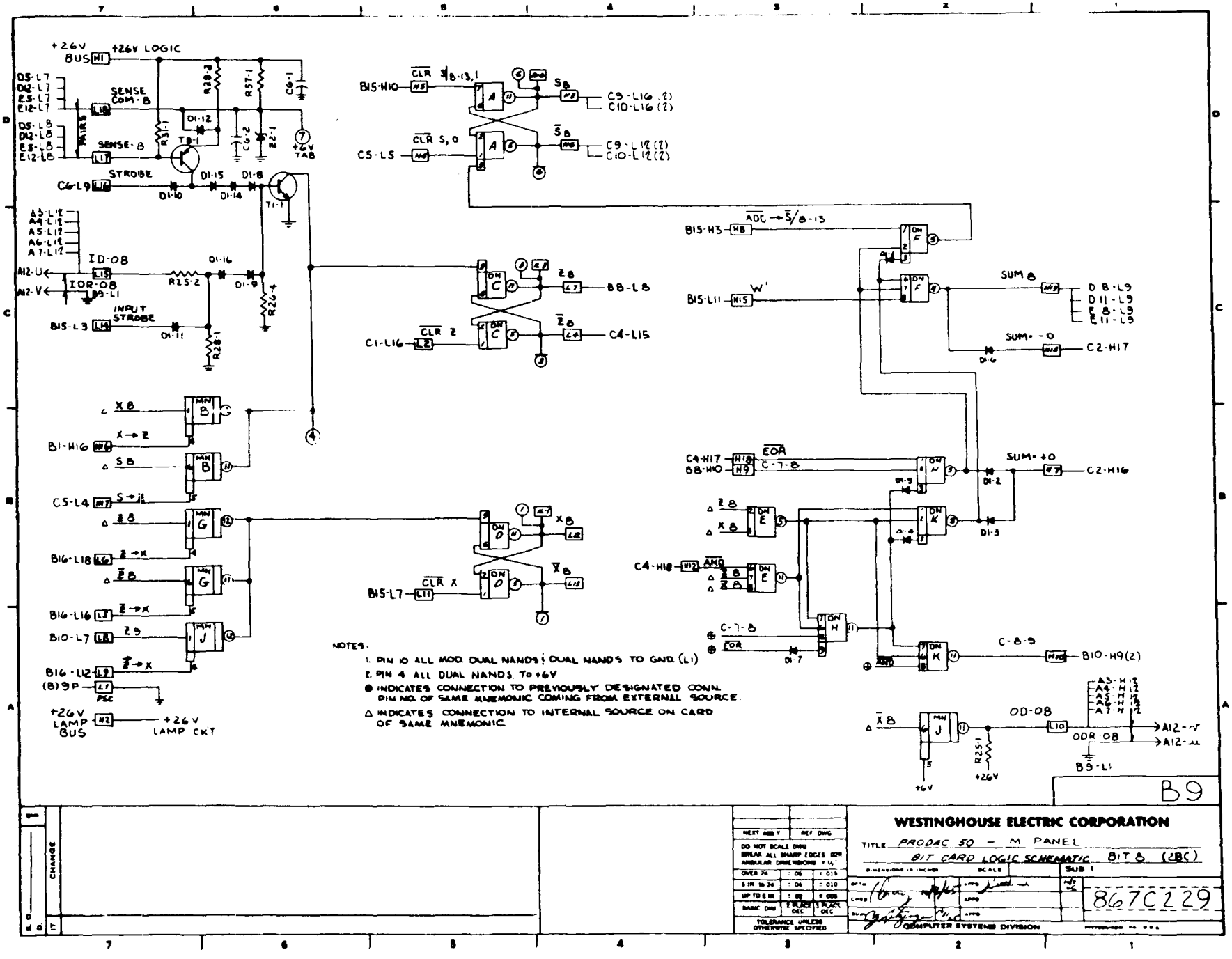
TITLE PRODAC 50 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT - (2BC)

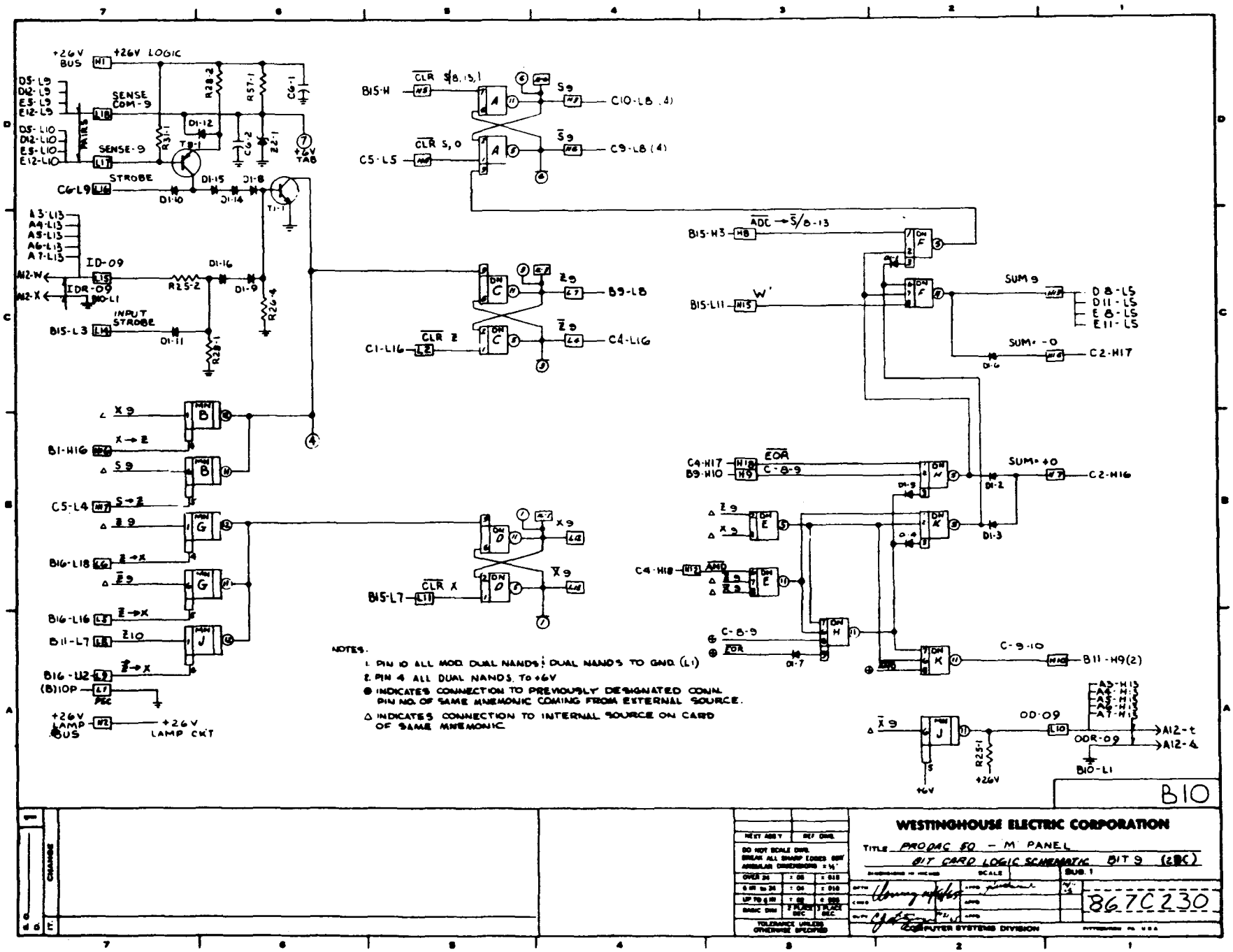
SCALE

SUB. 1

867C228

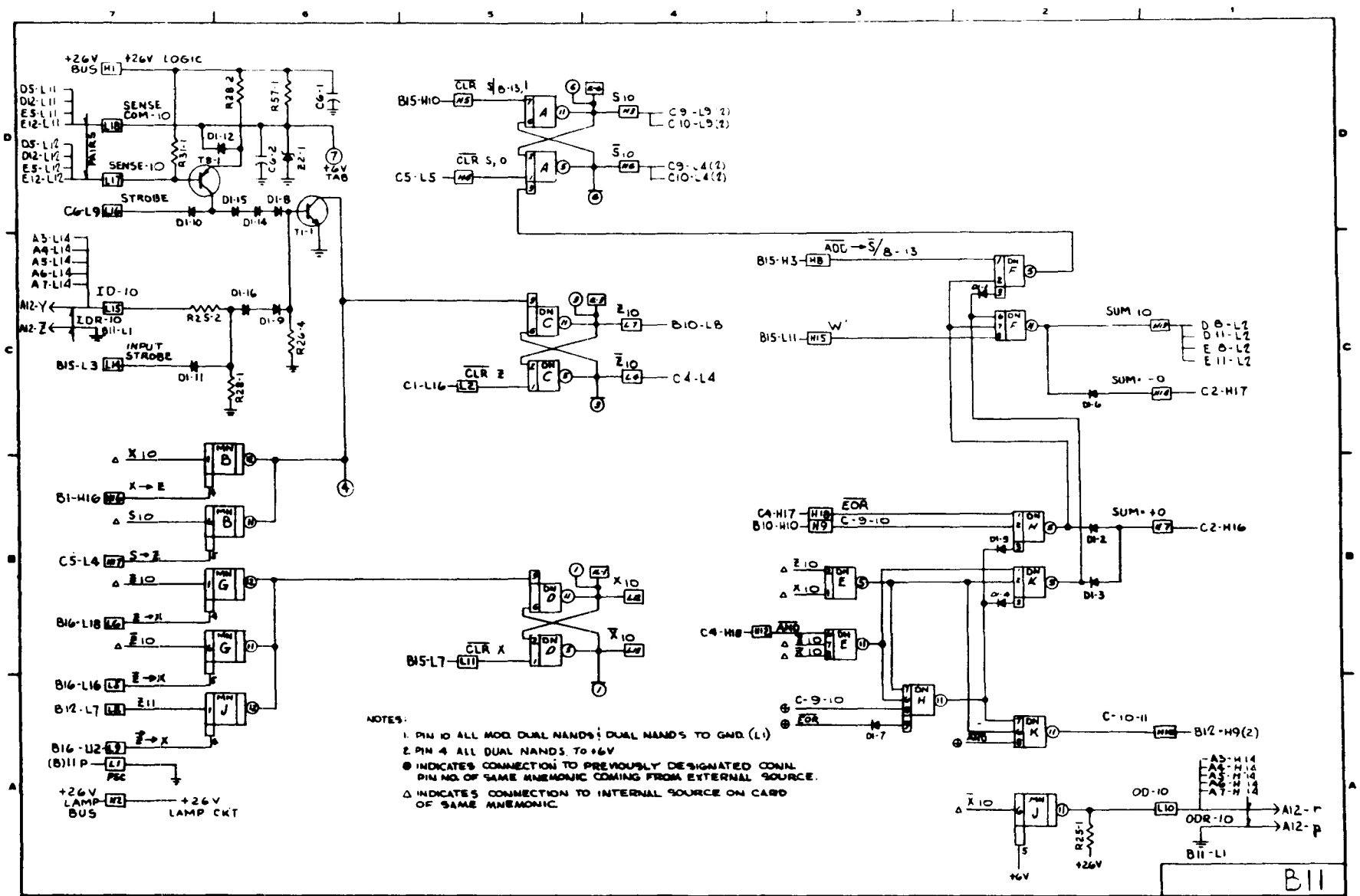
COMPUTER SYSTEMS DIVISION

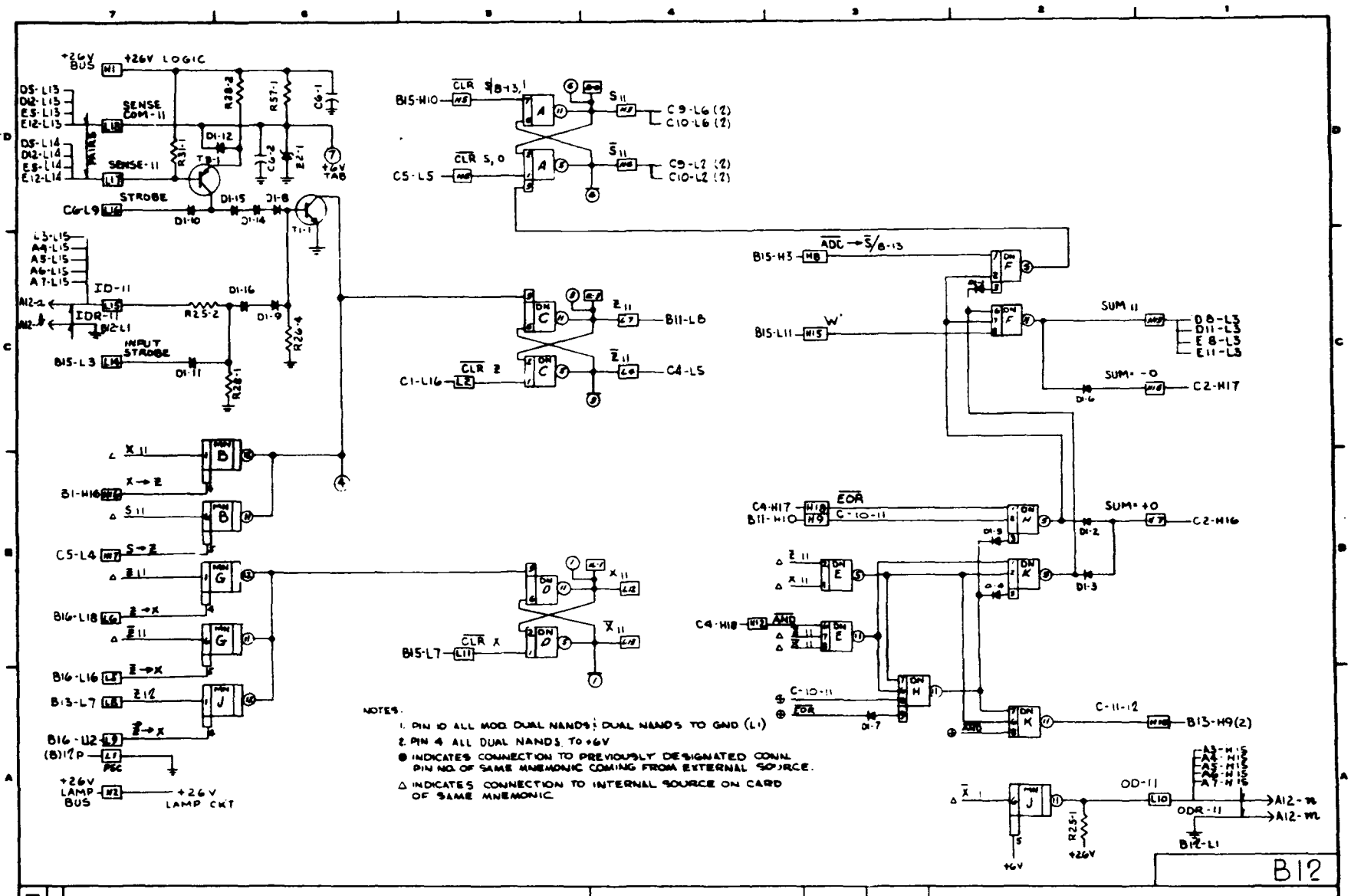

+26V BUS
+26V LOGIC
SENSE COM-B
SENSE-B
STROBE
ID-OB
IOR-OB
INPUT STROBE
+26V LAMP BUS
+26V LAMP CKT
PSC
CLR S B-13,1
CLR S, 0
CLR Z
CLR X
ADC → S/B-13
W'
EOR
AND
SUM B
SUM - 0
SUM - +0
OD-OB
ODR OB
+6V
+26V
NOTES.
1. PIN 10 ALL MOD. DUAL NANDS ; DUAL NANDS TO GND. (L1)
2. PIN 4 ALL DUAL NANDS TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
B9
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 8 (2BC)
SUB 1
867C129
COMPUTER SYSTEMS DIVISION

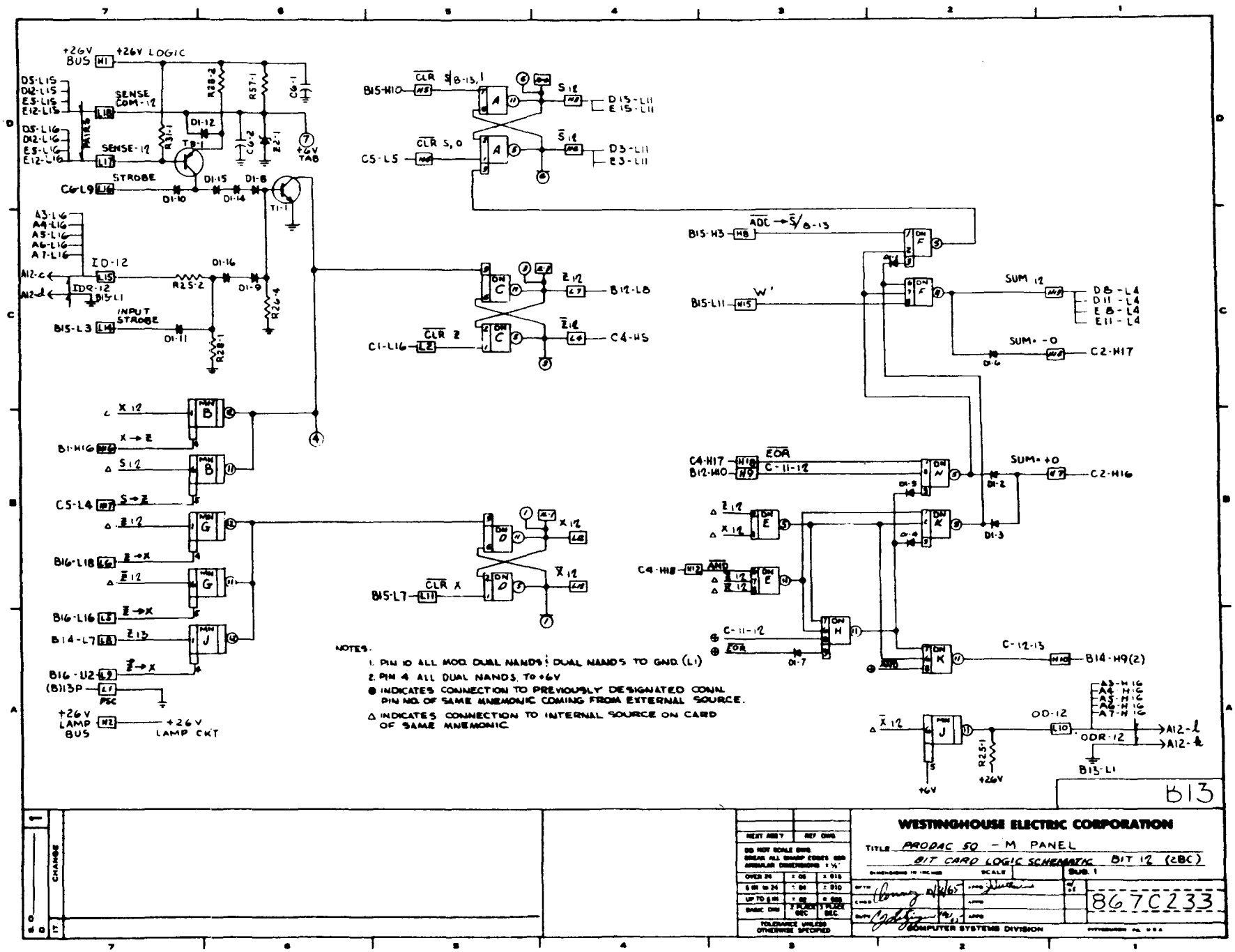


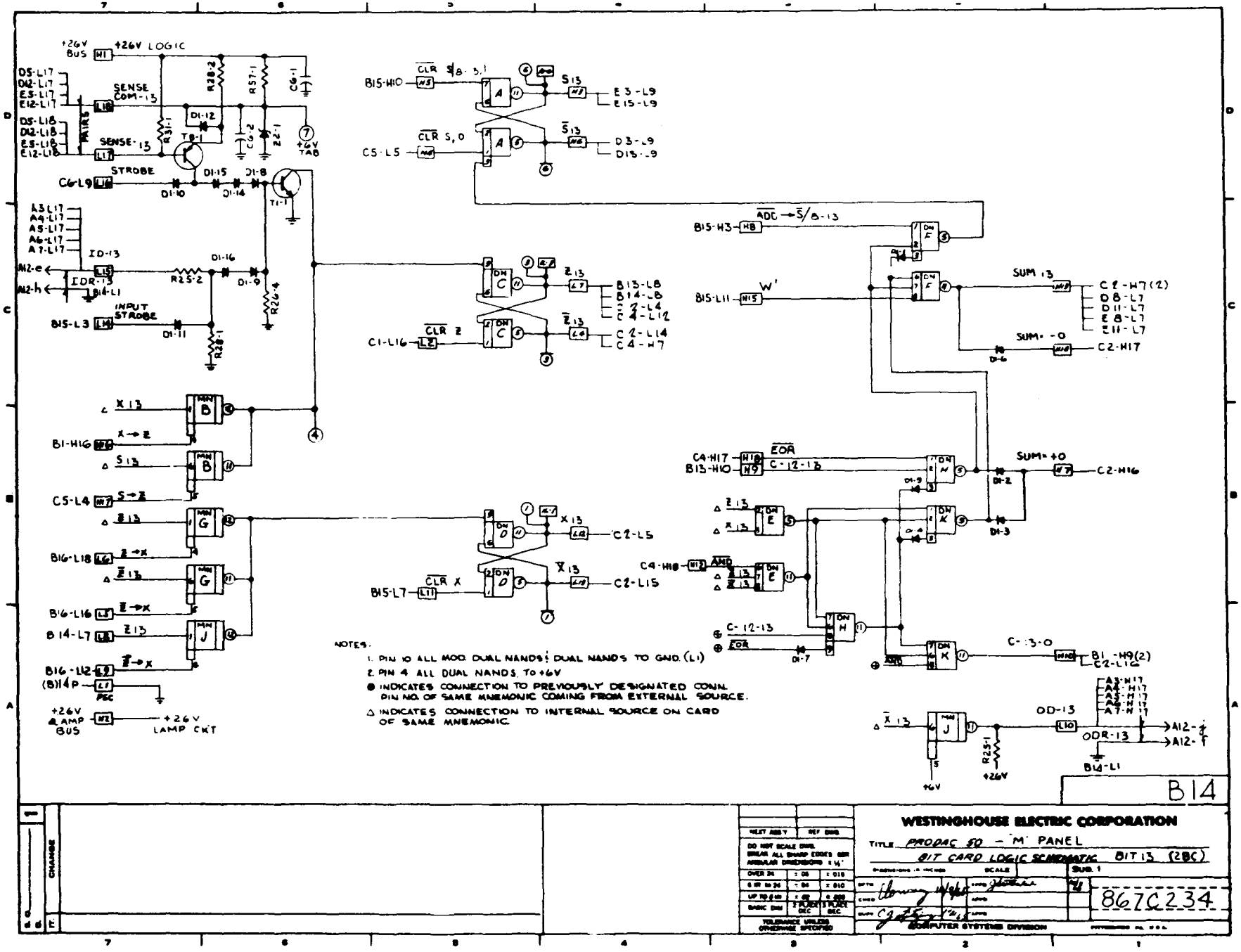
NOTES.

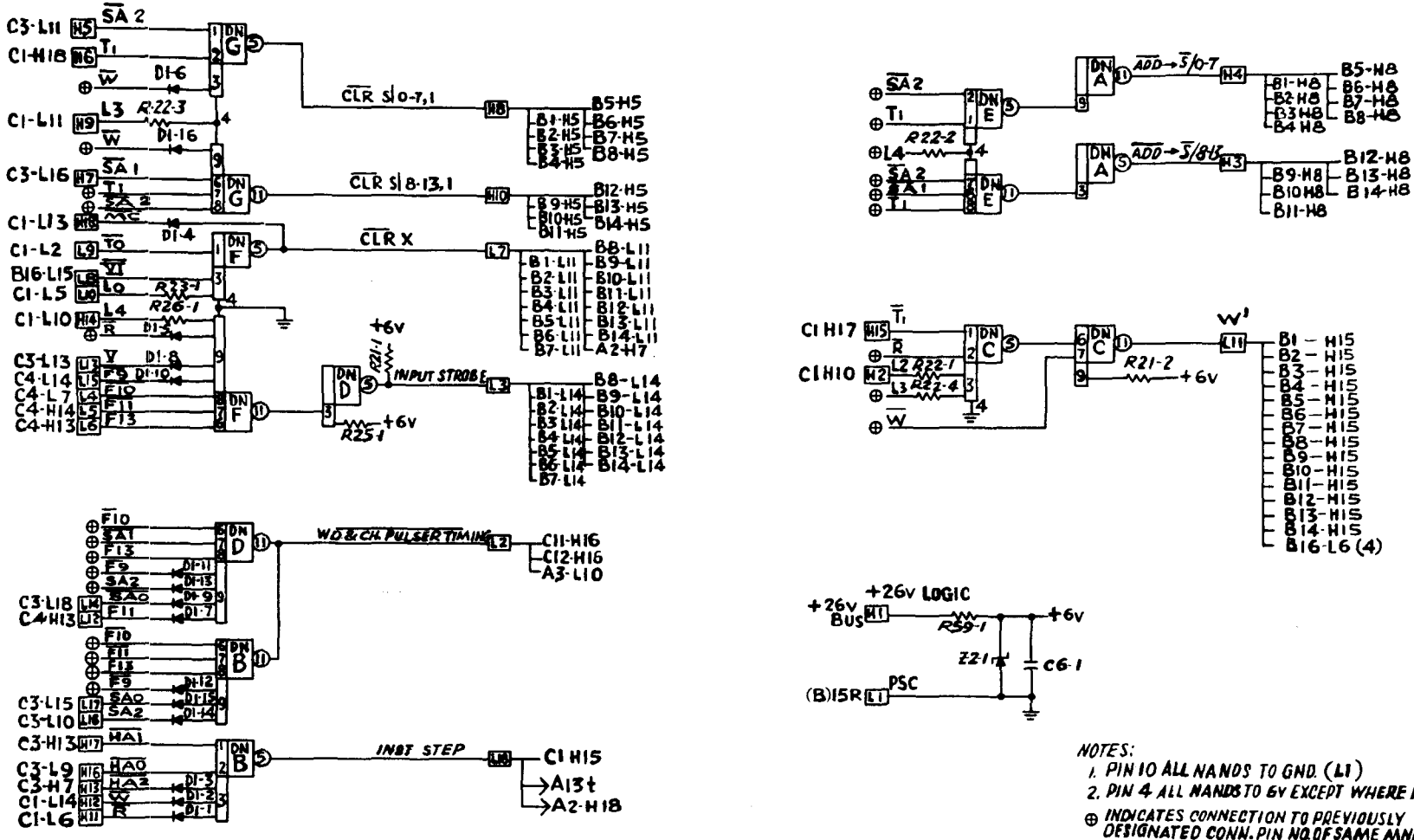
1. PIN 10 ALL MOD DUAL NANDS ; DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS, TO +6V
- ● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
- △ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC


+26V BUS
+26V LOGIC
SENSE COM-10
SENSE-10
STROBE
INPUT STROBE
ID-10
IDR-10
+6V TAB
CLR S, 0
CLR Z
CLR X
ADD → S/ B-13
W'
EOR
AND
SUM-10
SUM-0
SUM+0
OD-10
ODR-10
+26V LAMP BUS
+26V LAMP CKT
NOTES:
1. PIN 10 ALL MOD DUAL NANDS ; DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
B11
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - "M" PANEL
BIT CARD LOGIC SCHEMATIC BIT 10 (2BC)
SUB. 1
867C231
COMPUTER SYSTEMS DIVISION


+26V BUS
+26V LOGIC
SENSE COM-11
SENSE-11
STROBE
INPUT STROBE
ID-11
IDR-11
+26V LAMP BUS
+26V LAMP CKT
NOTES.
1. PIN 10 ALL MOD DUAL NANDS; DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
SUM 11
SUM +0
SUM -0
OD-11
ODR-11
B12
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 11 (2BC)
SCALE
SUB. 1
867C232
COMPUTER SYSTEMS DIVISION


+26V BUS
+26V LOGIC
SENSE COM-12
SENSE-12
STROBE
INPUT STROBE
ID-12
IDR-12
+26V LAMP BUS
+26V LAMP CKT
CLR S, 0
CLR Z
CLR X
ADC → S/B-13
W'
SUM 12
SUM= -0
SUM= +0
EOR
C-11-12
C-12-13
OD-12
ODR-12
NOTES:
1. PIN 10 ALL MOD. DUAL NANDS; DUAL NANDS TO GND. (L1)
2. PIN 4 ALL DUAL NANDS, TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
B13
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - M PANEL
BIT CARD LOGIC SCHEMATIC BIT 12 (2BC)
COMPUTER SYSTEMS DIVISION
867C233


+26V BUS
+26V LOGIC
SENSE COM-13
SENSE-13
STROBE
INPUT STROBE
IDR-13
ID-13
TB-1
TI-1
R28-2
R57-1
R23-2
R26-4
R28-1
C6-1
C6-2
Z2-1
D1-12
D1-15
D1-8
D1-10
D1-14
D1-16
D1-9
D1-11
+6V TAB
CLR S, 0
CLR Z
CLR X
ADD → S/B-13
W'
SUM-13
SUM-0
SUM+0
EOR
AND
C-12-13
C-13-0
OD-13
ODR-13
+26V LAMP BUS
+26V LAMP CKT
PSC
NOTES:
1. PIN 10 ALL MOD. DUAL NANDS; DUAL NANDS TO GND. (L1)
2. PIN 4 ALL DUAL NANDS, TO +6V
● INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC
B14
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 - 'M' PANEL
BIT CARD LOGIC SCHEMATIC BIT 13 (2BC)
COMPUTER SYSTEMS DIVISION
8671C234



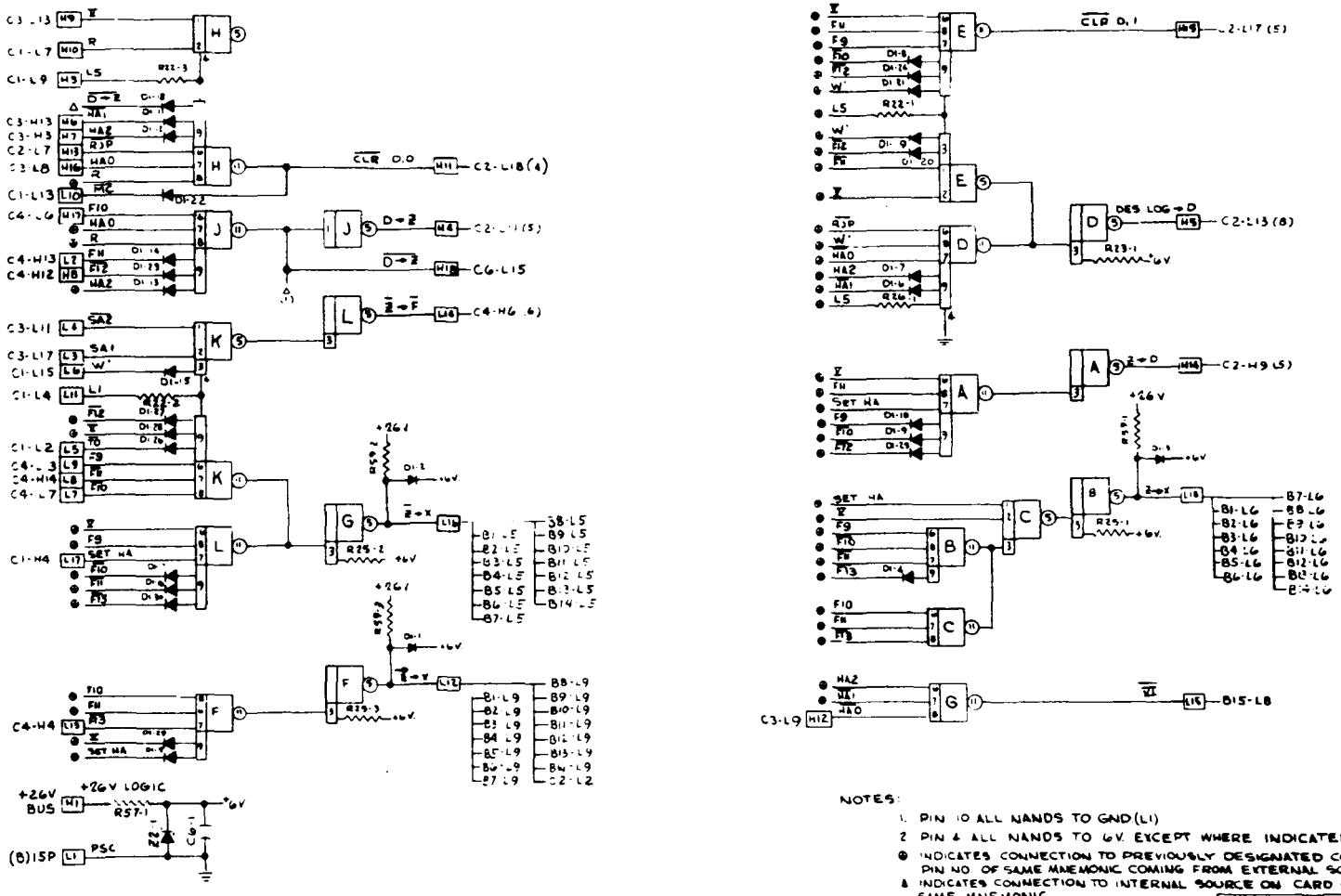
NOTES:

1. PIN 10 ALL NANDS TO GND. (L1)
2. PIN 4 ALL NANDS TO 6V EXCEPT WHERE INDICATED.

⊕ INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC, COMING FROM AN EXTERNAL SOURCE.

△ INDICATES CONNECTION TO AN INTERNAL SOURCE ON CARD OF SAME MNEMONIC.

PRODAC "50" SERIES M PANEL
"S" REG. DATA TRANSFER LOGIC SCHEMATIC
Reference Dwg. —867 C 235 --- B-15



B16

WESTINGHOUSE ELECTRIC CORPORATION

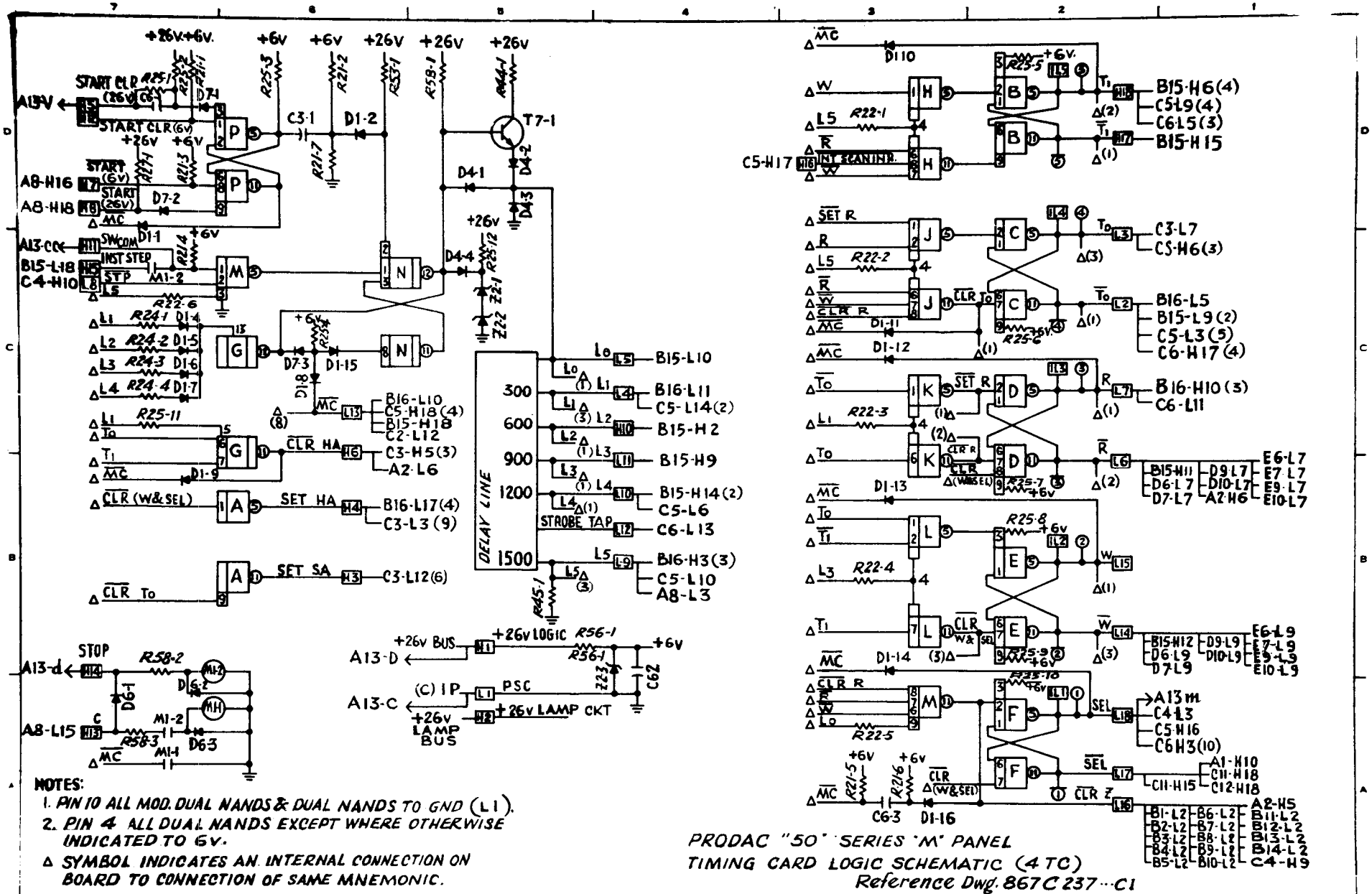
TITLE PRODAC 50 SERIES

Z → X DATA TRANSFER LOGIC SCHEMATIC (12V)

SUB. 1

867C236

COMPUTER SYSTEMS DIVISION

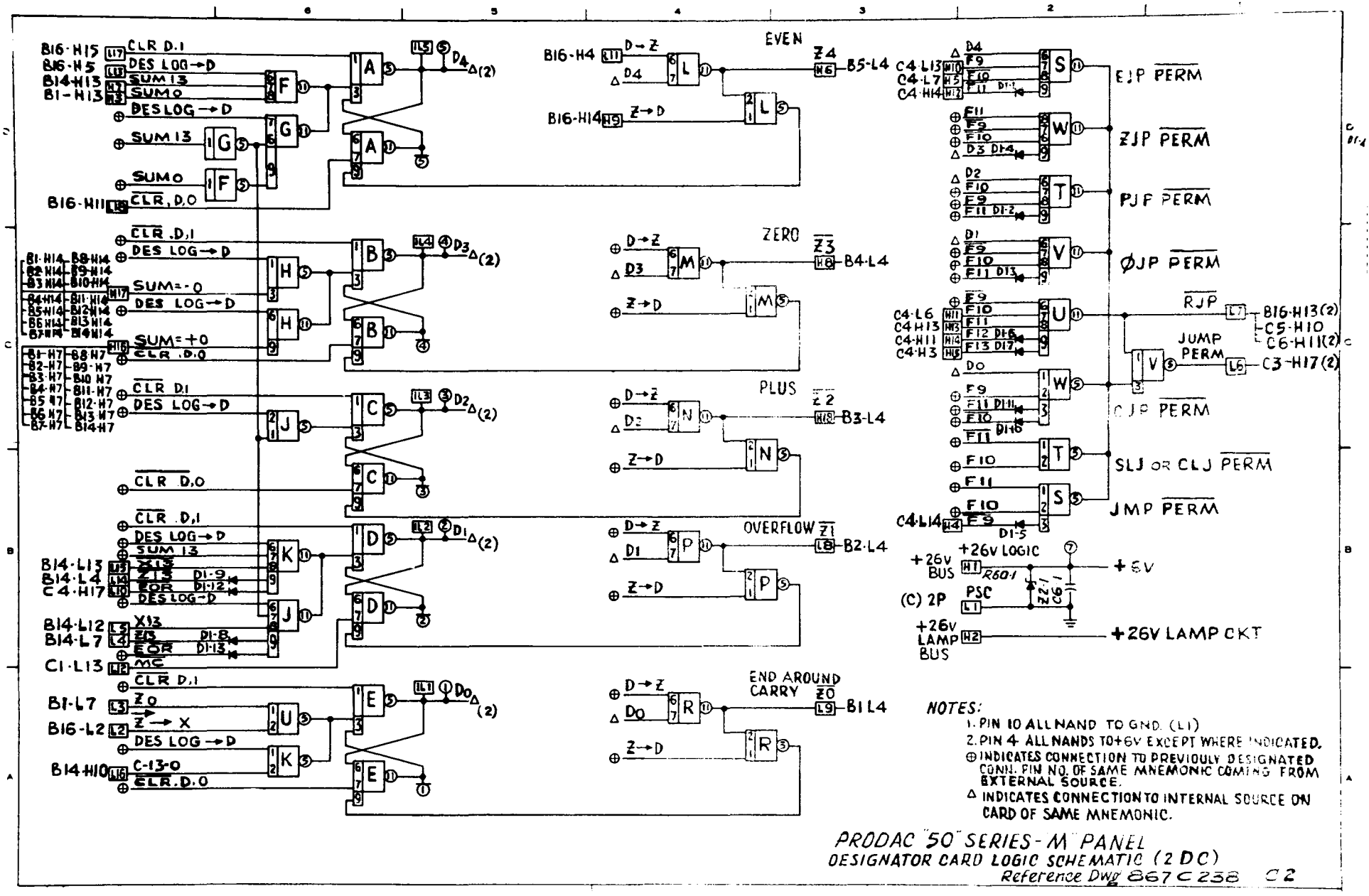


NOTES:

1. PIN 10 ALL MOD. DUAL NANDS & DUAL NANDS TO GND (L1).
2. PIN 4 ALL DUAL NANDS EXCEPT WHERE OTHERWISE INDICATED TO 6V.

△ SYMBOL INDICATES AN INTERNAL CONNECTION ON BOARD TO CONNECTION OF SAME MNEMONIC.

PRODAC "50" SERIES "M" PANEL
TIMING CARD LOGIC SCHEMATIC (4TC)
Reference Dwg. 867C237-C1



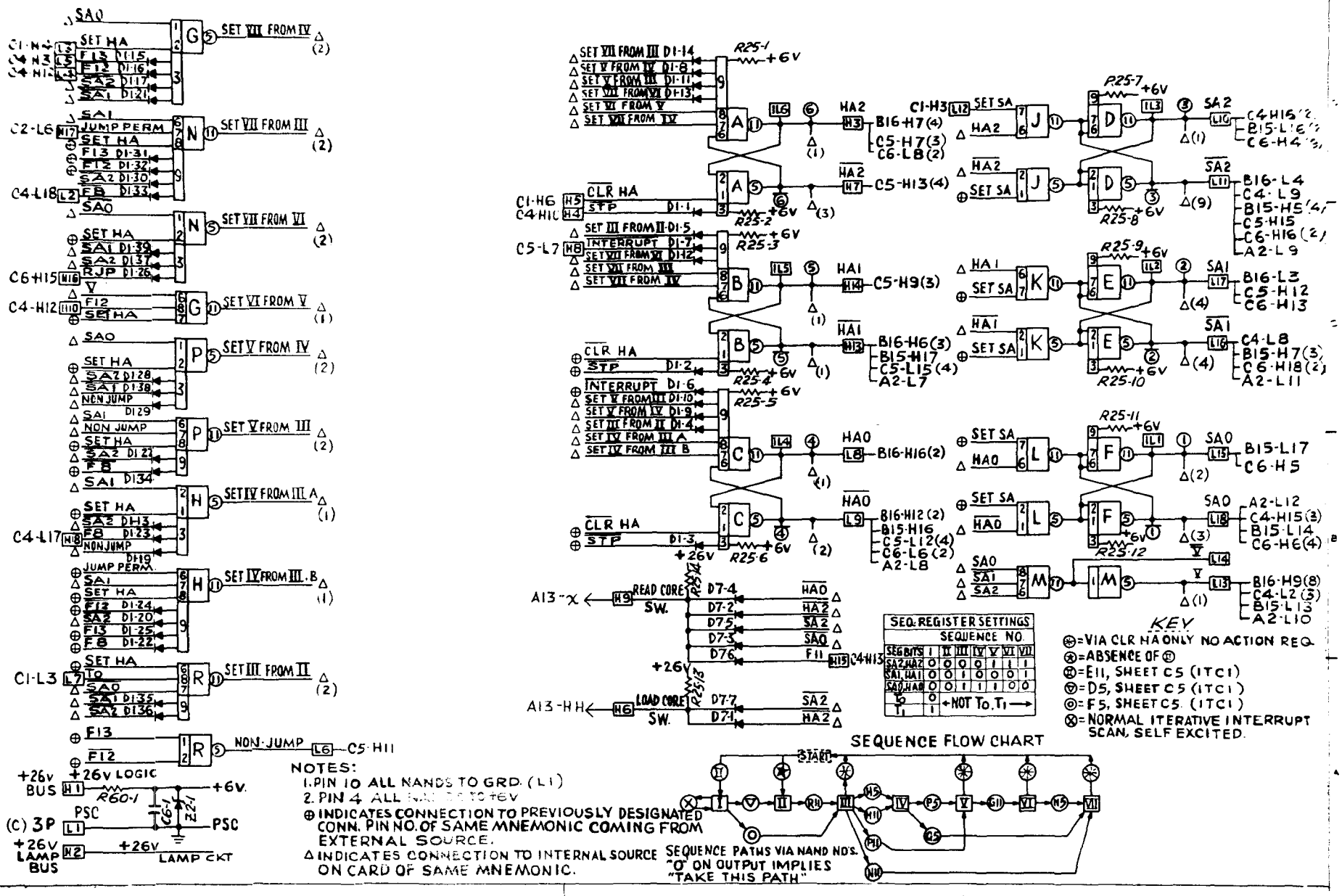
NOTES:

1. PIN 10 ALL NAND TO GND. (L1)
2. PIN 4 ALL NANDS TO +6V EXCEPT WHERE INDICATED.

⊕ INDICATES CONNECTION TO PREVIOULY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE.

△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC.

PRODAC 50 SERIES - M PANEL
DESIGNATOR CARD LOGIC SCHEMATIC (2 DC)
Reference Dwg 867C238 C2

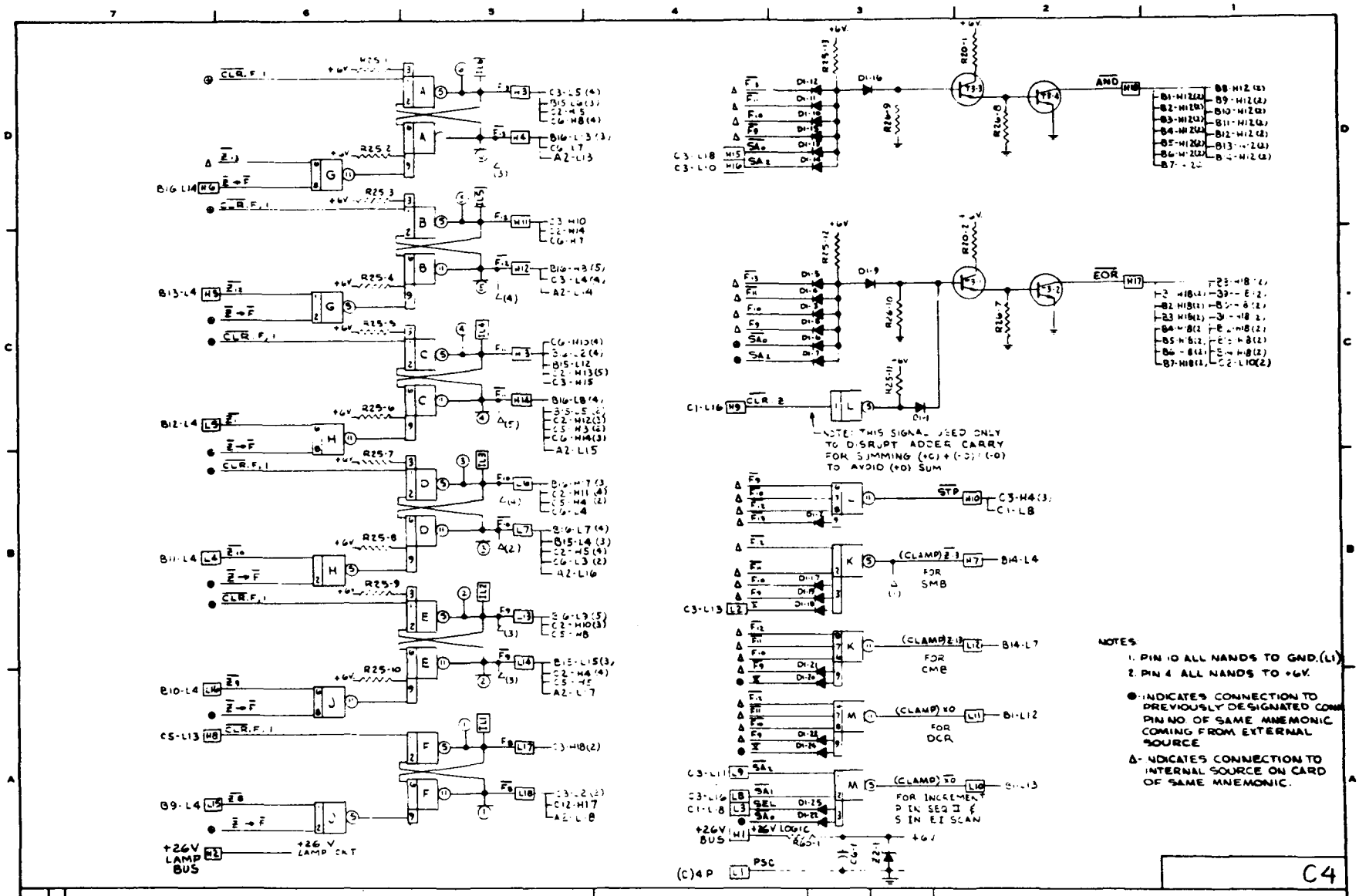


WESTINGHOUSE ELECTRIC CORPORATION

PRODAC "50" SERIES "M" PANEL

SEQUENCE CONTROL - CARD LOGIC SCHEMATIC (ICS)

Reference Dwg 867C239 [illegible]3



NEXT ASS'Y		REF DWG	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020 ANGULAR DIMENSIONS ±1°			
OVER 24	± .06	± .015	
6 IN. to 24	± .04	± .010	
UP TO 6 IN	± .02	± .005	
BASIC DIM	2 PLACE DEC	3 PLACE DEC	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

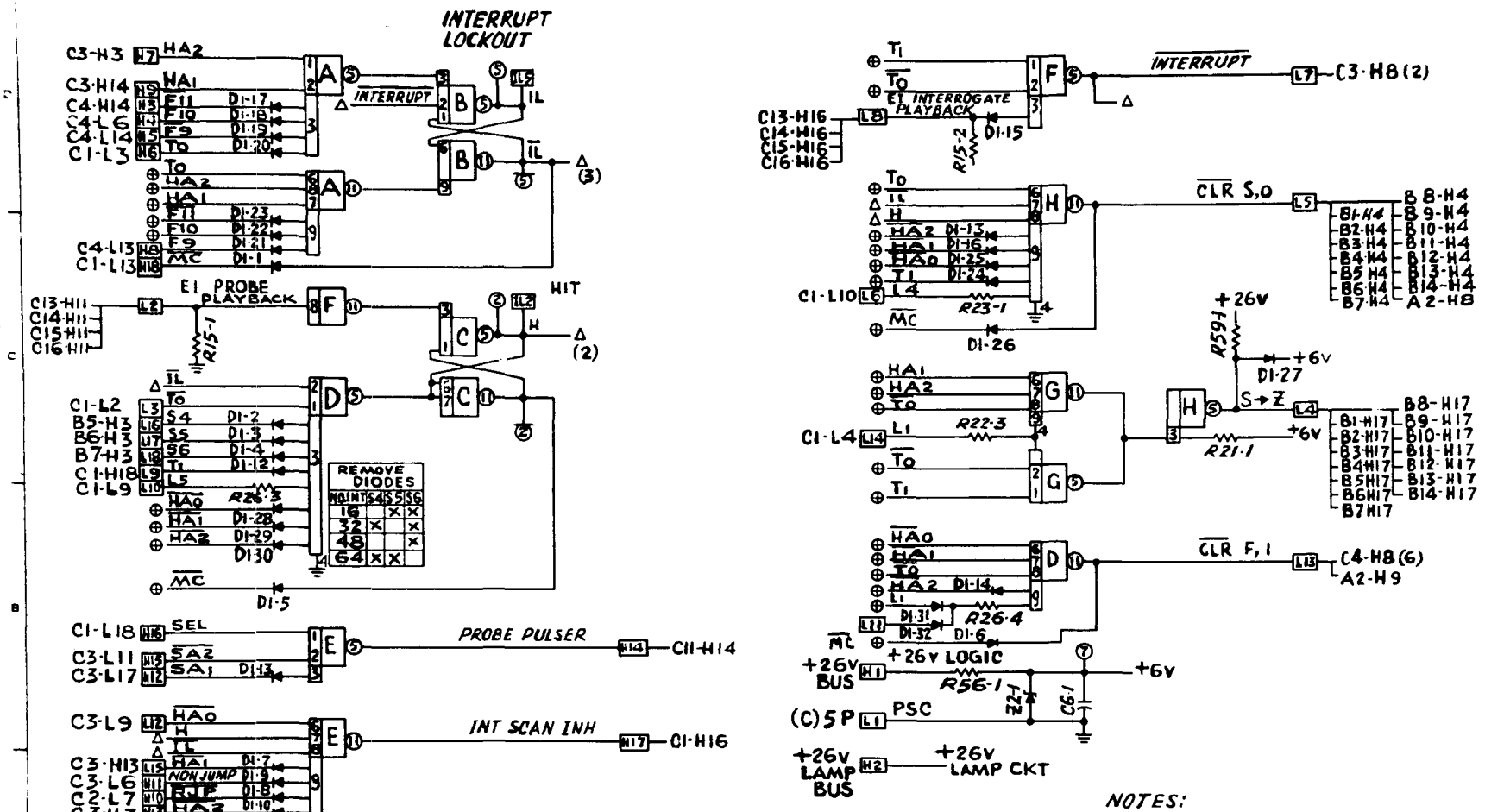
COMPUTER SYSTEMS DIVISION — PITTSBURGH PA. U.S.A.

TITLE PRODAC 50 SERIES - M PANEL
INSTRUCTION REGISTER LOGIC SCHEMATIC (2IR)

DRWG ONE IN INCHES | SCALE | SUB. 1

DRWN | CHKD | APPD | SUPV

867C240



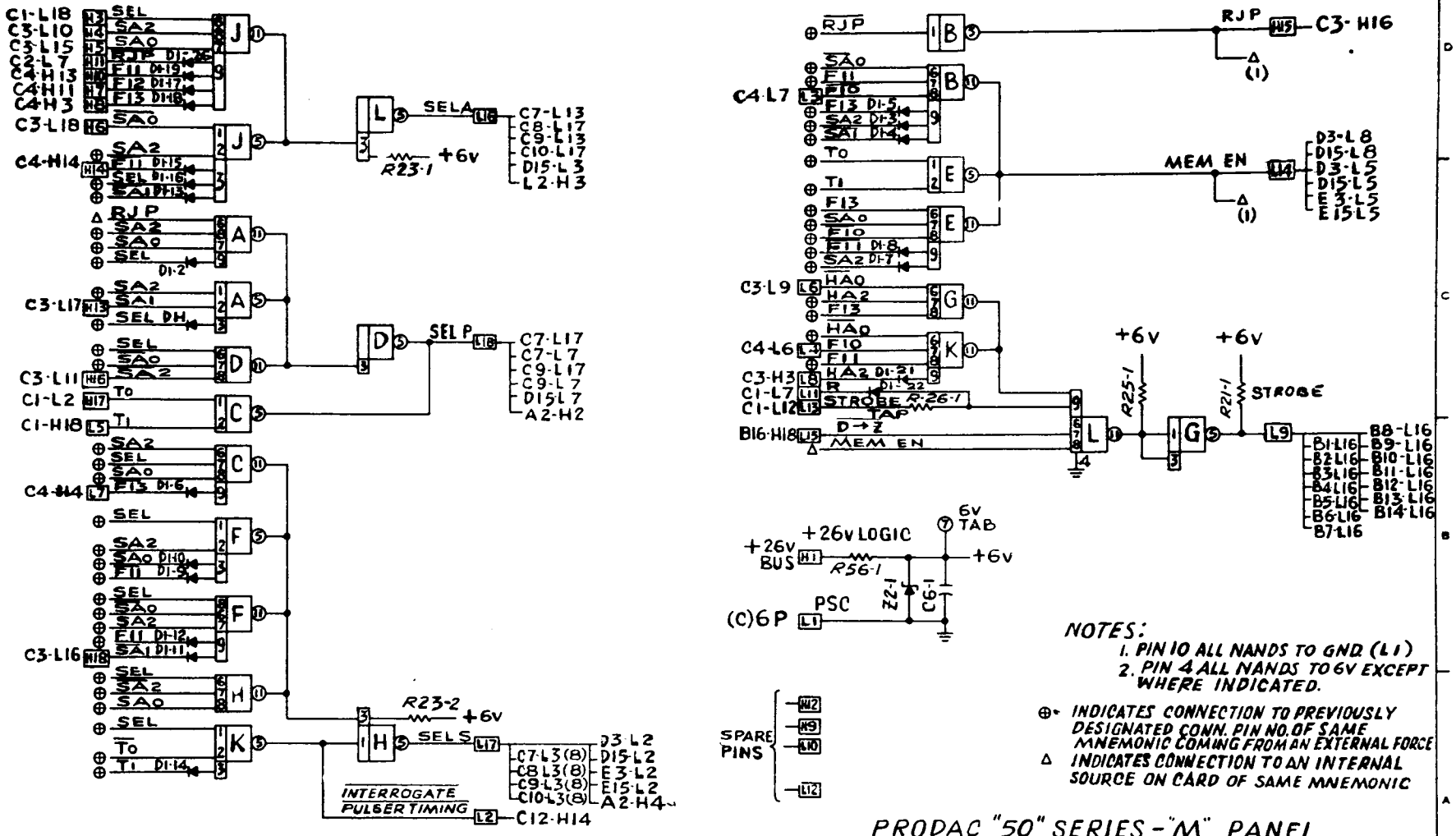
NOTES:

1. PIN 10 ALL NANDS TO GRD. (L 1)
2. PIN 4 ALL NANDS TO +6v EXCEPT WHERE INDICATED

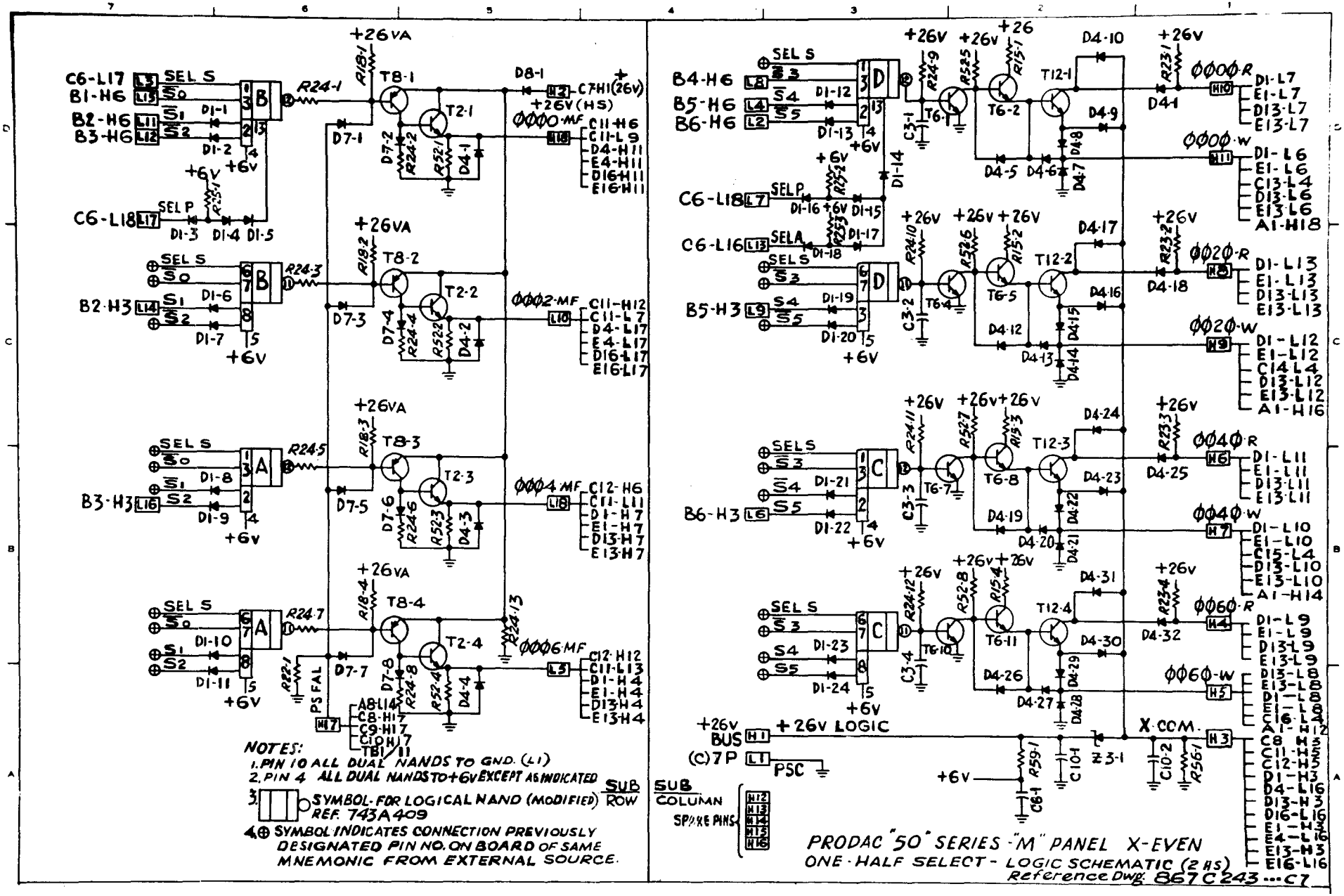
⊕ INDICATES CONNECTION TO PREVIOUSLY DESIGNATED CONN. PIN NO. OF SAME MNEMONIC COMING FROM EXTERNAL SOURCE

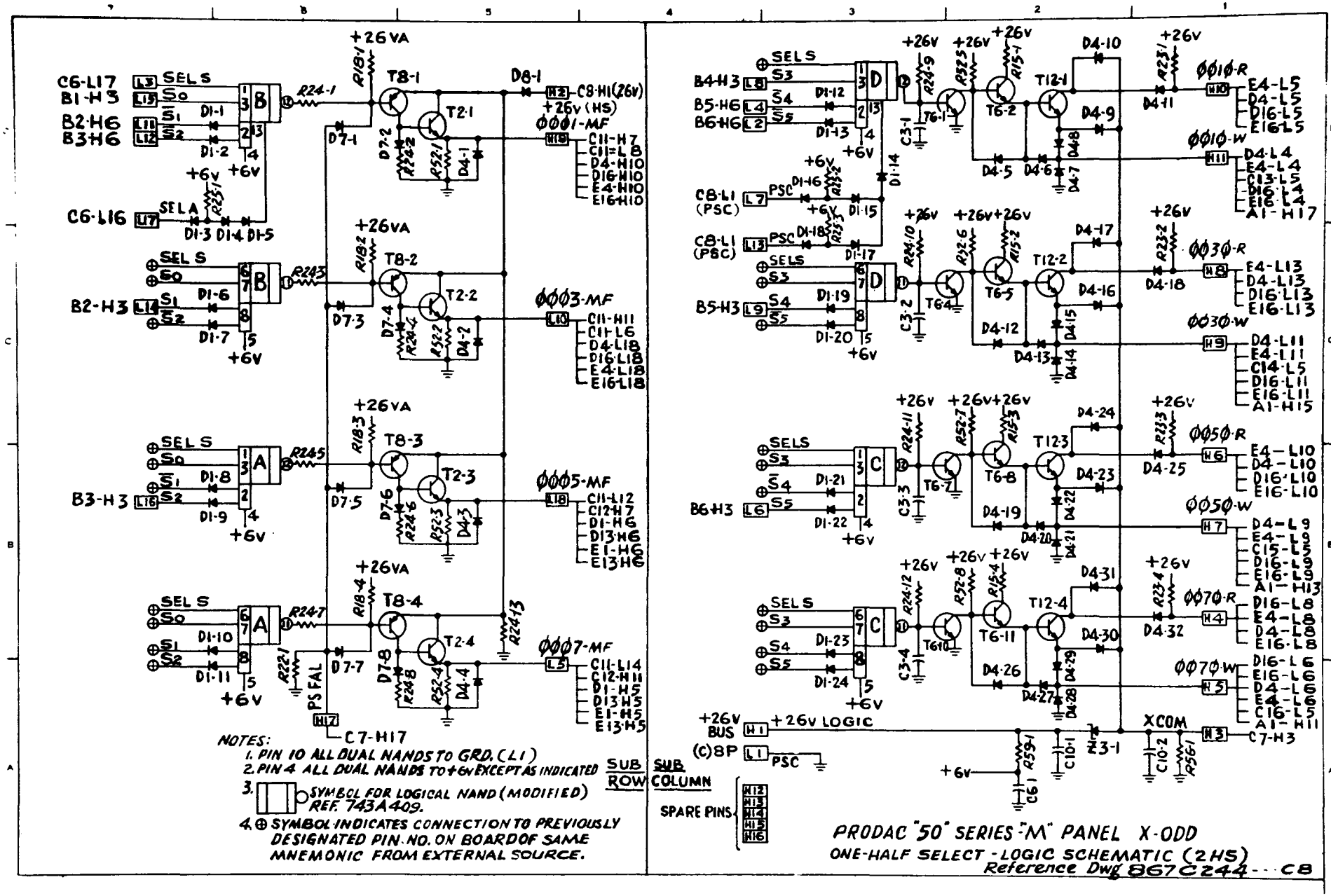
△ INDICATES CONNECTION TO INTERNAL SOURCE ON CARD OF SAME MNEMONIC.

PRODAC "50" SERIES -"M" PANEL 3IC1/2IC1
INTERRUPT SCAN CONTROL LOGIC SCHEMATIC
Reference Dwg 867C241-C5



PRODAC "50" SERIES - "M" PANEL
MEMORY ENABLE LOGIC SCHEMATIC (2ME)
Reference Dwg. 867C 242-C6

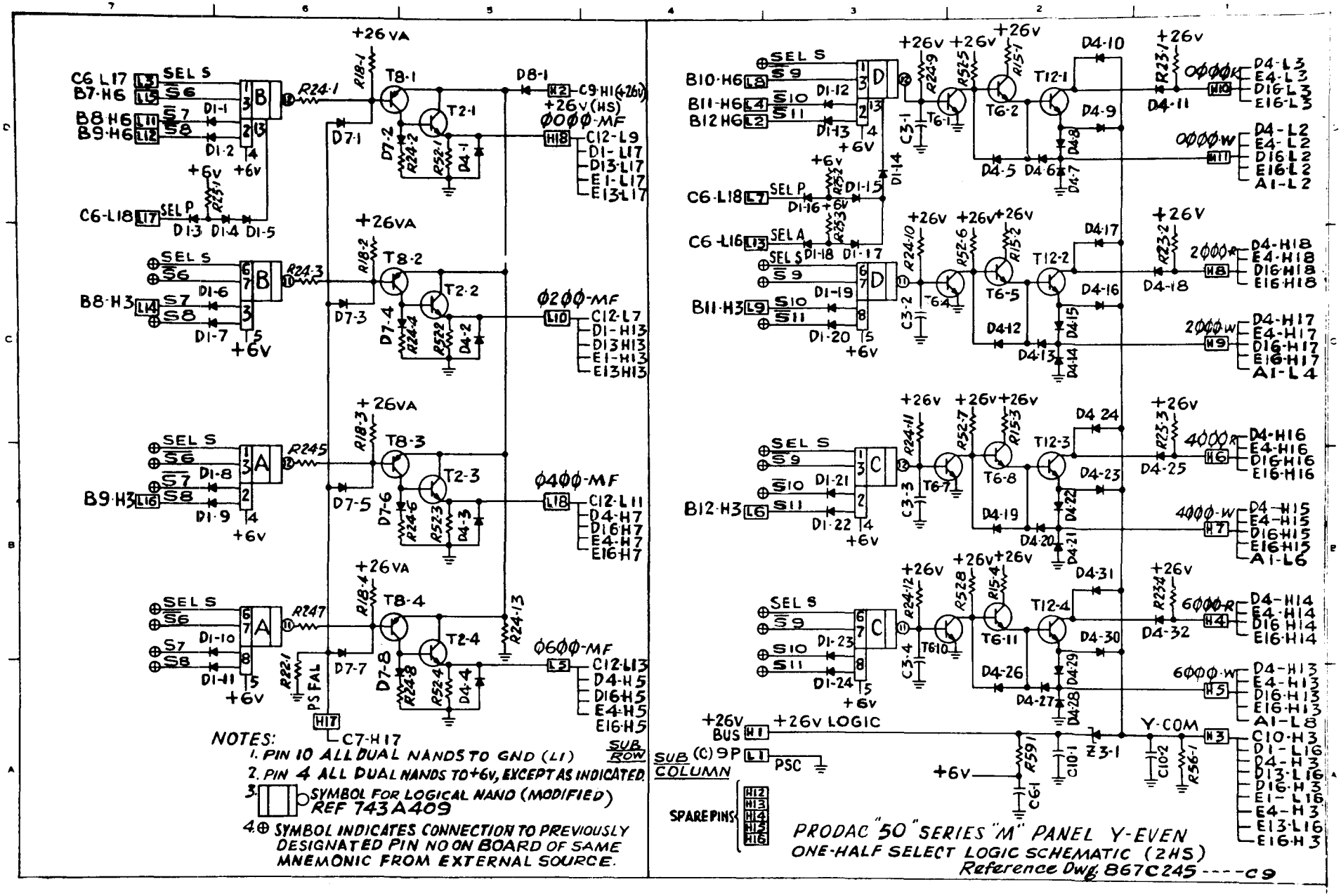

+26VA
C6-L17
B1-H6
B2-H6
B3-H6
SEL S
S0
S1
S2
DI-1
DI-2
+6V
R24-1
R18-1
T8-1
T2-1
D7-1
D7-2
R24-2
R52-1
D4-1
D8-1
+26V(HS)
ØØØØ-MF
C11-H6
C11-L9
D4-H11
E4-H11
D16-H11
E16-H11
C6-L18
SEL P
DI-3
DI-4
DI-5
R23-1
+26VA
R18-2
T8-2
T2-2
D7-3
D7-4
R24-4
R52-2
D4-2
R24-3
ØØØ2-MF
C11-H12
C11-L7
D4-L17
E4-L17
D16-L17
E16-L17
B2-H3
DI-6
DI-7
+26VA
R18-3
T8-3
T2-3
D7-5
D7-6
R24-6
R52-3
D4-3
R24-5
ØØØ4-MF
C12-H6
C11-L11
D1-H7
E1-H7
D13-H7
E13-H7
B3-H3
DI-8
DI-9
+26VA
R18-4
T8-4
T2-4
D7-7
D7-8
R24-8
R52-4
D4-4
R24-7
R24-13
ØØØ6-MF
C12-H12
C11-L13
D1-H4
E1-H4
D13-H4
E13-H4
DI-10
DI-11
R22-1
PS FAL
H17
A8-L14
C8-H17
C9-H17
C10-H17
TB1/11
NOTES:
1. PIN 10 ALL DUAL NANDS TO GND. (L1)
2. PIN 4 ALL DUAL NANDS TO +6V EXCEPT AS INDICATED
3. SYMBOL FOR LOGICAL NAND (MODIFIED) REF. 743A409
4. ⊕ SYMBOL INDICATES CONNECTION PREVIOUSLY DESIGNATED PIN NO. ON BOARD OF SAME MNEMONIC FROM EXTERNAL SOURCE.
SUB ROW
B4-H6
B5-H6
B6-H6
DI-12
DI-13
DI-14
+6V
C3-1
R24-9
R52-5
R15-1
T6-1
T6-2
T12-1
D4-10
D4-9
D4-8
D4-5
D4-6
D4-7
+26V
+26V
+26
R23-1
D4-1
ØØØØ-R
H10
ØØØØ-W
H11
DI-L7
E1-L7
D13-L7
E13-L7
DI-L6
E1-L6
C13-L4
D13-L6
E13-L6
A1-H18
C6-L18
SELP
DI-16
DI-15
DI-17
R25-3
R25-2
C6-L16
SELA
DI-18
R24-10
R52-6
R15-2
T6-4
T6-5
T12-2
D4-17
D4-16
D4-15
D4-12
D4-13
D4-14
D4-18
ØØ2Ø-R
H5
ØØ2Ø-W
H9
DI-L13
E1-L13
D13-L13
E13-L13
DI-L12
E1-L12
C14-L4
D13-L12
E13-L12
A1-H16
B5-H3
DI-19
DI-20
C3-2
R24-11
R52-7
R15-3
T6-7
T6-8
T12-3
D4-24
D4-23
D4-22
D4-19
D4-20
D4-21
R23-3
D4-25
ØØ4Ø-R
H6
ØØ4Ø-W
H7
DI-L11
E1-L11
D13-L11
E13-L11
DI-L10
E1-L10
C15-L4
D13-L10
E13-L10
A1-H14
B6-H3
DI-21
DI-22
C3-3
R24-12
R52-8
R15-4
T6-10
T6-11
T12-4
D4-31
D4-30
D4-29
D4-26
D4-27
D4-28
R23-4
D4-32
ØØ6Ø-R
H4
ØØ6Ø-W
H5
DI-L9
E1-L9
D13-L9
E13-L9
DI-L8
E13-L8
DI-L8
E1-L8
C16-L4
A1-H12
DI-23
DI-24
C3-4
+26V BUS
H1
+26V LOGIC
(C)7P
L1
PSC
+6V
C8-1
R59-1
C10-1
Z3-1
X COM.
C10-2
R56-1
H3
C8-H3
C11-H3
C12-H3
DI-H3
D4-L16
D13-H3
D16-L16
E1-H3
E4-L16
E13-H3
E16-L16
SUB COLUMN SPARE PINS
H12
H13
H14
H15
H16
PRODAC "50" SERIES "M" PANEL X-EVEN
ONE-HALF SELECT - LOGIC SCHEMATIC (2 AS)
Reference Dwg. 867C243 ... C7

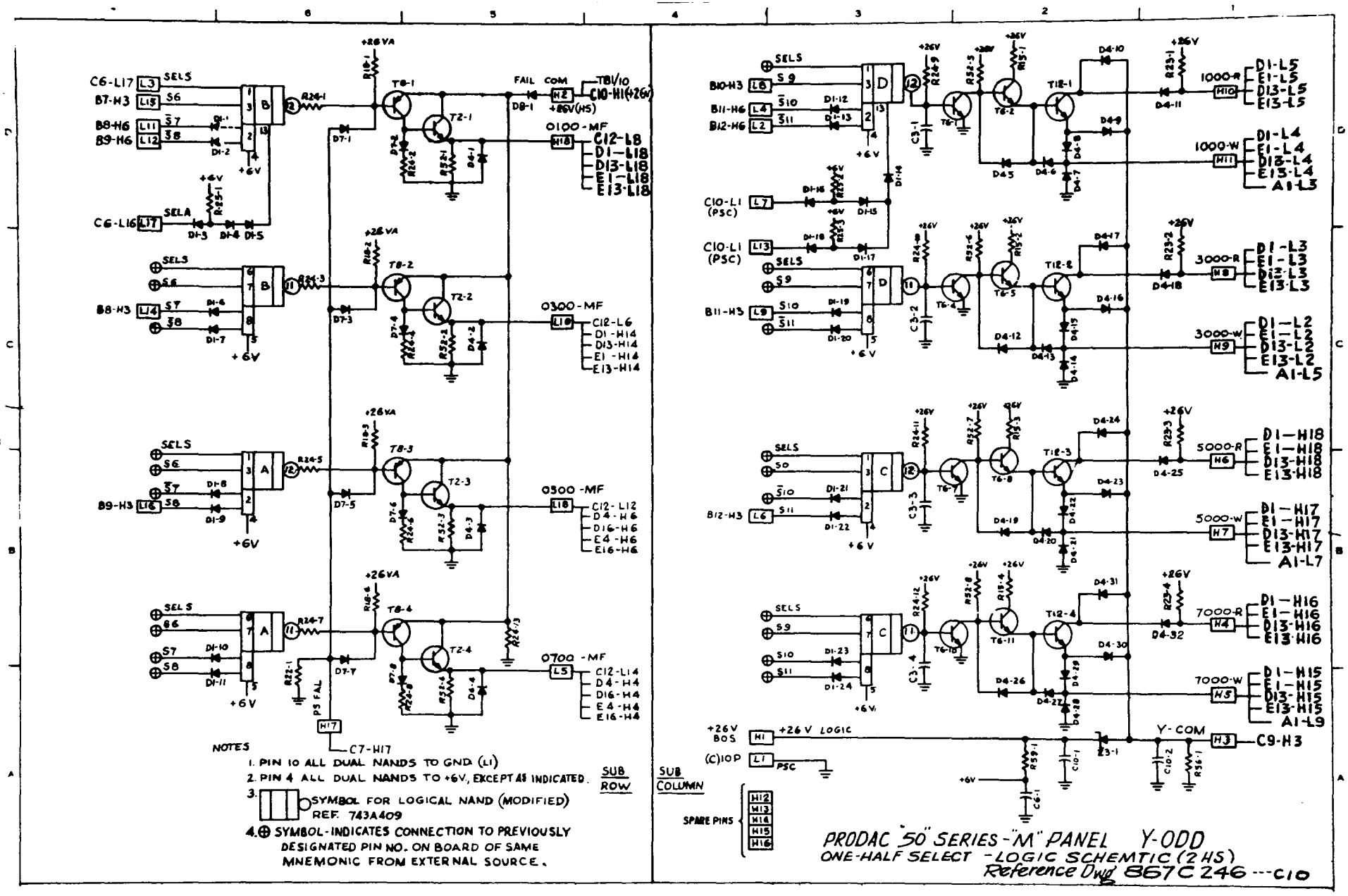


PRODAC "50" SERIES "M" PANEL X-ODD

ONE-HALF SELECT - LOGIC SCHEMATIC (2H5)

Reference Dwg 867C244 - - - C8

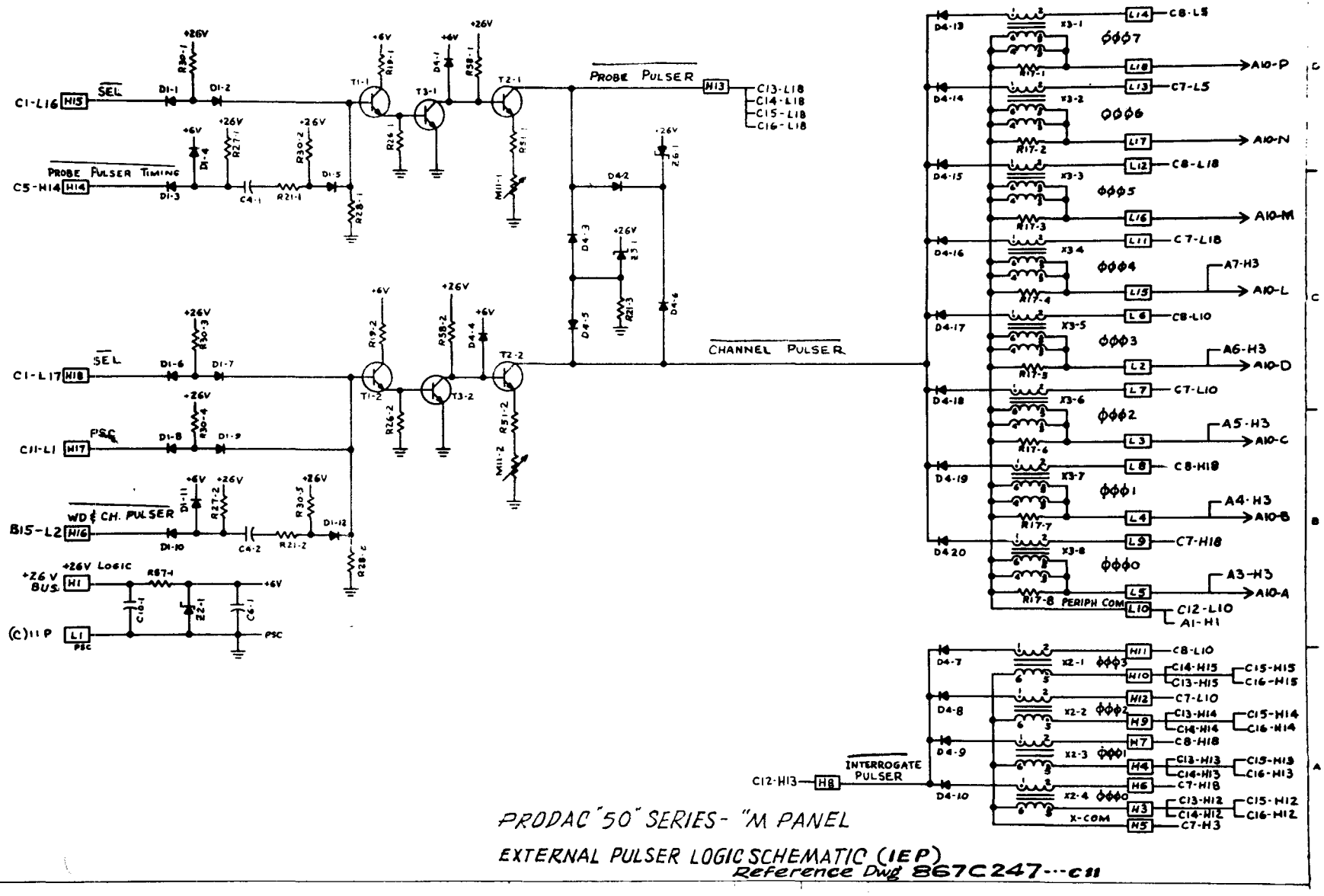

+26VA
C6 L17 L3
B7-H6 L5
B8 H6 L11
B9-H6 L12
SEL S
S6
S7
S8
DI-1
DI-2
+6v
R251
C6-L18 L17
SEL P
DI-3 DI-4 DI-5
R24-1
R18-1
T8-1
T2-1
D7-1
D7-2
R24-2
R52-1
D4-1
D8-1
N2
C9-H1(+26v)
+26v(HS)
ØØØØ-MF
H18
C12-L9
DI-L17
D13-L17
E1-L17
E13-L17
B8-H3 L14
DI-6
DI-7
R24-3
R18-2
T8-2
T2-2
D7-3
D7-4
R24-4
R52-2
D4-2
ØØØØ-MF
L10
C12-L7
DI-H13
D13-H13
E1-H13
E13-H13
B9-H3 L16
DI-8
DI-9
R245
R18-3
T8-3
T2-3
D7-5
D7-6
R24-6
R52-3
D4-3
ØØØØ-MF
L18
C12-L11
D4-H7
D16-H7
E4-H7
E16-H7
DI-10
DI-11
R247
R18-4
T8-4
T2-4
D7-7
D7-8
R24-8
R52-4
D4-4
R24-13
ØØØØ-MF
L5
C12-L13
D4-H5
D16-H5
E4-H5
E16-H5
R221
PS FAL
H17
C7-H17
NOTES:
1. PIN 10 ALL DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6v, EXCEPT AS INDICATED
3. SYMBOL FOR LOGICAL NAND (MODIFIED) REF 743A409
4. SYMBOL INDICATES CONNECTION TO PREVIOUSLY DESIGNATED PIN NO ON BOARD OF SAME MNEMONIC FROM EXTERNAL SOURCE.
SUB ROW
SUB (C) 9P L1
COLUMN
PSC
SPARE PINS H12 H13 H14 H15 H16
B10-H6 L8
B11-H6 L4
B12 H6 L2
SEL S
S9
S10
S11
DI-12
DI-13
+6v
R24-9
R52-5
R15-1
T12-1
T6-2
T6-1
D4-10
D4-9
D4-5
D4-6
D4-7
D4-8
C3-1
DI-14
C6-L18 L7
SEL P
DI-15
DI-16
R23-1
R23-3
C6-L16 L13
SEL A
DI-18
DI-17
B11-H3 L9
DI-19
DI-20
R24-10
R52-6
R15-2
T12-2
T6-5
T6-4
D4-17
D4-16
D4-12
D4-13
D4-14
D4-15
C3-2
R23-2
B12-H3 L6
DI-21
DI-22
R24-11
R52-7
R15-3
T12-3
T6-8
T6-7
D4 24
D4-23
D4-19
D4-20
D4-21
D4-22
C3-3
R23-3
DI-23
DI-24
R24-12
R52-8
R15-4
T12-4
T6-11
T6-10
D4-31
D4-30
D4-26
D4-27
D4-28
D4-29
C3-4
R23-4
+26v BUS H1
+26v LOGIC
Y-COM H3
Z3-1
C10-1
C10-2
R591
C61
R56-1
ØØØØK H10
D4-L3
E4-L3
D16-L3
E16-L3
D4-11
ØØØØW H11
D4-L2
E4-L2
D16-L2
E16-L2
A1-L2
2ØØØK H8
D4-H18
E4-H18
D16-H18
E16-H18
D4-18
2ØØØW H9
D4-H17
E4-H17
D16-H17
E16-H17
A1-L4
4ØØØK H6
D4-H16
E4-H16
D16-H16
E16-H16
D4-25
4ØØØ-W H7
D4-H15
E4-H15
D16-H15
E16-H15
A1-L6
6ØØØ-R H4
D4-H14
E4-H14
D16-H14
E16-H14
D4-32
6ØØØ-W H5
D4-H13
E4-H13
D16-H13
E16-H13
A1-L8
C10-H3
D1-L16
D4-H3
D13-L16
D16-H3
E1-L16
E4-H3
E13-L16
E16-H3
PRODAC "50" SERIES "M" PANEL Y-EVEN
ONE-HALF SELECT LOGIC SCHEMATIC (2HS)
Reference Dwg. 867C245 ---- C9

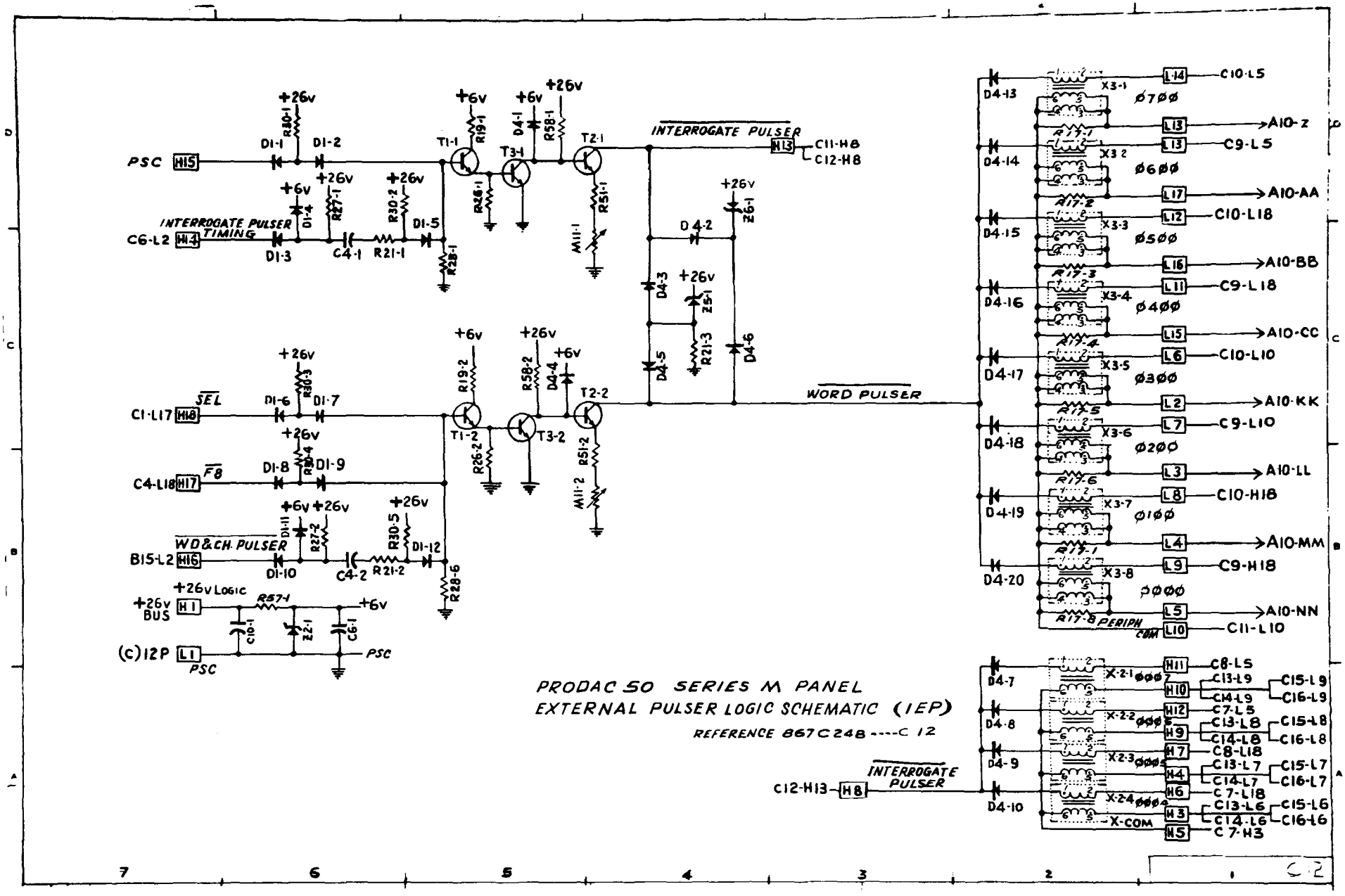


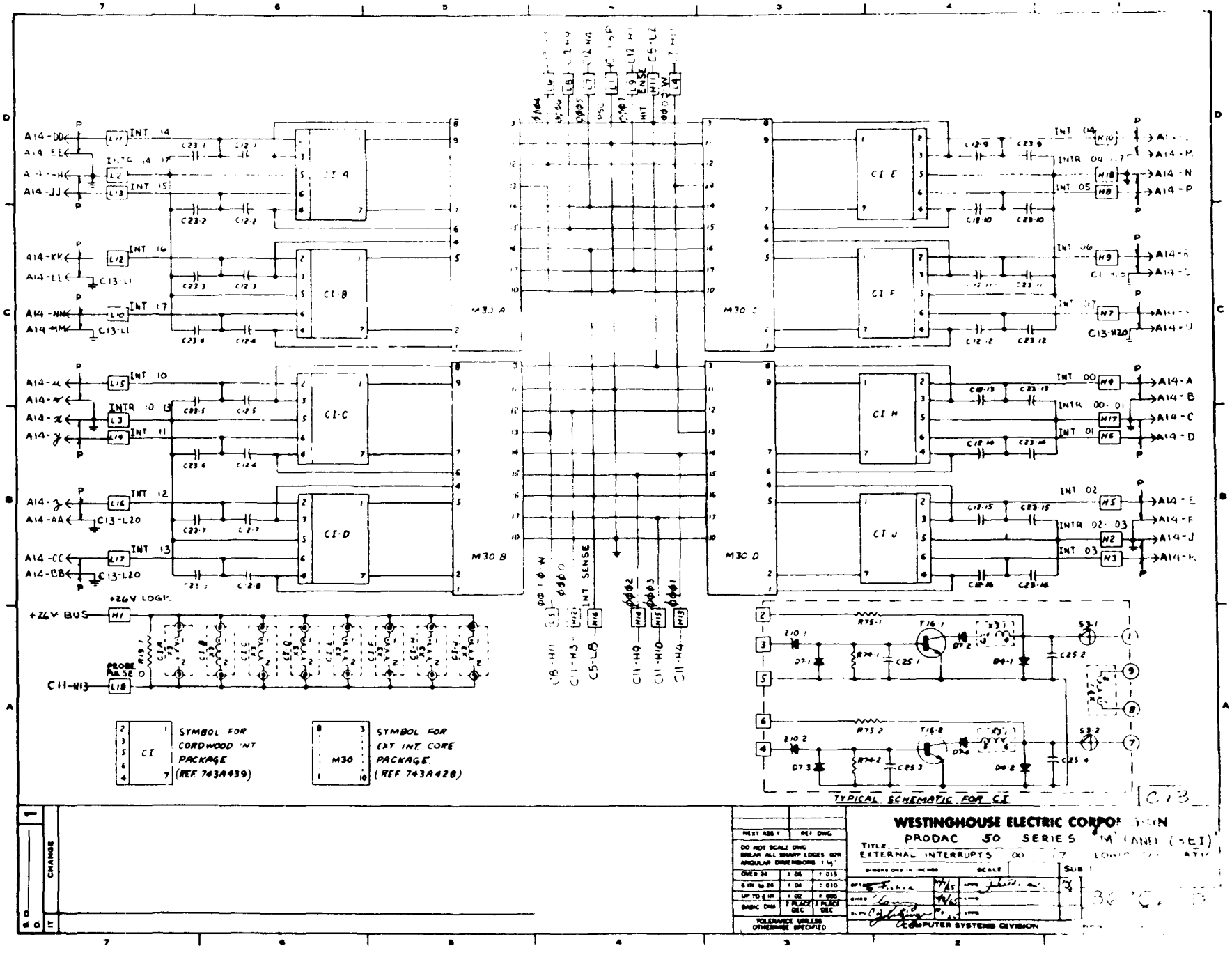
NOTES

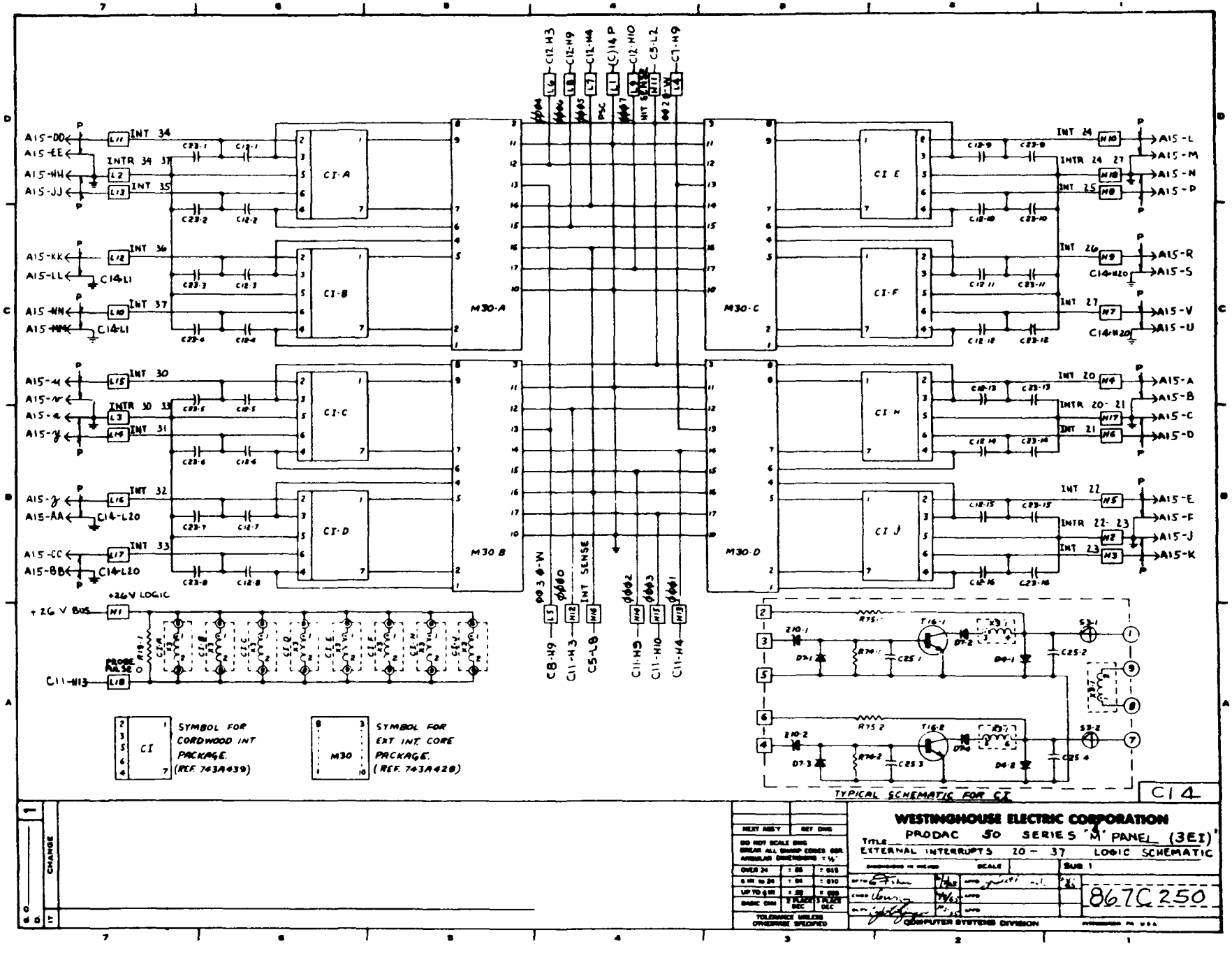
1. PIN 10 ALL DUAL NANDS TO GND (L1)
2. PIN 4 ALL DUAL NANDS TO +6V, EXCEPT AS INDICATED.
3. SYMBOL FOR LOGICAL NAND (MODIFIED) REF. 743A409
4. ⊕ SYMBOL-INDICATES CONNECTION TO PREVIOUSLY DESIGNATED PIN NO. ON BOARD OF SAME MNEMONIC FROM EXTERNAL SOURCE.

PRODAC "50" SERIES-"M" PANEL Y-000
ONE-HALF SELECT -LOGIC SCHEMTIC (2 HS)
Reference Dwg 867C246 ---C10


PRODAC "50" SERIES - "M PANEL
EXTERNAL PULSER LOGIC SCHEMATIC (IEP)
Reference Dwg 867C247---C11
PROBE PULSER
CHANNEL PULSER
INTERROGATE PULSER
C1-L16 H15
C5-H14 H14
C1-L17 H18
C11-L1 H17
B15-L2 H16
C12-H13 H8
+26V BUS H1
(C)11 P L1
C13-L18
C14-L18
C15-L18
C16-L18
A10-P
A10-N
A10-M
A10-L
A10-D
A10-C
A10-B
A10-A
A7-H3
A6-H3
A5-H3
A4-H3
A3-H3
C8-L5
C7-L5
C8-L18
C7-L18
C8-L6
C7-L10
C8-H18
C7-H18
C12-L10
A1-H1
C8-L10
C14-H15
C13-H15
C15-H15
C16-H15
C7-L10
C13-H14
C14-H14
C15-H14
C16-H14
C8-H18
C13-H13
C14-H13
C15-H13
C16-H13
C7-H18
C13-H12
C14-H12
C15-H12
C16-H12
C7-H3
PERIPH COM
X-COM
SEL
PSC
WD & CH. PULSER
PROBE PULSER TIMING
+26V LOGIC


PSC H15
INTERROGATE PULSER TIMING
C6-L2 H14
INTERROGATE PULSER
H13
C11-H8
C12-H8
WORD PULSER
SEL
C1-L17 H18
F8
C4-L18 H17
WD&CH PULSER
B15-L2 H16
+26v Logic
+26v BUS H1
(c)12P L1
PSC
D4-13
D4-14
D4-15
D4-16
D4-17
D4-18
D4-19
D4-20
X3-1 ø7øø
X3-2 ø6øø
X3-3 ø5øø
X3-4 ø4øø
X3-5 ø3øø
X3-6 ø2øø
X3-7 ø1øø
X3-8 øøøø
R17-8 PERIPH COM
L14 C10-L5
L13 A10-Z
L13 C9-L5
L17 A10-AA
L12 C10-L18
L16 A10-BB
L11 C9-L18
L15 A10-CC
L6 C10-L10
L2 A10-KK
L7 C9-L10
L3 A10-LL
L8 C10-H18
L4 A10-MM
L9 C9-H18
L5 A10-NN
L10 C11-L10
PRODAC 50 SERIES M PANEL
EXTERNAL PULSER LOGIC SCHEMATIC (IEP)
REFERENCE 867C248 ----C 12
C12-H13 H8
INTERROGATE PULSER
D4-7
D4-8
D4-9
D4-10
X-2-1 øøøø
X-2-2 øøøø
X-2-3 øøøø
X-2-4 øøøø
X-COM
H11 C8-L5
H10 C13-L9 C15-L9 C16-L9 C14-L9
H12 C7-L5
H9 C13-L8 C15-L8 C16-L8 C14-L8
H7 C8-L18
H4 C13-L7 C15-L7 C16-L7 C14-L7
H6 C7-L18
H3 C13-L6 C15-L6 C16-L6 C14-L6
H5 C7-H3


A14-DD
A14-EE
A14-JJ
INT 14
INT 15
A14-KK
A14-LL
INT 16
A14-NN
A14-MM
INT 17
C13-L1
C13-L11
CI A
CI B
M30 A
A14-LL
A14-MM
INT 10
INT 11
INT 12
INT 13
C13-L20
CI C
CI D
M30 B
CI E
CI F
M30 C
INT 04
INT 05
INT 06
INT 07
C13-M20
A14-K
A14-M
A14-N
A14-P
A14-R
A14-S
A14-U
CI H
CI J
M30 D
INT 00
INTR 00-01
INT 01
INT 02
INTR 02-03
INT 03
A14-A
A14-B
A14-C
A14-D
A14-E
A14-F
A14-J
A14-K
+24V BUS
+24V LOGIC
PROBE PULSE
C11-H13
INT SENSE
C11-H9
C11-H10
C11-H4
C5-L8
C11-H3
SYMBOL FOR CORDWOOD INT PACKAGE (REF 743A439)
SYMBOL FOR EXT INT CORE PACKAGE. (REF 743A428)
TYPICAL SCHEMATIC FOR CI
C13
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL (PEI)
EXTERNAL INTERRUPTS
COMPUTER SYSTEMS DIVISION



WESTINGHOUSE ELECTRIC CORPORATION

PRODAC 50 SERIES "M" PANEL (3EI)

TITLE EXTERNAL INTERRUPTS 20 – 37 LOGIC SCHEMATIC

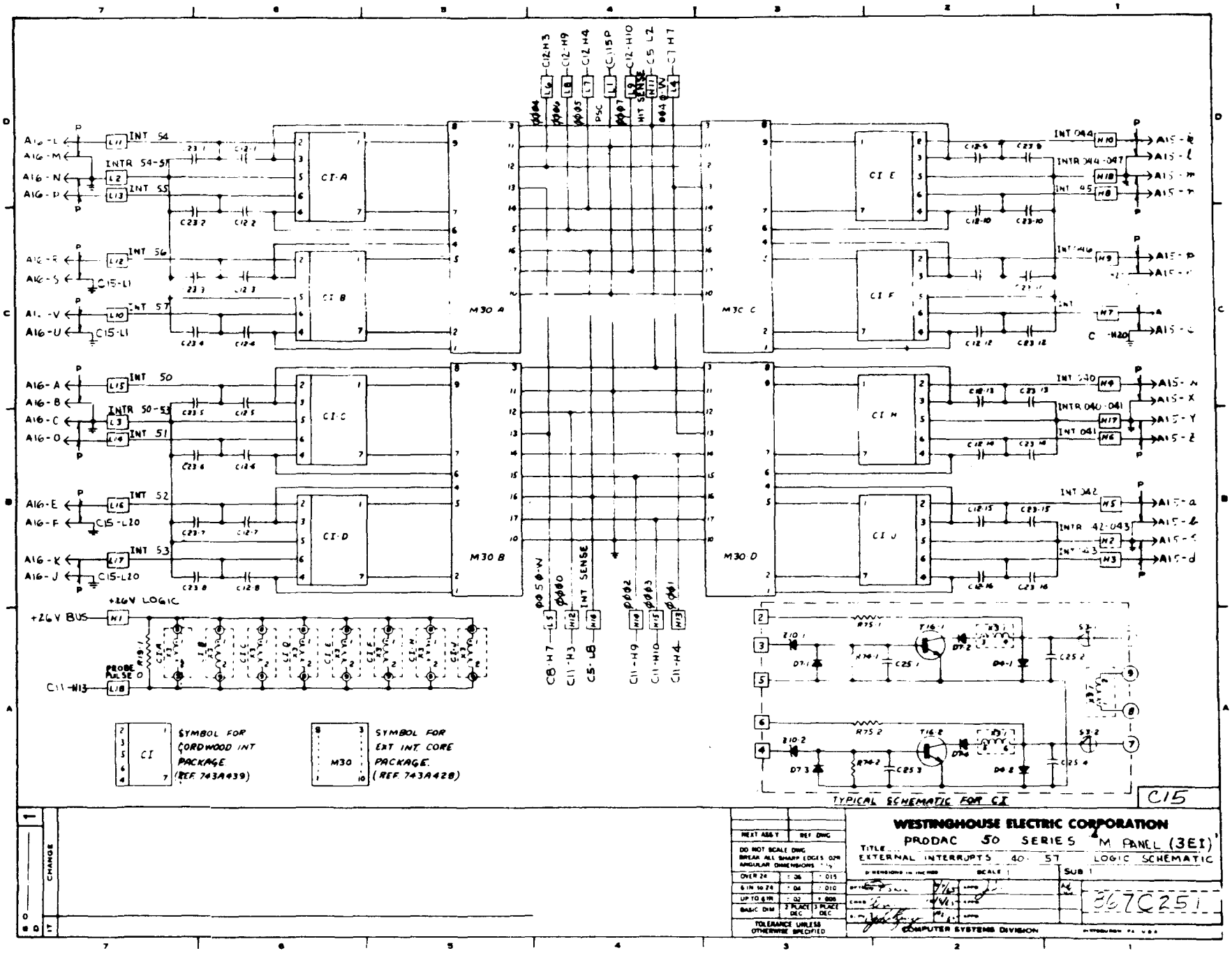
SCALE

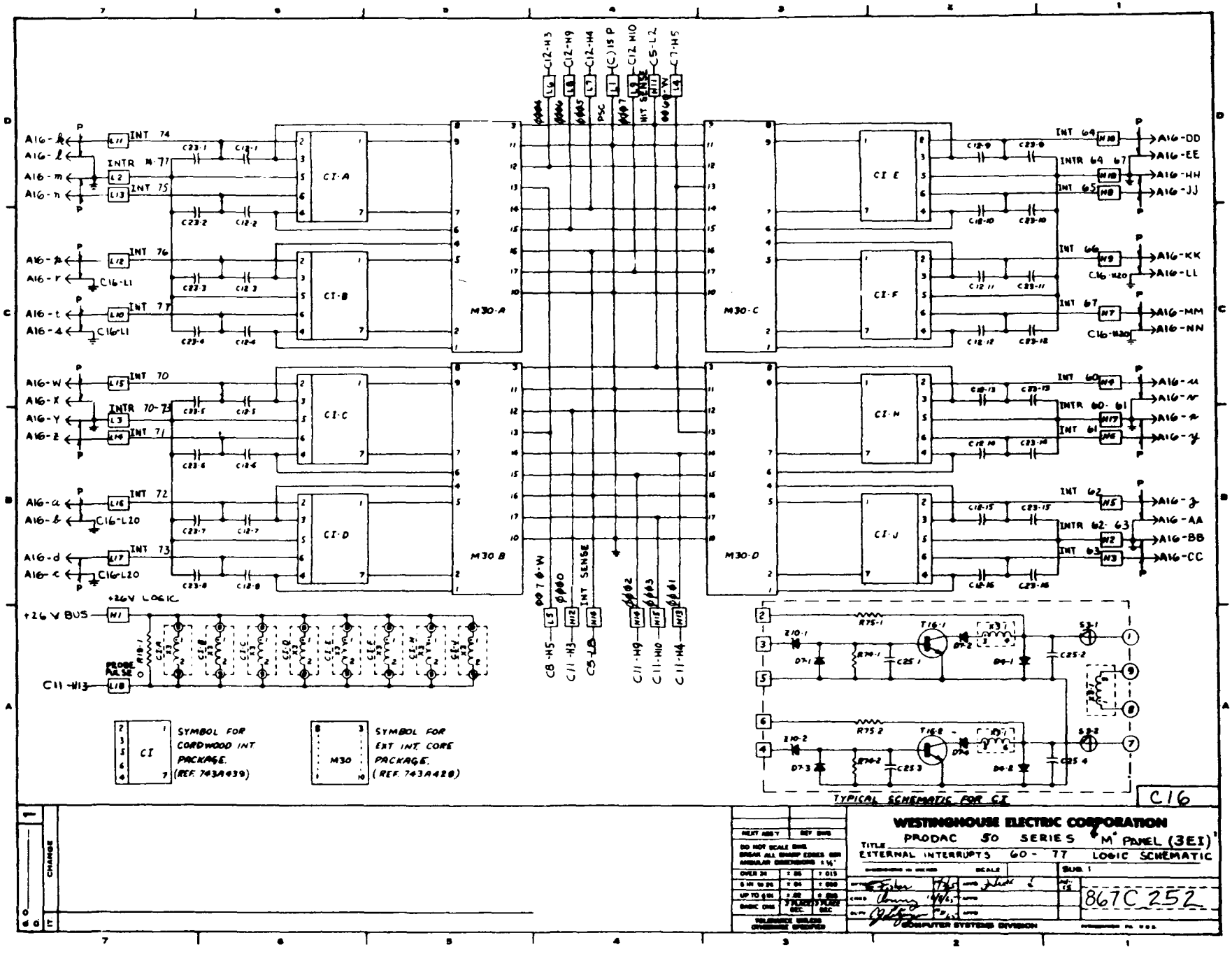
SUB 1

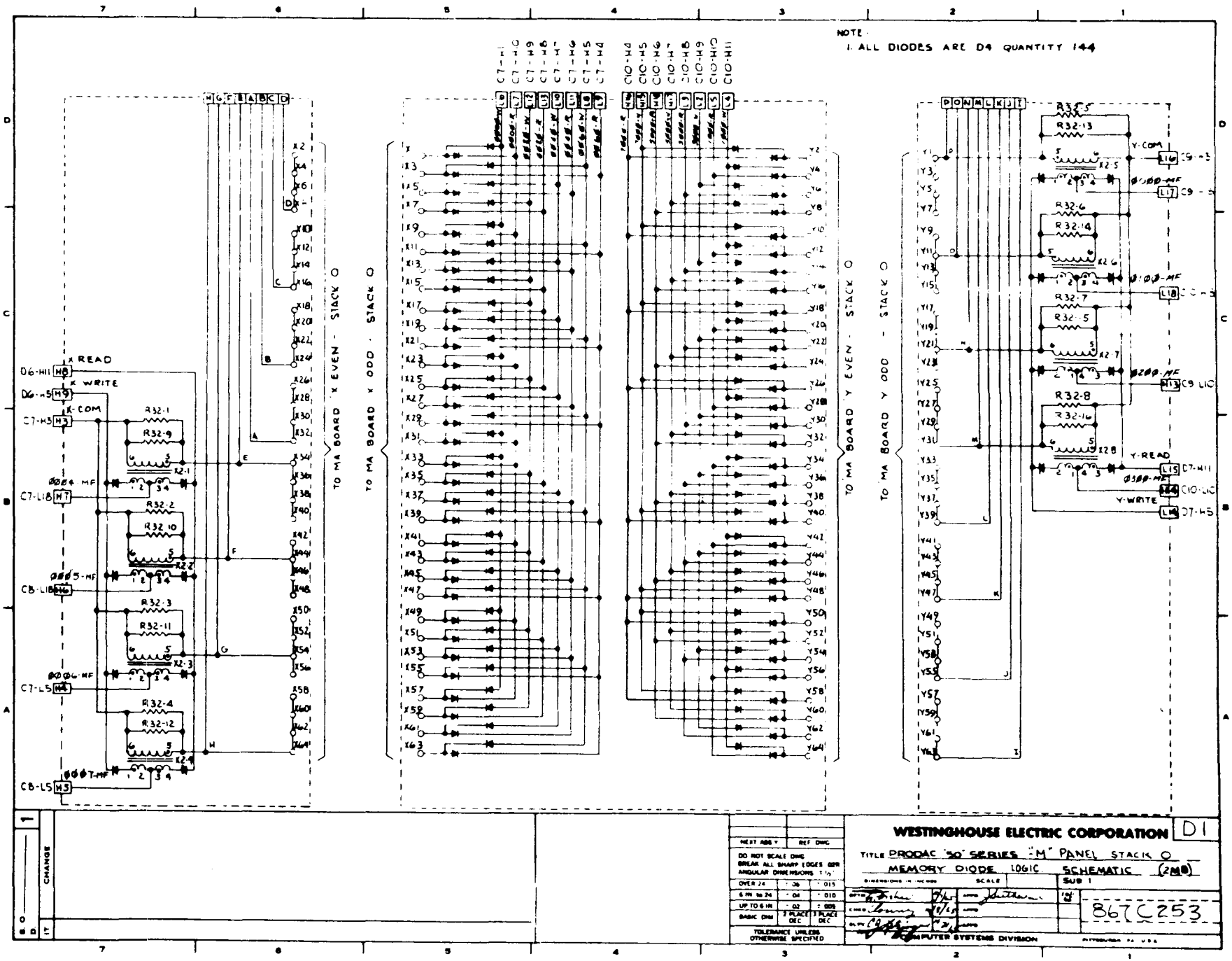
867C250

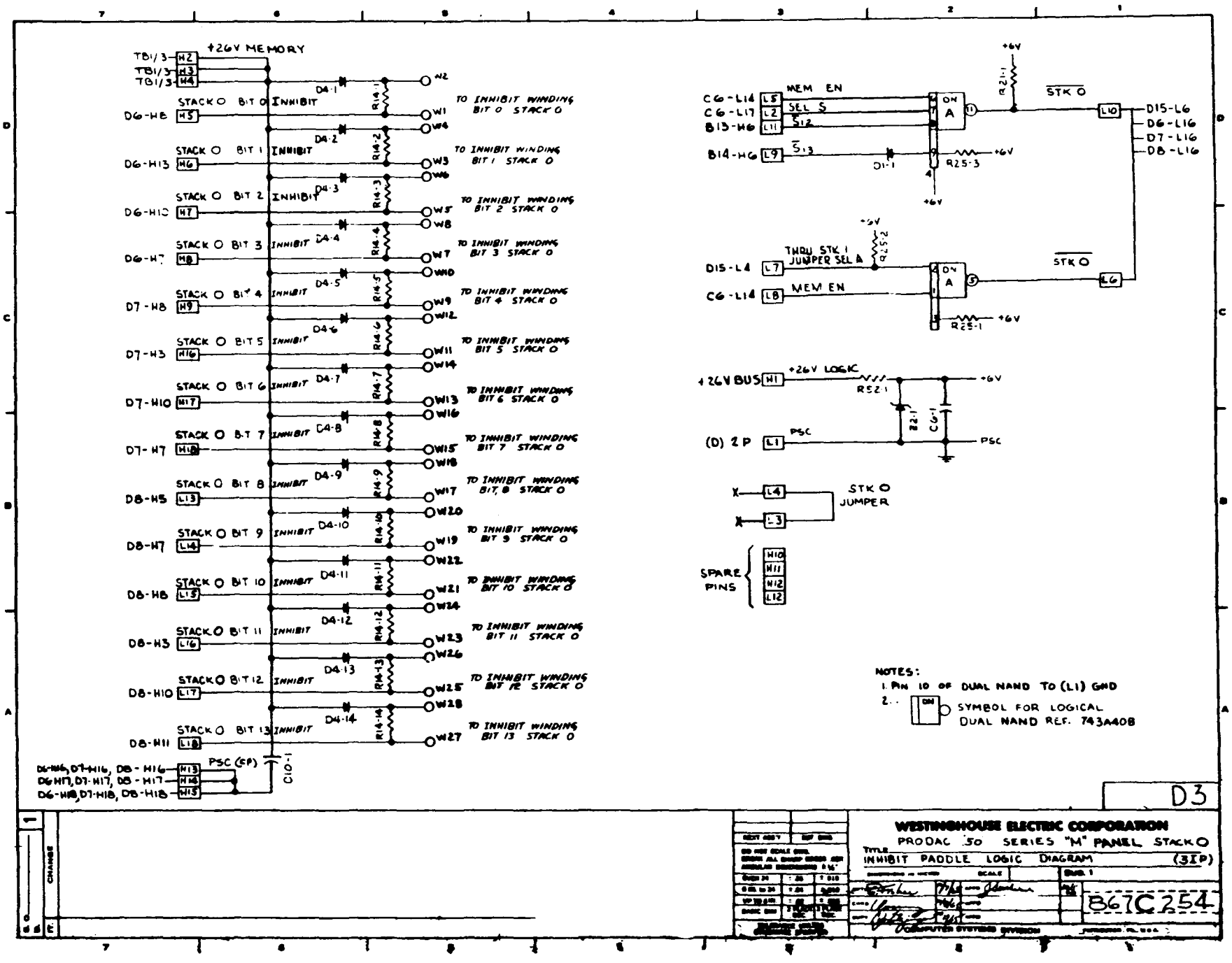
COMPUTER SYSTEMS DIVISION

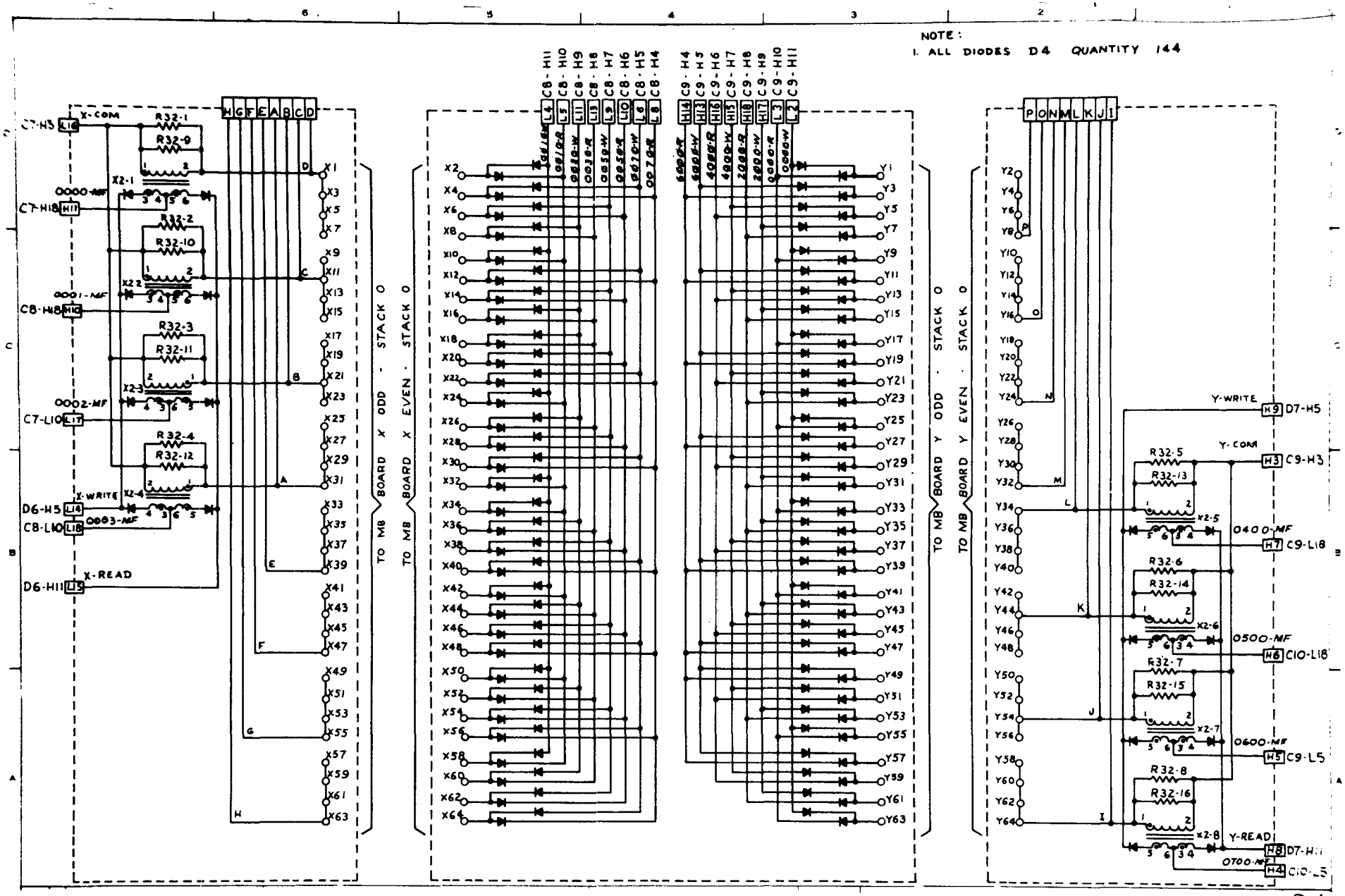
CHANGE


INT 54
INTR 54-57
INT 55
INT 56
INT 57
INT 50
INTR 50-53
INT 51
INT 52
INT 53
+26V LOGIC
+26V BUS
PROBE PULSE
M30 A
M30 B
M30 C
M30 D
CI A
CI B
CI C
CI D
CI E
CI F
CI H
CI J
INT 044
INTR 044-047
INT 045
INT 046
INT 040
INTR 040-041
INT 041
INT 042
INTR 42-043
INT 043
INT SENSE
PSC
SYMBOL FOR CORDWOOD INT PACKAGE. (REF 743A439)
SYMBOL FOR EXT INT. CORE PACKAGE. (REF 743A428)
TYPICAL SCHEMATIC FOR CI
C15
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES M PANEL (3EI)
EXTERNAL INTERRUPTS 40-57 LOGIC SCHEMATIC
COMPUTER SYSTEMS DIVISION
367C251


A16-k
A16-l
A16-m
A16-n
A16-p
A16-r
A16-t
A16-4
A16-w
A16-x
A16-y
A16-z
A16-a
A16-b
A16-d
A16-c
INT 74
INTR 74-77
INT 75
INT 76
C16-L1
INT 77
INT 70
INTR 70-73
INT 71
INT 72
C16-L20
INT 73
+26V LOGIC
+26 V BUS
PROBE PULSE
C11-H13
CI-A
CI-B
CI-C
CI-D
M30-A
M30 B
CI E
CI-F
CI-H
CI-J
M30-C
M30-D
INT 64
INTR 64 67
INT 65
INT 66
C16-H20
INT 67
A16-DD
A16-EE
A16-HH
A16-JJ
A16-KK
A16-LL
A16-MM
A16-NN
INT 60
INTR 60-61
INT 61
INT 62
INTR 62-63
INT 63
A16-u
A16-v
A16-x
A16-y
A16-z
A16-aa
A16-BB
A16-CC
C12-H3
C12-H9
C12-H4
C12 H10
C5-L2
C7-H5
C8-H5
C11-H3
C5-L8
C11-H9
C11-H10
C11-H4
INT SENSE
R75-1
R75-2
T16-1
T16-2
D7-1
D7-3
D9-1
D9-2
C25-1
C25-2
C25-3
C25-4
S2-1
S2-2
TYPICAL SCHEMATIC FOR CI
SYMBOL FOR CORDWOOD INT PACKAGE. (REF 743A439)
SYMBOL FOR EXT INT CORE PACKAGE. (REF 743A428)
C16
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES M PANEL (3EI)
EXTERNAL INTERRUPTS 60 - 77 LOGIC SCHEMATIC
867C252
COMPUTER SYSTEMS DIVISION


NOTE:
1. ALL DIODES ARE D4 QUANTITY 144
X READ
X WRITE
X-COM
TO MA BOARD X EVEN - STACK O
TO MA BOARD X ODD - STACK O
TO MA BOARD Y EVEN - STACK O
TO MA BOARD Y ODD - STACK O
Y-COM
Y-READ
Y-WRITE
R32-1
R32-2
R32-3
R32-4
R32-5
R32-6
R32-7
R32-8
R32-9
R32-10
R32-11
R32-12
R32-13
R32-14
R32-15
R32-16
WESTINGHOUSE ELECTRIC CORPORATION
D1
TITLE PRODAC "50" SERIES "M" PANEL STACK O
MEMORY DIODE LOGIC SCHEMATIC (2MB)
SUB 1
867C253
COMPUTER SYSTEMS DIVISION

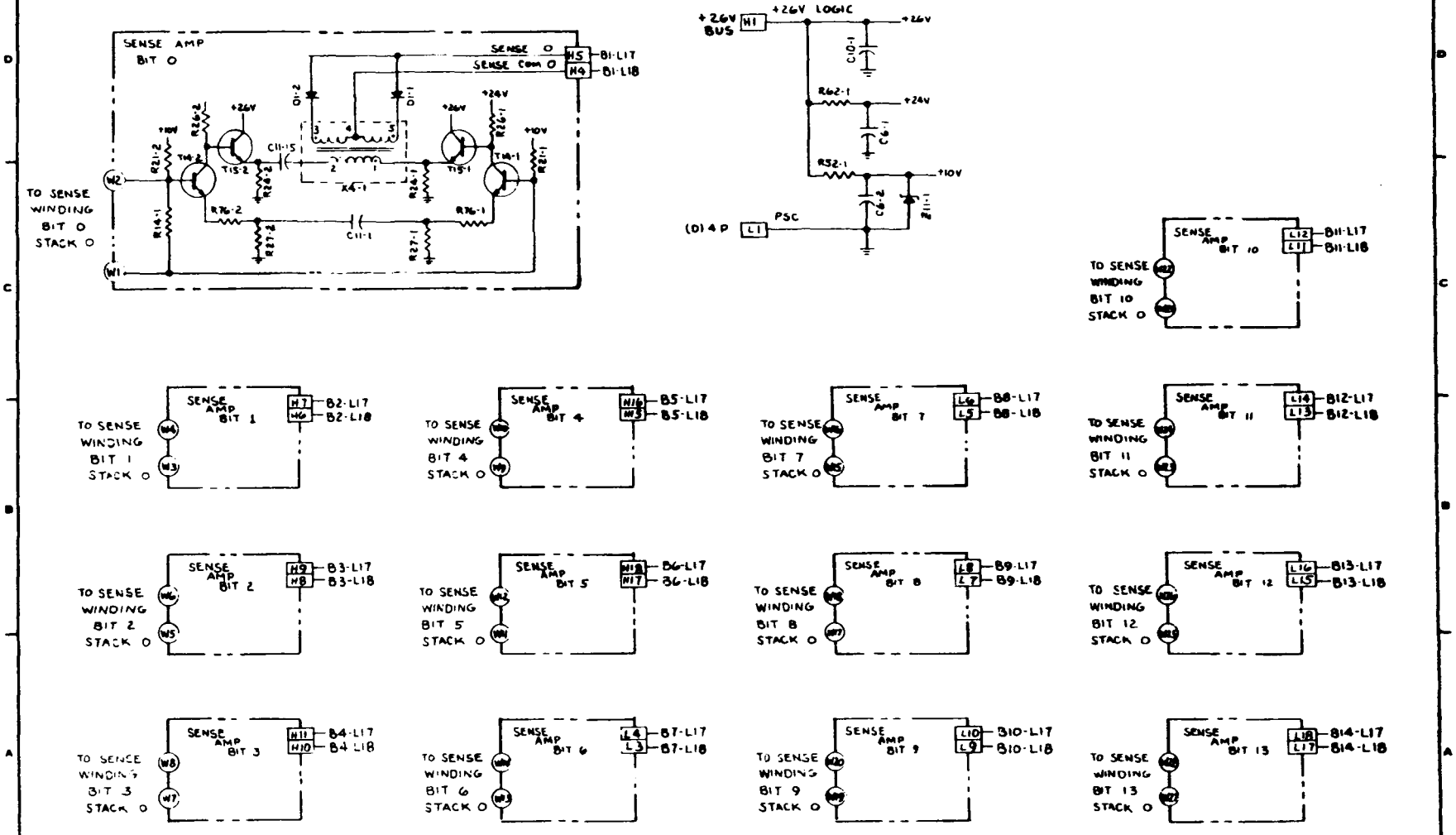

+26V MEMORY
TB1/3 H2
TB1/3 H3
TB1/3 H4
STACK O BIT 0 INHIBIT
D6-H8 H5
D4-1
R14-1
W2
W1
TO INHIBIT WINDING BIT 0 STACK 0
W4
STACK O BIT 1 INHIBIT
D6-H13 H6
D4-2
R14-2
W3
TO INHIBIT WINDING BIT 1 STACK 0
W6
STACK O BIT 2 INHIBIT
D6-H12 H7
D4-3
R14-3
W5
TO INHIBIT WINDING BIT 2 STACK 0
W8
STACK O BIT 3 INHIBIT
D6-H7 H8
D4-4
R14-4
W7
TO INHIBIT WINDING BIT 3 STACK 0
W10
STACK O BIT 4 INHIBIT
D7-H8 H9
D4-5
R14-5
W9
TO INHIBIT WINDING BIT 4 STACK 0
W12
STACK O BIT 5 INHIBIT
D7-H3 H16
D4-6
R14-6
W11
TO INHIBIT WINDING BIT 5 STACK 0
W14
STACK O BIT 6 INHIBIT
D7-H10 H17
D4-7
R14-7
W13
TO INHIBIT WINDING BIT 6 STACK 0
W16
STACK O BIT 7 INHIBIT
D7-H7 H18
D4-8
R14-8
W15
TO INHIBIT WINDING BIT 7 STACK 0
W18
STACK O BIT 8 INHIBIT
D8-H5 L13
D4-9
R14-9
W17
TO INHIBIT WINDING BIT 8 STACK 0
W20
STACK O BIT 9 INHIBIT
D8-H7 L14
D4-10
R14-10
W19
TO INHIBIT WINDING BIT 9 STACK 0
W22
STACK O BIT 10 INHIBIT
D8-H8 L15
D4-11
R14-11
W21
TO INHIBIT WINDING BIT 10 STACK 0
W24
STACK O BIT 11 INHIBIT
D8-H3 L16
D4-12
R14-12
W23
TO INHIBIT WINDING BIT 11 STACK 0
W26
STACK O BIT 12 INHIBIT
D8-H10 L17
D4-13
R14-13
W25
TO INHIBIT WINDING BIT 12 STACK 0
W28
STACK O BIT 13 INHIBIT
D8-H11 L18
D4-14
R14-14
W27
TO INHIBIT WINDING BIT 13 STACK 0
D6-H16, D7-H16, D8-H16 H13
D6-H17, D7-H17, D8-H17 H14
D6-H18, D7-H18, D8-H18 H15
PSC (EP)
C10-1
C6-L14 L5
C6-L17 L2
B13-H6 L11
B14-H6 L9
MEM EN
SEL S1
S2
S3
D1-1
R25-3
+6V
R21-1
STK O
L10
D15-L6
D6-L16
D7-L16
D8-L16
THRU STK 1 JUMPER SEL A
D15-L4 L7
C6-L14 L8
R25-2
R25-1
L6
+26V BUS H1
+26V LOGIC
R52-1
R22-1
C6-1
(D) 2P L1
PSC
X L4
X L3
STK O JUMPER
SPARE PINS H10 H11 H12 L12
NOTES:
1. PIN 10 OF DUAL NAND TO (L1) GND
2. SYMBOL FOR LOGICAL DUAL NAND REF. 743A408
D3
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK O
INHIBIT PADDLE LOGIC DIAGRAM (3IP)
867C254
COMPUTER SYSTEMS DIVISION



WESTINGHOUSE ELECTRIC CORPORATION D1

TITLE PRODAC "50" SERIES "M" PANEL STACK 0
MEMORY DIODE LOGIC SCHEMATIC (2MA)

867C255



D5

1	CHANGE	

NEXT ASS'Y | REF DWG

DO NOT SCALE DWG
BREAK ALL SHARP EDGES .005 MAX
ANGULAR DIMENSIONS ± ½°

OVER 24	± .06	± .015
6 IN to 24	± .04	± .010
UP TO 6 IN	± .02	± .005
BASIC DIM	2 PLACE DEC	3 PLACE DEC

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

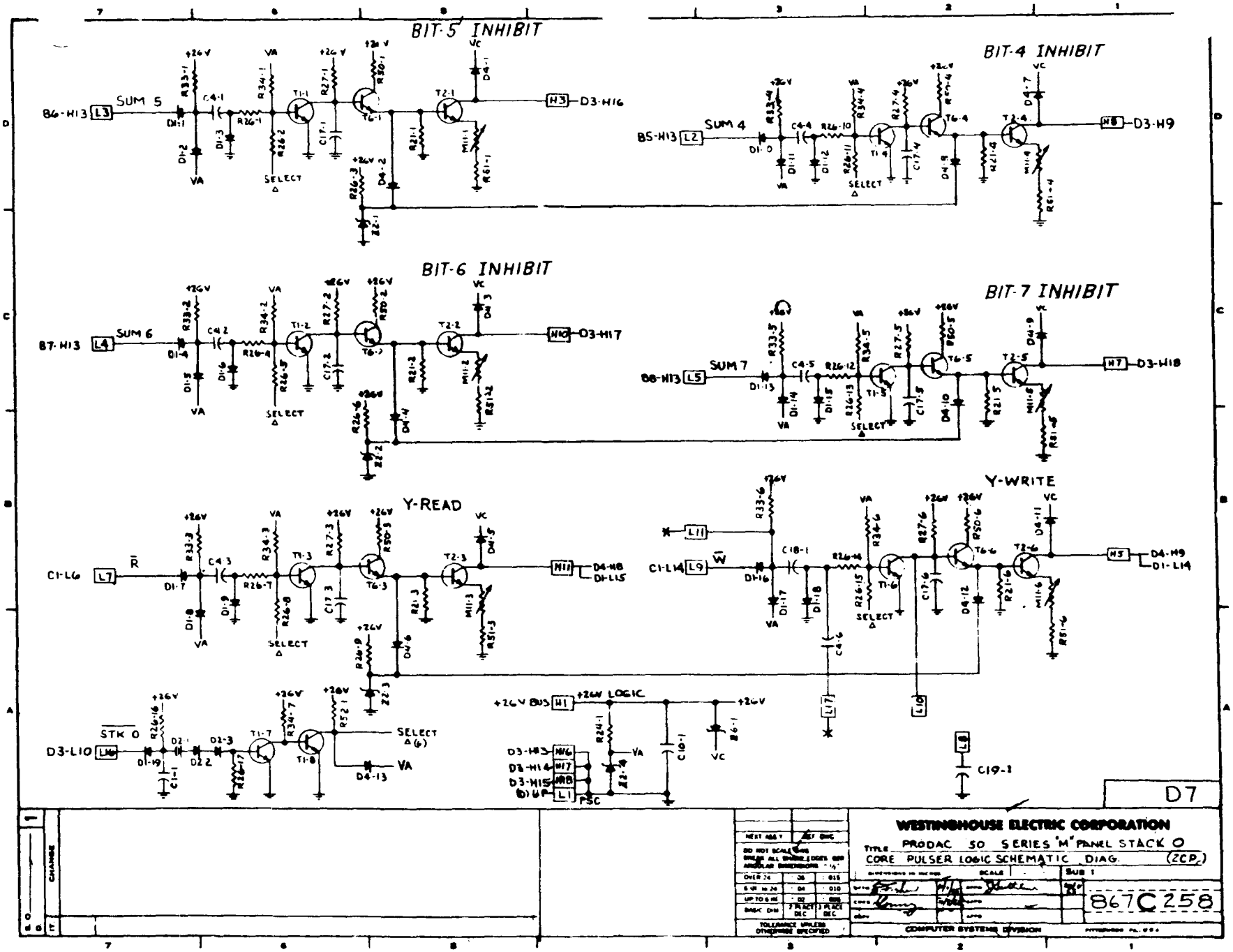
PRODAC 50 SERIES "M" PANEL STACK 0

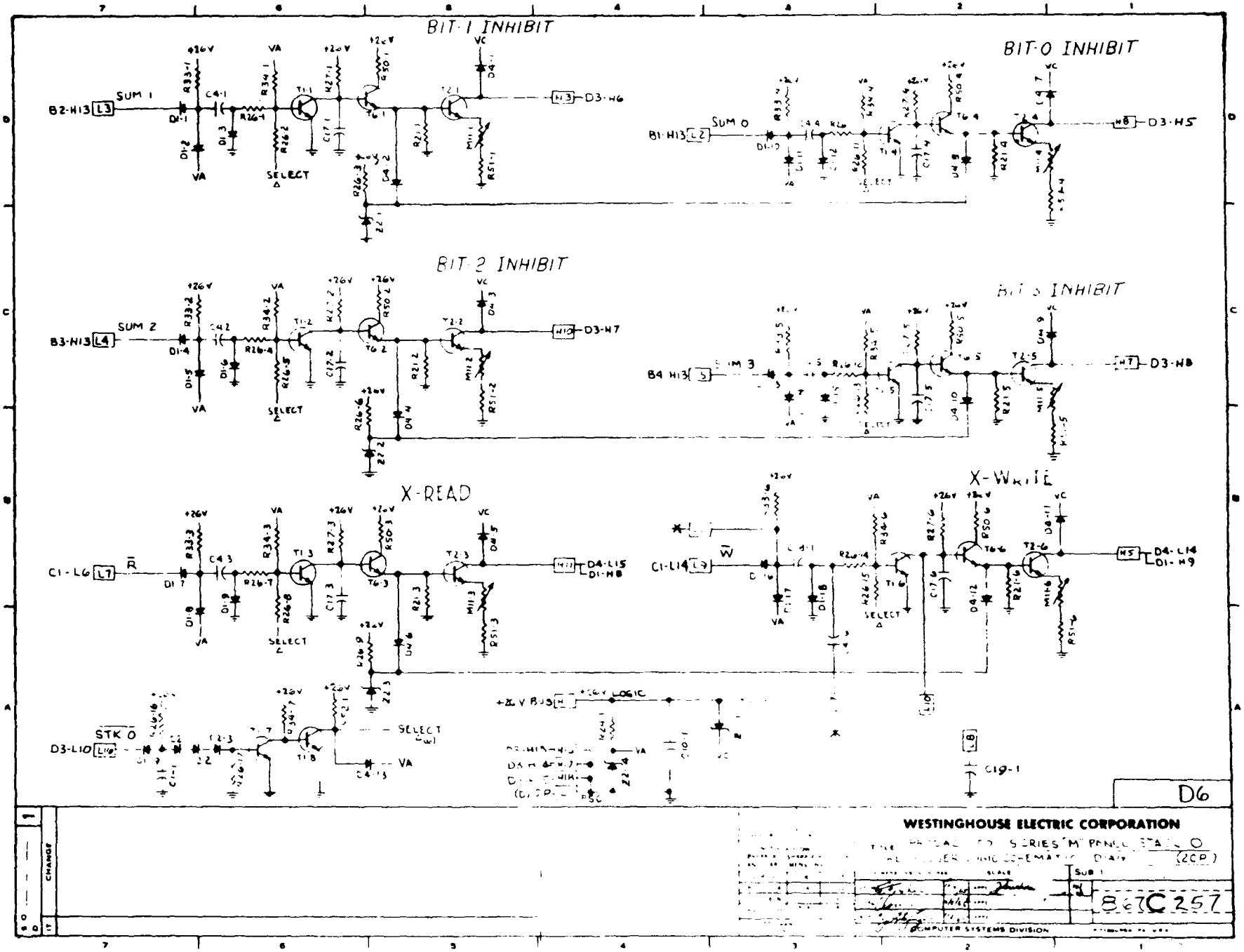
TITLE: SENSE AMPLIFIER LOGIC SCHEMATIC (ISA)

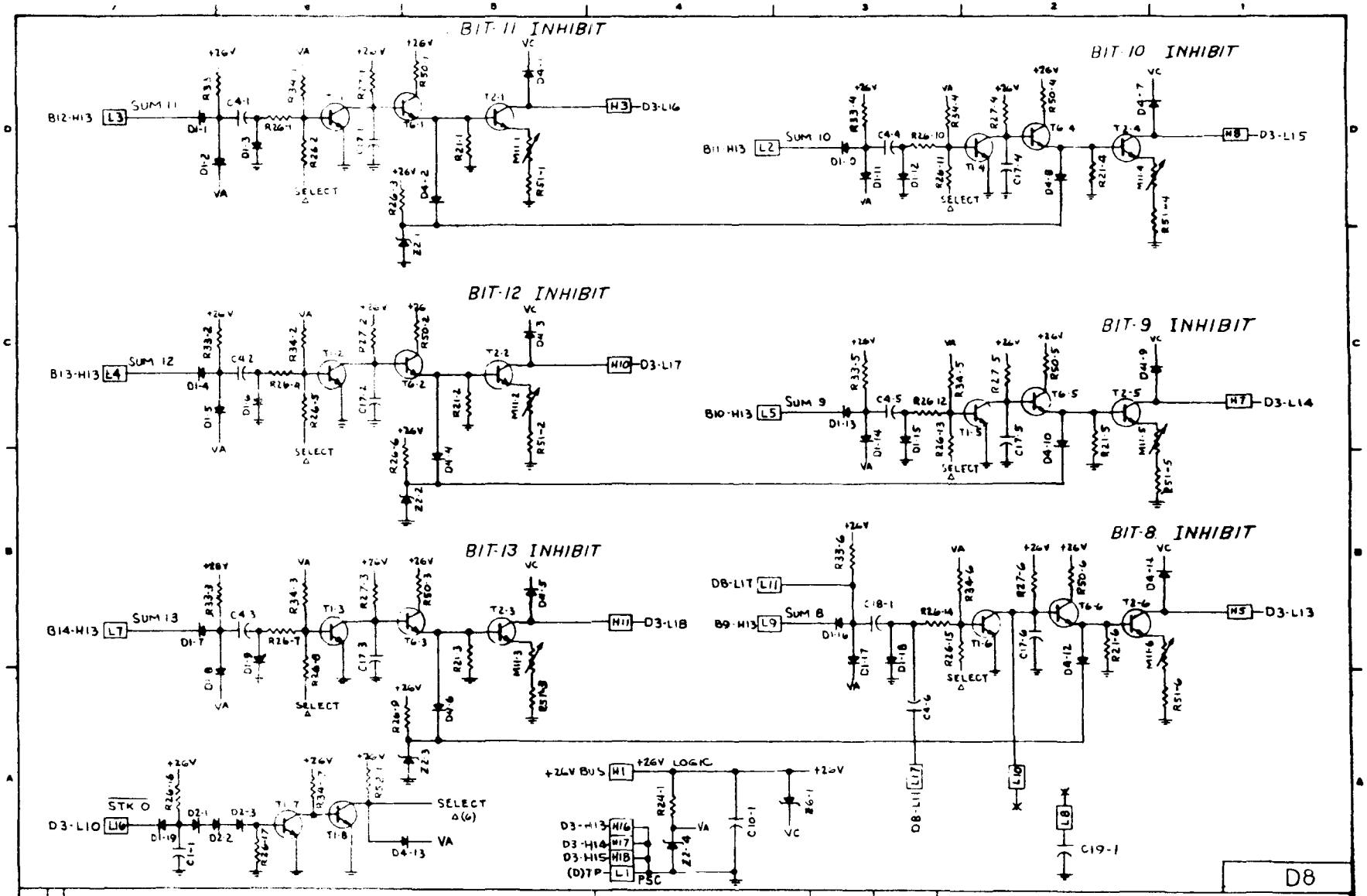
SCALE | SUB 1

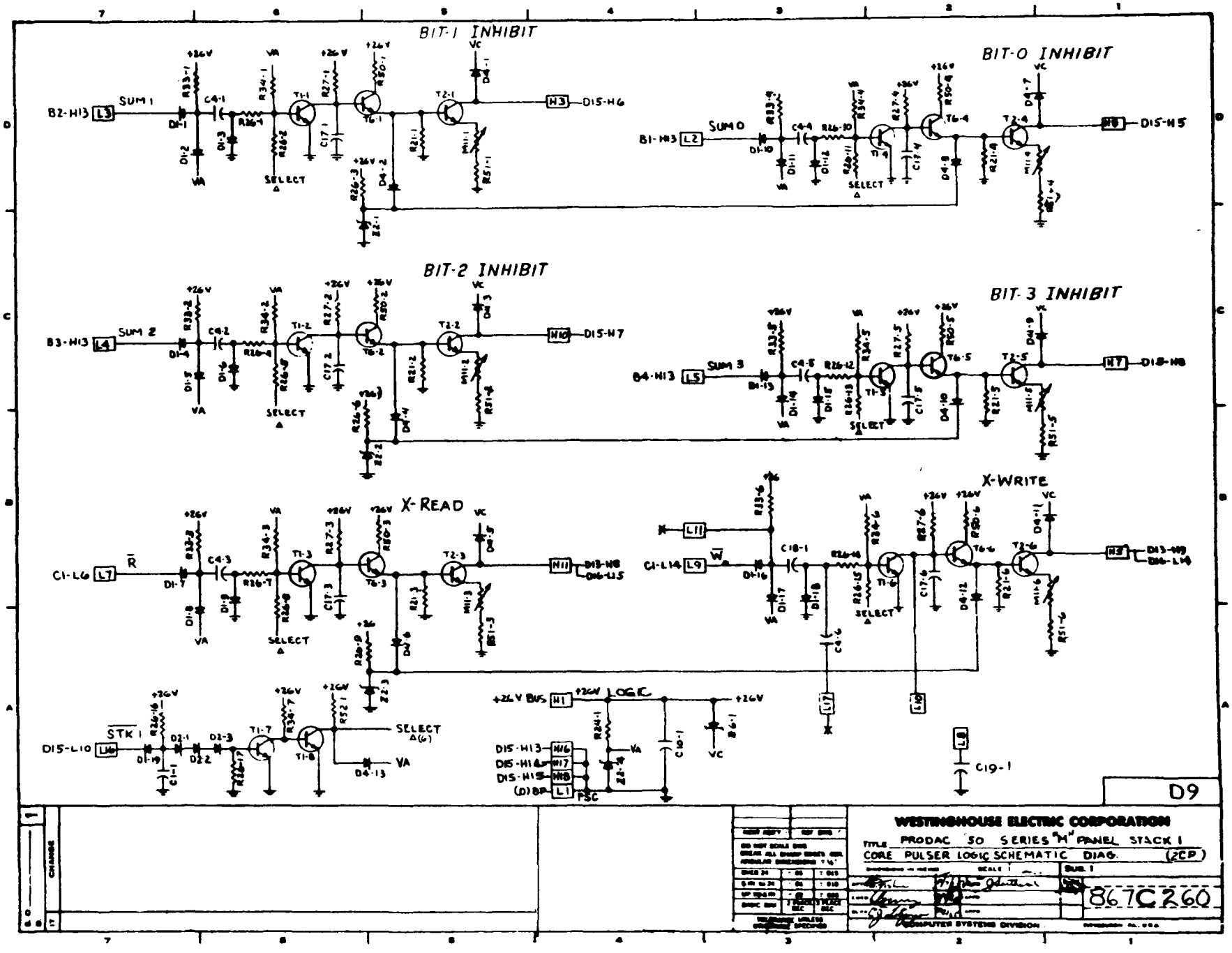
867C256

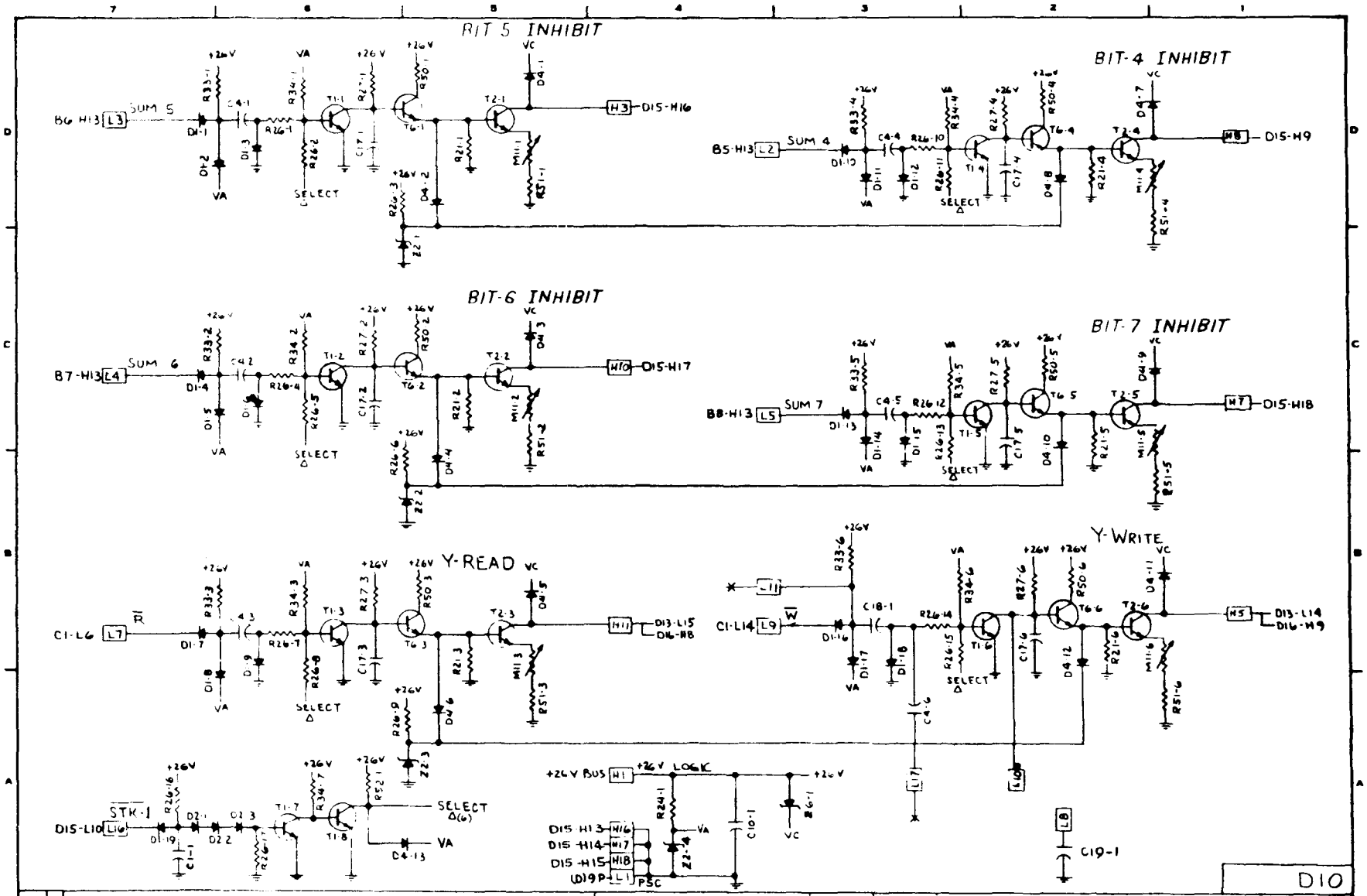
COMPUTER SYSTEMS DIVISION

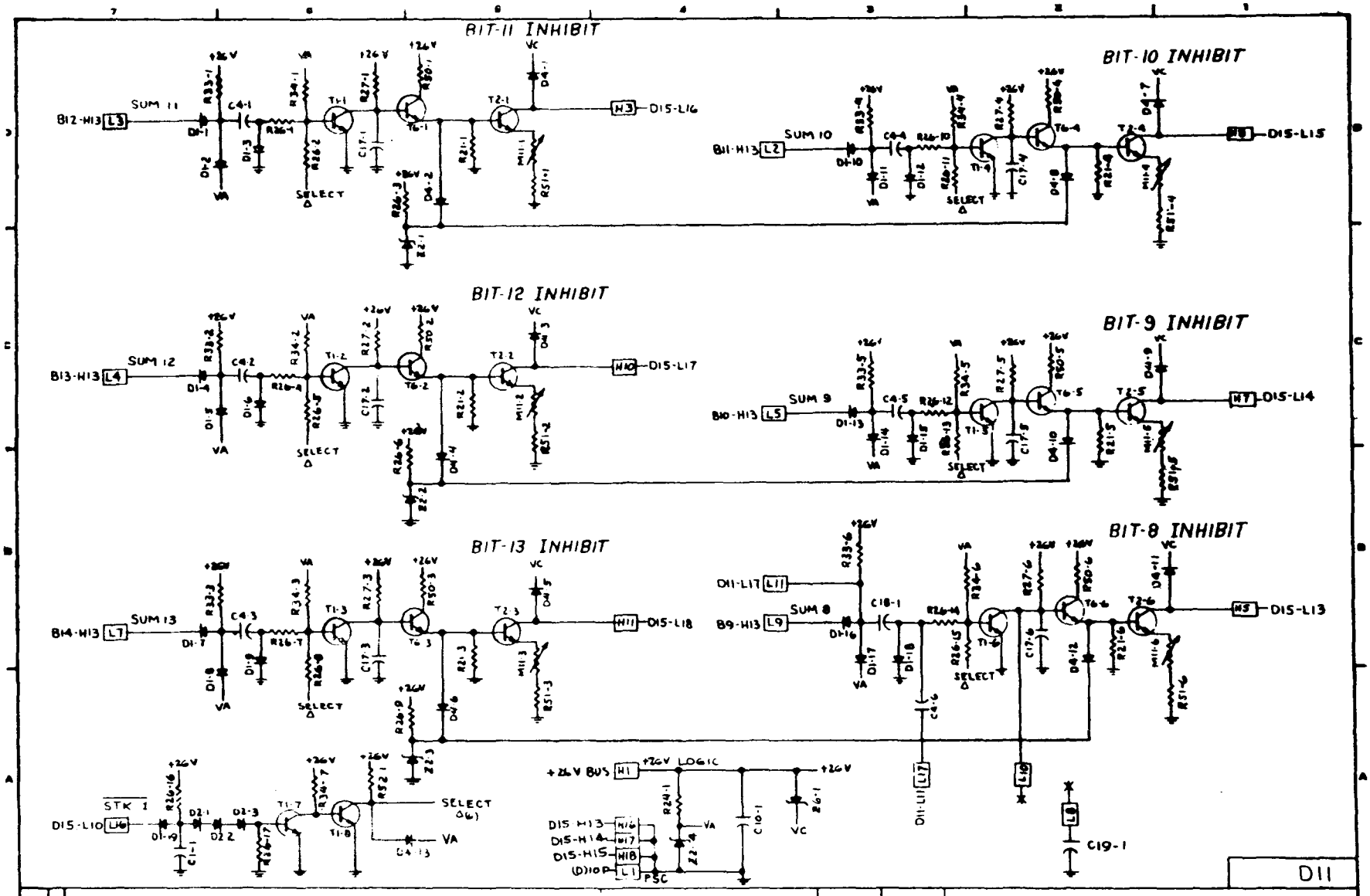

BIT-5 INHIBIT
SUM 5
B6-H13
L3
H3
D3-H16
BIT-4 INHIBIT
SUM 4
B5-H13
L2
H8
D3-H9
BIT-6 INHIBIT
SUM 6
B7-H13
L4
H4
D3-H17
BIT-7 INHIBIT
SUM 7
B8-H13
L5
H7
D3-H18
Y-READ
R
D1-L6
L7
H11
D4-H8
D1-L15
Y-WRITE
W
D1-L14
L9
H5
D4-H9
D1-L14
STK 0
D3-L10
L6
SELECT A(6)
VA
D4-13
+26V BUS
H1
+26V LOGIC
D3-H13
D3-H14
D3-H15
D3-H16
L1
PSC
L8
C19-1
L10
L11
L17
C4-6
D7
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK 0
CORE PULSER LOGIC SCHEMATIC DIAG. (ZCP)
SUB 1
867C258
COMPUTER SYSTEMS DIVISION


BIT-1 INHIBIT
BIT-0 INHIBIT
BIT-2 INHIBIT
BIT-3 INHIBIT
X-READ
X-WRITE
STK 0
SELECT
VA
VC
+26V
+2V BUS
+26V LOGIC
D6
WESTINGHOUSE ELECTRIC CORPORATION
COMPUTER SYSTEMS DIVISION
8677C257


BIT-11 INHIBIT
BIT-10 INHIBIT
BIT-12 INHIBIT
BIT-9 INHIBIT
BIT-13 INHIBIT
BIT-8 INHIBIT
SUM 11
SUM 10
SUM 12
SUM 9
SUM 13
SUM 8
B12-H13 L3
B11-H13 L2
B13-H13 L4
B10-H13 L5
B14-H13 L7
B9-H13 L9
D8-L11 L11
H3 D3-L16
H8 D3-L15
H10 D3-L17
H7 D3-L14
H11 D3-L18
H5 D3-L13
+26V
VA
VC
SELECT
STK 0
D3-L10 L16
SELECT Δ(6)
D4-13
+26V BUS H1
+26V LOGIC
+20V
D3-H13 H16
D3-H14 H17
D3-H15 H18
(D)TP L1
PSC
D8
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES "M" PANEL STACK 0
CORE PULSER LOGIC SCHEMATIC DIAG (2CP)
SCALE 1
SUB 1
867C259
COMPUTER SYSTEMS DIVISION


BIT-1 INHIBIT
BIT-0 INHIBIT
BIT-2 INHIBIT
BIT-3 INHIBIT
X-READ
X-WRITE
SUM 1
SUM 0
SUM 2
SUM 3
SELECT
STK 1
LOGIC
+26V BUS
D9
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "H" PANEL STACK 1
CORE PULSER LOGIC SCHEMATIC DIAG. (2CP)
COMPUTER SYSTEMS DIVISION
867C260


BIT 5 INHIBIT
BIT-4 INHIBIT
BIT-6 INHIBIT
BIT-7 INHIBIT
Y-READ
Y-WRITE
SUM 5
SUM 4
SUM 6
SUM 7
SELECT
B6-H13 L3
B5-H13 L2
B7-H13 L4
B8-H13 L5
D15-H16
D15-H9
D15-H17
D15-H18
D13-L15
D16-R8
D13-L14
D16-H9
C1-L6 L7
C1-L14 L9
STK-1
D15-L10 L16
+24V BUS H1
+24V LOGIC
D15-H13 H16
D15-H14 H17
D15-H15 H18
D19P-L1
PSC
C19-1
D10
867C261
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK 1
CORE PULSER LOGIC SCHEMATIC DIAG (2CP)
COMPUTER SYSTEMS DIVISION



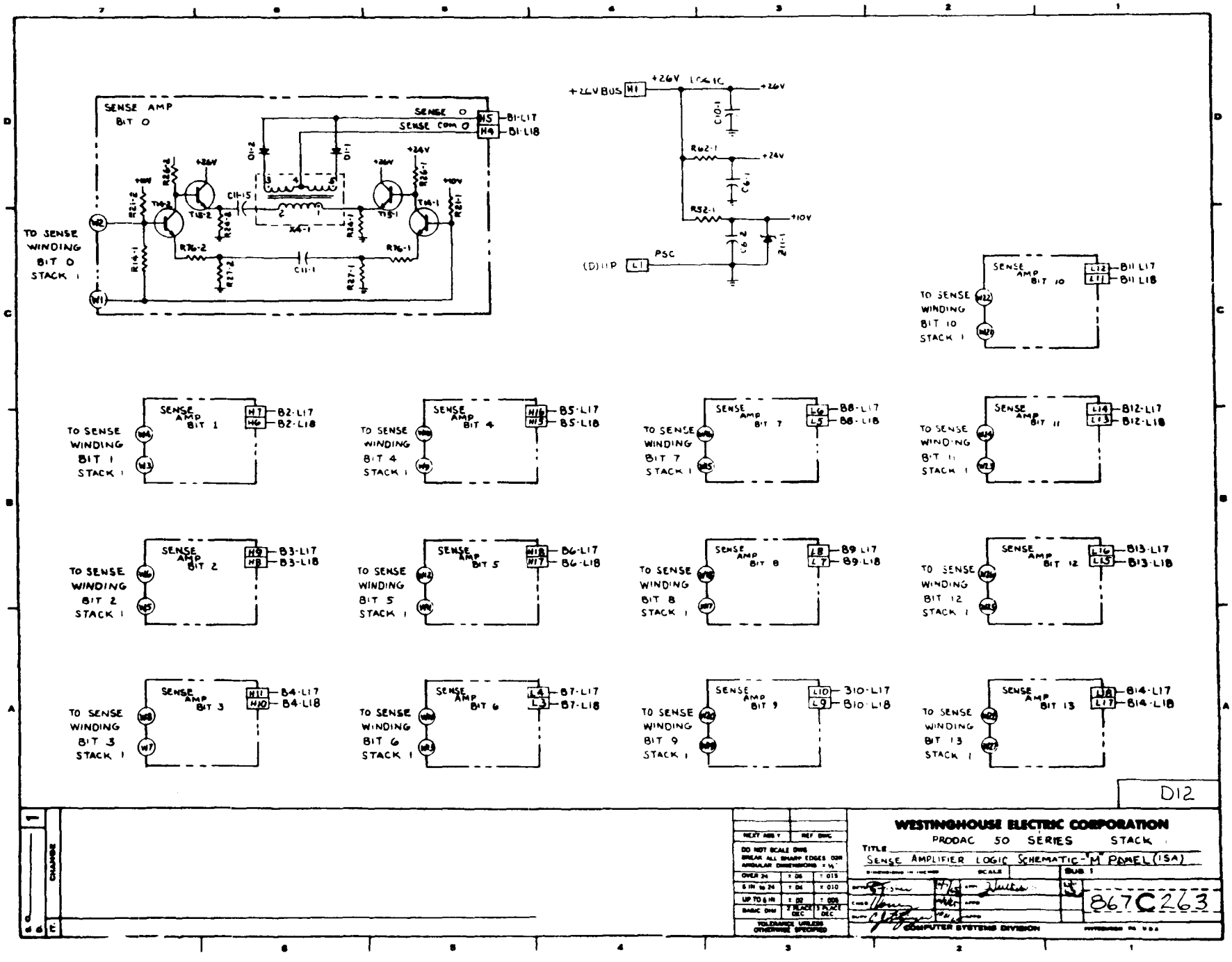
WESTINGHOUSE ELECTRIC CORPORATION

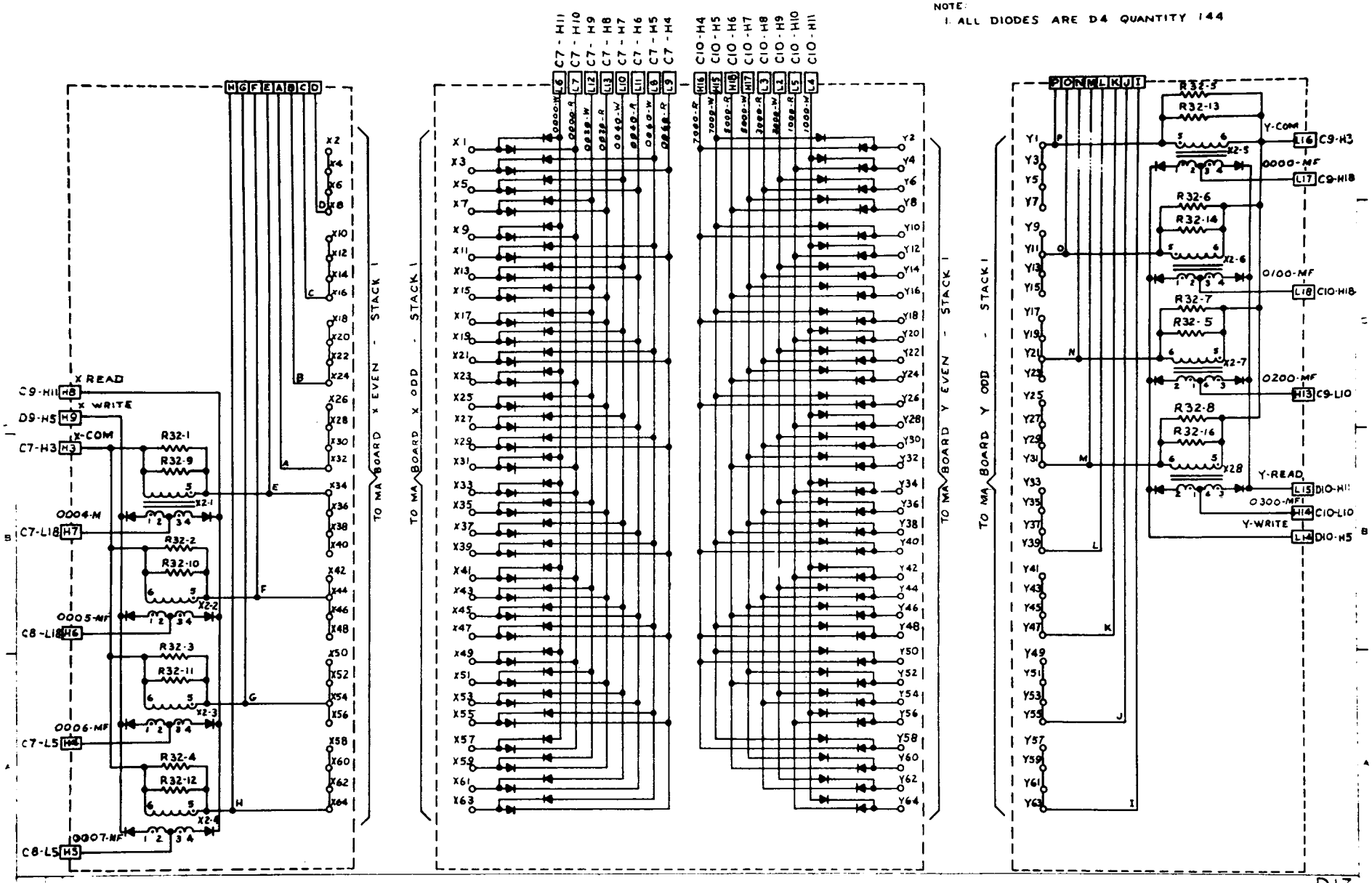
PRODAC 50 SERIES "M" PANEL STACK 1

CORE PULSER LOGIC SCHEMATIC DIAG. (2CP)

COMPUTER SYSTEMS DIVISION

867C262

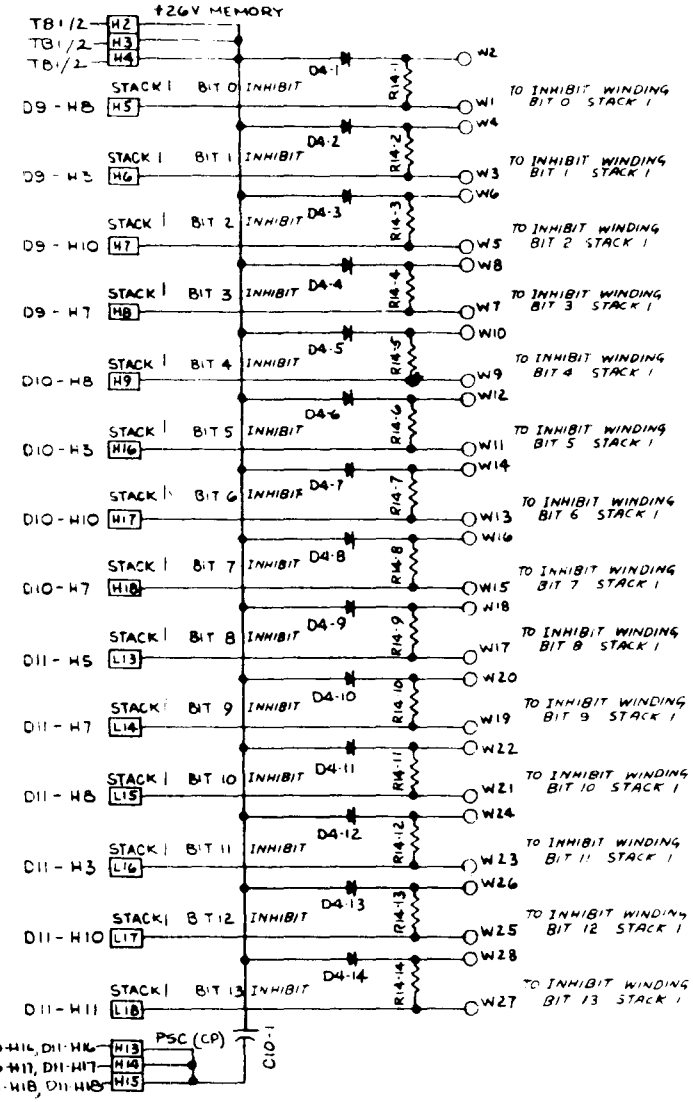

SENSE AMP BIT 0
SENSE 0
SENSE COM 0
B1-L17
B1-L18
TO SENSE WINDING BIT 0 STACK 1
+26V BUS
+26V LOGIC
PSC
SENSE AMP BIT 10
B11 L17
B11 L18
TO SENSE WINDING BIT 10 STACK 1
SENSE AMP BIT 1
B2-L17
B2-L18
TO SENSE WINDING BIT 1 STACK 1
SENSE AMP BIT 4
B5-L17
B5-L18
TO SENSE WINDING BIT 4 STACK 1
SENSE AMP BIT 7
B8-L17
B8-L18
TO SENSE WINDING BIT 7 STACK 1
SENSE AMP BIT 11
B12-L17
B12-L18
TO SENSE WINDING BIT 11 STACK 1
SENSE AMP BIT 2
B3-L17
B3-L18
TO SENSE WINDING BIT 2 STACK 1
SENSE AMP BIT 5
B6-L17
B6-L18
TO SENSE WINDING BIT 5 STACK 1
SENSE AMP BIT 8
B9 L17
B9-L18
TO SENSE WINDING BIT 8 STACK 1
SENSE AMP BIT 12
B13-L17
B13-L18
TO SENSE WINDING BIT 12 STACK 1
SENSE AMP BIT 3
B4-L17
B4-L18
TO SENSE WINDING BIT 3 STACK 1
SENSE AMP BIT 6
B7-L17
B7-L18
TO SENSE WINDING BIT 6 STACK 1
SENSE AMP BIT 9
B10-L17
B10-L18
TO SENSE WINDING BIT 9 STACK 1
SENSE AMP BIT 13
B14-L17
B14-L18
TO SENSE WINDING BIT 13 STACK 1
D12
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES STACK 1
TITLE SENSE AMPLIFIER LOGIC SCHEMATIC-'M' PANEL (ISA)
SUB 1
867C263
COMPUTER SYSTEMS DIVISION

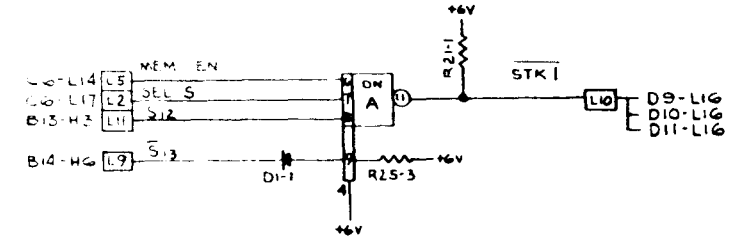


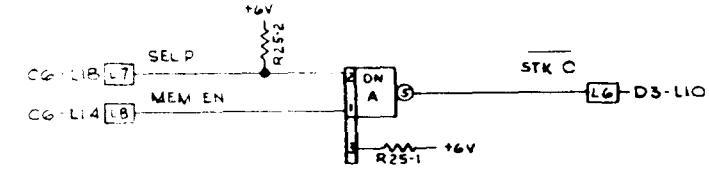
WESTINGHOUSE ELECTRIC CORPORATION D13

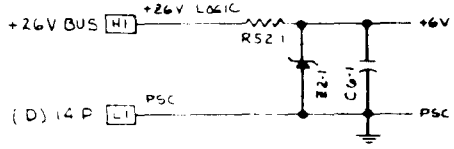
TITLE PRODAC "50" SERIES "M" PANEL STACK 1
MEMORY DIODE LOGIC SCHEMATIC (2MB)

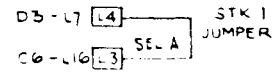
867C264









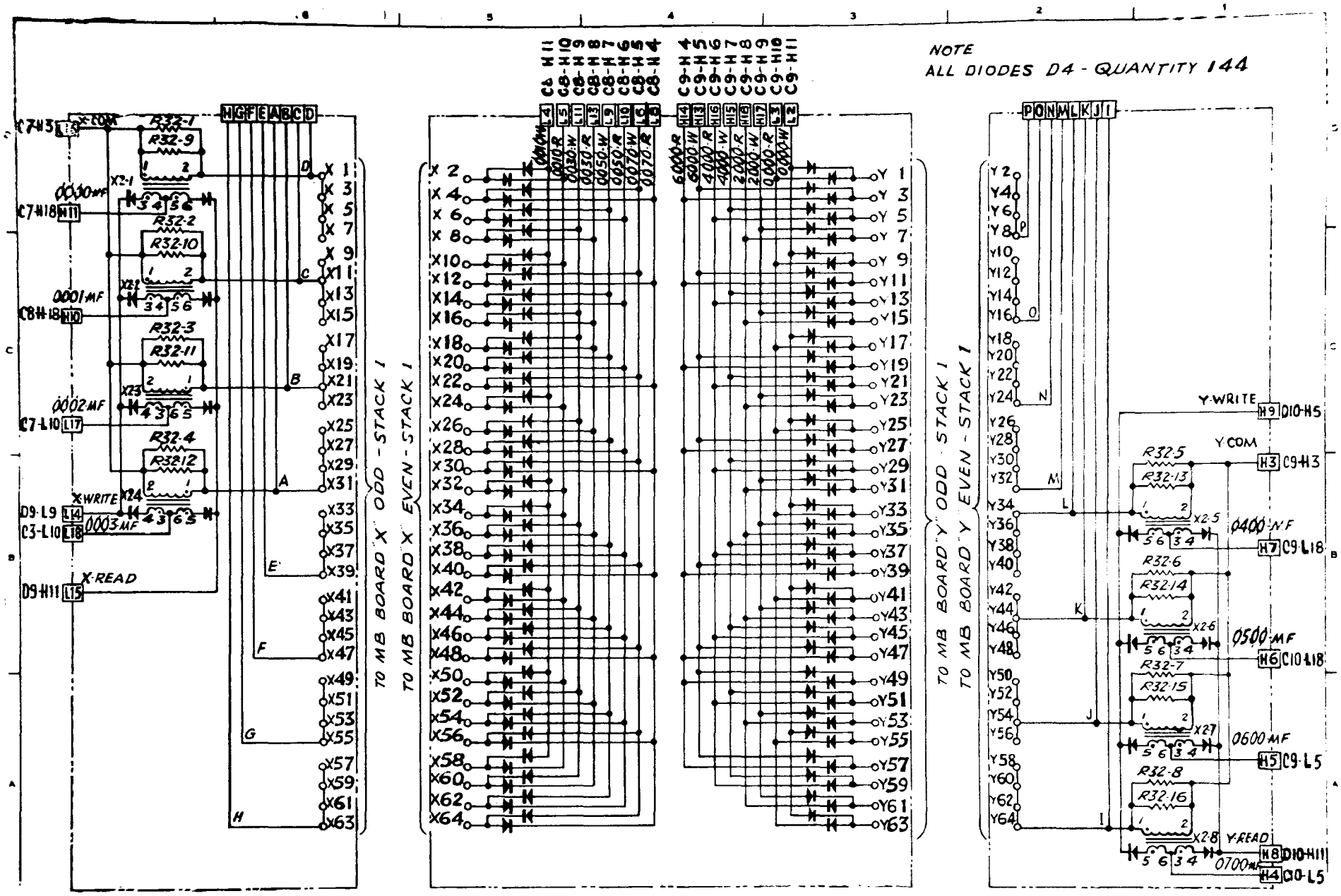


NOTES:
1 PIN 10 OF DUAL NAND TO (L1) GND
2 SYMBOL FOR LOGICAL DUAL NAND REF. 743A408

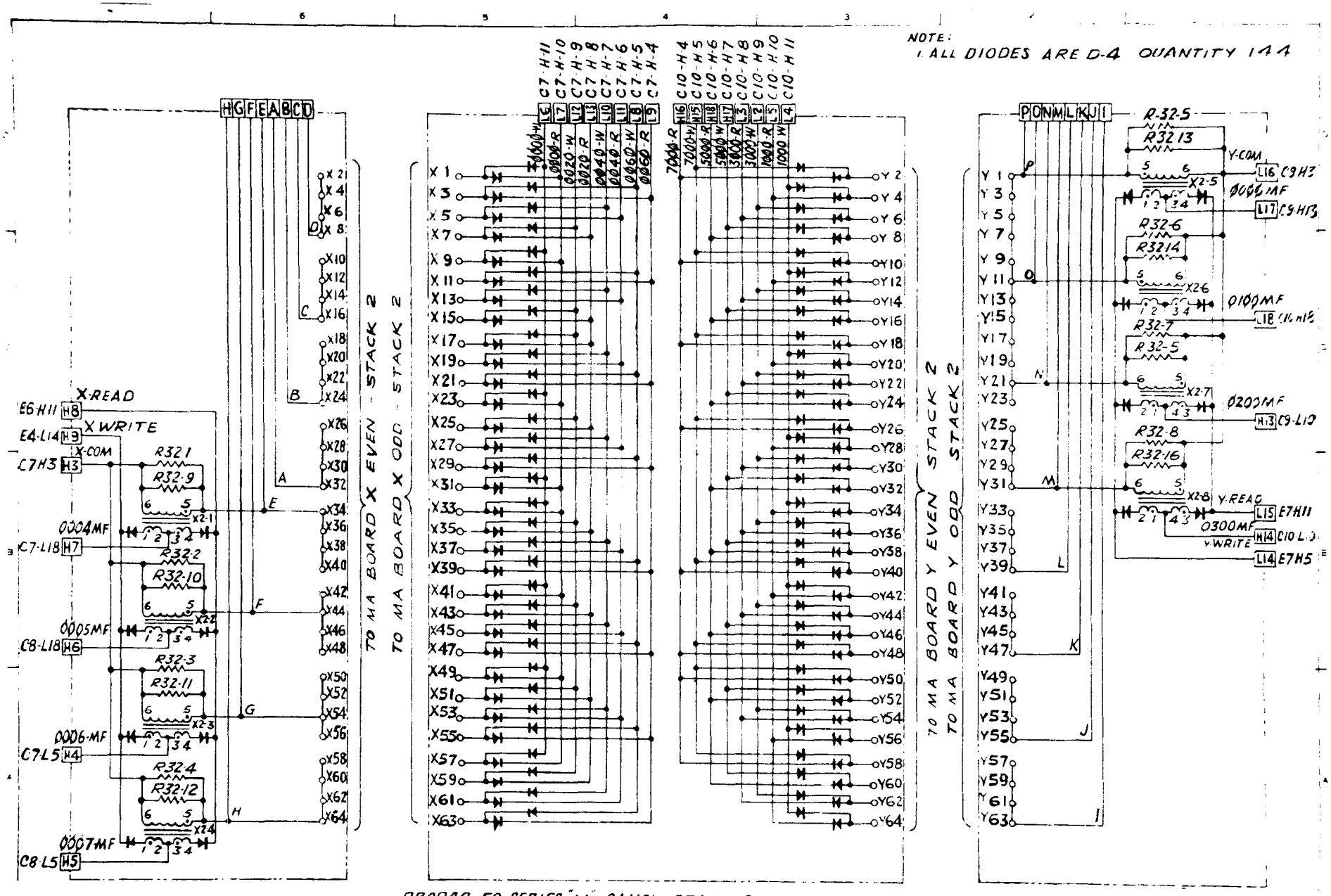
D15

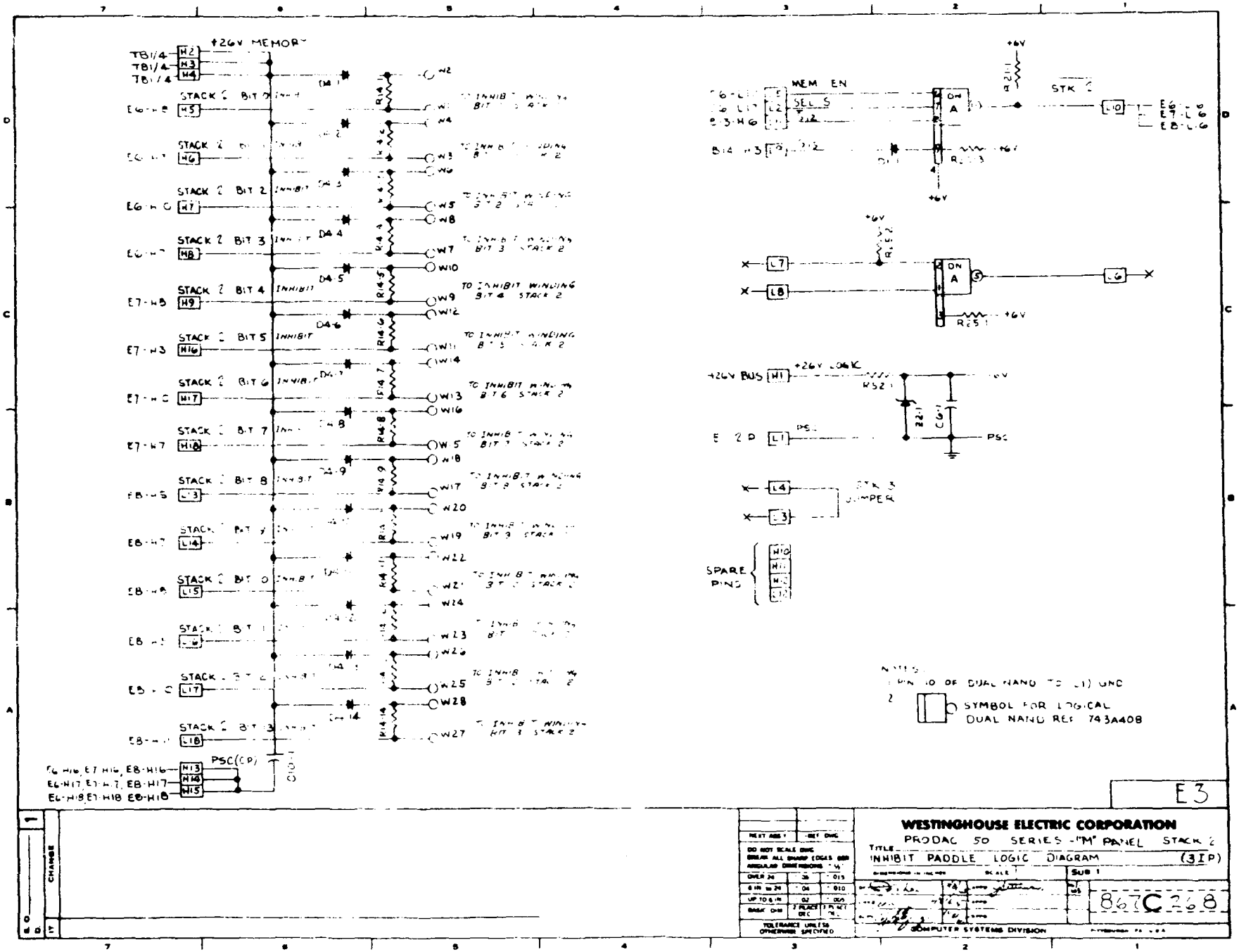
1	CHANGE	

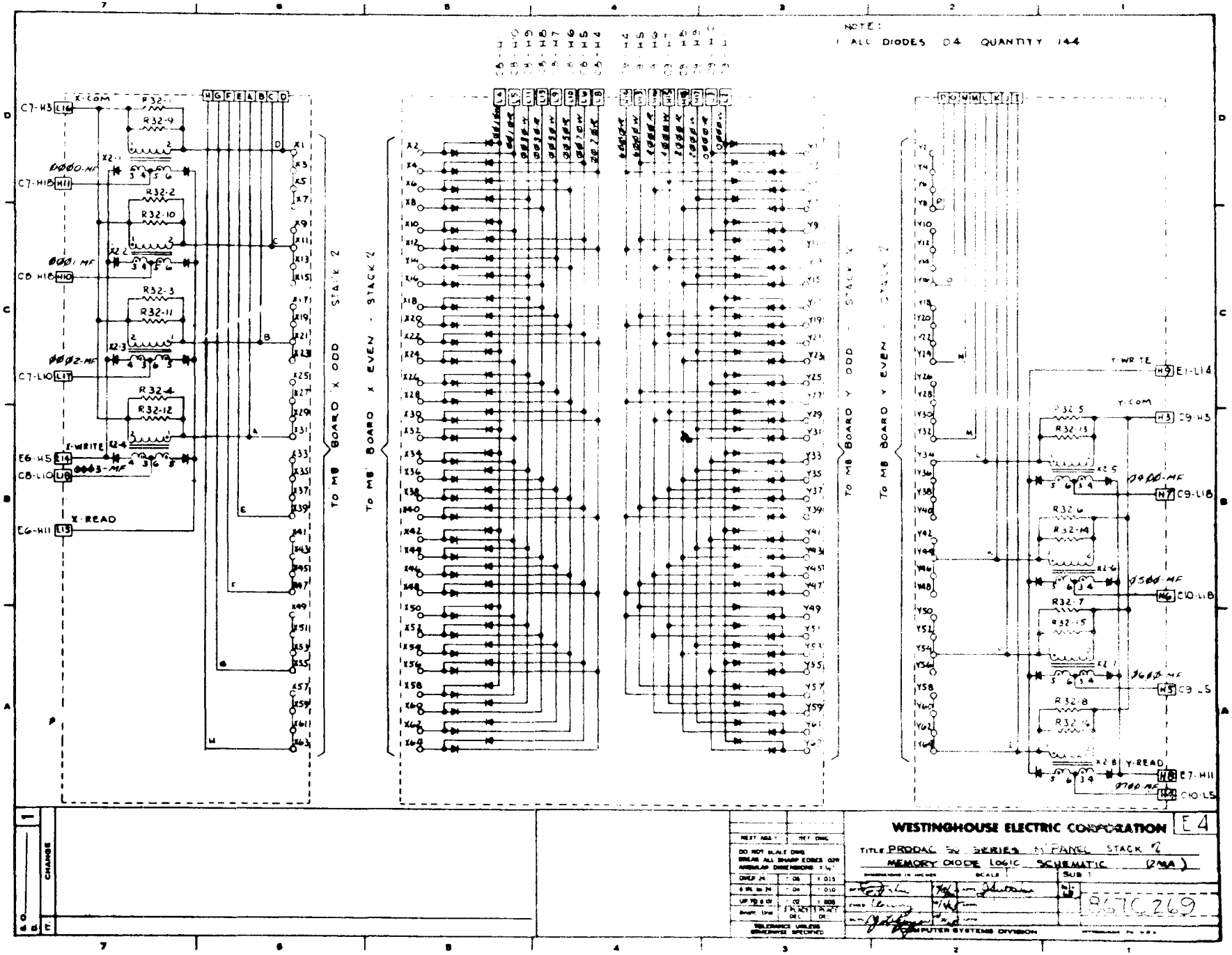
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK 1
TITLE INHIBIT PADDLE LOGIC DIAGRAM (3IP)
SUB 1
867C265
COMPUTER SYSTEMS DIVISION



PRODAC 50 SERIES "M" PANEL - STACK 1
MEMORY DIODE LOGIC SCHEMATIC (2 MA)
Reference Drawing 867C266 D16


NOTE:
1 ALL DIODES ARE D-4 QUANTITY 144
X-READ
X WRITE
X-COM
R32-1
R32-9
R32-2
R32-10
R32-3
R32-11
R32-4
R32-12
0004MF
0005MF
0006MF
0007MF
C7H3
C7L18
C8L18
C7L5
C8L5
E6H11
E4L14
TO MA BOARD X EVEN - STACK 2
TO MA BOARD X ODD - STACK 2
TO MA BOARD Y EVEN STACK 2
TO MA BOARD Y ODD STACK 2
R32-5
R32 13
R32-6
R32 14
R32-7
R32-5
R32-8
R32-16
Y-COM
0100MF
0200MF
0300MF
Y-READ
Y-WRITE
PRODAC 50 SERIES "M" PANEL - STACK 2
MEMORY DIODE LOGIC SCHEMATIC (2 MB)
REFERENCE 867 C 267 E 1


+26V MEMORY
MEM EN
SEL S
STK 2
+6V
PSC
+26V BUS
SPARE PINS
STK 3 JUMPER
SYMBOL FOR LOGICAL DUAL NAND REF 743A408
E3
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK 2
INHIBIT PADDLE LOGIC DIAGRAM (3IP)
COMPUTER SYSTEMS DIVISION
867C268



1	CHANGE				

WESTINGHOUSE ELECTRIC CORPORATION

E4

TITLE PRODAC 50 SERIES M PANEL STACK 2

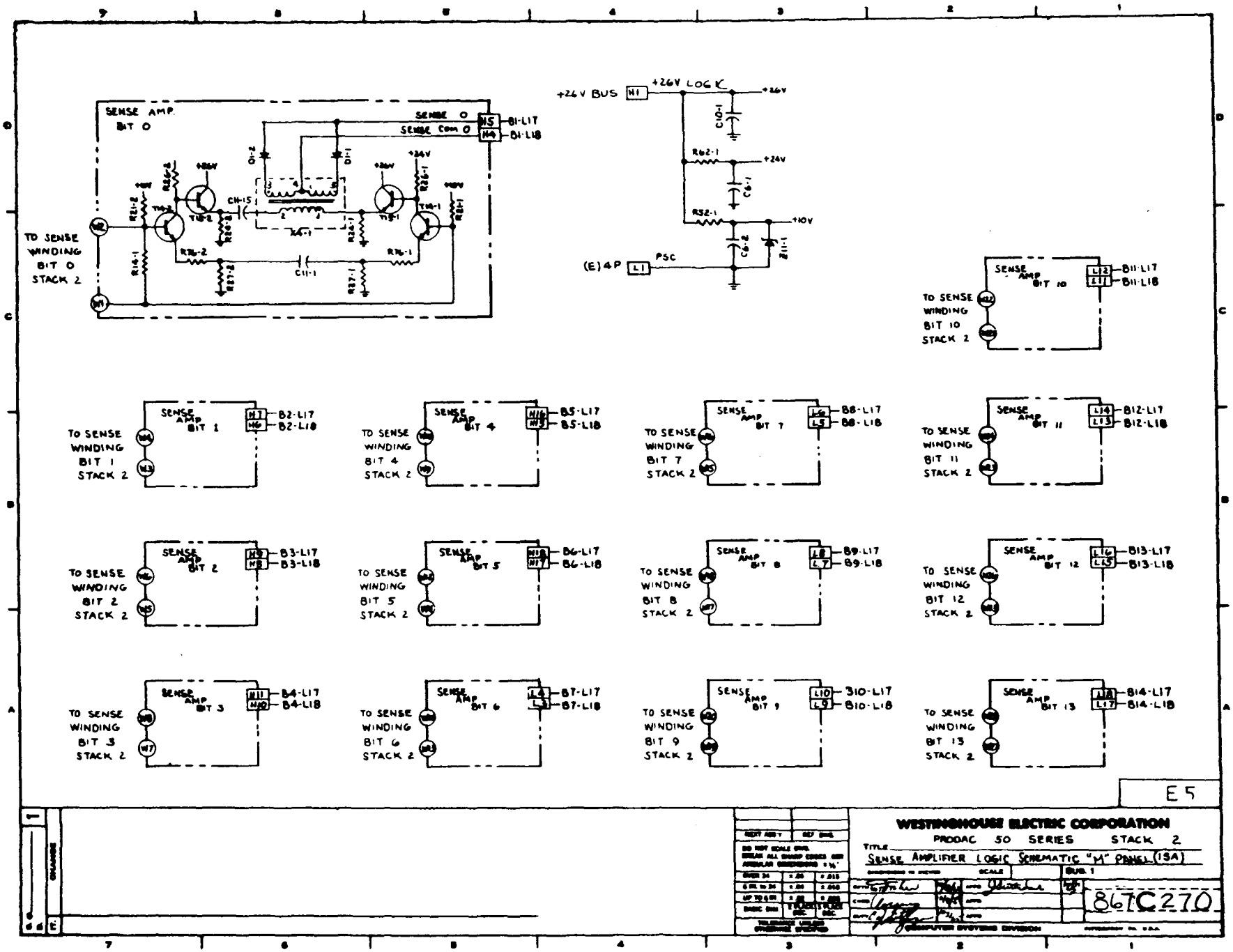
MEMORY DIODE LOGIC SCHEMATIC (2MA)

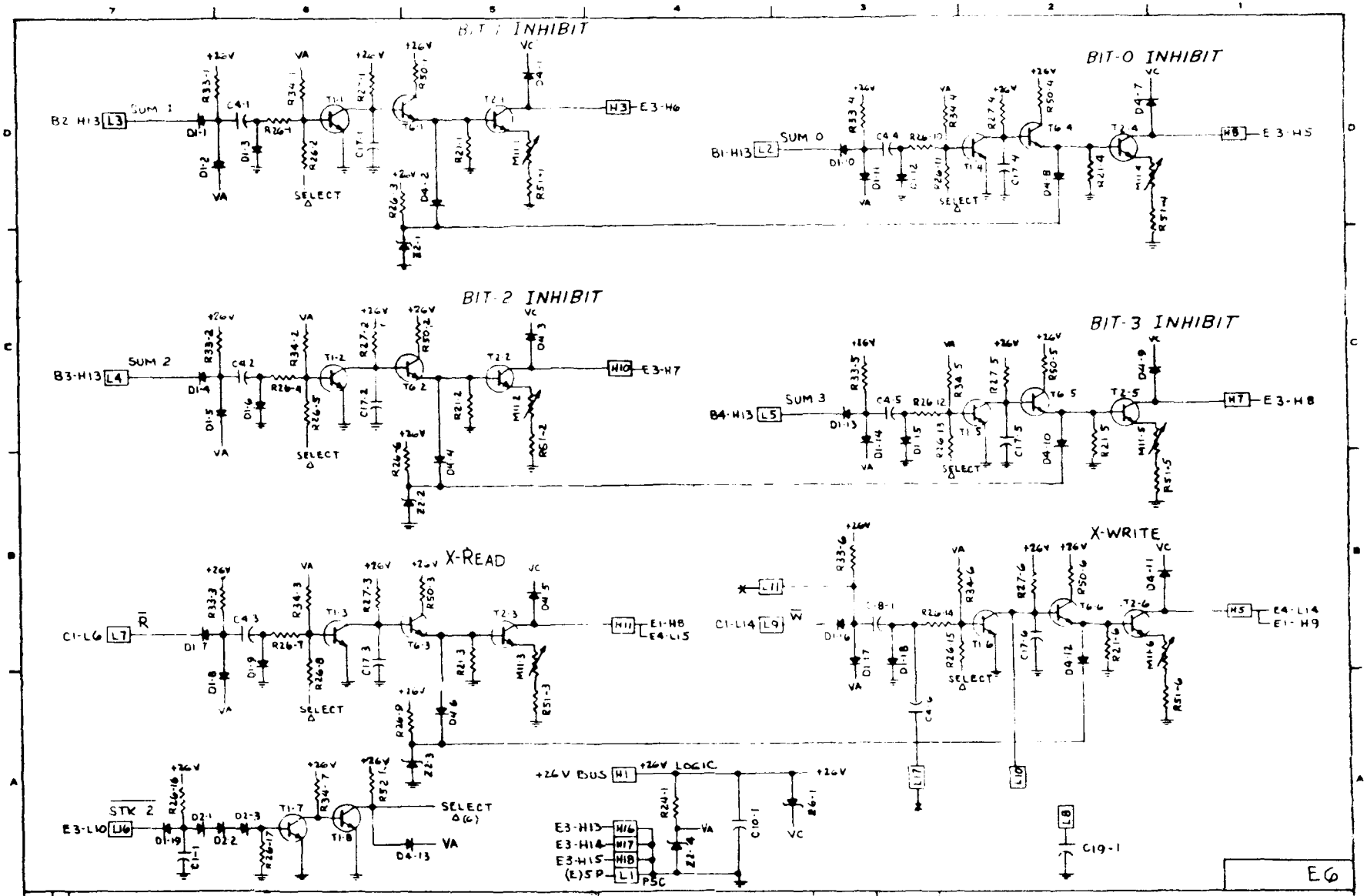
SCALE

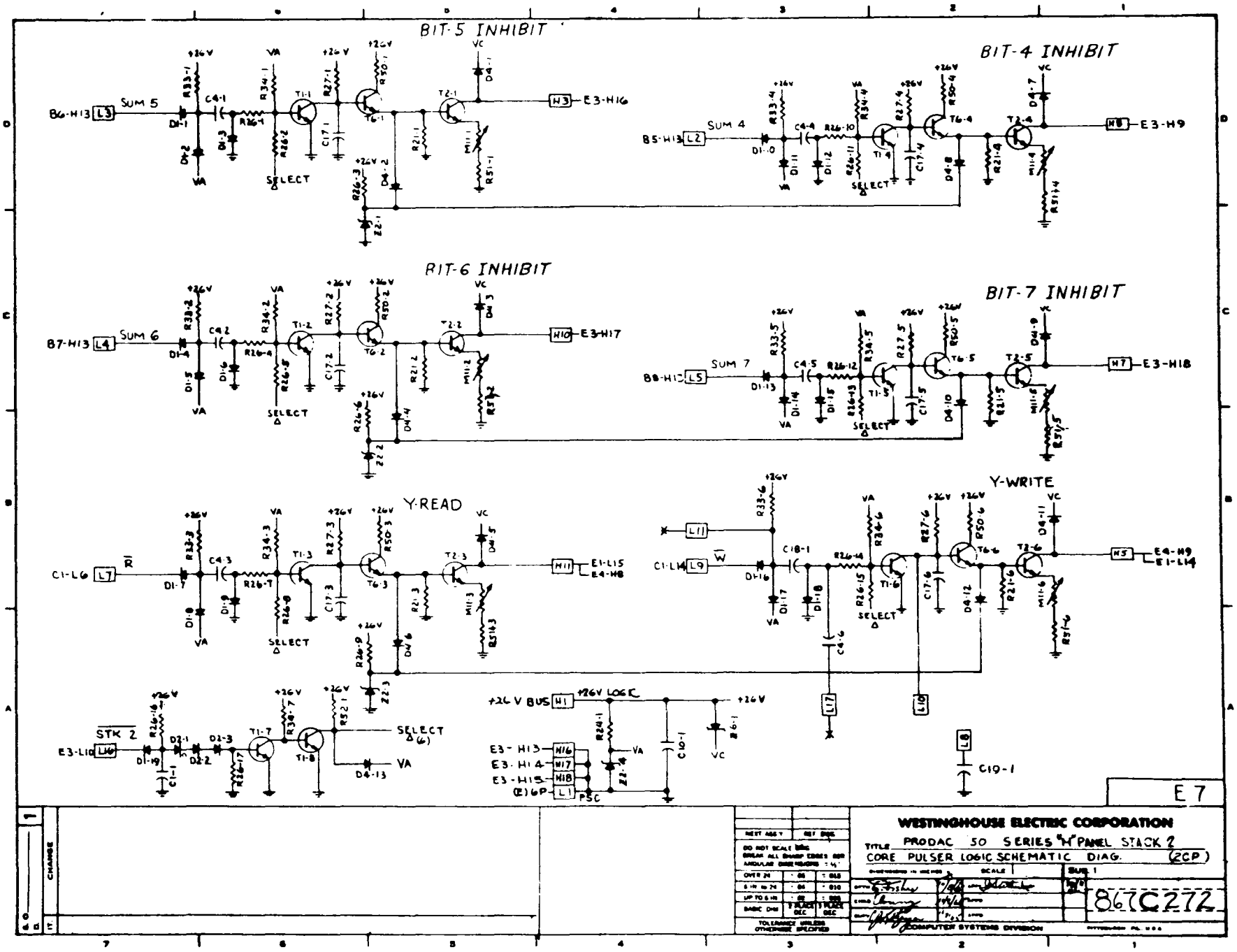
SUB 1

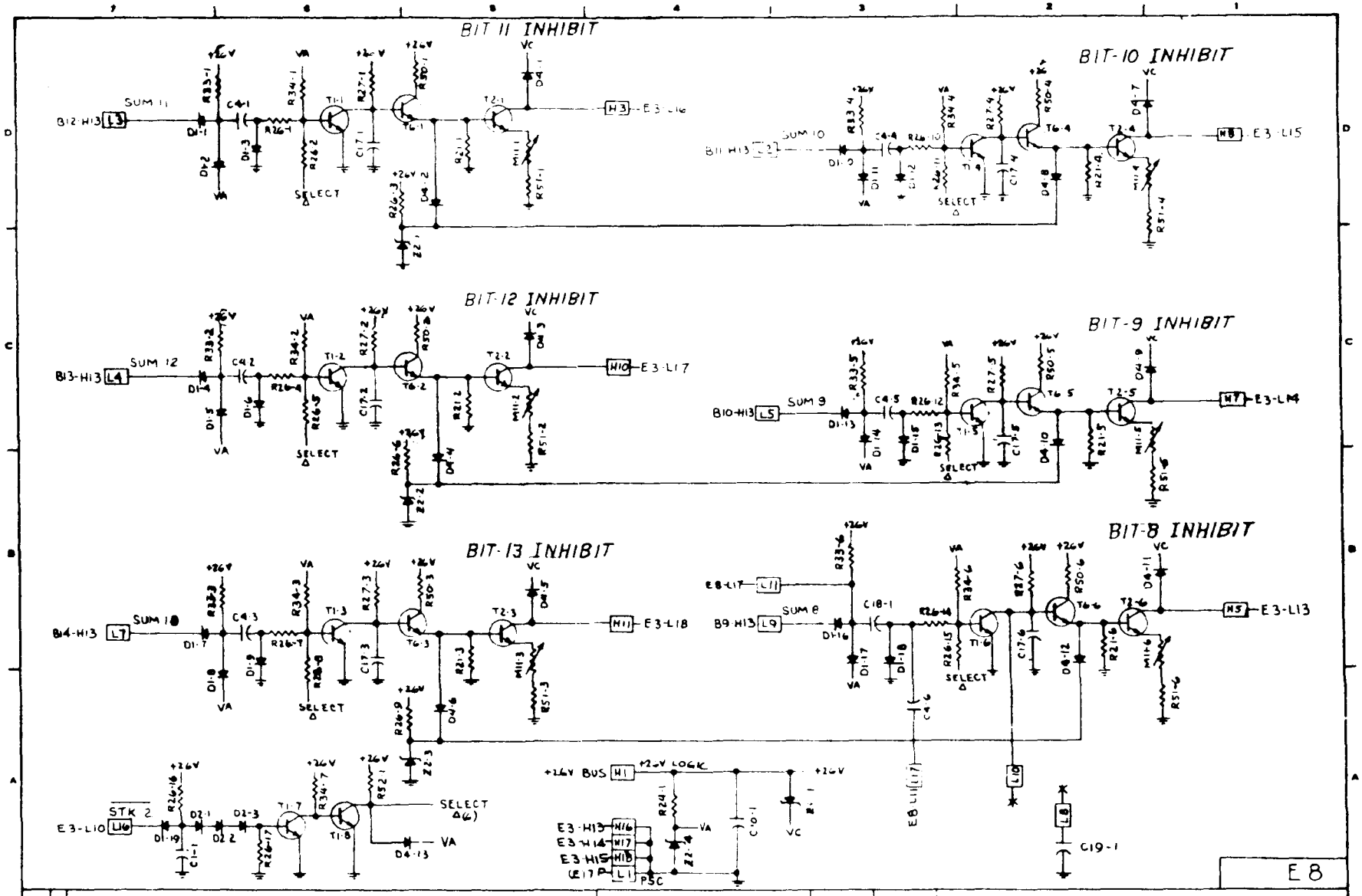
COMPUTER SYSTEMS DIVISION

8670269


SENSE AMP BIT 0
SENSE 0
SENSE COM 0
B1-L17
B1-L18
TO SENSE WINDING BIT 0 STACK 2
+24V BUS
+24V LOGIC
(E)4P
PSC
+10V
SENSE AMP BIT 10
B11-L17
B11-L18
TO SENSE WINDING BIT 10 STACK 2
SENSE AMP BIT 1
B2-L17
B2-L18
TO SENSE WINDING BIT 1 STACK 2
SENSE AMP BIT 4
B5-L17
B5-L18
TO SENSE WINDING BIT 4 STACK 2
SENSE AMP BIT 7
B8-L17
B8-L18
TO SENSE WINDING BIT 7 STACK 2
SENSE AMP BIT 11
B12-L17
B12-L18
TO SENSE WINDING BIT 11 STACK 2
SENSE AMP BIT 2
B3-L17
B3-L18
TO SENSE WINDING BIT 2 STACK 2
SENSE AMP BIT 5
B6-L17
B6-L18
TO SENSE WINDING BIT 5 STACK 2
SENSE AMP BIT 8
B9-L17
B9-L18
TO SENSE WINDING BIT 8 STACK 2
SENSE AMP BIT 12
B13-L17
B13-L18
TO SENSE WINDING BIT 12 STACK 2
SENSE AMP BIT 3
B4-L17
B4-L18
TO SENSE WINDING BIT 3 STACK 2
SENSE AMP BIT 6
B7-L17
B7-L18
TO SENSE WINDING BIT 6 STACK 2
SENSE AMP BIT 9
B10-L17
B10-L18
TO SENSE WINDING BIT 9 STACK 2
SENSE AMP BIT 13
B14-L17
B14-L18
TO SENSE WINDING BIT 13 STACK 2
E5
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES STACK 2
SENSE AMPLIFIER LOGIC SCHEMATIC "M" PANEL (ISA)
86C270


BIT 1 INHIBIT
BIT-0 INHIBIT
BIT-2 INHIBIT
BIT-3 INHIBIT
X-READ
X-WRITE
STK 2
+26V BUS
+26V LOGIC
SELECT
SUM 1
SUM 0
SUM 2
SUM 3
B2 H13
B1-H13
B3-H13
B4-H13
C1-L6
C1-L14
E3-L10
E3-H13
E3-H14
E3-H15
(E)5P
PSC
VA
VC
E6
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK C
CORE PULSER LOGIC SCHEMATIC DIAG. (2CP)
867C271


BIT-5 INHIBIT
BIT-4 INHIBIT
BIT-6 INHIBIT
BIT-7 INHIBIT
Y-READ
Y-WRITE
SUM 5
SUM 4
SUM 6
SUM 7
SELECT
B6-H13 L3
B5-H13 L2
B7-H13 L4
B8-H13 L5
C1-L6 L7
C1-L14 L9
E3-L10 L16
+26V BUS H1
+26V LOGIC
E3-H13 H16
E3-H14 H17
E3-H15 H18
(E)6P L1
PSC
E3-H16
E3-H9
E3-H17
E3-H18
E1-L15
E4-H8
E4-H9
E1-L14
STR 2
E7
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "H" PANEL STACK 2
CORE PULSER LOGIC SCHEMATIC DIAG. (2CP)
COMPUTER SYSTEMS DIVISION
867C272



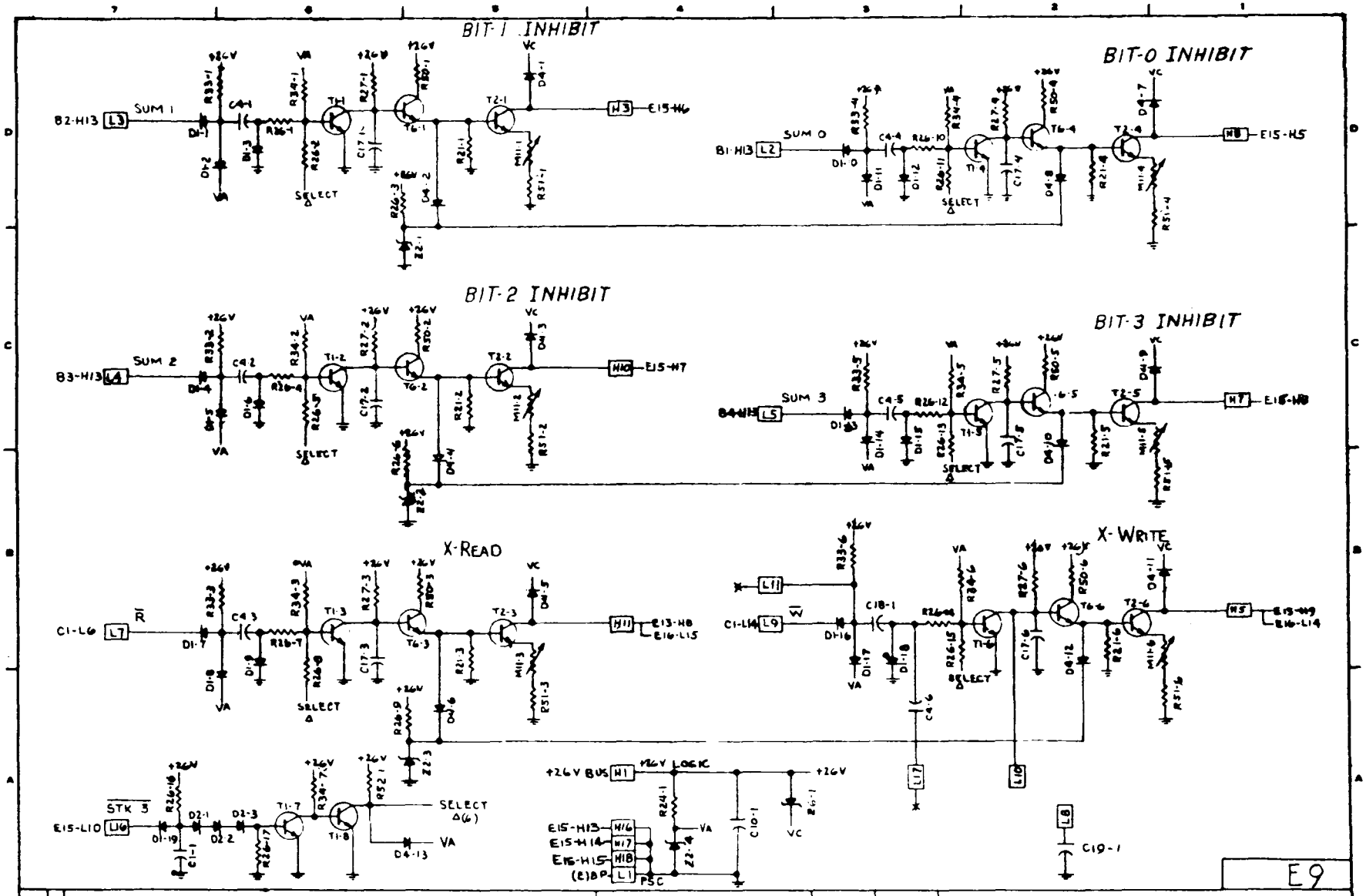
WESTINGHOUSE ELECTRIC CORPORATION

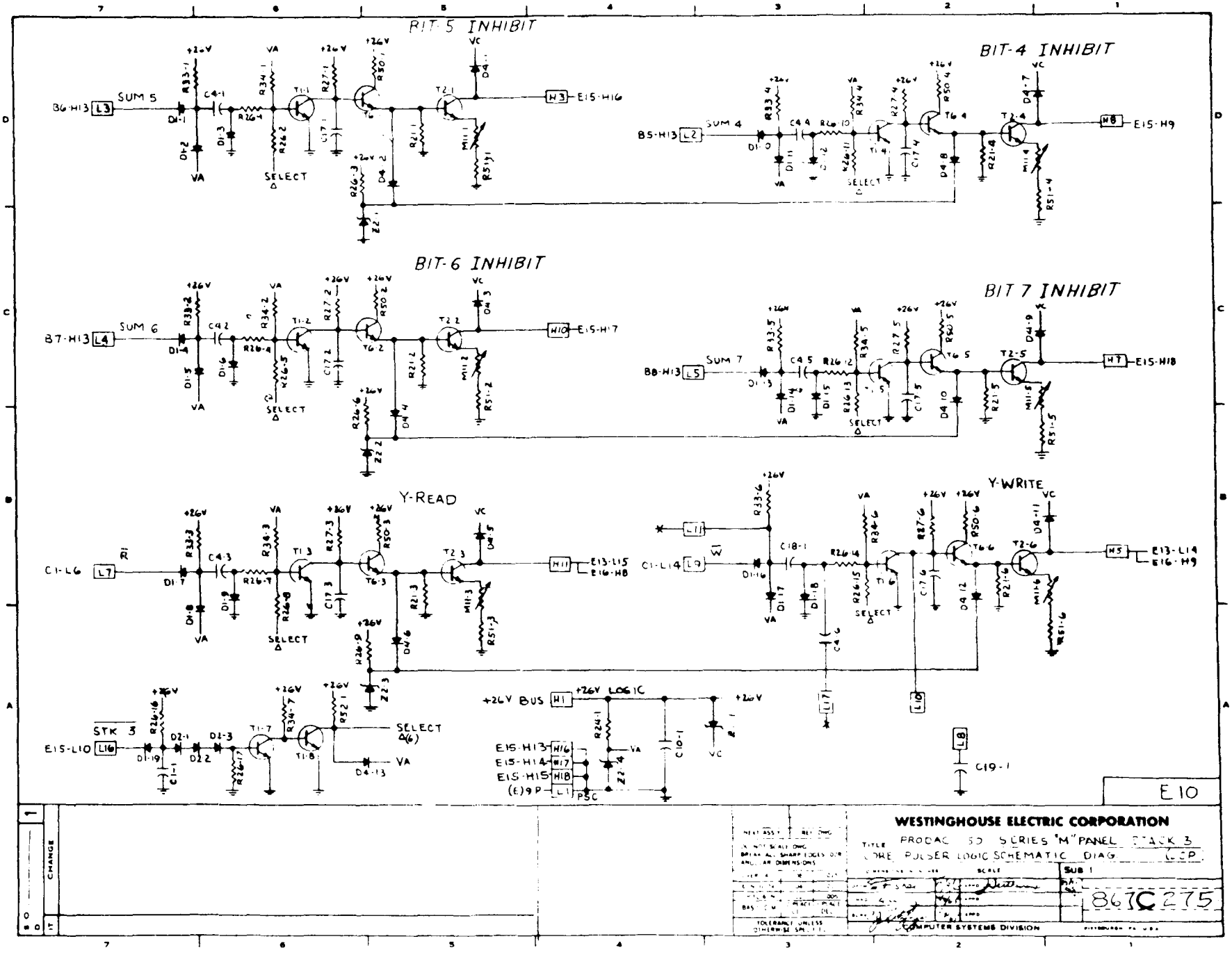
PRODAC 50 SERIES 'M' PANEL STACK 2

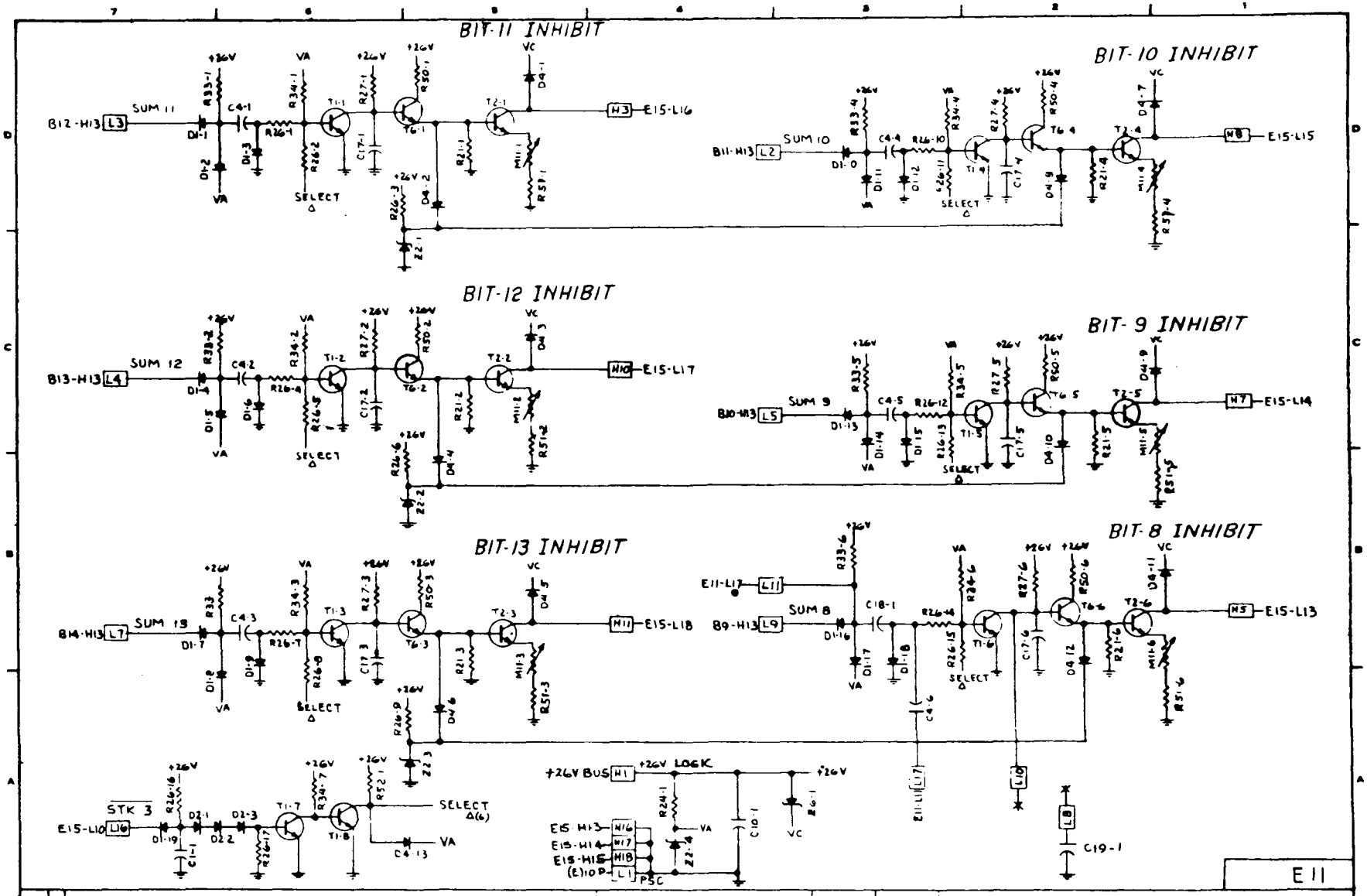
TITLE CORE PULSER LOGIC SCHEMATIC DIAG (2CP)

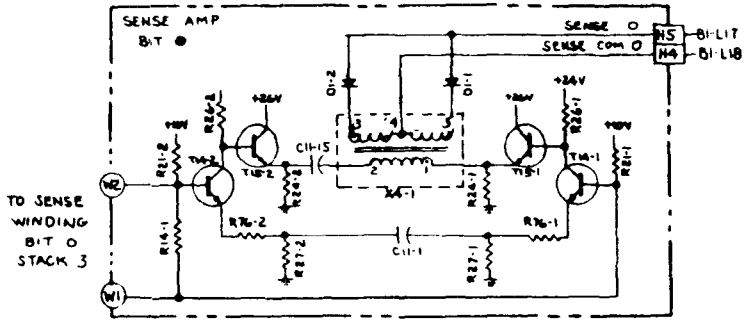
COMPUTER SYSTEMS DIVISION

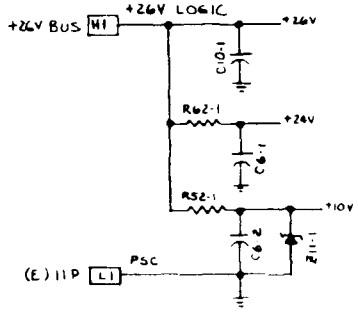
867C273

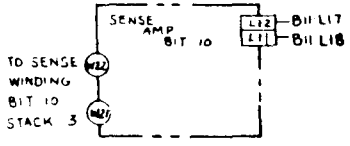

BIT-1 INHIBIT
BIT-0 INHIBIT
BIT-2 INHIBIT
BIT-3 INHIBIT
X-READ
X-WRITE
SUM 1
SUM 0
SUM 2
SUM 3
SELECT
B2-H13
B1-H13
B3-H13
B4-H13
C1-L6
C1-L14
E15-L10
+26V BUS
+26V LOGIC
E15-H13
E15-H14
E15-H15
(E)BP
PSC
VA
VC
E9
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50 SERIES "M" PANEL STACK 3
CORE PULSER LOGIC SCHEMATIC DIAG. (2CP)
COMPUTER SYSTEMS DIVISION
867C274

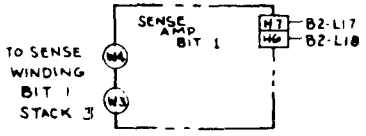

BIT-5 INHIBIT
BIT-4 INHIBIT
BIT-6 INHIBIT
BIT 7 INHIBIT
Y-READ
Y-WRITE
SUM 5
SUM 4
SUM 6
SUM 7
SELECT
+26V BUS
+26V LOGIC
E10
WESTINGHOUSE ELECTRIC CORPORATION
COMPUTER SYSTEMS DIVISION
8677C275

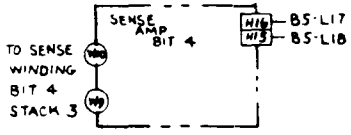

BIT-11 INHIBIT
BIT-10 INHIBIT
BIT-12 INHIBIT
BIT-9 INHIBIT
BIT-13 INHIBIT
BIT-8 INHIBIT
SUM 11
SUM 10
SUM 12
SUM 9
SUM 13
SUM 8
SELECT
VA
VC
+26V
+26V BUS
+26V LOGIC
STK 3
SELECT Δ(6)
PSC
E11
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "M" PANEL STACK 3
CORE PULSER LOGIC SCHEMATIC DIAG. (2CP)
COMPUTER SYSTEMS DIVISION
867C276

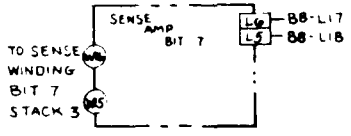


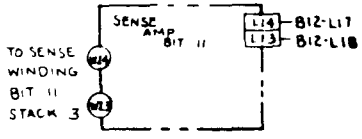


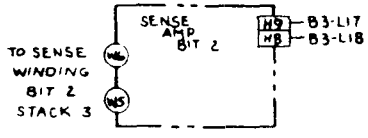


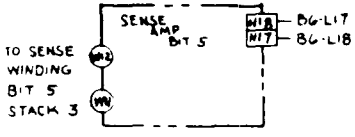


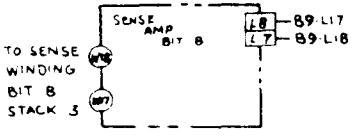


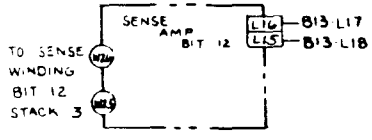


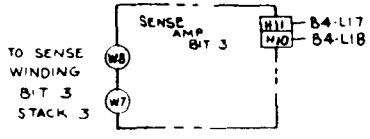


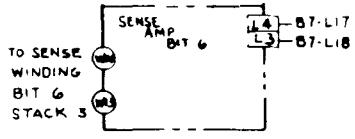


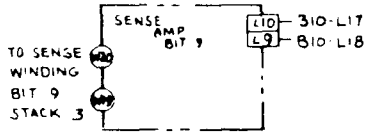


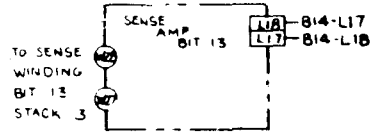












E12

NO.	CHANGE	DATE
1		

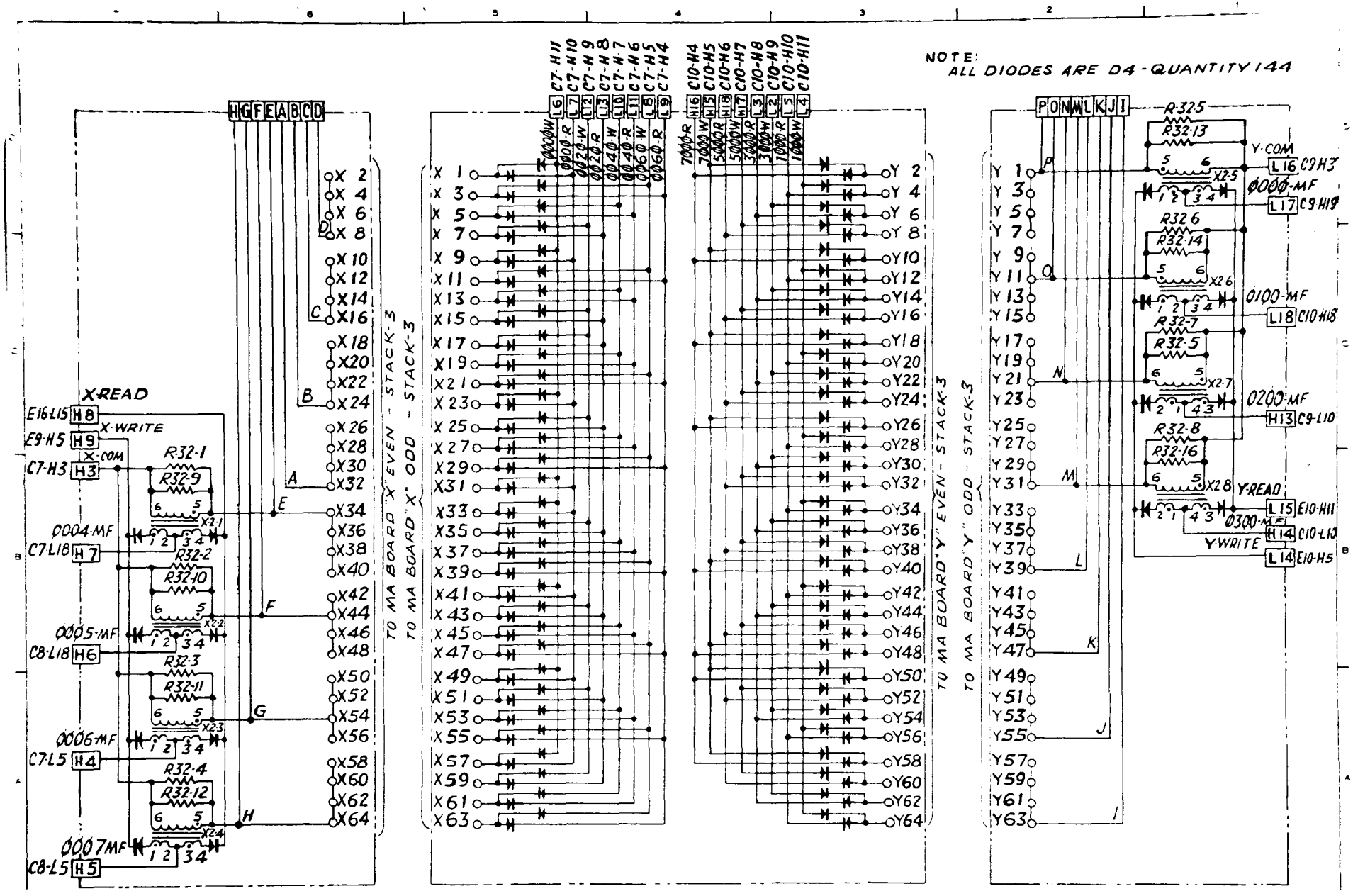
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES STACK 3

TITLE: SENSE AMPLIFIER LOGIC SCHEMATIC "M" PANEL (ISA)

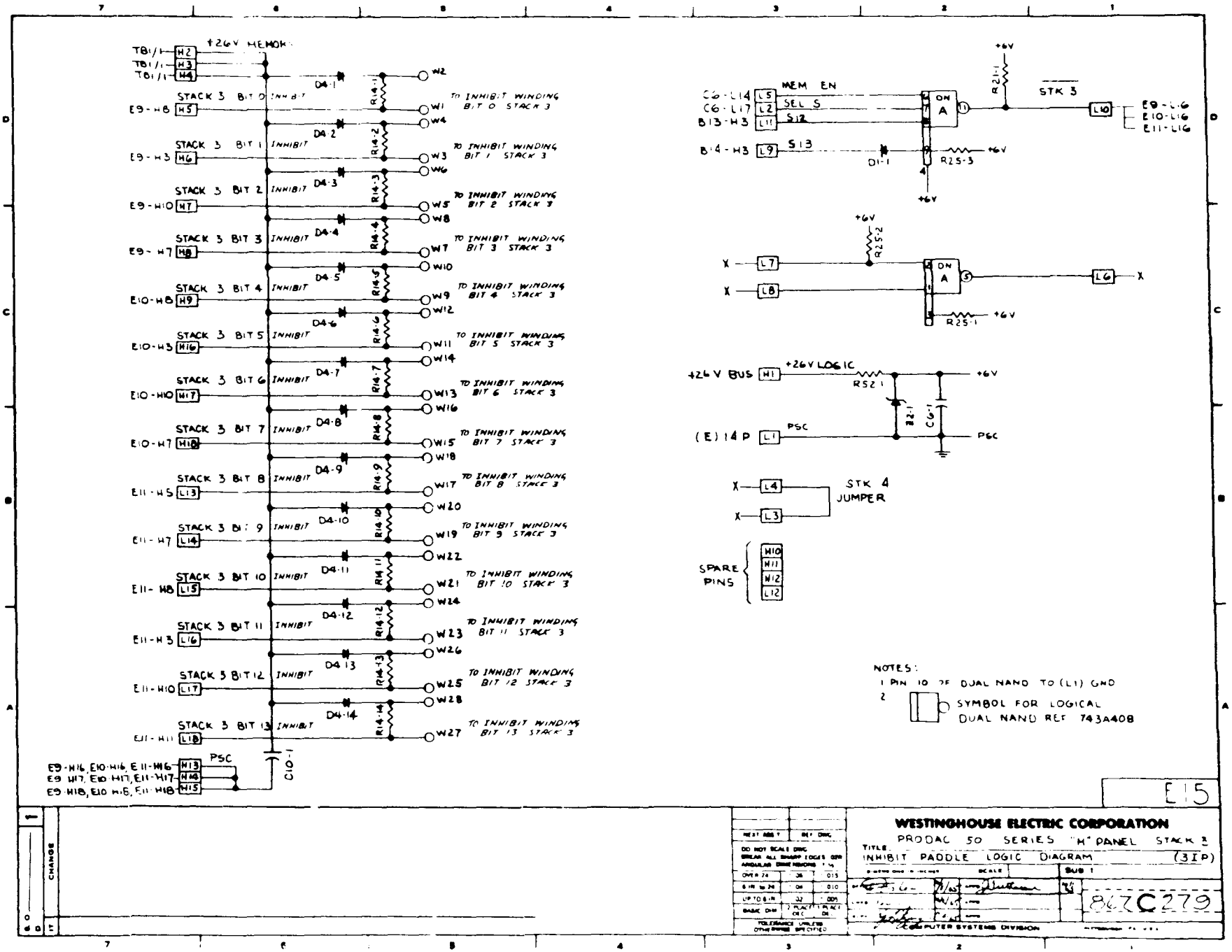
SUB 1

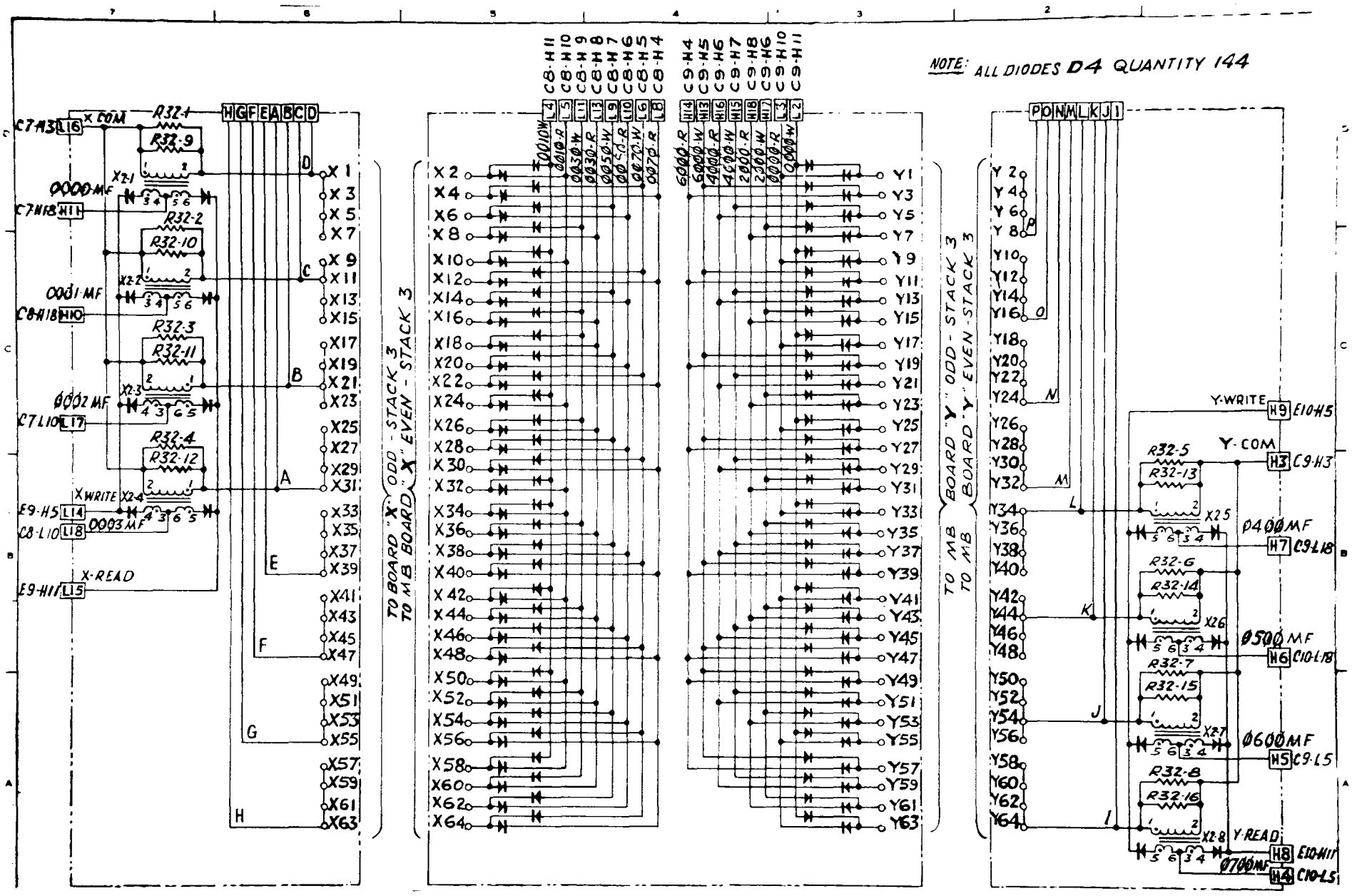
867C277

COMPUTER SYSTEMS DIVISION



PRODAC 50 SERIES M PANEL STACK 3
MEMORY DIODE LOGIC SCHEMATIC (2MB)
REFERENCE 867 C 278 - E 13


+26V MEMORY
TB1/1 H2
TB1/1 H3
TB1/1 H4
STACK 3 BIT 0 INHIBIT
E9-H8 H5
D4-1
R14-1
W2
W1
W4
TO INHIBIT WINDING BIT 0 STACK 3
STACK 3 BIT 1 INHIBIT
E9-H3 H6
D4-2
R14-2
W3
W6
TO INHIBIT WINDING BIT 1 STACK 3
STACK 3 BIT 2 INHIBIT
E9-H10 H7
D4-3
R14-3
W5
W8
TO INHIBIT WINDING BIT 2 STACK 3
STACK 3 BIT 3 INHIBIT
E9-H7 H8
D4-4
R14-4
W7
W10
TO INHIBIT WINDING BIT 3 STACK 3
STACK 3 BIT 4 INHIBIT
E10-H8 H9
D4-5
R14-5
W9
W12
TO INHIBIT WINDING BIT 4 STACK 3
STACK 3 BIT 5 INHIBIT
E10-H3 H16
D4-6
R14-6
W11
W14
TO INHIBIT WINDING BIT 5 STACK 3
STACK 3 BIT 6 INHIBIT
E10-H10 H17
D4-7
R14-7
W13
W16
TO INHIBIT WINDING BIT 6 STACK 3
STACK 3 BIT 7 INHIBIT
E10-H7 H18
D4-8
R14-8
W15
W18
TO INHIBIT WINDING BIT 7 STACK 3
STACK 3 BIT 8 INHIBIT
E11-H5 L13
D4-9
R14-9
W17
W20
TO INHIBIT WINDING BIT 8 STACK 3
STACK 3 BIT 9 INHIBIT
E11-H7 L14
D4-10
R14-10
W19
W22
TO INHIBIT WINDING BIT 9 STACK 3
STACK 3 BIT 10 INHIBIT
E11-H8 L15
D4-11
R14-11
W21
W24
TO INHIBIT WINDING BIT 10 STACK 3
STACK 3 BIT 11 INHIBIT
E11-H3 L16
D4-12
R14-12
W23
W26
TO INHIBIT WINDING BIT 11 STACK 3
STACK 3 BIT 12 INHIBIT
E11-H10 L17
D4-13
R14-13
W25
W28
TO INHIBIT WINDING BIT 12 STACK 3
STACK 3 BIT 13 INHIBIT
E11-H11 L18
D4-14
R14-14
W27
TO INHIBIT WINDING BIT 13 STACK 3
E9-H16, E10-H16, E11-H16 H13
E9-H17, E10-H17, E11-H17 H14
E9-H18, E10-H18, E11-H18 H15
PSC
C10-1
C6-L14 L5
C6-L17 L2
B13-H3 L11
MEM EN
SEL S
S12
B14-H3 L9
S13
D1-1
DN A
R21-1
+6V
STK 3
L10
E9-L16
E10-L16
E11-L16
R25-3
X L7
X L8
R25-2
L6
R25-1
+26V BUS H1
+26V LOGIC
R52-1
B2-1
C6-1
(E) 14 P L1
PSC
P6C
X L4
X L3
STK 4 JUMPER
SPARE PINS H10 H11 H12 L12
NOTES:
1 PIN 10 OF DUAL NAND TO (L1) GND
2 SYMBOL FOR LOGICAL DUAL NAND REF 743A408
E15
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES "H" PANEL STACK 3
TITLE
INHIBIT PADDLE LOGIC DIAGRAM (3IP)
SUB 1
867C279
COMPUTER SYSTEMS DIVISION



PRODAC 50 SERIES "M" PANEL STACK 3
MEMORY DIODE LOGIC SCHEMATIC (2 MA)
Reference 867 C 280 - E16

THE INTERRUPT SUBSYSTEM

GENERAL CHARACTERISTICS

Interrupt Defined

The Interrupt subsystem is the means by which a plant contact, a peripheral unit, or an external signal can call up directly a program in core. The subsystem is organized on a priority basis so that more important Interrupt inputs are scanned more frequently.

Interrupt Circuit

The Interrupt subsystem uses a saturating core buffer storage element for each interrupt input. Sixteen of these storage elements are located on each EI card.

A maximum of four cards can be used to bring the system up to its full capacity of 64 interrupts.

Operation of Interrupt Subsystem

Operation of the subsystem is as follows: Each sequence III the computer generates a probe pulse which checks the state of the interrupt input contact closures or signals. If a contact closure is present and the Interrupt core has not been previously set, a four-layer diode is triggered, and energy is dumped from a capacitor through a winding on the saturating core. As the core switches a signal is supported on a secondary winding called a "Hit" signal. The Hit signal sets a flip-flop. If the computer is not running under lockout, it completes its current instruction, then enters sequence I, which is the Interrupt scan. Successively the computer routes a pulse through each of the Interrupt cores until a response voltage is generated, and the lockout flip-flop is set. The computer then goes to the location identified with the particular core last scanned and does the instruction in that location.

After the particular program called out has been run, the program will clear the lockout flip-flop and the Interrupt scan will once again begin to find lower priority inputs or other high priority interrupts which may have been set while the computer was running under lockout. When the scan is completed without finding a core previously set and able to trigger the Lockout flip-flop, the computer will execute the next instruction as indicated by the program counter.

Block Diagram

A block diagram showing the Interrupt Subsystem is given in Figure 1-20. An interrupt is brought into the computer in two steps. First, the input voltage must rise to a sufficient level so that the Interrupt core can be set during probe time. When the core is set, a pulse is generated which sets the Hit flip-flop. Second, the computer must scan the Interrupt cores until a response voltage sets the Lockout flip-flop. The computer will then execute the instruction in the location associated with the last core to be interrogated.

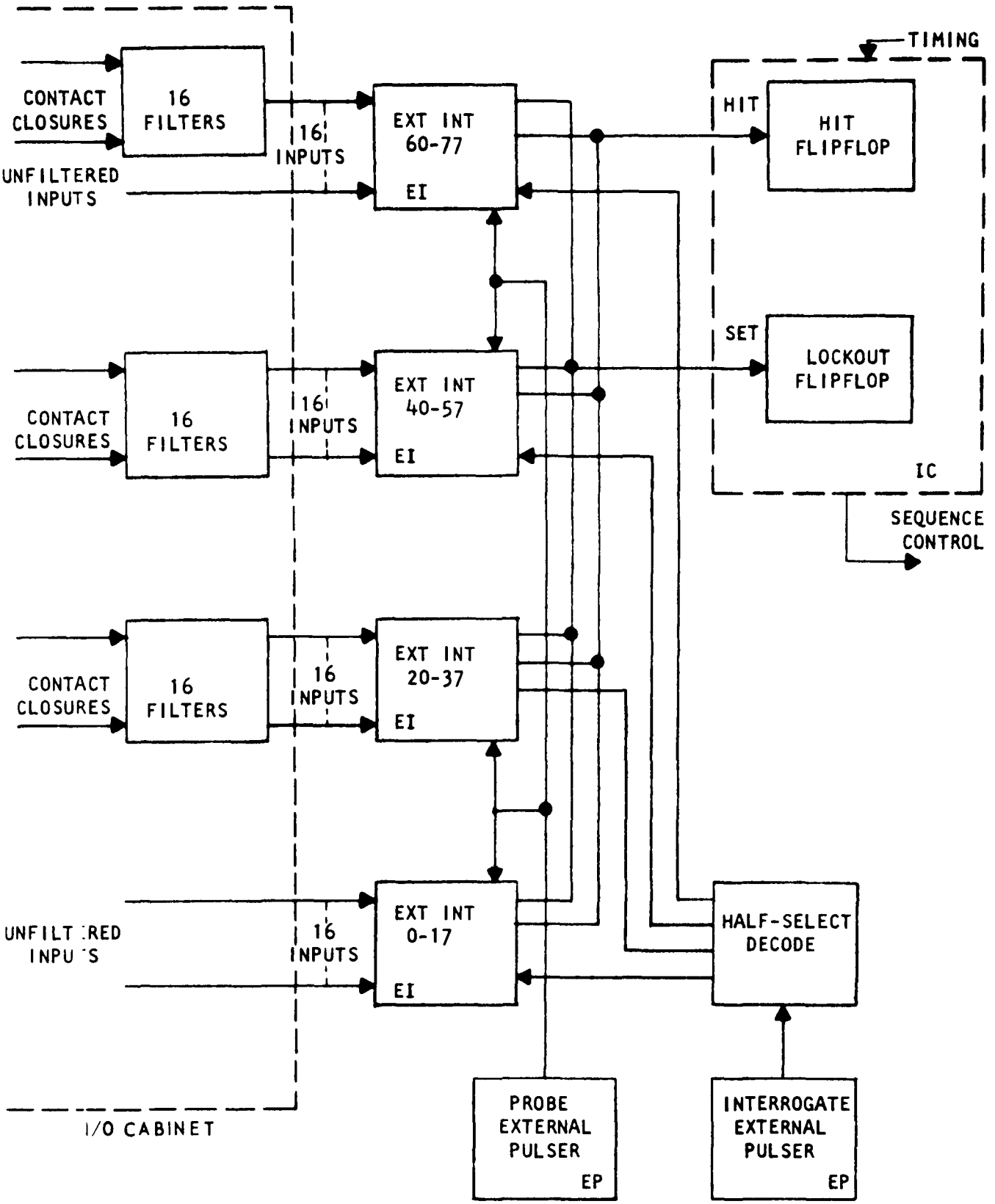


Figure 1-20. Interrupt Subsystem Block Diagram

SEQUENCE I DETAILS

Description of Sequence I

A flow diagram of Sequence I is shown in Figure 1-22. At the end of each instruction the Interrupt Lockout flip-flop is tested. If Lockout is set, the machine immediately proceeds to Sequence II. If lockout is not set, the Hit flip-flop is tested. If there has been no hit, the computer moves into Sequence II. If there has been a hit, the S register is cleared, and Sequence I is entered.

Before the end of each Sequence I, the S register is incremented, and the Interrupt is checked. If Interrupt Lockout has been set by the response voltage from an interrogate pulse, Sequence III will be entered, and the core location will be accessed as determined by the contents of the S register. If the Interrupt Lockout is not set, a check will be made to determine whether the scan has completed interrogation of 64 cores. If not, Sequence I will repeat.

An interrupt occurs in the central processor when the "Hit" flip-flop is set. An interrogate interrupt address scan is initiated and proceeds at a rate of 1.5 microseconds per address. The scan always starts interrogation with address 01 and proceeds to interrogate addresses 02, 03, 04, . . . n, where n is the address of the interrupt input which has occurred. When n is identified the scanning stops, the memory device containing n is reset, no other interrupts are permitted, and the central processor is caused to execute an instruction in the core memory location corresponding to n (64 core locations, one for each interrupt input address).

Generally the instructions so executed will be a Return Jump, which stores the location of the last instruction of the interrupted program, and initiates a new program. Thus any of 64 new programs may be initiated without losing track of the interrupted program.

It is important to note here that the interrupt unit is locked out when interrupt input address scan is initiated. It is necessary to clear interrupt lockout to recognize concurrent and future interrupt inputs. Figure 1-21 shows the interrogate interrupt input scan timing. Note that the "Hit" flip-flop remains set (scan continues) until last available address is interrogated.

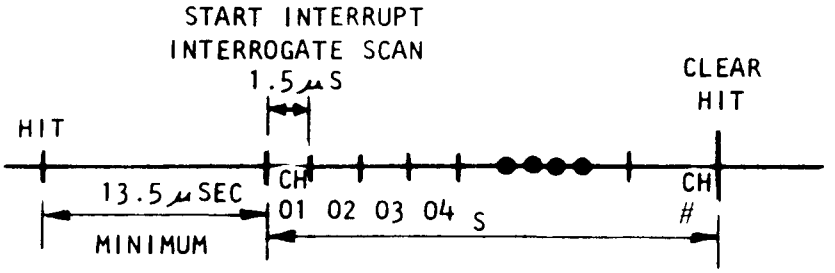


Figure 1-21. Timing - Interrupt Interrogate

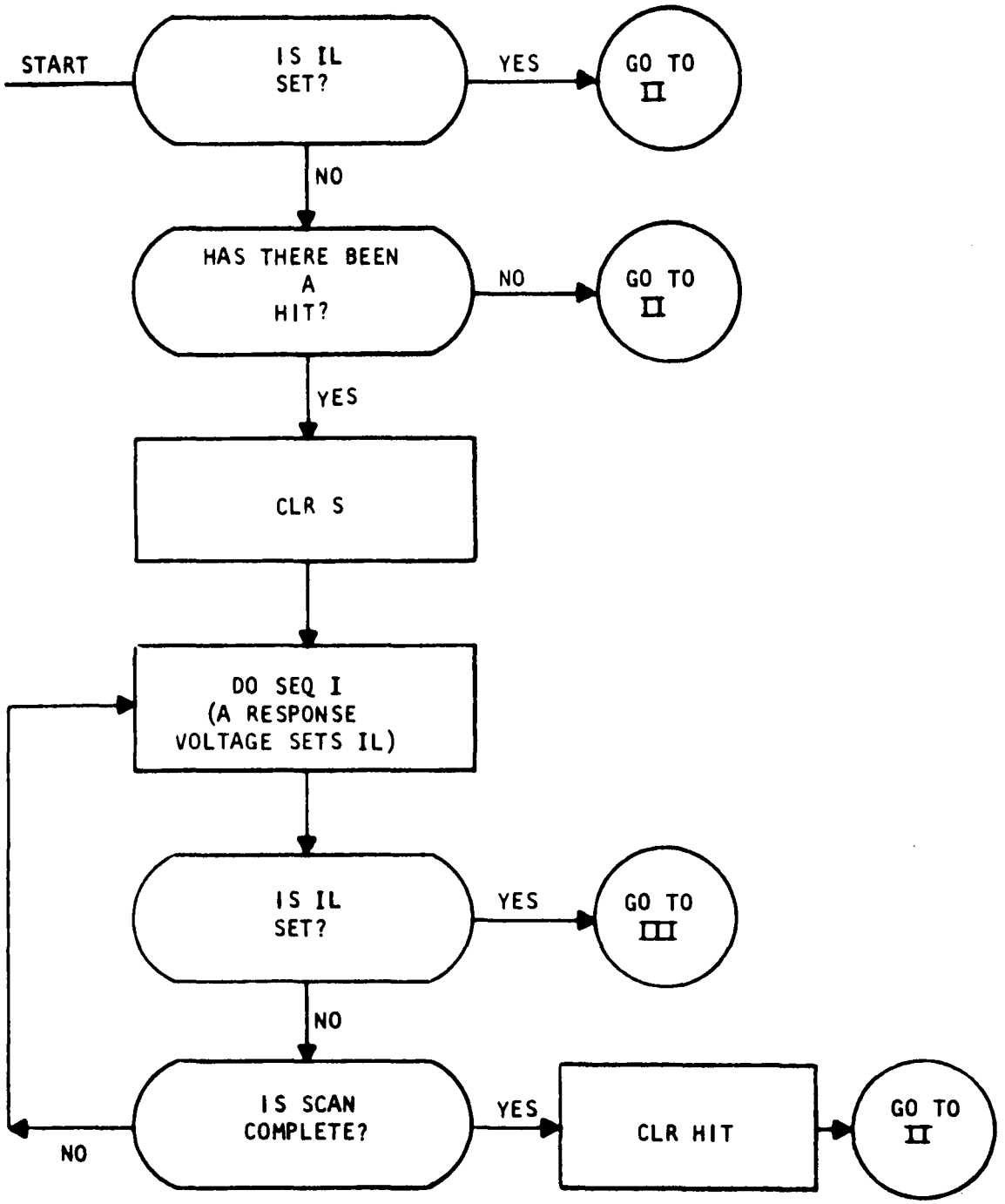


Figure 1-22. Interrupt Scan Flow Diagram

USE OF INTERRUPT INPUTS

As previously noted, interrupt inputs are used to obtain central processor attention. In the absence of interrupt input signals, the central processor proceeds completely unaware of the peripheral equipment associated with these input; consequently programming time normally required for monitoring purposes is reduced. In contrast, however, half the available interrupt inputs, on the average, must be scanned to locate an active one; therefore it is desirable to keep the number of interrupt inputs provided small. Average scan times are 36, 72, 108, and 144 microseconds, corresponding to the quantity of interrupts optionally available: 16, 32, 48, and 64. Examples follow of how interrupt inputs are used.

I/O Request

There is a finite time necessary for the peripheral system to react to a function given it by a central processor. If the function is to output, prerequisite to that output is knowledge that the peripheral system is not busy, hence ready to accept the output. If the function is an input, prerequisite to the input is data preparation and presentation for input. An interrupt input may be used in each case (output request, input request) to notify the central processor that the peripheral system is ready and can be committed to function.

Process Events

In application, whether for monitoring or for monitoring and controlling a process, an interrupt input may be used to define a particular time in the process which is critical to it. This time may be an incremental gate for the error signal to the computer as a direct digital controller, it may be a limit detector for temperature or level alarms, or it may define sequence in open loop control.

Avoid Over Use

In considering particular system interrupt input number and repetition rate requirements, both "hardware" and "software" restraints must be taken into account. The hardware presents an absolute maximum system capability (i.e., 64 inputs per maximum system). The address interrogation scan always starts with address 01 and proceeds to interrogate addresses 02, 03, . . ., n, where n is the address of the interrupt which has occurred; consequently, there is a priority of interrupt input assignment to be considered.

Programming limits the interrupt input repetition rate because some programmed routines are executed under interrupt lockout. When interrupt lockout is set, the central processor will not accept additional interrupts. It will store any interrupts that occur during lockout, and will accept them after lockout is cleared. However, if two or more interrupts occur on any one input during a continuous lockout, the central processor will recognize them as a single interrupt.

Filtering Available

Several interrupt input filter modules are available to provide interface between plant signals and the central processor interrupt input module. Sixteen inputs are provided for on one module. Interrupt rates, exclusive of programming constraints (charge and discharge time constants consideration), range from 15 interrupts per second to 200 interrupts per second.

USE OF MEMORY

Program Origins

The 64 interrupts access core location 00001 through 00100. The highest priority interrupt instruction should be entered in 00001; the lowest, in 00100.

Automatic Selection of Origin

The computer responds to an interrupt and immediately accesses the corresponding core location, and does the instruction in that location without modifying P.

Avoidance of P

The program counter location is not disturbed during an Interrupt scan.

Use of RJP, Y, I

Return Jump Indirect is typically stored in the Interrupt location to transfer control to a predetermined location and to save the P register contents. These predetermined locations are contained in addresses 00102 to 00201. For example, the P register is saved in the location that is in 00102 when the Interrupt comes into location 00001. The computer jumps to the next instruction called out by the 00102 address.

Shown below is a typical program accessed by interrupts showing Return Jump Indirect to a "link" location, storing of P, Designator and Accumulator, running of program, retrieving of Accumulator and Designator information of interrupted program, and CLJ Indirect to location containing P to end lockout operation and return to interrupted program:

LOC.	INSTR.	FUNCTION
1	RJP 101+1, I	Transfer to predetermined location and store program
102	5000	Transfer address for interrupt #0
5000	. . .	Storage location for contents of P Register at time of interrupt
	SDR A	Save registers for restart
	STL B	
	.	Execution of function requested by this interrupt
	.	
	.	
	ENL B	Reload registers for restart
	EDR A	
	CLJ 5000,I	Release lockout and transfer control to interrupted program

Use of CLJ, O, I and CLJ

Clear Lockout Jump Indirect to P (CLJ, O, I) stored in an Interrupt location to ignore an interrupt and return to the program that was interrupted.

Clear Lockout Jump (CLJ) is used any time the programmer wishes to end operation under lockout.

ADDING INTERRUPTS IN THE FIELD

Location of Cards

The EI Interrupt cards are located in slots C13, C14, C15, and C16. When using only one card in a system, the 3EI card should be located in slot C13. When adding cards to the system, the cards should be located in slots C14, C15, and C16 in that order.

Modification of Scan Termination

When only one EI card is used, the scan should end after 16 cores are terminated. When four EI cards are used, the termination should be altered to include 64 cores in the scan. Instructions for altering the termination are given on the IC Interrupt Scan Control Logic schematic.

Options

Options of 16, 32, 48, and 64 interrupt inputs are available in the system. The unit may expand in groups of 16 inputs. Required to add a group is:

1. One central processor interrupt input module
2. One or two interrupt filter modules for each type of filter required
3. One cable to connect central processor interrupt input module to the interrupt filter module
4. One cable to connect each interrupt filter module to standard termination areas. These cables will contain necessary terminal hardware to complete the assembly.

Interrupt Assignments - Standard

The following interrupts will execute out-of-sequence the instruction in the corresponding core location for any P-50 series computer. Of course these are only suggested as standard; each system is designed to the user's specifications.

Interrupt Number	Interrupt	Core Location
0	Power Supply Failure	01
1	Analog Conversion Complete	02
2	Real Time Clock (Sync.)	03
3	Contact Closure Input Read	04
4	Contact Closure Input Complete	05
5	High Speed Punch Complete	06
6	High Speed Reader Complete	07
7	ASR Input Complete	10
10	ASR Output Complete	11
11	Contact Closure Output Complete	12
12	Logger Complete	13

Other interrupts such as extra loggers, punches, readers, and process interrupts will follow the above in a preferred order.

TIMING CHART

The timing chart for Sequence I, which is the Interrupt scan Interrogate cycle, is shown in Figure 1-23.

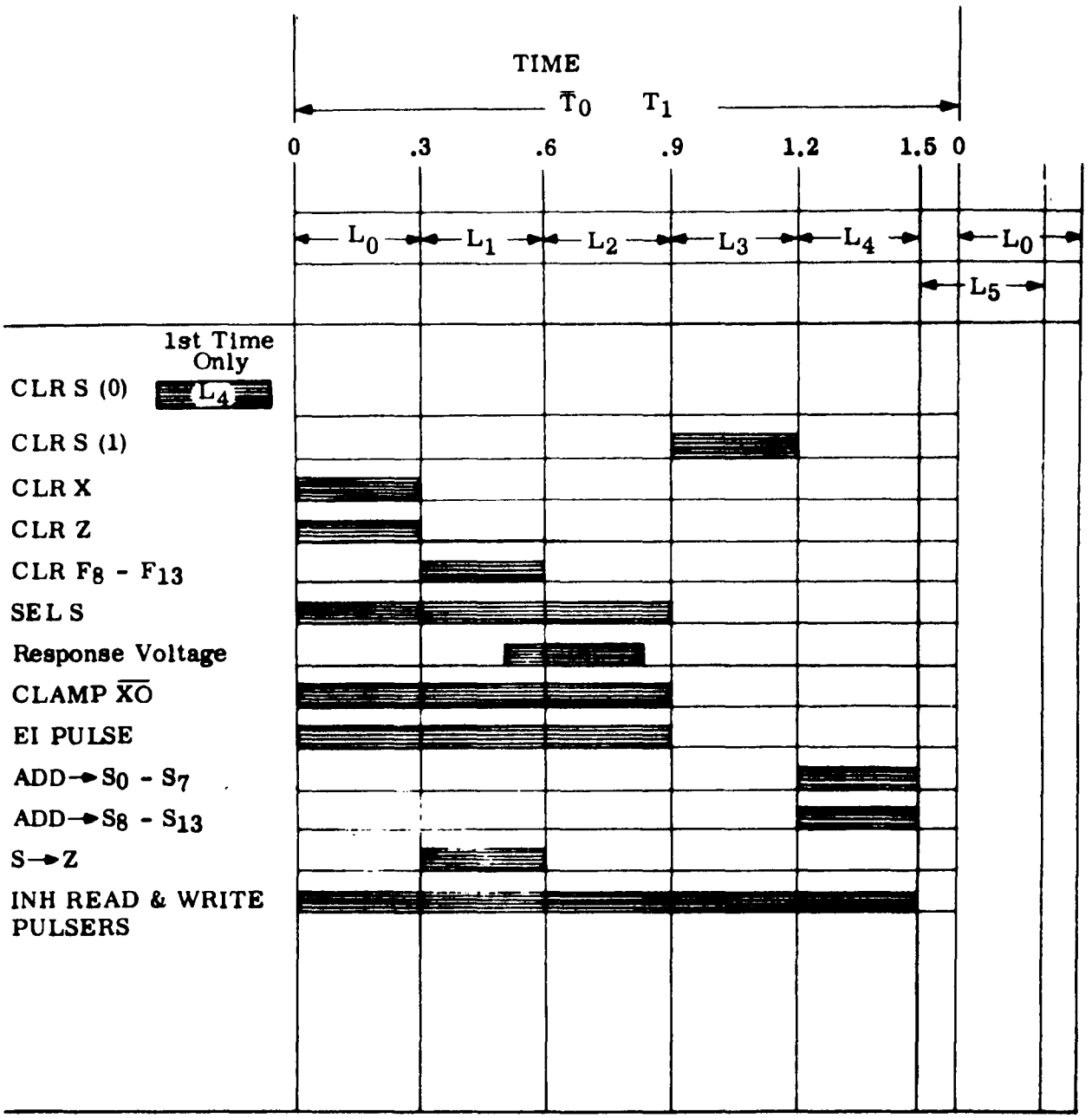


Figure 1-23. Sequence I Timing Chart

I/Ø DRIVER PANEL D PANEL IØO2

GENERAL DESCRIPTION

The I/Ø driver panel has card slot capability for translating half select lines and I/Ø data lines originating on the P-50 main frames or P-550 "T" panels to word and channel drive lines for either CCO or CCI multiplex xchemes. It also has channel driver capability for I/Ø devices such as the high speed reader, punch, ASR, and Selectric typewriter.

CIRCUIT OPERATION

Circuit operation is best explained by defining the back panel wiring layout in conjunction with the data lines from the computer main frame.

Each slot of the I/O driver panel from slot 1 to 14 is buss wired with I/O data Input and Output lines brought in on connector 21 or 23. Each slot then has an individual half select line brought in from connector 22 or 24 which serves as its own channel address. With the wiring so commoned any card which requires any of the above data can be interchanged and used in any of the 14 slots. The following is a list of the cards that can be used:

RB, DE, SL, TS, TN, TO, 4IF, PSS, CD, CB

The two slots 15-16 are wired for word drivers with 16 half select lines per slot. A specific addressing scheme exists and is shown on the attached block diagram.

There are a total of 4 "D" panels with addressing as shown. No word driver capability is available on D_3 and D_4 but the slots are wired for power.

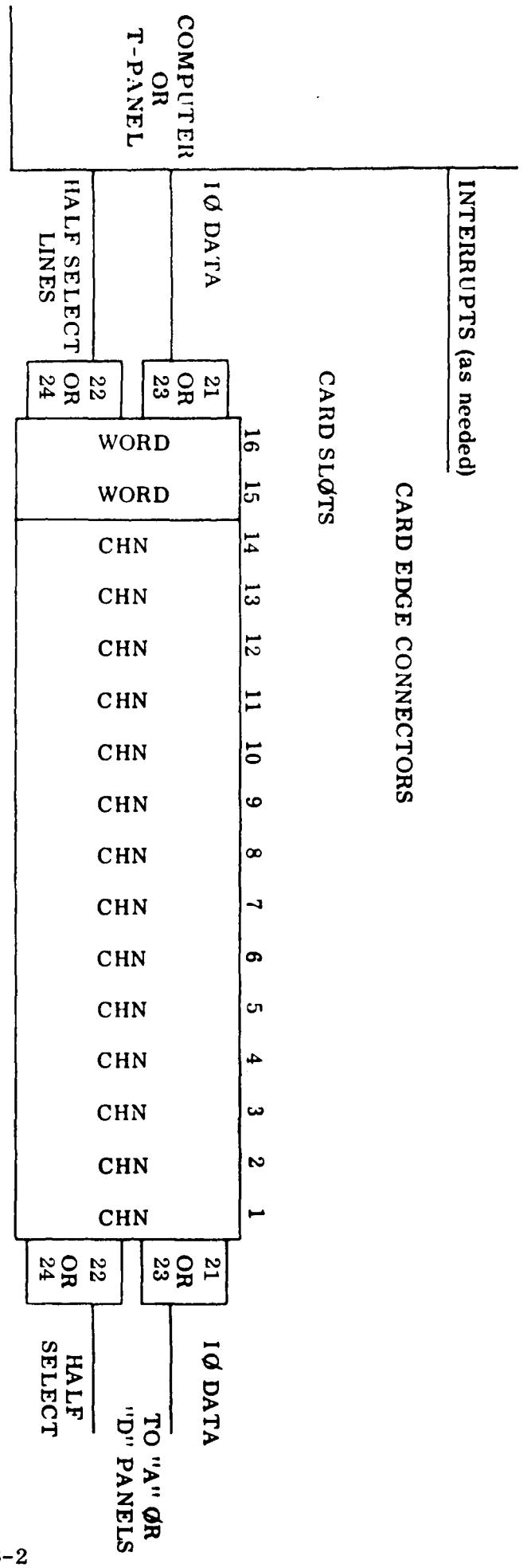
There are two cards which can be used in any slot of the panel and these are the 4IF and the PSS. The reason is that they require no back panel wiring in the case of the 4IF or only power in the case of the PSS.

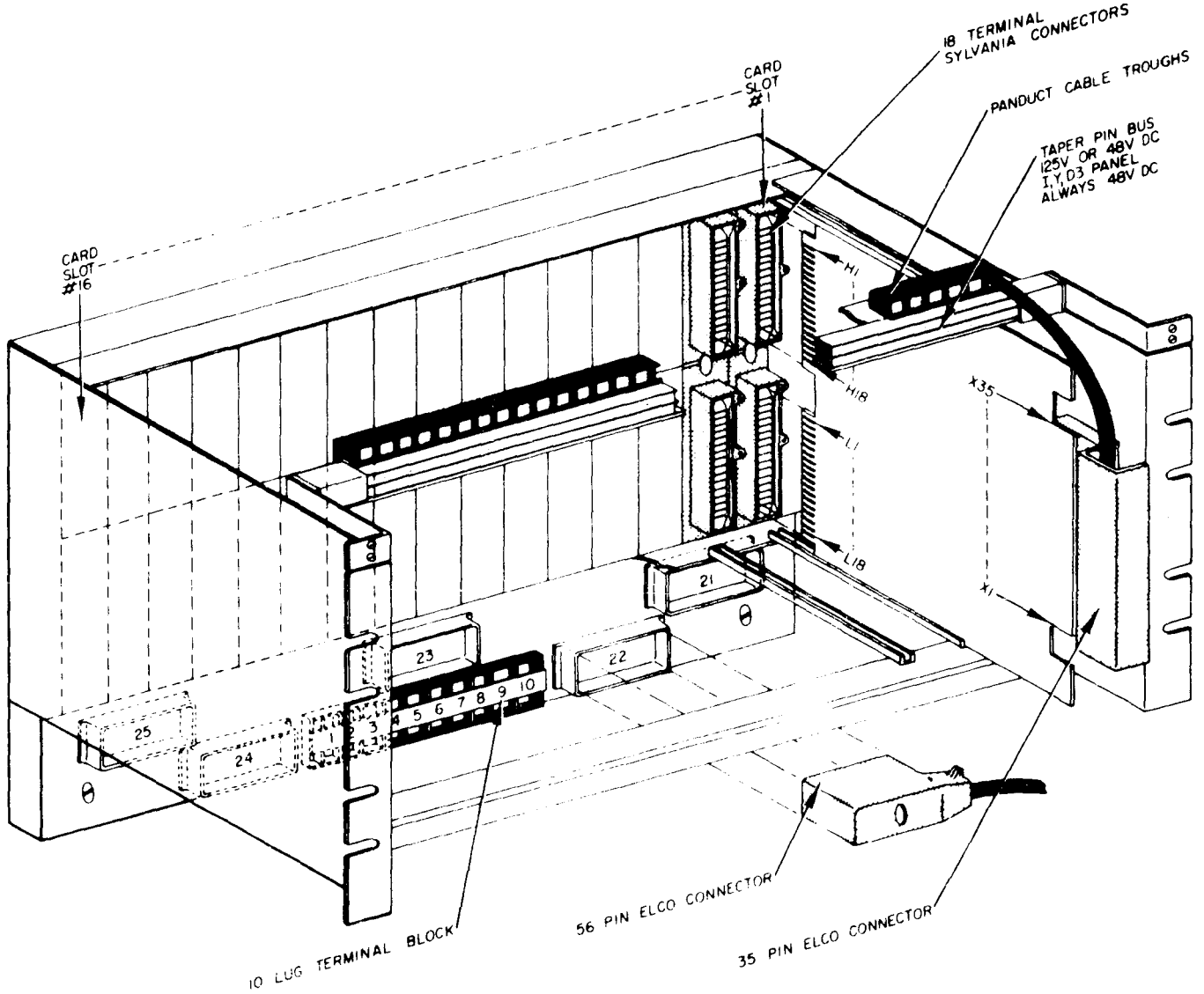
Interrupt wiring needed on many of the cards used in this panel is made on card edge connectors with separate cables and have no connection to the panel.

The 56 pin Elco connectors 21 and 23 are wired exactly alike and act as termination point from the computer or T-panel and is a transfer point to other "D" or "A" panels. The same is true of connectors 22 and 24.

MULTIPLEX ADDRESSING

PWR	ONLY	60-77	20-37
PWR	ONLY	40-51	0-17
75	55	35	15
74	54	34	14
73	53	33	13
72	52	32	12
71	51	31	11
70	50	30	10
67	47	27	7
66	46	26	6
65	45	25	5
64	44	24	4
63	43	23	3
62	42	22	2
61	41	21	1
60	40	20	0



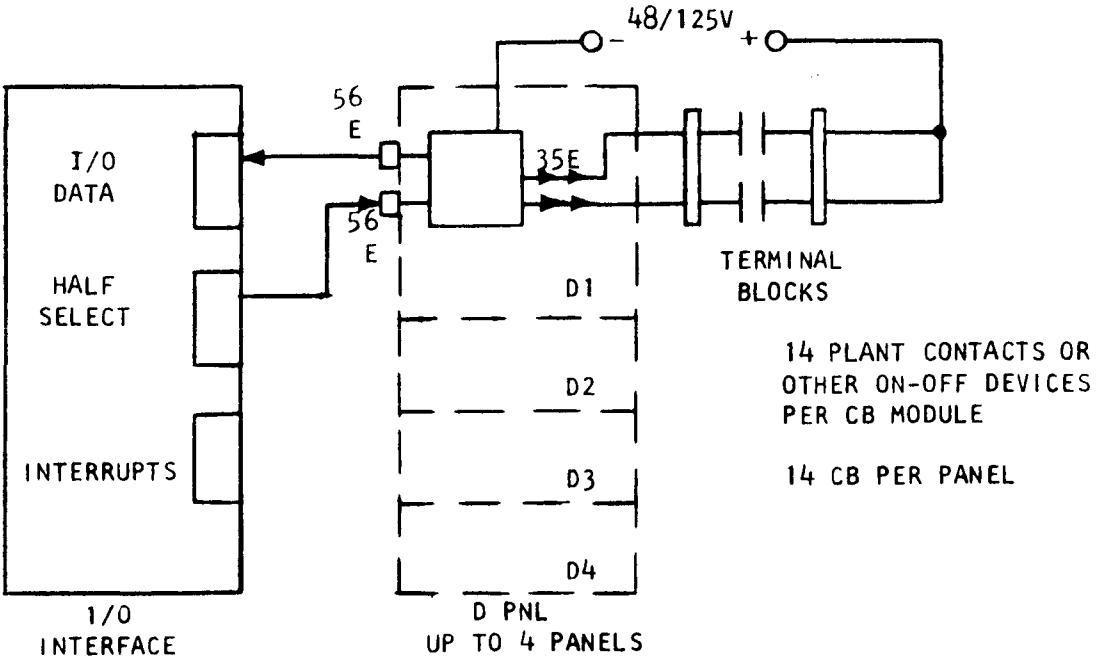

CARD SLOT #16
CARD SLOT #1
18 TERMINAL SYLVANIA CONNECTORS
PANDUCT CABLE TROUGHS
TAPER PIN BUS 125V OR 48V DC I,Y,D3 PANEL ALWAYS 48V DC
H1
H18
L1
L18
X35
X1
21
22
23
24
25
1 2 3 4 5 6 7 8 9 10
10 LUG TERMINAL BLOCK
56 PIN ELCO CONNECTOR
35 PIN ELCO CONNECTOR

NON-MULTIPLEXED CONTACT CLOSURE INPUT SUBSYSTEM

I. GENERAL DESCRIPTION

A. Non-multiplexed contact closure inputs (CCI) provide a fast means of entering 14 bits of data simultaneously into the computer. This is done by means of a Contact Buffer (CB) card located in a D panel. There is a maximum of 14 CB cards allowed per panel with a maximum of four panels assigned to a central processor interface unit.

Figure 1 is a block diagram of the non-multiplexed CCI sub-system.



NON-MULTIPLEXED CCI

Figure 1

B. Non-multiplexed CCI may be used in a variety of applications such as detecting process contact closures, computer-to-computer communication, sequence-of-

events recording and telemetry data collection. The first application above is the more general one, and will be discussed below. The latter three functions are similar, but for special applications.

II. SPECIFICATIONS

Input Requirements

CB cards to monitor process contact closures operate with inputs of 48 VDC or 125VDC. A 48VDC source is supplied with the computer. 125VDC may be supplied with the system or it may be supplied by the computer user. The supply should not vary more than ± 10%; the capacity of the supply depends on the number of CCI's being driven, and other loads on the supply.

Reference CB printed circuit card description for voltages required on the different CB cards.

III. CIRCUIT OPERATION

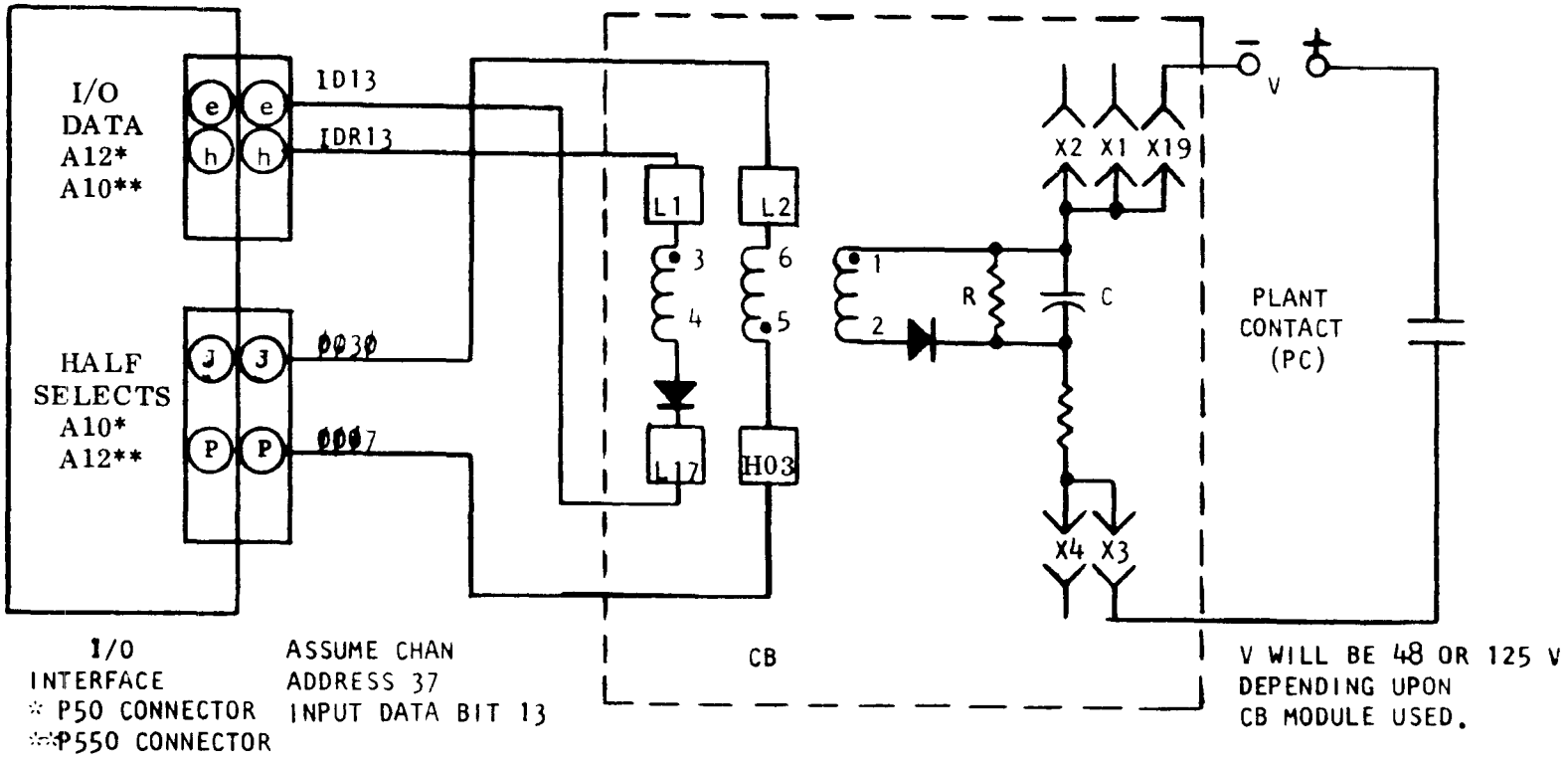
A. General

In the general application of detecting the status of process contacts, the non-multiplexed CCI circuits are operated in the open-loop mode. No timing adjustments are required.

CCI scan frequency is a function of (1) filter charge-discharge times and (2) programming. On both the 2CB4 (48V) and the 2CB6 (125V) cards, the charge time for the filter is approximately 0.80 milliseconds, and the discharge time for the filter capacitor is approximately 4.50 milliseconds. Both of these values are worst case figures for must-operate conditions. These charge-discharge periods indicate the maximum rate at which the inputs will follow the change in status of plant contacts. Software then initiates scanning of the inputs at appropriate intervals as required by the process. 14 bits of data (corresponding to the 14 process contacts tied to one CB card) are taken into the computer on the execution of an input command. The channel is addressed with the low order six bits of the instruction word specifying the channel number.

B. Circuit Description

Figure 2 is a simplified portion of a non-multiplexed CCI subsystem. It is one of fourteen stages on a CB card. The channel address shown for this card is channel 37, and the input data bit is number 13. If the plant contact, PC, is closed and the voltage V, is impressed across X19 and X3 charging capacitor C, input data bit 13 will present a "1" to the I/Ø interface when an input command is transmitted over channel 37. If the plant contact is open, capacitor C will be discharged through resistor R. Then when transformer X1 is pulsed through the action of the



SIMPLIFIED SCHEMATIC REPRESENTATIVE OF 14 SIMILAR STAGES ON CB CARD.
PLANT CONTACT IS SHOWN
ADDRESS IS CHANNEL 37, INPUT DATA BIT 13.

Figure 2

half-select circuits, capacitor C will short out the transformer, and a "0" will be presented to the I/Ø interface on the input data lines.

V. CONNECTORS & TERMINATIONS

A. Connector Breakdown I/O Interface Data

Note: This breakdown applies to the P50 Interface plug A12 or the P550 Interface plug A10.

56 PIN ELCO	DESIGNATION	56 PIN ELCO	DESIGNATION
A	IDO	h	IDR13
B	IDRO	j	OD13
C	ID1	k	ODR12
D	IDR1	l	OD12
E	ID2	m	ODR11
F	IDR2	n	OD11
H	ID6	p	ODR10
J	ID3	r	OD10
K	IDR3	s	ODR 9
L	ID4	t	OD 9
M	IDR4	u	ODR 8
N	ID5	v	OD 8
P	IDR5	w	ODR 6
R	ID7	x	ODR 7
S	IDR7	y	OD 7
T	IDR6	z	ODR 5
U	ID8	AA	OD 5
V	IDR8	BB	ODR 4
W	ID9	CC	OD 4
X	IDR9	DD	ODR 3
Y	ID10	EE	OD 3
Z	IDR10	FF	OD 6
a	ID11	HH	ODR 2
b	IDR11	JJ	OD 2
c	ID12	KK	ODR 1
d	IDR12	LL	OD 1
e	ID13	MM	ODR 0
f	ODR13	NN	OD 0

B. Connector Breakdown I/O Interface Half Select

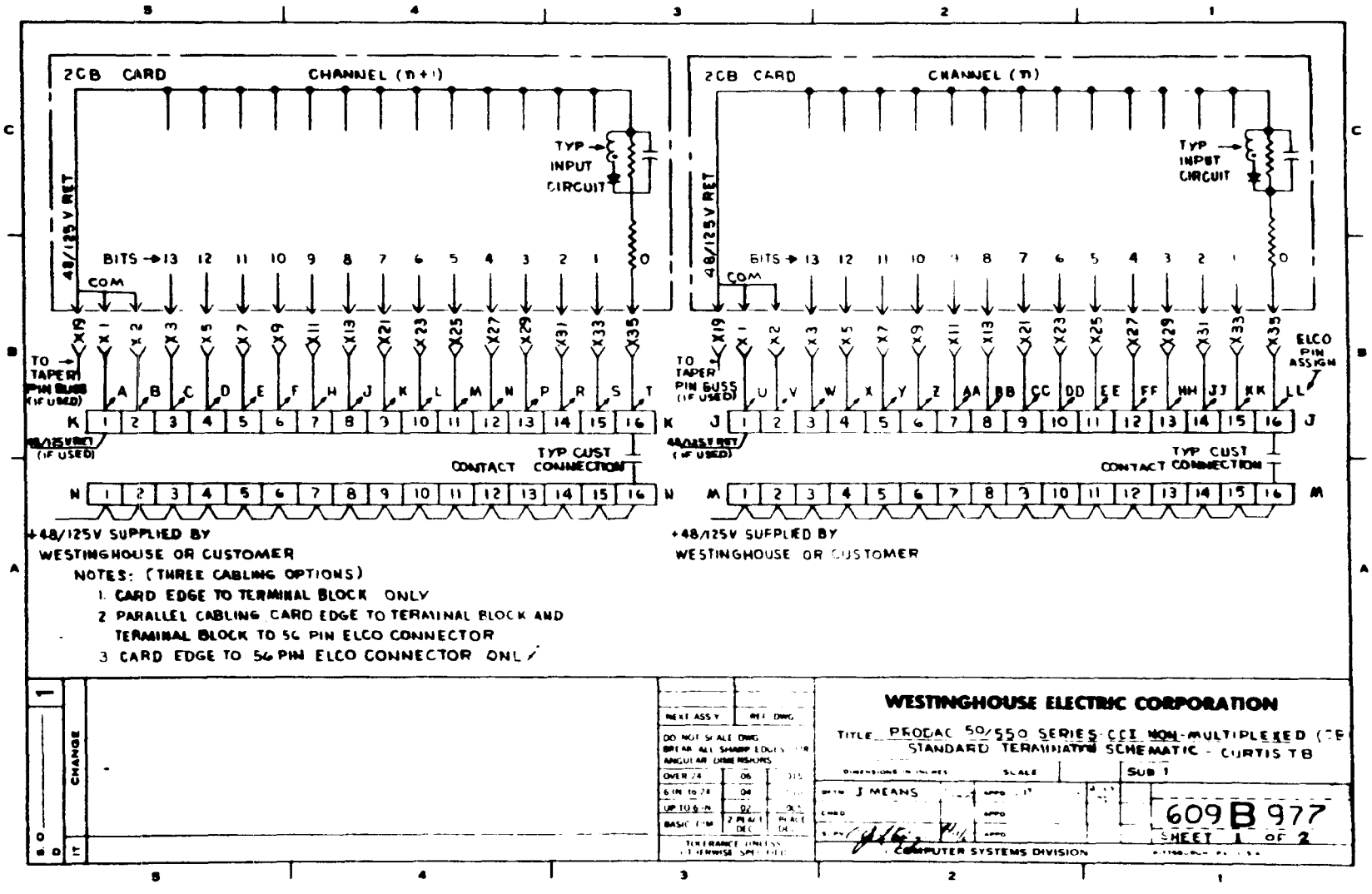
Note: This breakdown applies to the P50 interface plug A10 or the P550 interface plug A12.

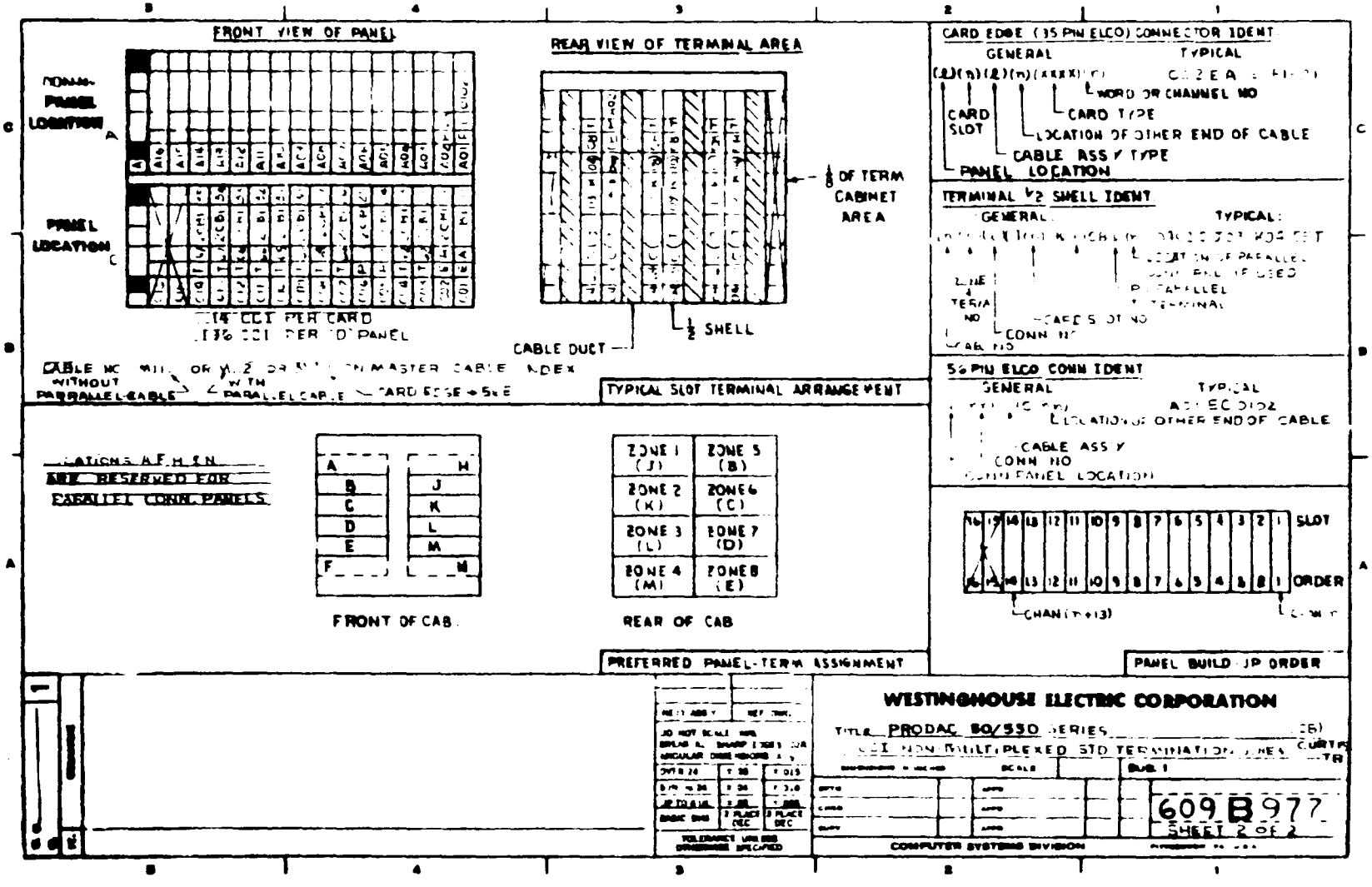
56 PIN ELCO	DESIGNATION		56 PIN ELCO	DESIGNATION
A	0000		V	7000
B	0001		W	6000
C	0002		X	5000
D	0003		Y	4000
E	0004		Z	0700
F	0010		AA	0600
H	0020		BB	0500
J	0030		CC	0400
L	0004		EE	3000
M	0005		FF	2000
N	0006		HH	1000
P	0007		JJ	0000
R	0040		KK	0300
S	0050		LL	0200
T	0060		MM	0100
U	0070		NN	0000

C. Terminations

Drawing 609B977 sheets 1 and 2 define the terminations available for the non-multiplexed CCI system.

Connectors J, K, L and M are the Curtis Terminal Blocks, this is the most commonly used type, however, these can be Rowan blocks which have the same terminal markings or they can be Elco connectors as shown in the drawing.


2CB CARD
CHANNEL (n+1)
2CB CARD
CHANNEL (n)
TYP INPUT CIRCUIT
48/125 V RET
COM
BITS → 13 12 11 10 9 8 7 6 5 4 3 2 1 0
TO TAPER PIN BUSS (IF USED)
ELCO PIN ASSIGN
TYP CUST CONTACT CONNECTION
+48/125V SUPPLIED BY WESTINGHOUSE OR CUSTOMER
NOTES: (THREE CABLING OPTIONS)
1. CARD EDGE TO TERMINAL BLOCK ONLY
2 PARALLEL CABLING CARD EDGE TO TERMINAL BLOCK AND TERMINAL BLOCK TO 56 PIN ELCO CONNECTOR
3 CARD EDGE TO 56 PIN ELCO CONNECTOR ONLY
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50/550 SERIES CCI NON-MULTIPLEXED (TB
STANDARD TERMINATION SCHEMATIC - CURTIS TB
SUB 1
609B977
SHEET 1 OF 2
COMPUTER SYSTEMS DIVISION


FRONT VIEW OF PANEL
REAR VIEW OF TERMINAL AREA
CARD EDGE (35 PIN ELCO) CONNECTOR IDENT
GENERAL
TYPICAL
CARD SLOT
CABLE ASSY TYPE
LOCATION OF OTHER END OF CABLE
CARD TYPE
WORD OR CHANNEL NO
PANEL LOCATION
TERMINAL ½ SHELL IDENT
GENERAL
TYPICAL
CABLE DUCT
½ SHELL
⅛ OF TERM CABINET AREA
56 PIN ELCO CONN IDENT
GENERAL
TYPICAL
CABLE ASSY
CONN NO
LOCATION OF OTHER END OF CABLE
CONN PANEL LOCATION
TYPICAL SLOT TERMINAL ARRANGEMENT
LOCATIONS A,F,H,E,N ARE RESERVED FOR PARALLEL CONN. PANELS
FRONT OF CAB
REAR OF CAB
ZONE 1 (J)
ZONE 5 (B)
ZONE 2 (K)
ZONE 6 (C)
ZONE 3 (L)
ZONE 7 (D)
ZONE 4 (M)
ZONE 8 (E)
PREFERRED PANEL-TERM ASSIGNMENT
SLOT
ORDER
PANEL BUILD UP ORDER
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC 50/550 SERIES
SEI NON MULTIPLEXED STD TERMINATION PANELS
609B9777
SHEET 2 OF 2
COMPUTER SYSTEMS DIVISION

CONTACT CLOSURE OUTPUT SUBSYSTEM

I. GENERAL DESCRIPTION

The contact closure output (CCØ) sub-system provides computer controlled electrically isolated relay contacts for the control of equipment and devices located external to the computer. A few examples of the many uses for contact closure outputs are listed below:

1. CCØ's may be used singly or in groups to communicate with operating personnel by means of lights, buzzers, alarm horns, and digital displays.

2. CCØ's may be used to initiate the action of plant or process devices such as motors and valve positioners.

3. CCØ's may be used to sequence a number of plant or process devices by initiating actions in a particular order and for specific times.

4. CCØ's may be used in combination with stepping motors or resistance networks to provide the computer with an analog output capability.

Owing to the wide range of possible applications, power for the operation of devices from CCØ's must always be supplied externally to the CCØ sub-system.

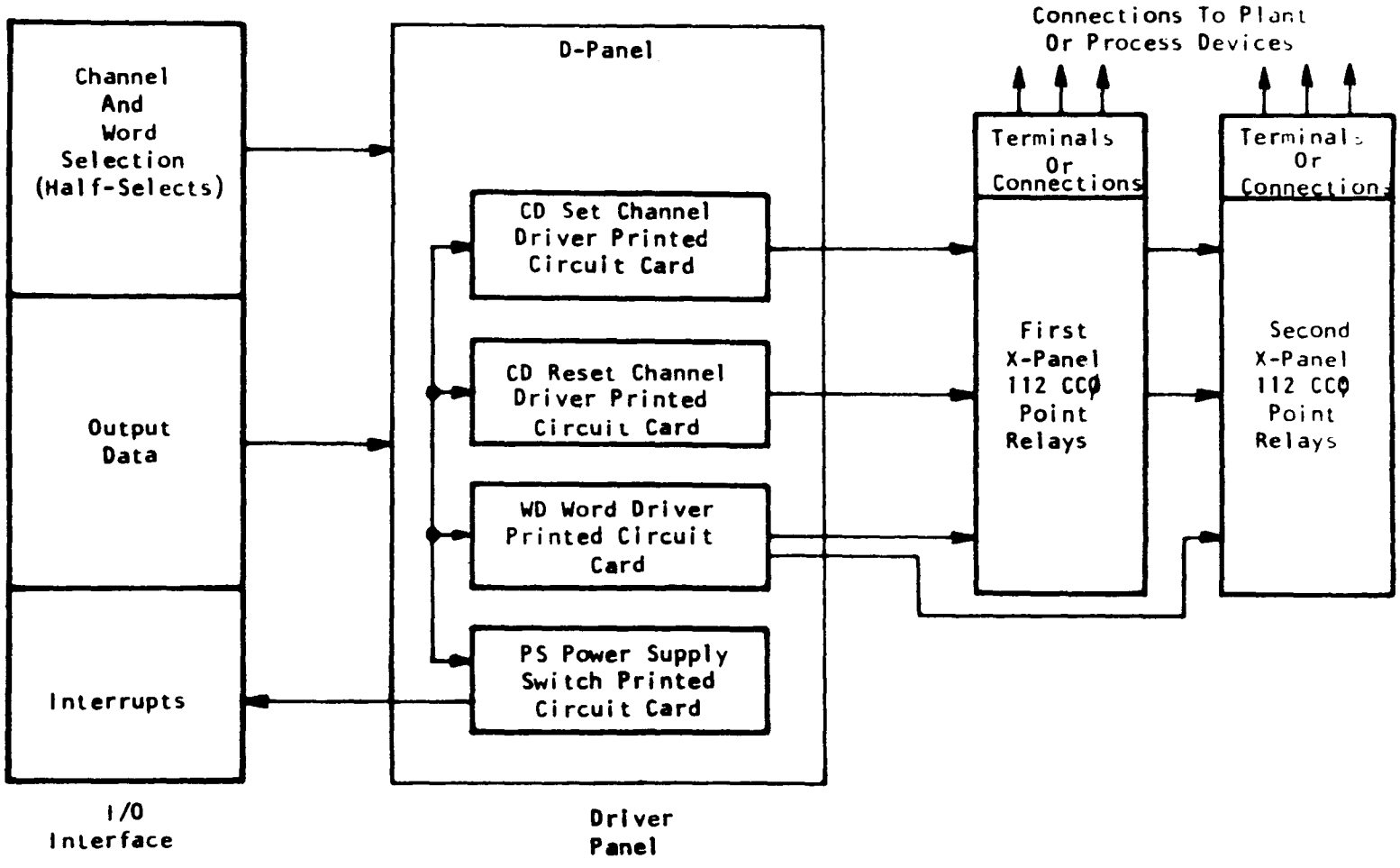
The contact closure output sub-system consists of CCØ point relay cards which are located on one or more X-panels, along with word and channel drive circuitry which resides on printed circuit cards located in a D-panel. CCØ point relays are bistable (latching), so both set and reset drive circuitry is required.

Figure 1a is a block diagram of a CCØ sub-system containing 224 individual point relays. One word driver printed circuit card and two channel driver printed circuit cards are required to select and energize the proper relays. One power supply switch printed circuit card is required for timing. A single CCØ point card contains seven relays, so that one full X-panel of CCØ cards will contain 16 x 7 = 112 CCØ point relays. By adding a second X-panel a total of 224 points can be obtained without additional drive circuitry.

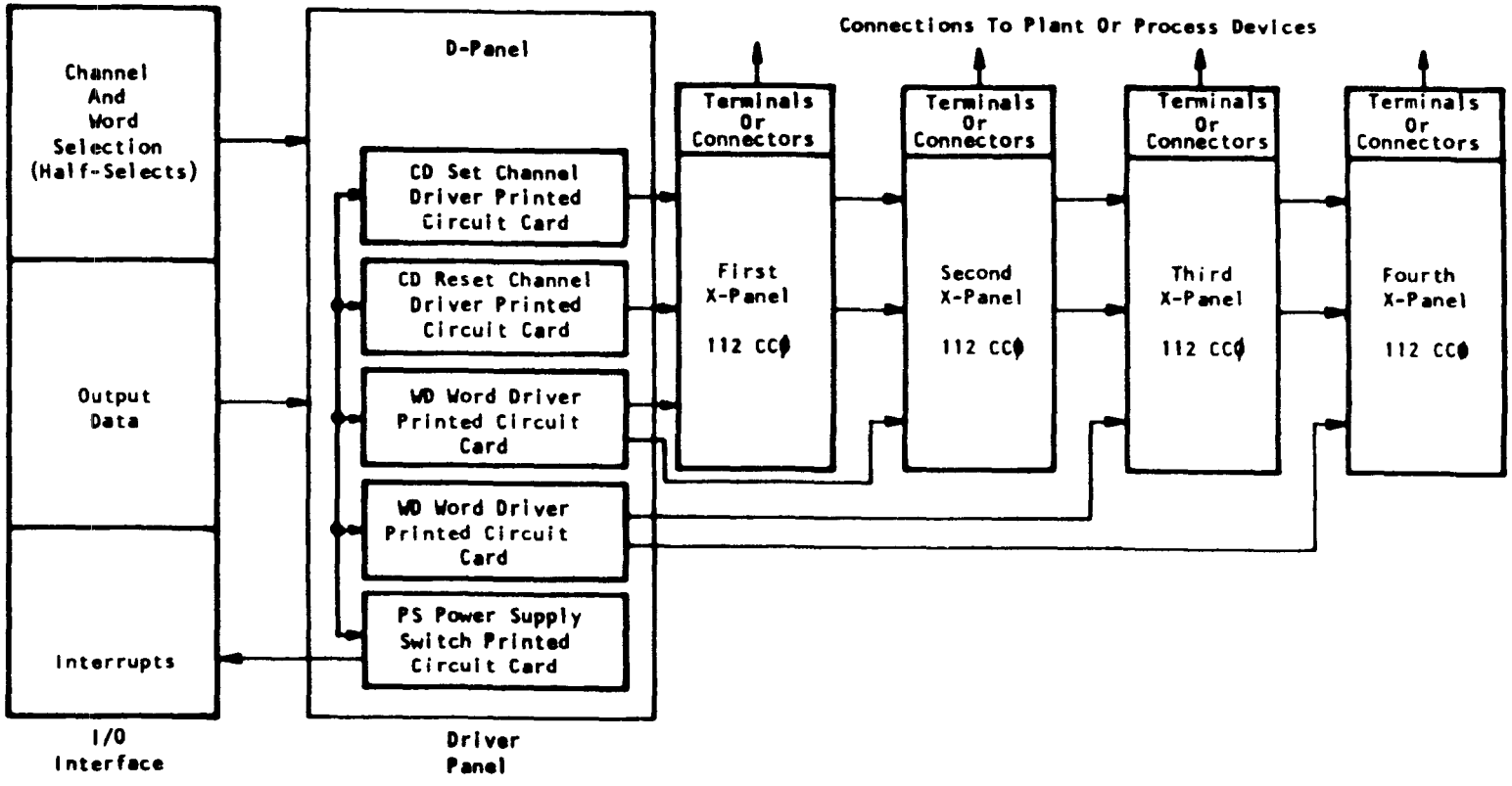
To expand a system to have between 225 and 448 CCØ point relays, an additional word driver must be added, as well as additional X-panels. Refer to Figure 1b for the block diagram of a 448 point system.

By adding two channel drivers, up to 896 CCØ point relays may be used. Refer to figure 1c for the block diagram of an 896 point system.

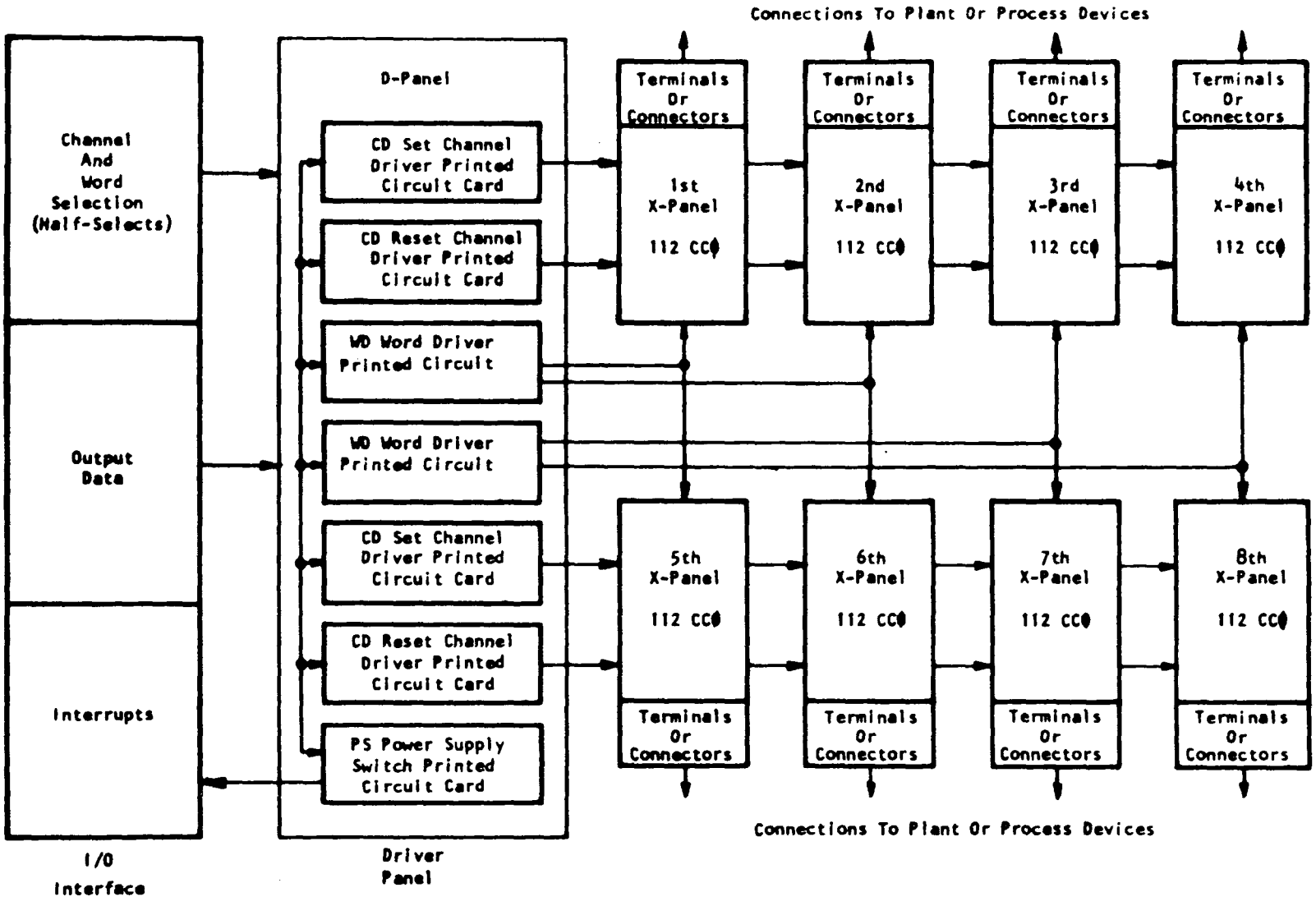
The greatest number of CCØ points available as a catalog standard is 896, although larger numbers can be obtained as a special item.



CCØ SUB-SYSTEM OF 224 POINTS
Figure 1a



CCO SUB-SYSTEM OF 448 POINTS
Figure 1b



CCO SUB-SYSTEM OF 896 POINTS
Figure 1c

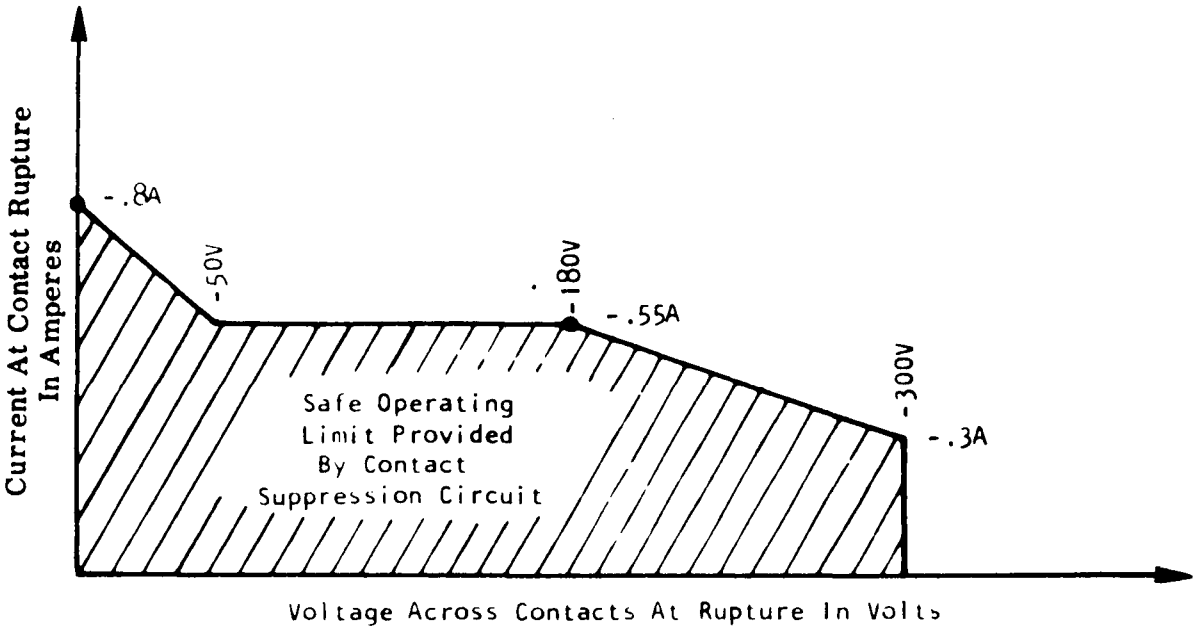
II. SPECIFICATIONS

A. Input Requirements - As with all other sub-systems, the CCØ sub-system interface with the computer central processor itself is via computer word and channel selection circuitry. The only inputs to the CCØ subsystem are from these computer I/Ø interface circuits.

B. Contact Specifications - All outputs from the CCØ subsystem are via electrically isolated mercury wetted relay contacts. Each relay contact is a bounce free, form D, "make-before-break" type having a normally open contact (NØ), a normally closed contact (NC) and an armature (A). The open contact will close before the closed contact opens. The "bridging" time, or time during which both contacts are closed, is approximately 0.1 milliseconds.

Each individual relay contact in the CCØ sub-system is provided with an R-C contact protection circuit. Figure 2 illustrates the range of safe operating loads which can be tolerated without additional contact protection external to the CCØ sub-system. Reliable, long-life operation will result provided that the current through the contacts just prior to opening and the peak voltage across the contacts as they open both lie within the shaded area of Figure 2. Switching of inductive loads such as small low energy relay coils (10 volt-amperes or less) at supply voltages in the 24 to 120 volt D.C. or A.C. RMS range will not generally result in transient voltages exceeding that of Figure 2. However, larger inductive loads must have additional remote protective circuits for limiting the inductive energy to the relay contacts. Diode clamps around all D.C. inductive loads are recommended as good general practice.

When using contact outputs to control AC devices, it must be remembered that a small amount of leakage current due to the R-C suppressor circuit will be present when the contacts are open. Refer to 2CØ printed circuit module description for more details concerning the leakage current.



CCO RELAY CONTACT RATINGS
Figure 2

C. Output rates and timing - Contact closure output relays are grouped into registers of fourteen. Outputs occur under program control one register at a time, so that the states of all fourteen relays within a given register can be changed simultaneously. Once set, a relay will remain set until another output causes it to be cleared. Within a given register, one or more relays may be set, cleared, or remain unchanged when an output occurs. Five milliseconds must elapse between outputs of individual registers to allow for relay settling times and program response time. Thus, outputs can occur at a maximum rate of 200 registers per second, and since one register contains fourteen relays this is equivalent to 2800 individual contact output points per second. This specification holds provided no attempt is made to change the state of any particular one of the relays more often than once every ten milliseconds.

In actual practice, output rates will vary and will be dependent upon program control.

III. CIRCUIT OPERATION

A. Functional Description

Contact closure output relays are combined in groups of fourteen, with each group of fourteen being referred to as a contact output "register". Outputs occur one

register at a time, so that the state of all fourteen relays within a register can be changed simultaneously. Each register has a word address and a channel address, or more precisely a SET channel address and a RESET channel address. Thus, a particular register is uniquely defined by the specification of two numbers, a word and a channel address. Any output on a computer channel must be accompanied by a fourteen bit "data word". Corresponding to each bit of the output data is one of the fourteen relays within the CCØ register. Thus a particular CCØ relay is uniquely defined by the specification of three numbers, a word and a channel and a bit.

The following example shows the state of a relay register before and after an output, along with the data word which caused the change. Note that for each bit of the data word which is a one, a corresponding relay is set, and for each bit which is a zero, a relay is reset. The final state of the CCØ relay register does not depend on its initial state, but depends only on the output data. When both ones and zeros are transferred, it is said that the data word is "copied" into the register. The "copy word" transfer is equivalent to a "copy ones" transfer followed by a "copy zero's" transfer.

	BIT	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
INITIAL STATE OF REGISTER		S	S	S	S	S	S	S	R	R	R	R	R	R	R	S=SET RELAY R=RESET RELAY
DATA WORD		1	0	1	0	1	0	1	0	1	0	1	0	1	0	
FINAL STATE OF REGISTER		S	R	S	R	S	R	S	R	S	R	S	R	S	R	

In order to copy a data word into a CCØ register, two outputs are actually required. Each CCØ relay has a set coil and a reset coil, a set channel and a reset channel. The data is first output on the set channel, then complemented (i.e. replace ones by zeros and zeros by ones) and output on the reset channel. For each "one" output on the set channel a relay is set, while for each "one" output on the reset channel a relay is reset. The two outputs occur under hardware lockout and are always done very close together in time (18 microseconds).

1. Data word is output on set channel.

2. Data word is complemented.

3. Complemented data word is output on reset channel.

	BIT	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INITIAL STATE OF REGISTER		S	S	S	S	S	S	S	R	R	R	R	R	R	R
DATA OUTPUT SET CHANNEL		1	0	1	0	1	0	1	0	1	0	1	0	1	0
DATA OUTPUT RESET CHANNEL		0	1	0	1	0	1	0	1	0	1	0	1	0	1
FINAL STATE OF REGISTER		S	R	S	R	S	R	S	R	S	R	S	R	S	R

S= SET RELAY
R= RESET RELAY

For convenience, the reset channel is always chosen adjacent to and one less than the set channel.

After a four millisecond time delay to allow for delay setting times, an interrupt is generated to request another output. Within 5 milliseconds the second register will be output by the computer.

Figure 3 is an illustration of the three dimensional nature of the CCØ address matrix. All of the relays in a given fourteen bit register have the same word address. In addition, the set and reset coils of a relay will always have the same word and bit address, but their channel addresses will differ by one.

Circuit Description

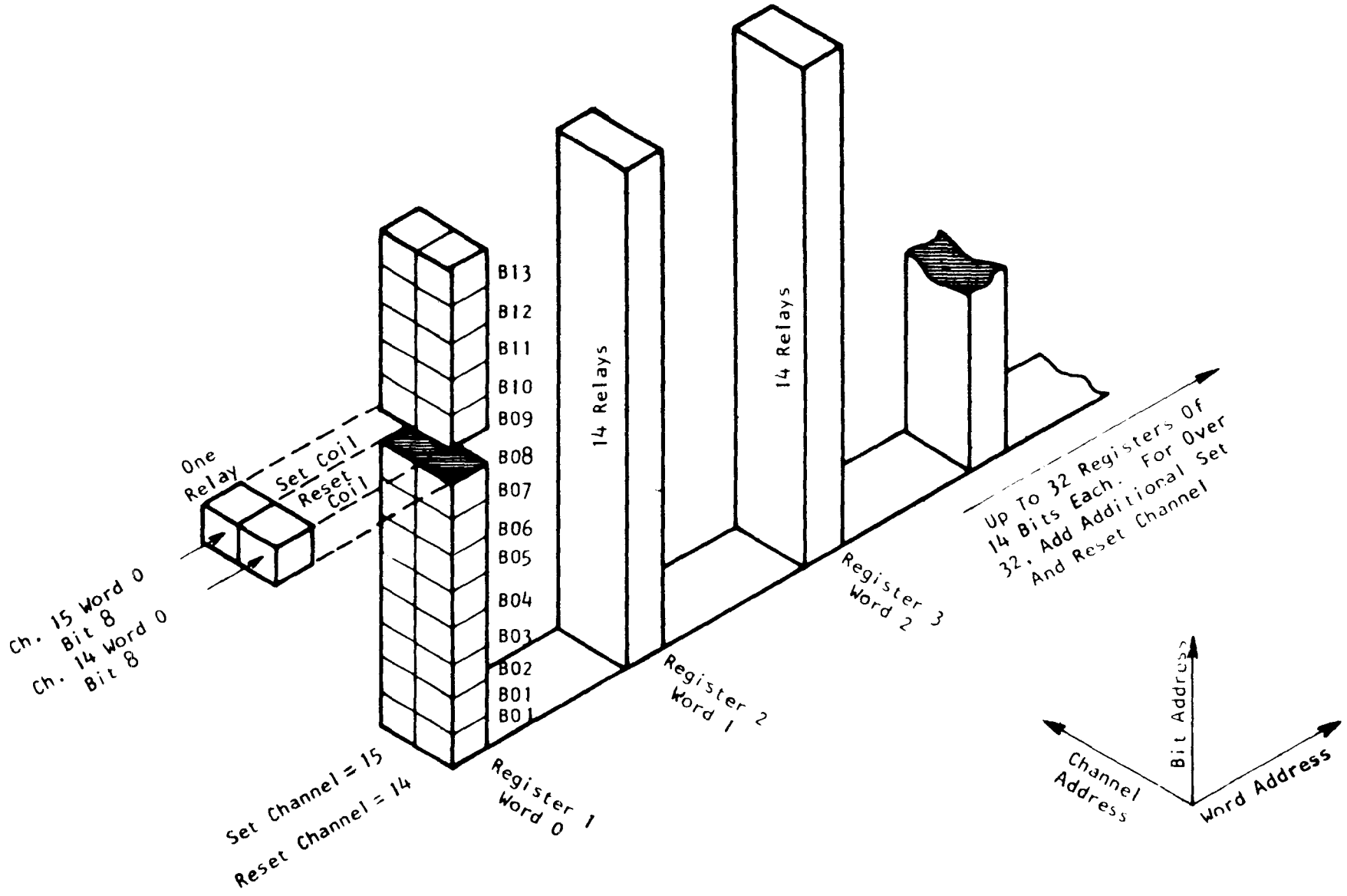
Refer to 867C560 which is a diagram of the circuitry required to set and reset one particular CCØ relay. The address of the relay pictured is word 0, set channel 15 (reset 14), bit 0. For simplicity only one relay and its associated driver are shown, so the following points are listed to place the diagram in its proper perspective:

1. One relay is shown but there are thirteen other relays in the same register which can all change state simultaneously along with the one shown. There may also be many other registers.

2. One set and one reset channel driver circuits are shown, but there are thirteen set and thirteen reset channel driver circuits not shown.

3. Only one word driver circuit is shown, but there are as many word drivers required as there are relay registers.

4. The power supply switch shown is the only one required no matter how large the total number of relays.



CCØ MULTIPLEXER ADDRESS BUILDUP
Figure 3

It is recommended that the reader refer to the description of the WD, CD, CØ, and P3 printed circuit modules before attempting to understand how they work together as in 867C560.

The word and channel drivers use silicon controlled rectifier (SCR's) to "route" current to the particular relay being addressed. An SCR is simply a "switch" which is either closed to pass current, or open to block current. Once set, or turned on, an SCR will remain closed and pass current until something in series with it "opens up" and stops the current flow. Once the flow of current through the SCR stops, no more current will flow until it is again set, or turned on.

To pick a relay, one word SCR and one channel SCR are turned on. Current will flow from the positive voltage supply through the word SCR, through the relay coil, through the channel SCR and through the power supply switch to ground. Current will continue to flow until the power supply switch "opens up", at which time current flow will cease and cause the SCR's to turn off.

Suppose that the relay pictured is in a reset state, and it is desired to set it. The computer will output bit 0 on channel 15 with word 0 selected. This will cause the word O SCR and the channel 15 bit O SCR to turn on and conduct current. Current will flow from pin H1 through the word O SCR and out pin X34. From X34 current flows through a cable which connects to the X-panel and through back-of-panel wiring to pin H17. Only one relay is shown but a total of 14 relays are connected to pin H17. The particular relay selected, and whether set or reset coil, depends on which channel bit SCR is turned on. In our example the channel 15 bit O SCR is turned on, so current will flow through the set coil, out pin L18, and back to the D-panel through the interpanel cable and into pin X35. From X35, current flows through the SCR and out pin X1. Tracing through the card edge jumper wiring, current flows into pin X9 of the power supply switch. The power supply switch transistor is conducting and completes the path to ground. As long as the power supply switch transistor remains ON, current will continue to flow. When it opens momentarily, current flow will cease and cause the SCR's to turn off.

Having discussed the circuitry which causes current to flow through a particular relay coil, the circuitry concerned with timing can be discussed. As was seen, all relay current flows to ground through a power supply switch whose function is to open up the current path at the proper time once the relay coil has been energized. The output of the power supply switch, pin X9, is normally at ground potential, while the trigger input, pin X12, is normally at +26 volts. If the trigger input pin is grounded, a time delay will expire, and at the end of the time delay the power supply switch output will momentarily open up. The output remains open for about 110 microseconds, just long enough to cause the SCR's to reset. The time delay between the grounding of the input and the opening of the output is adjustable by means of a potentiometer on the power supply switch printed circuit module. Also, when the time delay expires, an interrupt is generated at pin X16.

The trigger input to the power supply switch is grounded each time an output to a CCØ register is done. This initiates the time delay which expires, and then interrupts the computer to request that another output be done. Each channel driver has a trigger SCR which turns on every time an output is done on that channel. The function of this SCR is to ground the trigger input of the power supply switch. In 867C560, the trigger SCR connects from pin X18 of the channel driver to pin X12 of the power supply switch.

Following is a brief summary of the above:

1. The computer does an output which causes a word SCR and a channel bit SCR to turn on. This allows current to flow through a relay coil.

2. Simultaneously, a trigger SCR is turned on which grounds the trigger input of the power supply switch.

3. Four milliseconds later, the power supply switch opens up and causes all SCR's to be reset. At the same time, an interrupt is generated to inform the computer that another output may be done.

C. Adjustment

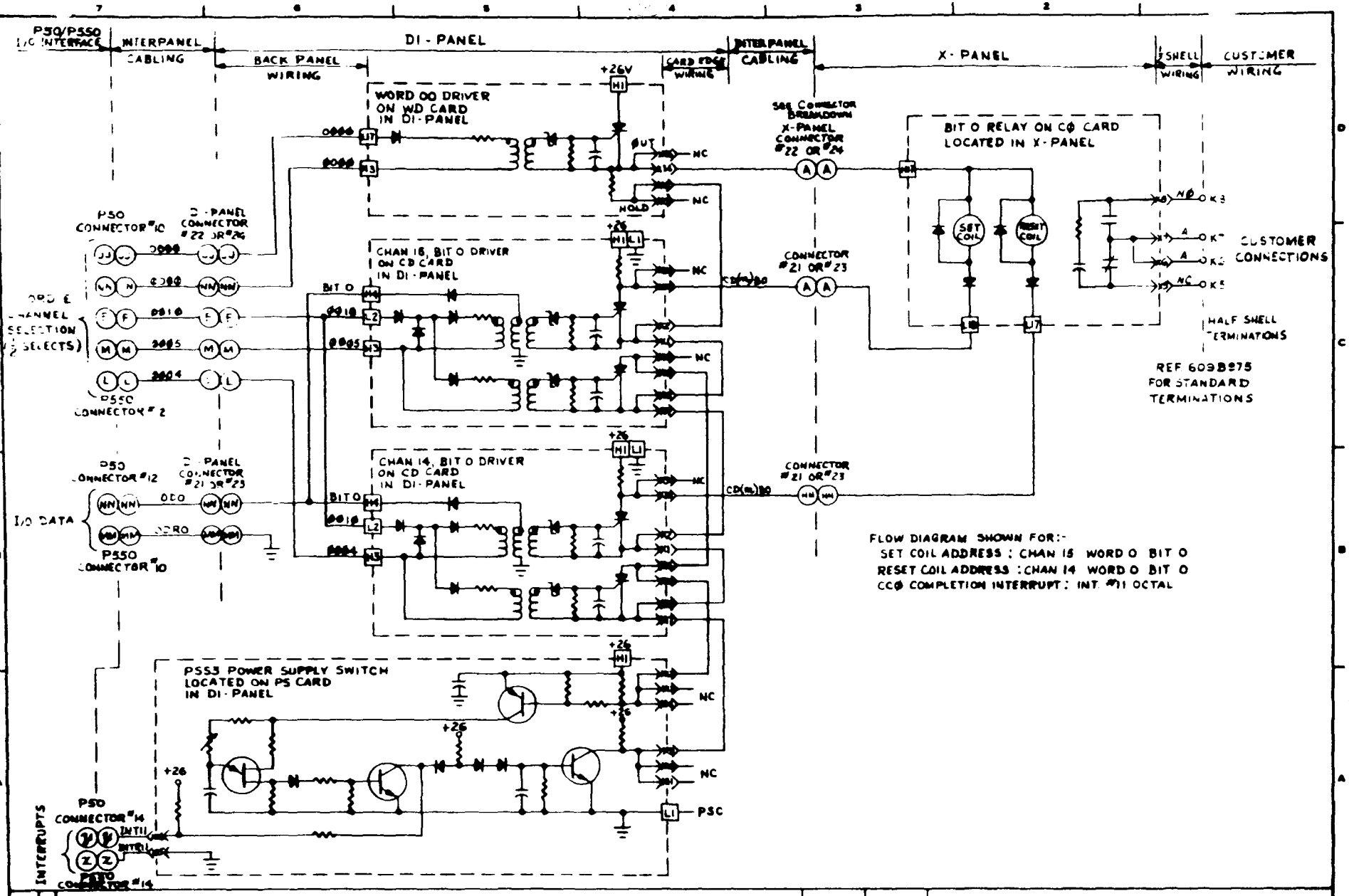
There is only one adjustment in the contact closure output sub-system. It is the adjustment of the time delay between an output and the occurrence of the CCØ completion interrupt. The adjustment is made by means of a potentiometer located on the PS power supply switch printed circuit module.

The adjustment should be made such that the time between the computer output and the generation of the completion interrupt equals 4.0 milliseconds.

The adjustment can be made using an oscilloscope by observing that the interrupt is generated 4.0 milliseconds after the power supply switch trigger is grounded.

If no oscilloscope is available it is possible to use the computer itself as a tool to accomplish the adjustment. This may be done by doing an output, and then incrementing a counter within the computer memory, with a stop command in the interrupt location. When the computer is started an output will occur and then the computer will stop when the interrupt is received. The accumulated count will then be proportional to the time delay between the output and the interrupt.

The oscilloscope method is generally preferred since it can be done "on-line" without disturbing existing programs or temporarily shutting down the system.



10-12

WESTINGHOUSE ELECTRIC CORPORATION			
PRODAC 50-550 SERIES			
TITLE: CØ FLOW SCHEMATIC DIAGRAM		SUB 1	
DRWN M. OLINICK	APP'D	867C560	
COMPUTER SYSTEMS DIVISION			

ANALOG OUTPUT SUBSYSTEM

I. GENERAL DESCRIPTION

The AØ Subsystem uses special contact closure outputs to switch resistors in a digital potentiometer to convert a digital input to an analog output. Two main categories exist:

1. Cards with 7 relays where the cards can be used in place of a CØ card.
2. Cards with more than 7 relays where an X panel with space for 16 analog outputs (16 words) replace 2 - X panels of CØ cards driven by the same word driver with 2 cards per word.

Figures 1, 2 and 3 show typical AØ and AØ/CCØ subsystems in block diagram form.

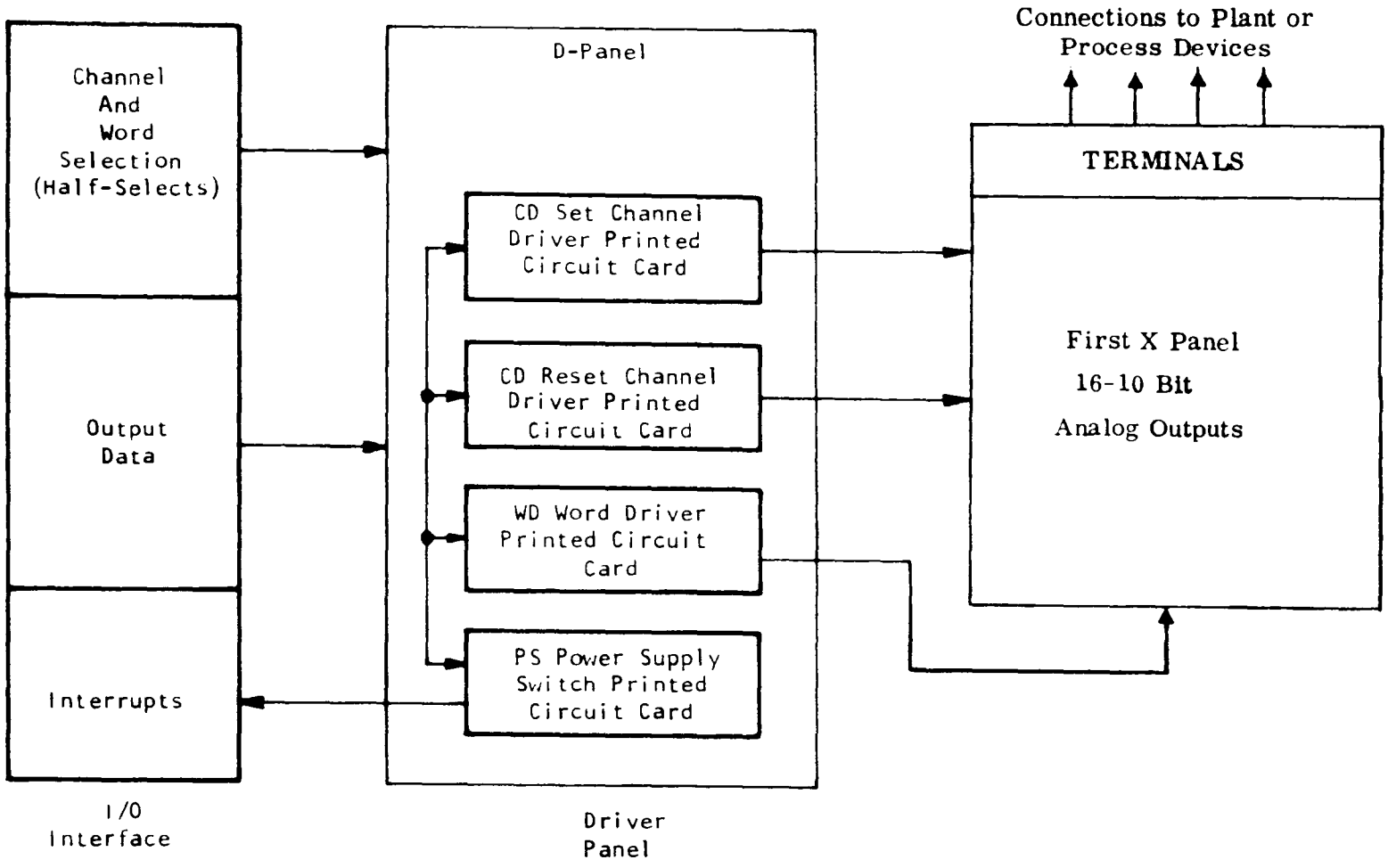
II. SPECIFICATIONS

A. Input Requirements - As with all other subsystems, the AØ subsystem interface with the computer central processor itself is via computer word and channel selection circuitry. The only inputs to the AØ subsystem are from these computer I/Ø interface circuits.

B. Contact Specifications - All contacts for analog outputs are mercury-wetted, non-bridging (except for reversing) and are bounce free. They switch resistors which draw current in the milliampere range and have no R-C contact protection, except for reversing.

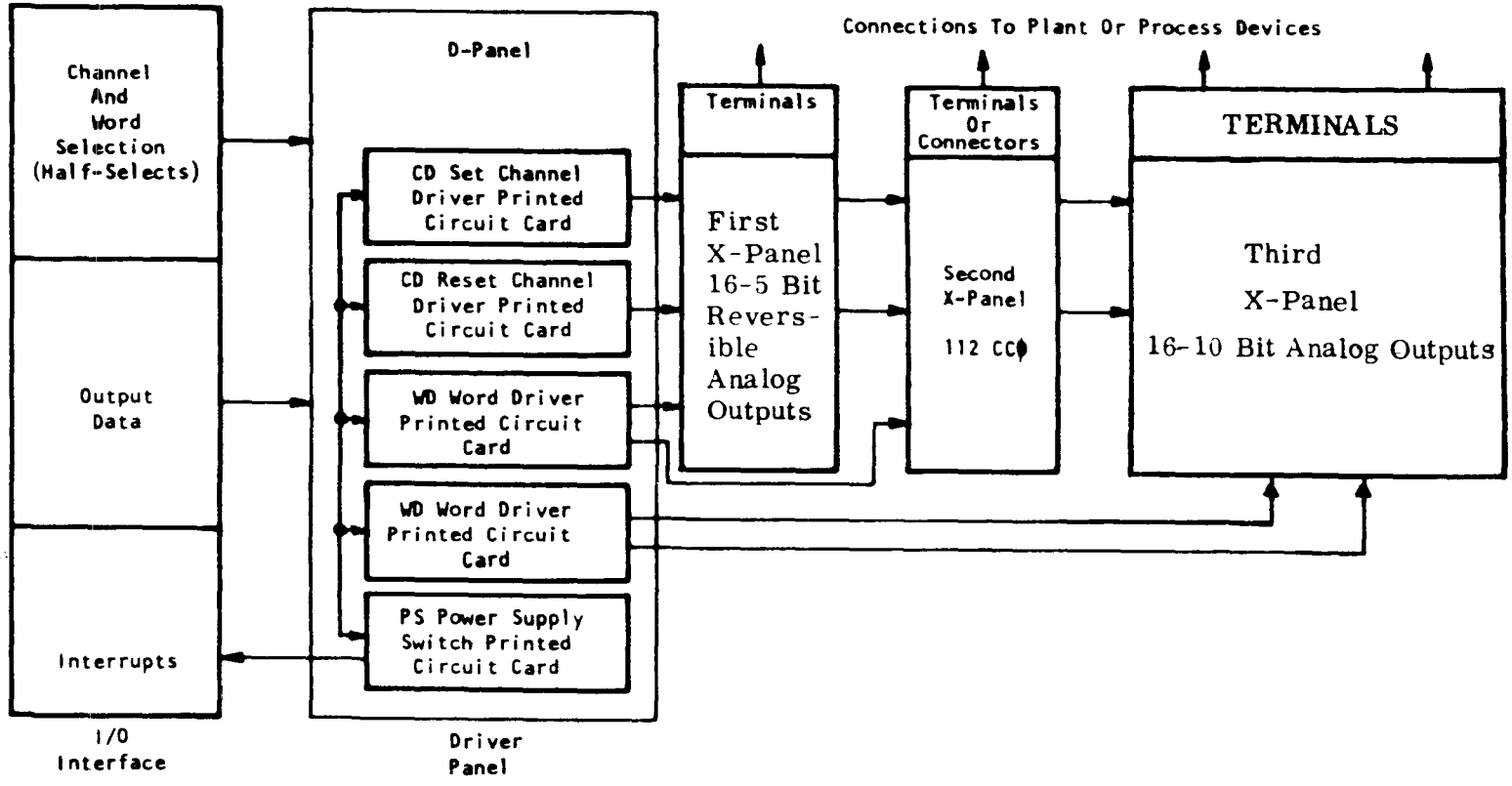
C. Output Rates and Timing - 1AØ2 cards (5-bit reversible) are grouped in twos to form registers of fourteen. Each 1AØ1 or 1AØ3 (10 or 11 bit) cards will serve as a fourteen bit register but will not furnish the 4 or 3 high order bit relays.

Outputs occur under program control one register at a time, so that the

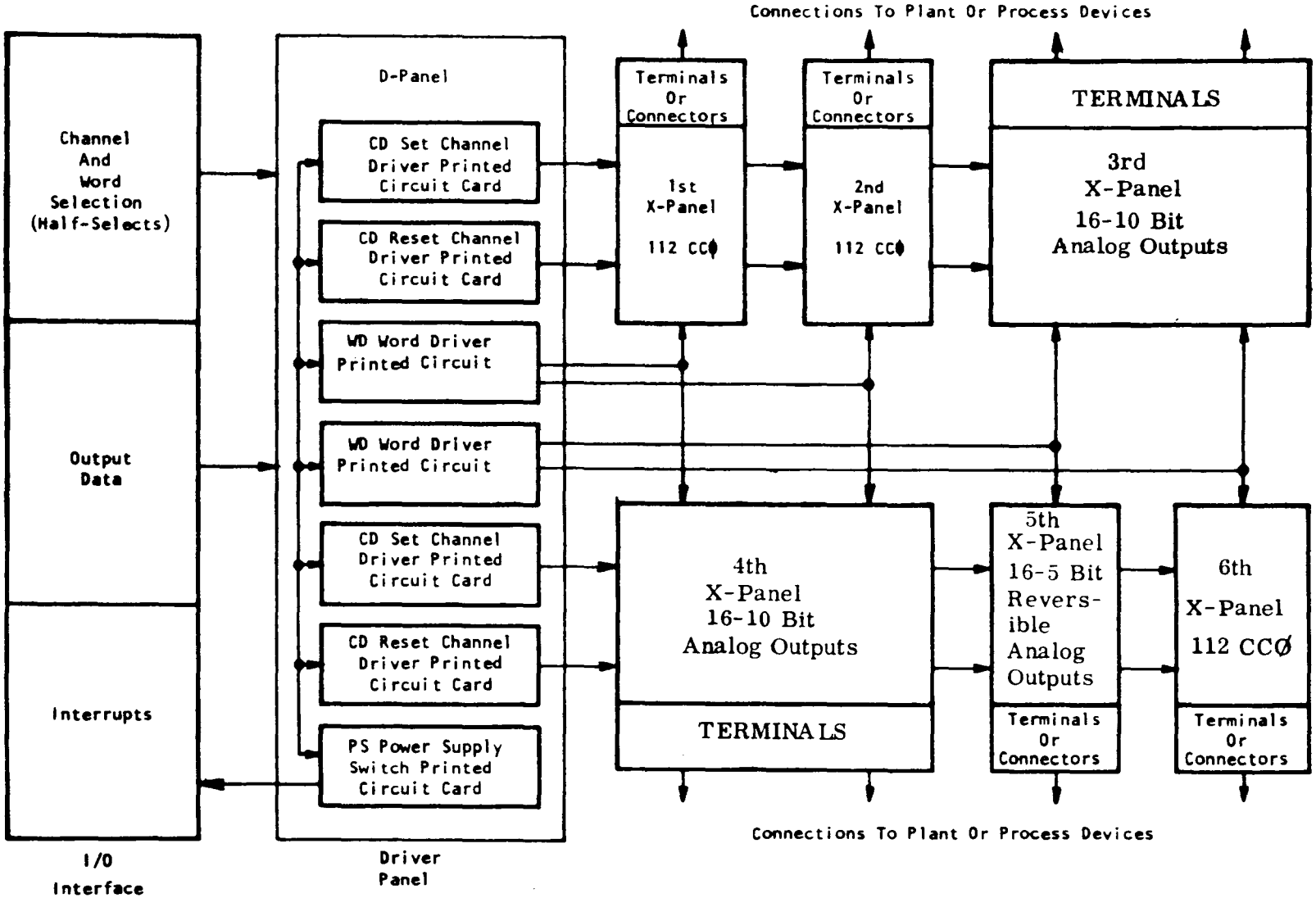


AØ SUBSYSTEM OF 16-10 BIT OUTPUTS

Figure 1



AØ & CCØ SUBSYSTEM OF 112 CCØ POINTS & 16-5 BIT REVERSIBLE & 16-10 BIT ANALOG OUTPUTS
Figure 2



AØ & CCØ SUBSYSTEM OF 336 CCØ POINTS & 16-5 BIT REVERSIBLE & 32-10 BIT ANALOG OUTPUTS
Figure 3

states of all relays within a given register can be changed simultaneously. Once set, a relay will remain set until another output causes it to be cleared. Within a given register, one or more relays may be set, cleared, or remain unchanged when an output occurs. Five milliseconds must elapse between outputs of individual registers to allow for relay setting times and program response time. Thus, outputs can occur at a maximum rate of 200 registers per second. This specification holds provided no attempt is made to change the state of any particular one of the relays more often than once every ten milliseconds.

In actual practice, output rates will vary and will be dependent upon program control.

III. CIRCUIT DESCRIPTION

A. Functional Description

Analog output relays are combined in groups of up to 1 or 2 cards per word, with each group being referred to as an analog output "register". Outputs occur one register at a time, so that the state of all fourteen relays within a register can be changed simultaneously. Each register has a word address and a channel address, or more precisely a SET channel address and a RESET channel address. Thus, a particular register is uniquely defined by the specification of two numbers, a word and a channel address. Any output on a computer channel must be accompanied by a fourteen bit "data word". Corresponding to each bit of the output data is one of the fourteen relays within the AØ register. Thus a particular AØ relay is uniquely defined by the specification of three numbers, a word, a channel, and a bit.

The following example shows the state of a relay register before and after an output, along with the data word which caused the change. Note that for each bit of the data word which is a one, a corresponding relay is set, and for each bit which is a zero, a relay is reset. The final state of the AØ relay register does not depend on its initial state, but depends only on the output data. When both ones and zeros are transferred, it is said that the

data word is "copied" into the register. The "copy word" transfer is equivalent to a "copy ones" transfer followed by a "copy zero's" transfer.

BIT	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
INITIAL STATE OF REGISTER	S	S	S	S	S	S	S	R	R	R	R	R	R	R	R=RESET RELAY
DATA WORD	1	0	1	0	1	0	1	0	1	0	1	0	1	0	S=SET RELAY
FINAL STATE OF REGISTER	S	R	S	R	S	R	S	R	S	R	S	R	S	R	

In order to copy a data word into a AØ register, two outputs are actually required. Each AØ relay has a set coil and a reset coil, a set channel and a reset channel. The data is first output on the set channel, then complemented (i.e., replace ones by zeros and zeros by ones) and output on the reset channel. For each "one" output on the set channel a relay is set, while for each "one" output on the reset channel a relay is reset. The two outputs occur under hardware lockout and are always done very close together in time (18 microseconds).

1. Data word is output on set channel.
2. Data word is complemented.
3. Complemented data word is output on reset channel.

BIT	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
INITIAL STATE OF REGISTER	S	S	S	S	S	S	S	R	R	R	R	R	R	R	R=RESET RELAY
DATA OUTPUT SET CHANNEL	1	0	1	0	1	0	1	0	1	0	1	0	1	0	S=SET RELAY
DATA OUTPUT RESET CHANNEL	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
FINAL STATE OF REGISTER	S	R	S	R	S	R	S	R	S	R	S	R	S	R	

For convenience, the reset channel is always chosen adjacent to and one less than the set channel.

After a four millisecond time delay to allow for delay setting times, an interrupt is generated to request another output. Within 5 milliseconds the second register will be output by the computer.

Figure 4 is an illustration of the three dimensional nature of the AØ address matrix. All of the relays in a given fourteen bit register have the same word address. In addition, the set and reset coils of a relay will always have the same word and bit address, but their channel addresses will differ by one.

B. Circuit Operation

Refer to 867C560 which is a diagram of the circuitry required to set and reset one particular CCØ relay, the coil circuits of which are a duplicate of the AØ coil circuits. The address of the relay pictured is word 0, set channel 15 (reset 14), but 0. For simplicity only one relay and its associated driver are shown, so the following points are listed to place the diagram in its proper perspective:

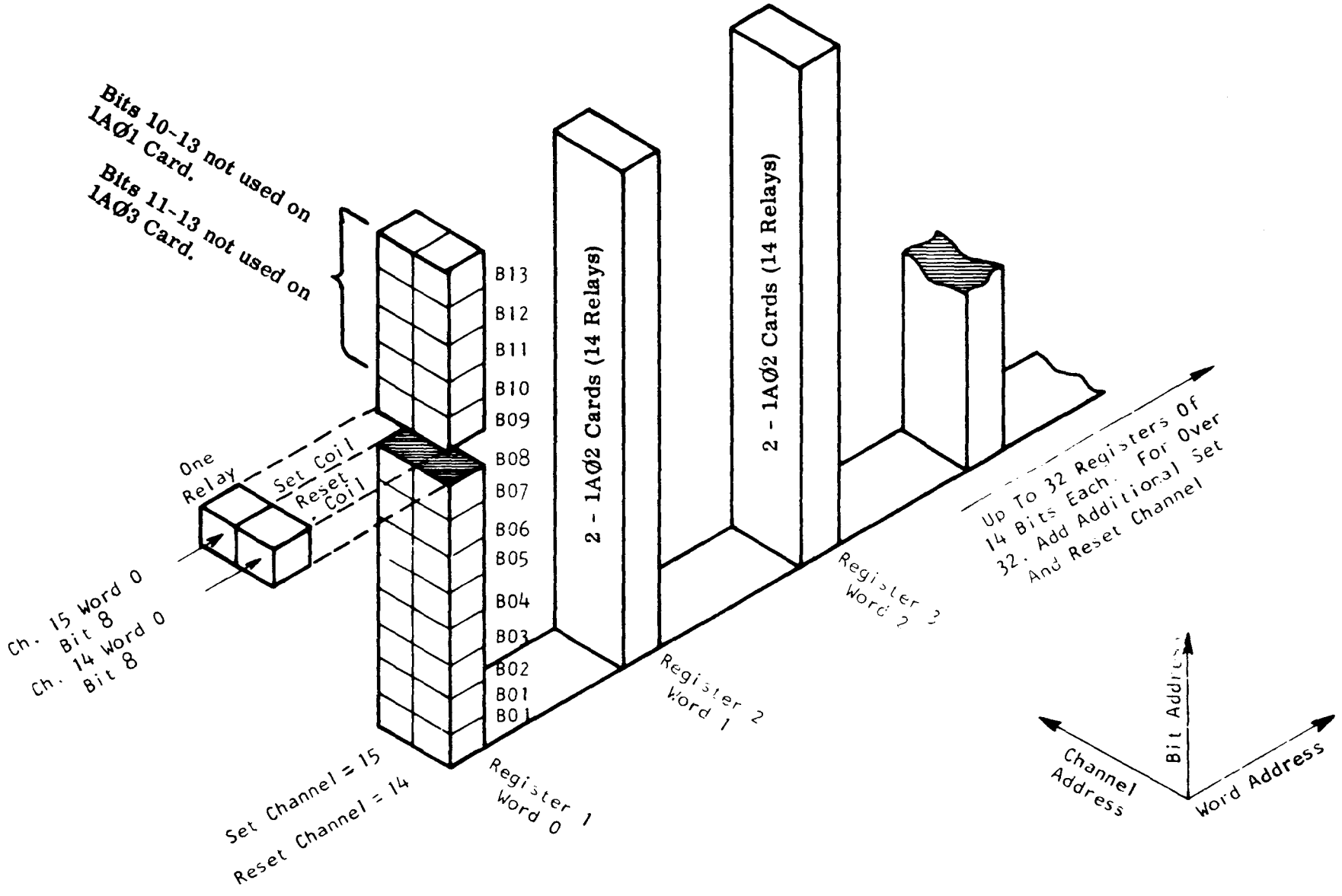
1. One relay is shown but there are up to thirteen other relays in the same register which can all change state simultaneously along with the one shown. There may also be many other registers.

2. One set and one reset channel driver circuit is shown, but there are thirteen set and thirteen reset channel driver circuits not shown.

3. Only one word driver circuit is shown, but there are as many word drivers required as there are relay registers per channel.

4. The power supply switch shown is the only one required no matter how large the total number of relays, including both AØ and CCØ relays.

It is recommended that the reader refer to the description of the WD, CD, AØ, and PS printed circuit modules before attempting to understand how they work together as in 867C560.



AØ MULTIPLEXER ADDRESS BUILDUP

Figure 4

The word and channel drivers use silicon controlled rectifier (SCR's) to "route" current to the particular relay being addressed. An SCR is simply a "switch" which is either closed to pass current, or open to block current. Once set, or turned on, an SCR will remain closed and pass current until something in series with it "opens up" and stops the current flow. Once the flow of current through the SCR stops, no more current will flow until it is again set, or turned on.

To pick a relay, one word SCR and one channel SCR are turned on. Current will flow from the positive voltage supply through the word SCR, through the relay coil, through the channel SCR and through the power supply switch to ground. Current will continue to flow until the power supply switch "opens up", at which time current flow will cease and cause the SCR's to turn off.

Suppose that the relay pictured is in a reset state, and it is desired to set it. The computer will output bit 0 on channel 15 with word 0 selected. This will cause the word 0 SCR and the channel 15 bit 0 SCR to turn on and conduct current. Current will flow from pin H1 through the word 0 SCR and out pin X34. From X34 current flows through a cable which connects to the X-panel and through back-of-panel wiring to pin H17. Only one relay is shown but up to 14 relays are connected to pin H17. The particular relay selected, and whether set or reset coil, depends on which channel bit SCR is turned on. In our example the channel 15 bit 0 SCR is turned on, so current will flow through the set coil, out pin L18, and back to the D-panel through the interpanel cable and into pin X35. From X35, current flows through the SCR and out pin X1. Tracing through the card edge jumper wiring, current flows into pin X9 of the power supply switch. The power supply switch transistor is conducting and completes the path to ground. As long as the power supply switch transistor remains ON, current will continue to flow. When it opens momentarily, current flow will cease and cause the SCR's to turn off.

Having discussed the circuitry which causes current to flow through a particular relay coil, the circuitry concerned with timing can be discussed.

As was seen, all relay current flows to ground through a power supply switch whose function is to open up the current path at the proper time once the relay coil has been energized. The output of the power supply switch, pin X9, is normally at ground potential, while the trigger input, pin X12, is normally at +26 volts. If the trigger input pin is grounded, a time delay will expire, and at the end of the time delay the power supply switch output will momentarily open up. The output remains open for about 110 microseconds, just long enough to cause the SCR's to reset. The time delay between the grounding of the input and the opening of the output is adjustable by means of a potentiometer on the power supply switch printed circuit module. Also, when the time delay expires, an interrupt is generated at pin X16.

The trigger input to the power supply switch is grounded each time an output to a CCØ or AØ register is done. This initiates the time delay which expires, and then interrupts the computer to request that another output be done. Each channel driver has a trigger SCR which turns on every time an output is done on that channel. The function of this SCR is to ground the trigger input of the power supply switch. In 867C560, the trigger SCR connects from pin X18 of the channel driver to pin X12 of the power supply switch.

Following is a brief summary of the above:

1. The computer does an output which causes a word SCR and a channel bit SCR to turn on. This allows current to flow through a relay coil.
2. Simultaneously, a trigger SCR is turned on which grounds the trigger input of the power supply switch.
3. Four milliseconds later, the power supply switch opens up and causes all SCR's to be reset. At the same time, an interrupt is generated to inform the computer that another output may be done.

C. Adjustment

Timing

There is only one timing adjustment in the analog output subsystem. It

is the adjustment of the time delay between an output and the occurrence of the CCØ or AØ completion interrupt. The adjustment is made by means of a potentiometer located on the PS power supply switch printed circuit module.

The adjustment should be made such that the time between the computer output and the generation of the completion interrupt equals 4.0 milliseconds.

The adjustment can be made using an oscilloscope by observing that the interrupt is generated 4.0 milliseconds after the power supply switch trigger is grounded.

If no oscilloscope is available it is possible to use the computer itself as a tool to accomplish the adjustment. This may be done by doing an output, and then incrementing a computer within the computer memory, with a stop command in the interrupt location. When the computer is started an output will occur and then the computer will stop when the interrupt is received. The accumulated count will then be proportional to the time delay between the output and the interrupt.

The oscilloscope method is generally preferred since it can be done "on-line" without disturbing existing programs or temporarily shutting down the system.

Voltage

The output supply voltage must be set as described under the card descriptions. Also, series dropping resistors and zero suppression resistors may be added as described. The remote sensing feature available on some power supplies may be used to regulate the voltage at the taper pin busses rather than at the power supply terminals.

MULTIPLEXED CONTACT CLOSURE INPUT SYSTEM

I. GENERAL DESCRIPTION

The multiplexed Contact Closure Inputs (MPLX CCI) are used to interrogate the status of process contacts. The multiplexing provides a low cost method of interrogating a large number of plant (or process) contacts.

Figure #1 is a functional diagram of a multiplexed CCI system that can accommodate a maximum of 781 contacts. Each pair of CM relays are wired to two sets of 14 plant contacts. One Channel Driver (CD) card can drive 14 pairs of CM relays. The other side of the plant contacts are tied together to provide two final sets of 14 data lines. Each set of 14 data lines is wired to an individual Contact Buffer (CB) card.

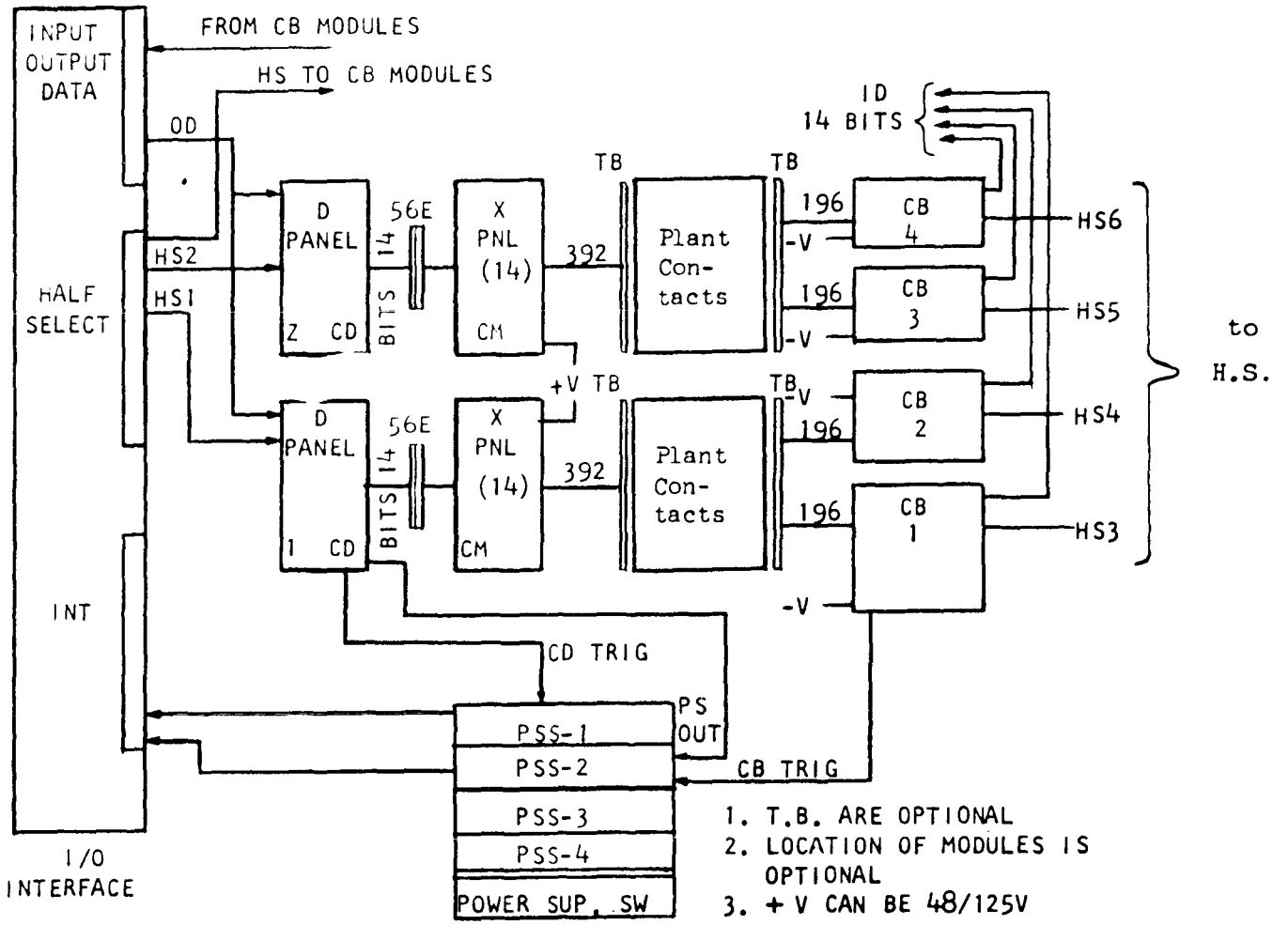


Figure 1

II. SPECIFICATIONS

A. Input Requirements

Input is via +48 or +125 VDC being presented to the CB card by customer's process contacts being closed.

A minimum of 10 milliseconds settling time is required for multiplexing and filtering. This 10 milliseconds is required for each group of 28 contacts in any block of 392 contact inputs. The maximum scan rate is therefore 2800 CCI/second per multiplexed CCI panel. Since it is possible to get 2 multiplexed CCI panels, the maximum system scan rate is 5600 CCI/second.

B. Power Requirements

The +48 or +125 volts dc can be supplied with the system or may be provided by the user. The voltage should be no more than ±10% of nominal value. The capacity of the supply will be dependent upon the total number of inputs to be supplied.

III. CIRCUIT OPERATION

A. General Instruction Format

The selection of a particular 14 bit contact input word is organized on a one word per bit basis. For each bit in the CCI address word, there is a corresponding 14 bit CCI data word.

To bring contact inputs into the computer, a sequence of two instructions is required, an output followed by an input. The output instruction which must be executed in the direct mode contains in bits 0-7 of the instruction word, the CCI channel address. The output data register must contain the CCI address word.

Caution is required on the output command since selection of more than one output bit will cause more than one process contact register to present itself to the input (CB module) register.

As mentioned before, an input instruction is part of the sequence of instructions required to sample plant contact input status. The execution of an input instruction in the direct mode with the low order bits of the instruction word specifying the input channel number will result in input data to the computer of the contact input data word addressed by the previous output instruction.

B. Interrupts

If more than 392 process contacts are being used, a second multiplexed CCI system, wired independent of the first, is used.

However, since only the first system will generate input request and output request interrupts, the second group of 392 process contacts must be called for first, then the first group.

C. Circuit Description

Drawing 867C601 is a flow diagram of the multiplexed CCI system.

If we assume that channel 40 is used to select the CD module, the CD module three winding transformer will be pulsed on pins L2 and H3, now if bit 13 was selected as the output bit, the SCR, S1-1 will be triggered thus allowing the CM relay, MA-1 to be picked. At the same time, the channel driver trigger circuit will be turned on and allows the power supply switch (PSS-1) to start its action (see 2PS1 description for details) and to provide an input request interrupt in six milliseconds. The six milliseconds is the time delay set in the power supply switch circuit (PSS-1) to insure CM relay contact closure/open and CB module filter charge/discharge time.

With MA-1 closed, its contacts will close to a specific group of 14 process contacts. These process contacts will have either +48 or 125 volts on them depending upon the system.

The isolation diodes on the CM module prevent sneak paths to non-associated input bits.

The status of the contacts will determine whether or not this voltage is impressed across the CB module filter.

If the voltage is presented to the CB module and if the input instruction is called for (Channel 37, in our example) the information will be presented to the input data lines (here Bit 13: ID13 and IDR13).

At the same time the information is sent to the input data lines, the CB trigger circuit will cause its SCR to be turned on. This will cause PSS-2 to turn on and one millisecond later, an output request interrupt will be initiated to the I/O interface.

When the PSS-1 and PSS-2 switches supply the interrupts, this also allows the CD trigger SCR and CB trigger SCR to be reset. See 2PS1 card description for details.

D. Panel Configuration

Drawing 867C944 is a block diagram of the Panel Configuration.

The maximum number of multiplexed CCI per X (or Q) panel, is 392. As

mentioned previously, a second group of 392 CCI is available. This will be located on a second X (or Q) panel.

The X or Q panels will contain the CM modules, with the CB modules, the CD module and PS module usually located on a D panel.

To use 392 CCI, it is necessary to have 14 CM modules, 1-CD module, 2-CB modules and 1 power supply switch. For the second group of 392 CCI, a duplicate complement of modules as used in the first group, except for the Power Supply switch.

As noted previously, only the first group of 392 CCI will cause an interrupt.

A 15 AND A18			A 15 AND A18	
56 PIN ELCO	DESIGNATION		56 PIN ELCO	DESIGNATION
A	INT 20		k	INT 44
B	INTR 20		l	INTR 44
C	INTR 21		m	INTR 45
D	INT 21		n	INT 45
E	INT 22		p	INT 46
F	INTR 22		r	INTR 46
			s	INTR 47
J	INTR 23		t	INT 47
K	INT 23		u	INT 30
L	INT 24		v	INTR 30
M	INTR 24			
N	INTR 25		x	INTR 31
P	INT 25		y	INT 31
R	INT 26		z	INT 32
S	INTR 26		AA	INTR 32
			BB	INTR 33
U	INTR 27		CC	INT 33
V	INT 27		DD	INT 34
W	INT 40		EE	INTR 34
X	INTR 40			
Y	INTR 41		HH	INTR 35
Z	INT 41		JJ	INT 35
a	INT 42		KK	INT 36
b	INTR 42		LL	INTR 36
c	INTR 43		MM	INTR 37
d	INT 43		NN	INT 37

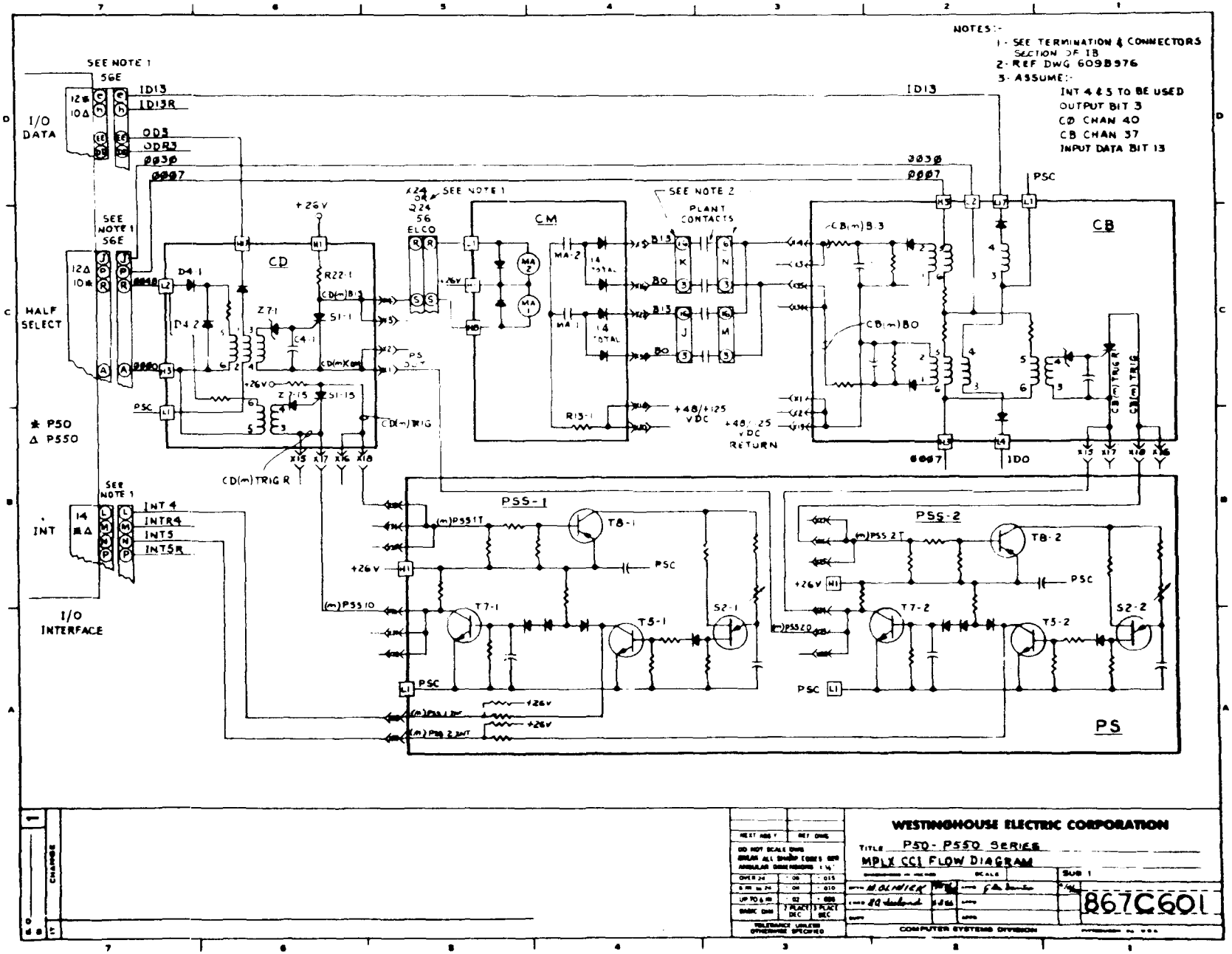
A16 AND A19	
56 PIN ELCO	DESIGNATION
A	INT 50
B	INTR 50
C	INTR 51
D	INT 51
E	INT 52
F	INTR 52
J	INTR 53
K	INT 53
L	INT 54
M	INTR 54
N	INTR 55
P	INT 55
R	INT 56
S	INTR 56
U	INTR 57
V	INT 57
W	INT 70
X	INTR 70
Y	INTR 71
Z	INT 71
a	INT 72
b	INTR 72
c	INTR 73
d	INT 73

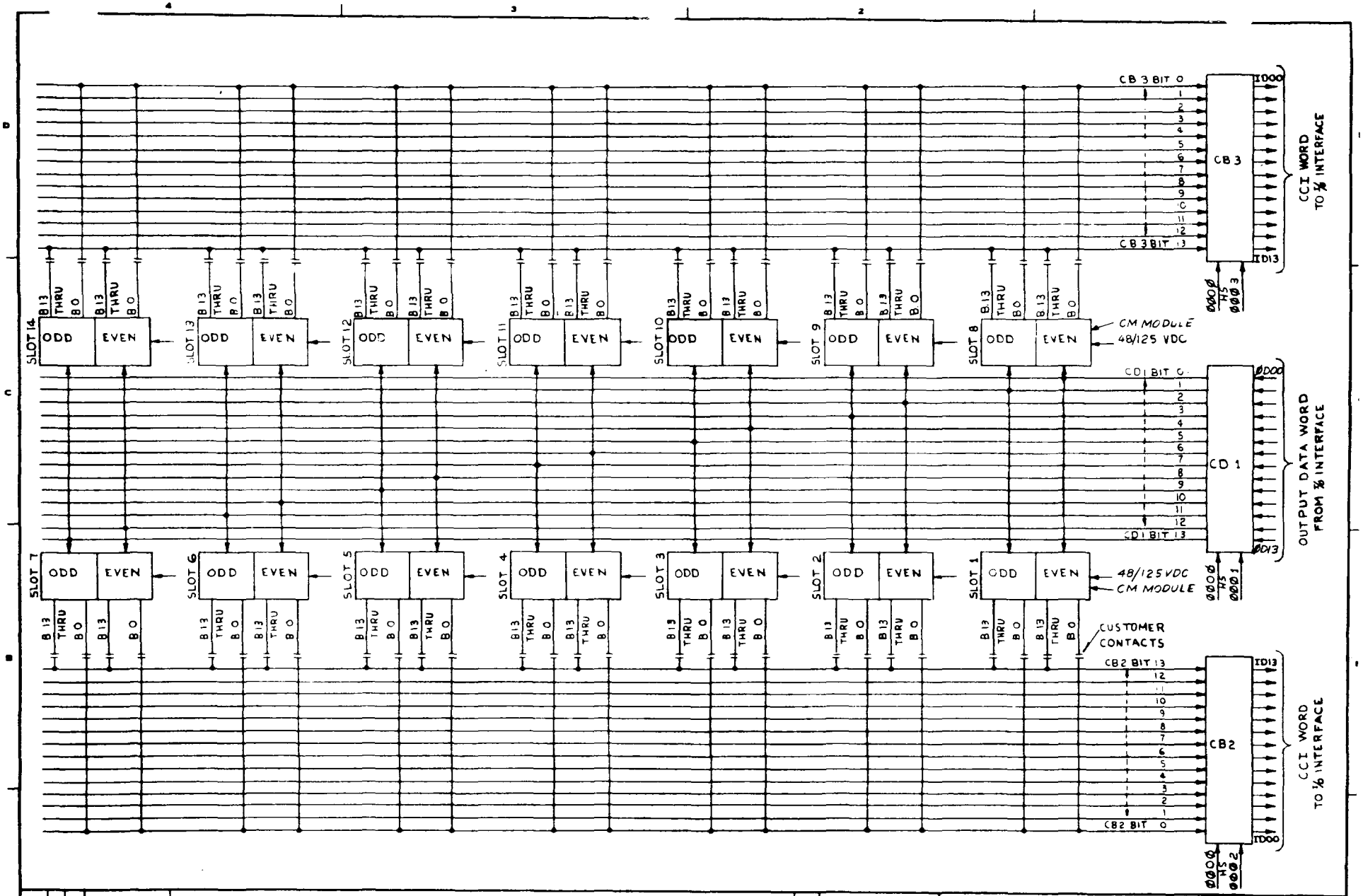
A16 AND A19	
56 PIN ELCO	DESIGNATION
k	INT 74
l	INTR 74
m	INTR 75
n	INT 75
p	INT 76
r	INTR 76
s	INTR 77
t	INT 77
u	INT 60
v	INTR 60
x	INTR 61
y	INT 61
z	INT 62
AA	INTR 62
BB	INTR 63
CC	INT 63
DD	INT 64
EE	INTR 64
HH	INTR 65
JJ	INT 65
KK	INT 66
LL	INTR 66
MM	INTR 67
NN	INT 67

E. Terminations

Drawing 609B976 sheets 1 and 2 define the terminations available for the multiplexed CCI system.

Connectors J, K, L and M are the Curtis Terminal Blocks, this is the most commonly used type, however, these can be Rowan blocks which have the same terminal markings or they can be Elco connectors as shown in the drawing.


NOTES:-
1- SEE TERMINATION & CONNECTORS SECTION OF IB
2- REF DWG 6098976
3- ASSUME:-
INT 4 & 5 TO BE USED
OUTPUT BIT 3
CD CHAN 40
CB CHAN 37
INPUT DATA BIT 13
I/O DATA
HALF SELECT
INT
I/O INTERFACE
* P50
Δ P550
CD
CM
CB
PS
PS5-1
PS5-2
PLANT CONTACTS
ELCO
+26V
+48/+125 VDC
+48/125 VDC RETURN
PSC
ID13
ID13R
OD3
OD3R
INT 4
INTR4
INT5
INT5R
WESTINGHOUSE ELECTRIC CORPORATION
TITLE P50-P550 SERIES
MPLX CCI FLOW DIAGRAM
867C601
COMPUTER SYSTEMS DIVISION



CHANGE	IT.	
1	AA11474	2

LOC ØDØØ HAS CDØØF
CCI ØØ13 HAS CD13
CM MODULE NOTE TO SLOT 8, 48/125VDC
SLOT 14 NOTE TO SLOT 1 WIRE NOT ON CONNECTOR
CHANGE 9-27-67
1-22-68

DO NOT SCALE DWG
MACHINED SURFACES
UNLESS OTHERWISE SPECIFIED
BREAK ALL SHARP EDGES .005
DEBURR ALL HOLES
ANGULAR DIMENSIONS ± .5°

OVER 24	± .06	± .015
6 IN. TO 24	± .04	± .010
UP TO 6 IN.	± .02	± .005
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.

TOLERANCE UNLESS OTHERWISE SPECIFIED

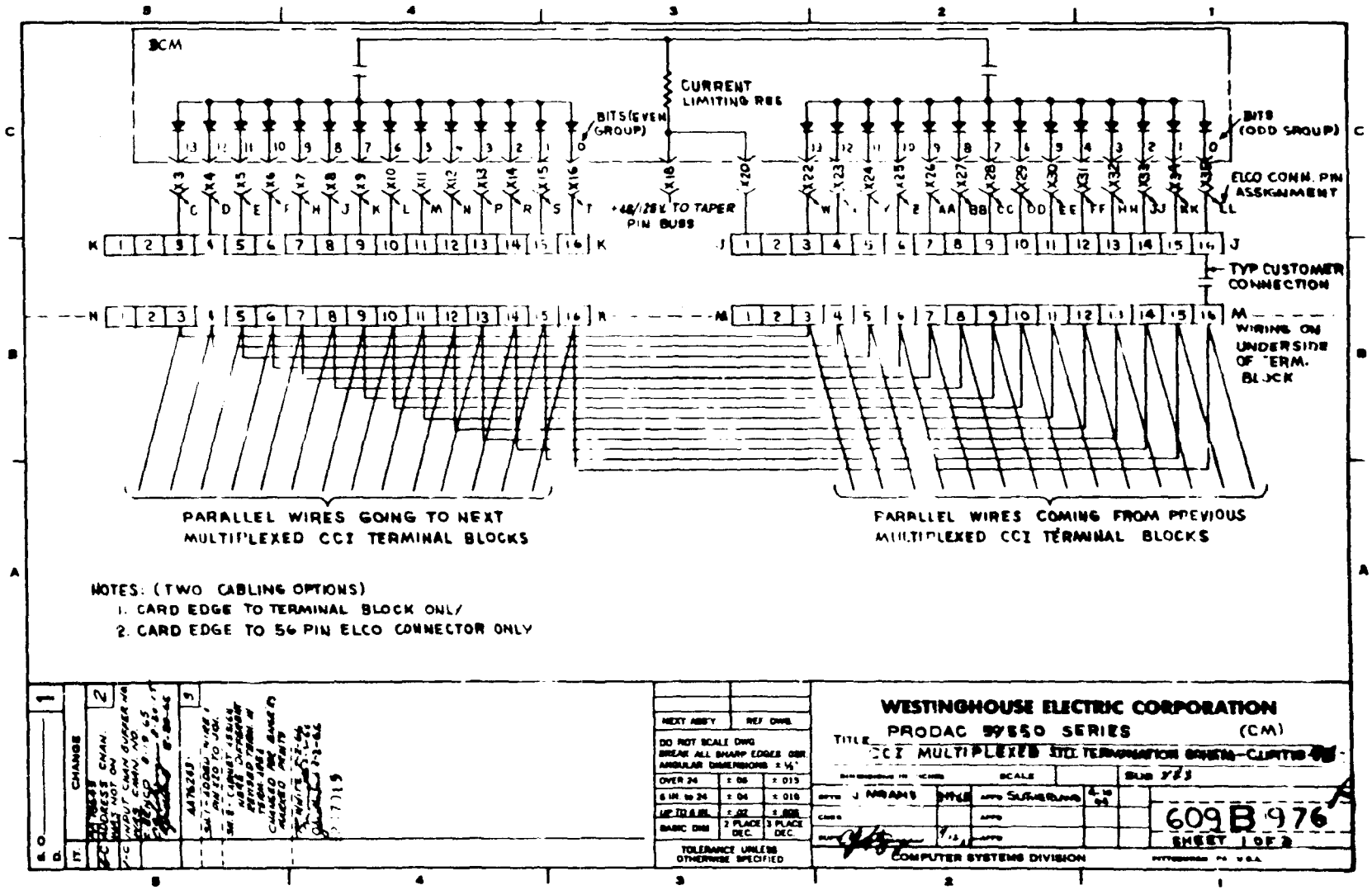
Westinghouse Electric Corporation

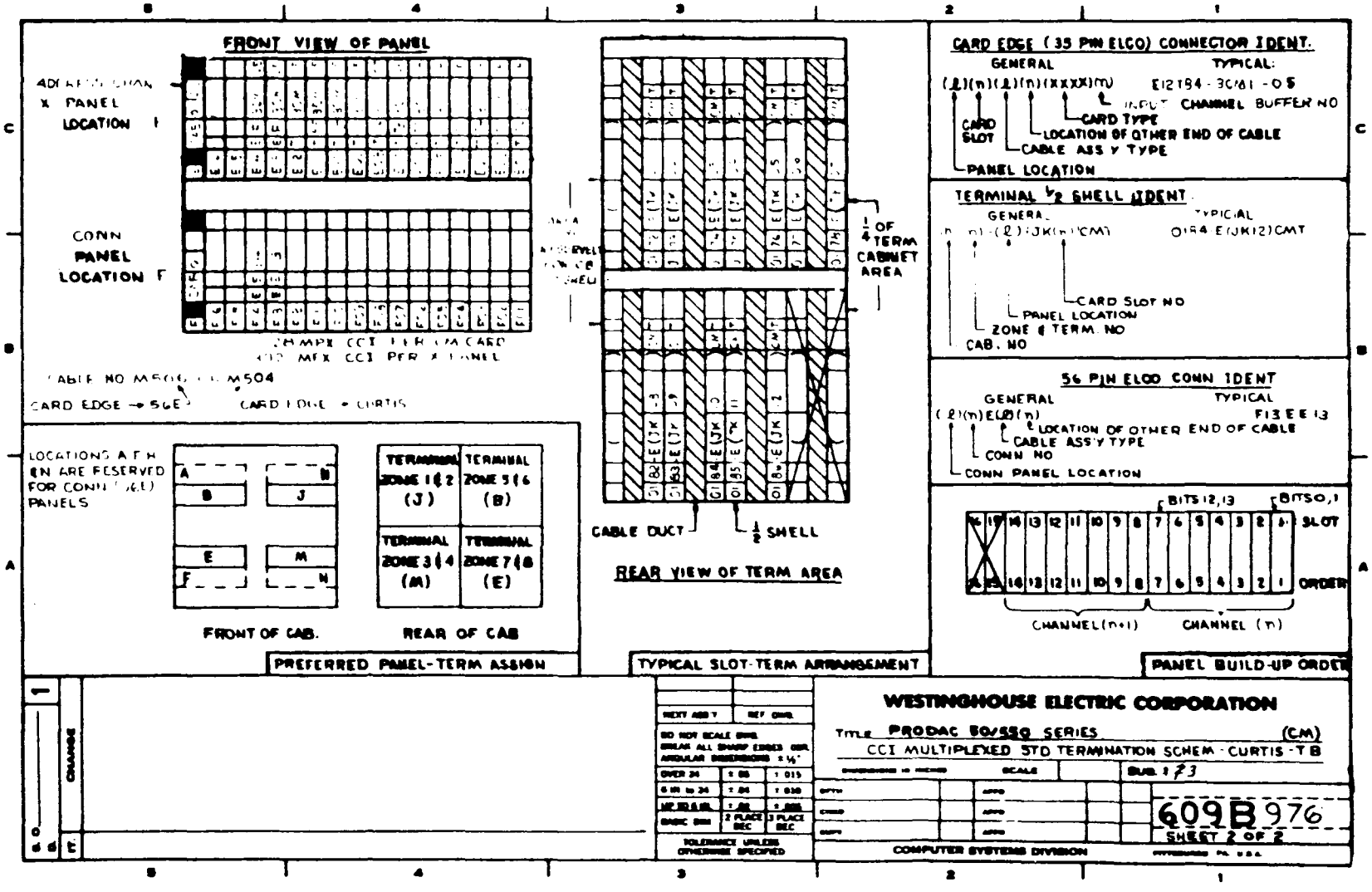
TITLE PRODAC SERIES
MPX CCI BLOCK DIAGRAM

DRWN R.B JACKSON 8/8/67
CHKD 9/15/67
MFG'R.
APPD
APPD
APPD

COMPUTER SYSTEMS DIVISION — PITTSBURGH, PA. U.S.A.

867C944


BCM
CURRENT LIMITING RES
BITS (EVEN GROUP)
BITS (ODD GROUP)
ELCO CONN. PIN ASSIGNMENT
+48/28V TO TAPER PIN BUSS
TYP CUSTOMER CONNECTION
WIRING ON UNDERSIDE OF TERM. BLOCK
PARALLEL WIRES GOING TO NEXT MULTIPLEXED CCI TERMINAL BLOCKS
PARALLEL WIRES COMING FROM PREVIOUS MULTIPLEXED CCI TERMINAL BLOCKS
NOTES: (TWO CABLING OPTIONS)
1. CARD EDGE TO TERMINAL BLOCK ONLY
2. CARD EDGE TO 56 PIN ELCO CONNECTOR ONLY
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 9950 SERIES (CM)
CCI MULTIPLEXER
609B976
SHEET 1 OF 2
COMPUTER SYSTEMS DIVISION



WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC 50/550 SERIES (CM)

CCI MULTIPLEXED STD TERMINATION SCHEM - CURTIS - TB

609B976

SHEET 2 OF 2

COMPUTER SYSTEMS DIVISION

AI01 - ANALOG INPUT SUBSYSTEM

GENERAL DESCRIPTION

The Analog Input subsystem provides for selection and sampling of analog signals and for conversion of the analog signals to digital form in order to be entered into the central processor.

The selection of an analog input is accomplished by a relay type multiplexer which connects the selected input to the analog-to-digital conversion circuits. The system is fail-safe against multiple analog point selection to any one analog-to-digital conversion circuit through the use of the analog trap and detection circuitry.

The analog signal is first converted into a frequency proportional to its instantaneous value by a voltage-to-frequency (V/F) converter. The output of the V/F converter is then counted for a period equal to one cycle of the power line frequency. By this method the noise components related to the power line frequency (which is the predominant noise) are integrated to zero and, thus, eliminated. The type of modules used in the Analog Input subsystem, and their interconnection, are shown on drawing 867C567 (Fig. 7).

The modules are mounted in the Analog Input Driver Panel ("A" panel) with the exception of the input multiplexer modules (AP) which are mounted in multiplexer panels ("X" panels).

The system shown on 867C567 is the maximum system which can be provided with one "A" panel.

In actual application the size of the system is determined by the number of analog points and by the number of V/F converters used.

SYSTEM SPECIFICATIONS

Maximum Sampling Rate

- 30 points/sec/V/F converters used (in 60 cycle environment).
- 25 points/sec/V/F converters used (in 50 cycle environment).

Input Signal Range

- 0-50 mV full scale (with -100% to + 200% overrange).
- 0-5V full scale (with -100% to + 120% overrange).

Input Impedance

- 5 Megohms on 50 mV range.
- 1000 Megohms/volt on 5V range.

System Accuracy

- 0.1% of full scale on both ranges.

Max. No. of V/F Converters

- 4 (per "A" panel).

Modularity

- 14 inputs per AP module.
- 224 inputs per "X" panel.

Max. No. of Inputs

- Not limited (determined by the number of word and channel drivers used).

Multiple Selection Protection

- An analog trap circuit prevents the selection of more than one analog input at a time, per V/F converter.

PRINTED CIRCUIT CARD REFERENCE

3AC4	Analog Control Card
4AP1/4AP2	Analog Point Selection Card
2AT3/2AT1/1SR1	Word & Channel Trap
4CD1	Channel Driver Card
5CL1	Calibrator Card
4CT1	Counter Module
1PL4/1PL5	Phase Locked Oscillator Card
3SB1	Span & Gain Card with Digital Input Buffer
1WD4	Word Driver Card

CIRCUIT OPERATION

General

The selection of analog inputs, the selection of gain and span connection, and the starting of the analog-to-digital conversion cycle is under program control.

The analog input address is formed by a word, channel and bit. Note that only one bit should be set for each

analog address. If more than one bit is set, this will cause more than one analog input connected to the V/F converter to be selected, which results in erroneous reading. Also note that if more than one input is selected (2, 3 or 4 V/F converters are used) the addresses should have the same channel and bit numbers.

The words normally used for the analog input selection are words 40 to 77. The channels normally used for the input selection are channels 17, 37 and 57 (channel 77 is also available if less than four V/F converters are used).

The analog addresses are assigned to the V/F converters as shown in Table 1.

For inputting the digitized analog value to the central processor, channels 16, 36, 56 and 76 are used (corresponding to V/F conv. #1, #2, #3 and #4).

The Analog-to-Digital Converter (ADC) bit pattern is as shown below:

Analog Voltage % of Full Scale	Input Data (octal)
-100	30000
-0	37777
+0	00000
+100	07777
+200	17777

The same channels 16, 36, 56 and 76 in output mode are used to set the span and gain to the V/F converters.

To compensate for absolute deviation of line frequency from 60 Hz, the system has the capability of adjusting "span" (frequency to voltage ratio). If, for example, the line frequency were to drop, the counter would be enabled for a longer period of time and the count would be too high. In this case the span must be decreased in order to correct the count. The span adjustment in effect decreases the slope of the V/F ratio line as shown in Figure 1. To check for frequency shift, a reference voltage from a calibrator card (CL) is read under program control and the deviation is calculated. A deviation of more than 0.05% can be corrected.

Bit 7 is used to reset the Span drivers, Bits 0-6 are used to select the required span. The span values corresponding to each bit are shown below:

Bit 0	0.05%	Bit 4	0.8%
Bit 1	0.1%	Bit 5	1.6%
Bit 2	0.2%	Bit 6	3.2%
Bit 3	0.4%	Bit 7	Reset

Since the V/F converter is offset 3.2% in the negative direction, any span bits set are added to this value. For example:

Data Word=01000000 is a span of 3.2% + (-3.2%) or 0% overall.

Data Word=00011010=span of 1.3% + (-3.2%) or -1.9% overall.

This gives a total range of -3.2% to +3.15%.

Bits 12 and 13 are used to select the gain, in the manner shown below:

Bit 13	Bit 12	Relay	Range
0	0	No Change	No Change
0	1	Energized	0-5 V
1	0	De-energized	0-50 mV
1	1	Not Used	

Note that both the span and gain can be output in the same data word.

The output of Bit 8 on Channel 16 is used to generate the READ TRIGGER signal which starts off the analog-to-digital conversion cycle. The analog-to-digital conversion cycle is automatic, controlled by the analog control (AC) module.

TABLE 1. ANALOG ADDRESSES FOR V/F CONVERTERS

Analog Words	One V/F Conv.	Two V/F Conv.	Three V/F Conv.	Four V/F Conv.
77-74	1	1	1	1
73-70	1	2	2	2
67-64	1	1	3	3
63-60	1	2	1	4
57-54	1	1	2	1
53-50	1	2	3	2
47-44	1	1	1	3
43-40	1	2	2	4

Upon completion of the conversion cycle, an interrupt signal is generated (which is recognized by the program) to indicate that the information is ready and a new cycle can be started. The instruction sequence should be as follows:

1. Read analog input value of previous output (Input on Ch. 16, 36, 56, 76).

2. Output new analog input address and bit number (Output on Ch. 17 or 37 or 57, Output word(s)).

NOTE

If more than one output is selected (2, 3 or 4 V/F converters used), the addresses should have the same channel and bit numbers.

3. Output span reset only if resetting span (Output Ch. 16, Bit 7).

4. Output span and gain if required (Output on Ch. 16, 36, 56, 76).

5. Output read trigger (Output Ch. 16, Bit 8).

6. Wait for interrupt.

7. Repeat steps 1 to 6.

Converting the Octal Printout to Decimal

Table 2 allows the user to convert octal printouts of the analog subsystem to decimal values. Conversely, a known decimal value can be converted to octal for comparison with the printout. The arrow (↓) in the table indicates the decimal point position.

For example, take octal printout:

7632	7000	=	4.3750
5 volt range	600	=	0.4687
	30	=	0.0293
	2	=	0.0024
			4.8754 Volts

or octal printout:

7632	7000	=	43.750
50 mV	600	=	4.687
range	30	=	0.293
	2	=	.024
			48.754 Millivolts

CIRCUIT DESCRIPTION

The flow diagram of the Analog Input subsystem for one analog input point is shown on drawing 867C568 (Fig. 8). Using word 77, channel 17 bit 0 for analog point address and channel 16 for input and for span-gain control, the operation of the circuit is explained as follows.

When word 77 is selected, the 4 μs pulse of 7ØØØ and Ø7ØØ will trigger the word driver SCR. This will apply - 10 V to the common leg of the relay coils on the AP card.

When bit 0 (OD00) is a "one" and channel 17 is selected, (ØØ1Ø and ØØØ7), both SCR's shown on the CD card will be turned on which will energize the point relay (I) and the guard relay (G) on the AP card. The guard relay contact then picks up the bus relay (B).

The analog point is now connected to the V/F converter via the analog bus.

The V/F converter generates an output pulse with a frequency proportional to the analog voltage signal, as shown in Figure 1.

TABLE 2. OCTAL TO DECIMAL CONVERSION TABLE

OCTAL	VOLTAGE 5 v	VOLTAGE 50 mV	OCTAL	VOLTAGE 5 v	VOLTAGE 50 mV	OCTAL	VOLTAGE 5 v	VOLTAGE 50 mV	OCTAL	VOLTAGE 5 v	VOLTAGE 50 mV
10000	5↓	0↓ 000									
7000	4	3 750	700	0↓	5↓ 469	70	0↓	0↓ 684	7	0↓	0↓ 085
6000	3	7 500	600	0	4 687	60	0	0 586	6	0	0 073
5000	3	1 250	500	0	3 906	50	0	0 488	5	0	0 061
4000	2	5 000	400	0	3 125	40	0	0 391	4	0	0 049
3000	1	8 750	300	0	2 344	30	0	0 293	3	0	0 037
2000	1	2 500	200	0	1 562	20	0	0 195	2	0	0 024
1000	0	6 250	100	0	0 781	10	0	0 098	1	0	0 012

NOTE

The values used in Figure 1 are for 60 Hz operation. At 50 Hz operation the following values apply:

204.8 kHz = Zero = 4096 pulses per cycle
409.6 kHz = Fullscale
614.4 kHz = Twice fullscale

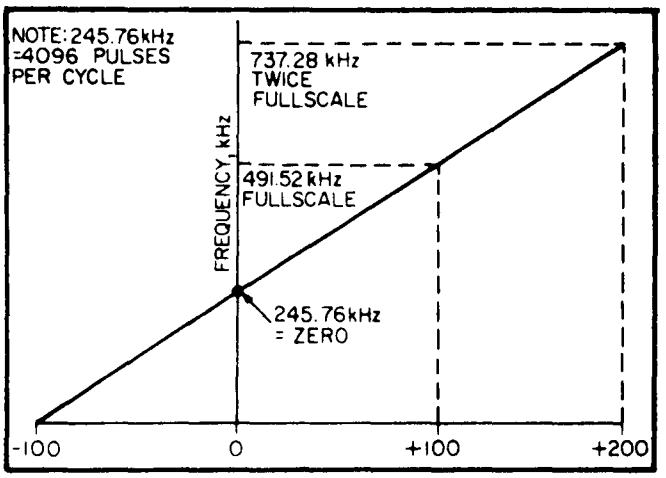


FIGURE 1. ANALOG SIGNAL PERCENT OF FULL SCALE

The setting of the span and the gain of the V/F converter is accomplished through the SB module. If bit 7 (OD07) is a "one" and channel 16 (ØØ1Ø, ØØØ6) is interrogated, the power supply switch on the CL module is triggered, which will turn off the span driver SCR's on the SB module. The status of bits 0-6 (OD00 through OD06) upon interrogating channel 16 will determine which span driver SCR's will be turned on. The SCR's which conduct will then energize the span relays in the V/F converter.

The status of bits 12 and 13 (OD12 and OD13), upon interrogating channel 16, will provide signals to turn on or off the gain flip-flop on the SB module. If the flip-flop is turned "on", the output of the flip-flop is "0" (PSC) which provides a current path for the gain relay coil in the V/F converter.

Outputting bit 8 (OD08) on channel 16 (SB card) will provide a 4 μs pulse (READ TRIGGER signal) to the analog control module (AC), which initiates the analog input sequence.

The timing signal for the analog control circuit (AC module) is obtained from the phase lock oscillator module (PL) in the form of a 120 pps square wave, which is phase locked with the 60 Hz power line frequency. Note that a 50 Hz oscillator module is also available (refer to PL card document).

Immediately following the READ TRIGGER pulse (see timing sequence of AC module), the analog control circuit generates a RESET signal to the counter (CT module), and times out a delay to permit settling time for both the point, guard, and bus relays of the analog point (AP) module and the V/F converter. Then it opens the gate for the V/F signal enabling the COUNT pulses to the CT module. The gate is kept open for two cycles of the 120 pps signal, which is equal to one cycle of the power line frequency.

Upon closing the gate, the analog control circuit generates a trigger signal to the power supply switch on the AC module. The power supply switch then opens to turn off the analog point selection word and channel driver SCR's.

The power supply switch delays closing to permit the analog point selection relays to dropout. Then, the power supply switch generates an interrupt signal informing the central processor that the analog value (output of the counter, CT module) is ready to be read.

To input the contents of the counter, the digital input buffer circuit on the SB module is used.

Interrogating channel 16, the signals on the input data lines (ID00 through ID13) will be dependent on the output of the counter (1CTB00 through 1CTB13). The interrogating 4 μs pulse is transmitted to an input data line only if the corresponding counter output line is a "one".

Reference voltages from the CL module can be connected as analog inputs for drift correction purposes.

The CL module also accommodates four RTD bridge circuits (only one shown on drawing 867C568) which can be used for measuring the cold junction box temperatures. The outputs of the bridges have to be connected as analog inputs.

Analog Signal Conditioners

To obtain the analog signals in the required range of the analog-to-digital converter range (0-50mV or 0-5V), or to eliminate other than line frequency component noise, the following signal conditioners are used in the analog input systems.

RTD Bridges (Using 15 volt power supply for RTD's)

RTD Resistance Span	(W) Part No.
2 - 7 ohms	610B249 G05
2 - 12 ohms	610B249 G03
2 - 22 ohms	610B249 G01
7 - 12 ohms	610B249 G06
12 - 17 ohms	610B249 G07
12 - 22 ohms	610B249 G04
12 - 32 ohms	610B249 G02
17 - 22 ohms	610B249 G08

RTD Bridges cont'd.

RTD Resistance Span	Ⓦ Part No.
20 - 70 ohms	682B420 G05
20 - 120 ohms	682B420 G03
20 - 220 ohms	682B420 G01
70 - 120 ohms	682B420 G06
120 - 170 ohms	682B420 G07
120 - 220 ohms	682B420 G04
120 - 320 ohms	682B420 G02
170 - 220 ohms	682B420 G08

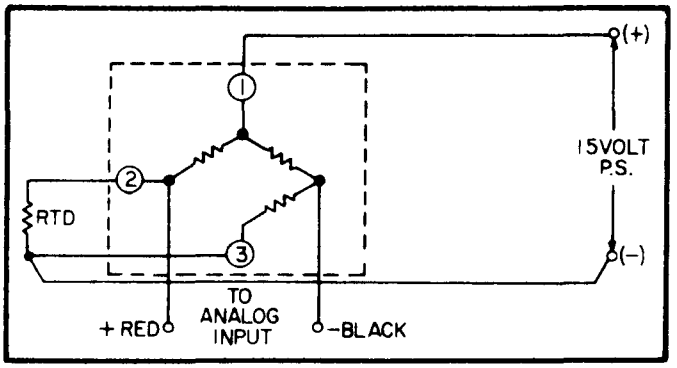


FIGURE 2. RTD BRIDGE SCHEMATIC

Current to Voltage Converter (For 5 volts fullscale for the following current ranges:)

Current Range	Dropping Resistor	Ⓦ Part No.
1-5 ma	1000 ohms	610B246 G03
2-10 ma	500 ohms	610B246 G04
4-20 ma	250 ohms	610B246 G01
10-50 ma	100 ohms	610B246 G02
200-1000 ma	5 ohms	610B246 G05
0.227-1.135 ma	4400 ohms	610B246 G06
0.333-1.665 ma	3000 ohms	610B246 G07

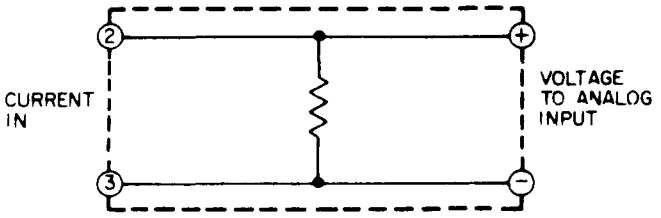


FIGURE 3. CURRENT-TO-VOLTAGE CONVERTER SCHEMATIC

Voltage Dividers - To reduce voltages greater than 5V to the 5V range in the following ratios: 2:1 (Ⓦ 682B683G01), 4:1 (Ⓦ 682B683G02), 8:1 (Ⓦ 682B683G03), 16:1 (Ⓦ 682B683G04).

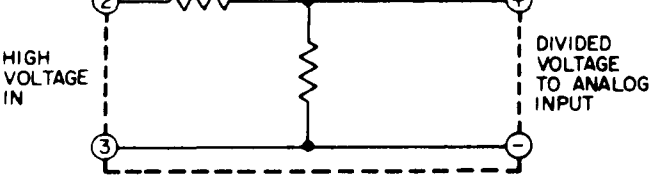


FIGURE 4. VOLTAGE DIVIDER SCHEMATIC

Low Voltage Filter (Time constant = 1.32 s for 0-100 MV signal. Ⓦ No. 682B685G01.)

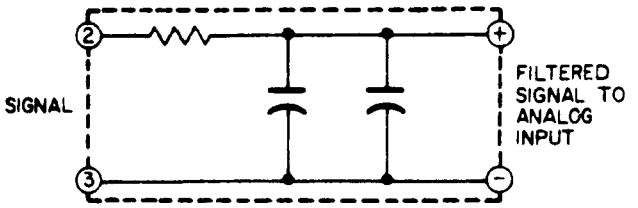


FIGURE 5. LOW VOLTAGE FILTER SCHEMATIC

High Voltage Filter (Time constant = 1.35 s for 0-6V signal. Ⓦ No. 682B686G01.)

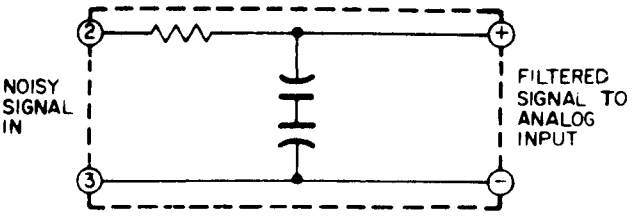


FIGURE 6 HIGH VOLTAGE FILTER SCHEMATIC

Each signal conditioner is an individually encapsulated block and mounted on the analog input half-shells adjacent to the terminal strips. Each analog input requiring special conditioning is equipped with the appropriate block.

ANALOG SUBSYSTEM LOGIC PRINTS

The following prints are included at the end of this document to show the logic connections of the cards used in the A-Panel. The number in the upper right hand corner designates the location of that card in the A-Panel. Also included are the Analog Trap cards which can be located in any panel.

These prints are shown for a maximum (4 converters) system. Less cards may be used for smaller systems.

Figure No.	Drawing No.	Logic Description
17	867C291	Phase Lock Oscillator
18	867C292	Analog Control Card
19	867C293	Calibrator Card
20	867C294	#1 Span & Gain w/Buffer
21	867C295	#1 Counter Card
22	867C296	#2 Span & Gain w/Buffer
23	867C297	#2 Counter Card
24	867C298	#3 Span & Gain w/Buffer
25	867C299	#3 Counter Card
26	867C300	#4 Span & Gain w/Buffer
27	867C301	#4 Counter Card
28	867C302	Channel Driver (17)
29	867C303	Channel Driver (37)
30	867C304	Channel Driver (57)
31	867C305	Word Driver (40-57)
32	867C306	Word Driver (60-67)
33	867C994	Analog Trap
34	867C995	Summing Resistors.

CONNECTORS AND TERMINATIONS

A-Panel Connectors

Drawing 774A717 sheets 1 and 2 show the connector breakdown on plugs A21-23 and A22-24 (Fig. 9 and 10).

X-Panel Connector Breakdown - AP Option

Plugs 21 and 23 are wired in parallel as below.

Back Panel Wiring (AP Card)	56 Pin ELCO	MNEMONIC	To 35 Pin ELCO on Chan. Driver on A-Panel*
H2	W	AIR0	35 - 34
H3	X	AIR1	33 - 32
H4	Y	AIR2	31 - 30
H5	Z	AIR3	29 - 28
H6	a	AIR4	27 - 26
H7	b	AIR5	25 - 24
H8	c	AIR6	23 - 22
H9	d	AIR7	21 - 20
H10	k	AIR8	14 - 13
H11	l	AIR9	12 - 11
H12	m	AIR10	10 - 9
H13	n	AIR11	8 - 7
H14	p	AIR12	6 - 5
H15	r	AIR13	4 - 3
H16	t	BUSRY	16 - 18

*Could be slot A12, 13 or 14 depending upon channel to be used.

Plugs 22 and 24 are wired in parallel as below:

Back Panel Wiring (AP Card) Card Slot	Pin	56 Pin ELCO	MNEMONIC	35 Pin ELCO WD Card
1	H17	A	WD60, 40	35 - 34
2	H17	C	WD61, 41	31 - 30
3	H17	E	WD62, 42	27 - 26
4	H17	H	WD63, 43	23 - 22
5	H17	L	WD64, 44	15 - 16
6	H17	N	WD65, 45	11 - 12
7	H17	R	WD66, 46	7 - 8
8	H17	NN	WD67, 47	3 - 4
9	H17	LL	WD70, 50	33 - 32
10	H17	JJ	WD71, 51	29 - 28
11	H17	FF	WD72, 52	25 - 24
12	H17	CC	WD73, 53	21 - 20
13	H17	AA	WD74, 54	13 - 14
14	H17	Y	WD75, 55	9 - 10
15	H17	W	WD76, 56	5 - 6
16	H17	T	WD77, 57	1 - 2

The WD card is in the A-panel slot A16 for words 60 to 77 and in slot A15 for words 40 to 57.

Plug 25 is wired as below:

56 Pin ELCO	MNEMONIC	Destination (AP Card)
A	Plus (n)	L2 Slots 1 - 4
B	Minus (n)	L3 Slots 1 - 4
C	Guard (n)	L4 Slots 1 - 4
E	Plus (n)	L2 Slots 5 - 8
F	Minus (n)	L3 Slots 5 - 8
H	Guard (n)	L4 Slots 5 - 8
L	Plus (n)	L2 Slots 9 - 12
M	Minus (n)	L3 Slots 9 - 12
N	Guard (n)	L4 Slots 9 - 12
R	Plus (n)	L2 Slots 13 - 16
S	Minus (n)	L3 Slots 13 - 16
T	Guard (n)	L4 Slots 13 - 16

Terminations

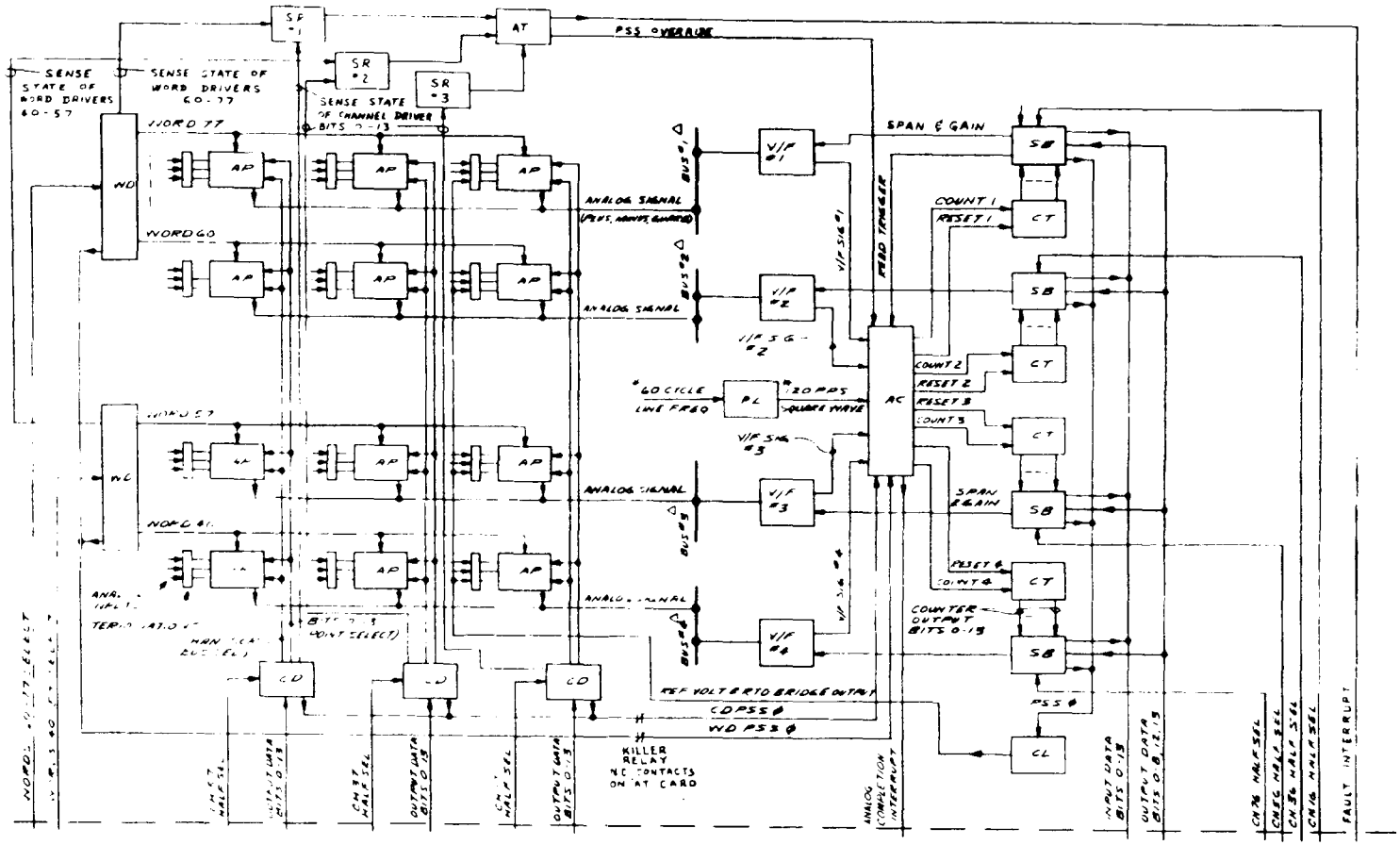
Drawing 6093979 sheets 1 and 2 show the analog input standard termination scheme used on TJC (Thermal Junction Box-Cold) (Fig. 11a - b).

Drawing 682B689 sheets 1 to 3 show the analog input standard termination scheme used when there is no TJC (Fig. 12a - c).

The following drawings show the recommended analog input termination schemes for each type of analog inpu

Figure No.	Drawing No.	Type of Input
13	682B684	Thermocouple
14	682B687	RTD
15	682B688	Voltage Sensor
16	682B690	Current Sensor

* * *



I/O INTERFACE

NOTES:

* 50 CPS & 100 PPS FOR 50 CPS SYSTEM.

Δ FOR ASSIGNMENT OF THE ANALOG SIGNALS TO THE V/F BUSSES, REFER TO SYSTEMS DESCRIPTION PART III.

FIGURE 7. A/I SUBSYSTEM BLOCK DIAGRAM (REF. DWG. 867C567, SUB 3)

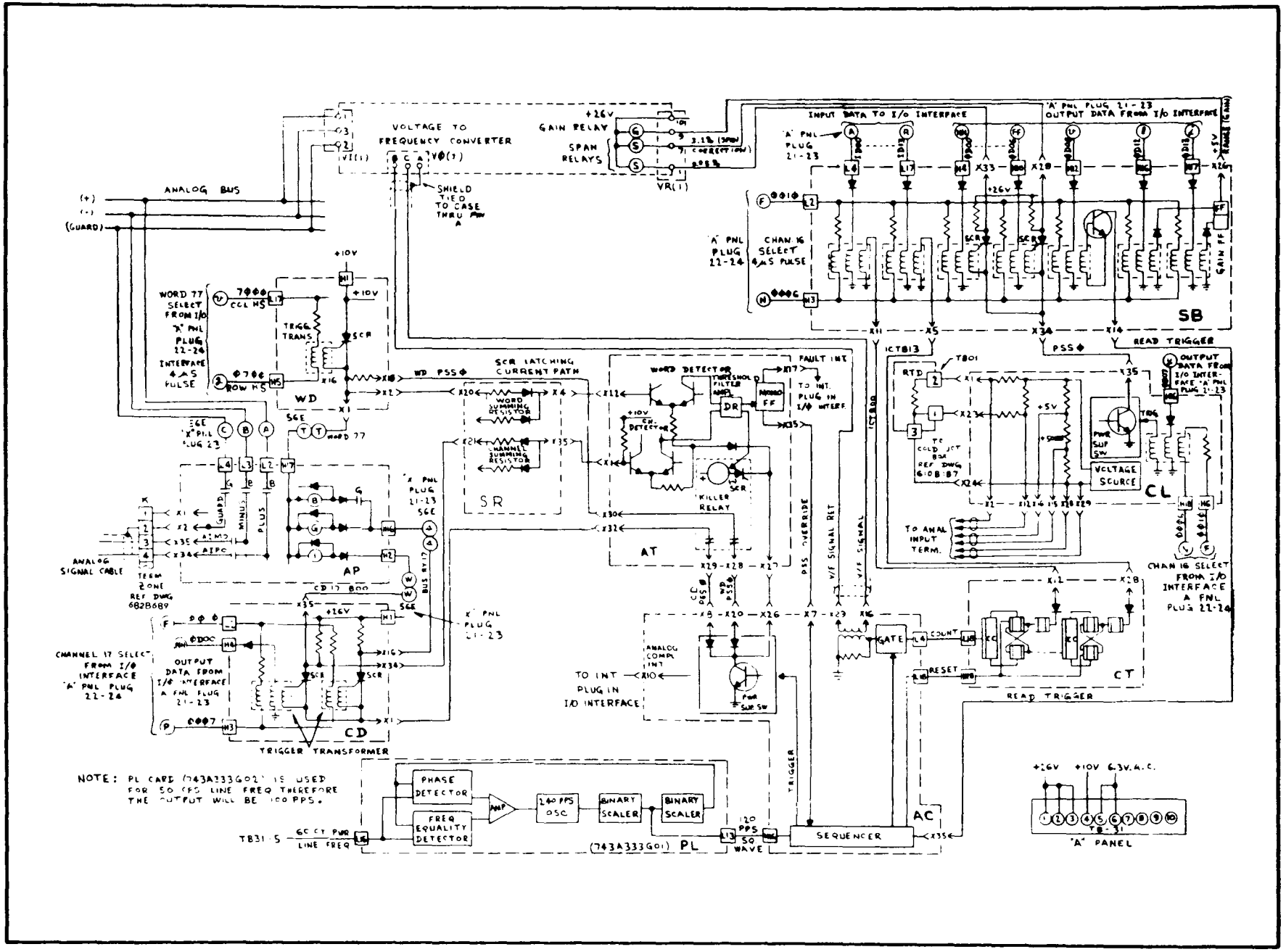


FIGURE 8. A-I SUBSYSTEM FLOW DIAGRAM (REF. DWG. 867C568, SUB 3)

56 – PIN ELCO CONNECTOR	DATA LINE	DATA RETURN	56 – PIN ELCO CONNECTOR	DATA LINE	DATA RETURN
A	ID0		h		IDR13
B		IDR0	j	OD13	
C	ID1		k		ODR12
D		IDR1	l	OD12	
E	ID2		m		ODR11
F		IDR2	n	OD11	
H	ID6		p		ODR10
J	ID3		r	OD10	
K		IDR3	s		ODR9
L	ID4		t	OD9	
M		IDR4	u		ODR8
N	ID5		v	OD8	
P		IDR5	w		ODR6
R	ID7		x		ODR7
S		IDR7	y	OD7	
T		IDR6	z		ODR5
U	ID8		AA	OD5	
V		IDR8	BB		ODR4
W	ID9		CC	OD4	
X		IDR9	DD		ODR3
Y	ID10		EE	OD3	
Z		IDR10	FF	OD6	
a	ID11		HH		ODR2
b		IDR11	JJ	OD2	
c	ID12		KK		ODR1
d		IDR12	LL	OD1	
e	ID13		MM		ODR0
f		ODR13	NN	OD0	

FIGURE 9. A-PANEL CONNECTOR BREAKDOWN - A21-23 (REF. DWG. 7714717, SHEET 1)

56 – PIN ELCO CONNECTOR	CHANNEL HALF SELECT	56 – PIN ELCO CONNECTOR	WORD HALF SELECT
A	ΦΦΦ0	h	
B	ΦΦΦ1	j	
C	ΦΦΦ2	k	
D	ΦΦΦ3	l	
E	ΦΦ0Φ	m	
F	ΦΦ1Φ	n	
H	ΦΦ2Φ	p	
J	ΦΦ3Φ	r	
K		s	
L	ΦΦΦ4	t	
M	ΦΦΦ5	u	
N	ΦΦΦ6	v	7ΦΦΦ
P	ΦΦΦ7	w	6ΦΦΦ
R	ΦΦ4Φ	x	5ΦΦΦ
S	ΦΦ5Φ	y	4ΦΦΦ
T	ΦΦ6Φ	z	Φ7ΦΦ
U	ΦΦ7Φ	AA	Φ6ΦΦ
V		BB	Φ5ΦΦ
W		CC	Φ4ΦΦ
X		DD	
Y		EE	3ΦΦΦ
Z		FF	2ΦΦΦ
a		HH	1ΦΦΦ
b		JJ	0ΦΦΦ
c		KK	Φ3ΦΦ
d		LL	Φ2ΦΦ
e		MM	Φ1ΦΦ
f		NN	Φ0ΦΦ

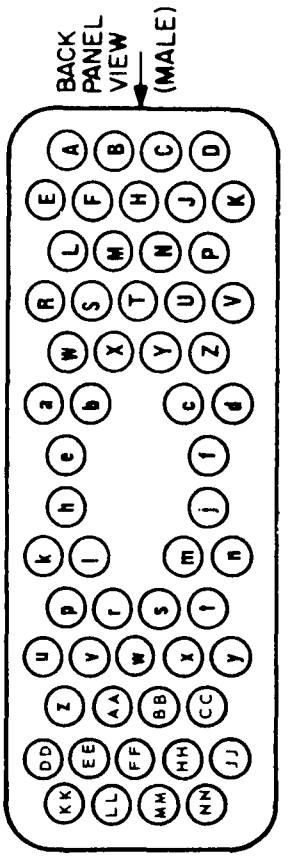


FIGURE 10. A-PANEL CONNECTOR BREAKDOWN - A22-24 (REF. DWG. 774A717, SHEET 2)

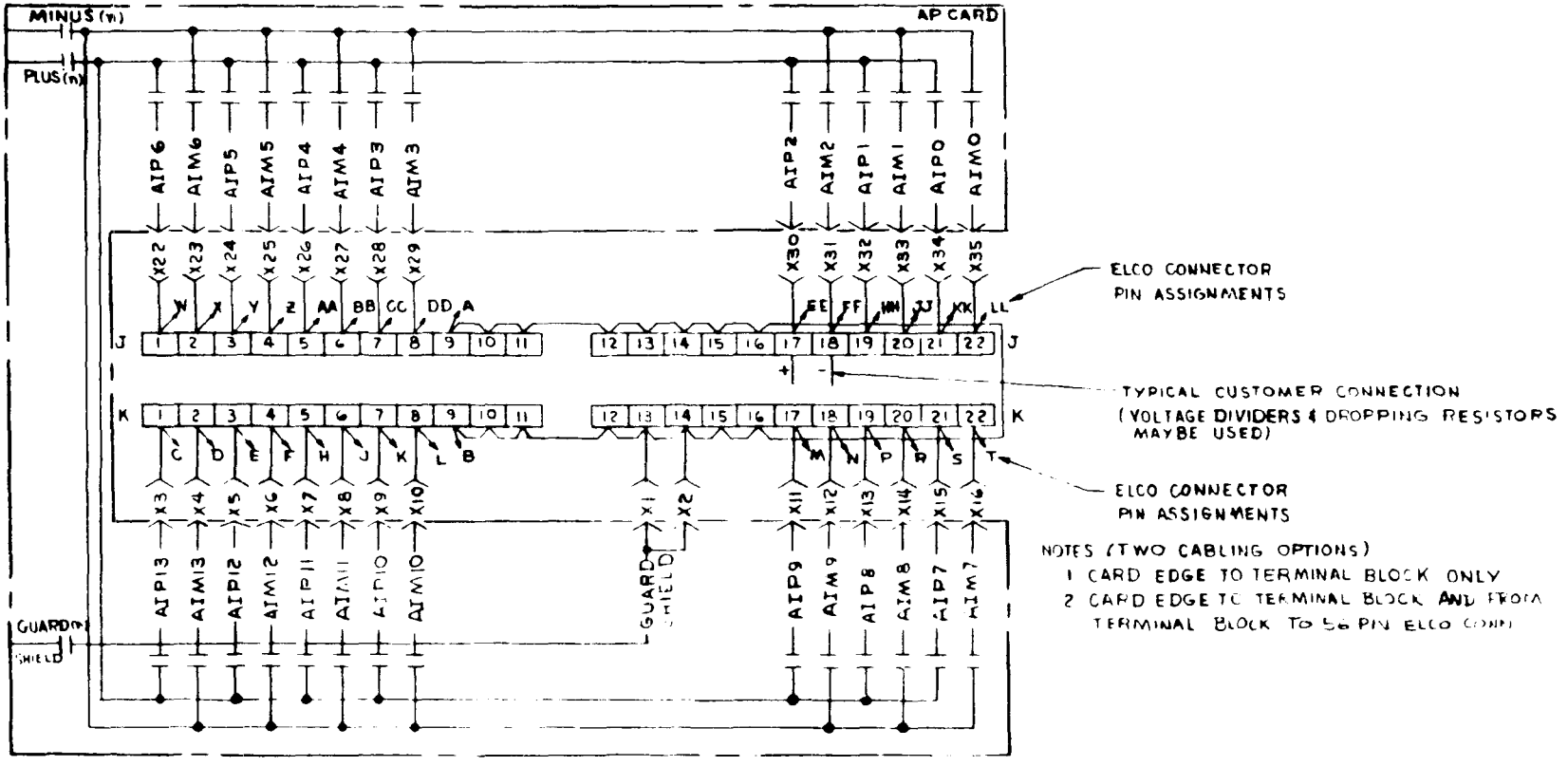


FIGURE 11a. TERMINATION SCHEME - THERMAL JUNCTION BOX-COLD (REF. DWG. 609B979, SHEET 1, SUB 4)

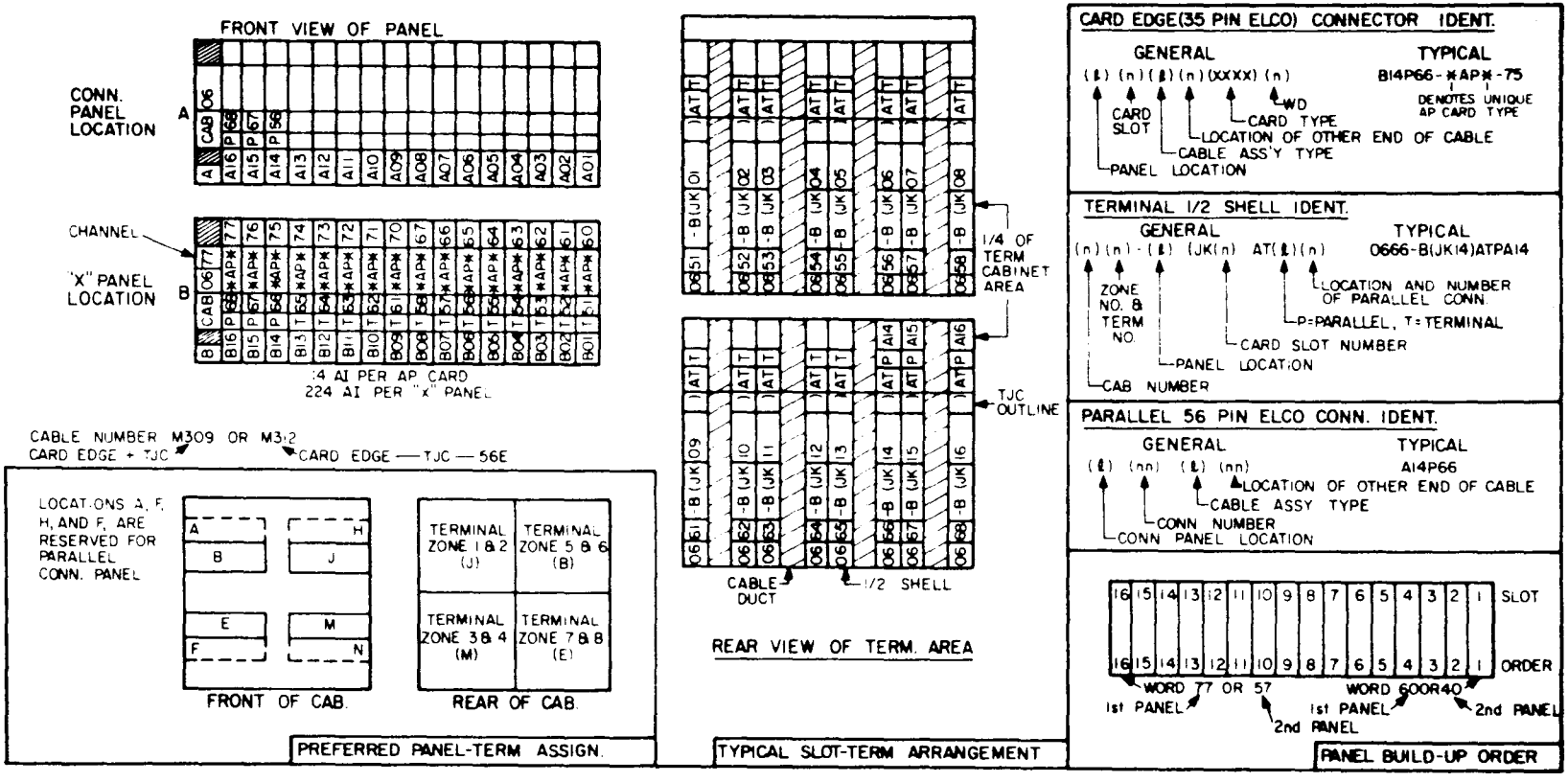


FIGURE 11b. TERMINATION SCHEME - THERMAL JUNCTION BOX-COLD (REF. DWG. 609B979, SHEET 2, SUB 4)

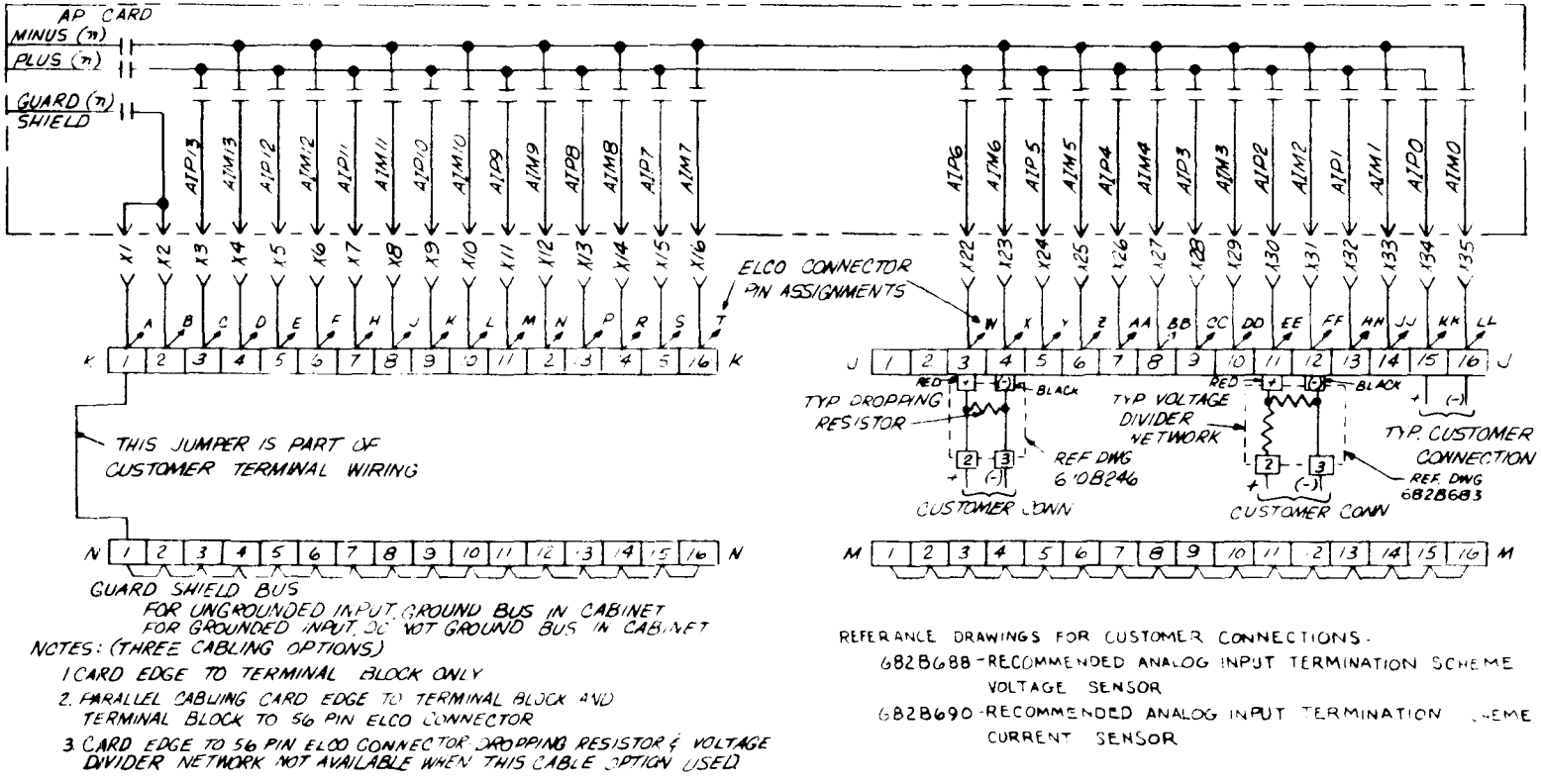
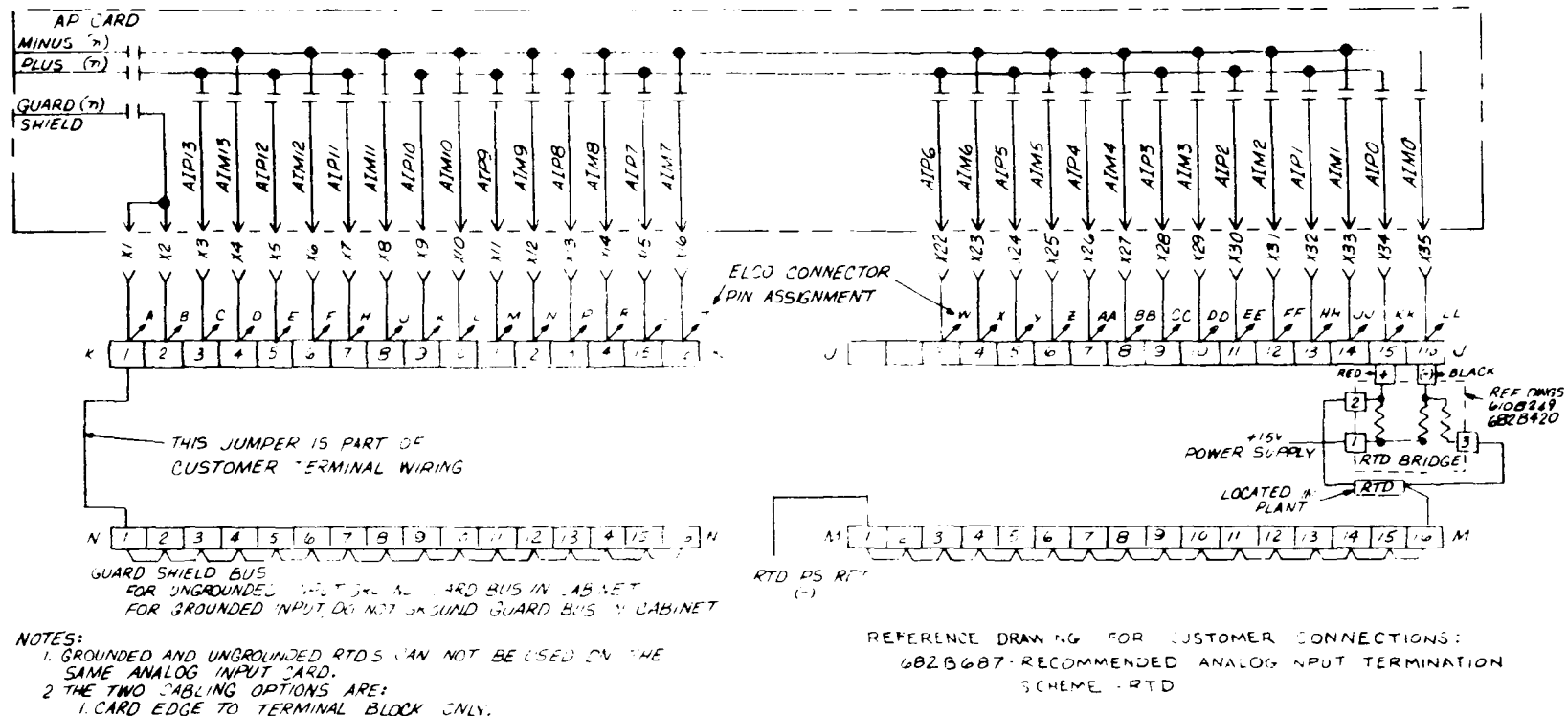


FIGURE 12a. STANDARD TERMINATION SCHEME WITHOUT TJC (REF. DWG. 682B689, SHEET 1)



NOTES:
1. GROUNDED AND UNGROUNDED RTDS CAN NOT BE USED ON THE SAME ANALOG INPUT CARD.
2. THE TWO CABLING OPTIONS ARE:
   1. CARD EDGE TO TERMINAL BLOCK ONLY.
   2. PARALLEL CABLING CARD EDGE TO TERMINAL BLOCK AND TERMINAL BLOCK TO 56 PIN ELCO CONNECTOR.

REFERENCE DRAWING FOR CUSTOMER CONNECTIONS:
682B687 - RECOMMENDED ANALOG INPUT TERMINATION SCHEME - RTD

FIGURE 126. STANDARD TERMINATION SCHEME WITHOUT TJC (REF. DWG. 682B689, SHEET 2)

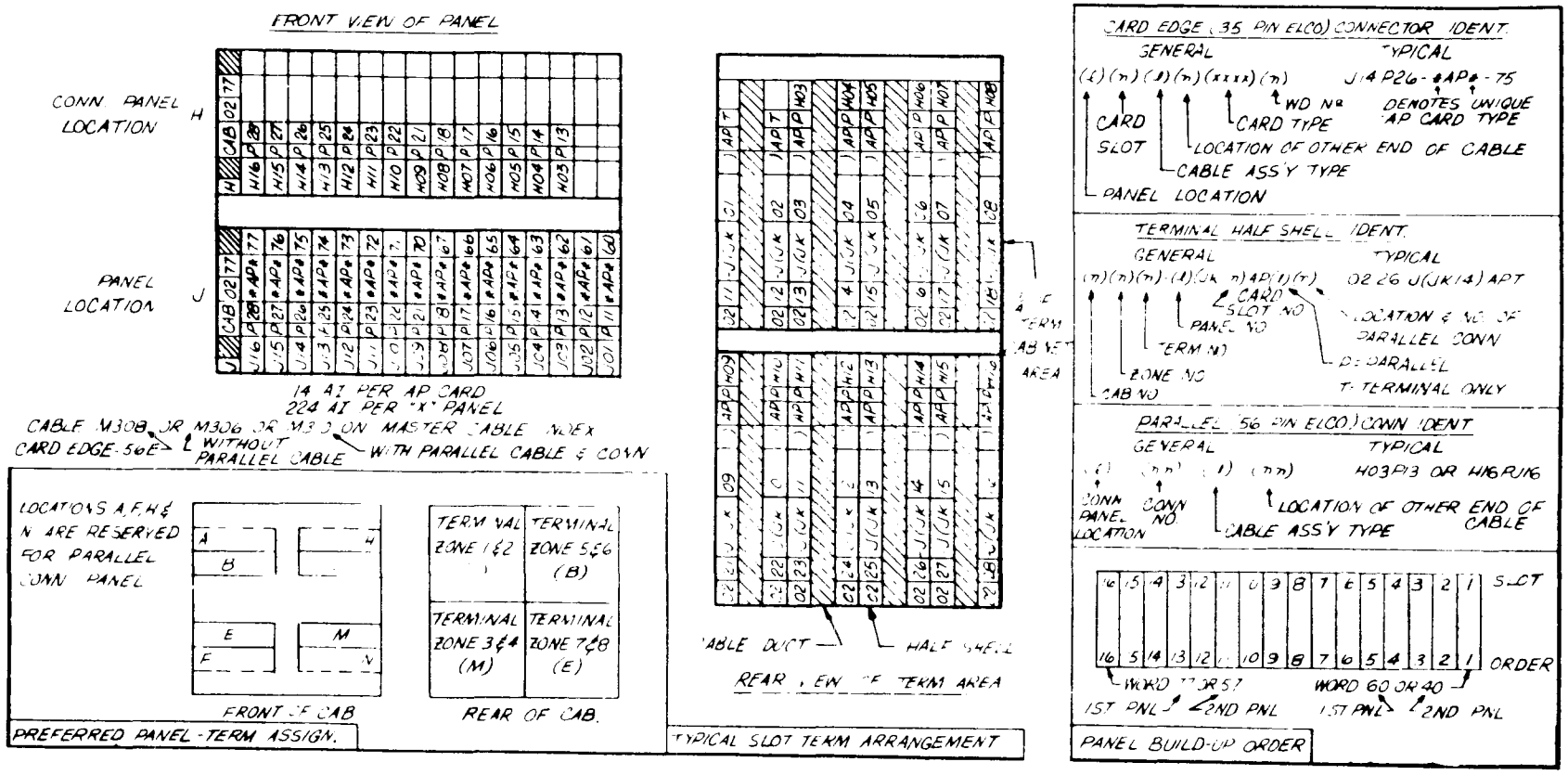


FIGURE 12c. STANDARD TERMINATION SCHEME WITHOUT TJC (REF. DWG. 682B689, SHEET 3)

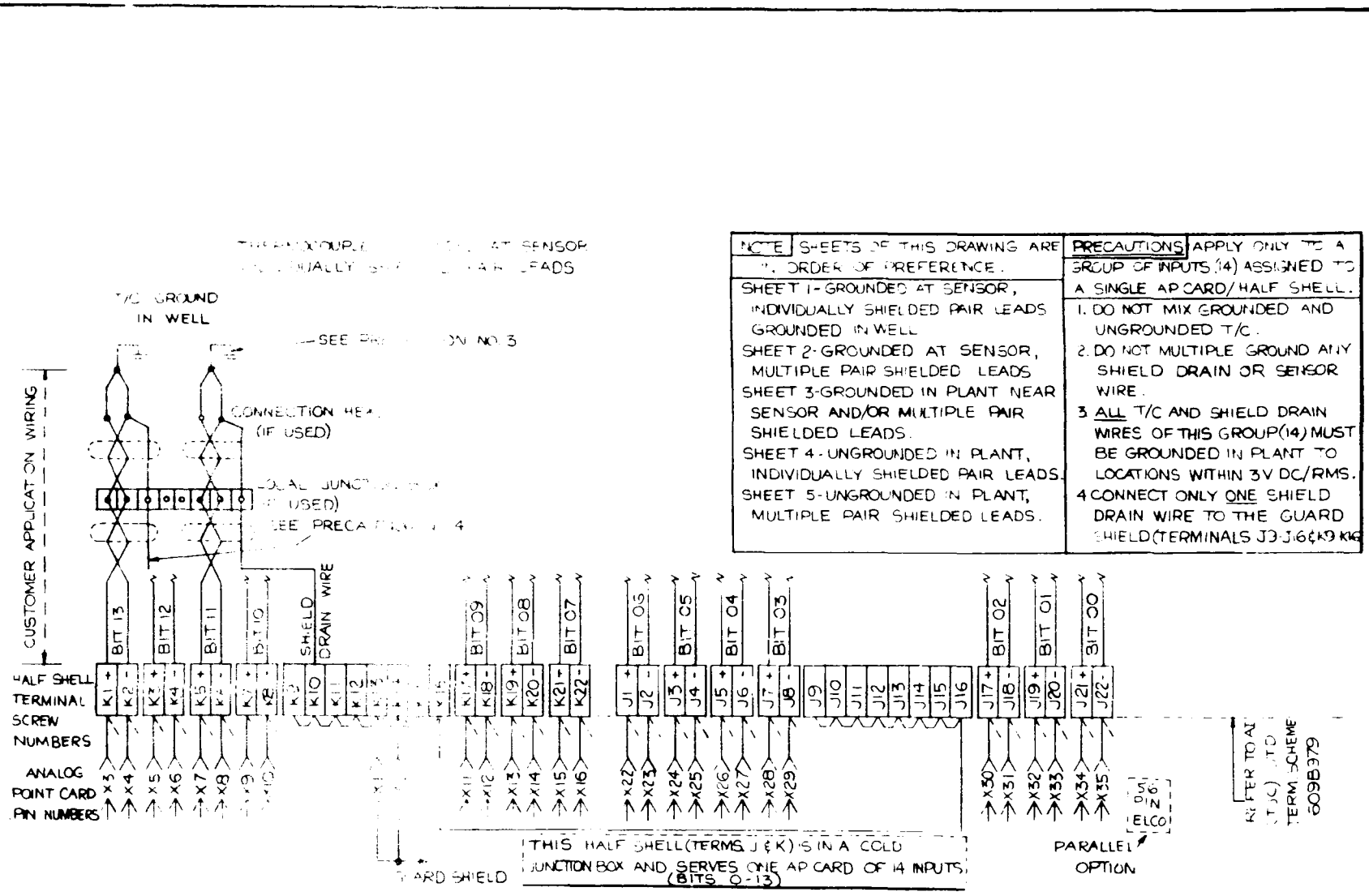


FIGURE 13a THERMOCOUPLE INPUT CONNECTIONS (REF. DWG 682B684, SHEET 1)

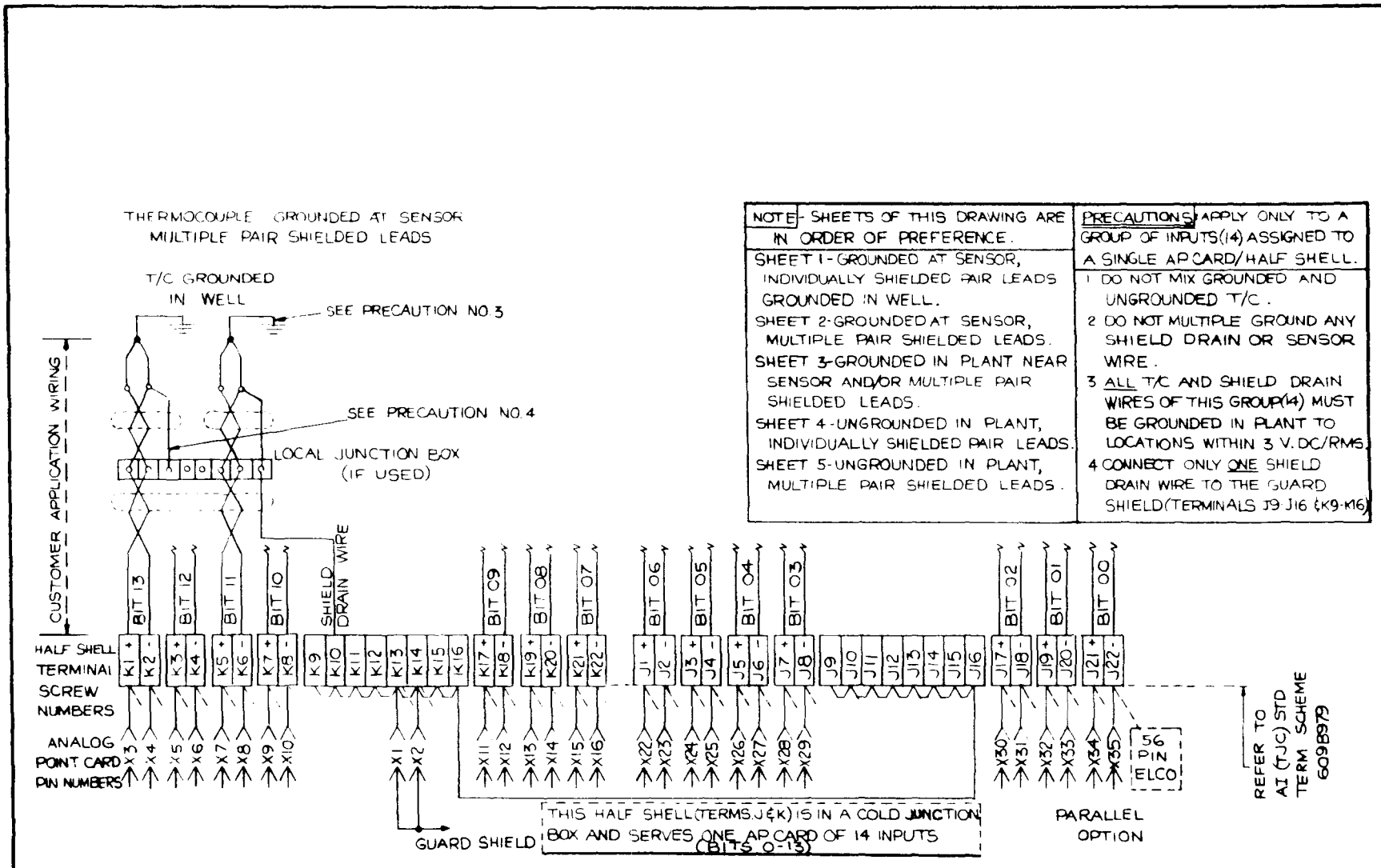


FIGURE 13b. THERMOCOUPLE INPUT CONNECTIONS (REF. DWG. 682B684, SHEET 2)

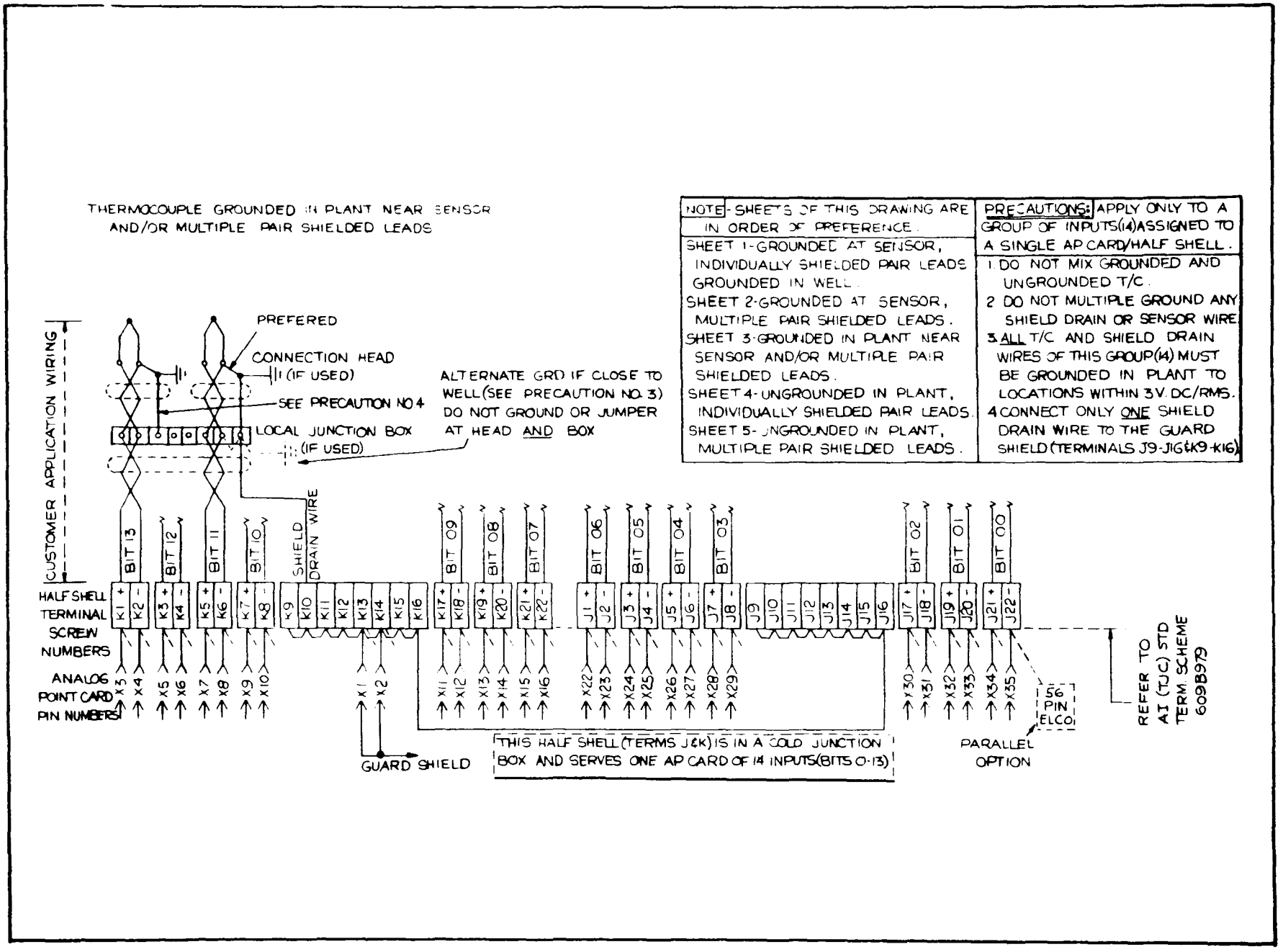


FIGURE 13c. THERMOCOUPLE INPUT CONNECTIONS (REF. DWG. 682B684, SHEET 3)

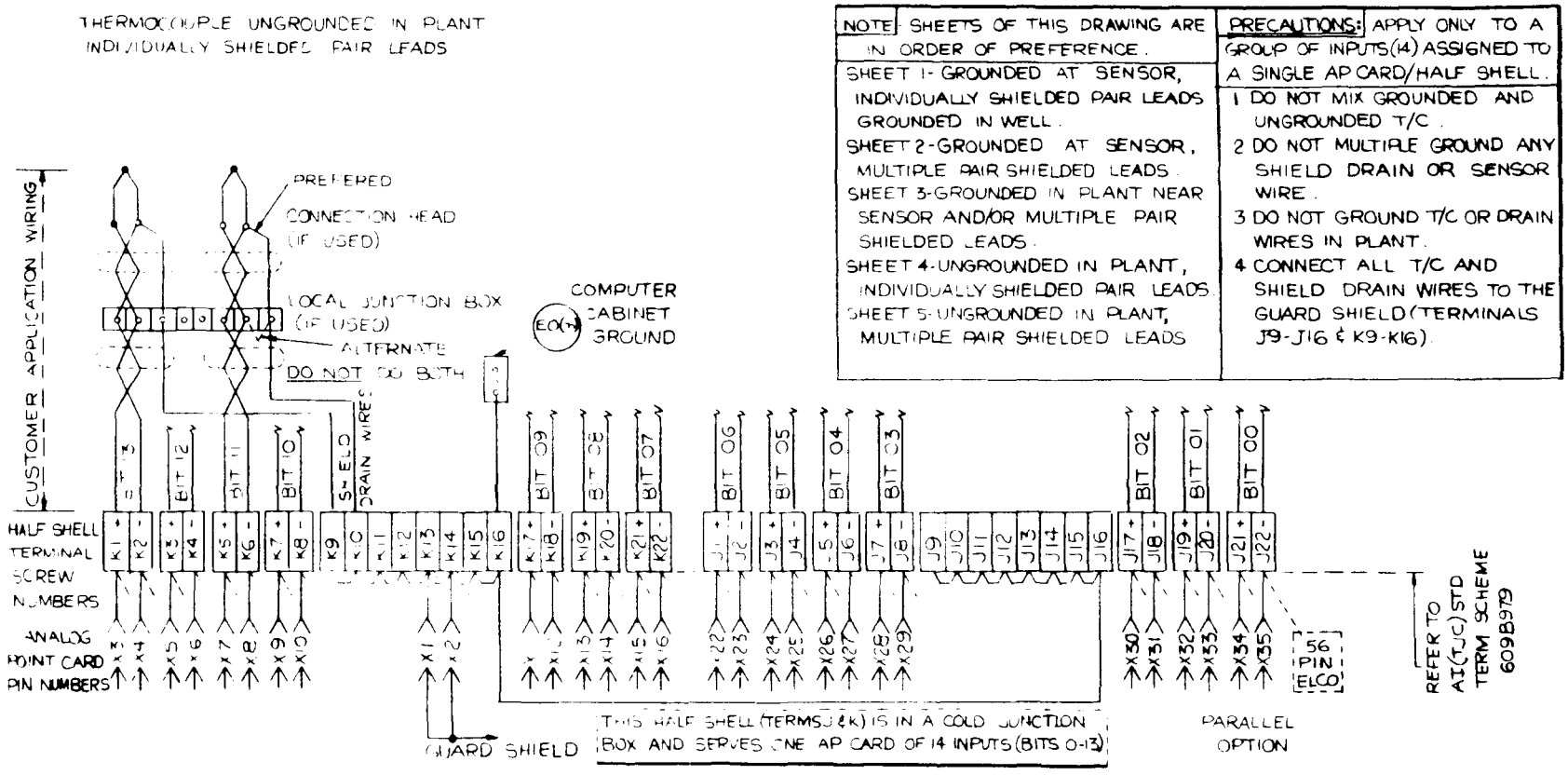


FIGURE 13d. THERMOCOUPLE INPUT CONNECTIONS (REF. DWG. 682B684, SHEET 4)

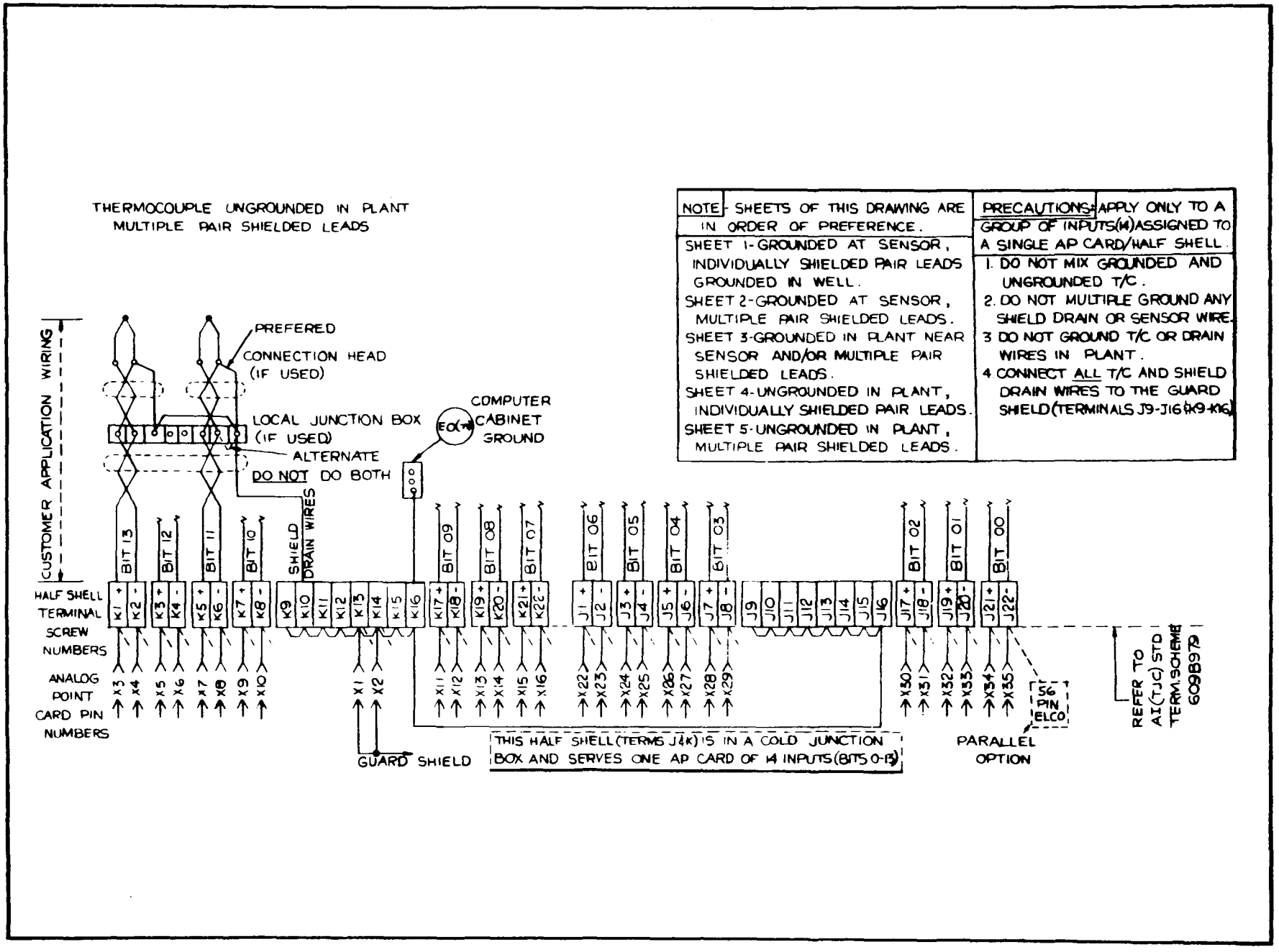


FIGURE 13e. THERMOCOUPLE INPUT CONNECTIONS (REF. DWG. 682B684, SHEET 5)

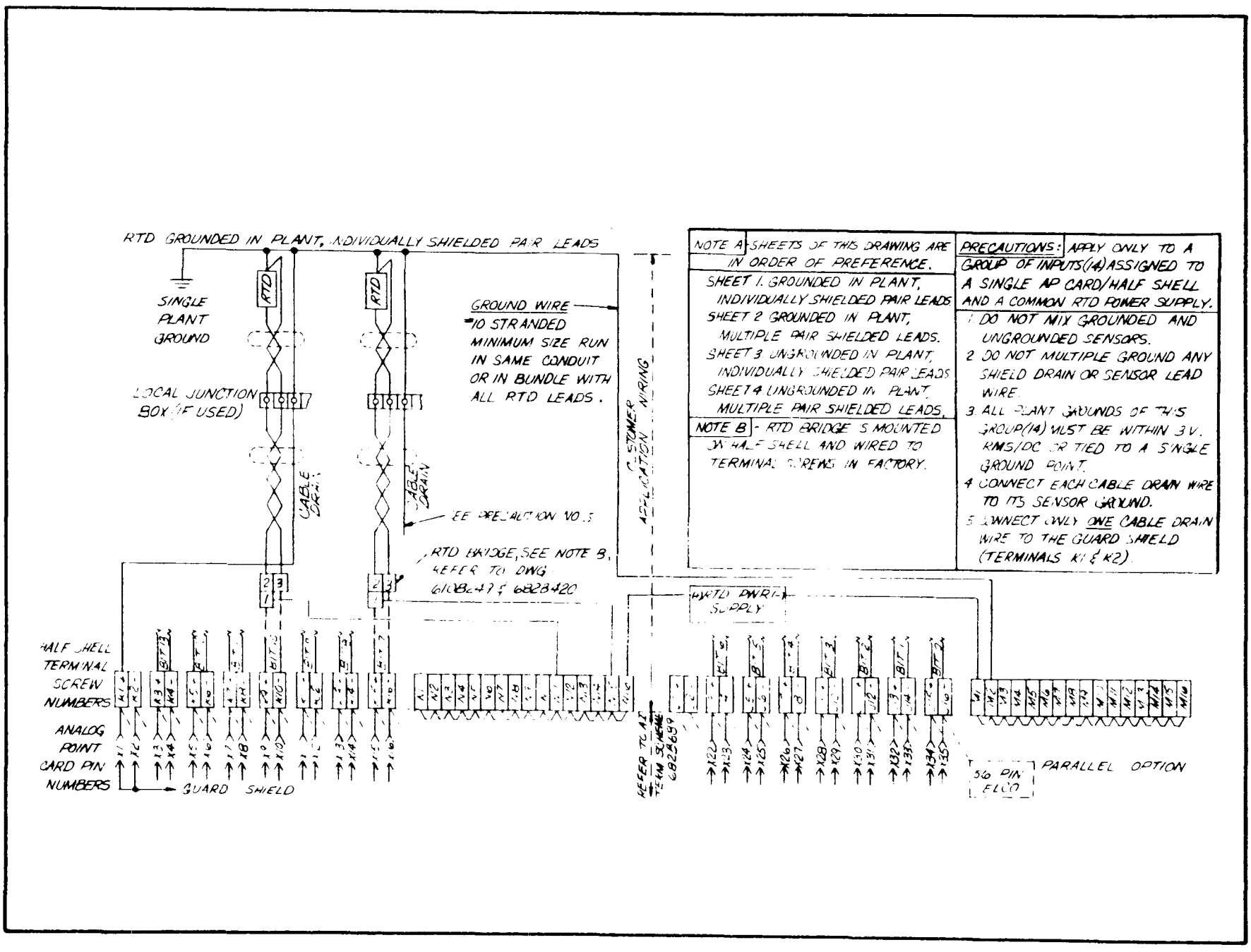


FIGURE 14a. RTD INPUT CONNECTIONS (REF. DWG. 682B687, SHEET 1)

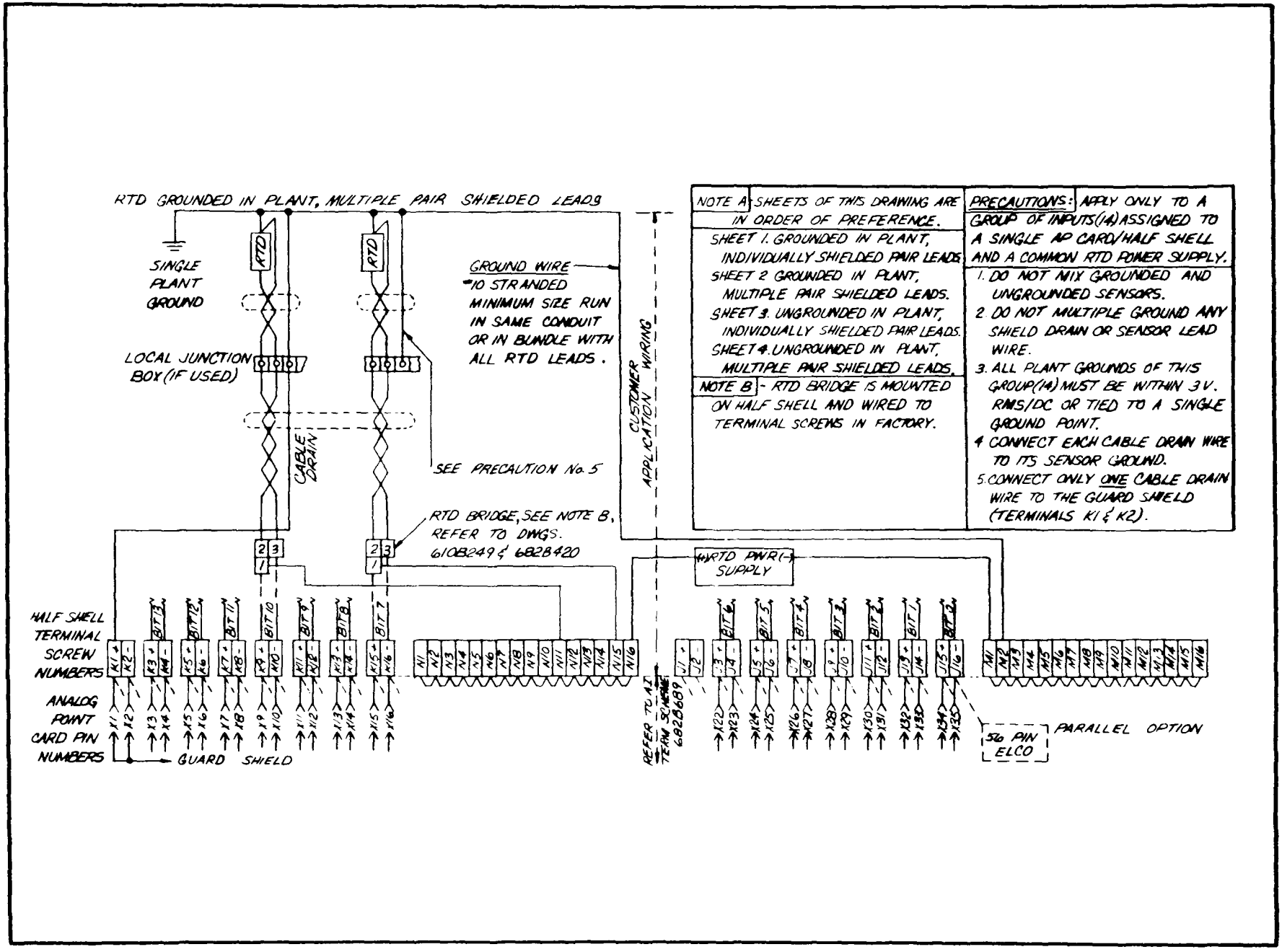


FIGURE 14b. RTD INPUT CONNECTIONS (REF. DWG. 682B687, SHEET 2)

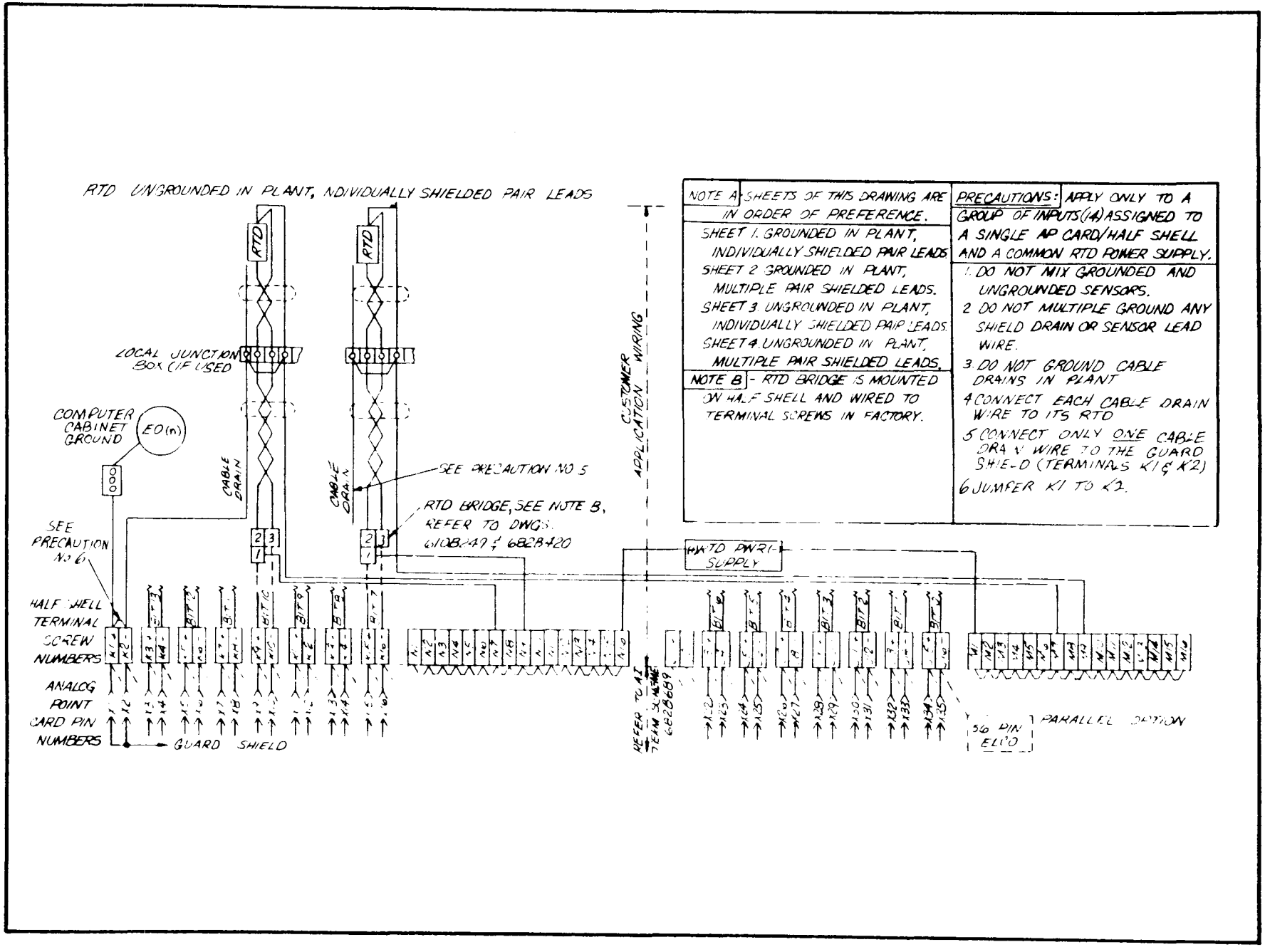


FIGURE 14c. RTD INPUT CONNECTIONS (REF. DWG. 682B687, SHEET 3)

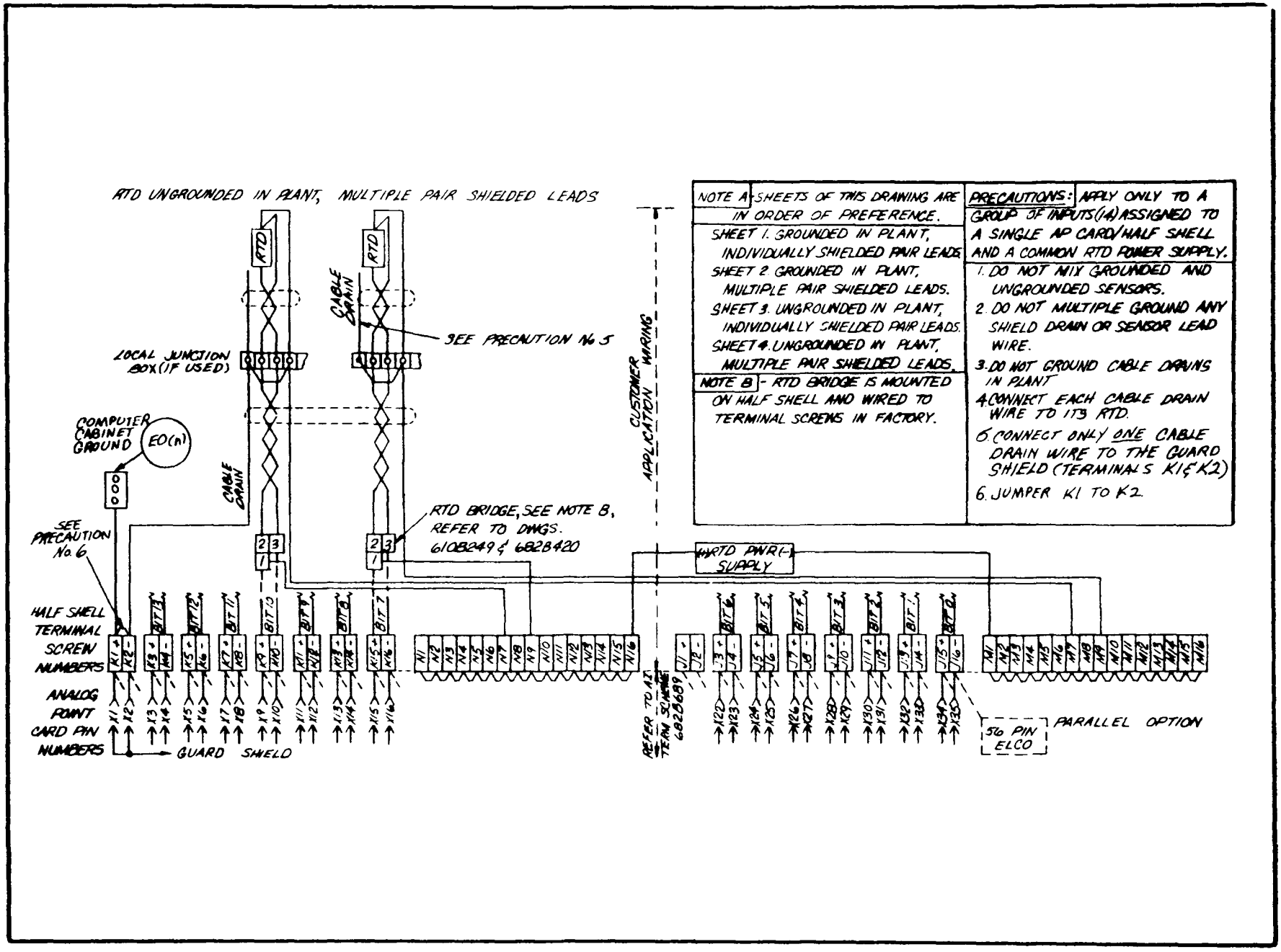


FIGURE 14d. RTD INPUT CONNECTIONS (REF. DWG. 682B687, SHEET 4)

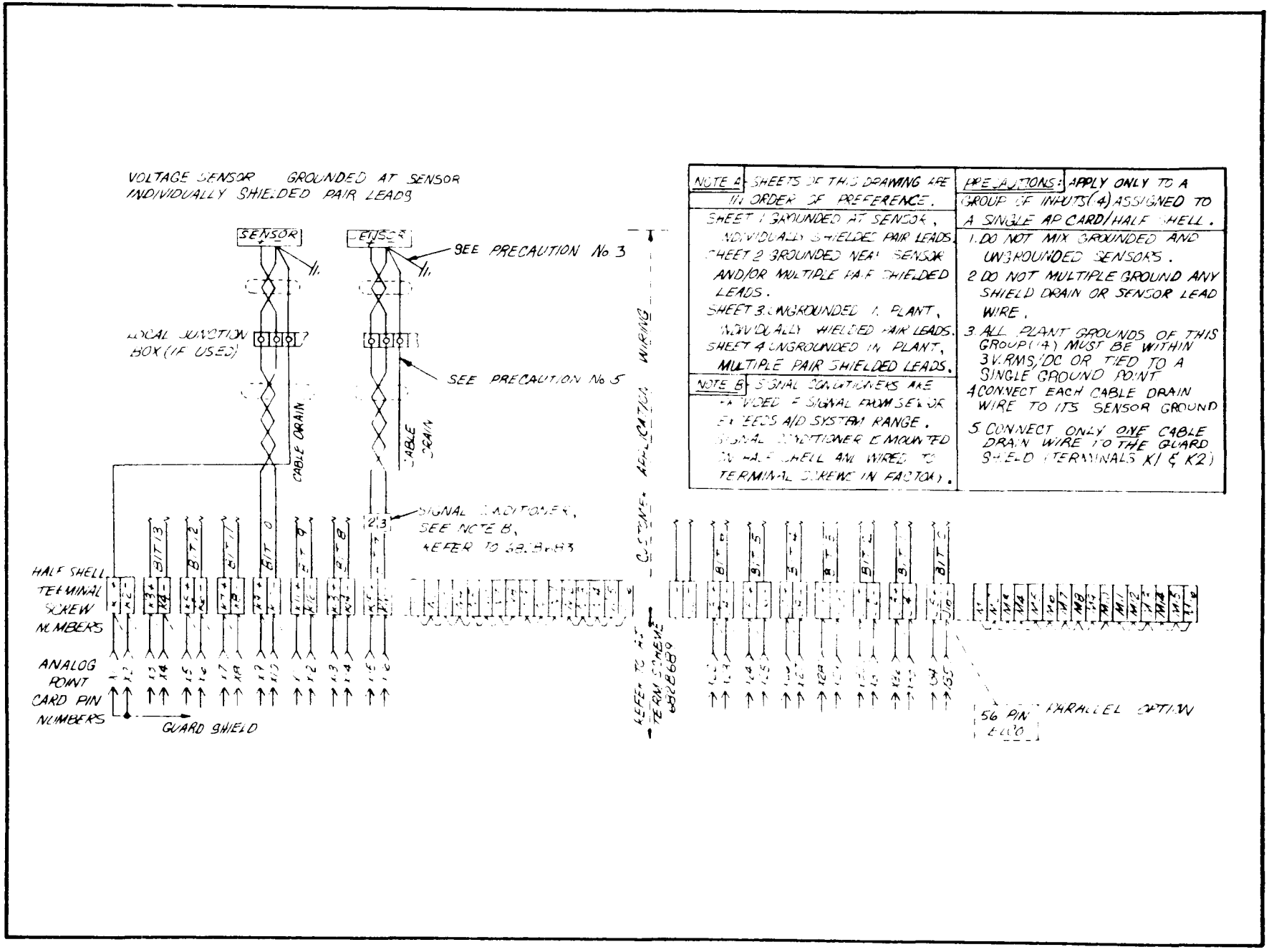


FIGURE 15a. VOLTAGE SENSOR INPUT CONNECTIONS (REF. DWG. 682B688, SHEET 1)

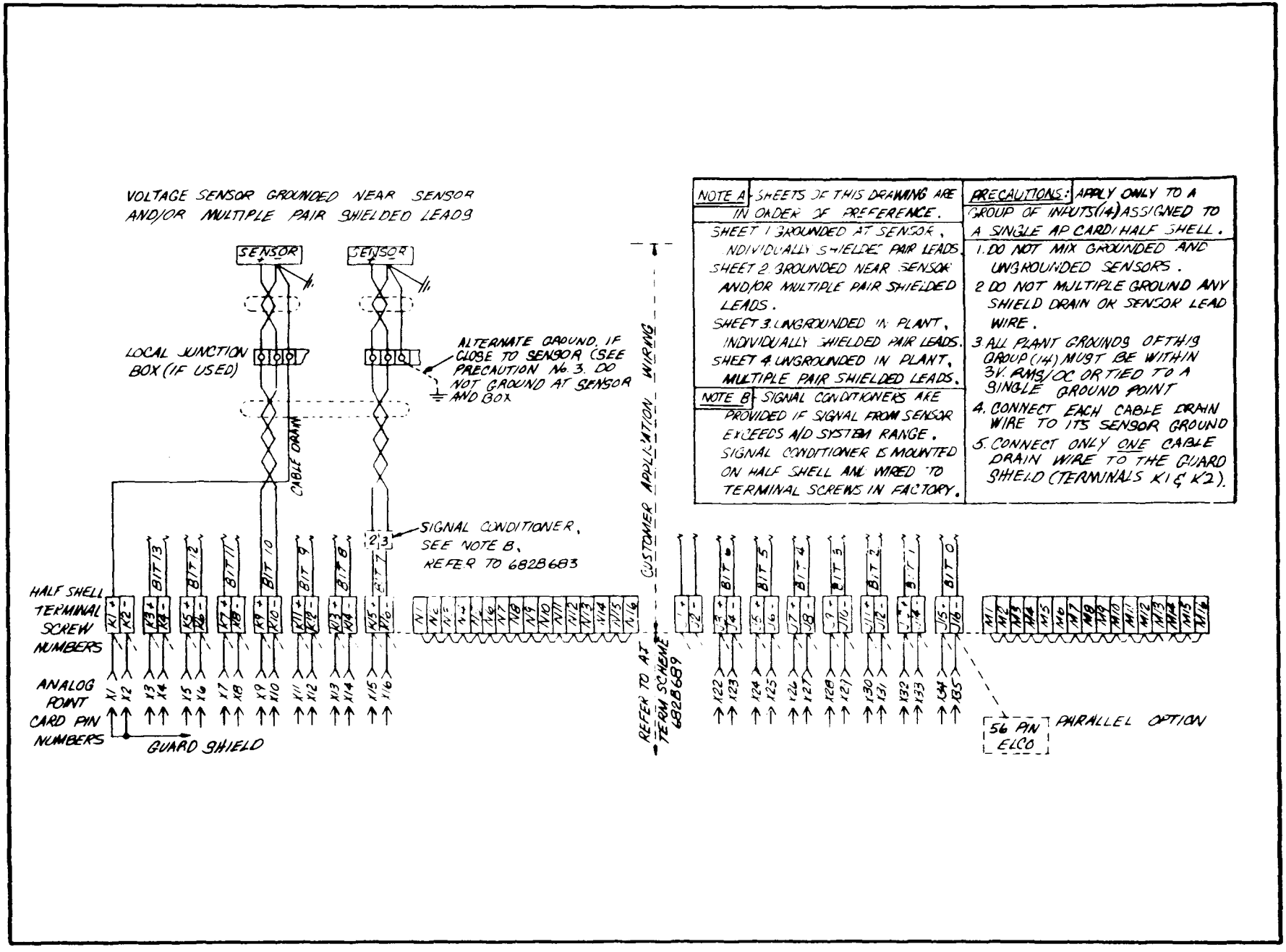


FIGURE 15b. VOLTAGE SENSOR INPUT CONNECTIONS (REF. DWG. 682B688, SHEET 2)

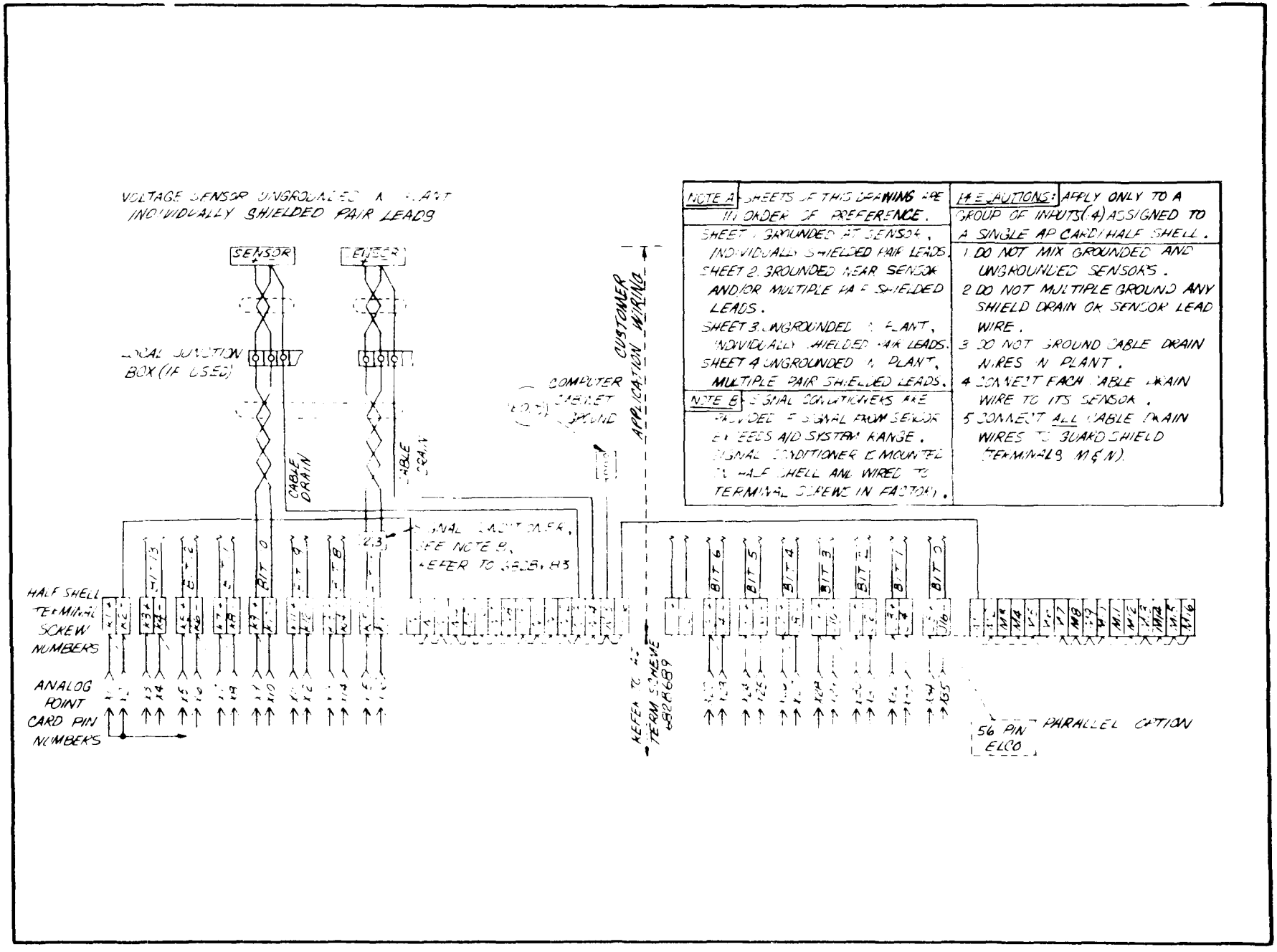


FIGURE 15c. VOLTAGE SENSOR INPUT CONNECTIONS (REF. DWG. 682B688, SHEET 3)

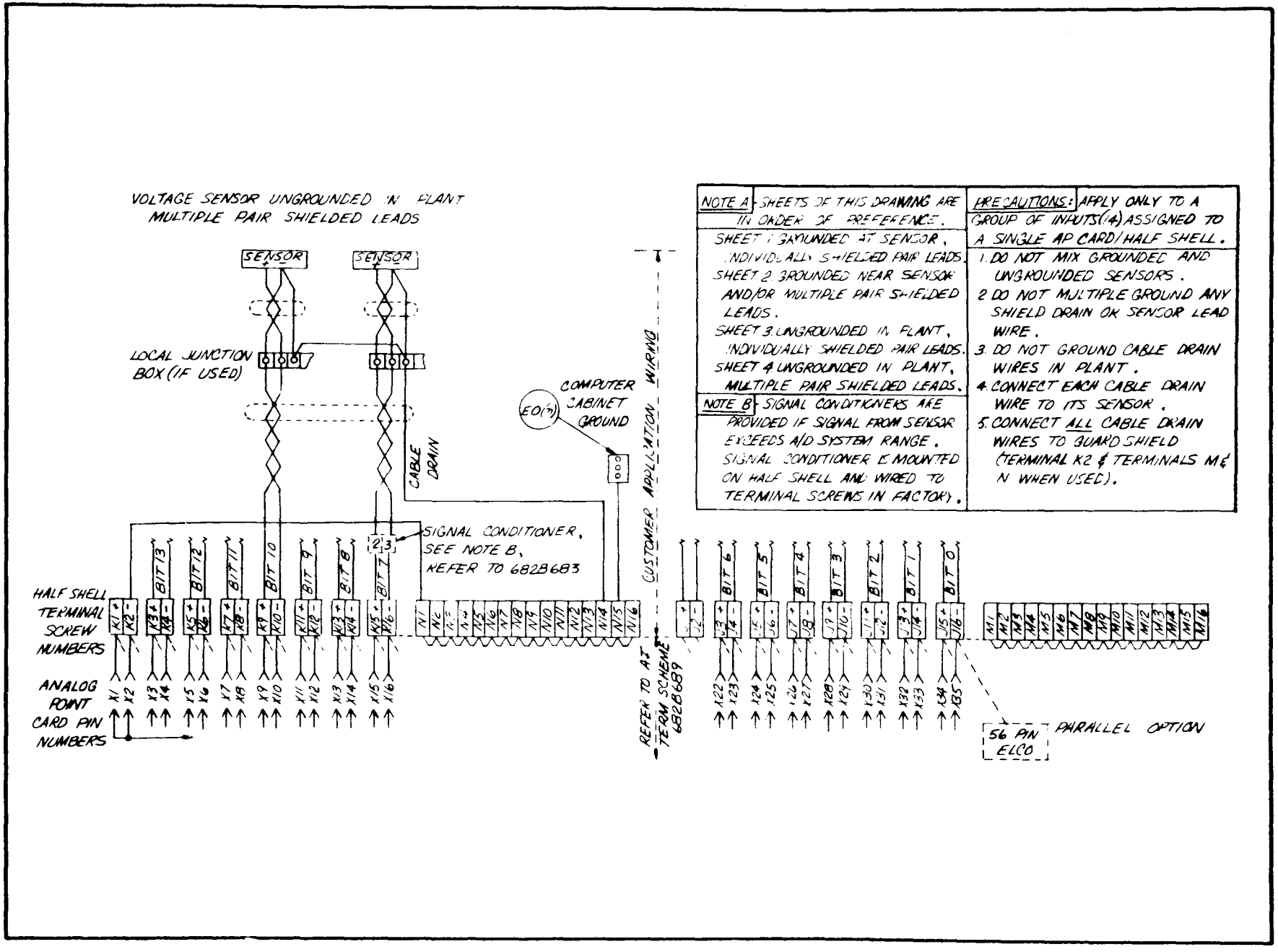


FIGURE 15d. VOLTAGE SENSOR INPUT CONNECTIONS (REF. DWG. 682B688, SHEET 4)

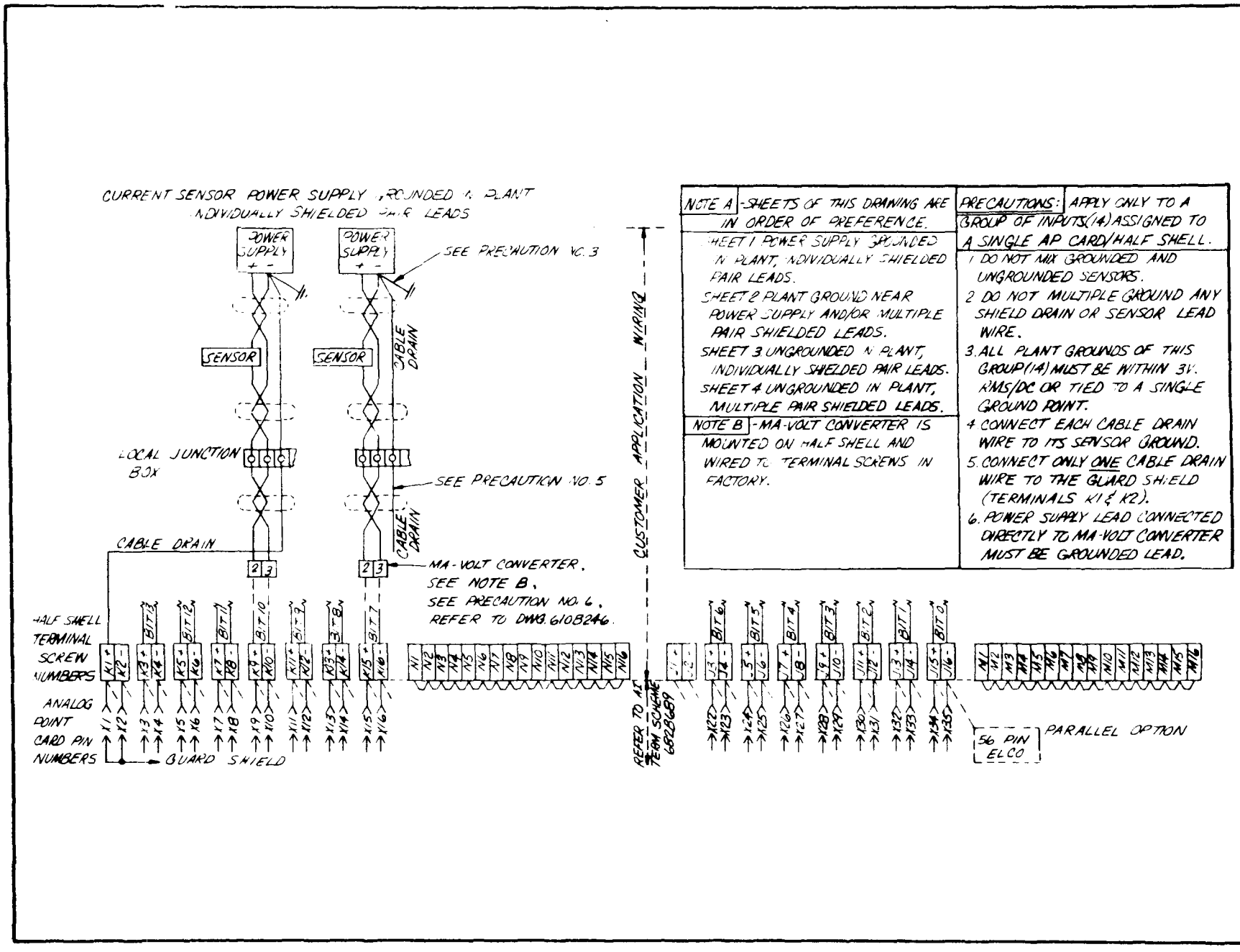


FIGURE 16a. CURRENT SENSOR INPUT CONNECTIONS (REF. DWG. 682B690, SHEET 1)

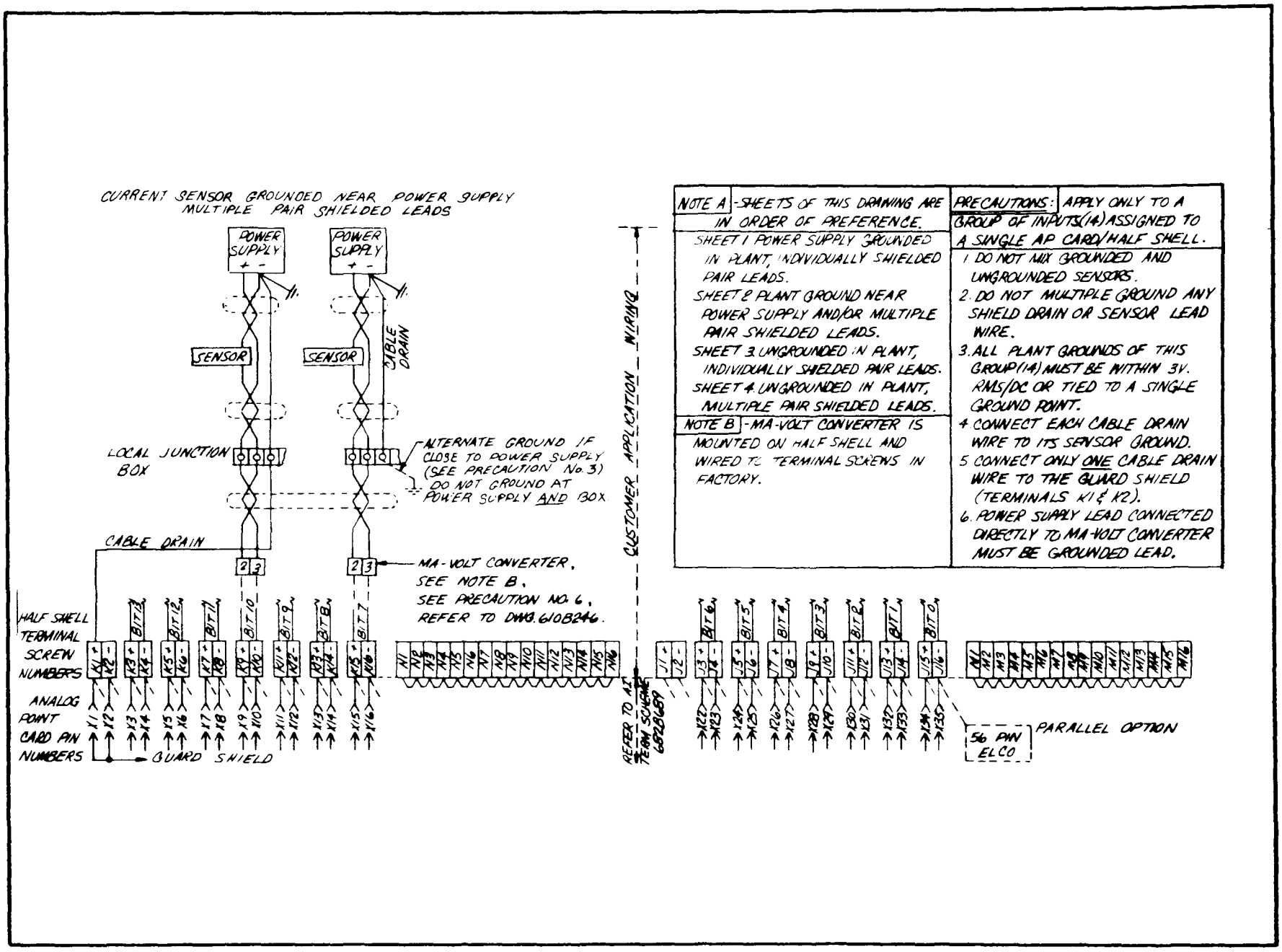


FIGURE 16b. CURRENT SENSOR INPUT CONNECTIONS (REF. DWG. 682B690, SHEET 2)

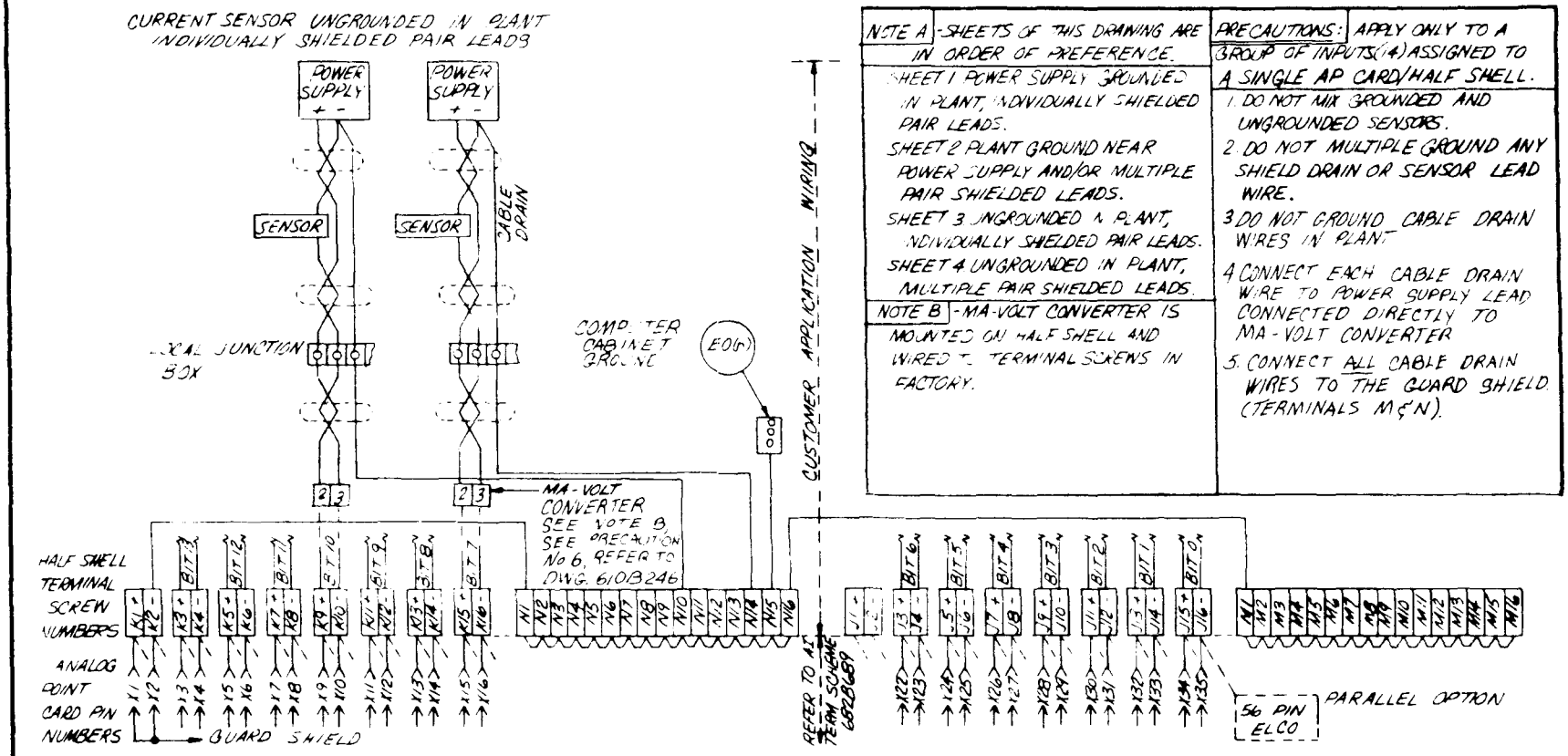


FIGURE 16c. CURRENT SENSOR INPUT CONNECTIONS (REF. DWG. 682B690, SHEET 3)

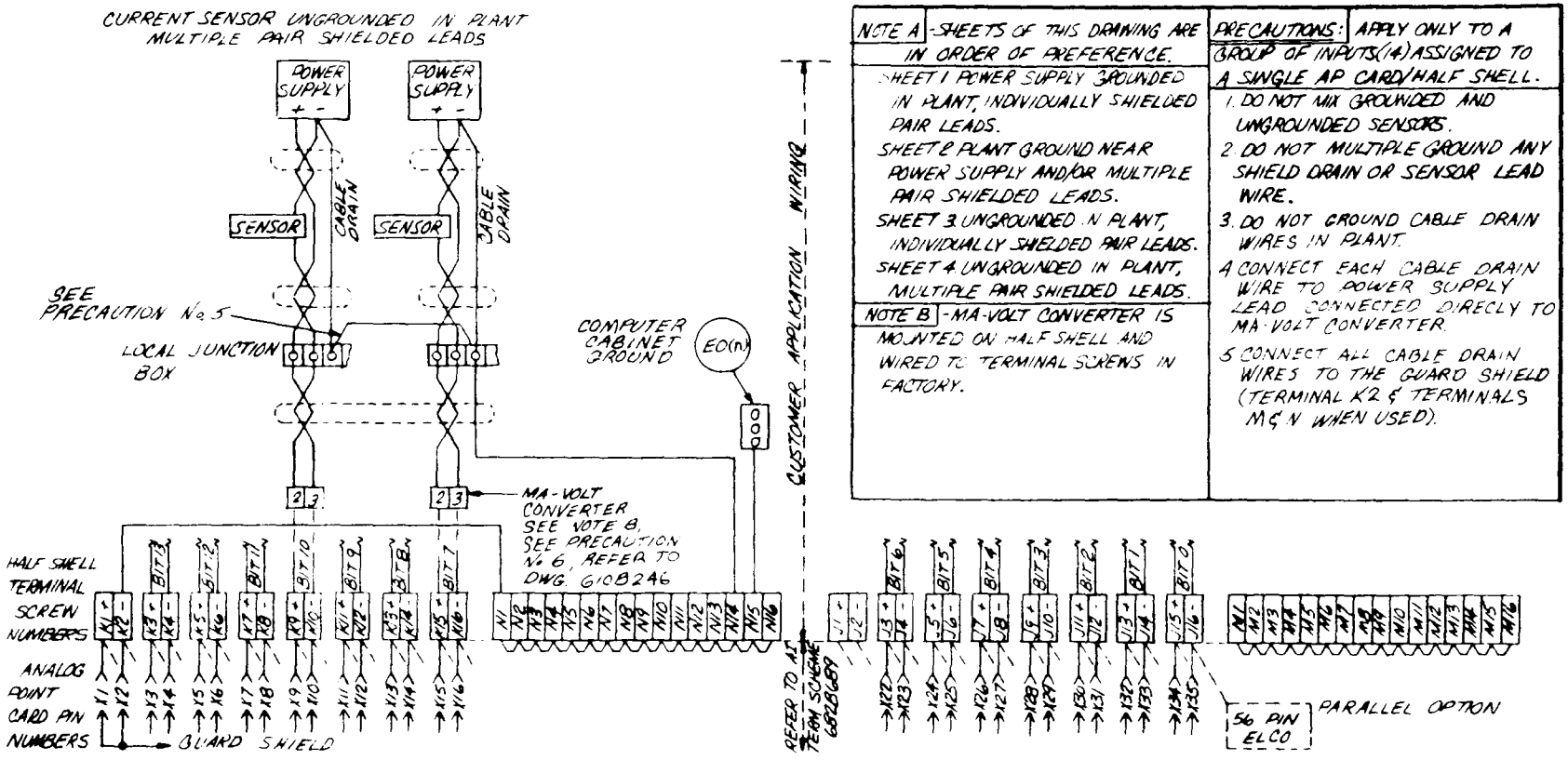


FIGURE 16d. CURRENT SENSOR INPUT CONNECTIONS (REF. DWG. 682B690, SHEET 4)

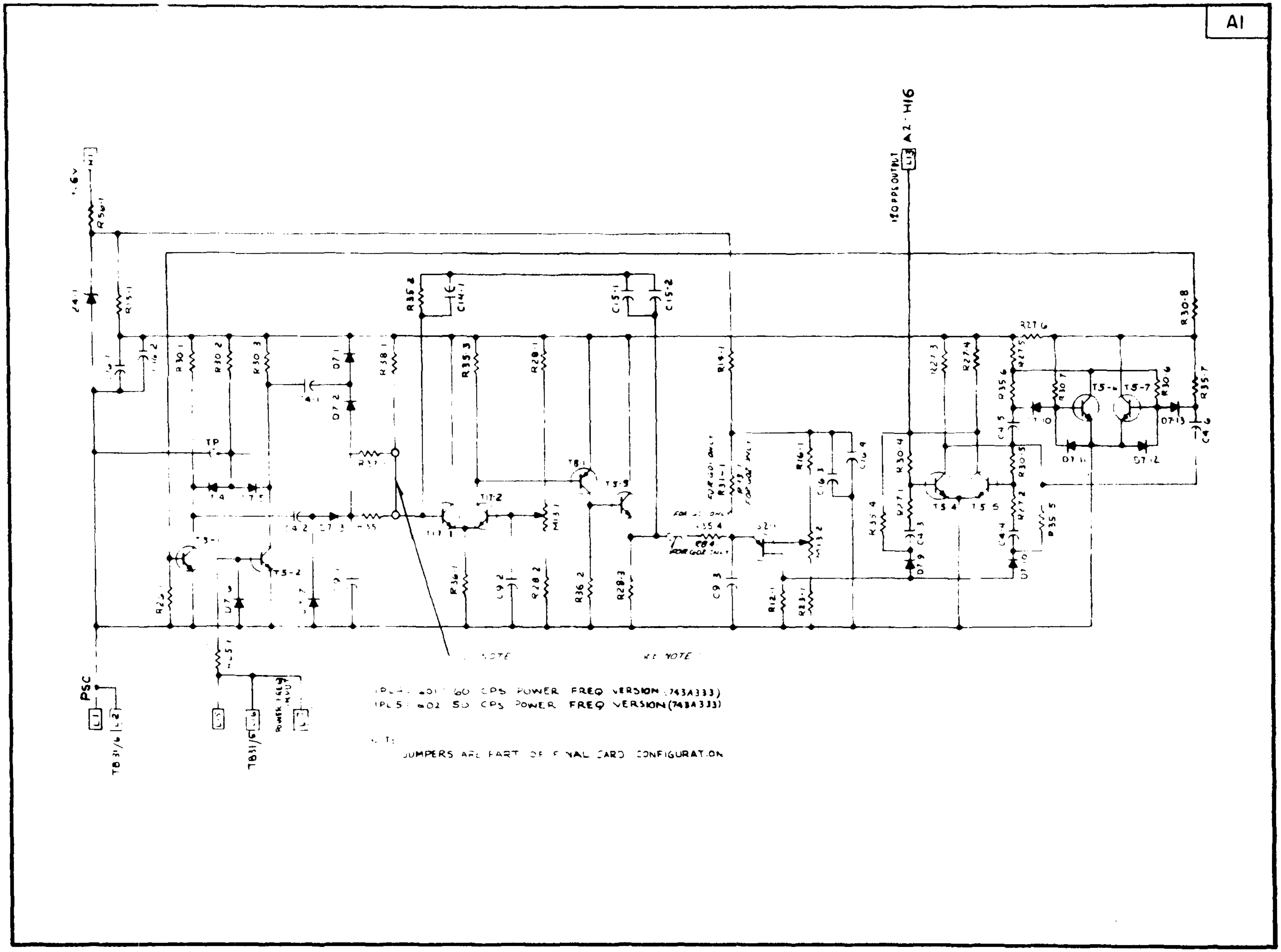


FIGURE 17. PHASE LOCK OSCILLATOR LOGIC (REF. DWG. 867C291, SUB 2)

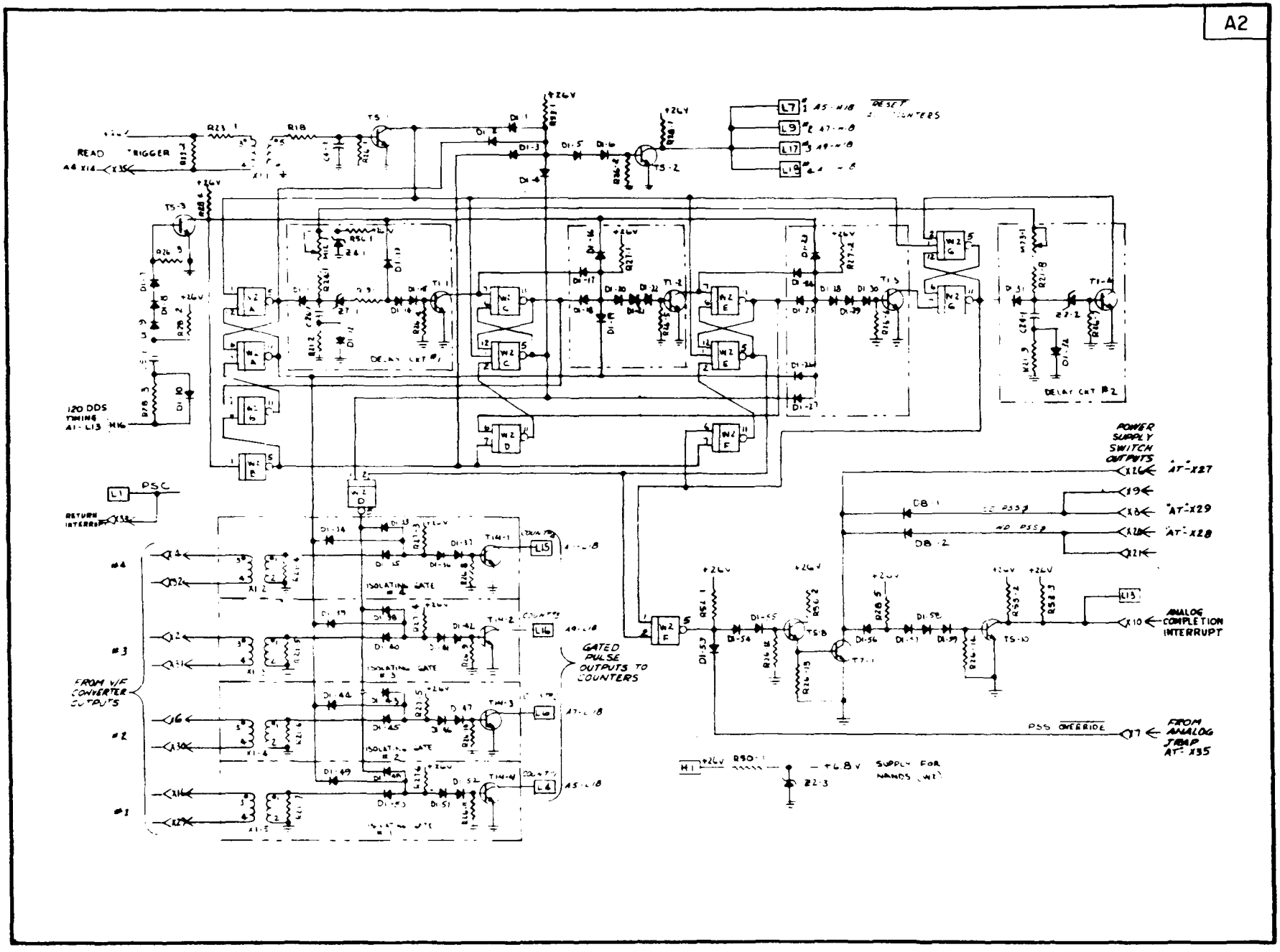


FIGURE 18. ANALOG CONTROL CARD LOGIC (REF. DWG. 867C292, SUB 2)

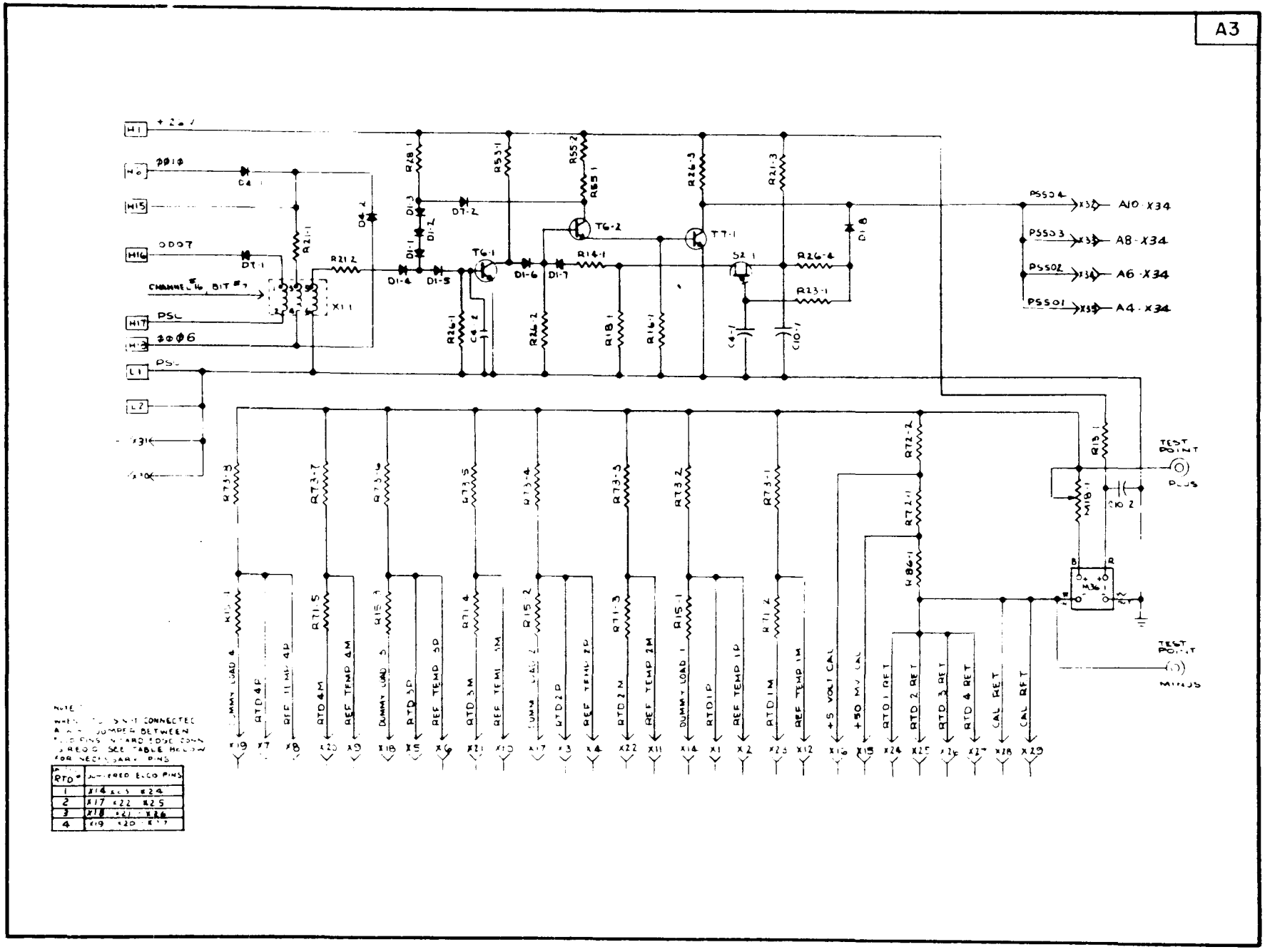


FIGURE 19. CALIBRATOR CARD LOGIC (REF. DWG. 867C293, SUB 2)

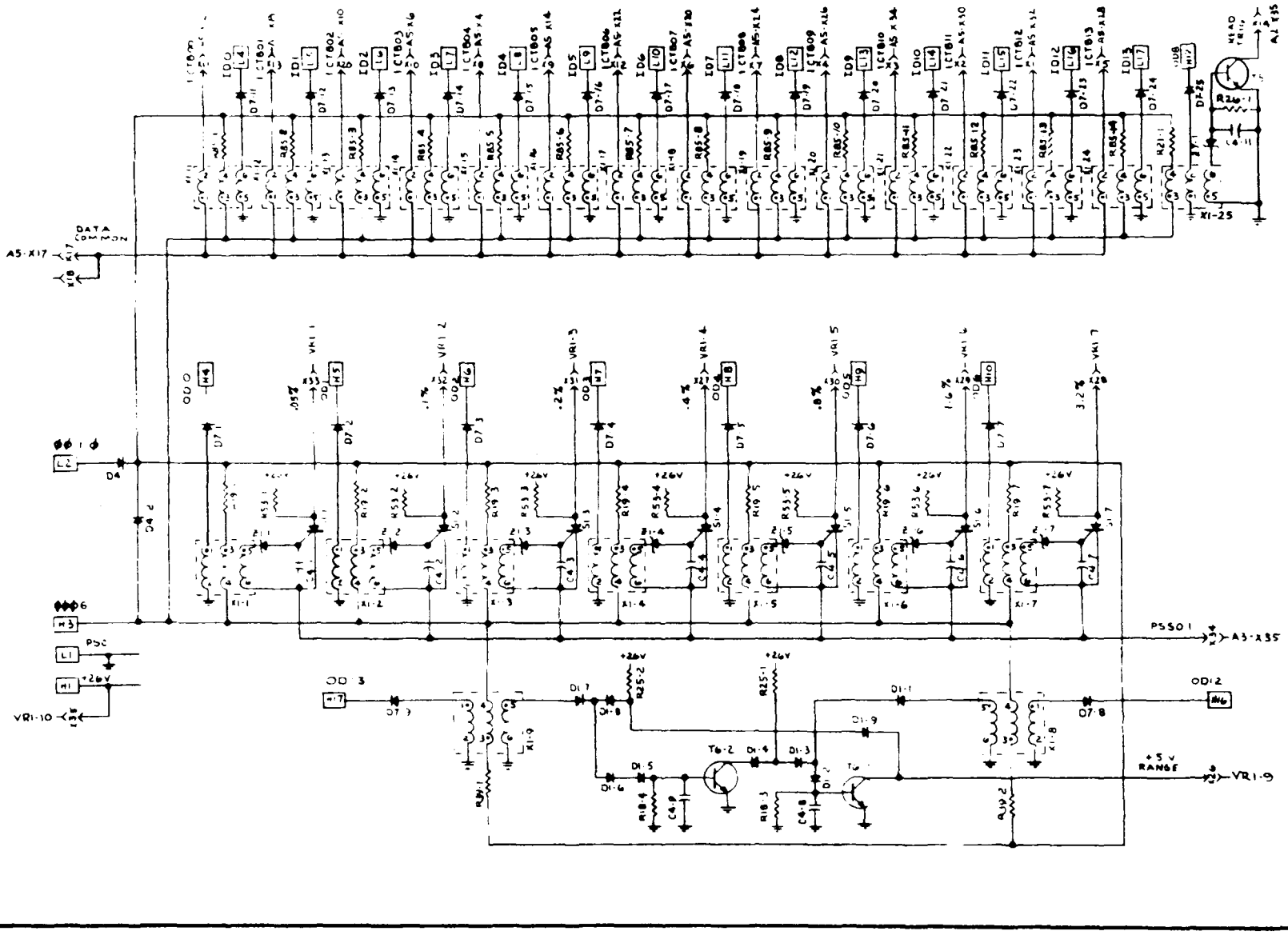


FIGURE 20. #1 SPAN & GAIN W/BUFFER LOGIC (REF. DWG. 867C294, SUB 3)

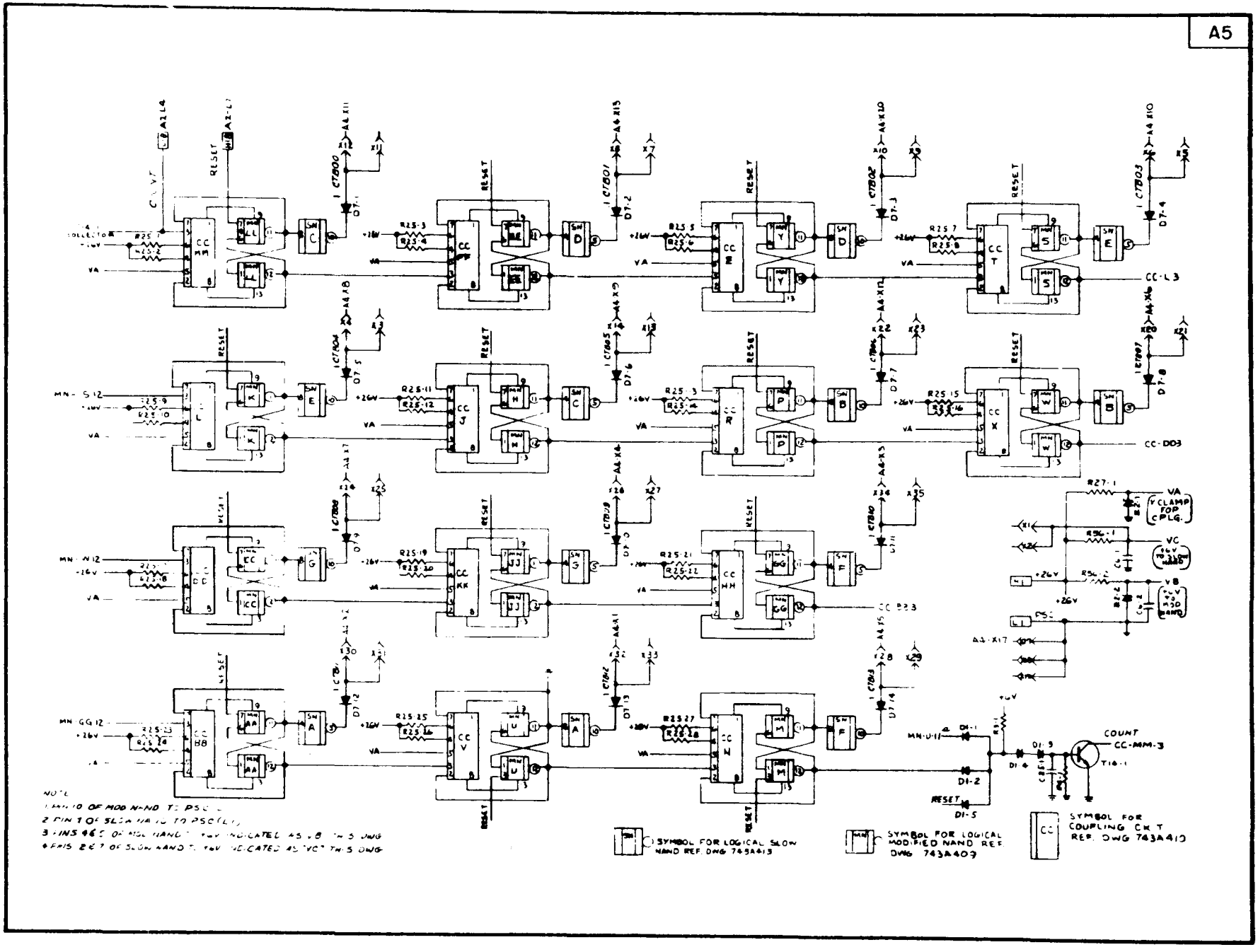


FIGURE 21. #1 COUNTER CARD LOGIC (REF. DWG. 867C295, SUB 2)

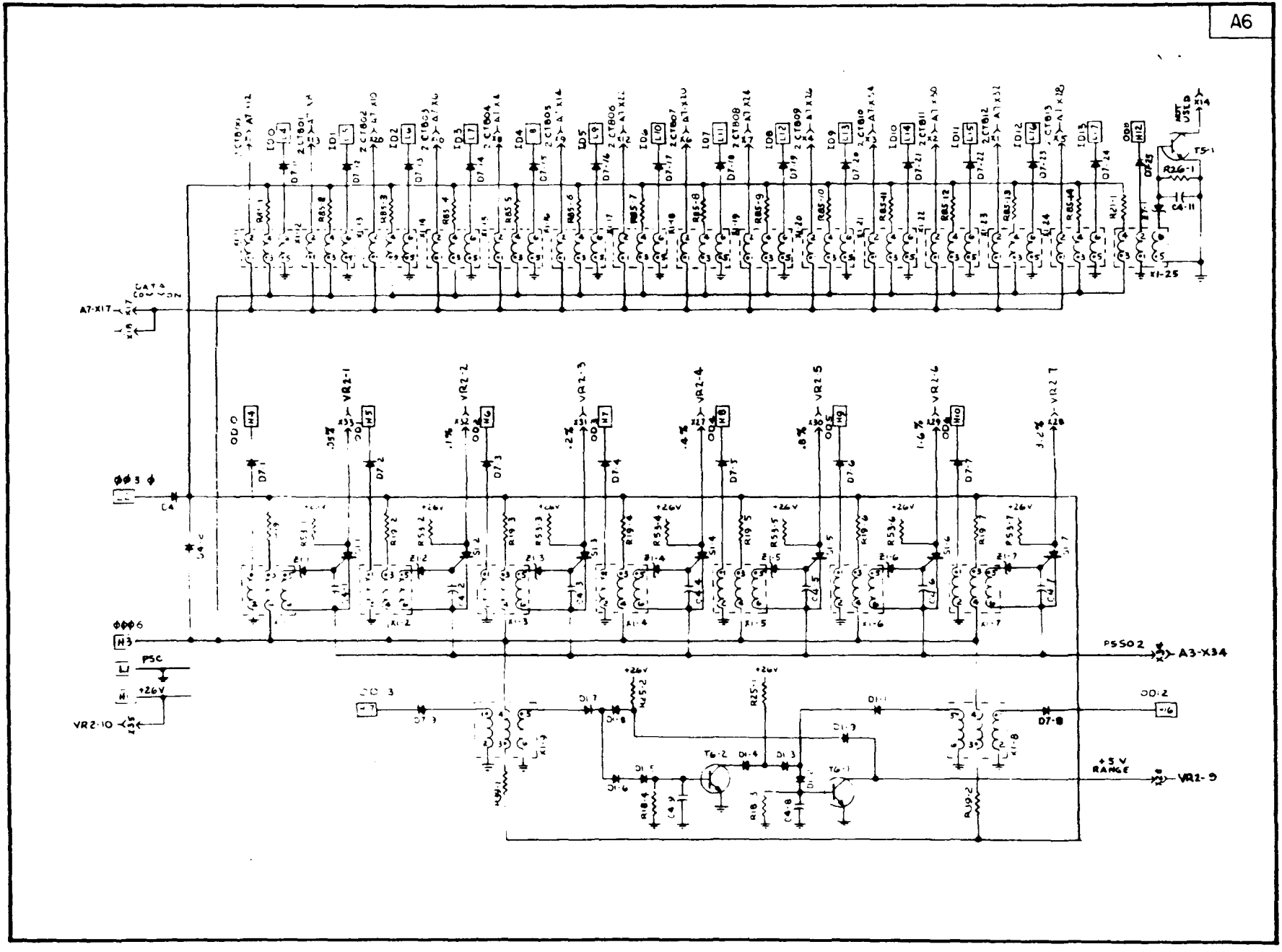


FIGURE 22. VR2 SPAN & GAIN W BUFFER LOGIC (REF. DWG. 867C296, SUB 3)

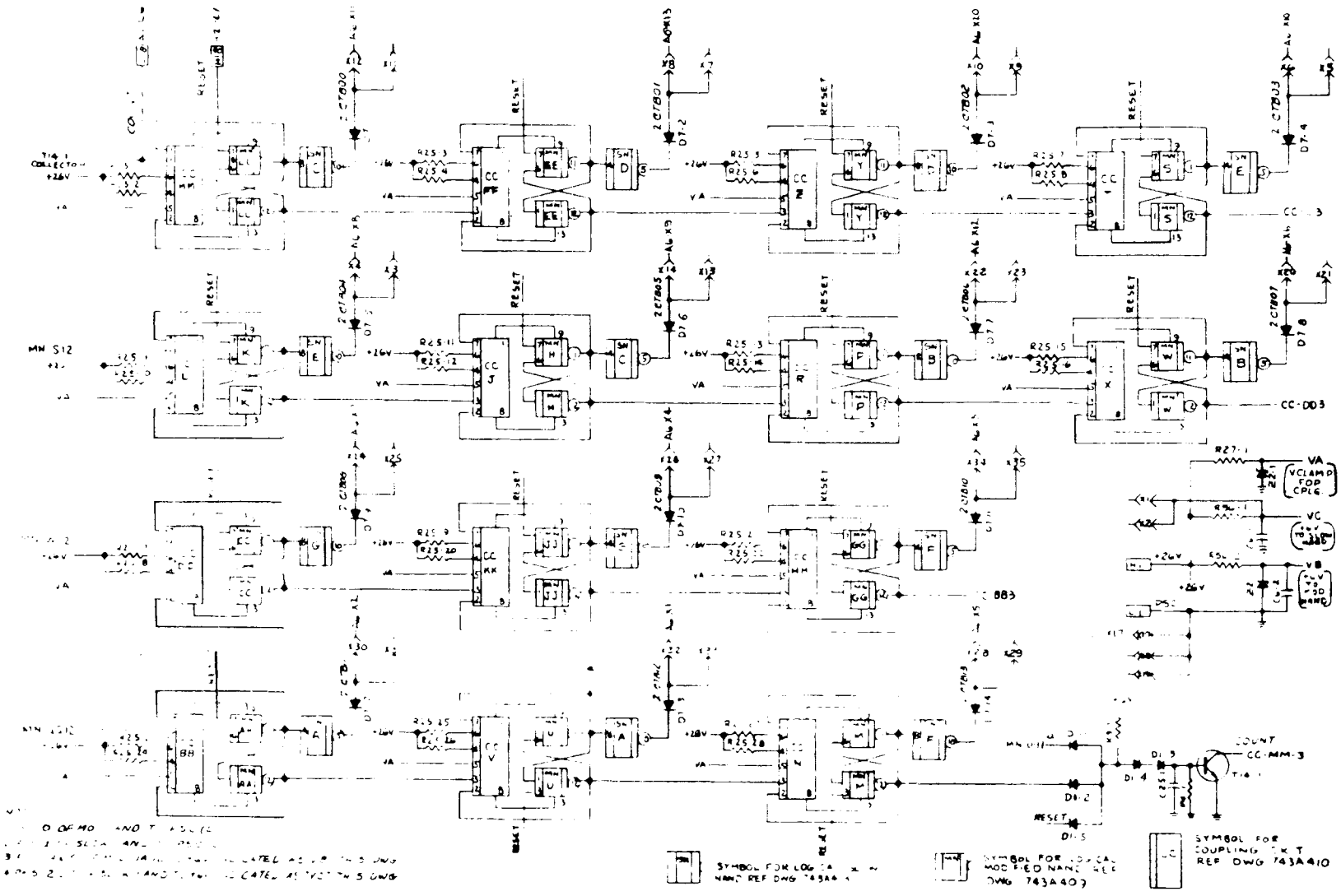


FIGURE 23. 2 COUNTER CARD LOGIC (REF. DWG. 867C297, SUB 2)

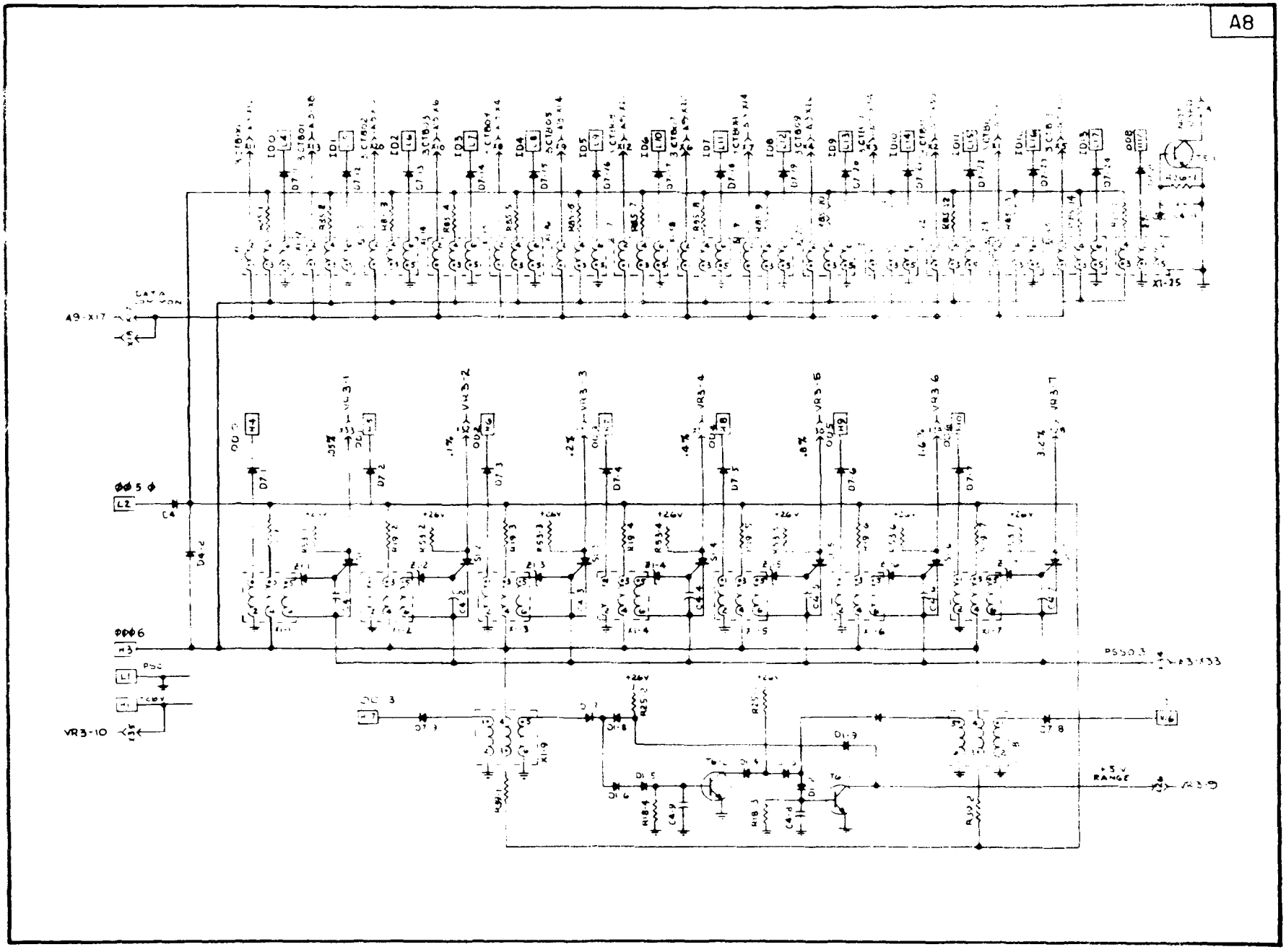


FIGURE 24. #3 SPAN & GAIN W BUFFER LOGIC (REF. DWG. 867C[illegible]

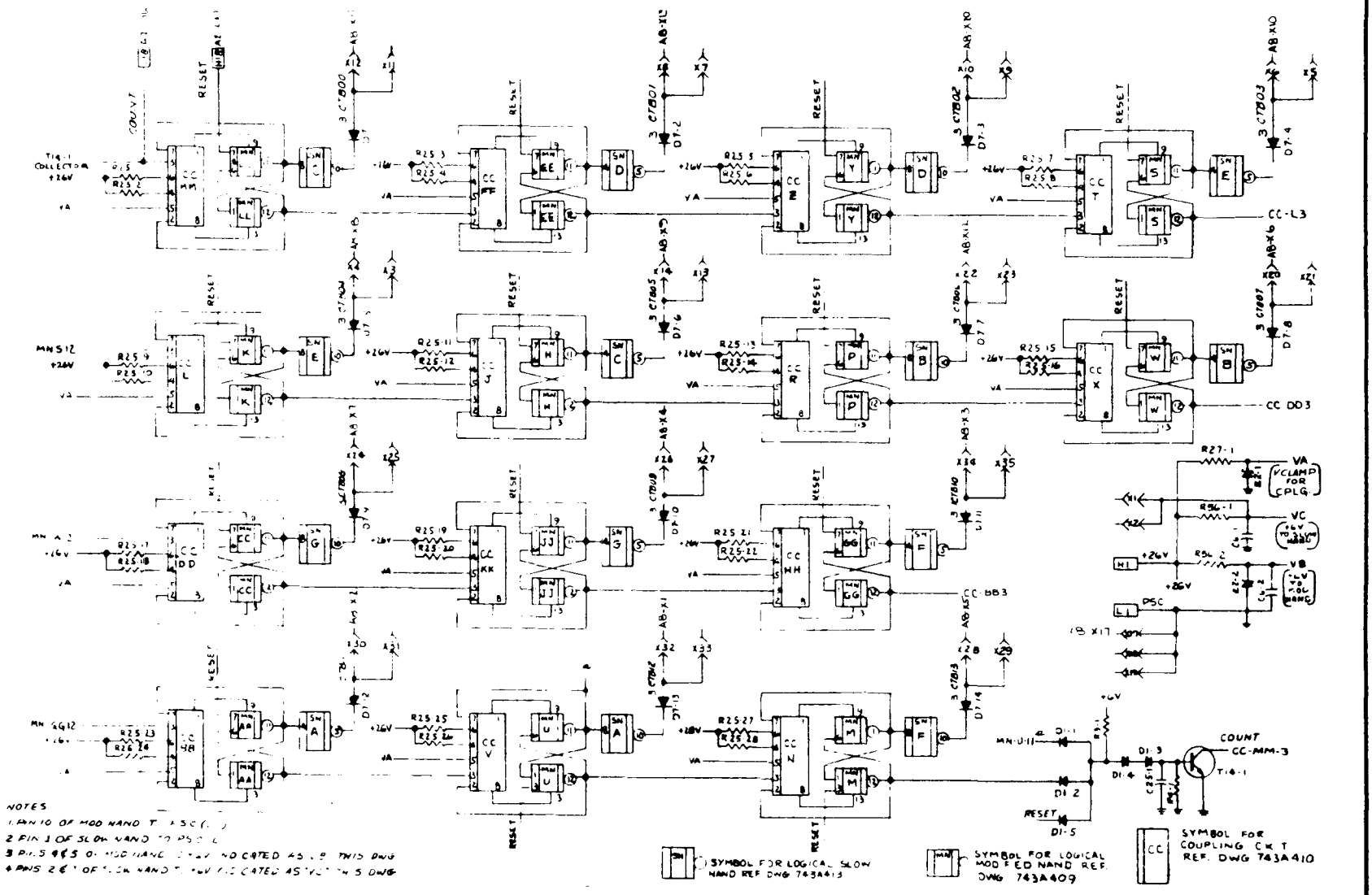


FIGURE 25. 43 COUNTER CARD LOGIC (REF. DWG. 867C299, SUB 2)

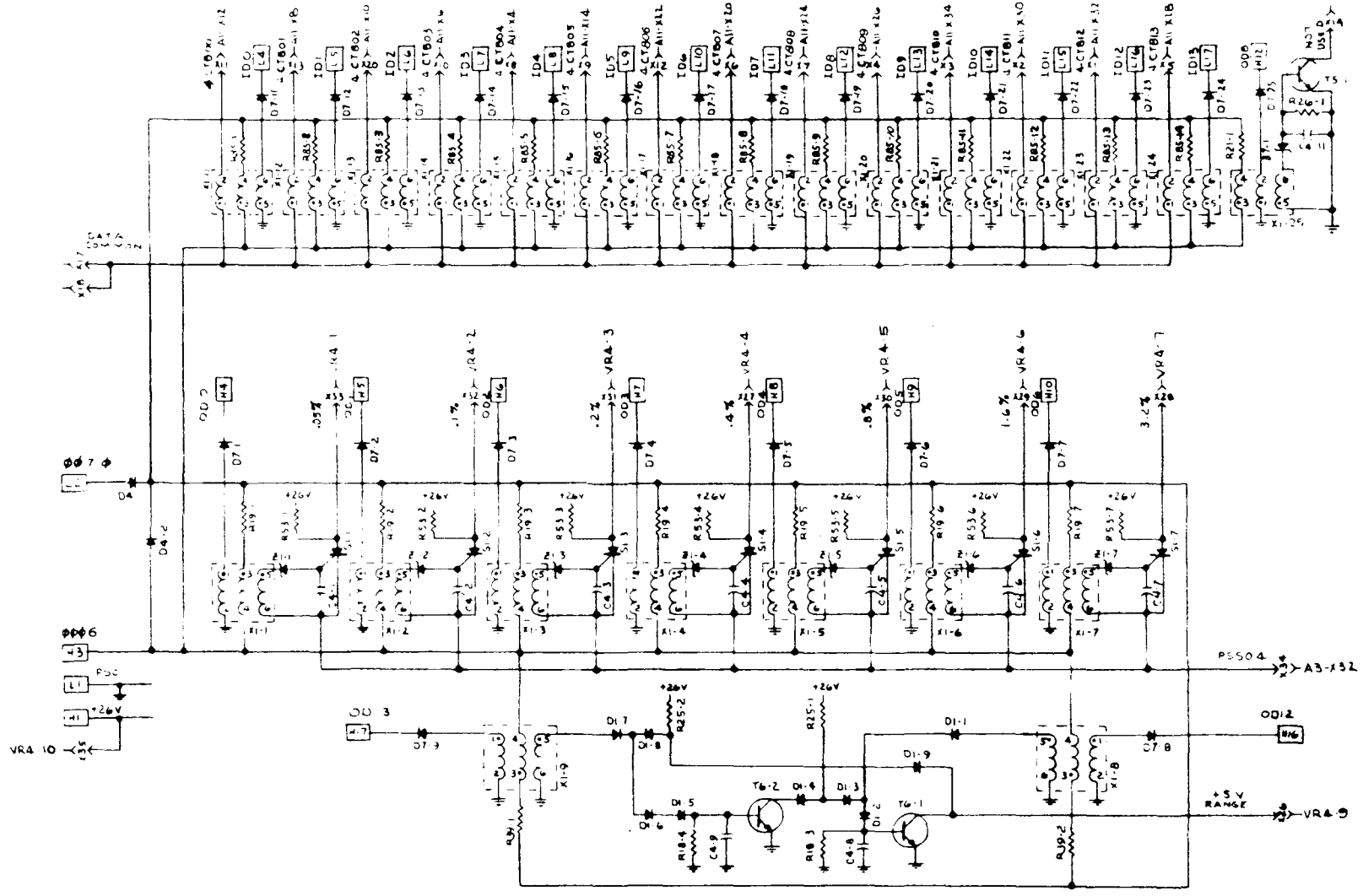


FIGURE 26. #4 SPAN & GAIN W BUFFER LOGIC (REF. DWG. 867C300, SUB 3)

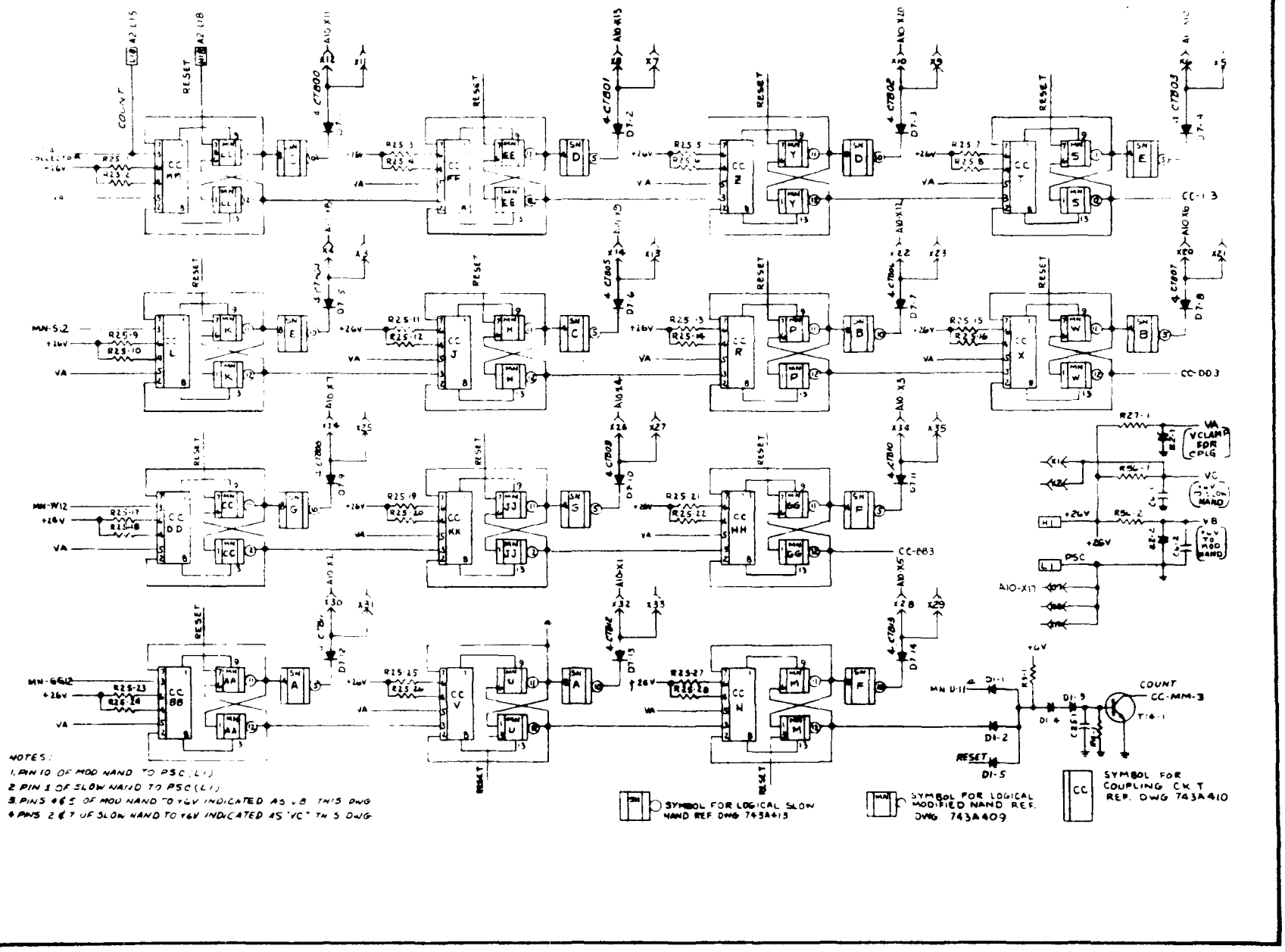


FIGURE 27. #4 COUNTER CARD LOGIC (REF. DWG. 867C301, SUB 2)

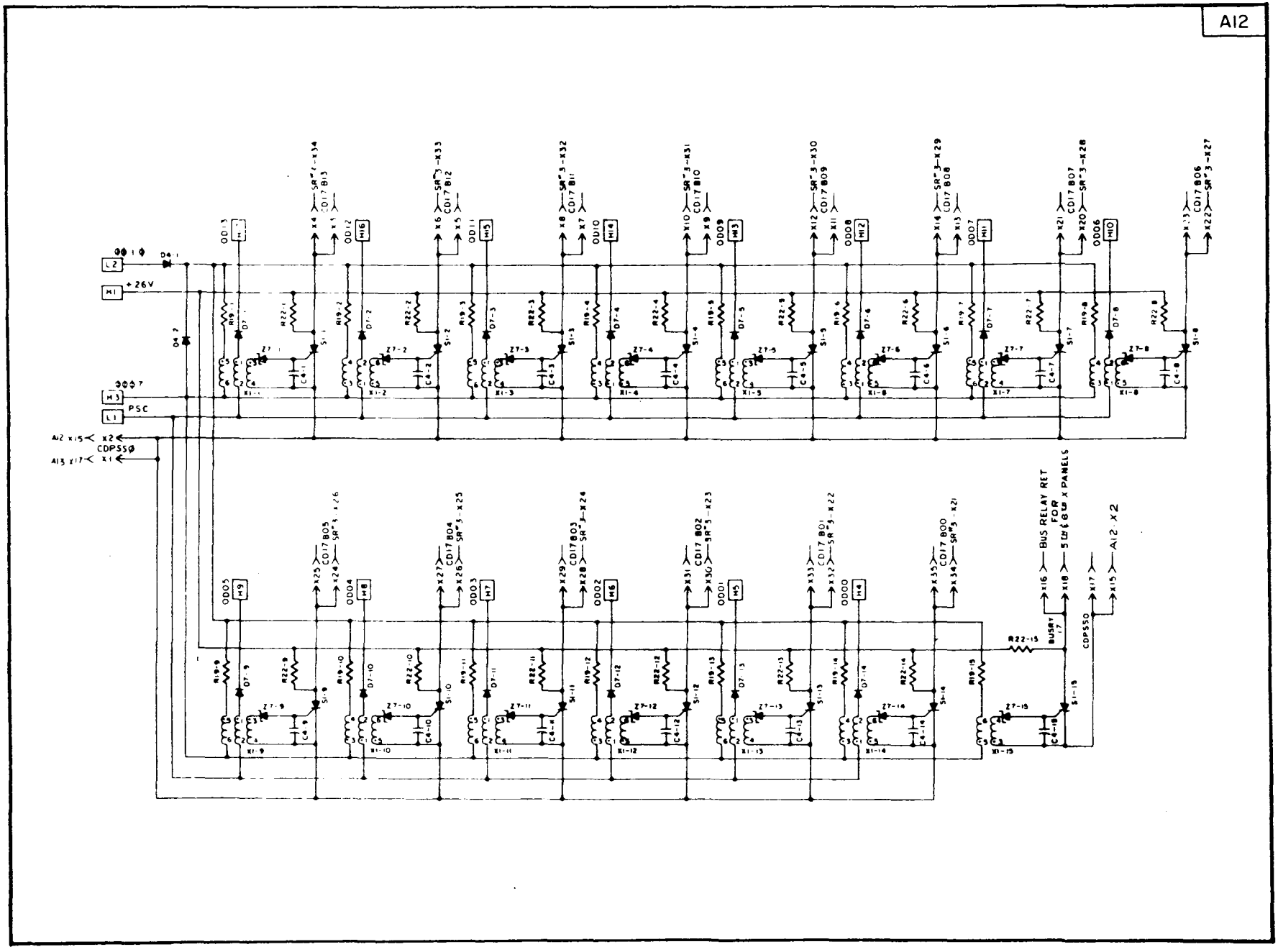


FIGURE 28. CHANNEL 17 DRIVER LOGIC (REF. DWG. 867C302, SUB 3)

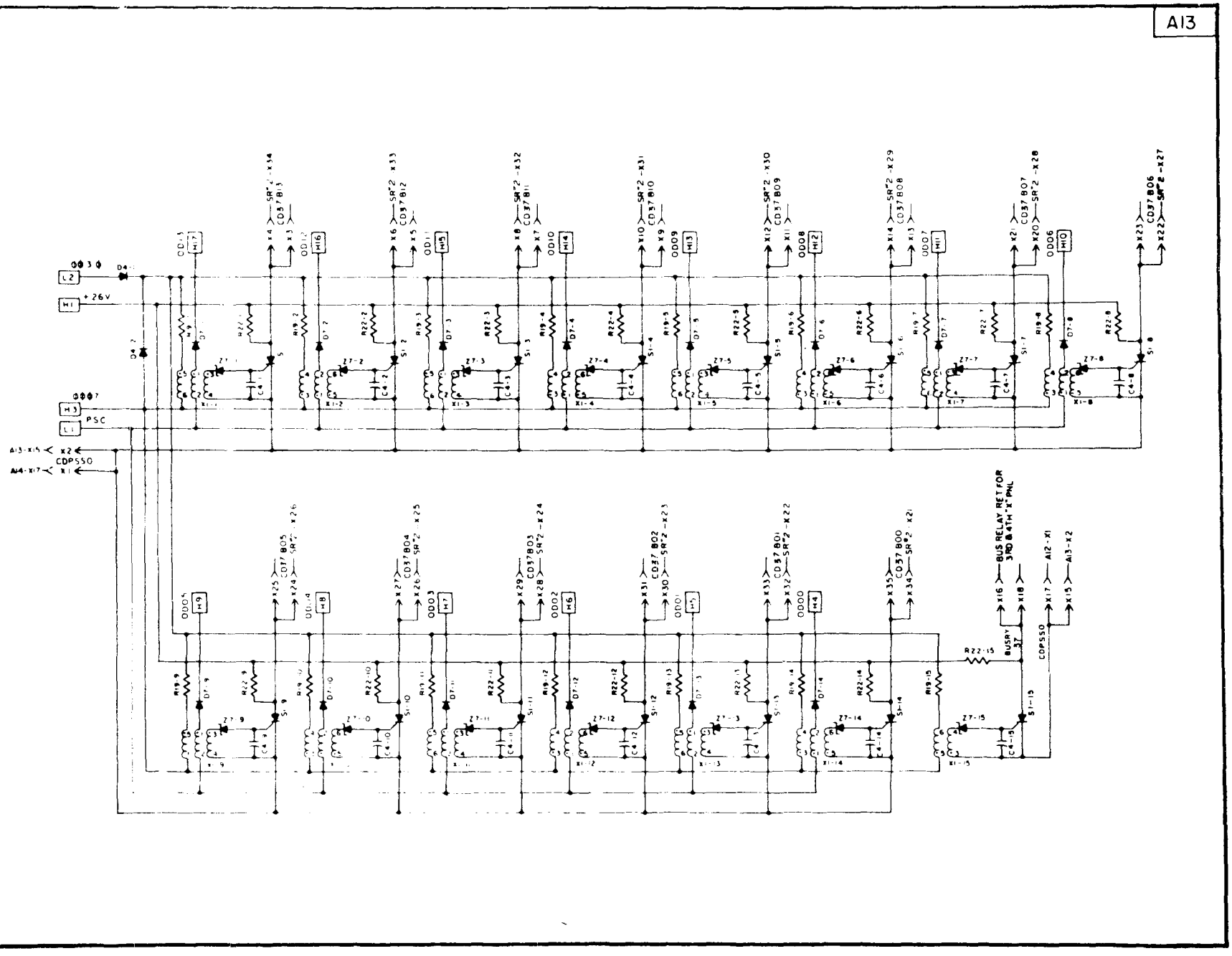


FIGURE 29. CHANNEL 37 DRIVER LOGIC (REF. DWG. 867C303, SUB 3)

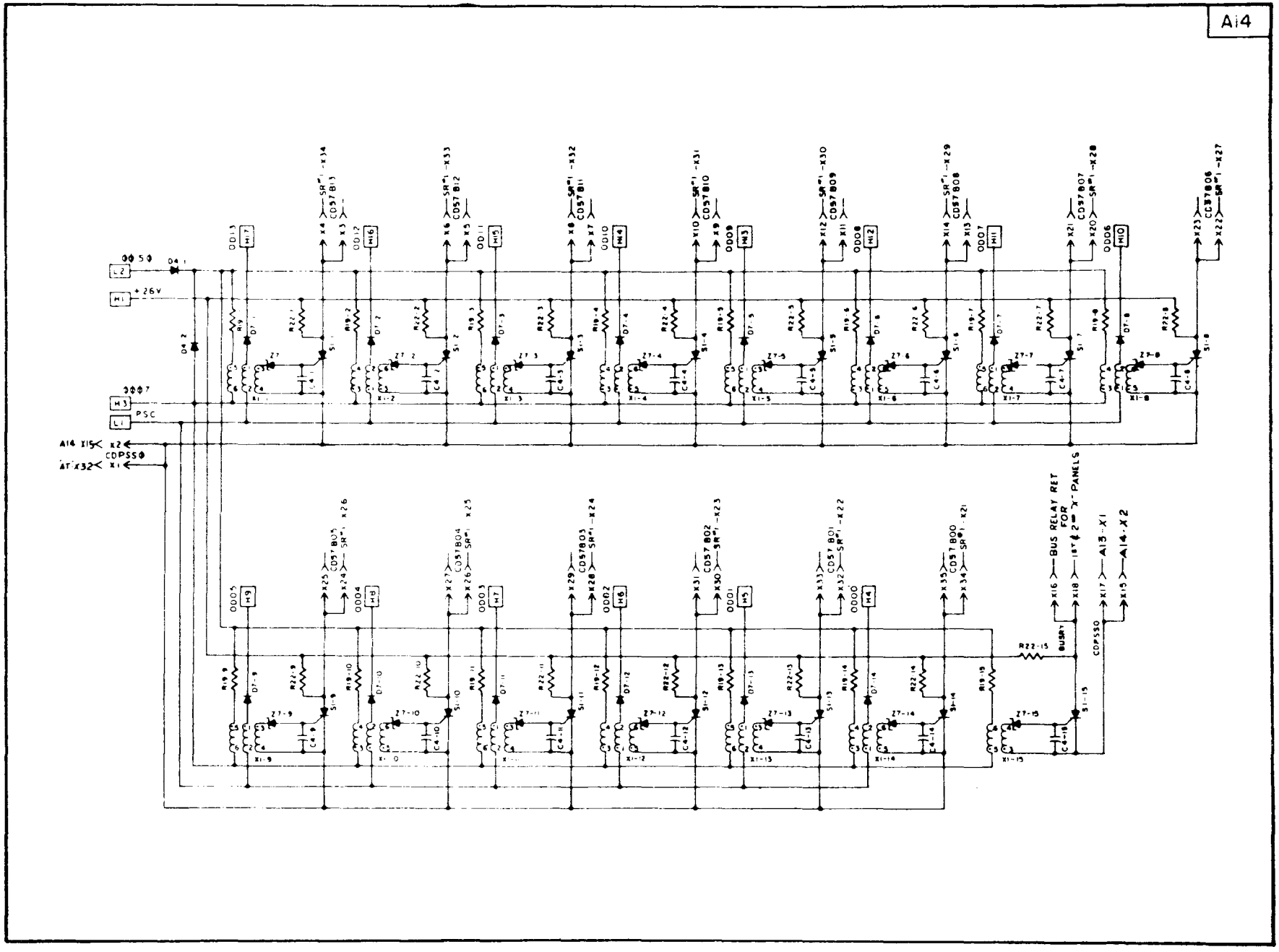


FIGURE 30. CHANNEL 57 DRIVER LOGIC (REF. DWG. 867C304, SUB 3)

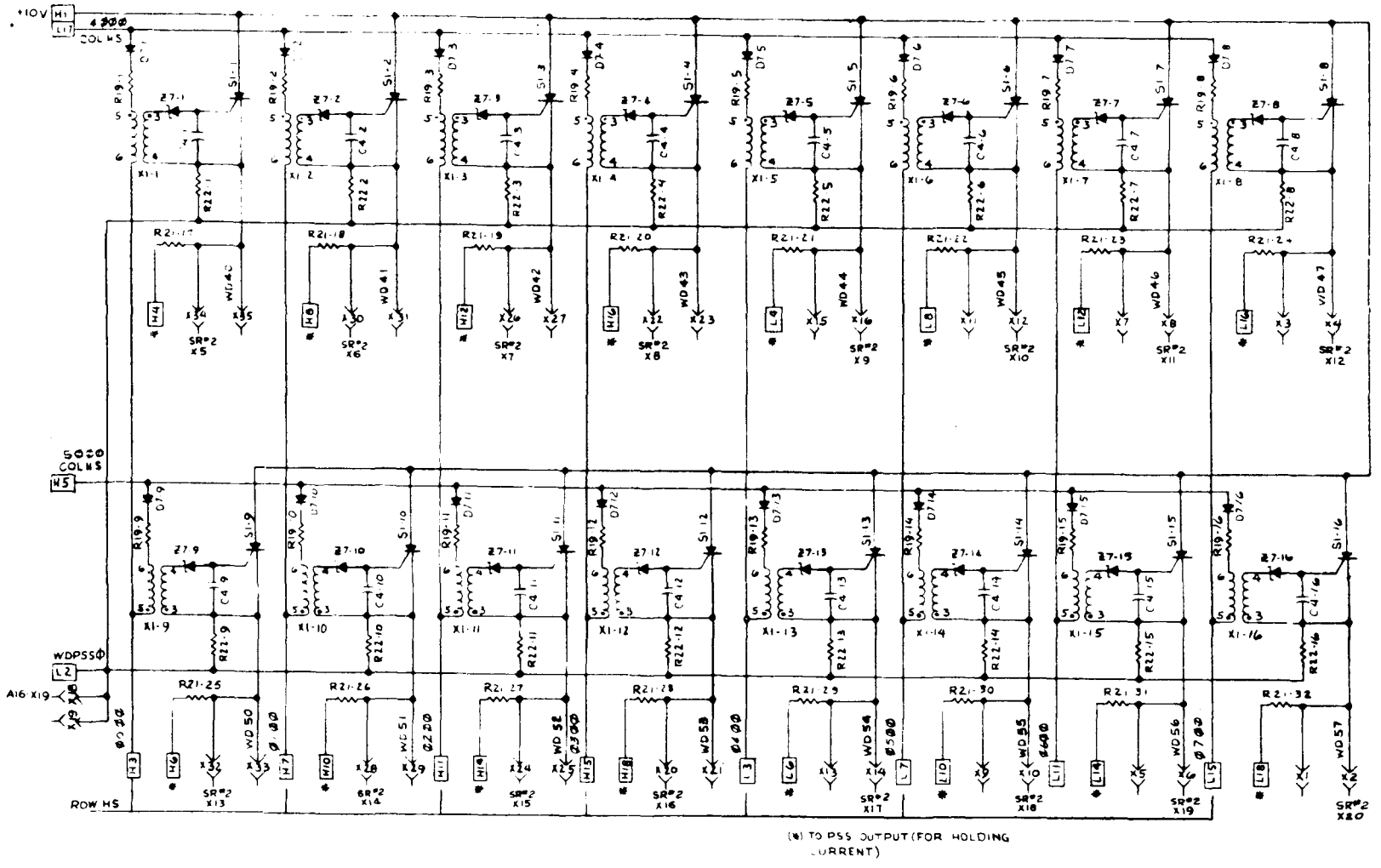


FIGURE 31. WORDS 40 TO 57 DRIVER LOGIC (REF. DWG. 867C305, SUB 3)

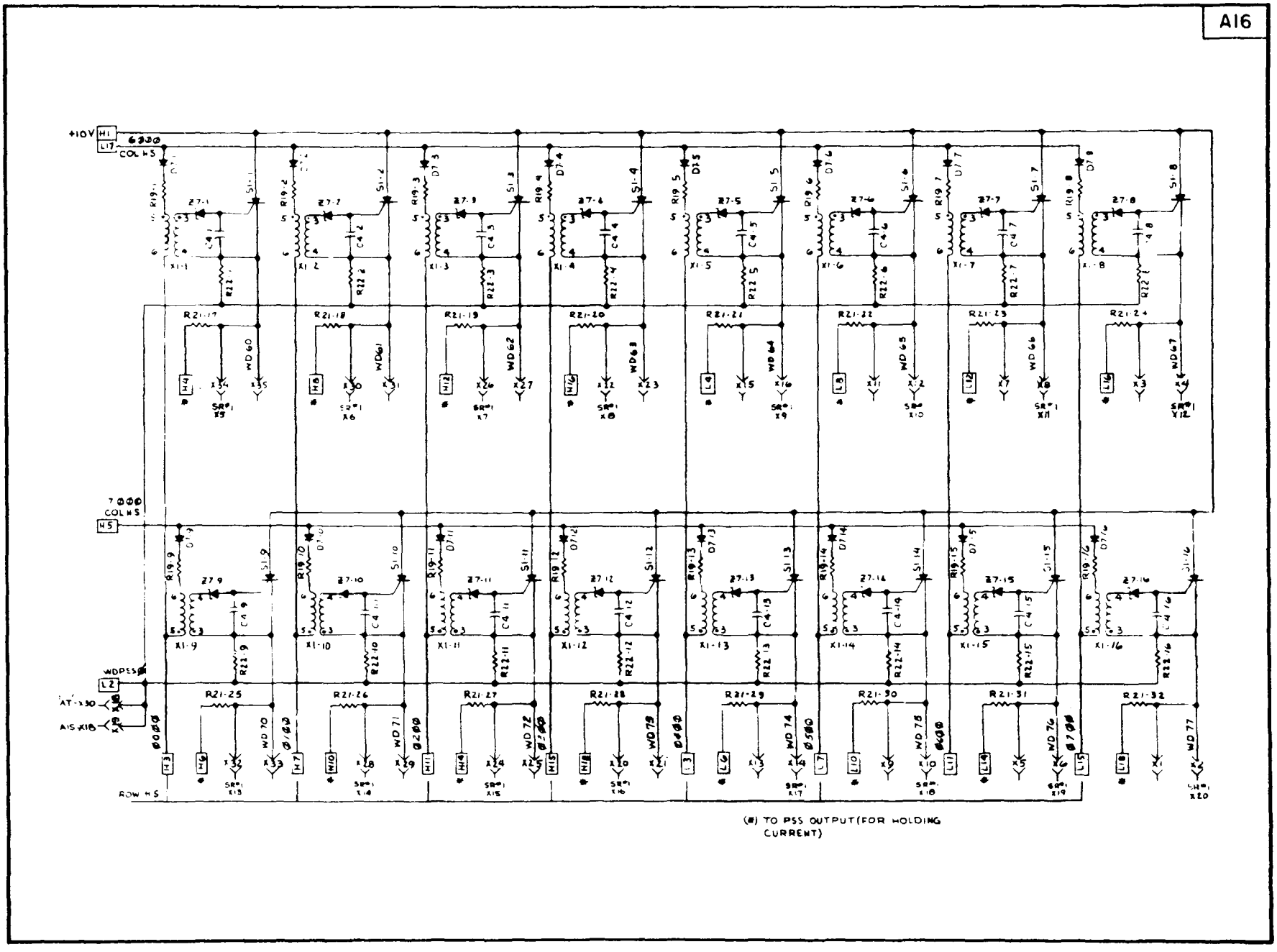


FIGURE 32. WORDS 60 TO 77 DRIVER LOGIC (REF. DWG. 867C306, SUB 3)

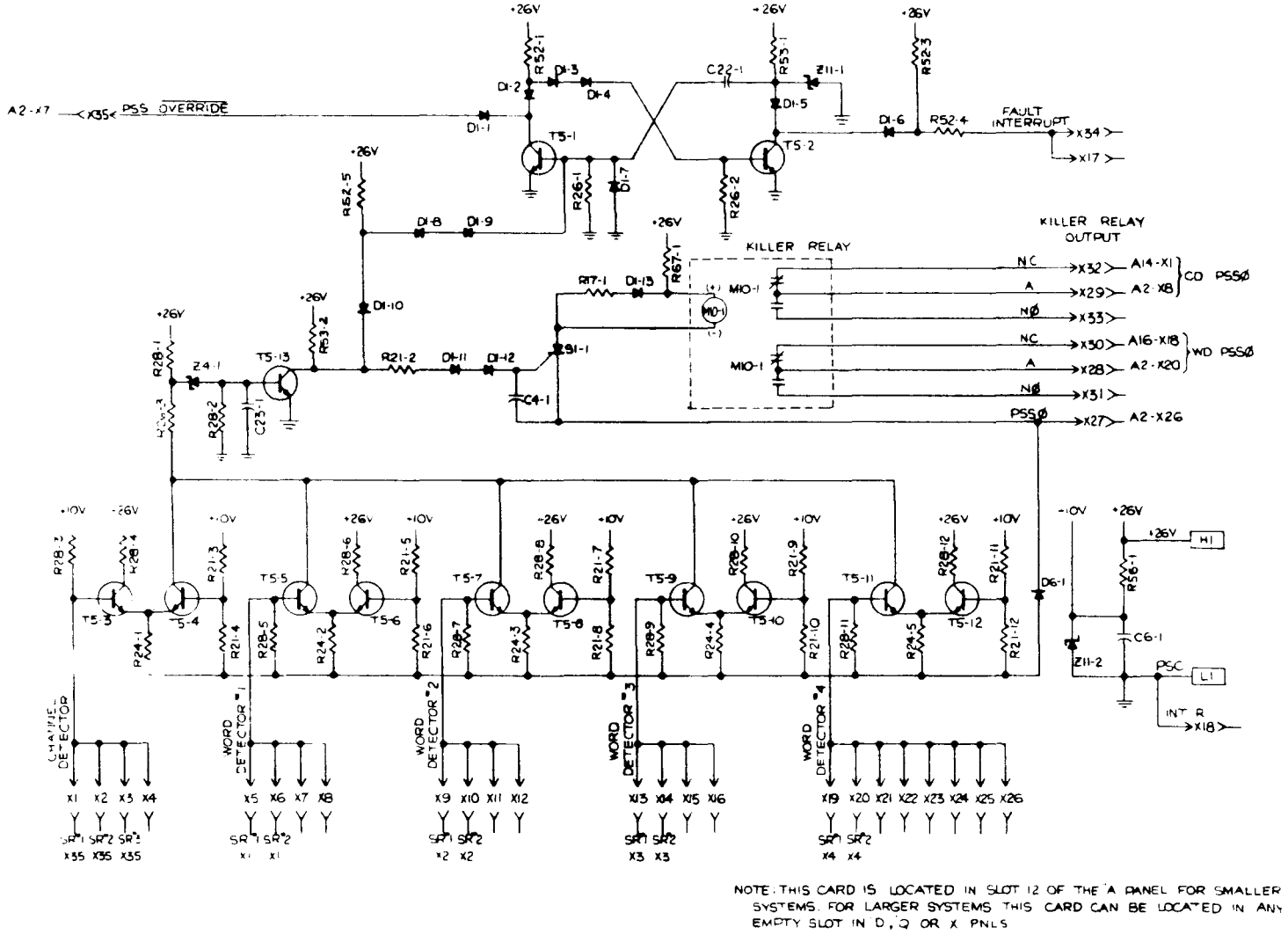


FIGURE 33. ANALOG TRAP LOGIC (REF. DWG. 867C994, SUB 2)

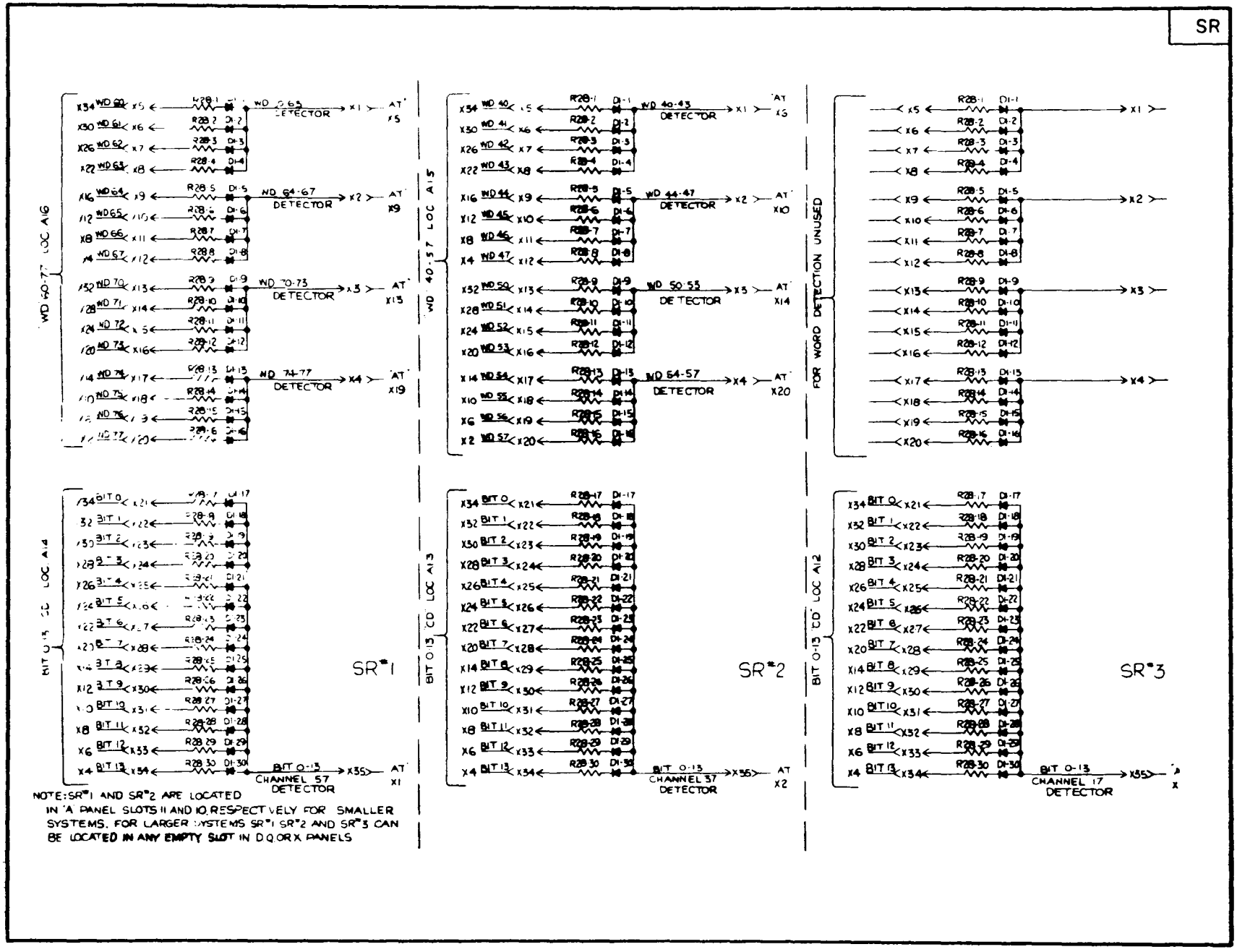


FIGURE 34. SUMMING RESISTORS LOGIC (REF. DWG. 867C995)

TELETYPE "CX" TAPE READER SYSTEM

I. GENERAL DESCRIPTION

The Teletype "CX" Tape Reader is used as a high speed tape input device that provides outputs corresponding to the intelligence recorded on fully perforated or chadless tape. The system operates asynchronously at rates up to 60 characters per second. The system contains a Teletype "CX" tape reader, an interface assembly, a channel buffer module (2RB3) and associated cables.

A block diagram of the reader system is shown in Figure 1. Table 1 indicates the actual terminations referenced in Figure 1.

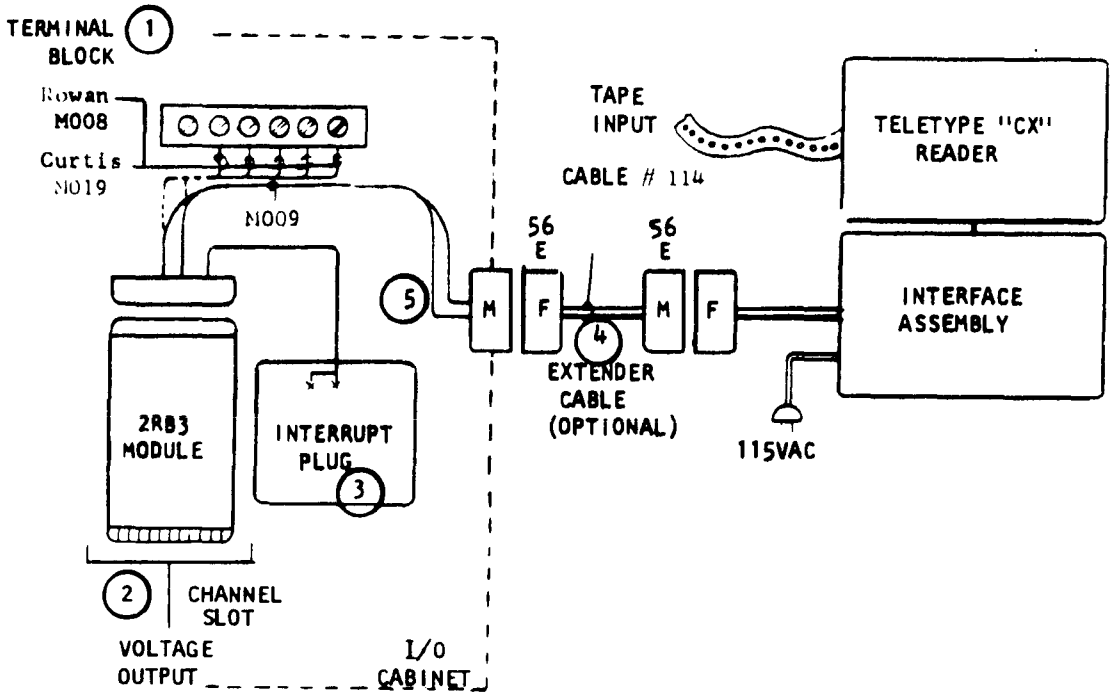


Figure 1

(1) Terminal block type and placement is optional

(2) Channel Slot is optional

(3) Interrupt assignment is optional

(4) Extender cable is optional

(5) Quick disconnect cable is optional

CARD EDGE	35 Pin Elco	I/O Processor Termination		Extension Cable	CX Tape Reader Interface
MNEMONIC	35E	CURTIS ROWAN	56E		56E
Bit 13	X22	K1	A		A
Bit 12	X23	K2	B		B
Bit 11	X24	K3	C		C
Bit 10	X25	K4	D		D
Bit 9	X26	K5	E		E
Bit 8	X27	K6	F		F
Bit 7	X28	K7	H		H
Bit 6	X29	K8	J		J
Read Adv.	X11	K10	T		T
CLR Reg.	X12	not used			
-28V Ext.	X20	K12	V		V
U Contact	X2	K16	Z		Z
+28V	X9	K13	W		W

Table 1

II. SPECIFICATIONS

A. Mechanical Specifications

1. An outline drawing of the Tape Reader Interface Package is shown in drawing 794C807.

2. All signal cables between the interface package and buffer card should use AWG #18 stranded wire. A signal distribution panel is available for screwdown type terminations which will accomodate all standard sizes up to AWG #16 wire.

3. The reader may be located at distances up to 1000 feet from the computer. A three foot pigtail cable is provided at the interface package so that the extension cable may be connected.

B. Environmental Specifications - Tape Reader

1. Temperature 50^{o} to 85^{o}F

2. Humidity 20 to 80% Relative

3. The Teletype CX Tape Reader should be checked visually every two weeks to insure that the code contacts are clean and the unit is properly lubricated. See section 5.1 in the Teletype CX Manual Bulletin 267B for detailed lubrication instructions.

C. Power Requirements - CX Tape Reader

Voltage - 115V AC ±10% single phase
Frequency - 60 cps ± 0.75%
Power Consumption - 75 watts
Input Current - Starting - 4.0 amps
- Full Load - 1.25 amps

D. Reference Drawings

1. CX Tape Reader Package
   a) Outline and Assembly 794C807
   b) Schematic 794C956

2. Tape Reader Flow. Diagram 867C553

3. Cables
   a) Refer To Master Cable List for specific job.
   b) Extender Cable - M114 for use up to 1000 feet
   c) 35E to Rowan M008
   d) 35E to 56E M009
   e) 35E to Curtis M019

4. Printed Circuit Card
   a) Reader Buffer Card 743A337

III. CIRCUIT DESCRIPTION

The Teletype CX Tape Reader is an electro-mechanical device with operate magnets and a code contact mechanism complete with leaf contacts. Perforated tape is the transmission medium for the system.

Drawing 867C553 serves as an interconnection diagram for the tape reader system. In addition to the forementioned features of the tape reader, a tight-tape mechanism (Start/stop contact) and a tape-out mechanism (tape-out contact) are used to disable the operating coils and serve to inhibit reader advance when either condition occurs.

The power switch mounted on the tape reader unit has been rendered inoperative. The power switch mounted on the interface package assembly serves to distribute a-c power to the reader motor and the 28 VDC operating coils supply contained within the interface package assembly.

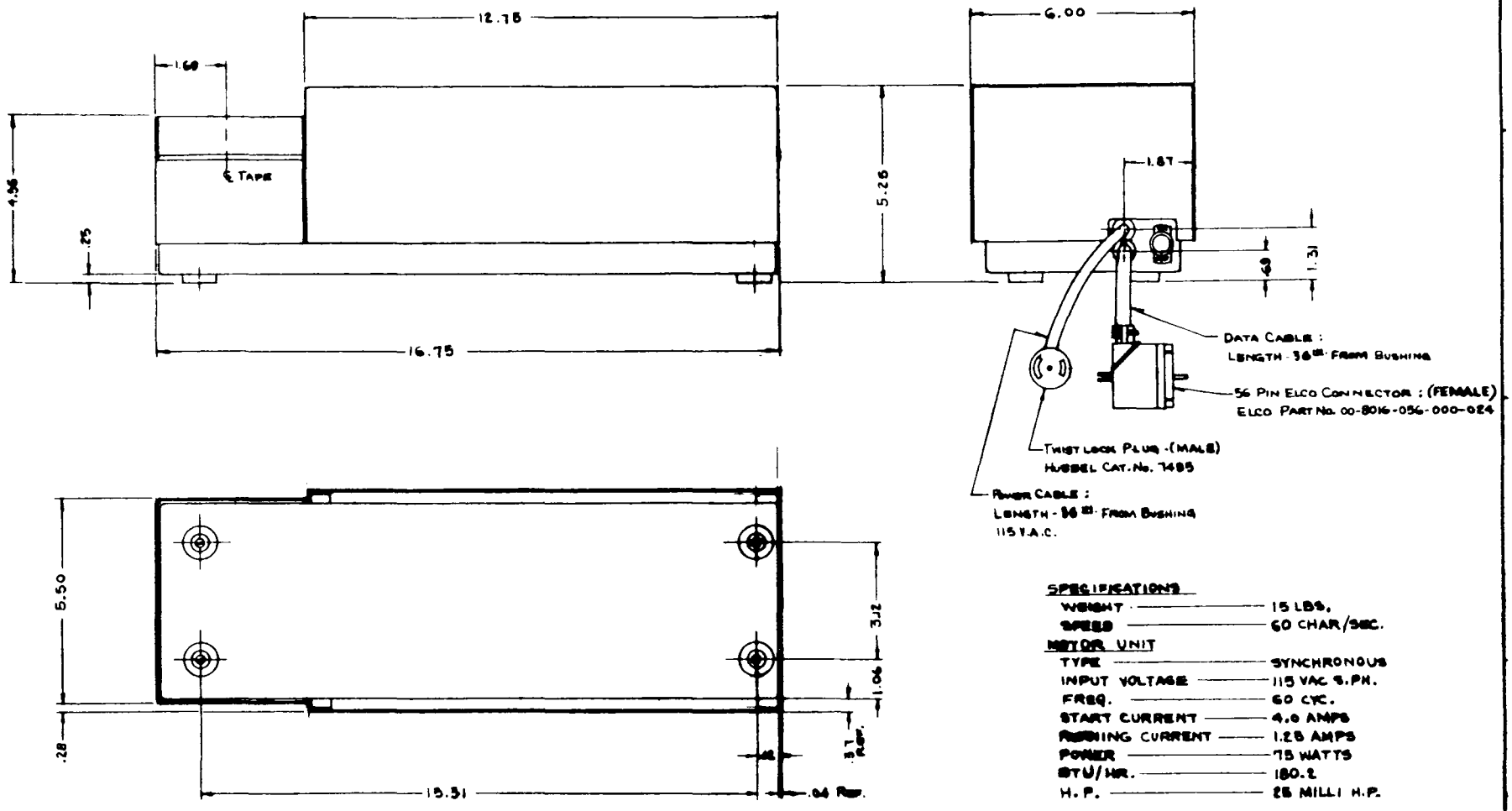
The interface package also contains a three foot pigtail cable which can be connected to an extension cable to allow the reader to operate up to 1000 feet from the computer.

The transfer of control and data signals between the interface package and the channel buffer module is described in terms of an impedance from PSC (Power Supply Common for the computer system). A signal is present means PSC is presented through a very low impedance, hereafter referred to as a logical "0". When a signal is not present ($\overline{\text{present}}$), it is presented through a high impedance, it will be referred to as a logical "1".

A. Eight Tape Level Data Signals to the buffer module. Logical "0" is present on any level when a perforation on the tape exists.

B. "U" Contact Signal to the buffer module. The "U" contact input is the "Universal" contact in the reader which closes every time a character is read. It is interpreted as a "Strobe Tape Level Data" command and a "Stop Reader Advance" command by the Reader Buffer Module.

C. Reader Advance Signal to the interface package assembly. This signal triggers the magnetic drive circuit.



SPECIFICATIONS

WEIGHT	15 LBS.
SPEED	60 CHAR/SEC.

MOTOR UNIT

TYPE	SYNCHRONOUS
INPUT VOLTAGE	115 VAC 1 PH.
FREQ.	60 CYC.
START CURRENT	4.0 AMPS
RUNNING CURRENT	1.25 AMPS
POWER	75 WATTS
BTU/HR.	180.2
H.P.	.25 MILLI H.P.

WIRING DIAGRAM # 1050226

WESTINGHOUSE ELECTRIC CORPORATION

TITLE: PRINTER "50" SERIES - TAPE READER INTERFACE PACKAGE OUTLINE

SCALE 1:2

SIZE A

194C891

COMPUTER SYSTEMS DIVISION

Three additional signals are required to complete the repertoire:

A. An Interrupt Input Signal to the I/O Interface is generated by the module in response to the "U" contact signal.

B. A Channel Read Signal (Channel half-select) must be programmed into the Central Processor as a response to the interrupt input, that is the program must read the data on a particular channel.

C. A Clear Data Register (CDR) Signal is processed within the module circuitry.

The sequence of events is described in detail in Section IV, "Printed Circuit Card Description." In general terms, the events are chronologically listed as follows:

A. Channel Read (Channel Half-Select):

1. Input Data

2. Initiate Reader Advance Signal

3. Initiate Clear Data Register

B_1 "U" Contact closes:

1. Turn Off Reader Advance Signal

2. Turn Off Clear Data Register Signal

3. Initiate Interrupt Input (Data Available)

When convenient, the Central Processor responds to Initiate Interrupt Input by initiating Channel Read, hence giving asynchronous operation. Data is interpreted as a "1" when the module data register bit output is in a positive voltage, and a "0" when the bit output is zero voltage. The eight tape levels are transmitted via the input data lines to the central processor core memory, bits 13 to 6 as shown in Figure 2.

Refer to the 2RB schematic and the Teletype Model CX Interface Schematic 794C956.

Transistor Q1 on 794C956 will conduct each time S1-1 (on the 2RB card) is turned on. This causes the operate coils in the reader to be energized, provided the start switch closed and there is tape in the reader. Each time the operate coils are energized, the reader advances and will read one character, then the "U" contacts close, which cause an interrupt and blocks SCR, S1-1, which deenergizes the operate coils. When an acknowledgment is received, S1-1 gets set, the reader will read another character.

Refer to Programmers Reference Manual for information relative to input data from external devices.

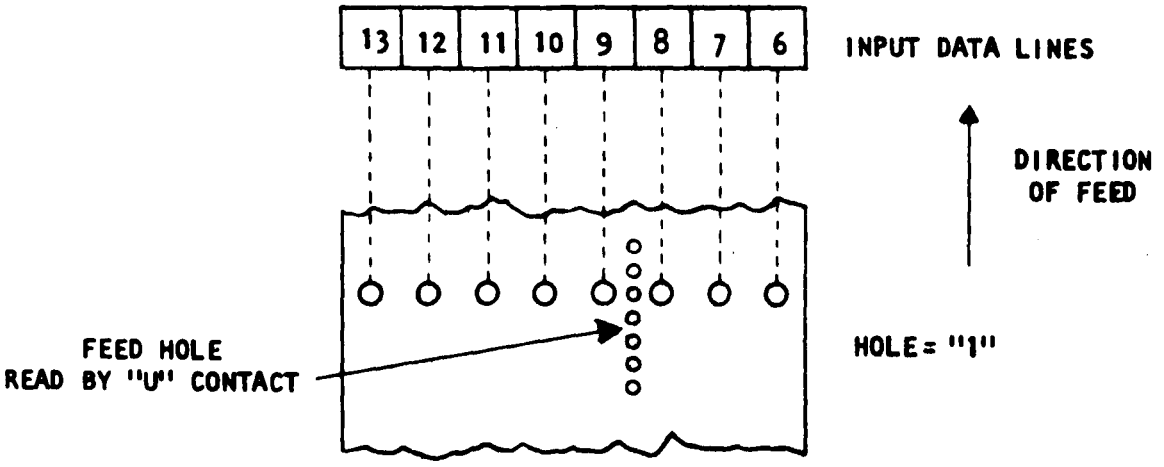
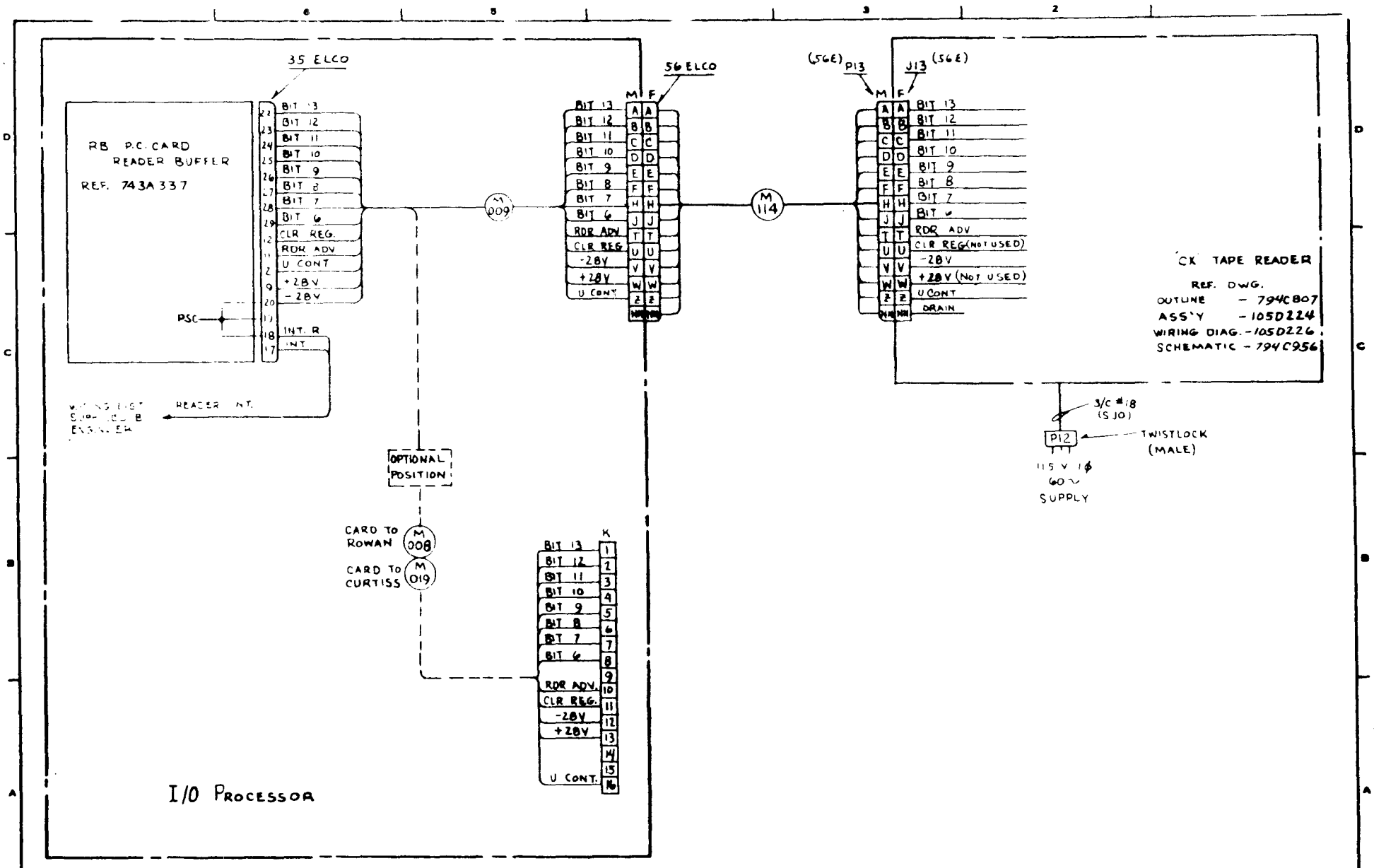

13
12
11
10
9
8
7
6
INPUT DATA LINES
DIRECTION
OF FEED
FEED HOLE
READ BY "U" CONTACT
HOLE = "1"

Figure 2



NEXT ASSY	REF. DWG.		
DO NOT SCALE DWG. BREAK ALL SHARP EDGES PER ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .010	
6 IN. to 24	± .06	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM	1 PLACE DEC.	2 PLACE DEC.	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

PRODAC SERIES

TITLE: CX TAPE READER INTERCONNECTION DIAGRAM

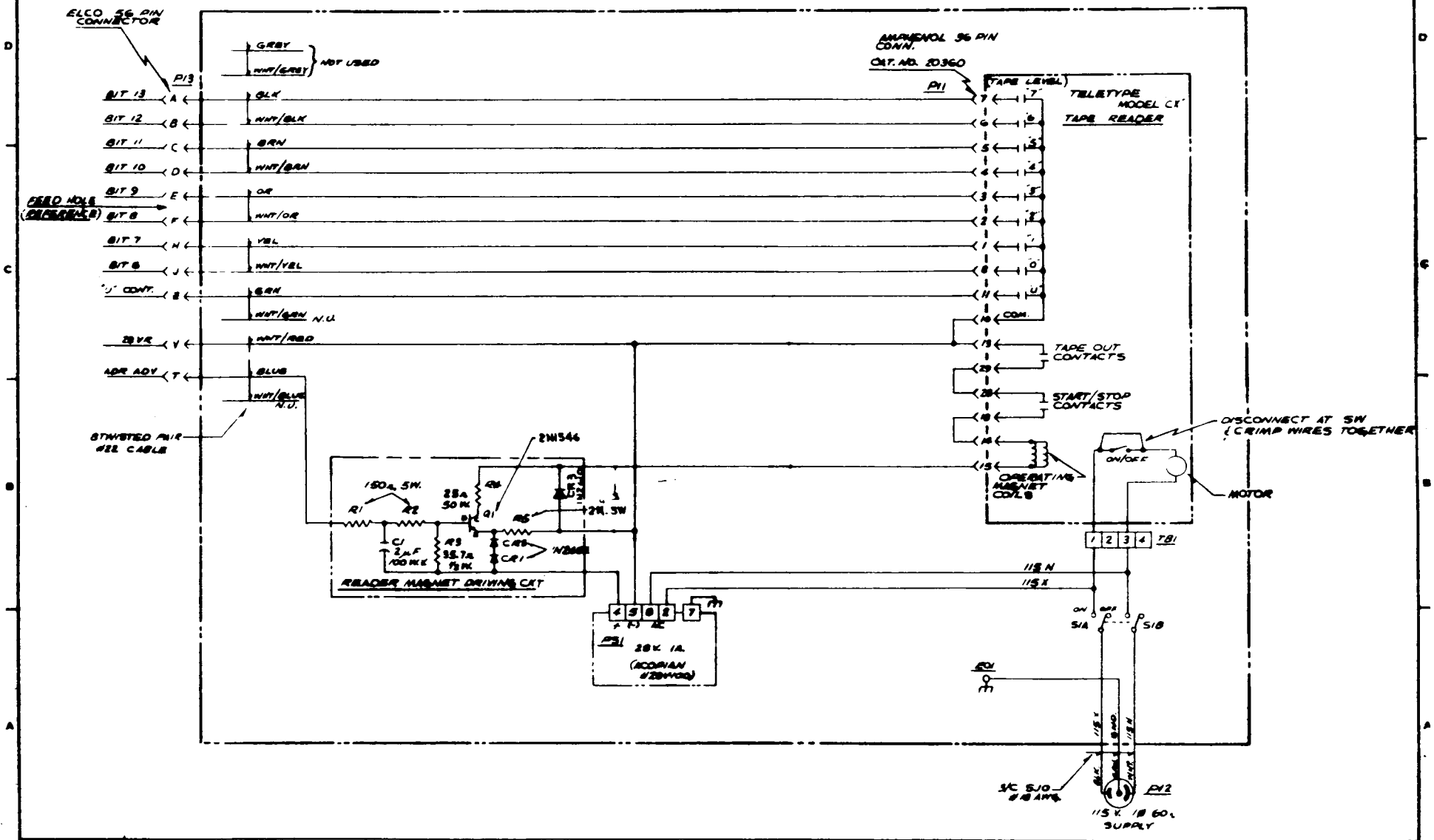
DIMENSIONS IN INCHES | SCALE | SUB. 1

DRWN | CHKD | DUPT | APPD | APPD | APPD

867C553

COMPUTER SYSTEMS DIVISION — PITTSBURGH, PA., U.S.A.

CHANGES



14-8

	WIRING	
1080824	1050256	
NEXT ASSY	REF DWG.	
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020 RADIUS UNDIMENSIONED ± 1/2°		
OVER 24	± .06	± .010
6 TO 24	± .04	± .010
UP TO 6 IN	± .02	± .005
BASIC DIM	3 PLACE DEC	4 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED		

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PROMIC 50 SERIES
TELETYPE MODEL CX INTERFACE - SCHEMATIC DWG.

SCALE

SUB. Y2

APPD K. W. Madden

794C956

COMPUTER SYSTEMS DIVISION

PITTSBURGH

CHANGE

E172 x 3

TELETYPE BRPE TAPE PUNCH SYSTEM

I. GENERAL DESCRIPTION

The Teletype BRPE Punch is used as a high speed remotely-located paper tape punch. The tape punch system consists of the Teletype BPRE type punch, an interface package including automatic motor on/off control, cables and a channel card, 1DE3. The system is capable of punching 8 level tape at speeds up to 63 characters per second. A block diagram of the tape punch system is shown in Figure 1.

II. SPECIFICATIONS

A. Mechanical Specifications

1. An outline drawing of the tape punch and interface package is shown in drawing 794C762. The tape punch may be mounted in a standard console or it may be set on a desk or table top.

2. All signal cables between interface package and I/Ø processor should use AWG #18 stranded wire. A signal distribution panel is available for screwdown type terminations which will accommodate all standard sizes up to AWG #16 stranded wire.

3. The tape punch may be located at distances up to 1000 feet from the I/Ø interface. A 3 foot pigtail cable is provided at the punch interface to which an extension cable may be connected. Table 1 indicates the actual terminations shown in Figure 1.

B. Environmental Specifications

1. Temperature - 50 to 110^{O}F

2. Humidity - 40 to 80% Relative

3. The BRPE tape punch should be lubricated at regular intervals as needed. The lubrication interval should not be more than 160 hours or one month of service, whichever occurs first. The maintenance time required is approximately 2 hours. Maintenance and lubrication instructions are found in Teletype Technical Manual - Bulletin 215B.

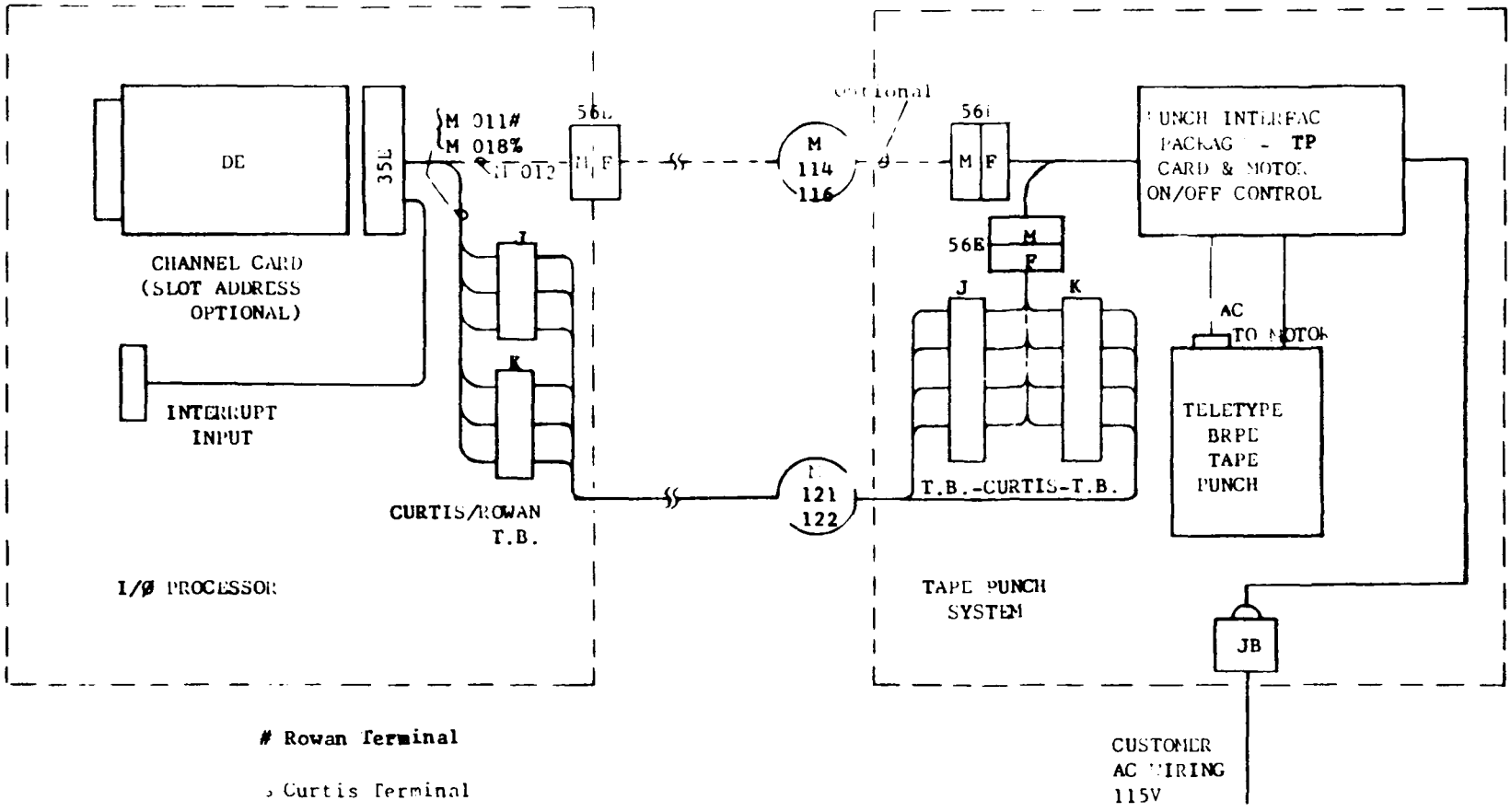
C. Power Requirements

1. Voltage 115 VAC ± 10% single phase

2. Frequency 60 cps ±.75% (50 cycle units also available)

3. Current 9 amp starting - Punch Motor
   2 amp running - Punch Motor
   2 amp (DC power supply)

D. Reference Drawings.



BLOCK DIAGRAM OF TELETYPE TAPE PUNCH SYSTEM

Figure 1

1. Teletype BRPE Punch and Interface Package

   a) Outline-Punch-794C762

   b) Schematic-105D279

2. System Cables (Refer to Table 1)

   a) 35 pin card edge to 56E - 743A498 — Ref. only*

   b) 35 pin card edge to ROWAN - 774A886 — Ref. only*

   c) 56E to 56E extension cable - 743A492 — Ref. only*

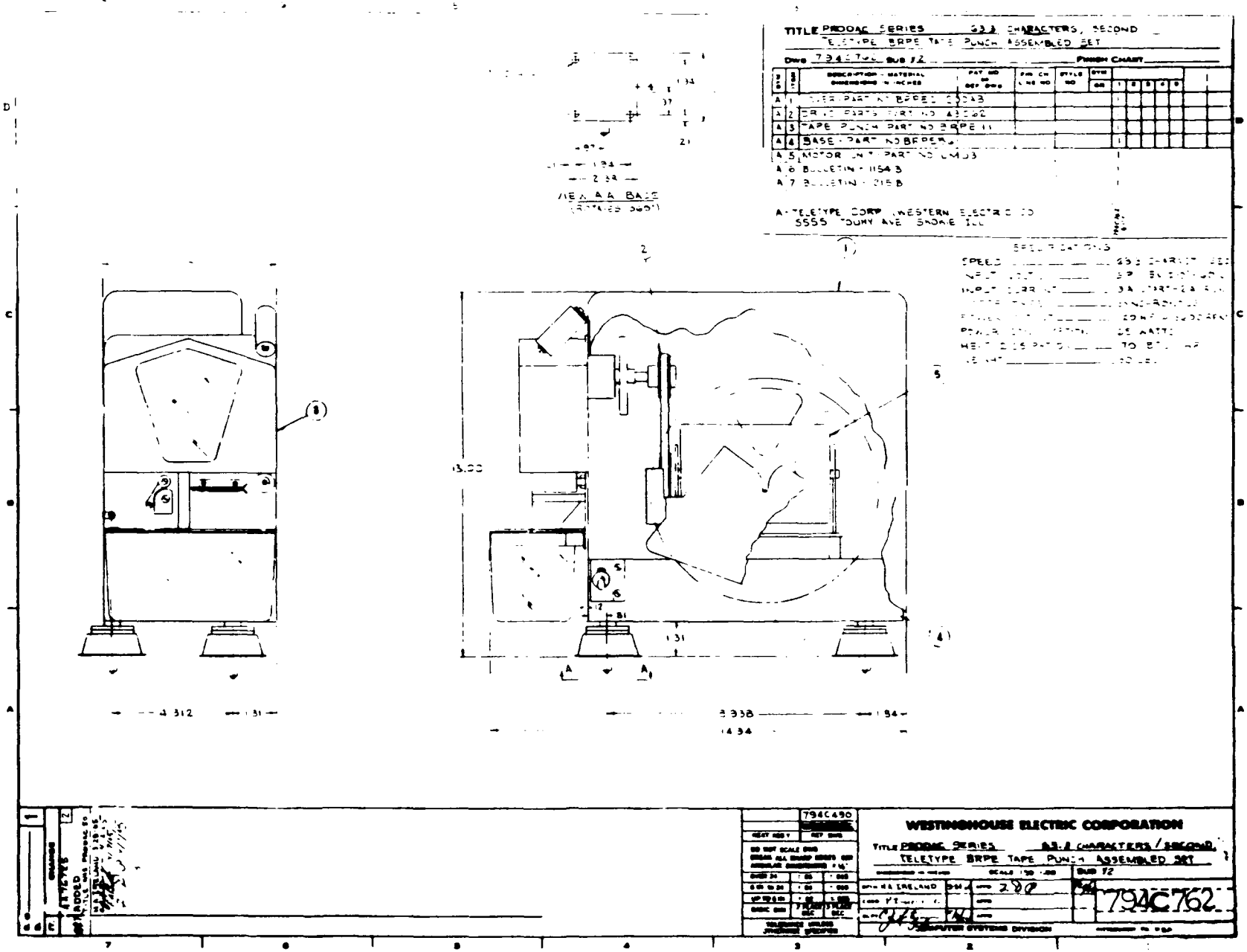
   d) 56E to 56E block extension cable — { M114 250 feet or less / M116 up to 1000 feet

   e) Curtis block to Curtis/Rowan — { M121 250 feet or less / M122 up to 1000 feet
   Note: M numbers refer to cable numbers, refer to Master Cable List for particular job.

3. Tape Punch Interconnection Diagram - 867C541

4. Tape Punch Channel Card - 743A328 (DE)
   Tape Punch Amplifier Card - 743A376 (TP)

*Table 1 is a composite listing of the information on these 3 Drawings.


TITLE PRODAC SERIES 533 CHARACTERS, SECOND
TELETYPE BRPE TAPE PUNCH ASSEMBLED SET
DWG 794C762 SUB 12
A 1 BASE PART NO BRPE1 CCAB
A 2 BRAKE PARTS PART NO A3C4C
A 3 TAPE PUNCH PART NO BRPE 11
A 4 BASE PART NO BRPE1
A 5 MOTOR UNIT PART NO LM03
A 6 BULLETIN 1154 B
A 7 BULLETIN 215 B
A TELETYPE CORP (WESTERN ELECTRIC CO)
5555 TOUHY AVE SKOKIE ILL
VIEW A A BASE
SPEED 533 CHARACTERS PER
WESTINGHOUSE ELECTRIC CORPORATION
TITLE PRODAC SERIES 533 CHARACTERS / SECOND
TELETYPE BRPE TAPE PUNCH ASSEMBLED SET
DWG 794C762
SUB 12
794C490

Card Edge	(35 Pin Elco)	I/Ø Processor Terminations		Extension Cable	Teletype Tape Punch Interface Terminations	
MNEMONIC	35E	ROWAN / CURTIS	56E		56E	CURTIS
Bit 13	X7	K1	A		A	K1
Bit 12	X8	K2	B		B	K2
Bit 11	X9	K3	C		C	K3
Bit 10	X10	K4	D		D	K4
Bit 9	X11	K5	E		E	K5
Bit 8	X12	K6	F		F	K6
Bit 7	X13	K7	H		H	K7
Bit 6	X14	K8	J		J	K8
Bit 5	X15	K9	K		K	K9
Bit 0	X16	K10	T		T	K10
		K11	U			K11
-28V Ext	X20	K12	V		V	K12
+28V Ext	X6	K13	W		W	K13
		K14	X			K14
		K15	Y			K15
Trigger	X1	K16	Z		Z	K16
-28V Ext		J1	L		L	J1
-28V Ext		J2	M		M	J2
-28V Ext		J3	N		N	J3
-28V Ext		J4	P		P	J4
-28V Ext		J5	R		R	J5
-28V Ext		J6	S		S	J6
		J7	AA			J7
		J8	BB			J8
		J9	CC			J9
		J10	DD			J10
		J11	EE			J11
		J12	FF			J12
		J13	HH			J13
		J14	JJ			J14
		J15	KK			J15
		J16	LL			J16
					NN(shield)	

Table 1

III. CIRCUIT DESCRIPTION

A. General

The Teletype BRPE tape punch requires 10 bits of information for punching tape and motor ON/OFF control. The punch motor is turned on and off under computer control to prevent excessive wear on the punch parts if the punch is inadvertently left idling.

A character on tape is made up of 8 channels corresponding to 8 bits of data and a feed hole. One bit controls the feed hole magnet which is energized for every character. Also this bit is used to turn on the punch motor and d.c. power. Another bit

of the output word is used to turn off the punch motor and d.c. power to the punch magnets. Therefore, the punch output character includes 10 bits, 8 bits of data and 2 for control.

The timing of the punch control circuitry is derived from a magnetic pickup mounted on the punch. This pickup generates a pulse indicating that the punch magnets may be energized. From this pulse, the control circuitry enables the magnet drivers for a period of 4.5 milliseconds. At the end of this period of time, the control circuitry inhibits the magnet drivers and generates an interrupt pulse which is sent to the computer asking for another character of output.

Drawing 867C541 is an inconnection diagram of the tape punch system and indicates the major components required.

The d.c. power supply located in the interface package supplies the required power for the tape punch system. The negative side of this 28 volt power supply is tied to, and common with, the negative side of the 26 volt I/Ø interface supply.

The following signals are required between the punch interface package and the channel buffer module, 1DE3.

1. Ten Data and Control signals from the buffer module to the punch interface package. Zero voltage implies the corresponding punch magnet will be energized.

2. Reset Signal from the punch interface package to the buffer module. This signal occurs each time the computer outputs a character and the magnetic pickup pulse has been generated. This pulse is used to clear the SCR buffer register and initiate an interrupt.

The following signals are required between the I/Ø interface and the buffer module.

1. An Interrupt Input Signal to the I/Ø interface indicating that the character has been punched and requests more output.

2. A Channel Output Signal addressing the selected channel and loading the SCR buffer with a data word.

   Therefore, in order to punch tape, it is necessary to address the selected channel which will load data into the SCR buffer register. The Punch motor will turn on and the corresponding magnets in the tape punch will be energized through intermediate power amplifiers; the punch will cycle; a reset pulse will reset the SCR buffer register and generate an interrupt. The computer may then output another data word at its convenience.

   The 10 bit code used with the punch is shown in Figure 2.

B. Punch Motor and Power Control

As mentioned previously, the punch may be turned ON and OFF under computer control. Both the punch motor and the d.c. power to the punch magnets are turned on and off by the computer as shown in Figure 3. A Struthers-Dunn relay (K2) is used since the switching contacts must be able to switch 9 amperes of starting current to the punch motor and carry 9 amperes of d.c. current to the punch magnets.

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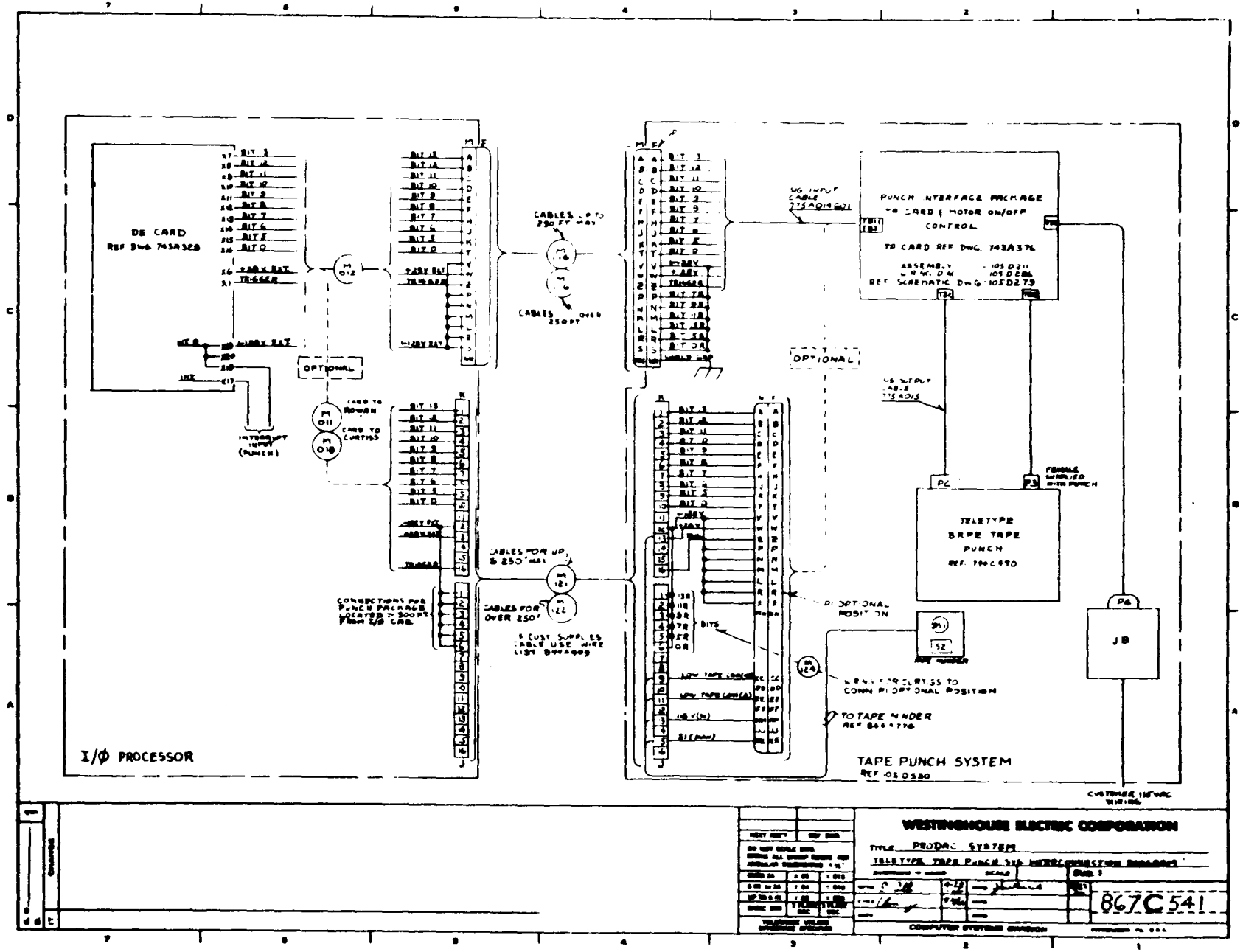
105D279


I/Φ PROCESSOR
DE CARD
REF DWG 743A328
OPTIONAL
CABLES UP TO 250 FT MAX
CABLES OVER 250FT
CABLES FOR UP TO 250' MAX
CABLES FOR OVER 250'
CONNECTIONS FOR PUNCH PACKAGE LOCATED >300 FT FROM I/O CAB.
PUNCH INTERFACE PACKAGE
TD CARD & MOTOR ON/OFF CONTROL
TD CARD REF DWG. 743A376
REF SCHEMATIC DWG 105D279
OPTIONAL
TELETYPE BRPE TAPE PUNCH
REF. 796C690
JB
TAPE PUNCH SYSTEM
REF 105D580
WESTINGHOUSE ELECTRIC CORPORATION
PRODAC SYSTEMS
867C541

735 SELECTRIC LOGGING TYPEWRITER

I. GENERAL DESCRIPTION

The IBM 735 "Selectric" typewriter is used as a logging printer in the computer system. The logger system consists of an IBM 735 printer, an interface package including automatic motor on/off control, cables, and a channel card, 1SL. The system is capable of printing alphanumerical characters at speeds up to 15 characters per second and has a maximum line width of 156 characters. A block diagram of the printer system is shown in Figure 1. Table 1 indicates the actual terminations referenced in Figure 1.

II. SPECIFICATIONS

A. Mechanical Specifications

1. An outline drawing of the printer and interface package is shown in Drawing 105D174. The printer may be mounted in a standard console or it may be set on a desk or table top.

2. All signal cables between the interface package and buffer card should use AWG #18 stranded wire. A signal distribution panel is available for screw-down type terminations which will accommodate all standard sizes up to AWG #16 wire.

3. Logging printer may be located at distances up to 1000 feet from the computer. A 3 foot pigtail cable is provided at the printer to which an extension cable may be connected.

B. Environmental Specifications

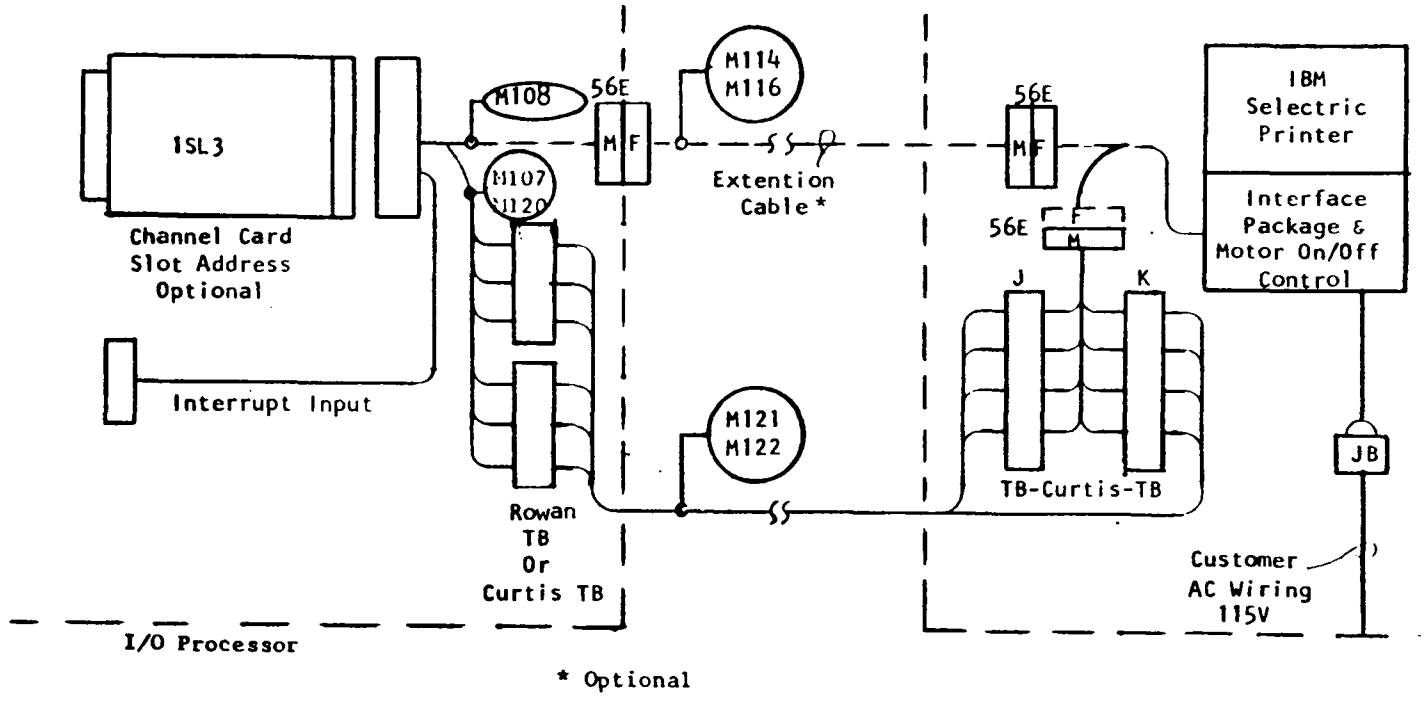
1. Temperature - 50° to 110°F

2. Humidity - 40% to 80% Relative

3. The IBM 735 logging printer is designed to operate reliably in office, warehouse, and light industrial environments. However, if unusual environmental conditions exist (excessive dust and dirt or a corrosive atmosphere) it is necessary that some protection (dust proof consoles, etc.) be provided to insure optimum reliability.

4. The printer should be checked and lubricated a minimum of once every 4 weeks. The maintenance time required is approximately one hour.

   Information on scheduled maintenance and lubrication of the 735 Selectric is contained in the "IBM Customer Engineering Universal Reference Manual, Selectric I/O Keyboard Printer" IBM Form/Part No. 241-5182-1. Also included in this manual are "Adjustment" and "Removal" Sections and the Selectric specifications, timing, etc. It should be noted that maintenance contracts are available from IBM for this equipment. Information about these contracts may be obtained from the Westinghouse Computer Systems Marketing Department.



* Optional

BLOCK DIAGRAM OF PRINTER SYSTEM
Figure 1

			I/O Processor Terminations				
Card Edge	(35 Pin Elco)		ROWAN or		Extension	IBM 735 Selectric Interface Terminations	
MNEMONIC	35E		CURTIS	56E	Cable	56E	CURTIS
Bit 13	X13		K1	A		A	K1
Bit 12	X12		K2	B		B	K2
Bit 11	X11		K3	C		C	K3
Bit 10	X10		K4	D		D	K4
Bit 9	X9		K5	E		E	K5
Bit 8	X7		K6	F		F	K6
Bit 7	X6		K7	H		H	K7
Bit 6	X5		K8	J		J	K8
Bit 5	X4		K9	K		K	K9
Bit 4	X3		K10	T		T	K10
Bit 3	X2		K11	U		U	K11
PSC(-28V)	X20	*	K12	* V		V	K12
+28V	X1		K13	W		W	K13
Reset	X14		K14	X		X	K14
TAB	-		K15	Y		Y	K15
TAB(RET.)	-		K16	Z		Z	K16
-28V	-		J1	L		L	J1
-28V	-		J2	M		M	J2
-28V	-		J3	N		N	J3
-28V	-		J4	P		P	J4
-28V	-		J5	R		R	J5
-28V	-		J6	S		S	J6
Keyb'd Lock	-		J7	AA		AA	J7
Keyb'd Lock (R)			J8	BB		BB	J8
Color Shift	-		J9	CC		CC	J9
Color Shift (R)			J10	DD		DD	J10
Back Space	-		J11	EE		EE	J11
Back Space (R)			J12	FF		FF	J12
Index	-		J13	HH		HH	J13
Index (R)			J14	JJ		JJ	J14
			J15	KK	SPARE	KK	J15
			J16	LL		LL	J16

PRINTER OPTIONS AVAILABLE TO CCO SPECIAL FOR EACH JOB.

*Additional returns when printer is 1000 ft. from I/O Processor

Table 1

C. Power Requirements - (735 Typewriter)

Voltage - 115 VAC ± 10% single phase

Frequency - 60 cps ± 0.75% (50 cps units also available)

Input current - 3 amps maximum

D. Reference Drawings

1. IBM 735 Selectric Interface Package
   a) Outline and Assembly - 105D174
   b) Schematic - 794C951

2. Device Distribution Panel Power and Signal Connections
   a) Assembly - 844A443
   b) Signal Cable (56E to Curtis TB) - 844A444

3. I/Ø Device "extension cable" - Master Cable List
   M114 - 56E to 56E
   M121 - Rowan to Curtis
   } The Selectric is less than 250 feet from I/Ø Interface and no options required.

   M116 - 56E to 56E
   M122 - Rowan to Curtis
   } The Selectric is greater than 250 feet and less than 1000 feet from I/Ø Interface or special options are required.

4. I/Ø Cabinet Wiring (Cables)
   a) Card edge to panel connector (56E) - M108 - Master Cable List
   b) Card edge to Rowan block - M107
   c) Card edge to Curtis block - M120

5. Selectric Card - 1SL3 - 743A341

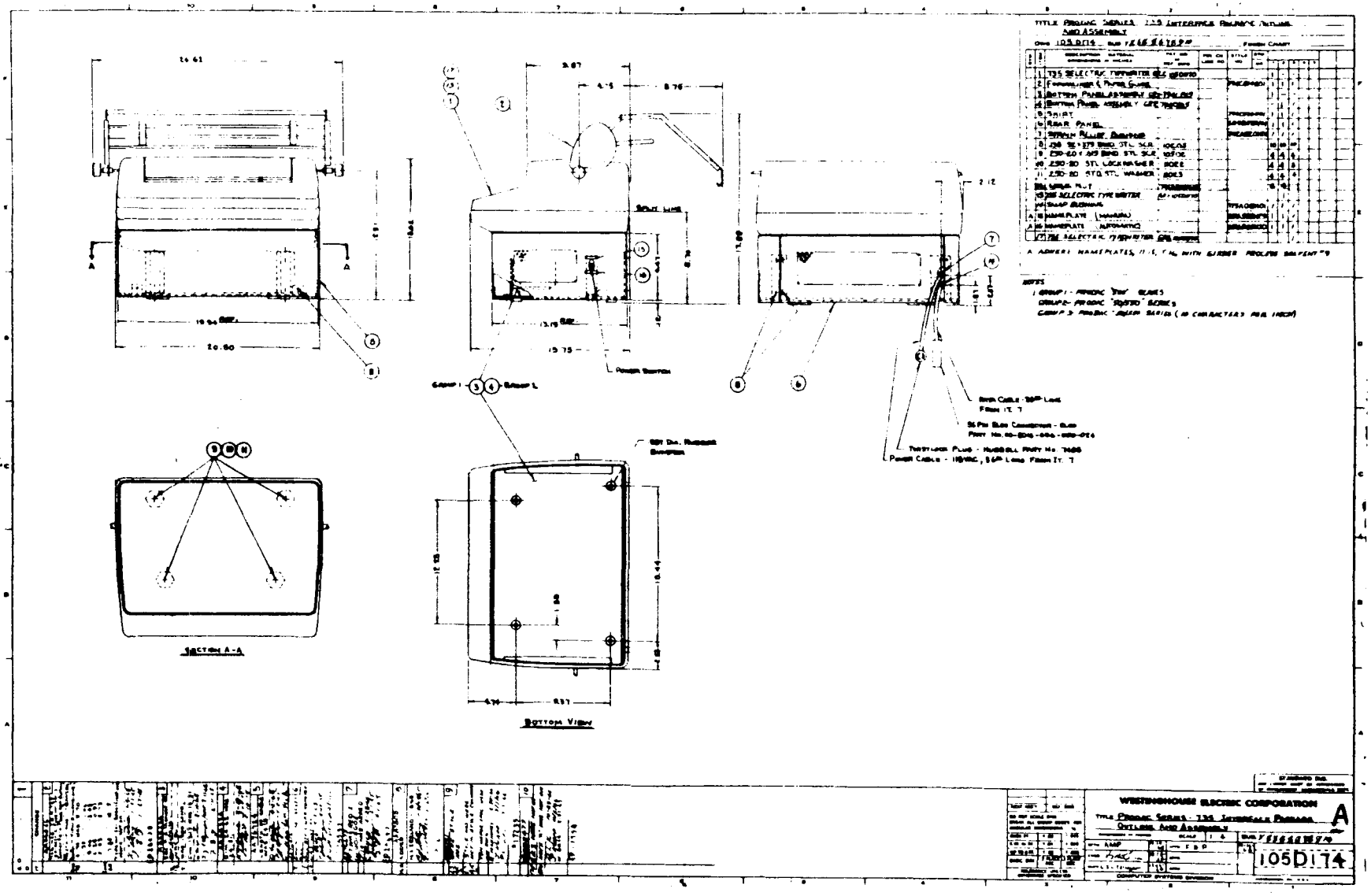
III. CIRCUIT DESCRIPTION

The IBM 735 Selectric printer requires an eleven bit code in order to print, space, shift, and carriage return. Seven of the bits are used for printing alphanumeric characters while the other four bits are used for function control. Each of the bits has an associated magnet which when energized will cause the printer to cycle. When the machine cycles, certain control contacts in the printer close, indicating the operation has been completed.

Drawing 867C505 is a complete flow diagram of the printer system and indicates the major components required.

The motor on-off switch mounted on the printer has been disconnected and replaced by one which places the printer in the off-line mode so that the motor is running but the computer cannot output to the printer. This mode of operation is covered in the Motor On-Off Control section.

The D.C. power supply located in the interface package supplies the required power for the printer system. The negative side of this 28 volt supply is tied to and common with the negative side of the 26 volt computer power supply.


WESTINGHOUSE ELECTRIC CORPORATION
105D174
A
SECTION A-A
BOTTOM VIEW

The following signals are required between the interface package and the buffer module.

1. Eleven Data Signals from the buffer module, zero voltage implies the corresponding magnet will be energized.

2. Reset Signal from the interface package to the buffer module. This signal occurs every time the printer cycles and is used to reset the buffer register.

The following signals are required between the computer I/O Interface and the buffer module.

1. An Interrupt Input signal to the I/O Interface indicating the function has been completed and requesting more output.

2. A Channel Output signal addressing the selected channel for loading the buffer with a data word.

Therefore, in order to output to the printer, it is necessary to address the selected channel which loads data into the buffer register (1SL3). The corresponding magnets in the printer will be energized; the printer will cycle; a reset signal will reset the buffer and generate an interrupt and the computer may output another data word at its convenience.

The eleven bit code required to print alphanumeric information is shown in Table 2.

MOTOR ON/OFF CONTROL

The Selectric motor will turn on when the computer outputs a character to the logging printer. As long as the computer continues to log or print data, the motor will remain on. If the computer stops outputting characters, the motor will turn off after a period of approximately 3 to 4 seconds.

The a.c. voltage to the printer motor is controlled by relay K1 contacts as shown in Drawing 867C505. Outputting any character as found in Table 2 will cause this relay to be energized and the printer motor will turn on.

The switch S1 is used to pick relay K1 if it is desired to operate the printer in the off-line mode. One pole of the switch is in series with the d.c. supply, so that when the printer is in the "MAN" mode the computer may not print on the logger. It is therefore necessary to place the switch S1 in the "AUTO" condition so that the computer has complete control of turning the printer on and off.

When the printer is not being used by the computer, K1 relay is de-energized and the 5000 μf capacitor, C3, will charge up through normally closed contacts (pins 5 and 6) and the 20 ohm resistor to the positive side of the power supply. When K1 is picked, the relay contacts transfer the charged capacitor to the relay coil. As long as the computer continues to output to the printer, K1 will remain energized and the capacitor will remain charged.

When the computer discontinues outputting to the printer, the capacitor will discharge through relay K1. The relay will remain energized until the capacitor voltage drops below the holding voltage for the relay. This is approximately 3 seconds. When the relay drops out, the capacitor will be recharged through the 20-ohm resistor.

In order for the computer to have complete control of the printer motor, it is necessary to bypass the ON/OFF switch mounted on the Selectric. This is done by disconnecting wires at the switch and crimping them together.

Another modification which is required for the Selectric is to disable the "Shift-Up Lock" on the keyboard. This must be done since it is possible to lock the shift mechanically at the keyboard. It may damage the printer "shift-up" solenoid since a completion signal will not be given when a shift-up command is given and therefore the shift-up magnet will remain energized.

OPTIONS

Several options are available and are indicated in Table 1. These include Tab, Keyboard Lock, Color Shift, Index and Back Space. The control of these options must be done using standard contact closure outputs. There is no standard feedback for these options; therefore they must receive their control through programming.

These options are brought back to the computer through the standard Selectric cables; however, the wiring to the CCO unit must be taken care of for each specific system.

Both Color Shift and Keyboard Lock require level-type signals, while Index, Back Space and Tab require a pulse for a single actuation of the magnet. Note that when these functions are performed, an interrupt from the 1SL3 card will occur. This can be used to open the CCO which initiated the function. There will be no interrupt for Color Shift and Keyboard Lock.

INTERFACE POWER SUPPLY

The power supply used in the interface package is an unregulated plug-in power supply which fits into a standard 8 pin octal socket.

The nominal output voltage of this supply is 40 volts.

This power supply is identified as PS1 on 867C505.

Table 2 shows the code required for the IBM 735 Printer

PRINT FUNCTION	Bit* 13	12	11	10	9	8
A	0	1	1	0	0	1
B	1	0	0	0	0	0
C	1	0	1	0	0	1
D	1	0	1	1	0	1
E	1	0	1	1	0	0
F	0	0	1	0	1	1
G	0	0	1	1	1	1
H	1	0	0	1	0	0
I	0	1	1	0	0	0
J	0	0	1	1	1	0
K	1	0	1	0	0	0
L	1	0	0	1	0	1
M	0	1	1	1	1	1
N	1	0	1	0	1	0
O	0	1	0	1	0	1
P	0	0	1	1	0	0
Q	0	0	1	0	0	0
R	0	1	1	1	0	1
S	0	1	0	0	0	1
T	1	0	1	1	1	0
U	1	0	1	0	1	1
V	0	1	1	0	1	1
W	0	1	0	0	0	0
X	1	0	1	1	1	1
Y	0	0	0	1	0	0
Z	1	1	1	1	1	0
1 ±	1	1	1	1	1	1
2 @	1	1	1	0	1	0
3 #	1	1	1	0	1	1
4 $	1	1	0	1	0	1
5 %	1	1	1	1	0	0
6 ¢	1	1	1	0	0	0
7 &	1	1	1	1	0	1
8 *	1	1	1	0	0	1
9 (	1	1	0	0	0	0
0)	1	1	0	1	0	0
= +	0	0	1	0	1	0
! °	0	1	1	1	1	0
/ ?	0	0	0	1	0	1
. .	0	1	1	0	1	0
, ,	0	0	1	0	0	1
' "	0	1	1	1	0	0
; :	0	0	1	1	0	1

Space "1" in Bit 6

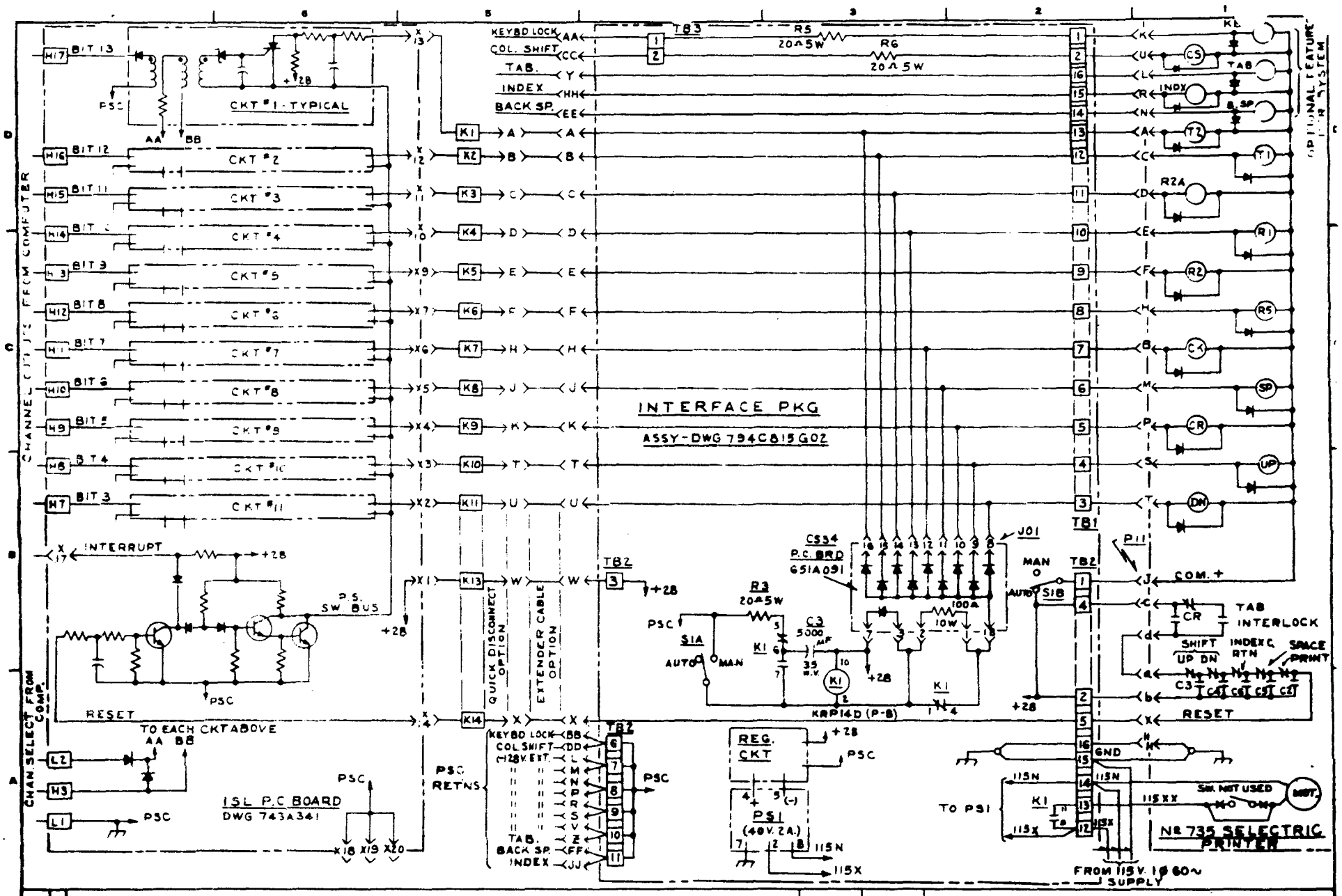
Carr. Ret. "1" in Bit 5

Shift up "1" in Bit 4

Shift down "1" in Bit 3

*When Bit 7 is a "1", the machine prints a dash (-).

Table 2



NEXT ASS'Y	REF. DWG.		
DO NOT SCALE DWG. BREAK ALL SHARP EDGES .005R. ANGULAR DIMENSIONS ± ½°			
OVER 24	± .06	± .015	
6 IN. to 24	± .04	± .010	
UP TO 6 IN.	± .02	± .005	
BASIC DIM	2 PLACES DEC.	3 PLACES DEC.	
TOLERANCE UNLESS OTHERWISE SPECIFIED			

WESTINGHOUSE ELECTRIC CORPORATION

PRODAC 50 SERIES - 735 SELECTRIC

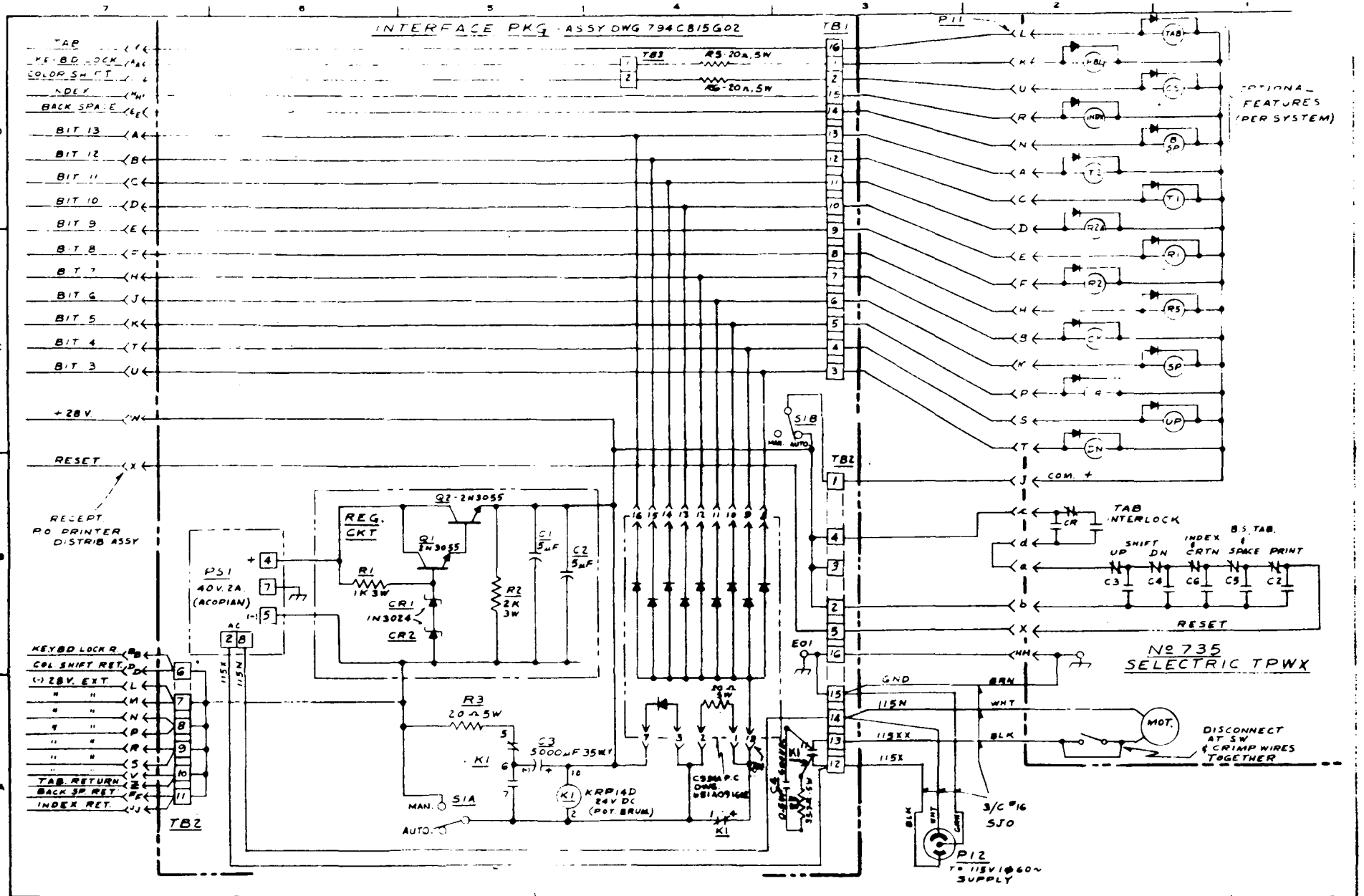
TITLE: SYSTEM DIAGRAM - DATA REG./CONTROL/INTERFACE

SCALE: NONE | SHEET 1

APPD R.J.M. & Wagner

867C505

COMPUTER SYSTEMS DIVISION



16-10

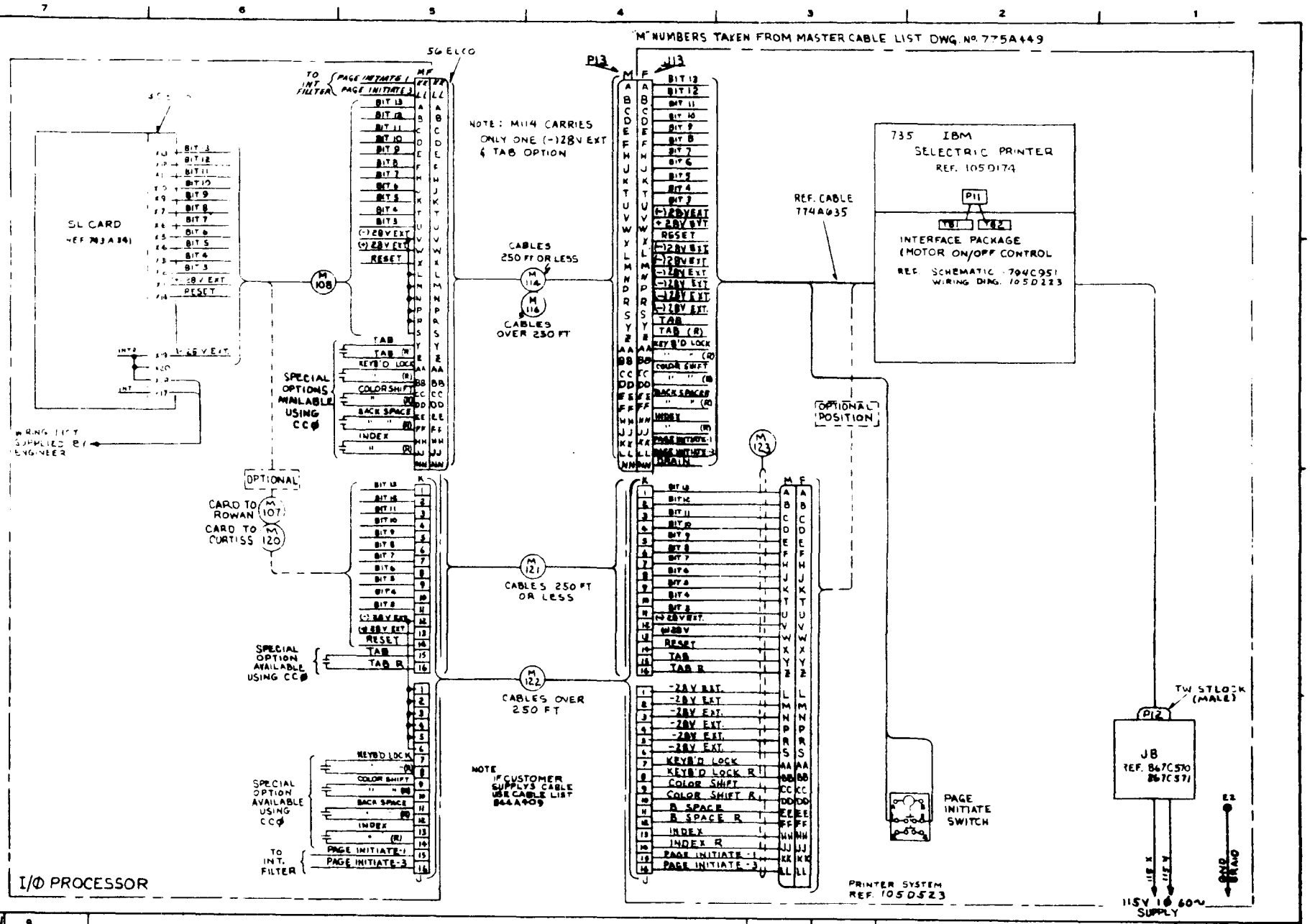
794C815G02	WIRING 105D223	
NEXT ASSY	REF DWG	

DO NOT SCALE DWG
BREAK ALL SHARP EDGES .020
ANGULAR DIMENSIONS ± ½°

OVER 24	± .06	± .015
6 IN to 24	± .04	± .010
UP TO 6 IN	± .02	± .005
BASIC DIM	2 PLACE DEC	3 PLACE DEC

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION
PRODAC 50 SERIES
A
TITLE 735 SELECTRIC INTERFACE - SCHEMATIC DIAGRAM
DIMENSIONS IN INCHES SCALE NONE SUB Z1815G
DRTN J. Hess 7/6/65
CHKD 7/6/65
APPD
794C951
COMPUTER SYSTEMS DIVISION PITTSBURGH PA U.S.A.



16-11

1	CHANGE		
2	AA85924 PAGE INITIATE WAS AVAILABLE WITH HALF SHELL ONLY, (B)+ ADDED TO J13 IS STANDARD NOW ALL FUNCTIONS		

NEXT ASS'Y	REF DWG

DO NOT SCALE DWG. BREAK ALL SHARP EDGES .020 ANGULAR DIMENSIONS ± ½°

OVER 24	± .06	± .015
6 IN. to 24	± .04	± .010
UP TO 6 IN.	± .02	± .005
BASIC DIM	2 PLACE DEC	3 PLACE DEC

TOLERANCE UNLESS OTHERWISE SPECIFIED

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC SYSTEM
SELECTRIC PRINTER CONSOLE INTERCONNECTION DIAG.

DIMENSIONS IN INCHES — SCALE — SUB. #2

DRN [illegible] — APPD [illegible] — 3

CHKD [illegible] — 5/3/66 — APPD

SUPV — APPD

867C569

COMPUTER SYSTEMS DIVISION — PITTSBURGH, PA. U.S.A.

DFTM. CHKD. SUPV. APPD. APPD. APPD. S.O. D. A47839

I.T. No. 8 & 10 HAVE BEEN DEL

3 | AA96102 | ITO WAS 32 IN GR.1

I.T.G WAS NO CANCELLED

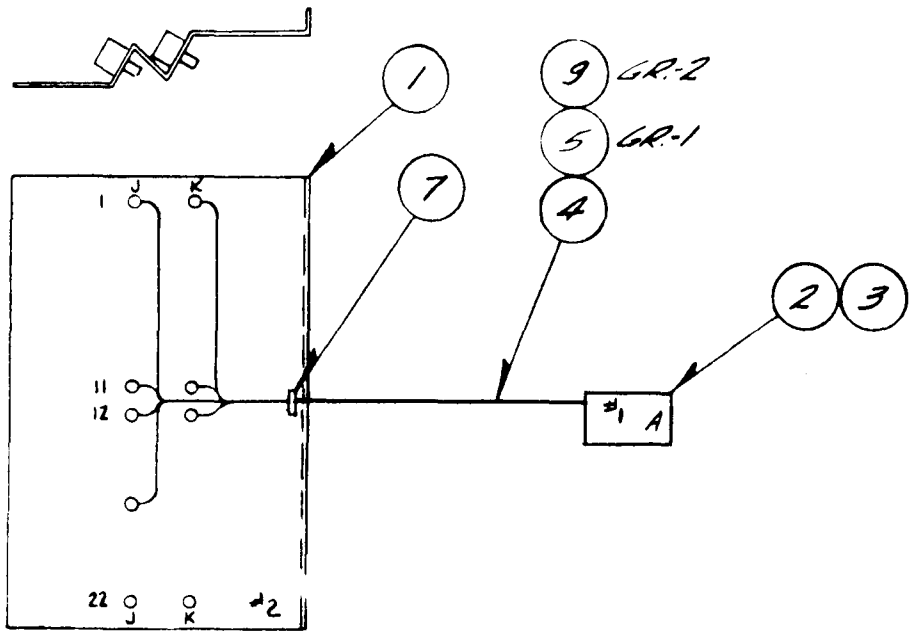
R.B.J 2-9-

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC SERIES
DEVICE CABLE HDWR. ASS'Y.

DWG. 844A444 SUB. X23 FINISH CHART

1	TERM. BLK. MTG. BRKT. GR-1	844A443			1	1
2	CONNECTOR (MALE HOODED)			742A967H05	1	1
3	PIN CONTACT			742A966H01	32	32
4	TAPER PIN			775A276H02	30	32
5	CABLE, 60" OF 16PR-22 AWG	743A059			1	
~~6~~	~~CABLE, 60" OF 2/C-18 AWG~~	~~770A665~~			~~1~~	
7	CABLE TIE			742A828H01	1	
8	WIRE LIST	844A437	SH. 1 & 2	-	1	1
9	CABLE, 12" OF 16PR-22 AWG	743A059				1
~~10~~	~~WIRE LIST~~	~~844A437~~	~~SH 1~~			~~1~~



844A444

DFTM.	CHKD.	SUPV.	APPD.	APPD.	APPD.	S.O. D.
2/9/64	[illegible]	[illegible] 2-19				

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC SERIES
TERM. BLK. MTG. BRKT. SUB ASS'Y.

DWG. 844A443 SUB. 1 FINISH CHART

SYM.	ITEM	DESCRIPTION — MATERIAL DIMENSIONS IN INCHES	PATT. NO. OR REF. DWG.	FIN. CH. LINE NO.	STYLE NO.	SYM. GR.	1	2	3	4	5		
	1	TERM. BLK. MTG. BRKT.			7AAC965H01		1						
	2	TERM. BLK.			7122A949H11		4						
	3	PUSH ON NUT			7A2A812H03		8						
	4	MARKING STRIP			6108114H01		1						

NOTES;

1- IT.-3 TO BE INSTALLED ON END TERMINALS OF IT.-2

2- ASSEMBLE IT.-4 TO IT.-1 AS SHOWN USING GIRDER PROCESS SOLVENT #9 FROM GIRDER PROCESS, HACKENSACK, N.J.

3- RUBBER STAMP IT.-1 AS SHOWN WITH .12 HIGH BLACK CHARACTERS PER FS 184K. COVER WITH CLEAR LACQUER FS 224Q

NEXT ASS'Y	REF. DWG.

DO NOT SCALE DWG.
BREAK ALL SHARP EDGES .02R
ANGULAR DIMENSIONS ±½°

OVER 24	±.06	±.015
6 IN. to 24	±.04	±.010
UP TO 6 IN.	±.02	±.005
BASIC DIM.	2 PLACE DEC.	3 PLACE DEC.

TOLERANCE UNLESS OTHERWISE SPECIFIED

SH-1 OF 2 SHEETS

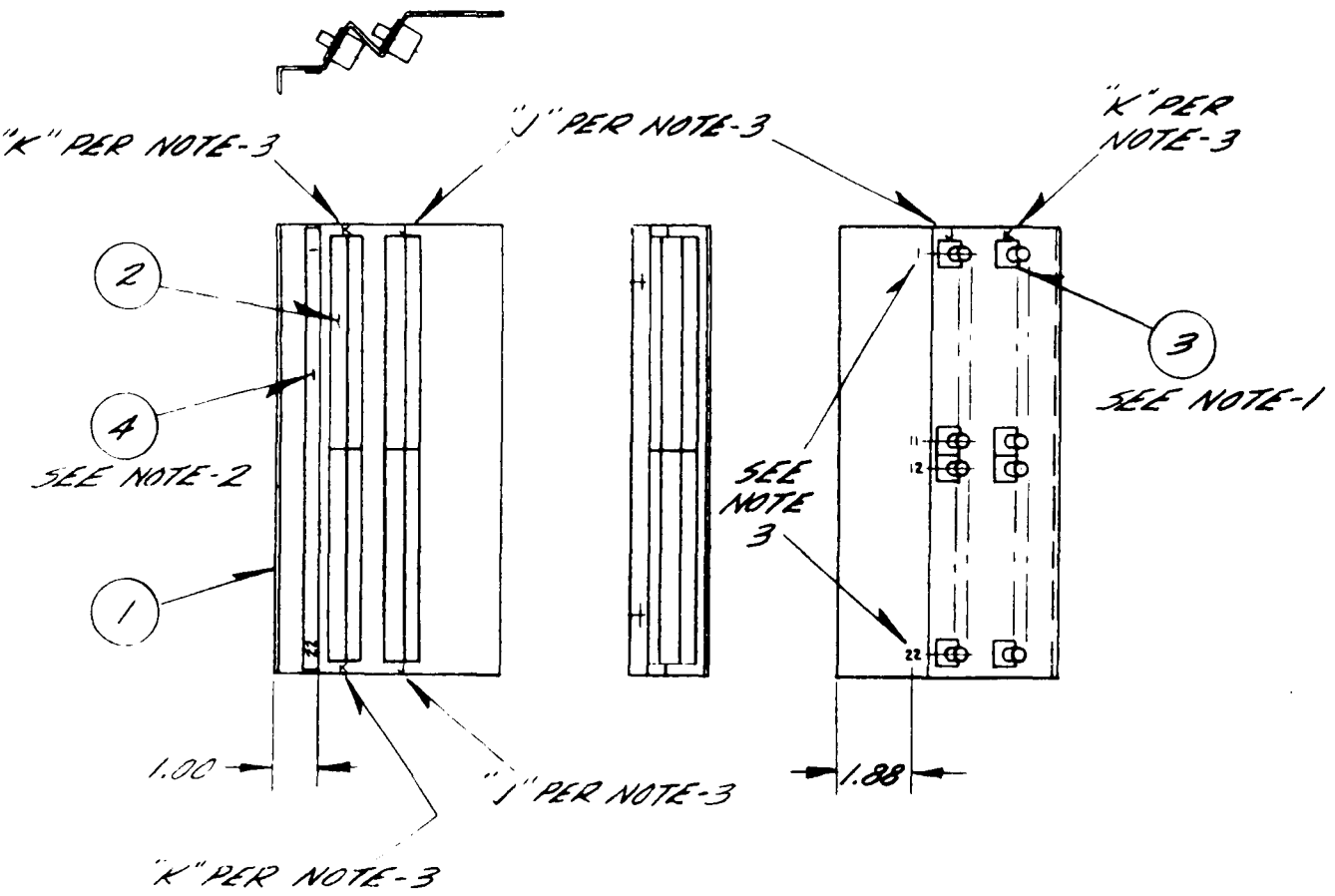
844A443

DFTM.	CHKD.	SUPV.	APPD.	APPD.	APPD.	S.O. D.

WESTINGHOUSE ELECTRIC CORPORATION COMPUTER SYSTEMS DIVISION PITTSBURGH, PA., U.S.A.

TITLE PRODAC SERIES
TERM. BLK. MTG. BRKT. SUB ASS'Y.

DWG. 844A443 SUB. 1 FINISH CHART



SH. 2 OF 2 SHEETS 844A443

TELETYPE MODEL 35 INPUT/OUTPUT SYSTEM

I. GENERAL DESCRIPTION

The Teletype Model 35 equipment is used as a low speed Input/Output to the I/Ø processor. The equipment uses the "American Standard Code for Information Interchange" and operates at a speed of 10 characters per second. When used for Input/Output the equipment may be a Model 35 ASR (punch, reader, keyboard and printer) or a Model 35 KSR (keyboard and printer). An Output only, the Model 35 RO is also available (printer only). The Model 35 Input/Output System is shown in Figure 1, and consists of the Model 35 (ASR, KSR, RO), an Interface package with automatic motor ON/OFF control, cables, and 3 channel cards. (2TN1, 4TO1, 3TS1) The 2 TN1 channel card is not required when the Model 35 RO is used.

II. SPECIFICATIONS

A. Mechanical Specifications

1. An outline drawing of the Model 35 ASR is shown in Drawing 105D369. Drawing 105D371 is an outline drawing of the Model 35 KSR and RO. The interface package and motor ON/OFF control is mounted in the stand of the equipment.

2. All signal cables between interface package and I/Ø processor should use at least AWG #22 stranded wire. A signal distribution panel is available for screwdown type terminations which will accommodate all standard sizes up to AWG #16 stranded wire.

3. The Model 35 equipment may be located up to 1 mile from the I/Ø processor using standard extension cables. However since this equipment is compatible with Dataphone and standard TWX, its location is effectively unlimited. A 3 foot pigtail cable is provided at the interface to which an extension cable may be connected. Table 1 indicates the actual terminations shown in Figure 1.

B. Environmental Specifications

1. Temperature - 50^{o} to 110^{o} F.

2. Humidity - 40% to 80% Relative

3. The Model 35 equipment should be lubricated at regular intervals as needed. The lubrication interval should not be more than 1500 hours or 6 months whichever occurs first. The maintenance time required is approximately 3 hours. Maintenance and Lubrication instructions are found in Teletype Technical Manual 280B (ASR) and 281B (KSR and RO).

C. Power Requirements

1. Voltage - 115 Volt AC $\pm$ 10% single phase

2. Frequency - 60 $\pm$ 0.5 cycles (50 cycle equipment available)

3. Current - 3 amperes

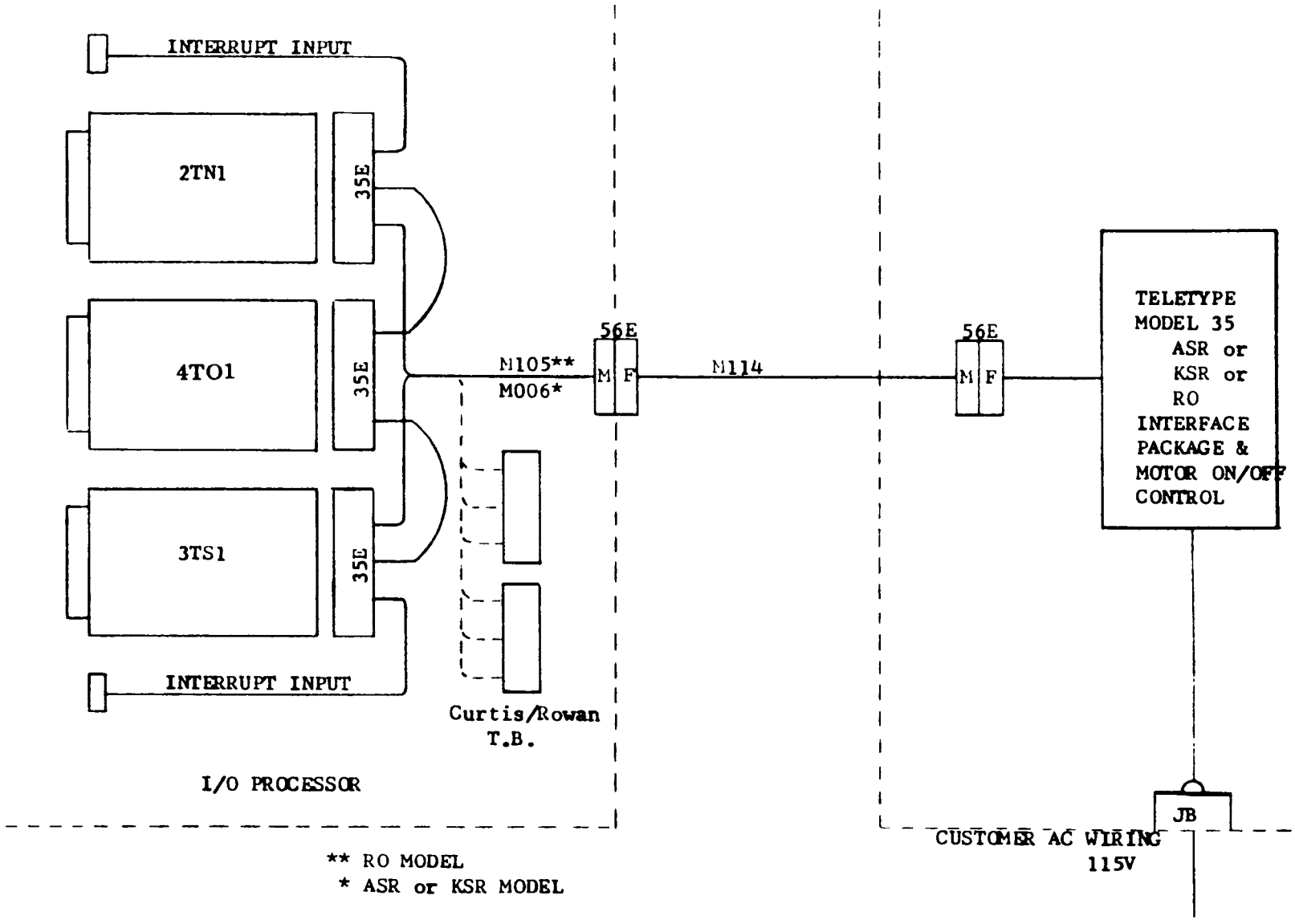
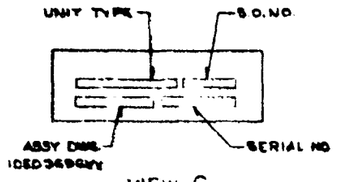
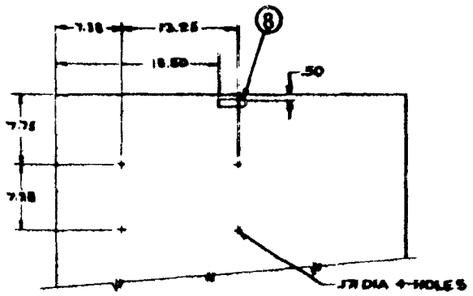

INTERRUPT INPUT
2TN1
35E
4TO1
35E
3TS1
35E
INTERRUPT INPUT
M105**
M006*
56E
M F
M114
56E
M F
TELETYPE
MODEL 35
ASR or
KSR or
RO
INTERFACE
PACKAGE &
MOTOR ON/OFF
CONTROL
Curtis/Rowan
T.B.
I/O PROCESSOR
JB
CUSTOMER AC WIRING
115V
** RO MODEL
* ASR or KSR MODEL

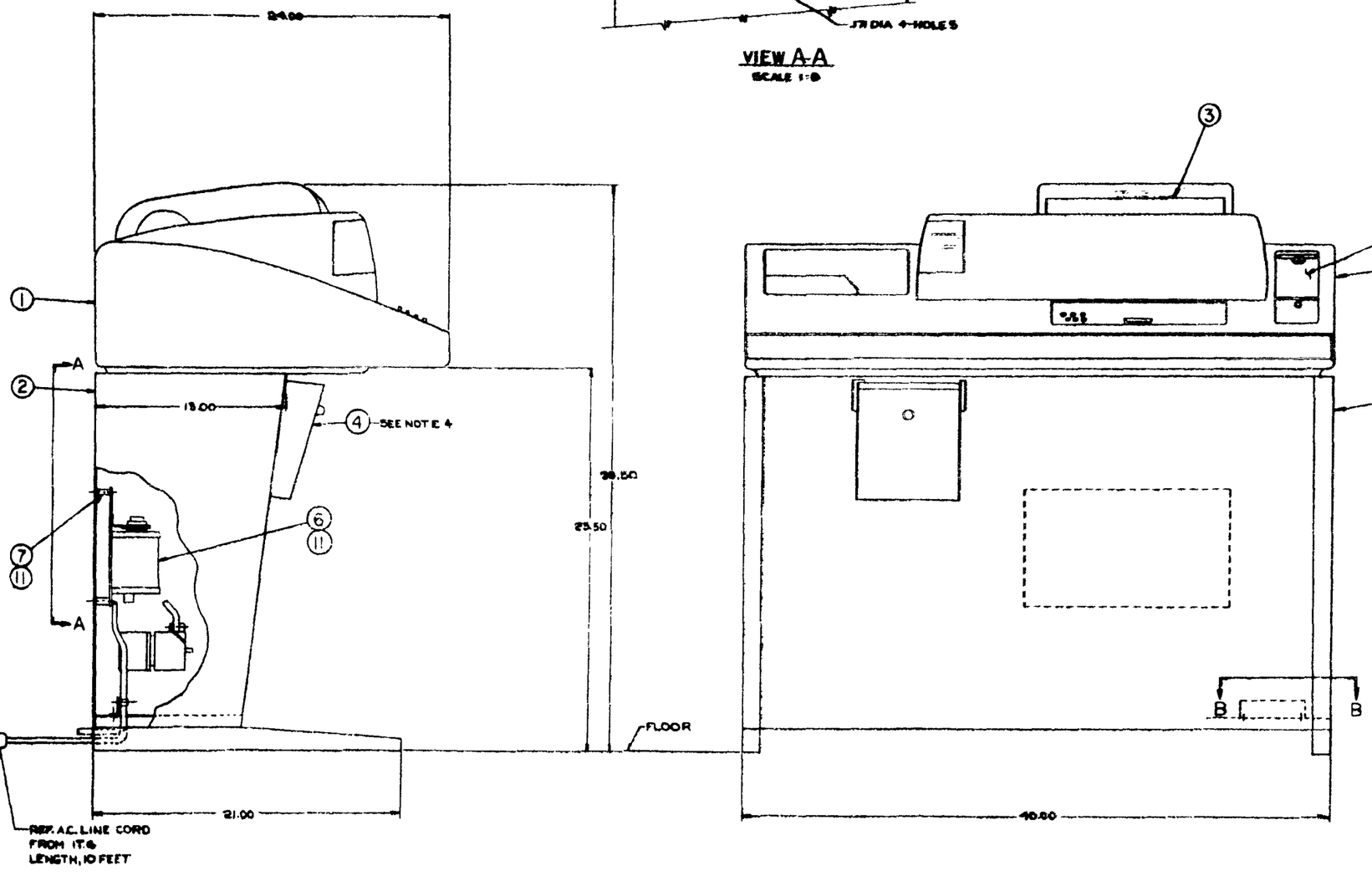
Figure 1



VIEW C
SCALE 1:1



VIEW A-A
SCALE 1:8



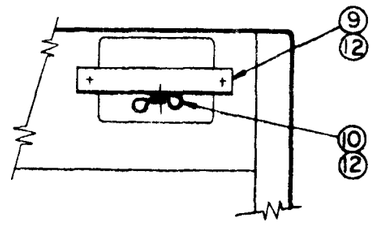
TITLE PRODAC 50
TELETYPE MODEL 35 AR OR 35 AS ASR ASSEMBLY
DWG. 105D369 SUB. 6

REV	ITEM	DESCRIPTION – MATERIAL DIMENSIONS IN INCHES	PART NO. OR REF. DWG.	FURNISHED UNDER NO.	STYLE NO.	SPEC. NO.	FINISH CHART 1	2	3	4	5
A	1	TELETYPE MODEL 35 AR ASR (SEE NOTE 1)					1				
A	2	STAND (SEE NOTE 4)					1	1			
	3	PAPER ROLL-WEST. FORM 24072				(SEE NOTE 2)	1	1			
A	4	SHAD CONTAINER (SEE NOTE 4)					1	1			
	5	ASR INTERRUPT ASSY	GR176C787				1	1			
	6	INTERFACE PANEL ASSY	GR186C704				1	1			
	7	STANDOFF			242A806H01		4	4			
	8	EQUIPMENT NAMEPLATE			451A278H02		1	1			
	9	BRACKET			175A294G01		1	1			
	10	CABLE CLAMP			242A806H05		2	2			
	11	.139-32 X .38 BIND. STL. SCR	10203				4	8			
	12	.190-32 X .50 BIND. STL. SCR	10402				3	3			
	13	WIRING DIAG	GR167C202				1	1			
	14	SCHEMATIC	105D372				1	1			
A	15	TELETYPE MODEL 35 AS ASR (SEE NOTE 1)					1	1			

A-TELETYPE CORP. 5555 TOUHY AVE., SKOKIE, ILL.

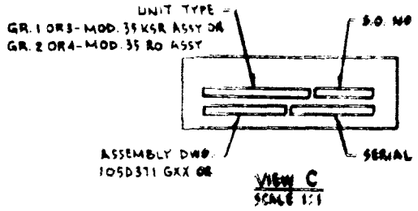
ITEM	TELETYPE	SPROCKET FEED PLATEN	FRICTION FEED PLATEN
1, 15	MODEL 35 ASR	P.D. NO. 112 MODEL 35 AS	P.D. NO. 111 MODEL 35 AR

NOTES:
1. PURCHASE ORDER FOR MODEL "35 AR OR AS ASR MUST CONTAIN THE FOLLOWING: 35 AR OR AS ASR TO BE EQUIPPED WITH ELAPSED TIME METER.
2. ITEM "3 MAY BE ORDER FROM WESTINGHOUSE PRINTING DIV. TRAFFORD, PA. FOR USE IN TELETYPE PRINTERS.
3. THE MAXIMUM PRINTING AREA FOR ITEM 1 IS 7.20 INCHES, 72 CHARACTERS ACROSS, 10 CHARACTERS TO THE INCH.
4. ITEMS 2 & 4 ARE SUPPLIED AS PART OF ITEM 1 OR ITEM 15.
5. ACCESS CLEARANCE REQUIREMENTS:
   A. BACK WALL TO ASR SET-MIN. 13 INCHES TO OPEN COVER
   B. BACK WALL TO ASR SET-MIN. 2 FT. TO REMOVE COVER

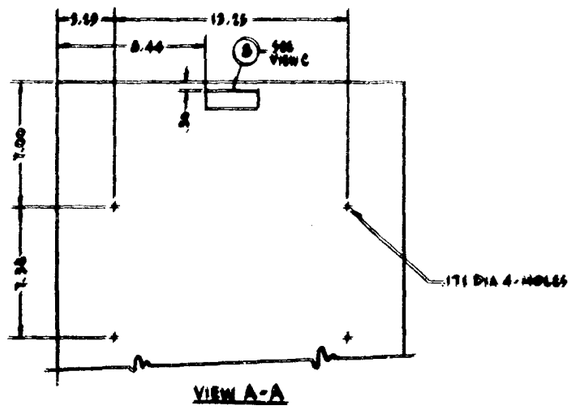


SECTION B-B
SCALE 1:2

MODEL 35 ASR ASSEMBLY
(Ref. Ⓦ Dwg. 105D369, sub 6)



VIEW C
SCALE 1:1



VIEW A-A

SPECIFICATIONS

WEIGHT	191 LBS. (INCLUDES STAND)
SPEEDS	100 W.P.M.
H.P.	.09 H.P.
STARTING CURRENT	8.0 AMPS
RUNNING CURRENT	2.0 AMPS
POWER	165 WATTS MAX.
BTU	493

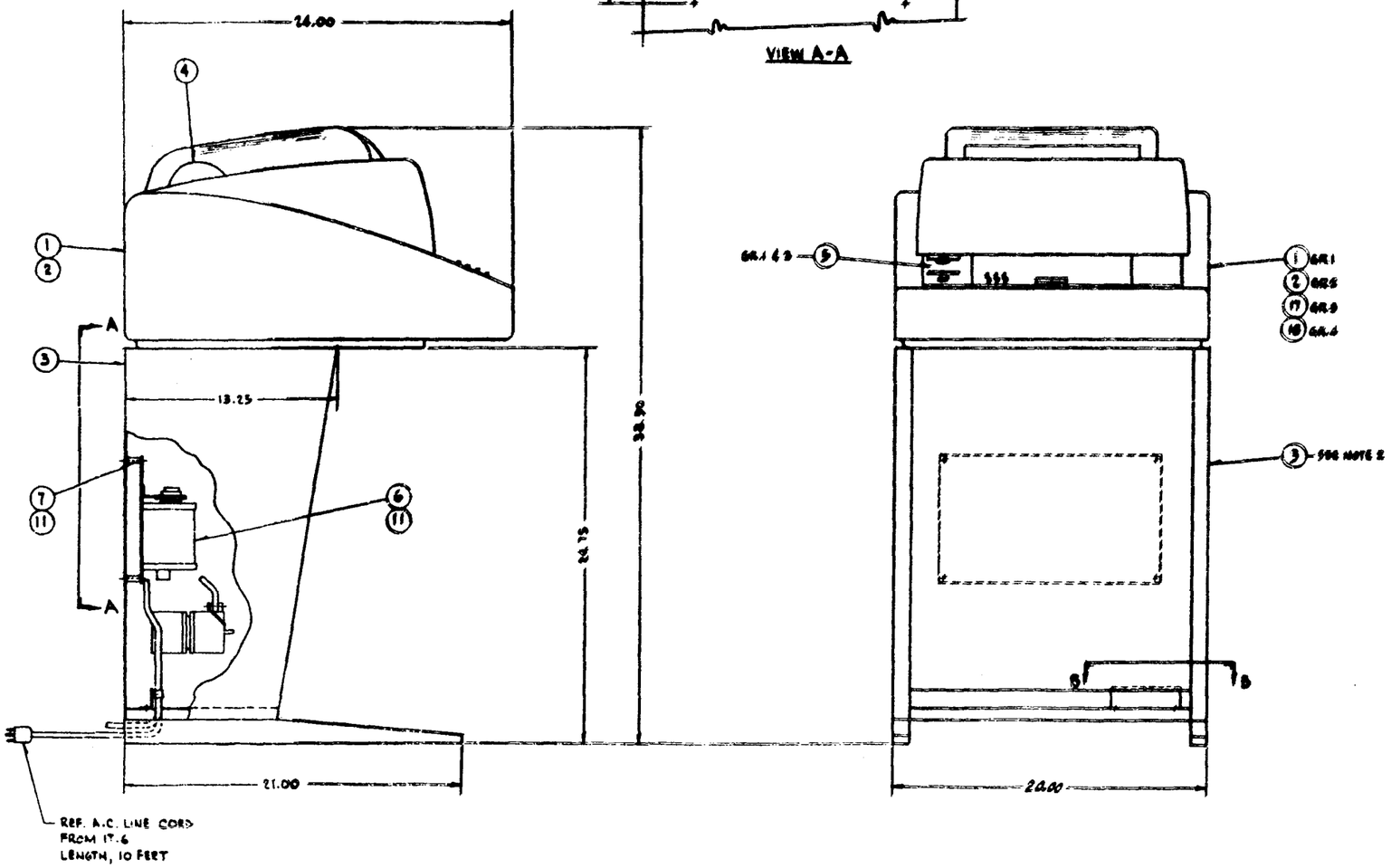
TITLE PRODAC 50
TELETYPE MODEL 35 KSR & 35 RO
DWG 105 & 371 SUB. 4 & 4

PINION CHART

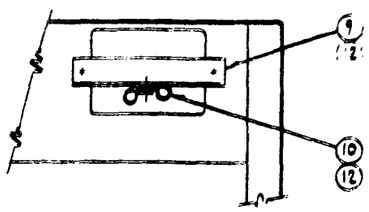
		DESCRIPTION - MATERIAL DIMENSIONS IN INCHES	PART NO OR REF DWG	FIN OR LINE NO	STYLE NO	QTY	1	2	17	18
A	1	TELETYPE - MODEL 35 KSR (SEE NOTE 1)	(8)				1			
A	2	TELETYPE - MODEL 35 AY RO	(SEE NOTE 1)					1		
A	3	STAND (SEE NOTE 2)					1	1	1	1
	4	PAPER ROLL - WEST. FORM	46072 (SEE NOTE 3)				1	1	1	1
	5	ASR INTERRUPT ASSY	[illegible]				1			
	6	INTERFACE PANEL ASSY	GR 1, 105D370				1	1	1	1
	7	STANDOFF			[illegible]	4	4	4	4	
	8	EQUIPMENT NAMEPLATE			[illegible]	1	1	1	1	
	9	BRACKET			[illegible]	1	1	1	1	
	10	CABLE CLAMP			[illegible]	2	2	2	2	
	11	.138 - 32 x .38 IND. STL. SCR.	10103			8	8	8	8	
	12	.190 - 32 x .50 IND. STL. SCR.	10401			2	2	2	2	
	13	WIRING DIAGRAM - (KSR)	867C310			1		1		
	14	WIRING DIAGRAM - (RO)	867C311				1		1	
	15	SCHEMATIC - (KSR)	105B313			1		1		
	16	SCHEMATIC - (RO)	105B314				1		1	
A	17	TELETYPE - MODEL 35 AP KSR	(SEE NOTE 1)						1	
A	18	TELETYPE - MODEL 35 AU RO	(SEE NOTE 1)							1

A - TELETYPE CORP. 5555 TOUHY AVE., SKOKIE, ILL.

	TELETYPE	SPROCKET FEED PLATEN	FRICTION FEED PLATEN
P	MODEL 35 KSR	PD 101 MODEL 35 AP	PD 101 MODEL 35
W	MODEL 35 RO	PD 102 MODEL 35 AU	PD 103 MODEL 35 AT



NOTES:
1. PURCHASE ORDER MUST SPECIFY THAT ITEMS 1, 2, 17 & 18 BE EQUIPPED WITH ELAPSED TIME METER.
2. ITEM 3 IS SUPPLIED AS PART OF ITEMS 1, 2, 17 & 18
3. ITEM 4 MAY BE ORDERED FROM WESTINGHOUSE PRINTING DIV., TRAFFORD, PA. FOR USE IN TELETYPE PRINTERS.
4. THE MAXIMUM PRINTING AREA FOR ITEMS 1 & 2 IS 7.50 INCHES, 75 CHARACTERS ACROSS, 10 CHARACTERS TO THE INCH.
5. IT CONSISTS OF LRB13 TD/ATJ TYPING UNIT AND ASSEMBLED SUB COMPONENTS VCL 312 HF.



SECTION B-B
SCALE 1:2

MODEL 35 KSR and RO ASSEMBLY
(Ref. Ⓦ Dwg. 105D371, sub 4)

	Card Edge	(35 Pin Elco)	I/Ø Processor Terminations		Extension Cable	Teletype Model 35 Interface Terminations	
			ROWAN	56E			
	MNEMONIC	35E	CURTIS			56E	CURTIS
ASR KSR	Line P(I/Ø)	TN_{X2}	K1	A		A	
	Line M	TS_{X11}	K2	B		B	
	+72V	TS_{X10}	K5	C		C	
	MOTOR ON	TS_{X3}	K6	D		D	
	+48/125V			E		E	
	CR INT			F		F	
	48R			H		H	
	ACK LAMP			J		J	
				K		K	
	125R			V		V	
	+48/125V			W		W	
	ATTN. INT			X		X	
	RD. ON { Not Used	TN_{X21}	K13	Y		Y	
	RD. ON R { on KSR }	TN_{X31}	K14	Z		Z	
RO	Line M	TS_{X11}	K2	B		B	
	+72V	TS_{X10}	K5	C		C	
	MOTOR ON	TS_{X3}	K6	D		D	
	+48/125V			E		E	
	CR INT			F		F	
	LINE P (OUTPUT)	TS_{X4}	K16	K		K	

Table 1

D. Reference Drawings

1. Model 35 Equipment and Interface

	Outline	Schematic
Model 35 ASR	105D369	105D372
Model 35 KSR	105D371	105D373
Model 35 RO	105D371	105D374

2. System Cables (Refer to Drawings 867C573, 867C574)

	Model 35 KSR,	35 ASR,	35 RO
a) 35 pin card edge to 56E	M006	M006	M105
b) 35 pin card edges to ROWAN	M005	M005	M104
c) 56E to 56E Extension	M114	M114	M114
d) 35 pin card edge to CURTIS	M004	M004	M103

3. Channel Cards

2TN1 - 743A339
4TO1 - 743A327
3TS1 - 743A342

III. CIRCUIT DESCRIPTION

A. General

To feed blank tape on the Model 35 ASR, it is necessary to depress the "control, shift, "P" and "Repeat" keys in that order. This will feed blank tape as long as the "Repeat" key is held depressed.

The mode switch on the Model 35 ASR is used to select different modes of Input/ Output when the equipment is ON-LINE.

Position "K" - The keyboard and printer are connected to the computer.

Position "KT" - The keyboard, printer, tape reader, and tape punch are connected to the computer. When the tape reader is transmitting, the message is copied by the printer and a duplicate tape is punched. The keyboard should not be operated when the tape reader is reading. When the keyboard is transmitting, the message is copied by the printer and a tape is punched.

Position "T" - The tape reader and printer are connected to the computer. The printer copies what is being transmitted by the tape reader or received from the computer. The keyboard and tape punch are left in an OFF-LINE condition and tape may be prepared locally from the keyboard while transmitting to and from the computer.

Position "TTS" - The tape reader reads binary tapes with no printing occurring. The keyboard and tape punch may be used to prepare tape without interference to the tape reader.

Position "TTR" - The tape punch is connected to the computer and may be used to punch binary tapes. The tape reader, printer and keyboard are disconnected. (This mode has no apparent use at present.)

The Model 35 KSR has no MODE switch and the keyboard and printer are always connected to the computer when the KSR set is ON-LINE.

When punching binary tapes using the programmer's console programs (BP) the operator should set the mode select switch to the KT position so that the limits of punching are not punched in the binary output tape. When the "trigger" character, return, is given, a 10 second program delay will occur to allow the operator to switch the mode select switch from KT mode to TTR mode. Binary punching will then occur. Any additional binary output requires switching to the KT mode, typing in the limits, and then switching back to the TTR mode.

Teletype Model 35 send-receive equipment uses an 8-level code (standard ASCII code) as shown in Table 2. An additional two bits of data are required for turning the motor on and off under computer control so that the total output character is made up of 10 bits while input data is 8 bits. Current on the line is defined to be 60 milliamperes for marking and 0 milliamperes for spacing. In addition to the intelligence portion of the code, control is required; since transmission is serial, a "start" and "stop" pulse must be generated. The start pulse precedes the first intelligence pulse of each character and is always a spacing pulse (open line), while the stop pulse follows the last intelligence pulse and is always a marking pulse (current in line).

The "start" pulse has the same duration as each of the character pulses, while the "stop" pulse has a duration of twice that of the others. If each character pulse is given a unit time duration, the total time required to transmit any character is 11.0 units. A transmission rate of 10 characters per second requires a rate of 110 units per second. Therefore, one unit of time is equal to 9.09 milliseconds. This is the basic unit of time for the Teletype serial transmission equipment.

The above general description indicates how a two wire teletype transmission system operates. In order to be compatible, so as to transmit serial data, it is necessary to open and close the line at the required rate. In order to receive serial data it is necessary to monitor the line, sychronized with the start pulse, and detect when there is current and when there is no current. This is done by using a mercury relay contact for output and a mercury relay coil for input, both of these being in series with the line as shown in Figure 2.

B. Information Transfer

Figure 2 indicates in block diagram form, the major components which make up the control of data transfer between the I/O interface and the Model 35 equipment. These components make up the 3 channel cards mounted in the I/O interface; 4TO1, 3TS1, and 2TN1 cards.

In order to provide the necessary timing required by the Model 35 equipment, a five-stage counter is used. This counter is stepped along by alternate pulses, P1 and P2. The timing of this counter is shown in Figure 3. P1 and P2 pulses are derived from a unijunction oscillator circuit and are timed to occur alternatively every 9.09 milliseconds, the basic unit of time of the 35 equipment. The five-stage counter can give 10 different states. These are shown in Figure 3. Note that state E·A is equivalent to the "start" for the 35 equipment. The eight succeeding states

Character	Level					Feedhole				Octal
	8	7	6	5	4		3	2	1	
@	1	1								300
A		1							1	101
B		1						1		102
C	1	1						1	1	303
D		1					1			104
E	1	1					1		1	305
F	1	1					1	1		306
G		1					1	1	1	107
H		1			1					110
I	1	1			1				1	311
J	1	1			1			1		312
K		1			1			1	1	113
L	1	1			1		1			314
M		1			1		1		1	115
N		1			1		1	1		116
O	1	1			1		1	1	1	317
P		1		1						120
Q	1	1		1					1	321
R	1	1		1				1		322
S		1		1				1	1	123
T	1	1		1			1			324
U		1		1			1		1	125
V		1		1			1	1		126
W	1	1		1			1	1	1	327
X	1	1		1	1					330
Y		1		1	1				1	131
Z		1		1	1			1		132
[	1	1		1	1			1	1	333
\		1		1	1		1			134
]	1	1		1	1		1		1	335
↑	1	1		1	1		1	1		336
←		1		1	1		1	1	1	137
SPACE	1		1							240
!			1						1	041
"			1					1		042
#	1		1					1	1	243
$			1				1			044
%	1		1				1		1	245
&	1		1				1	1		246
'			1				1	1	1	047
(			1		1					050
)	1		1		1				1	251

Character	Level					Feedhole				Octal
	8	7	6	5	4		3	2	1	
*	1		1		1			1		252
+			1		1			1	1	053
,	1		1		1		1			254
-			1		1		1		1	055
.			1		1		1	1		056
/	1		1		1		1	1	1	257
Ø			1	1						060
1	1		1	1					1	261
2	1		1	1				1		262
3			1	1				1	1	063
4	1		1	1			1			264
5			1	1			1		1	065
6			1	1			1	1		066
7	1		1	1			1	1	1	267
8	1		1	1	1					270
9			1	1	1				1	071
:			1	1	1			1		072
;	1		1	1	1			1	1	273
			1	1	1		1			074
=	1		1	1	1		1		1	275
·	1		1	1	1		1	1		276
?			1	1	1		1	1	1	077
EOT	1						1			204
WRU							1		1	005
RU							1	1		006
BELL	1						1	1	1	207
TAB					1				1	011
LINE					1			1		012
FEED										
VT	1				1			1	1	213
FORM					1		1			014
RETURN	1				1		1		1	215
X ON				1					1	021
TAPE				1				1		022
X OFF	1			1				1	1	223
TAPE				1			1			024
ACK	1	1	1	1	1		1			374
ALT		1	1	1	1		1		1	175
MODE										
RUB	1	1	1	1	1		1	1	1	377
OUT										

ASCII TELETYPE CODE
Table 2

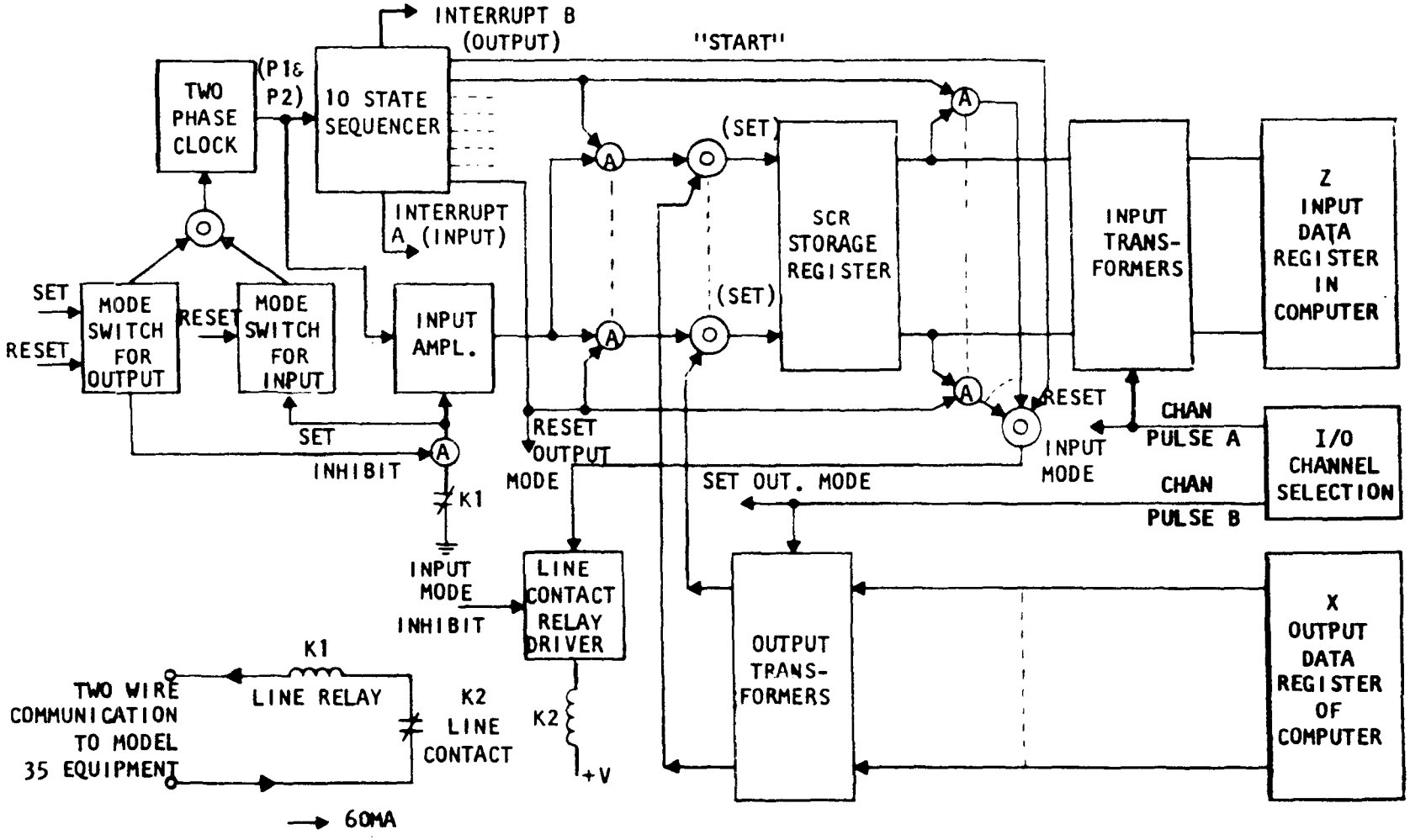

INTERRUPT B
(OUTPUT)
"START"
TWO PHASE CLOCK
(P1& P2)
10 STATE SEQUENCER
INTERRUPT A (INPUT)
SET
RESET
MODE SWITCH FOR OUTPUT
RESET
MODE SWITCH FOR INPUT
INPUT AMPL.
SET
INHIBIT
K1
INPUT MODE
INHIBIT
LINE CONTACT RELAY DRIVER
K1
TWO WIRE COMMUNICATION TO MODEL 35 EQUIPMENT
LINE RELAY
K2 LINE CONTACT
K2
+V
60MA
(SET)
(SET)
SCR STORAGE REGISTER
RESET OUTPUT MODE
RESET INPUT MODE
SET OUT. MODE
INPUT TRANS-FORMERS
Z INPUT DATA REGISTER IN COMPUTER
CHAN PULSE A
CHAN PULSE B
I/O CHANNEL SELECTION
OUTPUT TRANS-FORMERS
X OUTPUT DATA REGISTER OF COMPUTER

Figure 2

represent the 8 bits of data for the Model 35 code. "Stop" is represented by state $D \cdot \overline{E}$ of the sequencer and at this time an 18.18 millisecond delay is generated since "stop" is twice as long as the other states. This sequencer is used to serialize data during output and also for sequentially storing the serial data during input.

Figure 4 shows generally how data is transferred between the Model 35 equipment and the control logic. An SCR is used to buffer each of the eight bits which make up the 35 code. Each SCR may be set from the computer using the I/O processor data outputs and addressing the channel or it may be set as a result of inputting data from the Model 35 reader or keyboard.

As shown in Figure 4 the "line" is closed to the 35 equipment and may be opened by opening the K1 contacts (output) or by opening it within the 35 equipment (input), either by striking a key on the keyboard or by reading a character from tape.

1. Output Mode

   To output a character it is necessary to start the sequencer. This will happen when a character is loaded into the eight bit SCR buffer from the computer. The sequencer is reset to step $E \cdot A$ and a start pulse is given which occurs as a result of K1 relay being energized. Note that a "start" pulse will occur with every character that is loaded into the register during output.

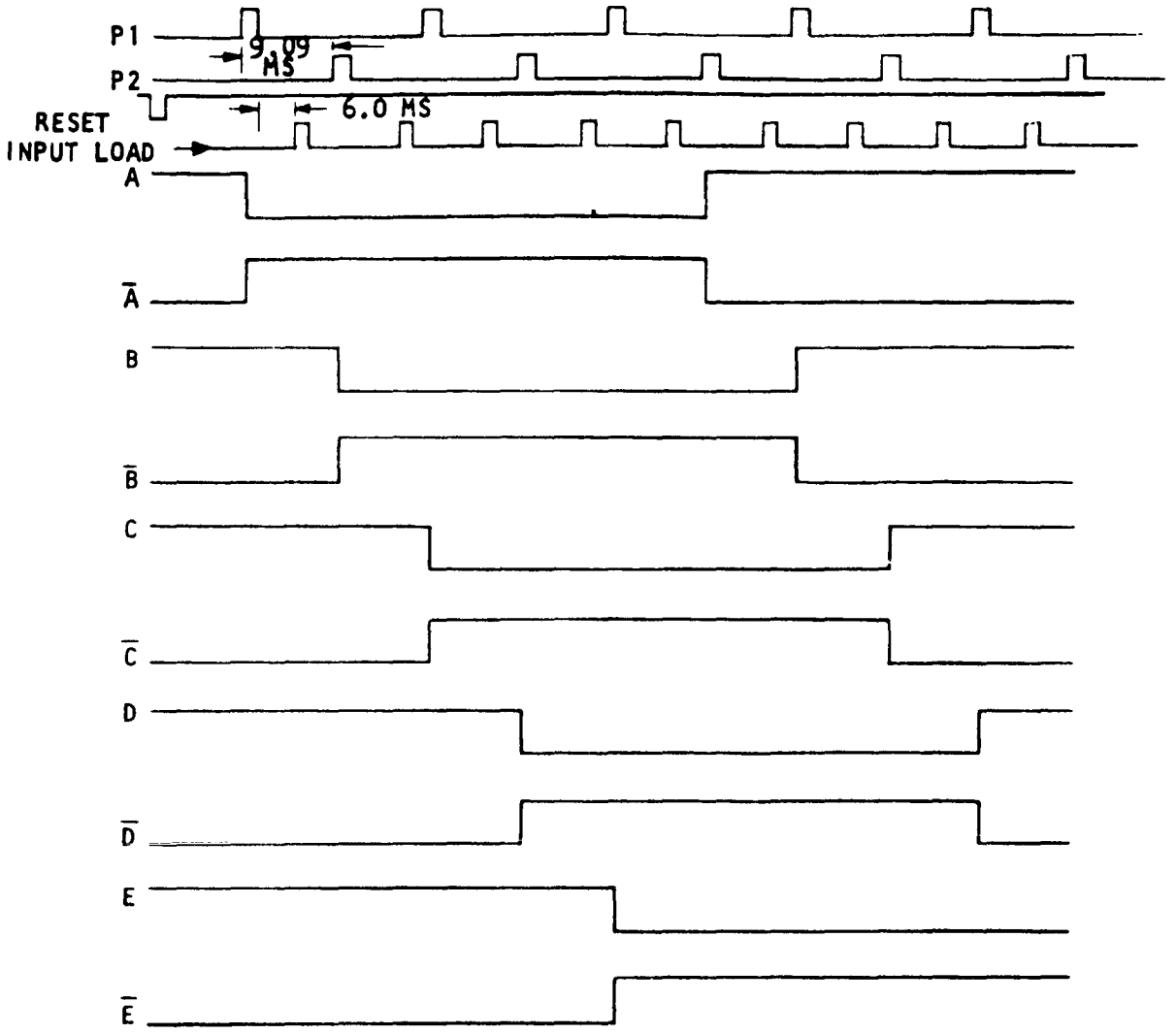
   The next step in the sequence $\overline{A} \cdot B$ will select Bit 5 of the SCR register. Point "S" (select) will go positive if the SCR has <u>not</u> been set (0) and will be clamped to ground if the SCR has been set (1). This output "S" is then OR'ed into the K1 driver so that if the SCR was set (1) the relay will not be energized and the "line" will remain closed. However, if the SCR was not set then the K1 driver will conduct and the relay contacts will open, opening the line. The next SCR, Bit 6, will be selected by the $\overline{B} \cdot C$ state of the sequencer and the line will be opened or closed depending on the state of the SCR. Each of the SCR's up to Bit 12 will be examined by the sequencer and the line will be opened or closed. Once the 8 bit code has been transmitted a "stop" pulse is given. This requires that the "line" be left closed for at least two units of time, 18.18 milliseconds. After this period of time a new character may be processed. The stop code occurs when state $D \cdot \overline{E}$ occurs and is generated by a unijunction time delay circuit covered later in the description of operation.

   After each output character is processed the register is cleared and an interrupt is given to the computer asking for another character.

2. Input Mode

   When a key is struck on the keyboard or a character is read from tape, the sequencer is reset and starts to step along in synchronism with the ASR set. A signal called "input load" is generated when the Input Mode is selected. This signal, shown in Figure 4, is used to strobe the condition of the "line" for each of the data bits. The input load signal occurs approximately 6.3 milliseconds after the beginning of each step of the sequencer.

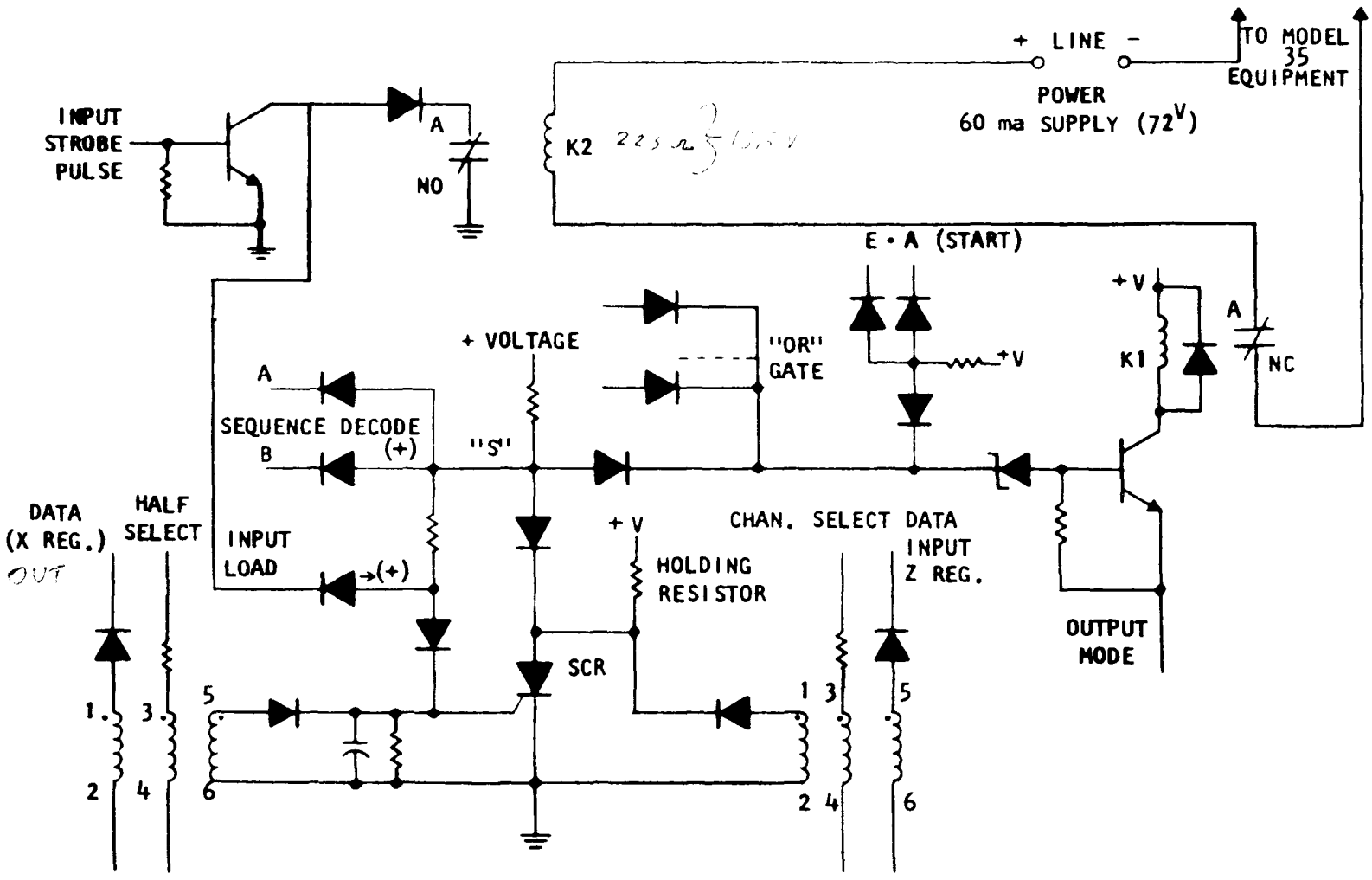
   The "input load" signal pulses the "gate" of the selected SCR. When this gate is allowed to go positive the SCR will be turned on. As shown in Figure 4, if the SCR is turned on when the input channel is selected the data input to the computer will be a logic "0" since the SCR shorts windings 1 and 2 of the pulse transformer. A logic "1" will be sent to the computer if the SCR is in the blocked state.



STEP	SEQUENCE STEP	BIT (OUTPUT MODE) "START"	BIT (INPUT MODE) "START"
9	$\bar{E}\cdot A$ (RESET)		
0	$\bar{A}\cdot B$	5	6
1	$\bar{B}\cdot C$	6	7
2	$\bar{C}\cdot D$	7	8
	(feedhole) ◄		
3	$\bar{D}\cdot E$	8	9
4	$\bar{E}\cdot\bar{A}$	9	10
5	$A\cdot\bar{B}$	10	11
6	$B\cdot\bar{C}$	11	12
7	$C\cdot\bar{D}$	12	13
8	$D\cdot\bar{E}$	"STOP"	"STOP"

ASR INPUT/OUTPUT SCAN SEQUENCE
Figure 3

"1" CURRENT ON THE LINE "0" NO CURRENT ON THE LINE



INFORMATION TRANSFER
Figure 4

Therefore, to transmit a logic "1" to the computer from the data register it is necessary to suppress the input load signal so that the SCR will remain blocked. This is done by using the contacts of a mercury relay as shown in Figure 4. The coil of the relay is in series with the line and is energized when the line is closed (1). The normally open contacts of this relay suppress the input load signal when the line is closed, a logic "1" condition. When the contacts open the input load signal is permitted to go positive. The contacts will open if the relay is de-energized, i.e., the line is open.

It is, therefore, possible to monitor the condition of the "line" and sequentially set the SCR data register. Since both the sequencer and the ASR set are in synchronism, it is possible to store the serial code in the buffer register. At step $\bar{A}\cdot B$ of the sequence point "S" is positive and if the "line" is open the input load pulse will not be inhibited and the SCR gate will be pulsed, setting the SCR. A logic "0" will be transmitted. If, however, when step $\bar{A}\cdot B$ occurs the "line" is closed the relay contacts will be closed and the "input load" signal will be suppressed and the SCR will not be set. A logic "1" will be transmitted to the computer. As each step of the sequence occurs the line contact will be monitored and the corresponding SCR will be turned on or left blocked.

When step $D\cdot\overline{E}$ occurs, the "stop" code is generated and an input interrupt is given, and the computer may then read the buffer register by addressing the particular channel.

3. Signal Requirements

The following signals are required between the Model 35 equipment interface package and the channel modules 2TN1, 4TO1, and 3TS1.

a) Two signal wire communication link with the capability of opening and closing the line for output; and the capability of monitoring the line opening and closing for input.

b) A reader control signal for start/stop control of Reader unit in Model 35 ASR.

c) Motor ON/OFF control signal for turning Model 35 equipment on and off under computer control.

The following signals are required between the I/O processor and the channel modules 2TN1, 4TO1, 3TS1.

a) Two Interrupt Input Signals

1) INPUT (2TN1) - indicating character is ready for transfer to I/O interface.

2) OUTPUT (3TS1) - indicating character has been processed by Model 35.

b) Two channel half selected signals, one for loading SCR Data Buffer for output and one for Inputting Data from SCR Buffer Register.

The 10 bit code used with the punch is shown in Figure 5.

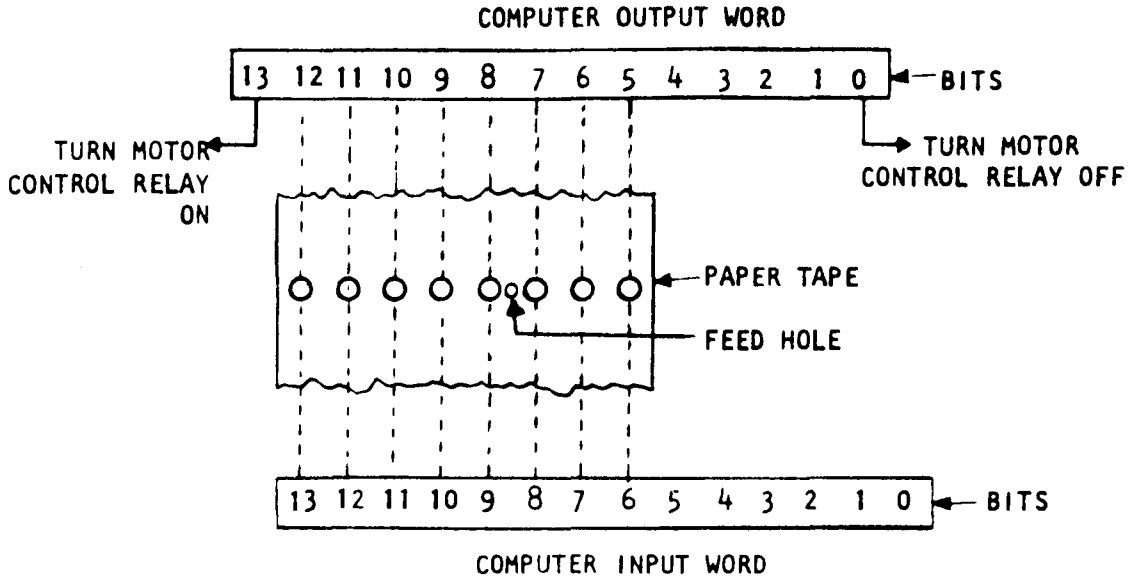


Figure 5

C. Motor On/Off Control

The motor in the Model 35 equipment may be turned on and off with the LINE/OFF/LOCAL switch on the set or by the computer which parallels the operation of this switch. Since the life of the equipment is related to the time that it is running, it is desirable to run the equipment only when it is necessary to print a message from the computer. For this reason the motor on/off circuitry has been installed.

As shown in Figure 6 there is a mercury relay on the 3TS1 card, which controls the motor on/off relay located on the interface package. The mercury relay is controlled by setting Bit 13 to a "1" which sets a bistable on the 4TO1 card. The output of this bistable energizes the mercury relay (M9-2). Bit 0 is used to reset the bistable which de-energizes the relay coil. The mercury wetted relay contact selects the power relay in the INTERFACE package located at the 35 equipment. The contacts of this power relay parallel the contacts of the switch (LINE/OFF/LOCAL) and put the set in the "Line" mode independent of the switch setting. The motor on the 35 set will then turn on.

As mentioned previously when the computer outputs a character to the 35 equipment, the sequencer will be "tripped off" and the line contact will open and cause the equipment to cycle. Proper operation of the equipment requires exact synchronism between the Model 35 equipment and the sequencer. The Sequencer cycles at the same rate at all times; however, the Model 35 equipment, if tripped off when the motor is coming up to speed, will not cycle at the correct speed since it is mechanical in nature. Therefore, the code which gets stored mechanically will be invalid and "nonsense" will be printed as the motor comes up to speed.

In order to prevent this invalid printing condition, the line contact on the TS card is shorted out while the motor comes up to speed. The line is not opened and a print cycle will not occur. This circuit is triggered by closure of the motor on contact. As shown in Figure 6 the output of this circuit, relay contacts, shorts out the line contact. When the "motor on" contact closes, a unijunction delay circuit fires after 1.0 seconds and sets an SCR which picks the blanking relay and the "line shorting" contacts open. By this time the motor is up to speed and printing may be done. When the motor on relay is opened by setting Bit 0 to a "1" the blanking relay will drop out.

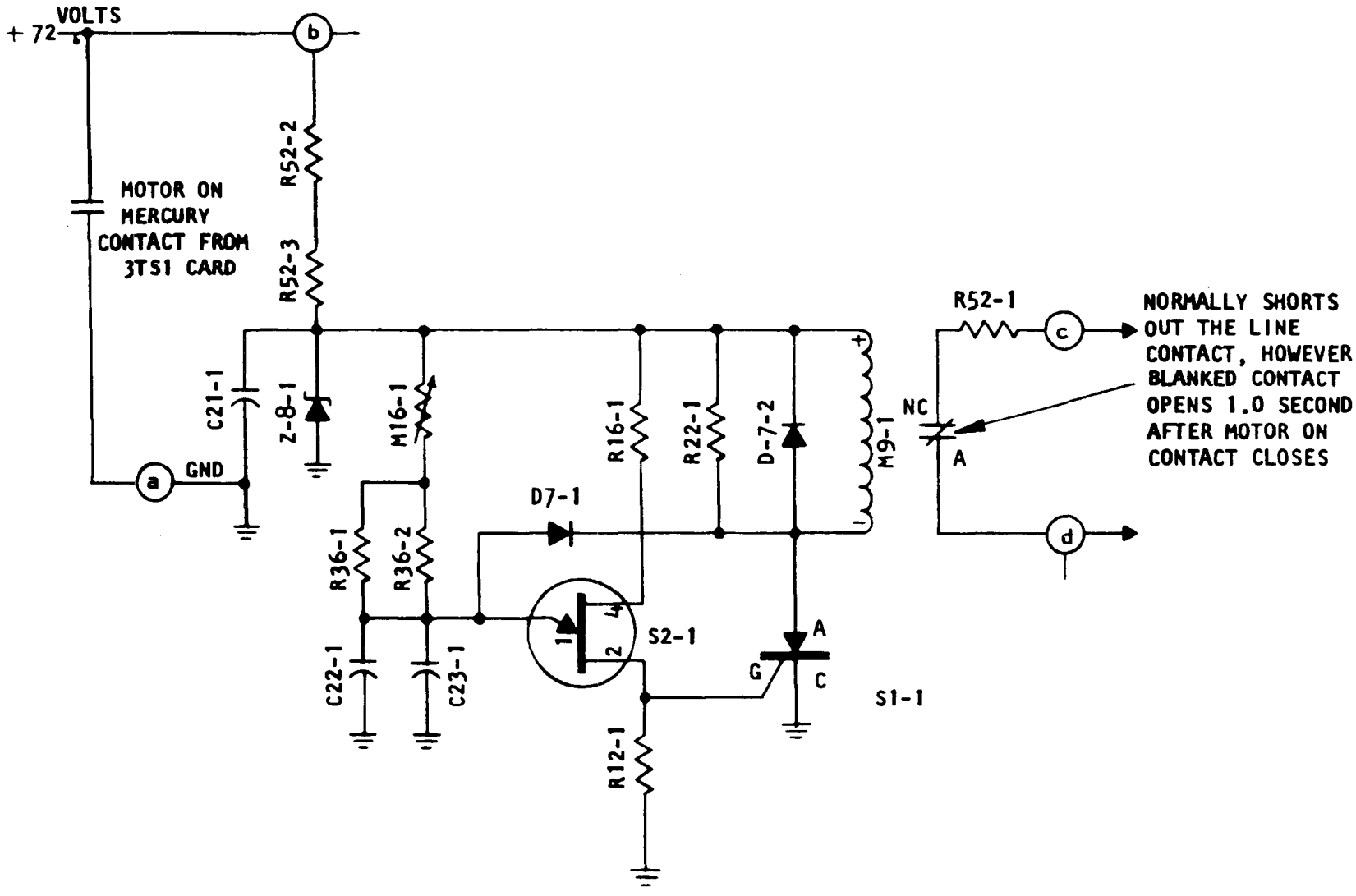

+ 72 VOLTS
b
MOTOR ON
MERCURY
CONTACT FROM
3TS1 CARD
R52-2
R52-3
C21-1
Z-8-1
M16-1
a
GND
R16-1
R22-1
D-7-2
M9-1
R52-1
c
NC
A
NORMALLY SHORTS
OUT THE LINE
CONTACT, HOWEVER
BLANKED CONTACT
OPENS 1.0 SECOND
AFTER MOTOR ON
CONTACT CLOSES
d
D7-1
R36-1
R36-2
S2-1
A
G
C
S1-1
C22-1
C23-1
R12-1

Figure 6

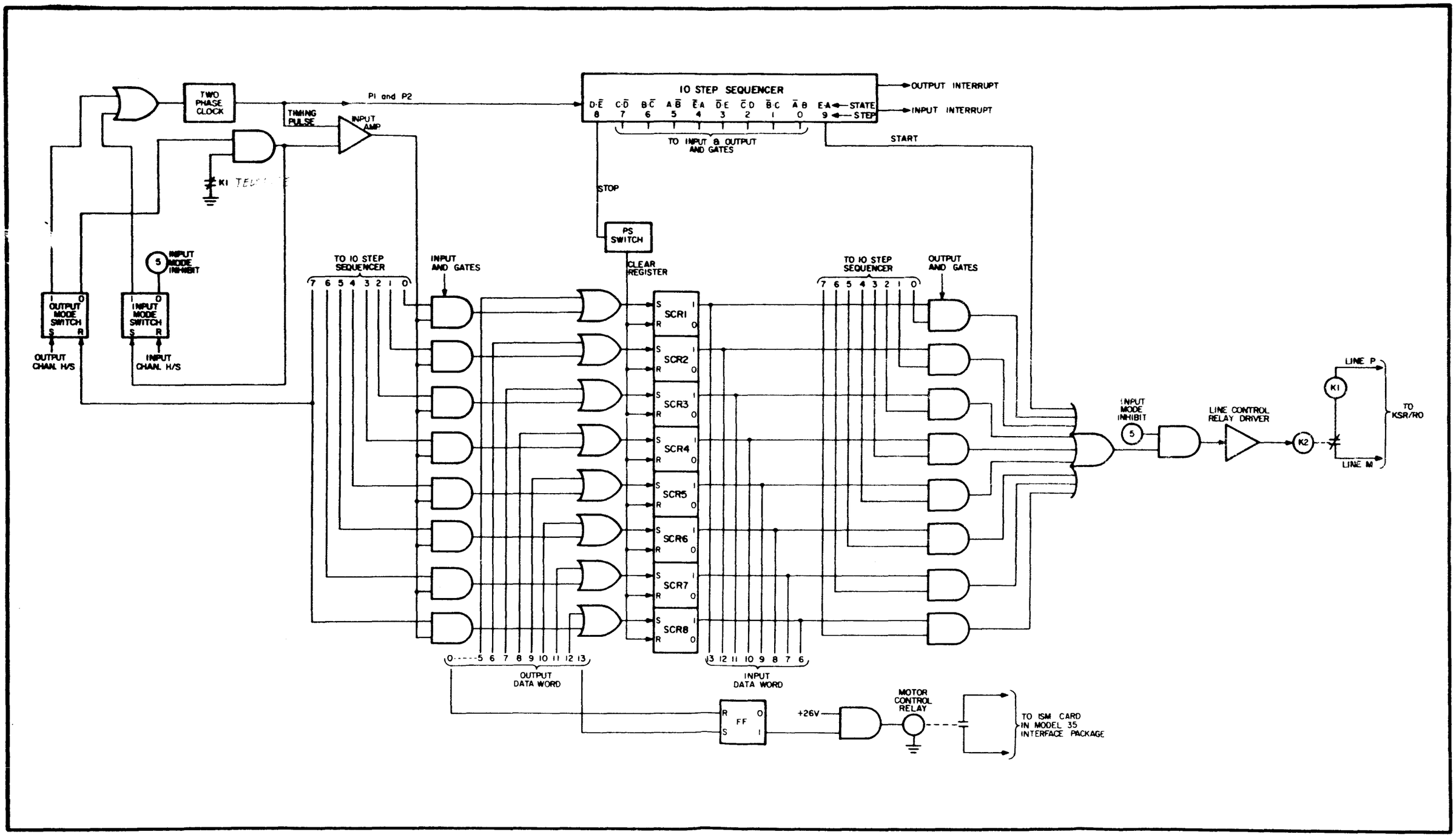


FIGURE 7-6. MODEL 35 INTERFACE LOGIC BLOCK DIAGRAM

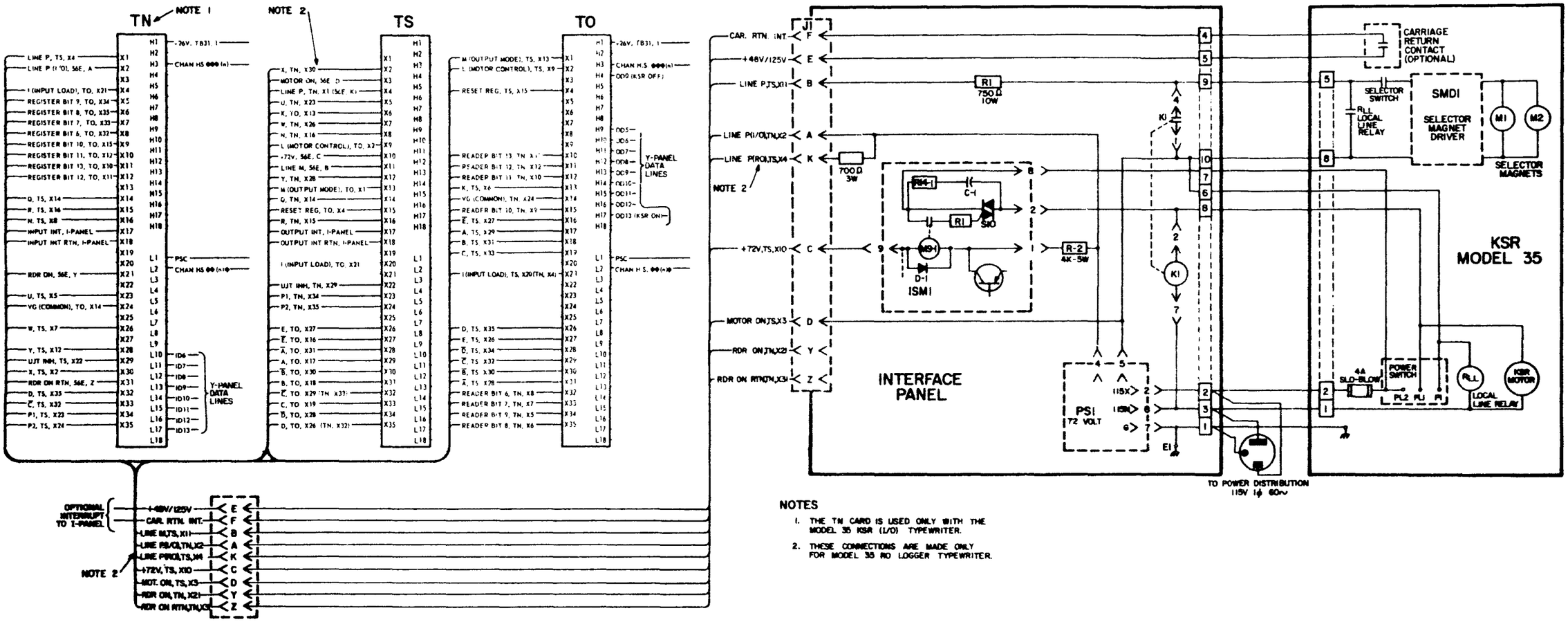
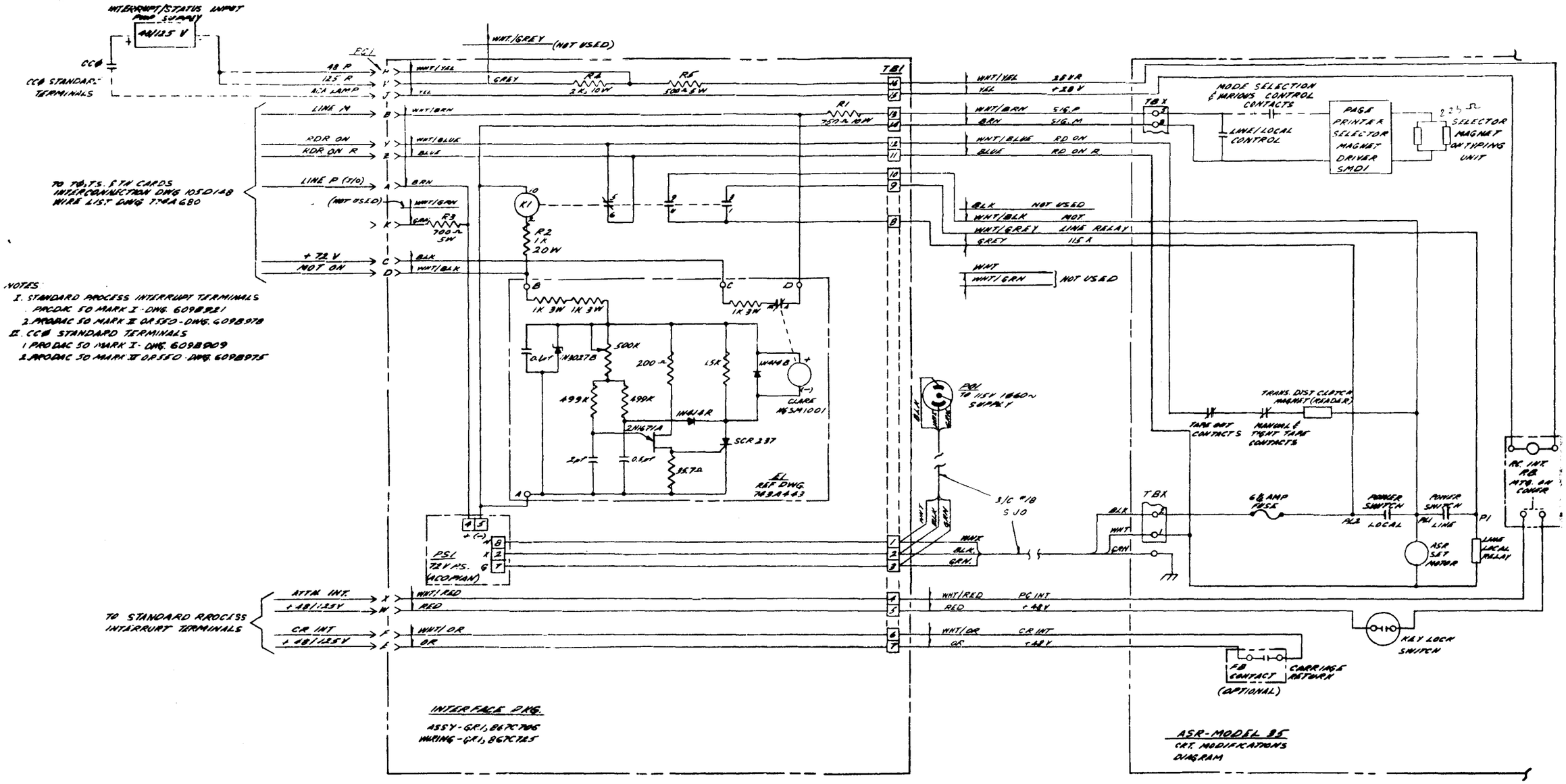


FIGURE 7-7. MODEL 35 LOGIC/WIRING DIAGRAM



NOTES:
I. STANDARD PROCESS INTERRUPT TERMINALS
1. PROLINC 50 MARK I - DWG. 609B981
2. PROLINC 50 MARK II OR 550 - DWG. 609B978
II. CC8 STANDARD TERMINALS
1. PROLINC 50 MARK I - DWG. 609B909
2. PROLINC 50 MARK II OR 550 - DWG. 609B975

REF. DWG. TABLE

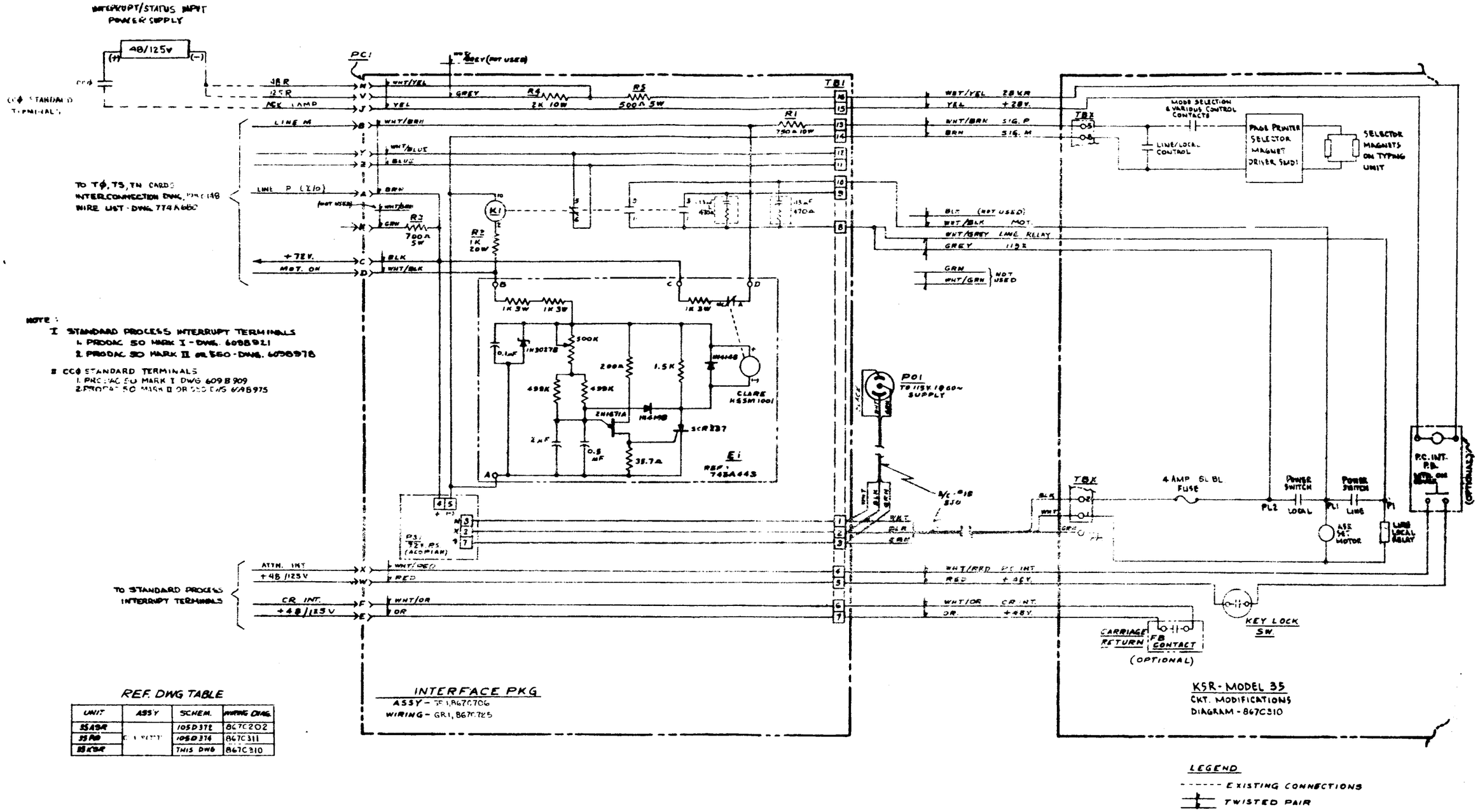
UNIT	ASS'Y	SCHEM	WIRING DWG.
35 ASR	GR1 867C706	THIS DWG	867C332
35 RO		105D374	867C311
35 KSR		105D373	867C310

LEGEND

-------EXISTING CONNECTION

TWISTED PAIR

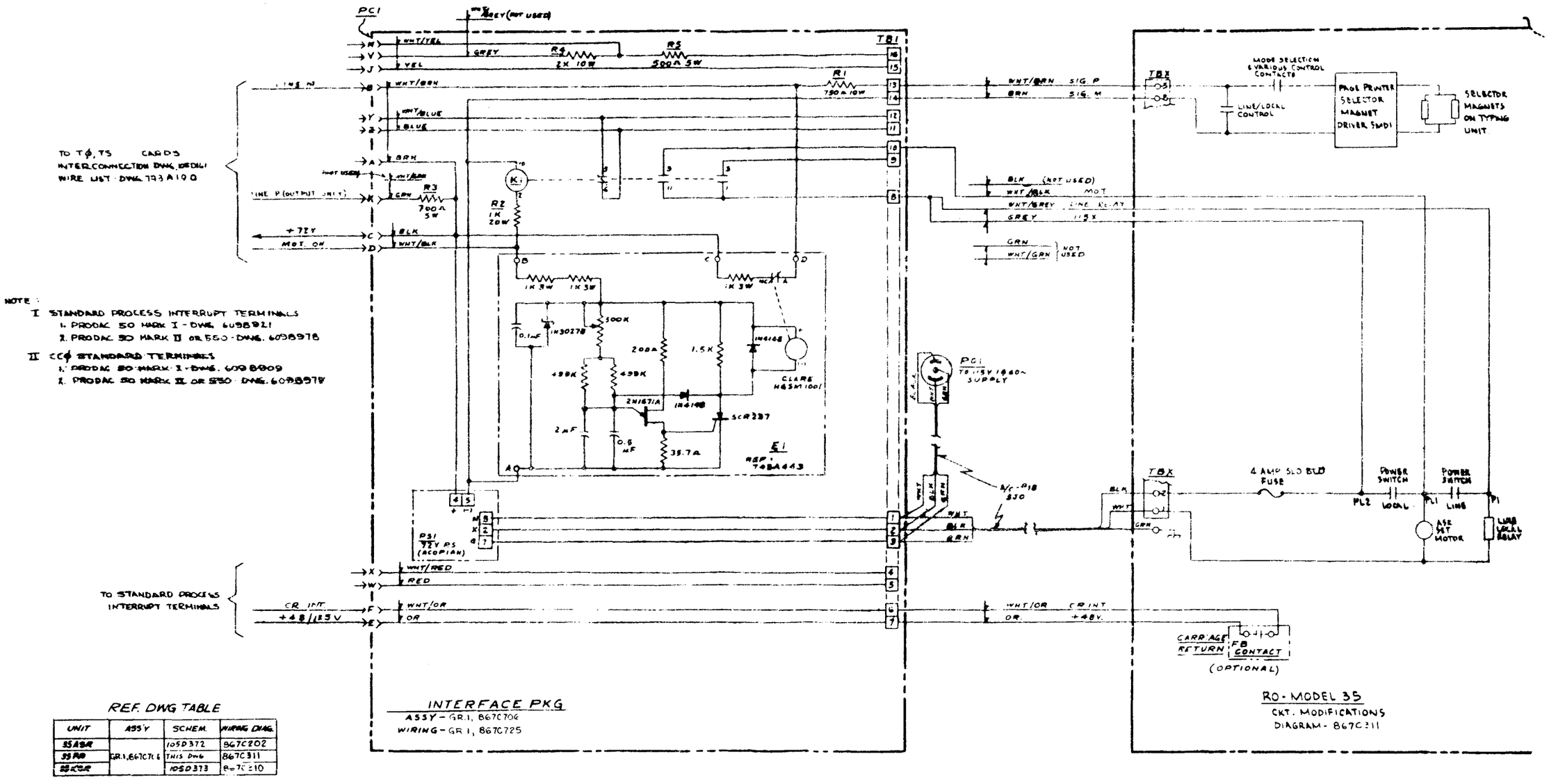
MODEL 35 ASR INTERFACE SCHEMATIC
(Ref. Ⓦ Dwg. 105D372, sub 5)



REF. DWG TABLE

UNIT	ASS'Y	SCHEM.	WIRING DIAG.
35 ASR		105D372	867C202
35 RO		105D374	867C311
35 KSR		THIS DWG	867C310

MODEL 35 KSR INTERFACE SCHEMATIC
(Ref. Ⓦ Dwg. 105D373, sub 6)



NOTE :

I STANDARD PROCESS INTERRUPT TERMINALS
1. PRODAC 50 MARK I - DWG. 6098121
2. PRODAC 50 MARK II OR 550 - DWG. 6098978

II CC⌀ STANDARD TERMINALS
1. PRODAC 50 MARK I - DWG. 6098809
2. PRODAC 50 MARK II OR 550 - DWG. 6098978

REF. DWG TABLE

UNIT	ASSY	SCHEM.	WIRING DWG.
35 ASR		105D372	867C202
35 RO	GR.1, 867C706	THIS DWG	867C311
35 KSR		105D373	867C210

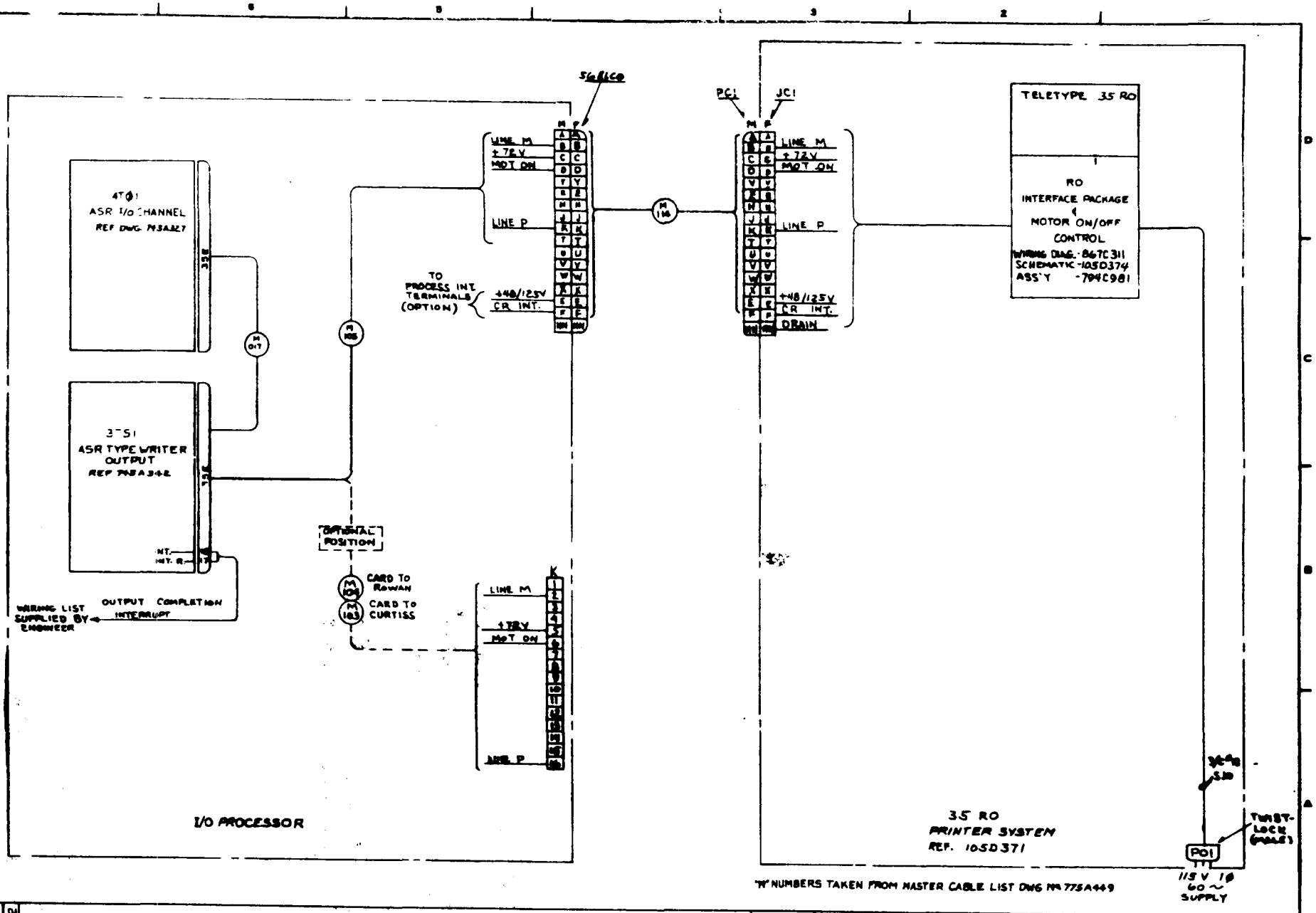
LEGEND

- - - - - - EXISTING CONNECTIONS

TWISTED PAIR

RO - MODEL 35
CKT. MODIFICATIONS
DIAGRAM - 867C311

MODEL 35 RO INTERFACE SCHEMATIC
(Ref. Ⓦ Dwg. 105D374, sub 7)



NEXT ASS'Y	REF DWG
DO NOT SCALE DWG. BREAK ALL SHARP EDGES AND REMOVE BURRS	
OVER 24	± 06 / ± 015
6 IN TO 24	± 04 / ± 010
UP TO 6 IN	± 02 / ± 005
BASIC DIM	2 PLACE DEC / 3 PLACE DEC
TOLERANCE UNLESS OTHERWISE SPECIFIED	

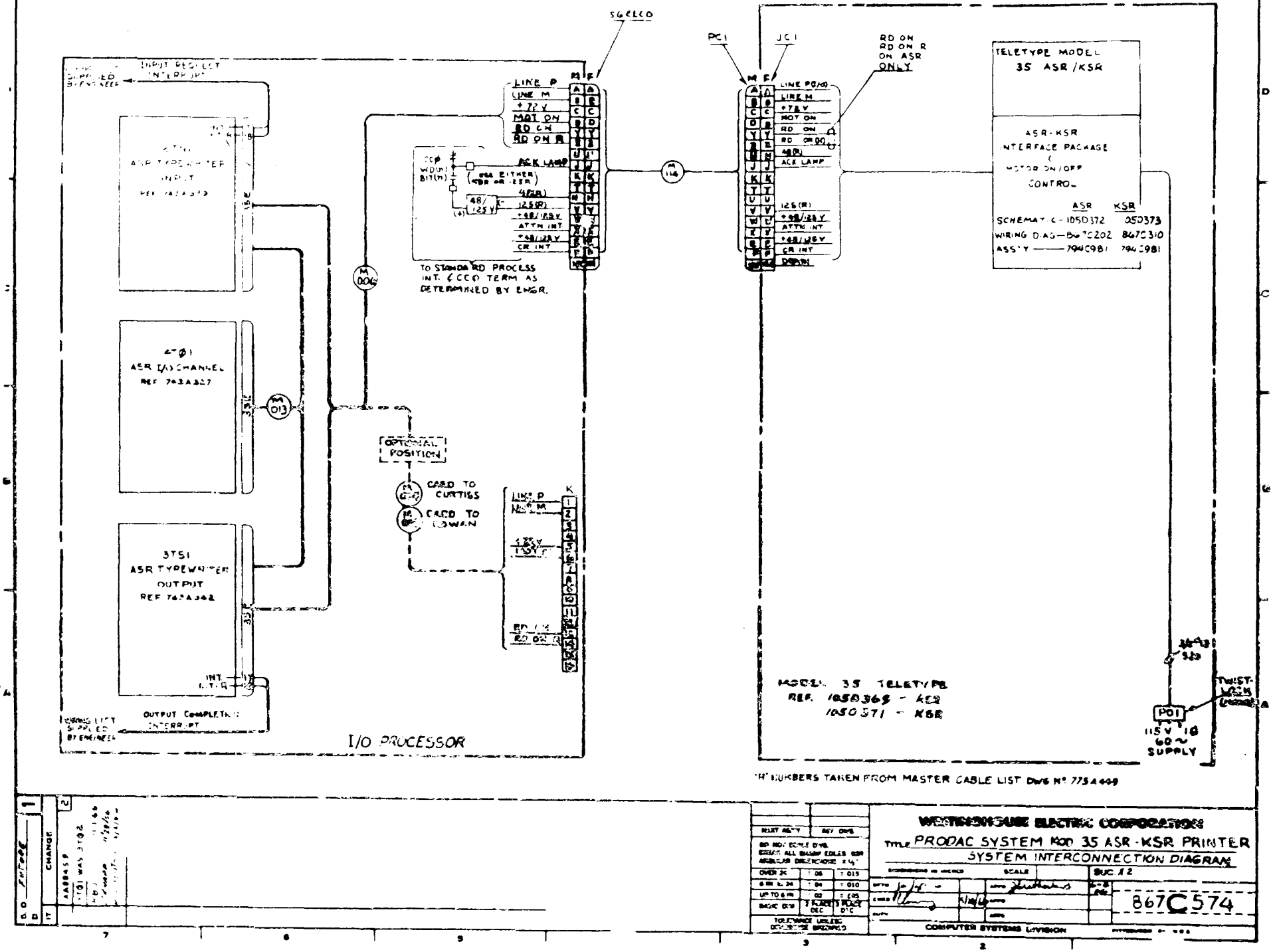
WESTINGHOUSE ELECTRIC CORPORATION

TITLE PRODAC SYSTEM MOD. 35 RO PRINTER
SYSTEM INTERCONNECTION DIAGRAM

SIZE E2 | SCALE | DRAWN | CHKD | APPD | DATE 1-6-66

867C573

COMPUTER SYSTEMS DIVISION



WESTINGHOUSE ELECTRIC CORPORATION

Title PRODAC SYSTEM 500 35 ASR-KSR PRINTER
SYSTEM INTERCONNECTION DIAGRAM

SIZE A2

867C574

COMPUTER SYSTEMS DIVISION

ENVIRONMENT AND GROUNDING

RECOMMENDED ENVIRONMENT

The following information was prepared for use by those persons who are responsible for the site preparation for a P-50 computing control system. A thorough understanding of, and close adherence to, the requirements and recommendations offered here are essential for an efficient system.

Site Selection

In considering possible locations for the computing system, the user should keep in mind his responsibility for providing all the necessary wiring, main circuit protection, and convenience receptacles required.

The following factors also should be considered:

1. The proposed area should be of sufficient size to accommodate not only the planned system but also any future expansion likely to be needed.
2. Doors, elevators, and corridors should have the strength and clearance necessary for moving individual units or assemblies making up the system, to the planned site. (The P-50 system generally is of such compact design and weight, however, that this rarely presents any problems.)
3. Floor construction should be adequate for support of the computer system, including peripheral units. (Again, normal industrial construction usually is more than adequate for the P-50.)
4. Sufficient clearance should be allowed for movement of test equipment around the computer system.
5. Environmental conditions should meet or exceed recommendations on recommended shock, vibration, temperature, and relative humidity.
6. Governing codes (local and/or state) concerning building construction, electrical wiring, fire protection, etc.

Computer Site Layout

Upon selection of the computer site, it is recommended that the user prepare a floor plan of the proposed computer area (1/4 to 1 foot scale). The plan should show all permanent objects such as support columns, piping, doors, walls, and any equipment considered indefinitely fixed in place. Also the floor plan should include a desired arrangement of the computer system that conforms with installation recommendations.

The plan should be given or sent to the Westinghouse project engineer assigned, for his information, review and comments.

Major areas of concern in the initial layout include:

1. The minimum required working area, for operation and maintenance of the computer equipment, including space for test equipment, tools, spare parts, and for whatever added room may be needed in the future in case of expansion of the system.

2. Positioning of computer units to permit operators to view displays, panels, etc., with little or no movement.
3. Power requirements of the system, and adequate air circulation.
4. Provision of an adequate service area.
5. Sufficient extra floor space for possible expansion of the system, including the facilities (power and air circulation) for such expansion.

Site Construction

Existing walls, floors and ceiling may be used to whatever degree is practicable, in keeping with the approved computer layout, and governing local and state construction codes as to entrances, fire exits, and other factors that may be involved. The floor should be true and level, and capable of sustaining the weight of the computer system and any additional equipment planned, without appreciable deviation. A raised or false floor is not required but can be convenient for running and locating cables. (Provision is needed in any case for bringing the power cabling and signal cables into the bottom of the cabinets.)

Wood floors are not recommended. If used, they should be covered appropriately for dust control, fire prevention and appropriate appearance.

Ceiling construction should be such as to keep down noise, and protect the equipment against moisture, oil, dust and objects that might fall from taller structures, cranes or other higher points.

Lighting should be capable of providing an over-all maintained intensity within the range of 55 to 75 foot candles at a height of 30 inches above the floor.

Area Housekeeping

Site construction should be completed before delivery of the computer equipment. All air ducts should be blown out and cleaned. The site and wiring troughs should be thoroughly cleaned of all dust, dirt and debris.

During connection of wiring, etc., to the computer system, care should be exercised to prevent metal filings, pieces of insulating material, dirt and other foreign matter from falling into the equipment.

After the equipment is installed and connected, but before power is turned on, cleaning of the entire area should be repeated.

During the regular scheduled cleaning of the area, the flooring should be cleaned with a damp mop. When a vacuum cleaner is used, the filter should first be cleaned.

Fire Protection

Beyond observance of all governing codes in providing fire protection, it is recommended that -- within the computer room and not more than 20 feet from the equipment -- either a CO_2 fire extinguisher or CO_2 hand hose system be installed. The number and capacity of extinguishers should of course be determined by the amount of equipment it is there to protect.

Also it is recommended that all documentation of programs and taped programs be prepared in duplicate, and a copy of each stored in a fireproof vault.

Power Considerations

Power Input: The basic input power for the system is as follows:

Voltage	115 v a-c
Frequency	60 cps
Allowable voltage deviation	± 10%
Allowable frequency deviation	± 0.6 cps

Primary Power Source: A separate power transformer should be provided for the computer system. When this is not possible, the power source used should be free of any heavy variable load such as elevator motors, air conditioning motors, etc. Means should be provided for disconnecting the primary power to the computer system in an emergency. It should be clearly marked "Emergency Power Disconnect," and shielded or enclosed to prevent accidental actuation. It should be located near the computer main frame and the main exit. Also it is recommended that all primary and distribution wiring meet UL recommendations.

Grounding: All grounding as specified herein is not intended to supplant but rather to complement those of the National Electric Code and Local Codes. Its primary purpose is to shield against noise and RF interference.

The following requirements must be strictly adhered to in order to provide optimum noise immunity on analog inputs to digital control computer. If they are not followed, no guarantee can be made as to system accuracy.

All low-level lines from sensors should be shielded twisted pairs. The shield should be grounded according to the following conditions:

1. A thermocouple which is not grounded at the well should have its shield grounded at the receiver end (computer terminal cabinet).
2. Thermocouples which are normally grounded at the source should have the shield grounded at the source. The most effective procedure includes a third wire, preferably one of the materials used in the thermocouple, which is connected to the top of the thermocouple and the shield. The shield is tied to the thermowell.
3. Transducers with balanced outputs should have the output guard tied to the shield, and the shield should be grounded at the receiver.
4. For transducer outputs of the single-ended variety, the shield must be grounded at the transmitter to be most effective.

In addition to these requirements, the routing of cables is a significant factor in minimizing pickup problems. The following recommendations must be followed in layout of wiring: All low level (0 to 50 millivolts) analog input signals should be routed through separate cable tray(s) and/or conduit(s). Under no circumstances whatsoever should a-c power or signal lines be routed with analog signals in either tray or conduit.

The cable tray should completely enclose the analog signal lines, and should be bonded firmly to the building ground system. The cable tray should effect at least 85 percent coverage of the analog cables. The only allowable exception to this is that low voltage (0 to 10 volts) d-c control cables may be routed in the same cable tray as the analog signals.

Cables carrying 125 volts a-c or lower should be spaced not less than 12 inches away from the analog tray; potentials of 440 a-c to 125 a-c volts should be spaced a minimum of 18 inches from the analog cables. Voltages above 440 volts shall be separated from the analog signals by a distance of not less than 2 feet. It is realized that in some circumstances power cables will run parallel to the analog cables. With the previously mentioned separation, this condition may exist for runs not exceeding 20 feet. Parallel runs are permissible to 50 feet by increasing

the recommended spacings a minimum of 1 foot. Longer runs of parallel length may be made by increasing the spacing requirement by 1 foot for every 30 feet above 50.

As previously mentioned, all analog signal lines should be twisted shield pairs. The shield encloses each pair and will offer not less than 85 percent coverage. The shield should be covered by insulation having suitable mechanical, electrical, chemical, and thermal properties. Multiple pair cables from the thermocouple reference junction to the computer input cabinet should not exceed 17 pair cables.

Convenience Outlets: The test equipment for the computer will require 120 v, 60 c, single-phase service. Convenience outlets should be provided near the equipment and around the perimeter of the room, at heights not exceeding 42 inches above the floor.

Air Filtration: The incoming air in the computer room or area should be clean or should first be filtered by a filter having 90 percent efficiency based on the Bureau of Standards Discoloration Test. A Westinghouse "Precipitron" unit is effective for this purpose.

Primary Power Source - General

A separate power transformer should be provided for the computer system. When this is not possible, the power source used must be without heavy variable loads such as elevator motors, air conditioning motors, etc., which might draw surge currents from the source sufficient to cause voltages to drop below allowable tolerances.

A means for disconnecting the primary power to the computer system in an emergency should be provided. It should be titled "Emergency Power Disconnect" and enclosed or shielded to prevent accidental actuation. The location should be near the central Processor and the main exit.

Loading

All standard equipment in the system operates on 115 volt 60 cycle per second single phase input voltage. Various parts of the system have been designed to accept 230 volt and 50 cycle input power; however, some modification is entailed in making a complete system conversion to these input power parameters.

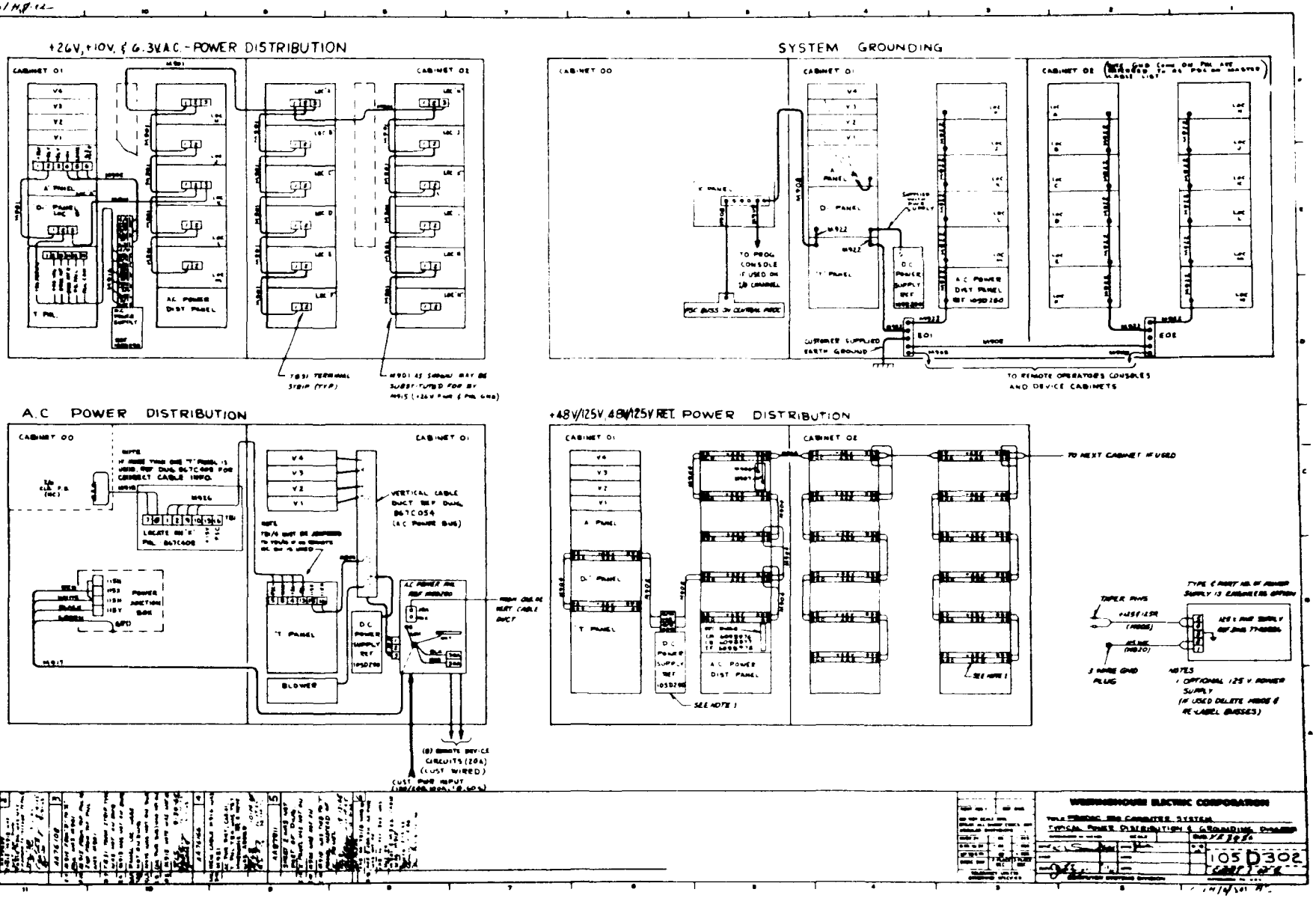
Grounding

The following requirements must be adhered to in order to provide optimum system performance. If they are not followed, no guarantee can be made as to system accuracy.

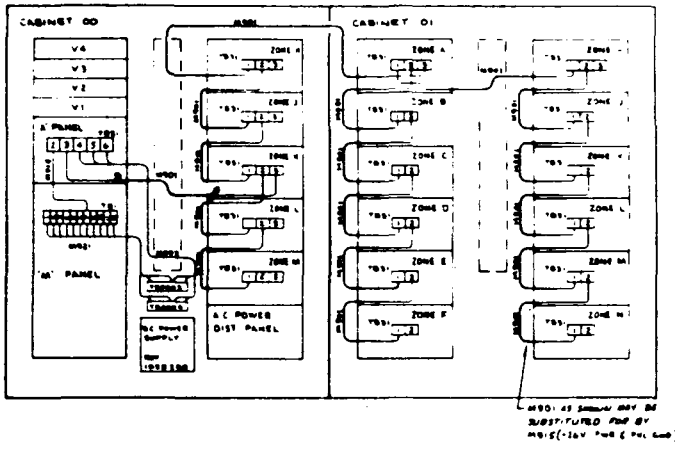
The following is aimed at providing adequate shielding for the computer system against noise and RF interference. It is intended that this recommendation will complement rather than replace any part of the National Electrical Code or local codes. A terminal is provided in the rear of the Central Processor Cabinet for a computer system ground connection. The preferred conductor for connecting the system to ground is a 1-1/2 inch minimum diameter copper braid with a minimum conducting cross-sectional area of 25,000 circular mils. This braid must be protected from physical damage. If copper braid is not available, a 6 AWG or larger copper conductor may be used. The computer system ground must be independent of plant ground and must have a resistance of less than 4 ohms to earth ground.

The shields of all cables to and from the computer must be grounded at one end only. This applies to external interrupt, analog, CCO, and CCI signal cables. It is often a function of the particular system which end of the cable shield is grounded. This must be decided on an individual system basis.

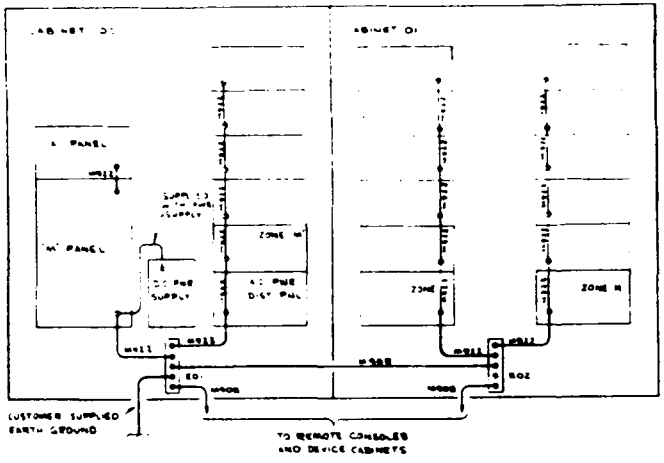
Drawing 105D302 shows a typical power distribution and grounding diagram for the P50 computer.


+26V, +10V, & 6.3V A.C. - POWER DISTRIBUTION
SYSTEM GROUNDING
A.C POWER DISTRIBUTION
+48V/125V, 48V/125V RET. POWER DISTRIBUTION
CABINET 00
CABINET 01
CABINET 02
A PANEL
D PANEL
T PANEL
V1
V2
V3
V4
A.C. POWER DIST PANEL
D.C. POWER SUPPLY
BLOWER
TO PROG CONSOLE IF USED ON LSI CHANNEL
CUSTOMER SUPPLIED EARTH GROUND
TO REMOTE OPERATORS CONSOLES AND DEVICE CABINETS
TO NEXT CABINET IF USED
SEE NOTE 1
3 WIRE GND PLUG
NOTES
1 OPTIONAL 125 V POWER SUPPLY (IF USED DELETE H0006 & RELABEL BUSSES)
WESTINGHOUSE ELECTRIC CORPORATION
105D302

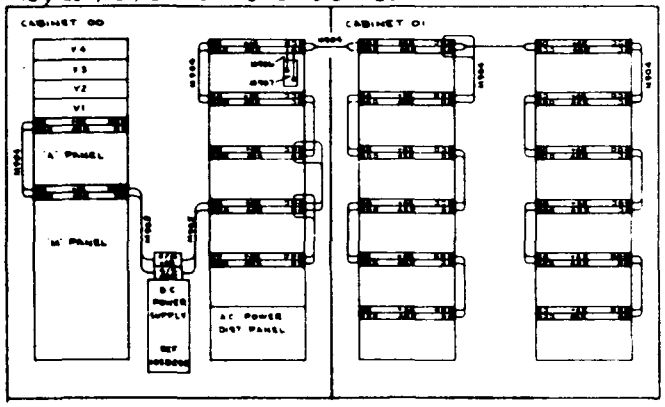
+26V, +10V, & 6.3 V.A.C. POWER DISTRIBUTION



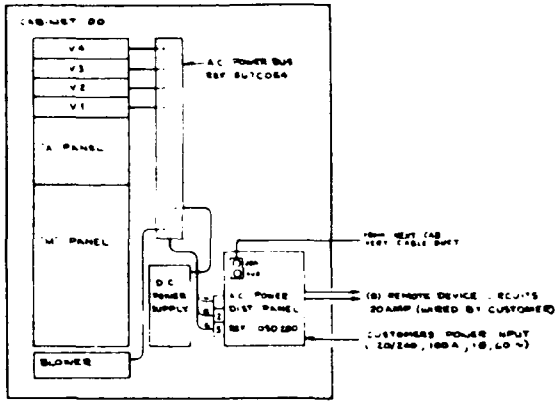
SYSTEM GROUNDING



+48V/125V, 48V/125V RET POWER DISTRIBUTION



A C POWER DISTRIBUTION



WESTINGHOUSE ELECTRIC CORPORATION

105 P302

Power Supply and Grounding Requirements

PRIMARY POWER SOURCE - GENERAL

A separate power transformer should be provided for the computer system. When this is not possible, the power source used must be without heavy variable loads such as elevator motors, air conditioning motors, etc., which might draw surge currents from the source sufficient to cause voltages to drop below allowable tolerances.

A means for disconnecting the primary power to the computer system in an emergency should be provided. It should be titled "Emergency Power Disconnect" and enclosed or shielded to prevent accidental actuation. The location should be near the Central Processor and the main exit.

LOADING

All standard equipment in the system operates on 115 volt 60 cycle per second single phase input voltage. Various parts of the system have been designed to accept 230 volt and 50 cycle input power; however, some modification is entailed in making a complete system conversion to these input power parameters.

115 V.A.C. SYSTEM OPERATION

1. Main Frame Power Supply

Input Voltage	115 v a.c. ±10%, 58-62 cps, 1Ø
Inrush Current	80 amperes max. peak current
Steady State Current	6.4 amperes kms (for max. system)
Power Factor	0.76 typical
Duty	Continuous

2. Fans

Input Voltage	115 v a.c. ±10%, 50-60 cps, 1Ø
Current	Approx. 0.9 amperes rms
Duty	Continuous

3. Analog-to-Frequency Converters

Input Voltage	115 v a.c. %10%, 58-62 cps, 1Ø
Power	Approx. 23 watts per converter to a maximum of 4 converters
Duty	Continuous

4. Model 33 ASR Set

Input Voltage	115 v a.c. ±10%, 60±0.45 cps, 1Ø
Current	Approx. 2 amperes, rms
Duty	Intermittent

5. High Speed Tape Reader

Input Voltage, Motor Unit	115 v a.c. ±10%, 60 cps ±0.75%, 1ø
Motor Current, Inrush	4.0 amperes rms
Running	1.25 amperes rms
D.C. Power Supply Unit	115 v a.c. ±10%, 50-60 cps, 1ø
Current Input	Approx. 0.25 amperes rms a.c.
Duty	Intermittent

6. High Speed Tape Punch

Input Voltage, Motor Unit	115 v a.c. ±10%, 60 cps ±1%, 1ø
Motor Current, Inrush	9 amperes rms
Running	2 amperes rms
D.C. Power Supply Unit	115 ±15 v a.c., 60 cps ±5%, 1ø
Current Input	3 amperes, rms a.c.
Input Power	280 watts
Duty	Intermittent

7. Model 735 Logger

Input Voltage, Motor Unit	117 v a.c. ±10%, 60 cps, 1ø
Motor Current, Running	1.2 amperes rms
D.C. Power Supply Unit	115 v a.c. ±10%, 50-60 cps, 1ø
Current Input	0.5 amperes rms, a.c.
Duty	Intermittent

230 V.A.C. SYSTEM OPERATION

1. Main Frame Power Supply

Input Voltage	230 v a.c. ±10%, 48-62 cps, 1ø
Inrush Current	40 amperes max. peak current
Steady State Current	3.4 amperes rms (for max. system)
Power Factor	0.76 typical
Duty	Continuous

GROUNDING

The following requirements must be adhered to in order to provide optimum system performance. If they are not followed, no guarantee can be made as to system accuracy.

The following is aimed at providing adequate shielding for the computer system against noise and RF interference. It is intended that this recommendation will complement rather than replace any part of the National Electrical Code or local codes. A terminal is provided in the rear of the Central Processor Cabinet for a computer system ground connection. The preferred conductor for connecting the system to ground is a 1-1/2 inch minimum diameter copper braid with a minimum conducting cross-sectional area

of 25,000 circular mils. This braid must be protected from physical damage. If copper braid is not available, a 6 AWG or larger copper conductor may be used. The computer system ground must be independent of plant ground and must have a resistance of less than 4 ohms to earth ground.

The shields of all cables to and from the computer must be grounded at one end only. This applies to external interrupt, analog, CCO, and CCI signal cables. It is often a function of the particular system which end of the cable shield is grounded. This must be decided on an individual system basis.

Analog signals require more exacting shielding and grounding considerations than CCI or EI. As a result, the following recommendations are made for shielding and grounding of analog signals:

Standard analog input modularity is 16 inputs on one printed circuit card, and each card has provision for one connection to the A/D converter guard shield. Therefore, analog inputs should be grouped on the card according to a criterion of like grounding requirements in order to maximize the one shield connection.

Each analog signal should be carried on a twisted pair. This pair of leads is to be shielded. It is preferable in most cases to use a multi-pair cable with an overall shield. The shield should be constructed to give 100% coverage when the cable is flexed, and each shield should have a copper drain wire. This drain wire should be grounded at one point only at both ends.

For an ungrounded thermocouple, the cable shield should be connected to one ground plane at the cold junction box. The analog converter guard shield should be tied to this cold junction box ground plane.

For grounded thermocouple(s), the cable shield should be connected to the ground plane in which the thermocouple is grounded. The other end of the shield is then tied to the analog converter guard shield. NOTE: All thermocouples in a cable and the shield ground must be in the same ground plane. If this is not possible, the cable shield and the analog converter guard shield should be grounded at the cold junction box ground plane. Common mode voltage between any thermocouple pair and the cable shield (analog converter guard shield) should not exceed 5 volts.

For a grounded voltage or current generator, the shield should be grounded at the transducer. All transducers must be grounded in the same ground plane. The shield is tied to the analog converter guard shield.

For a floating transducer, the cable shield is tied to the analog converter guard shield and to converter ground.

In every case, the common mode voltage between signal leads and cable shield should be restricted to less than 5 volts.

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POWER DISTRIBUTION & POWER SUPPLY PACKAGE

POWER DISTRIBUTION

Power as discussed in this section means a-c power taken to points within the central processor cabinet and to convenience outlets in this cabinet.

In general a-c power will be supplied from an unregulated 115 volt, 60 cps single phase source. The ac/dc power supply package in the central processor cabinet is designed to accept 115/230 volt, 50-60 cps power as determined by transformer winding jumper connections. However, other components which can be units of the cabinet, such as fans may not have this flexibility. As such, these items might have to receive special consideration in adapting a system to a 230 volt a-c or 50 cps power supply.

A-c power is brought into the cabinet to CB1. From here, it also branches out to 4 convenience circuit breakers. The other side of CB1 (15A) is connected to a filter capacitor then to TB0002-4. The neutral side is tied to another filter capacitor then to TB0002-3.

An additional breaker CB4, is used to provide power to an auxiliary receptacle mounted on the a-c distribution panel assembly. From the incoming side of CB4, power is also distributed to an additional 4 circuit breakers which can be used at the customers' discretion.

From TB0002, power is routed to the power distribution strip where the d-c power supply module receives its power.

POWER SUPPLY

Schematic diagram 105D312 shows the main power supply as used on the P50 computer.

As mentioned previously, power is received by this supply from the a-c distribution box, TB0002.

This power supply furnishes four output voltage levels; 48vdc, 26vdc, 10vdc, and 6.3vac. These four voltage levels furnish all the power necessary for memory and logic circuits within the computer plus the power for external interrupts.

The +26v is taken to TB0004 for distribution to the logic and memory and to TB0003, through a 6 amp fuse, for distribution to the maintenance lights on the printed circuit card and any peripheral power required.

The +10v is taken off of the +26 volt supply by tapping off a Zener diode, CR7 and distributing this voltage to TB0004 through a 1 amp fuse.

Note that in both cases above, the common side of the power supply is tied to frame ground at E01. This side will also be referred to as PSC (Power Supply Common).

The 48 volt supply is obtained from a center tapped full wave rectifier with a capacitor output filter. The +48v is tied to TB0004 through a 2 amp fuse, its return side, 48R is tied to TB0004 also. Note that this supply is isolated from PSC.

The 6.3vac is derived from the secondary of a filament transformer. This voltage is used to drive the synchronizer interrupt on the low voltage sensor card which is mounted in the power supply package.

The +26v is also routed to the low voltage sensor card for use in the Low Voltage Detection Circuit.

The 48R is used also on the low voltage sensor card in the Dead Computer Switch circuit.

For operation of this low voltage sensor card, refer to the printed circuit card descriptions.

TAP ADJUSTMENTS

The power supply has been designed to accept 115/230 volt, 50/60 cps, single-phase input. Jumpers on the primary windings of the three transformers in the supply must be wired correctly to match the transformers to the line voltage. Each transformer has a dual primary winding. These windings must be placed in series for 230vac operation or in parallel for 115vac operation. Schematic 105D312 gives the connections required for 230v operation.

With the exception of the 26vdc source, the transformers do not have taps for adjusting the output voltage to allow for small differences in nominal line voltages or differences in load. The loads are sufficiently insensitive to voltage variations that the output voltage can be allowed to swing with 100% switching of load currents and the line voltage variations of ±10% around 115vac or 230vac.

The 26vdc source transformer has secondary winding taps at 3% voltage increments which are used to adjust the output voltage to a nominal value for different loads on the supply (i.e., systems of various size) and for small differences in nominal line voltage. The output bus voltage should be at 27.3 ±0.5vdc with power applied to the system and the central processor in the Master Cleared mode.

GROUNDING, RF TRAPPING

Grounding

The entire system is tied to ground via a plant ground lead tie to point E01 in the central processor cabinet. From this point, all cabinets in the system as well as the power supply are tied together with braid binding straps. The 26vdc and 10 vdc current return paths are at system ground potential. Also, one side of the 6.3vac power supply output is tied to system ground.

RF Trapping

Precautions have been taken to keep high frequency noise on the input a-c power lines out of the power supply. For this purpose, a radio frequency interference filter has been placed in each of the two power input lines.

It is especially important to keep this radio frequency noise out of the 26vdc supply since logic and memory power is furnished by this bus. As an added precaution, the primary winding of this transformer is electrostatically shielded from the secondary. Figure 2-24 is a simplified representation of the RF1 filtering and system grounding.

Each cabinet structure has been designed to afford shielding to power distribution leads (as well as signal leads). Cabinets are fully enclosed, all-steel structures which are physically

joined together to form one mechanical unit. Thus the 26vdc, 10vdc, and 6.3vac leads are never taken outside the system. Within this steel enclosure, back-panel wiring is additionally protected by (1) the aluminum panel which supports the card cages, the card edge connectors and panel-to-panel cable connectors and (2) the cable support bracket which covers wire runs behind the card cages in the cabinets. (The aluminum panels which hold the card cage structures are tied together with the braid bonding strap. Within the cabinet, these panels establish the system ground reference plane.)

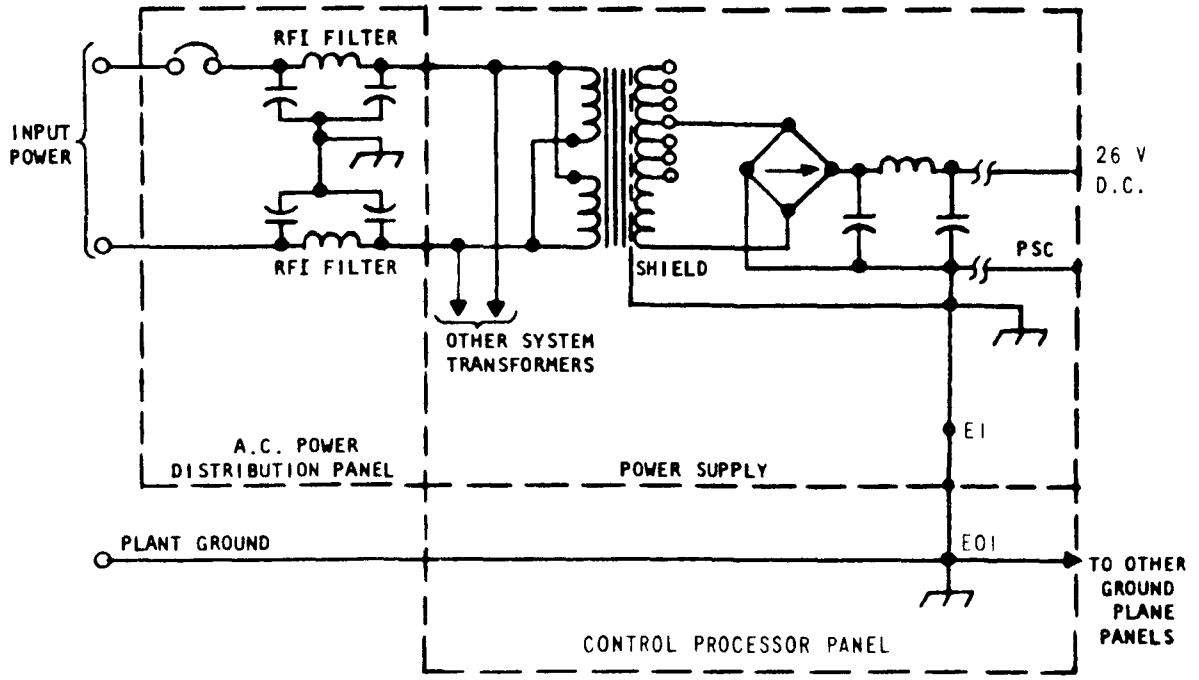
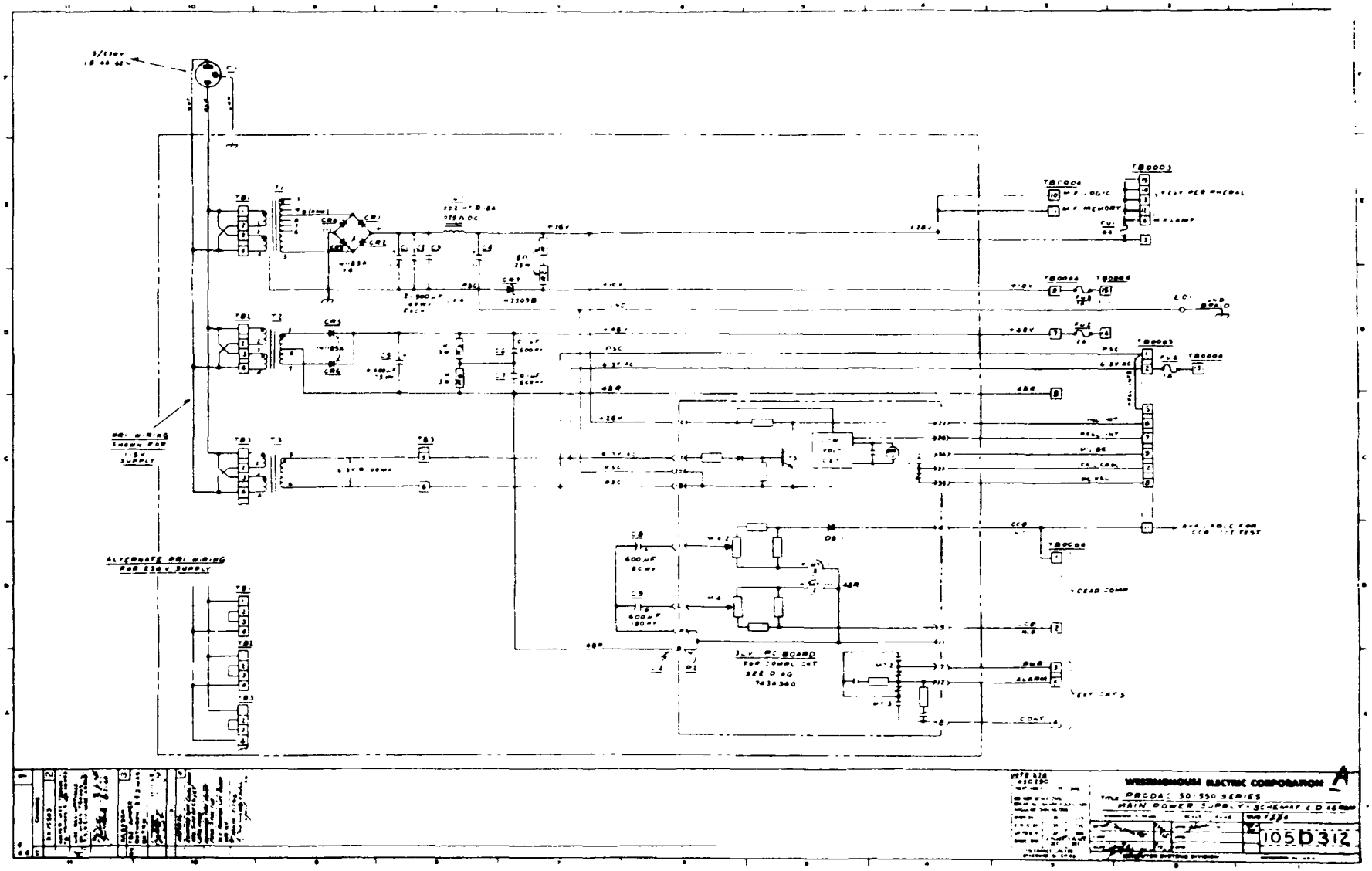


Figure 2-24.


ALTERNATE PRI. WIRING FOR 230 V. SUPPLY
WESTINGHOUSE ELECTRIC CORPORATION
105D312

STORAGE AND HANDLING

Because of its physical and electromechanical characteristics, the P-50 is capable of withstanding indefinitely the industrial environments in which men themselves are capable of working. It requires no "babying". However, as with any valuable equipment, the user who observes a few common-sense rules for handling, storage, maintenance and general care can thus avoid trouble which could be expensive in terms of time and/or money.

STORAGE RULES ARE SIMPLE AND FEW:

1. All mechanical units that make up the system should be stored upright in a dry, relatively dust-free area.
2. The dust covers supplied on the units should be kept on during storage.
3. Storage temperatures should not be below 32° or above 100°F.
4. The relative humidity should not exceed 90 per cent.
5. Storage of units should be such as to minimize the need for rehandling. It is recommended that cabinets, consoles, etc., be placed on 2 x 4's or 4 x 4's for ease in subsequent rehandling.
6. Area security should be maintained to prevent unauthorized personnel from gaining access to the computer equipment.
7. Cables should be kept in the cartons provided, and the cartons stacked on 2 x 4's, with stack height not to exceed three cartons.

HANDLING

Handling, lifting and moving also should be in accordance with certain simple rules:

1. Handling shock: not to exceed 4G.
2. Vibration: less than .03G for 15 cycles per second.
   less than .02G for 16 to 25 cycles per second.
   less than .01G for 26 to 33 cycles per second.
3. All central processors, input output cabinets and auxiliary units such as document devices (ASR sets, etc.) be kept upright at all times. Maximum allowable tilt, 45°.
4. Care should be exercised, in lifting cabinets, to avoid damage to side panels and doors.
5. Hooks, cargo nets are <u>not</u> recommended.
6. Floor-mounted consoles are not to be lifted by the writing surfaces or doors. It is recommended that dollies or other four-wheel devices be used, in preference to fork lift trucks.
7. Prior to movement of operator or printer consoles, the printers, readers, punches and other unsecured devices should be removed, packaged separately for safe movement, and kept packaged until they are to be connected and used.
8. For long-distance movement, furniture van or air shipment is recommended. Overseas shipments should be by air only.

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Timing Notes

This section discusses switching times of elements, delay times through important circuits, tolerances of timing pulses, and delay adjustments on power supply switches.

LOGIC ELEMENTS

CORDWOOD DUAL NAND

The typical average propagation time per stage is 20 nanoseconds. With variations in loading, supply voltage, temperature, and switching parameters, the average propagation time varies from 15 to 30 nanoseconds.

CORDWOOD MODIFIED DUAL NAND

Switching times for the modified dual NAND are slower than for the dual NAND. Typical average propagation time is 50 nanoseconds per stage. This varies from 30 to 70 nanoseconds.

CORDWOOD SLOW NAND

Storage time is the longest delay through this element and is typically 6 microseconds. Some elements may be as slow as 10 microseconds for high temperature, low fanout conditions. Turn-on is usually under a microsecond.

IMPORTANT CIRCUITS

CORE PULSER

Delay times through the core pulsers vary from 0.25 to 0.4 microsecond. Rise and fall times of the output current pulse are 0.25 to 0.3 microsecond.

SUBROW HALF-SELECT SWITCH

Turn-on delay varies from 0.1 to 0.3 microsecond. Turn-off time varies from 0.25 to 0.5 microsecond.

Subcolumn Half-Select Switch

Turn-on delay varies from 0.15 to 0.25 microsecond. Turn-off time varies from 0.2 to 0.3 microsecond.

SENSE AMPLIFIER

A delay time derived from the phase shift at 1 megacycle for the sense amplifier is 0.2 microsecond.

CORE STROBE TIMING

Core strobe is adjusted by displaying the amplified core response voltage and the strobe voltage. These signals may be viewed at any bit card by viewing pins L17 and L16 respectively with respect to ground.

DELAY LINE TIMING

Accumulated tolerance of the delay line taps is about 2% or 30 nanoseconds. More troublesome than the variation in the absolute value of the delay of each tap is the variation in rise time of the pulse sent down the line. In order to preserve a good delay to rise ratio a 1.5 microsecond line is used, and the line is traversed three times to produce the sequence timing. This is in contrast to using a 4.5 microsecond line where degradation of rise time would occur throughout the line length. Still, the 50-nanosecond rise time of the pulses contributes some variation in the length of a sequence, which may be as much as 0.15 microsecond.

POWER SUPPLY SWITCH

The power supply switch produces a 0.11 to 0.30 microsecond opening of the word and channel circuits after a delay from the point of outputting which is adjustable from 1 to 9 milliseconds. Delays for some applications of the power supply switch are:

1. CCO: 3 milliseconds to energize bistable relays
2. CCI: 9 milliseconds from output to interrupt
3. Contact Input Data: minimum delay
4. Data Link: minimum delay

PHASE-LOCKED OSCILLATOR CARD

The use of 60 cps as the gate frequency for the analog system voltage-to-frequency converter requires that the short-term variation in the zero crossing of the 60 cps line be integrated. A phase-locked oscillator is used to generate a precise gating period. The frequency and phase of the phase-locked oscillator are compared to the 60 cps line. An analog voltage is derived which controls the frequency of a voltage-controlled oscillator. The variation on the 16.667 millisecond square wave is about 1 microsecond. The observation to check whether the oscillator output is in phase is to check that the phase-locked oscillator output does not drift when synchronizing the oscilloscope trace with the 60-cps line.

POWER OUTAGE WARNING

When the a.c. power line opens, the power supply will droop at a rate of about 0.2 volt per millisecond. After approximately 20 milliseconds, an interrupt is sent to the computer. The interrupt must be answered within 7 milliseconds. From the time the interrupt is sent an 8-millisecond delay is begun, at the end of which a relay drops out to inhibit the core memory. The 1-millisecond difference between the maximum time needed to answer the interrupt and the 8-millisecond delay is to enable a routine to be run which guarantees orderly shutdown.

Standard Signal Specifications

CORDWOOD DUAL NAND

1. Switching Levels: 0.5 volt maximum for logic "zero" condition, 1.0 volt minimum for "one" state.
2. Fanout Capability: 10 NANDs with single drive; 20 NANDs maximum with double-base drive. (In "double base" drive, a 3K resistor is connected from the NODE of the diode AND to the +6.8 volt supply.)
3. Input Loading: One NAND input requires that 2.1 milliampere maximum be drawn to hold down to ground.
4. Supply Voltage: 6.8 volts ±5 per cent.
5. Collector Voltage Rating: Output should not swing more than 6.8 volts +5 per cent if pullup resistors or non-standard loads are connected to the collector.

CORDWOOD MODIFIED DUAL NAND

1. Switching Levels: 0.5 volt maximum for logic "zero" condition, 1.0 volt minimum for "one" state.
2. Fanout Capability: 10 NANDs with single drive; 20 NANDs with double-base drive.
3. Input Loading: One NAND input requires that 2.1 milliampere maximum be drawn to be held down to ground.
4. Supply Voltage: 6.8 volts ±5 per cent. Base resistors are not commoned as in dual NAND so that base resistors may be driven as in resistor-coupled logic circuits. In this case input swing should be 6.8 volts - 5 per cent minimum.
5. OR Input: The base device series diodes are tapped to enable diode OR connections to the base circuit.
6. Collector Voltage Rating: Collector rating is sufficient to tolerate pullup resistors returned to the + 26-volt supply.

CORDWOOD SLOW NAND

1. Switching Levels: 1.1 volt maximum for zero condition, 1.6 volt minimum for "one" state.
2. Fanout Capability: 10 slow NANDs or 63.5 milliamperes.
3. Input Loading: One slow NAND input requires that 6.3 milliamperes maximum be drawn to be held down to ground.
4. Supply voltage: 6 to 10 volts.
   Base resistors are not commoned as in dual NAND so that base resistors may be driven as in resistor-coupled logic circuits. In this case input swing should be 6 volts minimum.
5. OR Input: The base device series diodes are tapped to enable diode OR connection to the base circuit.
6. Collector Voltage Rating: Collector rating is sufficient to tolerate pullup resistors returned to the + 26-volt supply.

CHANNEL AND WORD DRIVERS

1. Current capability of the Word or Channel Drivers is 400 milliamperes d-c.

2. Voltage capability is 30 volts maximum.
3. Inductive loads must be shunted with a suppression diode.

POWER SUPPLY SWITCH

1. Current capability is 800 milliamperes maximum.
2. Voltage capability is 30 volts maximum.
3. Range of Adjustment: The load will be interrupted for 0.11 milliseconds minimum to 0.3 milliseconds maximum after an adjustable delay of one to nine milliseconds.

CCO SPECIFICATION

1. Contact Rating: The rating of the CCO contacts is 100 volt amperes.
2. CCO Rate: Energization time for relay is set at 3 milliseconds. CCO rates can be as high as 100 per second.

CCI SPECIFICATION

1. Threshold Levels: A voltage across terminals 1 to 2 of the CCI buffer transformer of 2.5 volts is the maximum voltage for a logic "zero" state indication, and a voltage of 8 volts is the minimum voltage for a "one" indication.
2. Supply Voltage: CCI filtered inputs may be switched to 48 volts +20 per cent -15 per cent.
3. CCI Rate: Maximum CCI rate is determined by power supply switch settings and program times, and can be as high as 100 per second.

INTERRUPT SPECIFICATIONS

1. Filtered Interrupts: Contact is closed to 48 volts, ±10 per cent. Input rate is 15 per second.
2. Unfiltered Interrupts: Unfiltered interrupts can be switched to the +26-volt supply through a 1K minimum resistance value. These interrupts when reset to ground through a 35-ohm minimum resistor can attain an interrupt rate of 200 interrupts per second, limited, of course, by program lockout times.

ADJUSTMENTS AND WAVEFORMS

ADJUSTMENTS

The following adjustment should be made on the P50 computer only if they become necessary.

CORE PULSER ADJUSTMENT

Equipment

1. Tektronix Oscilloscope 541, 545 or equivalent.
2. Tektronix Current Probe type P6016 with passive termination.
3. Two card extender boards.

Scope Sittings

1. One micro sec/cm
2. .05 v/cm
3. Connect positive external trigger to pin L3 of any of the four half selects.

Procedure

A. Read-Write current adjust.

1. Turn off power.
2. Put computer in Read mode.
3. Pull the appropriate half select (HS) and core pulser (CP) as noted in Figure 2-26. Insert card extenders and re-insert half select (HS) card and core pulser card.
4. Turn Power on.
5. Place the current probe on the appropriate pin of the half select card as shown in Figure 2-25. Place current probe on 2 ma/mv with scope setting at 0.05 v/cm. Each cm of deflection on scope will be equal to 100 ma.
6. Cycle start button and observe waveform.
7. Adjust appropriate pot of core pulser for proper value (350 ma) see Figure 2-26 for location of adjustment potentiometer.

B. Inhibit current adjust.

1. Place selector switch in dynamic read mode. (TO PLACE SWITCH IN READ MODE DEPRESS MECHANICAL STOP AND ROTATE SWITCH TO THE DYNAMIC READ MODE).
2. Place the current probe on the appropriate inhibit line (TWISTED PAIR WIRES LOOPED ON TOP OF CORE STACK). Place the probe on one wire of the twisted pair for each bit to be checked.
3. Push start button (Caution - Do not disturb the "S" Register as core contents will be destroyed).
4. Adjust appropriate pot on the core pulser for correct value. (332 milliamps)
5. See Figure 2-26 for slot and potentiometer location.

6. To adjust currents for core stacks other than 0 stop computer and set "S" Register to the following:

STACK	SETTING
0	00000
1	10000
2	20000
4	30000

Turn power on and proceed as per step 4 above. Consult Figure 2-26 for appropriate CP card location.

7. Potentiometer location on the core pulser card is shown in Figure 2-27. A top view of the card is shown. The slot location determines the inhibit, read and write adjustment for each core stack.

HALF SELECT	PIN LOCATION
X READ	C7H10
X WRITE	C7H11
Y READ	C9H10
Y WRITE	C9H11

Figure 2-25. (Half Select and Pin Location)

STACK	SLOT		
0	D8	D7	D6
1	D11	D10	D9
2	E8	E7	E6
3	E11	E10	E9

Figure 2-26. (Core Stack and Core Pulser Locations)

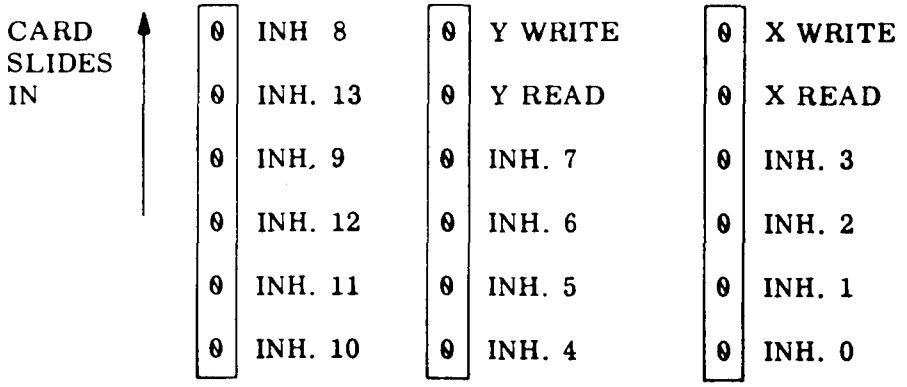


Figure 2-27. (Core Pulser Potentiometer Location for Each Core Stack) Top View

WAVEFORMS

The following pages show the waveforms for memory and interrupt.

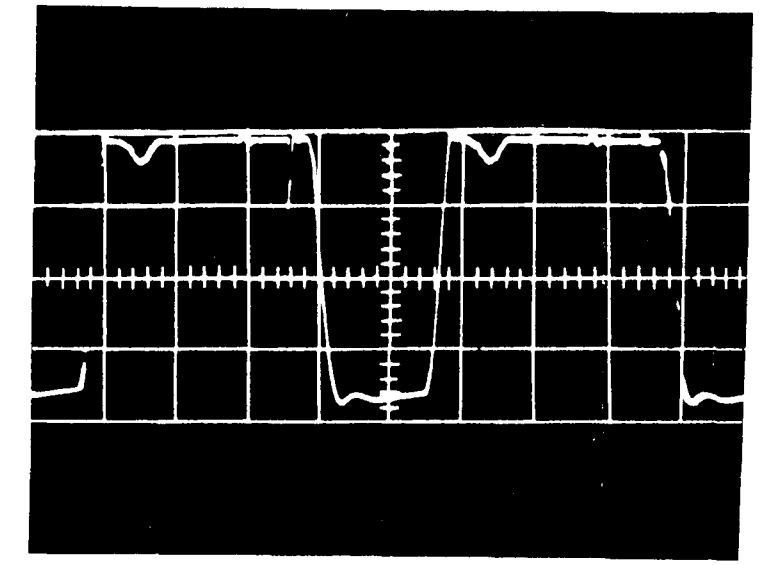
Core Memory

If it is decided to add additional 4K words to the existing system (up to 16K max.), it is a simple matter. The core stack, the diode boards (MA and MB), the inhibit paddle board (IP) the sense amplifier board (SA), and three core pulser boards (CP) are all that is required.

The only adjustment that should be needed is the setting of the core currents. Read and Write are set in single-step mode using the Read and Write positions of the mode switch. Inhibits can be set in Dynamic Read. Two card extender boards (one for the half select and one for the pulser cards) are required.

Follow the procedure given earlier in the section.

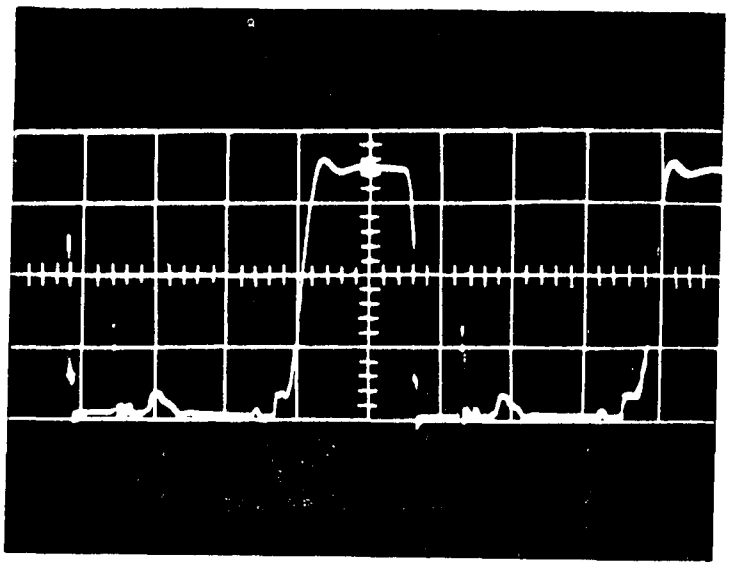
To establish that operation of the core memory is normal, the waveforms in Figures 2-28 and 2-29 may be checked. Figure 2-28 shows Read, Write, and Inhibit currents on a typical system. These currents are being viewed with the machine in the Dynamic Read mode. The Read and Write currents are being observed as they enter and leave the subcolumn half-select switch by means of a Tektronix Type P6016 current probe looping extender board wires. The Inhibit current is viewed at the Inhibit cable. Read and Write are normally adjusted to 350 milliamperes in single step. Inhibit is normally set at 332 milliamperes. Figure 2-29 shows the ideal placement of strobe with respect to the amplified response voltage. The threshold for the voltage under strobe is 0.6 volts. These waveforms are observed at extender and terminals connected to a bit card when a worst case core program is running.



X READ

100 mA/cm

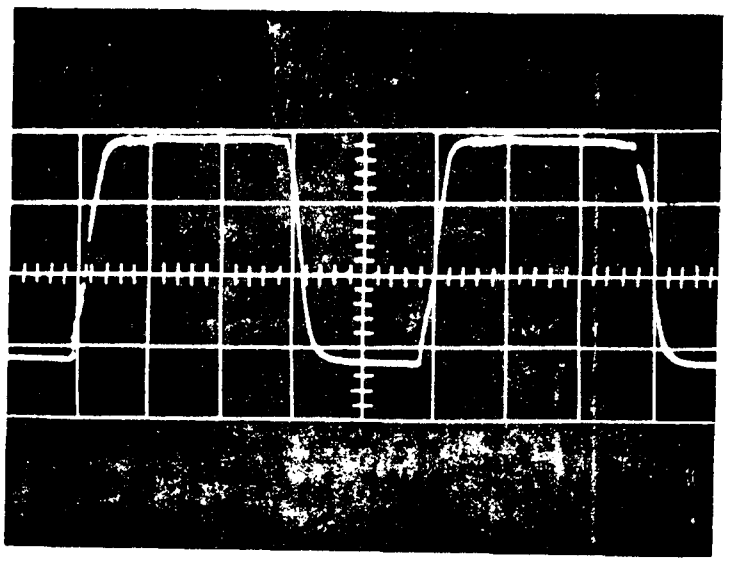
1 μS/cm



X WRITE

100 mA/cm

1 μS/cm

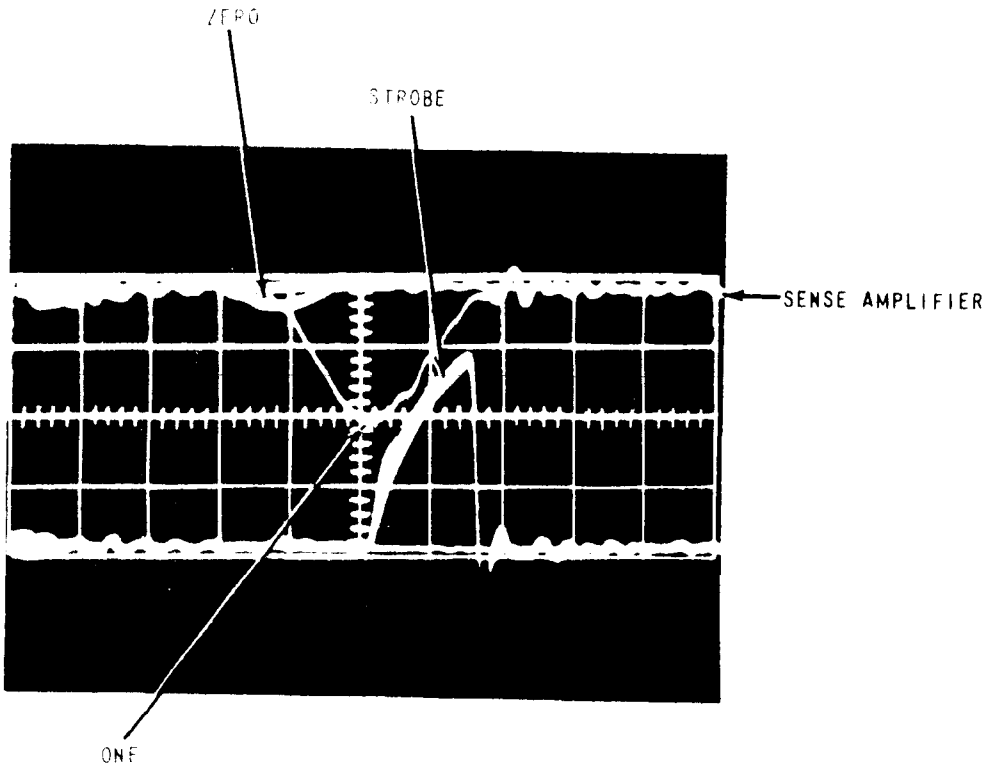


INHIBIT

100 mA/cm

1 μS/cm

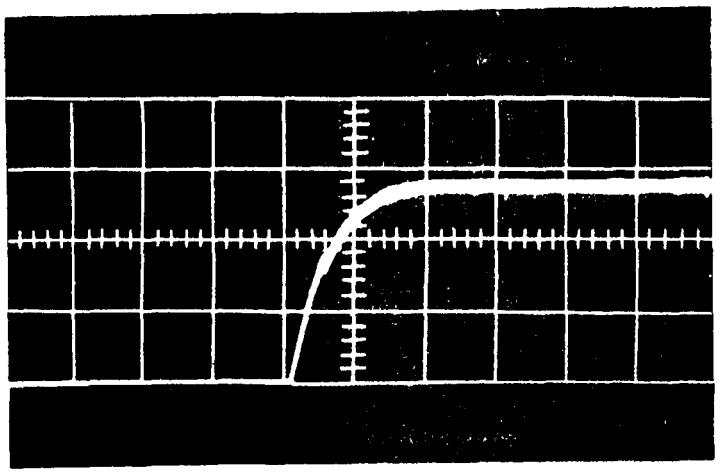
Figure 2-28. Core Memory Waveforms



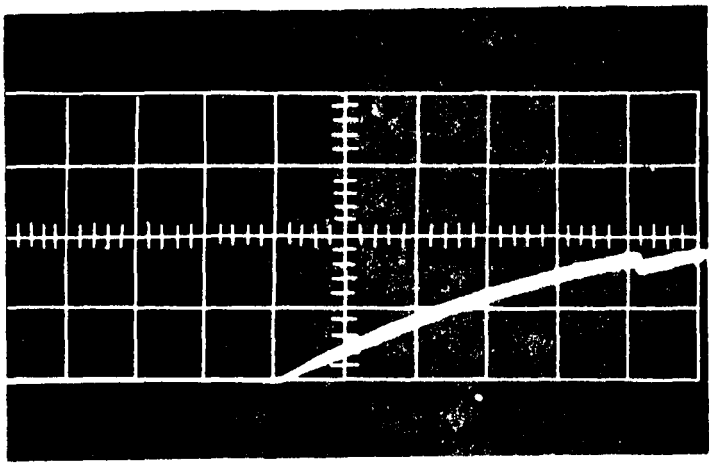
1v/cm - Sense Amp. Output
1v/cm - Strobe
0.2 μs/cm

Figure 2-29. Amplified Sense Output Showing the Position of the Strobe

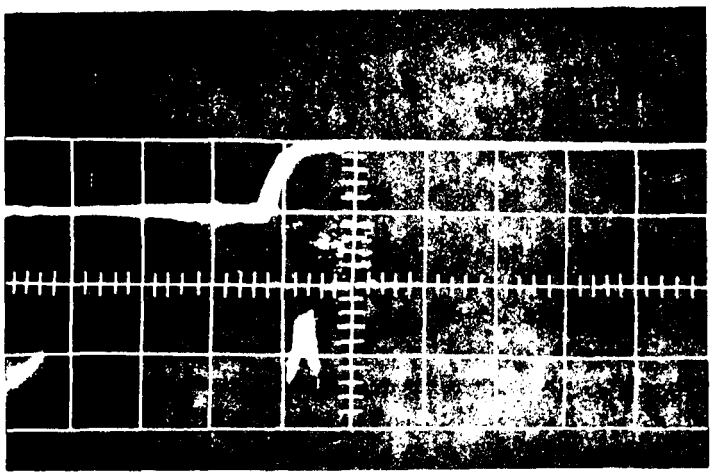
Figure 2-30 and 2-31 shows the response voltage resulting from the 400 milliampere Interrogate current. This response voltage as well as the Hit response voltage are similar in shape. A voltage greater than 1.5 volts across the 100-ohm terminating resistor is interpreted as a "one" to set the lockout flip-flop.



Unfiltered Interrupt Input
10v/cm
0.5 Ms/cm

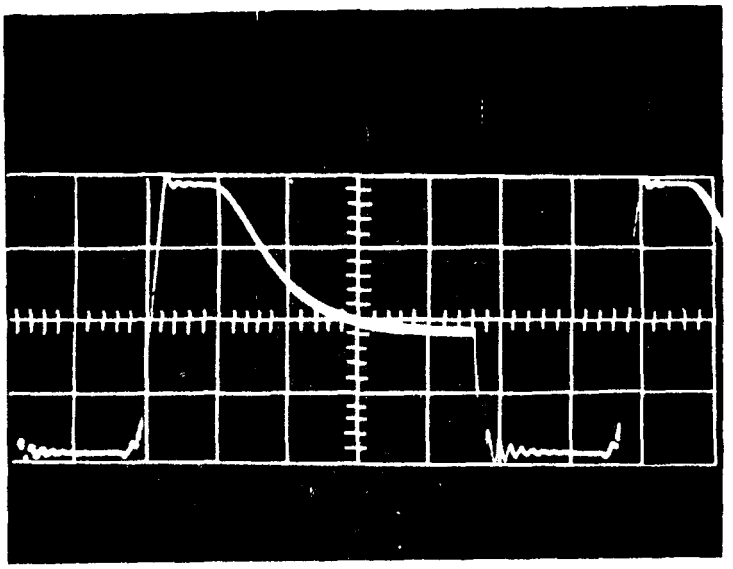


Filtered Interrupt Input
10v/cm
0.5 Ms/cm

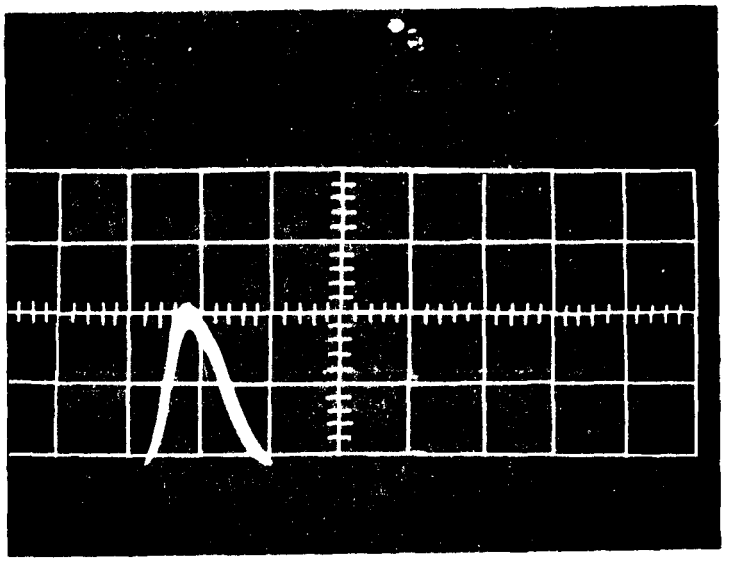


Top: Interrogate Current
400 mA/cm 0.5 μs/cm
Bottom: Sense Playback
1v/cm 0.5 μs/cm

Figure 2-30. Interrupt Waveforms



Probe Pulse
10v/cm
2μs/cm



Hit Playback
2v/cm
0.1 μs/cm

Figure 31. Interrupt Waveforms

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START-UP PROCEDURE

POWER CONNECTION

1. Measure the a-c line voltage where the computer will be connected. This must be between 103 and 128 vac, 60 cps ±1%. Record this voltage in log book.
2. Open the doors to the central processor and I/O cabinets and check to see that all cards are in the correct locations and seated properly.
3. Connect system ground; terminal E1 on a-c pushbutton panel assembly in central processor cabinet to plant ground. Ascertain that cabinet grounds for each cabinet are connected to terminal 5, TB0002.
4. Connect the incoming a-c to CB1 (hot side) and neutral side to E3 on the a-c distribution box. The incoming a-c should be 115v ±10% (or 230vac can be used if transformer primaries are changed).

Turn on the breaker and measure the d-c voltage at TB0004-10 on the power supply module. This voltage must be 27.3 volts +10%, -15%. If not in this range, the +26v transformer (T1) secondary taps must be adjusted to get this correct voltage envelope.

The "26" volt bus adjustments are made by changing taps on the power transformer winding (This is the largest transformer in the supply, and the only one with extra winding taps). Tap positions 6 through 12 are on the high side of the secondary and are to be used for adjusting the output voltage to the proper level according to the following procedure:

a. Insure that the system is complete and that all cards are in place so the "26" volt bus will be fully loaded.
b. With the system "ON" but with the central processor in a "MASTER CLEAR" condition, select a position for the secondary tap so the voltage on the bus will be 27.3vdc ±0.5 volts with 115 a-c ±10% on input terminals. Taps are at approximate 3% voltage intervals in ascending order as numbered. The nominal tap for an "average" system is tap #9 when adjusted with 115vac applied to the primary.
c. As a check, the drop in voltage on the "26" volt bus should be less than 1.0 volt with the memory cycling.

Reference 105D312 for the schematic drawing of the power supply module.

5. Measure the 6.3 vac voltage at TB0003-2 and TB0003-1. The 6.3vac allowed variation is ±10%.
6. Measure the 48vdc voltage (this is an ungrounded d-c supply) between TB0004-7 and TB0004-8. The 48v supply can be +20% -15% of 48v.
7. Record all values in the log book.
8. Check that maintenance lights on boards function properly. These can be checked by putting machine in "read" mode and setting and clearing the flip-flops manually. (Remember, the tabs on the left side of the boards are the clear side, and the tabs on the right are the set side.)
9. With lights set, depress "lamps" switch to see that lights extinguish.
10. Connect up all necessary cables to I/O section, ASR set loggers, etc. (See System Master Cable List for designation and destination.)

INSTALLATION TEST

In general the following tests should be run for installation.

Before attempting to execute these tests, first decide what means will be used to load the test tapes (ASR reader or high speed reader) so that the proper interrupt location can be used. Refer to the Interrupt Jumpering drawing supplied with the particular job for this information.

Read over the test procedures before an attempt is made to load to make sure the necessary information is available to initialize the tests.

1. Refer to writeup S3A, bootstrap loader, and load this program.
2. Refer to writeup S4A, bootstrapped binary loader, and load this program via the ASR or high speed reader. (Note: The sync. interrupt must be off. Also note that S4A can be loaded into core bay 0, 1, 2 or 3 as determined by the tape entered.)
3. Refer to writeup D9A, command execute test, load and execute this test. Suggested run time is 1/2 hour.

Note: Suggested run times differ from those in the test writeup since an installation test does not need to be as exhaustive as factory testing.

4. Refer to writeup D10A, core cross talk test; load and execute this test. Suggested run time is one complete cycle, which takes approximately 1 hour.
5. Refer to write-up D11A, worst case core pattern test; load and execute this program. Suggested run time - 1 hour.
6. Refer to write-up D12A, adder test; load and execute the program. Suggested run time - 10 minutes.
7. Refer to write-up D13A, 735 Selectric TW test; execute and load this program. Be sure that switch on side of 735 base is in the down (off) position. Suggested run time - 5 minutes.
8. Refer to write-up D15A, ASR Punch Reader Test; load and execute this program. Suggested run time - 10 minutes.
9. Refer to write-up D16A, High Speed Reader-Punch Test; load and execute this test. Suggested run time - 20 minutes.
10. Refer to write-up D17B, Analog Input Statistical Test; load and execute this program.
11. Refer to write-up D18B, Analog Input Scanner Test; load and execute this program.
12. Refer to write-up D37A, CCI test, load and execute this program.
13. Refer to write-up D38A, Interrupt, load and execute this program.
14. Refer to write-up D39A, CCØ Test, load and execute this program.

These tests are run to ascertain that the system is correct after arriving at user's site. More exhaustive tests have already been run on these computers at the Computer Systems Division Test Floor.

There are two additional tests which are available but are not normally run at this time. These are D19A, CCØ vs CCI; and D20A, CCØ vs Interrupt Test. These are tests which require the use of special test cables. These tests are essentially duplicated by tests D37A, D38A, and D39A.