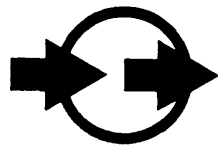


TC-130 TECHNICAL DESCRIPTION



**western peripherals**

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TC-130 TECHNICAL DESCRIPTION

WESTERN PERIPHERALS

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## SECTION I

### GENERAL DESCRIPTION

#### 1.1 INTRODUCTION

The Western Peripherals TC-130 Universal Magnetic Tape Controller provides both PE and NRZ tape formats in a single DEC System Unit. The TC-130 is compatible with the DEC PDP-11 Computer family. The four-board controller plugs into one system unit within the computer and connects with the tape drive through the rear of the computer.

#### 1.2 FUNCTIONAL DESCRIPTION

The Western Peripherals TC-130 Magnetic Tape Controller is a complete tape controller which provides tape command and status as well as writing and reading IBM-compatible, 9-track Phase Encoded (1600 bits per inch), 7-track NRF (800/556/200 bits per inch), or 9-track NRZ (800 bits per inch) magnetic tapes.

All of these functions are provided on four printed circuit boards with the ability to mix 7-track and 9-track NRZ, PE or dual density tape units in any combination up to eight (8) units.

On 7-track, 4-4-4-4 pack allows a core memory dump onto tape. A 33-word data buffer provides flexibility in assigning priorities when programming data transfer to the computer.

## 1.2 FUNCTIONAL DESCRIPTION (Continued)

Read-and-write on the fly allows automatic non-stop operation when doing consecutive read-write operations. This is accomplished automatically without special software.

Tape transport motion control, CRCC and LRCC generation, LRCC checking, inter-record gap generation and status reporting are included. All write clocks, delay times are derived from a crystal controlled oscillator. No adjustments are provided or required.

The TC-130 writes and recognizes IBM-compatible file marks. It provides for the "Edit" feature (allows a record anywhere on a previously recorded tape to be replaced with an updated record). It is compatible to entire 12.5 to 125 ips tape speed range.

The controller will interface with all industry-compatible tape drives.

The TC-130 will not operate incremental drives.

## 1.3 PHYSICAL DESCRIPTION

The Western Peripherals TC-130 Magnetic Tape Controller is constructed on 4 printed circuit boards. These boards are designed to fit into a single DEC System Unit embedded in the computer. Cable and adapter boards are provided to connect up to eight (8) tape drive units in "daisy chain" fashion. Three (3) flat ribbon cables connect from three of the four boards in the DEC module to adapters in each tape drive unit.

## 1.4 COMPUTER - TAPE TRANSPORT DATA TRANSFERS

Command and status information transfers between the tape unit and the computer are made under IOT control via addresses 772520 to 772536.

The TC-130 Tape Controller can only Read and Write data in the forward direction, but will space or move to a new position in both Forward and Reverse.

The controller may address up to eight (8) drives but can only Read, Write or Space one (1) drive at a time except for Rewind. This function requires only the initiation by the controller. That transport can then be left to rewind and the controller can service another drive.

## 1.5 SYSTEM SPECIFICATIONS

The following specifications describe the TC-130 Universal Magnetic Tape Controller.

### 1.5.1 Performance.

A. Compatible with the following mini-computers:

DEC PDP-11, All Series (TM-11)

### 1.5.2 Size.

A. Four (4) DEC Quad boards in one (1) DEC System Unit.

1.5.3 Number of Drives.

A. Eight (8) in any combination of PE, NRZ or PE/NRZ, 7- or 9-track.

1.5.4 Number of Tracks, 7 and 9.

Data Packing 200, 556, 800 NRZ or 1600 PE bits per inch, with tape organization of 8 bits, 8 bits per word in 9-track and 6 bits, 6 bits in 7-track with 4 bits, 4 bits, 4 bits, 4 bits per word in 7-track core dump mode.

1.5.5 Read and Write on the Fly.

Provides for automatic continuous operation when command sequence requires tape motion in the same direction as previous command. In this condition the Read mode will time through the IRG and the Write mode will write the IRG without stopping the tape.

1.5.6 Buffered Operation.

The unit is supplied with a 33-word standard buffer that will allow for tape operation during the time the bus is unable to service the unit. It will automatically transfer all data it has before stopping the operation. This buffer also allows for the checking of false Postambles when single dead track correction occurs in phase-encoded operation. In Read mode the 33-word buffer must be emptied before 1 ms after end-of-record detected at 25 ips or a data late error will be set. (See Figure 1-1 for other timing.)



FIGURE 1-1

Time allowed from End-of-Record to Empty Buffer on Read:

|          | <u>NRZ 9-TRACK</u> | <u>7-TRACK</u> | <u>PE</u> |
|----------|--------------------|----------------|-----------|
| 12.5 ips | 3.0 ms             | 15.0 ms        | 4.1 ms    |
| 25 ips   | 1.5 ms             | 7.5 ms         | 2.05 ms   |
| 37.5 ips | 1.0 ms             | 5.0 ms         | 1.37 ms   |
| 45 ips   | .83 ms             | 4.17 ms        | 1.14 ms   |
| 75 ips   | .5 ms              | 2.5 ms         | .68 ms    |
| 125 ips  | .3 ms              | 1.5 ms         | .41 ms    |

#### 1.5.7 Tape Speeds

The controller will handle any two (2) of the following speeds: 12.5 ips, 25, 37.5, 45, 75, and 125 ips. These speeds are selected by the setting of the speed set switches located on the controller boards. (See Figure 2-2 on Page 2-4.)

#### 1.5.8 Tape Format

All data is recorded using the IBM standard for both 7 and 9 tracks.

#### 1.5.9 Parity Check

- A. VRC Checks
- B. LRC Check
- C. CRC Writes
- D. LPC Writes (even)
- E. Even character parity writes and checks

1.5.10 Power

- A. 5.5 amps of  $\pm$  5 volts supplied from the CPU Power Supply.
- B. 75 ma of -15 volts supplied by CPU Power Supply (Pin A10).

1.5.11 Weight

Four (4) pounds.

1.5.12 Environment

- A. Operational at 0° to 55°C
- B. Storage 10°C to 70°C
- C. Humidity 10 to 90% (non-condensing)

SECTION II  
INSTALLATION PROCEDURE

2.1 SYSTEM UNIT REMOVAL

Remove any DEC blocks in module position in which TC-130 Controller is to be installed.

2.2 SPEED SELECTION

Set up appropriate tape speed(s) according to Table 2-2, page 2-4. Check that VCO filter is within correct range for tape speed(s) if phase encoded. (See Table 2-5, page 2-14.)

2.3 INTERRUPT LEVEL

Set up desired interrupt bus level according to page 2-3.

2.4 SYSTEM UNIT INSTALLATION

Fasten TC-130 System Unit in desired location.

2.5 BOARD PLACEMENT

Insert the controller boards in the order shown on Figure 2-1, page 2-3.

2.6 COMPUTER CONNECTIONS

Install power connector in "A" connector of Slot 3. Install Unibus Jumper Block(s) M920 and/or Unibus Terminator if last device on bus.

TABLE 2-1

INTERRUPT BUS LEVEL ASSIGNMENT  
BOARD #2

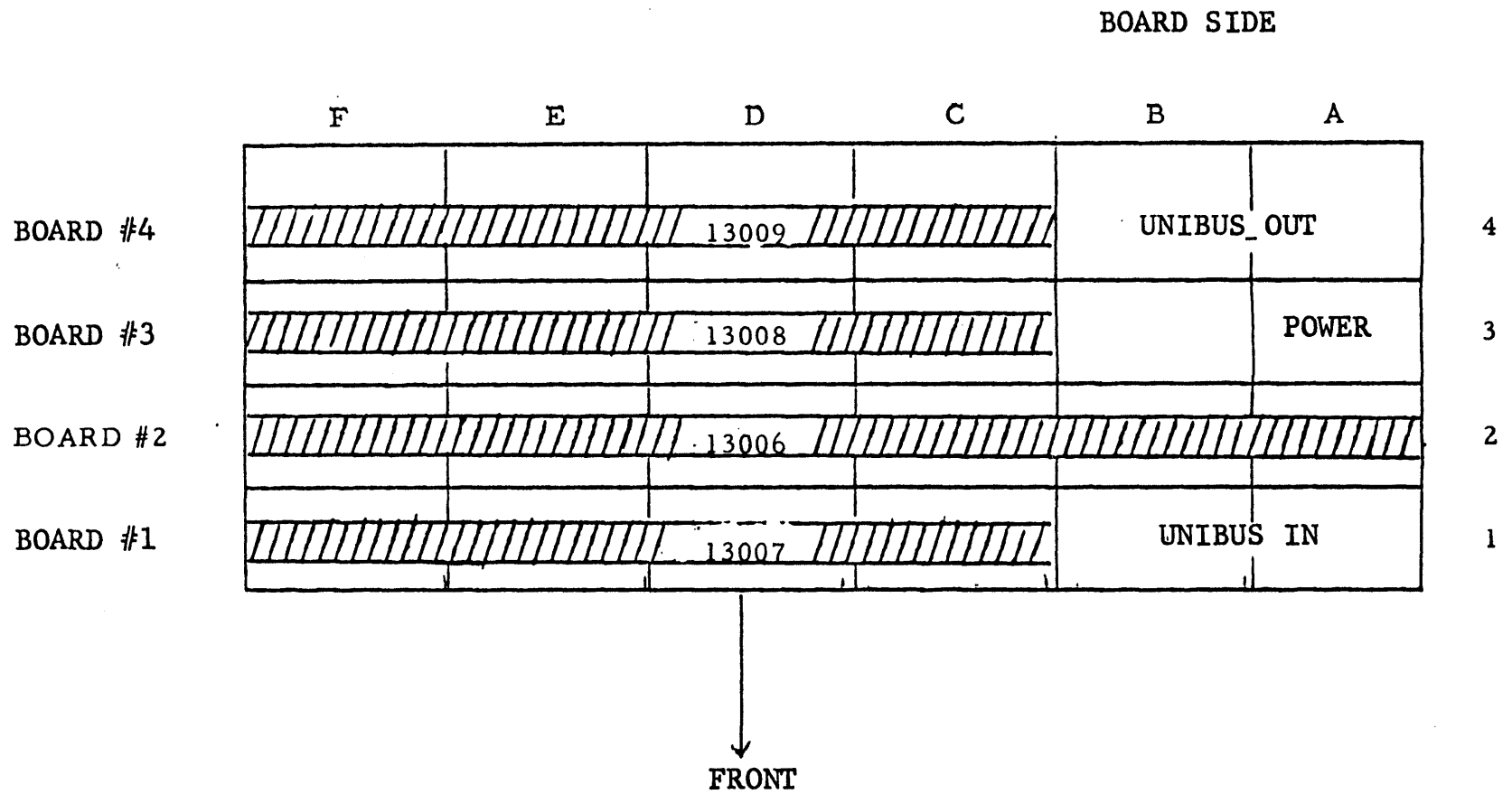
| INTERRUPT<br>BUS LEVEL | 4   | 5   | 6   | 7   |
|------------------------|-----|-----|-----|-----|
| SWITCH A18             |     |     |     |     |
| 1                      | OFF | OFF | OFF | ON  |
| 2                      | OFF | OFF | ON  | OFF |
| 3                      | OFF | ON  | OFF | OFF |
| 4                      | ON  | OFF | OFF | OFF |
| 5                      | OFF | OFF | OFF | ON  |
| 6                      | OFF | OFF | ON  | OFF |
| 7                      | OFF | ON  | OFF | OFF |
| 8                      | ON  | OFF | OFF | OFF |
| SWITCH B18             |     |     |     |     |
| 1                      | ON  | ON  | ON  | OFF |
| 2                      | ON  | ON  | OFF | ON  |
| 3                      | ON  | OFF | ON  | ON  |
| 4                      | OFF | ON  | ON  | ON  |
| 5                      | OFF | OFF | OFF | ON  |
| 6                      | OFF | OFF | ON  | OFF |
| 7                      | OFF | ON  | OFF | OFF |
| 8                      | ON  | OFF | OFF | OFF |

TABLE 2-2

SPEED SWITCH SETTINGS

|                       |      | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-----------------------|------|---|---|---|---|---|---|---|---|
| S<br>P<br>E<br>E<br>D | 12.5 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
|                       | 25   | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
|                       | 37.5 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
|                       | 45   | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
|                       | 75   | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
|                       | 125  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

(1 = + side of switch down)  
 (0 = open)



2-4

FIGURE 2-1

## SECTION III

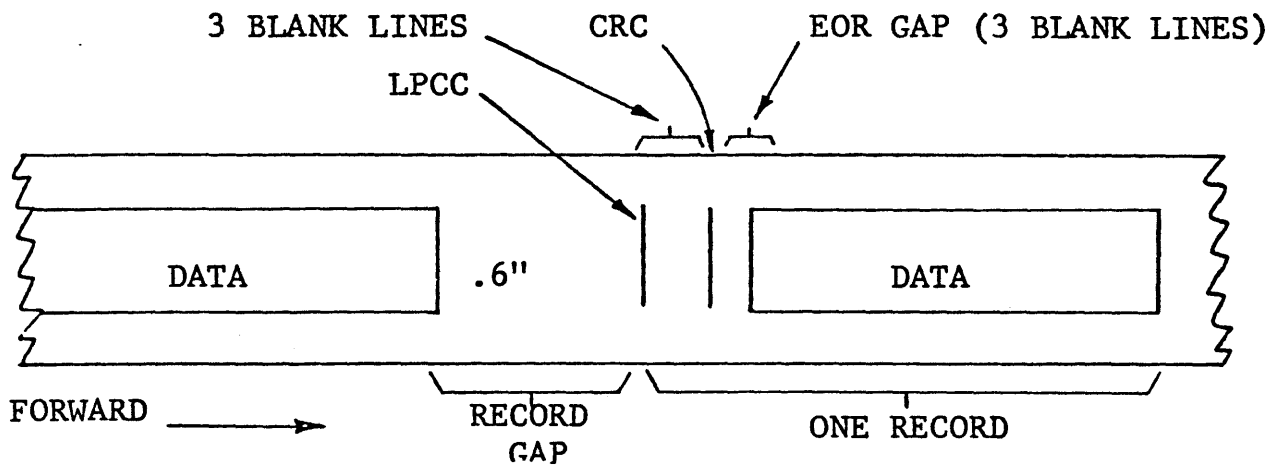
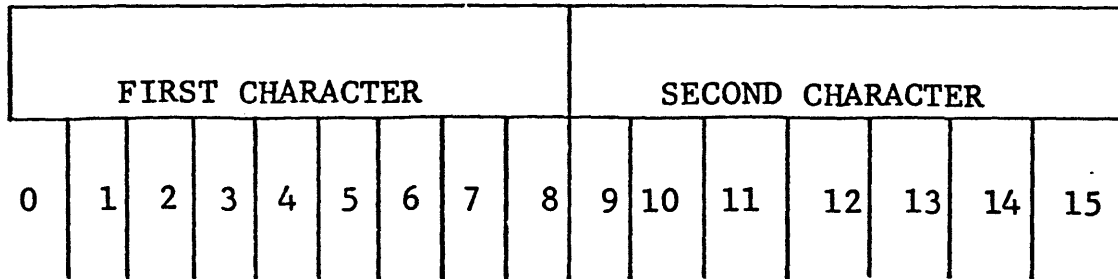
### TAPE FORMAT

#### 3.1 GENERAL

The Western Peripherals Tape Controller writes nine or seven bits of information, one bit in each track, laterally, or across the tape. A switch on the tape transport selects the density of the data written. Provisions are made in the logic to permit the computer to select tape density. A data record consists of data and error-checking characters. Every data character consists of the data byte plus a parity bit that is generated by the Controller to conform with odd or even parity as specified by the program. Every character is in either a data record or a file mark. A block of words from memory to the Controller is represented by the data bytes in a record taken together. The Controller separates adjacent records by automatically erasing a segment of tape to form an interrecord gap between them. The Controller always stops the magnetic tape in an interrecord gap.

The minimum record length is two words (or four data characters). Maximum length is limited only by the capacity of the Byte Counter to 32,768 words. In writing, the Controller divides the words into two data bytes. In reading, the bytes are reassembled.

### 3.2 NINE-TRACK FORMAT



In nine-track format, each word is written as two eight-bit characters. After the last line of a record is written, the Controller writes three (3) blank lines, a Cyclic Redundancy Character\* (CRC), three (3) blank lines and a Longitudinal Parity Check Character (LPCC).

\* As described in Paragraph 6 of USAS X3.22-1967, USA Standard Recorded Magnetic Tape for Information Interchange.



### 3.2 NINE-TRACK FORMAT (Continued)

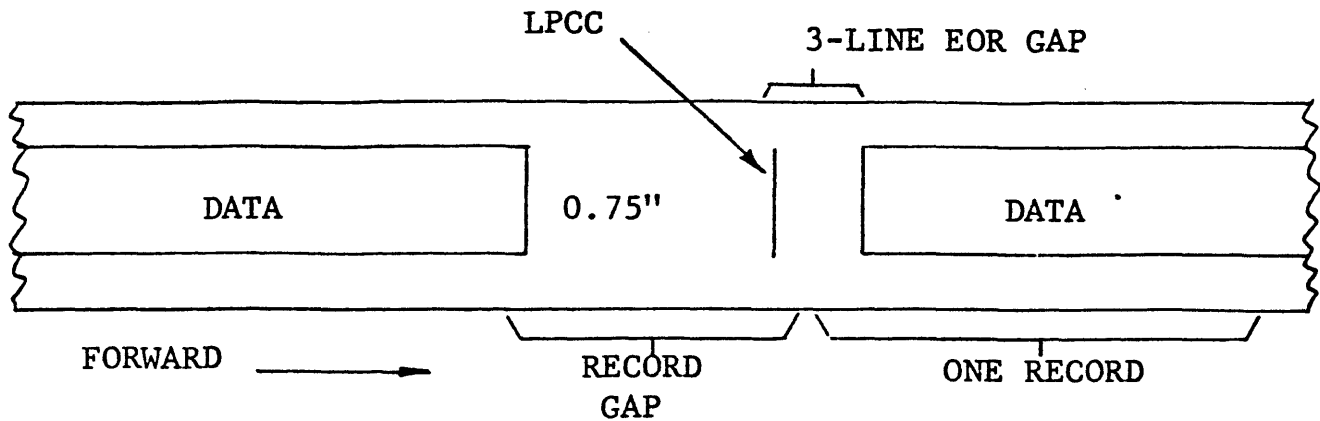
The three blank spaces following the Data is the End-of-Record Gap (ERG), used to detect the end of the record.

LPCC (always odd) produces an even longitudinal parity in each of the tracks along the length of the tape. Minimum record gap is 0.5 inch. To be compatible with IBM format, a record must be of high density and odd parity. Reading or writing, the Controller checks to ascertain that the lateral parity of every data line agrees with that specified by the program and that every track has even longitudinal parity.

### 3.3 SEVEN-TRACK FORMAT

In seven-track format, the Controller writes each word in two characters: Bits 2-7 and Bits 10-15. It ignores Bits 0, 1, 8, and 9.

| X |   | FIRST CHARACTER |   |   |   |   |   | X |   | SECOND CHARACTER |    |    |    |    |    |
|---|---|-----------------|---|---|---|---|---|---|---|------------------|----|----|----|----|----|
| 0 | 1 | 2               | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10               | 11 | 12 | 13 | 14 | 15 |
|   |   |                 |   |   |   |   |   |   |   |                  |    |    |    |    |    |



After writing the last line, the Controller writes an LPCC and an EOR gap. Minimum record gap is 0.75 inch. As shown above, the controller assembles pairs of bytes into words. Zeros appear in the unused bits.

### 3.4 7 TRACK CORE DUMP MODE (4444 FORMAT)

If Bits 13 and 14 of command register are set when reading or writing a 7 track tape, all bits of the computer word are utilized and the two most significant bits of the tape characters are not utilized.

Packing configuration is shown below:

| Computer Word Assignments | 1 ST. CHARACTER   |   |   |   | 2 ND. CHARACTER |   |   |   | 3 RD. CHARACTER |   |   |   | 4 TH. CHARACTER |   |   |   |
|---------------------------|-------------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|
|                           | Track Assignments | 8 | 4 | 2 | 1               | 8 | 4 | 2 | 1               | 8 | 4 | 2 | 1               | 8 | 4 | 2 |

In order to read record completely in core dump mode, record length must be a multiple of four (4) characters in length.

### 3.5 MISSING CHARACTERS

The Controller checks for missing characters when reading. Two or more contiguous missing characters will be interpreted as an EOR gap and the command will terminate with the Bad Tape flag set.

### 3.6 END-OF-FILE MARK

The program can group sets of data records into files. The end of a file is indicated by a File Mark. The NRZ File Mark is a special record containing one special data character and its LPCC. The PE File Mark is a combination of active and dead tracks. A Space Command automatically terminates when a File Mark is detected.

### 3.7 TAPE-END MARKERS

The ends of all tapes contain reflective strips that are detected by photo cells in the transport. The Load Point marker is located at least ten feet in from the beginning of the tape and constitutes the logical beginning of tape (BOT). Reverse commands stop automatically at this marker. At least three inches of tape intervene between BOT and the first record.

EOT, or end-of-tape reflective strip, is located at least 14 feet from the end of the tape. The program should not record more than a few feet beyond EOT, leaving at least ten feet of the tape for trailer. A status bit indicates when the tape is beyond EOT, but this condition only stops the tape automatically when it is spacing forward.

### 3.8 EFFECTIVE TRANSFER RATE

During the actual processing of the actual data part of a record, the data transfer rate is fixed. However, in a long tape the effective, or average, transfer rate depends upon record length. Record length determines the percentage of tape taken up by the gaps. At the highest density (1600 bpi) each record gap occupies the space of 480 words. The effective transfer rate is therefore determined by record length as well as tape speed and density.

## SECTION IV

### INSTRUCTIONS

#### 4.1 PERIPHERAL DEVICE CONTROL

Registers in peripheral devices are assigned addresses similar to memory: thus, all PDP-11 instructions that address memory locations can become I/O instructions. Data registers in devices can take advantage of all the arithmetic power of the processor. The PDP-11 controls devices differently than most computer systems. Control functions are assigned to addressable registers, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper-tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Status conditions are also handled by the assignment of bits within this register, and the status can be checked by program instructions. There is no limit to the number of registers that a device may have, providing an unlimited flexibility in the design and control of peripheral equipment.

#### 4.2 DATA TRANSFER OPERATIONS

A 33-word buffer register provides buffering of data between tape and tape channel. Therefore, the memory has almost 34 character-times

in which to respond to requests by the Controller. All Data Transfer operations are conducted in the word mode except for add bytes at the beginning or end of a block.

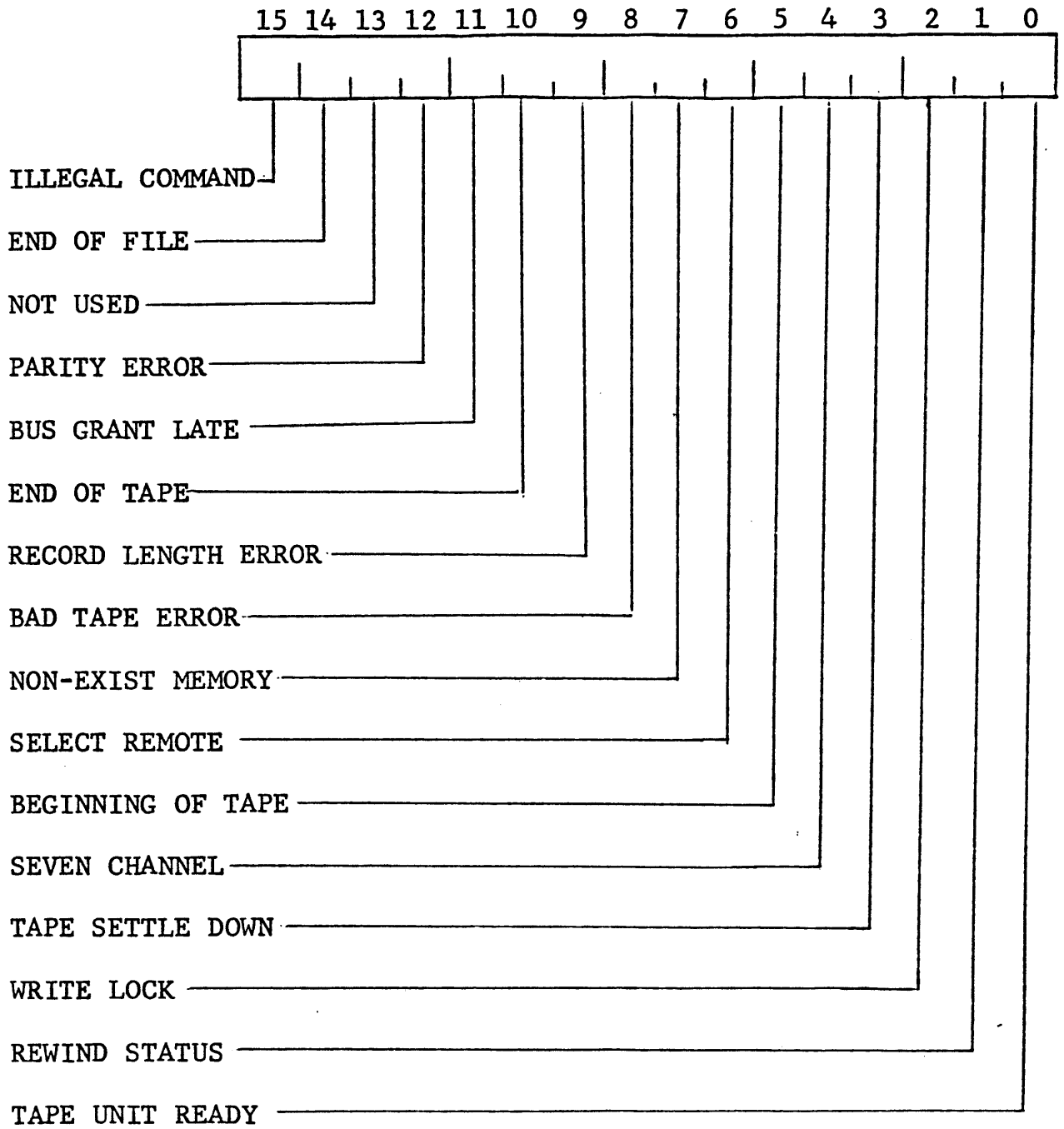
#### 4.3 TO RUN THE TAPE

To run the tape, the program must select a tape transport and a command. Most operations also require specification of parity density, an initial address to the 16-bit address counter for NFR operations, and the negative of a byte count in two's-complement form.

#### 4.4 I/O INSTRUCTIONS

All command and status instructions are used by manipulating or examining the contents of the six device register locations. Indications of operation complete can be through examination of the status and command registers, or by enabling interrupts.

4.4.1 Status Register (MTS) 772520



4.4.1 Status Register (MTS) 772520 (continued)

BIT NAME

15 Illegal Command

Set by any of the following illegal commands:

1. Any DATO or DATOB to the Command Register MTC during the tape operation period
2. A Write, write EOF, or write with extended IRG operation when the FILE PROTECT bit is a 1
3. A command to a tape unit whose SELECT REMOTE bit is a 0
4. The SELECT REMOTE (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition, the CU READY bit remains set.

14 END OF FILE (EOF)

Set when an EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the FILE MARK signal upon EOF detection.

12 Parity Error (PAE)

The OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected.

A parity error does not affect the transfer of data; that is, in a write operation, the entire record is transferred to tape and in a read operation, the entire record is written into core memory.



4.4.1 Status Register (MTS) 772520 (continued)

BIT NAME

12 (Continued)

For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF, and write with extended IRG operations. The entire record is checked including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of 1's is detected on any track in the record. A lateral parity error occurs when an even number of 1's is detected on any character when PEVN is a 0, or an odd number of 1's is detected on any character when PEVN is a 1.

11 Bus Grant Late (BGL)

Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.

10 End of Tape (EOT)

Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

9 Record Length Error (RLE)

Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop.

However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.

4.4.1 Status Register (MTS) 772520 (continued)

BIT NAME

8 Bad Tape Error (BTE)

Sets when a character is detected (RDS pulse) during the gap shutdown or settling down period for all operations (except rewind). When BTE is detected the ERR bit is set immediately, and if INT ENB is set, an interrupt sequence is started.

7 Non-Existent Memory (NXM)

Set during NPR operations, when the control unit is bus master, and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 microseconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

6 Select Remote (SELR)

Cleared when the tape unit addressed does not exist, is off line, or has its power turned off.

5 Beginning of Tape (BOT)

Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

4 Seven Channel (7 CH)

Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.

3 Tape Settle Down (SDWN)

Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

4.4.1 Status Register (MTS) 772520 (Continued)

BIT NAME

2 Write Lock (WRL)

Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.

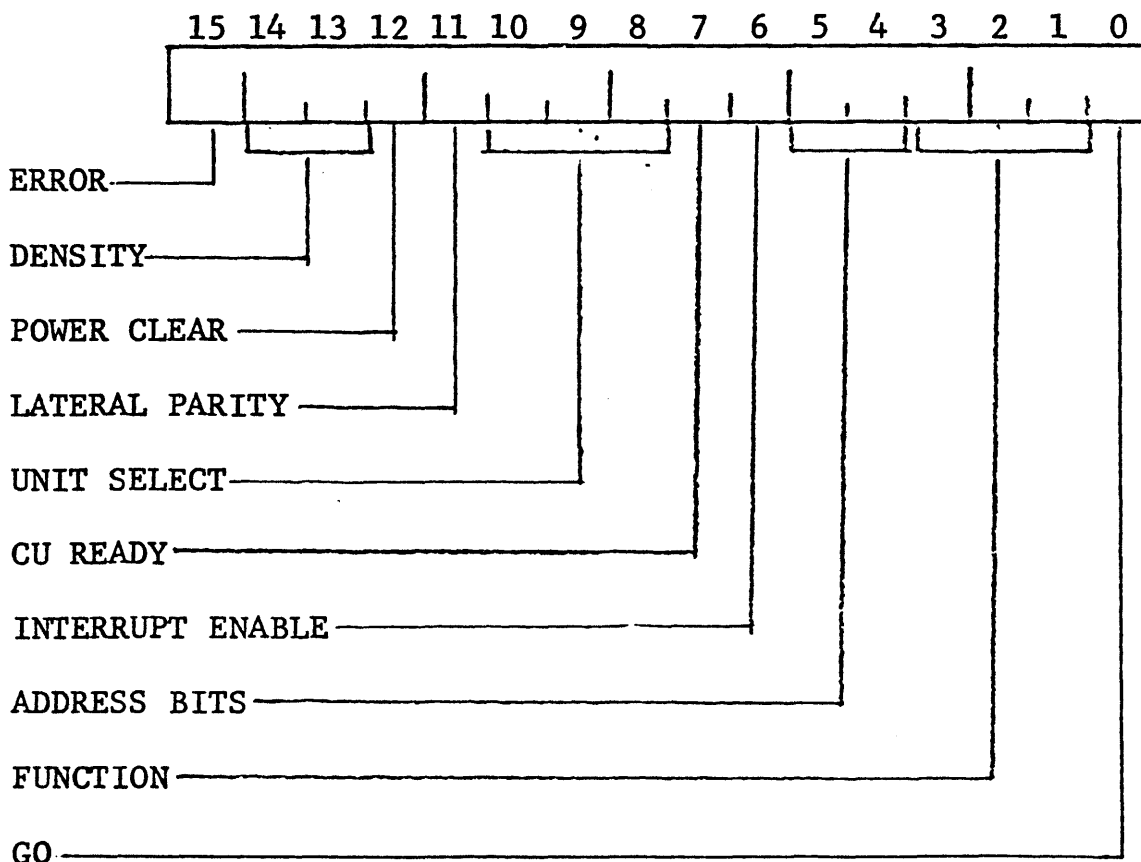
1 Rewind Status (RWS)

Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction.)

0 Tape Unit Ready (TUR)

Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

4.4.2 Command Register (MTC) 772522



#### 4.4.2 Command Register (MTC) 772522 (Continued)

BIT NAME

15 Error (ERR)

Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.

14-13 Density (DEN 8, DEN 5)

| BIT 14 | BIT 13 |                    |
|--------|--------|--------------------|
| 0      | 0      | 200 bpi 7 channel  |
| 0      | 1      | 556 bpi 7 channel  |
| 1      | 0      | 800 bpi 7 channel  |
| 1      | 1      | 800 bpi 9 channel  |
| 0      | 1      | 1600 bpi 9 channel |

12 Power Clear (PCLR)

Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.

11 Lateral Parity (PEVN)

Set for even parity. Cleared for odd parity. A search for parity error is made in all tape moving operations except space forward, space reverse, and rewind.

10-8 Unit Select

Specifies one of the eight possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.

7 CR Ready (CUR)

Cleared at start of a tape operation and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.

6 Interrupt Enable (INT ENB)

When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that

4.4.2 Command Register (MTC) 772522 (Continued)

BIT NAME

6 (Continued)

was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit (i. e. CU READY or ERROR = 1.

5-4 Address Bits

Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

3-1 Function Bits

Selects 1 of 8 functions (programmable commands).

| Bit 3 | Bit 2 | Bit 1 |                                     |
|-------|-------|-------|-------------------------------------|
| 0     | 0     | 0     | Off line                            |
| 0     | 0     | 1     | Read                                |
| 0     | 1     | 0     | Write                               |
| 0     | 1     | 1     | Write EOF                           |
| 1     | 0     | 0     | Space Forward                       |
| 1     | 0     | 1     | Space Reverse                       |
| 1     | 1     | 0     | Write with Extended Interrecord Gap |
| 1     | 1     | 1     | Rewind                              |

Write (See Figure 4-2). The program must specify parity, a (negative) byte count, and an initial address. If Write Lock is 1, go sets illegal command, and the Controller does not go into operation. Otherwise, the Controller makes an immediate data request for the first word (or byte), and it writes the words it receives via the data channel from the locations specified by the address counter until either the word counter overflows or BGL sets, at which time the Controller terminates the record.

Write End of File (See Figure 4-3). If Write Lock is 1, Start sets illegal, and the Controller does not go into operation. Otherwise, the Controller writes a file mark, and terminates.

4.4.2 Command Register (MTC) 772522 (Continued)

BIT NAME

3-1 Function Bits (Continued)

Read (See Figure 4-4). The program must specify parity, a (negative) byte count, and an initial address. The Controller reads a single record from tape, and sends the data via NPR operations to the locations specified by the address counter until it encounters the EOR gap or the word counter overflows, whichever occurs first. Giving a large word count (e. g. giving zero) ensures that the entire record will be read even if its length is unknown. The setting of BGL during the record indicates that information has been lost, but data transfers continue until overflow or the record ends. After completing the record, the Controller terminates the operation.

If the record read is a file mark, its single "data" character is sent to memory via the data channel. The length of a record of unknown size can be determined after it is read by comparing the byte counter at the end of the operation to the initial setting (provided, of course, that the byte count was large enough).

Space Forward (See Figure 4-5). The program should give a (negative) byte count equal to the number of records to be spaced. The Controller spaces forward over the given number of records unless it encounters a file mark or the end of tape, in which case it stops at the mark or at the end of the record in which the EOT marker is encountered. To space a file, the program can simply give a zero byte count.

Space Reverse (See Figure 4-6). The program should give a (negative) byte count equal to the number of records to be spaced. If Load Point is 1, Start sets Illegal, and the Controller does not go into operation. Otherwise, the Controller spaces reverse over the given number of records, but it stops the tape automatically upon encountering a file mark or the Load Point. To space a file, the program can simply give a zero word count.

Rewind (See Figure 4-7). Start does not affect the Controller, but simply initiates the rewind in the addressed transport and the Controller is free for further use by the program. The addressed transport rewinds the tape at high speed onto the supply reel and stops at Load Point.

4.4.2 Command Register (MTC) 772522 (Continued)

BIT NAME

3-1 Function Bits (Continued)

Write With Extended Interrecord Gap. The program must specify the same parameters as in Write. The operation is conducted in the same manner except a 2-1/2" length of tape is erased before data is written.

4.4.3 Byte Record Counter (MTBRC) 772524

The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

#### 4.4.3 Byte Record Counter (MTBRC) 772524 (Continued)

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN, but before the entire record has been traversed. Thus, both SWDN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

#### 4.4.4 Current Memory Address Register (MTCMA) 772526

The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfer in read, write and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 1, immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 1 of the last character in the record. In the error conditions Bus Grant



#### 4.4.4 Current Memory Address Register (MTCMA) 772526 (Continued)

Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPR's to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

#### 4.4.5 Data Buffer (MTD) 772530

The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In an NPR operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape. The polarity of the parity bit is determined by the PEVN bit in the MTC.

#### 4.4.5 Current Memory Address Register (MTCMA) 772526 (Continued)

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a zero. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is a 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is a 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 through 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

#### 4.4.6 TU10 Read Lines (MTRD) 772532

The memory locations allocated for the TU10 read lines are:

Bits 0 - 7 for the channels 7 - 0 respectively.

Bit 8 for the parity bit.

Bit 9 Identity status (PE).

Bit 10 IBM Pack mode.

Bit 11 Correctable parity error.

Bit 9 also used for edit mode instruction.

#### 4.4.6 TU10 Read Lines (MTRD) 772532 (Continued)

Bit 12 for the gap shutdown

Bit 13 for the BTE error generation

Bit 14 for the CRC, LPC character selector.

Bit 15 for the timer

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 13 is a pulse generated by the processor. Bit 14 is set and cleared by INIT. Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

#### Timer

TIMER is a 10 KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.